Petra
UMA Schematics Document
Ivy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

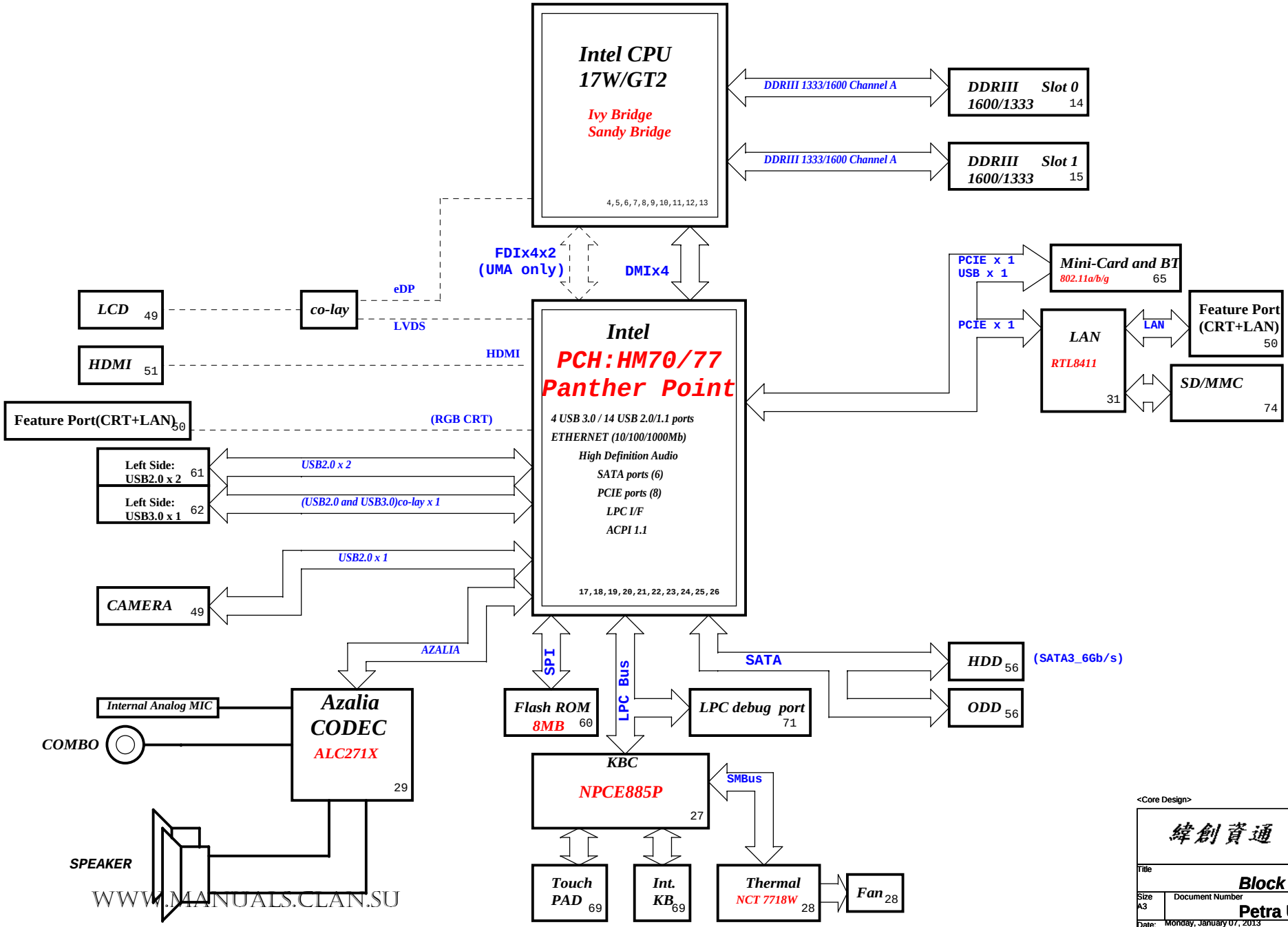
ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
Size: A3	Document Number: Petra Uma	Rev: -1
Date: Wednesday, February 22, 2012	Sheet 1 of 103	

Project code : 91.4VM01.001
PCB P/N : 48.4VM02.001
PCB No. : 11324
Revision : -1



CHARGER BQ24727 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8223MGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

CPU DC/DC ISL95836HRTZ 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC ISL95836HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC TPS51218DSCR 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

LDO RT9025-25ZSP 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

LDO G978 48	
INPUTS	OUTPUTS
1D05V_VTT	0D85V_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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Title: Block Diagram

Size	Document Number	Rev
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Date: Monday, January 07, 2013 Sheet 2 of 103

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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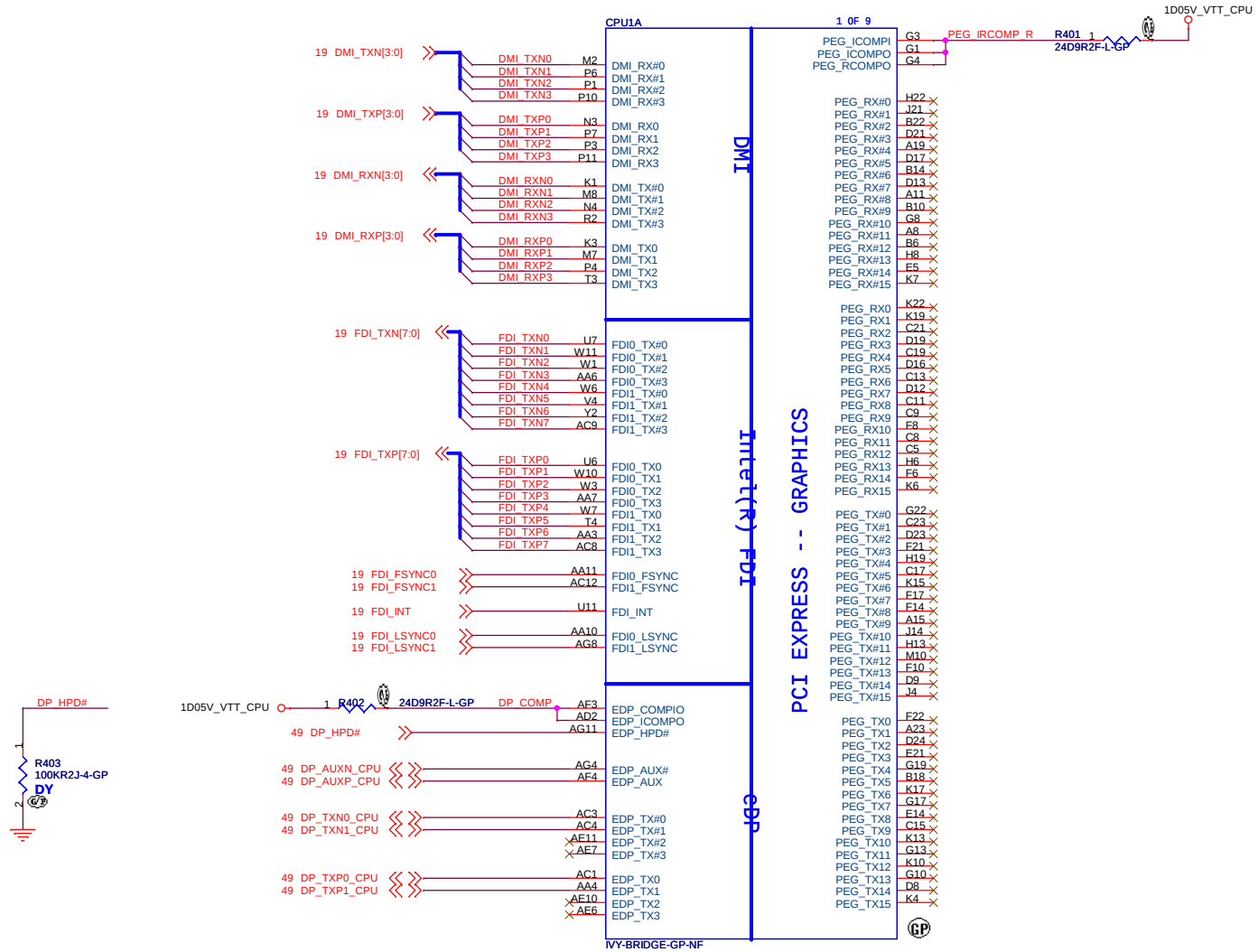
Title: Table of Content

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Wednesday, February 22, 2012 | Sheet 3 of 103

SSID = CPU



<Core Design>

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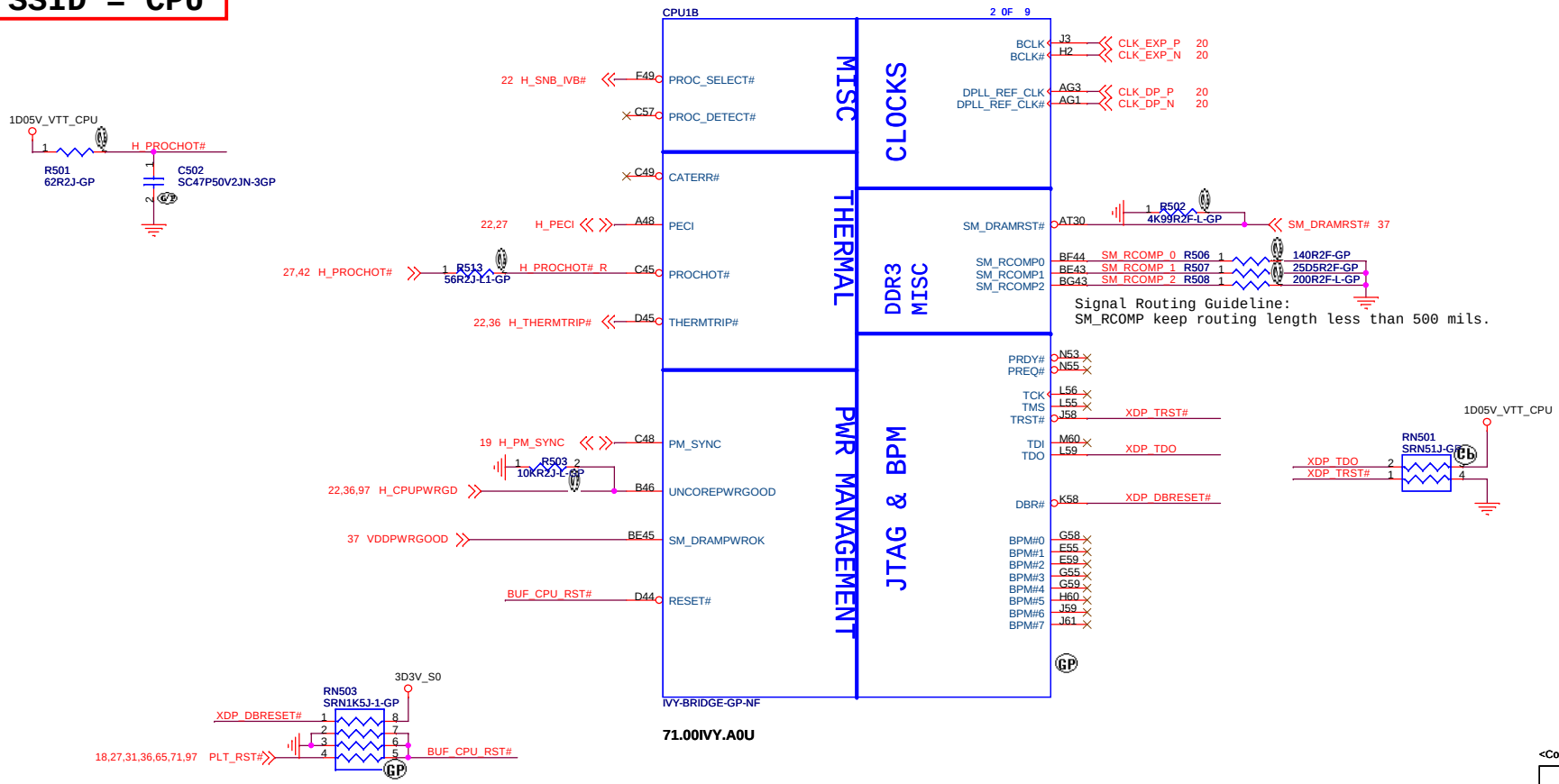
Title: ***CPU (PCIE/DMI/FDI)***

Size	Document Number	Rev
A3	Petra Uma	-1

Date: Tuesday, July 10, 2012 Sheet 4 of 103

SSID = CPU



<Core Design>

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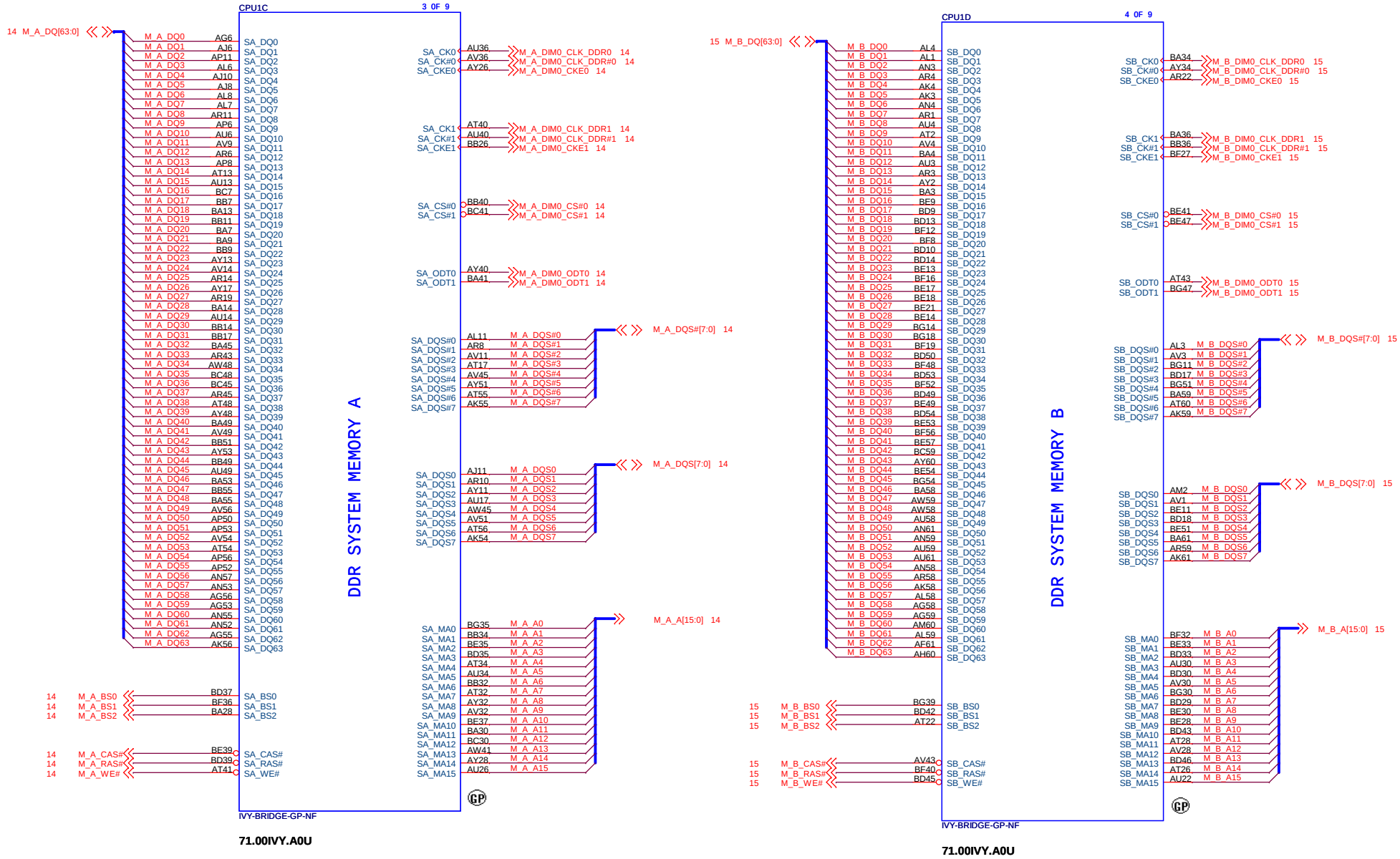
Title: CPU (THERMAL/CLOCK/PM)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 5 of 103

SSID = CPU



<Core Design>

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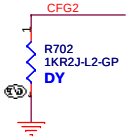
Title: CPU (DDR)

Size: A3 | Document Number: Petra Uma | Rev: -1

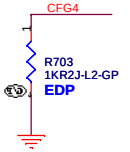
Date: Tuesday, July 10, 2012 | Sheet 6 of 103

SSID = CPU

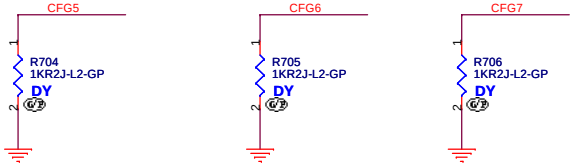
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



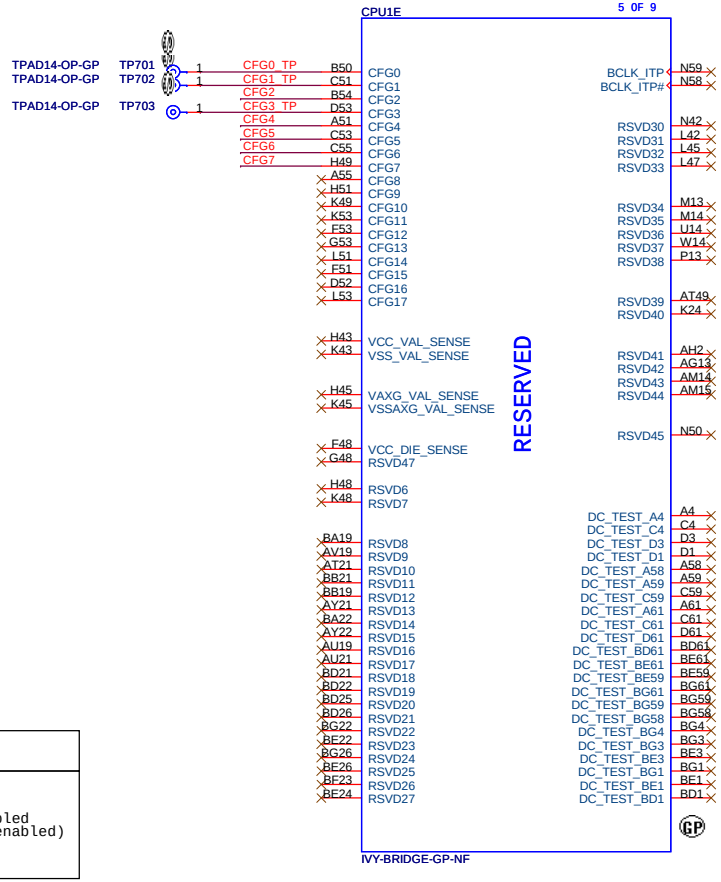
Enabl EDP function	
CFG4	1:Disable 0:Enable



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



71.00IVY.A0U

<Core Design>

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Title: **CPU (RESERVED)**

Size	Document Number	Rev
A3	Petra Uma	-1

Date: Wednesday, February 29, 2012 Sheet 7 of 103

SSID = CPU

POWER

ULV:17W
Iccmax:33A
ICC_TDC:25A

Iccmax:8.5A
ICC_TDC:8.5A

CPU1F

6 OF 9

CORE SUPPLY

PEG IO AND DDR IO

QUIET RAILS

SVID

SENSE LINES

IVY-BRIDGE-GP-NF

71.00IVY.A0U

Place near processor

Place near processor

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 8 of 103

SSID = CPU

POWER

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

VCC_GFXCORE

Iccmax:18A(GT1)
ICC_TDC:12A(GT1)

CPU1G — 7 OF 9

GRAPHICS: VAXG1, VAXG2, VAXG3, VAXG4, VAXG5, VAXG6, VAXG7, VAXG8, VAXG9, VAXG10, VAXG11, VAXG12, VAXG13, VAXG14, VAXG15, VAXG16, VAXG17, VAXG18, VAXG19, VAXG20, VAXG21, VAXG22, VAXG23, VAXG24, VAXG25, VAXG26, VAXG27, VAXG28, VAXG29, VAXG30, VAXG31, VAXG32, VAXG33, VAXG34, VAXG35, VAXG36, VAXG37, VAXG38, VAXG39, VAXG40, VAXG41, VAXG42, VAXG43, VAXG44, VAXG45, VAXG46, VAXG47, VAXG48, VAXG49, VAXG50, VAXG51, VAXG52, VAXG53, VAXG54, VAXG55, VAXG56

C902 SC10U6D3V5KX-1GP
C903 SC10U6D3V5KX-1GP
C904 SC10U6D3V5KX-1GP DY
C905 SC10U6D3V5KX-1GP
C908 SC10U6D3V5KX-1GP
C919 SC10U6D3V5KX-1GP
C920 SC10U6D3V5KX-1GP
C921 SC10U6D3V5KX-1GP DY

C907 SC1U6D3V2KX-1-GP
C909 SC1U6D3V2KX-1-GP
C914 SC1U6D3V2KX-1-GP
C916 SC1U6D3V2KX-1-GP

VREF: SM_VREF AY43 → +V_SM_VREF_CNT 37
SA_DIMM_VREFDQ BE7 ← M_VREF_DQ_DIMM0_C → M_VREF_DQ_DIMM0_C 37
SB_DIMM_VREFDQ BG7 ← M_VREF_DQ_DIMM1_C → M_VREF_DQ_DIMM1_C 37

BE7 and BG7 is NC ball in HR

RN902 SRN1KJ-7-GP DY

DDR3 - 1.5V RAILS: VDDQ1 AJ28, VDDQ2 AJ33, VDDQ3 AJ36, VDDQ4 AJ40, VDDQ5 AL30, VDDQ6 AL34, VDDQ7 AL38, VDDQ8 AL42, VDDQ9 AM33, VDDQ10 AM36, VDDQ11 AM40, VDDQ12 AN30, VDDQ13 AN34, VDDQ14 AN38, VDDQ15 AR26, VDDQ16 AR28, VDDQ17 AR30, VDDQ18 AR32, VDDQ19 AR34, VDDQ20 AR36, VDDQ21 AR40, VDDQ22 AV41, VDDQ23 AW26, VDDQ24 BA40, VDDQ25 BB28, VDDQ26 BG33

Iccmax:5A

1D5V_S0

C910 SC10U6D3V5KX-1GP
C911 SC10U6D3V5KX-1GP
C912 SC10U6D3V5KX-1GP DY
C913 SC10U6D3V5KX-1GP
C924 SC1U6D3V2KX-1-GP DY
C925 SC1U6D3V2KX-1-GP
C918 SC1U6D3V2KX-1-GP
C917 SC1U6D3V2KX-1-GP
C926 SC1U6D3V2KX-1-GP DY

PROCESSOR DDR 1.5V QUIET RAIL (BGA only)
+V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board

QUIET RAILS: VCCDQ1 AM28, VCCDQ2 AN26 ← +1.5S_VCCD_Q

1D5V_S0
R909 0R2J-1-GP
C923 SC1U6D3V2KX-L-1-GP

VCC_GFXCORE
R906 100R2F-L1-GP-U
R907 100R2F-L1-GP-U
R906,R907 close to CPU

VCC_AXG_SENSE
VSS_AXG_SENSE

SENSE LINES: 42 VCC_AXG_SENSE → F45 VAXG_SENSE; 42 VSS_AXG_SENSE → G45 VSSAXG_SENSE

1.8V RAIL: 1D8V_S0
C922 SC1U10V2KX-1GP
ICC_MAX:1.2A
VCCPLL1 BB3, VCCPLL2 BC1, VCCPLL3 BC4

SENSE LINES: VDDQ_SENSE BC43 TP_VDDQ_SENSE, VSS_SENSE_VDDQ BA43 TP_VDDQ_VSS
TP901 TPAD14-OP-GP
TP902 TPAD14-OP-GP

SA RAIL: 0D85V_S0
C915 SC10U6D3V5KX-1GP
ICC_MAX:6A
VCCSA1 L17, VCCSA2 L21, VCCSA3 N16, VCCSA4 N20, VCCSA5 N22, VCCSA6 P17, VCCSA7 P20, VCCSA8 R16, VCCSA9 R18, VCCSA10 R21, VCCSA11 U15, VCCSA12 V16, VCCSA13 V17, VCCSA14 V18, VCCSA15 V21, VCCSA16 W20

SENSE LINES: VCCSA_SENSE U10 ← VCCSA_SENSE

0D85V_S0
R902 100R2F-L1-GP-U
R902 need be close to pin U10.

VCCSA VID lines: VCCSA_VID0 D48 ← VCCSA_VID0; VCCSA_VID1 D49 ← VCCSA_VID1

VCCSA Voltage Select		
VID[1]	VID[0]	VCCSA
0	0	0.9 V
1	0	0.8 V
0	1	0.725 V
1	1	0.675 V

1D05V_VTT_CPU
R908 10KR2J-L-GP DY
R912 10KR2J-L-GP DY
VCCSA_VID0
VCCSA_VID1
VCCSA_VID0 48
VCCSA_VID1 48
R913 10KR2J-L-GP
R914 10KR2J-L-GP

IVY-BRIDGE-GP-NF

71.00IVY.A0U

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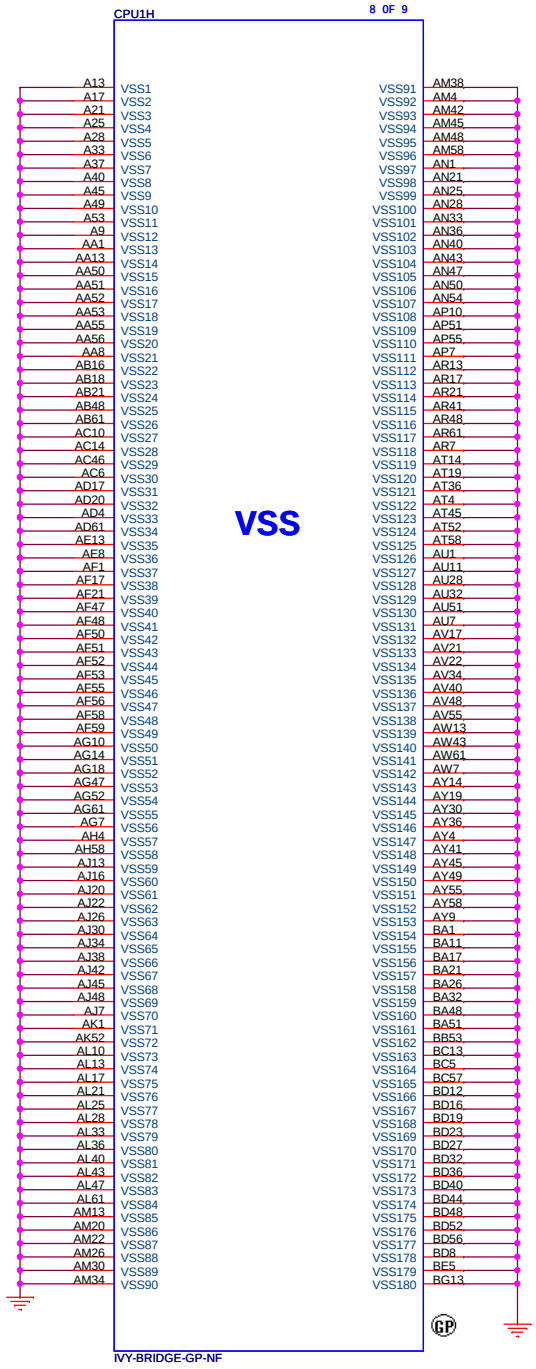
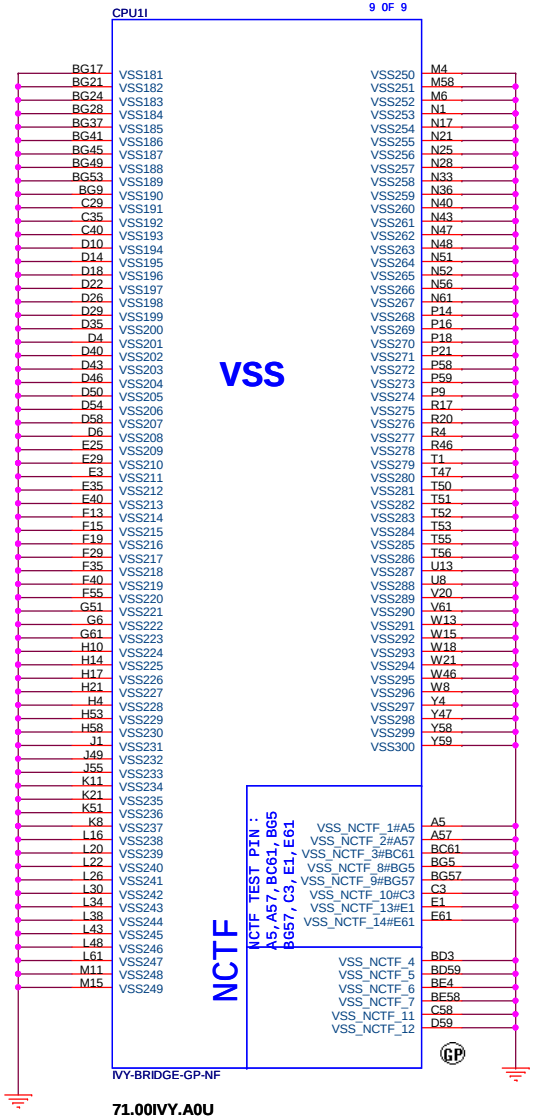
Title: CPU (VCC_GFXCORE)
Size: Custom
Document Number: Petra Uma
Rev: -1
Date: Tuesday, July 10, 2012
Sheet 9 of 103

SSID = CPU





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Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 10 of 103

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Title: XDP

Size: A4 | Document Number: Petra Uma | Rev: -1

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Title: ***Reserved***

Size	Document Number	Rev
A4	**Petra Uma**	**-1**

Date: Wednesday, February 22, 2012 Sheet 12 of 103

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<Core Design>

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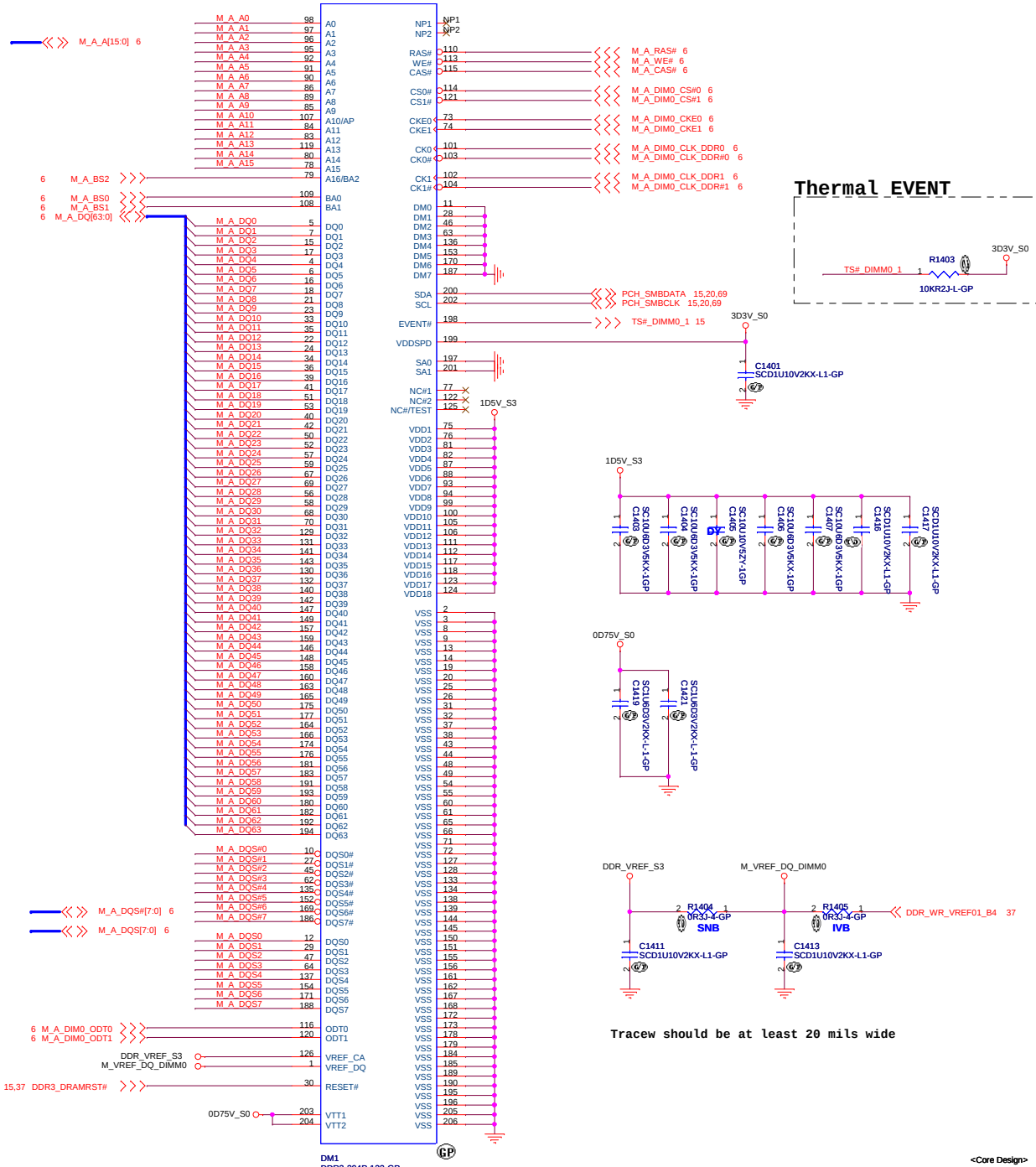
Title: ***Reserved***

Size	Document Number	Rev
A4	**Petra Uma**	**-1**

Date: Wednesday, February 22, 2012 Sheet 13 of 103

SSID = MEMORY



Thermal EVENT

Tracew should be at least 20 mils wide

<Core Design>

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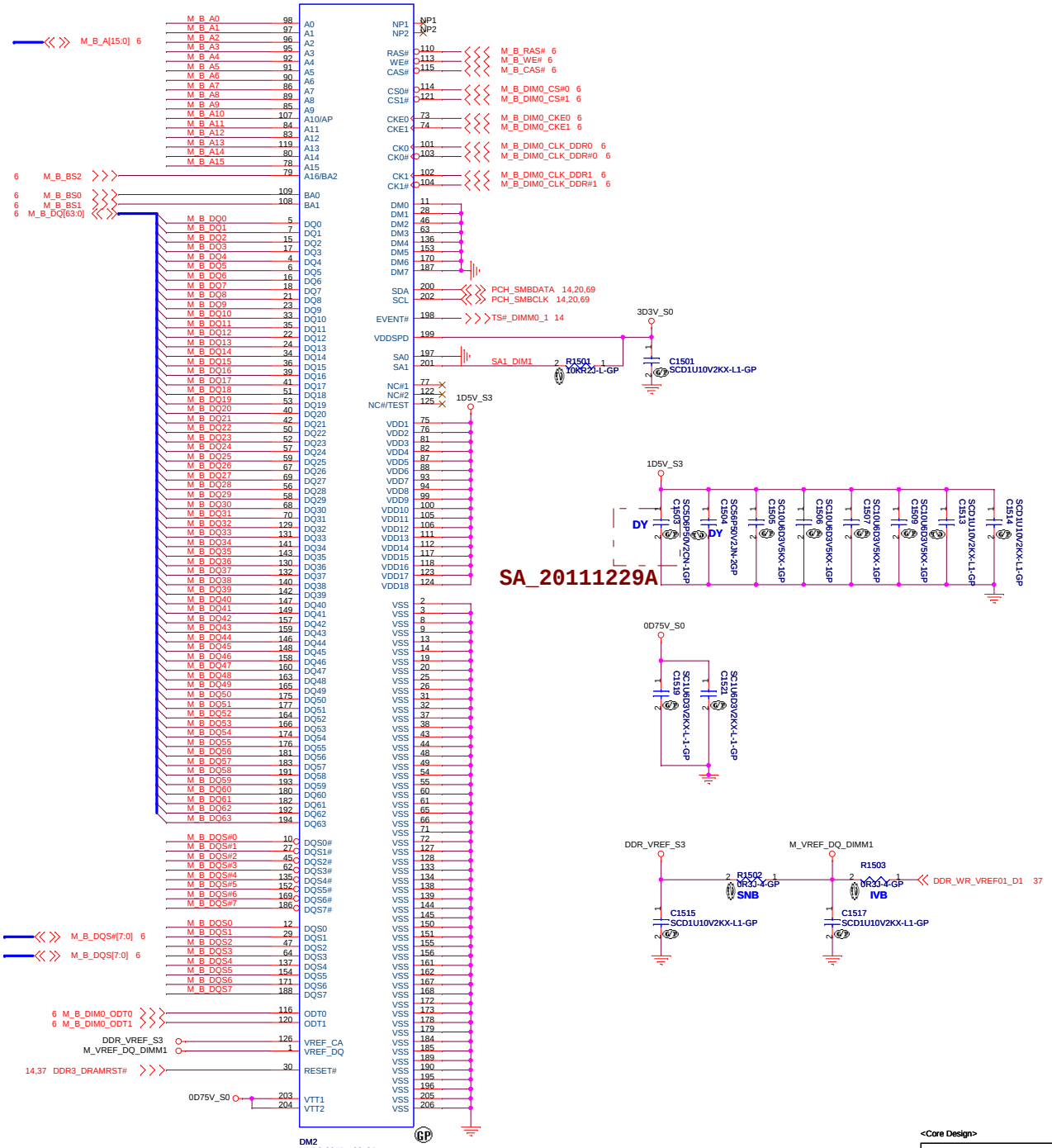
Title: ***DDR3-SODIMM1***

Size	Document Number	Rev
Custom	Petra Uma	-1

Date: Tuesday, July 10, 2012 Sheet 14 of 103

SSID = MEMORY



<Core Design>

緯創資通 **Wistron Corporation**
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Title: **DDR3-SODIMM2**

Size	Document Number	Rev
Custom	Petra Uma	-1

Date: Tuesday, July 10, 2012 Sheet 15 of 102

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<Core Design>

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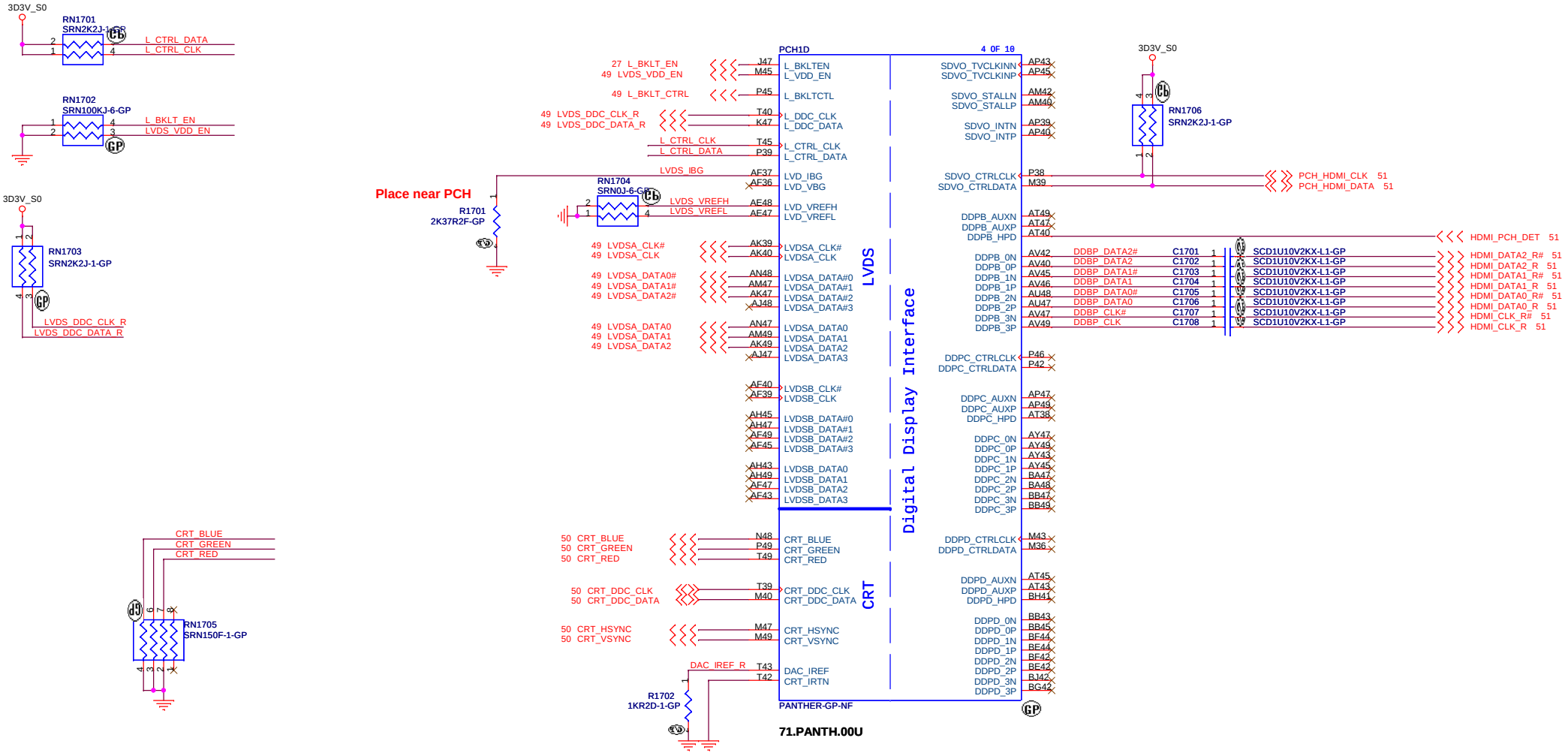
Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	**Petra Uma**	**-1**

Date: Wednesday, February 22, 2012 Sheet 16 of 103



<Core Design>

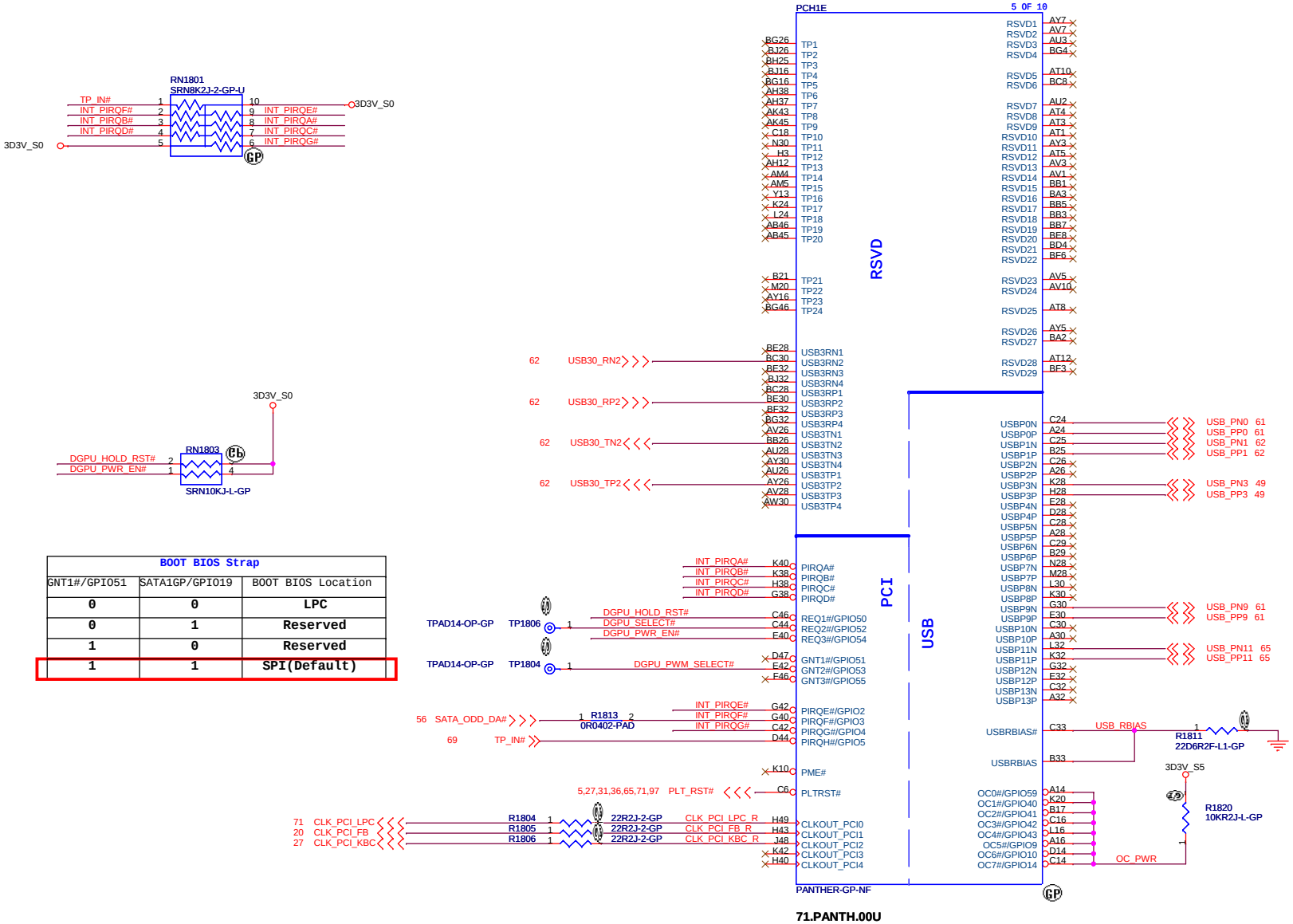
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (LVDS/CRT/DDI)**

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 17 of 103

SSID = PCH



BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Table

Pair	Device
0	USB2.0 Ext. port 1
1	USB3.0/USB2.0 Ext. port 2
2	
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

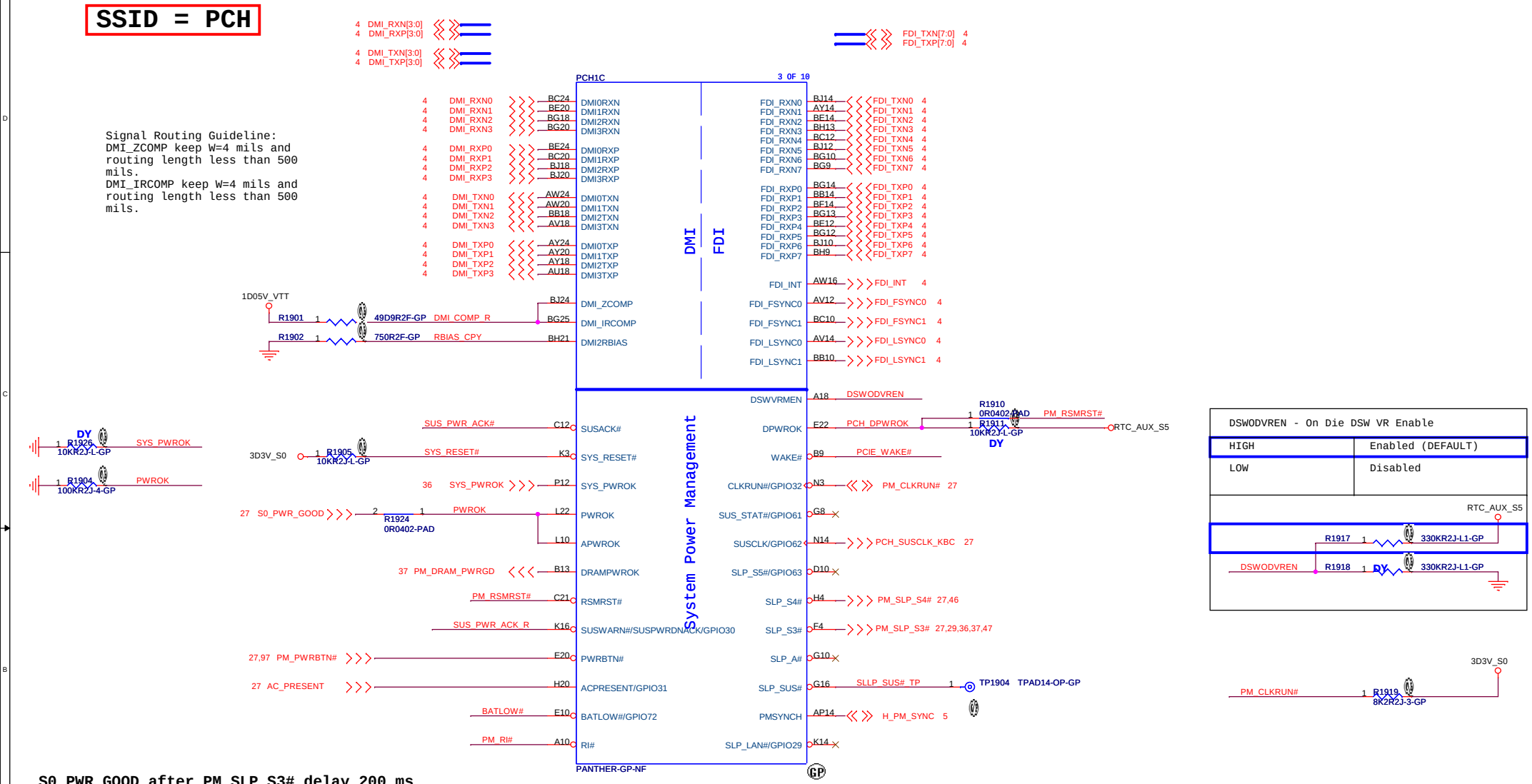
Title: PCH (PCI/USB/NVRAM)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 18 of 103

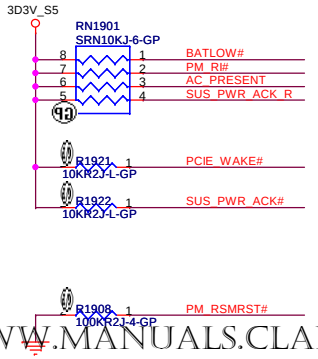
SSID = PCH

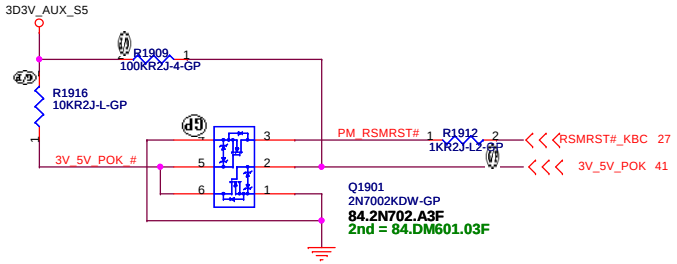
Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms





<Core Design>

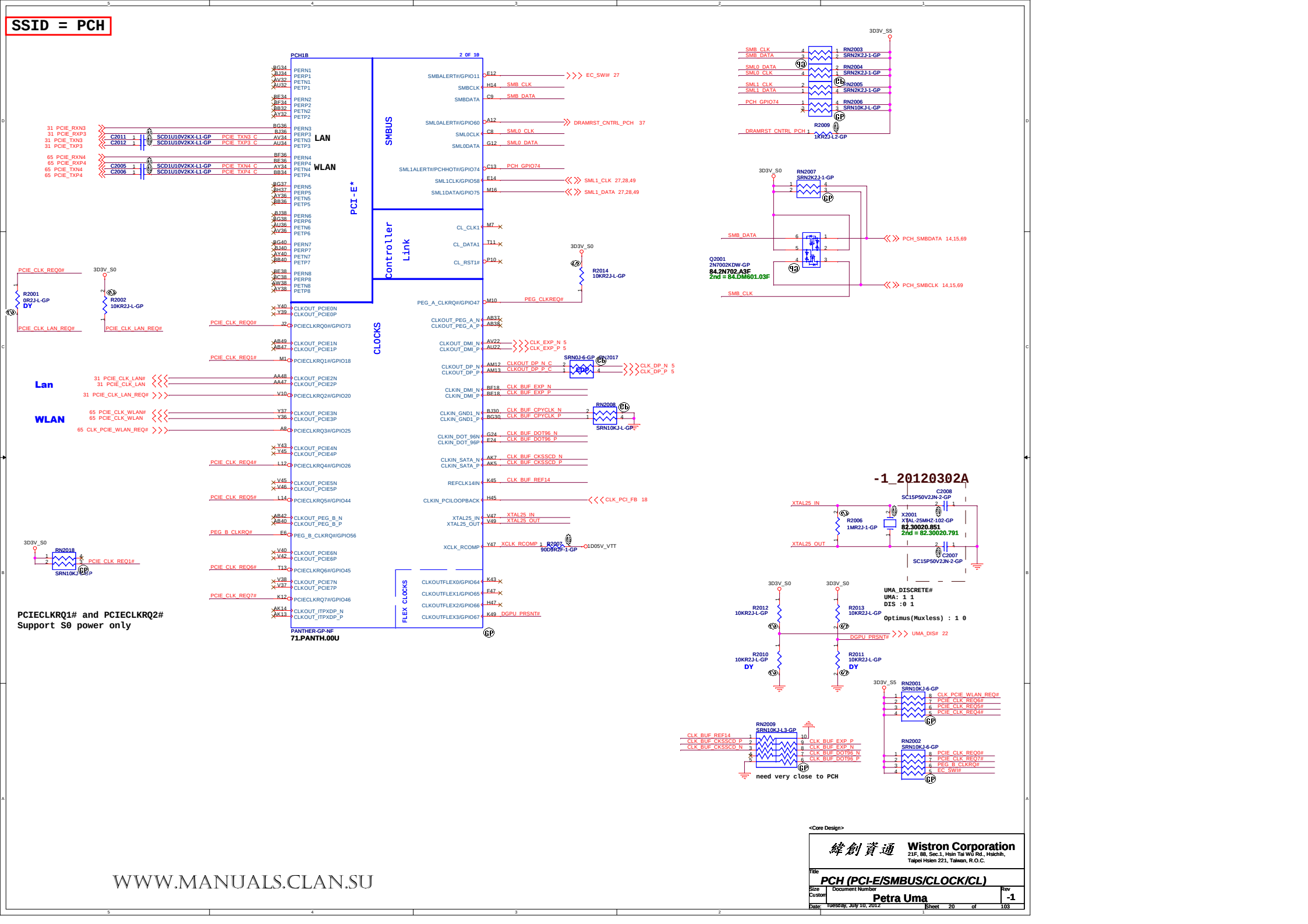
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 19 of 103

SSID = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size	Document Number	Rev
Custom	Petra Uma	-1

Date: Tuesday, July 10, 2012 Sheet 20 of 103

SSID = PCH

RTC_X1
RTC_X2
R2101 10MR2J-L-GP
X2101 X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.B21
C2101 SC6P50V2CN-1GP
C2102 SC6P50V2CN-1GP
-1_20120301

RTC_AUX_S5
R2115 20KR2F-L-GP
R2116 20KR2F-L-GP
C2103 SC1U16V3KX-5GP
-1_20120223

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

C2104 SC1U16V3KX-5GP
G2101 GAP-OPEN
R2104 1MR2J-L-GP
R2105 330KR2F-L-GP
RTC Reset

27 RTCRST_ON
R2106 100KR2F-L1-GP
R2111 2KR2F-3-GP
Q2102 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031

PCH1A 1 OF 10

RTC_X1	A20	RTCX1	RTC
RTC_X2	C20	RTCX2	
RTC_RST#	D20	RTCRST#	
SRTC_RST#	G22	SRTCRST#	
SM_INTRUDER#	K22	INTRUDER#	
PCH_INTVRMEN	C17	INTVRMEN	
HDA_BITCLK	N34	HDA_BCLK	IHDA
HDA_SYNC	L34	HDA_SYNC	
29 HDA_SPKR	T10	SPKR	
HDA_RST#	K34	HDA_RST#	
29 HDA_SDIN0	E34	HDA_SDIN0	
	G34	HDA_SDIN1	
	C34	HDA_SDIN2	
	A34	HDA_SDIN3	
27 ME_UNLOCK R2107 1KR2J-L2-GP	A36	HDA_SDO	
	C36	HDA_DOCK_EN#/GPIO33	
	N32	HDA_DOCK_RST#/GPIO13	
R2121 4K7R2J-L-GP PCH_JTAG_TCK_BUF	J3	JTAG_TCK	JTAG
	H7	JTAG_TMS	
	K5	JTAG_TDI	
	H1	JTAG_TDO	
27,60 SPI_CLK_R R2108 33R2J-L1-GP PCH_SPI_CLK	T3	SPI_CLK	SPI
27,60 SPI_CS0#_R R2109 33R2J-L1-GP PCH_SPI_CS0#	Y14	SPI_CS0#	
	T1	SPI_CS1#	
27,60 SPI_SI_R R2110 33R2J-L1-GP PCH_SPI_SI	V4	SPI_MOSI	
27,60 SPI_SO_R	U3	SPI_MISO	

PANTHER-GP-NF

71.PANTH.00U

FWH0/LAD0	C38	LPC_AD0	LPC
FWH1/LAD1	A38	LPC_AD1	
FWH2/LAD2	B37	LPC_AD2	
FWH3/LAD3	C37	LPC_AD3	
FWH4/LFRAME#	D36	LPC_FRAME# 27,71	
LDRQ0#	E36		
LDRQ1#/GPIO23	K36		
SERIRQ	V5	INT_SERIRQ 27	
SATA0RXN	AM3	SATA_RXN0 56	SATA 6G
SATA0RXP	AM1	SATA_RXP0 56	
SATA0TXN	AP7	SATA_TXN0 56	
SATA0TXP	AP5	SATA_TXP0 56	
SATA1RXN	AM10		
SATA1RXP	AM8		
SATA1TXN	AP11		
SATA1TXP	AP10		
SATA2RXN	AD7		
SATA2RXP	AD5		
SATA2TXN	AH5		
SATA2TXP	AH4		
SATA3RXN	AB8		
SATA3RXP	AB10		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	Y7	SATA_RXN4 56	SATA
SATA4RXP	Y5	SATA_RXP4 56	
SATA4TXN	AD3	SATA_TXN4 56	
SATA4TXP	AD1	SATA_TXP4 56	
SATA5RXN	Y3		
SATA5RXP	Y1		
SATA5TXN	AB3		
SATA5TXP	AB1		
SATAICOMPO	Y11		
SATAICOMPI	Y10	SATA_COMP R2112 37D4R2F-GP 1D05V_VTT	
SATA3RCOMPO	AB12		
SATA3COMPI	AB13	SATA3_COMP R2113 49D9R2F-GP 1D05V_VTT	
SATA3RBIAS	AH1	RBIAS_SATA3 R2114 750R2F-GP	
SATALED#	P3	SATA_LED#	
SATA0GP/GPIO21	V14	SATA_DET#0	
SATA1GP/GPIO19	P1		

LPC_AD[0..3] 27,71

HDD1
ODD

29 HDA_CODEC_SYNC R2122 33R2J-L1-GP HDA_SYNC
29 HDA_CODEC_SDOUT R2123 33R2J-L1-GP HDA_SDOUT
29 HDA_CODEC_RST#
29 HDA_CODEC_BITCLK
RN2102 SRN33J-5-GP-U HDA_RST# HDA_BITCLK

DY

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

+3VS_+1.5VS_HDA_IO
R2102 1KR2J-L2-GP HDA_SDOUT
DY

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

+3VS_+1.5VS_HDA_IO
R2103 1KR2J-L2-GP HDA_SYNC

5V_S0
HDA_CODEC_SYNC
Q2101 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
HDA_SYNC_R
R2124 33R2J-L1-GP HDA_SYNC

HDA_CODEC_BITCLK EC2102 SC4D7P50V2CN-1GP DY
HDA_CODEC_SDOUT EC2103 SC4D7P50V2CN-1GP DY
SPI_CS0#_R EC2101 SC4D7P50V2CN-1GP DY

3D3V_S0
RN2103 SRN10KJ-6-GP
22 PSW_CLR#
SATA_LED#
INT_SERIRQ
SATA_DET#0

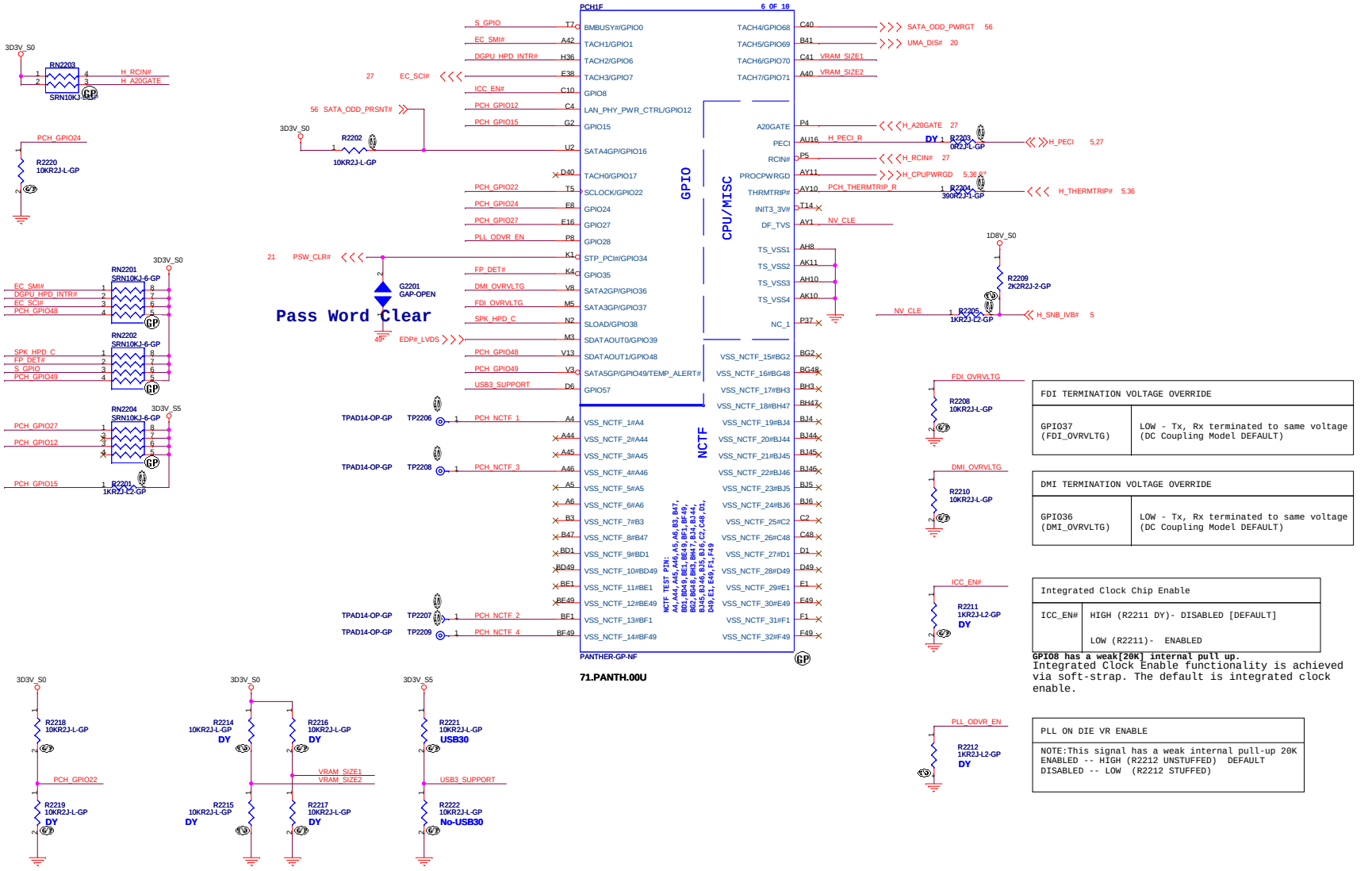
HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: Custom | Document Number: Petra Uma | Rev: -1
Date: Tuesday, July 10, 2012 | Sheet 21 of 103

SSID = PCH



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

<Core Design>

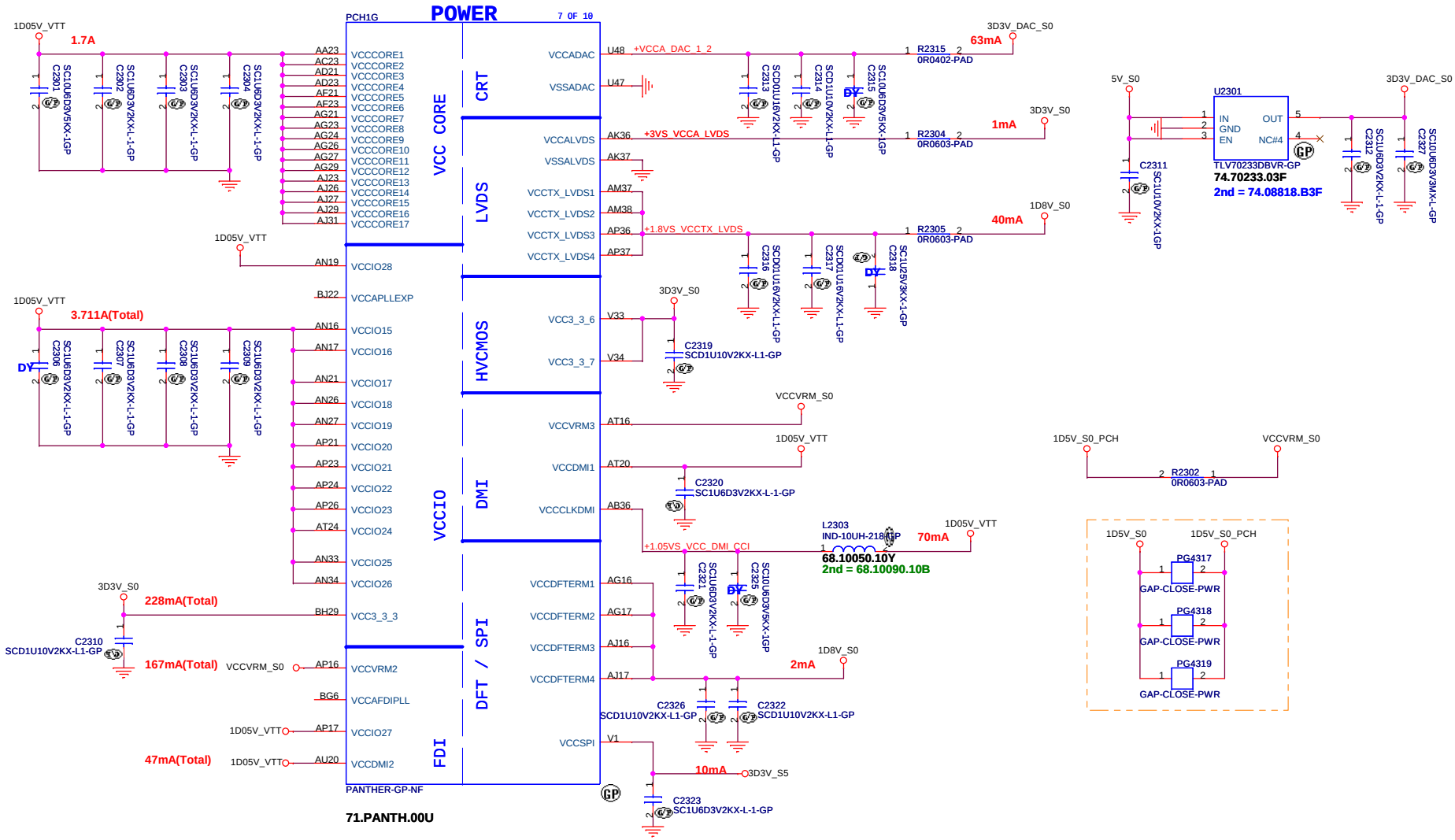
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 22 of 103

SSID = PCH



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 23 of 103

SSID = PCH

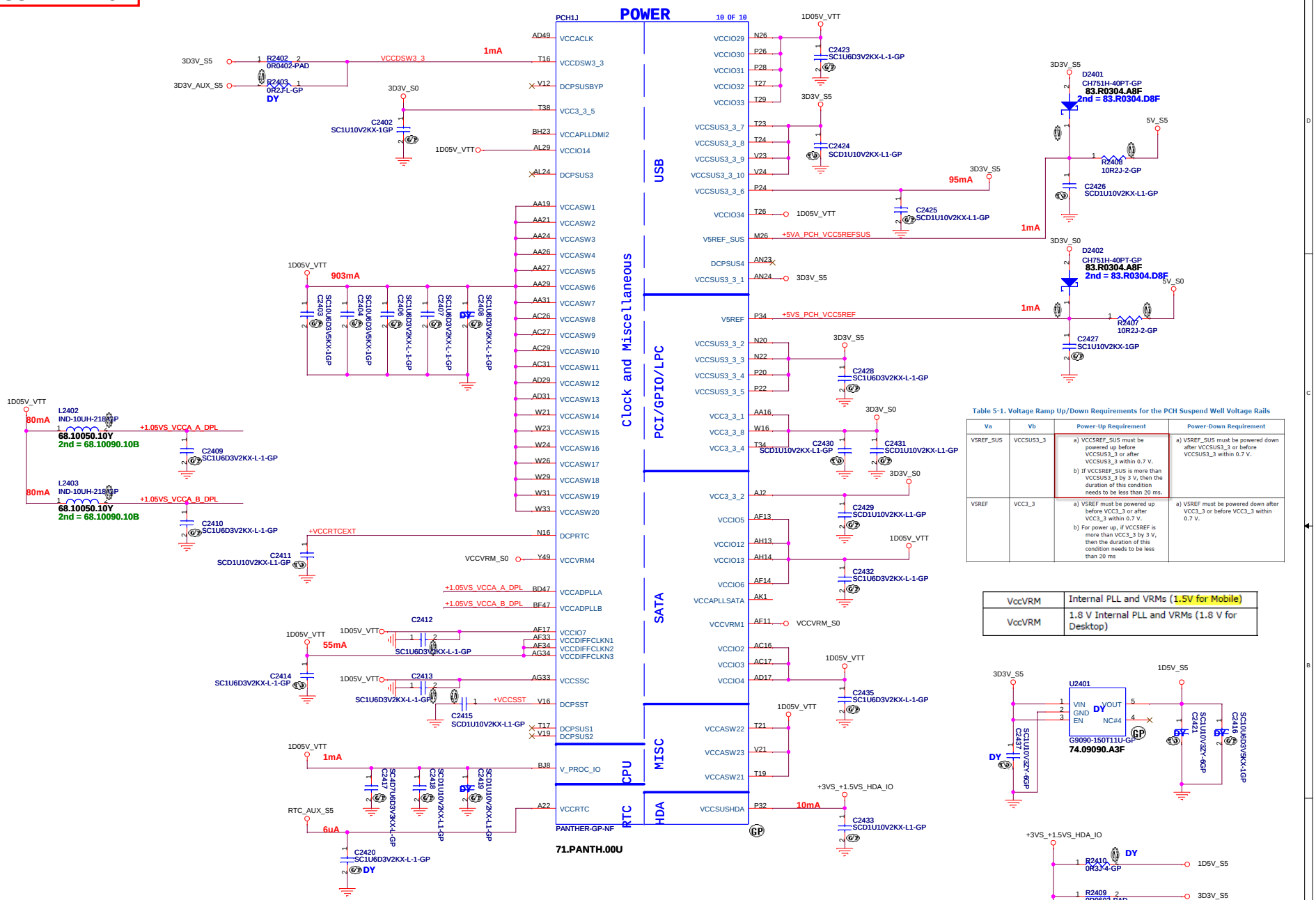


Table 5-1. Voltage Ramp Up/Down Requirements for the PCH Suspend Well Voltage Rails

Va	Vb	Power-Up Requirement	Power-Down Requirement
VSREF_SUS	VCCSUS3_3	a) VCC5REF_SUS must be powered up before VCCSUS3_3 or after VCCSUS3_3 within 0.7 V. b) If VCC5REF_SUS is more than VCCSUS3_3 by 3 V, then the duration of this condition needs to be less than 20 ms.	a) VSREF_SUS must be powered down after VCCSUS3_3 or before VCCSUS3_3 within 0.7 V.
VSREF	VCC3_3	a) VSREF must be powered up before VCC3_3 or after VCC3_3 within 0.7 V. b) For power up, if VCC5REF is more than VCC3_3 by 3 V, then the duration of this condition needs to be less than 20 ms	a) VSREF must be powered down after VCC3_3 or before VCC3_3 within 0.7 V.

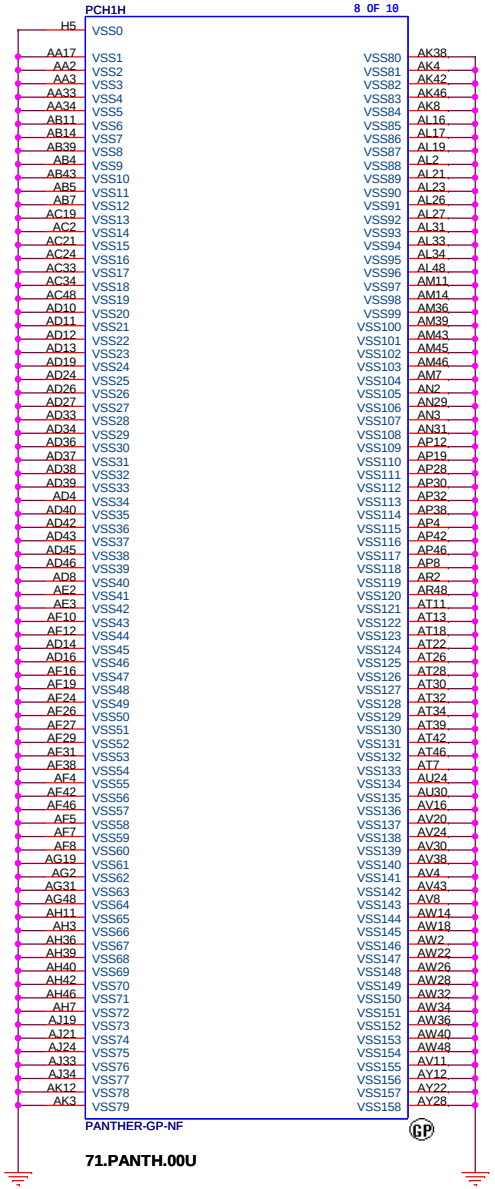
VccVRM	Internal PLL and VRMs (1.5V for Mobile)
VccVRM	1.8 V Internal PLL and VRMs (1.8 V for Desktop)

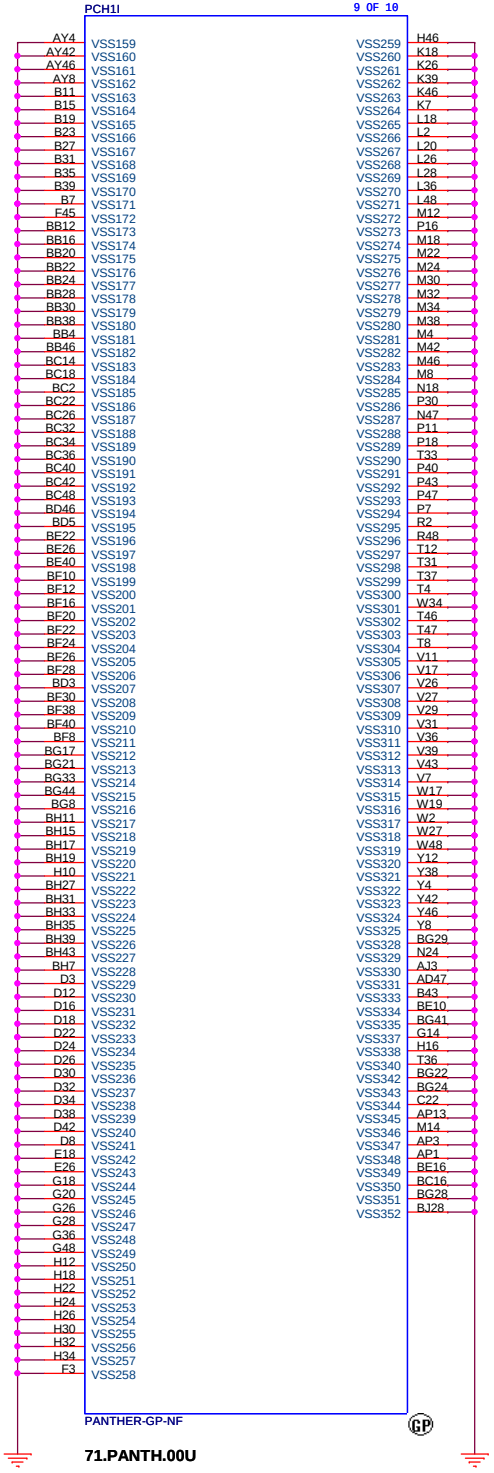
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER2)
Size: Custom | Document Number: Petra Uma | Rev: -1
Date: Tuesday, July 10, 2012 | Sheet 24 of 103

SSID = PCH





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 25 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Clock(colay)***

Size	Document Number	Rev
A4	**Petra Uma**	**-1**

Date: Wednesday, February 22, 2012 Sheet 26 of 103

SSID = KBC

-1_20120223

-1_20120221

-1_20120221

71.00885.A0G

PSL

FAE suggest

PSL Function

DISCRETE# will change to internal pull up

AC_IN#	KBC_PWRBTN#	EC_ENABLE#
Inputs		Output
PSL_IN1_GPI70	PSL_IN2_GPI06	Bit 1 of P7DOUT Register	PSL_OUT_GPIO71
Low	X	X	Low
High	High-to-Low	X	Low
High	X	0-to-1	High

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
-1M	100.0K	64.9K	2.0V
-2	100.0K	76.8	1.87V
-3	100.0K	100K	1.65V
-3M	100.0K	143.0K	1.358V
-1M For PCH B3	100.0K	174.0K	1.204V
		64.17435.6DL	
-4	100.0K	215.0K	1.047V

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

MODEL_ID	Pull-Low Register(R2712)	Pull-High Register(R2711)	SERIES RESISTOR(R2717)	Typical Voltage
14"(AMD)	30.0 K	100.0 K	40.2K	0.7615V
15"(AMD)	30.0 K	100.0 K	40.2K	0.4838V
14"(INV)	20.0 K	100.0 K	40.2K	0.55V
15"(INV)	20.0 K	100.0 K	40.2K	0.3888V
14"(UMA)	DY	100.0 K	40.2K	3.3V
15"(UMA)	DY	100.0 K	40.2K	0.9462V

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

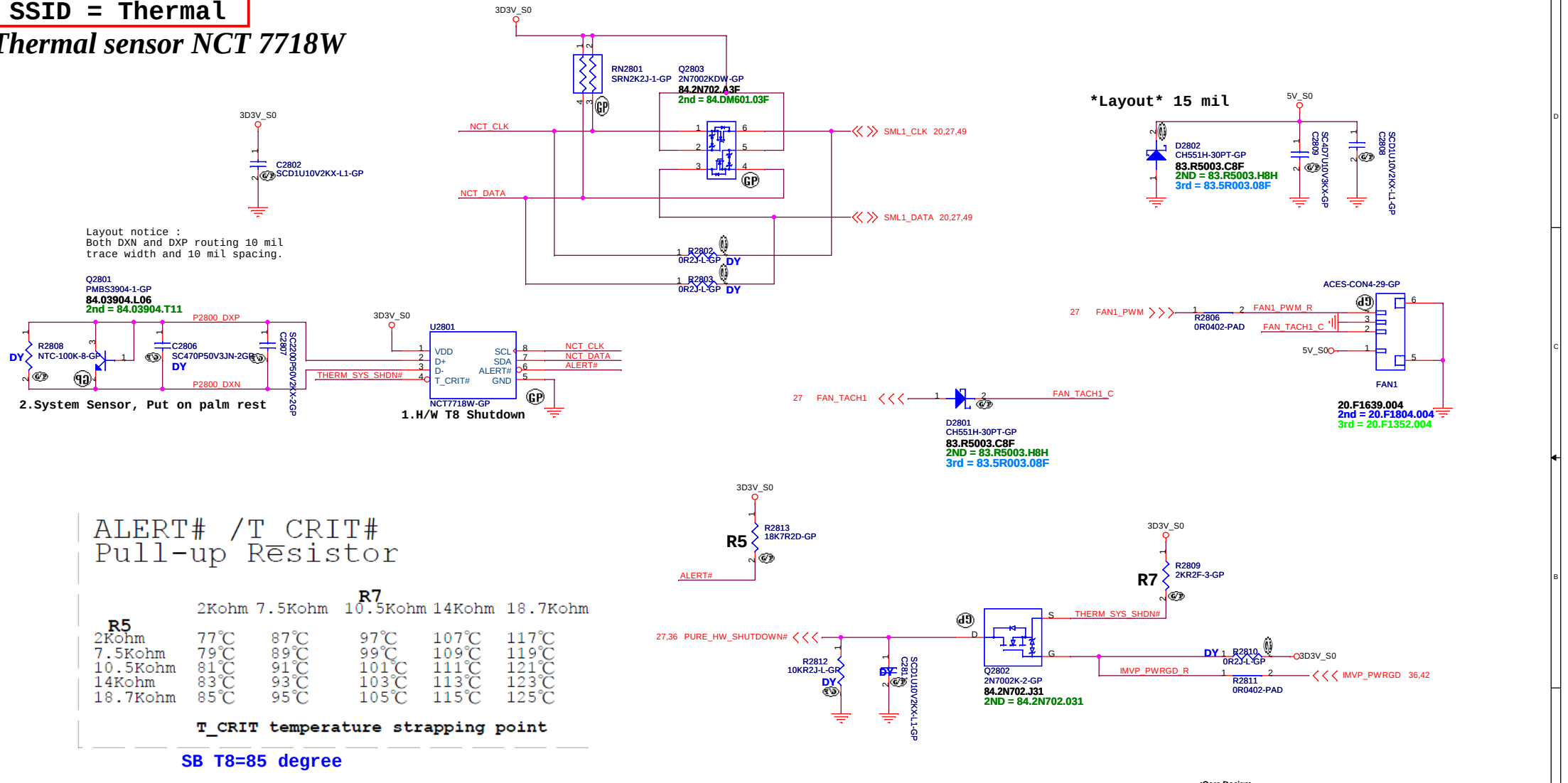
Title: KBC NPCE885

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 27 of 103

SSID = Thermal

Thermal sensor NCT 7718W



ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point

SB T8=85 degree

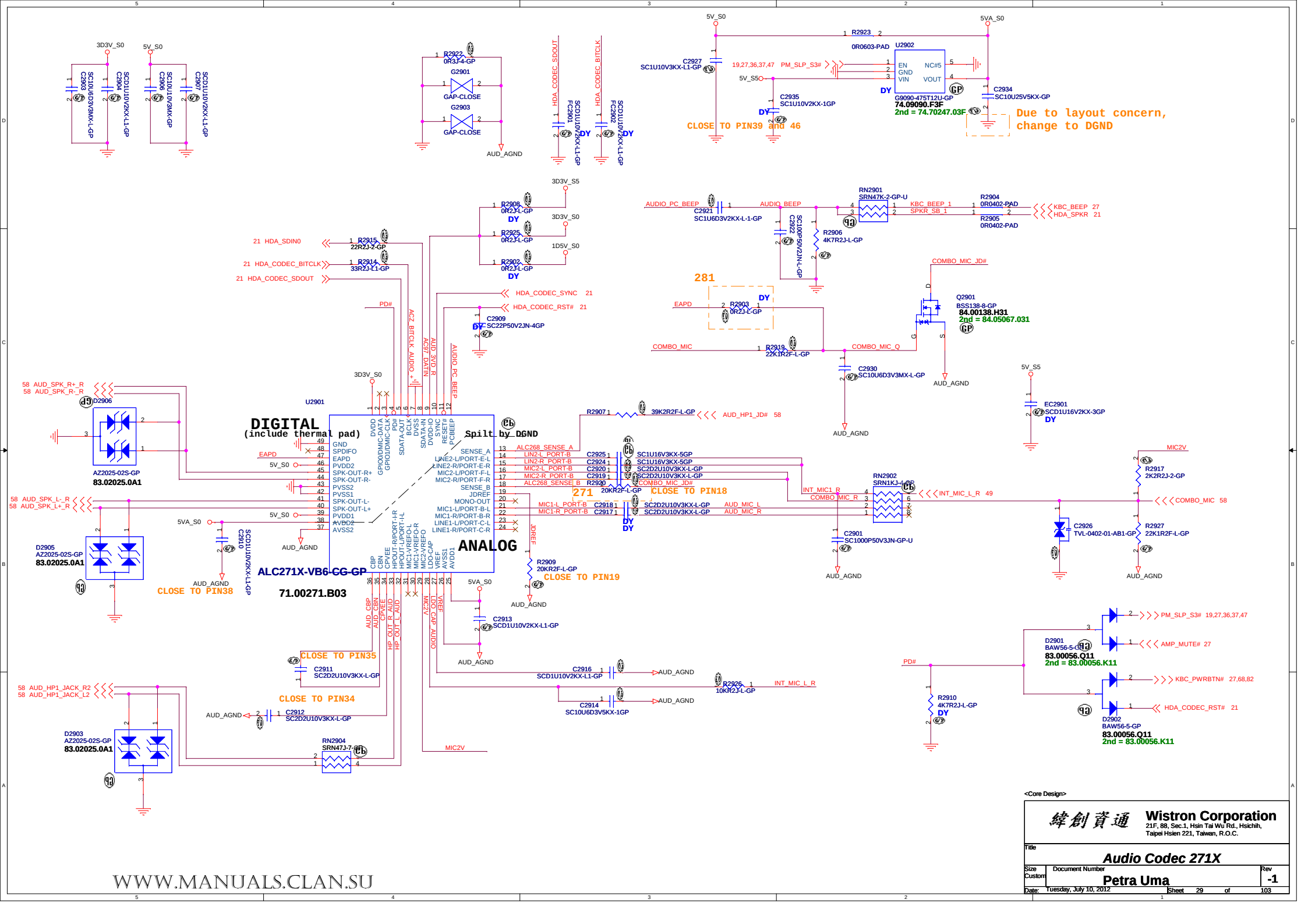
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal 7718/Fan Controllor P2793*

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 28 of 103



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec 271X**

Size: Custom | Document Number: **Petra Uma** | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 29 of 103

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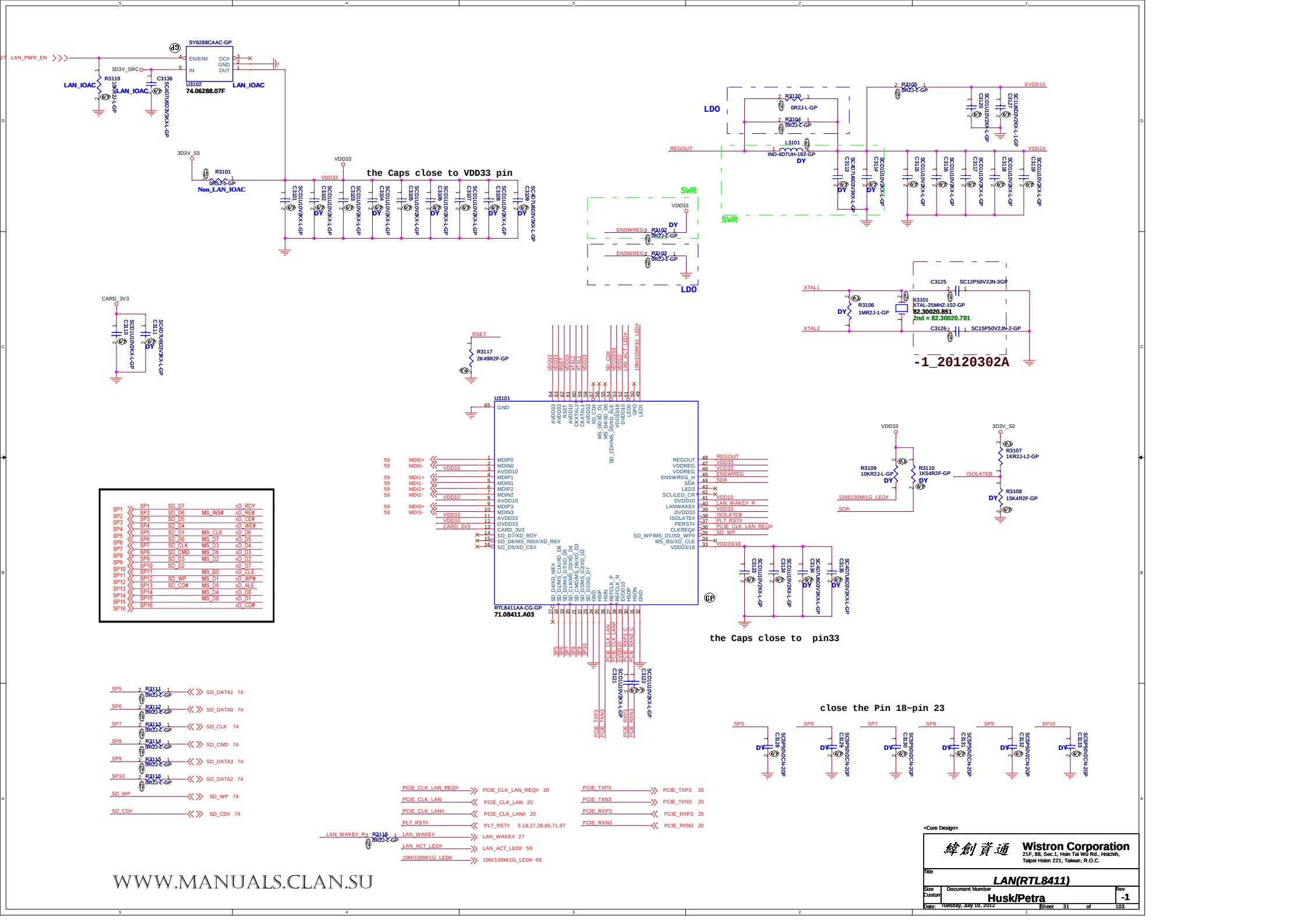
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio AMP***

Size	Document Number	Rev
A4	**Petra Uma**	**-1**

Date: Wednesday, February 22, 2012 Sheet 30 of 103



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN(RTL8411)

Size	Document Number	Rev
Custom	Husk/Petra	-1

Date: Tuesday, July 10, 2012 Sheet 31 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5159 (CARD READER)***

Size	Document Number	Rev
A4	**Petra Uma**	**-1**

Date: Wednesday, February 22, 2012 Sheet 32 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Petra Uma**	**-1**

Date: Wednesday, February 22, 2012 Sheet 33 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**Petra Uma**	**-1**

Date: Wednesday, February 22, 2012 Sheet 34 of 103

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<Core Design>

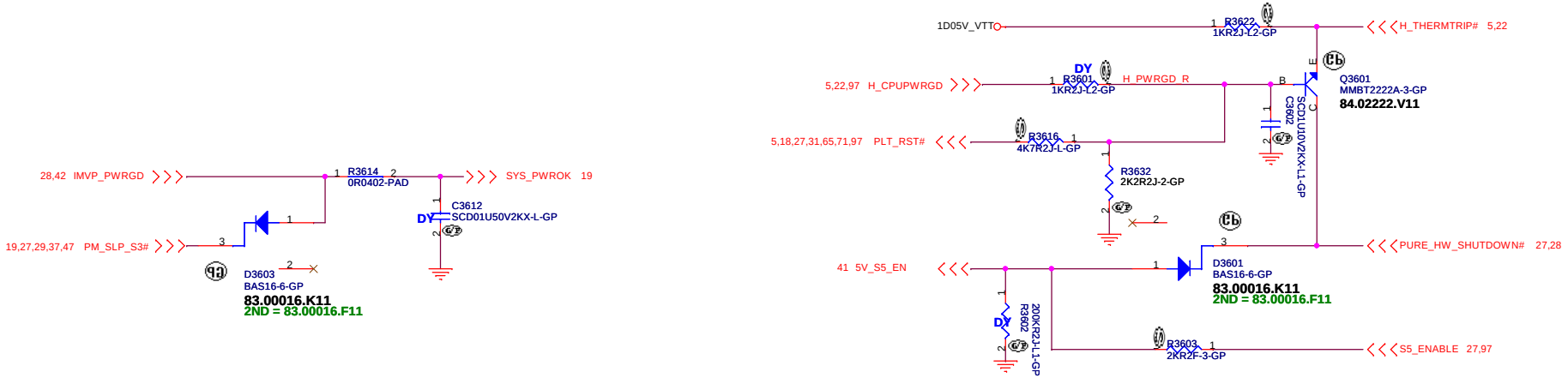
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

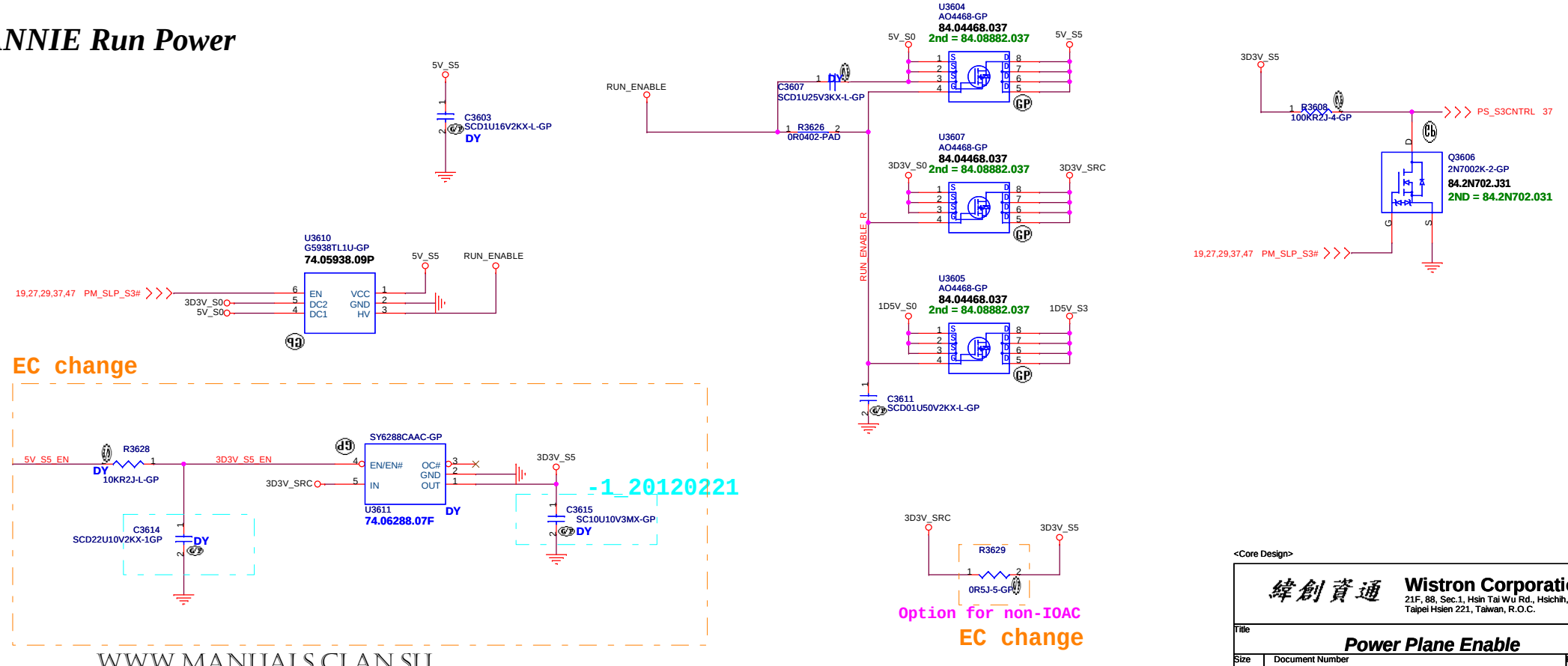
Size	Document Number	Rev
A4	**Petra Uma**	**-1**

Date: Wednesday, February 22, 2012 Sheet 35 of 103

Power Sequence



ANNIE Run Power



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	Petra Uma	-1

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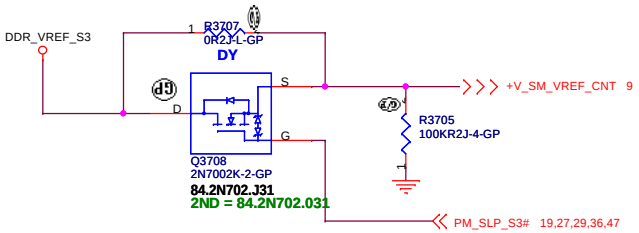
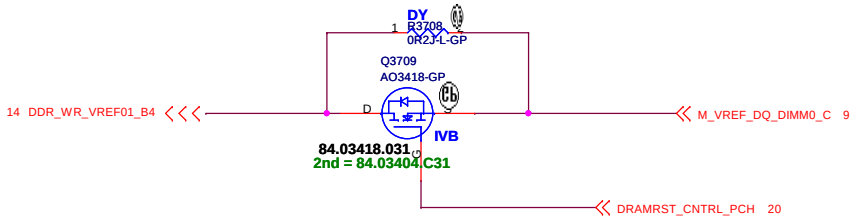
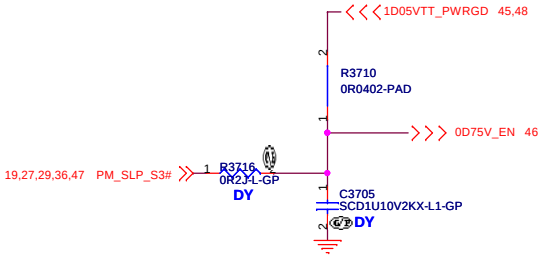
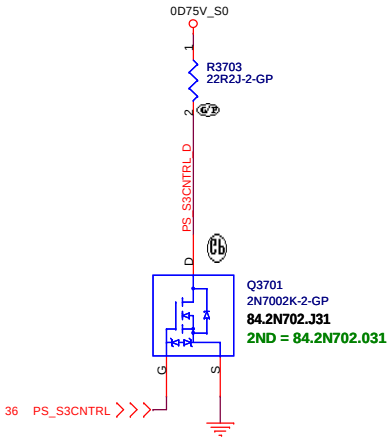
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

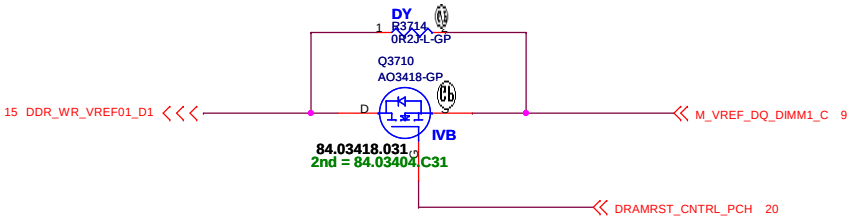




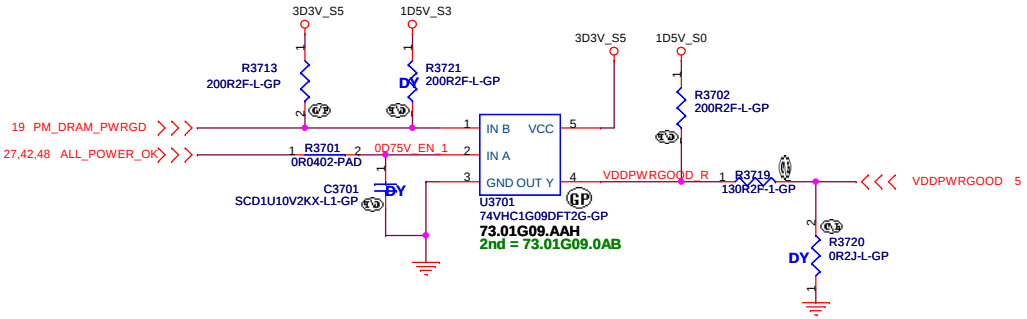
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



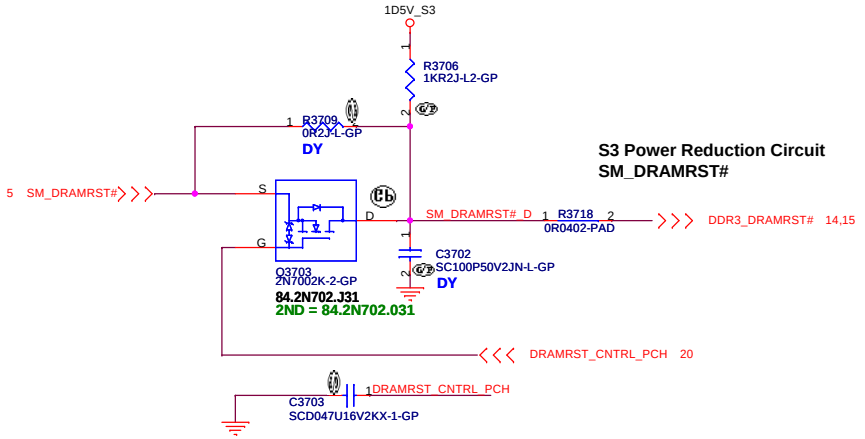




Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



S3 Power Reduction Circuit
SM_DRAMRST#

<Core Design>

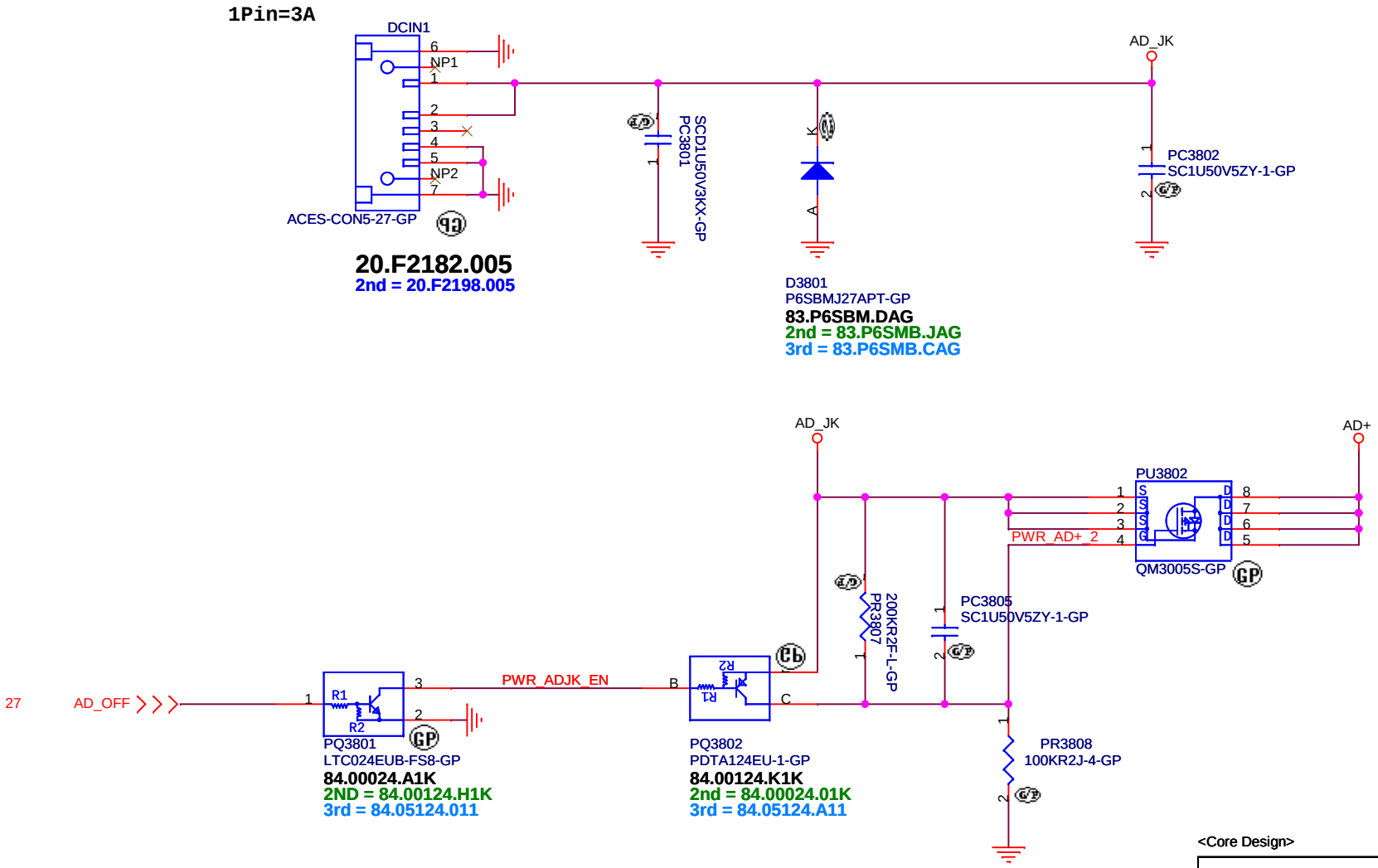
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADAPTER**

Size	Document Number	Rev
A3	Petra Uma	-1

Date: Tuesday, July 10, 2012 Sheet 37 of 103

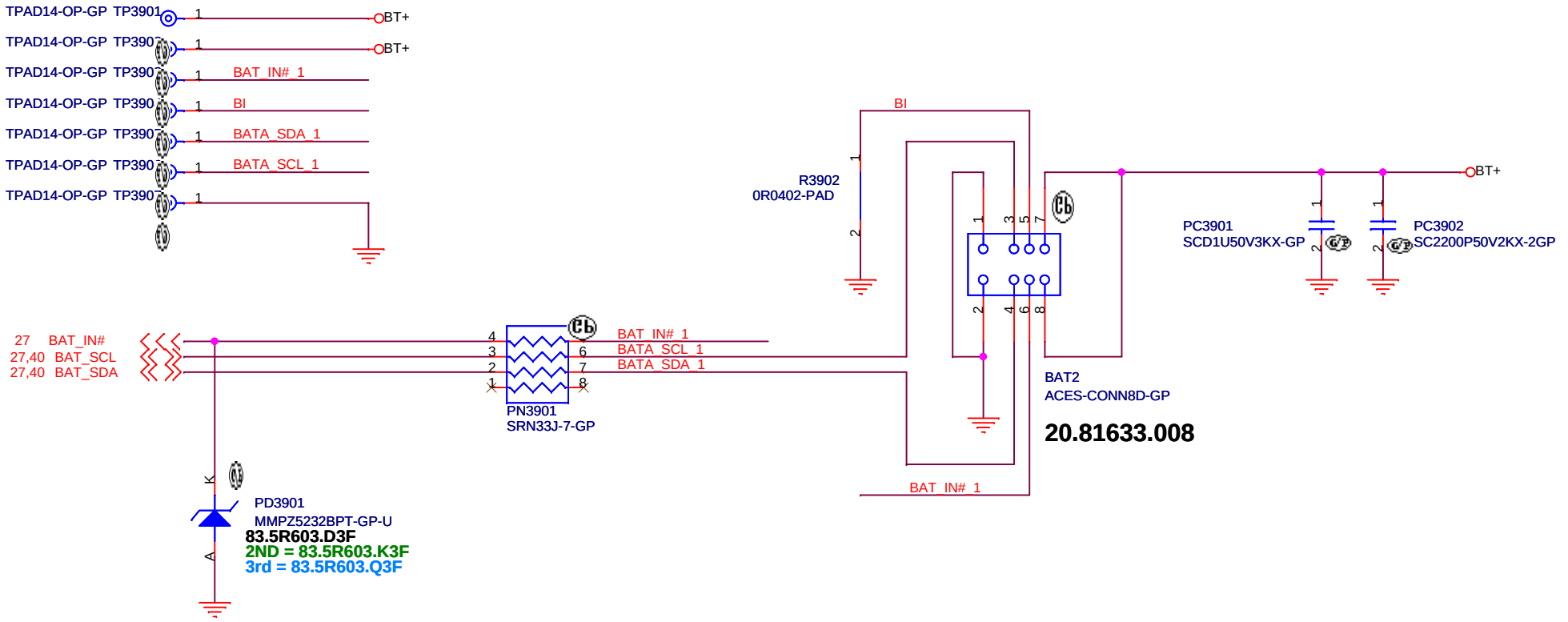
ANNIE solution
Adaptor in to generate DCBATOUT



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***DCIN JACK***
Size: A4	Document Number: **Petra Uma**
Rev: **-1**	
Date: Tuesday, July 10, 2012	Sheet 38 of 103

BATTERY CONNECTOR



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BATT CONN***

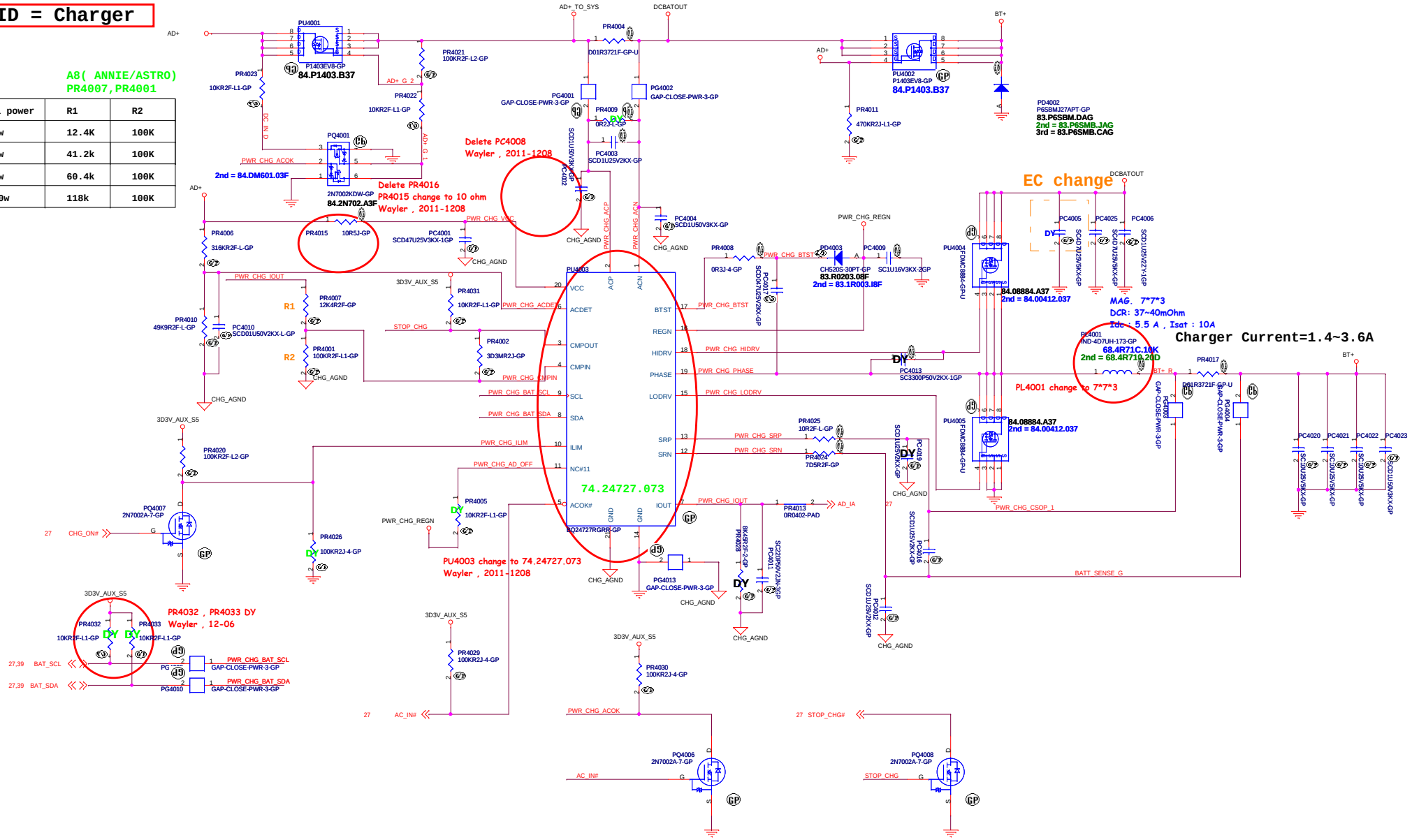
Size	Document Number	Rev
A4	**Petra Uma**	**-1**

Date: Tuesday, July 10, 2012 Sheet 39 of 103

SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4001

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



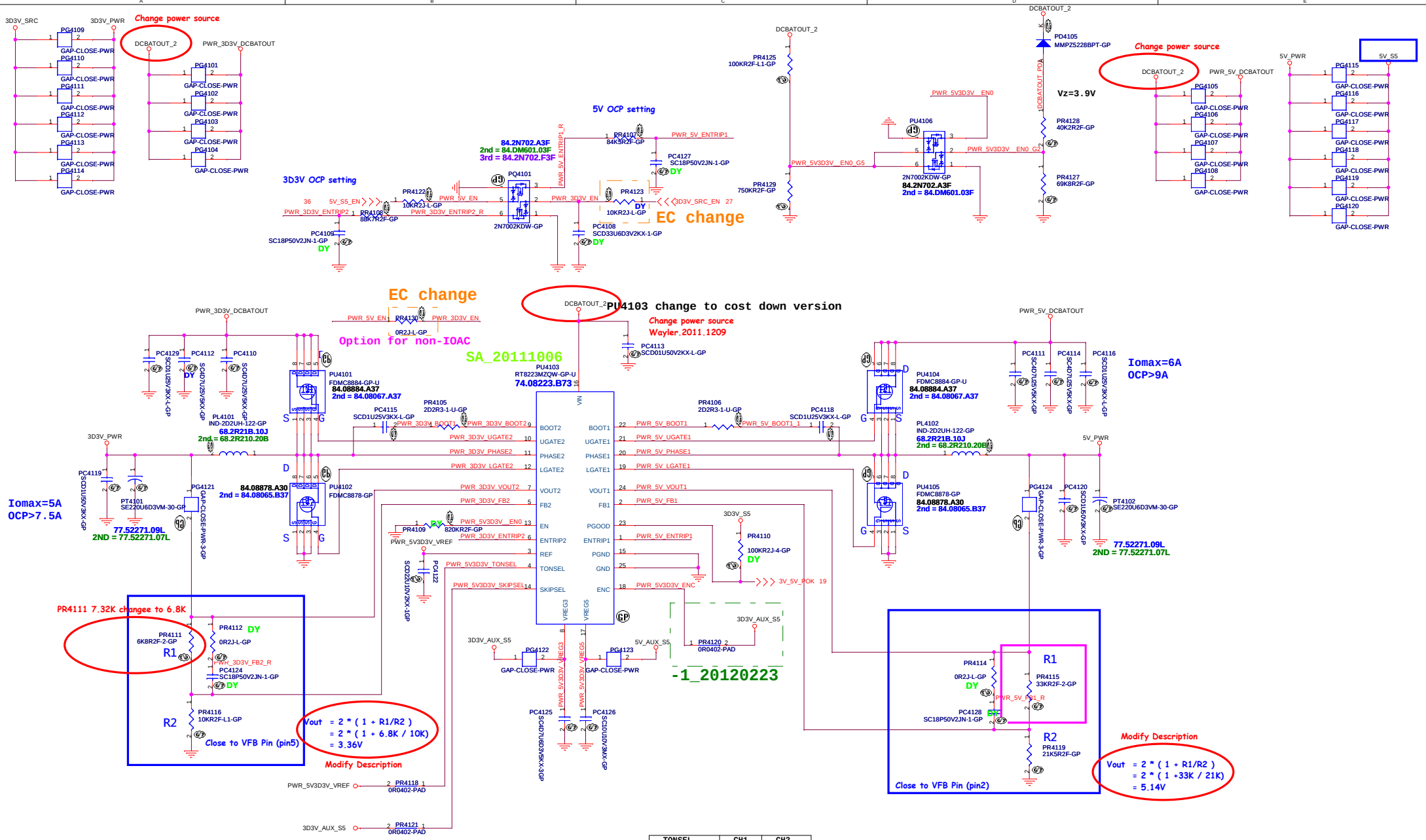
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24707A

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 40 of 108



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

<Core Design>

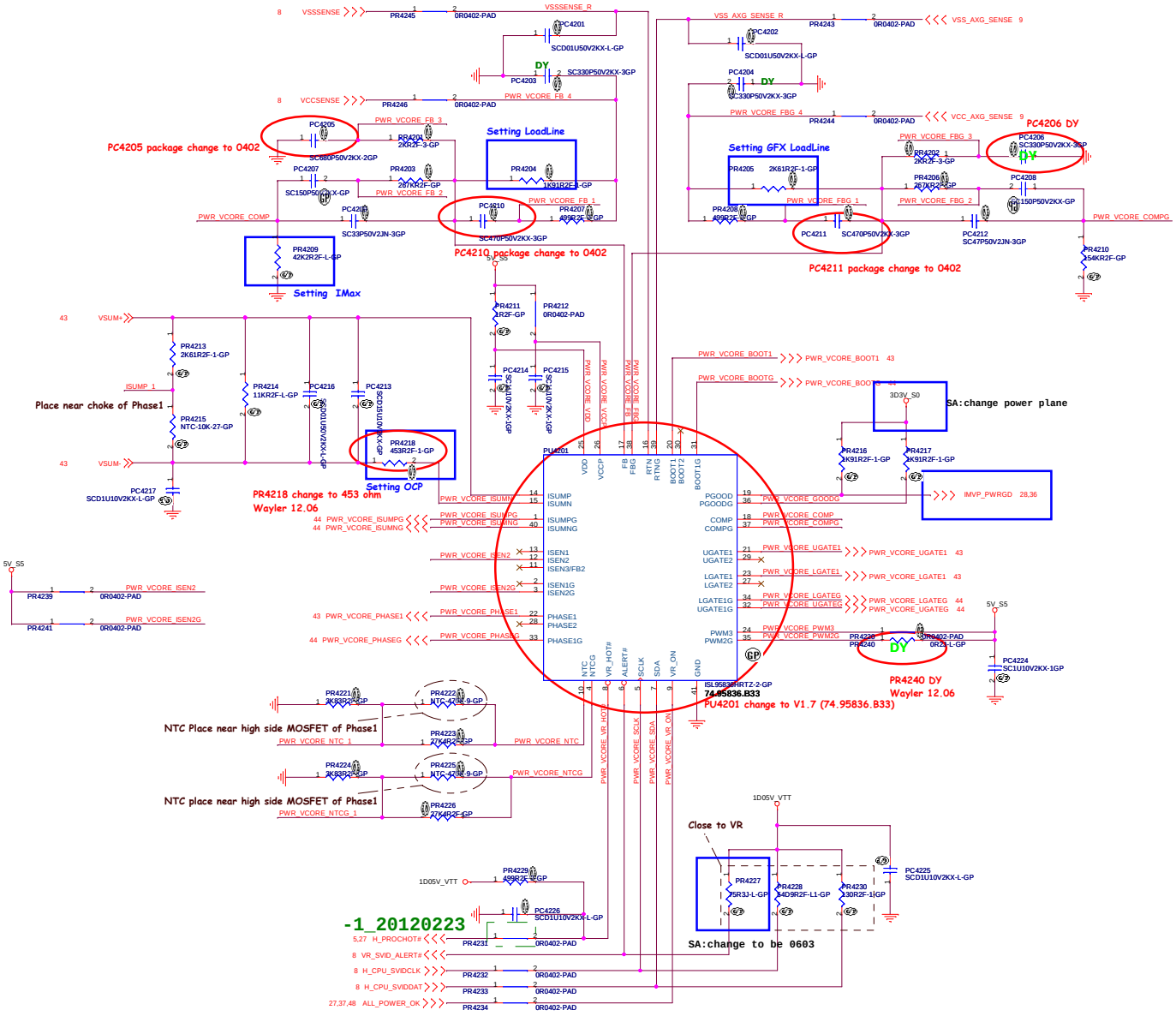
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V/3D3V(RT8223M)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 41 of 103

SSID = CPU.Regulator



WWW.MANUALS.CLAN.SU

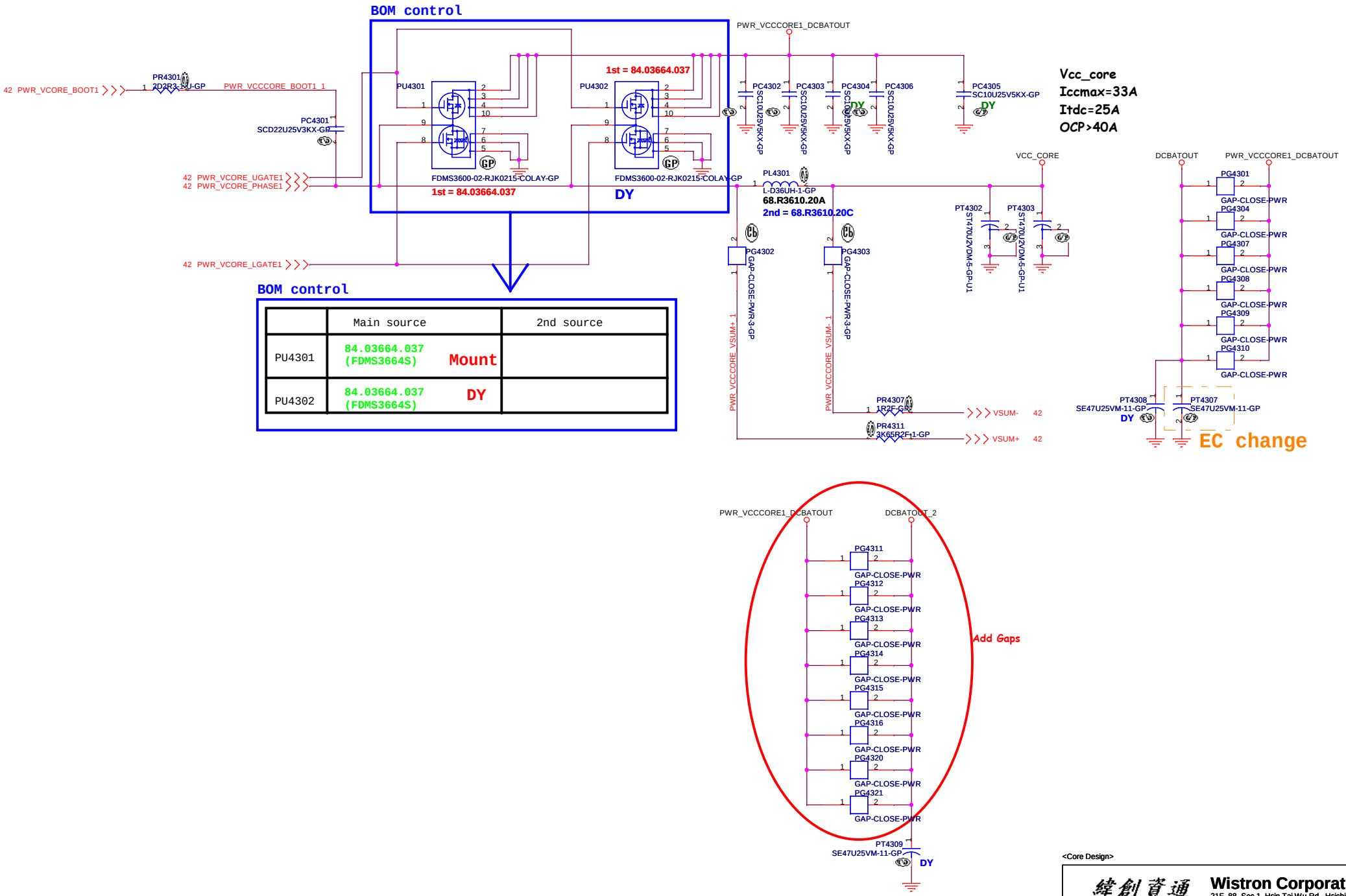
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(1/3)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 42 of 102



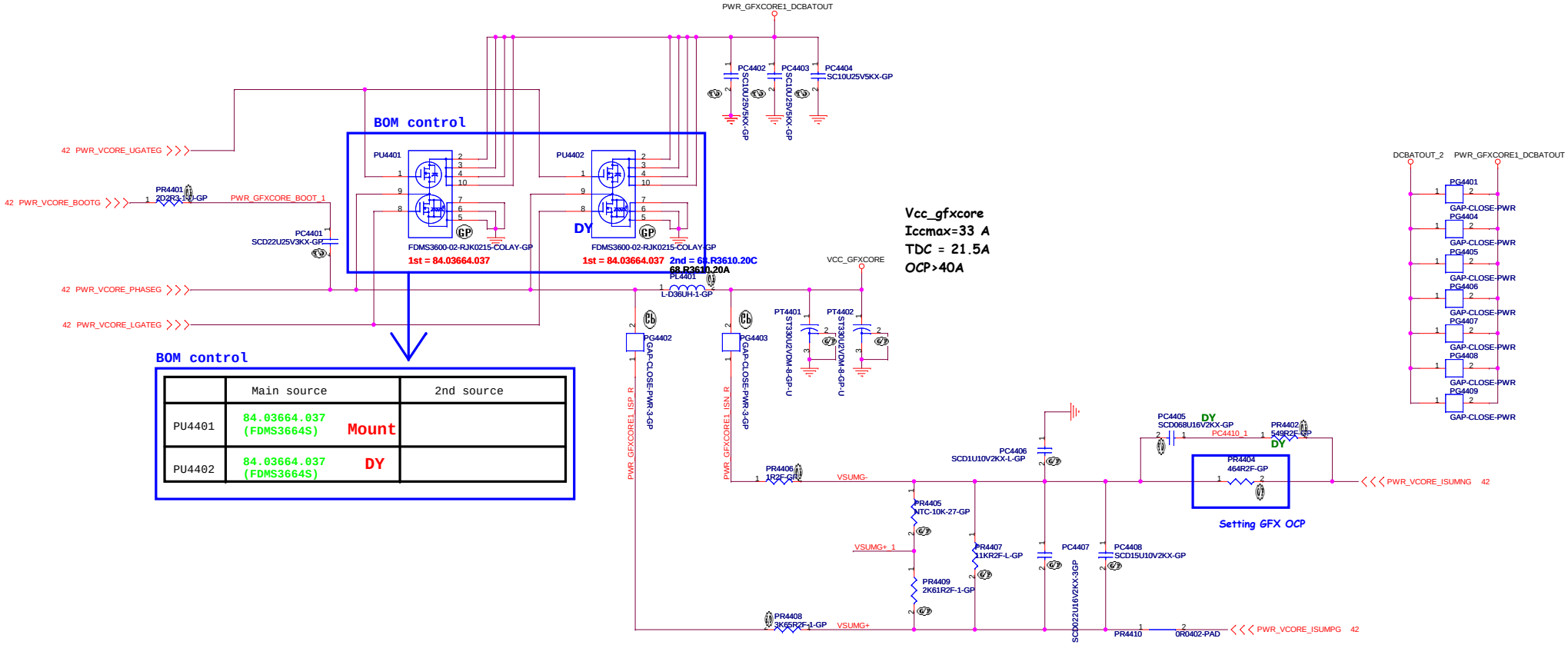
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(2/3)

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 43 of 102



BOM control

	Main source	2nd source
PU4401	84.03664.037 (FDMS3664S) Mount	
PU4402	84.03664.037 (FDMS3664S) DY	

<Core Design>

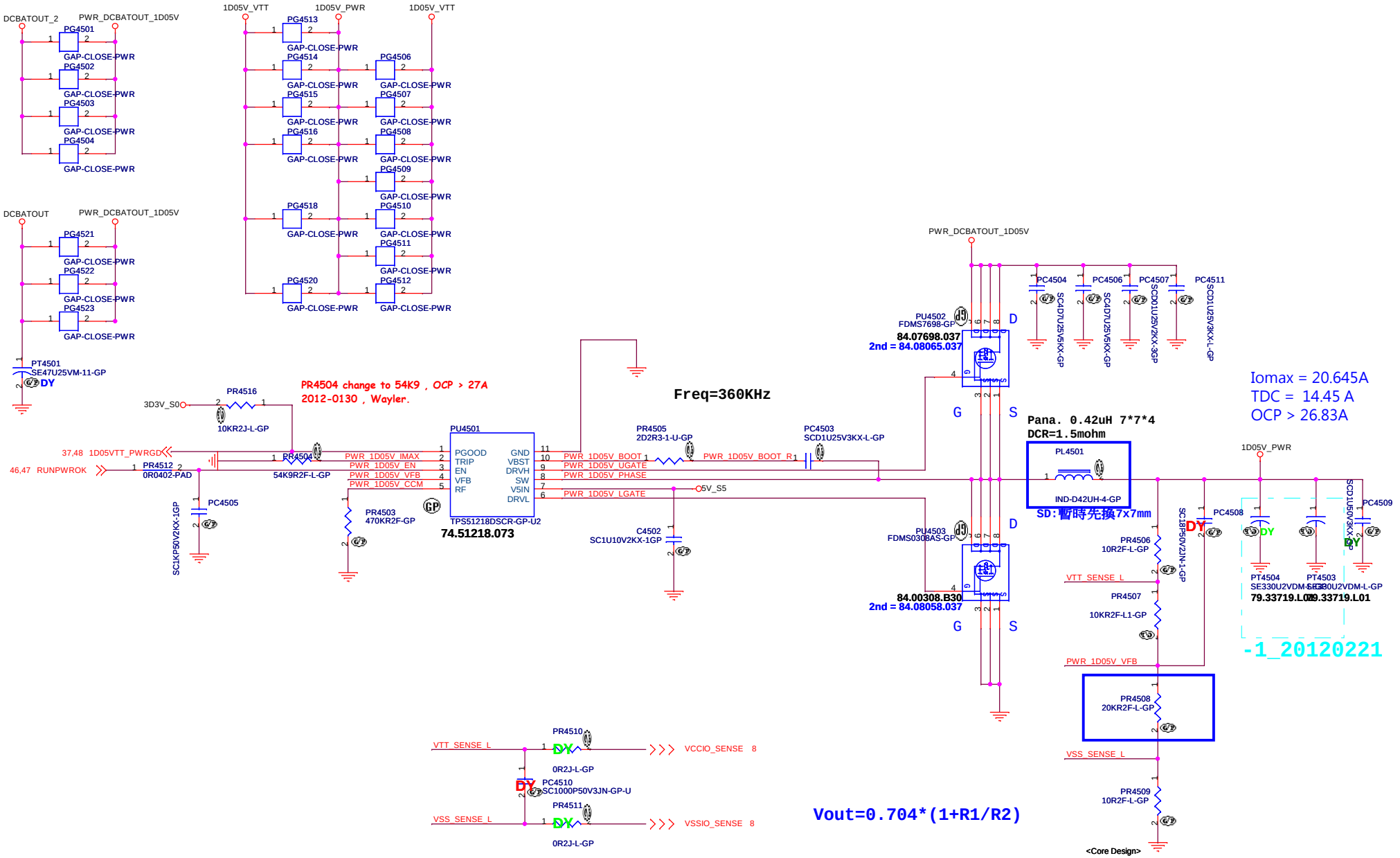
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95836_CPU_CORE(3/3)

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 44 of 102

TPS51218D for 1D05V

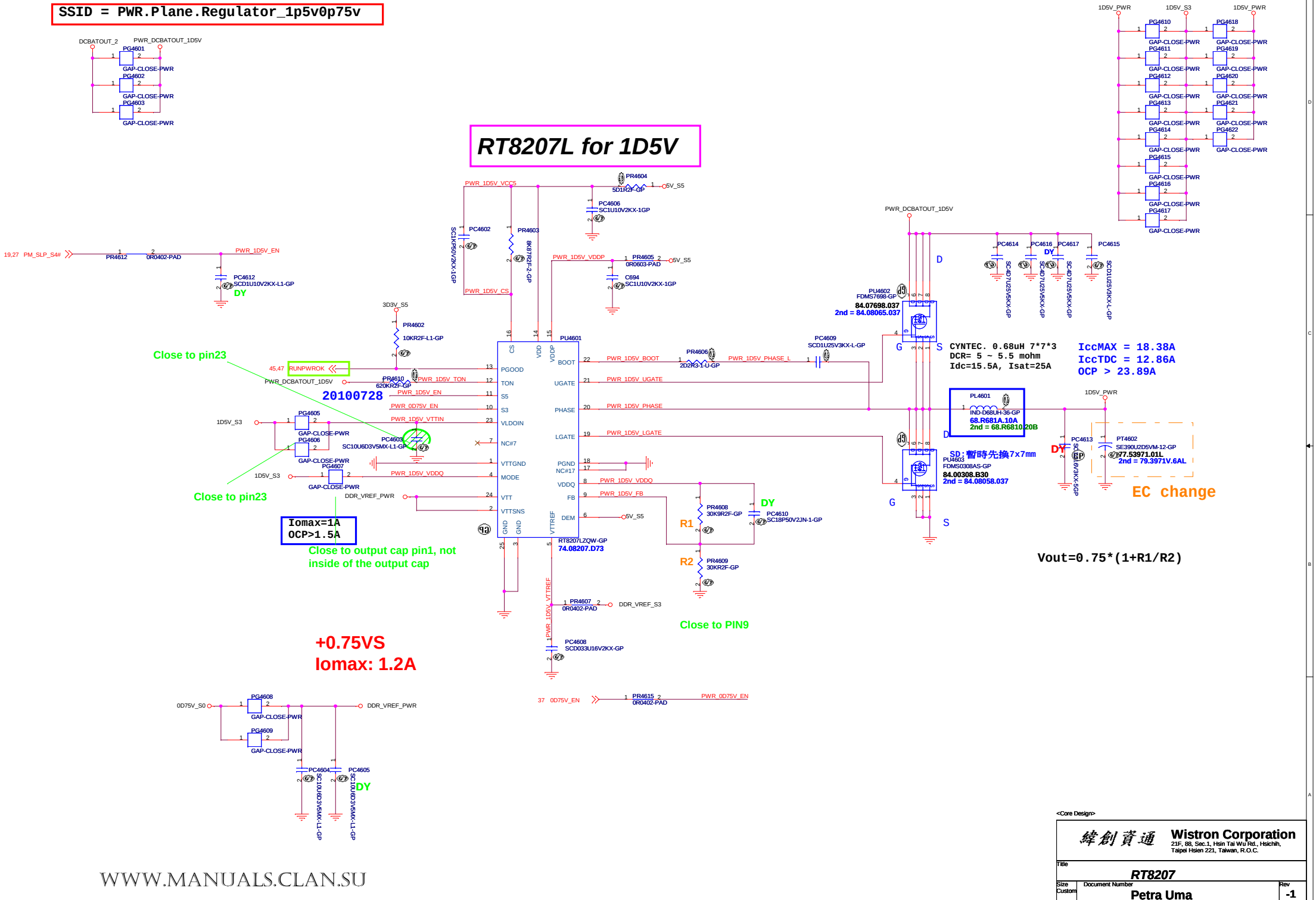


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC to DC 1D05V(TPS51218D)	
Size A3	Document Number Petra Uma	Rev -1
Date: Tuesday, July 10, 2012	Sheet 45 of 103	

SSID = PWR.Plane.Regulator_1p5v0p75v

RT8207L for 1D5V



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

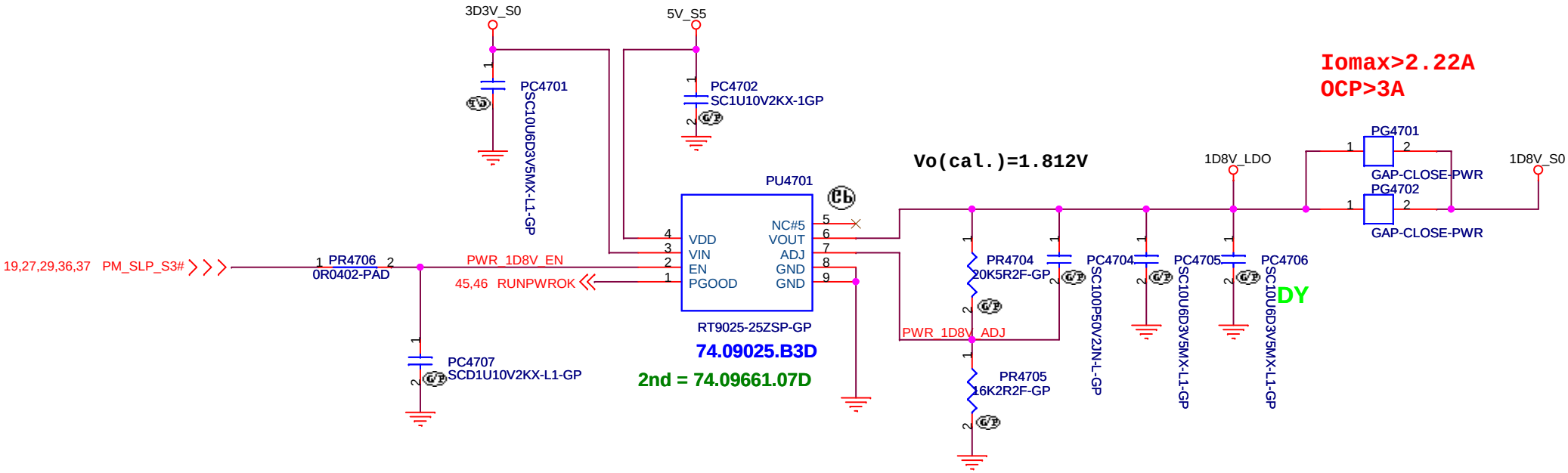
Title: RT8207

Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 46 of 103

SSID = PWR.Plane.Regulator_1p8v

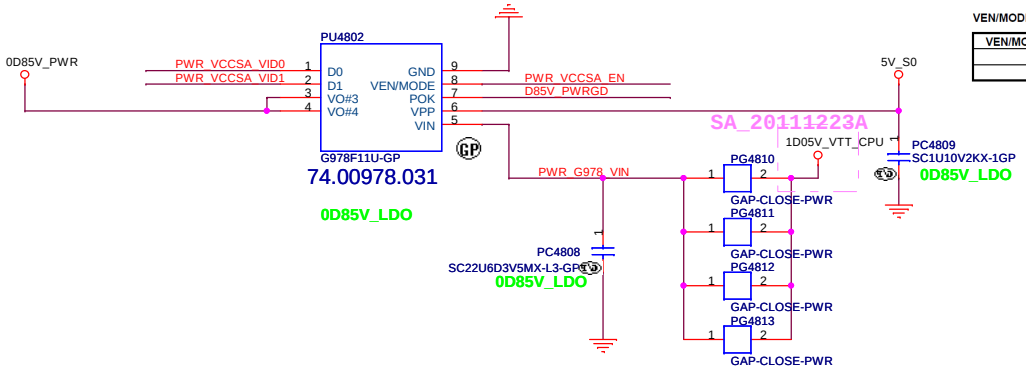
RT9025 for 1D8V_S0



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LDO_1D8V(RT9025)***
Size: A4	Document Number: **Petra Uma**
Rev: **-1**	
Date: Tuesday, July 10, 2012	Sheet 47 of 103

LDO G978 for VCCSA



D0, D1 V_O Selection Table

D0	D1	V_O, MODE=0	V_O, MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

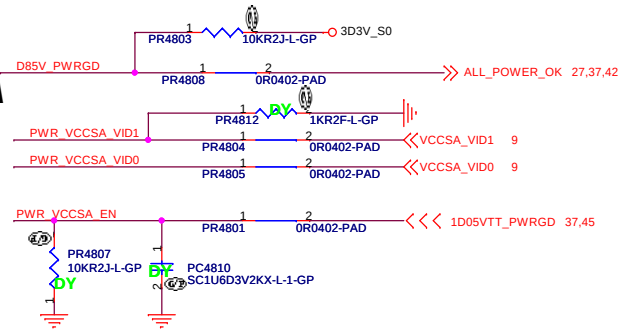
"x" means "don't care".

VEN/MODE Logic

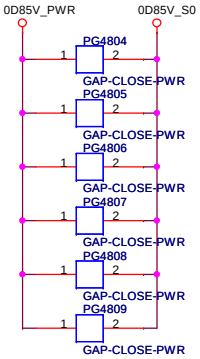
VEN/MODE (VPP=5V)	EN logic
<0.6V	0
>1.0V	1

VEN/MODE (VPP=5V)	MODE logic
<2.0V	0
>2.6V	1

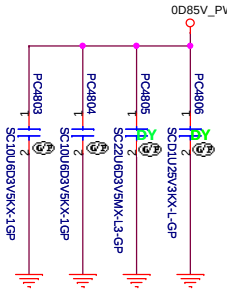
PWM SY8037 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V



Design Current =4 A



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VCCSA SY8037**

Size	Document Number	Rev
A3	Petra Uma	-1

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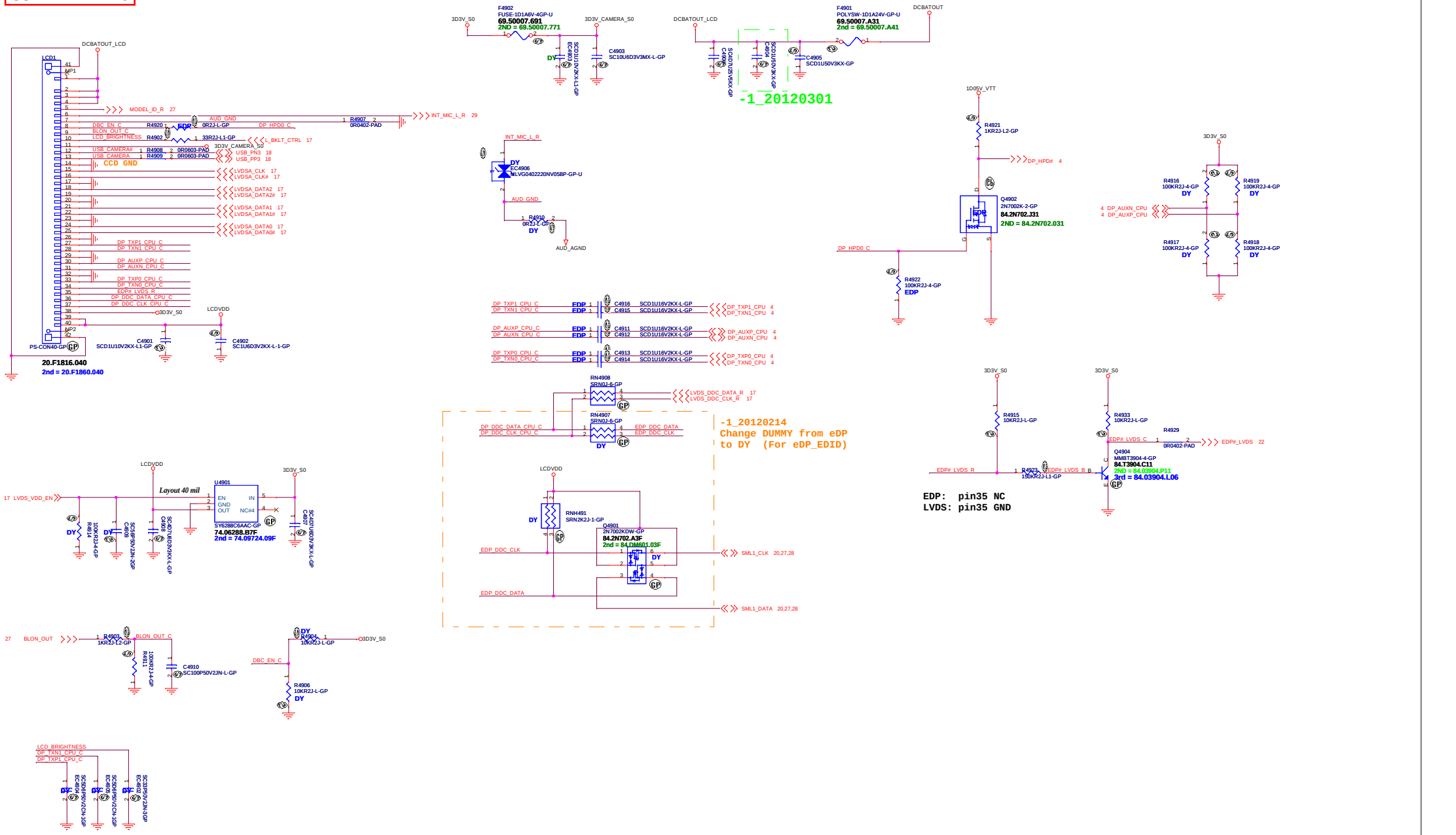
SSID = VIDEO



<Core Design>

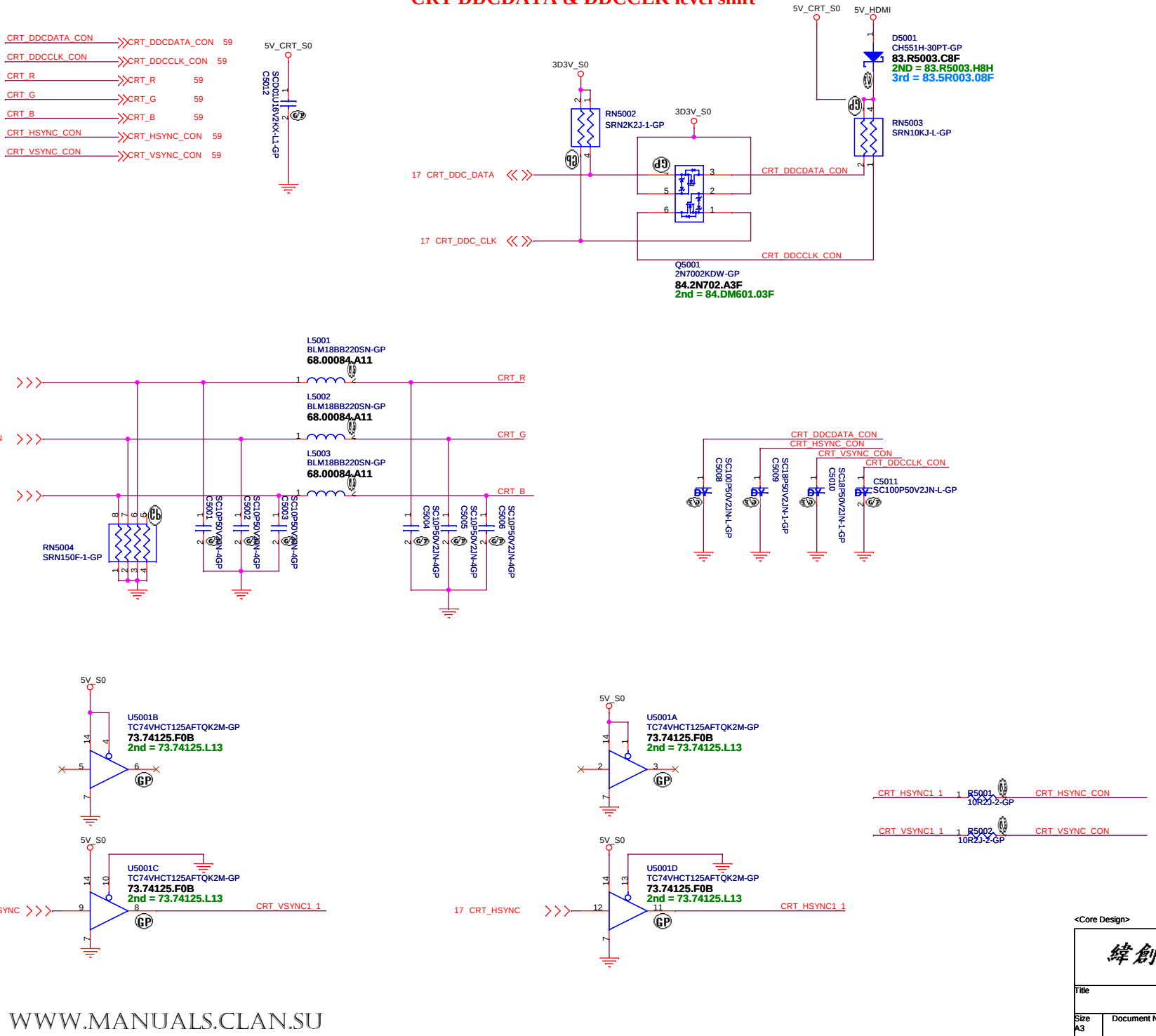
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD Connector**

Size: A2 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 49 of 103

CRT DDCDATA & DDCCLK level shift



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**		
Size: A3	Document Number: **Petra Uma**	Rev: -1
Date: Tuesday, July 10, 2012	Sheet 50 of 103	

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

Close to HDMI Connector

17 HDMI_CLK_R#
17 HDMI_CLK_R
17 HDMI_DATA0_R#
17 HDMI_DATA0_R
17 HDMI_DATA1_R#
17 HDMI_DATA1_R
17 HDMI_DATA2_R#
17 HDMI_DATA2_R

HDMI_DATA2_R#
HDMI_DATA2_R
HDMI_DATA0_R#
HDMI_DATA0_R
HDMI_DATA1_R
HDMI_DATA1_R#
HDMI_CLK_R
HDMI_CLK_R#

RN5114 SRN680J-1-GP
RN5115 SRN680J-1-GP

HDMI_PLL_GND

5V_S0

Q5105
2N7002A-7-GP

HDMI1
SKT-HDMI23-45-GP
22.10296.631

HDMI_DATA2_R
HDMI_DATA2_R#
HDMI_DATA1_R
HDMI_DATA1_R#
HDMI_DATA0_R
HDMI_DATA0_R#
HDMI_CLK_R
HDMI_CLK_R#
DDC_CLK_HDMI
DDC_DATA_HDMI
5V_HDMI

-1_20120221

5V_HDMI
5V_S0
F5101
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771

HPD_HDMI_CON
R5111 150KR2J-L1-GP
HDMI_HPD_B
R5110 200KR2J-L1-GP DY

3D3V_S0
Q5102
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.P11
3rd = 84.03904.L06
HDMI_HPD_E
R5129 0R0402-PAD
HDMI_PCH_DET 17
R5112 10KR2J-L-GP

D5103
BAW56-5-GP
83.00056.Q11
2nd = 83.00056.K11
5V_S0_D1
5V_S0_D2
5V_S0

RN5102 SRN2K2J-1-GP

Q5106
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
3D3V_S0

17 PCH_HDMI_CLK
17 PCH_HDMI_DATA
DDC_CLK_HDMI
DDC_DATA_HDMI

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector
Size: A3
Document Number: Petra Uma
Rev: -1
Date: Tuesday, July 10, 2012
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LED BACKLIGHT CONVERTER POWER

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*		
Size: A4	Document Number: Petra Uma	Rev: -1
Date: Wednesday, February 22, 2012	Sheet 52 of 103	

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	**Petra Uma**	**-1**

Date: Wednesday, February 22, 2012 Sheet 53 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

Size	Document Number	Rev
A4	**Petra Uma**	-1

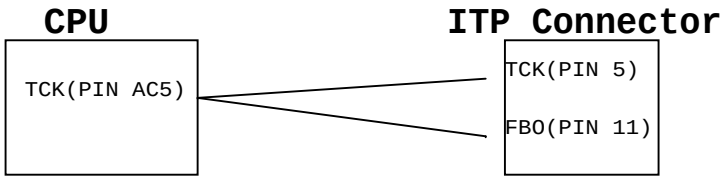
Date: Wednesday, February 22, 2012 Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max), others place near CPU side.

(Blanking)



<Core Design>

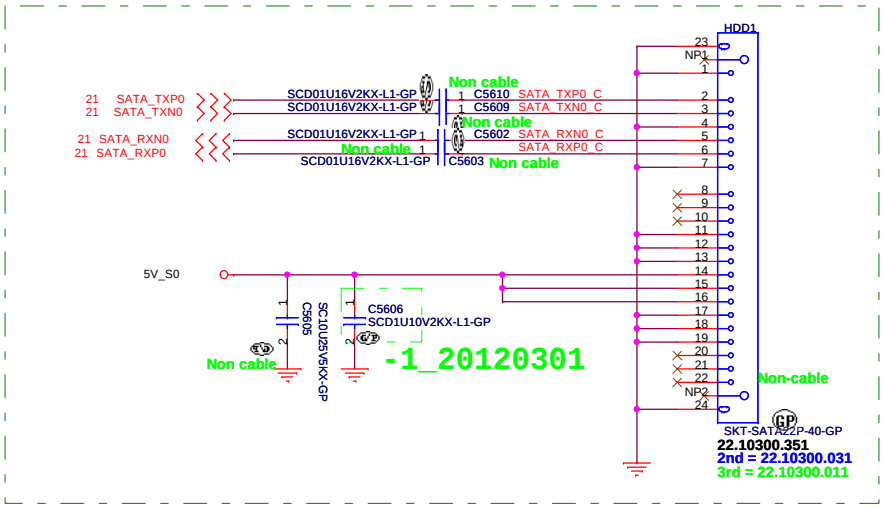
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

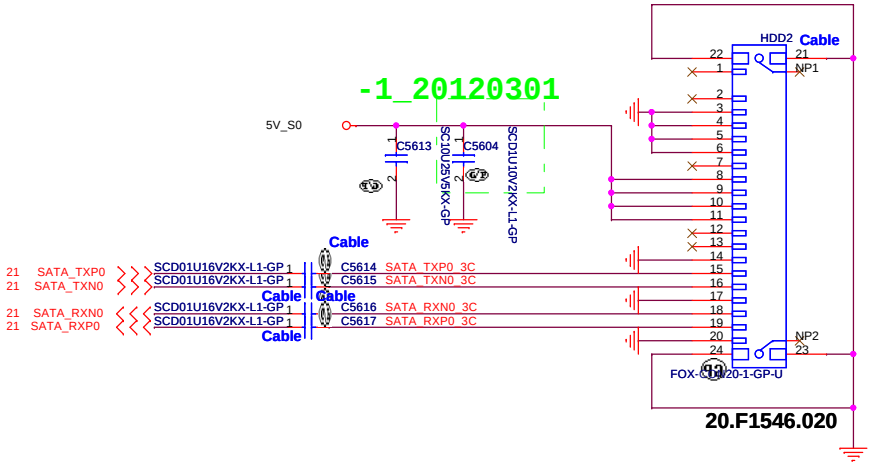
Title: ITP		
Size: A4	Document Number: Petra Uma	Rev: -1
Date: Wednesday, February 22, 2012	Sheet 55 of 103	

SSID = SATA

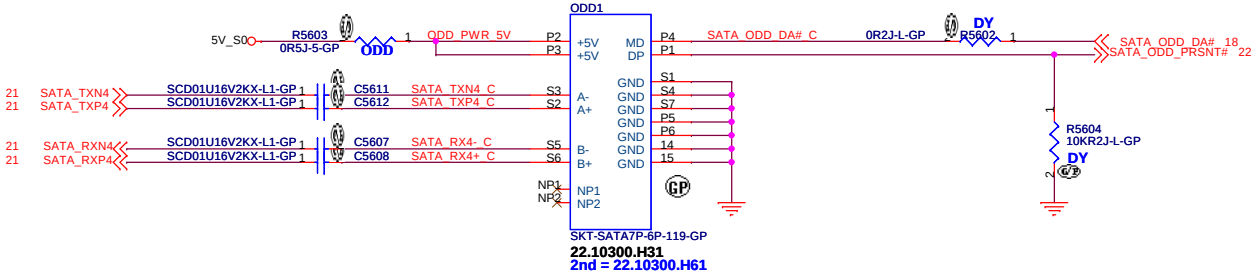
-1_20120223

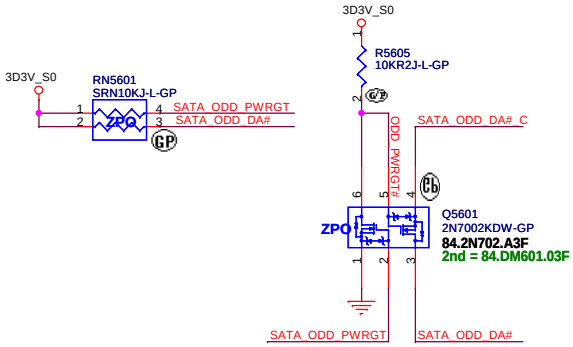
SATA HDD Connector



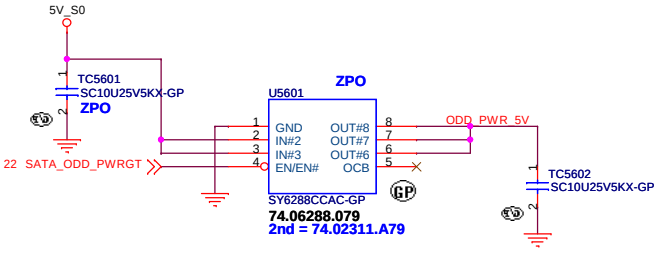


ODD Connector





SATA Zero Power ODD



High Active 2A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 56 of 103

ESATA Power

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<Core Design>

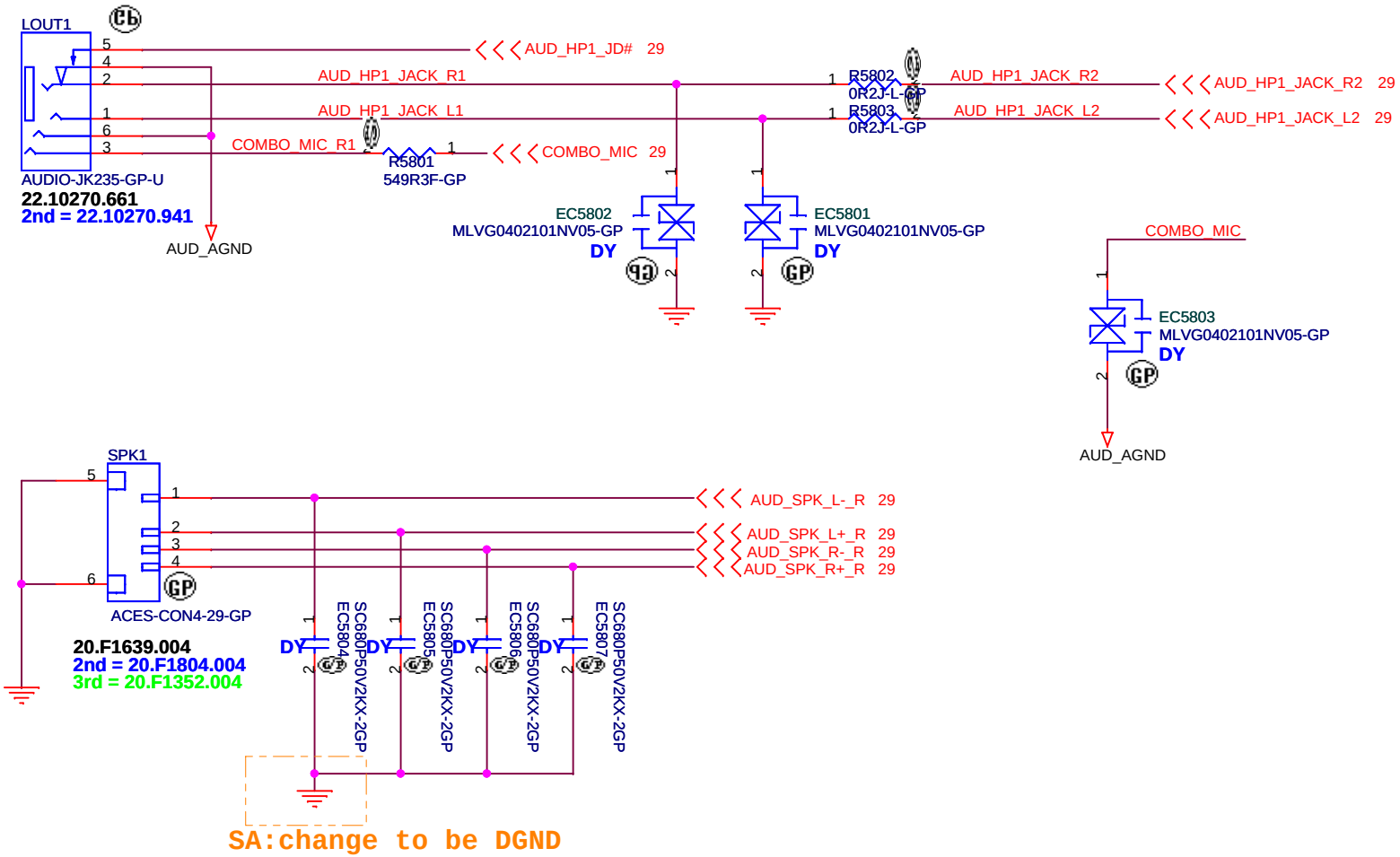
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: E-SATA/USB CHARGER

Size	Document Number	Rev
A4	Petra Uma	-1

Date: Wednesday, February 22, 2012 Sheet 57 of 103

SSID = AUDIO



<Core Design>

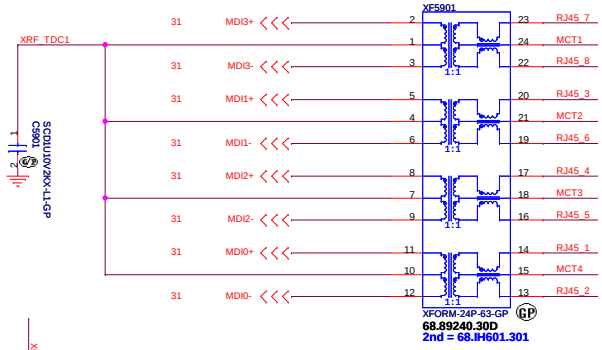
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

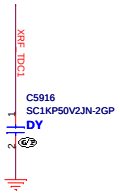
Title: ***Audio Jack***

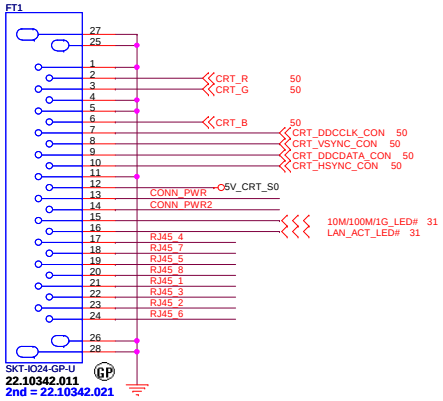
Size	Document Number	Rev
A4	Petra Uma	-1

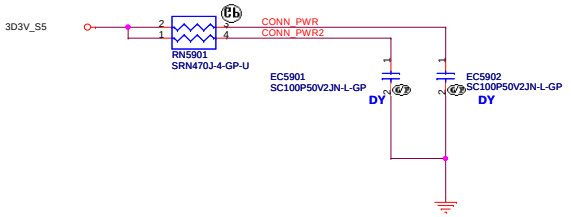
Date: Tuesday, July 10, 2012 Sheet 58 of 103

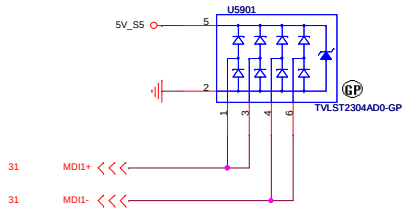
SSID = LAN

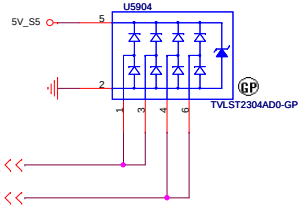


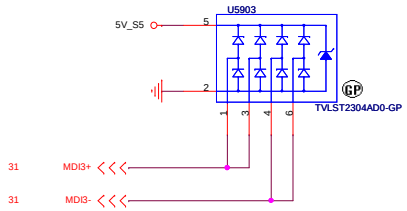


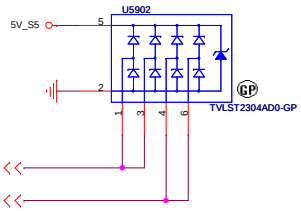


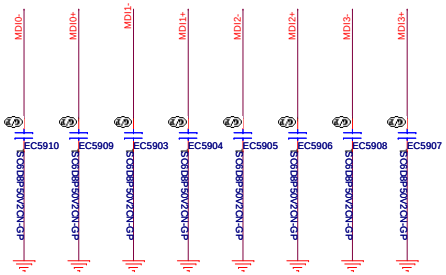


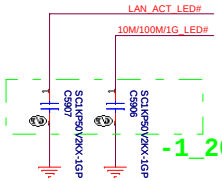




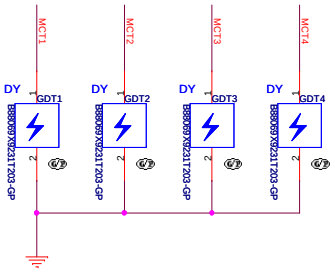


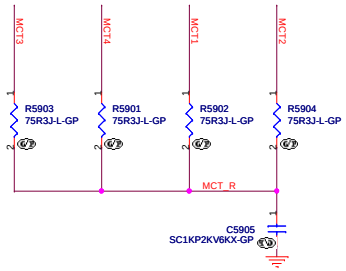






-1_20120301





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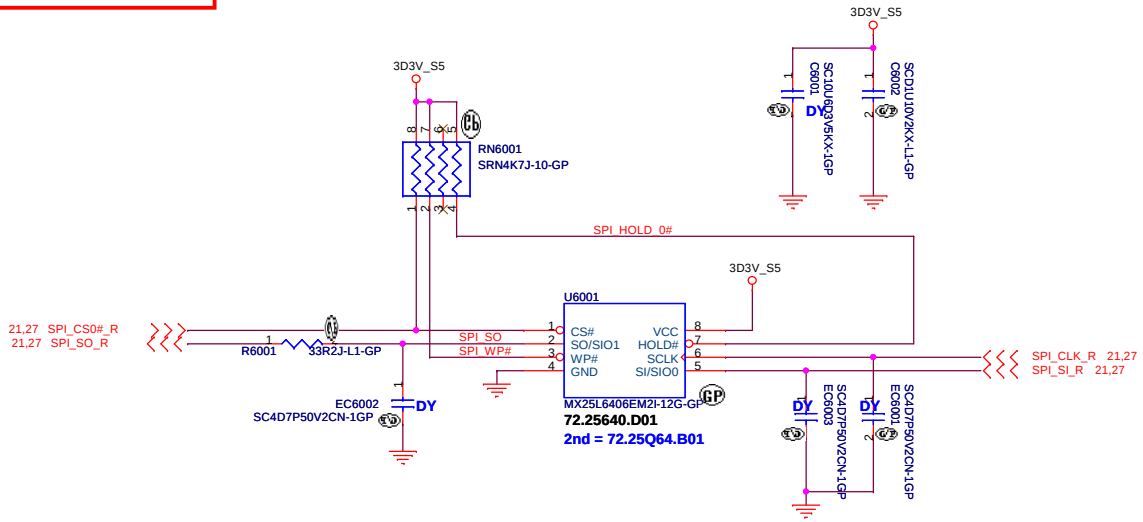
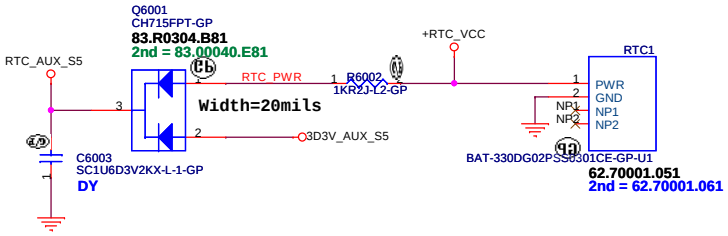
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LAN CONNECTOR***	
Size: Custom	Document Number: **Petra Uma**	Rev: **-1**
Date: Tuesday, July 10, 2012	Sheet 59 of 103	

SSID = Flash.ROM



SSID = RTC



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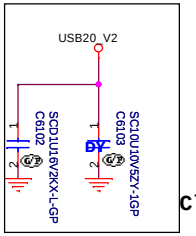
Title: Flash/RTC

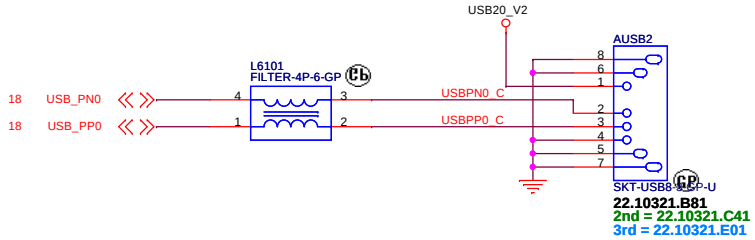
Size: Custom | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 60 of 103

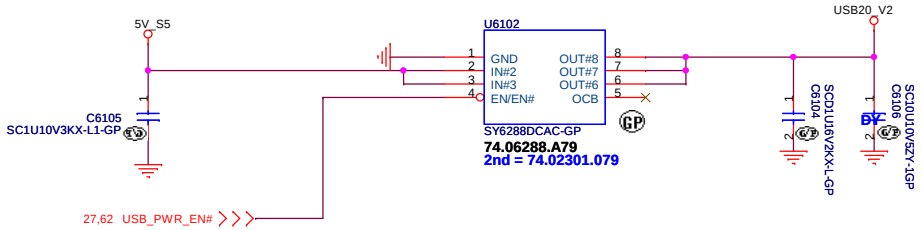
SSID = USB

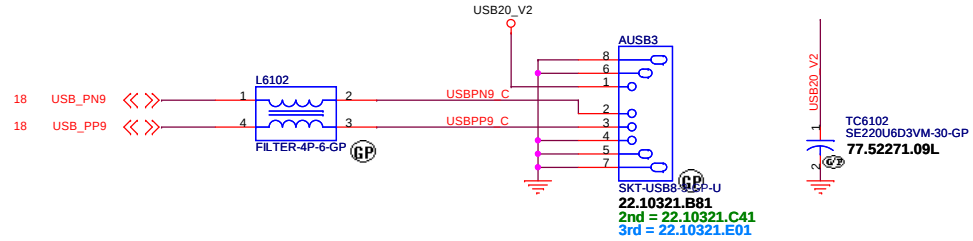


Close to AUSB2



Low Active 2A





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緯創資通 Wistron Corporation
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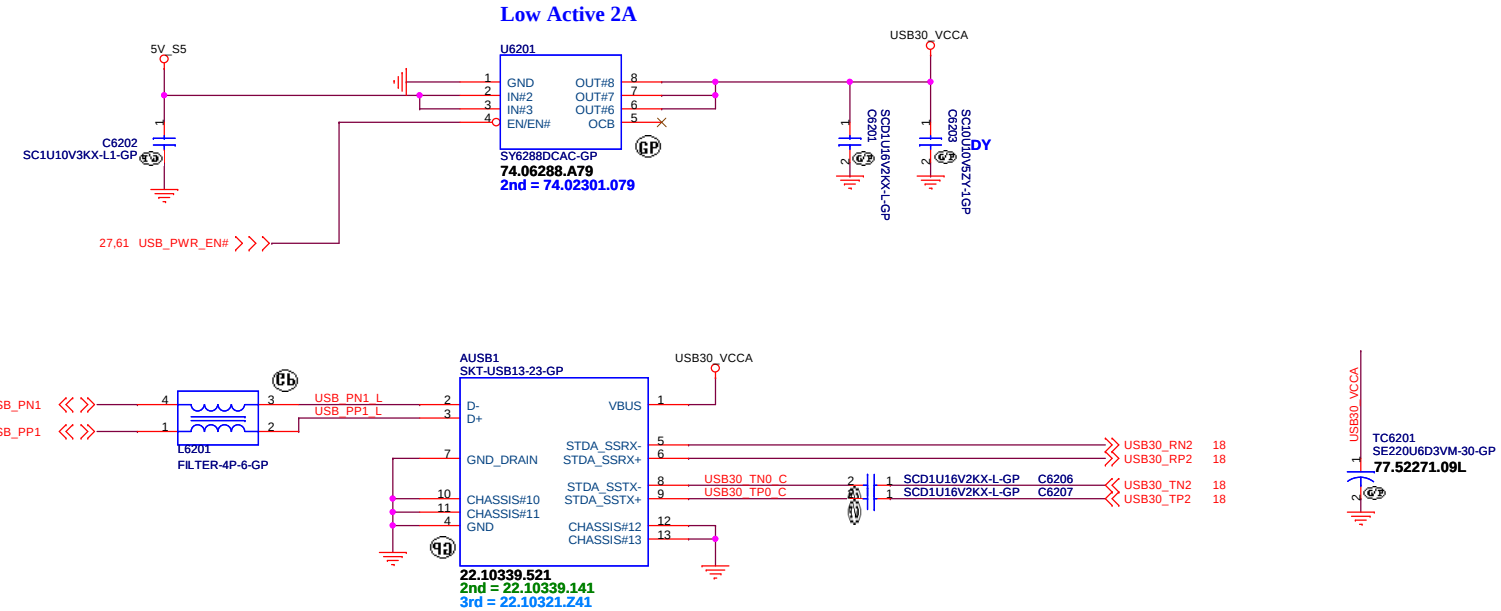
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Power SW**

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 61 of 103



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

<Core Design>

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Title: USB 3.0 Port

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 62 of 103

SSID = User.Interface

Bluetooth Module conn.

ANNIE Bluetooth Module

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Bluetooth***

Size	Document Number	Rev
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Date: Wednesday, February 22, 2012 Sheet 63 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

Size	Document Number	Rev
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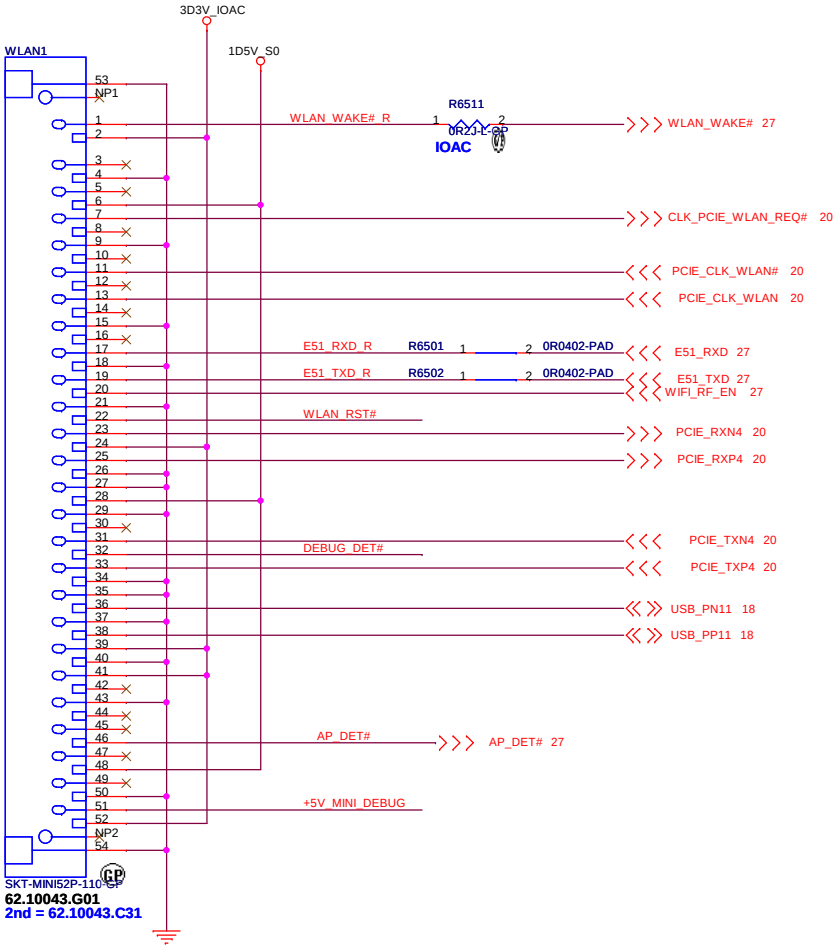
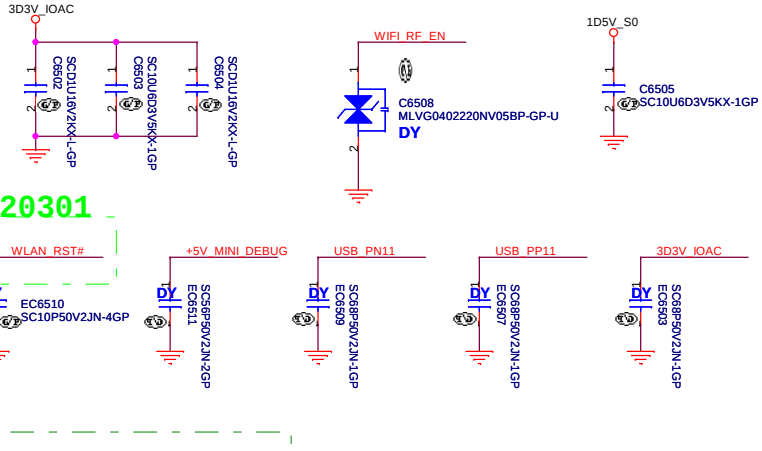
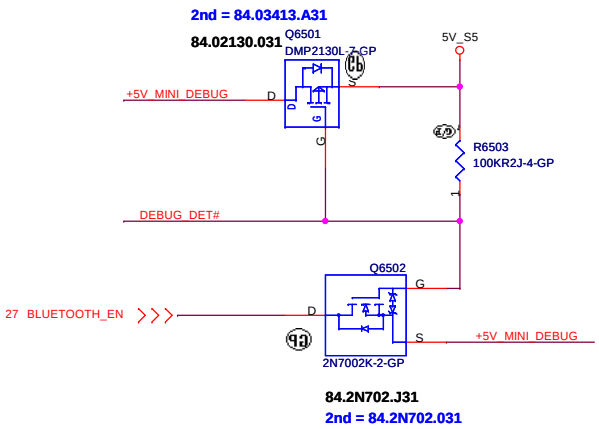
Date: Wednesday, February 22, 2012 Sheet 64 of 103

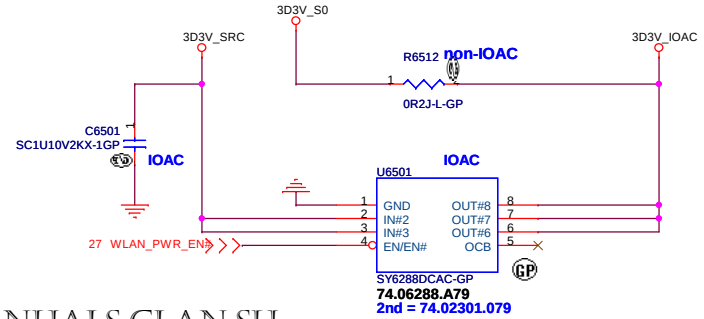
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: MINICARD(WLAN)/ITP CONN

Size: A3 | Document Number: Petra Uma | Rev: -1

Date: Tuesday, July 10, 2012 | Sheet 65 of 103

SSID = Wireless

Mini Card Connector(WWAN)

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<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***WWAN Connector***	
Size A4	Document Number **Petra Uma**	Rev **-1**
Date: Wednesday, February 22, 2012	Sheet 66 of 103	

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<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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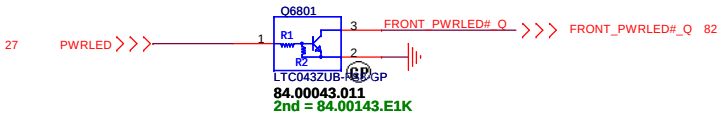
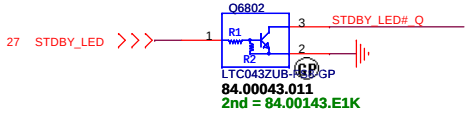
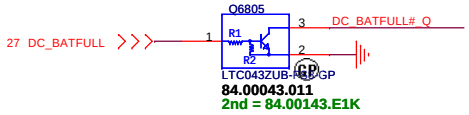
Power button LED



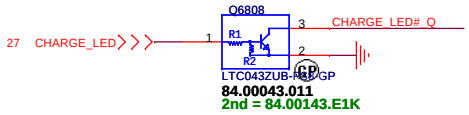
Power STDBY_LED

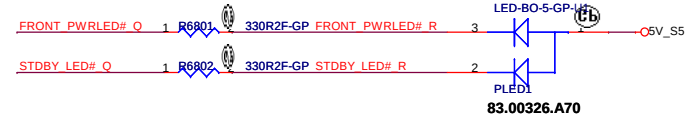


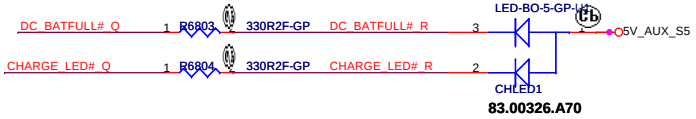
Battery LED2(DC_BATFULL)

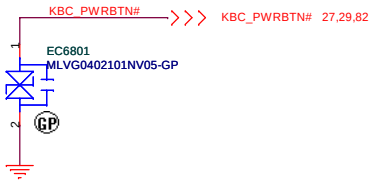


Battery LED1(CHARGE)









<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	***LED Bard/Power Button***	
Size: Custom	Document Number: **Petra Uma**	Rev: **-1**
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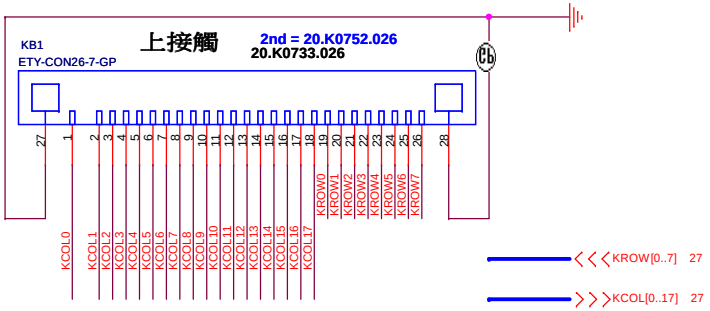
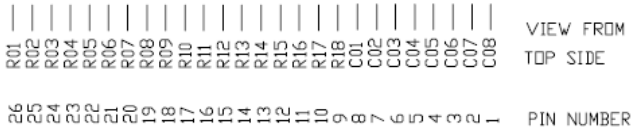
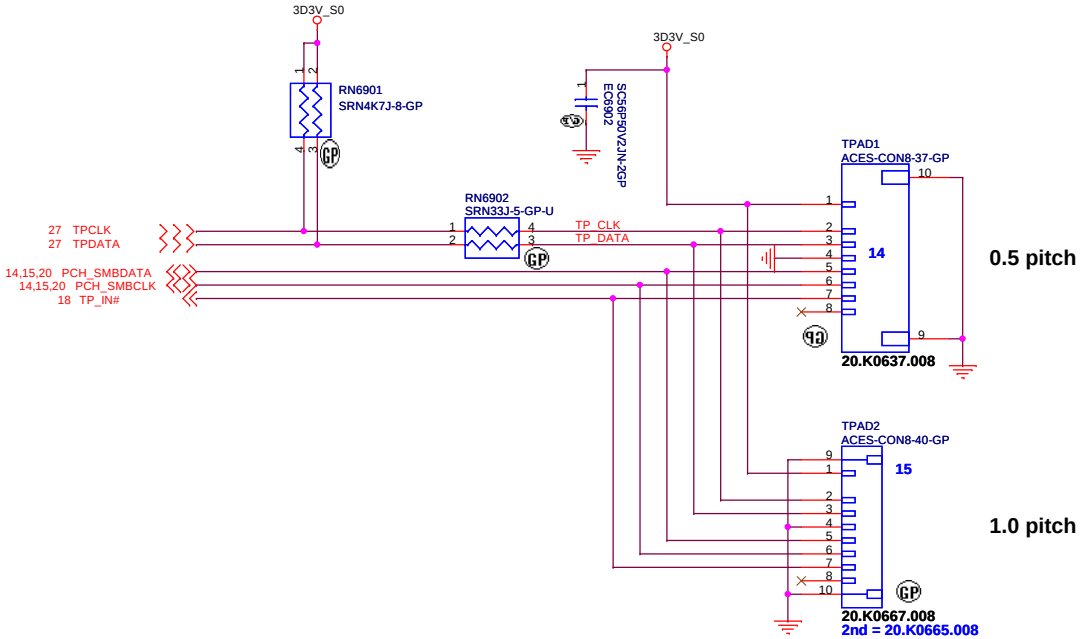
SSID = KBC

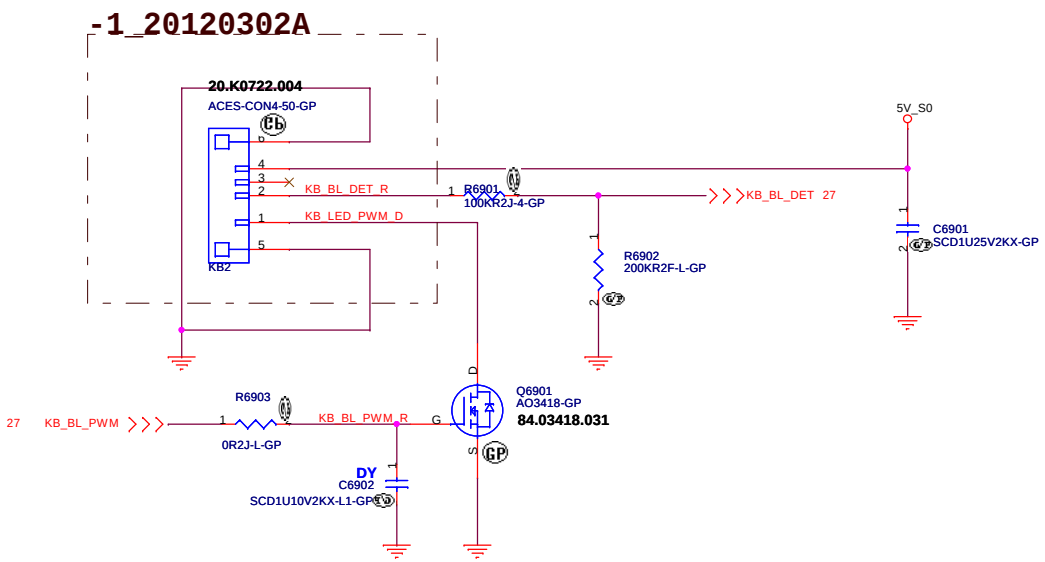
Internal KeyBoard Connector





TOUCH PAD





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
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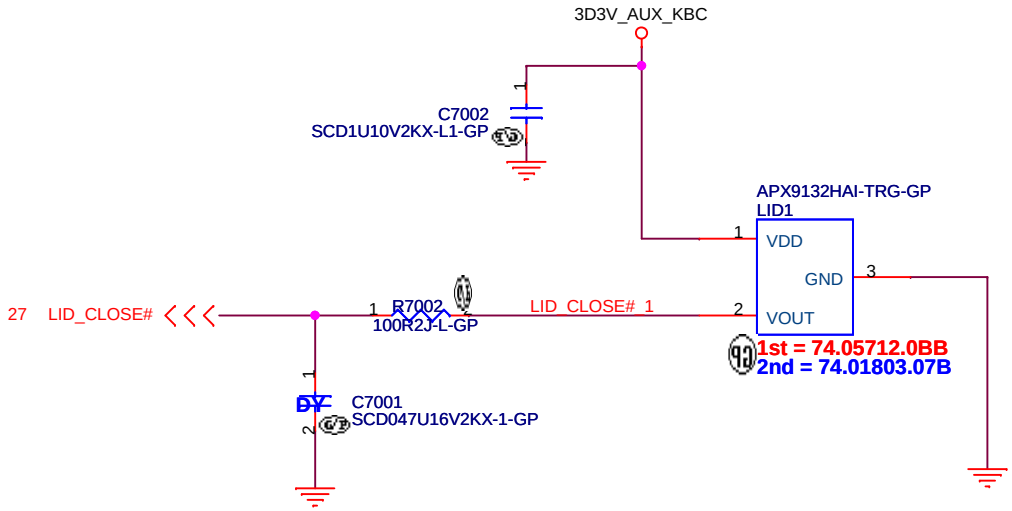

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	**Petra Uma**	**-1**

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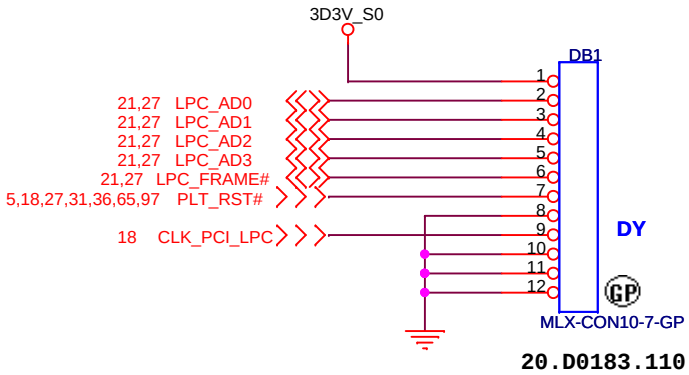

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**Petra Uma**	**-1**

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

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A4	**Petra Uma**	**-1**

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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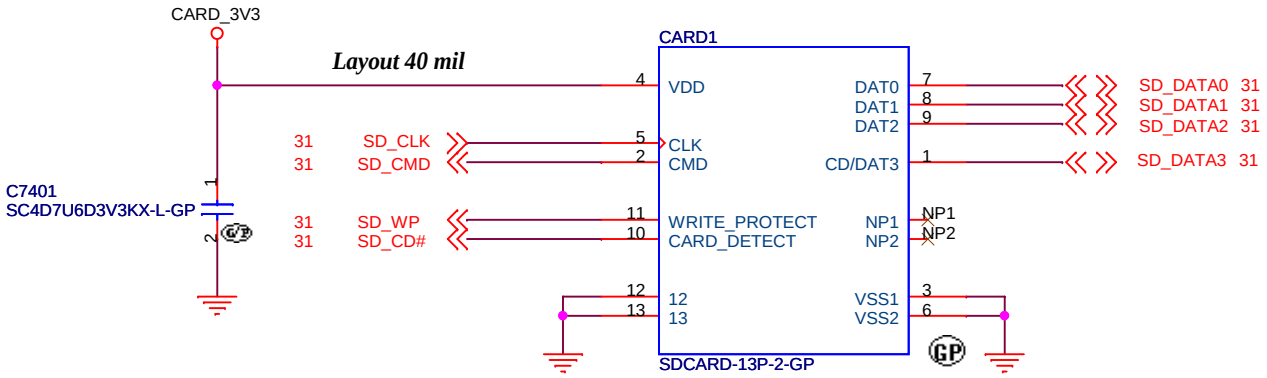
Title: ***Reserved***

Size	Document Number	Rev
A4	**Petra Uma**	-1

Date: Wednesday, February 22, 2012 Sheet 73 of 103

SSID = SDIO

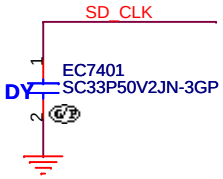
SD/MMC Card Reader



62.10051.C41

2nd = 62.10051.D71

BCM57765/BCM57785 Pin Number	*Signal Name*	*SD/MMC Interface*	*MS-Pro Interface*	*xD Interface*
21	CR_CLK/RY_BY#	CR_CLK	MS_CLK	RY_BY#
26	CR_CMD/CLE	CR_CMD	MS_BS	CLE
25	CR_DATA0	CR_DATA0	MS_DATA0	XD_DATA0
24	CR_DATA1	CR_DATA1	MS_DATA1	XD_DATA1
23	CR_DATA2	CR_DATA2	MS_DATA2	XD_DATA2
22	CR_DATA3	CR_DATA3	MS_DATA3	XD_DATA3
52	CR_DATA4	CR_DATA4	MS_DATA4	XD_DATA4
53	CR_DATA5	CR_DATA5	MS_DATA5	XD_DATA5
54	CR_DATA6	CR_DATA6	MS_DATA6	XD_DATA6
55	CR_DATA7	CR_DATA7	MS_DATA7	XD_DATA7
60	ALE	–	–	ALE
1	SD_DETECT/WE#	CR_DETECT	–	WE#
9	RE#	–	–	RE#
59	CE#/MS_INS#	–	MS_INS#	CE#
57	CR_WP#/XD_WP#	SD_WP#	–	WP#
68	XD_DETECT	–	–	XD_DETECT



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
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SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***New Card***

Size	Document Number	Rev
A4	**Petra Uma**	-1

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Petra Uma**	**-1**

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<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

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SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G- Sensor***

Size	Document Number	Rev
A4	**Petra Uma**	-1

Date: Wednesday, February 22, 2012 Sheet 79 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**Petra Uma**	-1

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Title: ***Reserved***

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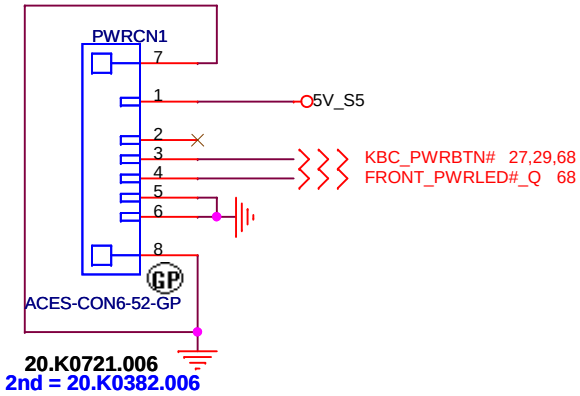

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

Size	Document Number	Rev
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size	Document Number	Rev
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緯創資通 Wistron Corporation
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Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
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<Core Design>

緯創資通 Wistron Corporation
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Title: RT8208F_+VGA_CORE

Size	Document Number	Rev
A4	Petra Uma	-1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: DISCRETE VGA POWER

Size	Document Number	Rev
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LVDS Channel A

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Panel BL brightness/Power En/BL En

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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS_Switch

Size: A4 | Document Number: Petra Uma | Rev: -1

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<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CRT_Switch***
Size: A4	Document Number: **Petra Uma**
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Date: Wednesday, February 22, 2012	Sheet 95 of 103

SSID = SDIO

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<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***TOUCH PANEL***	
Size A4	Document Number **Petra Uma**	Rev **-1**
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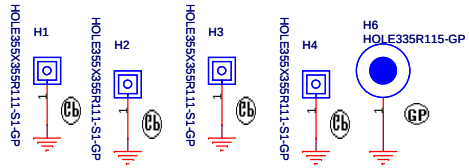

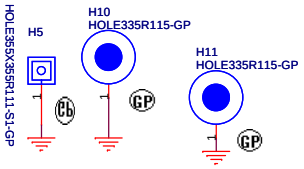

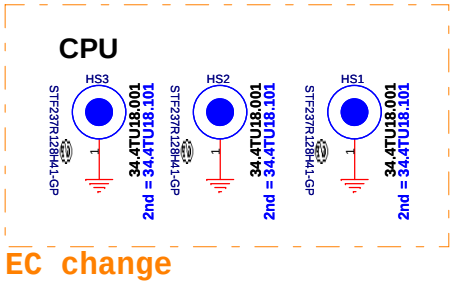

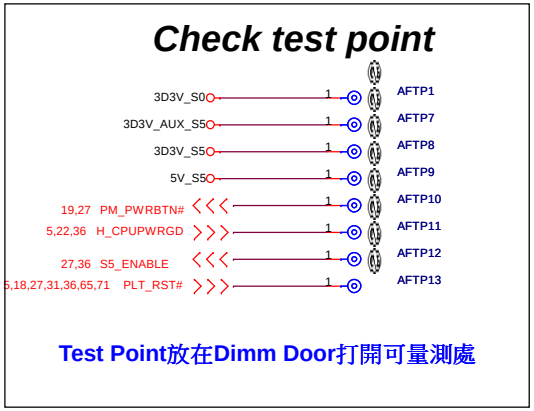

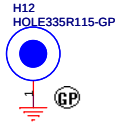

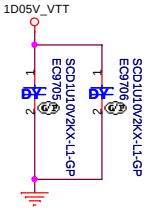

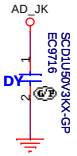

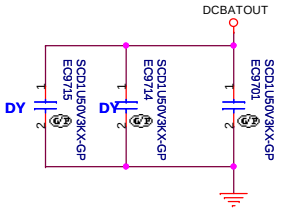

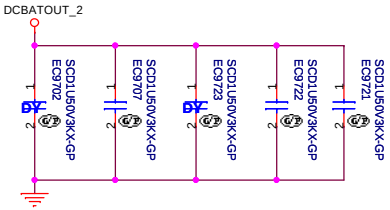

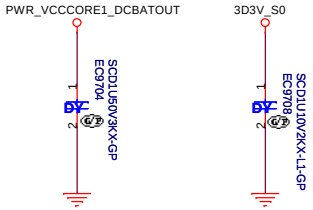

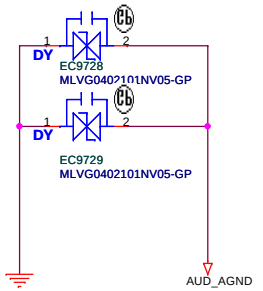

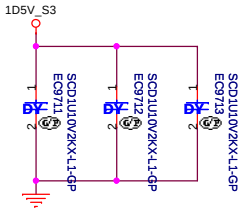

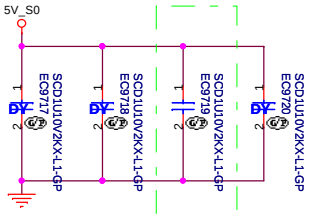

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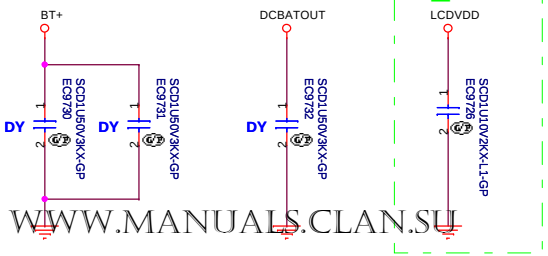

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Title: UNUSED PARTS/EMI Capacitors

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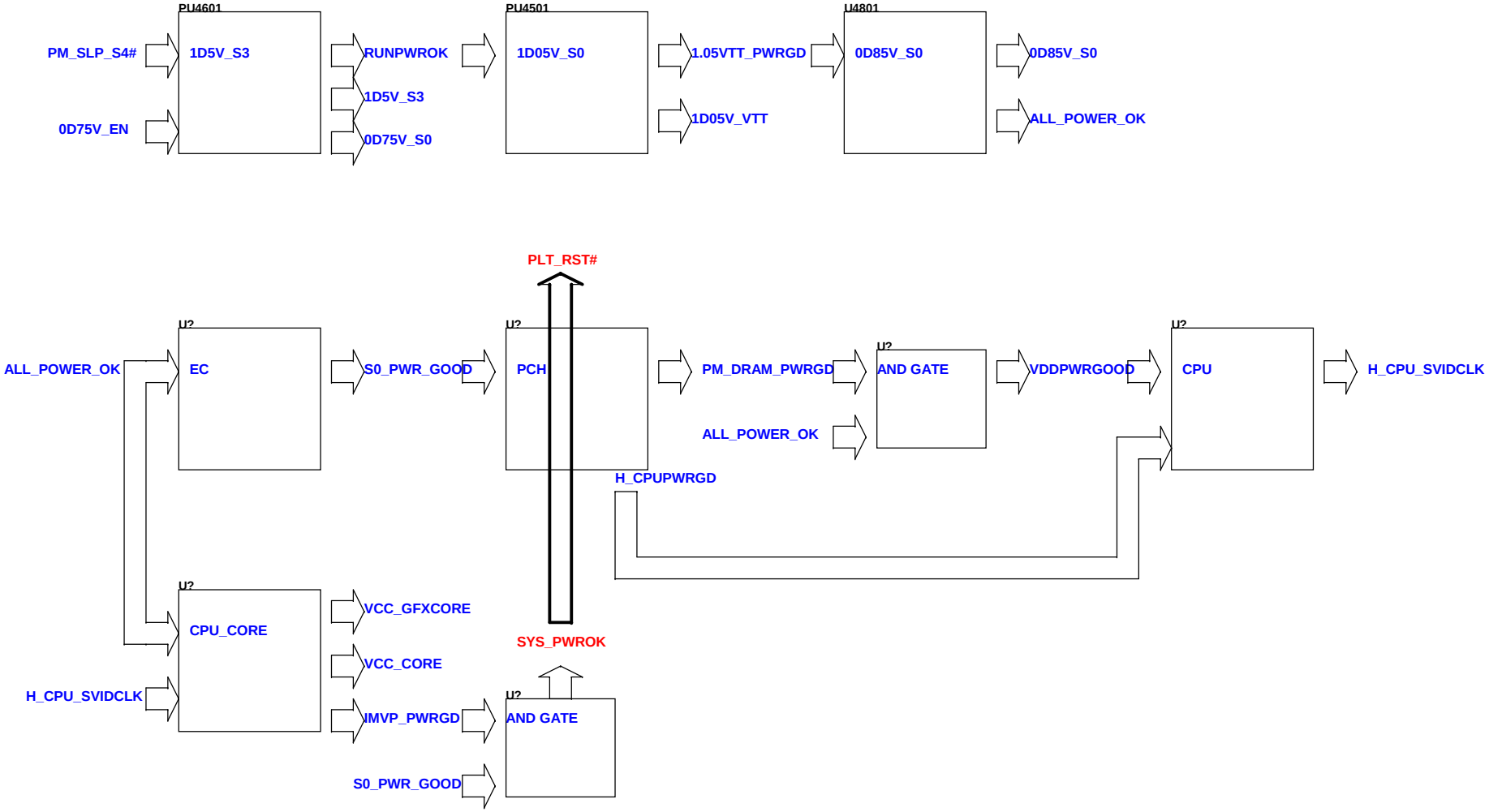
Power Sequence



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Title: Change History

Size: A3 | Document Number: Petra Uma | Rev: -1

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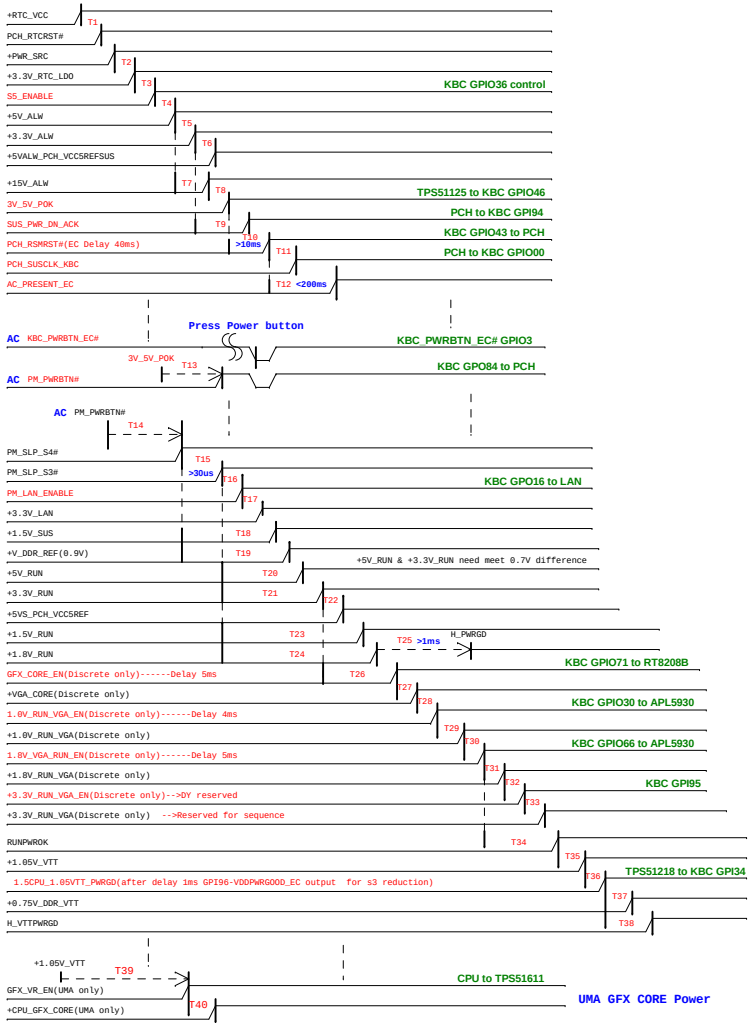
Intel-Power Up Sequence

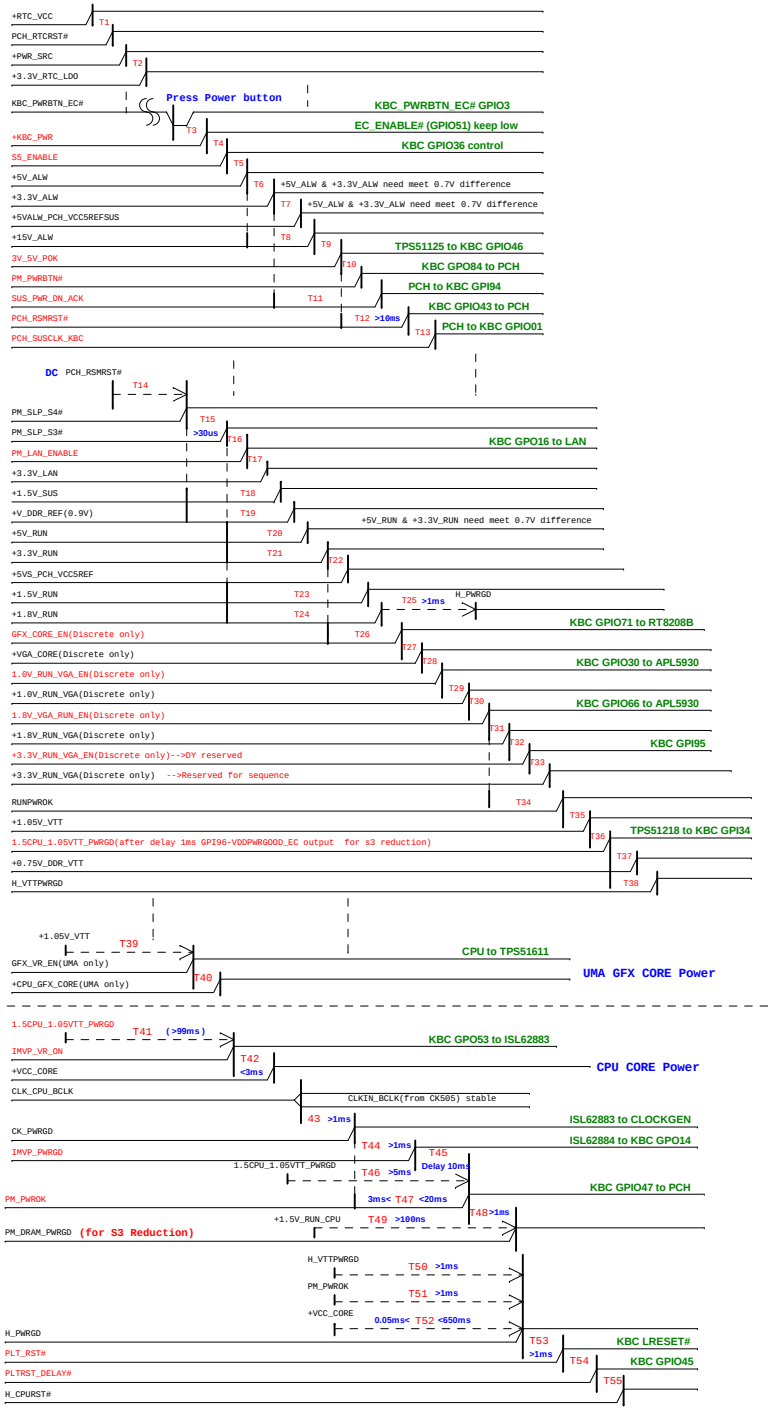
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



<Core Design>
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Title: Power Sequence
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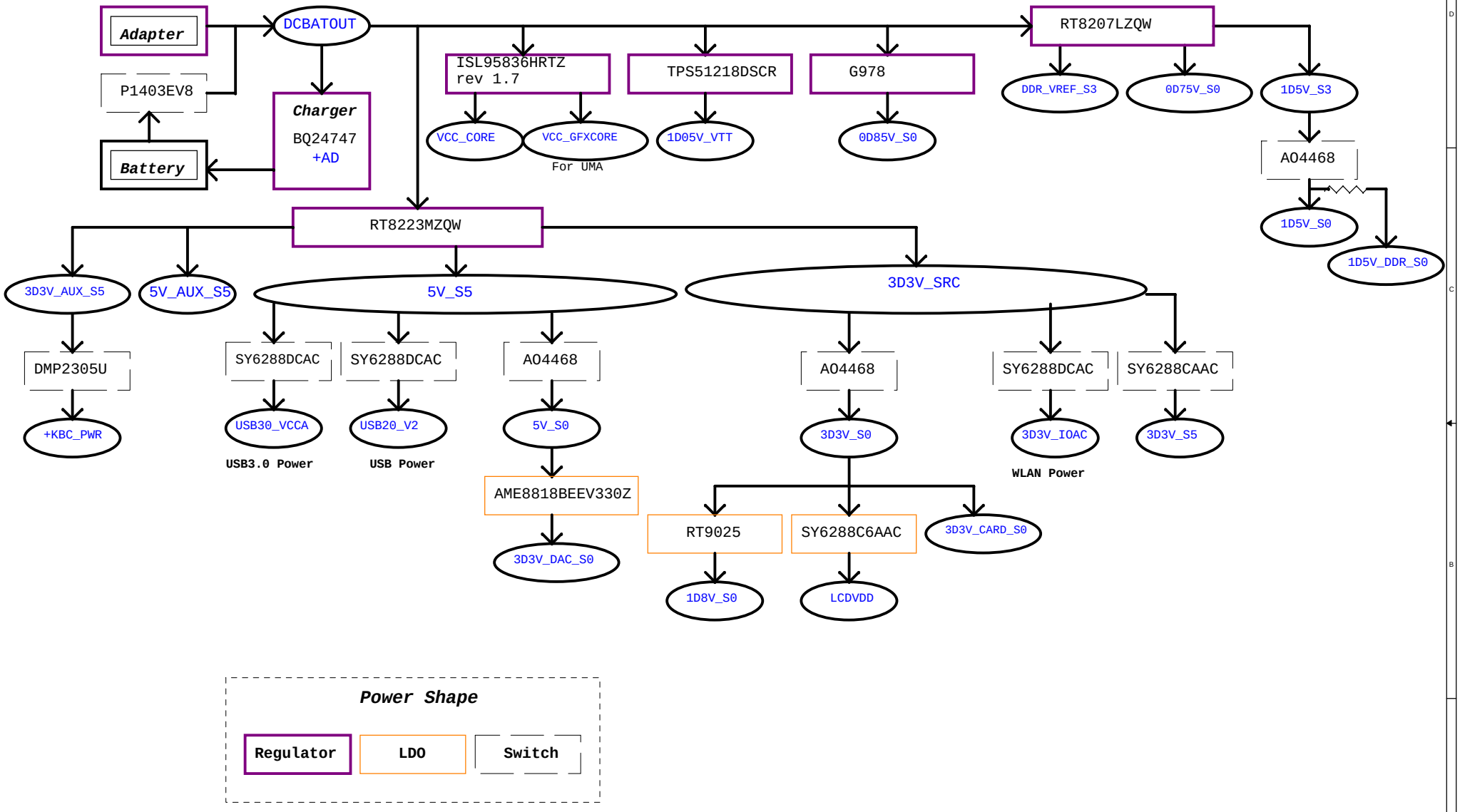

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Title: Power Block Diagram

Size: A3 | Document Number: Petra Uma | Rev: -1

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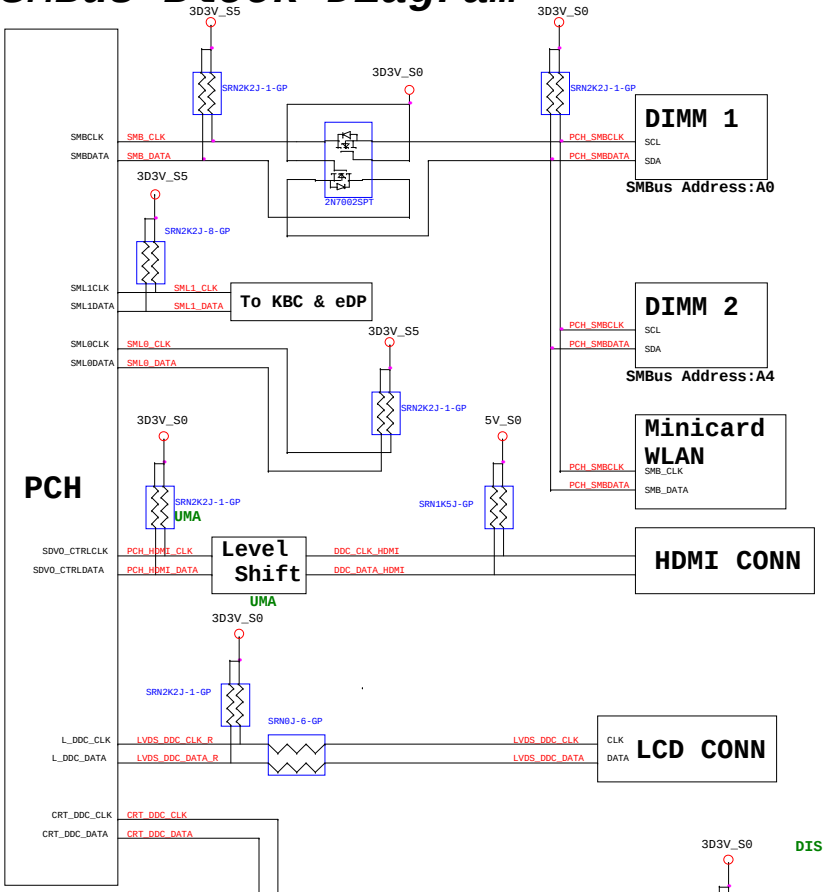
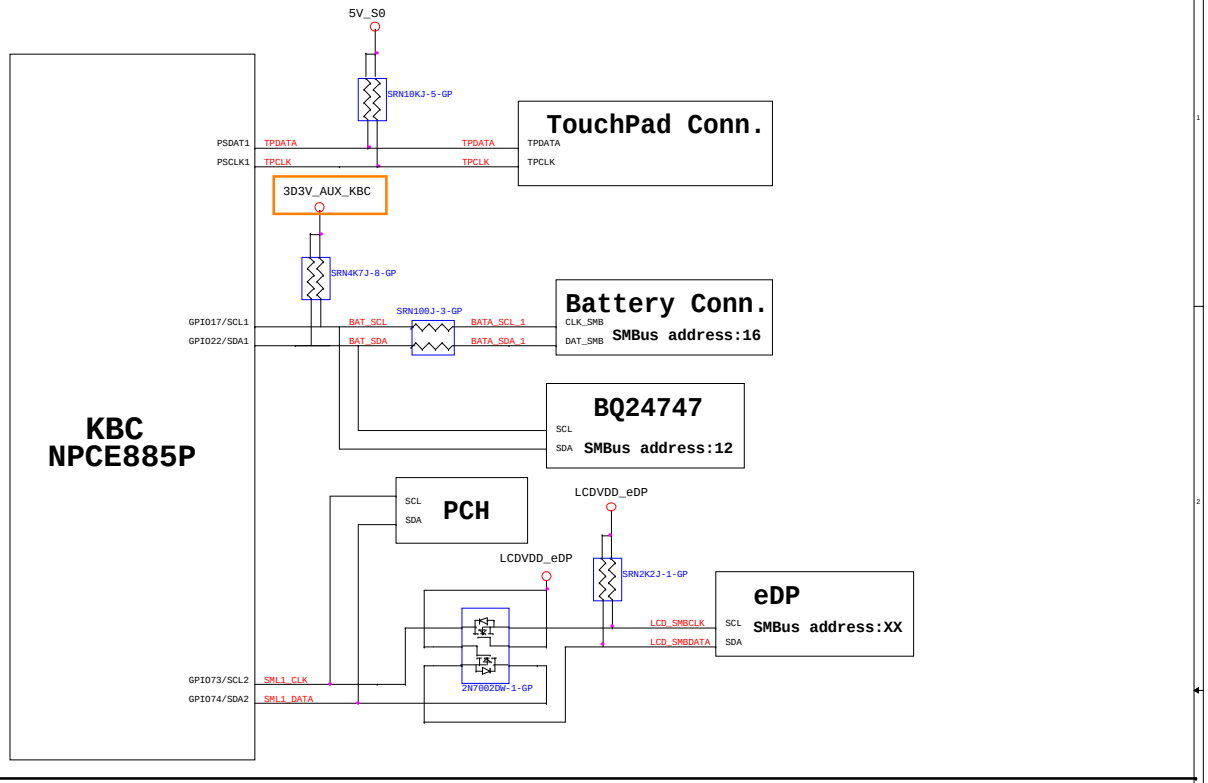
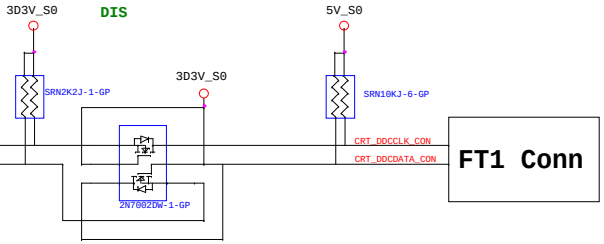
PCH SMBus Block Diagram



KBC SMBus Block Diagram





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Title: SMBUS Block Diagram
Size: A2
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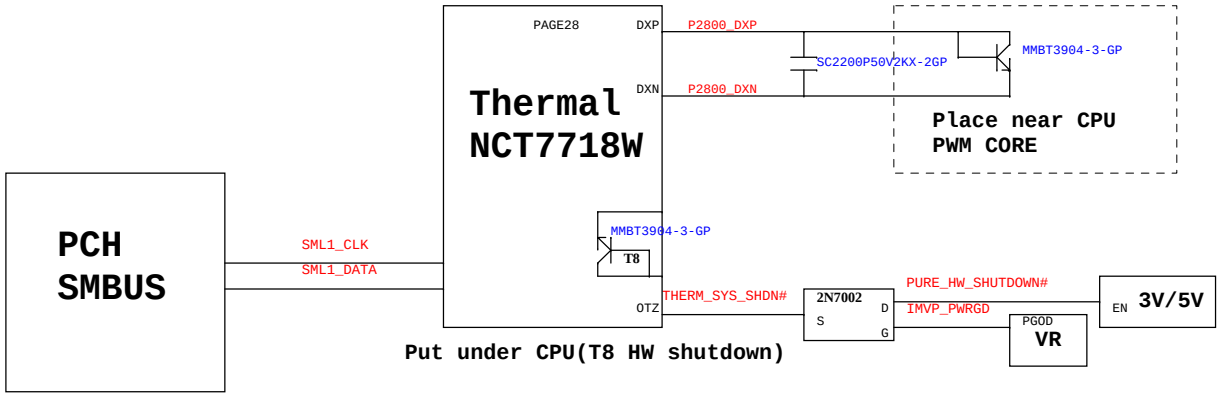
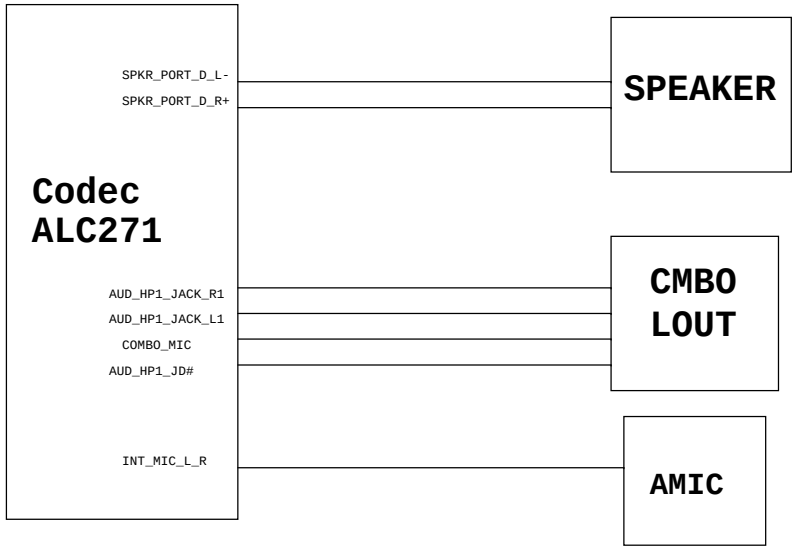
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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Title
USB charger

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