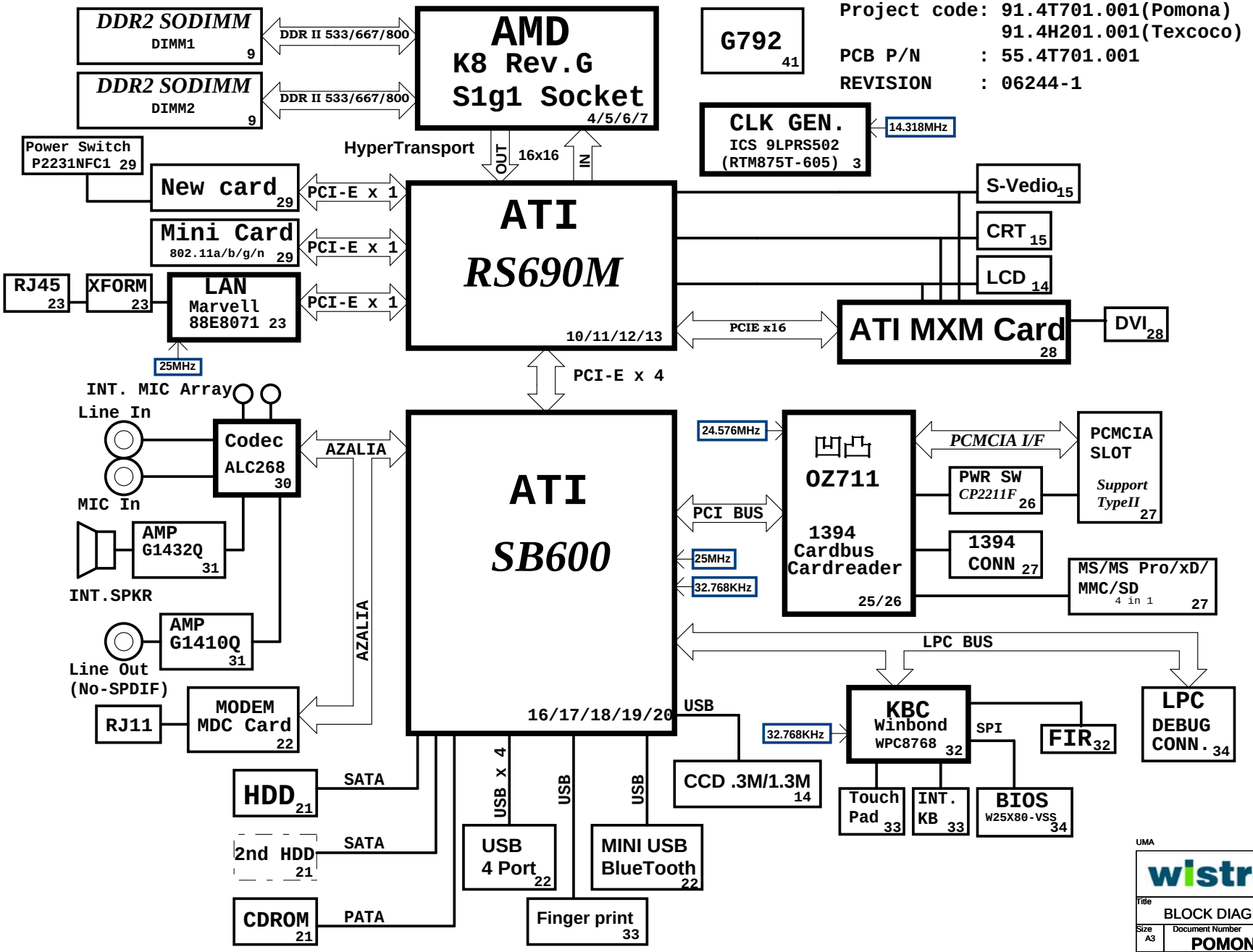
Pomona/Texcoco Block Diagram

Ver. -1



PCB Layer Stackup

- L1: Signal 1
- L2: VCC
- L3: Inner Signal 2
- L4: Inner Signal 3
- L5: GND
- L6: Signal 4

CPU V_CORE — ISL6264 38/39

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC — TPS51124 47

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC — ISL6236 46

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO — TPS51100 48

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO — APL5915 48

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO — ISL6236 46

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger — ISL6255 42

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

UMA

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BLOCK DIAGRAM

Size: A3 | Document Number: POMONA/TEXCOCO | Rev: 1

Date: Thursday, March 29, 2007 | Sheet 1 of 49

SA: 07/31/06 Start

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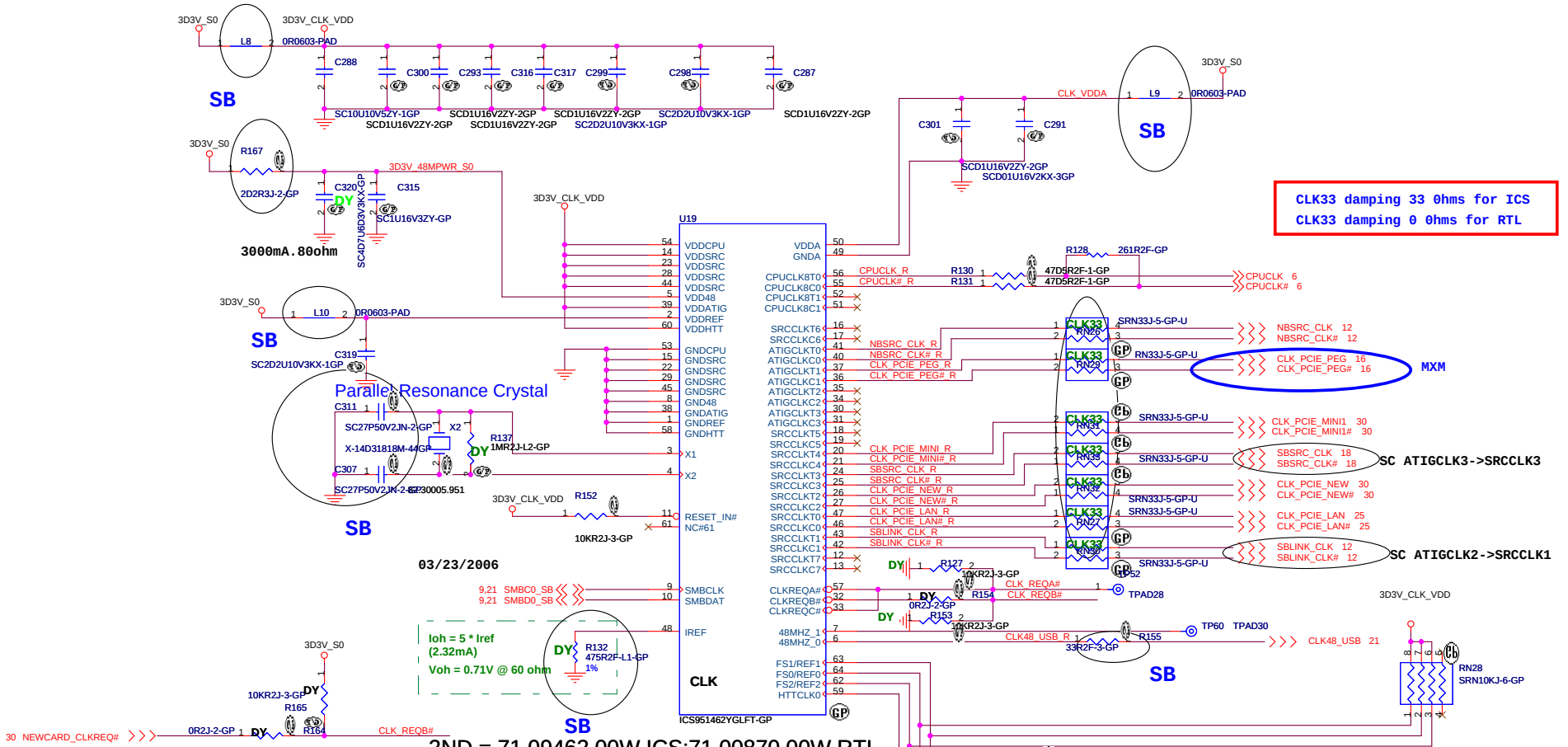
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHANGE HISTORY**

Size	Document Number	Rev
A3	**Pomona/Texcoco**	1

Date: Thursday, March 29, 2007 Sheet 2 of 49



CLK33 damping 33 0hms for ICS
CLK33 damping 0 0hms for RTL

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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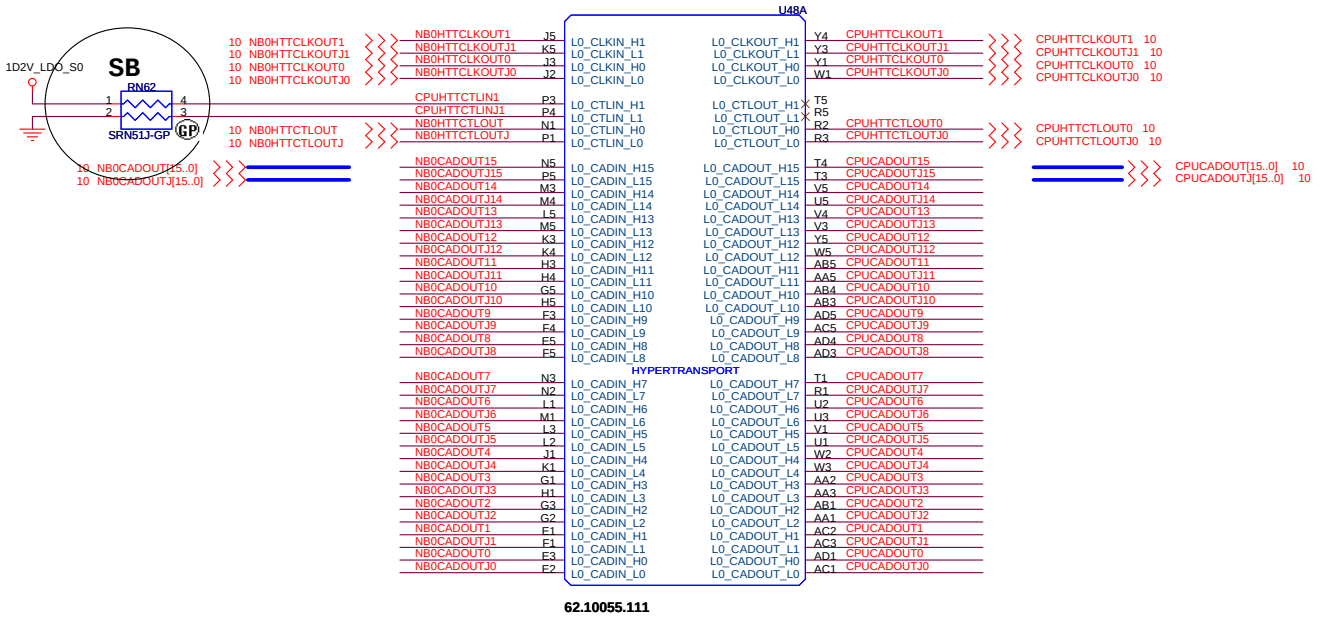
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS951462

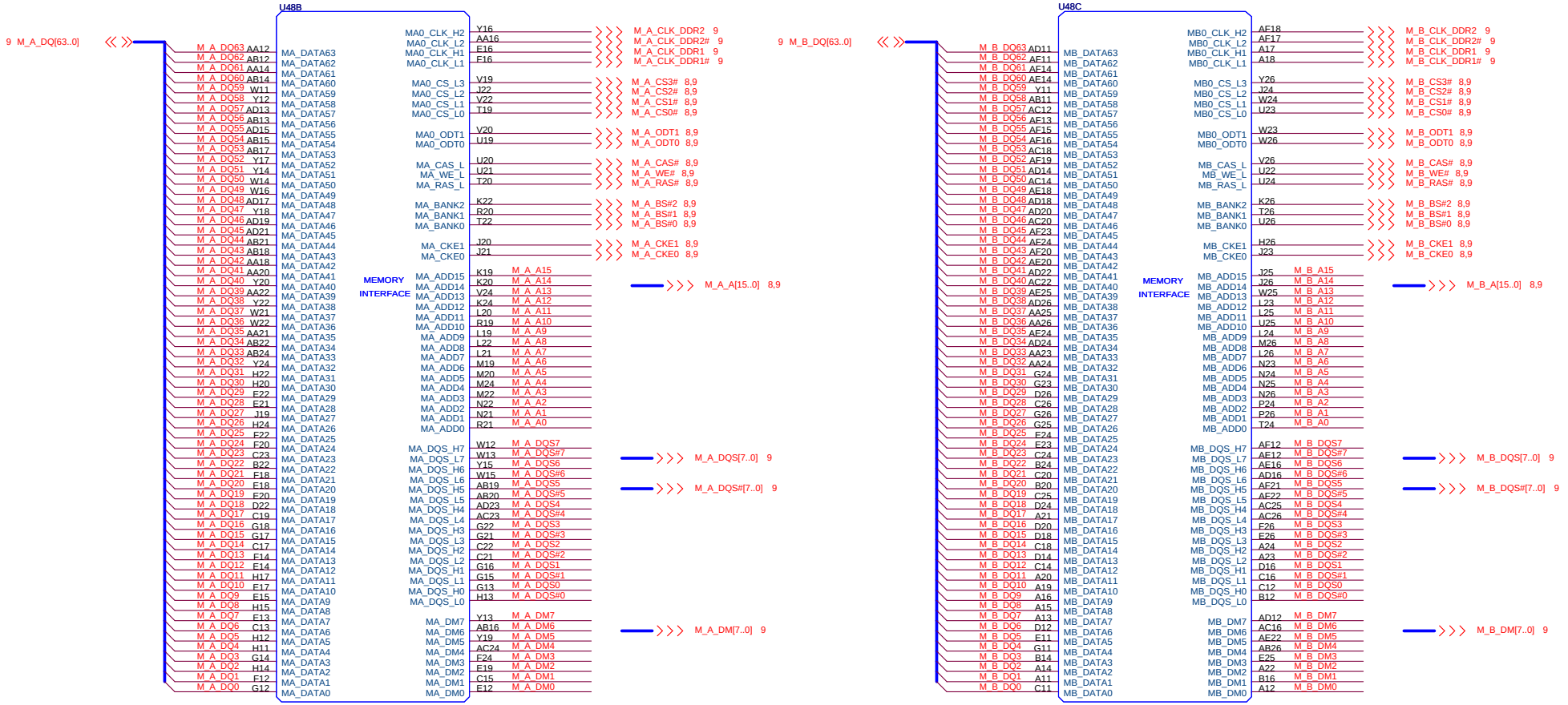
Size: A3 | Document Number: Pomona/Texcoco | Rev: 1

Date: Thursday, March 29, 2007 | Sheet 3 of 49



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU(1/4)_HyperTransport I/F***	
Size A3	Document Number **Pomona/Texcoco**	Rev 1
Date: Thursday, March 29, 2007	Sheet 4 of 49	



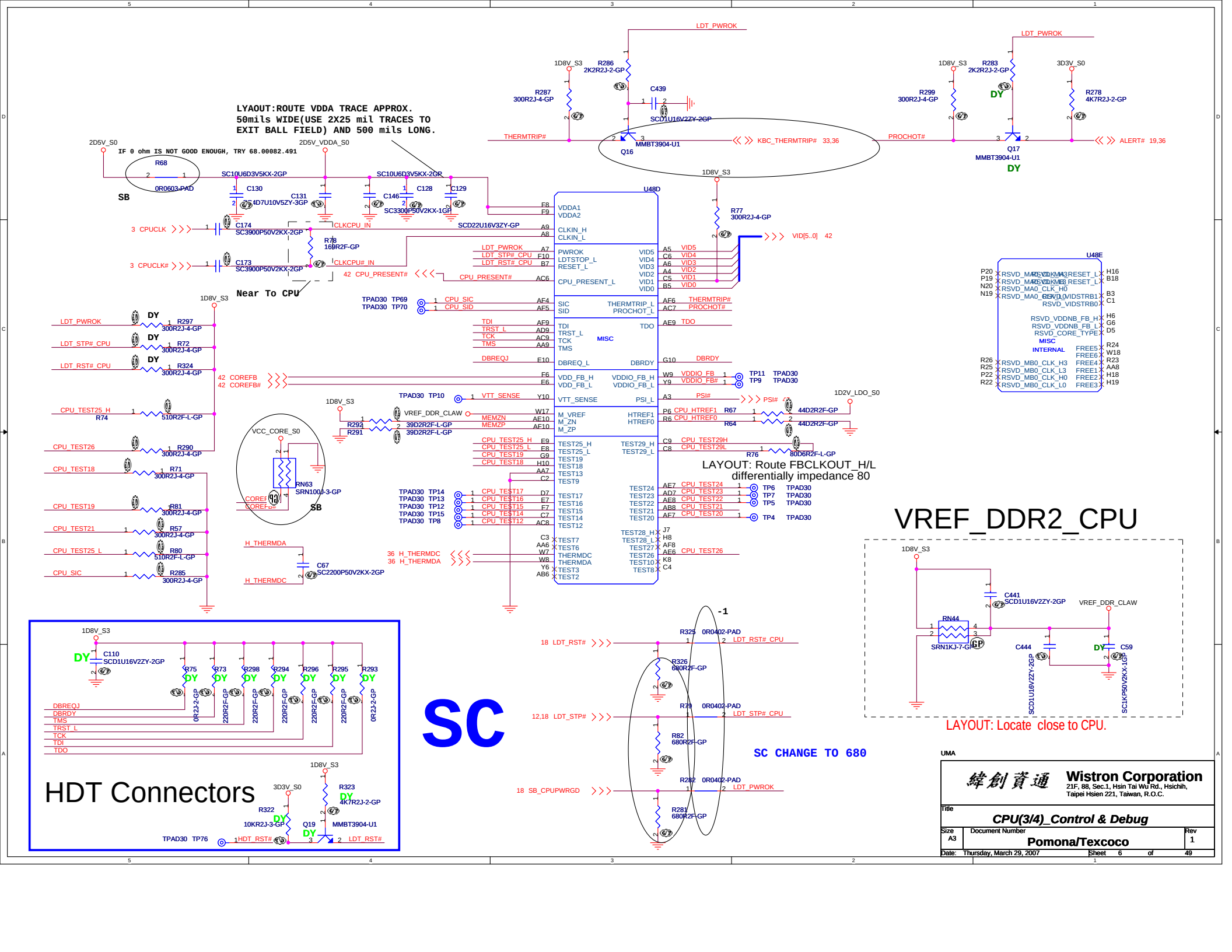
UMA

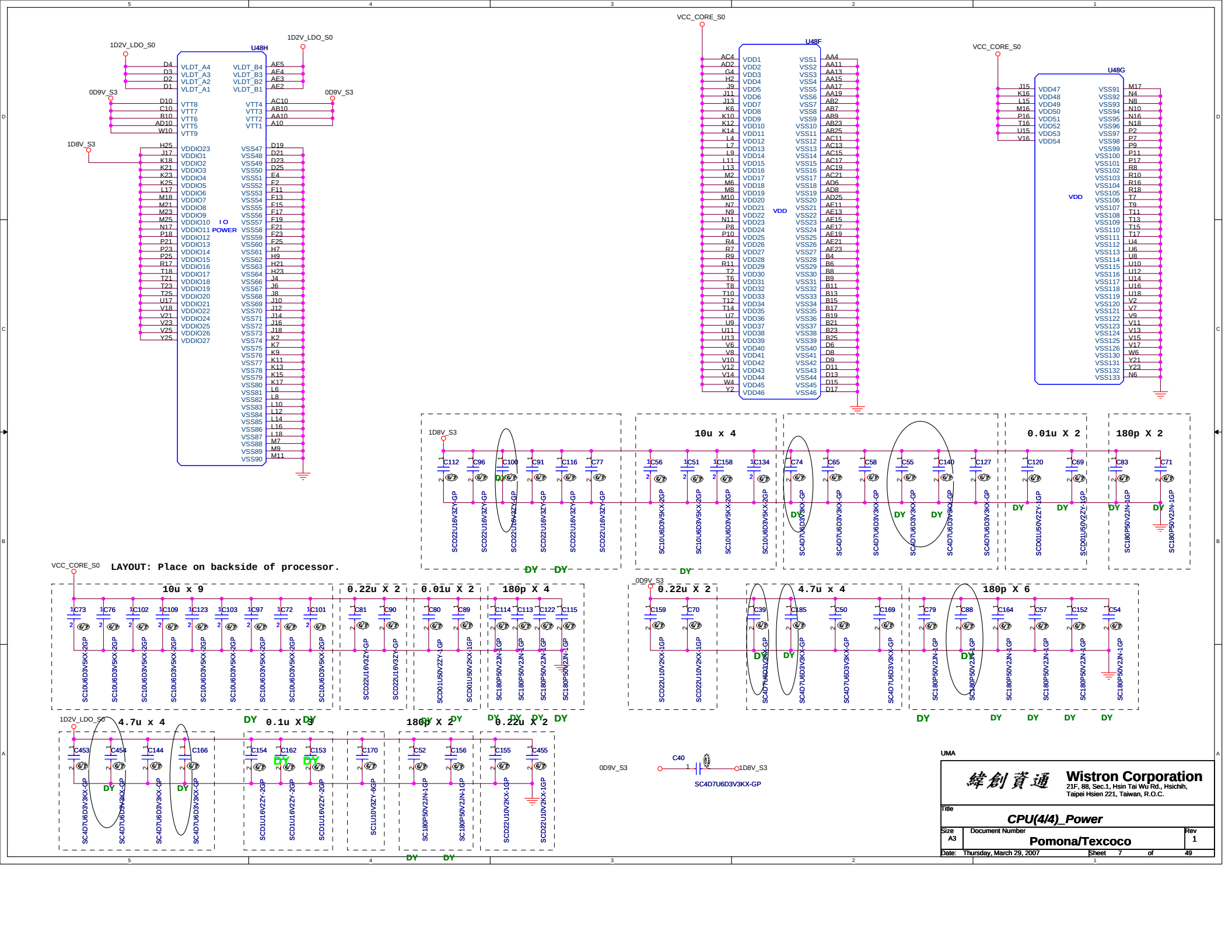
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU(2/4)_DDR2***

Size	Document Number	Rev
A3	**Pomona/Texcoco**	1

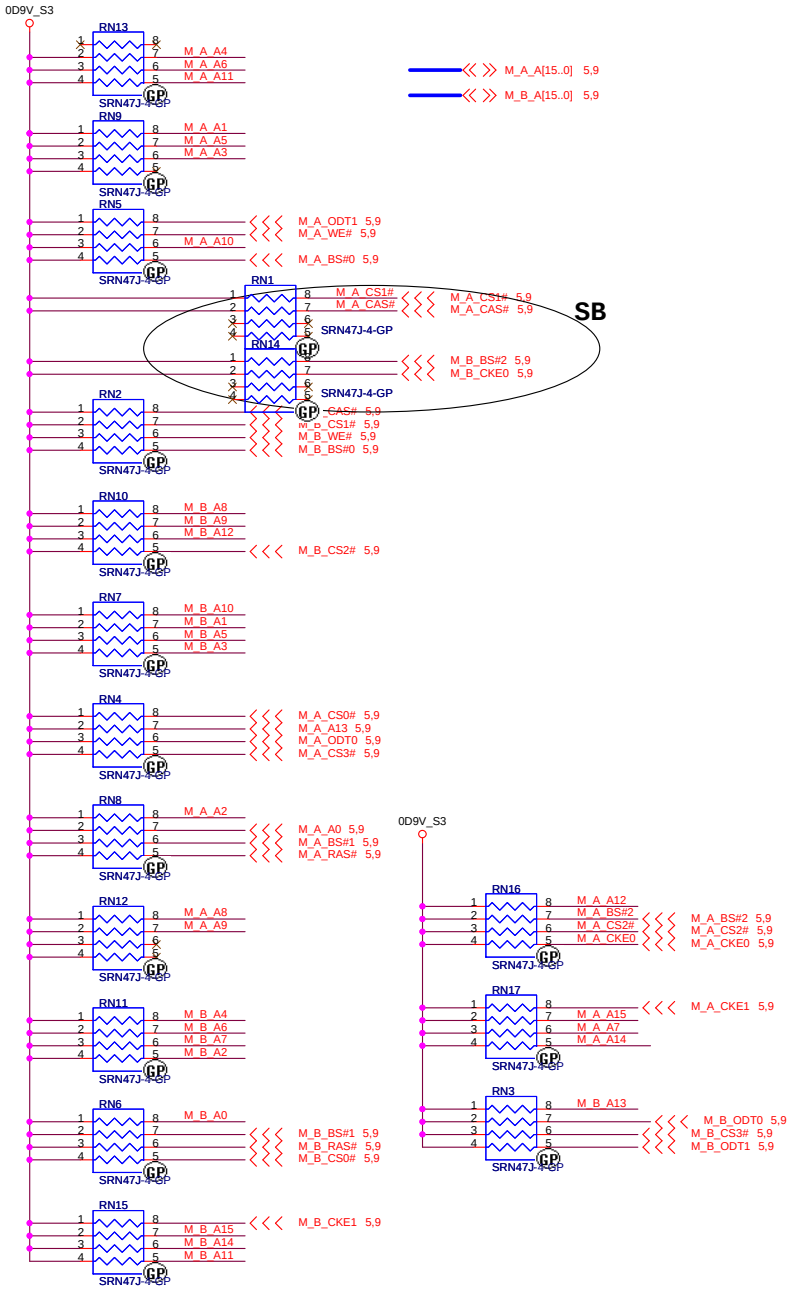
Date: Thursday, March 29, 2007 Sheet 5 of 49


LAYOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.
IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491
Near To CPU
LAYOUT: Route FBCLKOUT_H/L
differentially impedance 80
VREF_DDR2_CPU
LAYOUT: Locate close to CPU.
SC
SC CHANGE TO 680
HDT Connectors
U48D
U48E
LDT_PWROK
CPU_PRESENT#
THERMTRIP#
PROCHOT#
KBC_THERMTRIP# 33,36
ALERT# 19,36
VID[5..0] 42
CLKCPU_IN
CLKCPU# IN
VREF_DDR_CLAW
VCC_CORE_S0
2D5V_S0
2D5V_VDDA_S0
1D8V_S3
3D3V_S0
1D2V_LDO_S0
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU(3/4)_Control & Debug
Pomona/Texcoco
Rev 1
Date: Thursday, March 29, 2007
Sheet 6 of 49


1D2V_LDO_S0
U48H
0D9V_S3
1D8V_S3
VLDT_A4
VLDT_A3
VLDT_A2
VLDT_A1
VLDT_B4
VLDT_B3
VLDT_B2
VLDT_B1
VTT8
VTT7
VTT6
VTT5
VTT9
VTT4
VTT3
VTT2
VTT1
VDDIO23
VDDIO1
VDDIO2
VDDIO3
VDDIO4
VDDIO5
VDDIO6
VDDIO7
VDDIO8
VDDIO9
VDDIO10
VDDIO11
VDDIO12
VDDIO13
VDDIO14
VDDIO15
VDDIO16
VDDIO17
VDDIO18
VDDIO19
VDDIO20
VDDIO21
VDDIO22
VDDIO24
VDDIO25
VDDIO26
VDDIO27
I O
POWER
VSS47
VSS48
VSS49
VSS50
VSS51
VSS52
VSS53
VSS54
VSS55
VSS56
VSS57
VSS58
VSS59
VSS60
VSS61
VSS62
VSS63
VSS64
VSS66
VSS67
VSS68
VSS69
VSS70
VSS71
VSS72
VSS73
VSS74
VSS75
VSS76
VSS77
VSS78
VSS79
VSS80
VSS81
VSS82
VSS83
VSS84
VSS85
VSS86
VSS87
VSS88
VSS89
VSS90
VCC_CORE_S0
U48F
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDD10
VDD11
VDD12
VDD13
VDD14
VDD15
VDD16
VDD17
VDD18
VDD19
VDD20
VDD21
VDD22
VDD23
VDD24
VDD25
VDD26
VDD27
VDD28
VDD29
VDD30
VDD31
VDD32
VDD33
VDD34
VDD35
VDD36
VDD37
VDD38
VDD39
VDD40
VDD41
VDD42
VDD43
VDD44
VDD45
VDD46
VDD
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15
VSS16
VSS17
VSS18
VSS19
VSS20
VSS21
VSS22
VSS23
VSS24
VSS25
VSS26
VSS27
VSS28
VSS29
VSS30
VSS31
VSS32
VSS33
VSS34
VSS35
VSS36
VSS37
VSS38
VSS39
VSS40
VSS41
VSS42
VSS43
VSS44
VSS45
VSS46
U48G
VDD47
VDD48
VDD49
VDD50
VDD51
VDD52
VDD53
VDD54
VSS91
VSS92
VSS93
VSS94
VSS95
VSS96
VSS97
VSS98
VSS99
VSS100
VSS101
VSS102
VSS103
VSS104
VSS105
VSS106
VSS107
VSS108
VSS109
VSS110
VSS111
VSS112
VSS113
VSS114
VSS115
VSS116
VSS117
VSS118
VSS119
VSS120
VSS121
VSS122
VSS123
VSS124
VSS125
VSS126
VSS130
VSS131
VSS132
VSS133
10u x 4
0.01u X 2
180p X 2
SCD22U16V3ZY-GP
SC10U6D3V5KX-2GP
SC4D7U6D3V3KX-GP
SCD01U50V2ZY-1GP
SC180P50V2JN-1GP
DY
LAYOUT: Place on backside of processor.
10u x 9
0.22u X 2
0.01u X 2
180p X 4
SCD22U16V3ZY-GP
SCD01U50V2ZY-1GP
SC180P50V2JN-1GP
0.22u X 2
4.7u x 4
180p X 6
SCD22U10V2KX-1GP
SC4D7U6D3V3KX-GP
SC180P50V2JN-1GP
4.7u x 4
0.1u X 3
180p X 2
0.22u X 2
SC4D7U6D3V3KX-GP
SCD1U16V2ZY-2GP
SC1U10V3ZY-6GP
SC180P50V2JN-1GP
SCD22U10V2KX-1GP
C40
SC4D7U6D3V3KX-GP
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU(4/4)_Power
Size
A3
Document Number
Pomona/Texcoco
Rev
1
Date: Thursday, March 29, 2007
Sheet 7 of 49

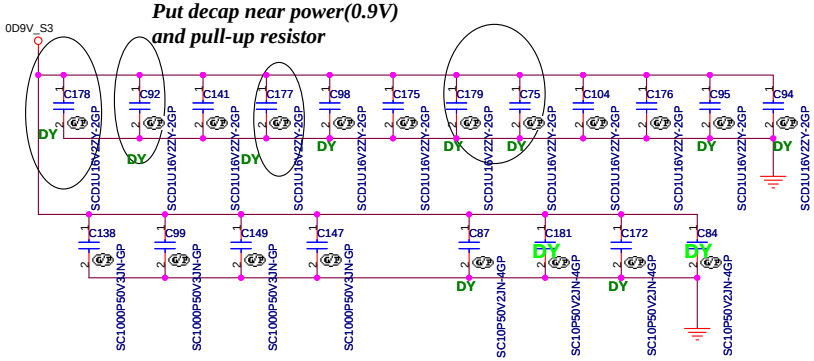
PARALLEL TERMINATION

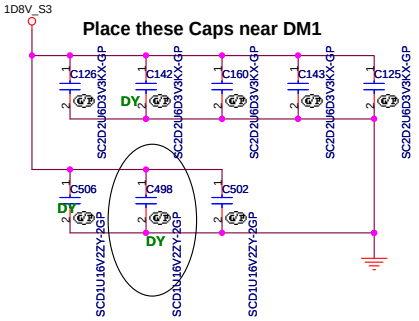
Put decap near power(0.9V) and pull-up resistor

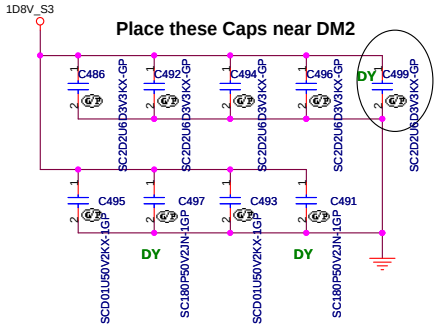


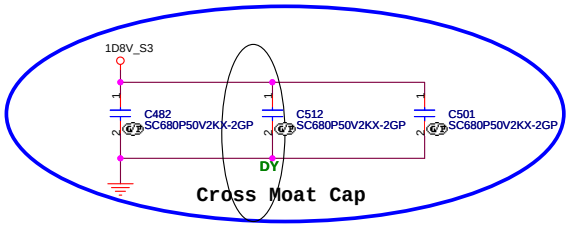
Decoupling Capacitor

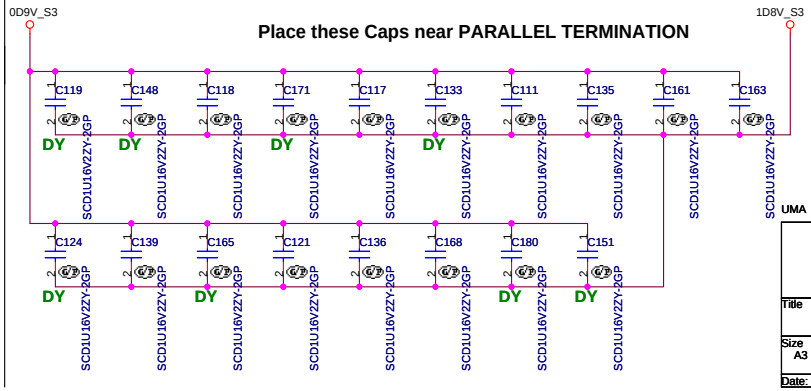
Put decap near power(0.9V) and pull-up resistor





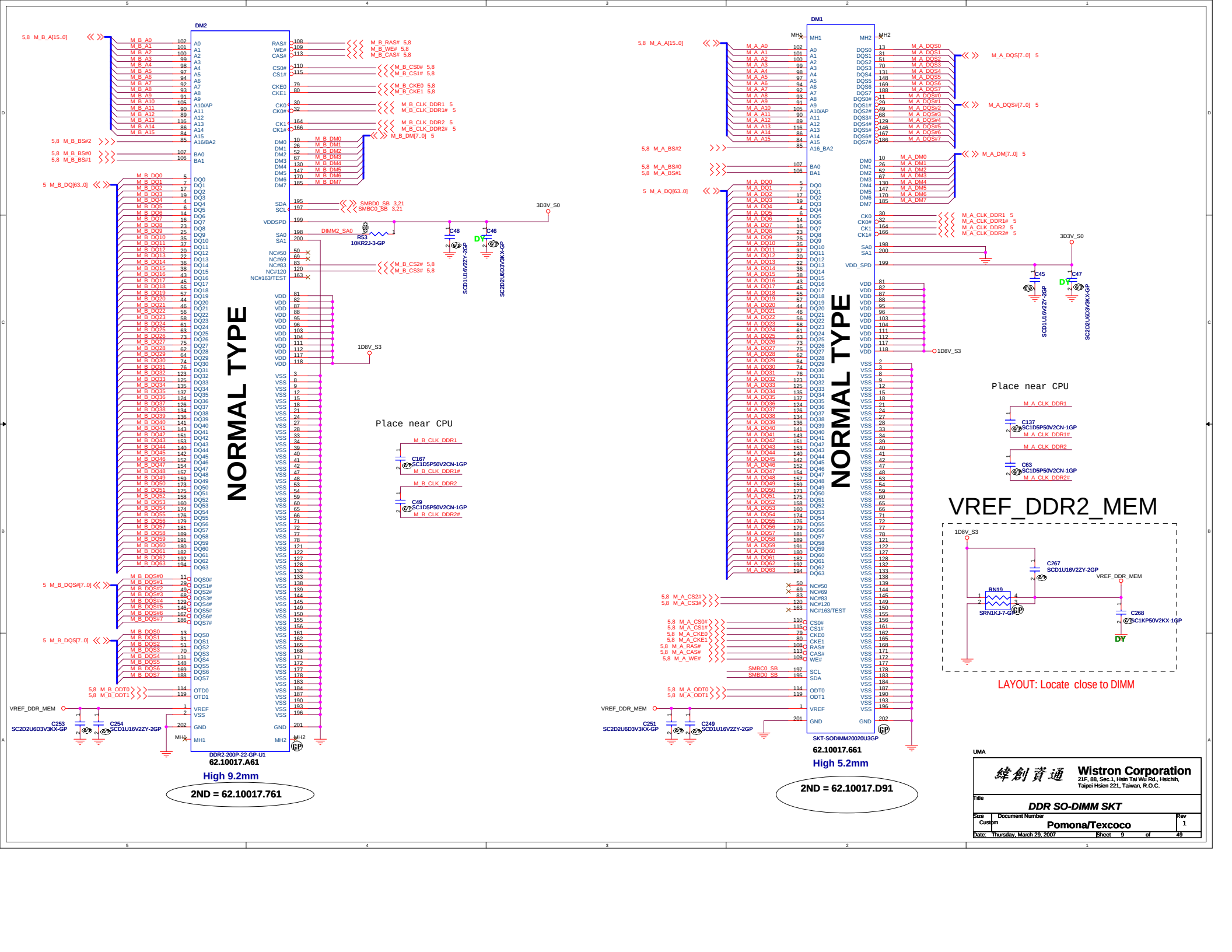






UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDR DAMPING & TERMINATION***	
Size A3	Document Number **Pomona/Texcoco**	Rev 1
Date: Thursday, March 29, 2007	Sheet 8 of 49	


DM2
NORMAL TYPE
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
2ND = 62.10017.761
DM1
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
High 5.2mm
2ND = 62.10017.D91
Place near CPU
M_B_CLK_DDR1
C167
SC1D5P50V2CN-1GP
M_B_CLK_DDR1#
M_B_CLK_DDR2
C49
SC1D5P50V2CN-1GP
M_B_CLK_DDR2#
Place near CPU
M_A_CLK_DDR1
C137
SC1D5P50V2CN-1GP
M_A_CLK_DDR1#
M_A_CLK_DDR2
C63
SC1D5P50V2CN-1GP
M_A_CLK_DDR2#
VREF_DDR2_MEM
1D8V_S3
C267
SCD1U16V2ZY-2GP
VREF_DDR_MEM
RN19
SRN1KJ-7-GP
C268
SC1KP50V2KX-1GP
DY
LAYOUT: Locate close to DIMM
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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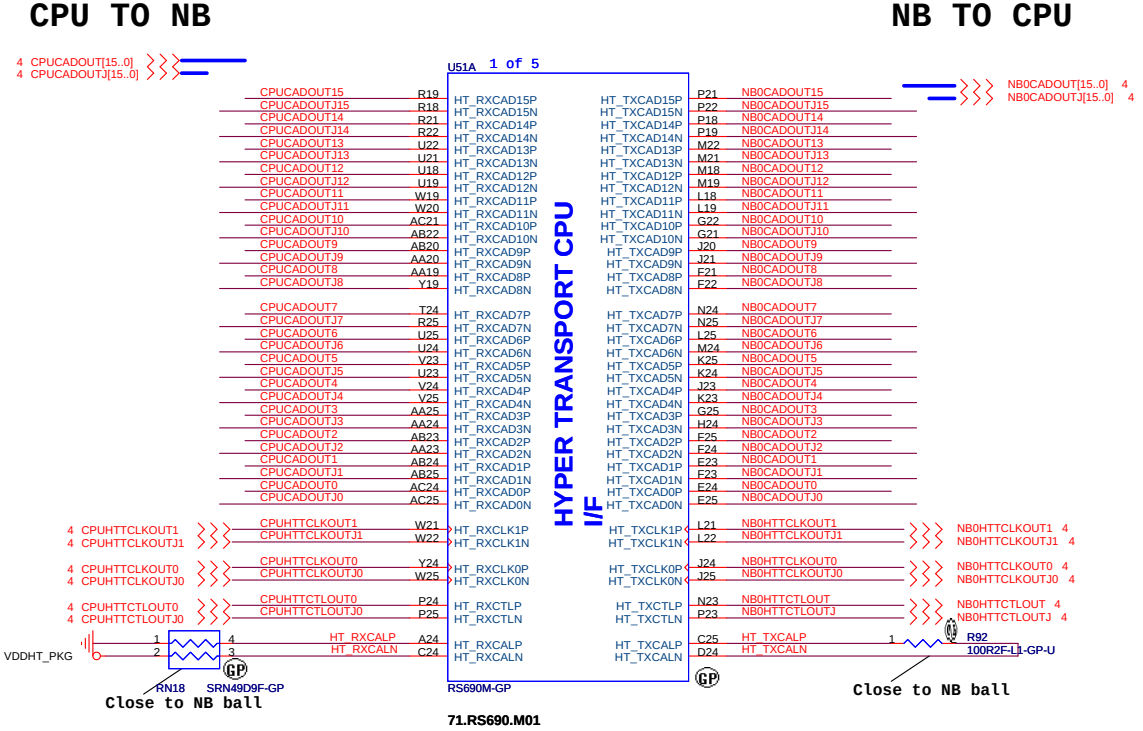
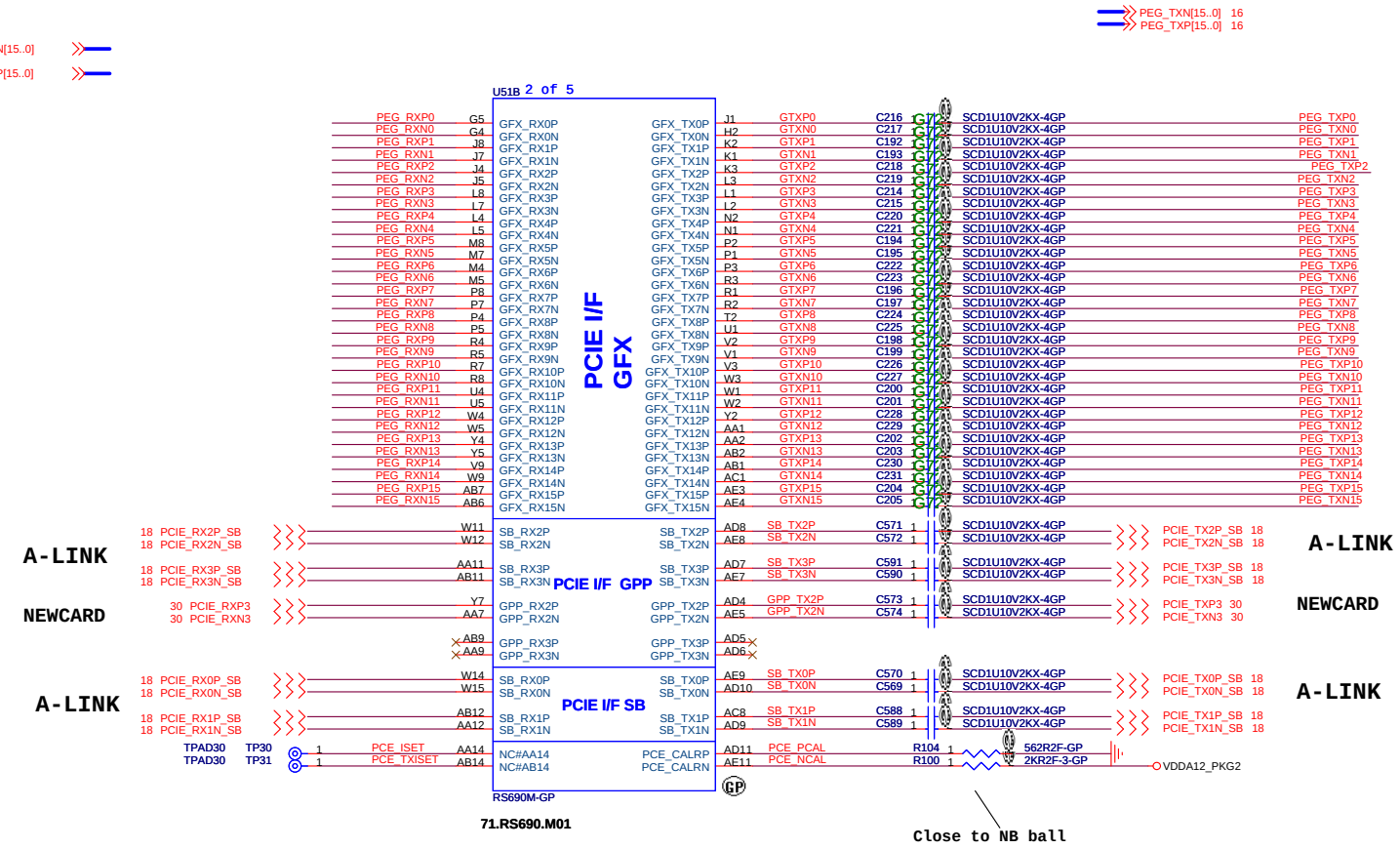
Title
DDR SO-DIMM SKT
Size
Custom
Document Number
Pomona/Texcoco
Rev
1
Date: Thursday, March 29, 2007
Sheet 9 of 49



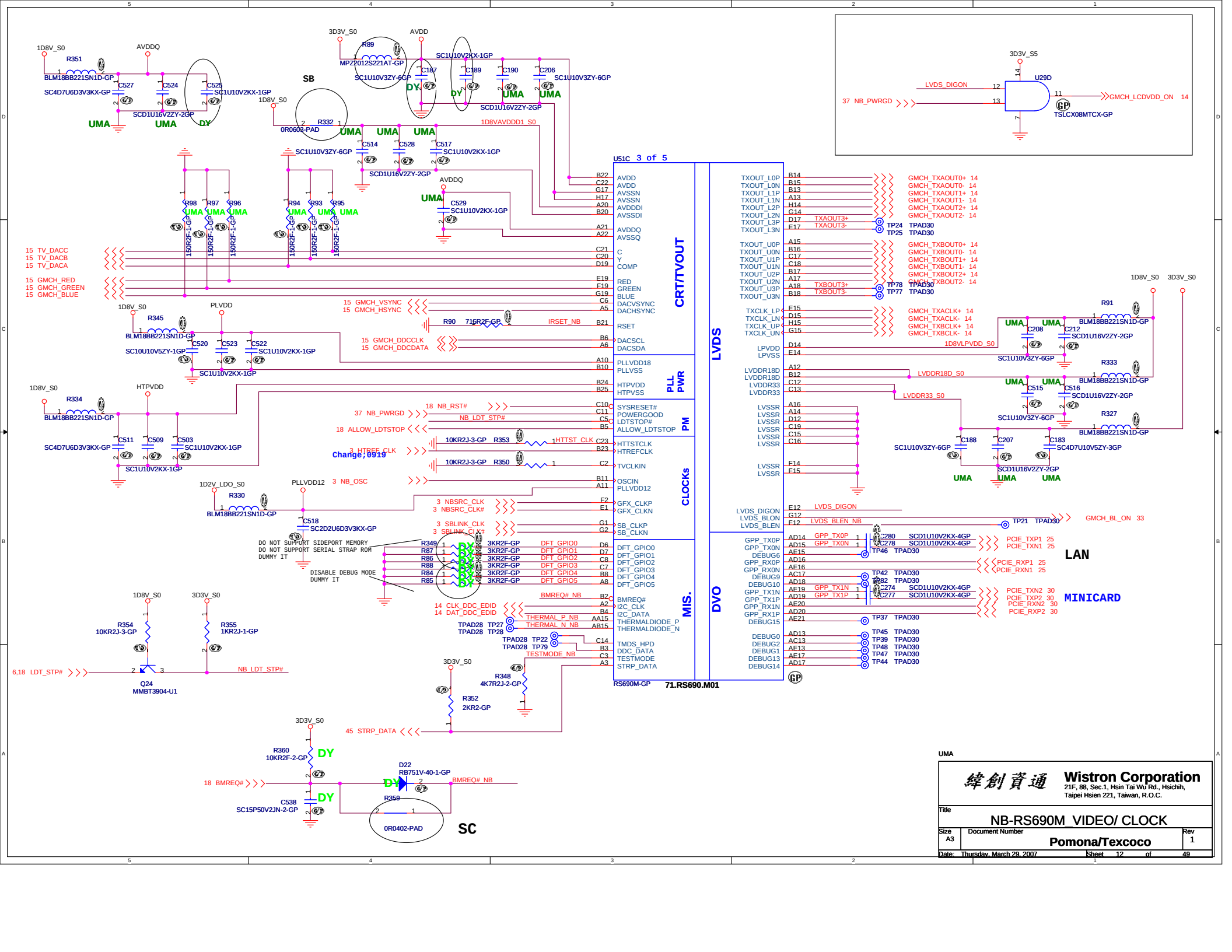
UMA

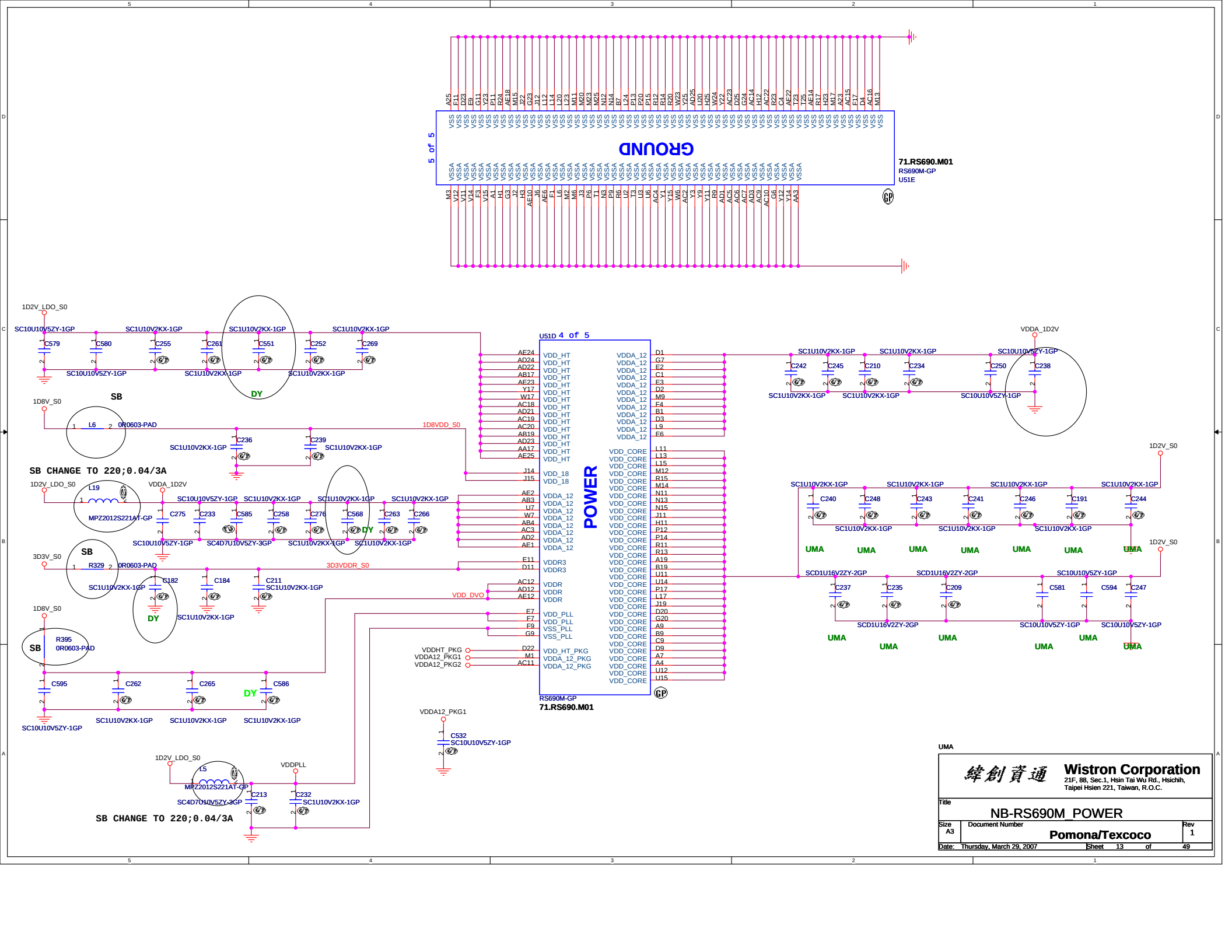
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***NB-RS690M_HT***	
Size A3	Document Number **Pomona/Texcoco**	Rev 1
Date: Thursday, March 29, 2007	Sheet 10 of 49	



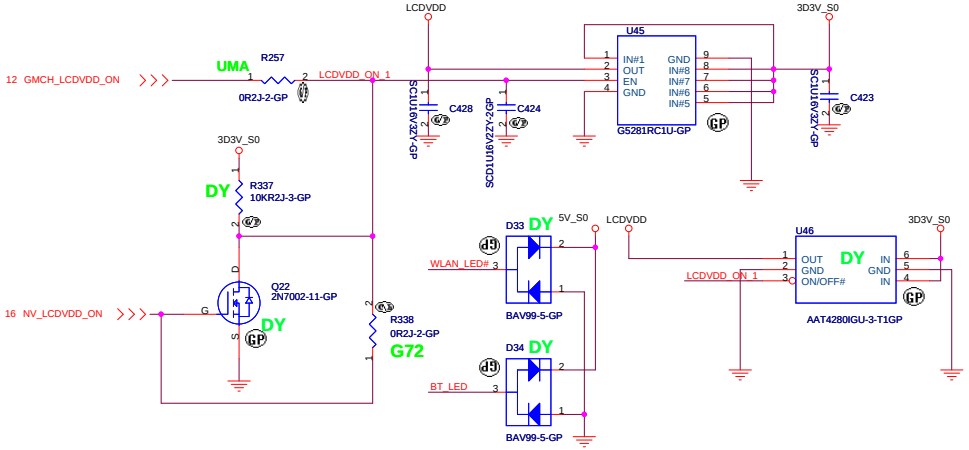
UMA

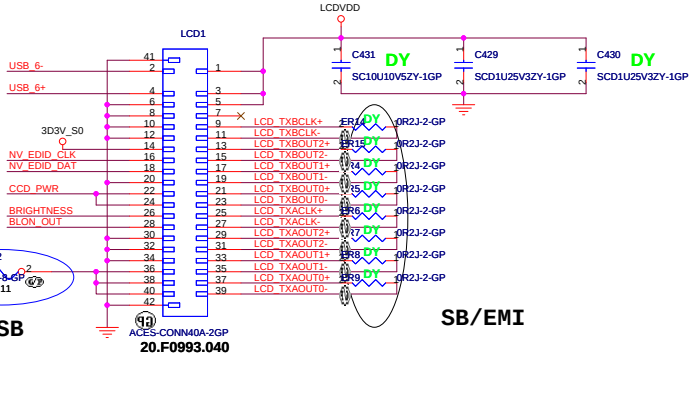
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	NB-RS690M_MEM/PCIE_LINK I/F
Size A3 / Document Number	Pomona/Texcoco / Rev 1
Date: Thursday, March 29, 2007	Sheet 11 of 49

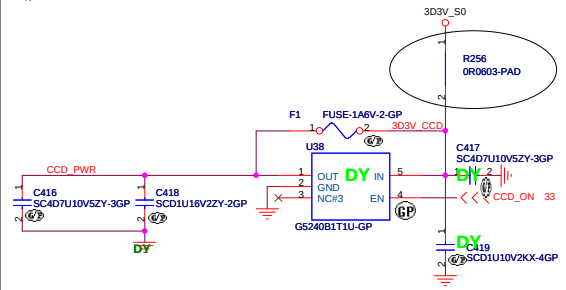

U51C 3 of 5
CRT/TVOUT
LVDS
PLL PWR
PM
CLOCKs
MIS.
DVO
RS690M-GP
71.RS690.M01
SB
SC
LAN
MINICARD
UMA
DY
Change:0919
DO NOT SUPPORT SIDEPORT MEMORY
DO NOT SUPPORT SERIAL STRAP ROM
DUMMY IT
DISABLE DEBUG MODE
DUMMY IT
Q24
MMBT3904-U1
D22
RB751V-40-1-GP
U29D
TSLCX08MTCX-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
NB-RS690M_VIDEO/ CLOCK
Pomona/Texcoco
Size A3
Rev 1
Date: Thursday, March 29, 2007
Sheet 12 of 49

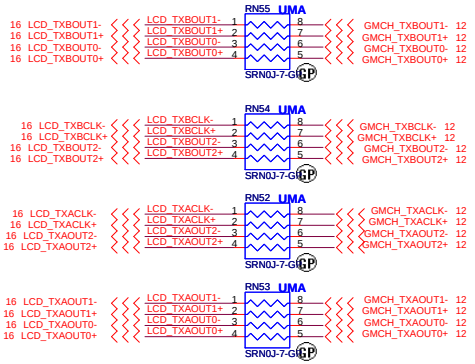

5 of 5
GROUND
71.RS690.M01
RS690M-GP
U51E
U51D 4 of 5
POWER
RS690M-GP
71.RS690.M01
1D2V_LDO_S0
1D8V_S0
3D3V_S0
VDDA_1D2V
1D8VDD_S0
3D3VDDR_S0
VDD_DVO
VDDHT_PKG
VDDA12_PKG1
VDDA12_PKG2
VDDPLL
SB
DY
UMA
SB CHANGE TO 220;0.04/3A
SB CHANGE TO 220;0.04/3A
MPZ2012S221AT-GP
0R0603-PAD
SC1U10V2KX-1GP
SC10U10V5ZY-1GP
SC4D7U10V5ZY-3GP
SCD1U16V2ZY-2GP
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS690M_POWER
Size
A3
Document Number
Pomona/Texcoco
Rev
1
Date: Thursday, March 29, 2007
Sheet 13 of 49

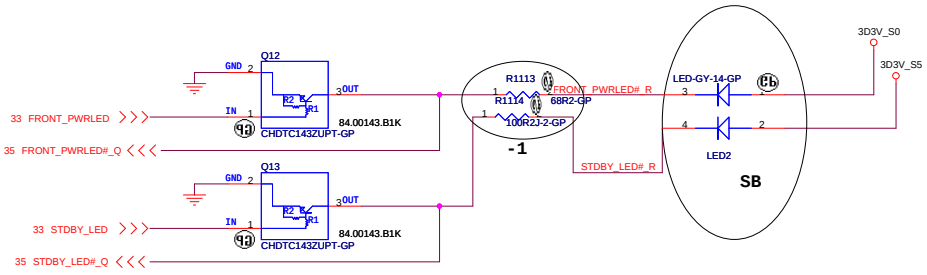
LCD/INVERTER CONN

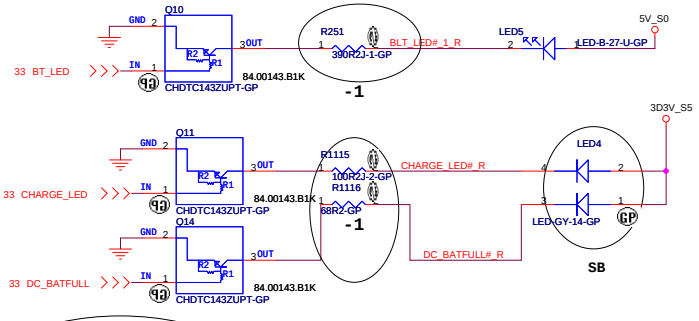


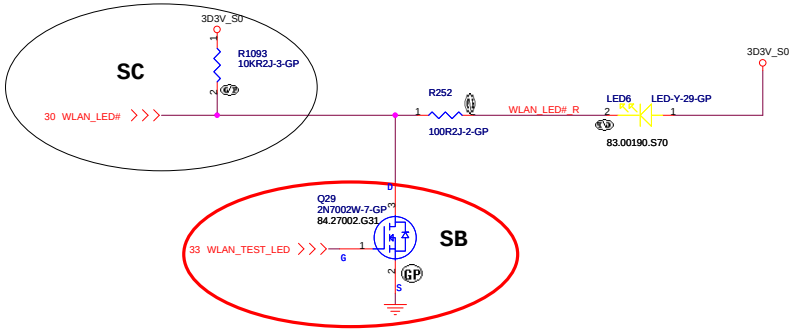


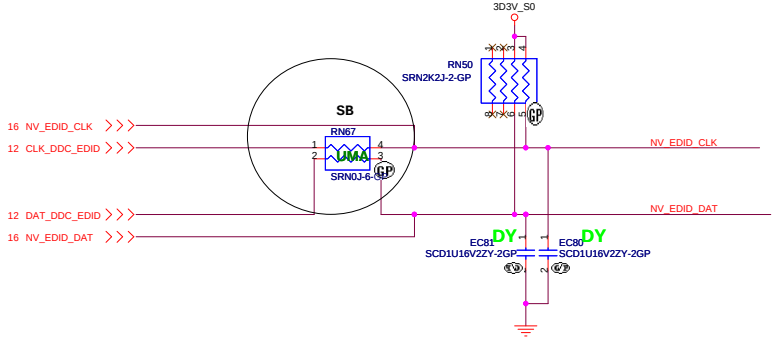








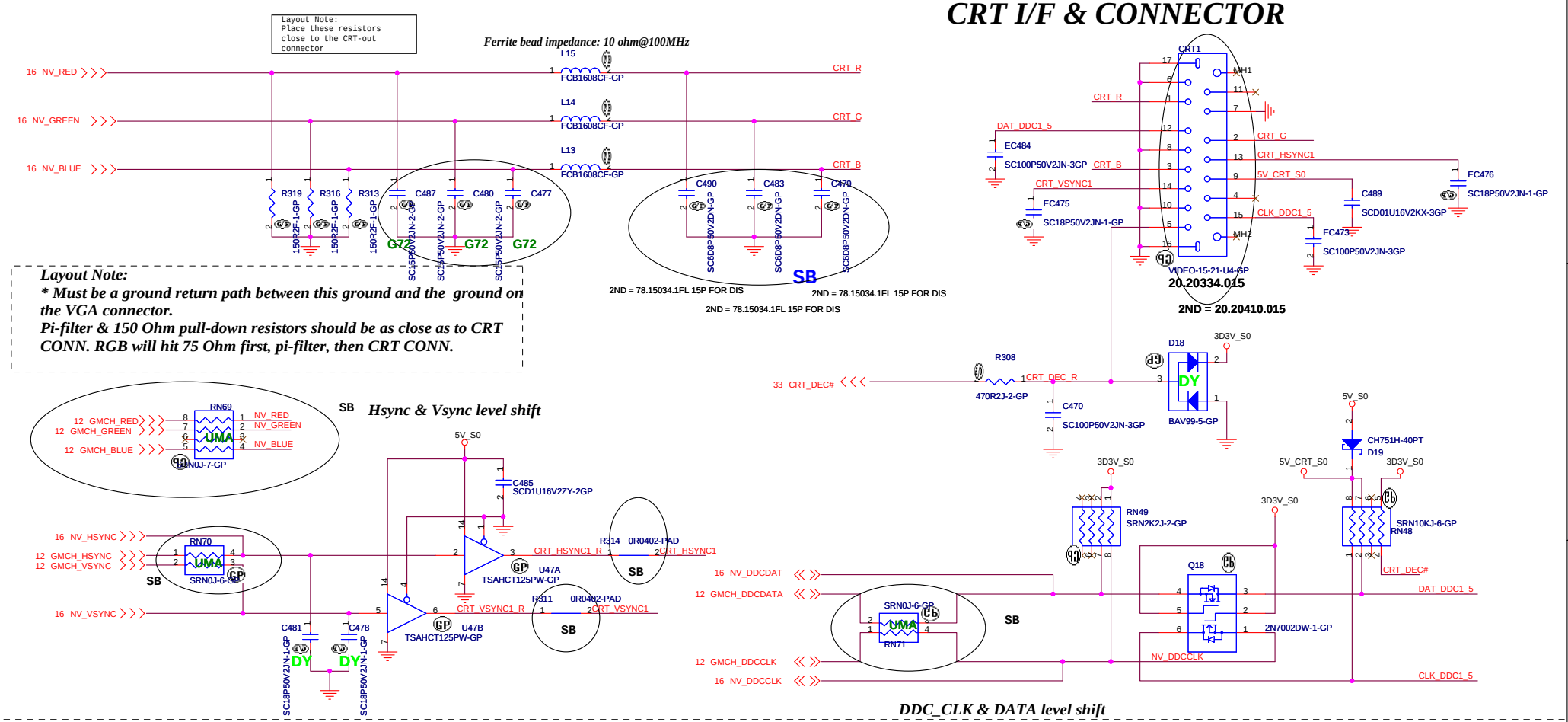




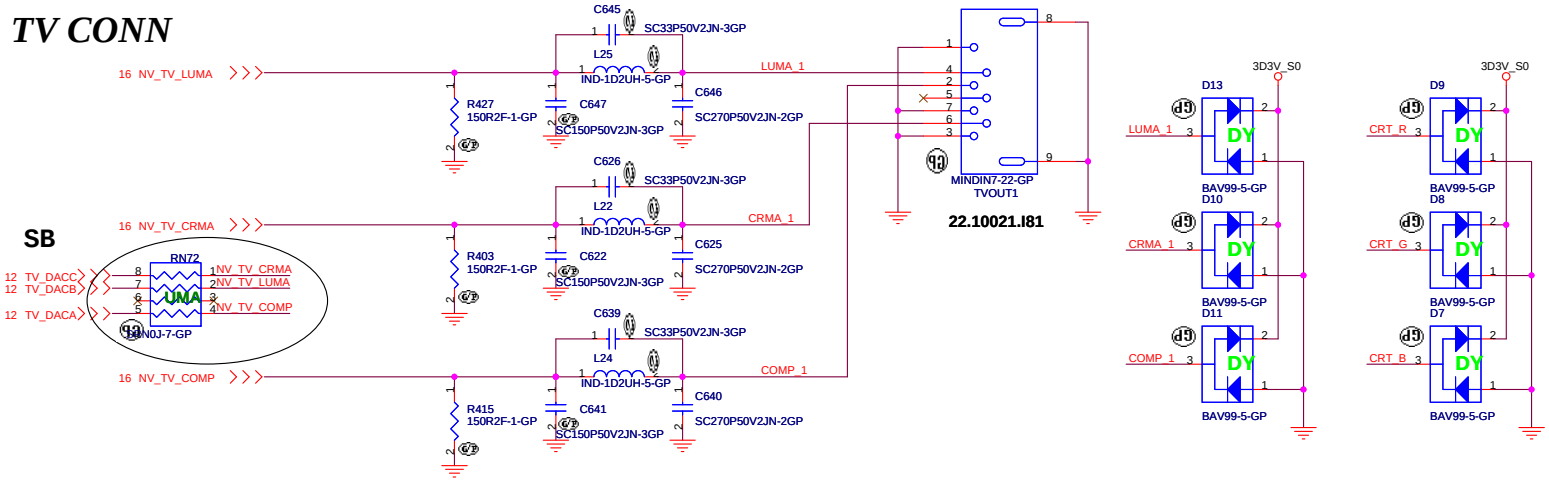
UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*LCD CONN & LED*	
Size	Document Number **Pomona/Texcoco**	Rev 1
Date: Thursday, March 29, 2007	Sheet 14 of 49	

CRT I/F & CONNECTOR



TV CONN



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CRT/TV Connector	
Size	Document Number: Pomona/Texcoco
Rev: 1	
Date: Thursday, March 29, 2007	Sheet 15 of 49

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

ENG MUST STUFF FOR ATI

Put near graphic connector

11 PEG_TXP[15..0]
11 PEG_TXN[15..0]
11 PEG_RXP[15..0]
11 PEG_RXN[15..0]

POWER-ON

SB/NV

SB

SC

RESET -1

EMI REQUEST

2ND = 20.F1031.230

MXM1
TYCO-CONN230A-GP-U3

DCBATOUT_MXM

DCBATOUT

G14 GAP-CLOSE-PWR
G13 GAP-CLOSE-PWR
G12 GAP-CLOSE-PWR
G11 GAP-CLOSE-PWR

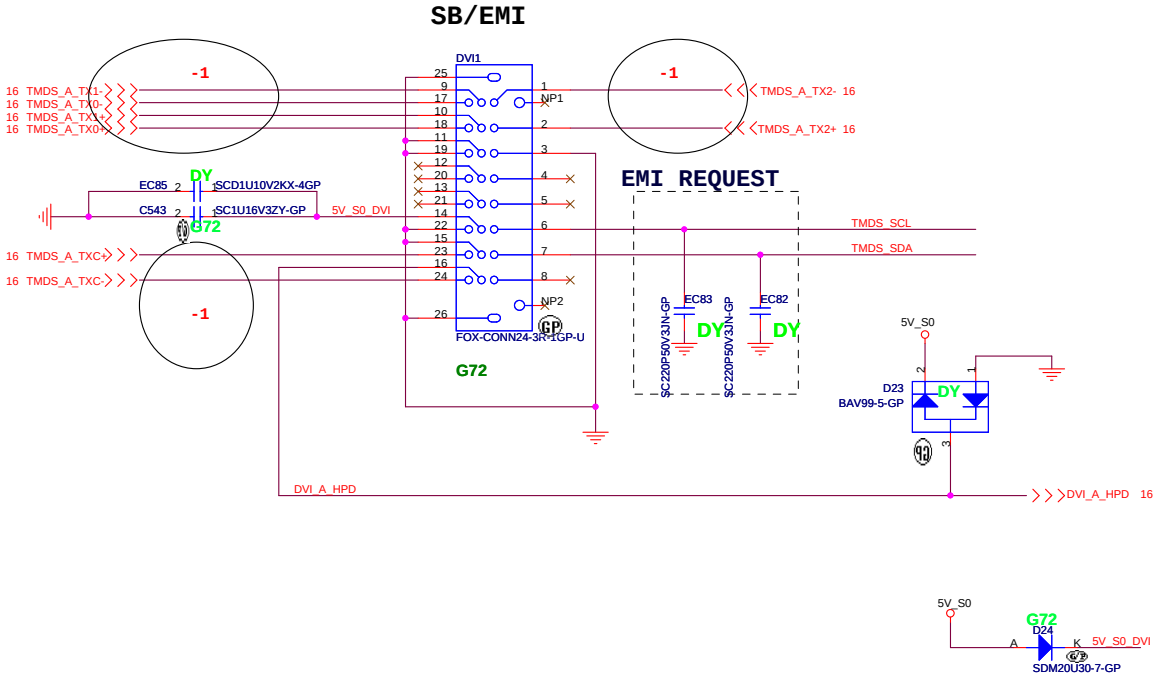
UMA

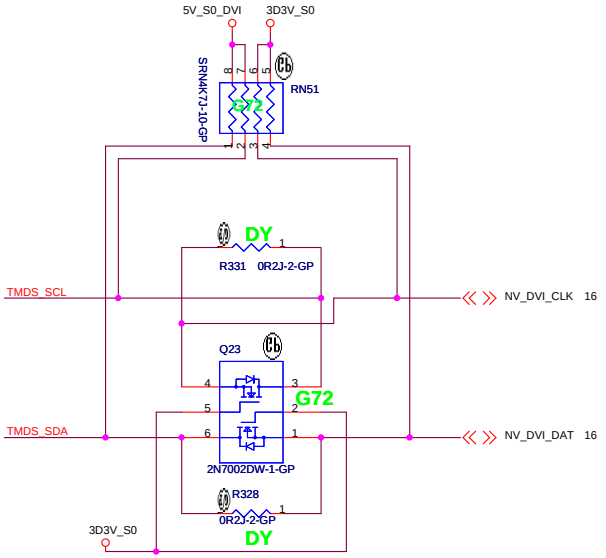
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Graphic MXM CONN

Size: A3 | Document Number: Pomona/Texcoco | Rev: 1

Date: Thursday, March 29, 2007 | Sheet 16 of 49





UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DVI CONNECTOR		
Size: A3	Document Number: Pomona/Texcoco	Rev: 1
Date: Thursday, March 29, 2007	Sheet 17 of 49	

Place these components close to U13
and use groud guard for 32K_X1 and 32K_X2.

SB

SB

SB600 asserts PLTRST# to reset
devices on the platform.

P/H 10K?

A_RST

Secondary PCI Bus reset signal.

-1

-1

PCIRST

Change 0921

UMA

SB600-GP

71.SB600.00U

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	SB600 PCI/CPU/LPC/RTC (1 of 5)
Size A3	Document Number: Pomona/Texcoco
Rev	1
Date: Thursday, March 29, 2007	Sheet 18 of 49

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB460

SATA

SATA_X1
SATA_X2
R441
10MR2J-L-GP
82.30020.571
X5
XTAL-25MHZ-67GP
C655 SC10P50V2JN-4GP
C656 SC12P50V2JN-3GP
SB

According to ATA_IXP600AD9
Change C936 and C937 from 27P to 10P.

SATA

PLLVDD_ATA
XTLVDD_ATA
AVDD_SATA
SATA

SCD01U50V2KX-1GP
C305 SATA_TXP0_SB
C306 SATA_TXN0_SB
C746 SATA_RXN0_SB
C747 SATA_RXP0_SB
2NDHDD C304 SATA_TXP1_SB
2NDHDD C303 SATA_TXN1_SB
2NDHDD C452 SATA_RXN1_SB
2NDHDD C449 SATA_RXP1_SB
SCD01U50V2KX-1GP

23 SATA_TXP0
23 SATA_TXN0
23 SATA_RXN0
23 SATA_RXP0
23 SATA_TXP1
23 SATA_TXN1
23 SATA_RXN1
23 SATA_RXP1

R430 1KR2F-3-GP
SATA_CAL

3D3V_S0
R445 10KR2J-3-GP
SATA_X1
SATA_X2
35 SATA_LED#

U16B 2 of 4

AH21	SATA_TXP0_SB	SATA_TX0+
AJ21	SATA_TXN0_SB	SATA_TX0-
AH20	SATA_RXN0_SB	SATA_RX0-
AJ20	SATA_RXP0_SB	SATA_RX0+
AH18	SATA_TXP1_SB	SATA_TX1+
AJ18	SATA_TXN1_SB	SATA_TX1-
AH17	SATA_RXN1_SB	SATA_RX1-
AJ17	SATA_RXP1_SB	SATA_RX1+
AH13		SATA_TX2+
AH14		SATA_TX2-
AH16		SATA_RX2-
AJ16		SATA_RX2+
AJ11		SATA_TX3+
AH11		SATA_TX3-
AH12		SATA_RX3-
AJ13		SATA_RX3+
AF12		SATA_CAL
AD16		SATA_X1
AD18		SATA_X2
AC12		SATA_ACT#/GPIO67
AD14		PLLVDD_SATA
AJ10		PLLVDD_SATA
AC16		XTLVDD_SATA

AVDD_SATA: AE14, AE16, AE18, AE19, AE19, AF21, AG22, AG23, AH22, AH23, AJ12, AJ14, AJ19, AJ22, AJ23

AVSS_SATA: AB14, AB16, AB18, AC14, AC18, AC19, AD12, AD19, AD21, AE12, AE21, AF11, AE14, AE16, AE18, AG11, AG12, AG13, AG14, AG16, AG17, AG18, AG19, AG20, AG21, AH10, AH19

SERIAL ATA
SERIAL ATA POWER

ATA 66/100

IDE_IORDY	AB29	IDE_PDIORDY 23
IDE_IRQ	AA28	INT_IRQ14 23
IDE_A0	AA29	IDE_PDA0 23
IDE_A1	AB27	IDE_PDA1 23
IDE_A2	Y28	IDE_PDA2 23
IDE_DACK#	AB28	IDE_PDDACK# 23
IDE_DRQ	AC27	IDE_PDDREQ 23
IDE_IOR#	AC29	IDE_PDIOR# 23
IDE_IOW#	AC28	IDE_PDIOW# 23
IDE_CS1#	W28	IDE_PDCS1# 23
IDE_CS3#	W27	IDE_PDCS3# 23
IDE_D0/GPIO15	AD28	IDE_PDD0 23
IDE_D1/GPIO16	AD26	IDE_PDD1 23
IDE_D2/GPIO17	AE29	IDE_PDD2 23
IDE_D3/GPIO18	AF27	IDE_PDD3 23
IDE_D4/GPIO19	AG29	IDE_PDD4 23
IDE_D5/GPIO20	AH28	IDE_PDD5 23
IDE_D6/GPIO21	AJ28	IDE_PDD6 23
IDE_D7/GPIO22	AJ27	IDE_PDD7 23
IDE_D8/GPIO23	AH27	IDE_PDD8 23
IDE_D9/GPIO24	AG27	IDE_PDD9 23
IDE_D10/GPIO25	AG28	IDE_PDD10 23
IDE_D11/GPIO26	AF28	IDE_PDD11 23
IDE_D12/GPIO27	AF29	IDE_PDD12 23
IDE_D13/GPIO28	AE28	IDE_PDD13 23
IDE_D14/GPIO29	AD25	IDE_PDD14 23
IDE_D15/GPIO30	AD29	IDE_PDD15 23

SPI ROM

SPI_DI/GPIO12	J3	TP93 TPAD30
SPI_DO/GPIO11	J6	TP94 TPAD30
SPI_CLK/GPIO47	G3	TP87 TPAD30
SPI_HOLD#/GPIO31	G2	TP86 TPAD30
SPI_CS#/GPIO32	G6	TP91 TPAD30
LAN_RST#/GPIO13	C23	TP85 TPAD30
ROM_RST#/GPIO14	G5	TP90 TPAD30

HW MONITOR

FANOUT0/GPIO3	M4	
FANOUT1/GPIO48	T3	
FANOUT2/GPIO49	V4	
FANIN0/GPIO50	N3	
FANIN1/GPIO51	P2	
FANIN2/GPIO52	W4	
TEMP_COMM	P5	
TEMPIN0/GPIO61	P7	
TEMPIN1/GPIO62	P8	
TEMPIN2/GPIO63	T8	
TEMPIN3/TALERT#/GPIO64	T7	ALERT# 6,36
VIN0/GPIO53	V5	PSW_CLR#
VIN1/GPIO54	L7	UMA_DIS 16
VIN2/GPIO55	M8	CLK_ID
VIN3/GPIO56	V6	
VIN4/GPIO57	M6	FP_ID 35
VIN5/GPIO58	P4	
VIN6/GPIO59	M7	
VIN7/GPIO60	V7	

SB600-GP

SC REMOVE FP_DETECT TO KBC

AVDD_HWM
AVDD N1
AVSS M1
3D3V_S0
L7 0R0603-PAD
DY
C281 SCD1U16V2ZY-2GP
C282 SC2D2U6D3V3KX-GP

3D3V_S0
R1057 10KR2J-3-GP
SB
PSW_CLR#
G15 GAPOPEN

3D3V_S0
R397 10KR2J-3-GP
R407 10KR2J-3-GP RTL
R416 10KR2J-3-GP DY
H AUTHERTEK
UMA_DIS
CLK_ID
FP_ID
R393 10KR2J-3-GP DY
R408 10KR2J-3-GP ICS
R413 10KR2J-3-GP DY
10KR2J-3-GP
L LTT

71.SB600.00U

3D3V_S0 SB XTLVDD_ATA
R444 0R0603-PAD
EC97 SCD1U16V2ZY-2GP
C658 SC2D2U6D3V3KX-GP

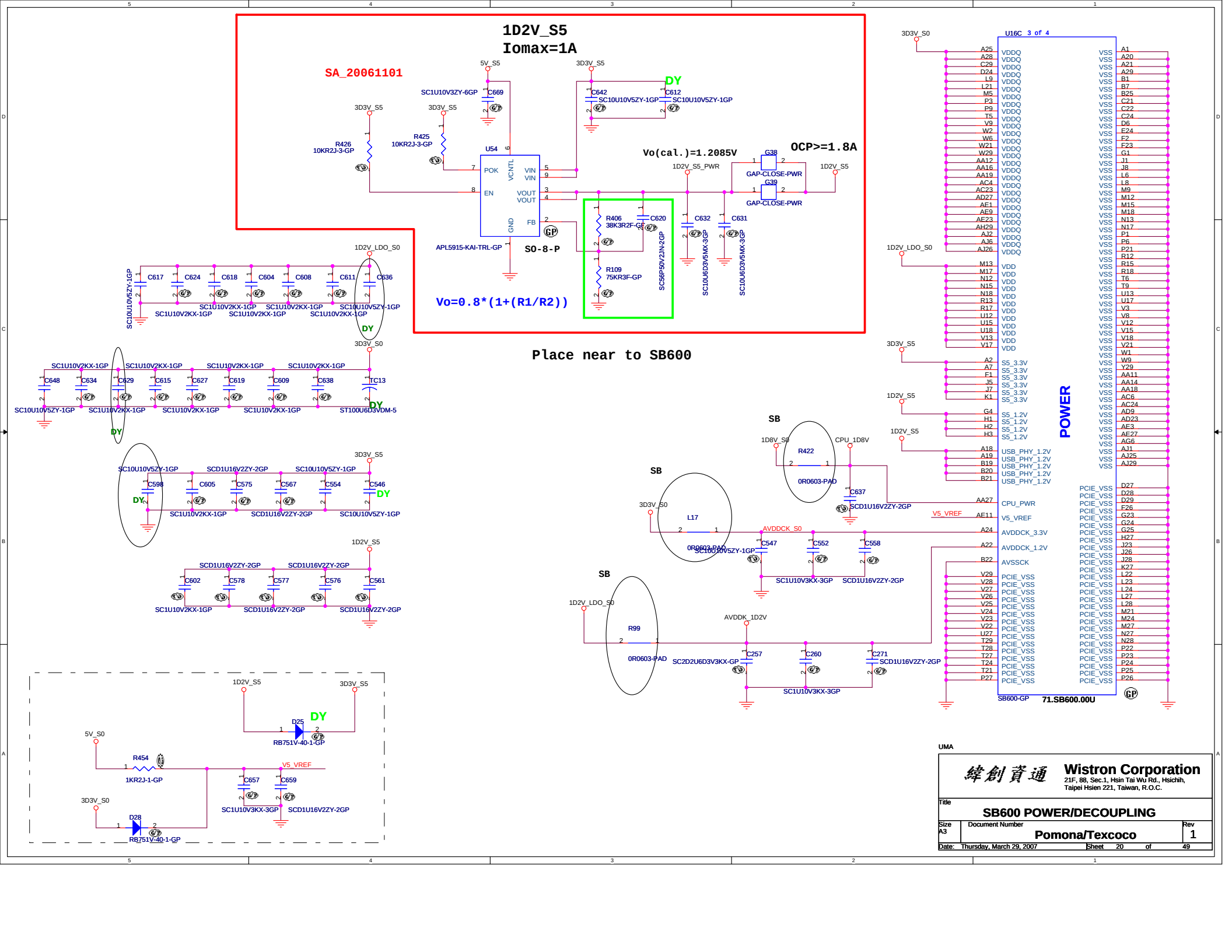
1D2V_LDO_S0 SB PLLVDD_ATA
R417 0R0603-PAD
EC88 SCD1U16V2ZY-2GP
C660 SC2D2U6D3V3KX-GP

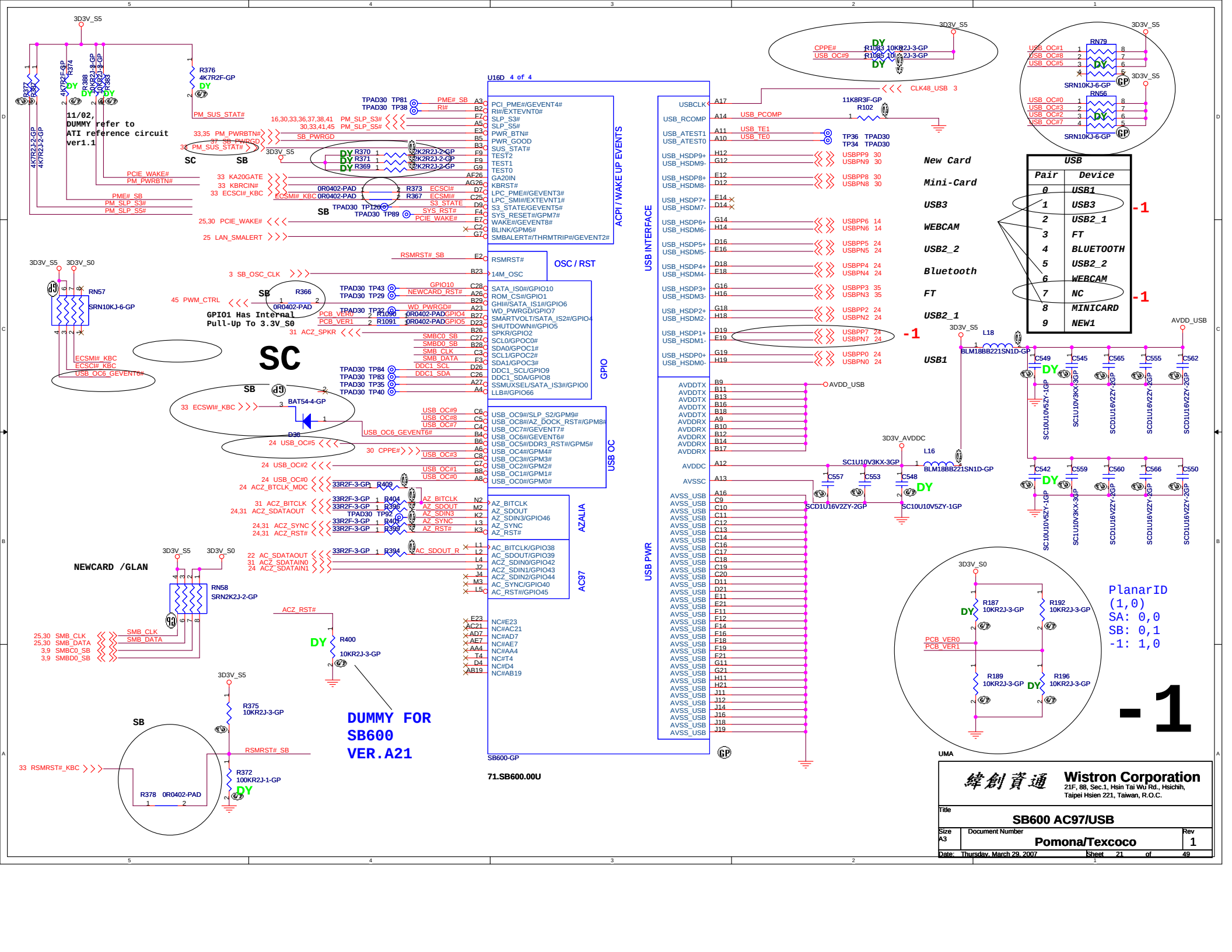
1D2V_LDO_S0 SB AVDD_SATA
R455 0R0603-PAD
EC87 SCD1U16V2ZY-2GP
1C664 SC10U6D3V5KX-2GP
1C665 SC10U6D3V5KX-2GP
EC92 SCD1U16V2ZY-2GP
EC94 SCD1U16V2ZY-2GP
EC93 SCD1U16V2ZY-2GP
EC95 SCD1U16V2ZY-2GP
EC96 SCD1U16V2ZY-2GP
DY DY DY DY DY DY

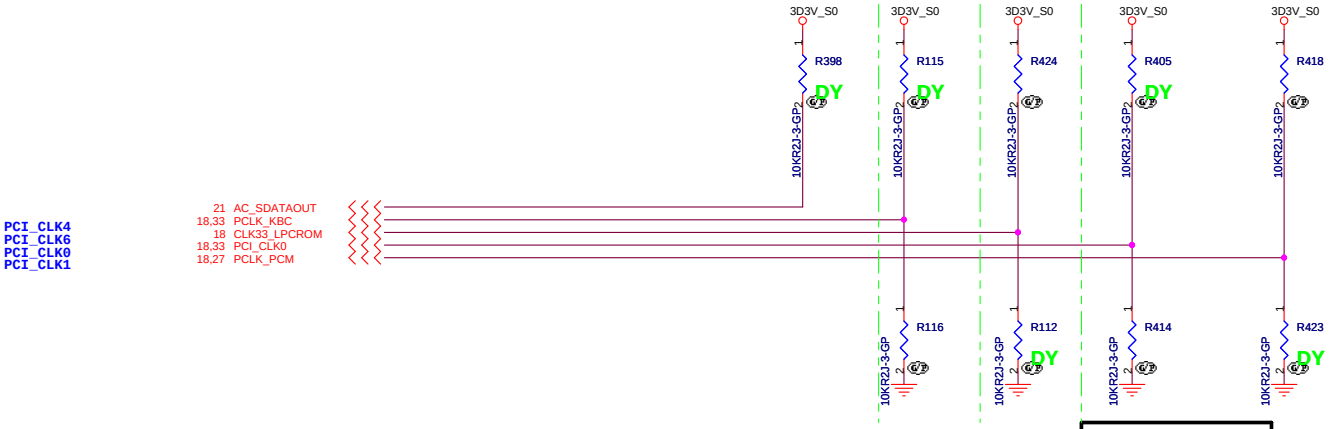
SATA

UMA

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	SB600 ACPI/GPIO/SATA/IDE (2 of 5)
Size A3	Document Number: Pomona/Texcoco
Rev	1
Date: Thursday, March 29, 2007	Sheet 19 of 49


1D2V_S5
Iomax=1A
SA_20061101
5V_S5
3D3V_S5
SC1U10V3ZY-6GP
C669
DY
C642
SC10U10V5ZY-1GP
C612
SC10U10V5ZY-1GP
R426
10KR2J-3-GP
R425
10KR2J-3-GP
U54
POK
EN
VCNTL
VIN
VIN
VOUT
VOUT
GND
FB
APL5915-KAI-TRL-GP
SO-8-P
Vo(cal.)=1.2085V
OCP>=1.8A
1D2V_S5_PWR
G38
GAP-CLOSE-PWR
G39
GAP-CLOSE-PWR
1D2V_S5
R406
38K3R2F-GP
C620
SC56P50V2JN-2GP
R109
75KR3F-GP
C632
SC10U6D3V5MX-3GP
C631
SC10U6D3V5MX-3GP
Vo=0.8*(1+(R1/R2))
Place near to SB600
1D2V_LDO_S0
C617
C624
C618
C604
C608
C611
C636
SC10U10V5ZY-1GP
SC1U10V2KX-1GP
SC1U10V2KX-1GP
SC1U10V2KX-1GP
SC1U10V2KX-1GP
SC1U10V2KX-1GP
SC10U10V5ZY-1GP
DY
3D3V_S0
SC1U10V2KX-1GP
SC1U10V2KX-1GP
SC1U10V2KX-1GP
SC1U10V2KX-1GP
C648
C634
C629
C615
C627
C619
C609
C638
TC13
SC10U10V5ZY-1GP
SC1U10V2KX-1GP
SC1U10V2KX-1GP
SC1U10V2KX-1GP
ST100U6D3VDM-5
DY
DY
3D3V_S5
SC10U10V5ZY-1GP
SCD1U16V2ZY-2GP
SC10U10V5ZY-1GP
C598
C605
C575
C567
C554
C546
DY
DY
SC1U10V2KX-1GP
SCD1U16V2ZY-2GP
SC10U10V5ZY-1GP
1D2V_S5
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
C602
C578
C577
C576
C561
SC1U10V2KX-1GP
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
1D2V_S5
3D3V_S5
DY
D25
RB751V-40-1-GP
5V_S0
R454
1KR2J-1-GP
V5_VREF
C657
C659
3D3V_S0
SC1U10V3KX-3GP
SCD1U16V2ZY-2GP
D28
RB751V-40-1-GP
U16C 3 of 4
POWER
3D3V_S0
1D2V_LDO_S0
3D3V_S5
1D2V_S5
1D2V_S5
VDDQ
VSS
S5_3.3V
S5_1.2V
USB_PHY_1.2V
PCIE_VSS
CPU_PWR
V5_VREF
AVDDCK_3.3V
AVDDCK_1.2V
AVSSCK
SB600-GP
71.SB600.00U
SB
1D8V_S0
R422
0R0603-PAD
CPU_1D8V
C637
SCD1U16V2ZY-2GP
3D3V_S0
L17
0R0603-PAD
SC10U10V5ZY-1GP
AVDDCK_S0
C547
C552
C558
SC1U10V3KX-3GP
SCD1U16V2ZY-2GP
1D2V_LDO_S0
R99
0R0603-PAD
AVDDK_1D2V
SC2D2U6D3V3KX-GP
C257
C260
C271
SCD1U16V2ZY-2GP
SC1U10V3KX-3GP
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB600 POWER/DECOUPLING
Size
A3
Document Number
Pomona/Texcoco
Rev
1
Date: Thursday, March 29, 2007
Sheet 20 of 49

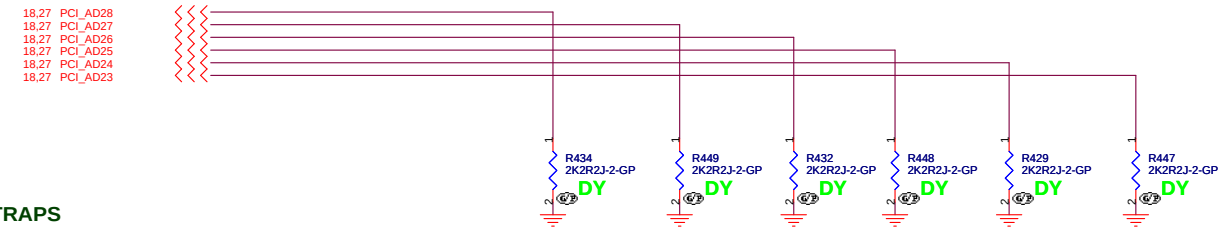

11/02,
DUMMY refer to
ATI reference circuit
ver1.1
SC
SB
GPIO1 Has Internal
Pull-Up To 3.3V_S0
NEWCARD /GLAN
DUMMY FOR
SB600
VER.A21
SB600-GP
71.SB600.00U
USB INTERFACE
ACPI / WAKE UP EVENTS
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
New Card
Mini-Card
USB3
WEBCAM
USB2_2
Bluetooth
FT
USB2_1
USB1
USB
Pair Device
0 USB1
1 USB3
2 USB2_1
3 FT
4 BLUETOOTH
5 USB2_2
6 WEBCAM
7 NC
8 MINICARD
9 NEW1
PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB600 AC97/USB
Pomona/Texcoco
Size A3
Rev 1
Date: Thursday, March 29, 2007
Sheet 21 of 49



REQUIRED SYSTEM STRAPS

	SB600				
	AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

UMA

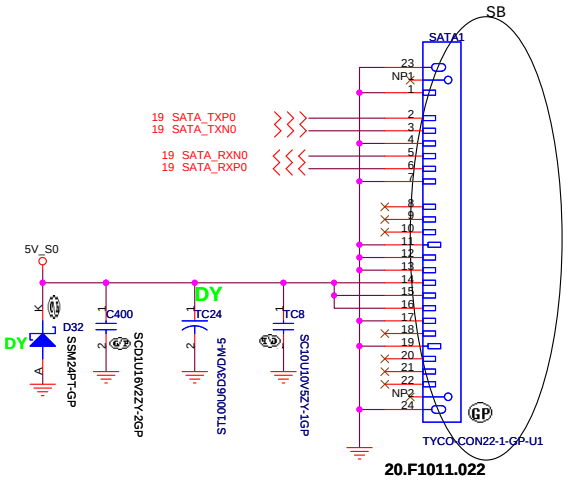
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 STRAPPING PIN

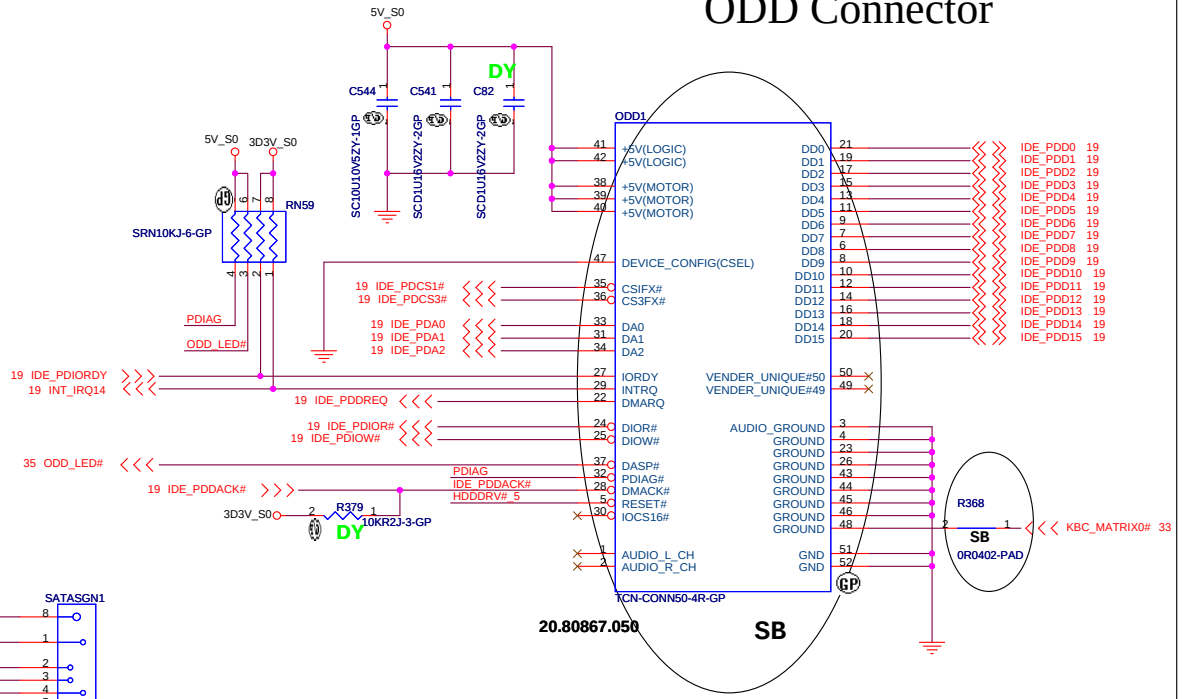
Size: A3 | Document Number: Pomona/Texcoco | Rev: 1

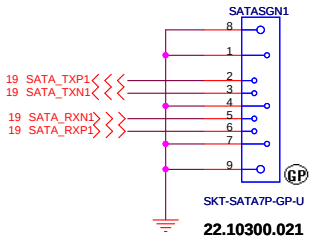
Date: Thursday, March 29, 2007 | Sheet 22 of 49

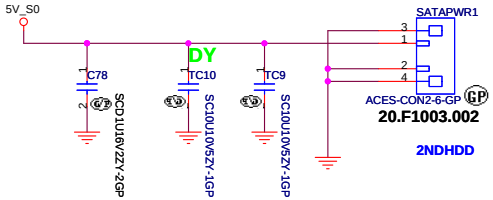
SATA HD Connector

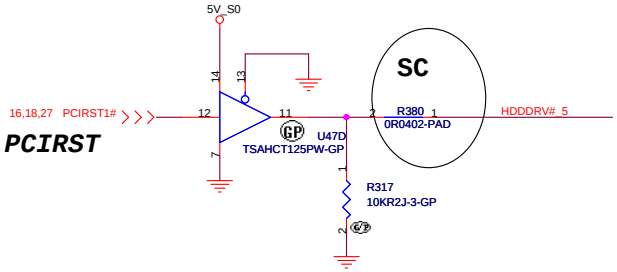


ODD Connector



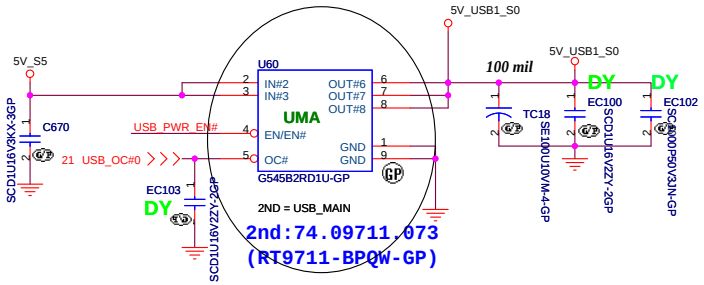


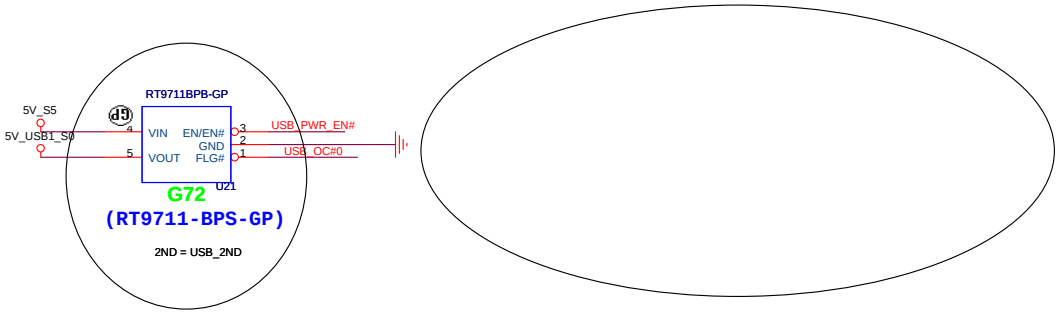


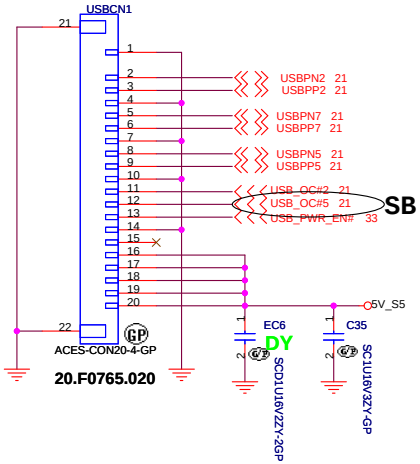


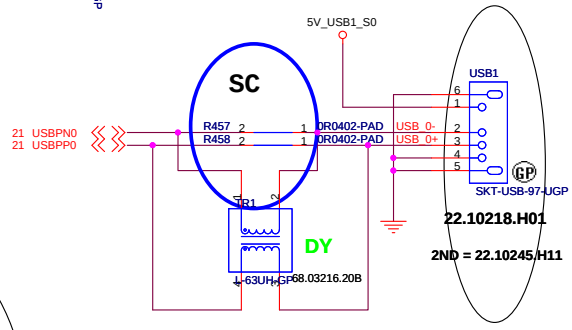
UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD and CDROM		
Size	Document Number: Pomona/Texcoco	Rev: 1
Date: Thursday, March 29, 2007	Sheet 23 of 49	

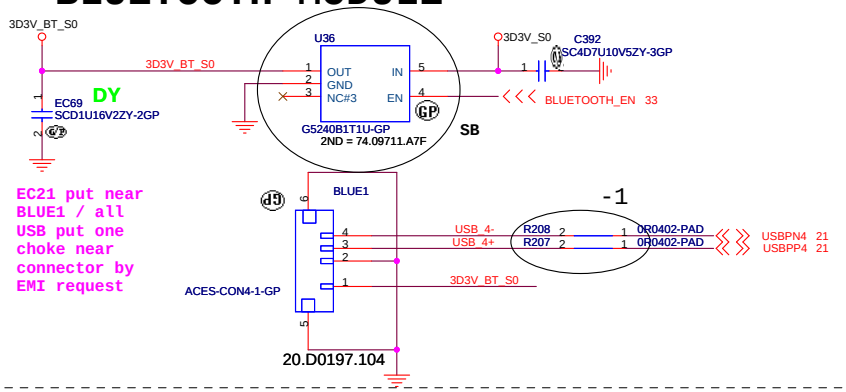




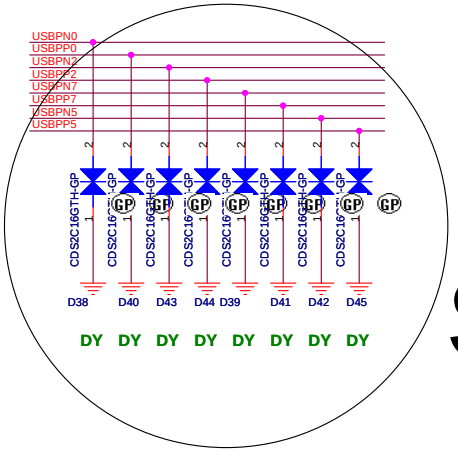




BLUETOOTH MODULE

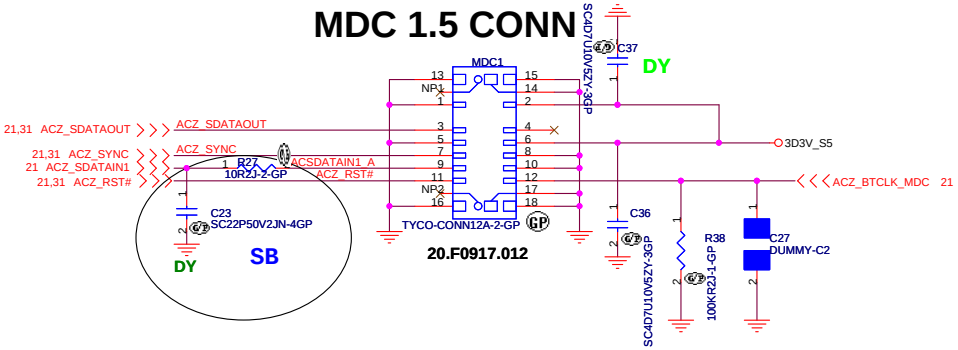


EC21 put near BLUE1 / all USB put one choke near connector by EMI request



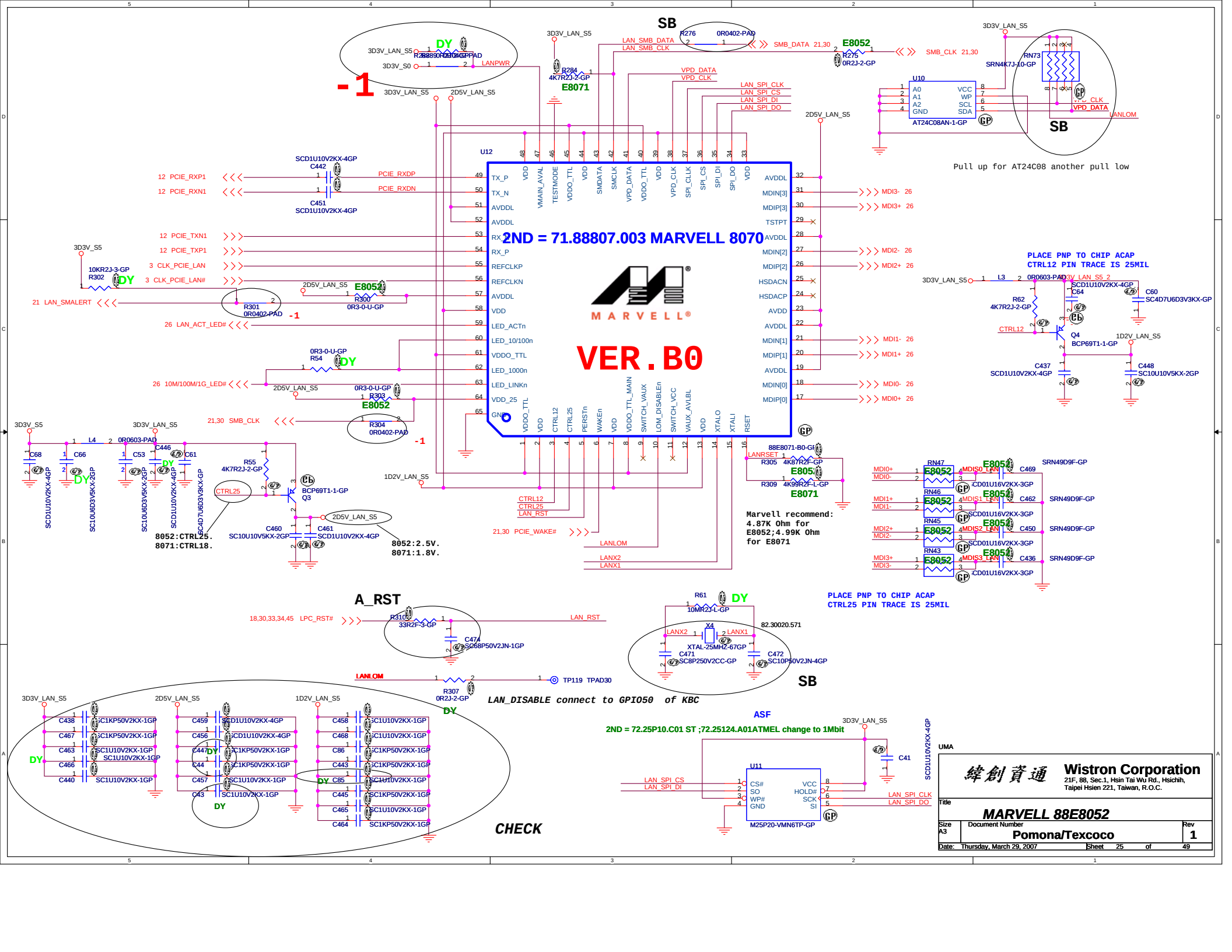
SC

MDC 1.5 CONN

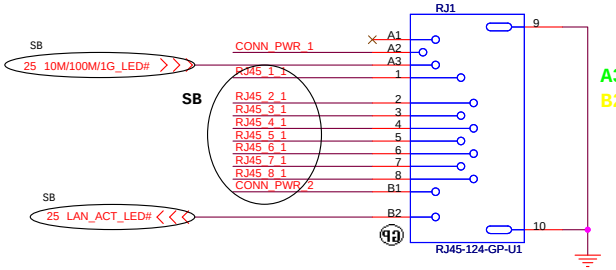


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB / MDC / BLUETOOTH***	
Size	Document Number **Pomona/Texcoco**	Rev 1
Date: Thursday, March 29, 2007	Sheet 24 of 49	


SB
2ND = 71.88807.003 MARVELL 8070
VER.B0
MARVELL
U12
E8052
E8071
-1
DY
Pull up for AT24C08 another pull low
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
Marvell recommend:
4.87K Ohm for
E8052;4.99K Ohm
for E8071
8052:CTRL25.
8071:CTRL18.
8052:2.5V.
8071:1.8V.
A_RST
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
LAN_DISABLE connect to GPIO50 of KBC
ASF
2ND = 72.25P10.C01 ST ;72.25124.A01ATMEL change to 1Mbit
CHECK
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MARVELL 88E8052
Size A3
Document Number
Pomona/Texcoco
Rev 1
Date: Thursday, March 29, 2007
Sheet 25 of 49

LAN Connector



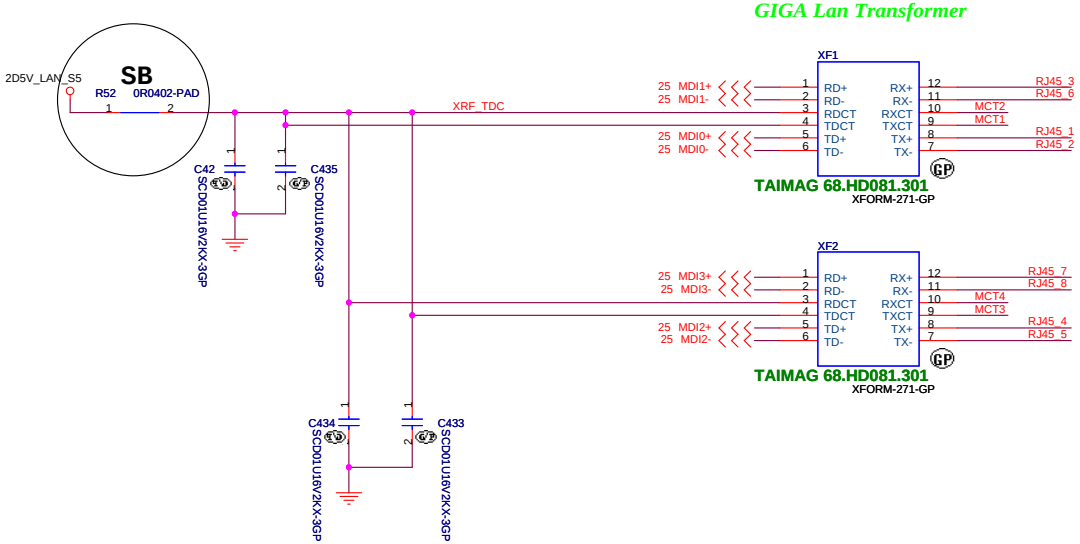
A3 : GREEN
B2 : Orange

22.10277.011

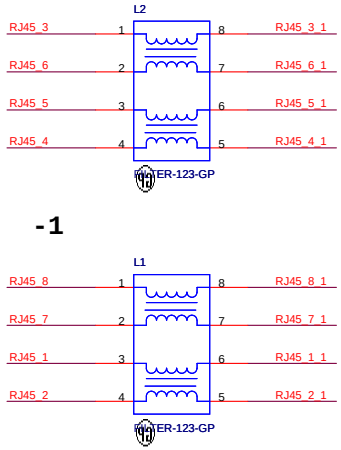
GIGA Lan Transformer

LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.



For EMI



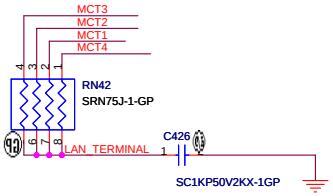
SC CHANGE 69.10106.021 TO 69.10106.011

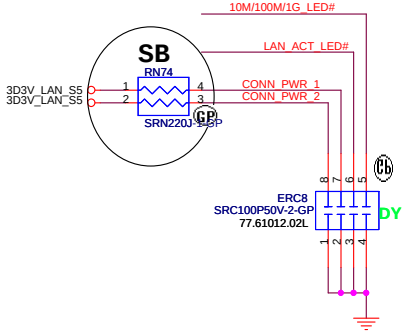
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6





CLOSE TO TRANSFORMER

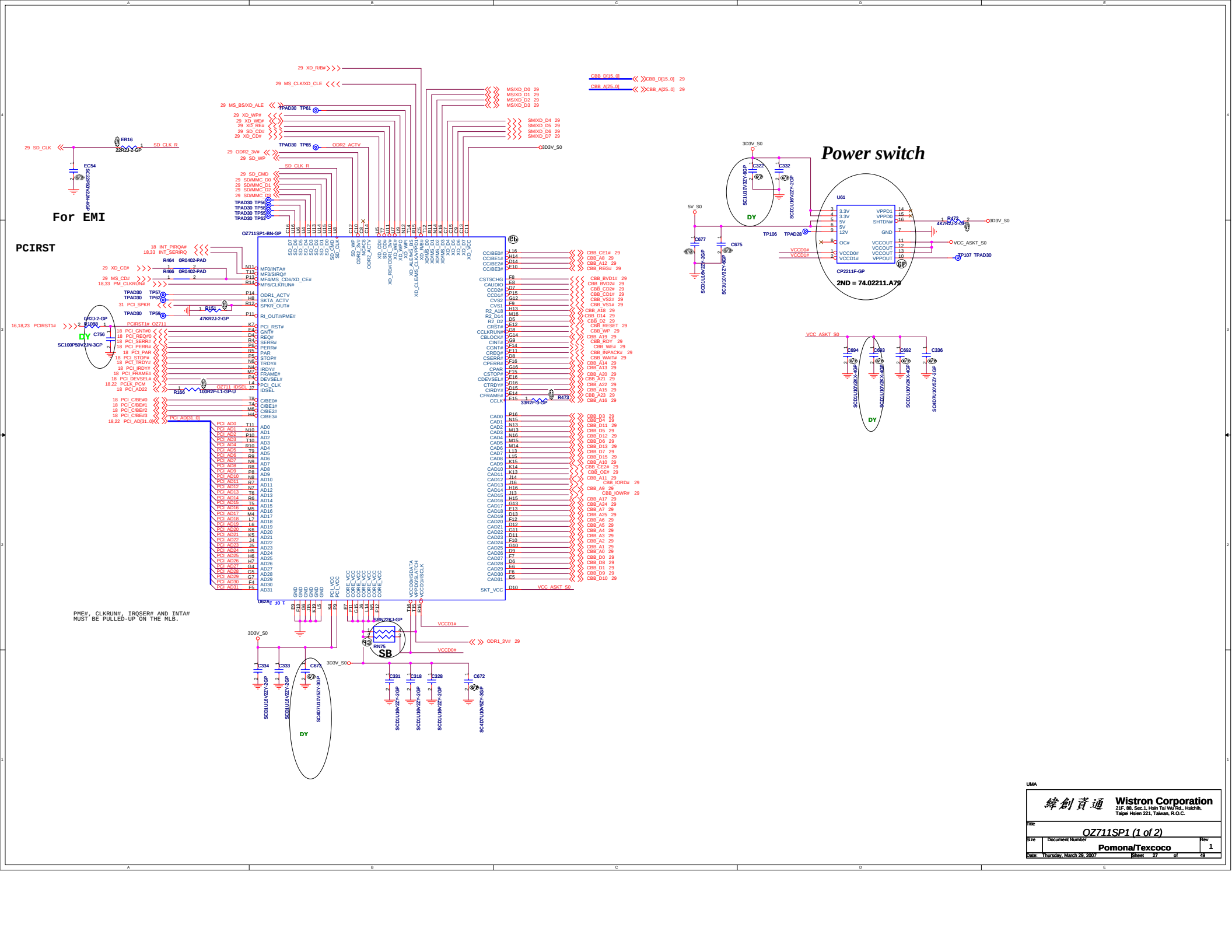
UMA

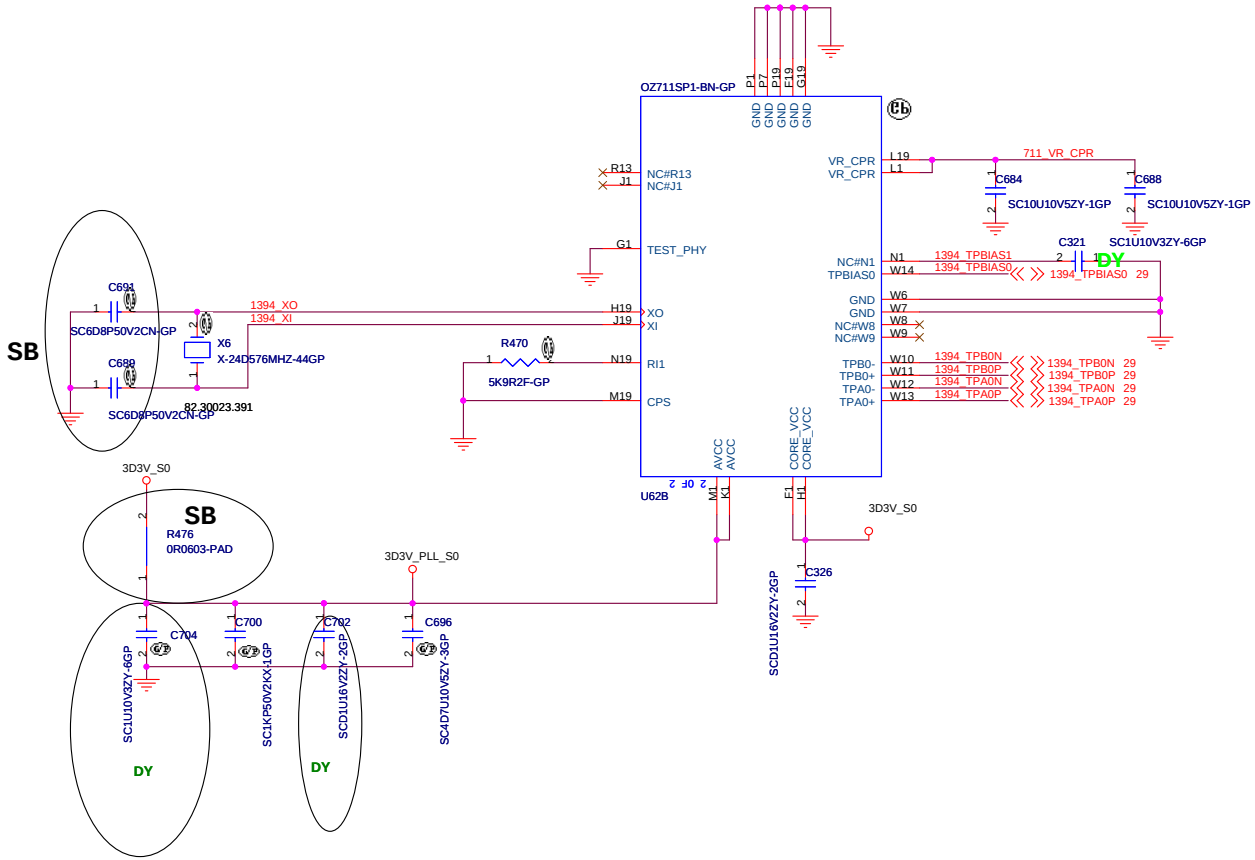
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
A3	Pomona/Texcoco	1

Date: Thursday, March 29, 2007 Sheet 26 of 49

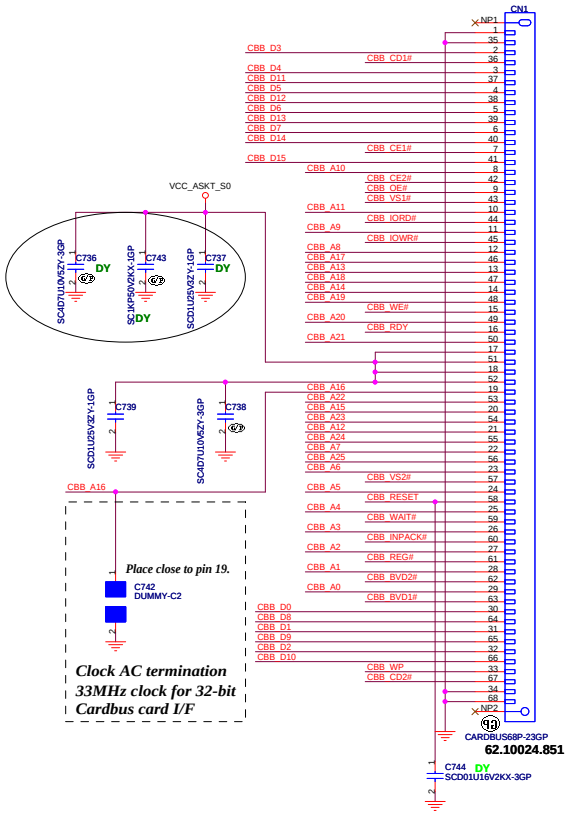

For EMI
PCIRST
Power switch
OZ711SP1-BN-GP
CP2211F-GP
2ND = 74.02211.A79
PME#, CLKRUN#, IRQSER# AND INTA#
MUST BE PULLED-UP ON THE MLB.
DY
SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
UMA
OZ711SP1 (1 of 2)
Pomona/Texcoco
Rev 1
Thursday, March 29, 2007
Sheet 27 of 49



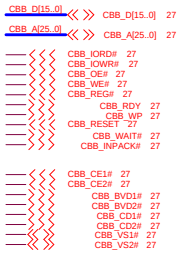
UMA

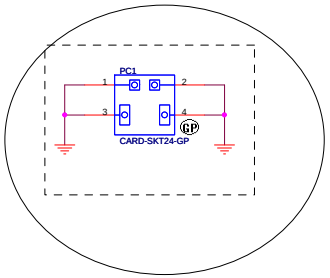
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*OZ711SP1 (2 of 2)*	
Size	Document Number **Pomona/Texcoco**	Rev 1
Date: Thursday, March 29, 2007	Sheet 28 of 49	

PCMCIA Socket

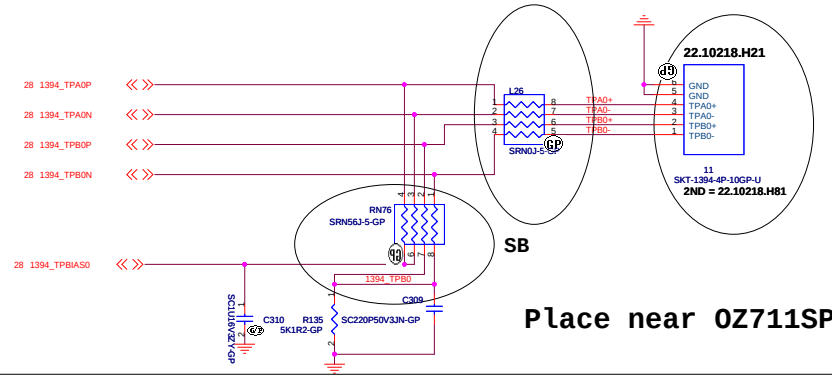


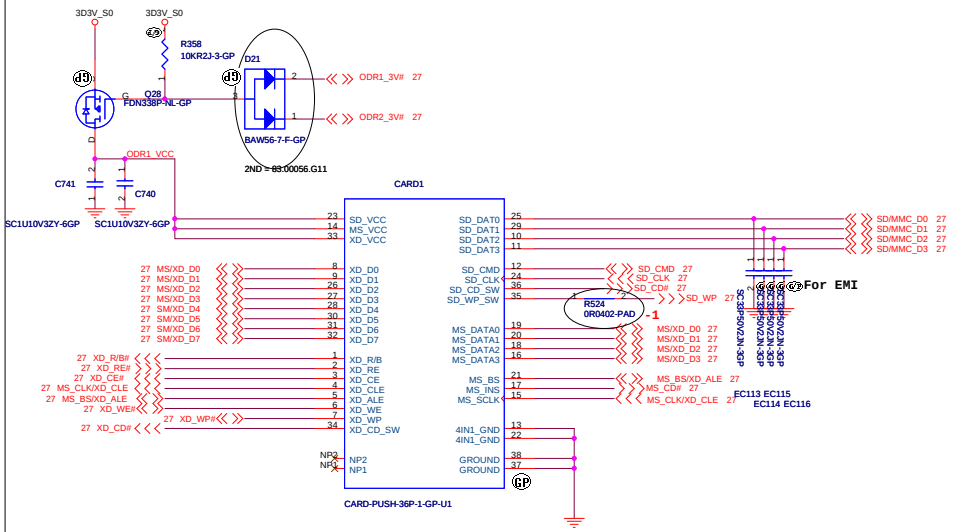
Cardbus I/F





1394 Connector





XD
MS / MS PRO
SD / SD IO / MMC

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

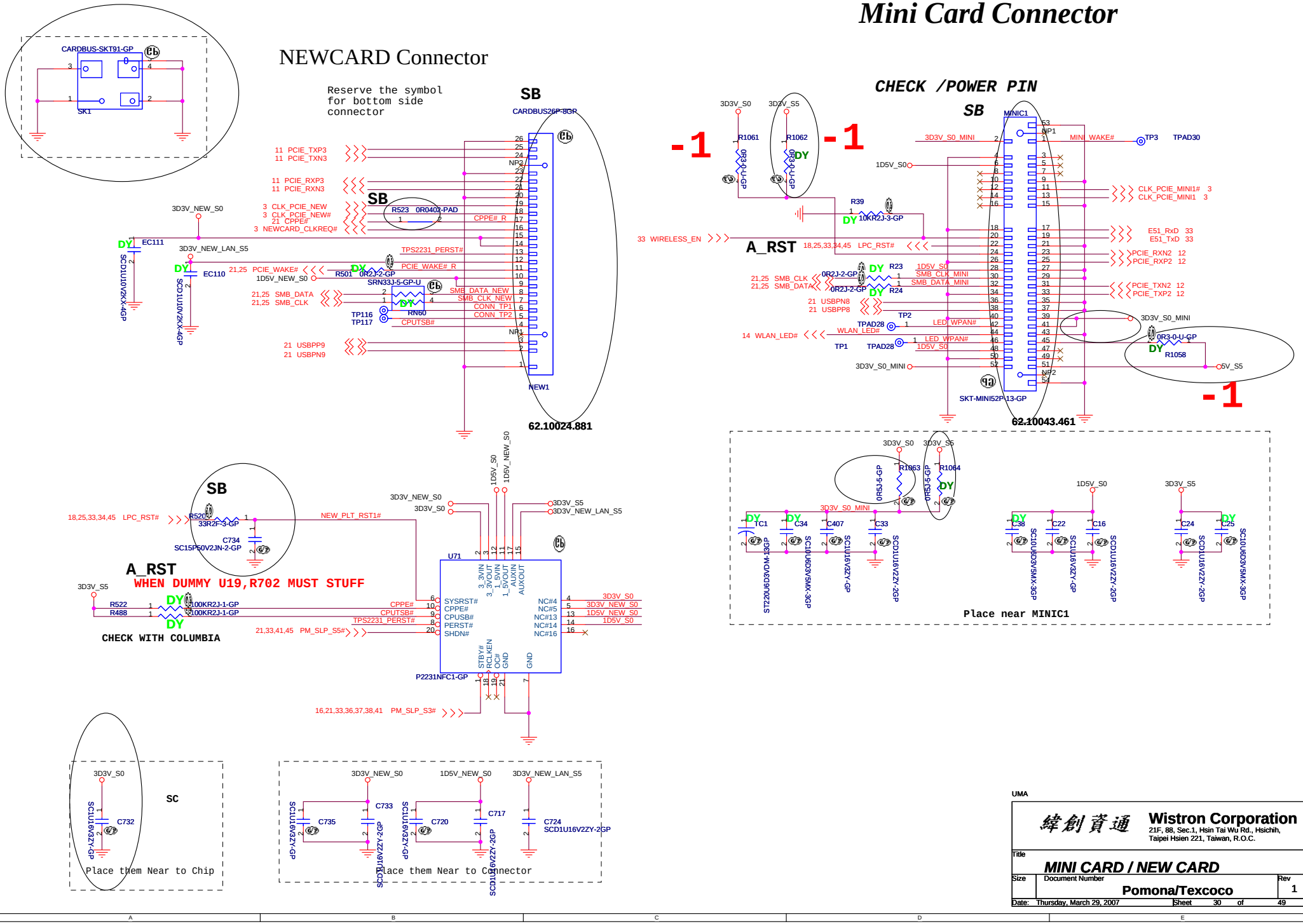
Title: *PCMCIA / 1394 / CARD READER*

Size	Document Number	Rev
	Pomona/Texcoco	1

Date: Thursday, March 29, 2007 Sheet 29 of 49

Mini Card Connector

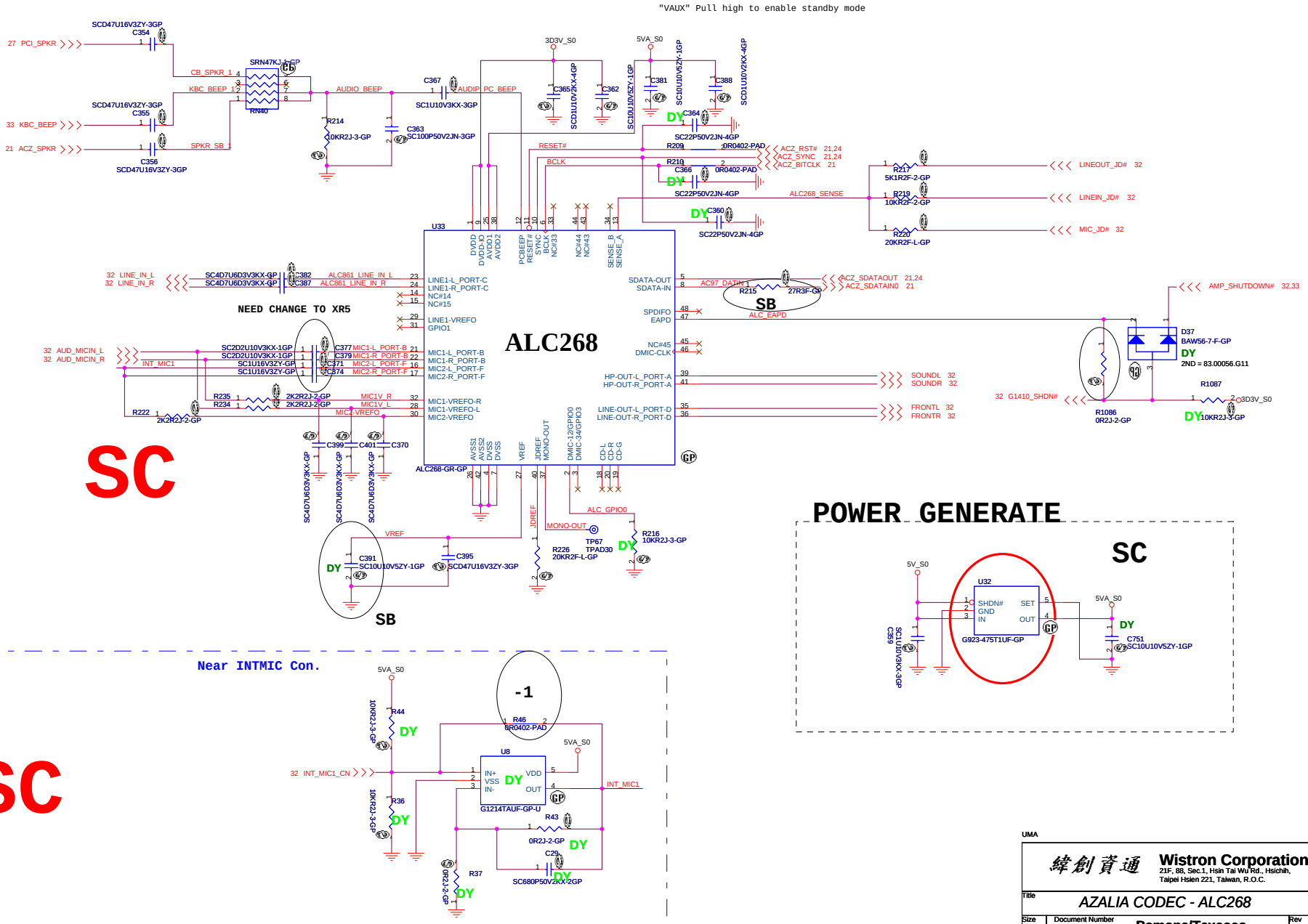
NEWCARD Connector



CHECK /POWER PIN

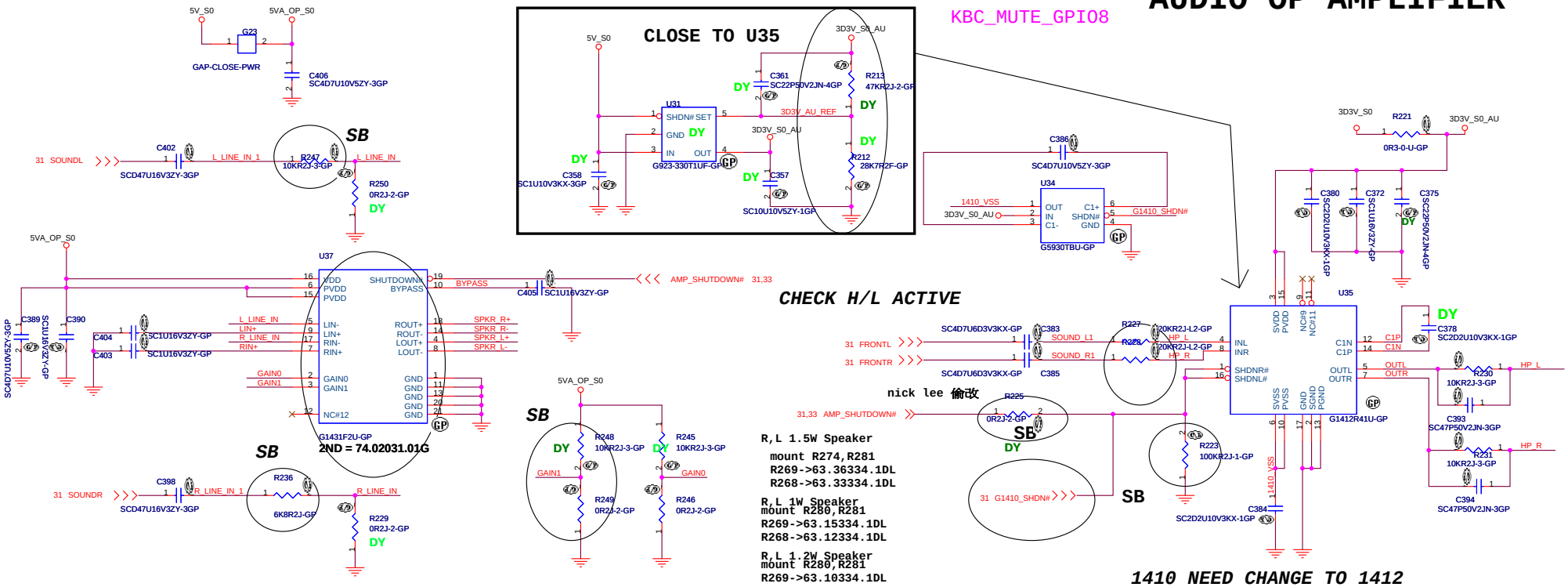
UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD / NEW CARD		
Size	Document Number: Pomona/Texcoco	Rev: 1
Date: Thursday, March 29, 2007	Sheet 30 of 49	

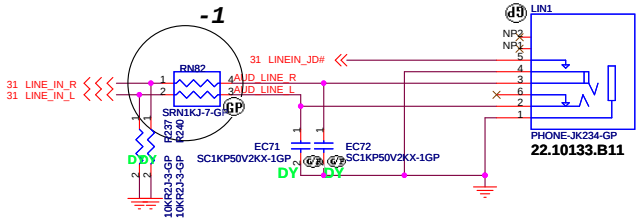

"VAUX" Pull high to enable standby mode
ALC268
U33
ALC268-GR-GP
NEED CHANGE TO XR5
SC
SB
SC
SB
POWER GENERATE
SC
Near INTMIC Con.
SC
U8
G1214TAUF-GP-U
U32
G923-475T1UF-GP
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AZALIA CODEC - ALC268
Size
Document Number
Pomona/Texcoco
Rev
1
Date: Thursday, March 29, 2007
Sheet 31 of 49

AUDIO OP AMPLIFIER

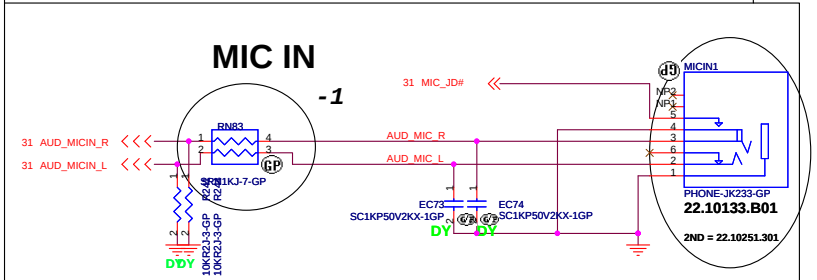
KBC_MUTE_GPIO8



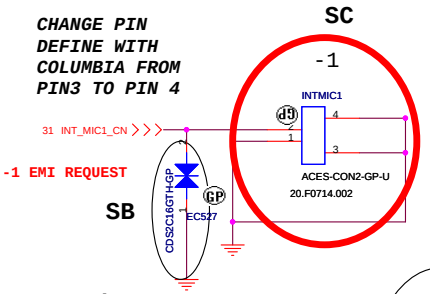
LINE IN



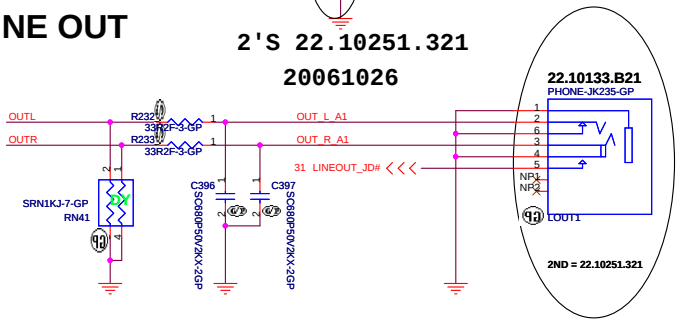
MIC IN



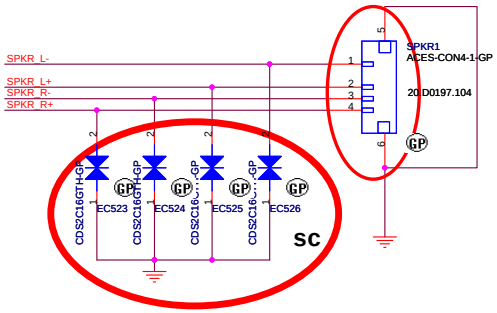
Internal Microphone



LINE OUT

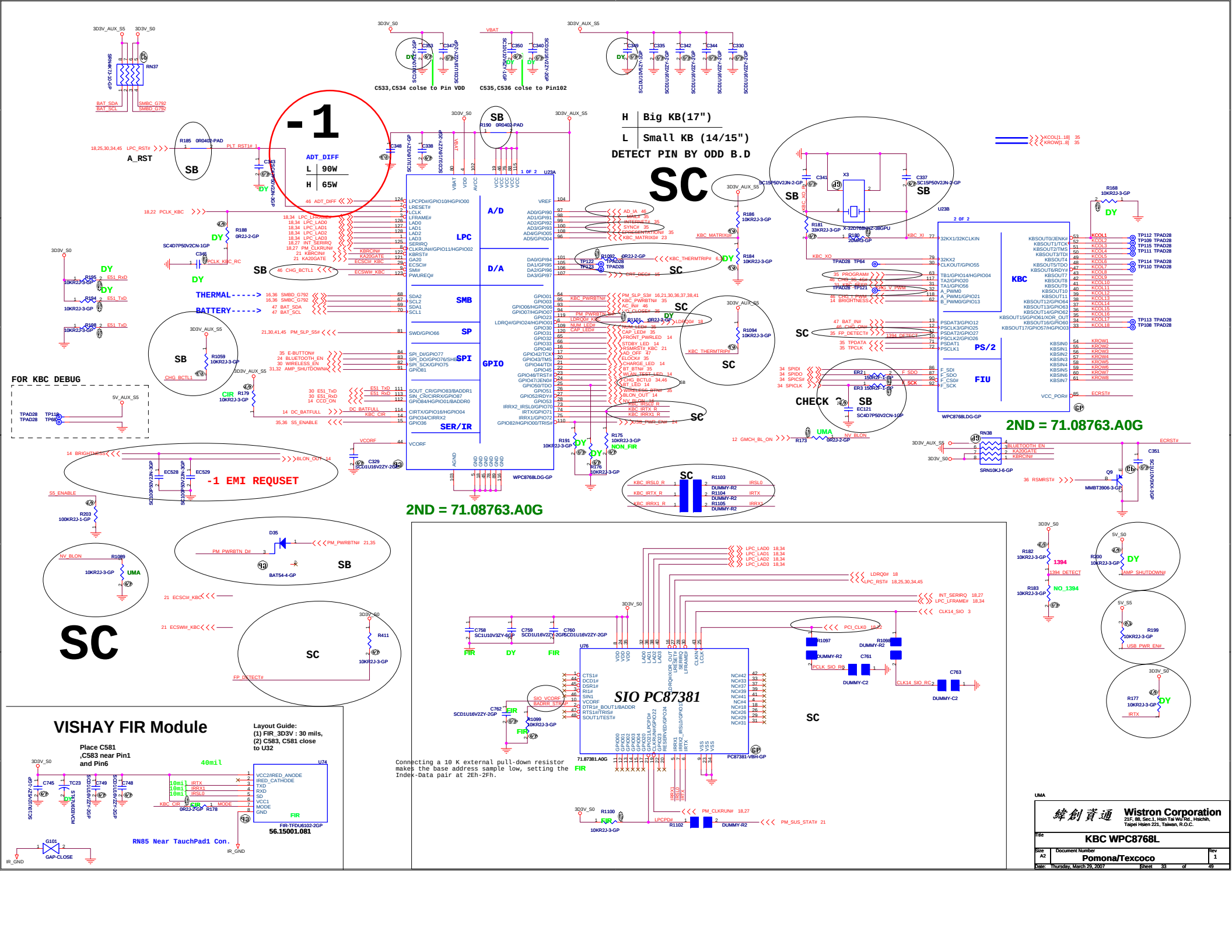


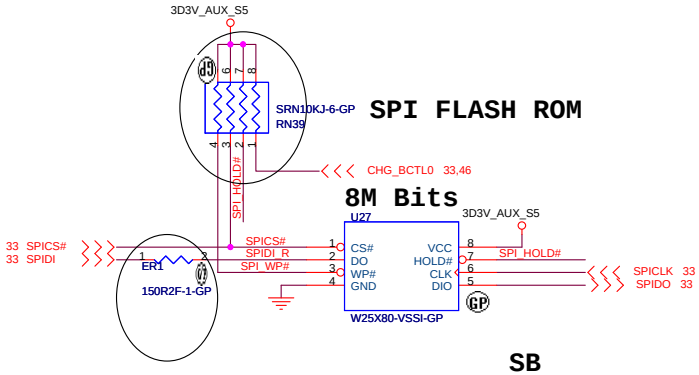
Internal Speaker

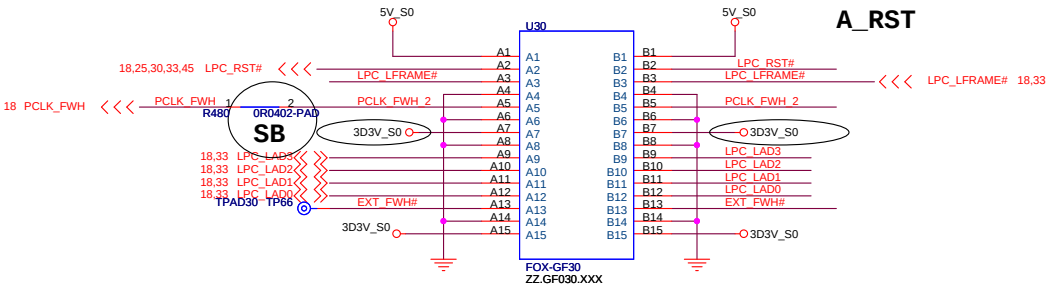


UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO AMP AND JACK		
Size	Document Number: Pomona/Texcoco	Rev: 1
Date: Thursday, March 29, 2007	Sheet 32 of 49	


-1
ADT_DIFF
L 90W
H 65W
H Big KB(17")
L Small KB (14/15")
DETECT PIN BY ODD B.D
SC
A_RST
C533,C534 colse to Pin VDD
C535,C536 colse to Pin102
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
THERMAL-----> 16,36 SMBD_G792 16,36 SMBC_G792
BATTERY-----> 47 BAT_SDA 47 BAT_SCL
FOR KBC DEBUG
-1 EMI REQUSET
2ND = 71.08763.A0G
2ND = 71.08763.A0G
SC
SC
SC
SC
SC
SC
SC
SC
SIO PC87381
71.87381.A0G
PC87381-VBH-GP
WPC8768LDG-GP
WPC8768LDG-GP
SRN4K/2.10-GP
SRN10KJ-6-GP
VISHAY FIR Module
Place C581 ,C583 near Pin1 and Pin6
Layout Guide:
(1) FIR_3D3V : 30 mils, (2) C583, C581 close to U32
40mil
RN85 Near TauchPad1 Con.
FIR-TFDU6102-2GP
56.15001.081
Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
Pomona/Texcoco
Date: Thursday, March 29, 2007
Sheet 33 of 49





GOLDEN FINGER FOR DEBUG BOARD
Check;MYALL M

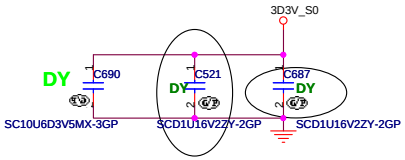
TOP VIEW

A15	(B1)
A14	(B2)
⋮	
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

1. Add serial resistor 150 Ohm and Bypass Cap 4.7P on SPI_CLK(Close to KBC)
2. Add serial resistor 150 Ohm on SPI_DO(Close to KBC)
3. Add serial resistor 150 Ohm on SPI_DI(Close to SPI Flash)

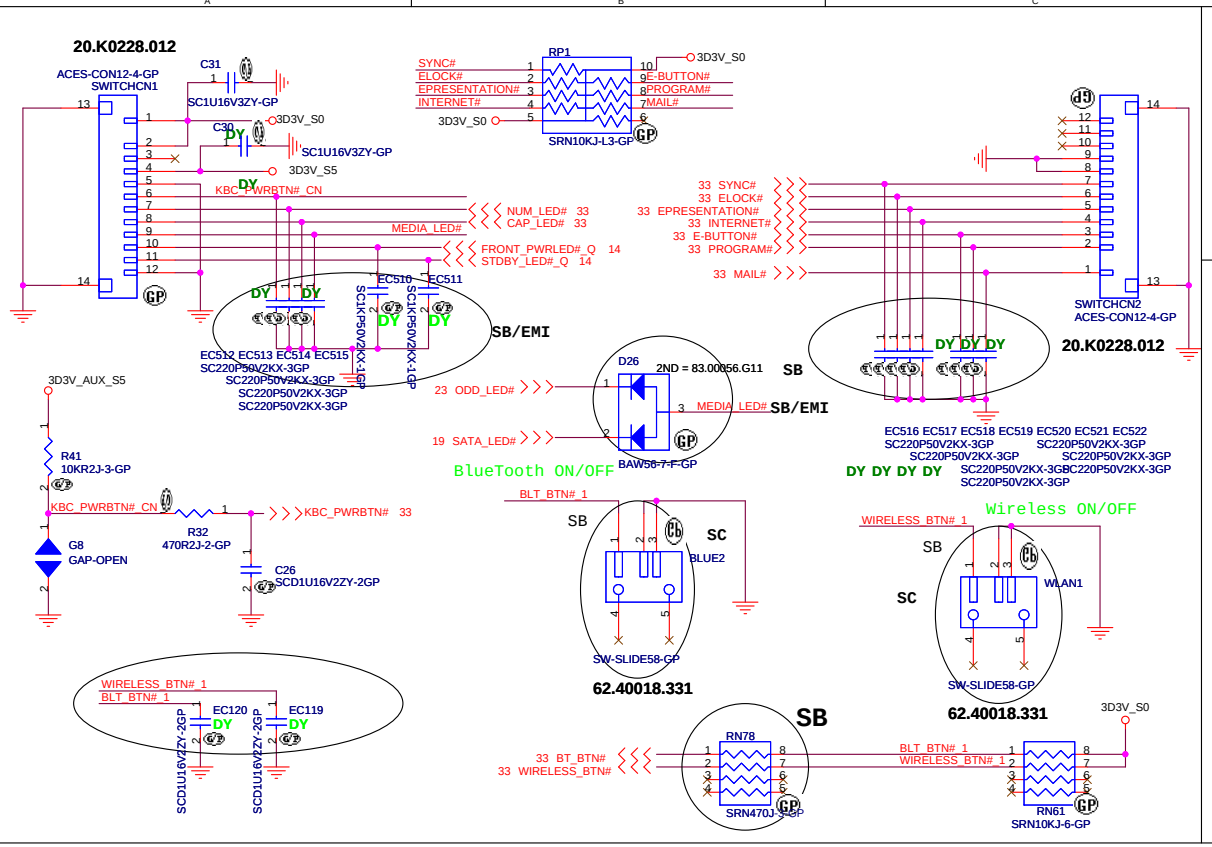
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



UMA

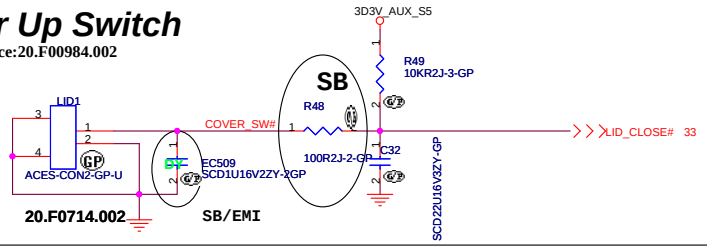
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BIOS	
Size A3	Document Number Pomona/Texcoco	Rev 1
Date: Thursday, March 29, 2007	Sheet 34 of 49	

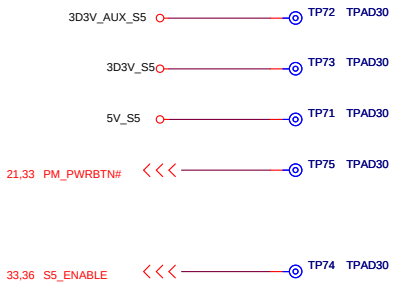


Cover Up Switch

2nd source:20.F00984.002



Check test point



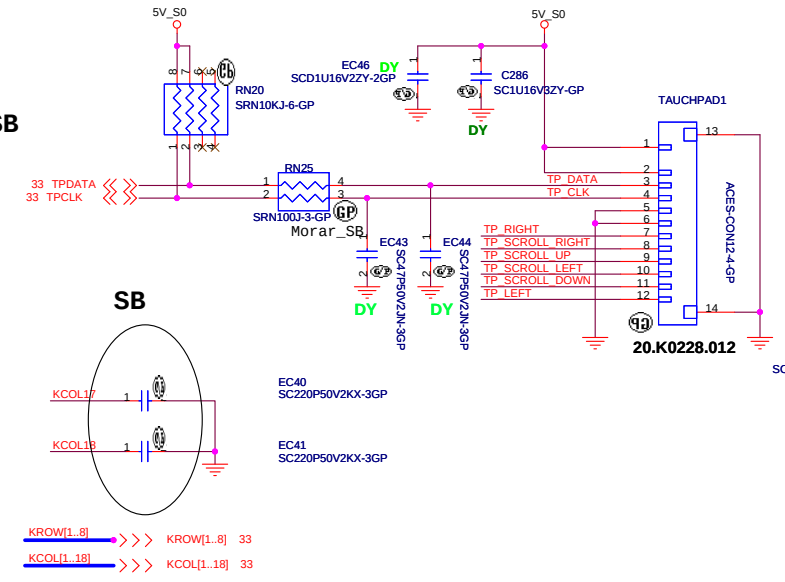
Test Point放在Dimm Door打開可量測處

Internal KeyBoard CONN

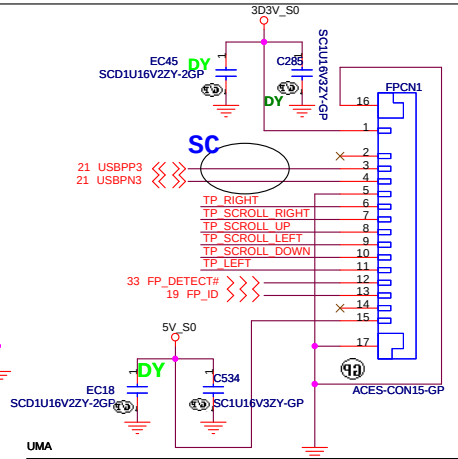
CHECK KB SPEC. AND PIN DEFINE

EMI Bypass cap.

SB

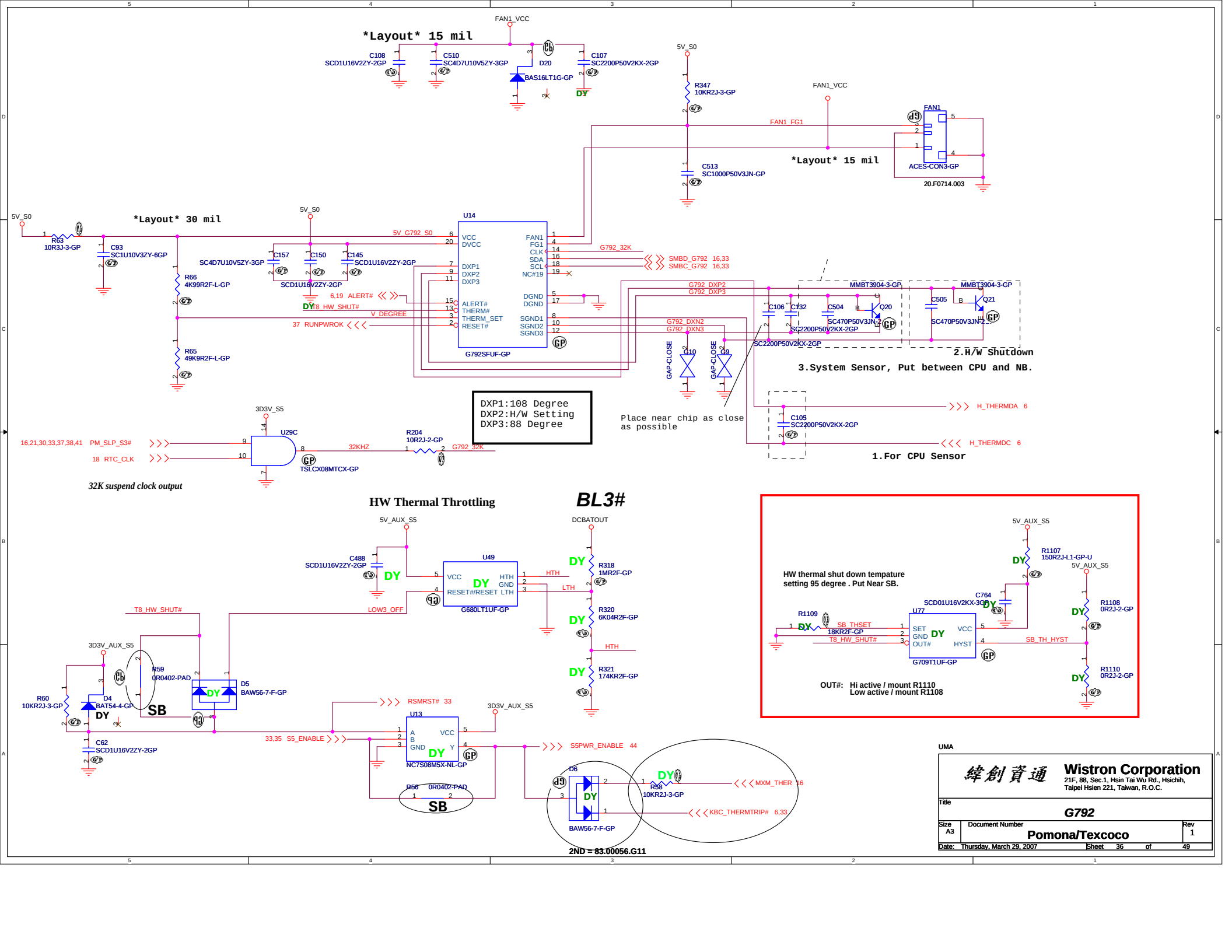


SB



UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BUTTONs / KB / TOUCHPAD	
Size	Document Number: Pomona/Texcoco	Rev: 1
Date: Thursday, March 29, 2007	Sheet 35 of 49	


Layout 15 mil
FAN1_VCC
C108 SCD1U16V2ZY-2GP
C510 SC4D7U10V5ZY-3GP
D20 BAS16LT1G-GP
C107 SC2200P50V2KX-2GP
DY
5V_S0
R347 10KR2J-3-GP
C513 SC1000P50V3JN-GP
FAN1_FG1
FAN1
ACES-CON3-GP
20.F0714.003
Layout 15 mil
Layout 30 mil
R63 10R3J-3-GP
C93 SC1U10V3ZY-6GP
R66 4K99R2F-L-GP
R65 49K9R2F-L-GP
C157 SC4D7U10V5ZY-3GP
C150
C145 SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
5V_G792_S0
U14
VCC DVCC
DXP1 DXP2 DXP3
ALERT# THERM# THERM_SET RESET#
FAN1 FG1 CLK SDA SCL NC#19
DGND DGND
SGND1 SGND2 SGND3
G792SFUF-GP
G792_32K
SMBD_G792 16,33
SMBC_G792 16,33
6,19 ALERT#
T8_HW_SHUT#
V_DEGREE
37 RUNPWROK
G792_DXP2
G792_DXP3
G792_DXN2
G792_DXN3
MMBT3904-3-GP
C106
C132
C504 SC470P50V3JN-2GP
Q20
SC2200P50V2KX-2GP
C505 SC470P50V3JN-2GP
Q21
SC2200P50V2KX-2GP
GAP-CLOSE
G10
G9
2.H/W Shutdown
3.System Sensor, Put between CPU and NB.
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
C109 SC2200P50V2KX-2GP
H_THERMDA 6
H_THERMDC 6
1.For CPU Sensor
3D3V_S5
U29C
TSLCX08MTCX-GP
16,21,30,33,37,38,41 PM_SLP_S3#
18 RTC_CLK
32KHZ
R204 10R2J-2-GP
G792_32K
32K suspend clock output
HW Thermal Throttling
BL3#
5V_AUX_S5
C488 SCD1U16V2ZY-2GP
U49
VCC RESET#/RESET
HTH GND LTH
G680LT1UF-GP
DCBATOUT
R318 1MR2F-GP
R320 6K04R2F-GP
R321 174KR2F-GP
HTH
LTH
T8_HW_SHUT#
LOW3_OFF
3D3V_AUX_S5
R59 0R0402-PAD
SB
D5 BAW56-7-F-GP
D4 BAT54-4-GP
R60 10KR2J-3-GP
C62 SCD1U16V2ZY-2GP
RSMRST# 33
33,35 S5_ENABLE
U13
NC7S08M5X-NL-GP
R56 0R0402-PAD
S5PWR_ENABLE 44
D6
BAW56-7-F-GP
R58 10KR2J-3-GP
MXM_THER 16
KBC_THERMTRIP# 6,33
2ND = 83.00056.G11
HW thermal shut down tempature setting 95 degree . Put Near SB.
R1109
SB_THSET 18KR2F-GP
U77
SET GND OUT# VCC HYST
G709T1UF-GP
C764 SCD01U16V2KX-3GP
R1107 150R2J-L1-GP-U
R1108 0R2J-2-GP
R1110 0R2J-2-GP
SB_TH_HYST
OUT#: Hi active / mount R1110
Low active / mount R1108
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G792
Size A3
Document Number
Pomona/Texcoco
Rev 1
Date: Thursday, March 29, 2007
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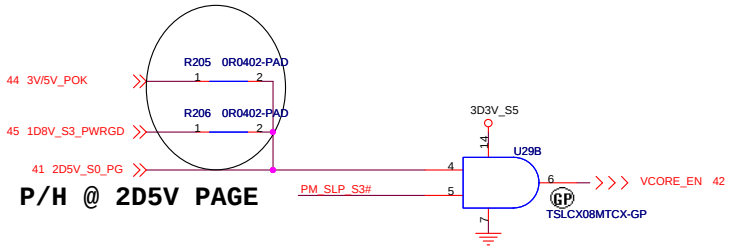

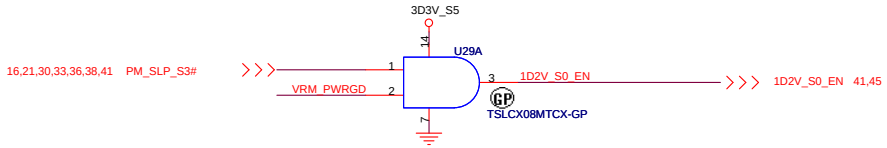

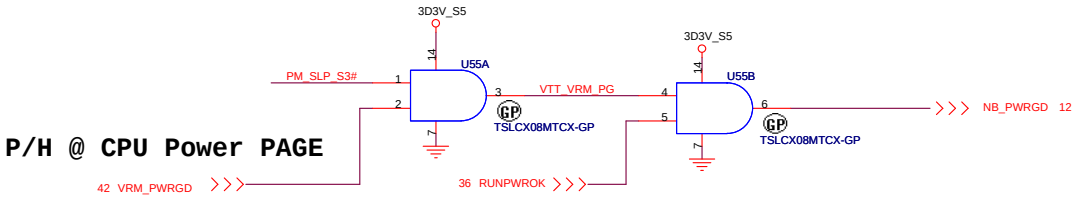

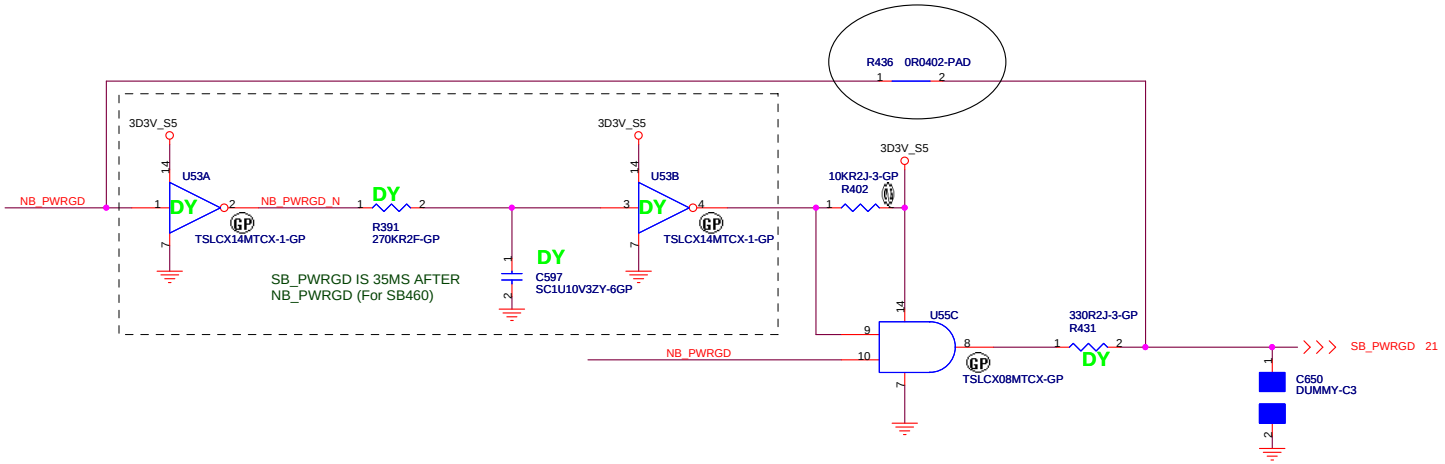

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWERGOOD&ENABLES(1/2)***

Size	Document Number	Rev
A3	Pomona/Texcoco	1

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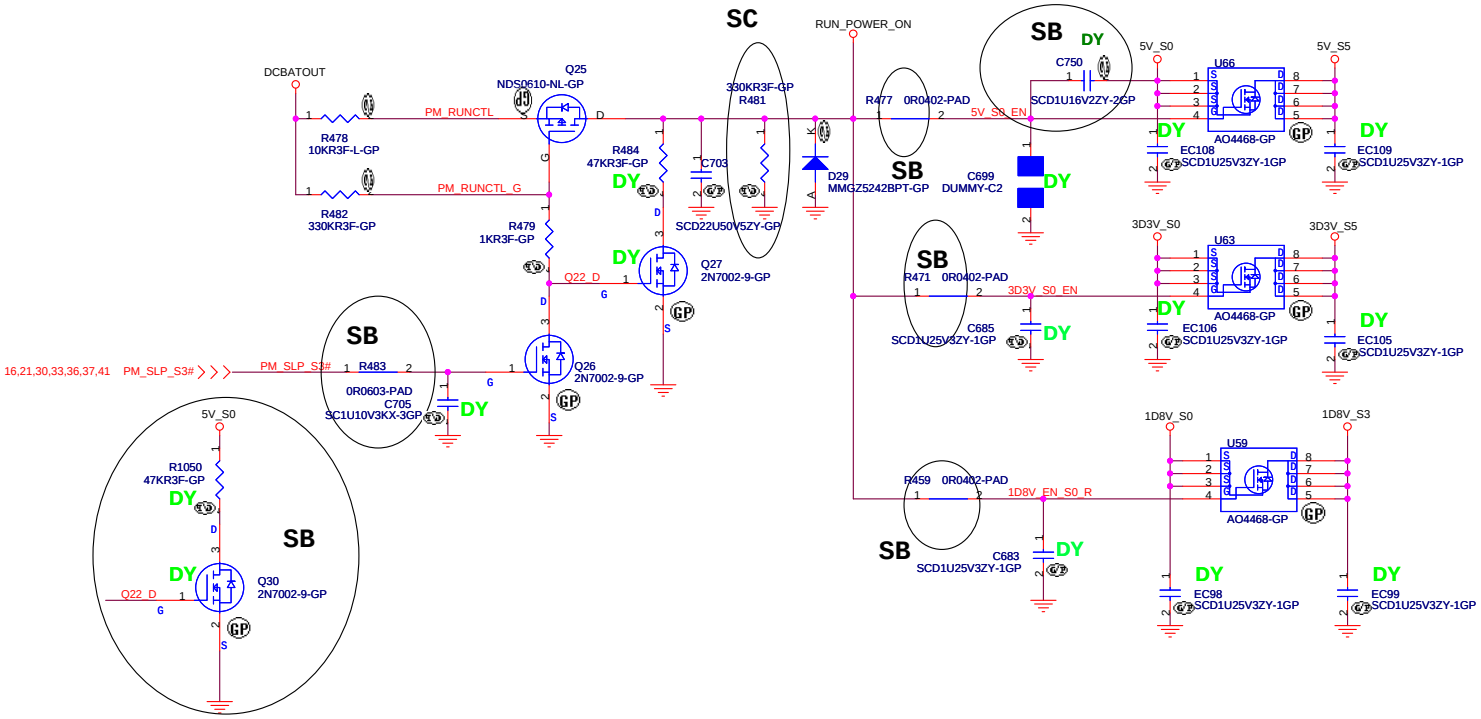
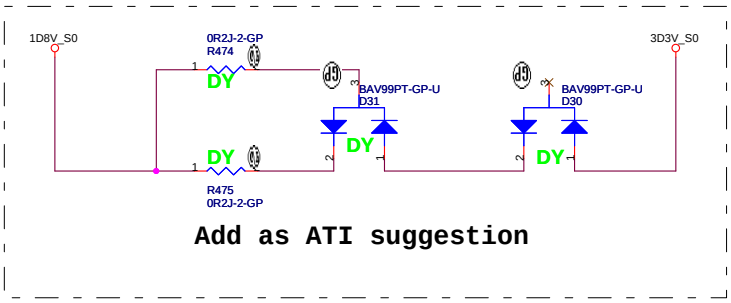
Run Power Switch





UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *PWR CTL LOGIC / PWR PLANE*		
Size: A3	Document Number: Pomona/Texcoco	Rev: 1
Date: Thursday, March 29, 2007	Sheet 38 of 49	

CPU_CORE
ISL6264CRZ

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TI TPS51120
3D3V/5V

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

DCBATOUT_51120

Input Power
VIN
REG5V_IN(I / 5V)

Output Power
5V_AUX_S5
3D3V_AUX_S5
5V(O)
5V_S5 (5.4A)
3D3V(O)
3D3V_S5 (4A)

2D5V_S0

3D3V_S0 — INPUT / OUT — 2D5V_S0

APL5913

1D8V_S5

3D3V_S5 — INPUT / OUT — 1D2V_S5

APL5332KAC-TRLGP

Adapter

Input Signal
AD_OFF
(I)

Output Signal
(O)
AD_IN

Input Power
AD_JK
VCC(I)
5V_AUX_S5
VCC(I)

Output Power
VCC(O)
AD+

Charger_ISL6255

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

AD_IN
CHARGE_LED#
BL2#

Output Power
VCC (O)
VCC (O)

DCBATOUT
BT+

Input Power
DCIN (I)

AD+

TI TPS51116
1.8V / 0.9V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
DCBATOUT
VCC(I)
5V_S5
VCC(I)

Output Power
VCC(O)
1.8V_S3
VCC(O)
0.9V_S3

ISL6268_1D2V

1D2V_S0_EN

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Output Power
1D2V_PWR

1D2V (6.5A)

5V_S5
DCBATOUT

Input Power
VCC
VIN

ISL6268_VGA_CORE

VGA_CORE_EN

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Output Power
1D2V_PWR

VGA_CORE_S0 (15A)

5V_S5
DCBATOUT

Input Power
VCC
VIN

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	Pomona/Texcoco	1

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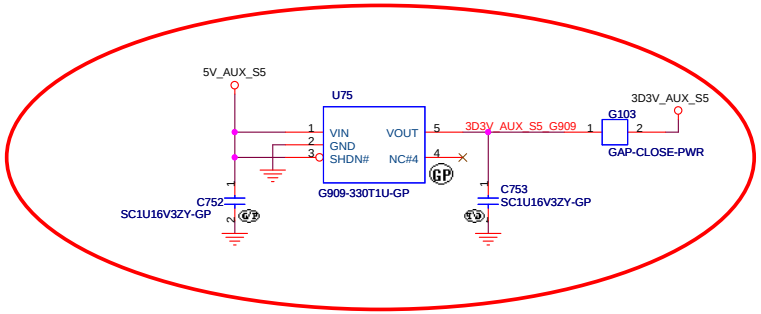
Aux Power 3D3V_AUX_S5

Aux Power 3D3V_AUX_S5



SB modify

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3D3V_AUX

Size: A3 | Document Number: Pomona/Texcoco | Rev: 1

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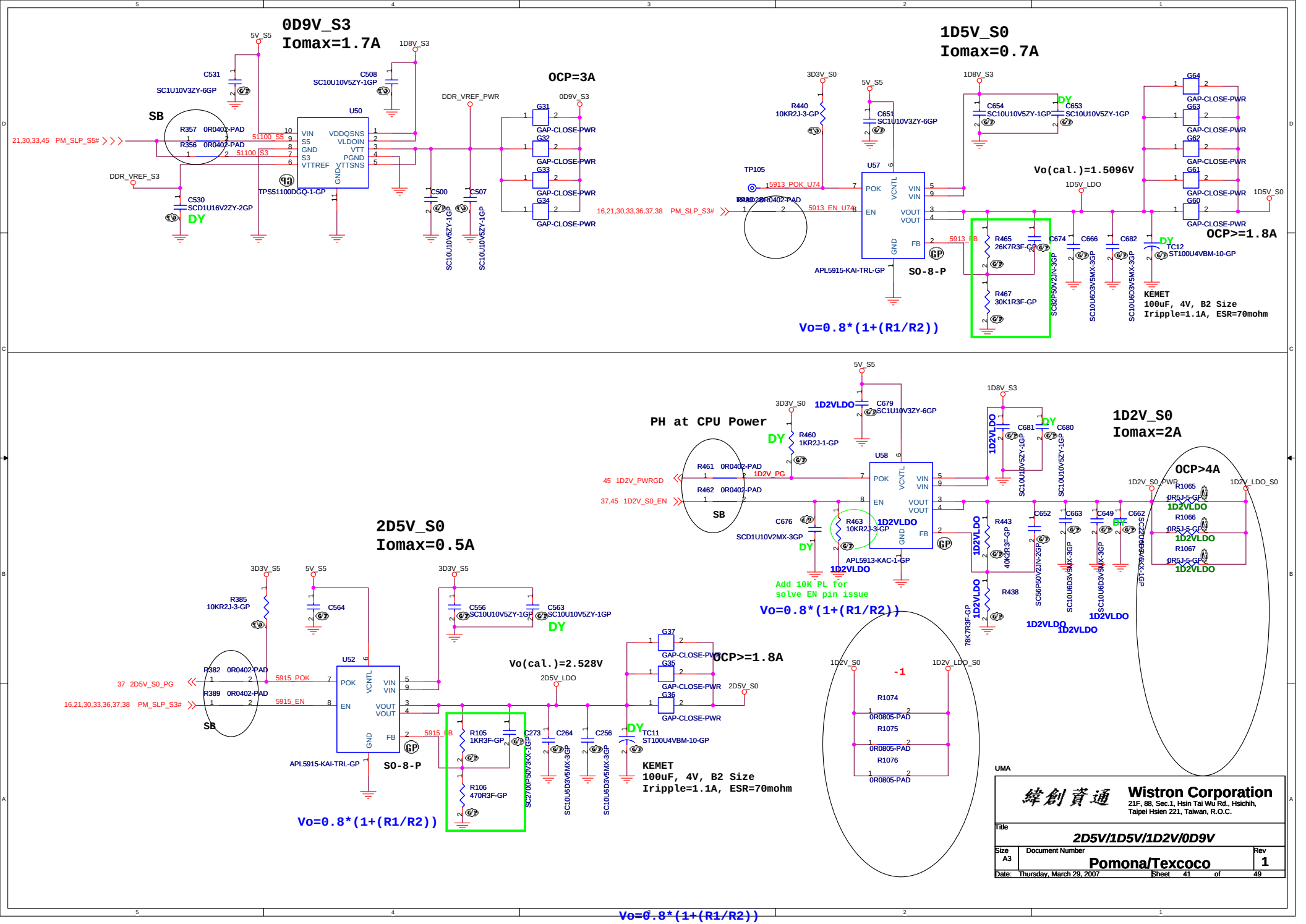

0D9V_S3
Iomax=1.7A
OCP=3A
1D5V_S0
Iomax=0.7A
Vo(cal.)=1.5096V
OCP>=1.8A
Vo=0.8*(1+(R1/R2))
KEMET
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm
APL5915-KAI-TRL-GP
SO-8-P
TPS51100DGQ-1-GP
2D5V_S0
Iomax=0.5A
Vo(cal.)=2.528V
OCP>=1.8A
1D2V_S0
Iomax=2A
OCP>4A
PH at CPU Power
Add 10K PL for
solve EN pin issue
Vo=0.8*(1+(R1/R2))
High(3D3V)=> Vout=1.2V
Low(0V) => Vout=1.0V
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
2D5V/1D5V/1D2V/0D9V
Pomona/Texcoco
Rev 1
Thursday, March 29, 2007
Sheet 41 of 49

CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375

SB
20061109

SET "H"-->Audio filter

RBIAS=1.55V
Inner 3K ohm

Positive offset:
(1.2V/R7)*R11

OCP:40A*1.25=50A
50A*2mV/A=10uA*Rocset
Rocset=10K

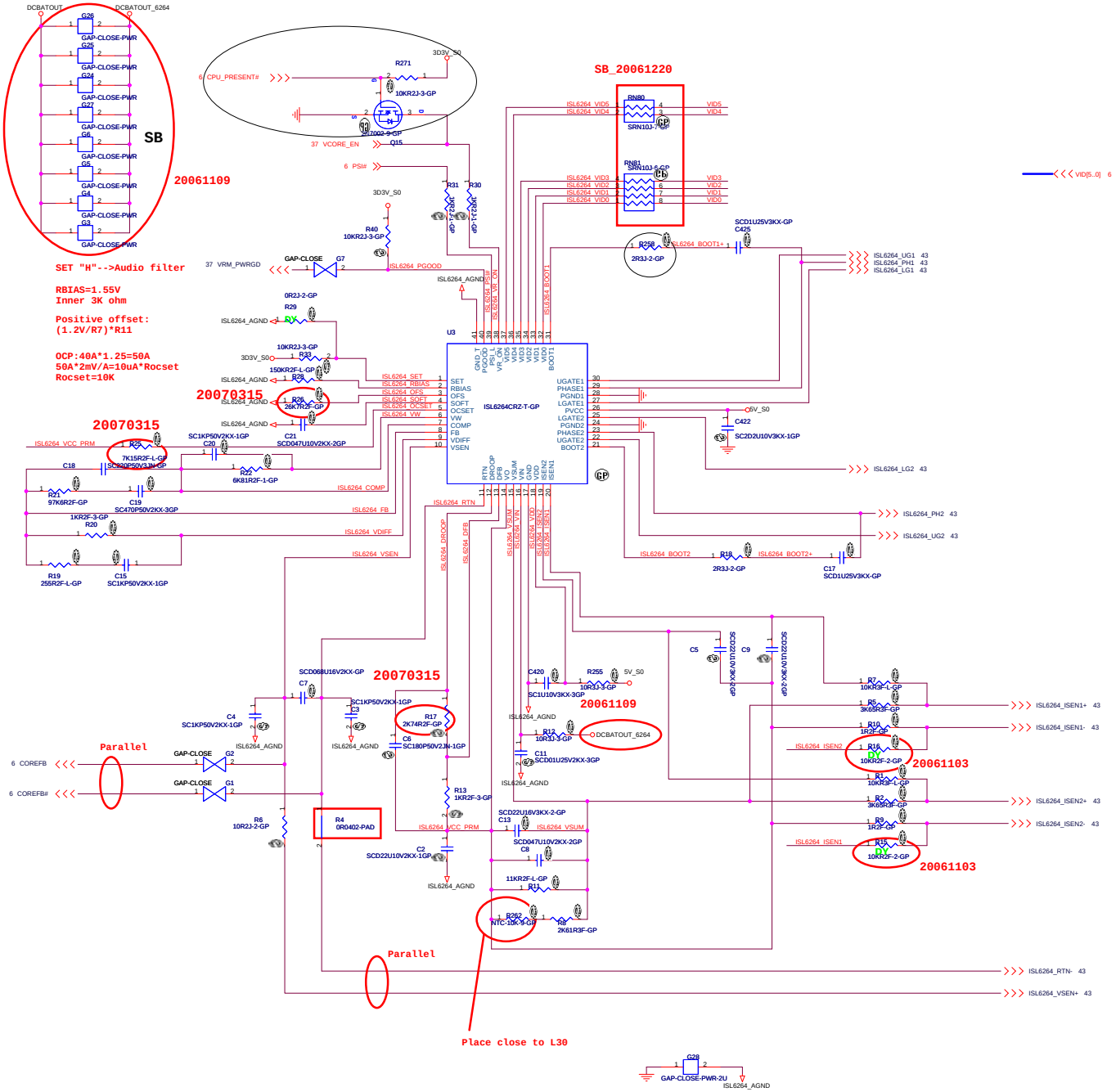
SB_20061220

20070315

20061109

Parallel

Place close to L30



UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_1

Size: A2 | Document Number: Pomona/Texcoco | Rev: 1

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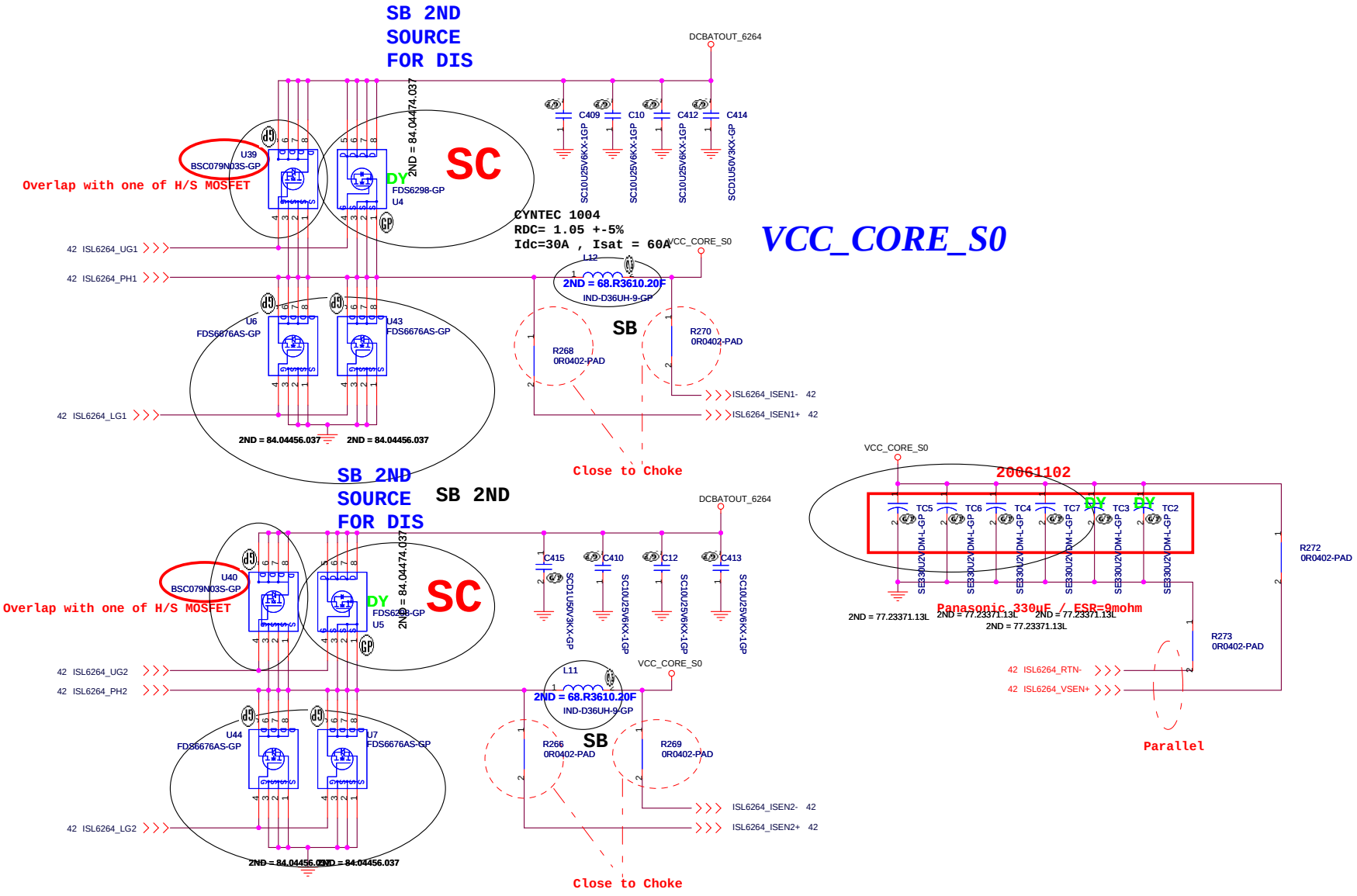

UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU Vcore Power_2		
Size: A3	Document Number: Pomona/Texcoco	Rev: 1
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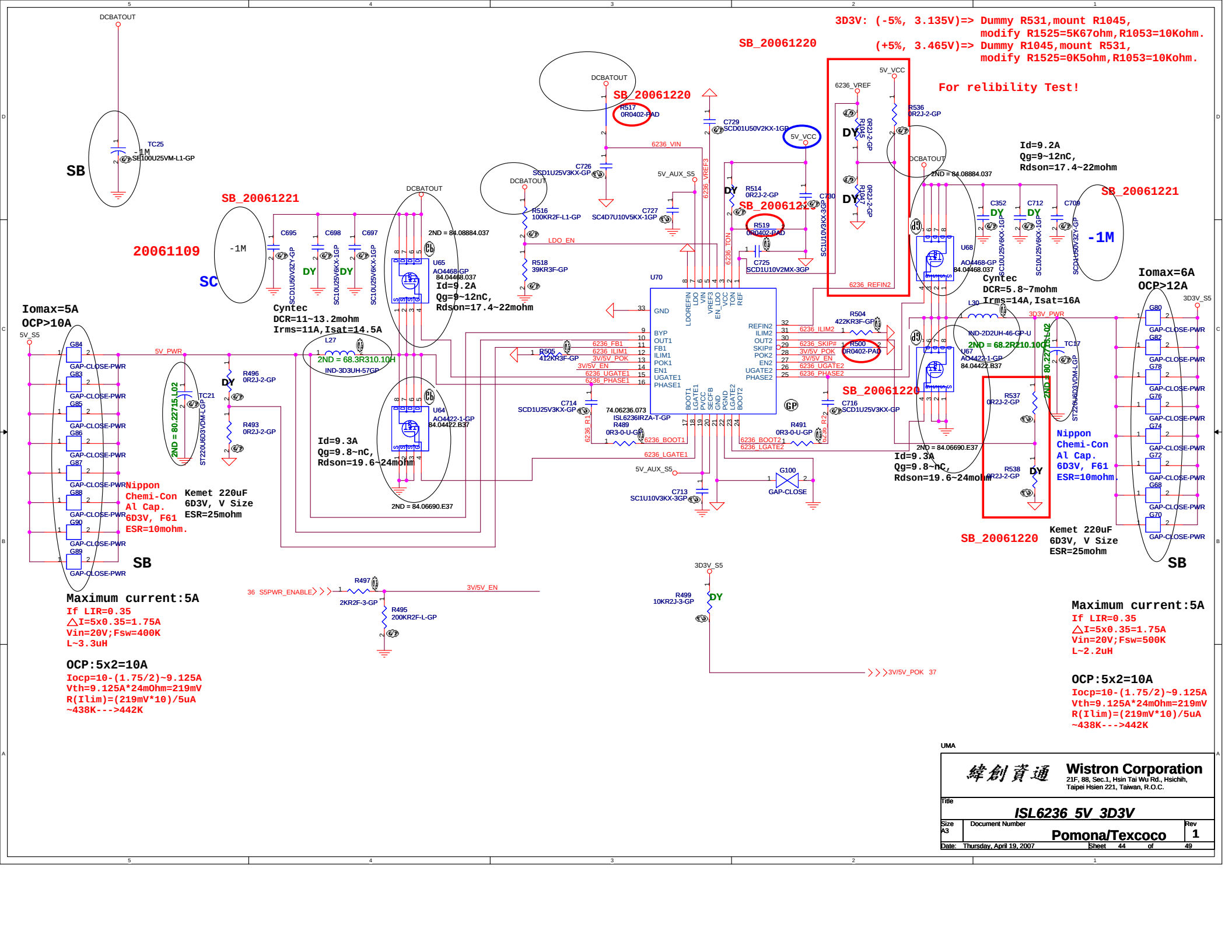
3D3V: (-5%, 3.135V)=> Dummy R531,mount R1045, modify R1525=5K67ohm,R1053=10Kohm.
(+5%, 3.465V)=> Dummy R1045,mount R531, modify R1525=0K5ohm,R1053=10Kohm.
For relibility Test!
SB_20061220
SB_20061221
20061109
SC
SB
DY
-1M
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
Cyntec
DCR=11~13.2mohm
Irms=11A,Isat=14.5A
Iomax=5A
OCP>10A
Id=9.3A
Qg=9.8~nC,
Rdson=19.6~24mohm
Cyntec
DCR=5.8~7mohm
Irms=14A,Isat=16A
Iomax=6A
OCP>12A
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
Kemet 220uF 6D3V, V Size ESR=25mohm
Maximum current:5A
If LIR=0.35
△I=5x0.35=1.75A
Vin=20V;Fsw=400K
L~3.3uH
OCP:5x2=10A
Iocp=10-(1.75/2)~9.125A
Vth=9.125A*24mOhm=219mV
R(Ilim)=(219mV*10)/5uA
~438K--->442K
Maximum current:5A
If LIR=0.35
△I=5x0.35=1.75A
Vin=20V;Fsw=500K
L~2.2uH
OCP:5x2=10A
Iocp=10-(1.75/2)~9.125A
Vth=9.125A*24mOhm=219mV
R(Ilim)=(219mV*10)/5uA
~438K--->442K
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ISL6236_5V_3D3V
Pomona/Texcoco
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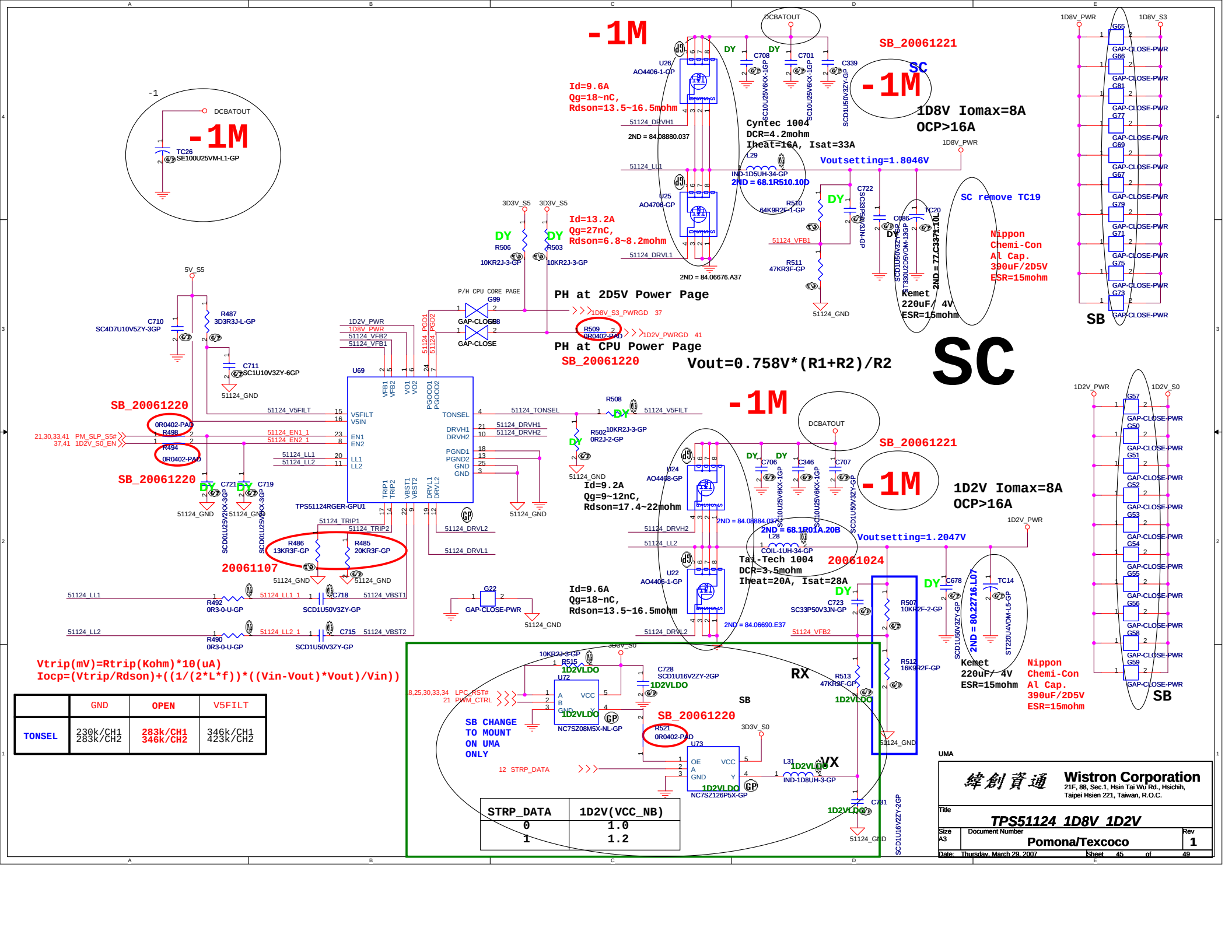

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V_1D2V

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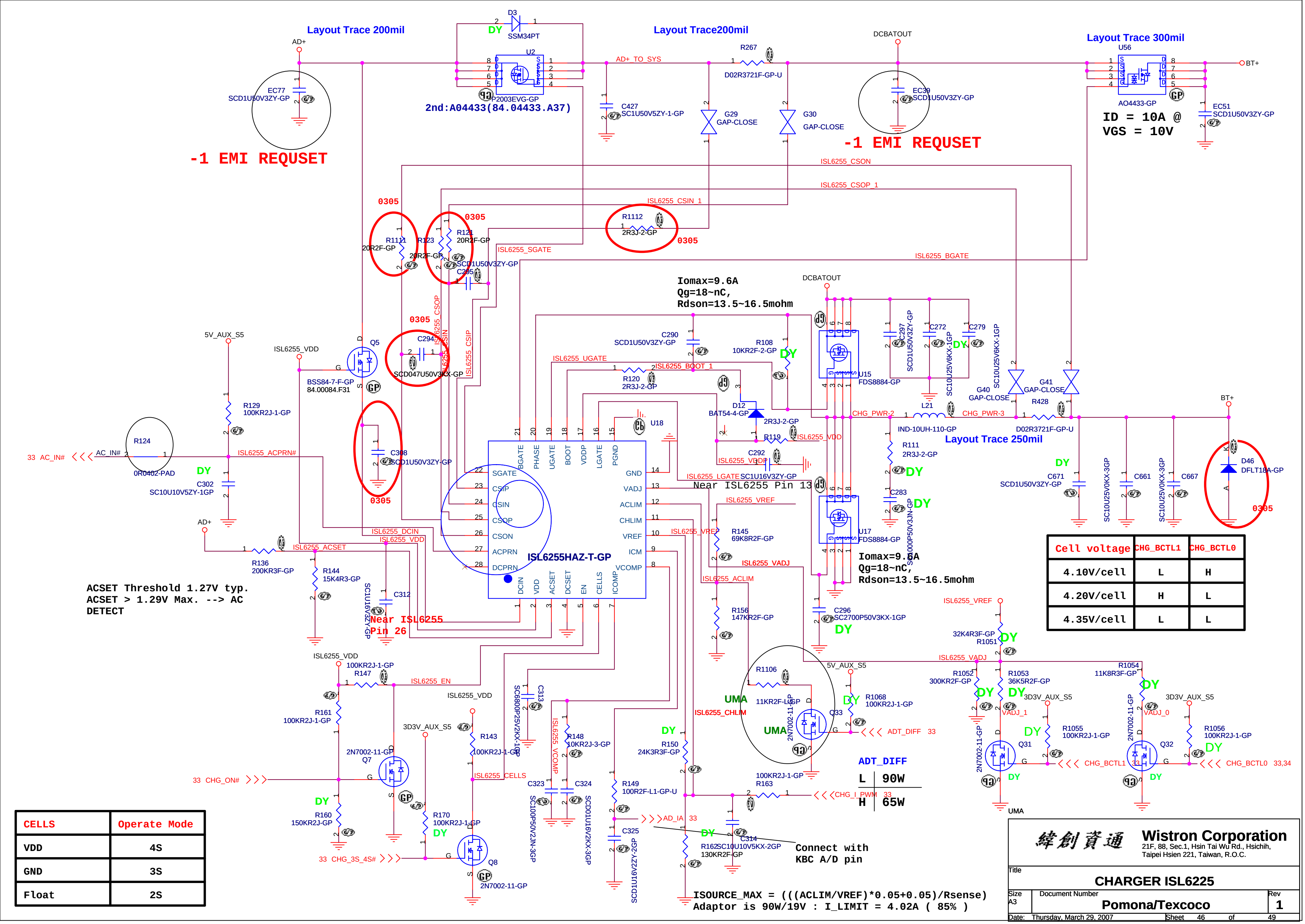

ACSET Threshold 1.27V typ.
ACSET > 1.29V Max. --> AC
DETECT

ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 90W/19V : I_LIMIT = 4.02A (85%)

ADT_DIFF	
L	90W
H	65W

Cell voltage	CHG_BCTL1	CHG_BCTL0
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL6225

Size: A3 | Document Number: Pomona/Texcoco | Rev: 1

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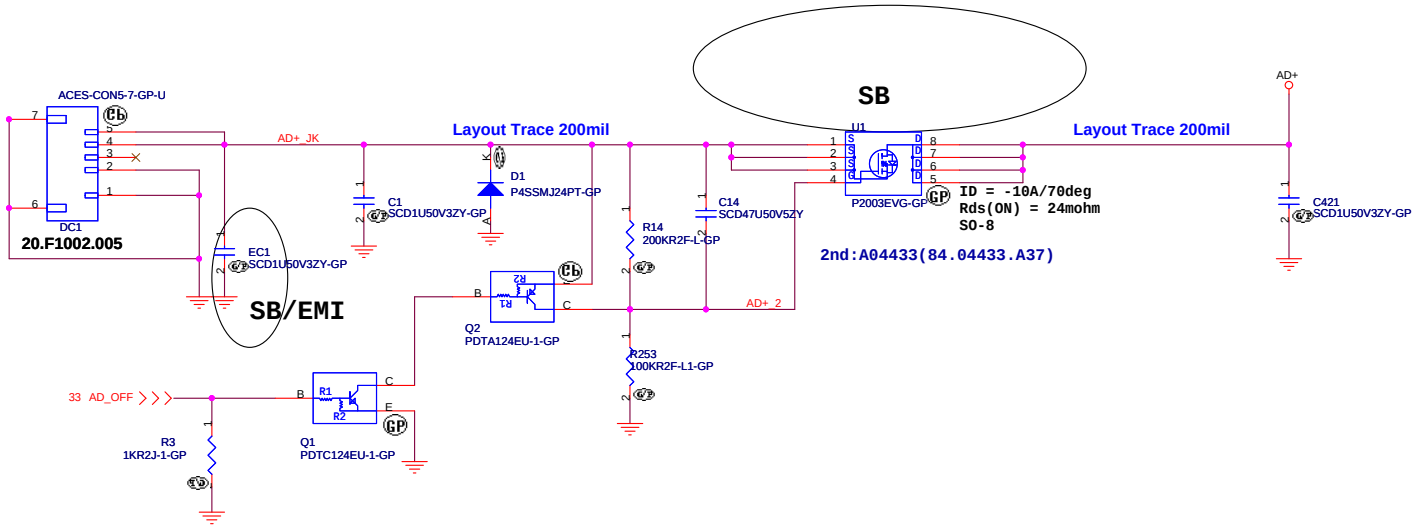
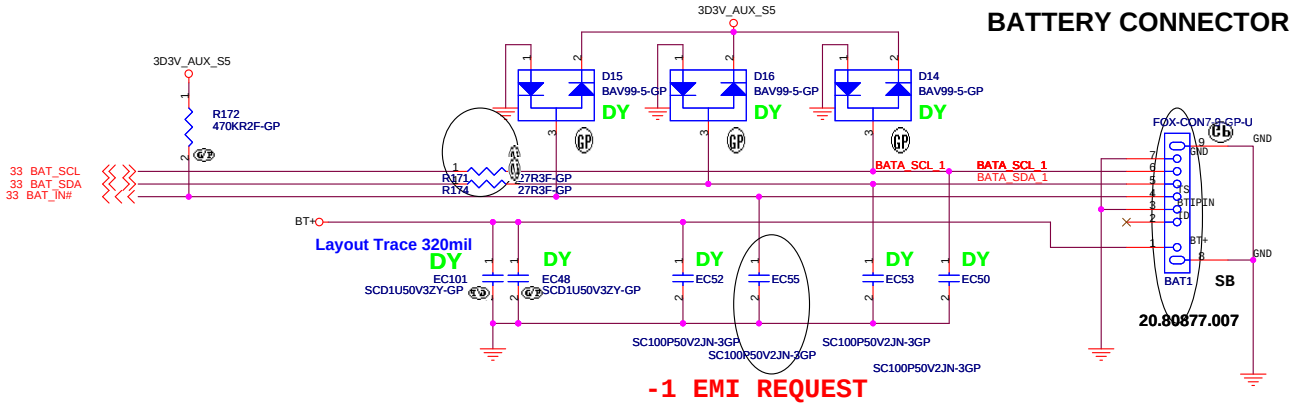
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



-1 EMI REQUEST

SC NEED CHANGE TO 83.00018.0AF

SC

UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AD/BATT CONN		
Size: A3	Document Number: Pomona/Texcoco	Rev: 1
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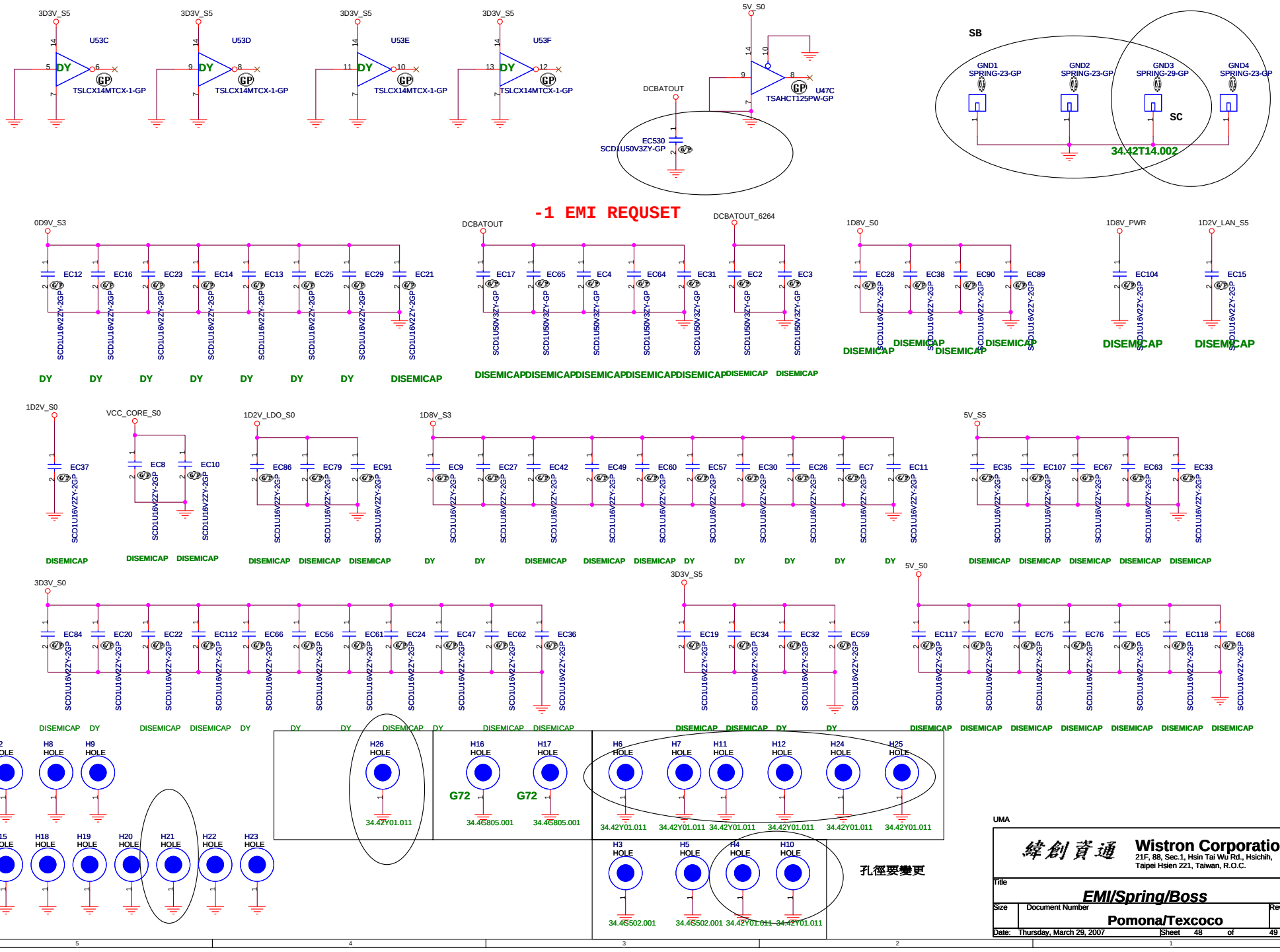
3D3V_S5
U53C
U53D
U53E
U53F
TSLCX14MTCX-1-GP
5V_S0
U47C
TSAHCT125PW-GP
DCBATOUT
EC530
SCD1U50V3ZY-GP
SB
GND1 SPRING-23-GP
GND2 SPRING-23-GP
GND3 SPRING-29-GP
GND4 SPRING-23-GP
SC
34.42T14.002
-1 EMI REQUSET
0D9V_S3
EC12
EC16
EC23
EC14
EC13
EC25
EC29
EC21
SCD1U16V2ZY-2GP
DY
DISEMICAP
DCBATOUT
EC17
EC65
EC4
EC64
EC31
SCD1U50V3ZY-GP
DCBATOUT_6264
EC2
EC3
1D8V_S0
EC28
EC38
EC90
EC89
1D8V_PWR
EC104
1D2V_LAN_S5
EC15
1D2V_S0
EC37
VCC_CORE_S0
EC8
EC10
1D2V_LDO_S0
EC86
EC79
EC91
1D8V_S3
EC9
EC27
EC42
EC49
EC60
EC57
EC30
EC26
EC7
EC11
5V_S5
EC35
EC107
EC67
EC63
EC33
3D3V_S0
EC84
EC20
EC22
EC112
EC66
EC56
EC61
EC24
EC47
EC62
EC36
3D3V_S5
EC19
EC34
EC32
EC59
5V_S0
EC117
EC70
EC75
EC76
EC5
EC118
EC68
H1 HOLE
H2 HOLE
H8 HOLE
H9 HOLE
H13 HOLE
H15 HOLE
H18 HOLE
H19 HOLE
H20 HOLE
H21 HOLE
H22 HOLE
H23 HOLE
H26 HOLE
34.42Y01.011
H16 HOLE
H17 HOLE
G72
34.4G805.001
H6 HOLE
H7 HOLE
H11 HOLE
H12 HOLE
H24 HOLE
H25 HOLE
H3 HOLE
H5 HOLE
H4 HOLE
H10 HOLE
34.4G502.001
孔徑要變更
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
Pomona/Texcoco
Rev
1
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PAGE3 DY RN21~24,RN34~RN36,R132,9LPR462AGLF INTERNAL P/D.
PAGE3 CHANGE X2,C307,C311 BY KDS SUGGESTION
PAGE14 ADD F2 BETWEEN DCBATOUT AND LCD CONN.
PAGE14 CHANGE LED2 TO DUAL COLOR LED FOR POWER LED AND STANDBY LED
PAGE14 CHANGE LED4 TO DUAL COLOR LED FOR CHARGER LED AND DC_BATFULL LED
PAGE15 CHANGE C477,480,487 TO 15P FROM DY FOR SOLVE SIV ISSUE,DIS ONLY
PAGE15 CHANGE C477,480,487 TO 15P FROM DY FOR SOLVE SIV ISSUE,DIS ONLY
PAGE15 CHANGE C479,483,490 TO 15P FROM 6.8P FOR SOLVE SIV ISSUE.DIS ONLY;UMA WILL KEEP 6.8P
PAGE18 CHANGE X1,C259,C270 BY KDS SUGGESTION
PAGE19 CHANGE X5,C655,C656 BY KDS SUGGESTION
PAGE19 PSW_CLR# P/U 10K TO 3D3V_S5
PAGE21 CHANGE R101 TO DY FOR ECSWI#_KBC AND CHANGE TO R531 THAT CONNECT TO USB_OC6#(GEVENT6#)
PAGE23 CHANGE SATA1 CONN.
PAGE23 CHANGE ODD1 CONN.
PAGE24 CHANGE R27 TO 10R FOR SOLVE ACZ_SDATAIN1 OF SIV FAIL ITEM
PAGE25 CHANGE X4,C471,C472 BY KDS SUGGESTION
PAGE26 CHANGE RJ1 CONN.AND LAN_ACT_LED# TO B2 FROM A1,10M/100M/1G_LED# FROM B2 TO A3
PAGE26 CHANGE LAN_ACT_LED# TO B2 FROM A1
PAGE26 CHANGE 10M/100M/1G_LED# FROM B2 TO A3
PAGE28 CHANGE C691,C689 TO 6.8P BY KDS SUGGESTION
PAGE30 CHANGE NEW1 CONN.
PAGE30 CHANGE MINIC1 CONN.
PAGE30 ADD R537 AND SET TO DY
PAGE31 CHANGE R215 TO 27R FOR SOLVE ACZ_SDATAIN0 OF SIV FAIL ITEM
PAGE31 ADD R538 0R AND SET INTERNAL MIC TO LEFT CHANNEL,DY R224,D17 AND ADD D36
PAGE31 SET C391 TO DY FOR POP SOUND
PAGE31 CHANGE R247 TO 10K;R236 TO 6.8K;R248 TO DY;249 TO STUFF FOR SET GAIN TO 1.2W
PAGE31 CHANGE R238,239,242,243 TO 0R
PAGE31 CHANGE R223 TO STUFF
PAGE31 CHANGE INTMIC1 CONN.
PAGE31 CHANGE SPKR1 CONN.
PAGE33 ADD D35 BETWEEN KBC AND PM_PWRBTN#
PAGE33 DY R197 AND STUFF R193 FOR SET PCB VER. TO 001
PAGE33 CHANGE X3,C337,C341 BY KDS SUGGESTION
PAGE34 Add serial resistor 150 Ohm and Bypass Cap 4.7P on SPI_CLK(Close to KBC)
Add serial resistor 150 Ohm on SPI_DO(Close to KBC)
Add serial resistor 150 Ohm on SPI_DI(Close to SPI Flash)
PAGE33 CHANGE WLAN1,BLUE2 CONN.
PAGE37 SET R453 TO DY
PAGE38 ADD C750

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1.Change U19 ATIGLCK3 to SRCCLK3.PAGE3
2.Change U19 ATIGLCK2 to SRCCLK1.PAGE3
3.Add CLK14_SIO of U19;PIN62 FOR Super I/O.PAGE3
4.Change THERMTRIP# TO KBC GPI94.PAGE6
5.Change LDT_RST#;LDT_STP#;SB_CPUPWRGD P/L resistor to 680 ohms by AMD recommand.PAGE6
6.Adjust current limit resistor for FRONT_PWRLED.R1113 change to 68 ohms.PAGE14
7.Adjust current limit resistor for BT_LED.R251 change to 390 ohms.PAGE14
8.Adjust current limit resistor for DC_BATFULL LED.R1116 change to 68 ohms.PAGE14
9.Add R1093 P/H 10K ohms TO 3D3V_S0 for slove WLAN_LED light leak in dos mode.PAGE14
10.Remove damping resistor of TMDS signal.PAGE16
11.Remove bridge resistor of TMDS signal.PAGE17
12.Change FP_DETECT TO KBC GPIO27.PAGE19
13.Chamge USB7 from PORT7 to PORT1 of U19.PAGE21
14.Change PCB_VER0/1 form KBC to GPIO4/5 of U19.PAGE21
15.Add ESD diode D38~D45 for USB signal.PAGE23
16.Add damping resistor 22 ohms and P/L CAP 22P for SD_CLK for EMI.PAGE27
17.Add P/L CAP 33P for SD/MMC_D0~D3 for EMI.PAGE29
18.Dummy R1062,R1058 and mount R1061 for MINICARD.PAGE30
19.Remove MIC array design.PAGE31
20.Add ESD diode EC523~526 for internal speaker.PAGE32
21.Add AD_DIFF on GPIO10 for separate 65W/90W adapter.PAGE33
22.Change KBC_MATRIX0# P/H to 3D3V_AUX_S5.PAGE33
23.Add SUPER IO circuit U76 for FIR function.PAGE33
24.BLON_OUT and BRIGHTNESS P/L cap close to KBC.PAGE33
25.Add R1089 to set BLON timing.PAGE33
26.Add U77 T8 shutdown circuit FOR U19(SB600).PAGE36
28.Change KBC_THERMTRIP# to KBC GPI94.PAGE36
29.Change value of R25.R26 and mount R17 to modify SUSTAND LOAD LINE to meet AMD spec.PAGE42
30.Add AD_DIFF for separate 65W/90W adapter.PAGE46
31.Add D46 and modify resistor value of R1111,R1112,R121,C294,C308 by vendor recommand.PAGE46

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