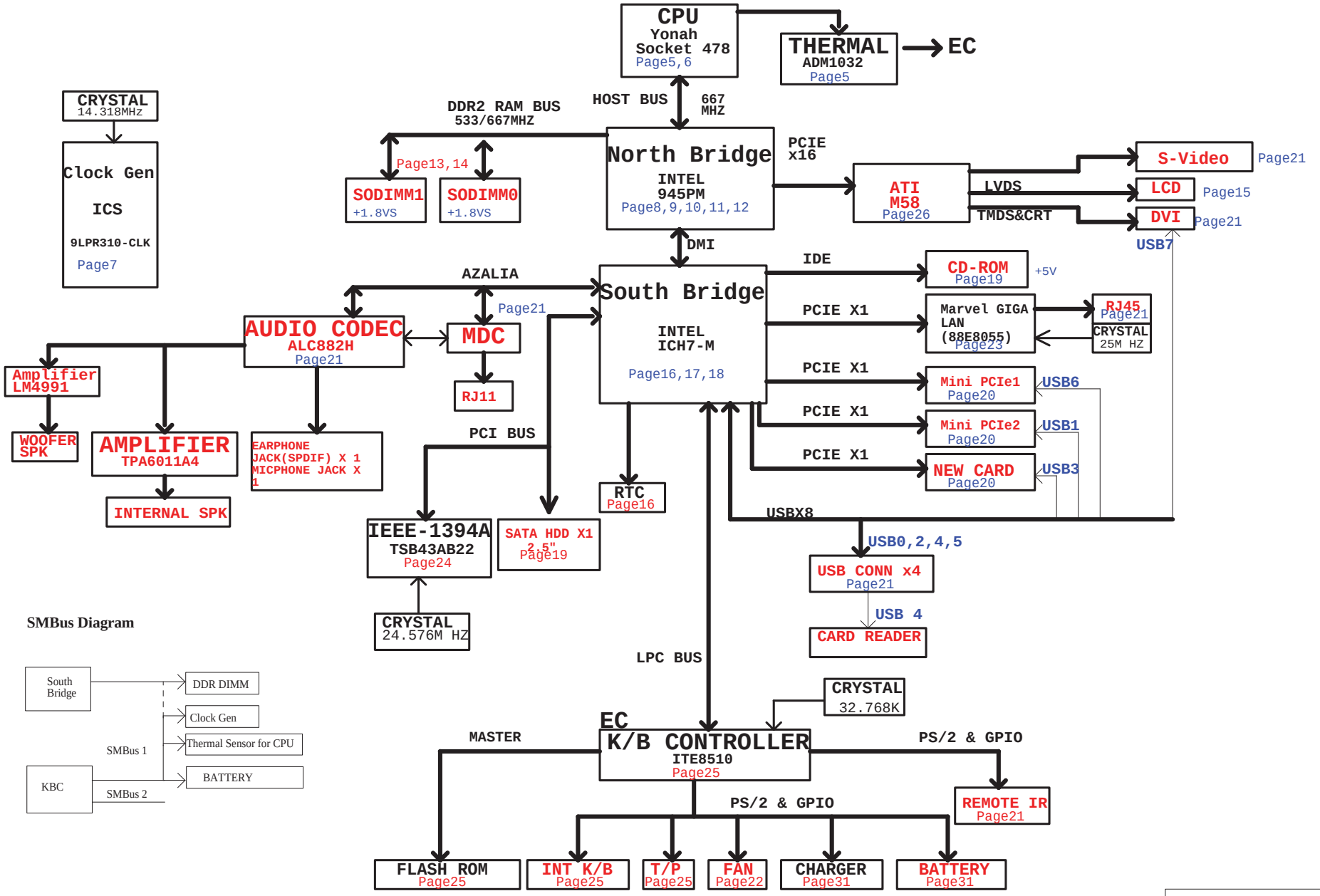
Model : X72IA6

Intel Yonah CPU + 945PM / ICH7-M Chipset

Revision History		
A		ORIGINAL RELEASE
B		

UNIWILL COMPUTER (SIP) Co.,LTD		
Title: X72IA6		
Size	Document Number: SCHEMATIC1 — INDEX	Rev: B
Date: Tuesday, April 11, 2006	Sheet 1 of 32	

X72IA6 SYSTEM BLOCK DIAGRAM



SMBus Diagram

UNIWILL COMPUTER (SIP) Co.,LTD		
Title: X72IA6		
Size	Document Number: SYSTEM BLOCK DIAGRAM	Rev: B
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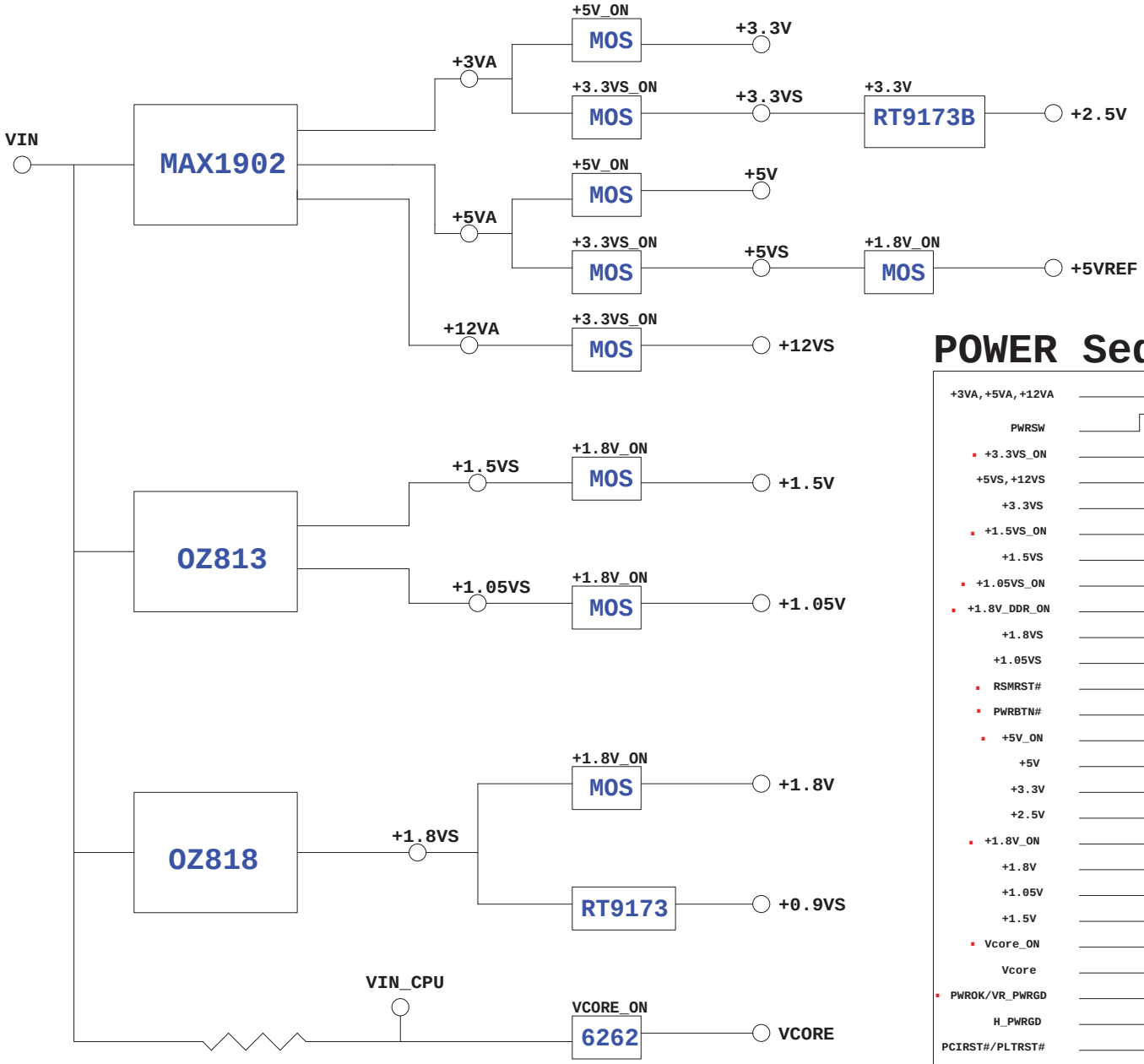
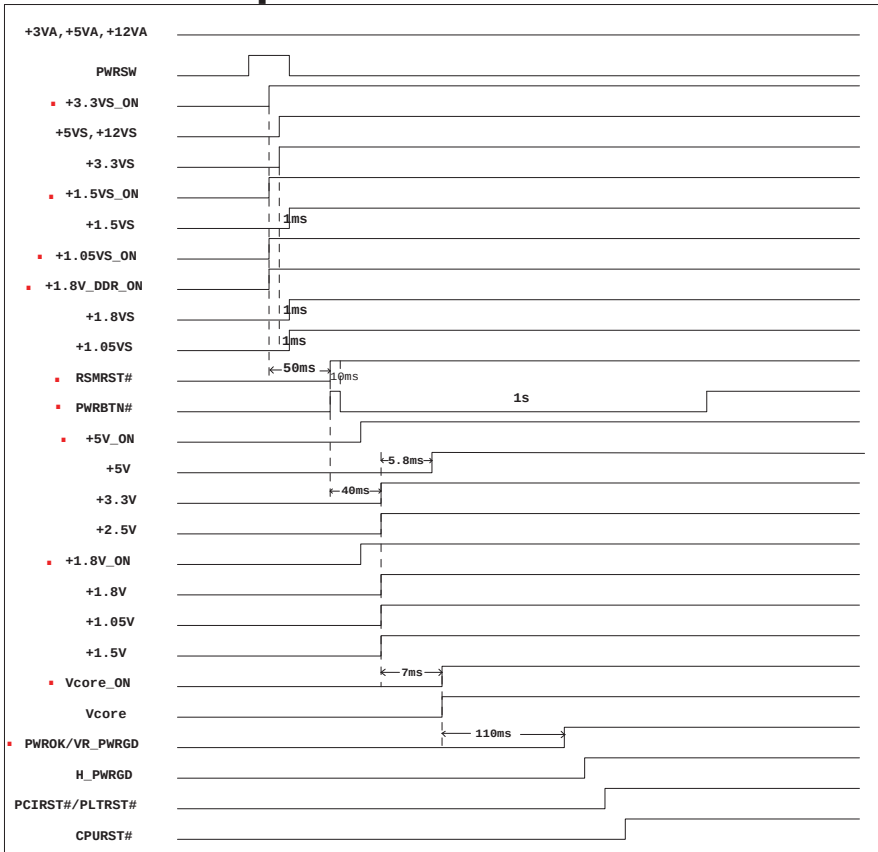
POWER BLOCK DIAGRAM



POWER Sequence



UNIWILL COMPUTER (SIP) Co.,LTD		
Title: X72IA6		
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ICH7-M GPIO

GPIO0	BM_BUSY#
GPIO9	EC_EXTSMI#
GPIO11	SMB_ALERT#
GPIO12	PNLSW0
GPIO13	PNLSW1
GPIO14	PNLSW2
GPIO16	PM_DPRSLPVR
GPIO18	PM_STPPCI#
GPIO20	PM_STPCPU#
GPIO49	H_PWRGD

ITE8510E GPIO

GPCF0	RF_SW#
GPCF1	SILENT#/
GPCF2	IR_PS2CLK1
GPCF3	IR_PS2DAT1
GPCF4	TP_CLK
GPCF5	TP_DATA
GPCF6	KEY_16
GPCF7	KEY_17
GPI0	SCROLL_LED#
GPI1	CAPS_LED#
GPI2	NUM_LED#
GPI3	CHG_R_LED#
GPI4	CHG_G_LED#
GPI5	SUSLED_LED#
GPI6	IR_MAXVOLUME
GPH0	+1.8V_DDR_ON
GPH1	+1.8V_ON
GPH2	+1.05VS_ON
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	SET_V
GPH6	+1.5VS_ON
GPH7	VCORE_ON
GPG4	TP_DISABLE
GPG5	LCDSW
GPG6	MUTE#
GPG7	EXTTS#0
GPB0	ROM_WE_DIS
GPB1	NA
GPB2	PM_RSMRST#
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	RFLED_ON#
GPE0	***NA***
GPE1	EC_CPU_BSEL1
GPE2	***NA***
GPE3	***NA***
GPE4	PWRSW
GPE5	LID#
GPE6	PCM#
GPE7	PM_SLP_S3#
GPD0	ADAP_IN
GPD1	REMOTE_ON#
GPD2	PCI_RST#/PLT_RST#
GPD3	EC_EXTSMI#
GPD4	PM_SLP_S4#
GPD5	PM_THROTTLING#
GPD6	FAN_SPD#
GPD7	NA
GPA0	BTL_BEEP
GPA1	NA
GPA2	NA
GPA3	NA
GPA4	NA
GPA5	SMP1_EN#
GPA6	MAIL#
GPA7	PWRBTN#

ITE8510E GPIO

GPC0	PWROK
GPC1	BAT2_SMBCLK
GPC2	BAT2_SMBDAT
GPC3	SB_ALERT#1/EC_171
GPC4	SB_ALERT#2/BROWSER#
GPC5	TP_LED#
GPC6	CHG_ON
GPC7	SILENT_LED#
ADC0	BAT_TEMP
ADC1	ADAPTOR_I
ADC2	DDR2_TEMP
ADC3	VGA_TEMP
DAC0	BRIGHTADJ
DAC1	CHG_I
DAC2	FAN_CTRL0
DAC3	***NA***

CPU

	CPU CORE(V)	ICC(mA)	W	TEMP(℃)
2.0G	1.525	35.7	54.3	69
2.2G	1.525	37.5	57.1	70
2.26G	1.525	38.1	58.0	70
2.4G	1.525	39.3	59.8	71
2.5G	1.525	40	61.0	72
2.53G	1.525	40.4	61.5	72
2.6G	1.525	41.05	62.6	72
2.66G	1.525	43.35	66.1	74
2.8G	1.525	44.86	68.4	75
3.06G	1.525	55.9	85.2	81

MCHE

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	108.19	0.357	70
+3.3VA	501.3	1.254	
+2.5V	1390	2.502	
+1.5V	33.4	0.084	
+VCCP	10	0.018	
+VCC_GMCH_CORE	266	0.452	

ICH6-M

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	96	0.315	70
+3.3VA	275	0.909	
+1.5V	487	0.876	
+1.5VA	27	0.049	
+3.3VA_RTC	0.003	0.00001	

ITE8510E

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	300	1	70

CLOCK GENERATOR

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	180	0.594	70

ALC880

VCC	ICC(mA)	W	TEMP(℃)
+3.3V(DVDD)	71	0.234	70

TPA6011A4

VCC	ICC(mA)	W	TEMP(℃)
3.3V	30	0.099W	85

ADM1032

VCC	ICC	W	TEMP(℃)
+3.3V	170uA	0.56mW	150

UNIWILL COMPUTER (SIP) Co.,LTD

Title: X72IA6

Size | Document Number: SCHEMATIC1 — GPIO & Power Consumption | Rev: B

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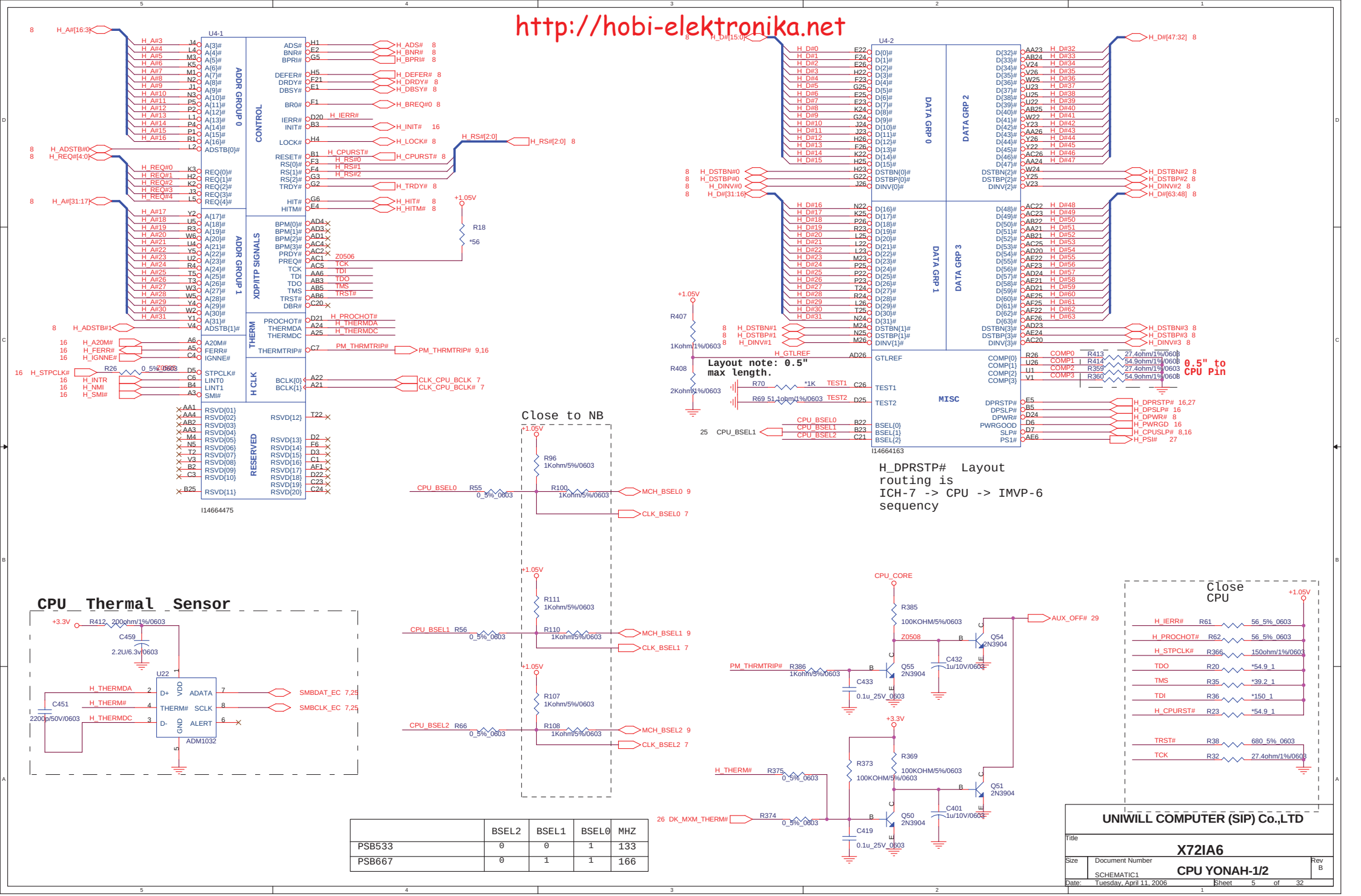

	BSEL2	BSEL1	BSEL0	MHZ
PSB533	0	0	1	133
PSB667	0	1	1	166

UNIWILL COMPUTER (SIP) Co.,LTD	
Title	X72IA6
Size	Document Number: SCHEMATIC1 — CPU YONAH-1/2 — Rev B
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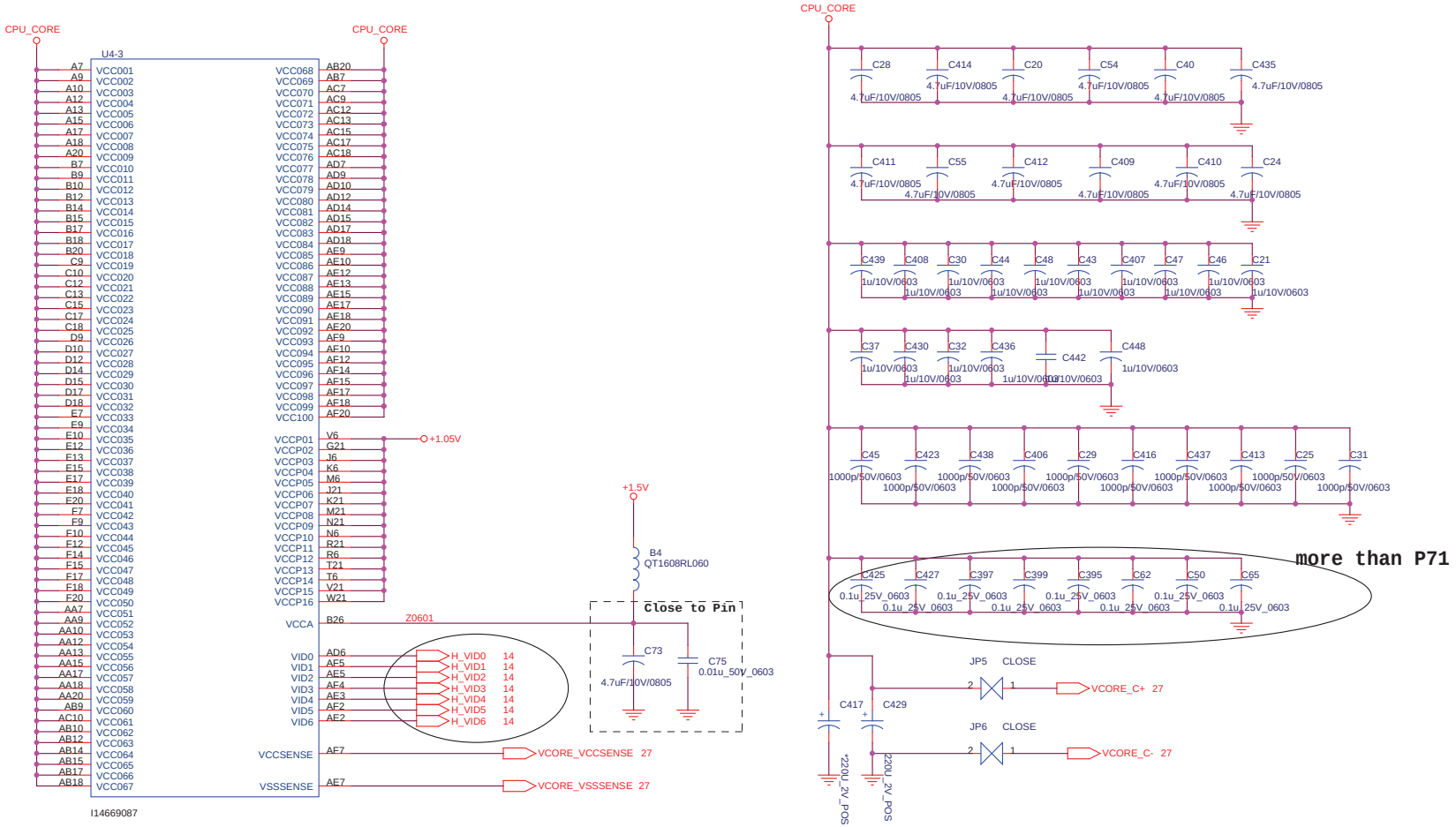
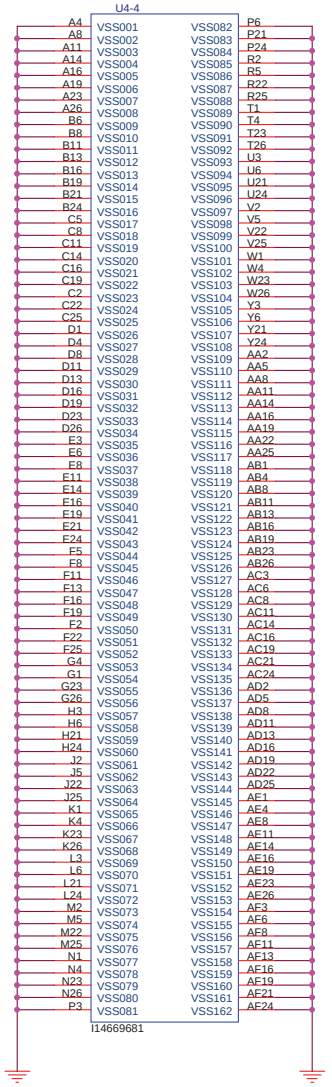
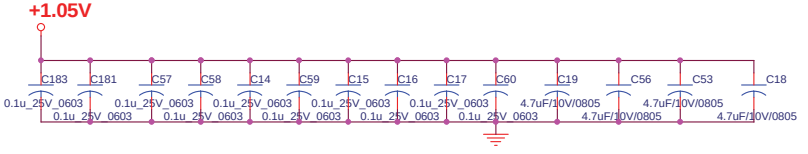




QT1608GRL600 = 200mA
QT1608RL120 = 200mA
QT1608RL600 = 200 mA
QT1608RL030 = 500mA
QT1608RL060 = 500mA



UNIWILL COMPUTER (SIP) Co.,LTD		
Title: X72IA6		
Size	Document Number: CPU YONAH-2/2	Rev: B
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Modify13

Reserved FOR EMI

C206 *150PF PCI3
C598 *150PF PCI2
C208 *150PF PCI1
C799 *150PF PCI0
C201 *200PF CLKBSEL1
C198 *100PF CLKBSEL0

All the Capacitor must be add close to Clock GEN at the same side

Close pin 28,42

Close pin 50

Close pin 56

Close pin 1,7

200mA

200mA

+3.3V

CLK_VDDA
C185 C187 C186 C190 C188
0.1u_25V_0603 0.1u_25V_0603 0.1u_25V_0603 4.7uF/10V/0805
0.1u_25V_0603 0.1u_25V_0603

B9 QT1608RL600

B10 QT1608RL600

R161 2.2_5%_0603
VDD_A_CR
C194 C195
0.1u_25V_0603 4.7uF/10V/0805

PCI Power

PCI-E Power

U29

Z0703 Z0704
C199 C203
0.1u_25V_0603 *4.7U_10V_0805
R180 2.2_5%_0603
VDD_REF_CR

C593 C603 C209
0.1u_25V_0603 0.1u_25V_0603 4.7uF/10V/0805
R178 1_5%_0603

Xtal Power

C202 0.1u_25V_0603

Bsel [0,2]
Vil = 0.3
Vih = 0.7

Modify8

5 CLK_BSEL2 R513 2.2Kohm/1%/0603 CLKBSEL2
5 CLK_BSEL1 R510 2.2Kohm/1%/0603 CLKBSEL1
5 CLK_BSEL0 R175 *2.2K CLKBSEL0

24 PCICLK_1394_A R512 33_5%_0603 PCI3
25 TEST_PCI R639 33_5%_0603 PCI2
25 CLK_PCI_LPC R528 33_5%_0603 PCI1
17 CLK_PCI R179 33_5%_0603 PCI0

VDDPCIEX 28
VDDPCIEX 42
VDDCPU 50
PCICLK3 5
PCICLK2_2X 4
PCICLK1_2X 3
PCICLK0_2X 64

VDDPCI1 7
VDDPCI0 1

PLL Power

VDD48 11
VDDREF 56
VDDA 45
GNDA 46
CLK_VDDA

PCI/PCIEX_STOP# 63 Z0705
CPU_STOP# 62 Z0706
R530 0_5%_0603 *0
R523
PM_STPPCI# 17
PM_STPCPU# 17

Changed 10/08

CPUCLKT1 49 CPU1
CPUCLKC1 48 CPU#1
R497 R494 22_5%_0603
CLK_MCH_BCLK 8
CLK_MCH_BCLK# 8

CPUCLKT0 52 CPU0
CPUCLKC0 51 CPU#0
R165 R163 22_5%_0603
CLK_CPU_BCLK 5
CLK_CPU_BCLK# 5

SELDOT , 1= Pin 14/15 DOT 96MHZ , Pin 17/18 LCDCLK
0= Pin 14/15 27MHZ Fix/SS Pin 17/18 PCIEX

SELDOT/ PCICLK_F1 9
PCICLK_F0 8

CLKBSEL2 61
17 CLK_ICH14 R176 33_5%_0603 CLKBSEL1 60
17 CLK_USB48 R168 33_5%_0603 CLKBSEL0 12
FLSC/REF1
FLSB/REF0
FLSA/USB_48M_2X

+3.3V R171 100_5%_0603

CLKGEN_DATA 55
CLKGEN_CLK 54
SDATA
SCLK

LCD_SSCGT/PCIEXOT 17
LCD_SSCGC/PCIEXOC 18

16 SATA_CLKP R151 22_5%_0603 SATACLKP 26
16 SATA_CLKN R152 22_5%_0603 SATACLKN 27
SATACLKT
SATACLKC

20 MINICARD_CLK_REQ2# 33
PEREQ4#
PEREQ3# 32
9 NB_CLK_REQ# 34
20 MINICARD_CLK_REQ1# 16
PEREQ2#
PEREQ1#

R726 R727 R682 R681
*0 *0 *0 *0

Changed 10/08

XTAL_OUT 57
XTAL_IN 58
X2_OUT
X1_IN

IREF 47
R487 4.3Kohm/1%/0603
VREF

9LPR310-CLK

GND 2 6 13 29 37 53 59

VTT_PWRGD#/PD 10

PCIEXT1 19 PCIE1
PCIEXC1 20 PCIE#1
R160 R159 22_5%_0603
GCLK 9
GCLK# 9

PCIEXT2 22 PCIE2
PCIEXC2 23 PCIE#2
R493 R486 22_5%_0603
CLK_PCIE_NEW_CARD 20
CLK_PCIE_NEW_CARD# 20

PCIEXT3 24 PCIE3
PCIEXC3 25 PCIE#3
R483 R481 22_5%_0603
CLK_PCIE_ICH 17
CLK_PCIE_ICH# 17

PCIEXT4 30 PCIE4
PCIEXC4 31 PCIE#4
R479 R471 22_5%_0603
CLK_PCIE_MXM 26
CLK_PCIE_MXM# 26

PCIEXT5 36 PCIE5
PCIEXC5 35 PCIE#5
R480 R472 22_5%_0603
CLK_PCIE_LAN 23
CLK_PCIE_LAN# 23

PCIEXT6 39 PCIE6
PCIEXC6 38 PCIE#6
R484 R482 22_5%_0603
CLK_PCIE_Mini card1 20
CLK_PCIE_Mini card1# 20

PCIEXT7 41 PCIE7
PCIEXC7 40 PCIE#7
R724 R725 22_5%_0603
CLK_PCIE_Mini card2 20
CLK_PCIE_Mini card2# 20

PCIEXT8 44
PCIEXC8 43

DOTT_96M 14
DOTC_96M 15

+3.3V
R502 10KOHM/5%/0603
R679 *0
6262CLK_EN# 27
R680 330_5%_0603
+1.05V
Q90 2N3904

Changed 10/08

Modify13

CPU0 C800 22PF/10V/0402/NPO
CPU#0 C801 22PF/10V/0402/NPO
CPU1 C802 22PF/10V/0402/NPO
CPU#1 C803 22PF/10V/0402/NPO

SATACLKP C818 *20PF
SATACLKN C819 *20PF

All the Capacitor must be add close to Clock GEN at the same side

XTAL_OUT
XTAL_IN
Y2
14.318MHz_DIP
R185 *10M
C212 33pF/50V/0603
C213 33pF/50V/0603

Ce = 2*CL - (Cs + Ci)
CL = Crystal Load Cap = 20P
Ci = IC internal Cap = 5P
Cs = 2P
Ce = Crystal external Cap = 33P

13,17,20,23 SB_SMB_DATA R173 *0 CLKGEN_DATA
5,25 SMBDAT_EC R172 0_5%_0603
5,25 SMBCLK_EC R169 0_5%_0603 CLKGEN_CLK
13,17,20,23 SB_SMB_CLK R170 *0

GCLK => PCI-E & DMI (100MHZ)
DREFCLK => Dispaly PLLA (nun- ss 96MHZ)
DRESSFCLK => Display LVDS PLLB (ss 100MHZ)

	FS4	FS3	BSEL2 FSLC	BSEL1 FSLB	BSEL0 FSLA	CPU MHZ	PCI MHZ	PCI-E MHZ	SPREAD %
PSB533	0	0	0	0	1	133	33	100	0.5% DOWN
PSB667	0	0	0	1	1	166			
PSB533	0	1	0	0	1	133	33	100	+/- 0.25% CENTER
PSB667	0	1	0	1	1	166			

FS3 , FS 4 SEETING BY I2C BUS

PCI-Express

	Reserve	MCH	N_Card	ICH7-M	VGA	LAN	Mini_C1	Mini_C2	Reserve
	0	1	2	3	4	5	6	7	8
PEREQ1#	V						V		
PEREQ2#		V							V
PEREQ3#			V		V				
PEREQ4#				V		V		V	

UNIWILL COMPUTER (SIP) Co.,LTD

Title: X72IA6

Size | Document Number: SCHEMATIC1 CLOCK GEN ICS9LPR310 | Rev B

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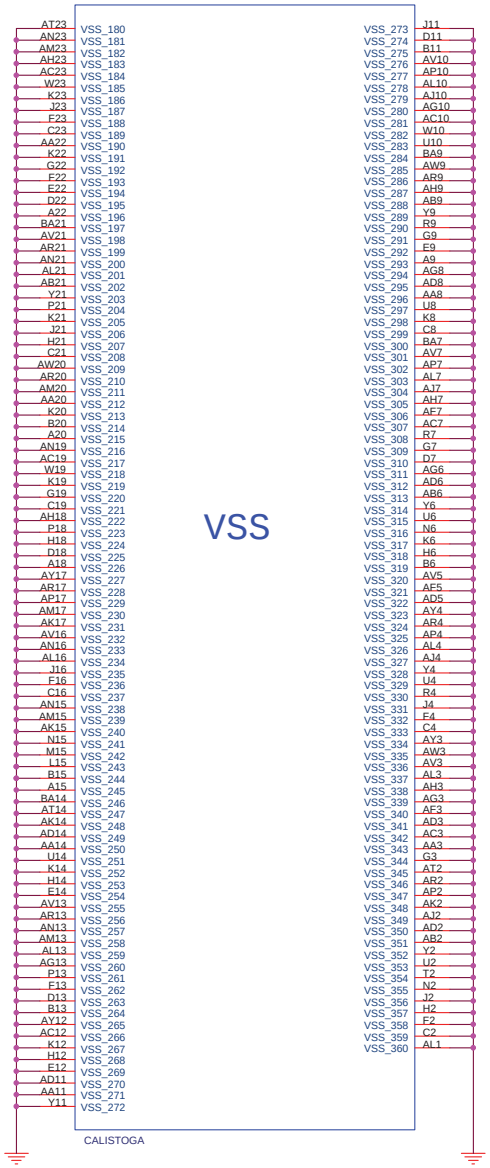
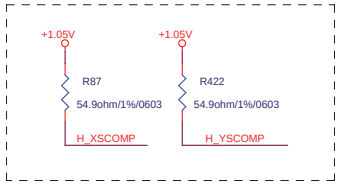
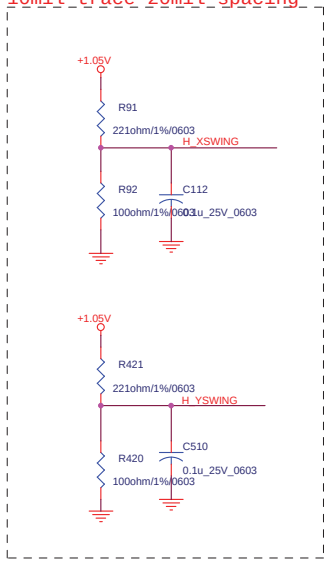


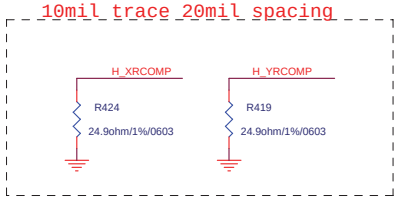
FSB I/O slew rate compensation

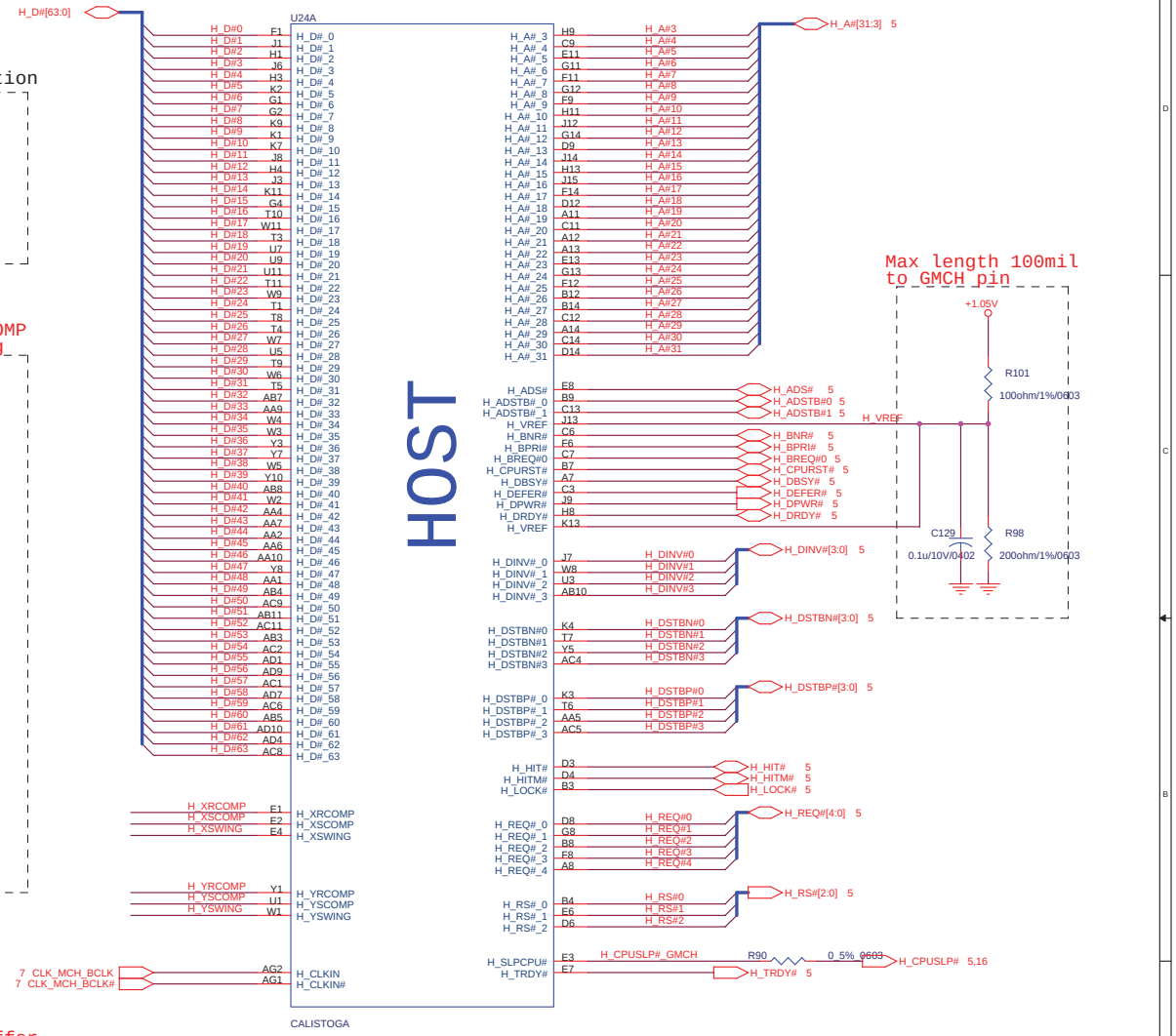


Reference Voltage for RCOMP
10mil trace 20mil spacing



Calibration FSB I/O Buffer
10mil trace 20mil spacing





UNIWILL COMPUTER (SIP) Co.,LTD	
Title	X72IA6
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U24B

DMI
DMI_RXP[3:0] → DMI_RXP3 AG41, DMI_RXP2 AF37, DMI_RXP1 AE41, DMI_RXP0 AC37
DMI_RXN[3:0] → DMI_RXN3 AH41, DMI_RXN2 AG37, DMI_RXN1 AF41, DMI_RXN0 AE37
DMI_TXP[3:0] → DMI_TXP3 AG39, DMI_TXP2 AF35, DMI_TXP1 AE39, DMI_TXP0 AC35
DMI_TXN[3:0] → DMI_TXN3 AH39, DMI_TXN2 AG35, DMI_TXN1 AF39, DMI_TXN0 AE35
DMI_TXP_3, DMI_TXP_2, DMI_TXP_1, DMI_TXP_0
DMI_TXN_3, DMI_TXN_2, DMI_TXN_1, DMI_TXN_0
DMI_RXP_3, DMI_RXP_2, DMI_RXP_1, DMI_RXP_0
DMI_RXN_3, DMI_RXN_2, DMI_RXN_1, DMI_RXN_0

NC
NC18 A3, NC17 A39, NC16 A4, NC15 A40, NC14 AW1, NC13 AW41, NC12 AY1, NC11 AY41, NC10 B2, NC9 B41, NC8 BA1, NC7 BA2, NC6 BA3, NC5 BA39, NC4 BA40, NC3 BA41, NC2 C1, NC1 C41, NC0 D1

MISC
CLK_REQ# H32 → Z0907 → NB_CLK_REQ# 7
LT_RESET# K28 → NB_SYNC# 17
SDVO_CTRLDATA H27
SDVO_CTRLCLK H28

Asserted to control the raw PCI-E clock

Asserted to synchronize with ICH on fault

CLK
R468 0_5%_0603 Z0901 D41
R470 0_5%_0603 Z0902 C40
R438 0_5%_0603 Z0906 A26
R441 0_5%_0603 Z0912 A27
D_REFSSCLKIN, D_REFSSCLKIN#, D_REFCLKIN, D_REFCLKIN#
GCLK AG33, GCLK# AF33
G_CLKIN, G_CLKIN#

PM
RSTIN# AH34 ← Z0911 R157 100_5%_0603 ← PLT_RST# 17,19,26
PWROK AH33 ← DELAY_VR_PWRGOOD ← DELAY_VR_PWRGOOD 17
CLK ICH7_THRMTRIP# G6
PM_THRMTRIP# H26 ← PM_EXTTS#1 R112 *0_5%_0603 D6 BAT54 A C → PM_DPRSLPVR 17,27
PM_EXTTS#_1 F25 ← PM_EXTTS#0 → EXTTS#0 14,25
PM_EXTTS#_0 G28 → BM_BUSY# 17
PM_BMBUSY#
Modify3

GHCH integrated graphics busy

DDR MUXING
M_VREF_MCH → SM_VREF_1 AK41, SM_VREF_0 AK1
M_RCOMPP AT9, M_RCOMPN AV9 → SM_RCOMP, SM_RCOMP#
SM_ODT_3 AU21, SM_ODT_2 AY20, SM_ODT_1 BA12, SM_ODT_0 BA13
13,14 MB_ODT3, 13,14 MB_ODT2, 13,14 MA_ODT1, 13,14 MA_ODT0
M_OCDCOMP1 → SM_OCDCOMP_1 AF10
M_OCDCOMP0 → SM_OCDCOMP_0 AL20
as short as possible
R97 *40.2_1, R106 *40.2_1
13,14 MB_CS#3 AW21, 13,14 MB_CS#2 AY21, 13,14 MA_CS#1 AW12, 13,14 MA_CS#0 AW13
SM_CS#_3, SM_CS#_2, SM_CS#_1, SM_CS#_0
13,14 MB_CKE3 AY29, 13,14 MB_CKE2 BA29, 13,14 MA_CKE1 AT20, 13,14 MA_CKE0 AU20
SM_CKE_3, SM_CKE_2, SM_CKE_1, SM_CKE_0
13 MB_CK#3 AY40, 13 MB_CK#4 AY7, 13 MA_CK#1 AT1, 13 MA_CK#0 AW35
SM_CK#_3, SM_CK#_2, SM_CK#_1, SM_CK#_0
13 MB_CK3 AW40, 13 MB_CK4 AW7, 13 MA_CK1 AR1, 13 MA_CK0 AY35
SM_CK_3, SM_CK_2, SM_CK_1, SM_CK_0

CFG
CFG_20 J26, CFG_19 K27 → CFG19 12
CFG_18 J25 → CFG18 12
CFG_17 H15
CFG_16 G18 → CFG16 12
CFG_15 H16
CFG_14 C15
CFG_13 K15 ← Z0903 R104 *1K
CFG_12 G15 ← Z0904 R105 *1K
CFG_11 D15
CFG_10 E16
CFG_9 G16 → CFG9 12
CFG_8 D16
CFG_7 D19
CFG_6 E18
CFG_5 F15 → CFG5 12
CFG_4 E15
CFG_3 F18
CFG_2 J18 → MCH_BSEL2 5
CFG_1 K18 → MCH_BSEL1 5
CFG_0 K16 → MCH_BSEL0 5

Base on RSTIN#

RSVD
RSVD_13 D27, RSVD_12 D28, RSVD_11 A34, RSVD_10 A35, RSVD_9 A41, RSVD_8 J19, RSVD_7 H7, RSVD_6 AF11, RSVD_5 AG11, RSVD_4 F7, RSVD_3 F3, RSVD_2 R32, RSVD_1 T32

CALISTOGA

GCLK = PCI-E & DMI (100MHZ)
DREFCLK = Dispaly PLLA (nun- ss 96MHZ)
DRESSFCLK = Display LVDS PLLB (ss 100MHZ)

SDVODATA has internal pull down
0= no DVO device
1= DVO device present
SDVOCLK has internal pull down .

U24C

LVDS
L_BKLTCTL D32, L_BKLTEN J30, L_CLKCTLA H30, L_CLKCTLB H29, L_DDC_CLK G26, L_DDC_DATA G25, L_IBG B38, L_VBG C35, L_VDDEN F32, L_VREFH C33, L_VREFL C32
LA_CLK# A33, LA_CLK A32, LB_CLK# E27, LB_CLK E26
LA_DATA#_0 C37, LA_DATA#_1 B35, LA_DATA#_2 A37
LA_DATA_0 B37, LA_DATA_1 B34, LA_DATA_2 A36
LB_DATA#_0 G30, LB_DATA#_1 D30, LB_DATA#_2 F29
LB_DATA_0 F30, LB_DATA_1 D29, LB_DATA_2 F28

TV
+1.5V
TV_DACA_OUT A16, TV_DACB_OUT C18, TV_DACC_OUT A19
TV_IREF J20, TV_IRTNA B16, TV_IRTNB B18, TV_IRTNC B19
O/A
TV_DCONSEL0 K30, TV_DCONSEL1 J29

VGA
+1.05V
CRT_BLUE E23, CRT_BLUE# D23, CRT_GREEN C22, CRT_GREEN# B22, CRT_RED A21, CRT_RED# B21
CRT_DDC_CLK C26, CRT_DDC_DATA C25, CRT_HSYNC G23, CRT_IREF J22, CRT_VSYNC H23

PCI-EXPRESS GRAPHICS
EXP_A_COMPI D40 → PEG_COMP R469 24.9ohm/1%/0603 → +1.5V
EXP_A_COMPO D38
EXP_A_RXN_0 F34 → PEG_RXN0, EXP_A_RXN_1 G38 → PEG_RXN1, EXP_A_RXN_2 H34 → PEG_RXN2, EXP_A_RXN_3 J38 → PEG_RXN3, EXP_A_RXN_4 L34 → PEG_RXN4, EXP_A_RXN_5 M38 → PEG_RXN5, EXP_A_RXN_6 N34 → PEG_RXN6, EXP_A_RXN_7 P38 → PEG_RXN7, EXP_A_RXN_8 R34 → PEG_RXN8, EXP_A_RXN_9 T38 → PEG_RXN9, EXP_A_RXN_10 V34 → PEG_RXN10, EXP_A_RXN_11 W38 → PEG_RXN11, EXP_A_RXN_12 Y34 → PEG_RXN12, EXP_A_RXN_13 AA38 → PEG_RXN13, EXP_A_RXN_14 AB34 → PEG_RXN14, EXP_A_RXN_15 AC38 → PEG_RXN15
PEG_RXN[15..0] 26
EXP_A_RXP_0 D34 → PEG_RXP0, EXP_A_RXP_1 F38 → PEG_RXP1, EXP_A_RXP_2 G34 → PEG_RXP2, EXP_A_RXP_3 H38 → PEG_RXP3, EXP_A_RXP_4 J34 → PEG_RXP4, EXP_A_RXP_5 L38 → PEG_RXP5, EXP_A_RXP_6 M34 → PEG_RXP6, EXP_A_RXP_7 N38 → PEG_RXP7, EXP_A_RXP_8 P34 → PEG_RXP8, EXP_A_RXP_9 R38 → PEG_RXP9, EXP_A_RXP_10 T34 → PEG_RXP10, EXP_A_RXP_11 V38 → PEG_RXP11, EXP_A_RXP_12 W34 → PEG_RXP12, EXP_A_RXP_13 Y38 → PEG_RXP13, EXP_A_RXP_14 AA34 → PEG_RXP14, EXP_A_RXP_15 AB38 → PEG_RXP15
PEG_RXP[15..0] 26
EXP_A_TXN_0 F36 → PEG_TXN0, EXP_A_TXN_1 G40 → PEG_TXN1, EXP_A_TXN_2 H36 → PEG_TXN2, EXP_A_TXN_3 J40 → PEG_TXN3, EXP_A_TXN_4 L36 → PEG_TXN4, EXP_A_TXN_5 M40 → PEG_TXN5, EXP_A_TXN_6 N36 → PEG_TXN6, EXP_A_TXN_7 P40 → PEG_TXN7, EXP_A_TXN_8 R36 → PEG_TXN8, EXP_A_TXN_9 T40 → PEG_TXN9, EXP_A_TXN_10 V36 → PEG_TXN10, EXP_A_TXN_11 W40 → PEG_TXN11, EXP_A_TXN_12 Y36 → PEG_TXN12, EXP_A_TXN_13 AA40 → PEG_TXN13, EXP_A_TXN_14 AB36 → PEG_TXN14, EXP_A_TXN_15 AC40 → PEG_TXN15
PEG_TXN[15..0] 26
EXP_A_TXP_0 D36 → PEG_TXP0, EXP_A_TXP_1 F40 → PEG_TXP1, EXP_A_TXP_2 G36 → PEG_TXP2, EXP_A_TXP_3 H40 → PEG_TXP3, EXP_A_TXP_4 J36 → PEG_TXP4, EXP_A_TXP_5 L40 → PEG_TXP5, EXP_A_TXP_6 M36 → PEG_TXP6, EXP_A_TXP_7 N40 → PEG_TXP7, EXP_A_TXP_8 P36 → PEG_TXP8, EXP_A_TXP_9 R40 → PEG_TXP9, EXP_A_TXP_10 T36 → PEG_TXP10, EXP_A_TXP_11 V40 → PEG_TXP11, EXP_A_TXP_12 W36 → PEG_TXP12, EXP_A_TXP_13 Y40 → PEG_TXP13, EXP_A_TXP_14 AA36 → PEG_TXP14, EXP_A_TXP_15 AB40 → PEG_TXP15
PEG_TXP[15..0] 26

CALISTOGA

+1.05V → C196 1000p/50V/0603

+1.8VS → R89 150ohm/1%/0603 → 0.05A → M_VREF_MCH → C169 C105 0.1u_25V_0603 → R88 150ohm/1%/0603

+1.8VS → R95 80.6ohm/1%/0603 → M_RCOMPN
M_RCOMPP → R94 80.6ohm/1%/0603

For MEN bus throttling
+3.3V → R114 10KOHM/5%/0603 → PM_EXTTS#1
R115 10KOHM/5%/0603 → PM_EXTTS#0 → PM_EXTTS#0 13
Check with S/W

Modify2
IPU ICH7_THRMTRIP# R755 0_5%_0603 → PM_THRMTRIP# 5,16

Colse to NB
DELAY_VR_PWRGOOD → C193 0.1u_25V_0603

CFG20 (IPD) => 1= Only SDVO or PCI-E
0 = SDVO and PCI-E
CFG7 (IPU) => 1= Mobility CPU
0 = Reverse

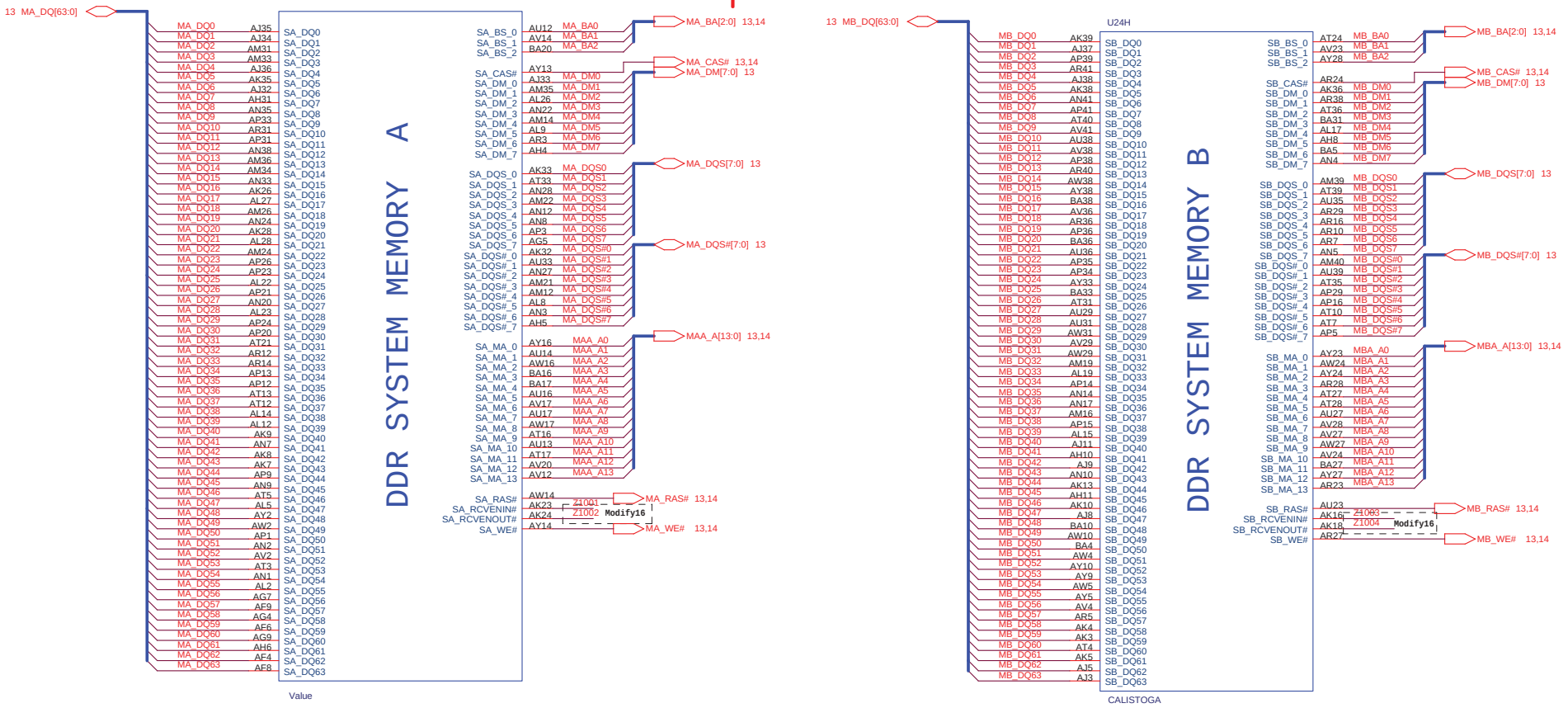
Only Base on Discreted VGA

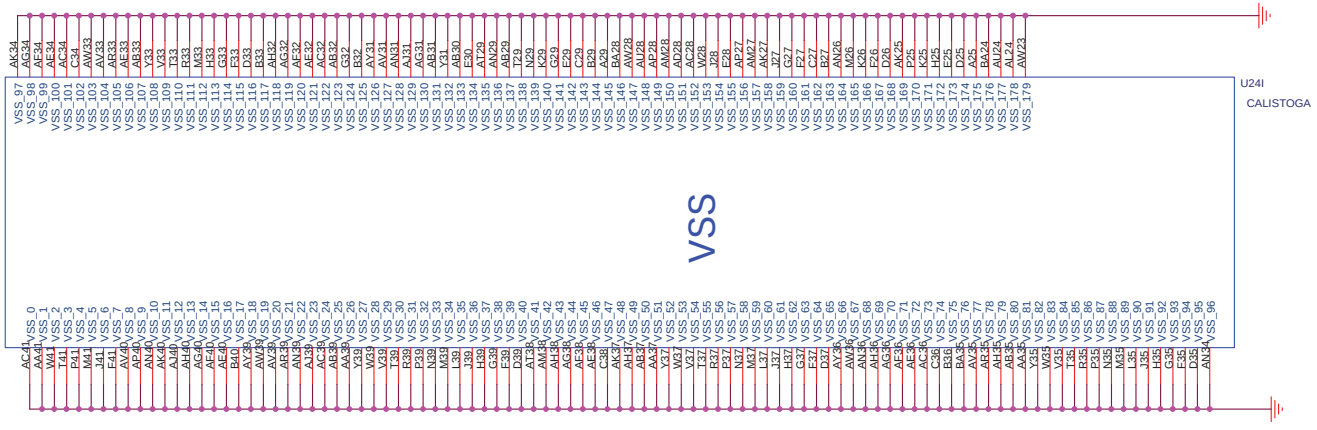
VCCA_DPLLA , VCCA_DPLLB => NC
DREF_CLKP / DREF_SSCLKP = GND
DREF_CLKN / DREF_SSCLKN = GND

VCCA_DPLLA , VCCA_DPLLB =>1.5V
DREF_CLKP / DREF_SSCLKP = 1.5V
DREF_CLKN / DREF_SSCLKN = GND

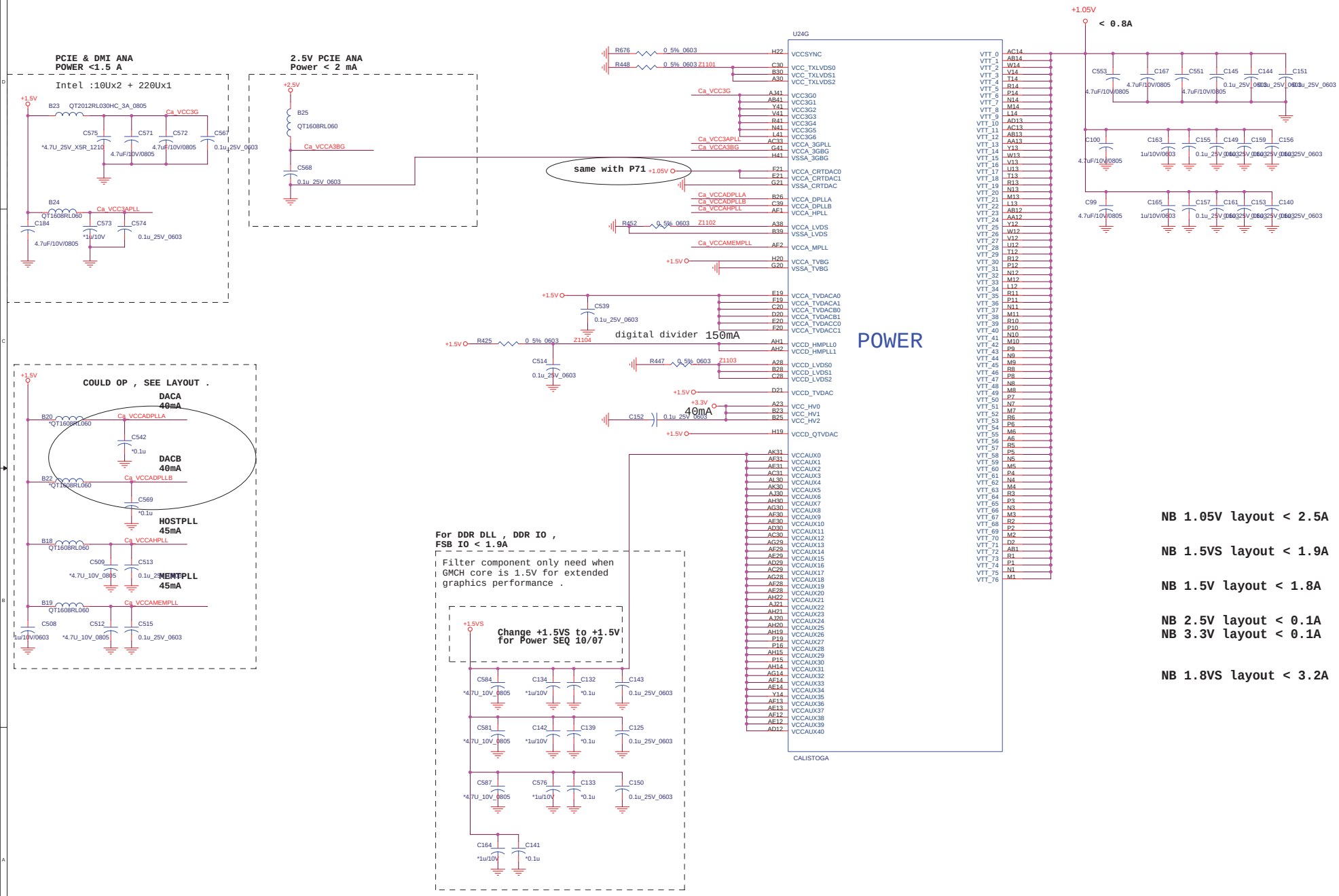
CFG0	CFG1	CFG2	Host Clock frequency
1	0	0	133
1	1	0	166

UNIWILL COMPUTER (SIP) Co.,LTD
Title: X72IA6
Size | Document Number: SCHEMATIC1 NB DDRCLK/VGA/PCIe-2/5 | Rev B
Date: Tuesday, April 11, 2006 Sheet 9 of 32

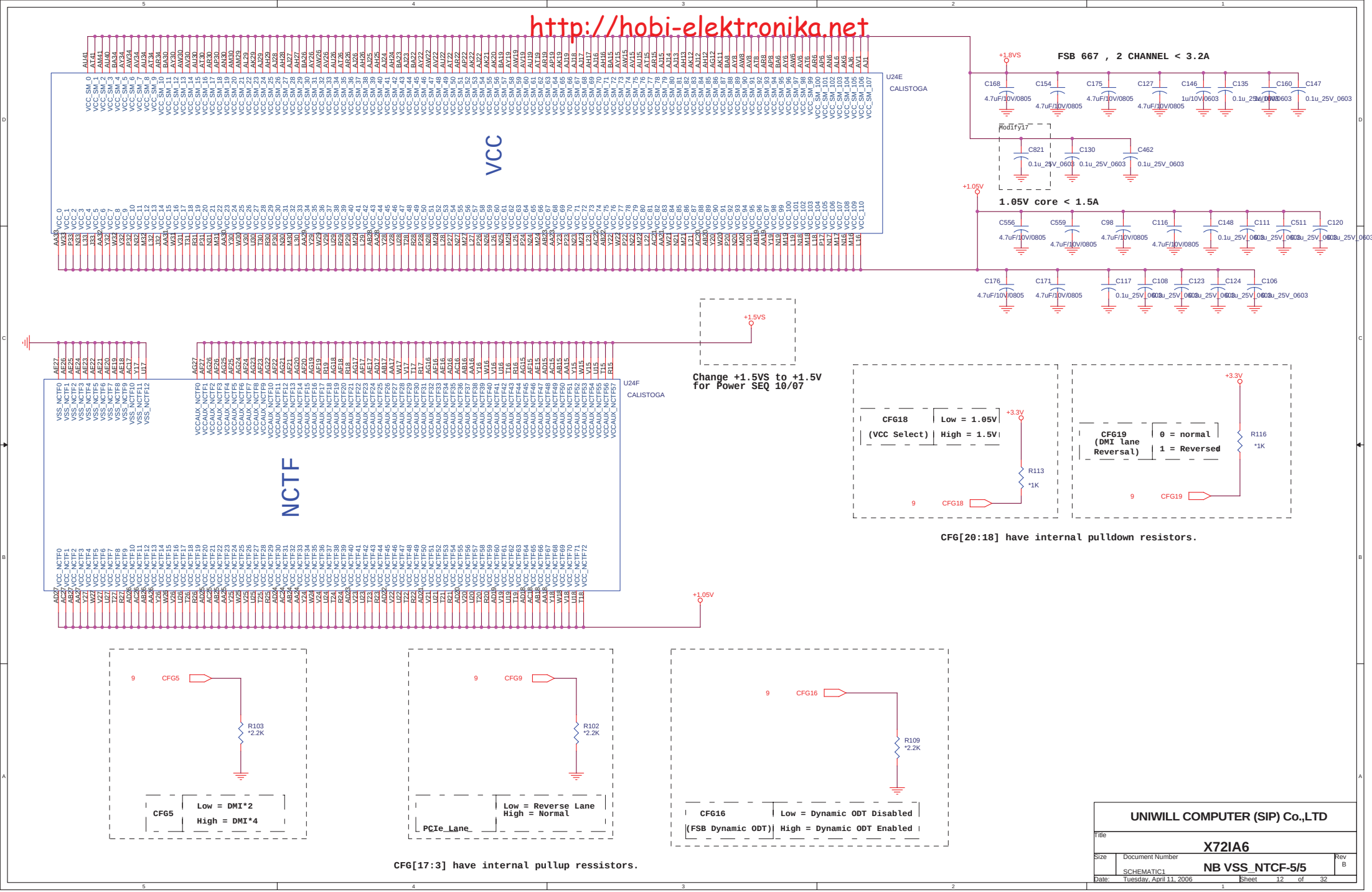




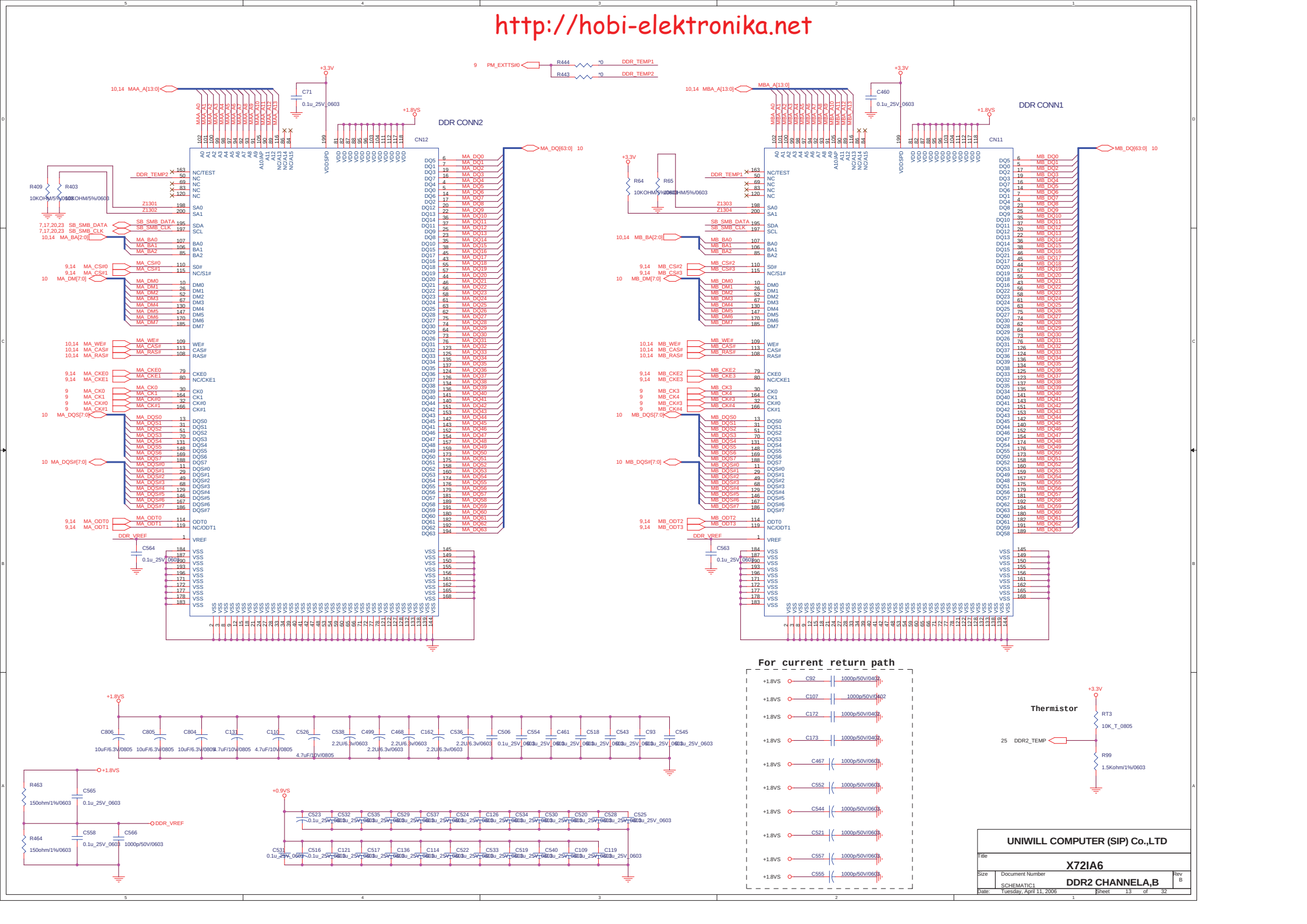
UNIWILL COMPUTER (SIP) Co.,LTD			
Title: X72IA6			
Size	Document Number: SCHEMATIC1 — NB DDR_MEM SYSTEM-3/5		Rev: B
Date: Tuesday, April 11, 2006	Sheet 10 of 32		



UNIWILL COMPUTER (SIP) Co.,LTD			
Title	X72IA6		
Size	Document Number	NB POWER-4/5	Rev B
	SCHEMATIC1		
Date: Tuesday, April 11, 2006	Sheet 11 of 32		



UNIWILL COMPUTER (SIP) Co.,LTD		
Title	X72IA6	
Size	Document Number: SCHEMATIC1 — NB VSS_NTCF-5/5	Rev B
Date: Tuesday, April 11, 2006	Sheet 12 of 32	



UNIWILL COMPUTER (SIP) Co.,LTD			
Title	X72IA6		
Size	Document Number		Rev
	SCHEMATIC1	DDR2 CHANNELA,B	B
Date:	Tuesday, April 11, 2006	Sheet 13 of 32	

SMART POWER

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	+_mV
0	0	0	0	0	0	0	1.5000	-0mV
0	0	0	0	0	0	1	1.4875	-2.5mV
0	0	0	0	0	1	0	1.4750	-5mV
0	0	0	0	1	0	0	1.4500	-50mV
0	0	0	1	0	0	0	1.4000	-100mV
0	0	1	0	0	0	0	1.3000	-200mV
0	1	0	0	0	0	0	1.1000	-400mV
1	0	0	0	0	0	0	0.7000	-800mV
0	0	1	1	0	1	1	1.1625	
0	0	1	0	0	0	1		
0	0	1	0	0	1	0		
0	0	1	0	1	0	0		
0	0	1	0	1	1	0		
0	0	1	1	0	0	1		
0	0	1	1	0	1	0		

OP for R:A test

DC IN

TOTAL POWER

USE .1% R

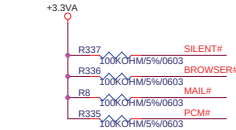
BC CHANGE

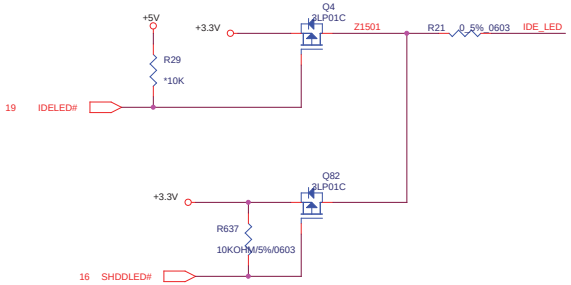
UNIWILL COMPUTER (SIP) Co.,LTD

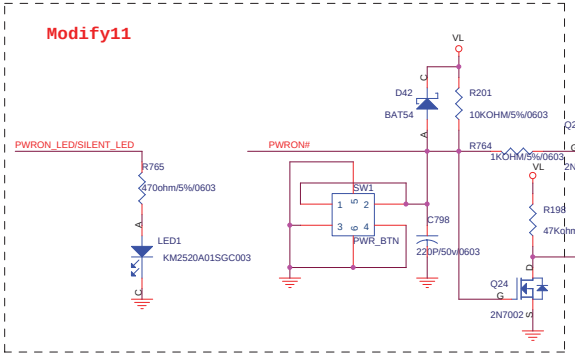
Title: X72IA6

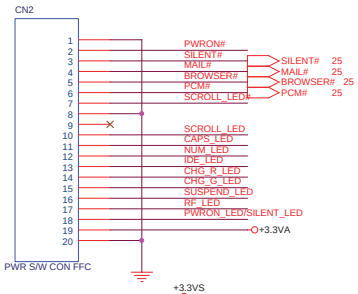
Size: | Document Number: SCHEMATIC1 | DDR2 Terminate/SMP/DC-IN | Rev: B

Date: Tuesday, April 11, 2006 | Sheet 14 of 32

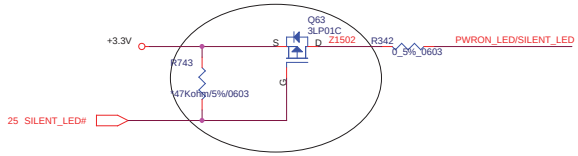


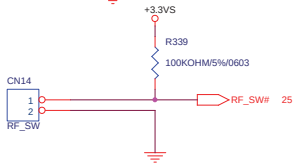


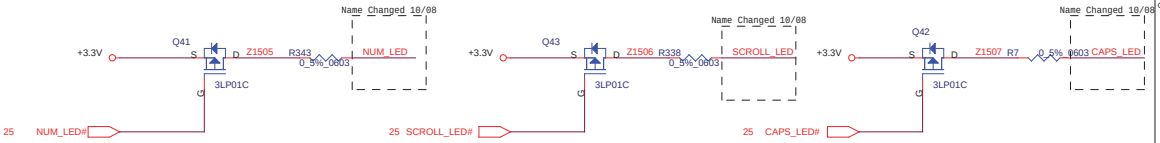




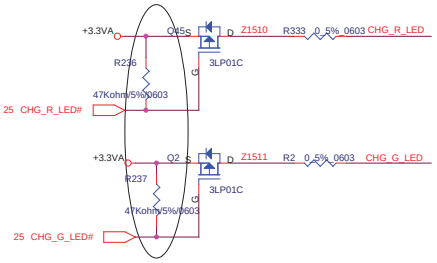
add silent fun
3/16/06

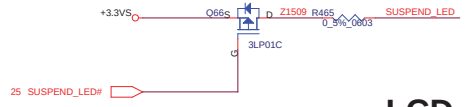




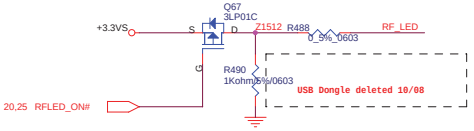


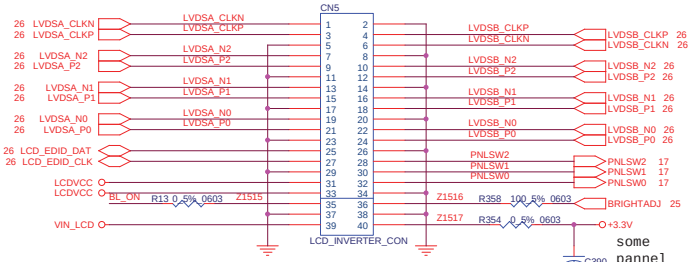
midify 3/16/06





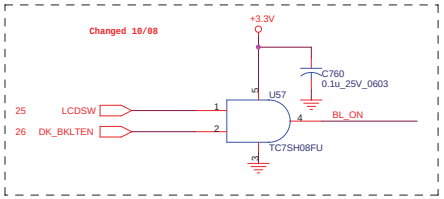
LCD





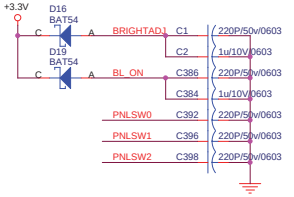
some pannel without bypass C in lcd PANNEL

INVERTER

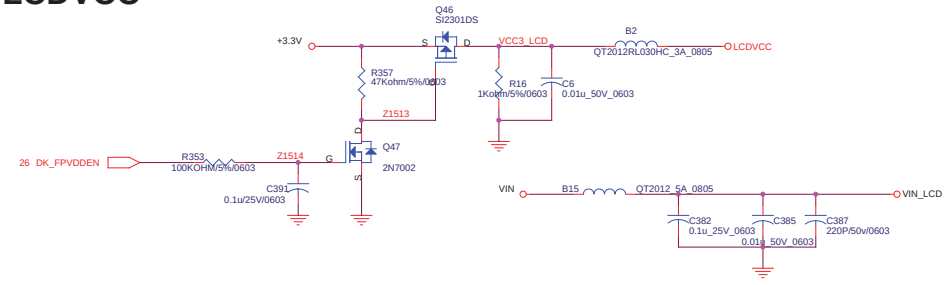


PANNEL SELECT

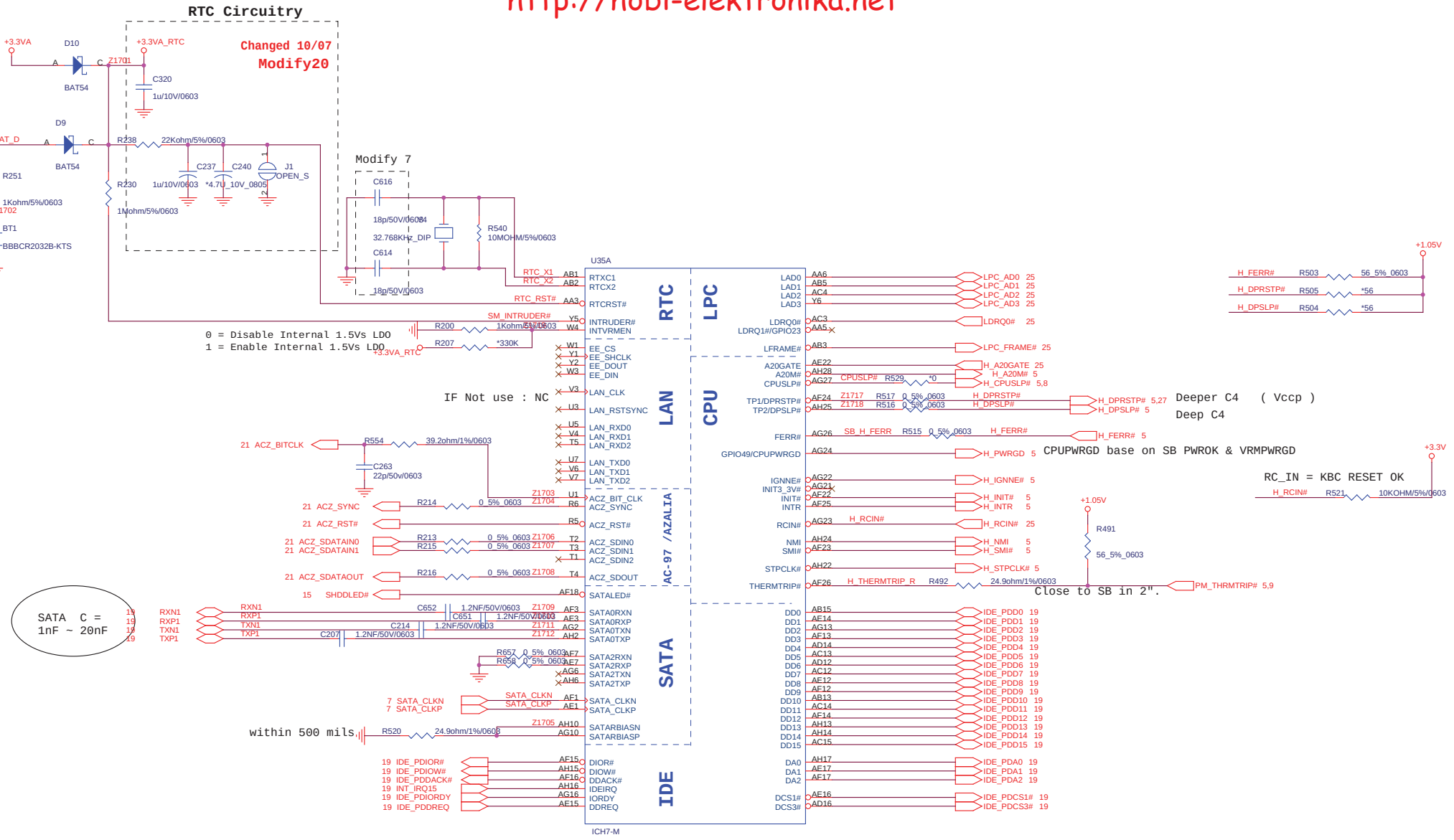
PNLSW2	PNLSW1	PNLSW0	
L	L	L	reserved
L	L	H	reserved
L	H	L	reserved
L	H	H	1280X800
H	L	L	1440X900
H	L	H	1680X1050
H	H	L	1920X1200
H	H	H	reserved



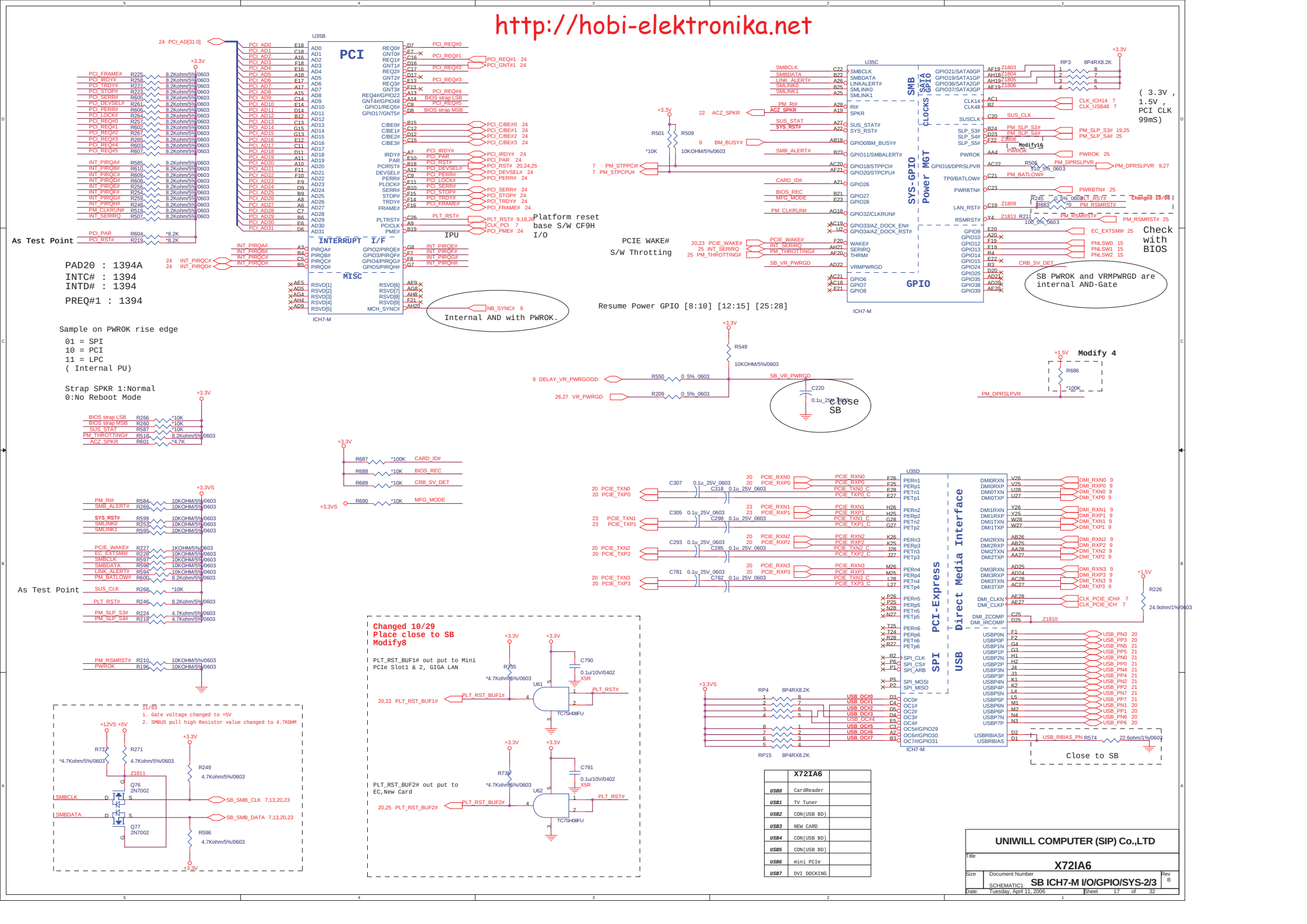
LCDVCC



UNIWILL COMPUTER (SIP) Co.,LTD	
Title	X72IA6
Size	Document Number SCHEMATIC1 PWR S/W/LCD/Invertor/CRT/TV Rev B
Date: Tuesday, April 11, 2006	Sheet 15 of 32

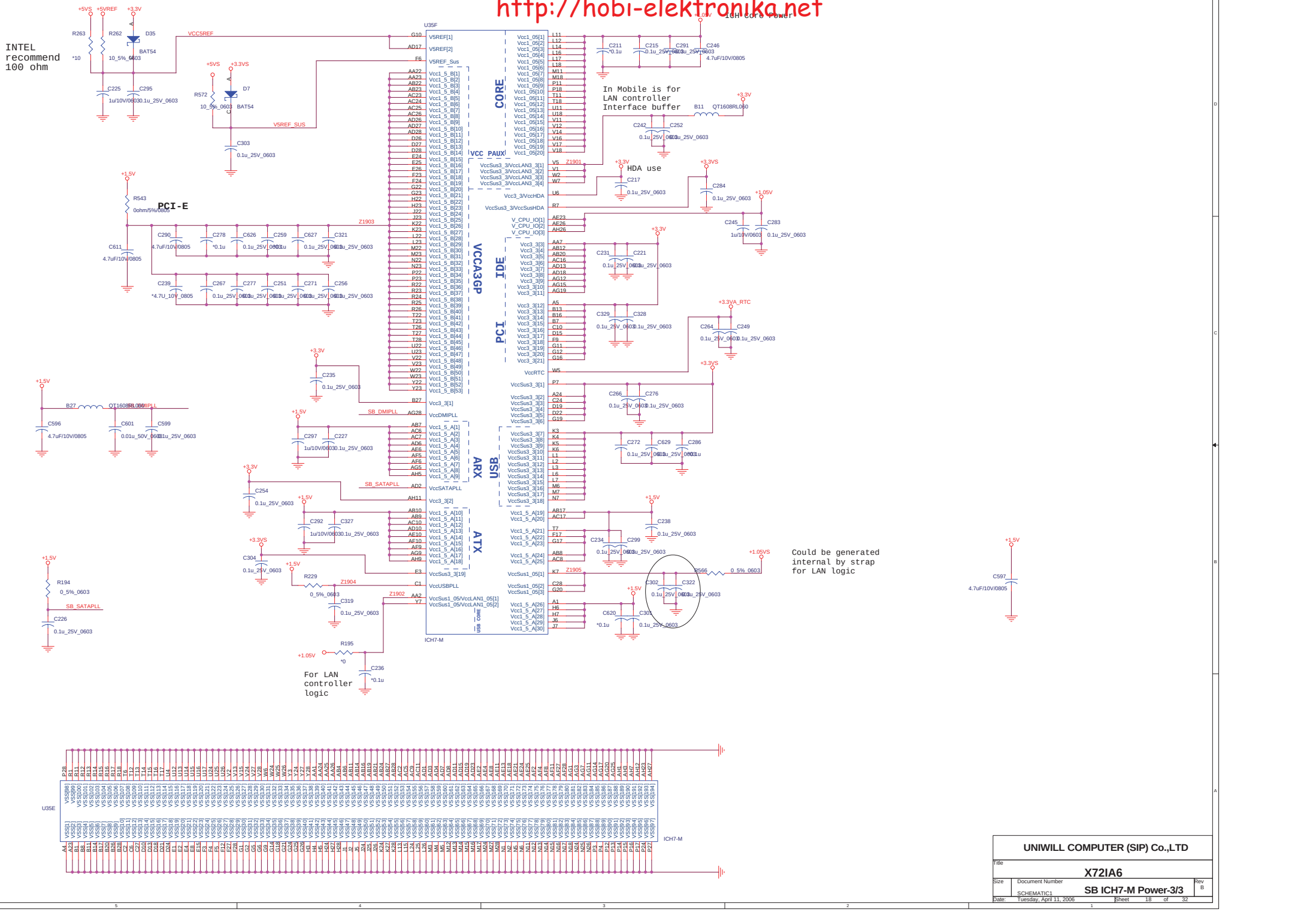


UNIWILL COMPUTER (SIP) Co.,LTD		
Title: X72IA6		
Size	Document Number: SCHEMATIC1 SB ICH7-M CPU/SATA/IDE-1/3	Rev: B
Date: Tuesday, April 11, 2006	Sheet 16 of 32	



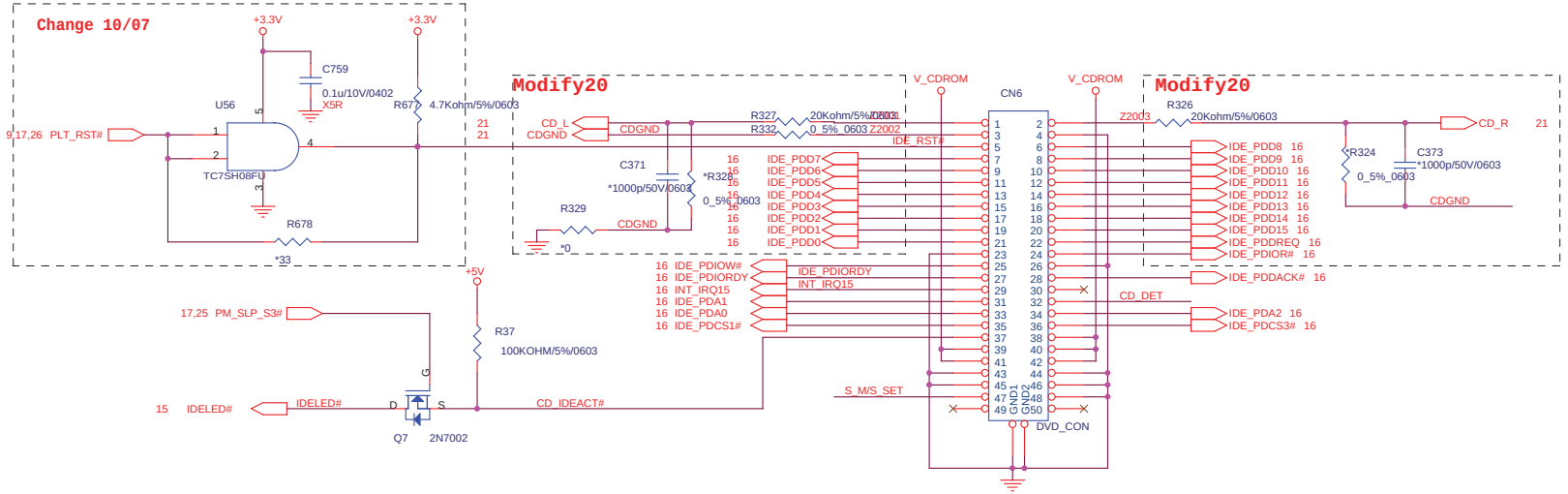
	X72IA6	
USB0	CardReader	
USB1	TV Tuner	
USB2	CON(USB BD)	
USB3	NEW CARD	
USB4	CON(USB BD)	
USB5	CON(USB BD)	
USB6	mini PCIe	
USB7	DVI DOCKING	

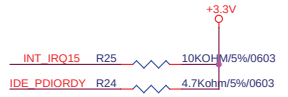
UNIWILL COMPUTER (SIP) Co.,LTD		
Title: X72IA6		
Size	Document Number: SCHEMATIC1 — SB ICH7-M I/O/GPIO/SYS-2/3	Rev: B
Date: Tuesday, April 11, 2006	Sheet 17 of 32	



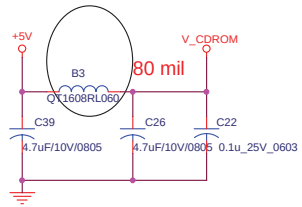
UNIWILL COMPUTER (SIP) Co.,LTD			
Title	X72IA6		
Size	Document Number	SB ICH7-M Power-3/3	Rev B
	SCHEMATIC1		
Date: Tuesday, April 11, 2006	Sheet 18 of 32		

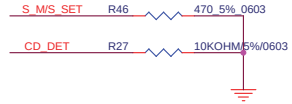
CR-ROM





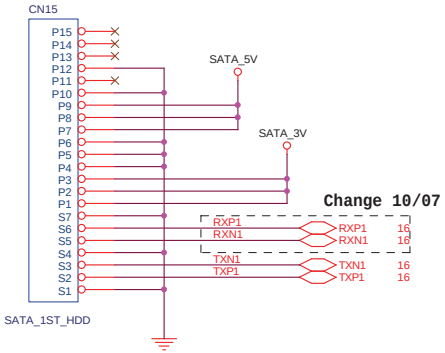
500mA Bead => 80 mils trace ?

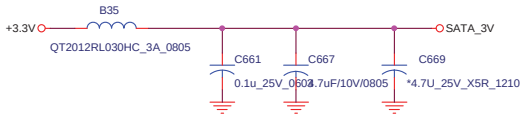


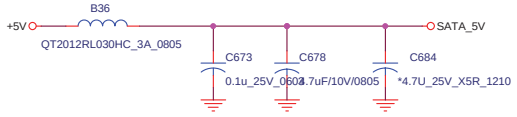


CSEL : Master = 0 / Slave = 1

SATA HDD







UNIWILL COMPUTER (SIP) Co.,LTD		
Title: X72IA6		
Size	Document Number: SCHEMATIC1 — HDD/CD-ROM CON	Rev: B
Date: Tuesday, April 11, 2006	Sheet 19 of 32	

2/22/2006

MINI CARD CONN

Intel PRO/Wireless 2100 LAN

PIN11	LED_WLAN_LINK	Hi(3.3V)	Solid ON	Associated AP
		Low(0V)	1 flash/3 sec LED OFF	Not Associated with an AP Power OFF or RF_Kill active
PIN12	LED_WLAN_ACT	Hi(3.3V)	Rapid Blinking Slow Blinking	Passing data traffic to AP Beacon traffic to Ap
		Low(0V)	LED OFF	Power OFF or not activity or RF_Kill active
PIN13	HW_RadioXMIT_OFF#	Hi(3.3V)	Enable	Radio transmitter is ON
		Low(0V)	Disable	Radio transmitter turn off

Changed_02/22

ADD 11/04
Modify14

Modify8

Modify_2/22

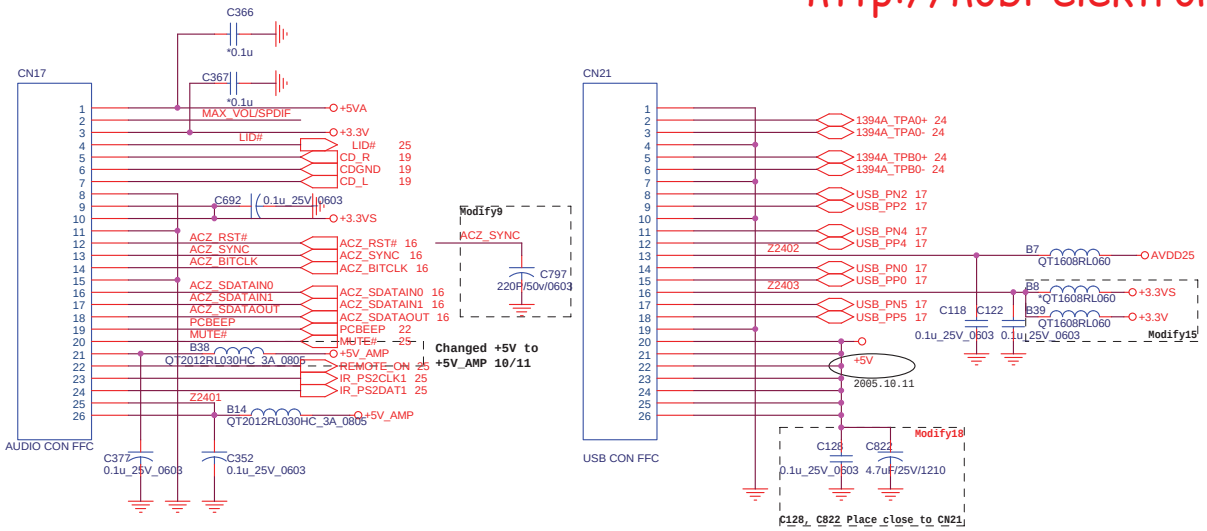
Place Close to Mini PCIe CONN

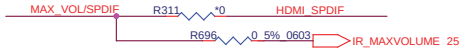
CLOSE TO OZ27C10L

CLOSE TO NEW CARD CON

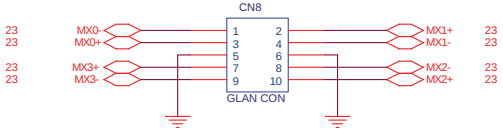
Modify4

UNIWILL COMPUTER (SIP) Co.,LTD			
Title	X72IA6		
Size	Document Number		Rev
	SCHEMATIC1	PCIe/New Card	B
Date: Tuesday, April 11, 2006		Sheet 20 of 32	



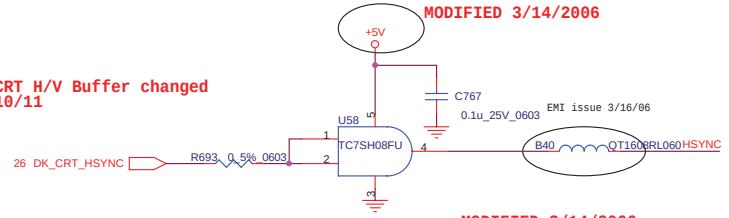


All the CMC placed on the sub BD

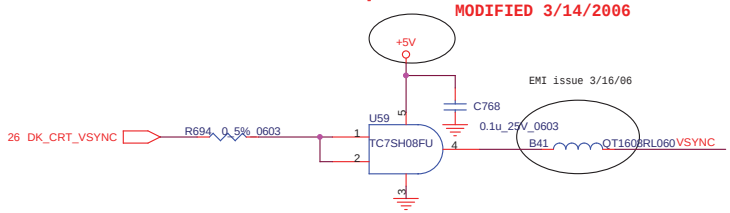


MODIFIED 3/14/2006

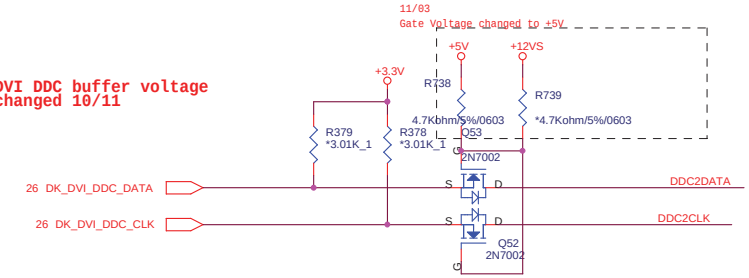
CRT H/V Buffer changed 10/11



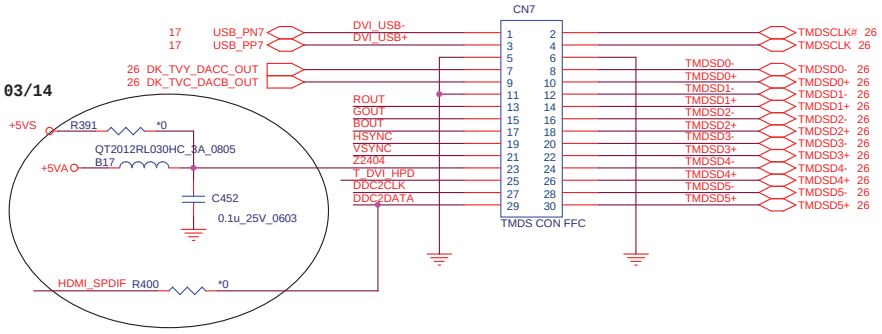
MODIFIED 3/14/2006



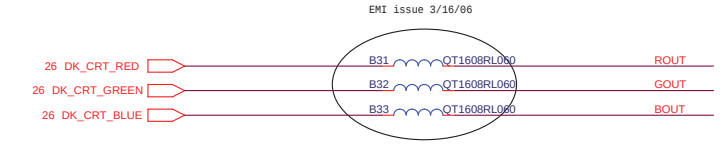
DVI DDC buffer voltage changed 10/11



Change 03/14



Reserve For HDMI Demo



UNIWILL COMPUTER (SIP) Co.,LTD		
Title: X72IA6		
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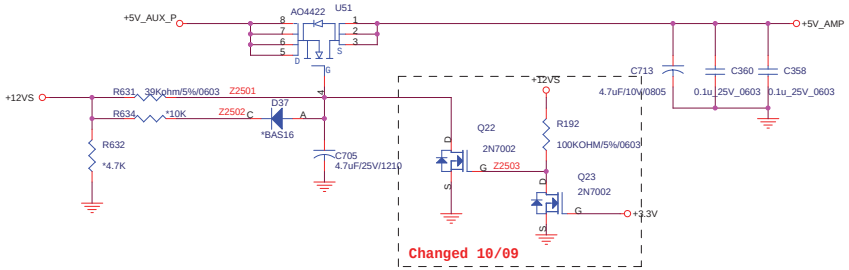
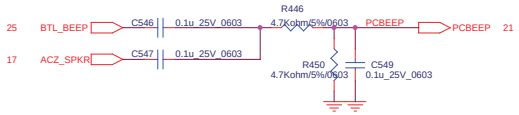
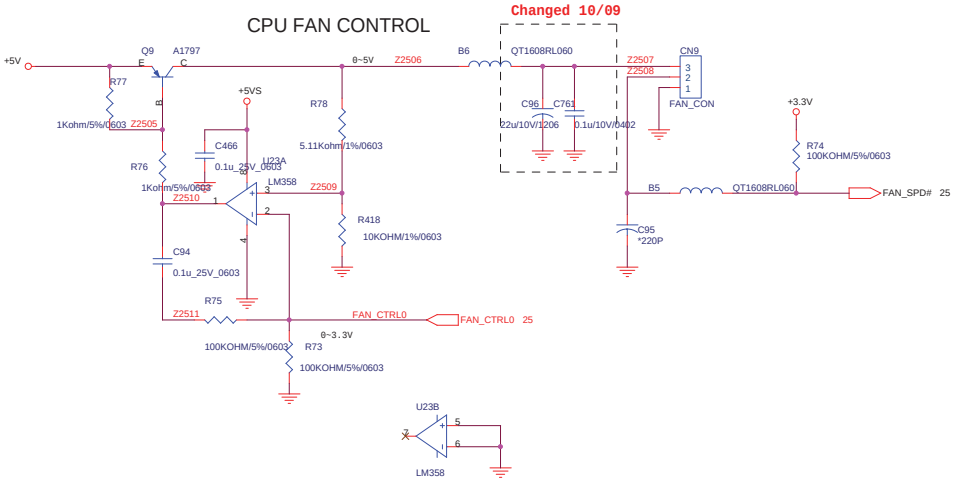
AMP VDD

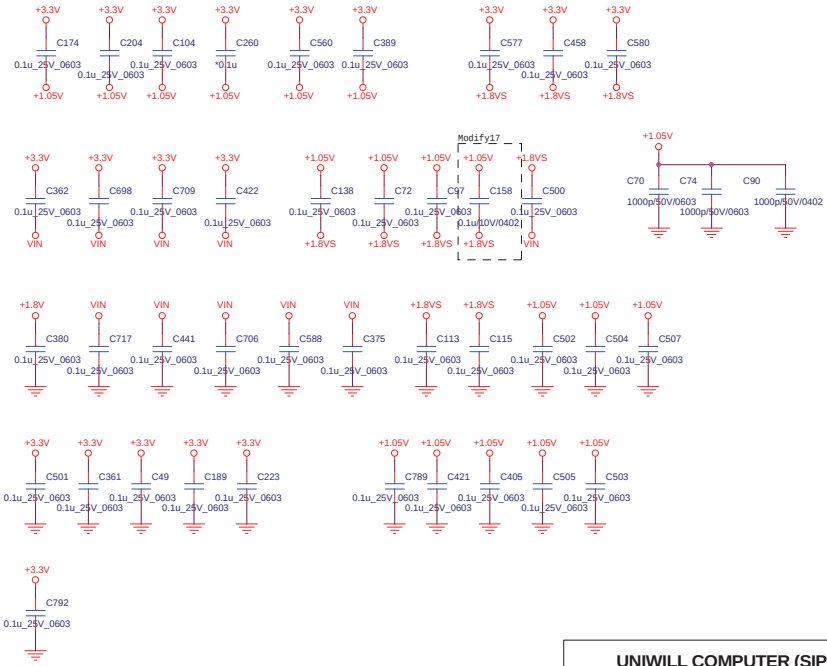




CPU FAN CONTROL



FOR EMI



UNIWILL COMPUTER (SIP) Co.,LTD		
Title	X72IA6	
Size	Document Number: SCHEMATIC1	Rev: B
Date: Tuesday, April 11, 2006	Sheet 22 of 32	Audio PWR/FAN CTL/EMI

If use 88E8053, Pin42,Pin43 must be pulled up to 3.3V with 4.7KOHM

R671 as close as possible to ASIC
88E8053: R671=4.87Kohm/1%/0603
R759,R760,R761,R762,R763 Stuff

88E8055: R671=4.99Kohm/1%/0603
(Default)R759,R760,R761,R762,R763 not Stuff

	88E8053	88E8055
AVDD25	2.5V	1.8V

Change Net name 12/12

7,13,17,20 SB_SMB_CLK
7,13,17,20 SB_SMB_DATA
17,20 PLT_RST_BUF1#
17,20 PCIE_WAKE#
7 CLK_PCIE_LAN
7 CLK_PCIE_LAN#
17 PCIE_RXP1
17 PCIE_RXN1
17 PCIE_TXP1
17 PCIE_TXN1

MDI3-/MDI3+ MDI2-/MDI2+ MDI1-/MDI1+ MDI0-/MDI0+

R663 R664 R665 R666 R667 R668 R669 R670 49.9ohm/1%/0402

C724 C725 0.1u/10V/0402 1000p/50V/0402 X7R
C726 C727 C728 C729 C730 C731 0.1u/10V/0402 1000p/50V/0402 X7R

Delete C733~C736

Add C763~C766

C763 C764 C765 C766 C732 0.1u/10V/0402 X7R

AVDD25

C739 C740 C741 C742 C743 0.1u/10V/0402 X7R

Note: Place Bypass Cap. as close as possible with every power pin.

3V3_main=0 at S5 for PnG function

Note: Must use 0402 or 0603 size

SB_SMB_CLK R659 *0
SB_SMB_DATA R660 *0

VPD_DATA
VPD_CLK

+3.3VS
VDD
AVDD25

U55 88E805X

PCIE_RXP1_LAN C722 0.1u/10V/0402
PCIE_RXN1_LAN C723 0.1u/10V/0402
R760 *0_5%_0402
R761 *0_5%_0402
PCIE_TXN1_LAN
PCIE_TXP1_LAN
PCIE_CLK_LAN
PCIE_CLK_LAN#
R762 *0_5%_0402
R763 *0_5%_0402

TX_P TX_N AVDDL AVDDL RX_N RX_P REFCLKP REFCLKN AVDDL VDD LED_LNK/ACTn LED_LINK10/100n VDDO_TTL LED_LINK1000n LED_LINKn VDD25 EPAD

VDD VMAIN_AVAL TESTMODE VDDO_TTL VDD SMDATA SMCLK VPD_DATA VDDO_TTL VDD VPD_CLK SPI_CLK SPI_CS SPI_DI SPI_DO VDD

AVDDL MDIN[3] MDIP[3] TSTPT AVDDL MDIN[2] MDIP[2] HSDACN HSDACP AVDD AVDDL MDIN[1] MDIP[1] AVDDL MDIN[0] MDIP[0]

MDI3- MDI3+ MDI2- MDI2+ MDI1- MDI1+ MDI0- MDI0+

VDDO_TTL VDD CTRL12 CTRL25 PERSTn WAKEn VDD VDDO_TTL_MAIN SWTCH_VAUX LOM_DISABLEn SWTCH_VCC VAUX_AVLBL VDD XTALO XTALI RSET

R759 *0_5%_0402
R671 4.99Kohm/1%/0402
XTALI
XTALO

+3.3VS
CTRL12
CTRL25
Change Net name 12/12
PLT_RST_BUF1#
PCIE_WAKE#
R672 0_5%_0603
R673 4.7Kohm/5%/0603

88E8053 rev. A2 issue:
Reset IC to delay 250ms when VAUX33 available.
Or use GPIO to control LOM_DISABLEn

+3.3VS
R661 R662 4.7Kohm/5%/0603
U54 M24C08 EEPROM
VPD_CLK VPD_DATA
C721 0.1u/10V/0402 X7R

Modify5
Y6 CRYSTAL 25MHz
C737 C738 22p/50V/0402 NPO

+3.3VS
C744 4.7uF/10V/0805 Y5V
C746 0.1u/10V/0402 X7R
C745 4.7uF/10V/0805 Y5V
R674 4.7Kohm/5%/0603
Q88 A1797
CTRL12
VDD
C747 4.7uF/10V/0805 Y5V
C748 0.1u/10V/0402 X7R

VDD
C755 C756 C757 C758 0.1u/10V/0402 X7R

Changed 10/08

+3.3VS
L15 QT1608RL060HC_3A_0603
C751 0.1u/10V/0402 X7R
C749 4.7uF/10V/0805 Y5V
C752 0.1u/10V/0402 X7R
C750 4.7uF/10V/0805 Y5V
R675 4.7Kohm/5%/0603
Q89 A1797
CTRL25
+1.8VS
L17 *QT1608RL060HC_3A_0603
AVDD25
C753 4.7uF/10V/0805 Y5V
C754 0.1u/10V/0402 X7R

PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS
25MIL

For PCIE and IEEE1394 current return path

+3.3V
C772 C773 C774 C775 0.1u/10V/0402 X7R

Title	X72IA6
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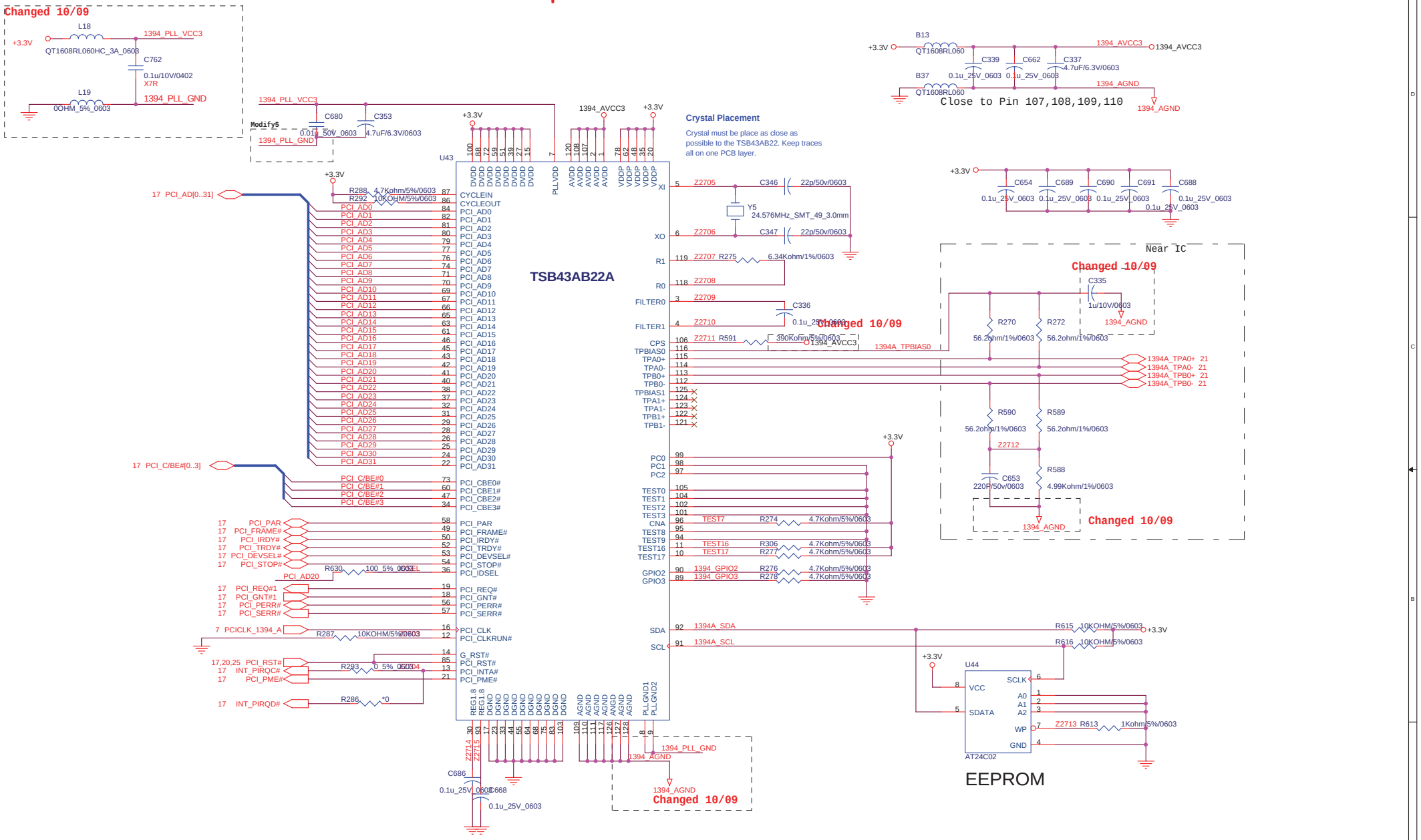
UNIWILL COMPUTER (SIP) Co.,LTD



K/B CONTROLLER

IT8510E
Embedded Controller

Power Supply
System & LPC Bus
KB Matrix Interface
Flash Interface

RC_IN = KBC RESET

CHECK WITH EC

change 3/15/2006

Modify12

Debug CON 3801-X14XR

80 Port

TOOHPAD CONNECTOR

solving IR remote controller's PS/2 pull high weak issue

11/03 Gate voltage changed to +5V

Thermal IC , CLK GEN

Only VGA

Only BAT

FLASH ROM

A29040L

KEYBOARD_CON

solving system power off lekage current over 2mA@10.8V issue

STRAP define

(ID2) NUMLED#	(ID1) CAPLED#	(ID0) SCROLED#	ID / MODEL
0	0	0	X72IA6
0	0	1	X52IA6
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

	BSEL2	BSEL1	BSEL0	MHZ
PSB533	0	0	1	133
PSB667	0	1	1	166

UNIWILL COMPUTER (SIP) Co.,LTD

Title: X72IA6

Size: | Document Number: SCHEMATIC1 | EC IT8510E/BIOS/TP CON | Rev: B

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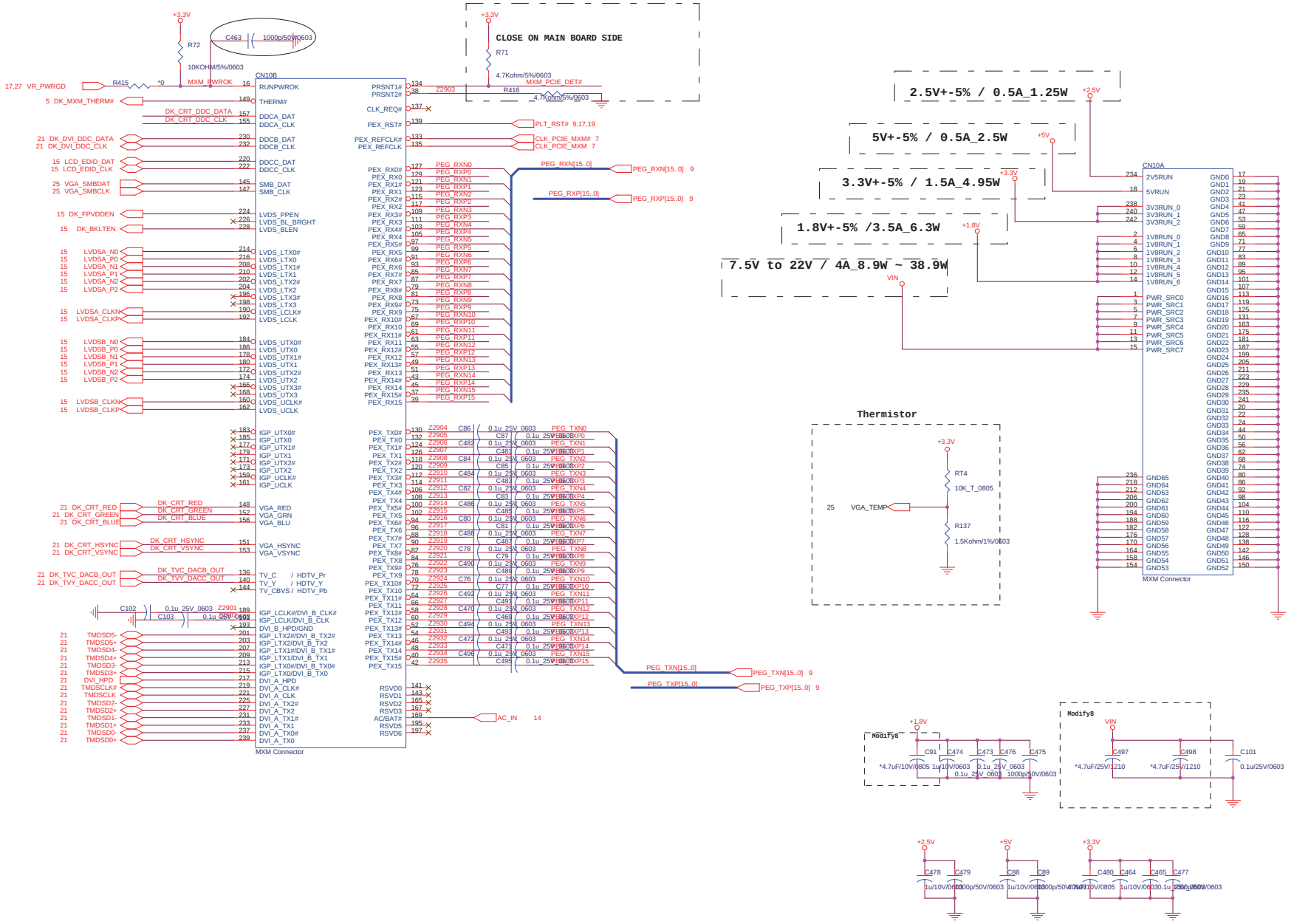
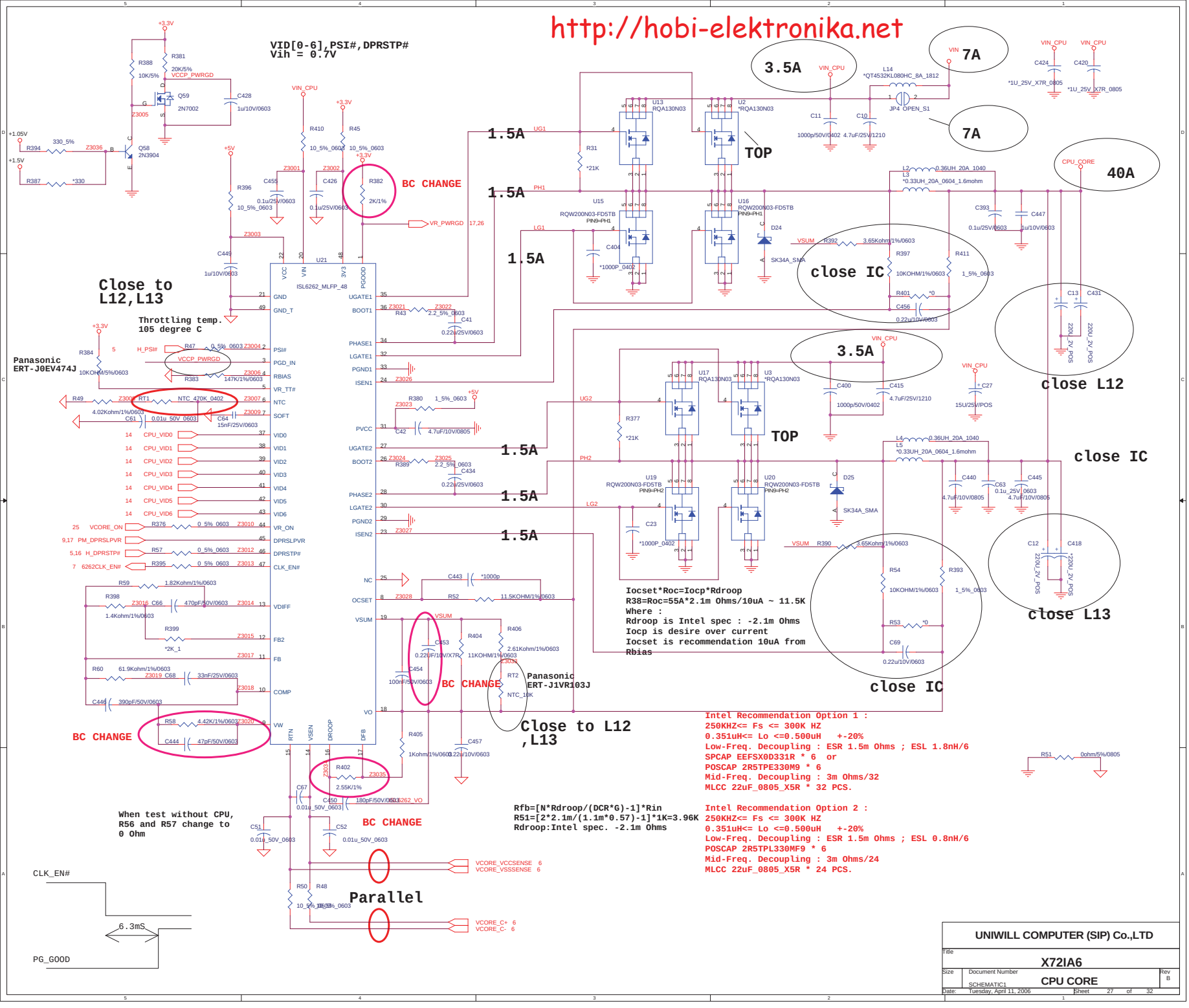


UNIWILL COMPUTER (SIP) Co.,LTD	
Title	X72IA6
Size	Document Number: SCHEMATIC1 — VGA MXM CON — Rev B
Date: Tuesday, April 11, 2006	Sheet 26 of 32



UNIWILL COMPUTER (SIP) Co.,LTD	
Title	X72IA6
Size / Document Number	CPU CORE
Rev	B
Date: Tuesday, April 11, 2006	Sheet 27 of 32

ON Vih = 0.6V

0.6V ~ 2.1V = PWM ON
> 2.1V PWM + SKIP

ALL CLOSE IC

813_VREF = 2.75 V

OZ813

OZ813_QFN24

ALL CLOSE IC

ALL CLOSE IC

1.5A

1A

1A

BC CHANGE

ALL CLOSE IC

6A

+1.5VS
NB: 2A

+1.5V
NB: 2A
SB :1A
others :1A

BC CHANGE

+1.05VS
SB: ~ 0 A

+1.05V
CPU : 2.5A (MAX = 6A at boot)
NB: 2.5A
SB :1A

1A

1A

BC CHANGE

ALL CLOSE IC

10A

ALL CLOSE IC

1.5A

mem = 6A
MXM = 2A
0.9Vs = 2A

BC CHANGE

10A

DDR2 Termination Power

2A

818_VREF = 2.75 V

OZ818

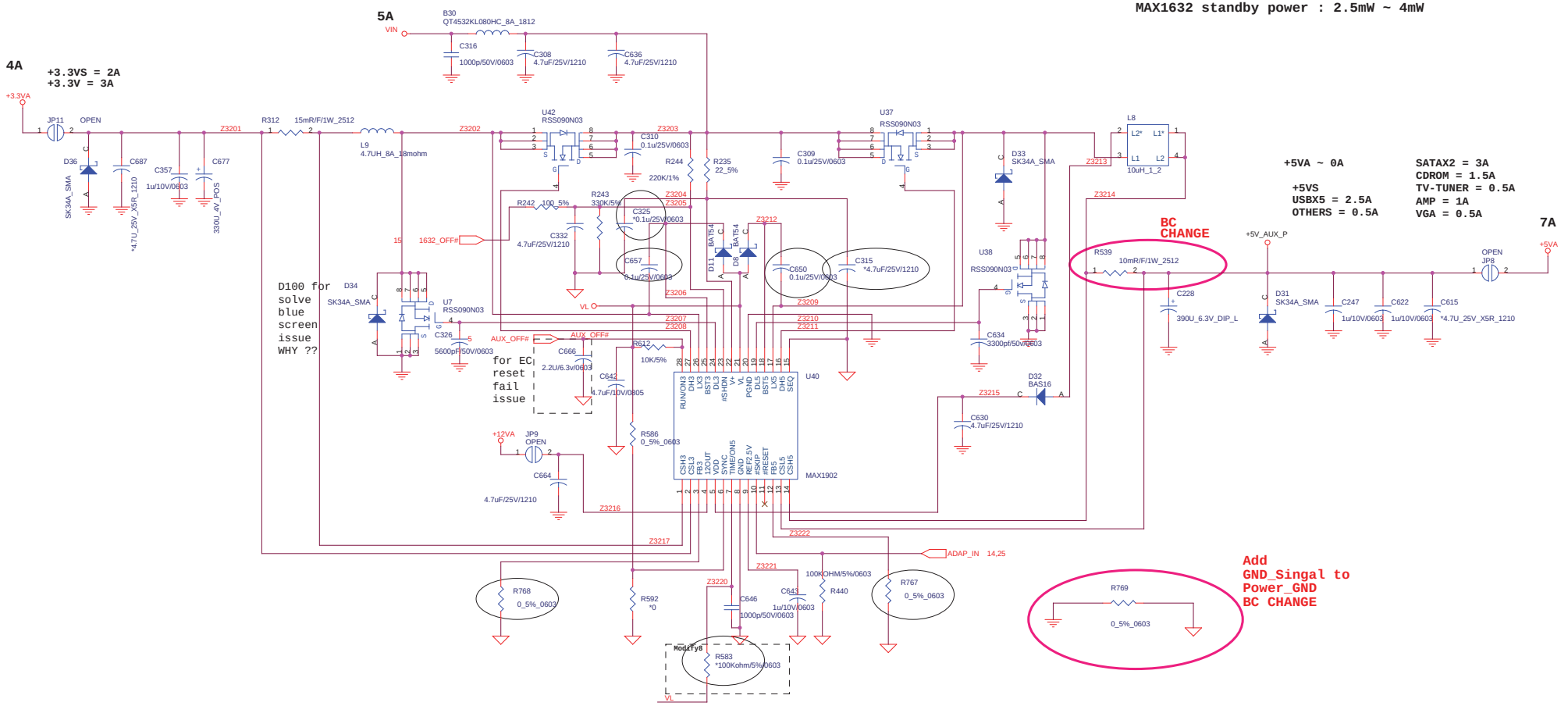
ALL CLOSE IC

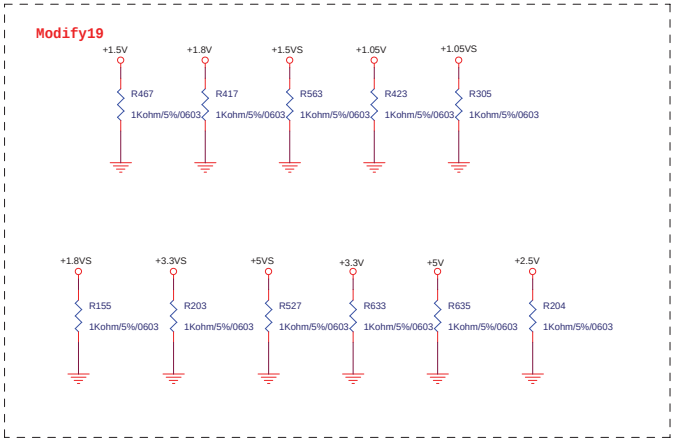
ON Vih = 0.6V

ALL CLOSE IC

UNIWILL COMPUTER (SIP) Co.,LTD	
Title	X72IA6
Size	Document Number: SCHEMATIC1 — 1.05V/1.5V/1.8V/2.5V/0.9V — Rev: B
Date: Tuesday, April 11, 2006	Sheet 28 of 32

MAX1632 shutdown current : 4~10uA (SHDN# pin = low)
MAX1632 standby power : 2.5mW ~ 4mW





	MAX1632 MAX1902	SC1404
R767	0	100pF
R768	0	100pF
R583	100K_OP	100K
R312,R539	15mR,15mR	8mR,8mR
C315	OP	4.7U_25V
C325	OP	0.1U_25V
C650,C657	0.1U_16V	0.22U_25V

UNIWILL COMPUTER (SIP) Co.,LTD		
Title: X72IA6		
Size	Document Number: SCHEMATIC1	Rev: B
	+3.3VA/+5VA/+12VA	
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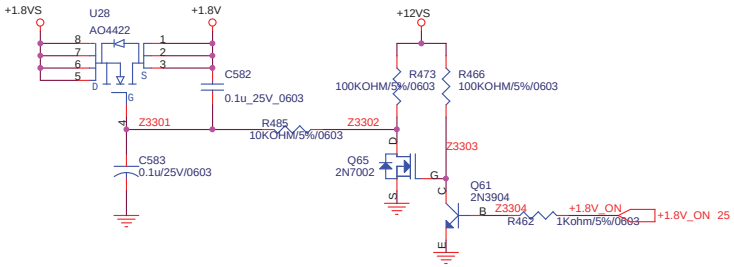

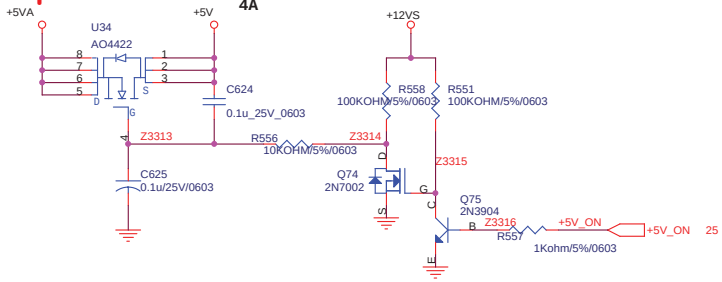

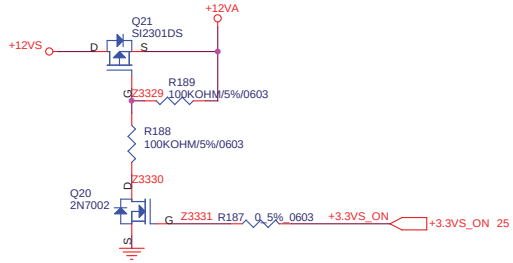

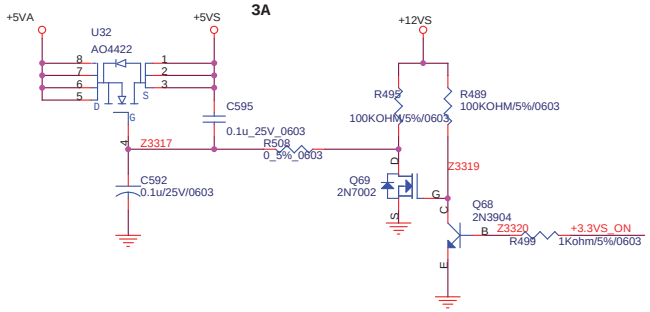

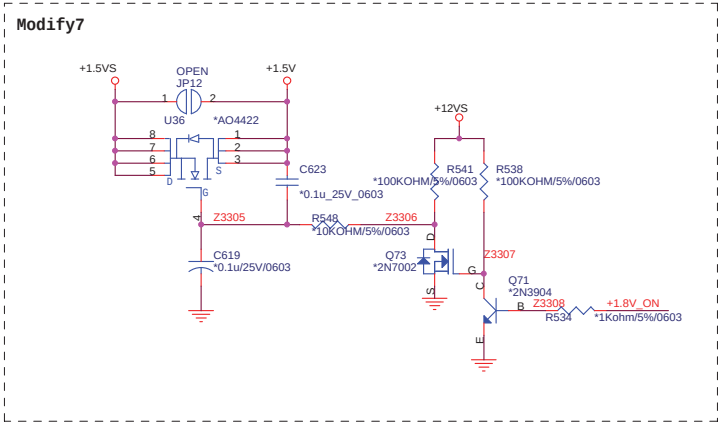

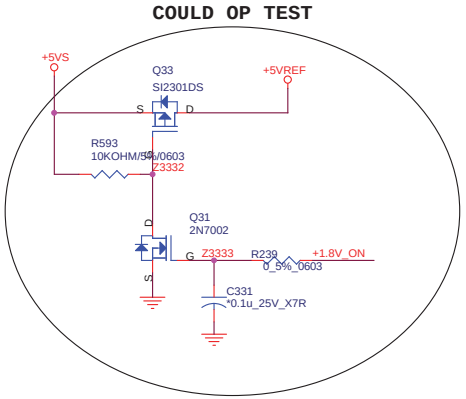

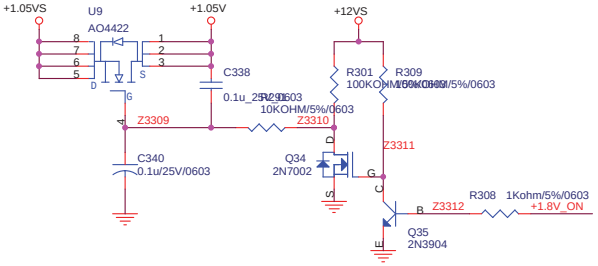

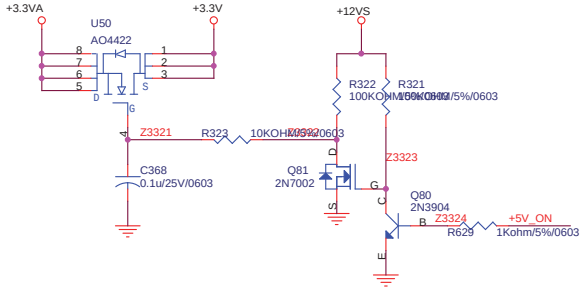

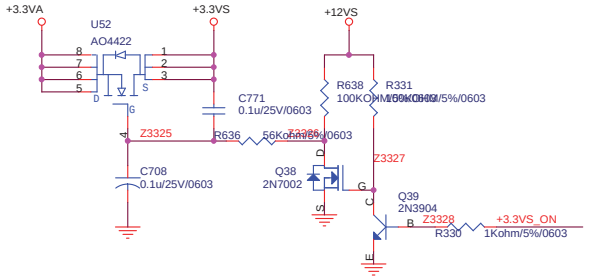

UNIWILL COMPUTER (SIP) Co.,LTD		
Title: X72IA6		
Size	Document Number: SCHEMATIC1 — VCC SW/+1.05VS/+1.5VS	Rev: B
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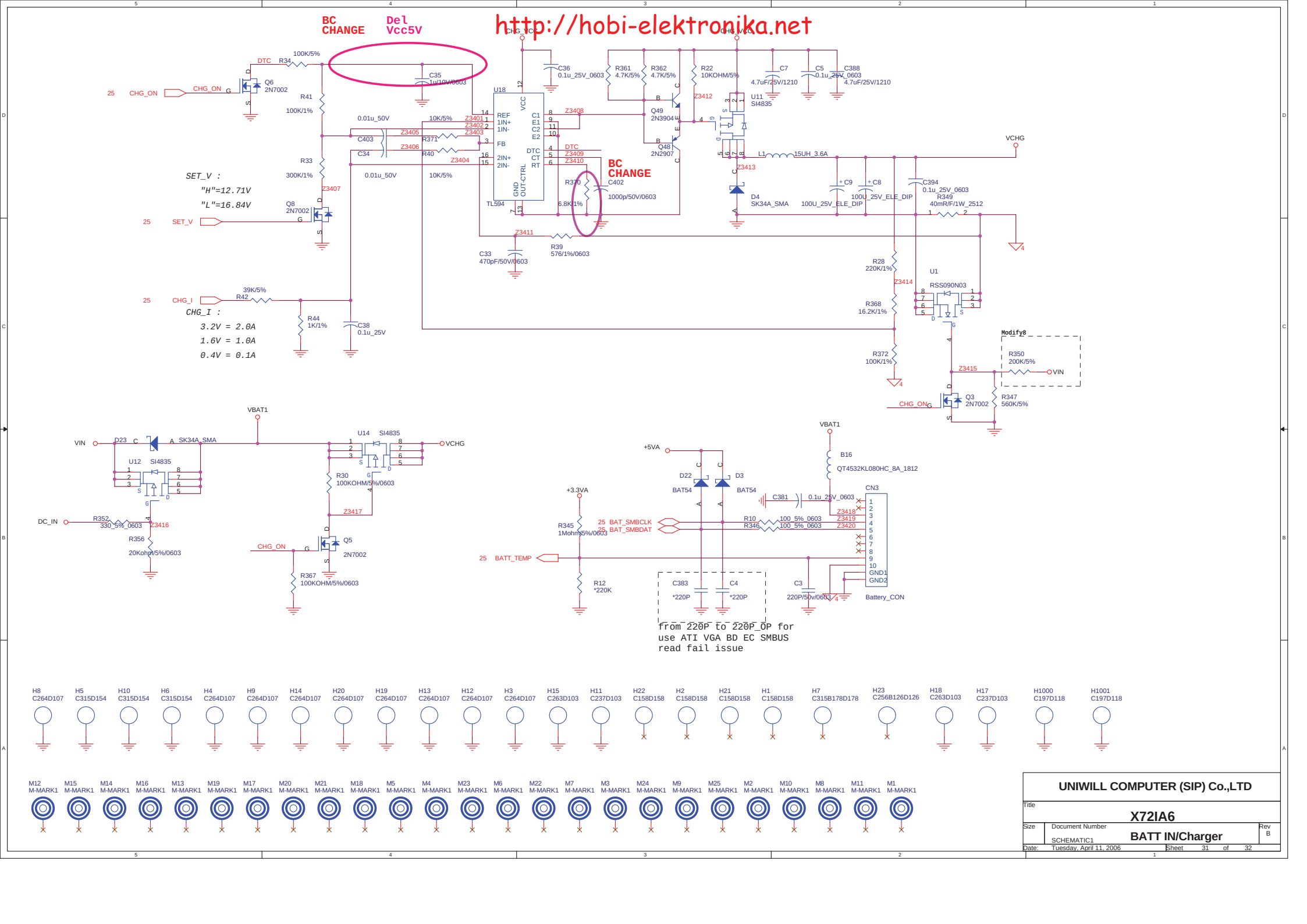
BC CHANGE
Del Vcc5V
http://hobi-elektronika.net
CHG_VCC
CHG_VCC
CHG_ON
Q6 2N7002
R34 100K/5%
C35 1u/10V/0603
R41 100K/1%
C403
C34
R371
R40
R33 300K/1%
Z3407
Q8 2N7002
SET_V
SET_V :
"H"=12.71V
"L"=16.84V
CHG_I
R42 39K/5%
R44 1K/1%
C38 0.1u_25V
CHG_I :
3.2V = 2.0A
1.6V = 1.0A
0.4V = 0.1A
U18
TL594
REF
1IN+
1IN-
FB
2IN+
2IN-
GND
OUT-CTRL
VCC
C1
E1
C2
E2
DTC
CT
RT
C36 0.1u_25V_0603
R361 4.7K/5%
R362 4.7K/5%
R22 10KOHM/5%
C7 4.7uF/25V/1210
C5 0.1u_25V_0603
C388 4.7uF/25V/1210
Q49 2N3904
Q48 2N2907
U11 SI4835
BC CHANGE
R370 6.8K/1%
C402 1000p/50V/0603
R39 576/1%/0603
C33 470pF/50V/0603
L1 15UH_3.6A
D4 SK34A_SMA
C9 100U_25V_ELE_DIP
C8 100U_25V_ELE_DIP
C394 0.1u_25V_0603
R349 40mR/F/1W_2512
VCHG
R28 220K/1%
U1 RSS090N03
R368 16.2K/1%
R372 100K/1%
Modify8
R350 200K/5%
VIN
Z3415
Q3 2N7002
R347 560K/5%
CHG_ON
VBAT1
VIN
D23 SK34A_SMA
U12 SI4835
U14 SI4835
VCHG
R30 100KOHM/5%/0603
Z3417
DC_IN
R352 330_5%_0603
Z3416
R356 20Kohm/5%/0603
Q5 2N7002
R367 100KOHM/5%/0603
+5VA
+3.3VA
D22 BAT54
D3 BAT54
B16 QT4532KL080HC_8A_1812
C381 0.1u_25V_0603
CN3
BAT_SMBCLK
BAT_SMBDAT
R10 100_5%_0603
R346 100_5%_0603
R345 1Mohm/5%/0603
BATT_TEMP
R12 *220K
C383 *220P
C4 *220P
C3 220P/50v/0603
GND1
GND2
Battery_CON
from 220P to 220P_0P for
use ATI VGA BD EC SMBUS
read fail issue
H8 C264D107
H5 C315D154
H10 C315D154
H6 C315D154
H4 C264D107
H9 C264D107
H14 C264D107
H20 C264D107
H19 C264D107
H13 C264D107
H12 C264D107
H3 C264D107
H15 C263D103
H11 C237D103
H22 C158D158
H2 C158D158
H21 C158D158
H1 C158D158
H7 C315B178D178
H23 C256B126D126
H18 C263D103
H17 C237D103
H1000 C197D118
H1001 C197D118
M12 M-MARK1
M15 M-MARK1
M14 M-MARK1
M16 M-MARK1
M13 M-MARK1
M19 M-MARK1
M17 M-MARK1
M20 M-MARK1
M21 M-MARK1
M18 M-MARK1
M5 M-MARK1
M4 M-MARK1
M23 M-MARK1
M6 M-MARK1
M22 M-MARK1
M7 M-MARK1
M3 M-MARK1
M24 M-MARK1
M9 M-MARK1
M25 M-MARK1
M2 M-MARK1
M10 M-MARK1
M8 M-MARK1
M11 M-MARK1
M1 M-MARK1
UNIWILL COMPUTER (SIP) Co.,LTD
Title
X72IA6
Size
Document Number
SCHEMATIC1
BATT IN/Charger
Rev B
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Rev: B

Modify2: I945PM Add Thermal Strap, Add R755, Delete D5 at Page09

Modify3: Reserved R112 at Page09

Modify4: Revise NewCard Power supply, Reserved R234, Stuff R231 & change to 4.7KOHM , Add R756,R757,R758,R766 at Page20

Modify5: Revise 1393 PLL Ground, Change C680,C353 GND net to 1394_PLL_GND at Page24

Modify6: For cost down, Change Y6 P/N at Page23

Modify7: Change +1.5V Power Supply method, Reserve U36,Q73,Q71,C619,C623,R534,R538,R541,R548 at Page30

Modify8: Change U4 P/N at Page4,5
Change R350 P/N at Page31,
Change R510,R513 P/N at Page07
Change Q88,Q89 P/N at Page23
Change CN27 C794,C795,C796 P/N at Page20
Reserve R583 at Page29
Reserve C91,C497,C498 at Page26
Reserve R735, R736 at Page17

Modify9: For solve ACZ_BITCLK crosstalk on ACZ_SYNC, Add C797 at Page21

Modify10: For 88E8053,88E8055 Pin-To-Pin compatible, Add & Reserved R759,R760,R761,R762,R763 at Page23
R671 changed to 4.99Kohm for 88E8055

Modify11: Add R764,R765,SW1,LED1,C798,D42 at Page15

Modify12: Debug Connector signal define changed at Page25

Modify13: Add Low pass circuit for clock at Page07

Modify14: According to the SIM_Card's Requirement, CN27 Pin8 connect to +3.3V & Add C820 at Page20

Modify15: Add B39 and Reserved B8, for CardReader Power Supply Changed to +3.3V. at Page21

Modify16: Delete TP1,TP2,TP3,TP4,TP6,TP7,TP8,TP9,TP12,TP13,TP14,TP15

Modify17: Revise C158's Net at Page22;
Add C821 at Page12;
Stuff C800,C801,C802,C803 at Page07
For solve CPU_CLK duty cycle under Spec issue.

Modify18: Add C822 for USB Drop test fail issue at Page21

Modify19: To Decrease static current under S3, Change R155, R203, R204, R305, R417, R423,
R467, R527, R563, R633 P/N at Page29.

Modify20: Delete Analog CD_In Circuit at Page19
Reserve R326, R327,R332, C371, C373;
Change R324, R328 P/N

Modify21: Del D27,D14,C315,C325,L3,L5, C637, C659
Change C218,R535,R402,C453,C454,R312,R539,C657,C650,U40,L1,C677,C365 P/N
Add L2,L4, R767, R768

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	Appendix A.Ver.History	
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