DRESDEN-INT

PCB Thinckness:1.1mm

CPU : AMD GRIFFIN
Chip Set : AMD RS780MN + SB700
Remarks : AMD PUMA Platform w/ IGP
2 SODIMMs DDR2

Model Name : DRESDEN-INT
PBA Name : MAIN
PCB Code : BA41-01024A (GCE)
BA41-01025A (NY)
BA41-01026A (HST)
Dev. Step : MP(PR)
Revision : 1.00
T.R. Date : 2008.12.24

DRAW	CHECK	APPROVAL
-	-	-

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APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A
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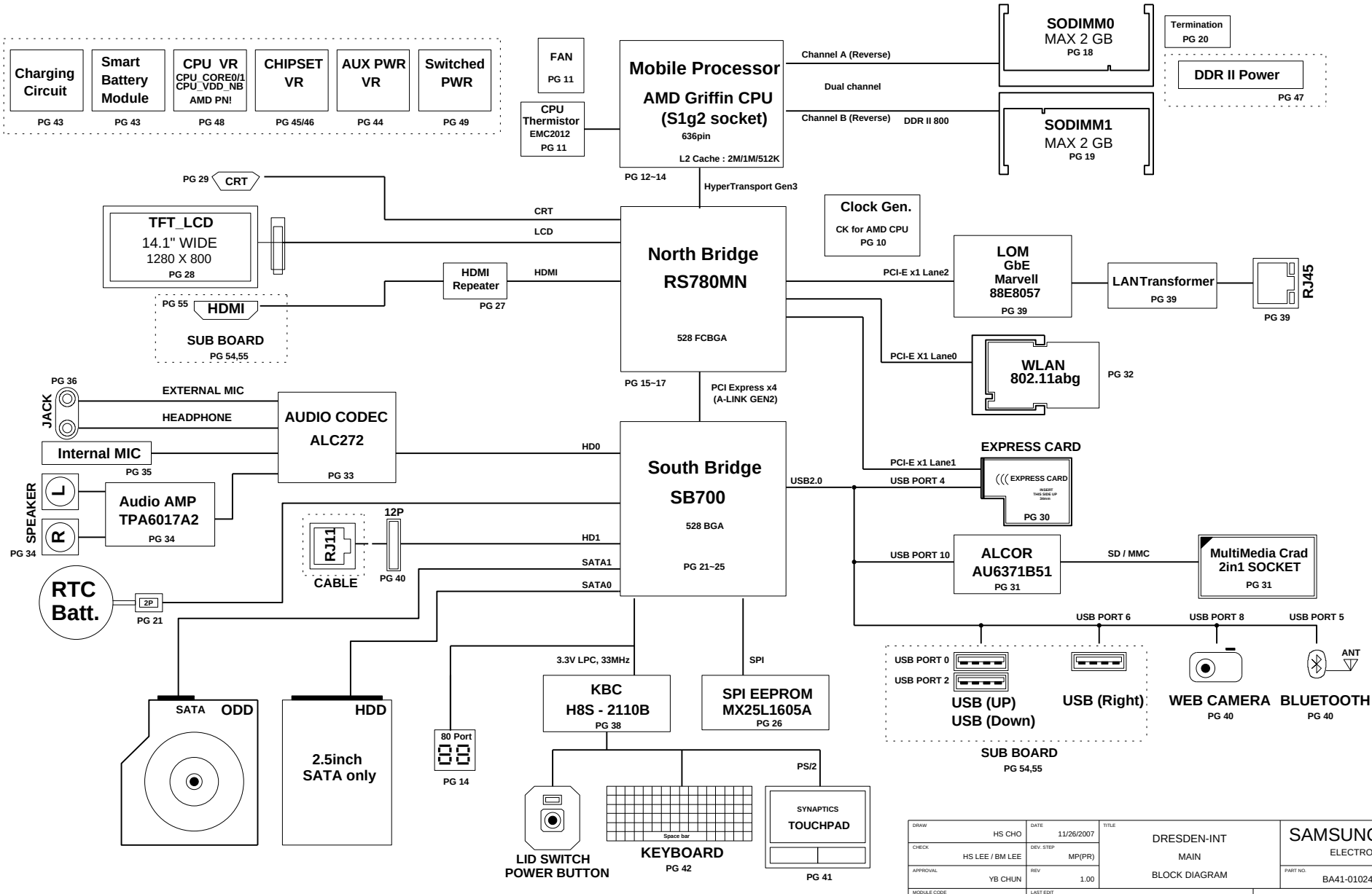
OPERATION BLOCK DIAGRAM



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APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A
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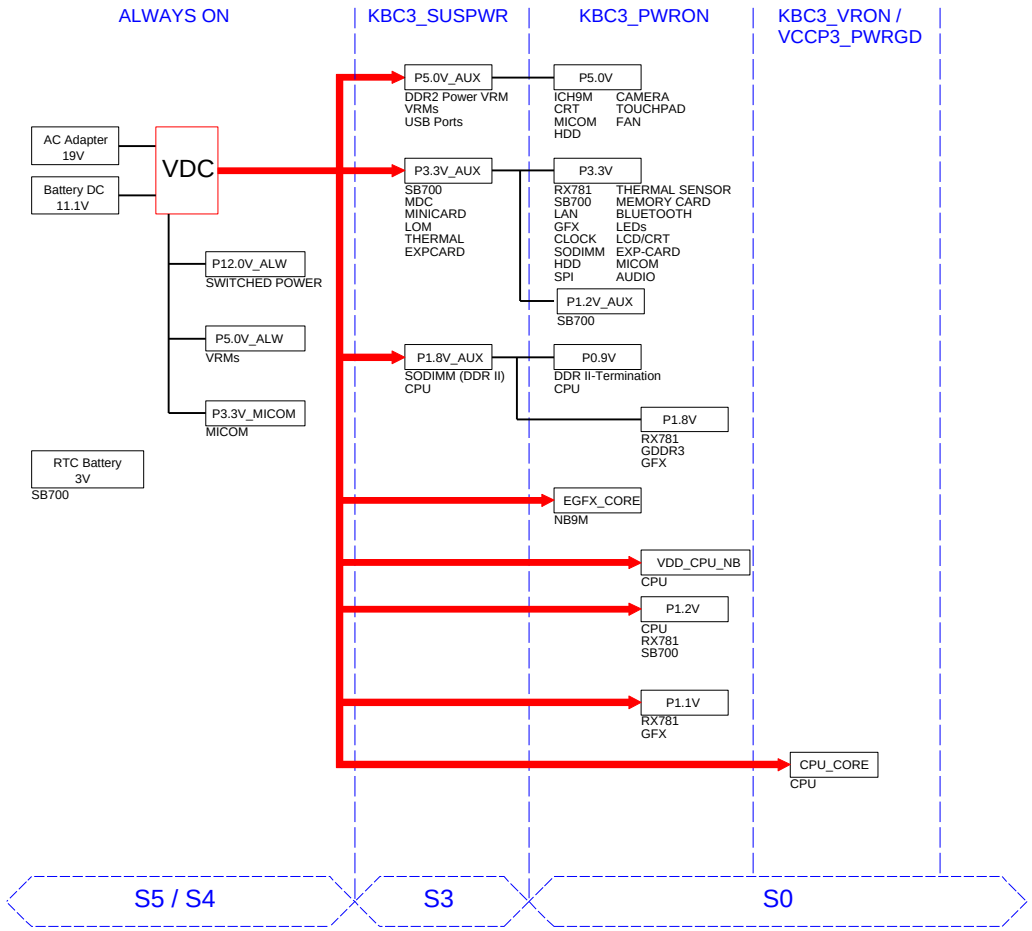
POWER DIAGRAM



Rail / State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	OFF	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

DRAW: HS CHO	DATE: 11/26/2007	TITLE: DRESDEN-INT / MAIN / POWER DIAGRAM	SAMSUNG ELECTRONICS		
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APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A		
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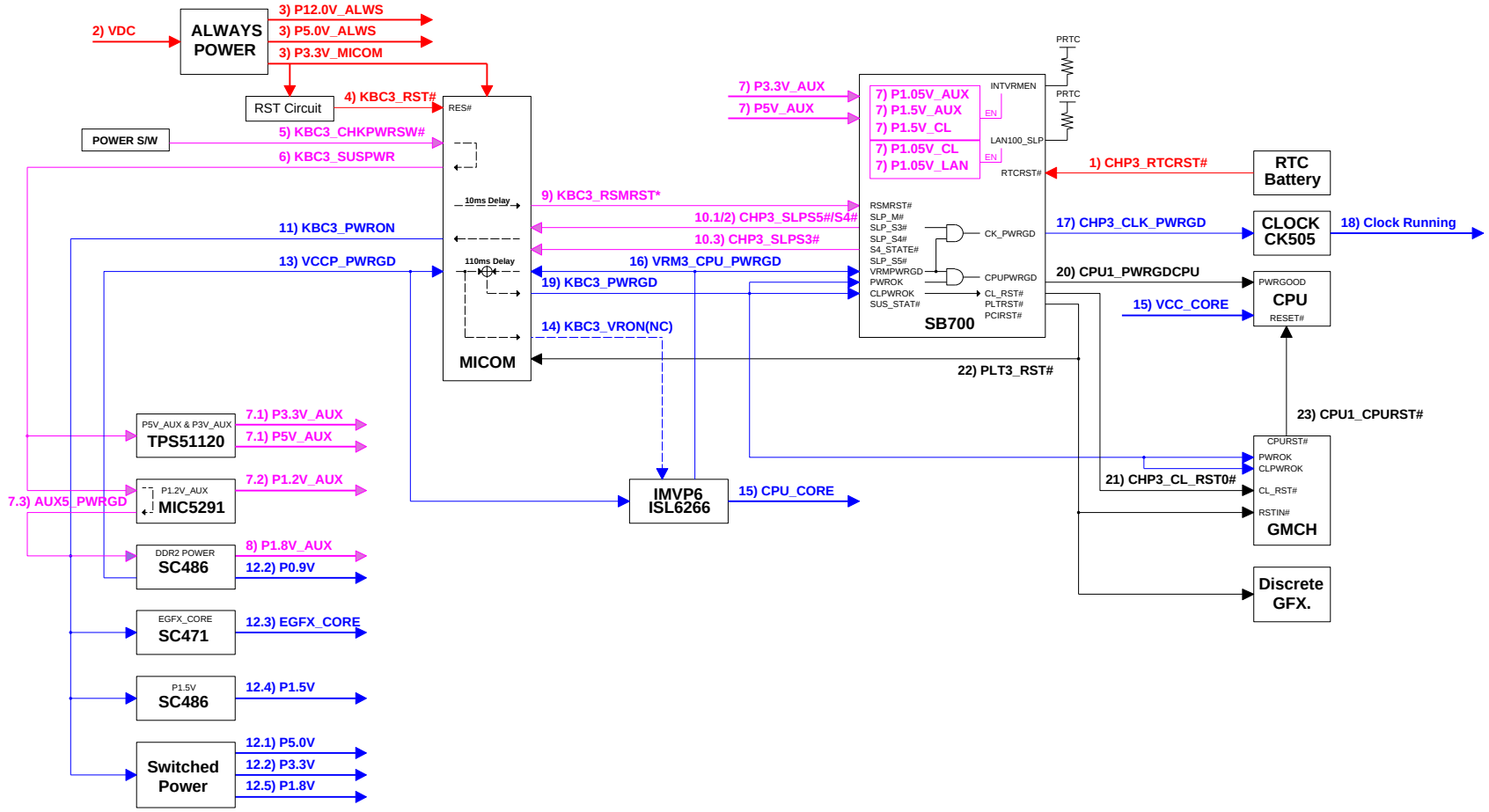
POWER SEQUENCE Rev. 0.1



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CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A
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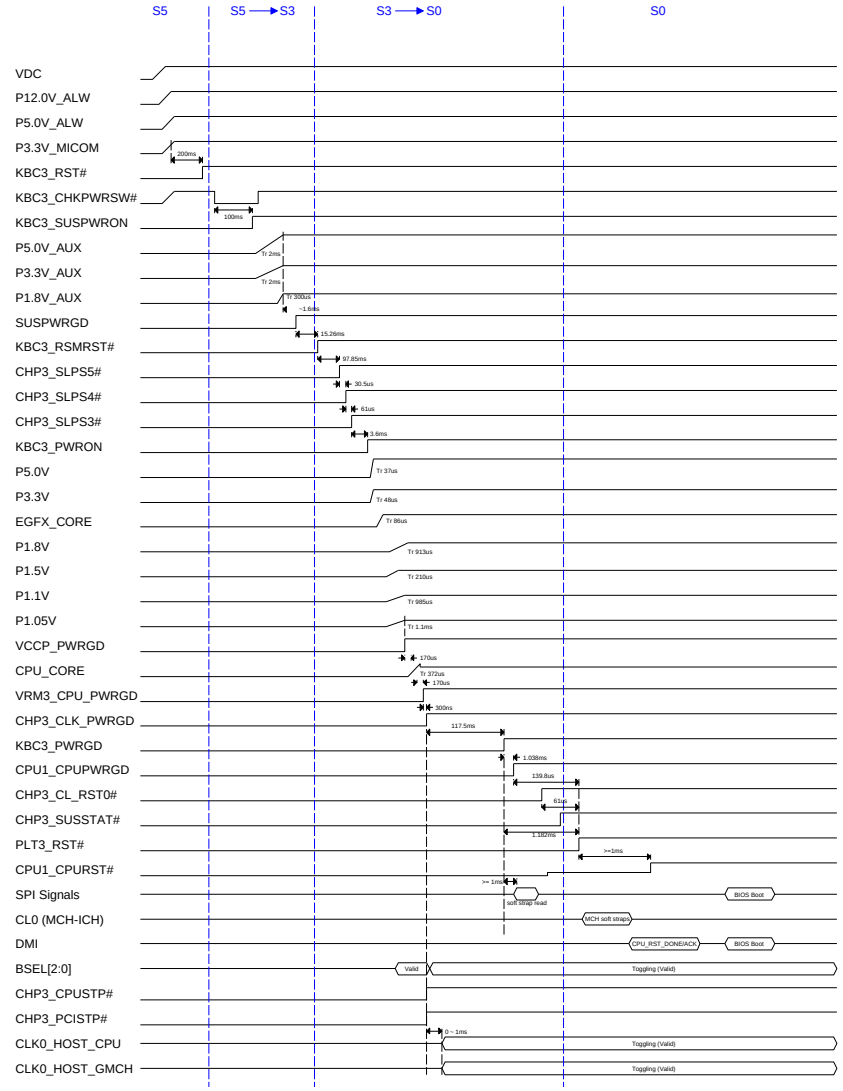
Timing Diagram, Power ON

Rev. 0.1 Phil 2008-04-15



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APPROVAL: YB CHUN	REV: 1.00		
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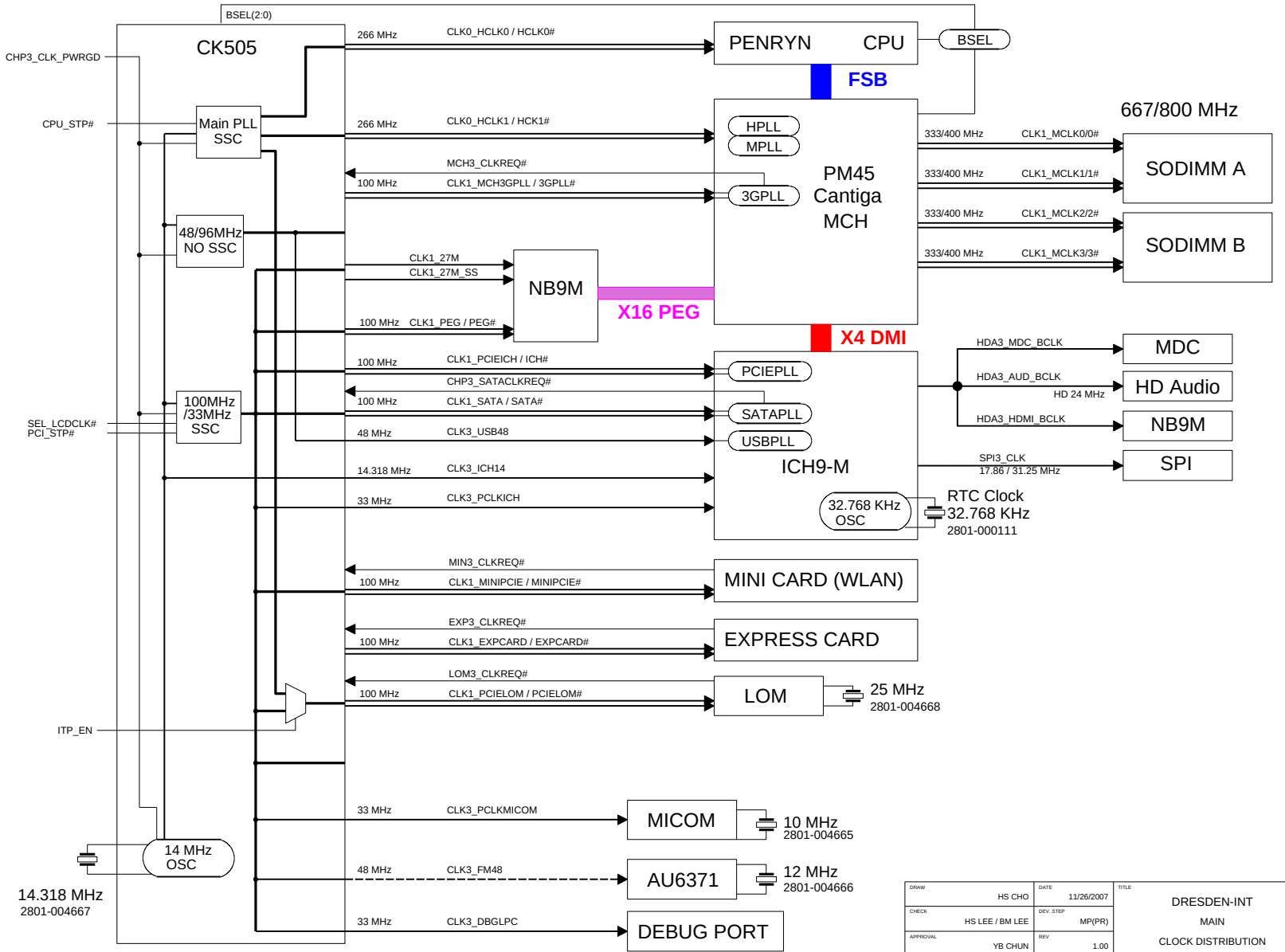
CLOCK DISTRIBUTION Rev. 0.1



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CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A
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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
-	-	-	-

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for Processor (1.308~1.068V)
P1.05V	Processor System Bus(PSB) Termination (1.05V) GMCH & ICH8 Core Voltage
P1.8V_AUX	1.8V power rail for DDR2 (off in S4-S5)
P0.9V	0.9V switched power rail (off in S3-S5)
P1.8V	1.8V power rail for GDDR3 (off in S3-S5)
P1.1V	1.1V power rail for GFX (off in S3-S5)
P1.5V	1.5V power rail for ICH (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
PRTC_BAT	3.0V power rail (ALWAYS ON)
P3.3V_MICOM	3.3V always on power rail for MICOM
P5.0V_ALW	5V power rail (Always On)
P12.0V_ALW	12V power rail (Always On)

I²C / SMB Address

Devices	Address	Hex	Bus
ICH	Master	-	SMBUS Master
SODIMM0	1010 000X	A0h	-
SODIMM1	1010 010X	A4h	-
CK-505 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
MICOM	Master	-	SMBUS Master
BATTERY	0001 011X	16h	-
EMC2102(Thermal Sensor)	0111 101X	7Ah	Thermal Sensor

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1	SYSTEM PORT B
4	EXPRESS CARD
5	BLUETOOTH
6	SYSTEM PORT C
8	CAMERA
9	MINIPCI-E (WLAN)
10	MEMORY CARD

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other criticial subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH	Real Time Clock
Crystal	10MHz	MICOM	H8S/2110BV
Crystal	14.318MHz	CLOCK-GENERATOR	ICS951461
Crystal	12MHz	MEMORY CARD	MEMORY CARD
Crystal	25MHz	LAN	LAN

CPU Core Voltage Table IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 **1** **1**	1.4125 V	0 1 0 1 1 **1** **1**	0.9125 V	1 0 1 1 0 **0** 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 **1** 0 1 **1** **1**	1.2125 V	0 1 **1** 1 1 **1** **1**	0.7125 V	1 1 **0** 1 0 0 **0**	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 **1** 0 0 **1** **1** 1	1.0125 V	1 **0** 0 1 **1** **1** 1	0.5125 V	1 **1** 1 1 0 **0** 0	0.0000 V
		1 **0** 1 0 **0** **0** 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active
DPRSLPVR 0
DPRSTP* 1
PSI2* 0 or 1

Deeper Slp
DPRSLPVR 1
DPRSTP* 0
PSI2* 0 or 1

*"1111111" : 0V power good asserted.

DRAW: HS CHO	DATE: 11/26/2007	TITLE: DRESDEN-INT / MAIN / BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
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CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A
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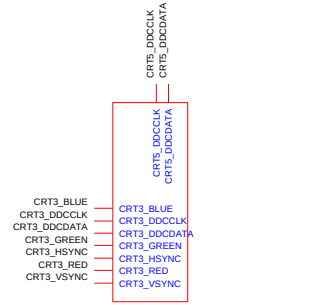
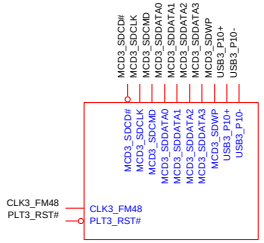
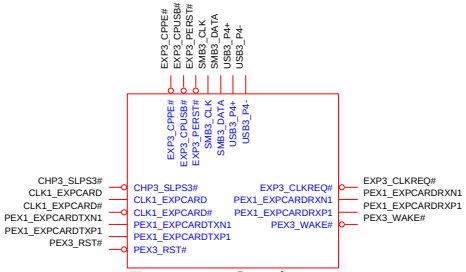


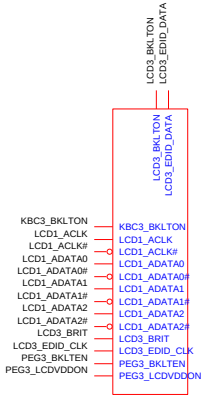
Graphics_IF_CRT



Multi_MV_Au6371



Express_Card



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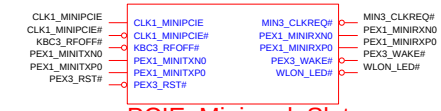
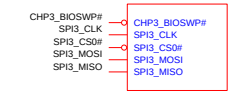


PCIE_Minicard_Slot



SPI_BIOS_ROM_16Mbit

DRAW: HS CHO	DATE: 11/26/2007	TITLE: DRESDEN-INT / MAIN / BLOCKS (2/2)	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A
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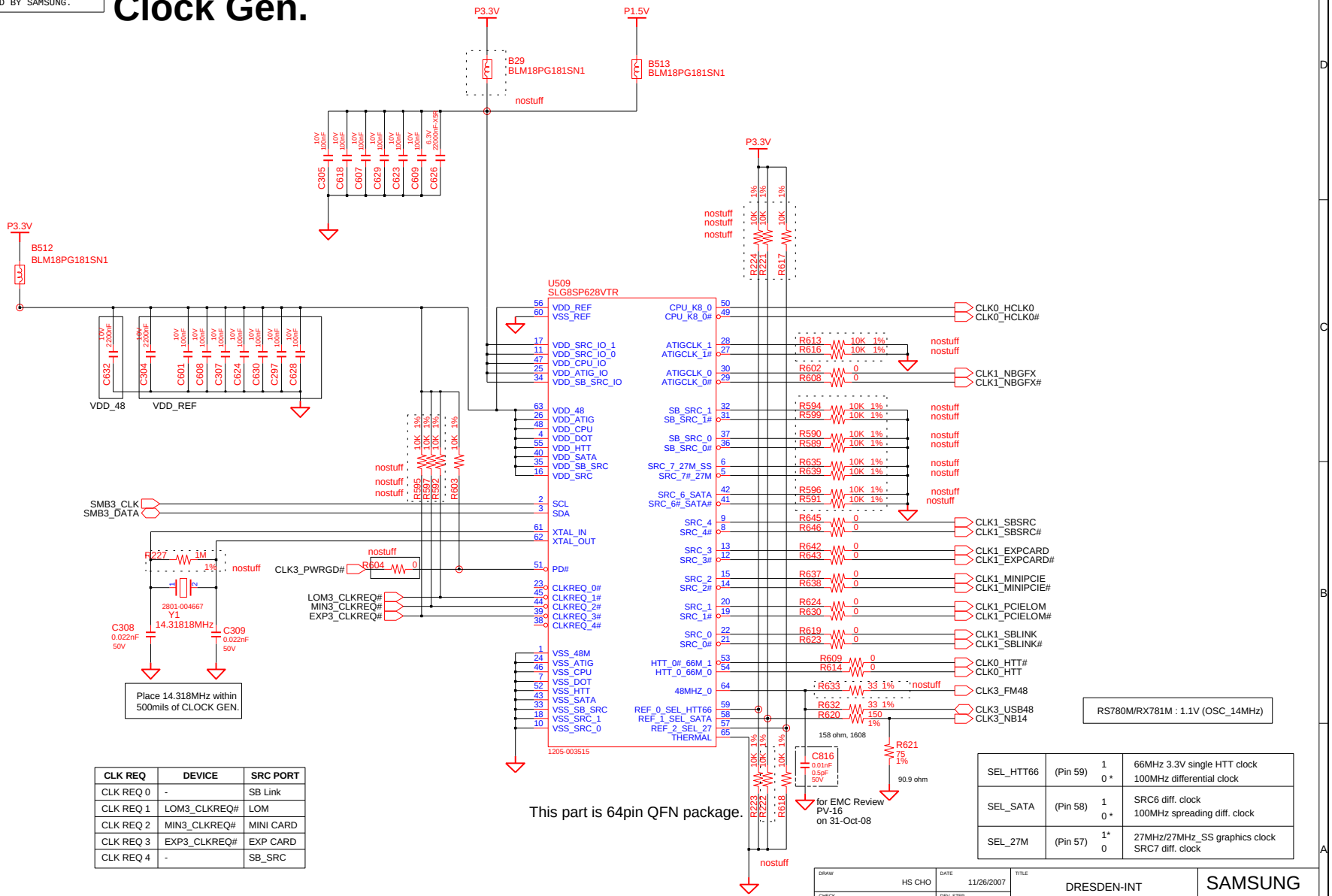
Clock Gen.



This part is 64pin QFN package.

CLK REQ	DEVICE	SRC PORT
CLK REQ 0	-	SB Link
CLK REQ 1	LOM3_CLKREQ#	LOM
CLK REQ 2	MIN3_CLKREQ#	MINI CARD
CLK REQ 3	EXP3_CLKREQ#	EXP CARD
CLK REQ 4	-	SB_SRC

RS780M/RX781M : 1.1V (OSC_14MHz)

SEL_HTT66	(Pin 59)	1	66MHz 3.3V single HTT clock
		0 *	100MHz differential clock
SEL_SATA	(Pin 58)	1	SRC6 diff. clock
		0 *	100MHz spreading diff. clock
SEL_27M	(Pin 57)	1*	27MHz/27MHz_SS graphics clock
		0	SRC7 diff. clock

DRAW	HS CHO	DATE	11/26/2007
CHECK	HS LEE / BM LEE	DEV. STEP	MP(PR)
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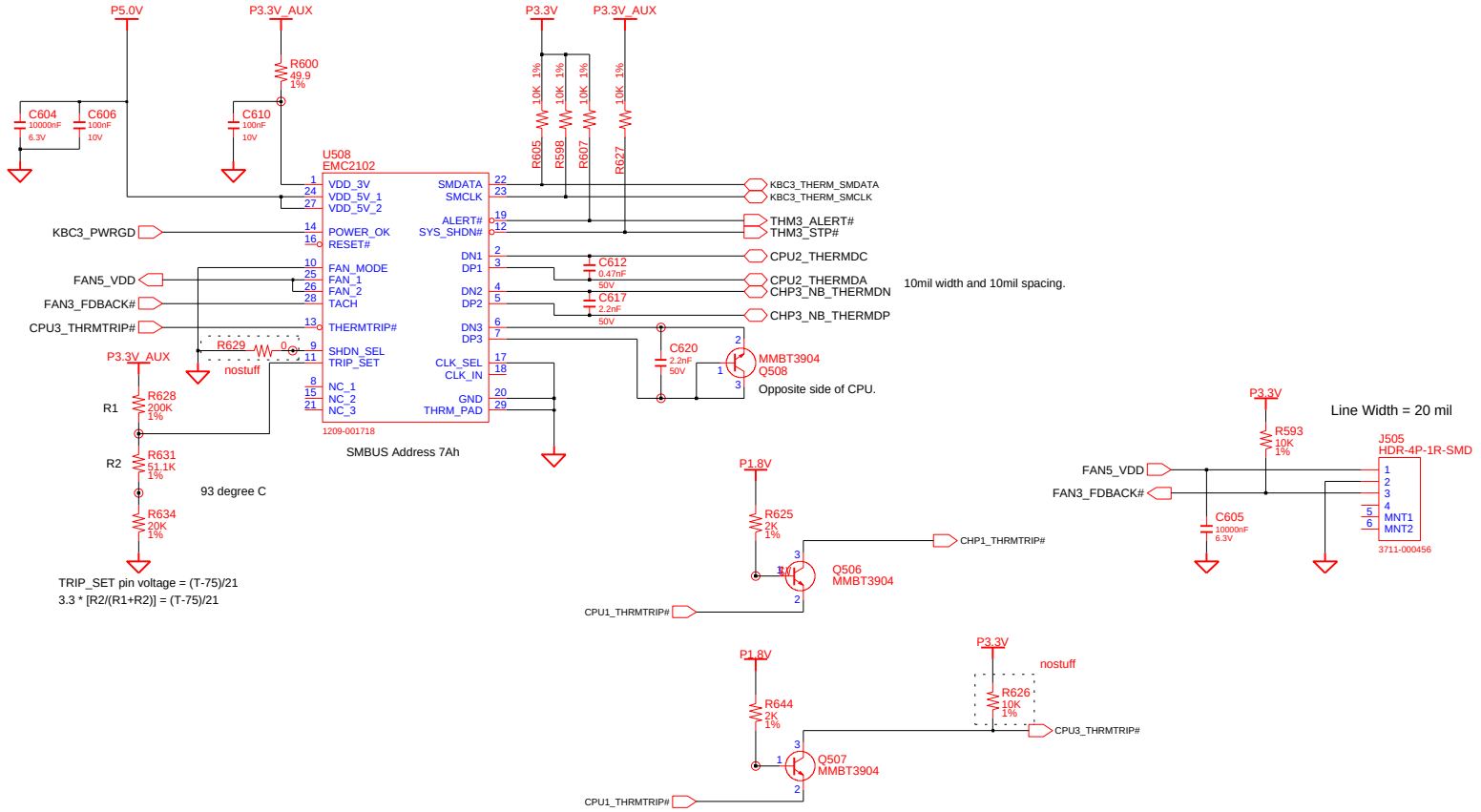
TITLE: DRESDEN-INT / MAIN / CLOCK GEN

SAMSUNG ELECTRONICS

PART NO. BA41-01024~6A

THERMAL SENSOR & FAN CONTROL



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CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A
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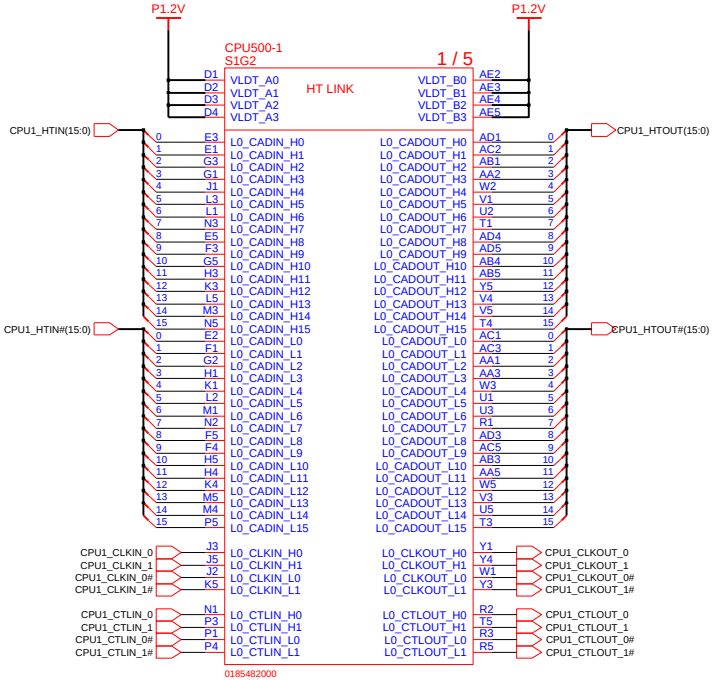
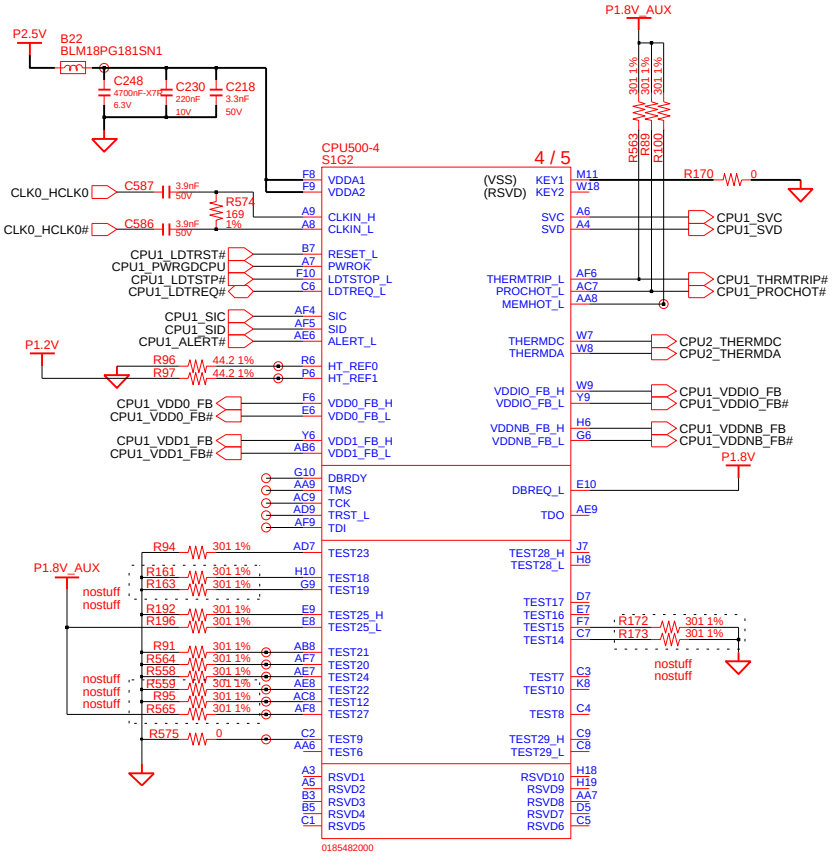
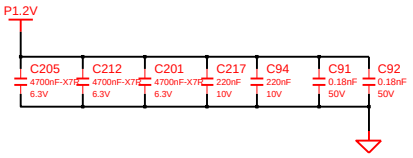
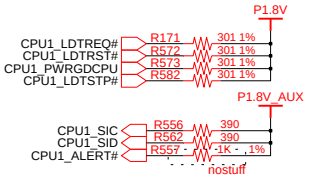
S1g2 CPU (1/3)



CPU Socket : 0185482000 (3704-001228)







DRAW: HS CHO	DATE: 11/26/2007	TITLE: DRESDEN-INT / MAIN / S1G2 CPU 1/3	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A
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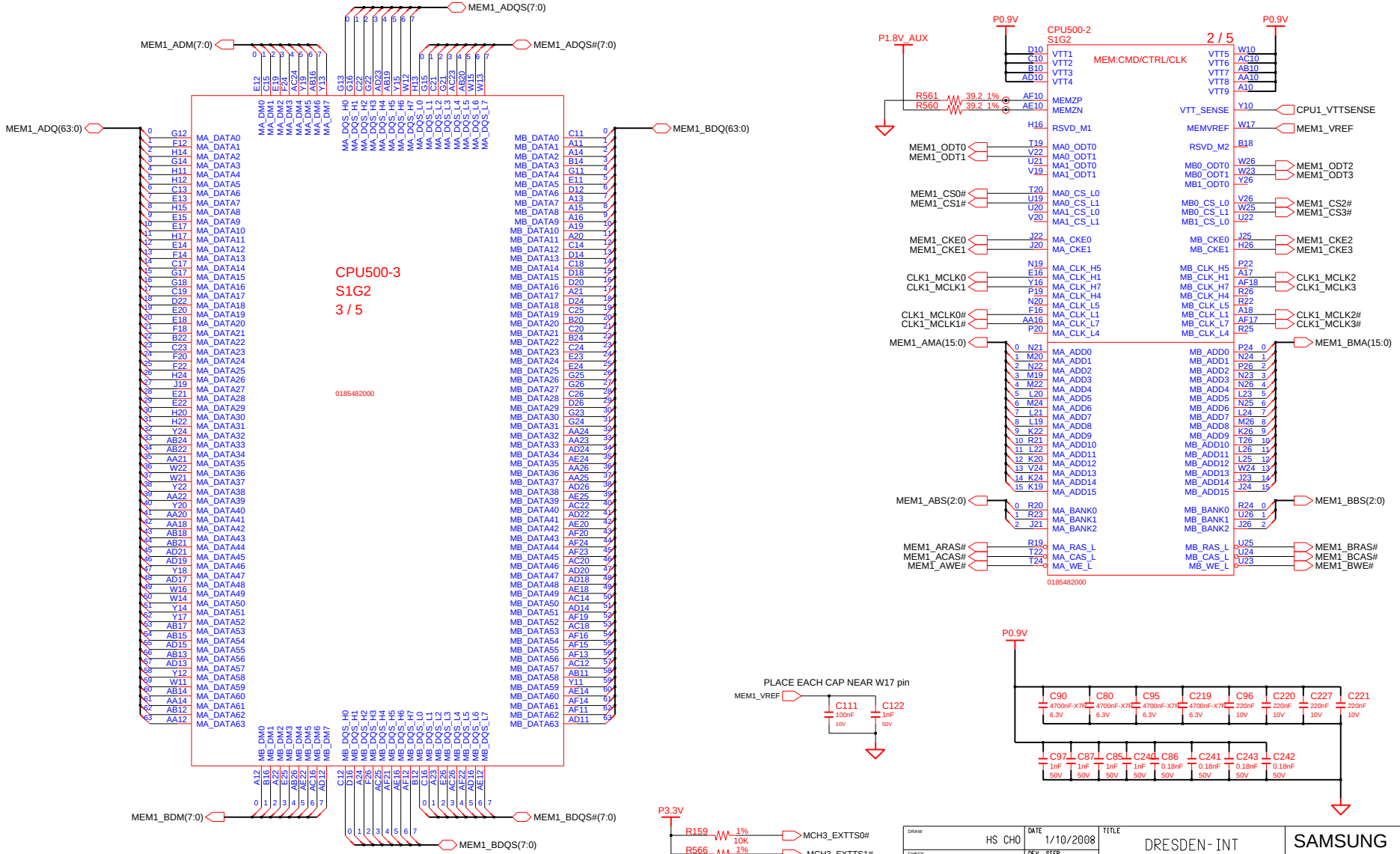
S1g2 CPU (2/3)



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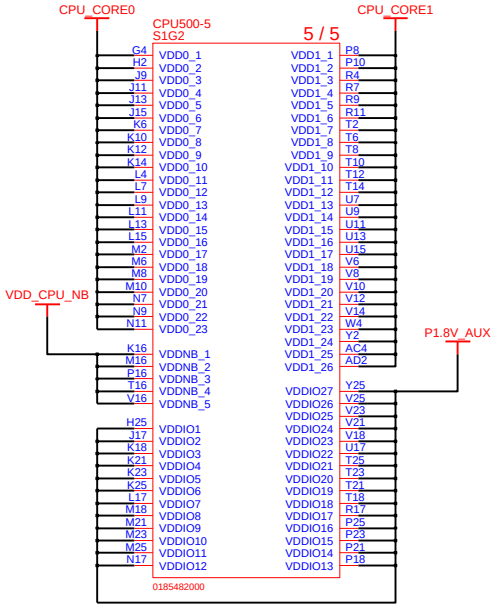
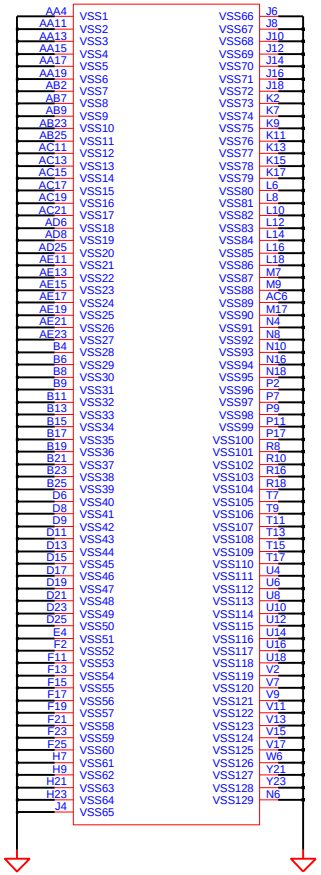
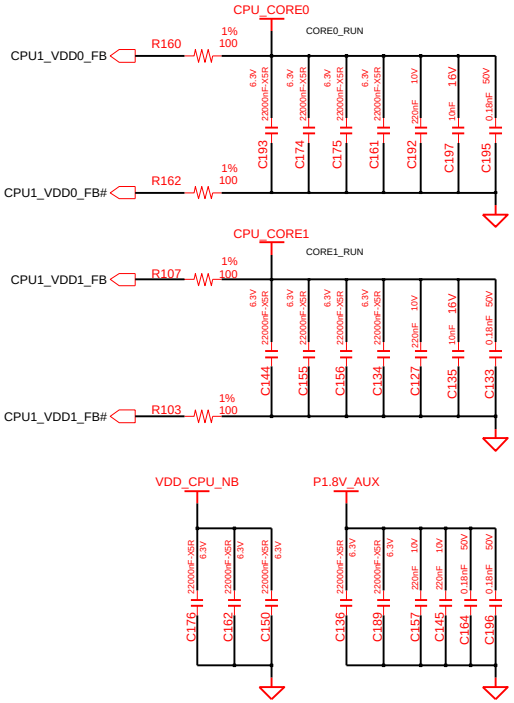
S1g2 CPU (3/3)



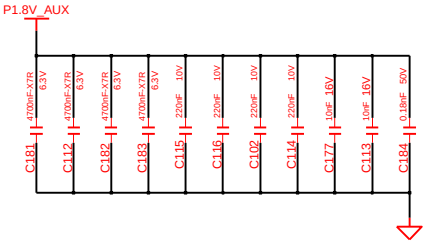
CPU Socket : 0185482000



Bottom side decoupling

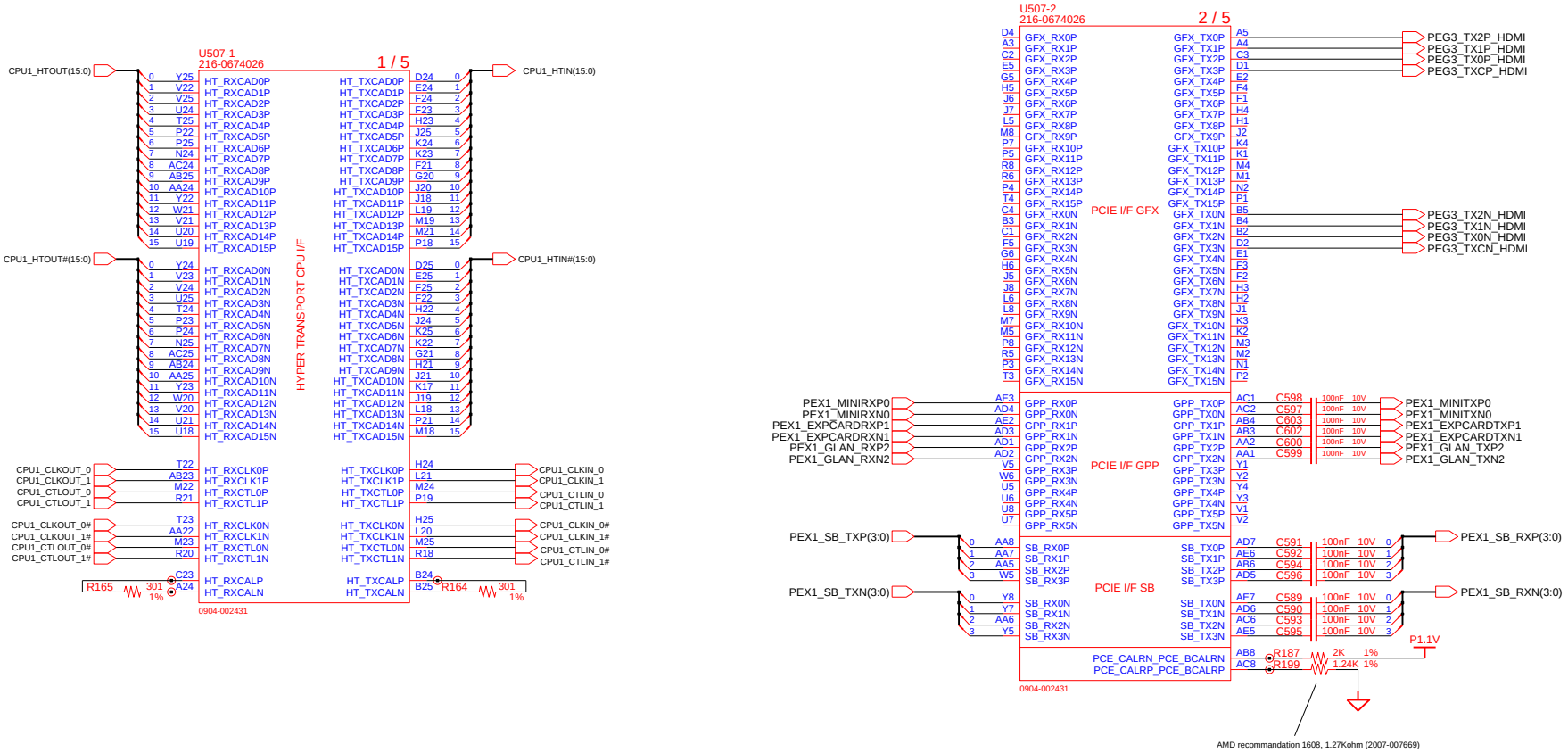


Decoupling between processor and Memory
Place close to processor as possible



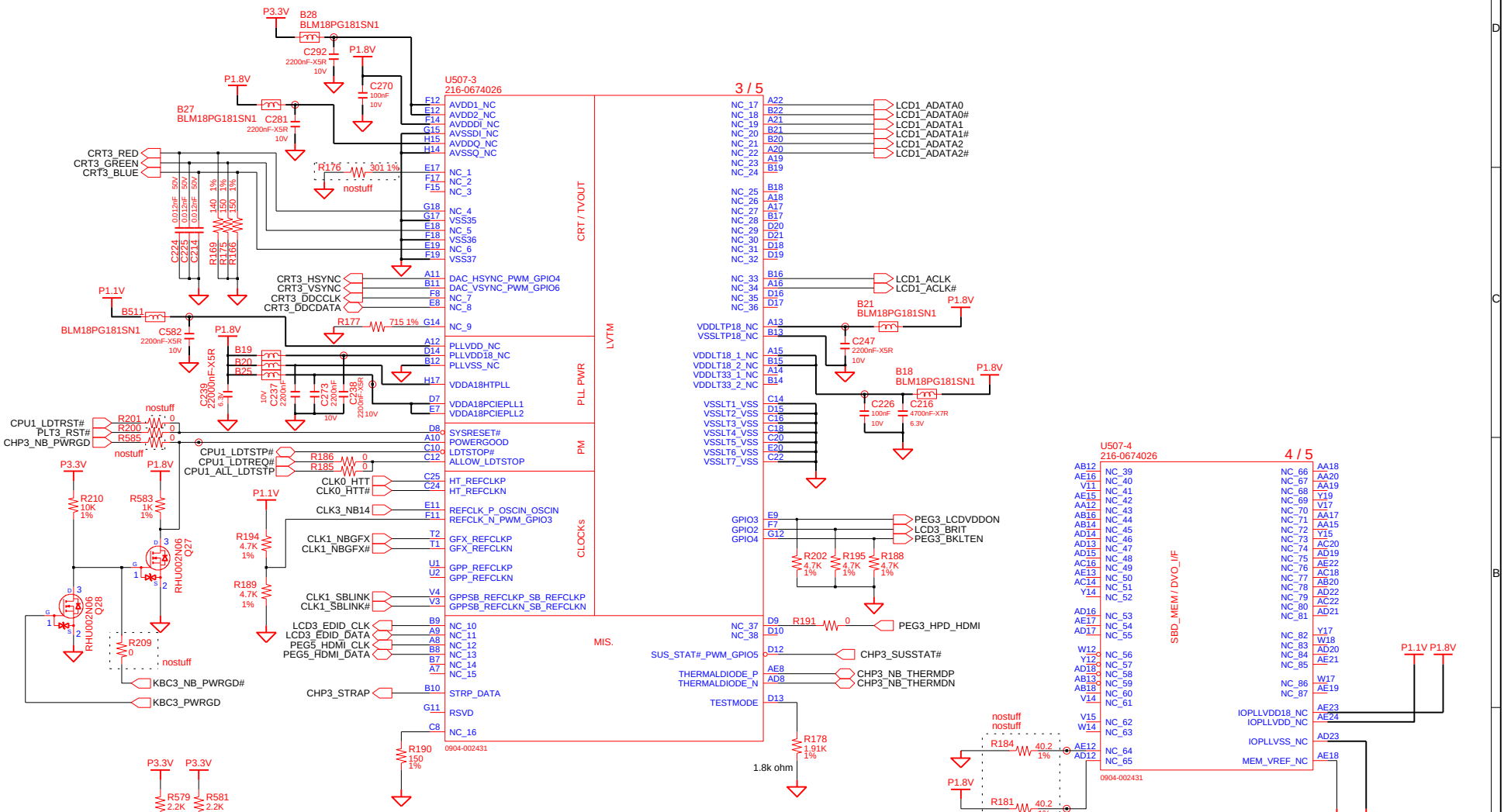
DRAW: HS CHO	DATE: 11/26/2007	TITLE: DRESDEN-INT / MAIN / S1G2 CPU 3/3	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024~6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 14 OF 49	

RS780MN(1/3)



DRAW: HS CHO	DATE: 11/26/2007	TITLE: DRESDEN-INT / MAIN / RS780MN 1/3	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024~6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 15 OF 49	

RS780MN(2/3)

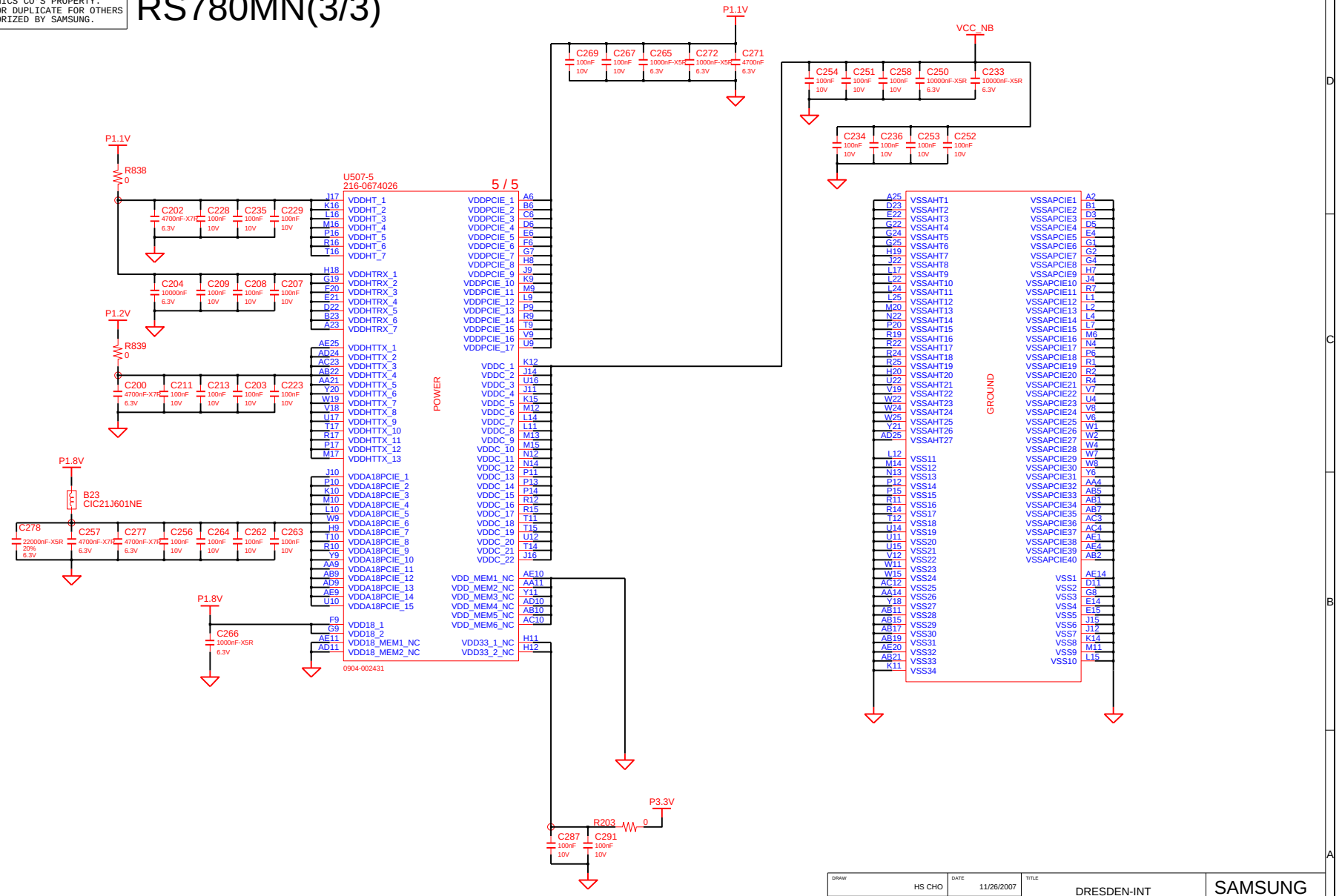


CRT3_HSYNC (Side Port Memory Option)
High : Not Available *
Low : Available

CRT3_VSYNC (Debug Bus Access)
High : Disable *
Low : Enable

DRAW: HS CHO	DATE: 11/26/2007	TITLE: DRESDEN-INT / MAIN / RS780MN 2/3	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024~6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 16 OF 49	

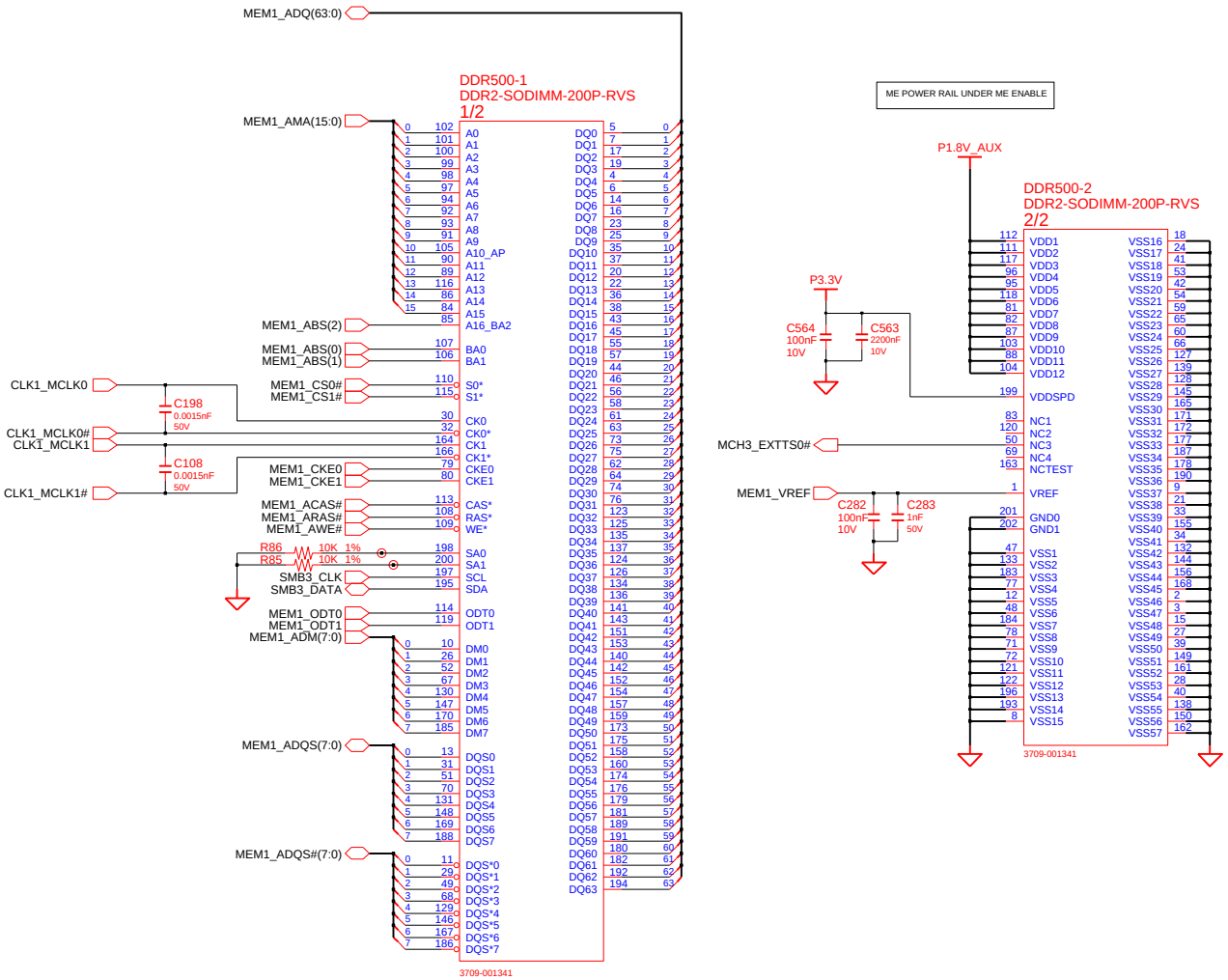
RS780MN(3/3)



DRAW: HS CHO	DATE: 11/26/2007	TITLE: DRESDEN-INT MAIN RS780MN 3/3	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 17 OF 49	

DDR SO-DIMM #0

Height : 5.2mm (Reverse)

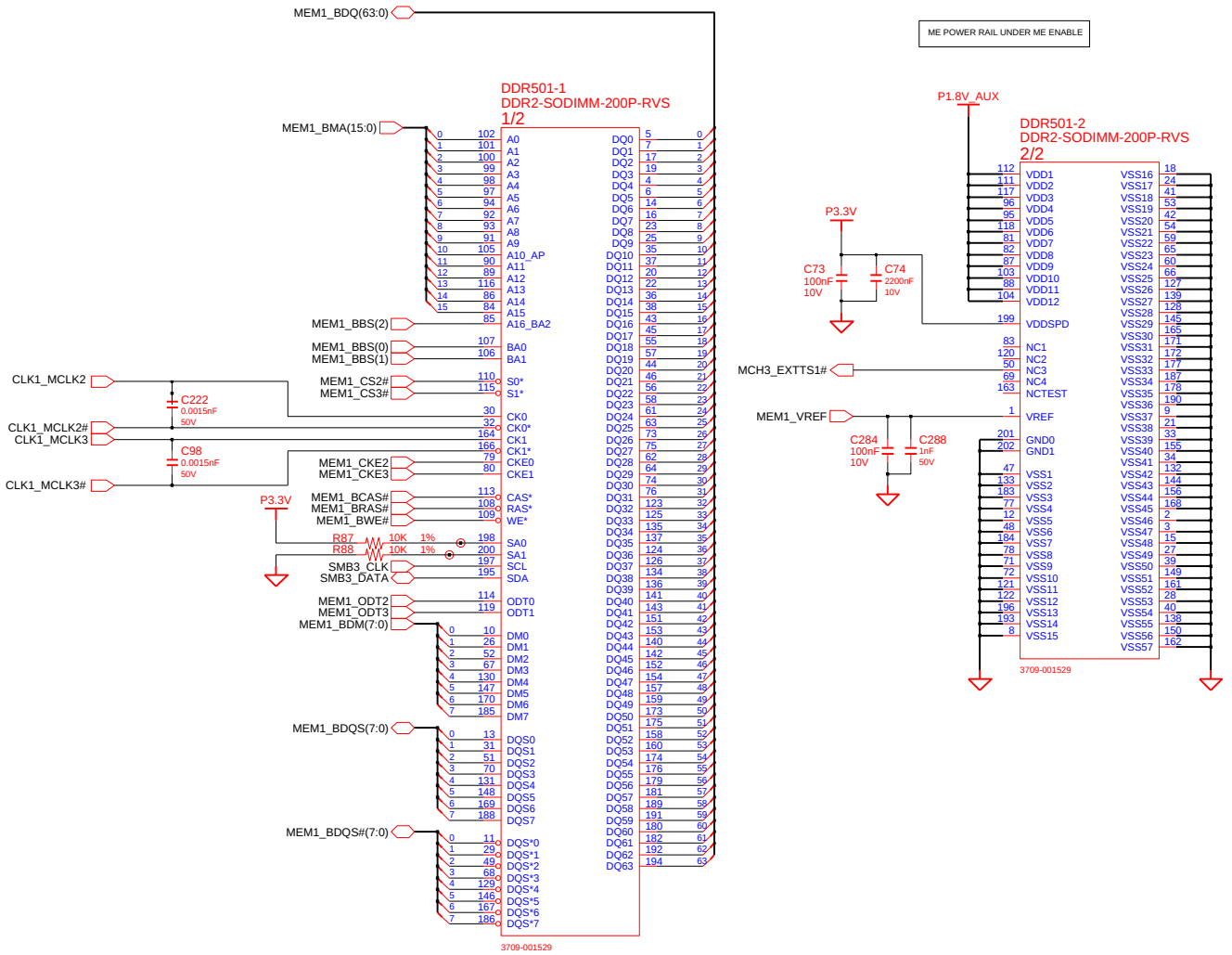


Tyco/Foxcn : 3709-001341
Suyin : 3709-001502

DESIGN: HS CHO	DATE: 9/1/2008	TITLE: DRESDEN-INT MAIN SODIMM DDR2	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 18 OF 49	

DDR SO-DIMM #1

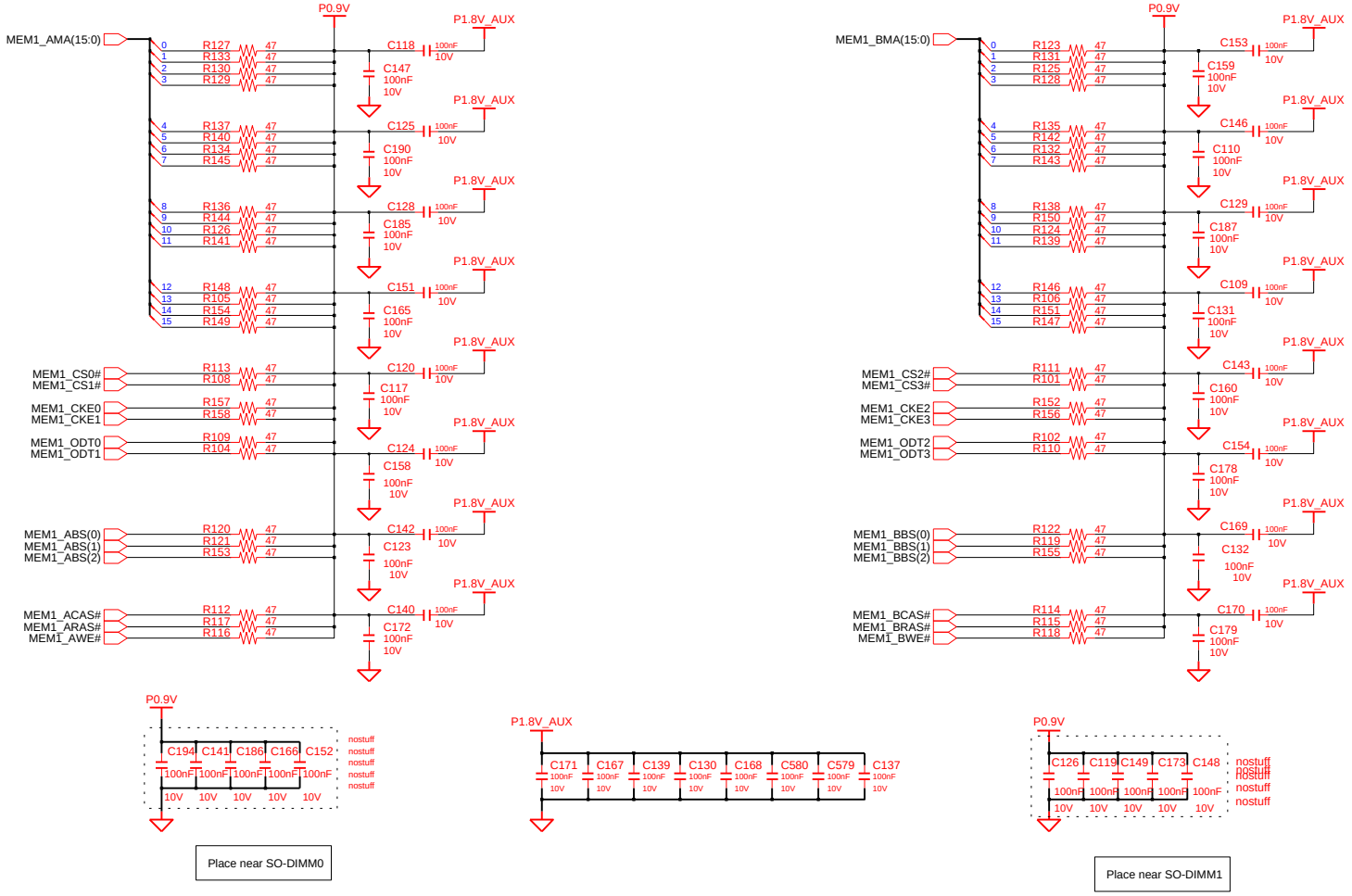
Height : 9.2mm (Reverse)



Foxcn : 3709-001390
Suyin : 3709-001503

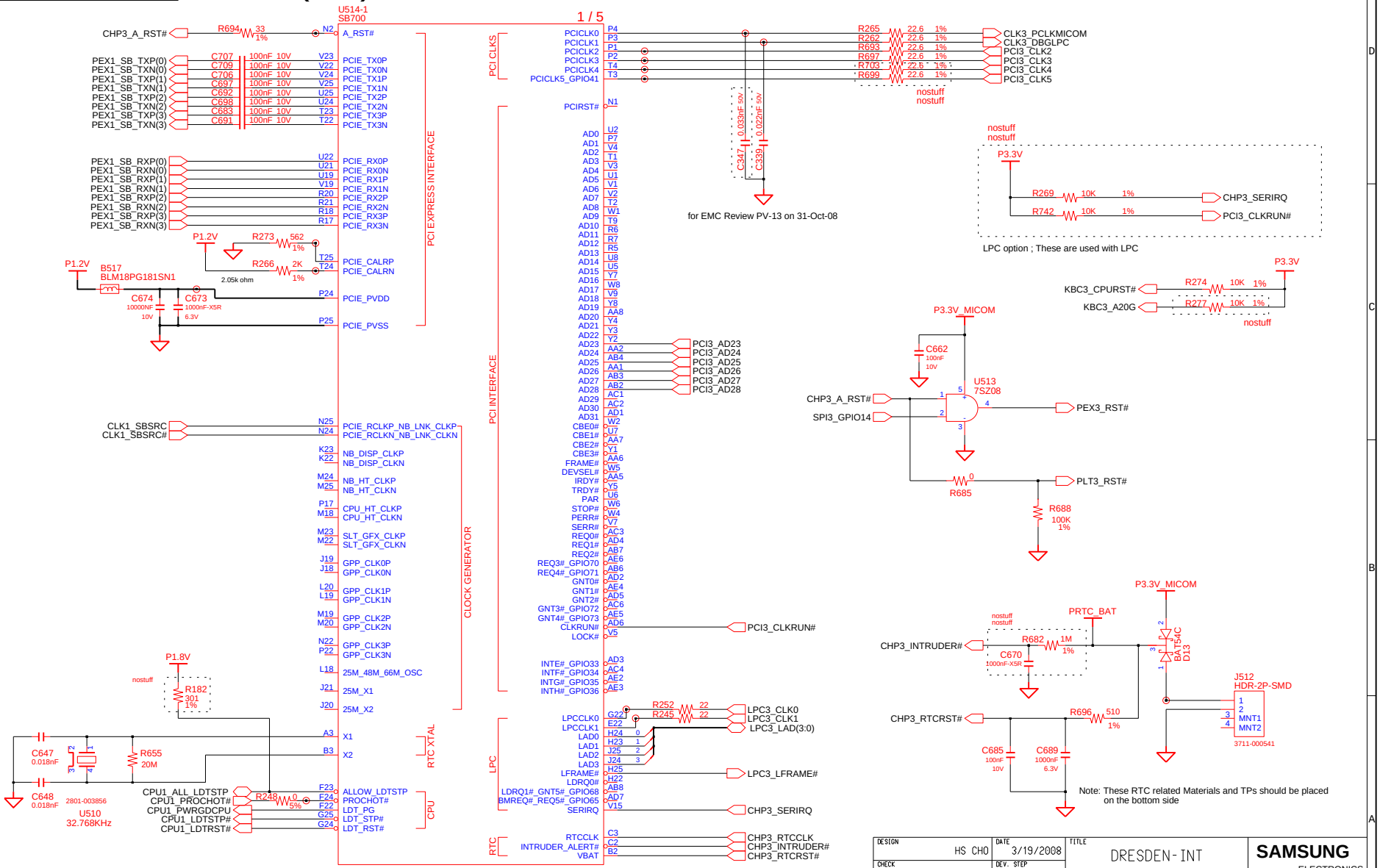
DESIGN: HS CHO	DATE: 9/1/2008	TITLE: DRESDEN-INT MAIN SODIMM DDR2	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO. BA41-01024*6A
MODULE CODE	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 19 OF 49	

SODIMM TERMINATION



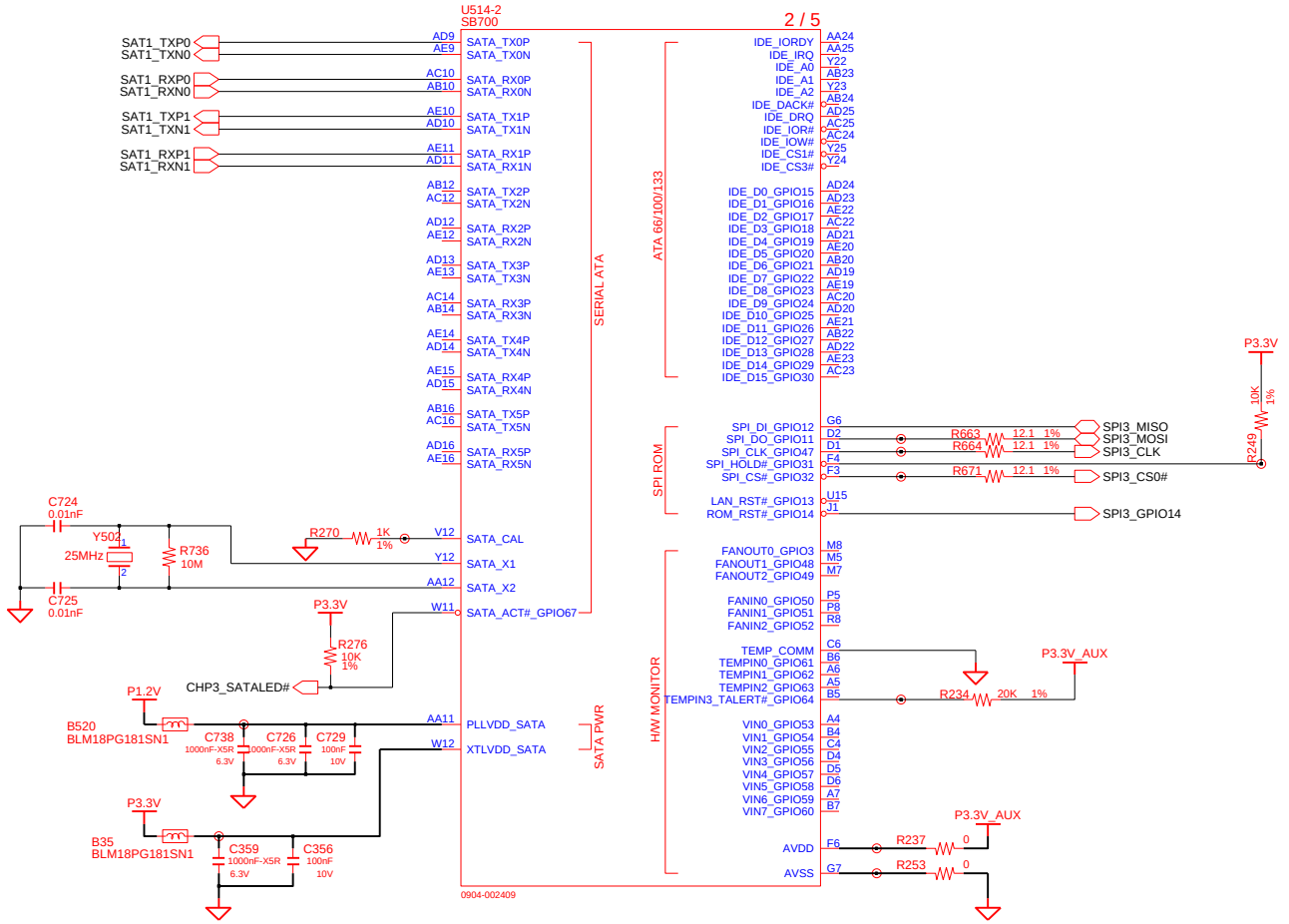
DRAW: HS CHO	DATE: 5/28/2007	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	SODIMM TERMINATION	PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 20 OF 49	

SB700(1/4)



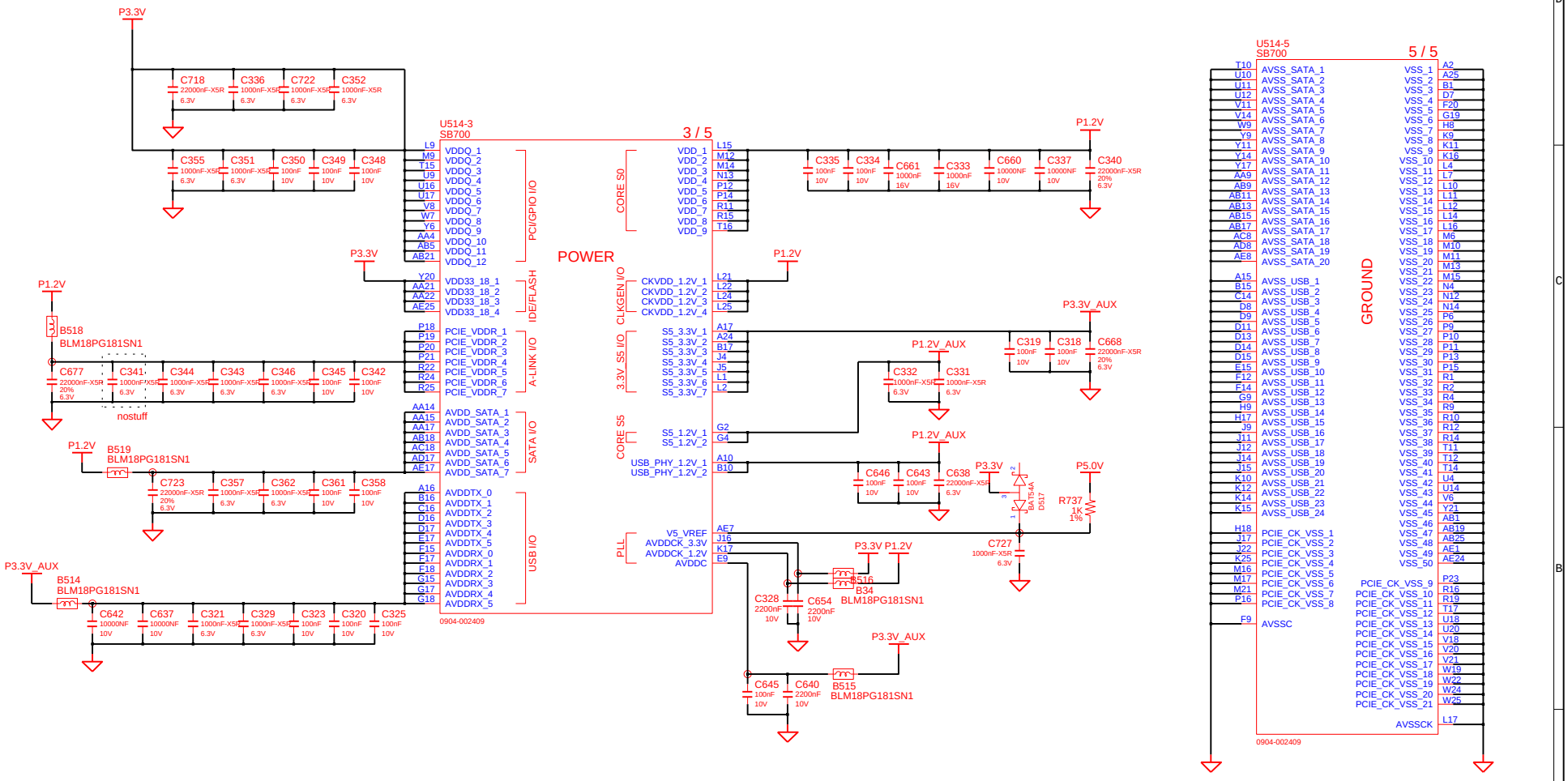
DESIGN: HS CHO	DATE: 3/19/2008	TITLE: DRESDEN-INT MAIN SB700 1/4	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 21 OF 49	

SB700(2/4)



DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT MAIN SB700 2/4	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 22 OF 49	

SB700(3/4)

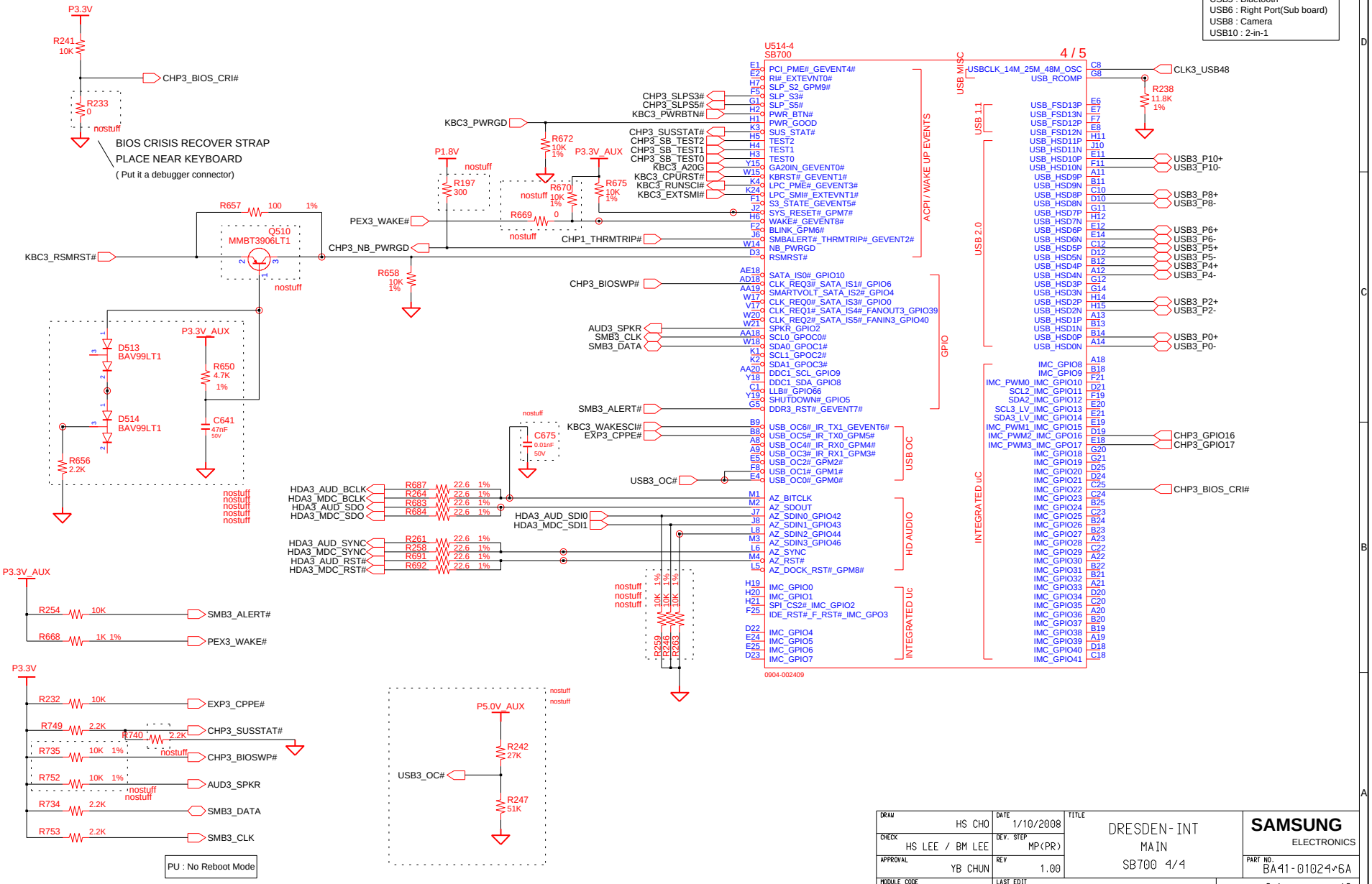


DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT MAIN SB700 3/4	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 23 OF 49	

SB700(4/4)

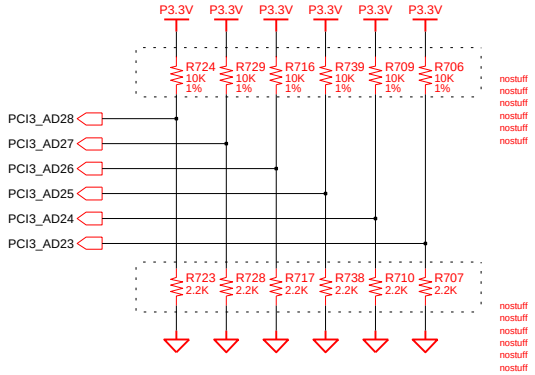
USB0 and 6 ports should be connected with external ports

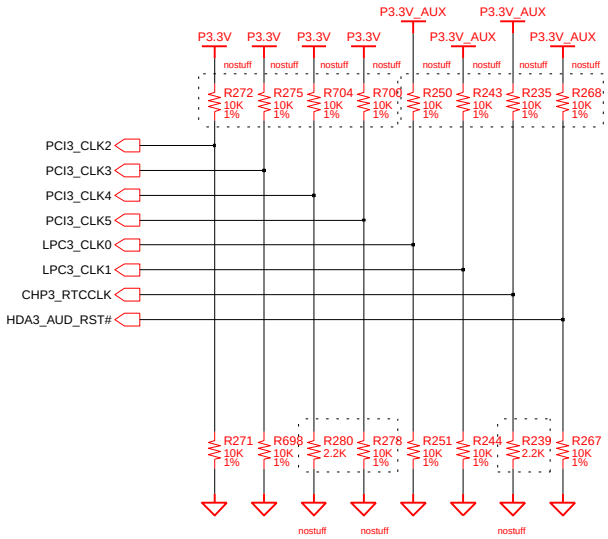
- USB0, 2 : Rear Port(Sub board)
- USB4 : Express USB
- USB5 : Bluetooth
- USB6 : Right Port(Sub board)
- USB8 : Camera
- USB10 : 2-in-1



DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT MAIN SB700 4/4	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 24 OF 49	

SB700 HW STRAP

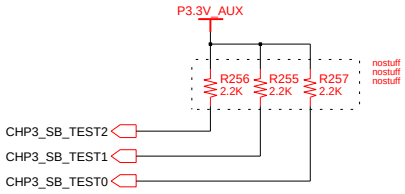


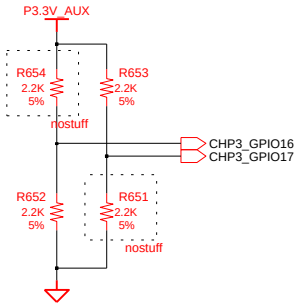


DEBUG STRAPS

	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	LPC3_CLK0	LPC3_CLK1	RTC_CLK	AUD_RST#
STRAP HIGH	BOOTFAIL TIMER ENABLED	USER DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC	ENABLE PCI MEM BOOT
STRAP LOW	BOOTFAIL TIMER DISABLED	IGNORE DEBUG STRAPS	RESERVED	RESERVED	EC DISABLED	CLKGEN DISABLED	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT



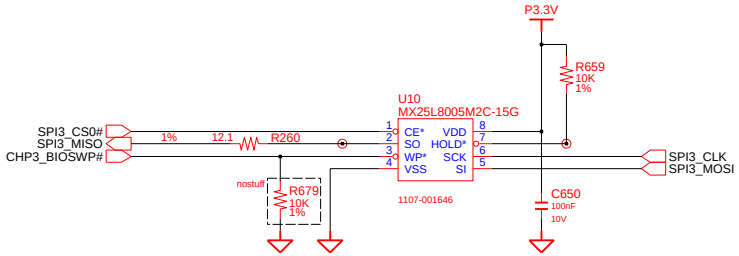


GPIO17	GPIO16

ROM TYPE
H, H = PCI ROM
H, L = SPI ROM
L, H = LPC ROM
L, L = FWH ROM

DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	SB700 HW STRAP	PART NO.: BA41-01024A-6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 25 OF 49	

BIOS ROM

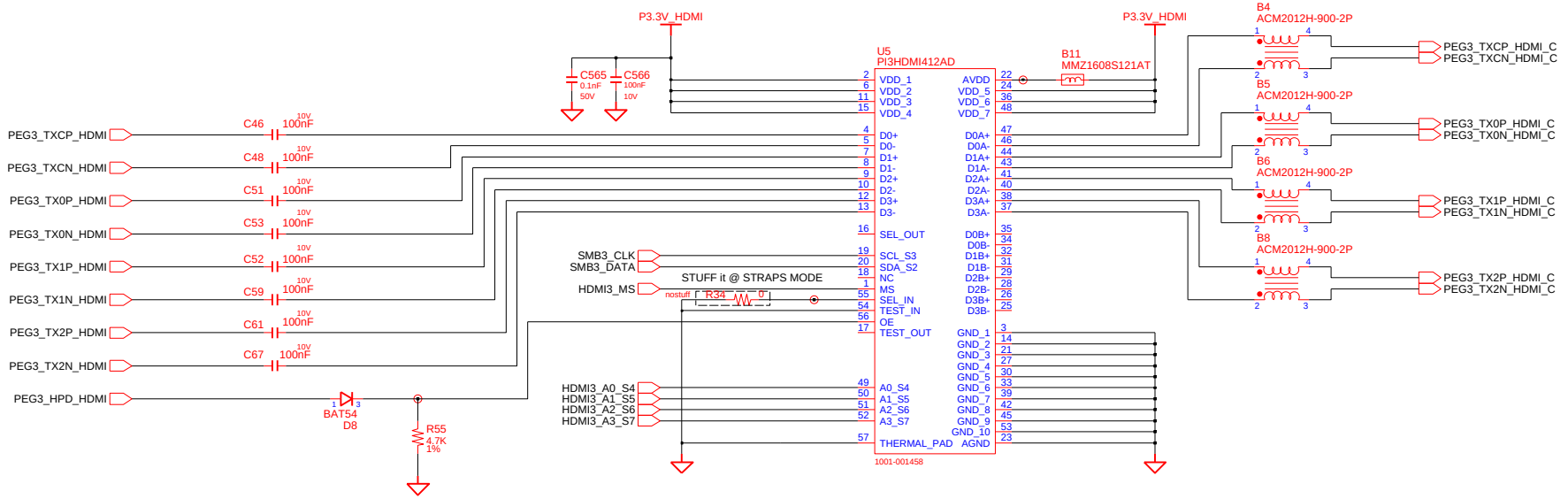


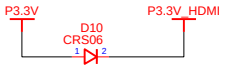
1MByte (8Mbit)

02	VERIFY REAL MODE
03	DISABLE NMI
04	GET CPU TYPE
06	INIT. SYSTEM H/W
08	INIT. CHIPSET REG.
09	SET IN POST FLAG
0A	INIT CPU.REG
0B	CPU CACHE ON
0C	INIT.CACHE TO POST
OE	INIT. I/O VALUE
0F	ENABLE THE L-BUS IDE
10	INIT. POWER MANAGER
11	LOAD ALTERNATE REG.
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE
14	INIT. KEYBOARD CONTROLLER
16	CHECK CHECKSUM
18	8254 TIMER INIT.
1A	8237 DMA CONTROLLER INIT.
1C	RESET INTERRUP CONTROLLER
20	TEST DRAM REFRESH
22	TEST 8742 KEYBOARD CONTROLLER
24	SET ES SEGMENT REG. TO 4GB
26	ENABLE A20
28	AUTO SIZING DRAM
32	COMPUTE THE CPU SPEED
34	TESET CMOS RAM
38	SHADOW SYSTEM BIOS ROM
3A	AUTO SIZING CACHE
3C	CONFIGURE ADVANCED CHIPSET REG.
3D	LOAD ALTER REG. WITH CMOS VALUE
42	INIT. INTERRUPT VECTOR
44	INIT. BIOS INTERRUPT
46	CHECK ROM COPYRIGHT NOTICE
47	INIT. I20 SUPPORT IF INSTALLED
48	CHECK VIDEO CONFIGURE AGAINST CMOS
49	INIT. PCI BUS AND DEVICE
4A	INIT. ALL VIDEO BIOS ROM
4C	SHADOW VIDEO BIOS ROM
50	DISPLAY CPU TYPE AND SPEED
52	TEST KEYBOARD
54	SET KEYCLICK IF ENABLED
56	ENABLE KEYBOARD
58	TEST FOR UNEXPECTED INTERRUPTS
5A	DISPLAY " PRESS ..... SETUP"
5C	TEST RAM GETWEEN 512K AND 640K
60	TEST EXTENDED MEMORY
62	TEST EXTENDED MEMORY ADDRESS LINE
64	JUMP TO USER PATCH 1
66	CONFIGURE ADVANCE CACHE REG.
6A	DISPLAY EXTERNAL CACHE SIZE
6C	DISPLAY SHADOW MESSAGE
6E	DISPLAY NON-DISPOSABLE SEGMENT
70	DISPLAY ERROR MESSAGE
72	CHECK FOR CONFIGURATION ERROR
74	TEST REAL-TIME CLOCK
76	CHECK FOR KEYBOARD EERROR
7C	SETUP HARDWARE INTERRUPT VECTOR
7E	TEST COPROCESSER IF PRESENT
80	DISABLE ON-BOARD I/O PORT
82	DETECT AND INSTALL EXT.RS232C
84	DETECT AND INSTALL EXT.PARALLEL
86	RE-INIT. ON-BOARD I/O PORT
88	INIT. BIOS DATA ROM
8A	INIT.EXTENDED BIOS DATA AREA
8C	INIT. FDD CONTROLLER
9A	SHADOW OPTION ROMS
9C	SETUP POWER MANAGEMENT
9E	ENABLE H/W INTERRUPT
A0	SET TIME OF DAY
A4	INIT. TYPEMATIC RATE
A8	ERASE F2 PROMPT
AA	SCAN FOR F2 KEY STROKE
AC	ENTER SETUP
AE	CLEAR IN POST FLAG
B0	CHECK FOR ERRORS
B2	POST DONE-PREPARE TO BOOT O/S
B4	ONE BEEP
B6	CHECK PASSWORD (OPTION)
B7	ACPI INIT
BA	DMI INIT
BE	CLEAR SCREEN
C0	TRY BOOT WITH INT19
D0	INTERRUPT HANDLER ERROR
D2	UNKNOWN INTERRUPT ERROR
D4	PENDING INTERRUPT ERROR
D6	SHUTDOWN 5
D8	SHUTDOWN ERROR
DA	EXTENDED BLOCK MOVE
DC	SHUTDOWN 10
89	ENABLE NMI
90	INIT. HDD CONTROLLER
91	INIT. LOCAL BUS HDD CONTROLLER
92	JUMP TO USER PATCH 2
94	DISABLE A20 ADDRESS LINE
96	CLEAR HUGE ES SEGMENT REG.
98	SEARCH FOR OPTION ROMS

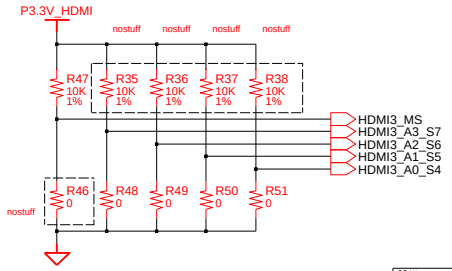
DRAW: HS CHO	DATE: 8/12/2006	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	SPI_BIOS_ROM	
APPROVAL: YB CHUN	REV: 1.00	BIOS_ROM (1M)	PART NO.: BA41-01024~6A
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 32 OF 60	

HDMI REPEATER





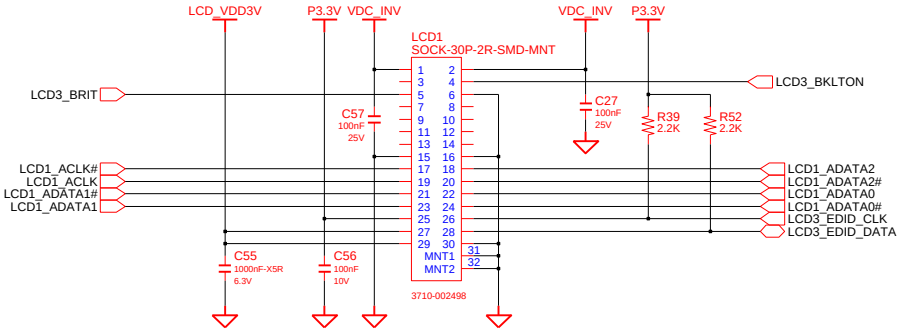
HDMI3_MS HIGH: SMBUS mode (Address = 110 A3A2A1A0 x = 1100 000x)
HDMI3_MS LOW: STRAPS mode



DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT MAIN HDMI REPEATER	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024*6A
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 26 OF 49	

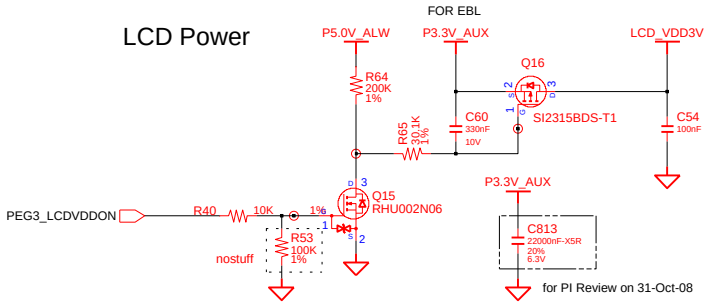
LVDS

1CH WXGA LCD CONNECTOR

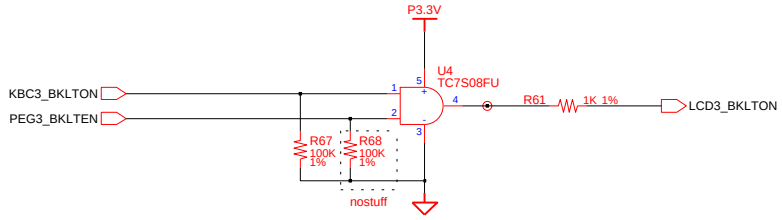


Signals : #40AWG
LCD Vdd : #36AWG
Inverter Vdd : #36AWG
GND : #36AWG

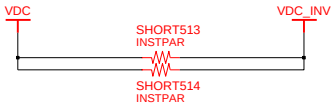
LCD Power



Backlight ON

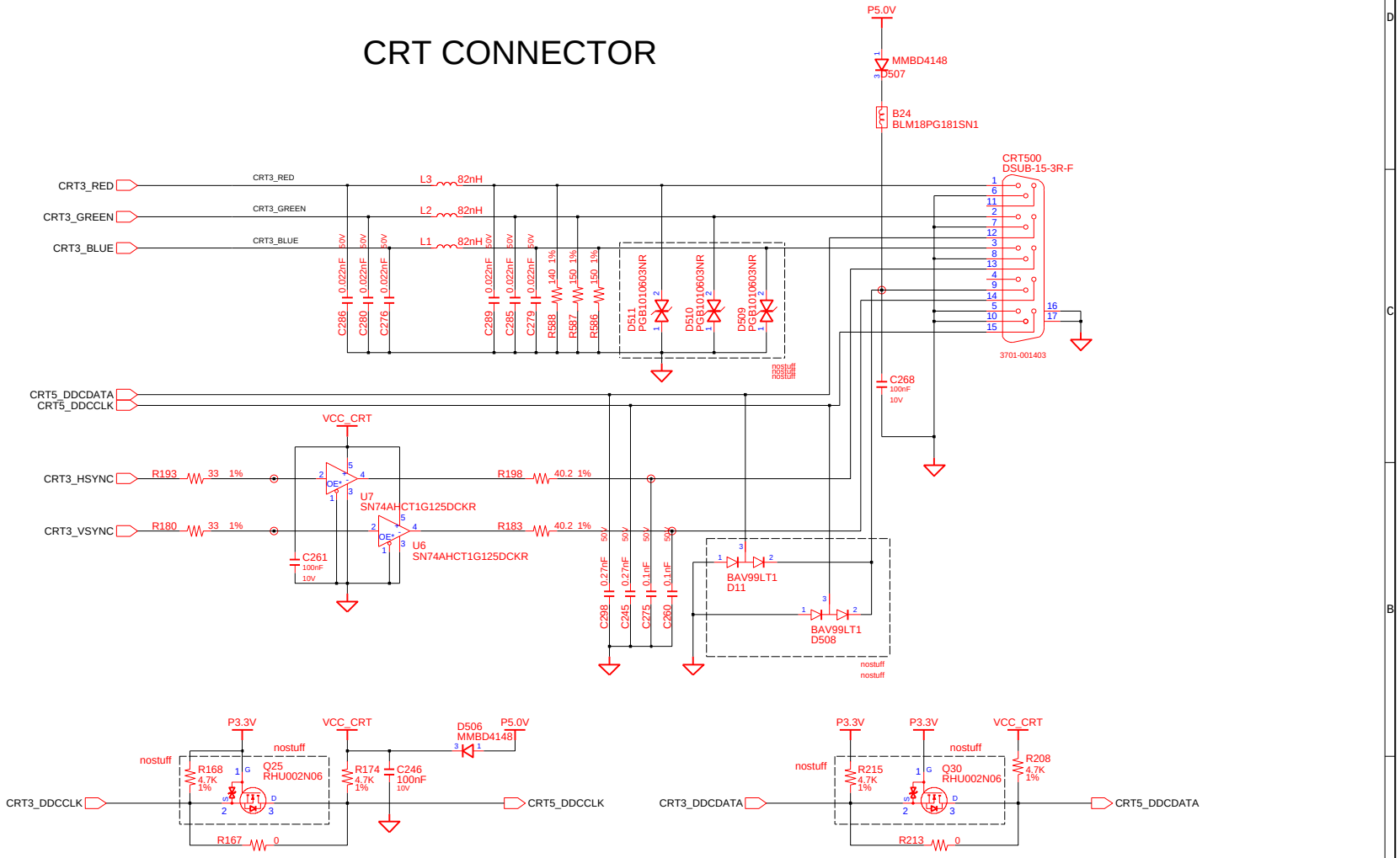


Inverter Power



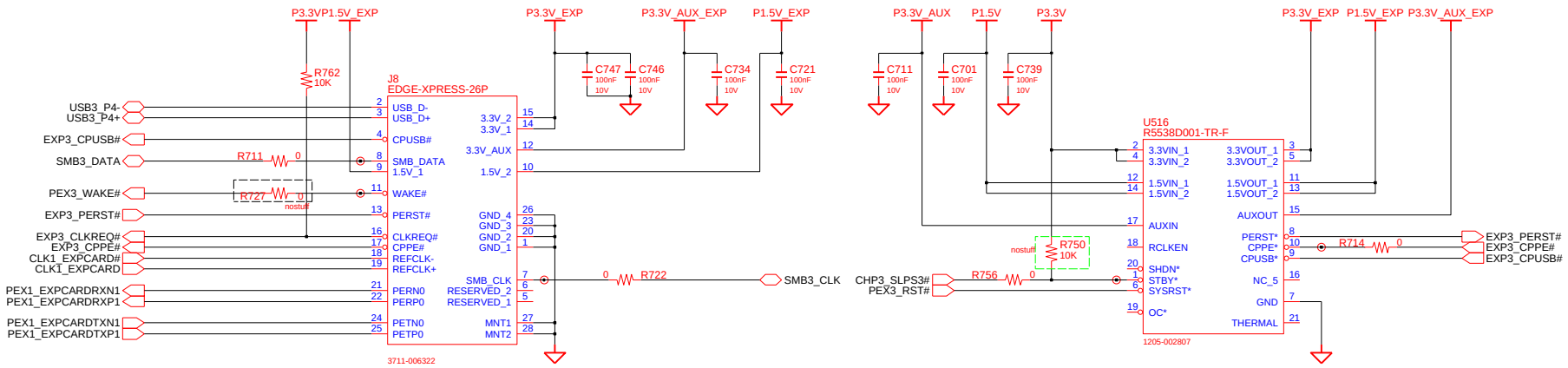
DRAW: HS CHO	DATE: 8/12/2006	TITLE: DRESDEN-INT / LCD_IF / LVDS	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 34 OF 63	

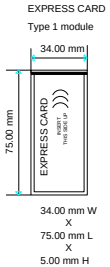
CRT CONNECTOR

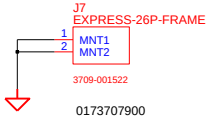


DRAW: HS CHO	DATE: 8/12/2006	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	CRT_IF	
APPROVAL: YB CHUN	REV: 1.00	CRT	PART NO.: BA41-01024~6A
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 35 OF 63	

EXPRESS CARD



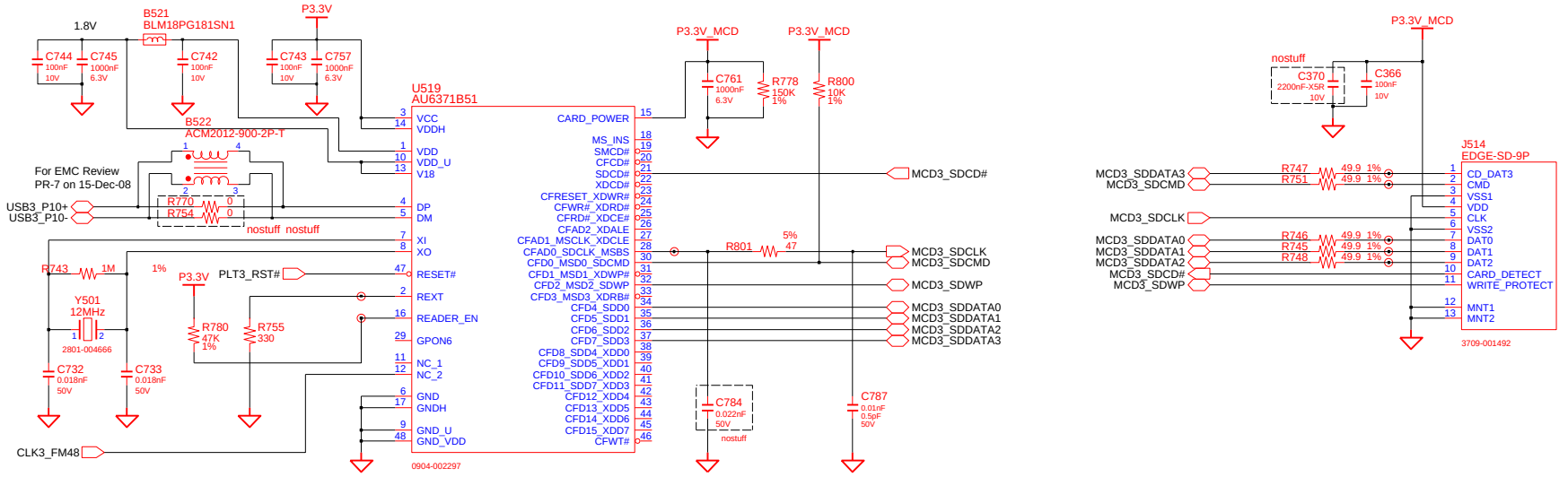




0173707900

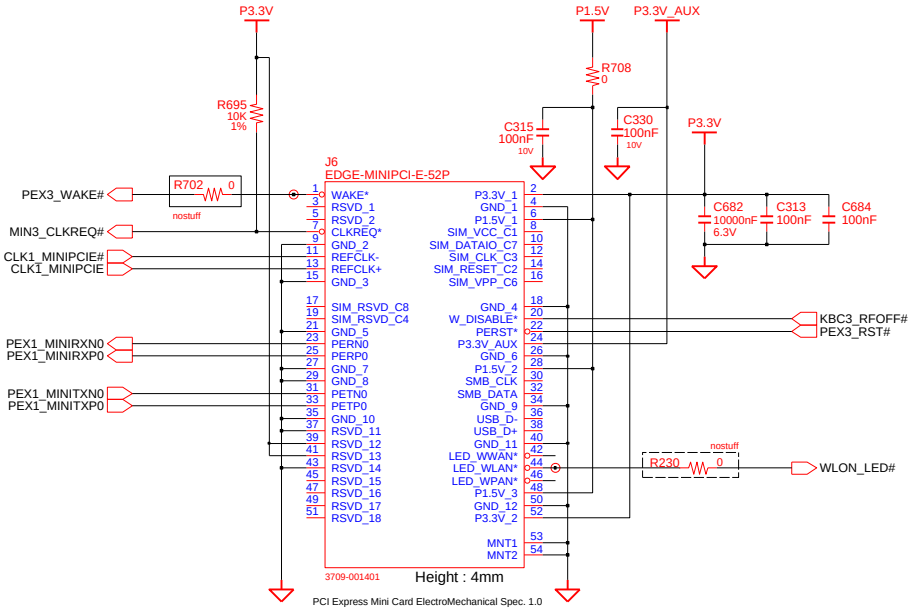
DRAW: HS CHO	DATE: 8/17/2007	TITLE: DRESDEN-INT / EXPRESS_CARD / EXPRESS_CARD (34mm)	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 42 OF 60	

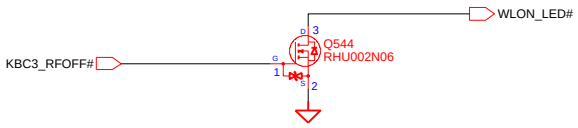
MEMORY CARD (2 IN 1)



DRAW: HS CHO	DATE: 8/17/2007	TITLE: DRESDEN-INT MEMORY CARD MMC (2-IN-1)	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024~6A
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 41 OF 60	

Mini PCI-E Card (WLAN)





WLAN MINICARD NUT
Height : 4mm

For Full size minicard

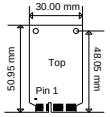
(Top)

WLAN MINICARD NUT
Height : 4mm

For half size minicard

(Top)

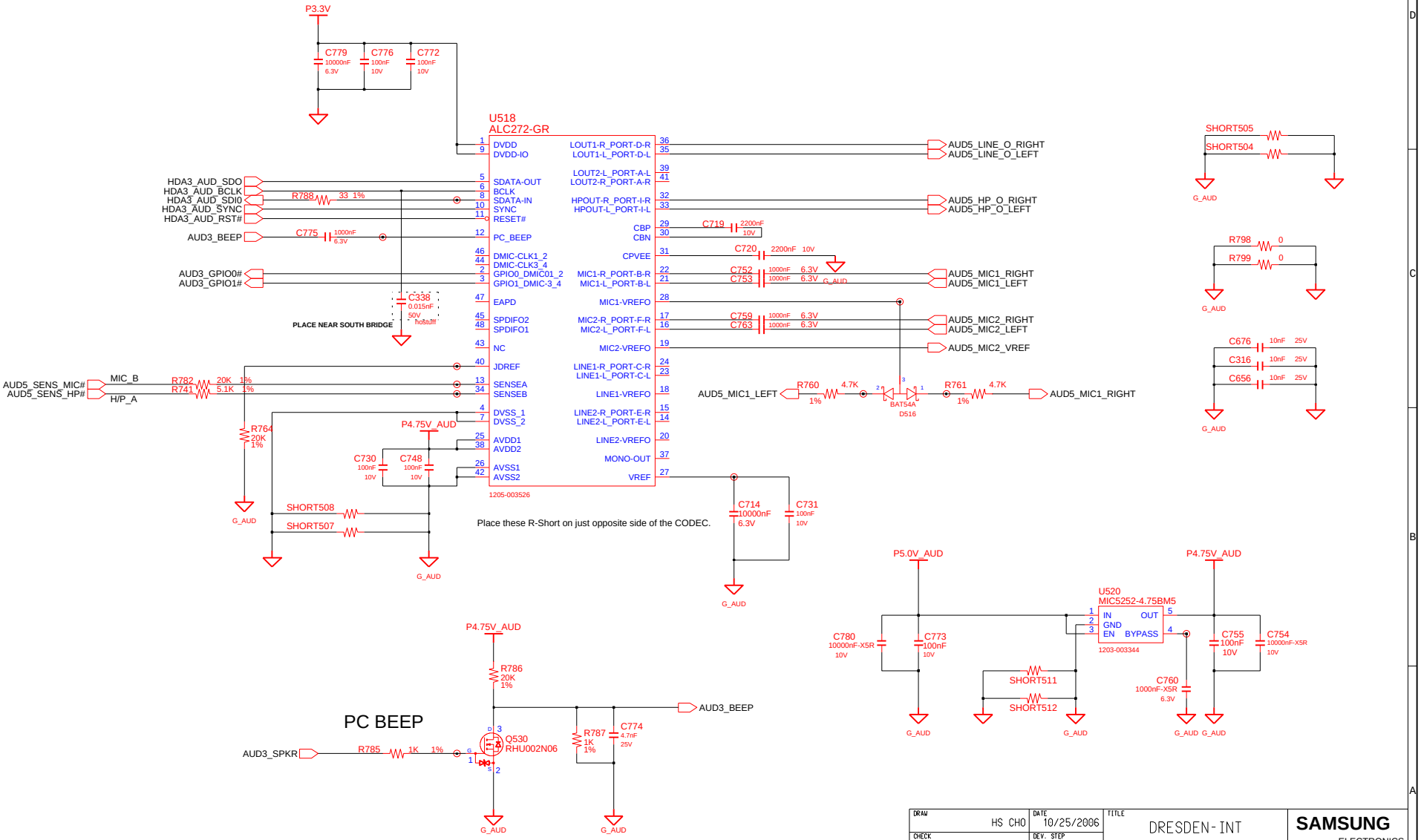
Mini PCI Express Card



Odd Pins : Top side
Even Pins : Bottom Side

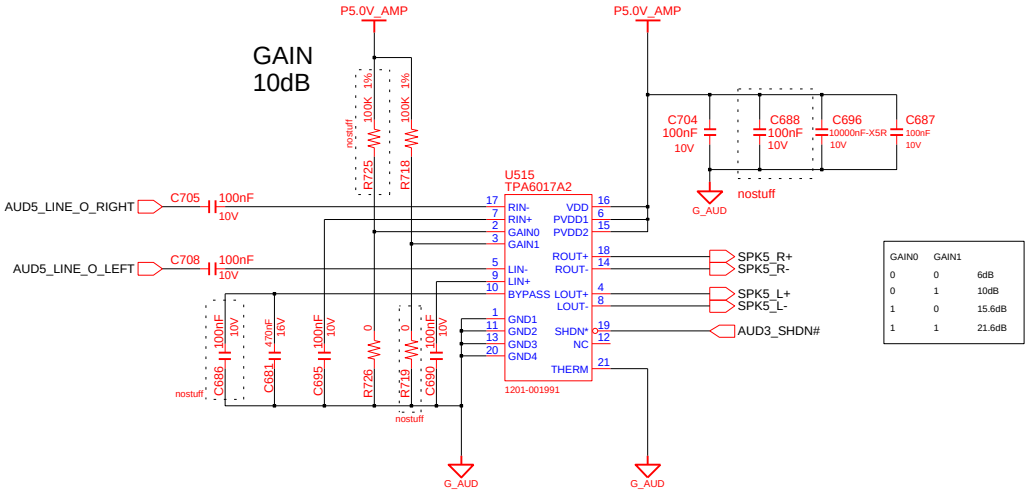
DRAW: HS CHO	DATE: 8/12/2006	TITLE: DRESDEN-INT PCIE_MINICARD WLAN	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024~6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 40 OF 60	

HDA CODEC ALC272

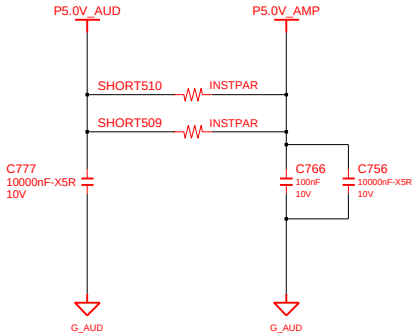


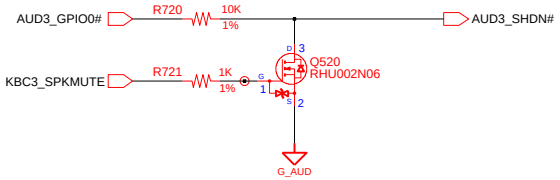
DRAW: HS CHO	DATE: 10/25/2006	TITLE: DRESDEN-INT / MAIN / HDA CODEC	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 27 OF 49	

AUDIO AMP & INT. SPEAKER

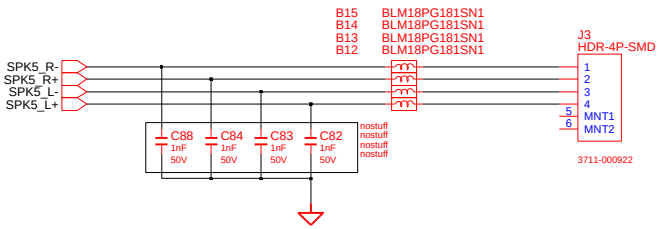


GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



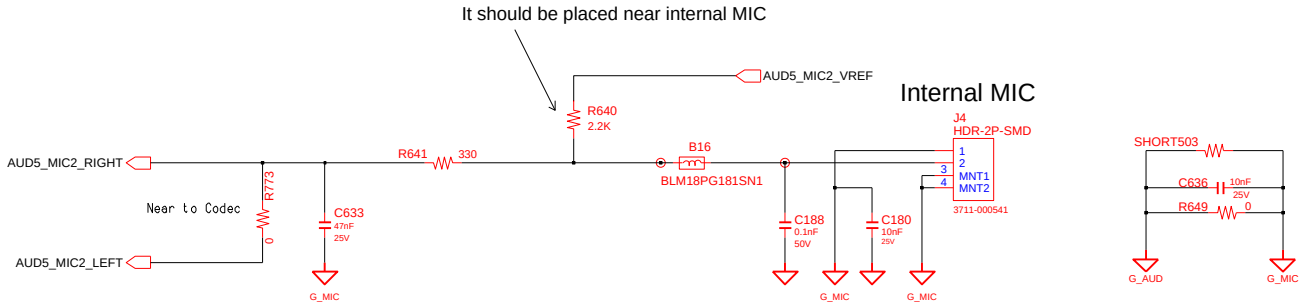


INTERNAL STEREO SPEAKERS

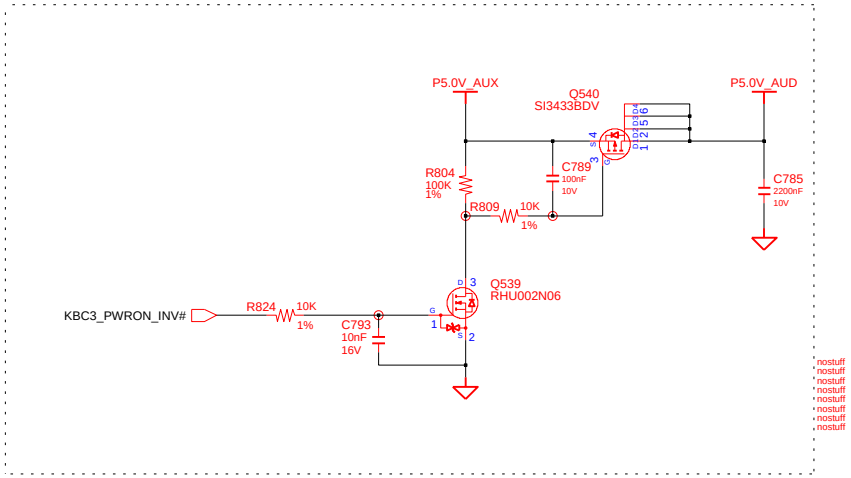


DRAW: HS CHO	DATE: 10/25/2006	TITLE: DRESDEN-INT MAIN AUDIO AMP & INT. SPEAKER	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO. BA41-01024v6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 28 OF 49	

AUDIO POWER & INT. MIC



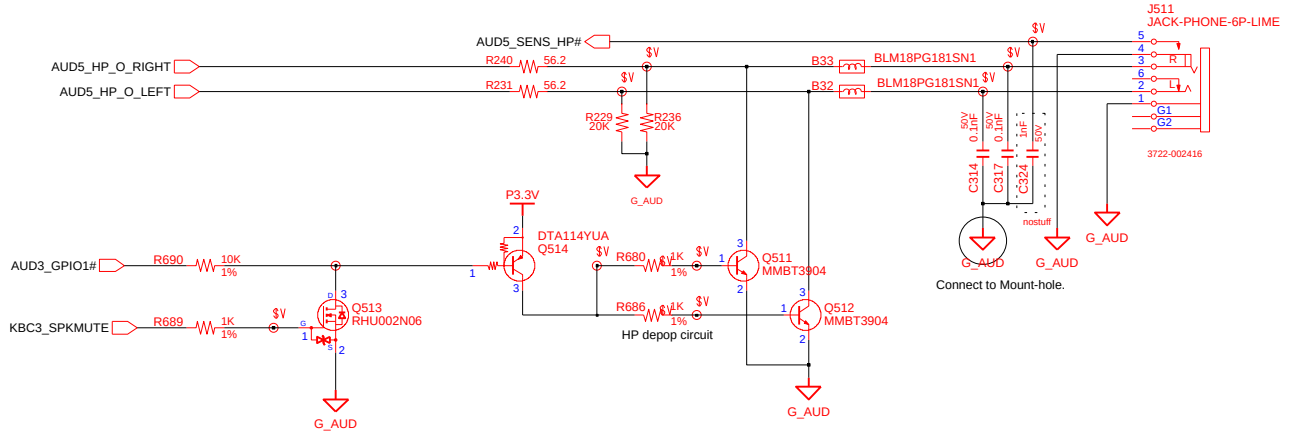
Audio Power (nostuff)

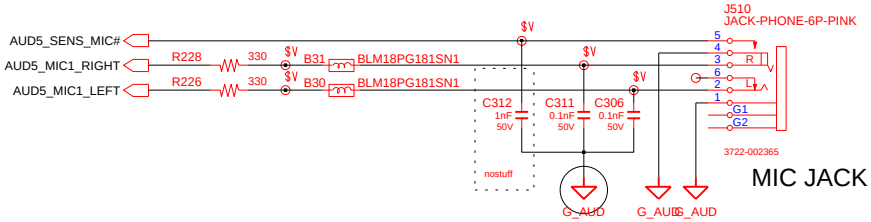


DRAW: HS CHO	DATE: 10/25/2006	TITLE: DRESDEN-INT MAIN AUDIO POWER & INT.MIC	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024A-6A
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 29 OF 49	

HEADPHONE & EXT. MIC

HEADPHONE





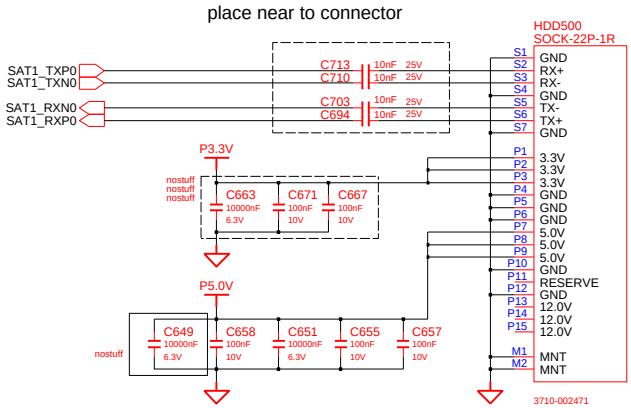
MIC JACK

The traces led to Audio Jacks have the width over 10mil

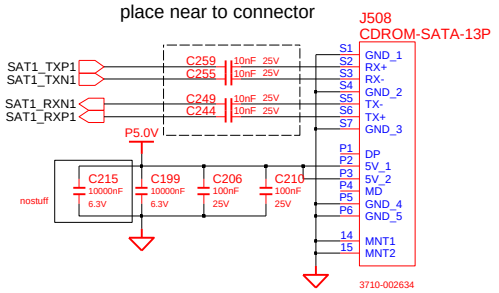
DRAW: HS CHO	DATE: 10/25/2006	TITLE: DRESDEN-INT MAIN HEADPHONE&EXT.MIC	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024A-6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 30 OF 49	

SATA IF CONNECTOR

Main to HDD



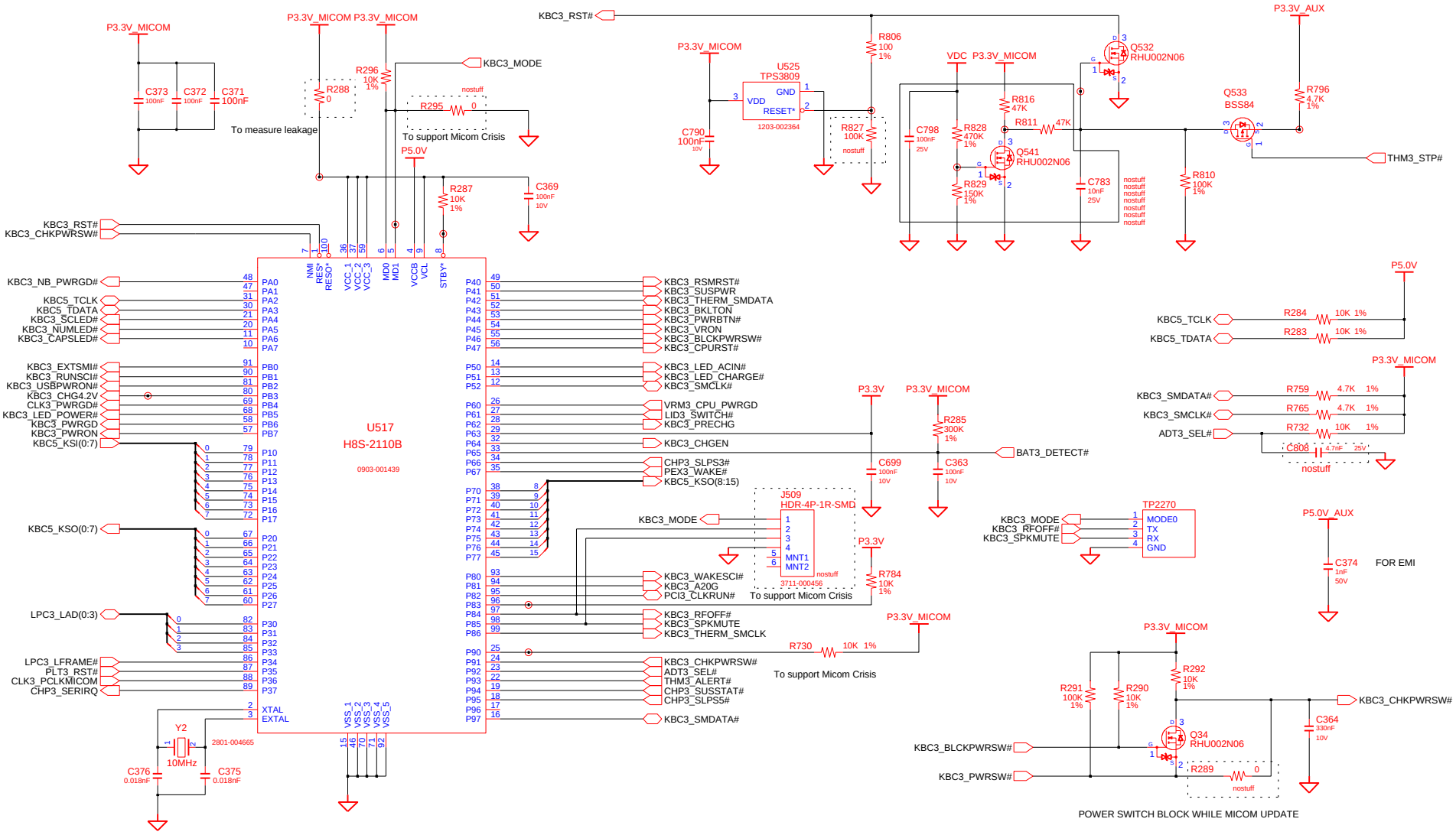
Main to ODD



DRAW: HS CHO	DATE: 8/12/2006	TITLE: DRESDEN-INT MAIN SATA IF CONN	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 31 OF 49	

MICOM

MICOM RESET

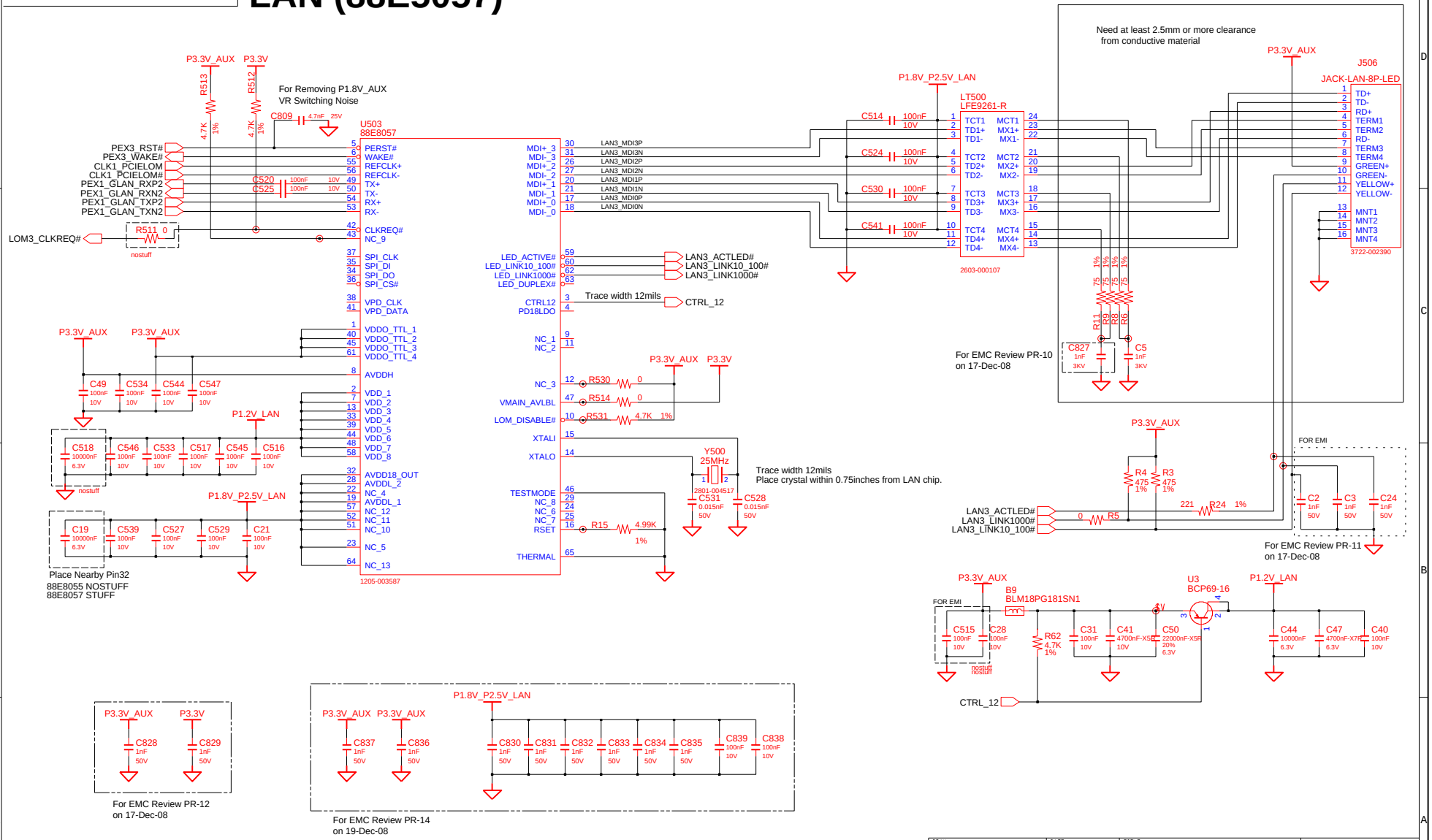


MICOM Crisis Update

Condition: P90=P91=P92=High(MICOM_P3V)
MD0=MD1=Low(0V)
Serial Port: P84 & P85

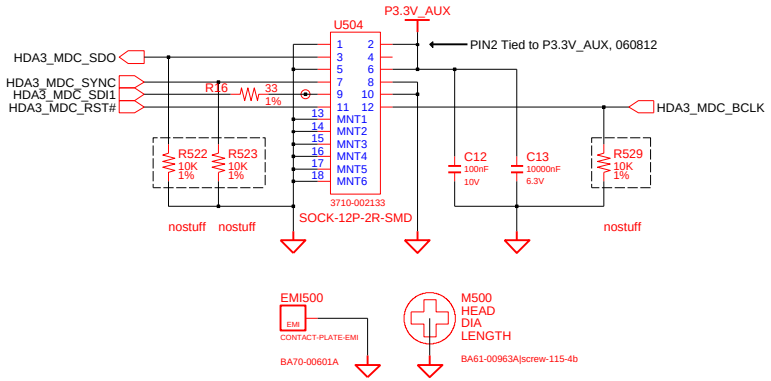
DRAW: HS CHO	DATE: 10/26/2006	TITLE: DRESDEN-INT MAIN MICOM	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 32 OF 49	

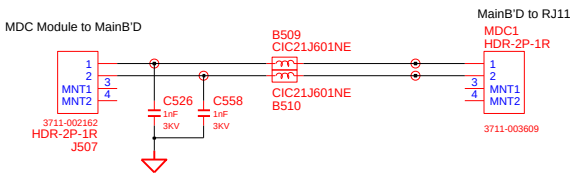
LAN (88E5057)



DRAW: HS CHO	DATE: 11/8/2006	TITLE: DRESDEN-INT MAIN LAN (88E8057)	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 33 OF 49	

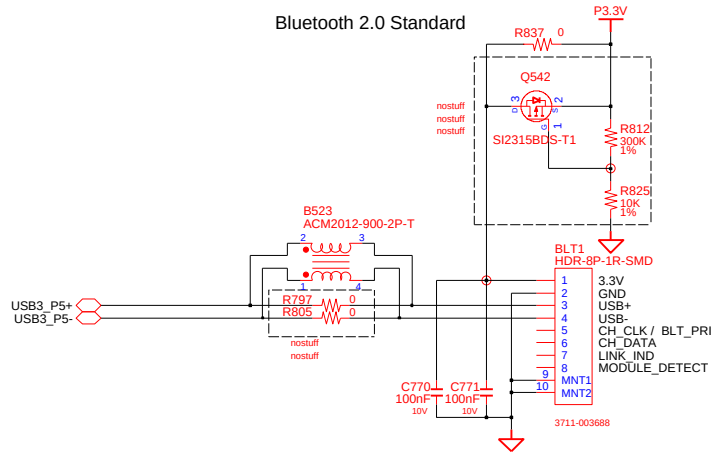
MDC connector



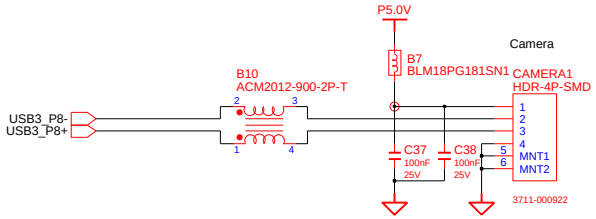


BLUETOOTH

Bluetooth 2.0 Standard

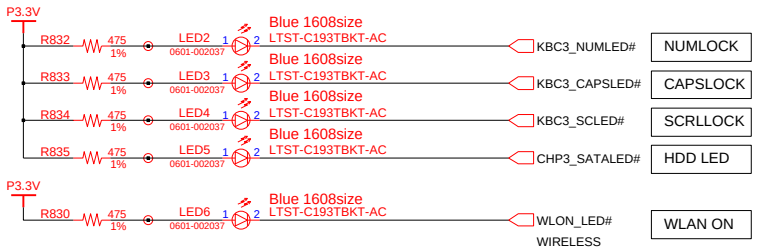


CAMERA

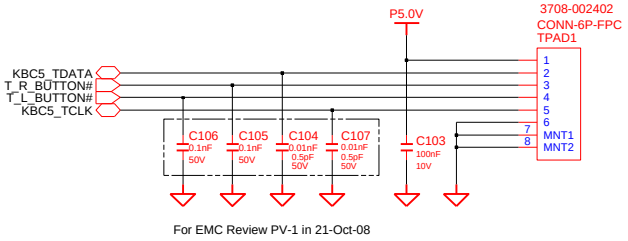


DRAW: HS CHO	DATE: 8/14/2007	TITLE: DRESDEN-INT MAIN CAMERA/BLUETOOTH/MDC	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024*6A
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 34 OF 49	

LEDS

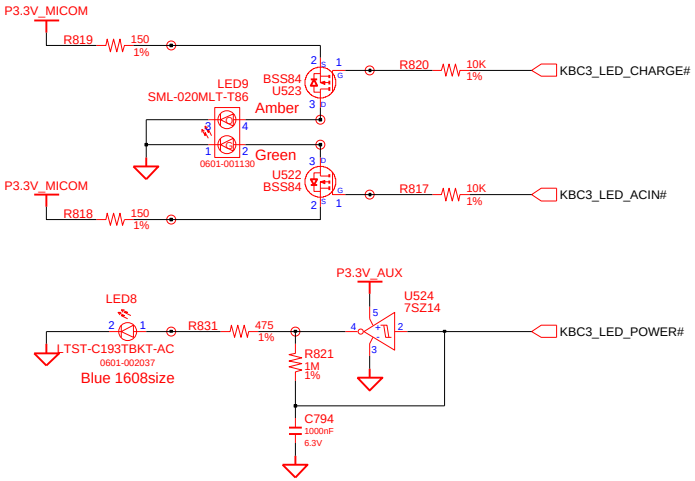


TOUCH PAD

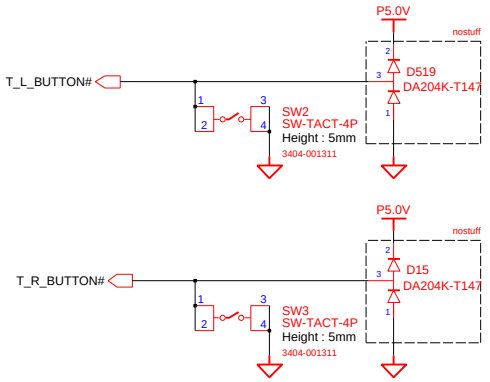


For EMC Review PV-1 in 21-Oct-08

Adaptor-In / Charging LED

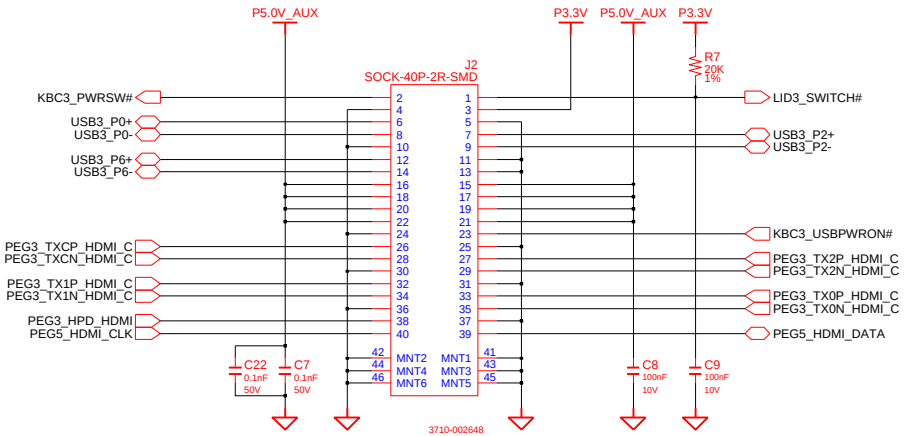


TP_SWITCH

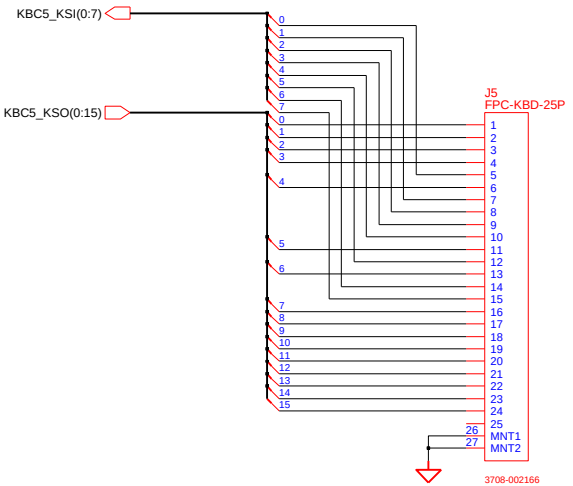


DRAW: HS CHO	DATE: 8/14/2007	TITLE: DRESDEN-INT MAIN LED/TOUCH PAD	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024*6A
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 35 OF 49	

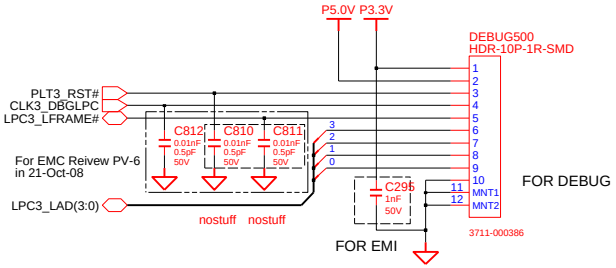
Main to SUB Connector



KEYBOARD

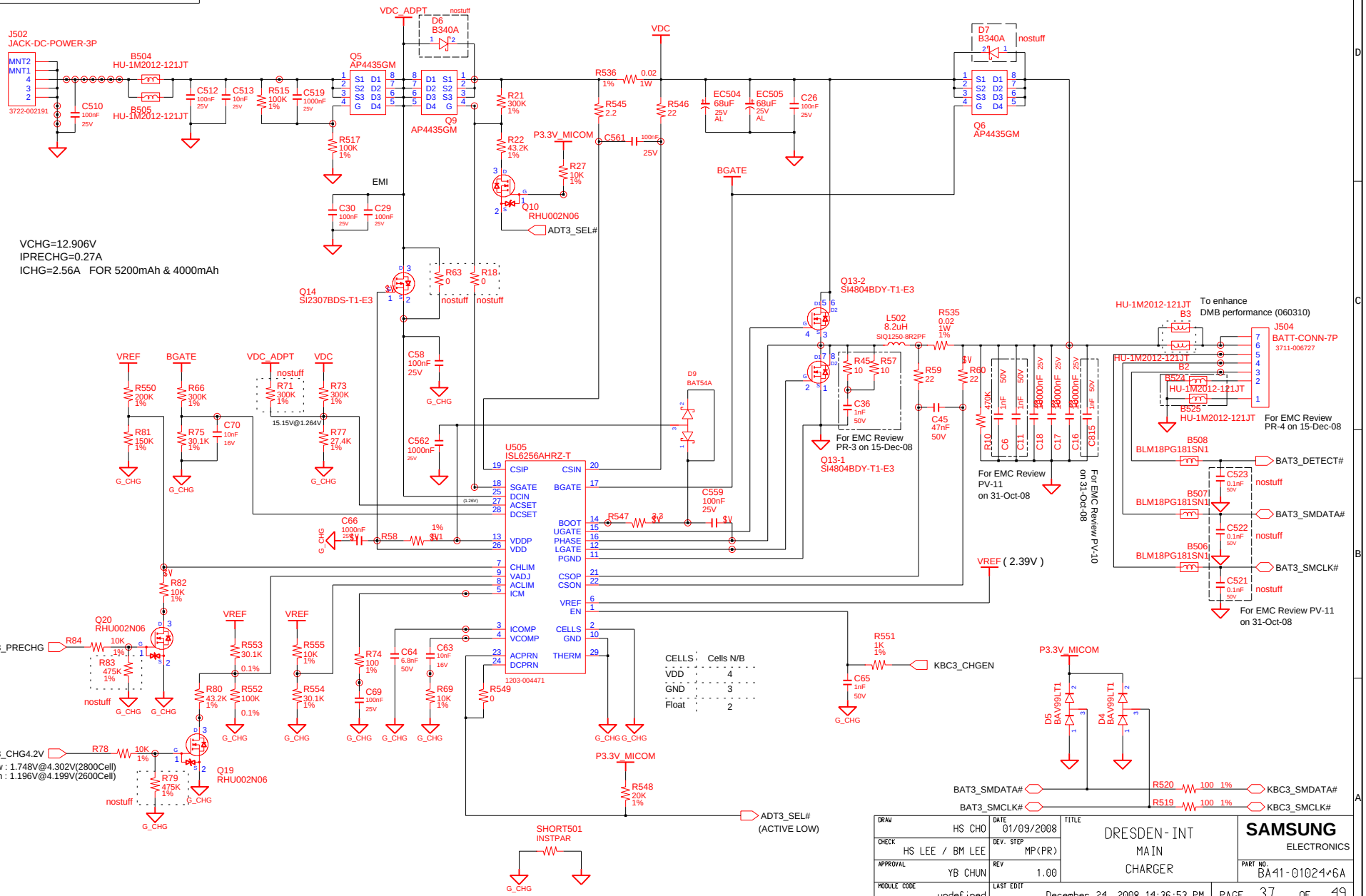


DEBUG PORT



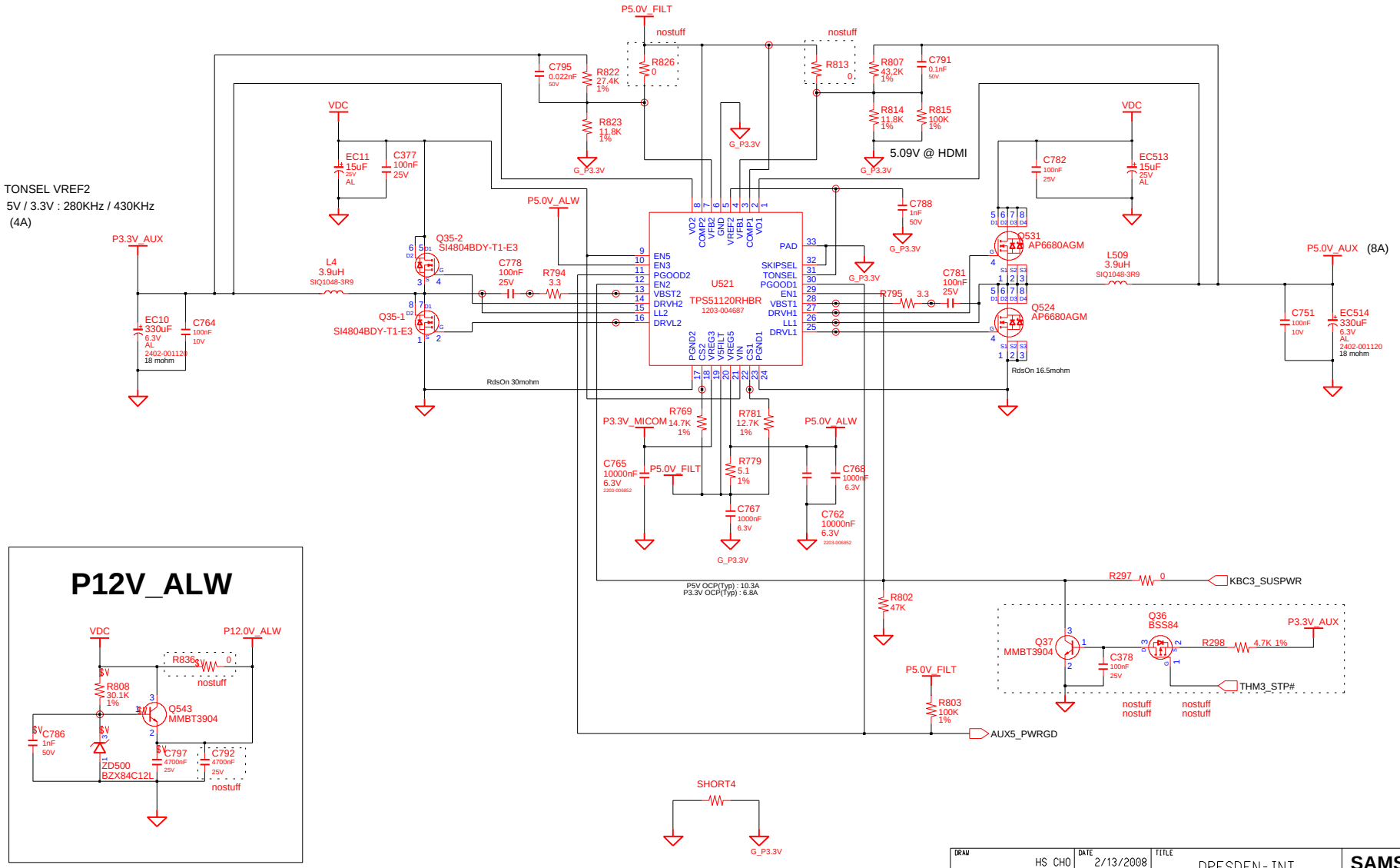
DRAW: HS CHO	DATE: 12/5/2007	TITLE: DRESDEN-INT MAIN SUB/DEBUG/KBD	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 36 OF 49	

CHARGER & POWER MANAGEMENT



DRAW: HS CHO	DATE: 01/09/2008	TITLE: DRESDEN-INT MAIN CHARGER	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		
APPROVAL: YB CHUN	REV: 1.00		PART NO. BA41-01024*6A
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 37 OF 49	

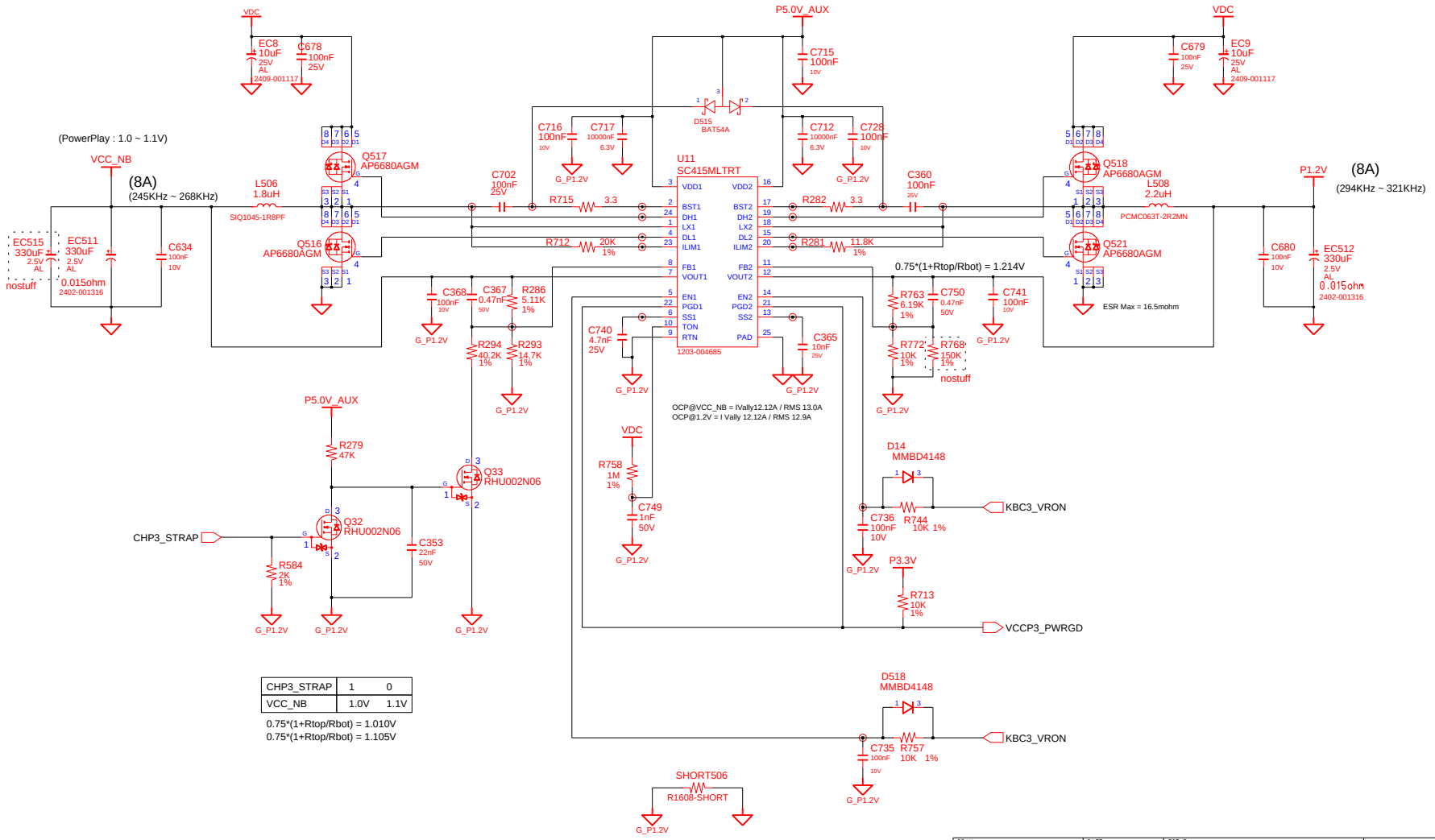
P3.3V_AUX & P5.0V_AUX



P12V_ALW

DRAW: HS CHO	DATE: 2/13/2008	TITLE: DRESDEN-INT / MAIN / AUX POWER	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 38 OF 49	

CHIPSET POWER(VCC_NB & P1.2V)



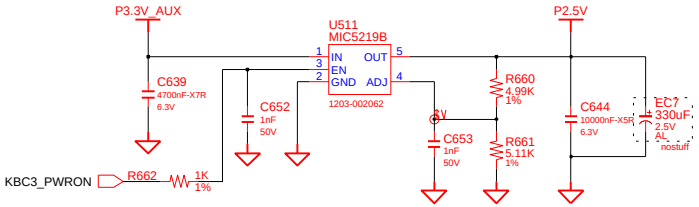
CHP3_STRAP	1	0
VCC_NB	1.0V	1.1V

0.75*(1+Rtop/Rbot) = 1.010V
0.75*(1+Rtop/Rbot) = 1.105V

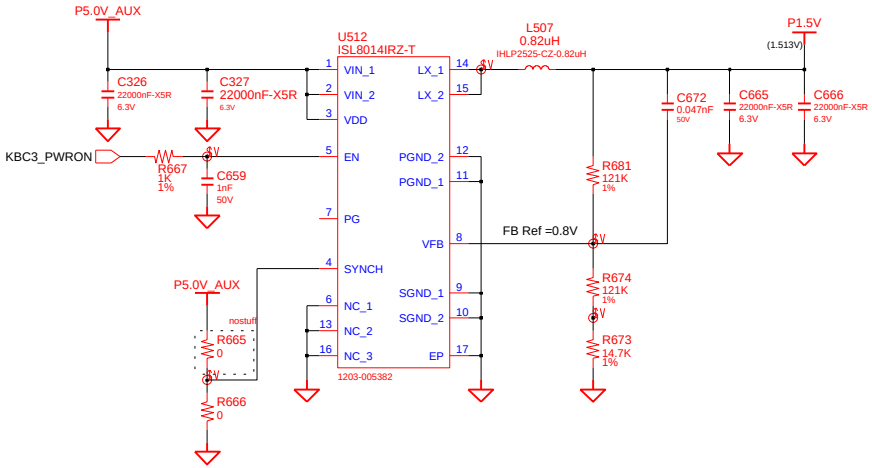
DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	CHIPSET POWER(1/2)	PART NO. BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 39 OF 49	

CHIPSET POWER(P2.5V & P1.5V & P1.1V & P1.2V_AUX)

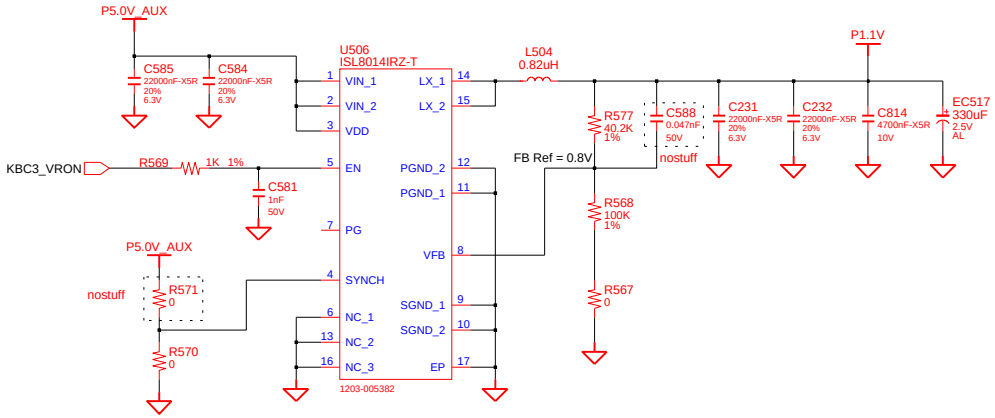
P2.5V



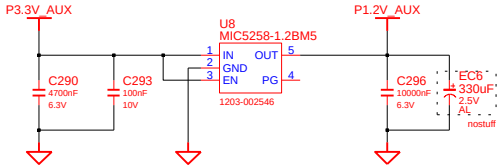
P1.5V



P1.1V

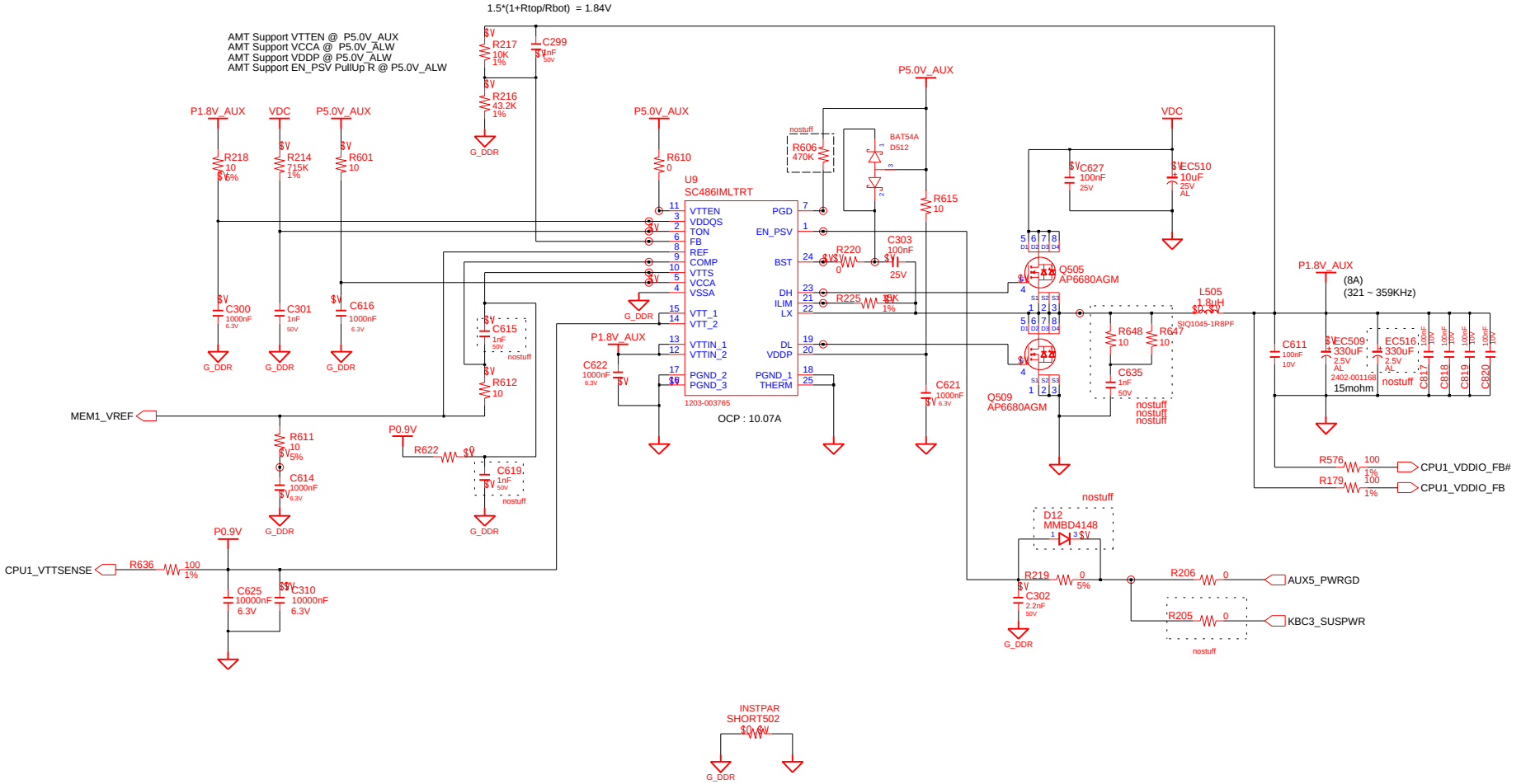


P1.2V_AUX



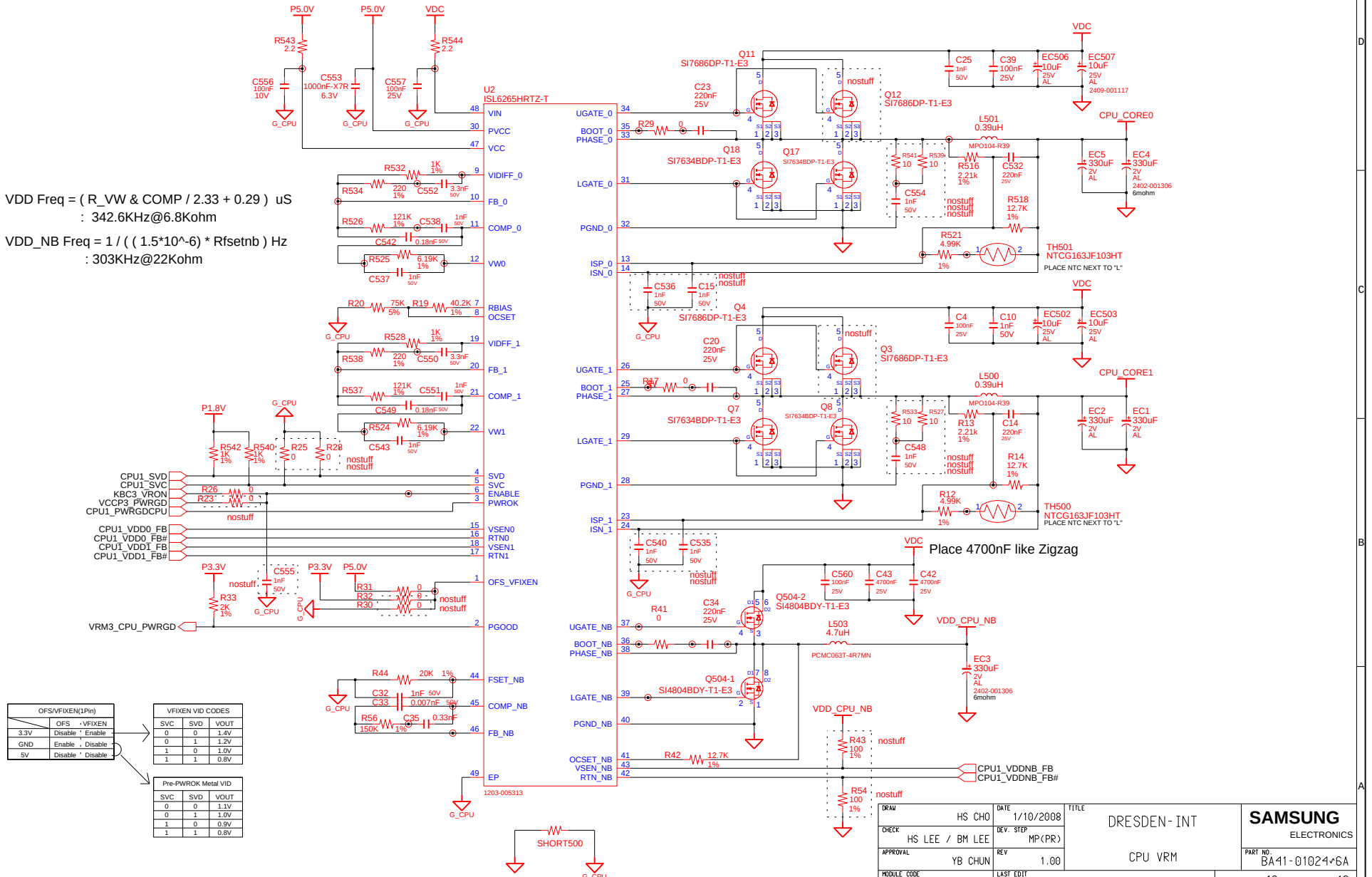
DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	CHIPSET POWER(2/2)	PART NO. BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 40 OF 49	

DDR2 Power



DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	DDR2 POWER	PART NO. BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 41 OF 49	

CPU VRM [INTERSIL]



OFS/VFIXEN(1Pin)	OFS	VFIXEN
3.3V	Disable	Enable
GND	Enable	Disable
5V	Disable	Disable

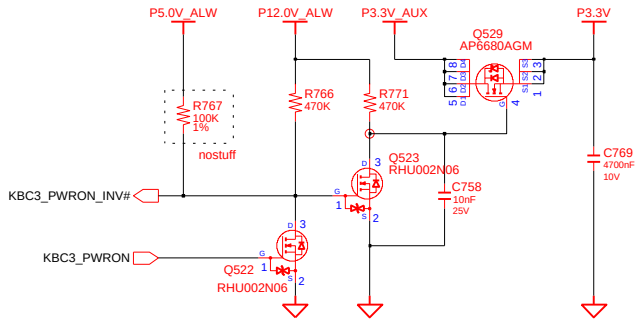
VFIXEN VID CODES		
SVC	SVD	VOUT
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

Pre-PWROK Metal VID		
SVC	SVD	VOUT
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

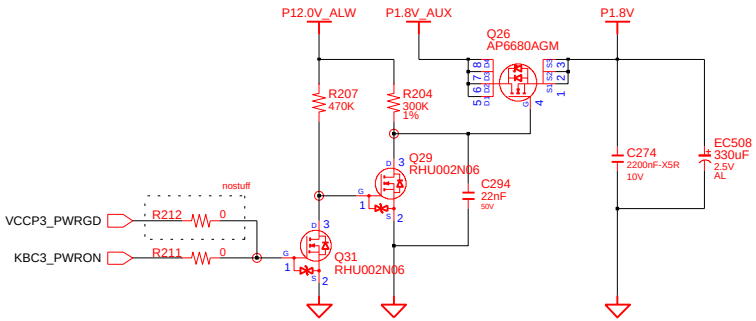
DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	CPU VRM	PART NO. BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 42 OF 49	

Switched Power

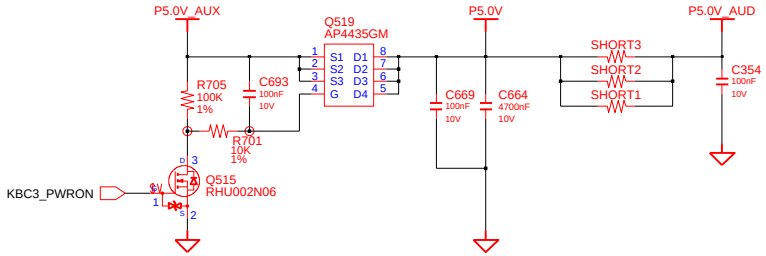
Switched Power On (P3.3V)



Switched Power On (P1.8V)

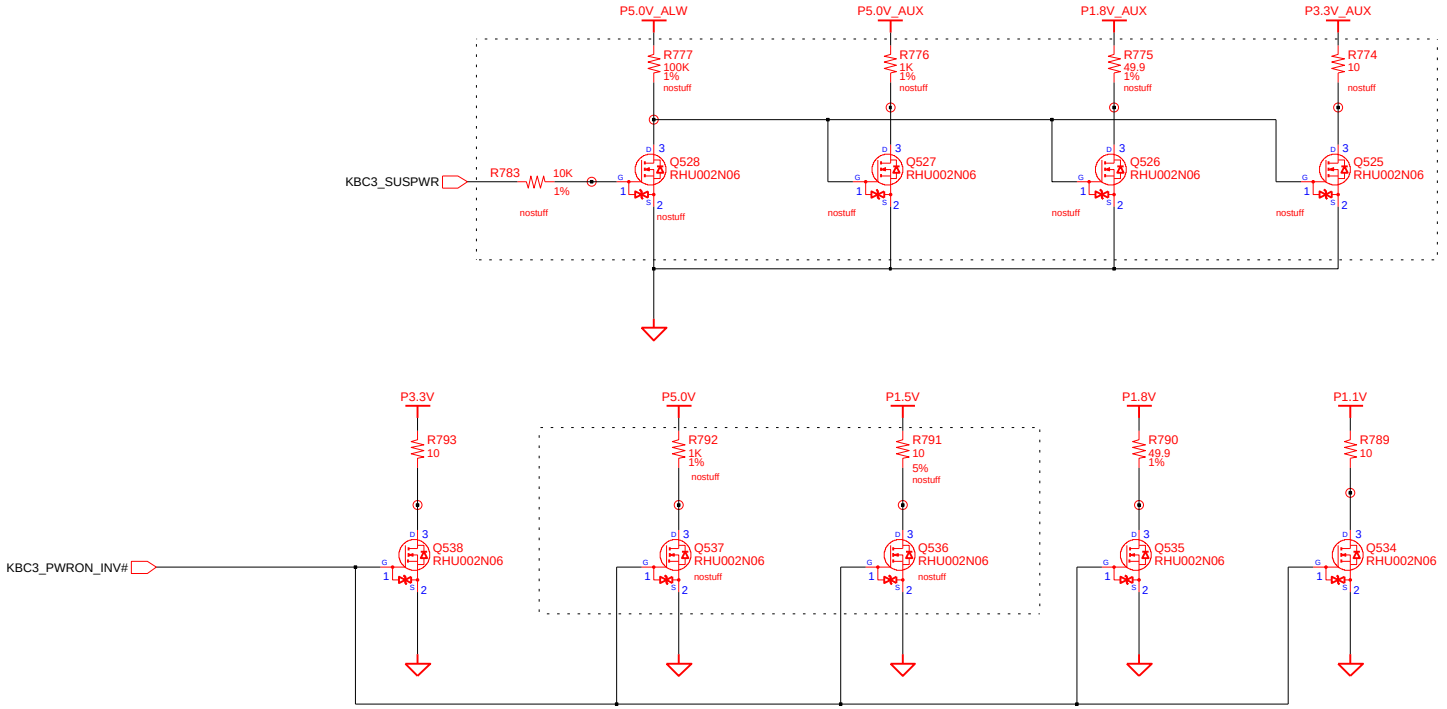


Switched Power On (P5.0V)



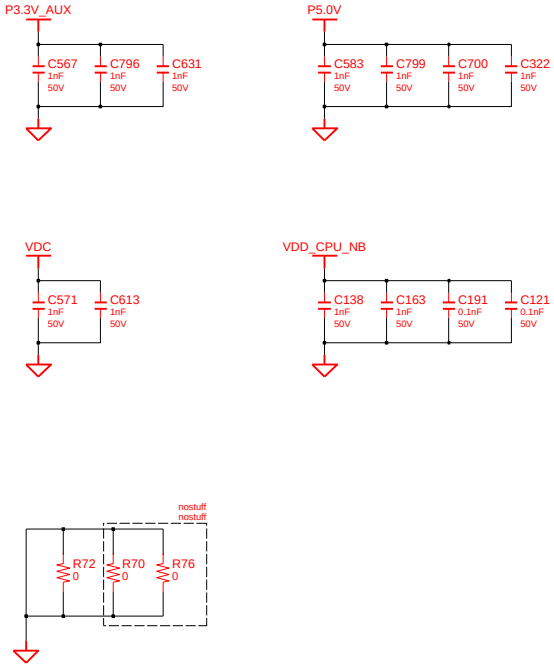
DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	Swiched Power	PART NO.: BA41-01024*6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 43 OF 49	

POWER DISCHARGER

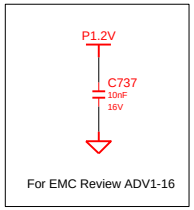


DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	POWER DISCHARGER	PART NO. BA41-01024A-6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 44 OF 49	

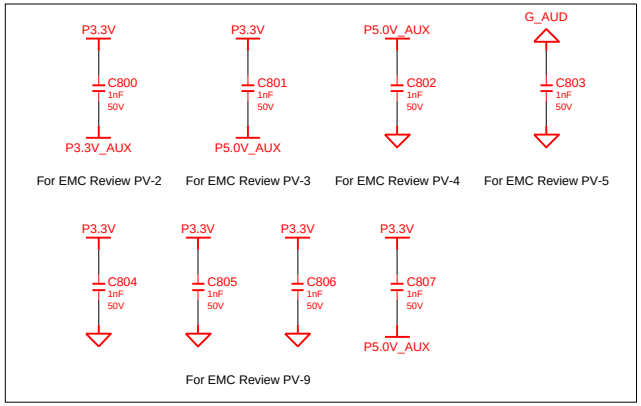
EMC



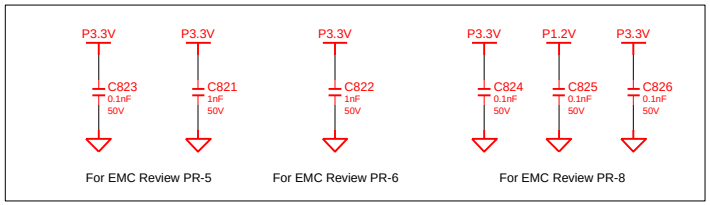
Added on 18-Sep-08



Added on 21-Oct-08

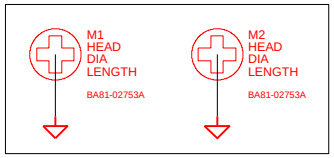


Added on 15-Dec-08

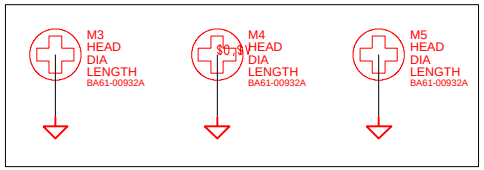


DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	EMC	
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024*6A
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 45 OF 49	

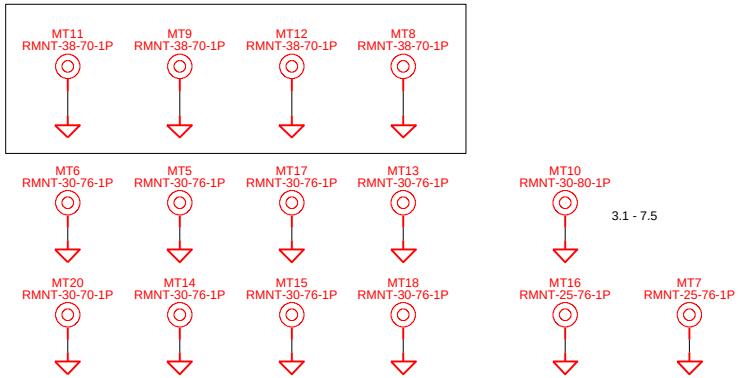
FAN-NUT



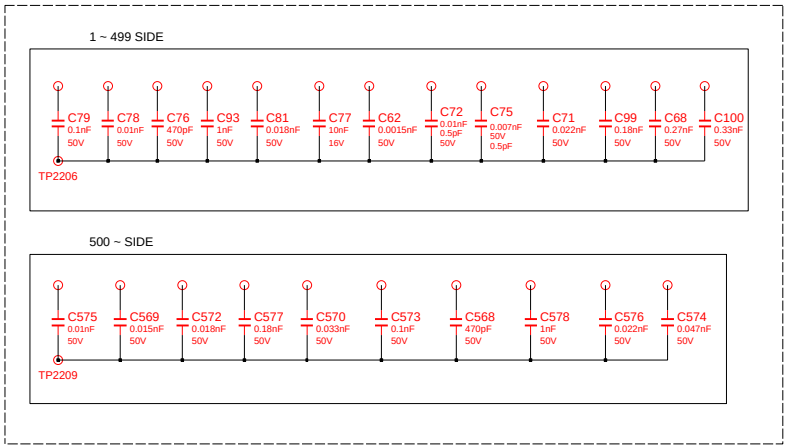
THERMAL-NUT



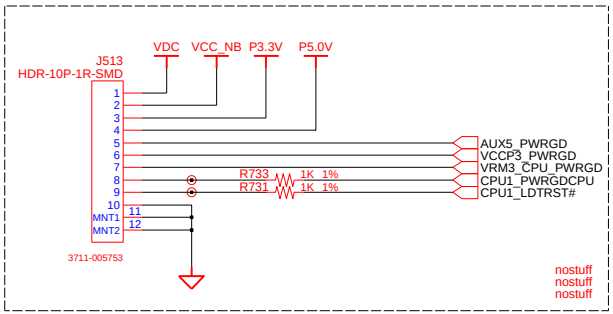
CPU RHE



ICT Cap : need to change with last BOM



ICT PORT



PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			ADV1
2	1-2			PV
3	2-3		1.0	MP(PR)
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	MTH/ICT	
APPROVAL: YB CHUN	REV: 1.00		PART NO. BA41-01024*6A
MODULE CODE	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 46 OF 49	

MCD3_SDWP
MEM1_VREF
PCI3_AD23
PCI3_AD24
PCI3_AD25
PCI3_AD26
PCI3_AD27
PCI3_AD28
PEX3_WAKE#
PEX3_RST#
AUD3_GPIO0#
AUD3_GPIO1#
BAT3_SMCLK#
CHP3_A_RST#
CHP3_GPIO16
CHP3_GPIO17
CHP3_SERIRQ
CHP3_SLPS3#
CHP3_SLPS5#
CLK3_DBGLPC
CLK3_PWRGD#
CPU1_ALERT#
CRT3_DDCCLK
CRT5_DDCCLK
CRT3_DDCDATA
CRT5_DDCDATA
EXP3_CPUSB#
EXP3_PERST#
SMB3_DATA
SPI3_CS0#
SPI3_MISO
SPI3_MOSI
THM3_STP#
WLON_LED#
AUD3_SHDN#
AUX5_PWRGD
CRT3_HSYNC
CRT3_VSYNC

EXP3_CPPE#
KBC3_CHGEN
KBC3_PWRGD
KBC3_PWRON
KBC3_PRECHG
KBC3_PWRSW#
KBC3_RFOFF#
KBC3_SCLED#
KBC3_SMCLK#
KBC3_SUSPWR
KBC5_KSI(0)
KBC5_KSI(1)
KBC5_KSI(2)
KBC5_KSI(3)
KBC5_KSI(4)
KBC5_KSI(5)
KBC5_KSI(6)
KBC5_KSI(7)
KBC5_KSO(0)
KBC5_KSO(1)
KBC5_KSO(2)
KBC5_KSO(3)
KBC5_KSO(4)
KBC5_KSO(5)
KBC5_KSO(6)
KBC5_KSO(7)
KBC5_KSO(8)
KBC5_KSO(9)
MCD3_SDCD#
MCD3_SDCLK
MCD3_SDCMD
LCD3_BKLTON
LPC3_LAD(0)
LPC3_LAD(1)
LPC3_LAD(2)
LPC3_LAD(3)
CPU2_THERMDA
CPU2_THERMDC

EXP3_CLKREQ#
FAN3_FDBACK#
CHP3_NB_THERMDN
CHP3_NB_THERMDP
HDA3_AUD_SDO
HDA3_MDC_SDO
KBC3_CPURST#
KBC3_EXTSMI#

KBC3_NUMLED#
KBC3_PWRBTN#
KBC3_RSMRST#
KBC3_RUNSCI#
KBC3_SMDATA#
KBC3_SPKMUTE
KBC5_KSO(10)
KBC5_KSO(11)
KBC5_KSO(12)
KBC5_KSO(13)
KBC5_KSO(14)
KBC5_KSO(15)
LAN3_ACTLED#
LID3_SWITCH#

LPC3_LFRAME#
MCD3_SDDATA0
MCD3_SDDATA1
MCD3_SDDATA2
MCD3_SDDATA3
MCH3_EXTTS0#

THM3_ALERT#
VCCP3_PWRGD
BAT3_DETECT#
BAT3_SMDATA#
CHP3_RTCRST#
SMB3_ALERT#
MIN3_CLKREQ#
PCI3_CLKRUN#
CHP3_NB_PWRGD
CHP3_SATALED#
CHP3_SB_TEST0
CHP3_SB_TEST2
CHP3_SUSSTAT#
PEG3_HPD_HDMI

PEG5_HDMI_CLK
AUD5_LINE_O_LEFT
AUD5_HP_O_RIGHT
AUD5_MIC1_RIGHT
AUD5_MIC2_RIGHT
AUD5_HP_O_LEFT
AUD5_MIC1_LEFT
AUD5_MIC2_LEFT
AUD5_MIC2_VREF
CHP1_THRMTRIP#
CHP3_BIOS_CRI#
CHP3_INTRUDER#

CPU1_PROCHOT#

CPU1_VDD0_FB#
CPU1_VDD1_FB#
CPU1_VDDIO_FB
CPU1_VDDNB_FB
HDA3_AUD_BCLK
HDA3_AUD_RST#
HDA3_AUD_SDI0
HDA3_AUD_SYNC
HDA3_MDC_BCLK
HDA3_MDC_RST#
HDA3_MDC_SDI1
HDA3_MDC_SYNC
KBC3_CAPSLED#
KBC3_NB_PWRGD#
VRM3_CPU_PWRGD
CPU1_ALL_LDTSTP
KBC3_BLCKPWRSW#
KBC3_LED_POWER#
KBC3_PWRON_INV#
USB3_SUB_PWRON#
CHP3_STRAP
KBC3_LED_CHARGE#
KBC3_THERM_SMCLK
LAN3_LINK10_100#
CPU1_THRMTRIP#
CPU1_VDDIO_FB#
CPU1_VDDNB_FB#
CPU3_THRMTRIP#
USB3_SUB_DISCHG#
AUD5_LINE_O_RIGHT
KBC3_THERM_SMDATA
PEG3_HDMI_SUB_CLK

PEG5_HDMI_SUB_CLK
PEG3_HDMI_SUB_DATA

KBC3_CHKPWRSW#
KBC3_LED_ACIN#
KBC3_USBPWRON#
LAN3_LINK1000#
PEG5_HDMI_DATA
KBC3_WAKESCI#
LCD3_EDID_CLK
PEG5_HDMI_SUB_DATA

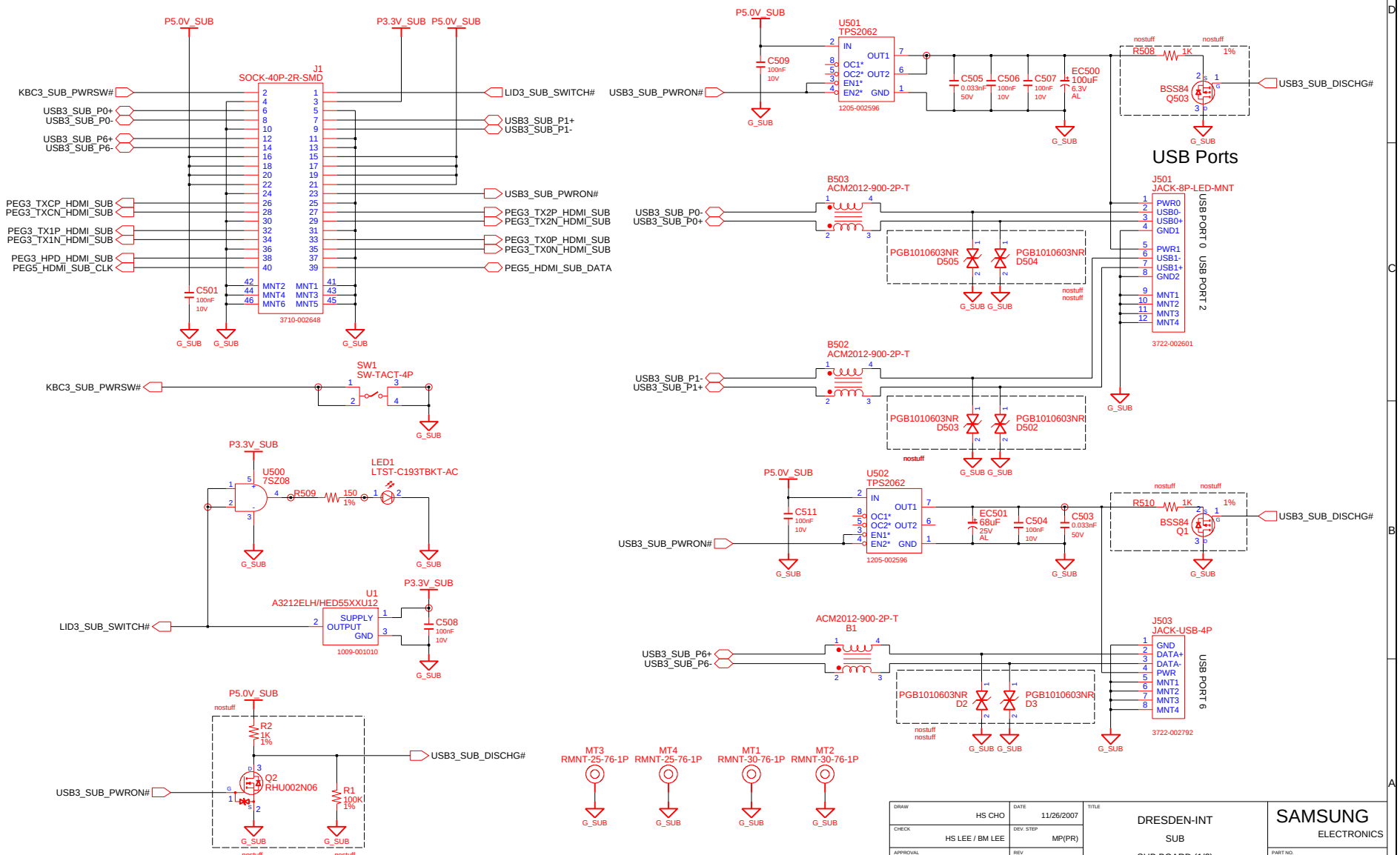
HDMI3_MS
SMB3_CLK
SPI3_CLK
ADT3_SEL#
AUD3_BEEP
AUD3_SPKR
KBC3_A20G
KBC3_VRON
CTRL_12
SPK5_L+
SPK5_L-
SPK5_R+
SPK5_R-
FAN5_VDD

T_L_BUTTON#
T_R_BUTTON#
KBC3_BKLTON
KBC3_RST#
KBC5_TCLK
KBC5_TDATA
P3.3V_AUX_EXP
P1.8V_P2.5V_LAN
VDC
VREF
VDC_INV
VDC_ADPT
VDD_CPU_NB
P1.1V
P3.3V_MCD
P5.0V_ALW
P5.0V_AMP
P5.0V_AUD
P5.0V_AUX
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
BGATE
CPU_CORE0
CPU_CORE1
G_AUD
G_CHG
G_CPU
G_DDR
G_MIC

G_P1.2V
G_P3.3V
LCD_VDD3V
P0.9V
P1.2V
P1.5V
P1.8V
P2.5V
P5.0V_SUB
P12.0V_ALW
P3.3V_HDMI
P4.75V_AUD
P5.0V_FILT
P3.3V_MICOM
P3.3V
PRTC_BAT
P1.2V_AUX
P1.2V_LAN
P1.5V_EXP
P1.8V_AUX
P3.3V_AUX
P3.3V_EXP
VCC_NB
P5.0V
VCC_CRT

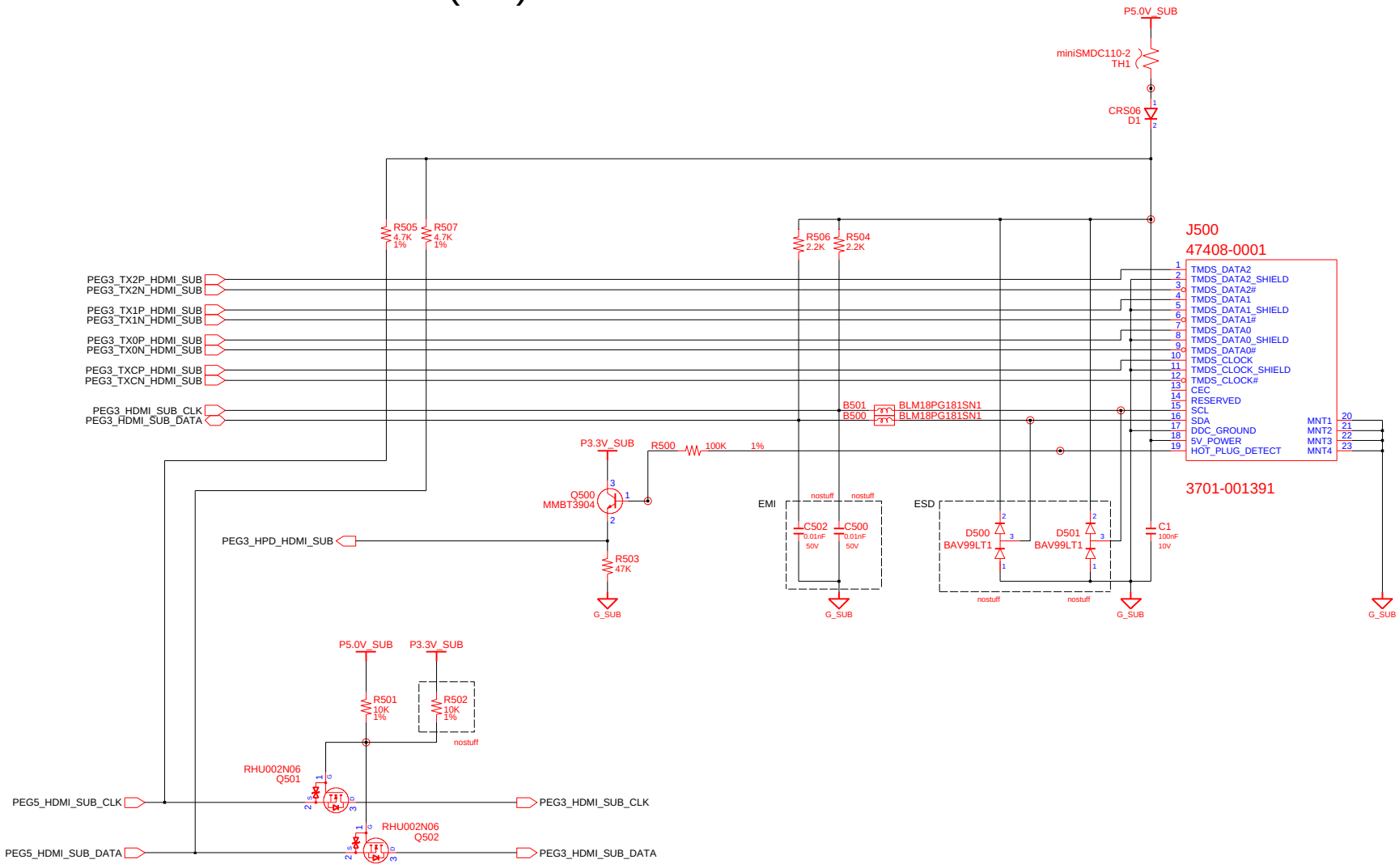
DRAW: HS CHO	DATE: 1/10/2008	TITLE: DRESDEN-INT	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)	TP	
APPROVAL: YB CHUN	REV: 1.00		PART NO.: BA41-01024*6A
MODULE CODE: undefined	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 47 OF 49	

Sub Board (1/2)



DRAW: HS CHO	DATE: 11/26/2007	TITLE: DRESDEN-INT / SUB / SUB BOARD (1/2)	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024~6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 48 OF 49	

Sub Board (2/2)



Note: These FETs should be placed near HDMI Connector

DRAW: HS CHO	DATE: 11/26/2007	TITLE: DRESDEN-INT / SUB / SUB BOARD (2/2)	SAMSUNG ELECTRONICS
CHECK: HS LEE / BM LEE	DEV. STEP: MP(PR)		PART NO.: BA41-01024~6A
APPROVAL: YB CHUN	REV: 1.00		
MODULE CODE:	LAST EDIT: December 24, 2008 14:36:53 PM	PAGE 49 OF 49	

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