INTEL PINETRAIL Platform

F10T

Version : A

Drawing by :Wain

Notes:

Part Value Prefix : "POP=NA" means nopop

Net Value postfix : "#" means Low Active

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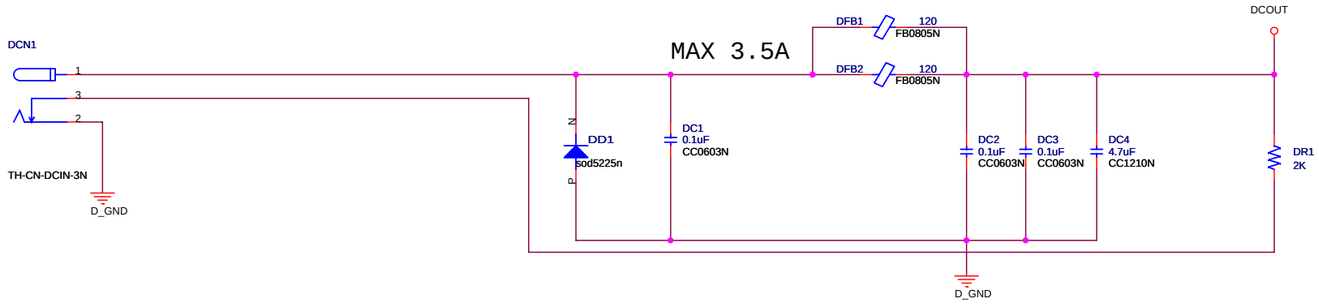
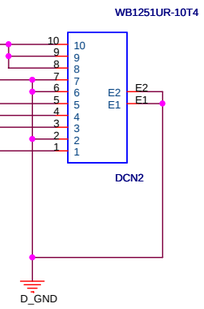
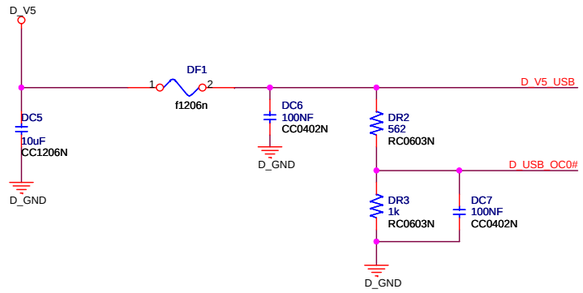
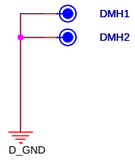
ENGINEER:	Wain	Title <Title>	
		Size C / Sheet Name: Cover sheet	Rev A
		Date: Wednesday, November 04, 2009	Sheet 1 of 36

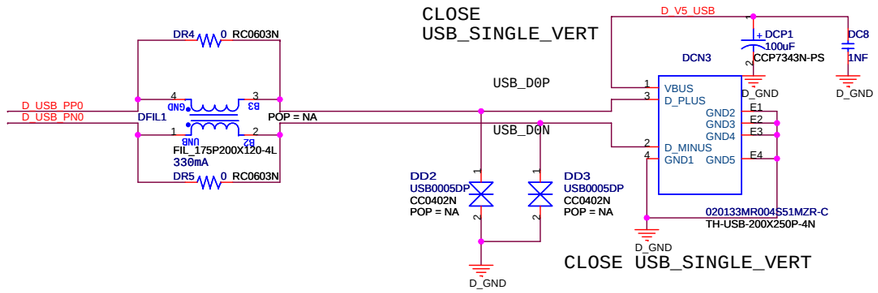








USB Port1



Title	<Title>	
Size C	Document Number <Doc>	Rev
Date: Wednesday, November 04, 2009	Sheet 1 of 1	

BLOCK DIAGRAM

CLK_CPU_BCLK#,CLK_CPU_BCLK

CLK_MCH_BCLK#,CLK_MCH_BCLK
DREFCLK#,DREFCLK
DREFSSCLK#,DREFSSCLK
CLK_MCH_3GPLL#,CLK_MCH_3GPLL

14.318MHz

Clock Gen

CLK_PCIE
CLK_AC97
CLK_TPMPCI
CLK_KBCPCI

FAN — KBC — THERMAL IC

Intel
Pineview-M

CRT — R.G.B

LVDS — LVDS

DDR2-533 — SO DIMM1

CLK_LAN

DMI X4
400MB/S
@
200MHz

32.768KHz

CLK_ICH14
CLK_ICHPCI
CLK_USB48
CLK_PCIE_SATA#,CLK_PCIE_SATA
CLK_PCIE_ICH#,CLK_PCIE_ICH

PCIE

Hard Disk — SATA

Tiger point

USB2.0 — RTS5156

24.576MHz

USB2.0 — USB0, USB1, USB7

32.768KHz — LPC BUS

CLK_KBCPCI

KBC — BIOS&EC, KB, TOUCH PAD

TCM

Azalia — Audio Codec, Modem Codec

CLK_Azalia

PCI-E — LAN — 25MHz

MINI CARD

System Power
O2 815

CPU Power
ISL6266
/ISL6261

Chipset Power
APW7138

DDR2 Power
APW7138

Charger
ISL6253

S3/S4 Control
and Discharge

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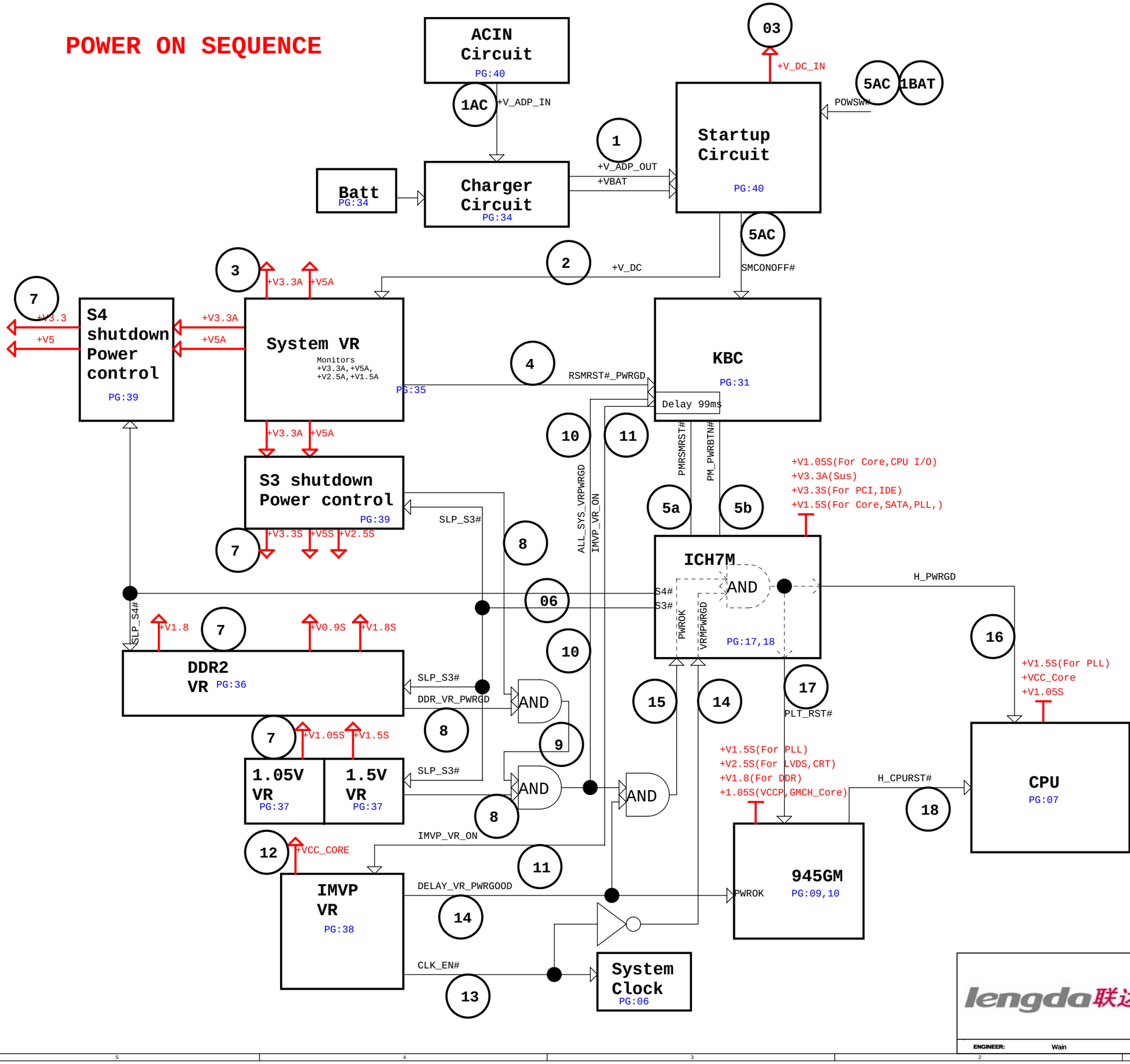
Title	<Title>		
Size C	Sheet Name	Glock Diagram	Rev A
Date:	Wednesday, November 04, 2009	Sheet 2 of 36	

ENGINEER: Wain

POWER ON SEQUENCE



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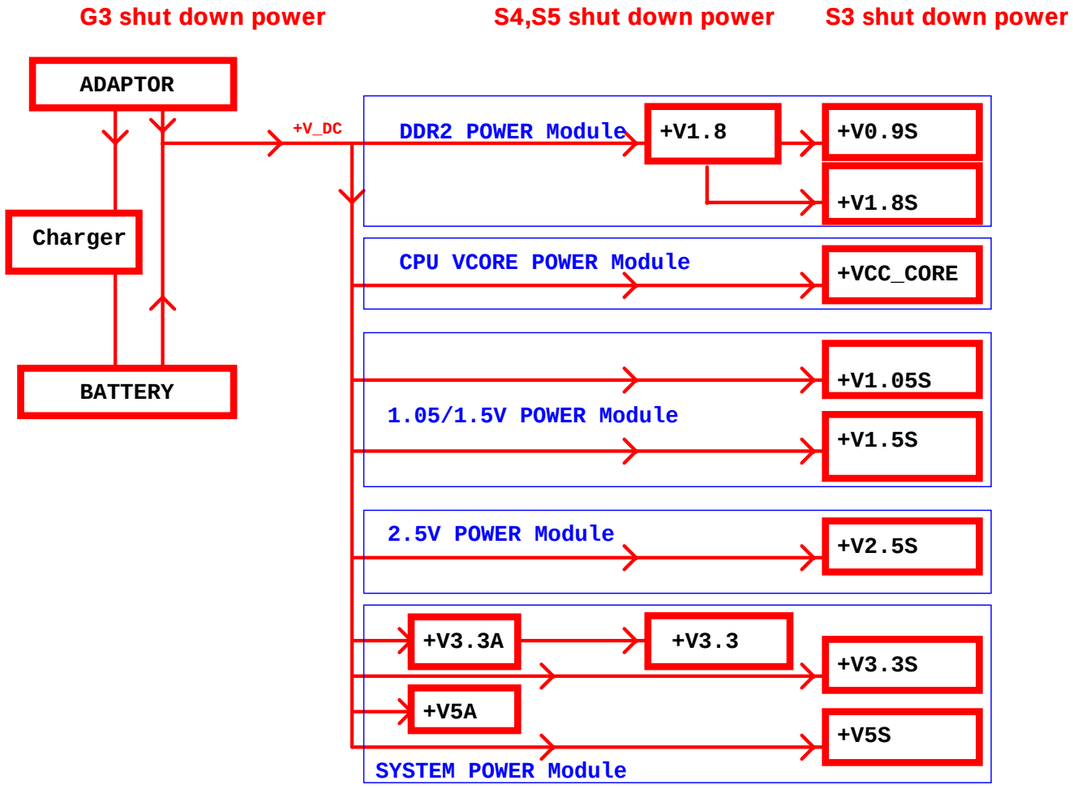
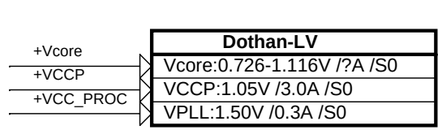
		Title <Title>	
		Size C / Sheet Name Power_On_sequence	Rev A
		Date: Wednesday, November 04, 2009	Sheet 3 of 36

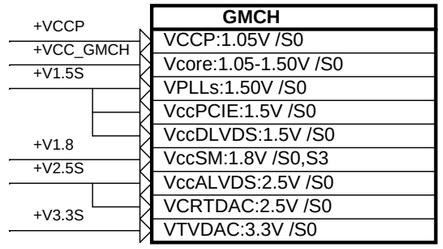
POWER Delivery Architectural Block Diagram





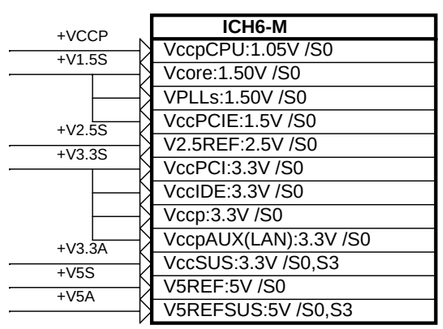
Dothan-LV
Vcore:0.726-1.116V /?A /S0
VCCP:1.05V /3.0A /S0
VPLL:1.50V /0.3A /S0

+Vcore, +VCCP, +VCC_PROC



GMCH
VCCP:1.05V /S0
Vcore:1.05-1.50V /S0
VPLLs:1.50V /S0
VccPCIE:1.5V /S0
VccDLVDS:1.5V /S0
VccSM:1.8V /S0,S3
VccALVDS:2.5V /S0
VCRTDAC:2.5V /S0
VTVDAC:3.3V /S0

+VCCP, +VCC_GMCH, +V1.5S, +V1.8, +V2.5S, +V3.3S



ICH6-M
VccpCPU:1.05V /S0
Vcore:1.50V /S0
VPLLs:1.50V /S0
VccPCIE:1.5V /S0
V2.5REF:2.5V /S0
VccPCI:3.3V /S0
VccIDE:3.3V /S0
Vccp:3.3V /S0
VccpAUX(LAN):3.3V /S0
VccSUS:3.3V /S0,S3
V5REF:5V /S0
V5REFSUS:5V /S0,S3

+VCCP, +V1.5S, +V2.5S, +V3.3S, +V3.3A, +V5S, +V5A

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		Title <Title>	
		Size: C	Sheet Name: Power_Block — Rev: A
		Date: Wednesday, November 04, 2009	Sheet 4 of 36

POWER RAIL	DESTINATION	VOLTAGE	S0 CURRENT
VCORE_CPU	Banias	0.7-1.708V	32A
VCCP	Banias	0.9-1.105V	2.5A
	ICH4M MontaraGM		0.72A
1.8VDDM	Banias (PLL)	1.8V	0.3A
	MontaraGM(PLL)		0.099A
1.2VDDM		1.2V	1.89A
	(CORE, HUB, DDRDDL)		(1.4A, 0.09A, 0.4A)
1.5VDDM	MontaraGM	1.5V	0.23A
	(LVDS, DAC, DVO)		(0.07A, 0.07A, 0.09A)
	ICH4M (CORE)		0.5A
2.5VDDS	MontaraGM	2.5V	2.12A
	(DDR, LVDSIO)		(2.07A, 0.05A)
	DDR RAM		1.046A(Idle) 1.692A (Run 3DMark)
	R5C551		0.13A
1.8VDDS	82541EI		0.22A
1.25VDDM	DDR RAM	1.25V	0.0769A
1.5VDDS	ICH4M (LAN)	1.5V	0.0155A
1.2VDDS	82541EI	1.2V	0.47A
1.5VDDA	ICH4M (SUS)	1.5V	0.0675A
3VDDM	ICH4M (IO)	3.3V	0.528A
	R5C551		0.13A
	MiniPCI		
	FWH BIOS		
	LPC KBC		0.0308A (Idle)
	AC97 CODEC		0.0461A (Idle)
	CLK GEN		0.36A
	LVDS		0.246A
3VDDS	ICH4M (LAN)	3.3V	0.0092A
	R5C551		
	MiniPCI		
	82540EM		0.15A
	PCMCIA VCCA		
3VDDA	ICH4M (SUS)	3.3V	0.165A
5VDDM	AMP2020		0.0615A (Idle) 0.338A (Run)
	CDROM		0.0461A (Idle) 0.677~0.8A(Run)
	HDD		0.0461A (Idle) 0.492A (Run)
	INT KB/ INT MS		
	INVERTER		0.0615A (Idle) 0.569A (Run)
5VDDS	PCMCIA VCCA		
5VDDA	ICH4M		10UA
	USB		
PMU3V	PMU08		0.0615A
PMU5V	ASIC_B0		0.0615A

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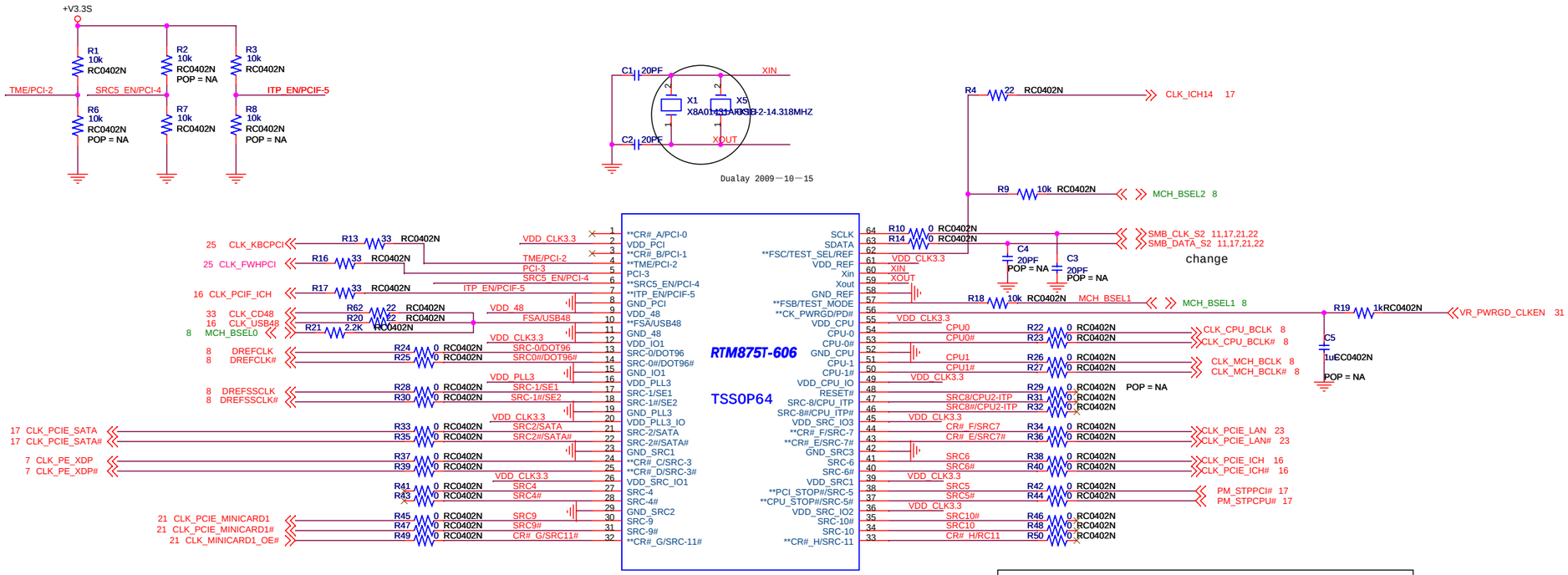
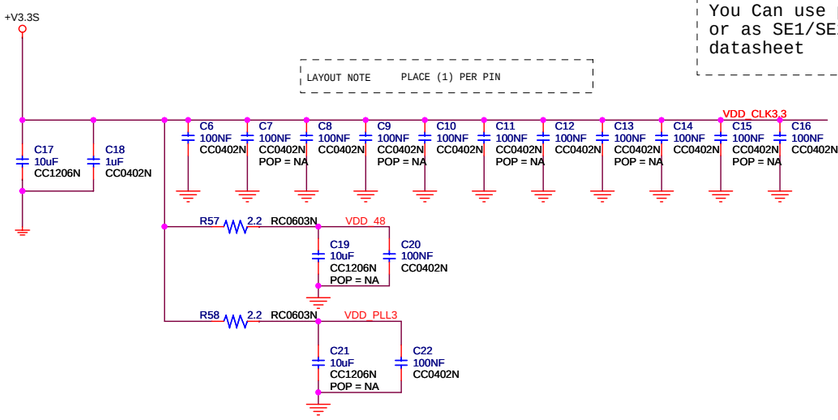
Title <Title>

Size	Sheet Name	Rev
C	Power_Budget	A

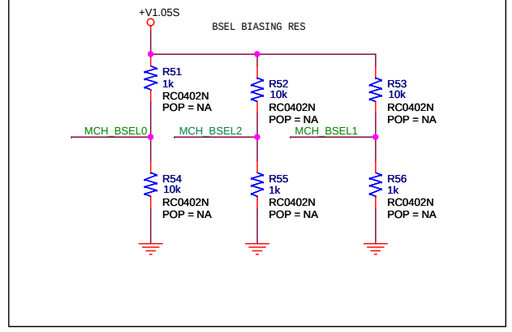
Date: Wednesday, November 04, 2009 Sheet 5 of 36

ENGINEER: Wain



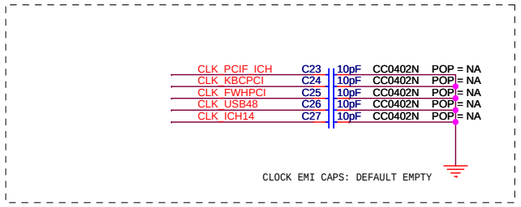


You Can use pin 24/25 either as SRC1T/SRC1C or as SE1/SE2. Details please reference the datasheet



FS_LC	FS_LB	FS_LA	CPU	SRC	PCI	DOT	REF	USB
Bit2	Bit1	Bit0	(MHz)	(MHz)	(MHz)	(MHz)	(MHz)	(MHz)
0	0	0	266.66	100.00	33.33	96.00	14.318	48.00
0	0	1	133.33	100.00	33.33	96.00	14.318	48.00
0	1	0	200.00	100.00	33.33	96.00	14.318	48.00
0	1	1	166.66	100.00	33.33	96.00	14.318	48.00
1	0	0	333.33	100.00	33.33	96.00	14.318	48.00
1	0	1	100.00	100.00	33.33	96.00	14.318	48.00
1	1	0	400.00	100.00	33.33	96.00	14.318	48.00
1	1	1	200.00	100.00	33.33	96.00	14.318	48.00

STRAP	MODE	STUFF	UNSTUFF
TME	NO OVERCLOCKING	R2 PULL UP	R4 PULLDOWN
	NORMAL	R4 PULLDOWN	R2 PULL UP
SRC5_EN	SRC5 ENABLED	R1 PULL UP	R5 PULLDOWN
	SRC5 DISABLED	R5 PULLDOWN	R1 PULL UP
ITP_EN	ITP ENABLED	R3 PULL UP	R6 PULLDOWN
	SRC8 ENABLED	R6 PULLDOWN	R3 PULL UP



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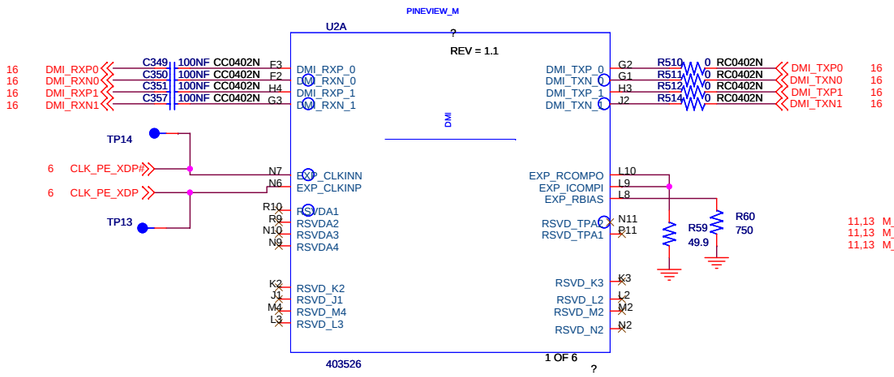
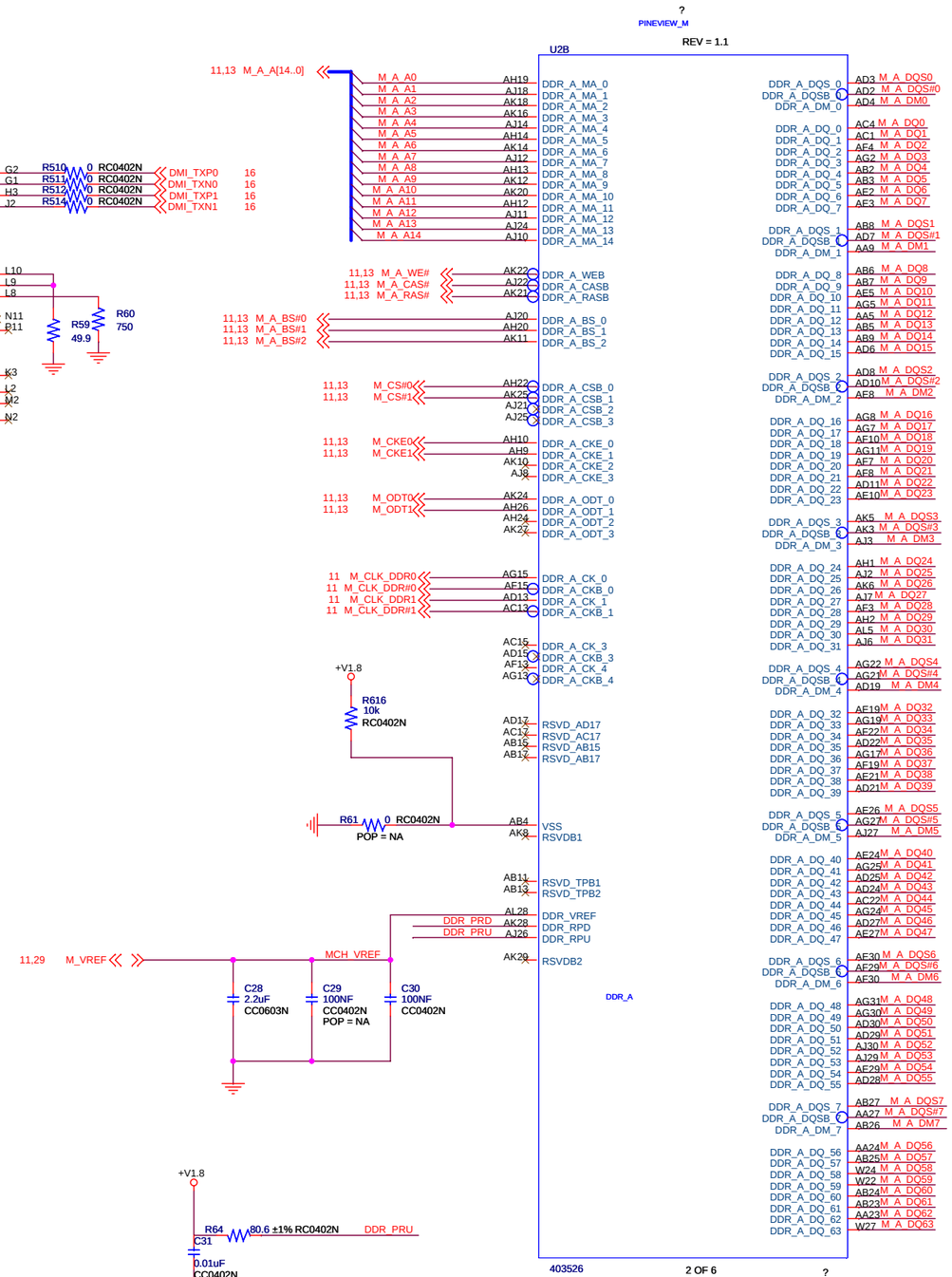
Title <Title>

Size	Sheet Name	Rev
C	Clock Generator	A

Date: Wednesday, November 04, 2009 Sheet 6 of 36





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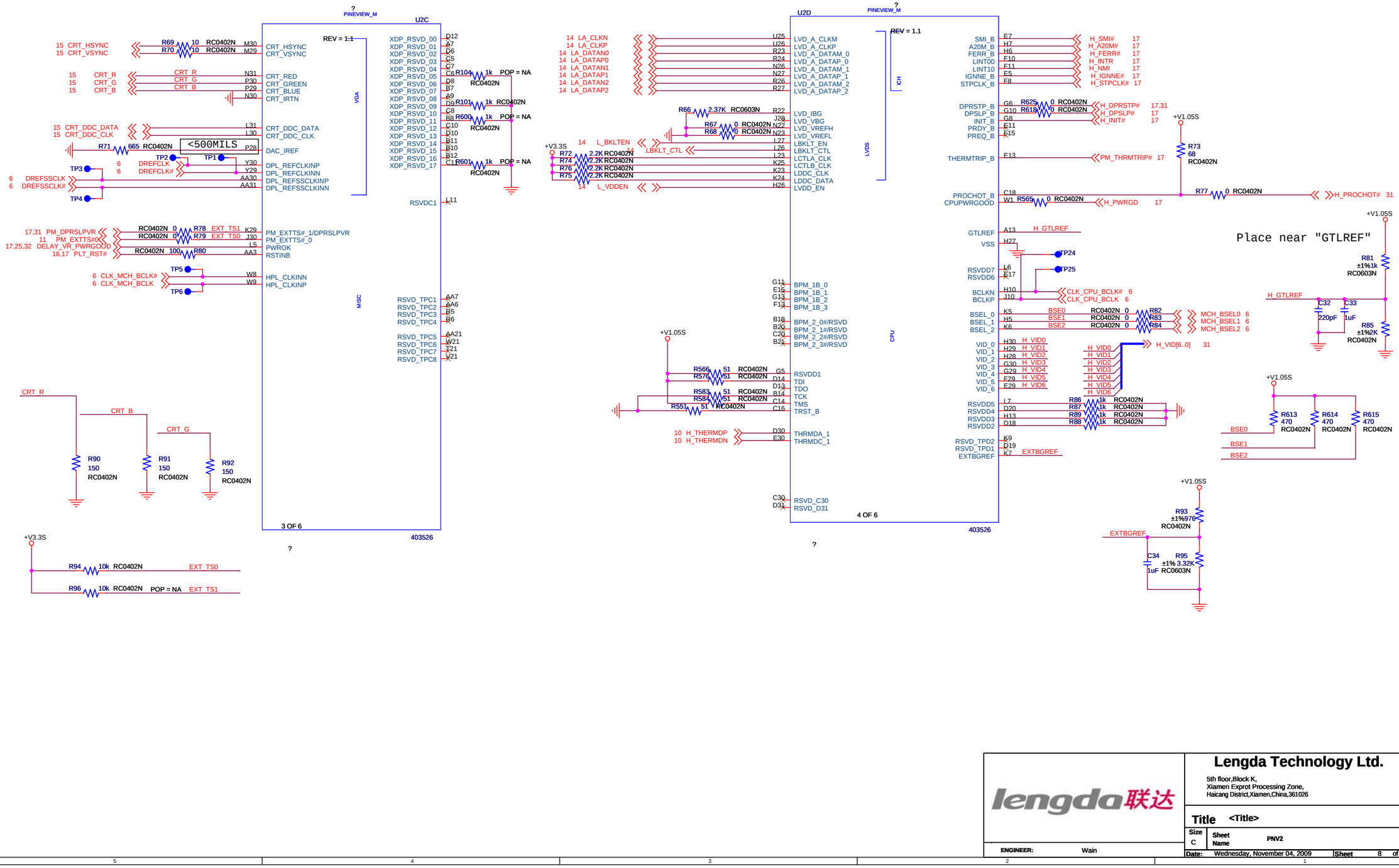
Title	<Title>		
Size C	Sheet Name PNV1		Rev A
ENGINEER: Wain	Date: Wednesday, November 04, 2009	Sheet 7 of 36	


U2C
PINEVIEW_M
REV = 1.1
VGA
MISC
3 OF 6
403526
U2D
PINEVIEW_M
REV = 1.1
LVDS
CH
CPU
4 OF 6
403526
<500MILS
Place near "GTLREF"
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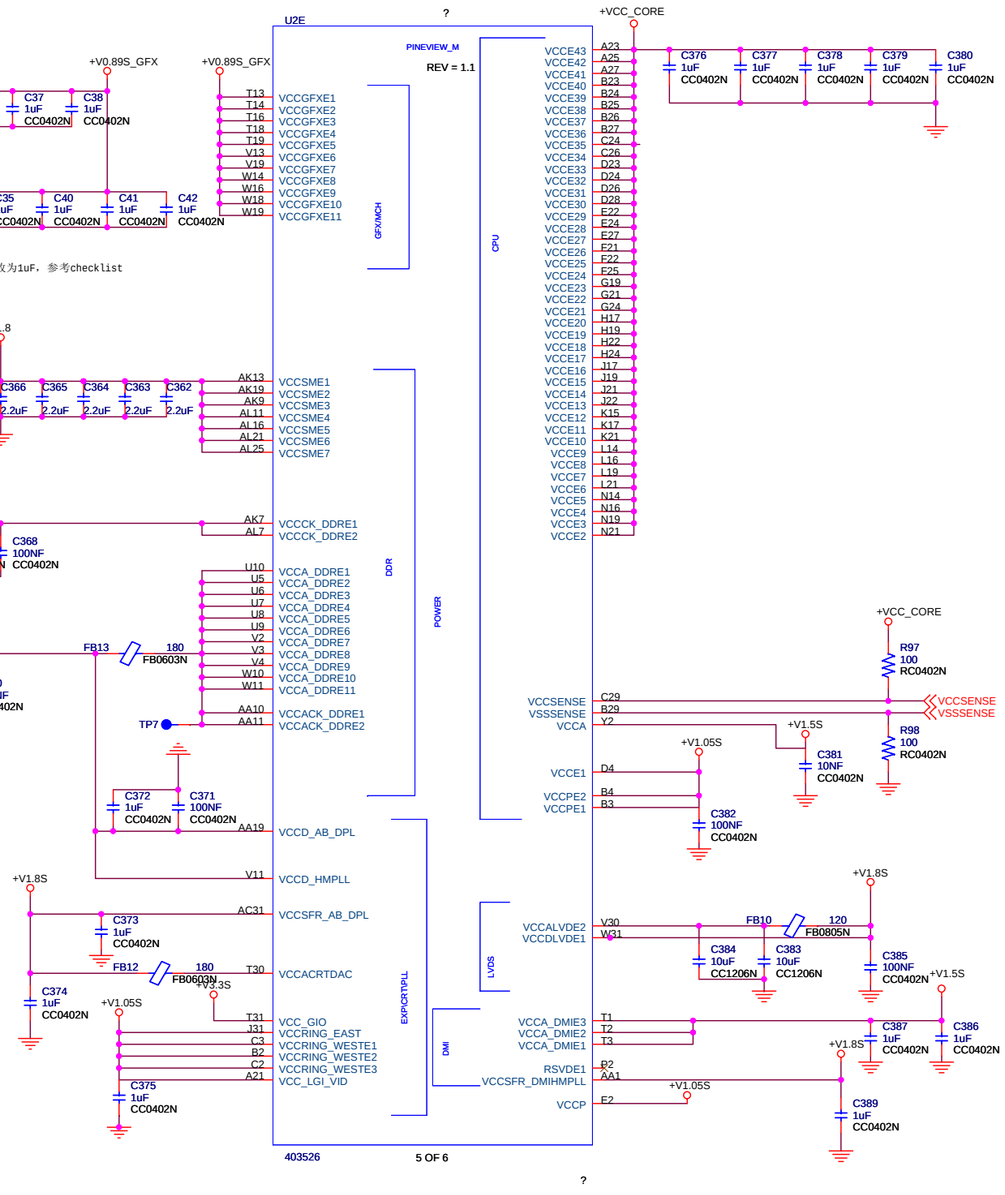
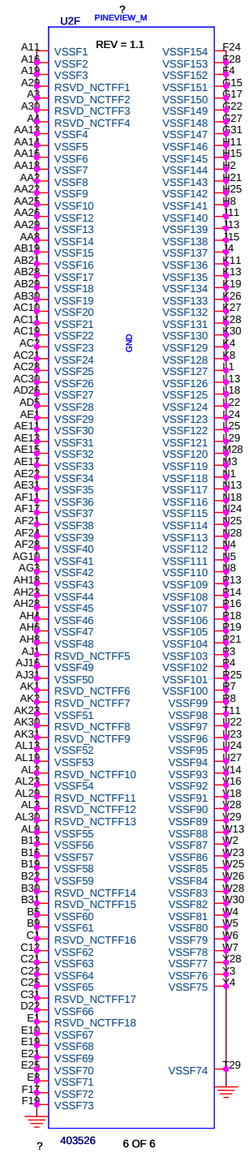
Haicang District,Xiamen,China,361026
Title <Title>
Size C
Sheet Name PNV2
Rev A
ENGINEER: Wain
Date: Wednesday, November 04, 2009
Sheet 8 of 36





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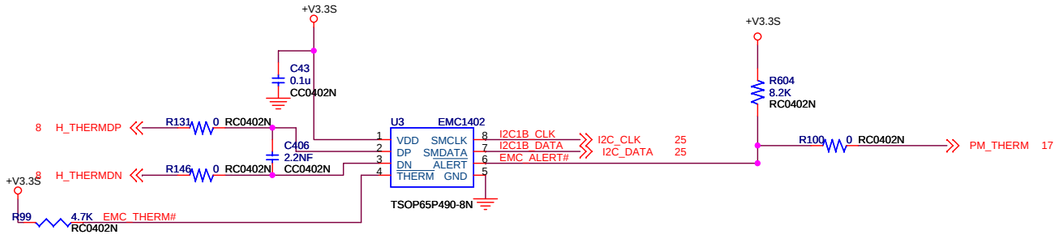
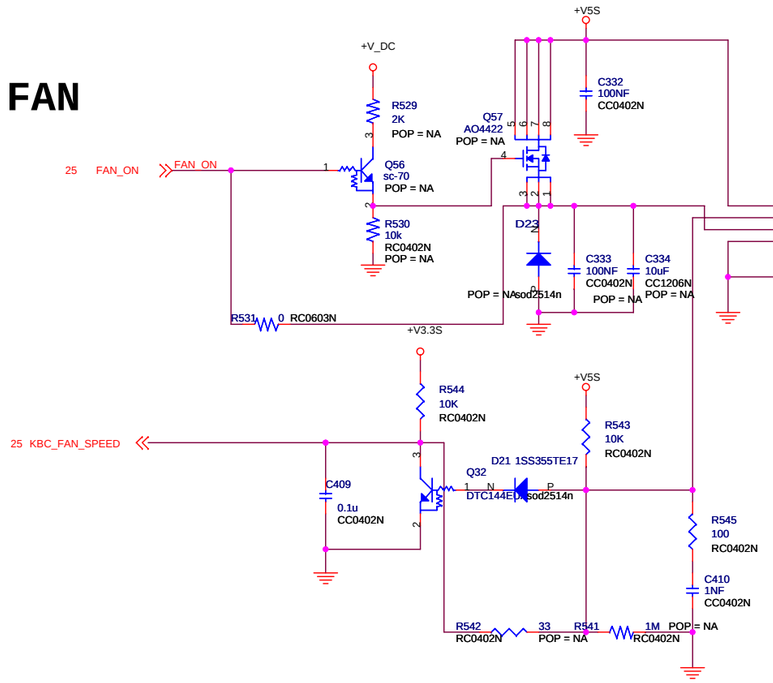
Title	<Title>		
Size C	Sheet Name PNV3		Rev A
Date: Wednesday, November 04, 2009	Sheet 9 of 36		
ENGINEER: Wain			



FAN



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ENGINEER: Wain	**Title** <Title>	
	Size C / Sheet Name Thermal&Fan	Rev A
	Date: Wednesday, November 11, 2009	Sheet 10 of 36

DDR2 SODIMM0

M_CLK_DDR0

C44 10pF CC0402N

Layout Note:
Place near SO-DIMM

M_CLK_DDR#0

M_CLK_DDR1

C50 10pF CC0402N

Layout Note:
Place near SO-DIMM

M_CLK_DDR#1

CN23A

7,13	M_CKE0	M_CKE0	79	CKE0	DQ0	5	M_A_DQ0
7,13	M_CKE1	M_CKE1	80	CKE1	DQ1	7	M_A_DQ1
					DQ2	17	M_A_DQ2
7	M_CLK_DDR0	M_CLK_DDR0	30	CK0	DQ3	19	M_A_DQ3
7	M_CLK_DDR#0	M_CLK_DDR#0	32	CK0#	DQ4	4	M_A_DQ4
					DQ5	6	M_A_DQ5
7	M_CLK_DDR1	M_CLK_DDR1	164	CK1	DQ6	16	M_A_DQ6
7	M_CLK_DDR#1	M_CLK_DDR#1	166	CK1#	DQ7	18	M_A_DQ7
					DQ8	23	M_A_DQ16
7,13	M_A_BS#[2..0]	M_A_BS#0	107	BA0	DQ9	25	M_A_DQ17
		M_A_BS#1	106	BA1	DQ10	35	M_A_DQ18
					DQ11	37	M_A_DQ19
7,13	M_A_A[14..0]	M_A_A0	102	A0	DQ12	20	M_A_DQ20
		M_A_A1	101	A1	DQ13	22	M_A_DQ21
		M_A_A2	100	A2	DQ14	36	M_A_DQ22
		M_A_A3	99	A3	DQ15	38	M_A_DQ23
		M_A_A4	98	A4	DQ16	41	M_A_DQ8
		M_A_A5	97	A5	DQ17	45	M_A_DQ9
		M_A_A6	94	A6	DQ18	55	M_A_DQ10
		M_A_A7	92	A7	DQ19	57	M_A_DQ11
		M_A_A8	93	A8	DQ20	49	M_A_DQ12
		M_A_A9	91	A9	DQ21	51	M_A_DQ13
		M_A_A10	105	A10/AP	DQ22	56	M_A_DQ14
		M_A_A11	90	A11	DQ23	58	M_A_DQ15
		M_A_A12	89	A12	DQ24	61	M_A_DQ24
		M_A_A13	116	A13	DQ25	63	M_A_DQ25
		M_A_A14	86	A14	DQ26	70	M_A_DQ26
			84	A15	DQ27	75	M_A_DQ27
		M_A_BS#2	85	A16_BA2	DQ28	62	M_A_DQ28
					DQ29	64	M_A_DQ29
7,13	M_CS#0	M_CS#0	110	S0#	DQ30	74	M_A_DQ30
7,13	M_CS#1	M_CS#1	115	S1#	DQ31	76	M_A_DQ31
					DQ32	123	M_A_DQ32
7,13	M_A_RAS#	M_A_RAS#	108	RAS#	DQ33	125	M_A_DQ33
7,13	M_A_CAS#	M_A_CAS#	113	CAS#	DQ34	135	M_A_DQ34
7,13	M_A_WE#	M_A_WE#	109	WE#	DQ35	137	M_A_DQ35
					DQ36	124	M_A_DQ36
R103	10k RC0402N	SA0_DIM1	198	SA0	DQ37	126	M_A_DQ37
R102	10k RC0402N	SA1_DIM1	200	SA1	DQ38	136	M_A_DQ38
					DQ39	138	M_A_DQ39
		M_A_DM0	10	DM0	DQ40	141	M_A_DQ40
7	M_A_DM[7..0]	M_A_DM2	26	DM1	DQ41	143	M_A_DQ41
		M_A_DM1	52	DM2	DQ42	151	M_A_DQ42
		M_A_DM3	67	DM3	DQ43	153	M_A_DQ43
		M_A_DM4	130	DM4	DQ44	140	M_A_DQ44
		M_A_DM5	147	DM5	DQ45	142	M_A_DQ45
		M_A_DM6	170	DM6	DQ46	152	M_A_DQ46
		M_A_DM7	185	DM7	DQ47	154	M_A_DQ47
					DQ48	157	M_A_DQ48
		M_A_DQS0	13	DQS_0	DQ49	159	M_A_DQ49
7	M_A_DQS[7..0]	M_A_DQS2	31	DQS_1	DQ50	172	M_A_DQ50
		M_A_DQS1	51	DQS_2	DQ51	174	M_A_DQ51
		M_A_DQS3	70	DQS_3	DQ52	158	M_A_DQ52
		M_A_DQS4	131	DQS_4	DQ53	160	M_A_DQ53
		M_A_DQS5	148	DQS_5	DQ54	171	M_A_DQ54
		M_A_DQS6	169	DQS_6	DQ55	173	M_A_DQ55
		M_A_DQS7	188	DQS_7	DQ56	175	M_A_DQ56
					DQ57	177	M_A_DQ57
		M_A_DQS#0	11	DQS_#0	DQ58	179	M_A_DQ58
7	M_A_DQS#[7..0]	M_A_DQS#2	29	DQS_#1	DQ59	181	M_A_DQ59
		M_A_DQS#1	49	DQS_#2	DQ60	180	M_A_DQ60
		M_A_DQS#3	68	DQS_#3	DQ61	182	M_A_DQ61
		M_A_DQS#4	129	DQS_#4	DQ62	192	M_A_DQ62
		M_A_DQS#5	146	DQS_#5	DQ63	194	M_A_DQ63
		M_A_DQS#6	167	DQS_#6			
		M_A_DQS#7	186	DQS_#7	SCL	197	SMB_CLK_S2
					SDA	195	SMB_DATA_S2
7,13	M_ODT0	M_ODT0	114	ODT0			
7,13	M_ODT1	M_ODT1	119	ODT1			

M_A_DQ[63..0] 7

SMB_CLK_S2 6,17,21,22
SMB_DATA_S2 6,17,21,22

P20

P21

DDR200-F521SB
SMD-DDR-60X760P-200N-R

E1 E2

+V1.8

C45 2.2uF CC0603N
C46 2.2uF CC0603N POP = NA
C47 2.2uF CC0603N
C48 2.2uF CC0603N POP = NA
C49 2.2uF CC0603N

+V1.8

C51 100NF CC0402N
C52 100NF CC0402N POP = NA
C53 100NF CC0402N
C56 100NF CC0402N POP = NA

+V1.8

C57 100NF CC0402N
C58 100NF CC0402N POP = NA
C59 100NF CC0402N
C60 100NF CC0402N POP = NA

+V1.8

CN23B

112	VDD_01	VSS16	18
111	VDD_02	VSS17	34
117	VDD_03	VSS18	41
96	VDD_04	VSS19	53
95	VDD_05	VSS20	62
118	VDD_06	VSS21	54
81	VDD_07	VSS22	59
82	VDD_08	VSS23	65
87	VDD_09	VSS24	60
103	VDD_10	VSS25	66
88	VDD_11	VSS26	127
104	VDD_12	VSS27	139
		VSS28	128
199	VDDSPD	VSS29	145
		VSS30	165
83	NC1	VSS31	171
120	NC2	VSS32	172
50	NC3	VSS33	177
69	NC4	VSS34	187
163	NCTEST	VSS35	178
		VSS36	190
1	VREF	VSS37	3
		VSS38	31
		VSS39	33
		VSS40	155
		VSS41	44
		VSS42	132
47	VSS1	VSS43	144
133	VSS2	VSS44	156
183	VSS3	VSS45	168
7	VSS4	VSS46	2
12	VSS5	VSS47	7
48	VSS6	VSS48	15
184	VSS7	VSS49	17
76	VSS8	VSS50	39
71	VSS9	VSS51	149
72	VSS10	VSS52	161
121	VSS11	VSS53	28
122	VSS12	VSS54	40
194	VSS13	VSS55	138
193	VSS14	VSS56	150
8	VSS15	VSS57	162

+V3.3S

C54 2.2uF CC0603N
C55 100NF CC0402N

8 PM_EXTTS#0

7,29 M_VREF

C61 2.2uF CC0603N POP = NA
C62 100NF CC0402N

DDR200-F521SB
SMD-DDR-60X760P-200N-R

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Title <Title>

Size	Sheet Name	Rev
C	DDR2_SODIMM2	A

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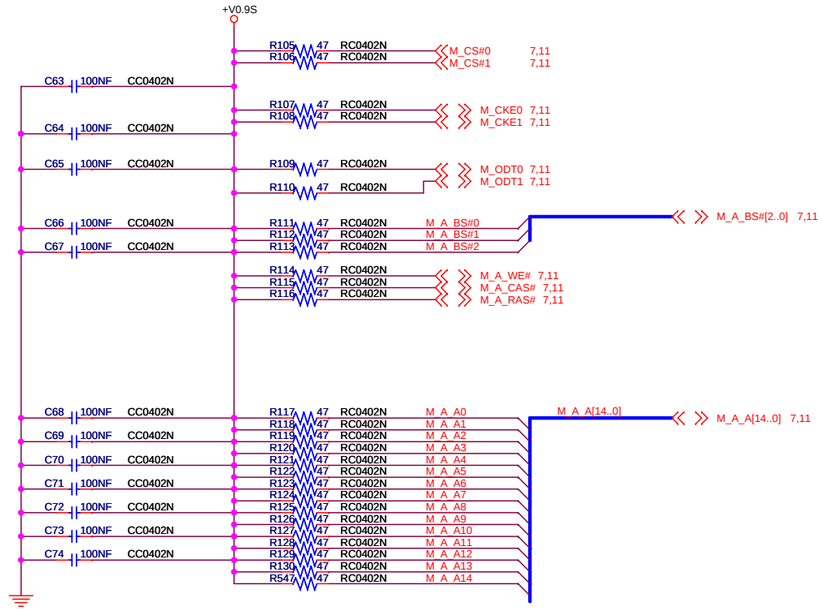
DDR2 Termination

Layout note:
Place one cap close to every 2 pullup resistors teminated to +0.9S



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ENGINEER: Wain	**Title** <Title>	
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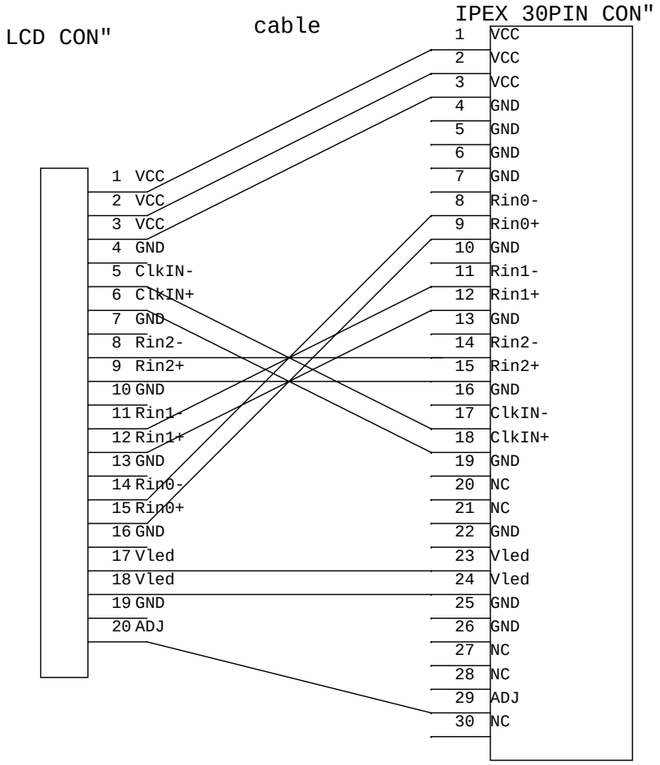
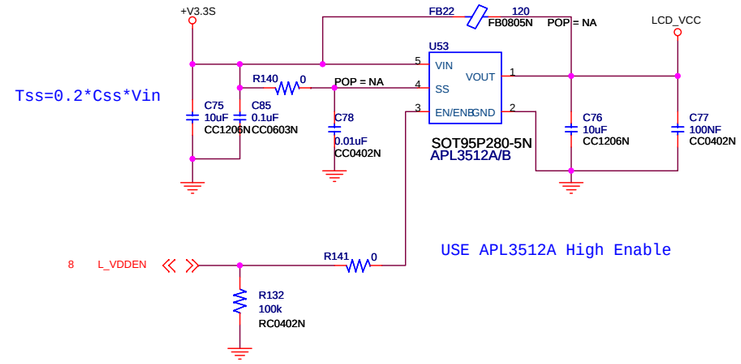
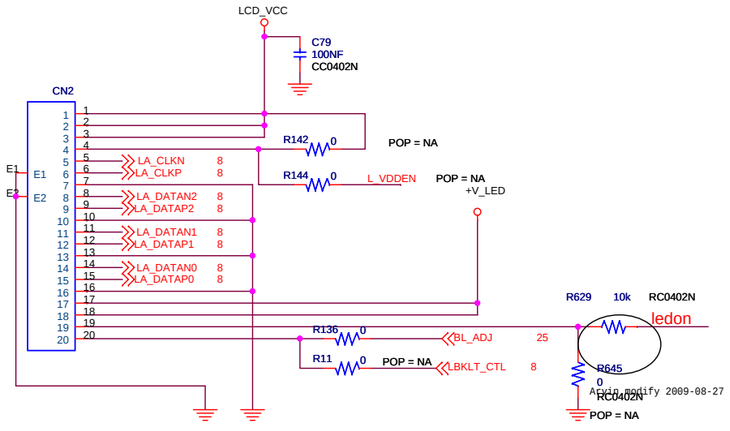
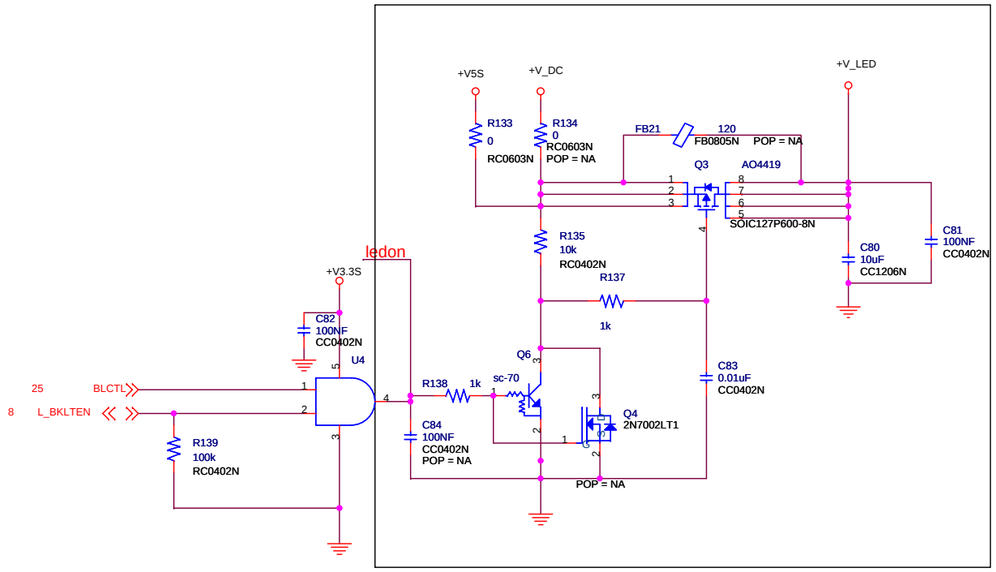
LVDS Connector









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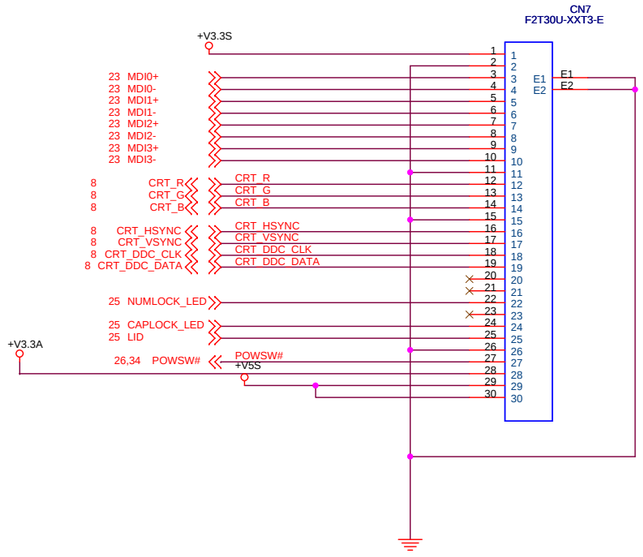

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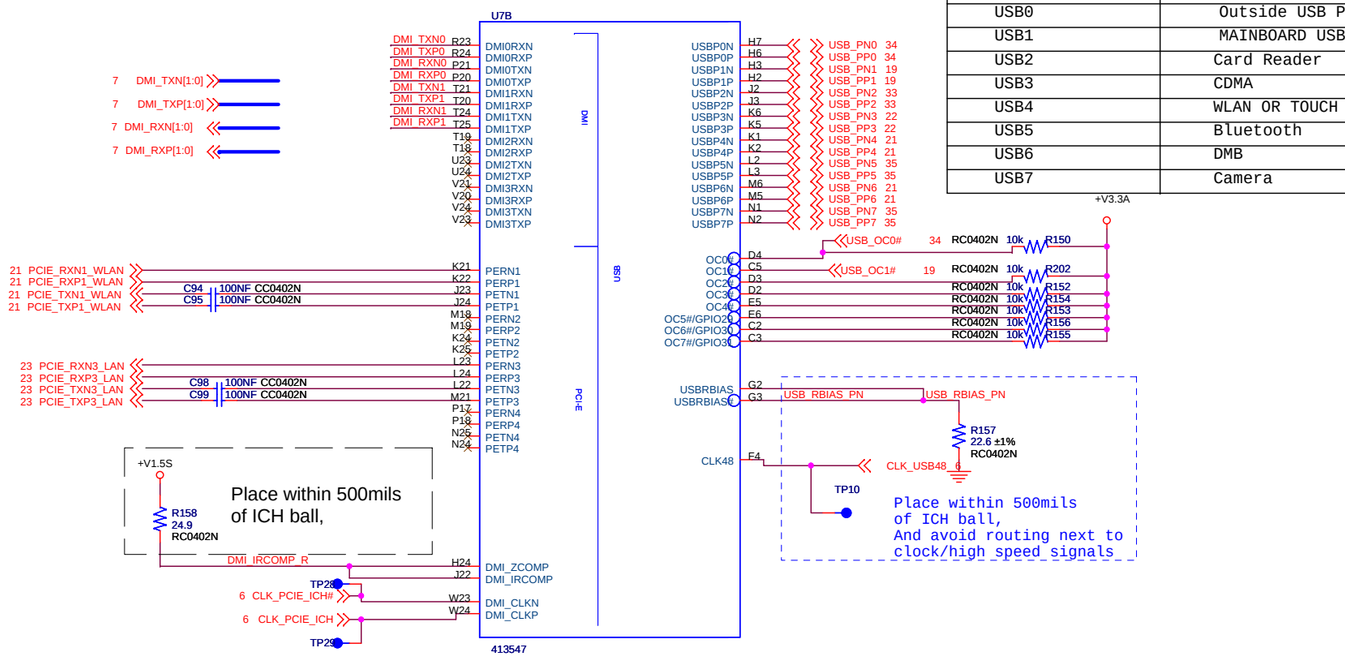
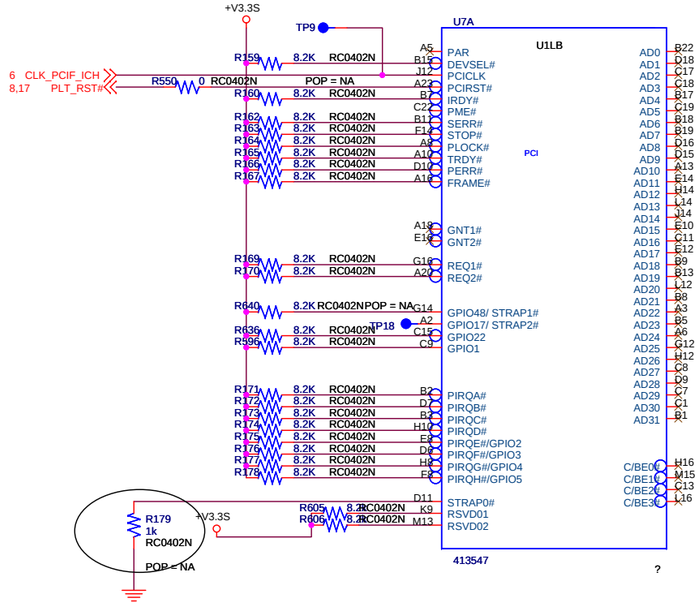
USN PORT	USED FOR
USB0	Outside USB PORT
USB1	MAINBOARD USB PORT
USB2	Card Reader
USB3	CDMA
USB4	WLAN OR TOUCH SCREEN
USB5	Bluetooth
USB6	DMB
USB7	Camera





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Title <Title>

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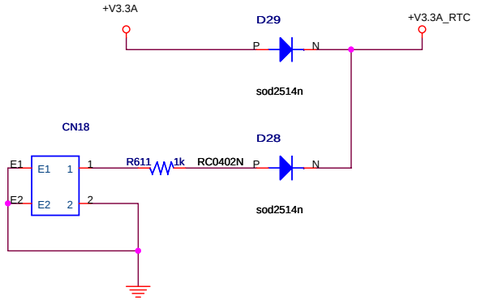
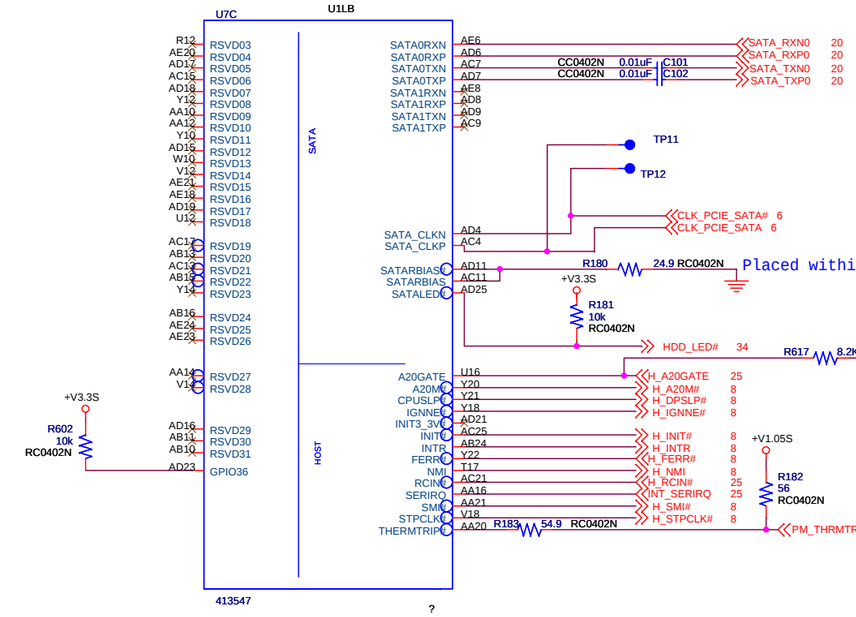
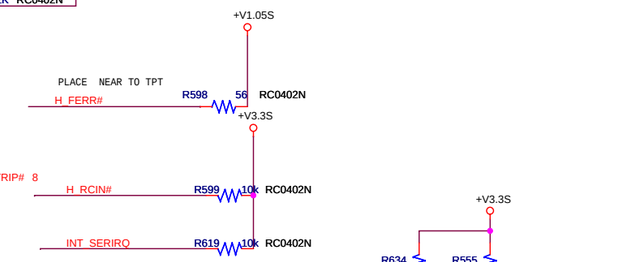
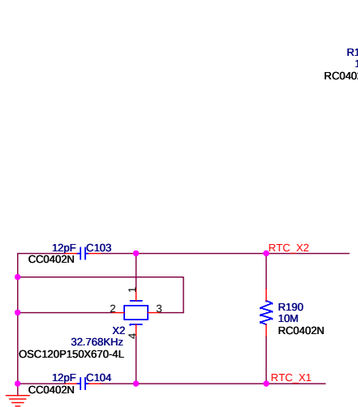
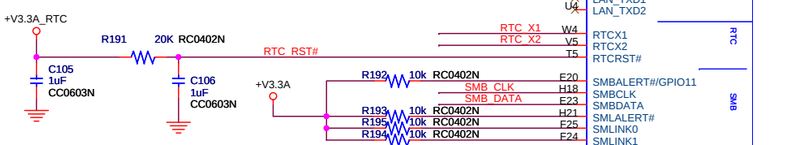
ENGINEER: Wain

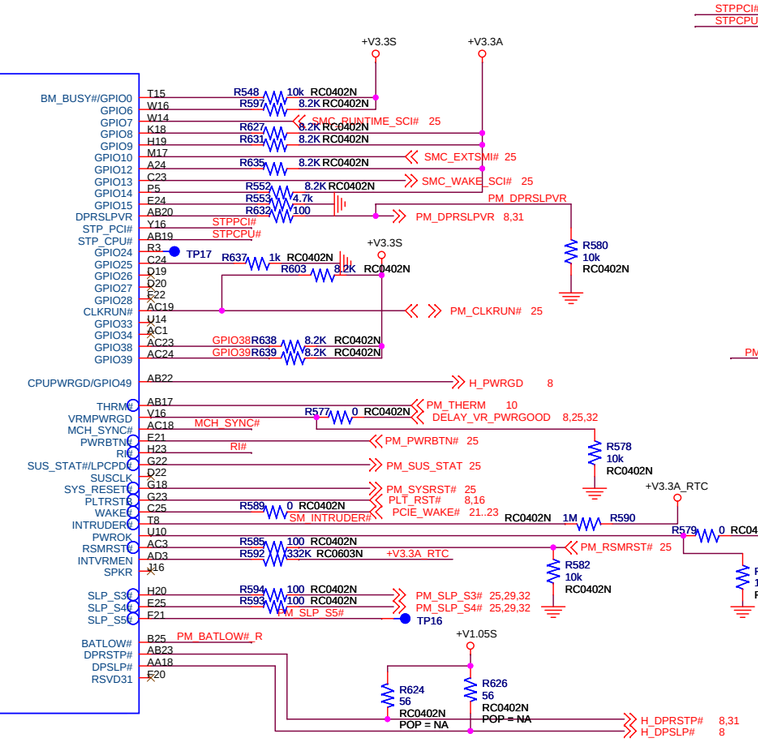


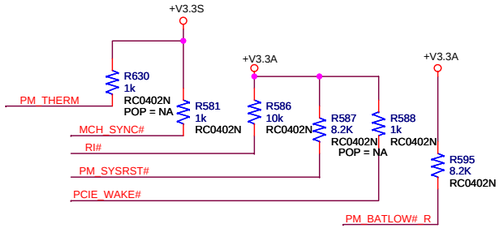


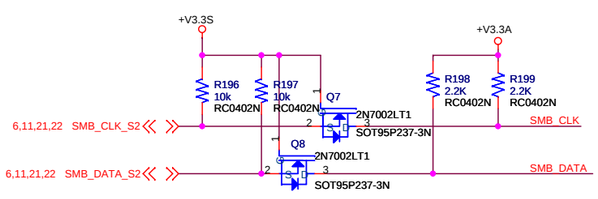


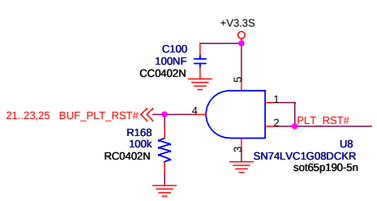












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Title <Title>

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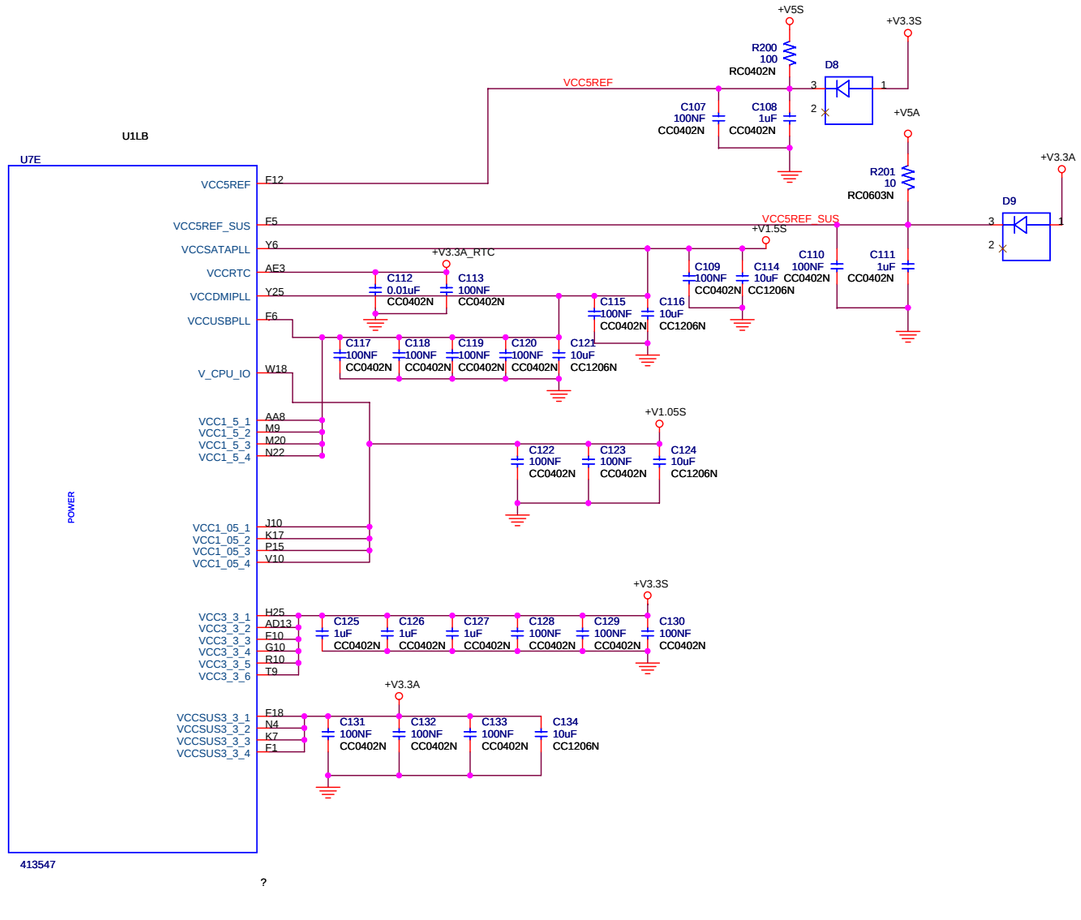

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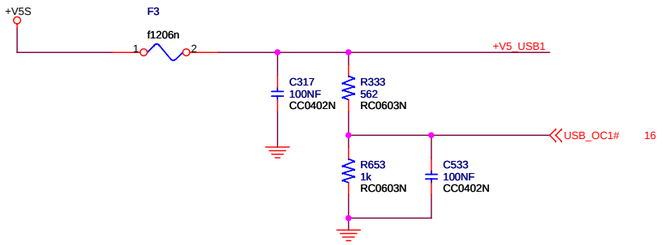
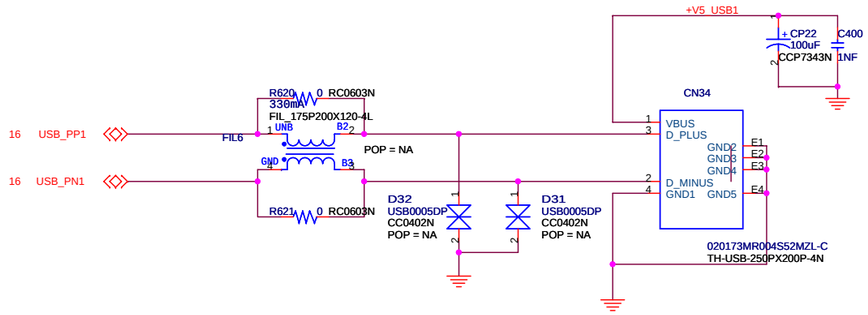
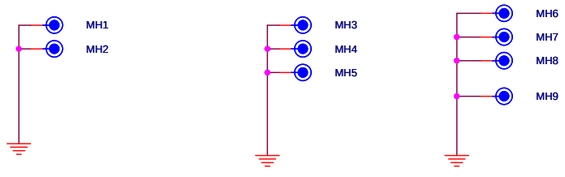
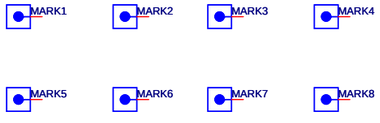
USB

USB Port3









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Title	<Title>	
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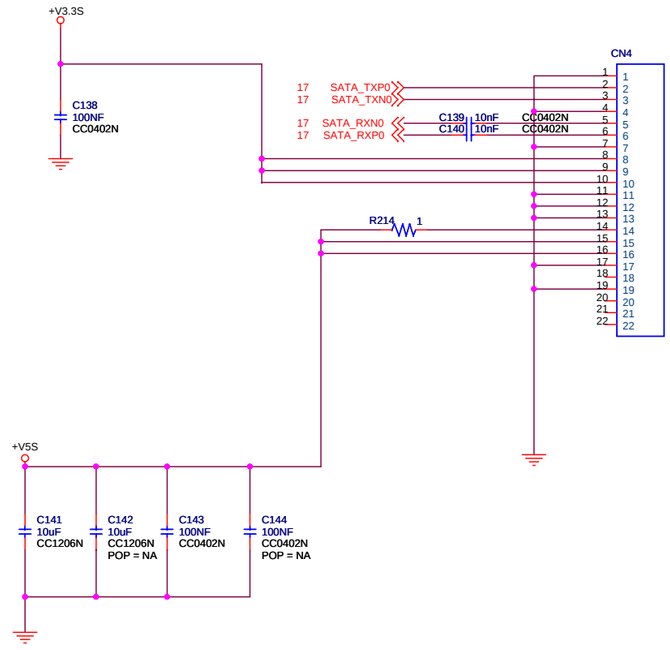

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Title	<Title>	
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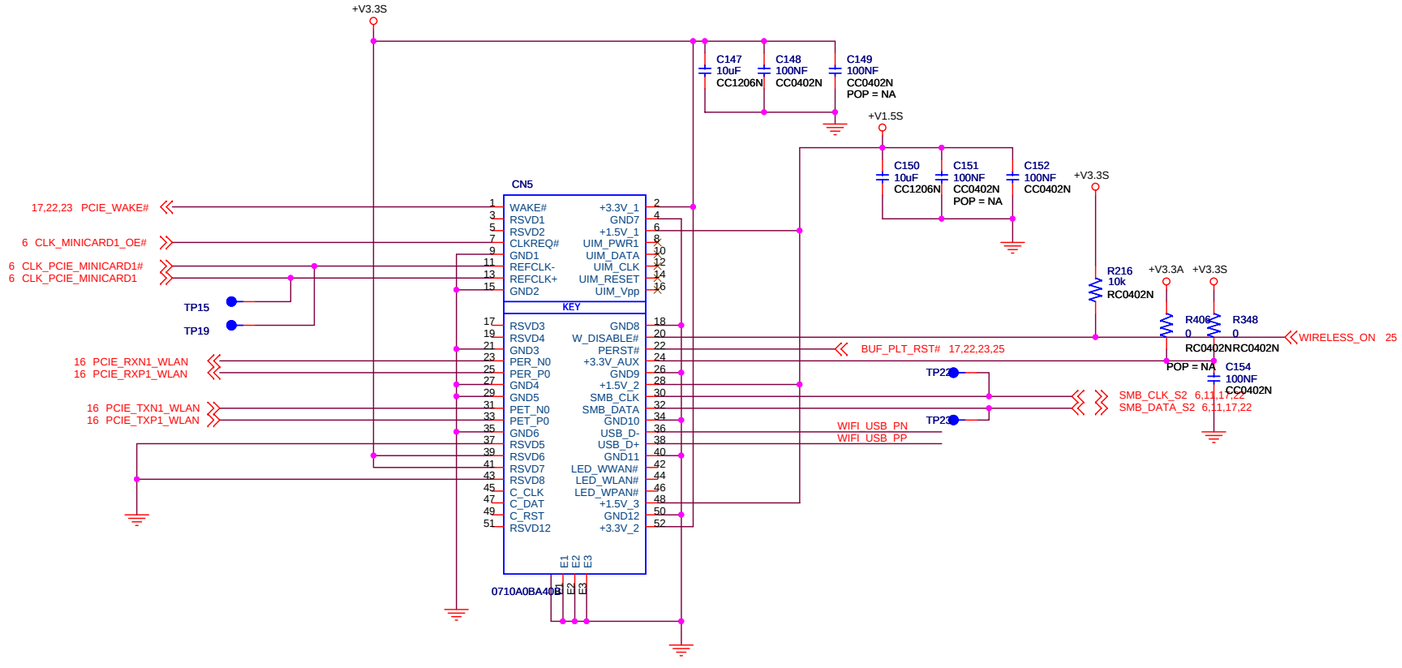
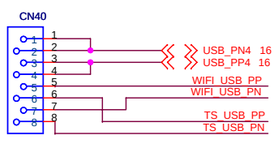
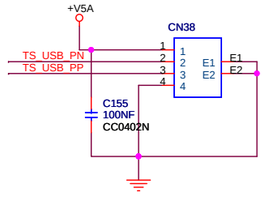
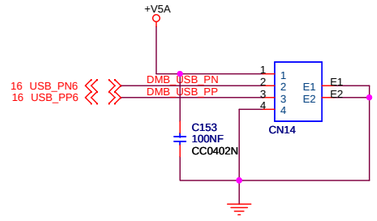
Minicard









Add Touchscreen connector (use an usb port with wifi) & dmb connector 2009-10-15

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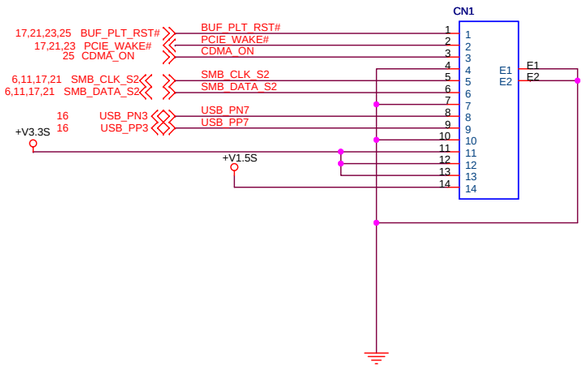
CDMA



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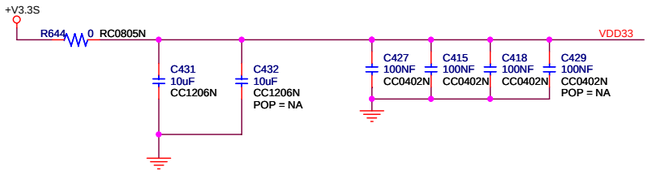
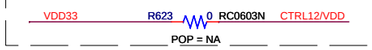


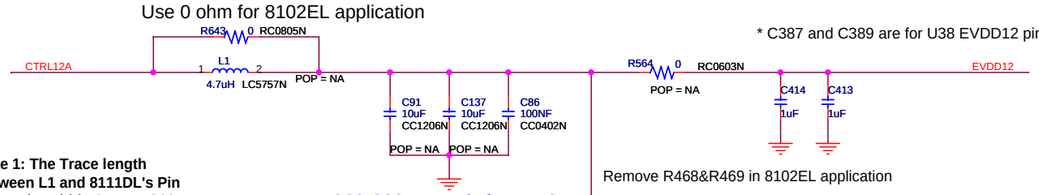
C341 C353 C381 C376 are for 8111DL VDD33 pins-- 1, 29, 37, 40.

C341 C353 C381 are for 8102EL VDD33 pins-- 1, 29, 37.

For RTL8111DL, use this block



Use 0 ohm for 8102EL application

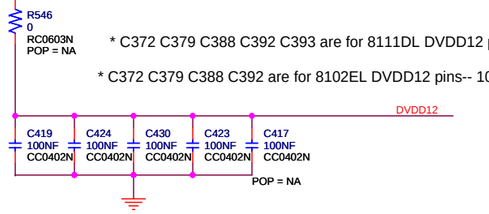


* C387 and C389 are for U38 EVDD12 pin 19.

Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C29 and C54 to L8 must be within 0.5cm. Refer to Layout guide for more detail.

Remove R468&R469 in 8102EL application

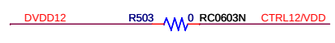
C29 C32 are only for RTL8111DL.

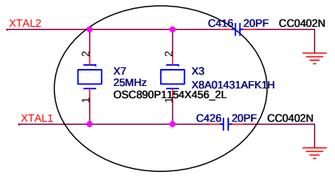


* C372 C379 C388 C392 C393 are for 8111DL DVDD12 pins-- 10, 13, 30, 36, 39.

* C372 C379 C388 C392 are for 8102EL DVDD12 pins-- 10, 13, 30, 36.

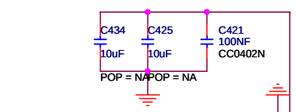
For RTL8102EL, use this block.





Dualay 2009—10—15

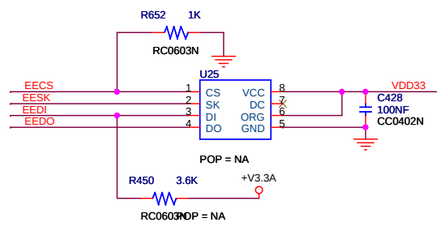
C344 C346 are only for 8111DL

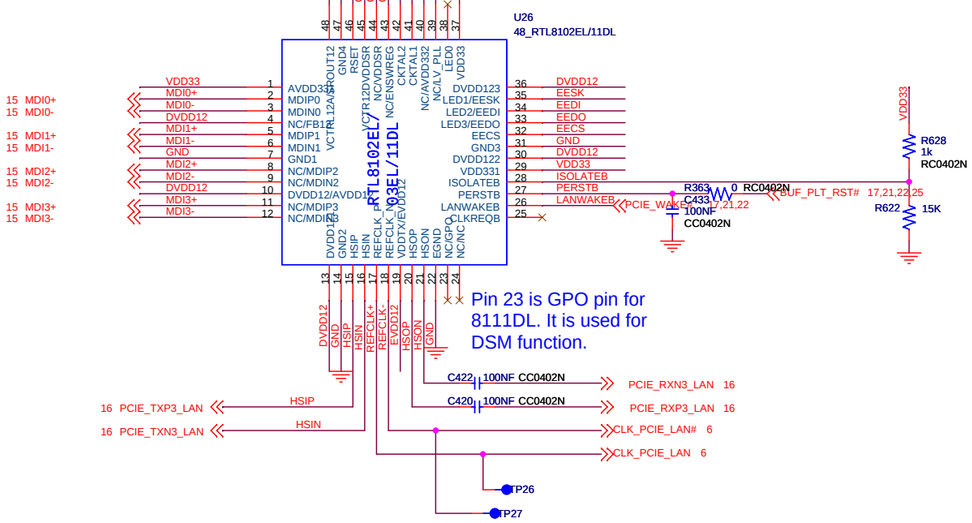


Remove R423 and R426 for RTL8102EL application.
R423 and R426 are used in the RTL8111DL application.
Remove R426 if switching regulator is enabled. Remove R423 if external power 1.2V is used.

R433 value should be 2.49K (1%) for all application.

R461 is only required by RTL8102EL





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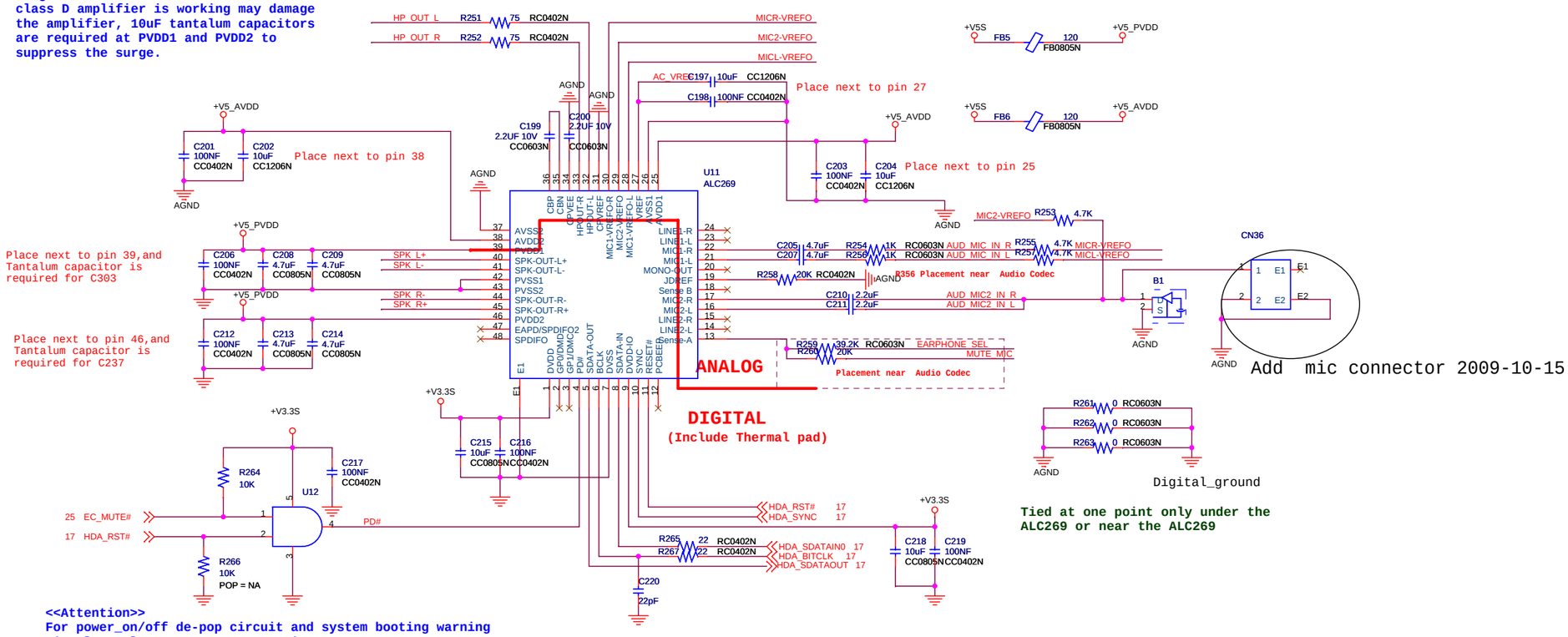
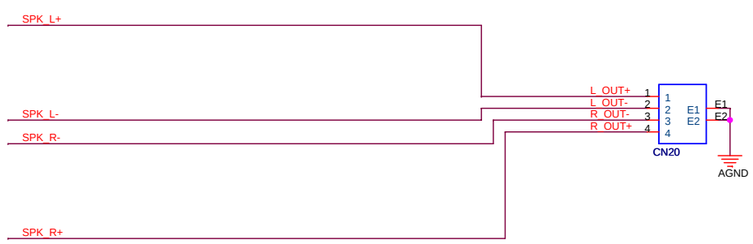
<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

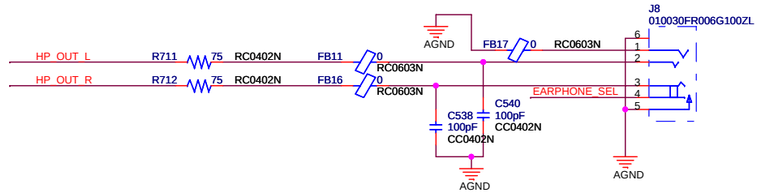


<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High first.
2.When you want to exit your Bios Programming Code, please let the EC_MUTE# Low.(The programming is different from before .)

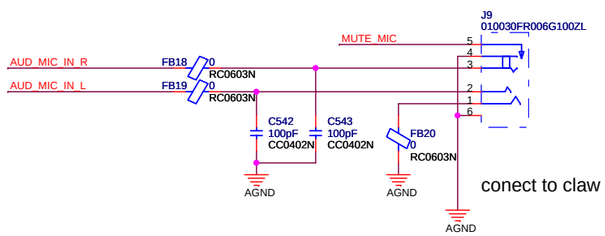
PD#=0V : Power down Class D SPK amplifer

PD#=3.3V : Power up Class D SPK amplifer





<<Attention>>
If mount the LC filter((L9~L12;C295/C299;C300/C293/C294/C296),Please let them togather and close to codec. If the PCB trace and Speaker wire length is less than 20cm, don't need the LC filter(L9~L12;C295/C299) to eliminate the EMI,If L9,L0,L11,L12 are replaced by 0 ohm/1.6A resistetor(please don't use general bead, because it may influence the THD+N quality) ,and C295,C299 should be NC.And,please make the trace length/ Speaker wire length of SPKL+/L-/R+/R- be the same as possible as you can.
C300/C293/C294/C296 are reserved for EMI fine-tune ; For EMI issue, please also refer our ALC269 Layout guide document



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IT8502E/F/G(JX)

Layout Note:
Recommended net "+V3.3A" and "+V3.3A_RTC" minimum trace width 12mils.

Add LINUX POWER SWITCH 2009-10-15

Please do not place any pull-up resistor on GPG0, GPG2, and GPG6 (Reserved hardware strapping).

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

ITE Modify

LPC debug Port

KBC Debug Port

Serial Debug Port

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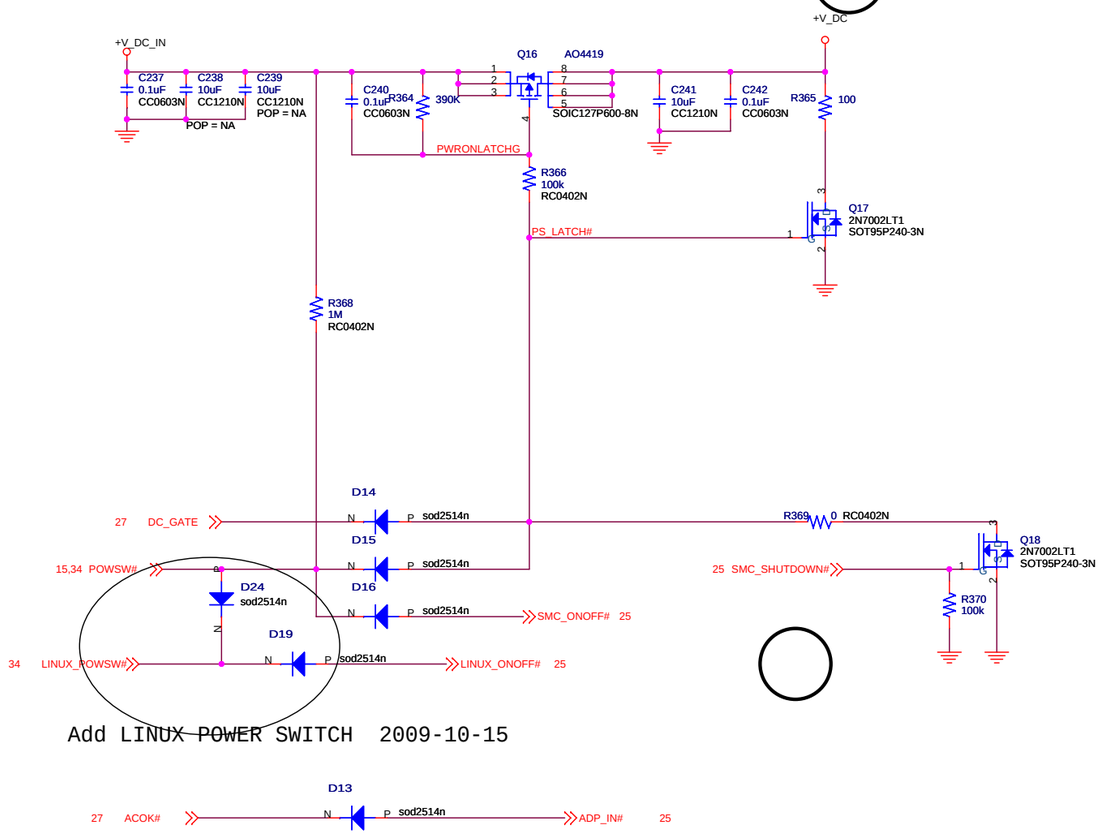
Sheet Name	KBC
Rev	A
ENGINEER:	Wain
Date:	Wednesday, November 11, 2009
Sheet	25 of 36

Power Button Detect & Latch

Power Sequence

05



Add LINUX POWER SWITCH 2009-10-15

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Size	C
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Power Sequence

1AC

Layout NOTE:
The AGND_CHG connect to
GND through E1 pin;
by via only!

AC current limit: 3.64A

Charge current:2.02A

TI Tony Modify!

Please near to the IC

Close to IC

Set Vacdet must be 2.4V

和M11A保持一致，采用19V~20V适配器

后续增加 09-10-28

Ichg=((VCH/VREF)*(0.1/Rsr)=1.18A
Set charge current about 1.18A
Set prechg current about 111.349MA

Iac=(VAC/VREF)*(0.1/Rac)=2.5A

Isyn set 303MA?

t<0度或t>45度，Ichg=0
0<t<15度，Ichg= 0.325A
15度<t<45度，Ichg=1.18A

Set the default 4.2V per cell

Set the 2 Cells

Place near to the IC

Battery Connector

?????长pin电源有无问题

根据飞毛腿要求，更改次序。

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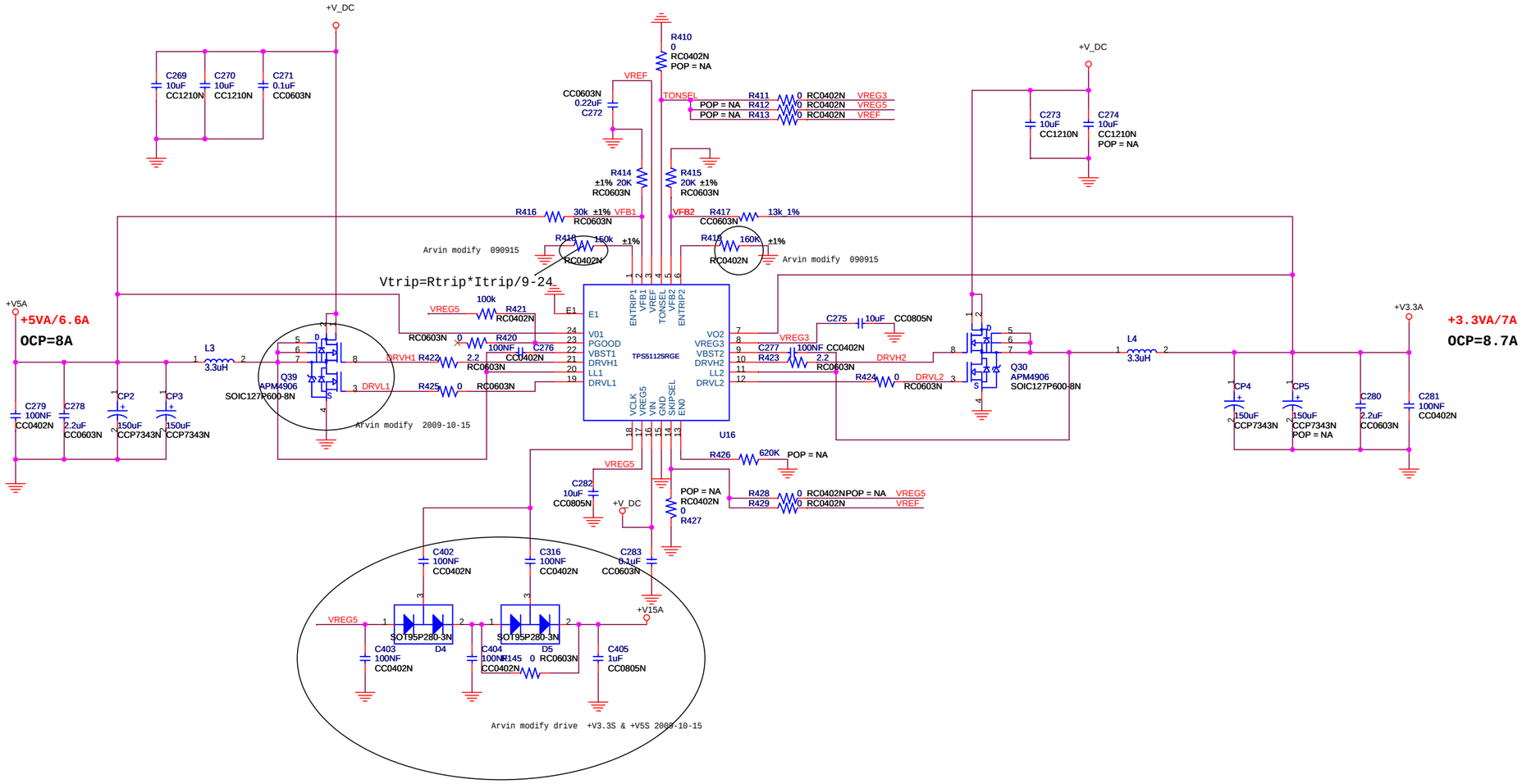
		Title <Title>	
		Size C / Sheet Name: Power_charger&Battery CONN	Rev A
		Date: Wednesday, November 04, 2009	Sheet 27 of 36



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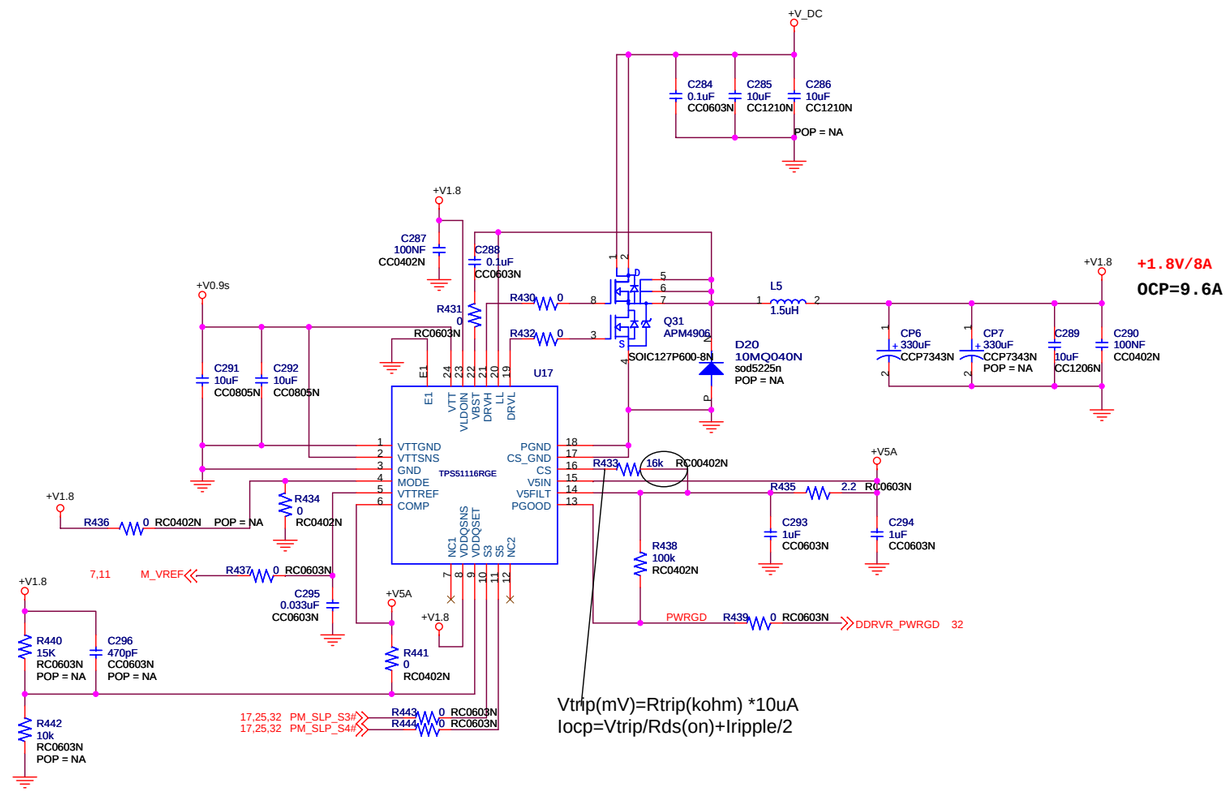
Title	<Title>	
Size C	Sheet Name: Power_+V5A&+V3.3A	Rev A
Date: Wednesday, November 04, 2009	Sheet 28 of 36	

MODE	DISCHARGE MODE
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge



S3 & S5 Control

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF(HI-Z)
S4/S5	LO	LO	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

VDDQSET	VDDQ (V)	VTTREF & VTT	NOTE
GND	2.5	VDDQSNS/2	DDR
V5IN	1.8	VDDQSNS/2	DDR2
FB Resistors	Adjustable	VDDQSNS/2	1.5V< VDDQ<3V

(100*VDDQ-75)kohm

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Title <Title>

Size	Sheet Name	Rev
C	Power_+v1.8	A

ENGINEER: Wain

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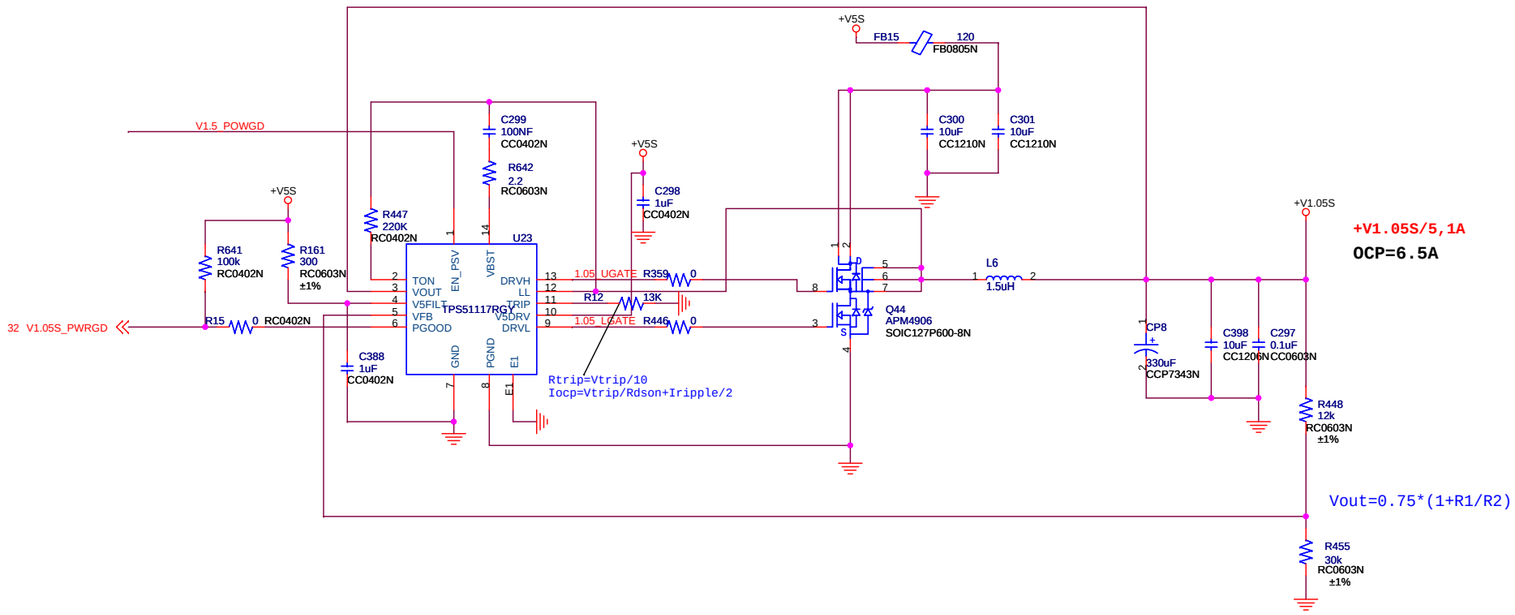

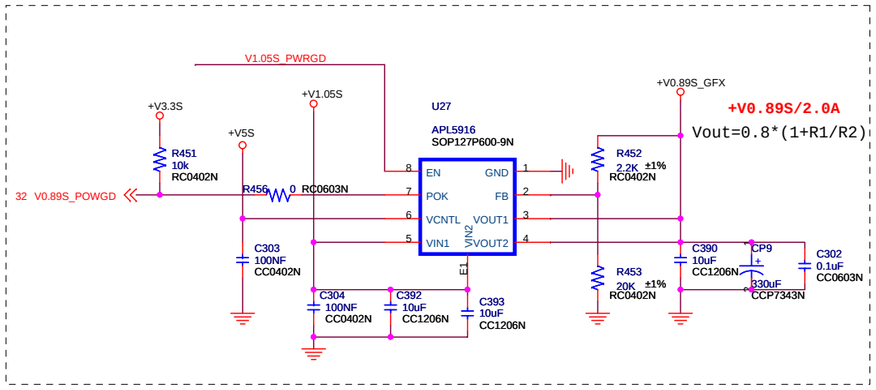

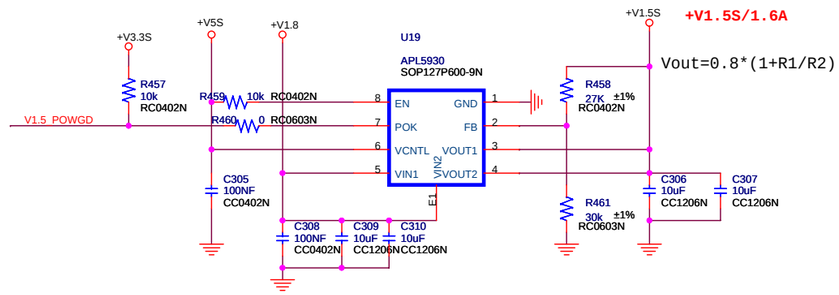

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Title	<Title>	
Size C	Sheet Name: Power_+V1.5S&+V2.5S	Rev A
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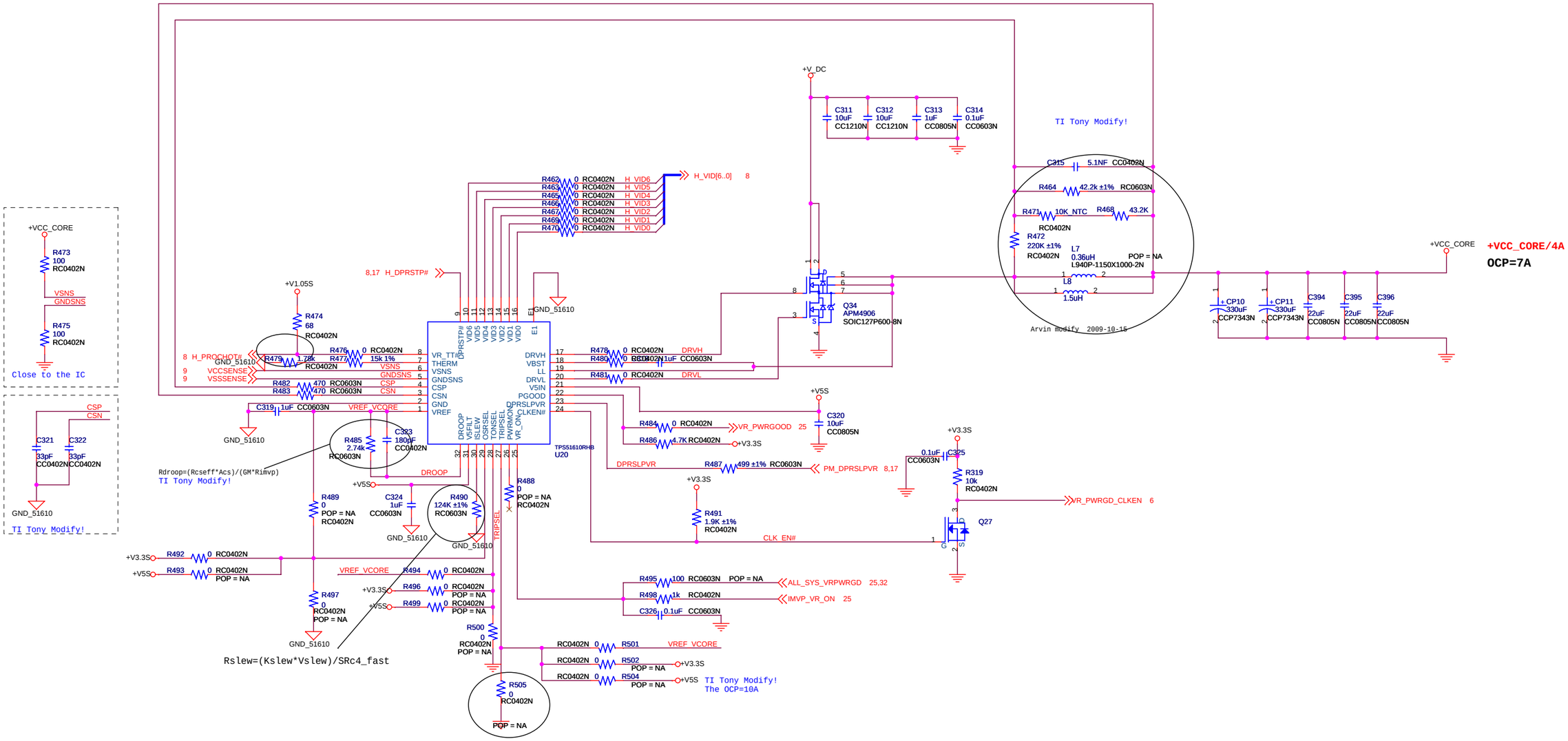

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Title	<Title>
Size C	Sheet Name: Power_V_CPU_CORE
Rev A	
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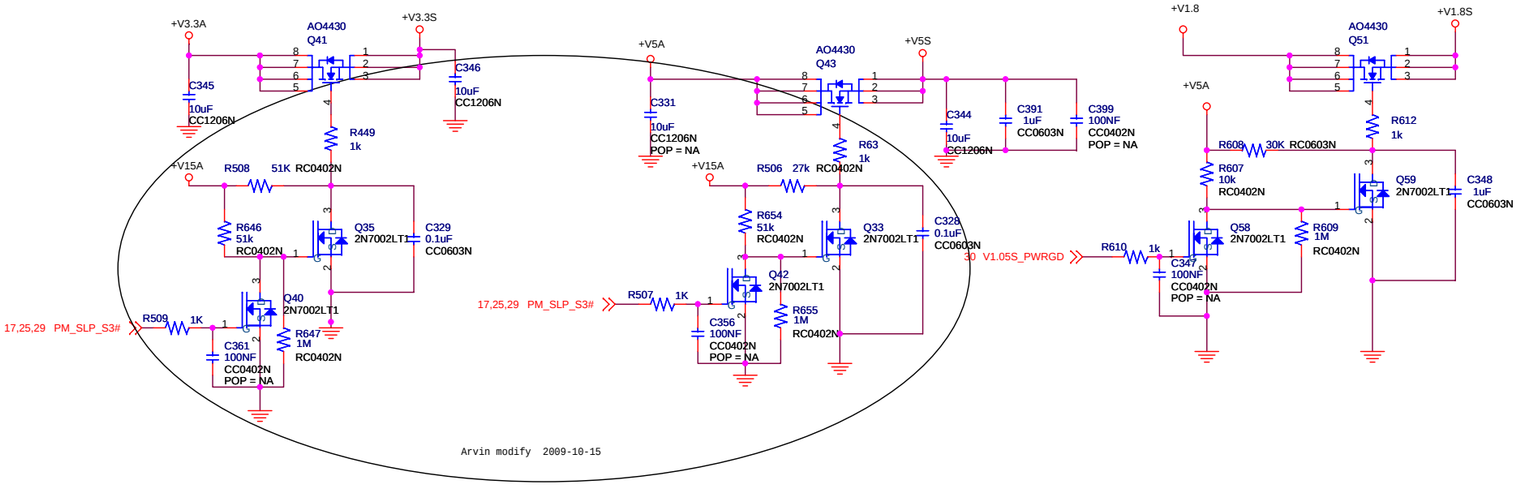
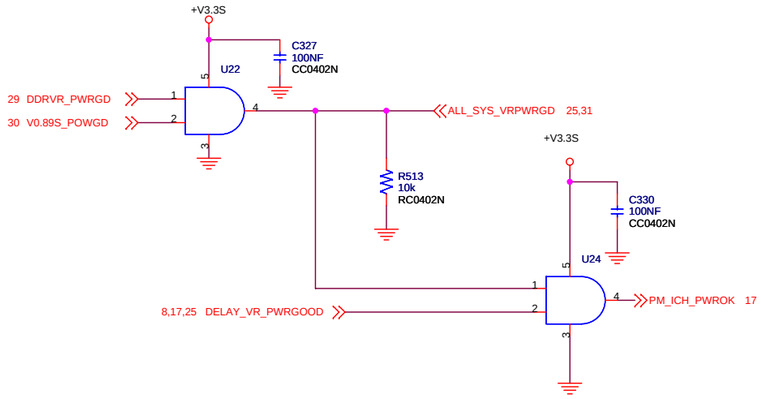
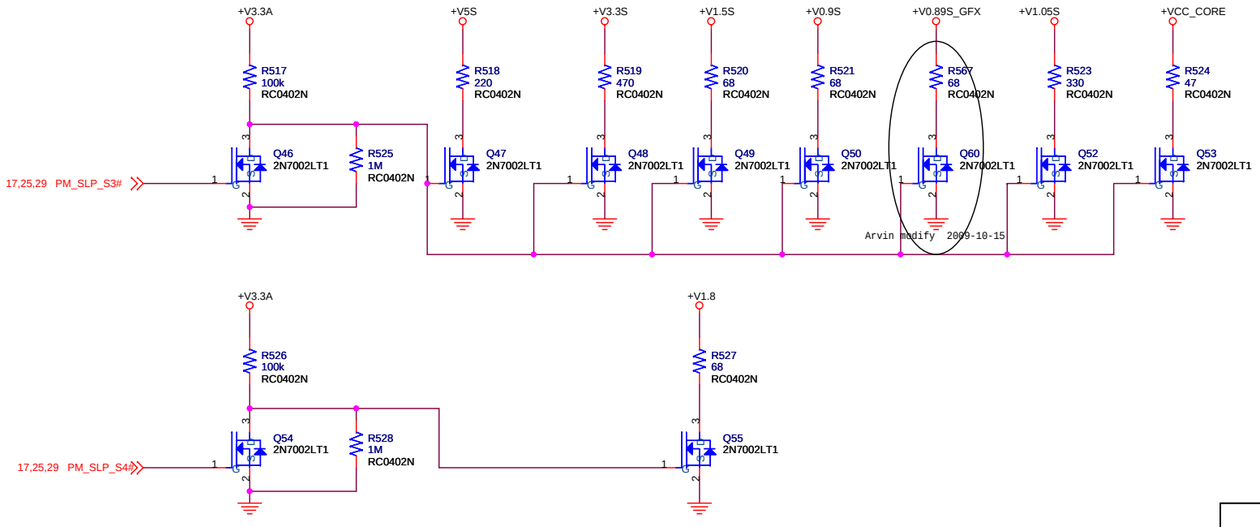
S3 /S4 Power control



Power Good



Power Discharge Circuit



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Title	<Title>	
Size C	Sheet Name: Power_S3_S4/Power Good	Rev A
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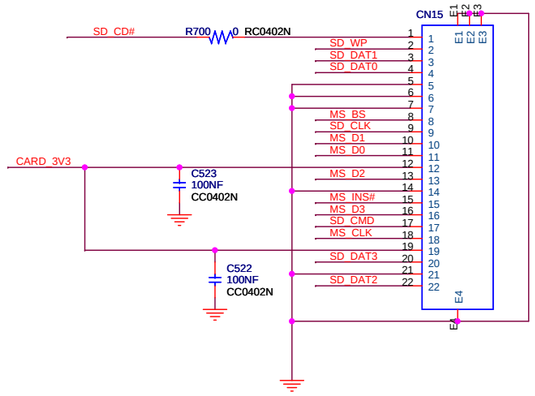
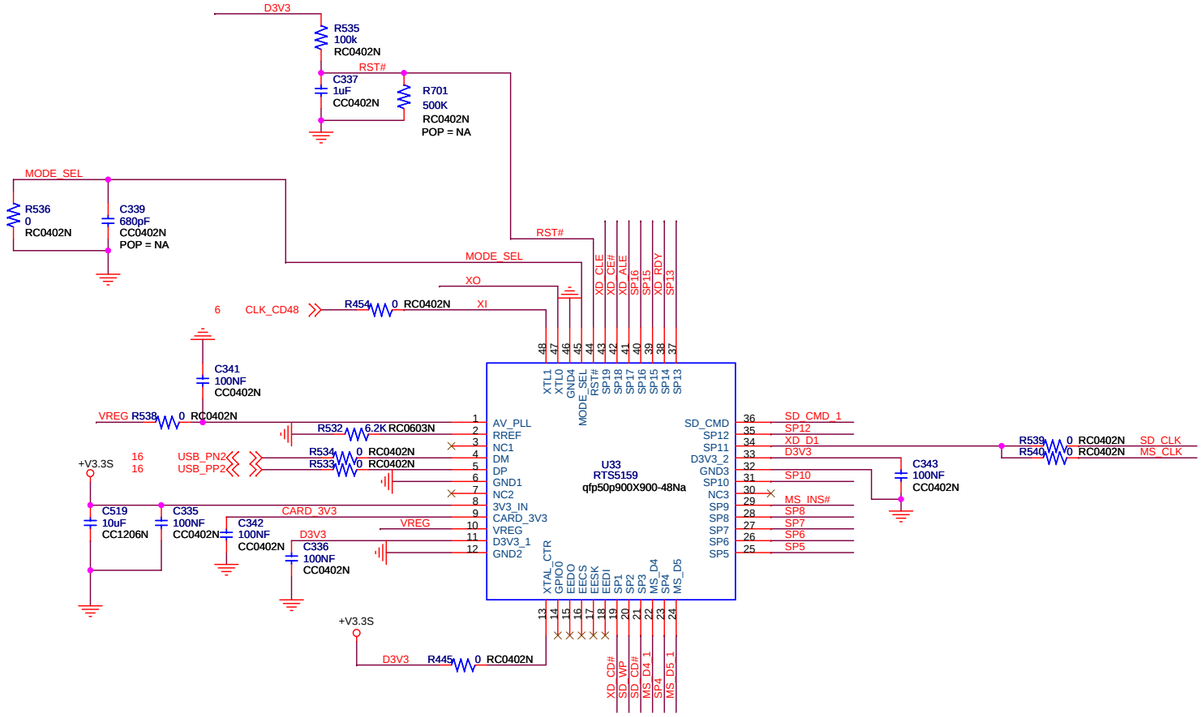
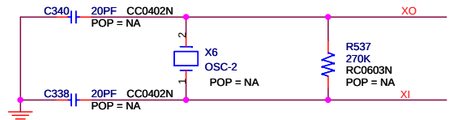
Cardreader





MS_D4_1			MS_D4
SP4	XD_D4	SD_DAT1	
MS_D5_1			MS_D5
SP5	XD_D5		MS_BS
SP6	XD_D3		MS_D1
SP7	XD_D6	SD_DAT0	MS_D0
SP8	XD_D2	SD_DAT7	MS_D2
SP10	XD_D7	SD_DAT6	MS_D3
SP12	XD_D0	SD_DAT5	MS_D6
SD_CMD_1		SD_CMD	
SP13	XD_WP#	SD_DAT4	MS_D7
SP15	XD_WE#	SD_DAT3	
SP16	XD_RE#	SD_DAT2	



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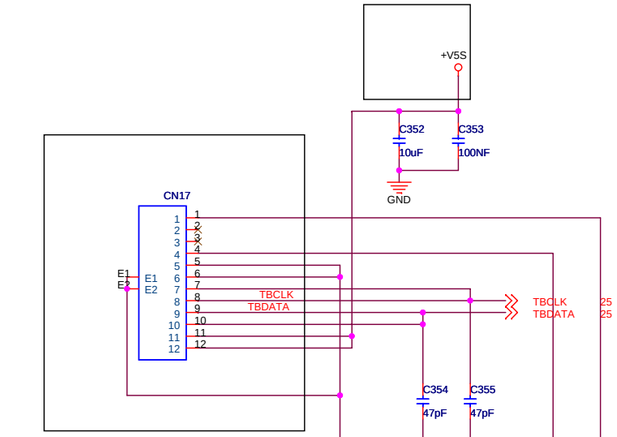
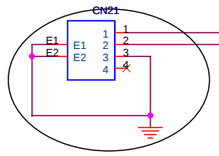
Title	<Title>		
Size C	Sheet Name: Card reader		Rev A
Date: Wednesday, November 04, 2009		Sheet 33 of 36	



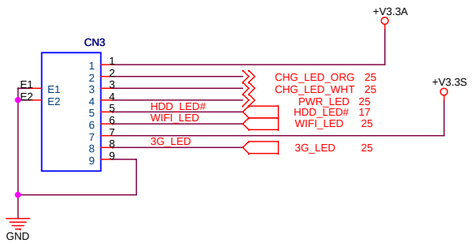
Connect to Touch PAD



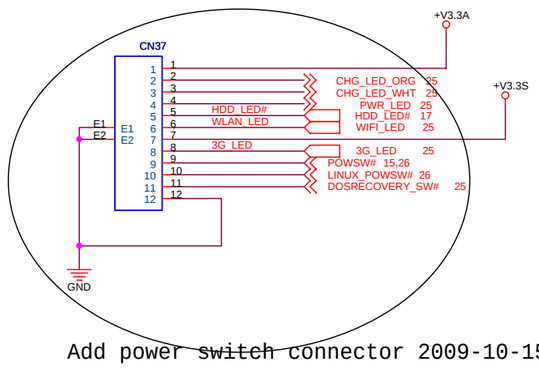
modify 1.0mm pitch 2009-10-15

TO TP_BOARD

TO LED_BOARD

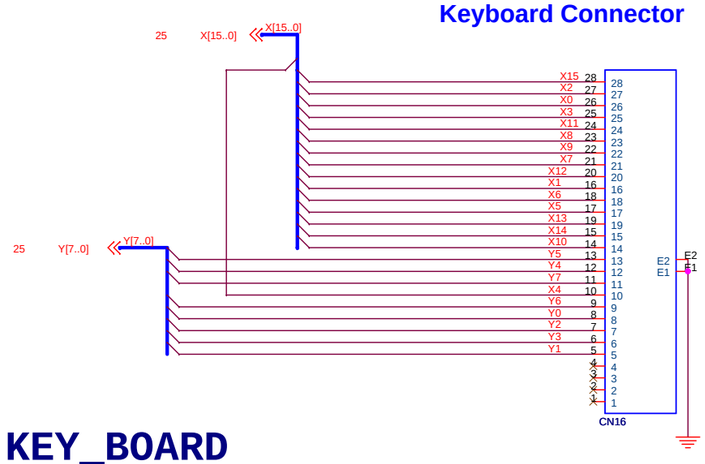


TO princeton sw_BOARD



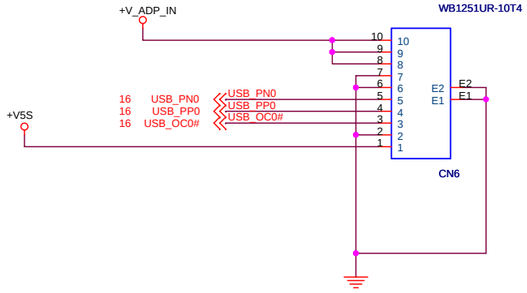
Add power switch connector 2009-10-15

Keyboard Connector



TO KEY_BOARD

TO DCIN_BOARD



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		Size C / Sheet Name: Main_Board CONNECTOR	Rev A
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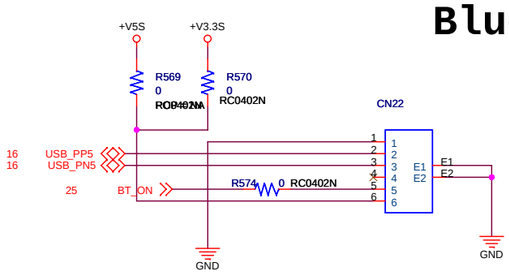
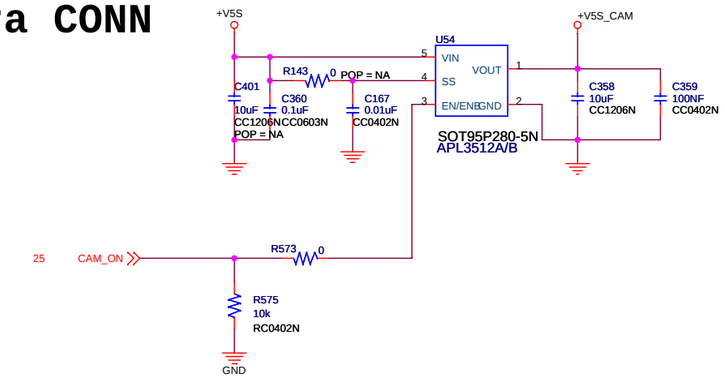
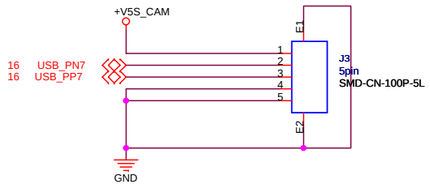
Bluetooth CONN



Camera CONN





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	Size C / Sheet Name: Option decice:BT/Camera	Rev A
	Date: Wednesday, November 04, 2009	Sheet 35 of 36

1.H_PROCHOT# 上拉改到电阻前，靠近CPU PIN

2.CN15:RTC 电池插座，PIN1和PIN2对换

3.Add X5,with X1 dualay,;X7,with X3 dualay 2009-10-15

4.Add touchscreen conector dmb conector mic connector 2009-10-15

5 Add 12pin connector & startup on system function 2009-10-15

6 Add L8,with L7 dualay 2009-10-15

7 modify +V3.3S & +V5S CIRCUIT 2009-10-15

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		Size: C	Sheet Name: Changelist	Rev: A
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