BAD40_HC
DIS/UMA Schematics Document
Sandy&Ivy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

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BAD40 HC Block Diagram (Discrete/UMA/co-lay)

Project Code: 91.4SA01.001
Project Name: BAD40_HC
PCB No: 11245
PCB Version: 1
PCB Name: BAD40 HC MB

Buttom Docking

VGA/HDMI(DVI)/DP
HP OUT/SPDIF/MIC IN/LINE IN/
USB2.0/USB3.0/DC JACK/
LAN/SERIAL PORT/PARALLEL PORT

##OnMainBoard
VRAM 2GB/1GB 88,89,90,91
DDR3 900MHz
Nvidia N13PGS 83,84,85,86,87
27MHz
PCIe x 16
(Discrete only)
Discreet/UMA/PX Co-lay
Intel CPU
IVY Bridge 4,5,6,7,8,9,10,11,12,13
DDRIII 1333 Channel A
DDRIII 1333 Channel B
DDRIII 1333 Slot 0 14
DDRIII 1333 Slot 1 15
FDIx4x2 (UMA only)
DMIx4
QM77
Intel PCH Panther Point
10 USB2.0 ports
4 USB3.0 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA 3G ports (4)
SATA 6G ports (2)
PCIE ports (8)
LPC I/F
ACPI 1.1
17,18,19,20,21,22,23,24,25,26
SMBus
32.768 KHz
25MHz
EDP 49
HDMI 51
LCD 49
CRT 50
SWITCH
EDP
HDMI
LVDS(Dual Channel)
RGB CRT
Display Port
PCIE
G sensor 79
PCIE x 1
Express Card 75
PCIE x 1 USB x 1
Mini-Card 802.11a/b/g 65
PCIE x 1
BCM 57760 31
PCIE x 1
intel 82579 105
25MHz
SWITCH
RJ45 CONN 59
25MHz
USB x 1
CardReader RTS5209 32
SD/MMC+/MS/ MS Pro/xD
PCIE x 1,USB x 2
Mini-Card WWAN 66
USB x1
SIM 66
USB3.0 x3
Right Side: USB x 3
Right Side: USB x 1
USB CHARGER USB x 1 107
Bluetooth 63
CAMERA 49
Smart Card 76
##External Module
USB2.0 x 4
AZALIA
SPI
LPC Bus
Flash ROM 8MB+4MB 60
LPC debug port 71
SATA3.0
HDD 56
SATA3.0
mSATA 66
SATA2.0
OOD 56
KBC
NUVOTON NPCE885 27
SMBus
Touch PAD 69
Int. KB 69
Thermal T7718 28
Fan 28
Internal Analog MIC
HP1
MIC IN
Azalia CODEC CX20584 29
2CH SPEAKER

SYSTEM DC/DC TPS5146 48	
INPUTS	OUTPUTS
5V_S5	0D85V_S0

CPU DC/DC VT1317SFCX 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC RT8237AGQW 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC RT8239CGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC VT1317SFCX 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208AGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT8015AGQW 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC	
INPUTS	OUTPUTS

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top	L5:Power
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

HR PX

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	N/A
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	N/A
LANE6	Intel /BCM LAN
LANE7	New Card
LANE8	N/A

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	N/A

USB Table

Pair	Device
0	USB. port 1
1	USB. port 2
2	USB. port 3
3	Dock
4	X
5	Fingerprint
6	X
7	X
8	Mini Card2 (WWAN) &BT
9	X
10	3G SIM
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

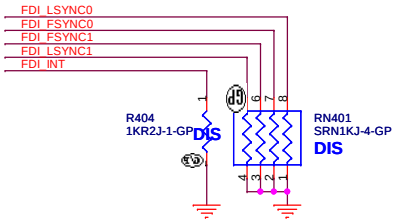
Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics function for power saving.



CPU1A — IVY-BRIDGE — 1 OF 9

DMI: DMI_TXN[3:0] / DMI_TXP[3:0] / DMI_RXN[3:0] / DMI_RXP[3:0]

Intel(R) FDI: FDI_TXN[7:0] / FDI_TXP[7:0] / FDI_FSYNC0 / FDI_FSYNC1 / FDI_INT / FDI_LSYNC0 / FDI_LSYNC1

eDP: DP_COMP (R402 24D9R2F-L-GP) / eDP_HPD (R403 10KR2J-3-GP) / eDP_AUXP_CPU / eDP_AUXN_CPU / eDP_TXP0_CPU / eDP_TXP1_CPU / eDP_TXN0_CPU / eDP_TXN1_CPU

PCI EXPRESS* - GRAPHICS

PEG_ICOMPI J22 — PEG_IRCOMP_R — R401 24D9R2F-L-GP — 1D05V_VTT
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_RXN[0..15] 83
PEG_RXP[0..15] 83
PEG_TXN[0..15] 83
PEG_TXP[0..15] 83

PEG_RX	PEG_RXN	PEG_RXP
#0	K33	J33
#1	M35	L35
#2	L34	K34
#3	J35	H35
#4	J32	H32
#5	H34	G34
#6	H31	G31
#7	G33	F33
#8	G30	F30
#9	F35	E35
#10	E34	E33
#11	E32	E32
#12	D33	D34
#13	D31	E31
#14	B33	C33
#15	C32	B32

PEG_TX	PEG_C_TXN	C401–C416	PEG_C_TXP	C417–C432	PEG_TXN	PEG_TXP
#0	M29	C401	M28	C417	PEG_TXN15	PEG_TXP15
#1	M32	C402	M33	C418	PEG_TXN14	PEG_TXP14
#2	M31	C403	M30	C419	PEG_TXN13	PEG_TXP13
#3	L32	C404	L31	C420	PEG_TXN12	PEG_TXP12
#4	L29	C405	L28	C421	PEG_TXN11	PEG_TXP11
#5	K31	C406	K30	C422	PEG_TXN10	PEG_TXP10
#6	K28	C407	K27	C423	PEG_TXN9	PEG_TXP9
#7	J30	C408	J29	C424	PEG_TXN8	PEG_TXP8
#8	J28	C409	J27	C425	PEG_TXN7	PEG_TXP7
#9	H29	C410	H28	C426	PEG_TXN6	PEG_TXP6
#10	G27	C411	G28	C427	PEG_TXN5	PEG_TXP5
#11	E29	C412	E28	C428	PEG_TXN4	PEG_TXP4
#12	F27	C413	F28	C429	PEG_TXN3	PEG_TXP3
#13	D28	C414	D27	C430	PEG_TXN2	PEG_TXP2
#14	F26	C415	E26	C431	PEG_TXN1	PEG_TXP1
#15	E25	C416	D25	C432	PEG_TXN0	PEG_TXP0

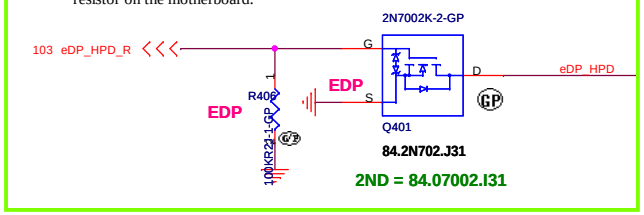
All C401–C432: DIS_PX_Muxless SCD22U10V2KX-1GP

62.10055.321

SB 0923

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.



2ND = 84.07002.I31

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Title: CPU (PCIE/DMI/FDI)

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SSID = CPU

CPU1B — IVY-BRIDGE — 2 OF 9

MISC
- 22 H_SNB_IVB# → C26 PROC_SELECT#
- AN34 SKTOCC#

CLOCKS
- BCLK A28 / BCLK# A27 → CLK_EXP_P 20 / CLK_EXP_N 20
- DPLL_REF_CLK A16 / DPLL_REF_CLK# A15 → CLK_DP_P_R 20 / CLK_DP_N_R 20

THERMAL
- AL33 CATERR#
- 22,27 H_PECI ↔ AN33 PECI
- 27,42 H_PROCHOT# → R513 56R2J-4-GP → H_PROCHOT# R → AL32 PROCHOT#
- 22,36 H_THERMTRIP# → AN32 THERMTRIP#

DDR3 MISC
- SM_DRAMRST# R8 → R502 4K99R2F-L-GP → SM_DRAMRST# 37
- SM_RCOMP0 AK1 → SM_RCOMP_0 R506 140R2F-GP
- SM_RCOMP1 A5 → SM_RCOMP_1 R507 25D5R2F-GP
- SM_RCOMP2 A4 → SM_RCOMP_2 R508 200R2F-L-GP

PWR MANAGEMENT
- 19 H_PM_SYNC → AM34 PM_SYNC
- R503 10KR2J-3-GP
- 22,36 H_CPUPWRGD → AP33 UNCOREPWRGOOD
- 19,37 PM_DRAM_PWRGD → R505 0R2J-2-GP → V8 SM_DRAMPWROK
- 37 VDDPWRGOOD
- BUF_CPU_RST# → AR33 RESET#

JTAG & BPM
- PRDY# AP29 / PREQ# AP27
- TCK AR26 / TMS AR27 / TRST# AP30 → XDP_TRST#
- TDI AR28 / TDO AP26 → XDP_TDO
- DBR# AL35 → XDP_DBRESET#
- BPM#0 AT28 / BPM#1 AR29 / BPM#2 AR30 / BPM#3 AT30 / BPM#4 AP32 / BPM#5 AR31 / BPM#6 AT31 / BPM#7 AR32

1D05V_VTT
- R501 62R2J-GP
- H_PROCHOT#
- C502 SC47P50V2JN-3GP

CRB : 47pf
CEKLT:43pf

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

RN502 SRN1KJ-1-GP
- CLK_DP_P_R
- CLK_DP_N_R
- 1D05V_VTT

20100628 V1.3
DIS

RN501 SRN51J-GP
- XDP_TDO
- XDP_TRST#
- 1D05V_VTT

RN503 SRN1K5J-1-GP
- 3D3V_S0
- XDP_DBRESET#
- PLT_RST# (7,31,32,36,65,66,71,75,82,83,97,105)
- BUF_CPU_RST#

EC501 SC120P50V2JN-1GP
- H_CPUPWRGD

EC502 SC5P50V2CN-2GP
- BUF_CPU_RST#
- DY

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Title	CPU (THERMAL/CLOCK/PM)	
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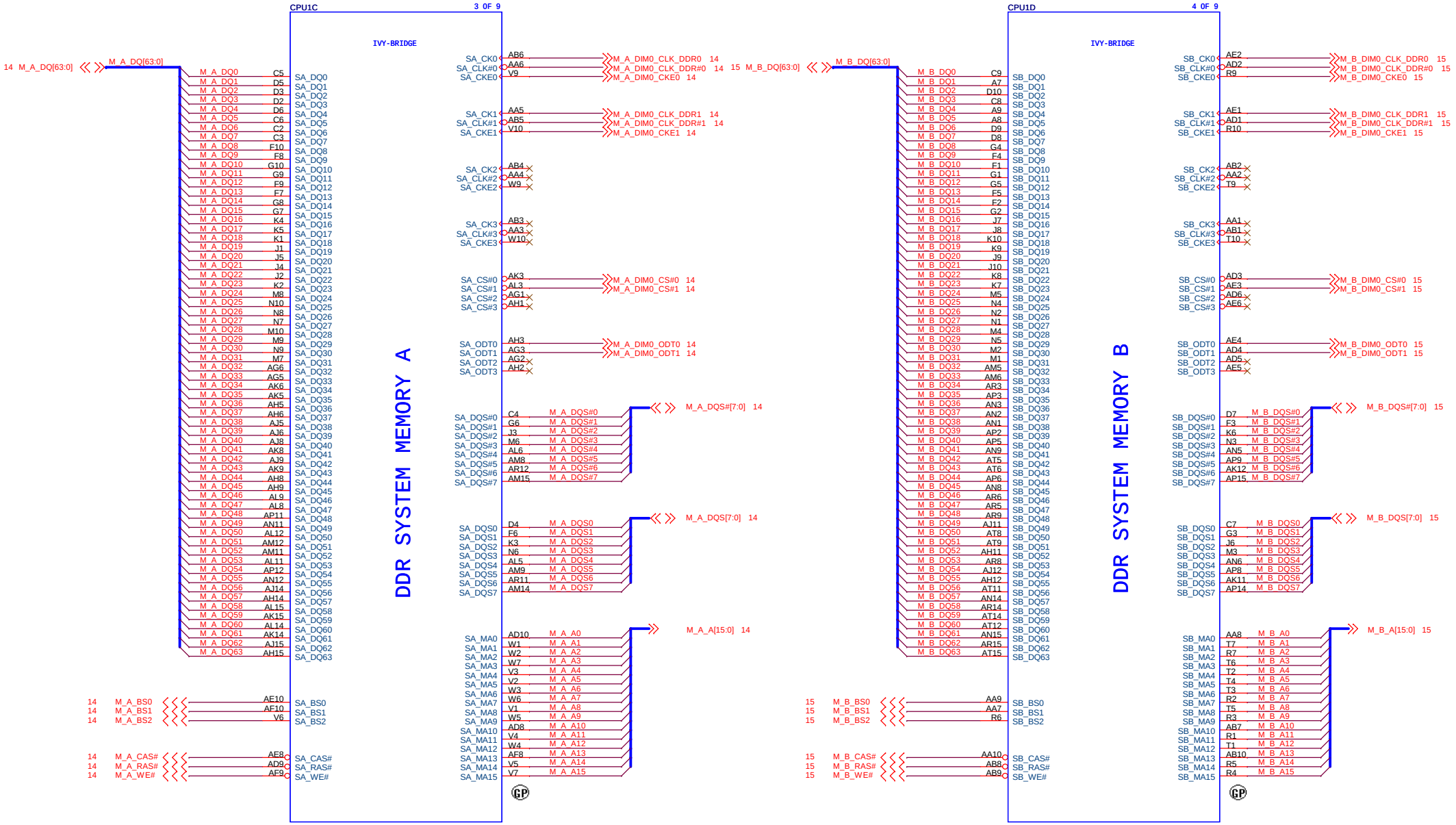
SSID = CPU



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<Variant Name>

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Title	***CPU (DDR)***	
Size A3	Document Number **BAD40_HC**	Rev **1**
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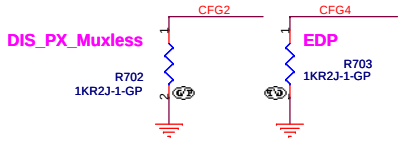
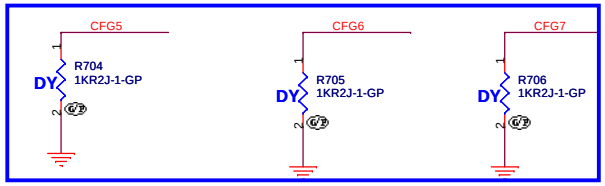
SSID = CPU



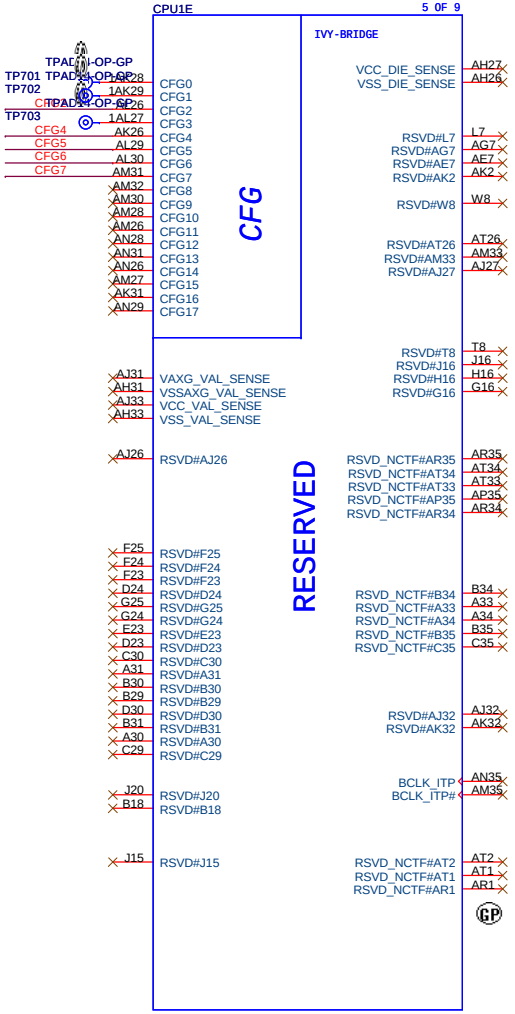
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

SA



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



62.10055.321

HR PX

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Title: CPU (RESERVED)

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SSID = CPU

POWER

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CPU1F

IVY-BRIDGE

PROCESSOR CORE POWER

53A

VCC_CORE

0308 -1
change to 78.2261T.5BL for acousit noice

0308 -1

0308 -1
change to 78.2261T.5BL for acousit noice

0312 -1

0308 -1

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

close to CPU

H_CPU_SVIDDAT R804 130R2F-1-GP

VR_SVID_ALERT# R805 75R2F-2-GP

0412 -1M

R801,R802 close to CPU

R801 100R2F-L1-GP-U

R802 100R2F-L1-GP-U

1215 SC

TP801 TPAD14-OP-GP

TP802 TPAD14-OP-GP

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

62.10055.321

<Variant Name>

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Title: CPU (VCC_CORE)

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SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

POWER

CPU1G — 7 OF 9 — IVY-BRIDGE

GRAPHICS

SENSE LINES
VAXG_SENSE
VSSAXG_SENSE
AK35
AK34
VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF
SM_VREF
AL1
+V_SM_VREF_CNT 37
SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
B4
D1
M_VREF_DQ_DIMM0_C 37
M_VREF_DQ_DIMM1_C 37

Chief River

DDR3 -1.5V RAILS
VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15
AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

SA RAIL
VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8
M27 M26 L26 J26 J25 J24 H26 H25

MISC
VCCSA_SENSE
H23
VCCSA_SENSE 48
VCCSA_VID0
VCCSA_VID1
C22
C24
VCCIO_SEL
A19
H_SNB_IVB#_PWRCTRL

1.8V RAIL
VCCPLL1 VCCPLL2 VCCPLL3
B6 A6 A2

62.10055.321

PROCESSOR VAXG: 38A

1201 SC

UMA_PX_Muxless

C901 C902 C903 C904 C905 C906 — SC10U6D3V5KX-1GP — DY

PROCESSOR VDDQ: 10A

C909 C910 C911 C912 C913 C914 — SC10U6D3V5KX-1GP — DY

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

SNB 上件，1010 back IVB

M_VREF_DQ_DIMM0_C
M_VREF_DQ_DIMM1_C
1D5V_S0
RN902 SRN1KJ-7-GP
DY

C907 C908 C918 C919 C920 C921 — SC10U6D3V5KX-1GP — DY

C923 C925 C926 C927 C928 C929 C930 — SC22U6D3V5MX-2GP — DY

C931 C932 — SC22U6D3V5MX-2GP — DY

PROCESSOR VCCSA: 6A

0D85V_S0

C916 C915 — SC10U6D3V5KX-1GP — DY

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

R902 100R2F-L1-GP-U
R902 need be close to pin H23.

PROCESSOR VCCPLL: 1.8A

1D8V_S0
C922 SC10U10V2KX-1GP

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

SB 1020 change to DY for co-lay
3D3V_S5
R911 100KR2J-1-GP DY
H_SNB_IVB#_PWRCTRL

1D05V_VTT
R908 10KR2J-3-GP DY
R912 10KR2J-3-GP DY
R913 10KR2J-3-GP
R914 10KR2J-3-GP
VCCSA_VID0 48
VCCSA_VID1 48

VCC_GFXCORE
R903 0R3J-0-U-GP DIS
R904 0R3J-0-U-GP DIS
R905 0R3J-0-U-GP DIS
R901 0R3J-0-U-GP DIS

PIn A19

1.05V	H
1V	L

VCCSA Voltage Select

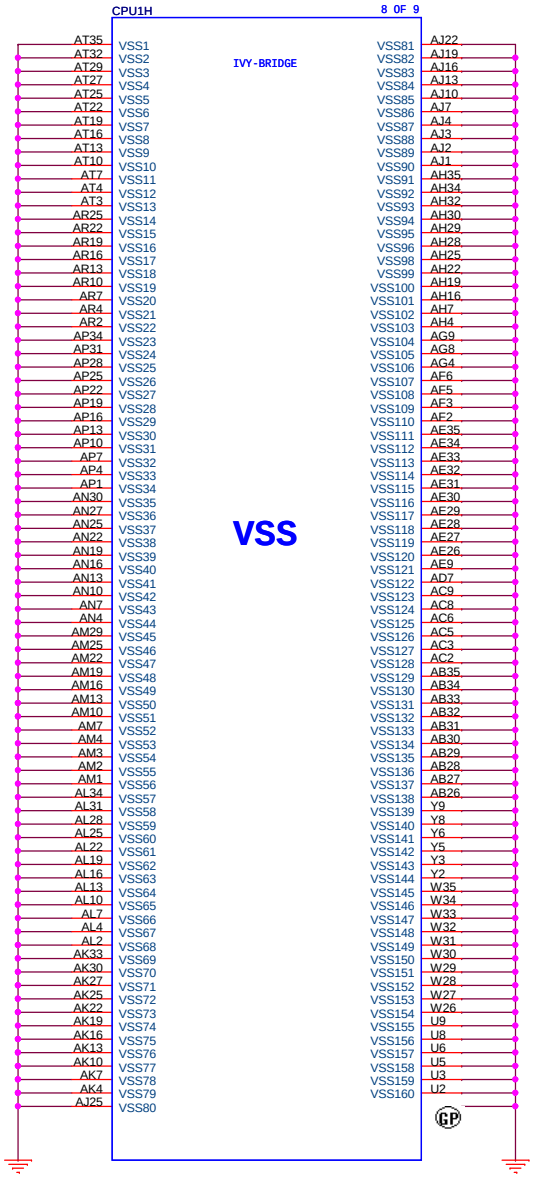
VID[1]	VID[0]	VCCSA
0	0	0.9 V
1	0	0.8 V
0	1	0.725 V
1	1	0.675 V

<Variant Name>

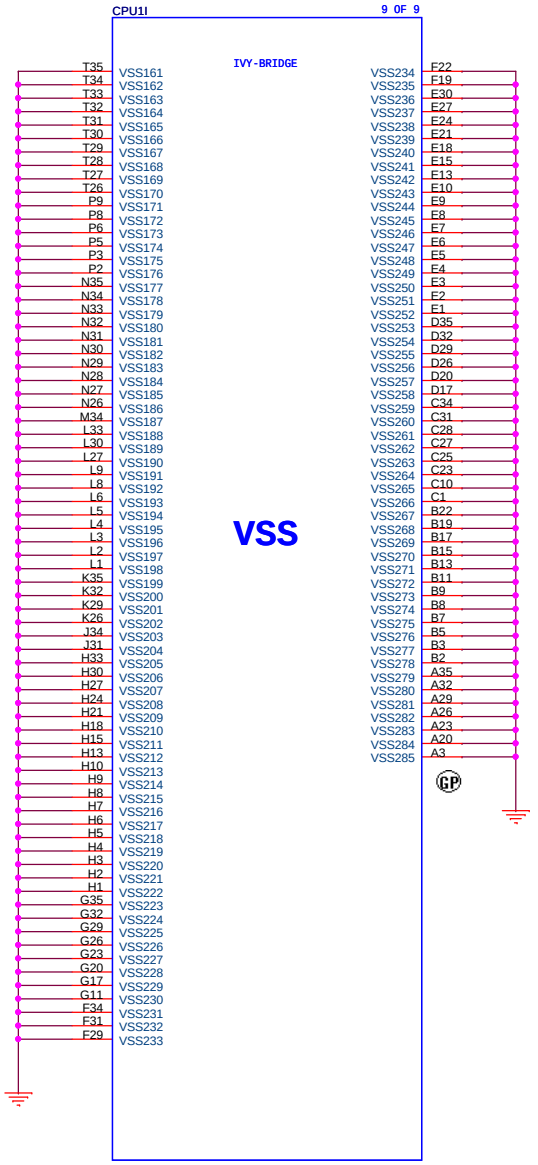
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)
Size: Custom | Document Number: BAD40_HC | Rev: 1
Date: Thursday, April 12, 2012 | Sheet 9 of 108

SSID = CPU



62.10055.321



62.10055.321

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 10 of 108

reserve

JE40 delete XDP function

HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***XDP***		
Size: A4	Document Number: **BAD40_HC**	Rev: **1**
Date: Thursday, April 12, 2012	Sheet 11 of 108	

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 12 of 108

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 13 of 108

SSID = MEMORY

DM1

M_A_A[15:0] 6

M_A_BS2 6

M_A_BS0 6
M_A_BS1 6
M_A_DQ[63:0] 6

M_A_DQS#[7:0] 6
M_A_DQS[7:0] 6

M_A_DIM0_ODT0 6
M_A_DIM0_ODT1 6

DDR_VREF_S3
M_VREF_DQ_DIMM0
15,37 DDR3_DRAMRST#
0D75V_S0

M_A_RAS# 6
M_A_WE# 6
M_A_CAS# 6
M_A_DIM0_CS#0 6
M_A_DIM0_CS#1 6
M_A_DIM0_CKE0 6
M_A_DIM0_CKE1 6
M_A_DIM0_CLK_DDR0 6
M_A_DIM0_CLK_DDR#0 6
M_A_DIM0_CLK_DDR1 6
M_A_DIM0_CLK_DDR#1 6

PCH_SMBDATA 15,20,66,79
PCH_SMBCLK 15,20,66,79
TS#_DIMM0_1 15

3D3V_S0
1D5V_S3

DDR_WR_VREF01_B4 37

0308 -1
R1404 2
0R0603-PAD
M1

1228 SC
M1405
0R3J-0-U-GP
DY

Tracew should be at least 20 mils wide

C1411 SCD1U10V2KX-5GP
C1413 SCD1U10V2KX-5GP
C1401 SCD1U10V2KX-5GP

Place these caps close to VTT1 and VTT2.

1125 SC for RF
C1419 SC1U6D3V2KX-GP
C1420 SC1U6D3V2KX-GP
C1421 SC1U6D3V2KX-GP
C1422 SC220P50V2KX-2GP
C1418 SCD1U10V2KX-5GP
DY

H =4mm

DDR3-204P-122-GP

62.10017.Z51
2nd = 62.10017.V51

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT
TS#_DIMM0_1
R1403 10KR2J-3-GP
3D3V_S0

SODIMM A DECOUPLING
1D5V_S3
C1403 SC10U6D3V5KX-1GP
C1404 SC10U6D3V5KX-1GP
C1405 SC10U10V5ZY-1GP
C1406 SC10U6D3V5KX-1GP
C1407 SC10U6D3V5KX-1GP
C1408 SC10U10V5ZY-1GP
C1409 SC10U6D3V5KX-1GP
C1410 SC10U6D3V5KX-1GP
DY
C1416 SCD1U10V2KX-5GP
C1417 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMA.

HR PX

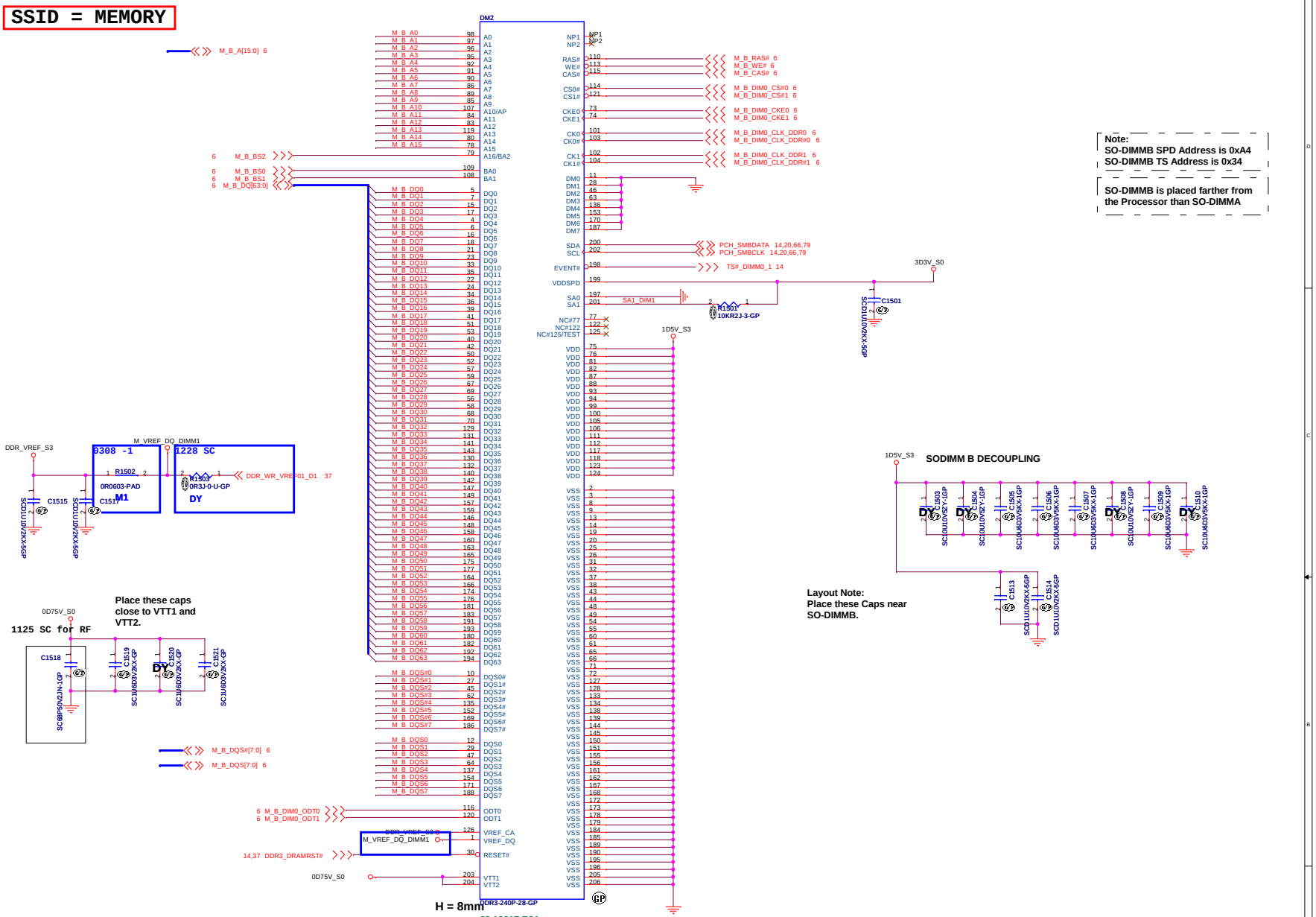
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size	Document Number	Rev
Custom	BAD40_HC	11

Date: Thursday, April 12, 2012 Sheet 14 of 108

SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

H = 8mm

62.10017.R91

1st = 62.10024.G01

2nd = 62.10024.D41

HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 15 of 108

(Blanking)

<Variant Name>

緯創資通

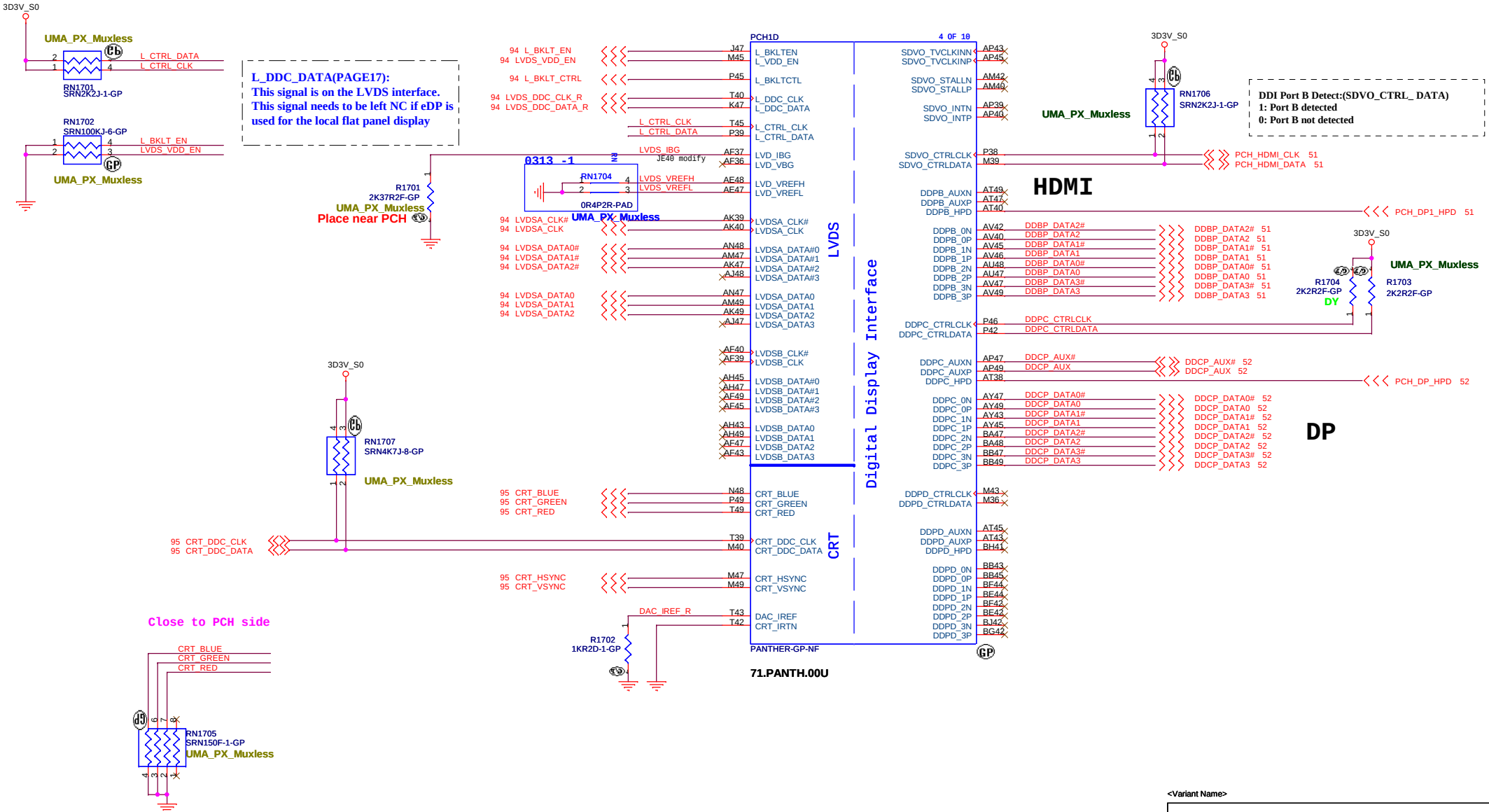
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DDR3-SODIMM2

Size	Document Number	Rev
A4	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 16 of 108



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

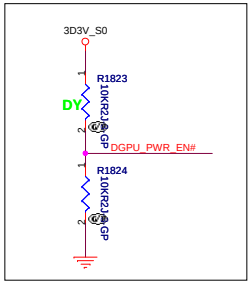
Title: PCH (LVDS/CRT/DDI)

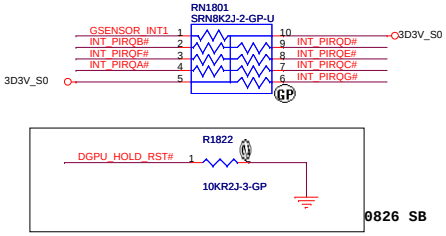
Size	Document Number	Rev
A3	BAD40_HC	11

Date: Thursday, April 12, 2012 Sheet 17 of 108

SSID = PCH

0826 SB





0826 SB

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

PCH1E

5 OF 10

RSVD

PCI

USB

PANTHER-GP-NF

71.PANTH.00U

SB 0920

USB Ext. port 1 (HS)
External debug port use on Huron river platform

1216 SC

0915 SB

1208 SC

0131 SD

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

0314 -1 for EMI

1125 SC for RF

USB Table

Pair	Device
0	USB port 2 on S/B
1	USB port 3 on S/B
2	USB port 4 on S/B(usb charger)
3	DOCK
4	BLUETOOTH(from port3)
5	Fingerprint(from port2)(NO USE)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB port1(SATA Combo),on M/B
10	3G Card
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card or USB HUB(New/Smart)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

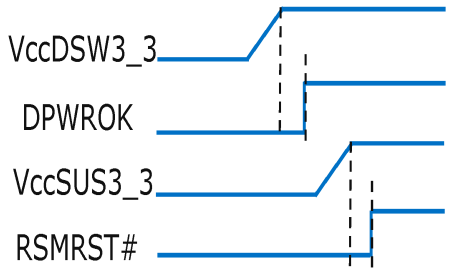
Title: PCH (PCI/USB/NVRAM)

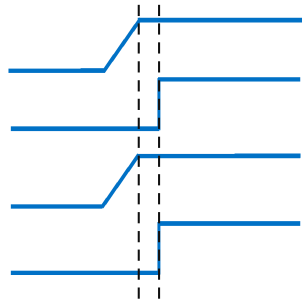
Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 18 of 108

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.





For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

PCH1C — 3 OF 10

DMI: DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN, DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP, DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN, DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP

FDI: FDI_RXN0–7, FDI_RXP0–7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

System Power Management: DMI_ZCOMP, DMI_IRCOMP, DMI2RBIAS, SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT/GPIO31, BATLOW#/GPIO72, RI#, DSWVRMEN, DPWROK, WAKE#, CLKRUN#/GPIO32, SUS_STAT#/GPIO61, SUSCLK/GPIO62, SLP_S5#/GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN#/GPIO29

PANTHER-GP-NF

71.PANTH.00U

R1901 49D9R2F-GP DMI_COMP_R
R1902 750R2F-GP RBIAS_CPY
R1926 10KR2J-3-GP DY
R1904 100KR2J-1-GP PWROK
0628 Modify: Change R1904 to 100K 0402 from 10K and default stuff.
JE40 modify SUS_PWR_ACK
R1905 10KR2J-3-GP SYS_RESET#
0302 -1 for SBA
R1924 0R0402-PAD PWROK
R1930 0R2J-2-GP Non_iAMT_SBA
R1929 0R2J-2-GP APWROK
iAMT_SBA
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms
R1910 0R0402-PAD DSWVRMEN
R1911 10KR2J-3-GP DY DPWROK
1222 SC
R1928 0R2J-2-GP DY SLP_S3#
R1927 0R2J-2-GP SLP_A#
iAMT_SBA SLP_SUS#
0302 -1 for SBA

DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled

R1917 330KR2J-L1-GP
R1918 330KR2J-L1-GP DY
R1919 8K2R2J-3-GP

RN1901 SRN10KJ-6-GP
R1922 10KR2J-3-GP Non_iAMT_SBA
R1921 10KR2J-3-GP

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

R1909 100KR2J-1-GP
R1916 10KR2J-3-GP
R1912 1KR2J-1-GP
Q1901 2N7002KDW-GP
84.2N702.A3F
2nd = 84.2N702.F3F

PWRBTN#
This signal has an internal pull-up resistor

R1908 100KR2J-1-GP

PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**
Size: A3 | Document Number: **BAD40_HC** | Rev: 1
Date: Thursday, April 12, 2012 | Sheet 19 of 108

SSID = PCH

PCH1B

2 OF 10

PCI-E*

SMBUS

CLOCKS

Controller Link

FLEX CLOCKS

3GLAN

Card Reader

WLAN

USB 3.0

Intel/BCM LAN

NEW CARD

1201 sc

0921 SB

3GLAN CLK

Card Reader

WLAN CLK

USB3.0 CLK(reserve)

LAN CLK

0907 SB

0312 -1

0308 -1

1215 SC

1212 SC

SB 0920 For RF

CRB : 1K

CEKLT: 10K

2nd = 84.2N702.F3F

2nd = 82.30020.I01

need very close to PCH

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

PANTHER-GP-NF
71.PANTH.00U

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
Optimus(Muxless) : 1 0

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 20 of 108

SSID = PCH

SB 0923

82.30001.A41
2nd = 82.30001.841

RTC Reset

1103 SC for AFR

1103 SC

84.2N702.J31
2ND = 84.07002.I31

PCH1A

1 OF 10

PANTHER-GP-NF

71.PANTH.00U

1223 SC

DUAL RGM

1208 SC

HDD1

mSATA

ODD

ESATA

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

**This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310**

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

H->Smart Card
L->Non Smart Card

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size: A3 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 21 of 108

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

3D3V_S0 — RN2203 SRN10KJ-5-GP — H_RCIN# / H_A20GATE

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

3D3V_S5 — **0908 SB**
R2220 10KR2J-3-GP (DY) — PCH_GPIO24 — R2207 100KR2J-1-GP

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

	LVDS	eDP
EDP#_LVDS	H	L

PassWord Clear
G2201 GAP-OPEN

1124 SC del R2206

1208 SC for Del e-SATA
3D3V_S0 — R2224 10KR2J-3-GP — eSATA_DET# — R2209 10KR2J-3-GP (DY)

3D3V_S0 — RN2201 SRN10KJ-5-GP — DGPU_HPD_INTR# / EC_SCI#
RN2202 SRN10KJ-8-GP — MFG_MODE / S_GPIO / PCH_TEMP_ALERT#
3D3V_S5 — RN2204 SRN10KJ-6-GP — USB3_PWR_ON / LAN_DIS#
PCH_GPIO15 — R2201 1KR2J-1-GP

VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

3D3V_S0 — R2218 10KR2J-3-GP — UMA_VRAM800MHZ — PCH_GPIO22 — R2219 10KR2J-3-GP — VRAM900MHZ

VRAM Size
3D3V_S0 — R2214 2G — R2216 1G — VRAM_SIZE1 / VRAM_SIZE2 — R2215 1G_512M — R2217 512M_2G

PCH1F — 6 OF 10 — PANTHER-GP-NF — **71.PANTH.00U**

GPIO:
S_GPIO T7 — EC_VPS_SMI# A42 — DGPU_HPD_INTR# H36 — E38 — ICC_EN# C10 — LAN_DIS# C4 — PCH_GPIO15 G2 — SATA_ODD_PRSNT# U2 — DGPU_PWROK D40 — PCH_GPIO22 T5 — PCH_GPIO24 E8 — PCH_GPIO27 E16 — PLL_ODVR_EN P8 — PSW_CLR# K1 — eSATA_DET# K4 — DMI_OVRVLTG V8 — FDI_OVRVLTG M5 — MFG_MODE N2 — M3 — TPM_TCM_TYPE2 V13 — PCH_TEMP_ALERT# V3 — USB3_PWR_ON D6
BMBUSY#/GPIO0 — TACH1/GPIO1 — TACH2/GPIO6 — TACH3/GPIO7 — GPIO8 — LAN_PHY_PWR_CTRL/GPIO12 — GPIO15 — SATA4GP/GPIO16 — TACH0/GPIO17 — SCLOCK/GPIO22 — GPIO24 — GPIO27 — GPIO28 — STP_PCI#/GPIO34 — GPIO35 — SATA2GP/GPIO36 — SATA3GP/GPIO37 — SLOAD/GPIO38 — SDATAOUT0/GPIO39 — SDATAOUT1/GPIO48 — SATA5GP/GPIO49/TEMP_ALERT# — GPIO57

CPU/MISC:
TACH4/GPIO68 C40 — SATA_ODD_PWRGT 56
TACH5/GPIO69 B41 — UMA_DIS# 20
TACH6/GPIO70 C41 — VRAM_SIZE1
TACH7/GPIO71 A40 — VRAM_SIZE2
A20GATE P4 — H_A20GATE 27
PECI AU16 — H_PECI_R — R2203 0R2J-2-GP (DY) — H_PECI 5,27
RCIN# P5 — H_RCIN# 27
PROCPWRGD AY11 — H_CPUPWRGD 5,36
THRMTRIP# AY10 — PCH_THERMTRIP_R
INIT3_3V# T14
DF_TVS AY1 — NV_CLE
TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37

NCTF:
VSS_NCTF_15#BG2 — VSS_NCTF_16#BG48 — VSS_NCTF_17#BH3 — VSS_NCTF_18#BH47 — VSS_NCTF_19#BJ4 — VSS_NCTF_20#BJ44 — VSS_NCTF_21#BJ45 — VSS_NCTF_22#BJ46 — VSS_NCTF_23#BJ5 — VSS_NCTF_24#BJ6 — VSS_NCTF_25#C2 — VSS_NCTF_26#C48 — VSS_NCTF_27#D1 — VSS_NCTF_28#D49 — VSS_NCTF_29#E1 — VSS_NCTF_30#E49 — VSS_NCTF_31#F1 — VSS_NCTF_32#F49
NCTF TEST PIN: A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49, B62, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48, D1, D49, E1, E49, F1, F49
VSS_NCTF_1#A4 — VSS_NCTF_2#A44 — VSS_NCTF_3#A45 — VSS_NCTF_4#A46 — VSS_NCTF_5#A5 — VSS_NCTF_6#A6 — VSS_NCTF_7#B3 — VSS_NCTF_8#B47 — VSS_NCTF_9#BD1 — VSS_NCTF_10#BD49 — VSS_NCTF_11#BE1 — VSS_NCTF_12#BE49 — VSS_NCTF_13#BF1 — VSS_NCTF_14#BF49

TPAD14-OP-GFP2203 — PCH_GPIO27
TPAD14-OP-GFP2204 — TP11 — PCH_TEMP_ALERT#
TPAD14-OP-GFP2210 — USB3_PWR_ON
TPAD14-OP-GFP2206 — PCH_NCTF_1
TPAD14-OP-GFP2208 — PCH_NCTF_3
TPAD14-OP-GFP2207 — PCH_NCTF_2
TPAD14-OP-GFP2209 — PCH_NCTF_4

21 PSW_CLR# — JE40 delete FP function
56 SATA_ODD_PRSNT# — 3D3V_S0 — R2202 200KR2F-L-GP
27 EC_VPS_SMI# / 27 EC_SCI# / 105 LAN_DIS#
0806 delete TP2202, TP2203
49 EDP#_LVDS

1D8V_S0 — R2221 2K2R2J-2-GP — NV_CLE — R2222 1KR2J-1-GP — H_SNB_IVB# 5

-1. 4/11
RN2205 SRN56J-4-GP (DY) — 1D05V_VTT
PCH_THERMTRIP_R — R2204 390R2F-2GP — H_THERMTRIP# 5,36

FDI_OVRVLTG — R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI_OVRVLTG — R2210 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

0908 SB
3D3V_S5 — R2223 10KR2J-3-GP — ICC_EN# — R2211 1KR2J-1-GP (DY)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN DY 1 — R2212 1KR2J-1-GP

<Core Design>
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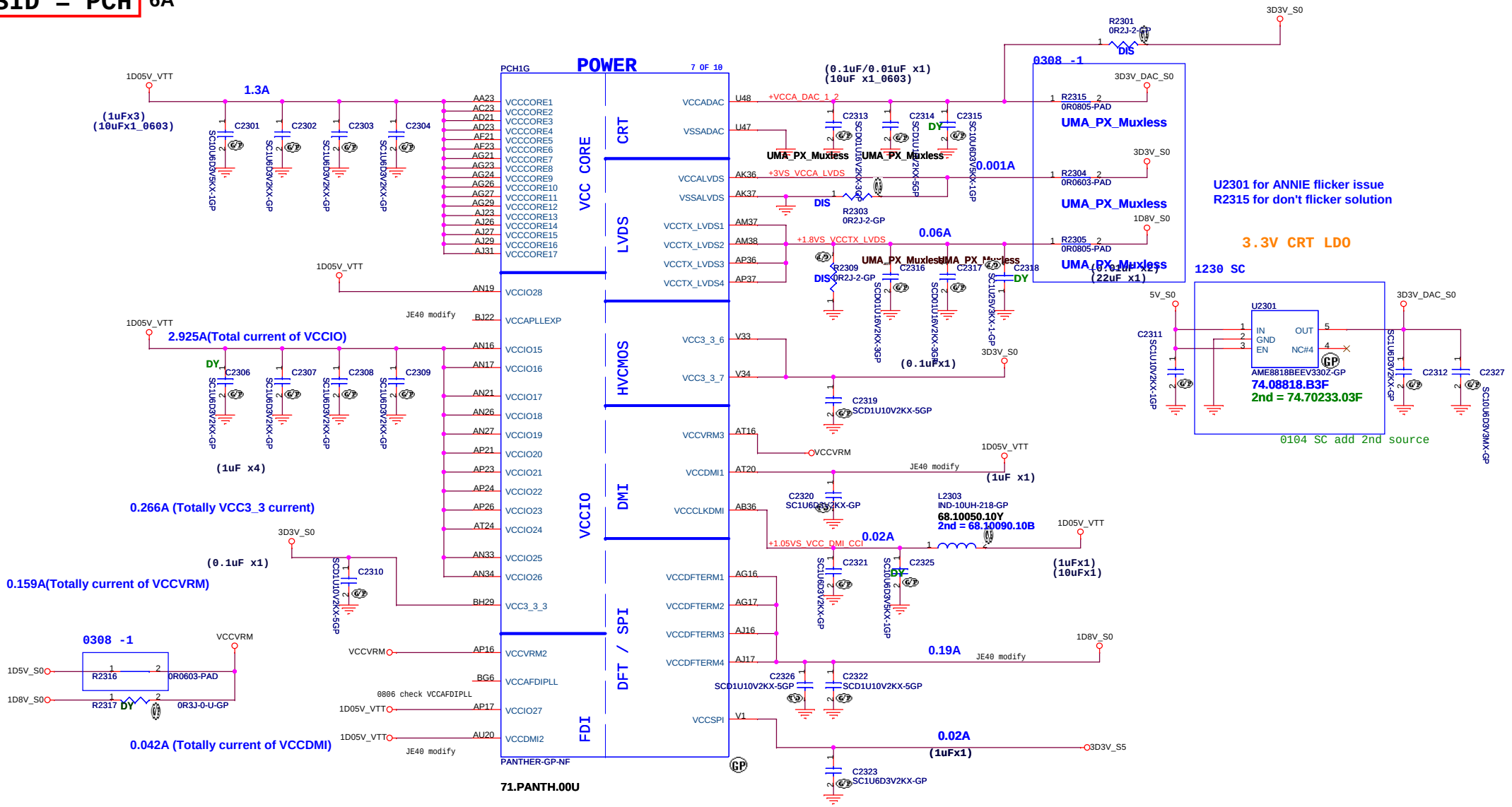
Title: **PCH (GPIO/CPU)**
Size: Custom | Document Number: BAD40_HC | Rev: 1
Date: Thursday, April 12, 2012 | Sheet 22 of 108

SSID = PCH 6A



<Variant Name>

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Title: PCH (POWER1)

Size: A3 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 23 of 108

SSID = PCH

POWER

PCH1J — 10 OF 10

Clock and Miscellaneous

TP17 TPAD14-OP-GP — VCCACK — AD49 VCCACLK

3D3V_S5 — 0.002A — T16 VCCDSW3_3

(10uFx1) (1uFx1) (0.1uFx1)

V12 DCPSUSBYP

3D3V_S0 — C2402 SC1U10V2KX-1GP — TP19 TPAD14-OP-GP — VCCAPLLDMI2 — BH23 VCCAPLLDMI2

1D05V_VTT — (10uFx1) — AL29 VCCIO14

AL24 DCPSUS3

1D05V_M — 1.01A (Total current of VCCASW)

C2403 C2404 C2406 C2407 C2408 — DY — (22uFx2_0603) (1uFx3)

AA19 VCCASW1
AA21 VCCASW2
AA24 VCCASW3
AA26 VCCASW4
AA27 VCCASW5
AA29 VCCASW6
AA31 VCCASW7
AC26 VCCASW8
AC27 VCCASW9
AC29 VCCASW10
AC31 VCCASW11
AD29 VCCASW12
AD31 VCCASW13
W21 VCCASW14
W23 VCCASW15
W24 VCCASW16
W26 VCCASW17
W29 VCCASW18
W31 VCCASW19
W33 VCCASW20

+VCCRTCEXT — C2411 SCD1U10V2KX-5GP (0.1uFx1) — N16 DCPRTC

0.16A (Totally current of VCCVRM)

VCCVRM — Y49 VCCVRM4

+1.05VS_VCCA_A_DPL — BD47 VCCADPLLA

+1.05VS_VCCA_B_DPL — BF47 VCCADPLLB

JE40 modify 07/16

1D05V_VTT — C2412 SC1U6D3V2KX-GP — JE40 modify (1uFx1) — AF17 VCCIO7

AF33 VCCDIFFCLKN1
AF34 VCCDIFFCLKN2
AG34 VCCDIFFCLKN3

1D05V_VTT (1uFx1) — 0.055A — C2414 SC1U6D3V2KX-GP

C2413 SC1U6D3V2KX-GP — JE40 modify (1uFx1) — 0.095A — AG33 VCCSSC

1D05V_VTT — +VCCSST — (0.1uFx1) — V16 DCPSST

C2415 SCD1U10V2KX-5GP — T17 DCPSUS1

1D05V_M — R2416 0R2J-2-P — DY — 1D05V_M_DCPSUS — V19 DCPSUS2

C2421 DY SC1U6D3V2KX-GP

1D05V_VTT — BJ8 V_PROC_IO

(0.1uFx2) (4.7uFx1_0603) — C2417 SC4D7U6D3V3KX-GP — C2418 SCD1U10V2KX-5GP — DY C2419 SCD1U10V2KX-5GP

RTC_AUX_S5 — 6uA — A22 VCCRTC

(0.1uFx2) (1uFx1) — C2420 SC1U6D3V2KX-GP — DY

PANTHER-GP-NF

71.PANTH.00U

USB

VCCIO29 N26 — 1D05V_VTT — (1uFx1) — C2423 SC1U6D3V2KX-GP
VCCIO30 P26
VCCIO31 P28
VCCIO32 T27
VCCIO33 T29

0.097A (Totally current of VCCSUS3_3)

VCCSUS3_3_7 T23 — 3D3V_S5 — (0.1uFx1) — C2424 SCD1U10V2KX-5GP
VCCSUS3_3_8 T24
VCCSUS3_3_9 V23
VCCSUS3_3_10 V24
VCCSUS3_3_6 P24 — 3D3V_S5 — (0.1uFx1) — C2425 SCD1U10V2KX-5GP

VCCIO34 T26 — 1D05V_VTT

V5REF_SUS M26 — +5VA_PCH_VCC5REFSUS — 0.001A

3D3V_S5 — 5V_S5 — 83.R0304.D8F — D2401 CH751H-40-1-GP — R2408 10R2J-2-GP — (0.1uFx1) — C2426 SCD1U10V2KX-5GP

DCPSUS4 AN23 — TP21 TPAD14-OP-GP

VCCSUS3_3_1 AN24 — 3D3V_S5

PCI/GPIO/LPC

V5REF P34 — +5VS_PCH_VCC5REF — 0.001A

3D3V_S0 — 5V_S0 — DY — D2402 CH751H-40-1-GP — R2407 10R2J-2-GP — (1uFx1) — C2427 SC1U10V2KX-1GP

VCCSUS3_3_2 N20
VCCSUS3_3_3 N22 — 3D3V_S5 — JE40 modify (1uFx1) — C2428 SC1U6D3V2KX-GP — JE40 modify 07/16
VCCSUS3_3_4 P20
VCCSUS3_3_5 P22

VCC3_3_1 AA16
VCC3_3_8 W16 — 3D3V_S0 — (0.1uFx2) — C2430 SCD1U10V2KX-5GP — C2431 SCD1U10V2KX-5GP
VCC3_3_4 T34

R2414 909R2F-GP — 3D3V_S5 — DY — 1D05V_S5 — R2402 750R2F-GP — DY

VCC3_3_2 AJ2 — 3D3V_S0 — (0.1uFx1) — C2429 SCD1U10V2KX-5GP

VCCIO5 AF13
VCCIO12 AH13 — 1D05V_VTT — (1uFx1)
VCCIO13 AH14
VCCIO6 AF14 — C2432 SC1U6D3V2KX-GP

VCCAPLLSATA AK1 — VCCAPLLSATA — TPAD14-OP-GP TP27

VCCVRM1 AF11 — VCCVRM

3D3V_S5 — U2401 G9090-150T11U-GP (VIN GND EN VOUT NC#4) — 1D05V_S5 — C2436 SC1U10V3Y-6GP — C2416 SC1U10V3Y-6GP — C2405 SC1U6D3V5KX-1GP — 74.09090.A3F

SATA

VCCIO2 AC16
VCCIO3 AC17
VCCIO4 AD17 — 1D05V_VTT — JE40 modify (1uFx1) — C2435 SC1U6D3V2KX-GP

MISC

1D05V_M — VCCASW22 T21
VCCASW23 V21
VCCASW21 T19

+3VS_+1.5VS_HDA_IO — R2409 DY 0R3J-0-U-GP — 3D3V_S5
R2415 DY 0R3J-0-U-GP — 1D05V_S0
R2413 0R0603-PAD — 1D05V_S5
0308 -1

HDA

VCCSUSHDA P32 — +3VS_+1.5VS_HDA_IO — 0.01A — (0.1uFx1) — C2433 SCD1U10V2KX-5GP

CPU

1D05V_VTT — 0.08A (1uFx1) (220uFx1) — +1.05VS_VCCA_A_DPL — IND-10UH-218-GP L2402 — 68.10050.10Y — 2nd = 68.10090.10B — C2409 SC1U6D3V2KX-GP

0.08A (1uFx1) (220uFx1) — +1.05VS_VCCA_B_DPL — IND-10UH-218-GP L2403 — 68.10050.10Y — 2nd = 68.10090.10B — C2410 SC1U6D3V2KX-GP

RTC

RTC_AUX_S5 — 6uA

<Variant Name>

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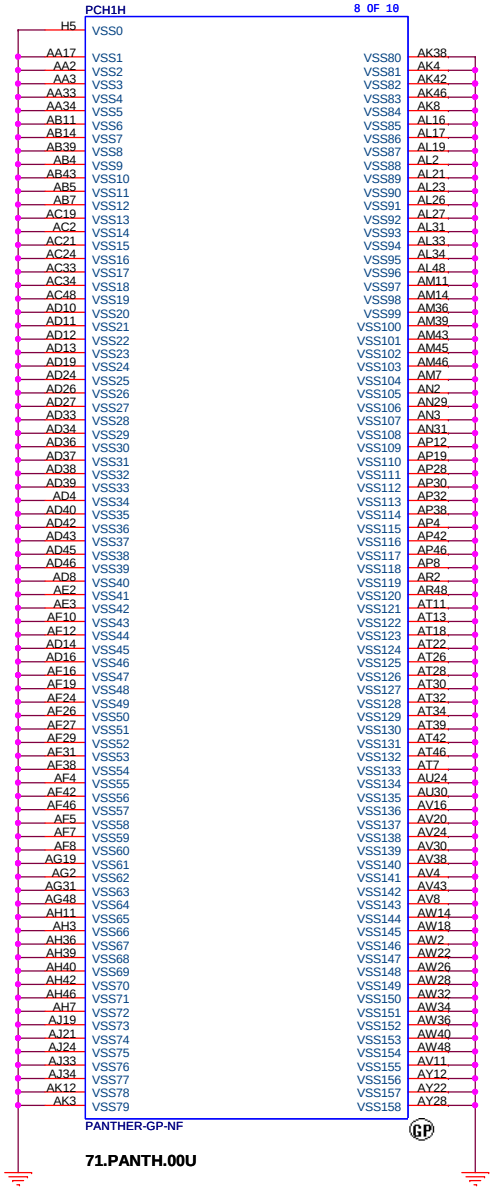
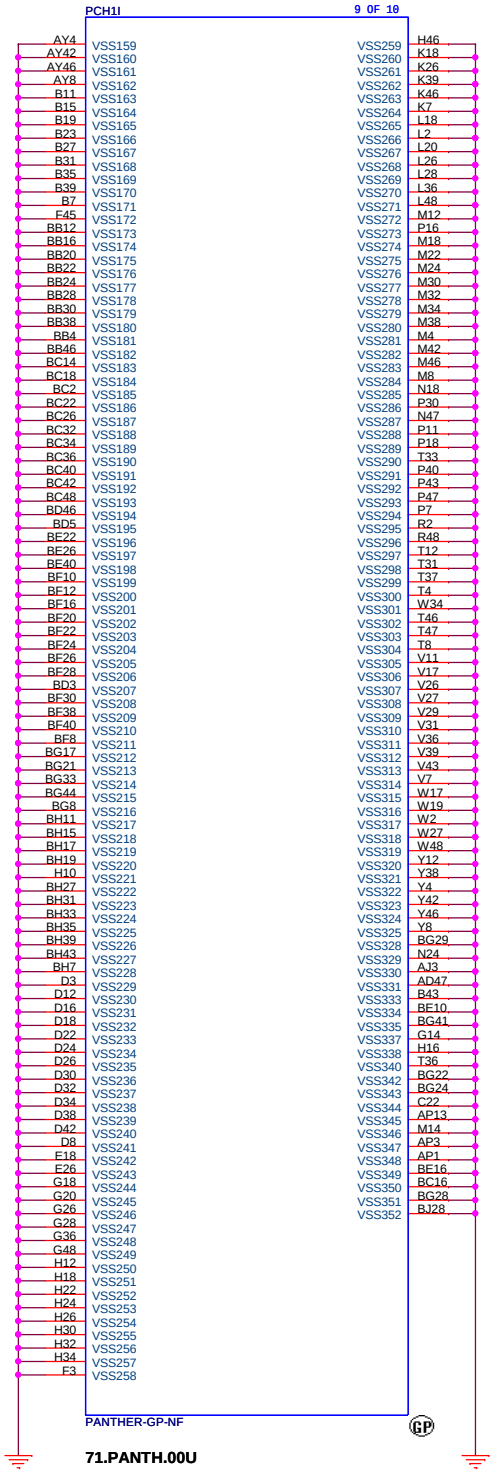
Title: **PCH (POWER2)**

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 — Sheet 24 of 108

SSID = PCH





<Variant Name>

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Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 25 of 108

<variant_name><Variant Name></variant_name>

緯創資通

Wistron Corporation

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Title

Clock(colay)

Size	Document Number	Rev
A4	**BAD40_HC**	**1**

Date: Thursday, April 12, 2012 Sheet 26 of 108

SSID = KBC

H:MIC UNMUTE/L:MIC MUTE

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-1	100.0K	64.9K	2.0V
-2	100.0K	76.8	1.87V
-3	100.0K	100.0K	1.65V

1227 SC
Del USB_CHARGER_STATUS#

1108 SC

SB 0923

0207 SD

0302 -1

SB 0915 for KBC885

0131 SD

1128 SC

1220 SC

1227 SC

TP

BATTERY / CHARGER

PCH / EDP

0604 Modify:
RN2704 pull-Low 10K Resistor to DY on BLUETOOTH_EN.

SB LID_CLOSE# can not pull high, because push pull suggest RN2708 Pin5 change FAN_TACH1

NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

1st = 71.00885.A0G

71.00795.00G

2nd = 84.03906.F11

Prevent BIOS data loss

EC_GPIO47 High Active

2nd = 84.07002.I31

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete

NCT5606Y-0 (Addr: 0x32)

NCT5606Y-0 (Addr: 0x30)

1128 SC for model ID reporting

MODEL_ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
BAD50-HC	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V
BAD40-HC	100.0 K	20.0 K	2.750 V	2.7591	>= 2.616 V < 2.875 V
BAD30-HC	100.0 K	33.0 K	2.481 V	2.4935	>= 2.363 V < 2.616 V

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Title: KBC Nuvoton NPCE795

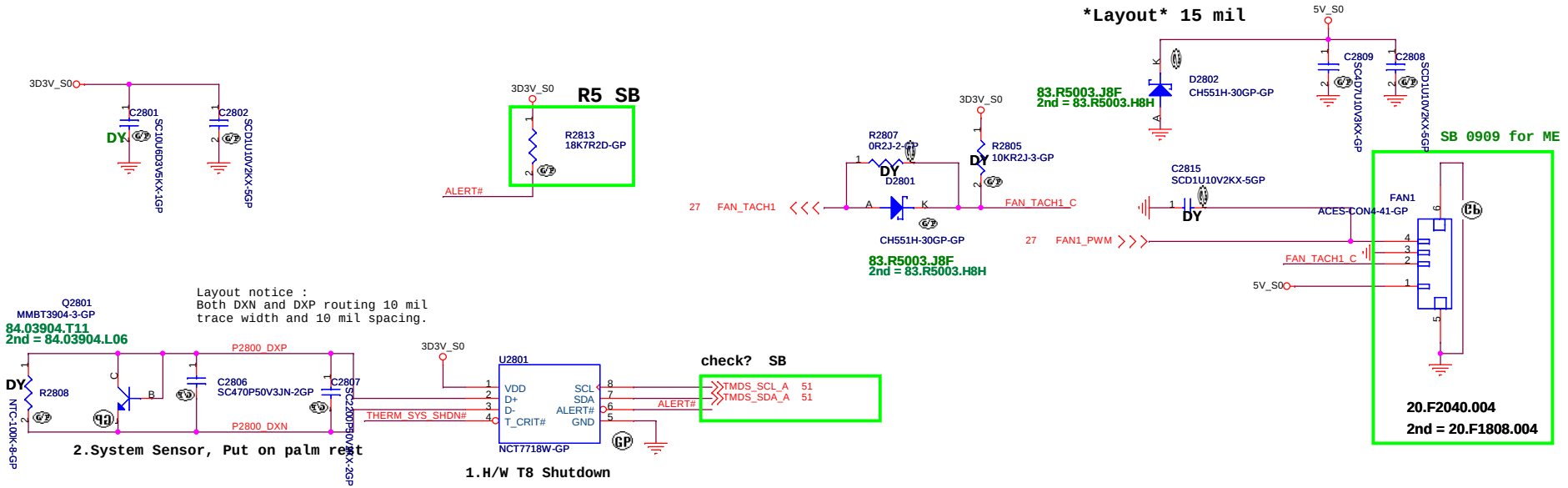
Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 27 of 108

SSID = Thermal

Fan controller P2793

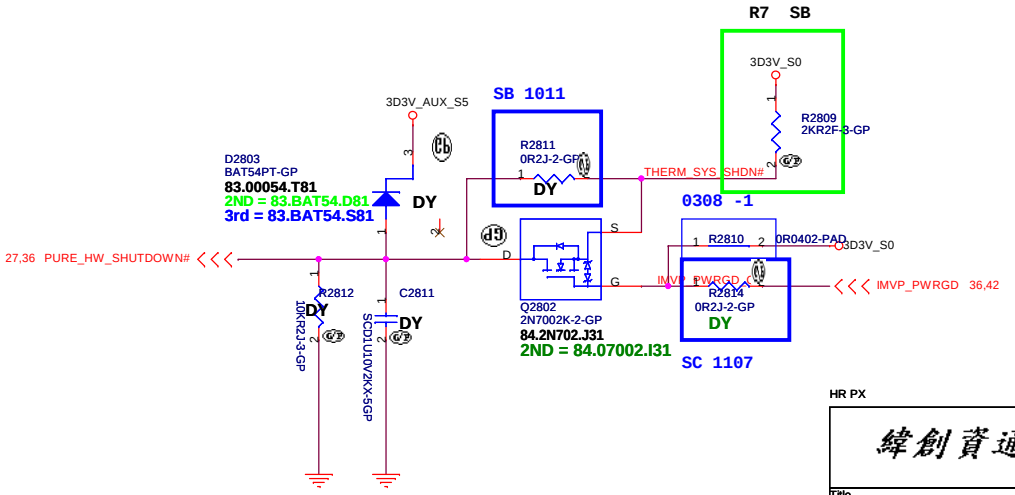
Layout 15 mil



ALERT# /T_CRIT# Pull-up Resistor

R5 \ R7	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77℃	87℃	97℃	107℃	117℃
7.5Kohm	79℃	89℃	99℃	109℃	119℃
10.5Kohm	81℃	91℃	101℃	111℃	121℃
14Kohm	83℃	93℃	103℃	113℃	123℃
18.7Kohm	85℃	95℃	105℃	115℃	125℃

T_CRIT temperature strapping point



HR PX

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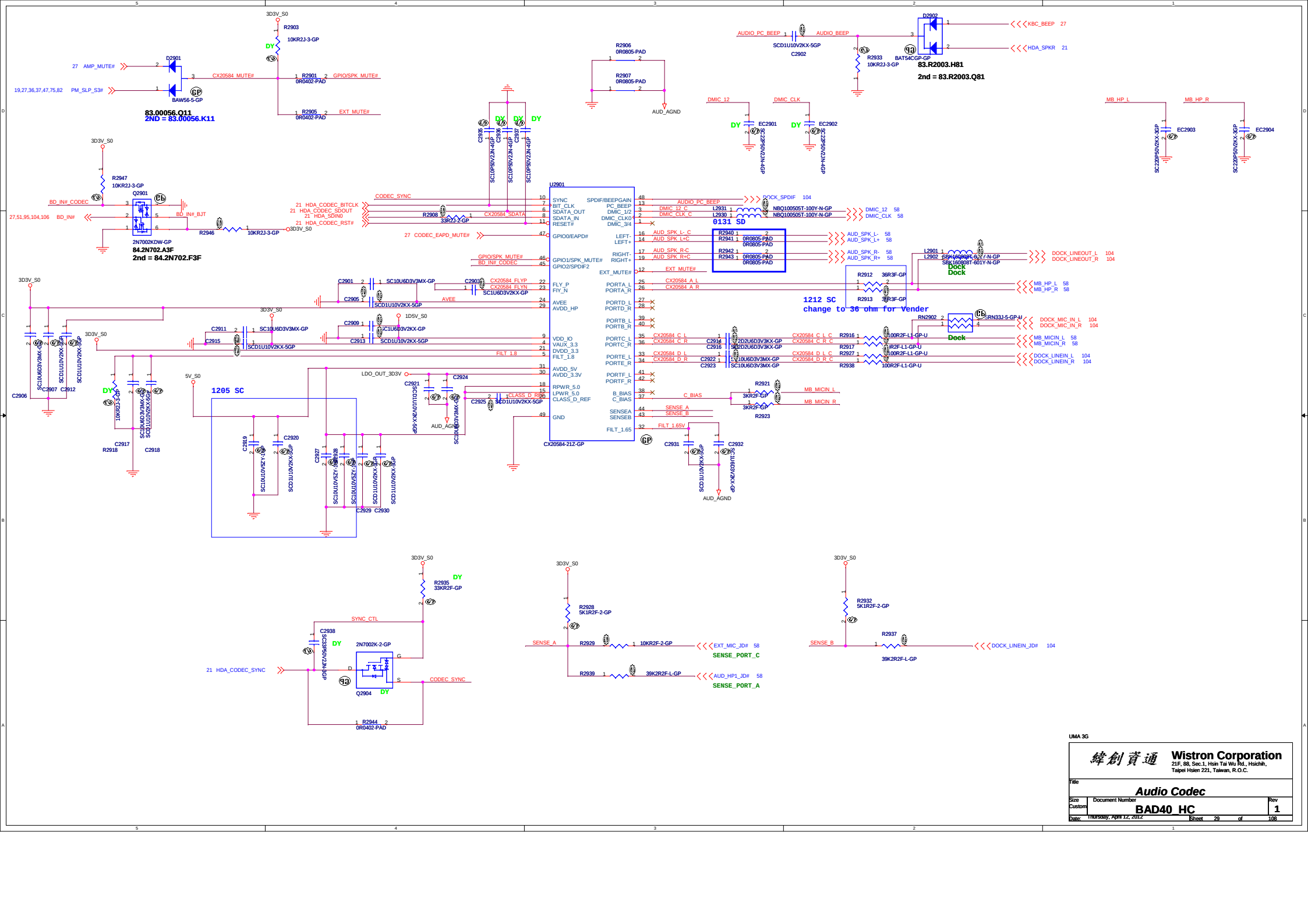
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal T7718/Fan Controllor P2793**

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 28 of 108


U2901
CX20584-21Z-GP
83.00056.Q11
2ND = 83.00056.K11
84.2N702.A3F
2nd = 84.2N702.F3F
83.R2003.H81
2nd = 83.R2003.Q81
0131 SD
1212 SC
change to 36 ohm for Vender
1205 SC
Dock
SENSE_PORT_C
SENSE_PORT_A
Wistron Corporation
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Audio Codec
BAD40_HC
UMA 3G
Thursday, April 12, 2012
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AUDIO OP AMPLIFIER

<Variant Name>

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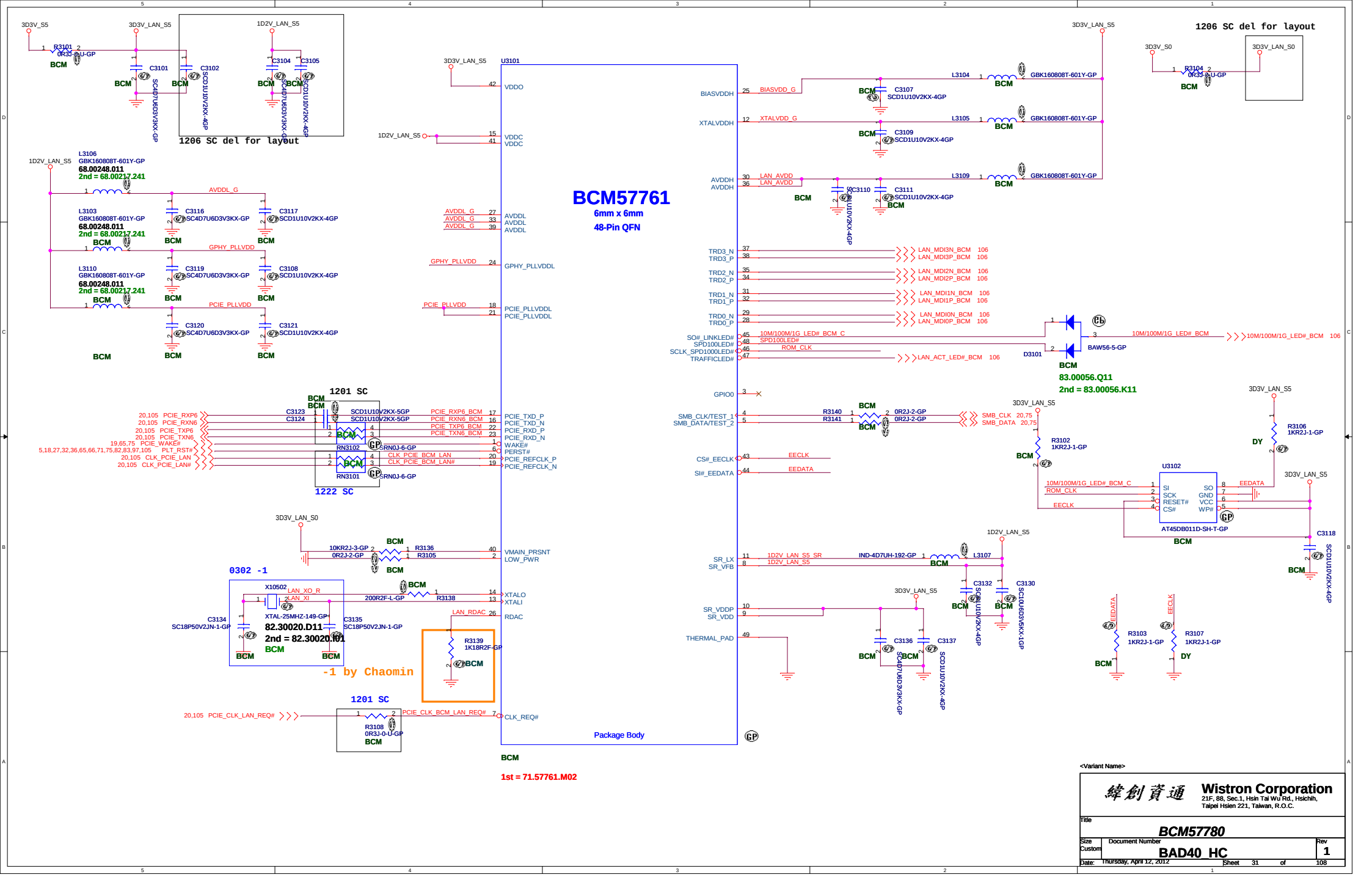
Title
Audio AMP

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 30 of 108


BCM57761
6mm x 6mm
48-Pin QFN
Package Body
U3101
1206 SC del for layout
1201 SC
1222 SC
0302 -1
-1 by Chaomin
1206 SC del for layout
83.00056.Q11
2nd = 83.00056.K11
82.30020.D11
2nd = 82.30020.M01
1st = 71.57761.M02
AT45DB011D-SH-T-GP
D3101
BAW56-5-GP
Wistron Corporation
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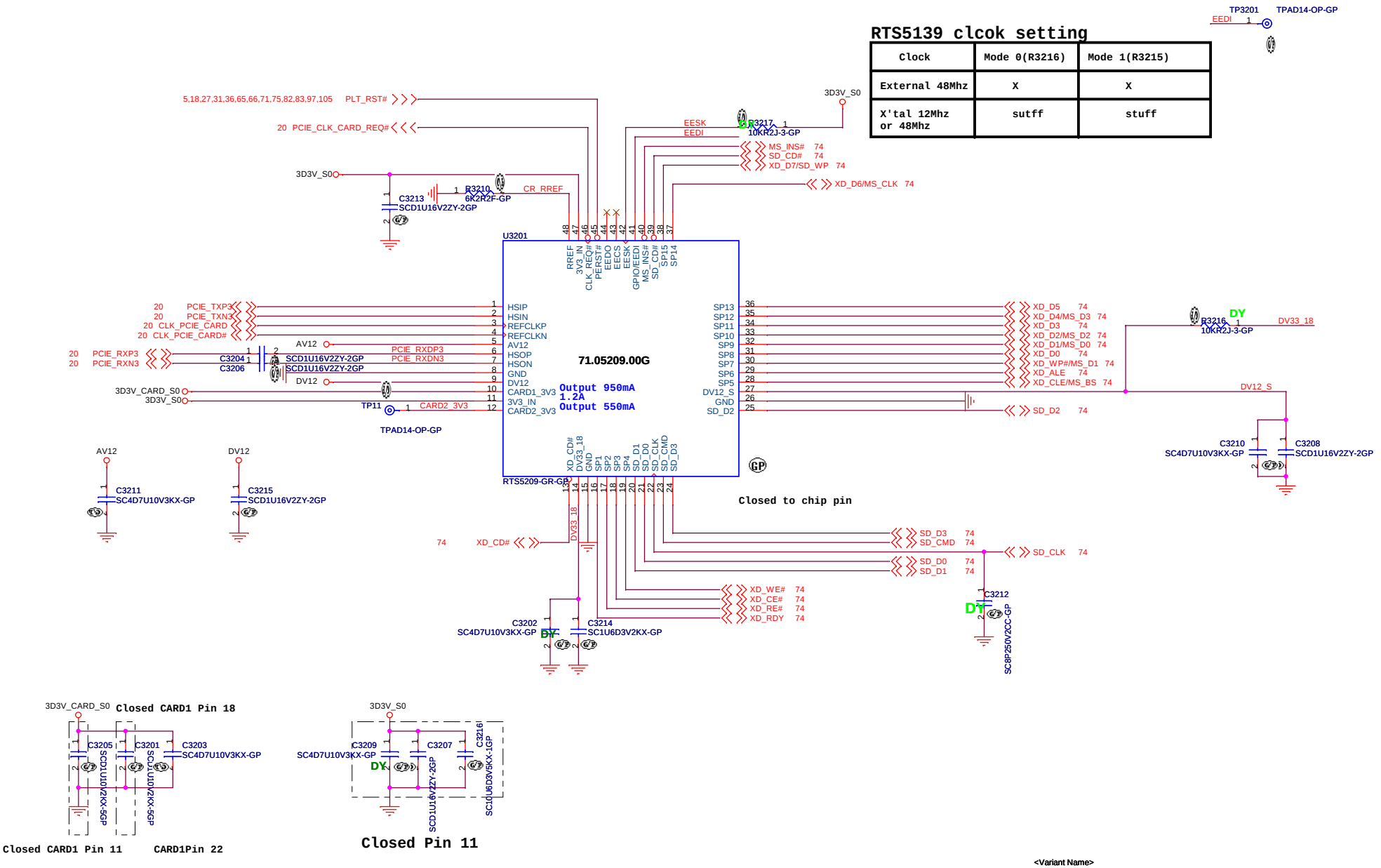
Taipei Hsien 221, Taiwan, R.O.C.
BCM57780
BAD40_HC
Thursday, April 12, 2012
Sheet 31 of 108

RTS5139 clcok setting

Clock	Mode 0(R3216)	Mode 1(R3215)
External 48Mhz	X	X
X'tal 12Mhz or 48Mhz	sutff	stuff



<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RTS5209(CARD READER)***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 32 of 108

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 33 of 108

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 34 of 108

reserve

HR

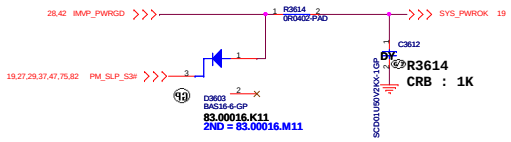
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

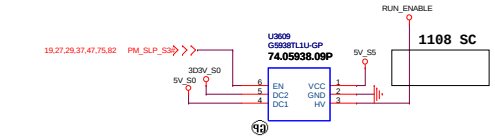
Size	Document Number	Rev
Custom	BAD40_HC	1

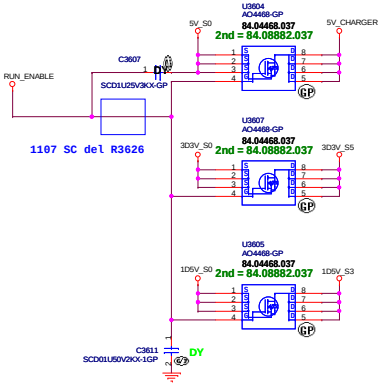
Date: Thursday, April 12, 2012 Sheet 35 of 108

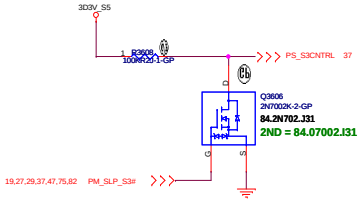
Power Sequence

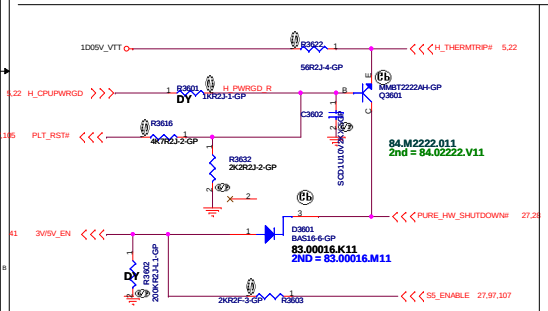


ANNIE Run Power

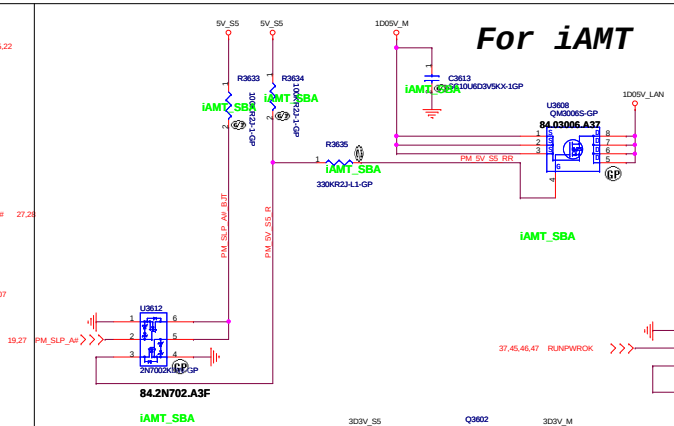


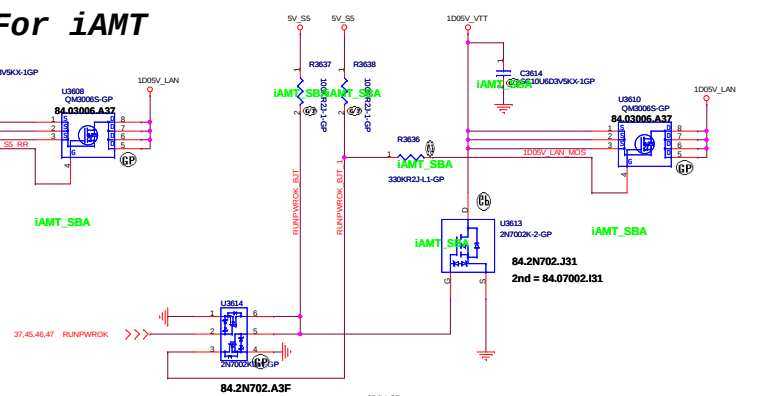






For iAMT

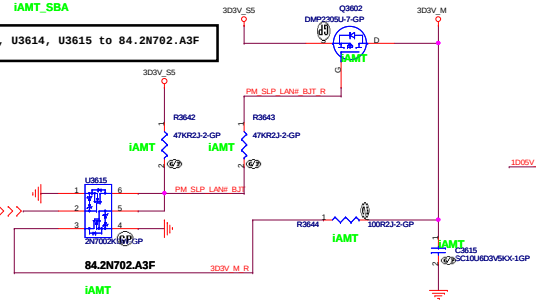


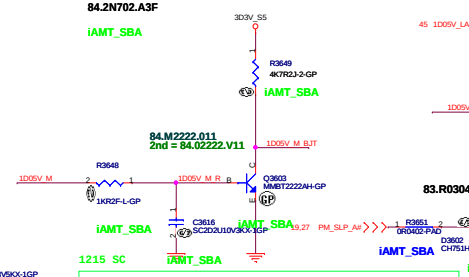


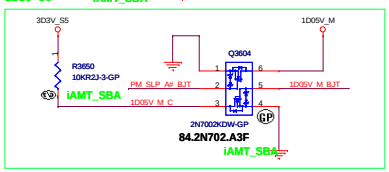
0312 -1 del for layout

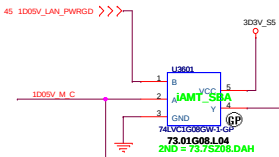
0412 -1M del for layout

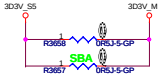
change U3612, U3614, U3615 to 84.2N702.A3F
0822 SB











HR PX

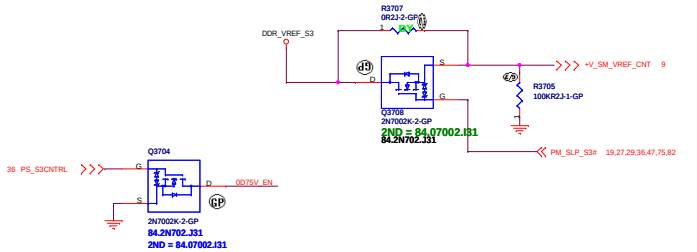
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

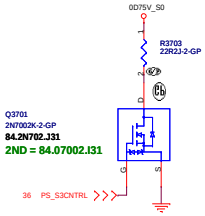
Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 36 of 108

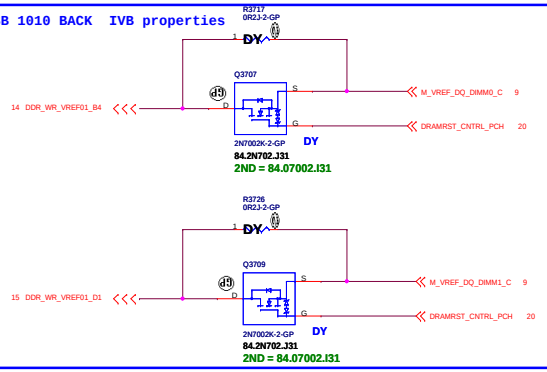
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

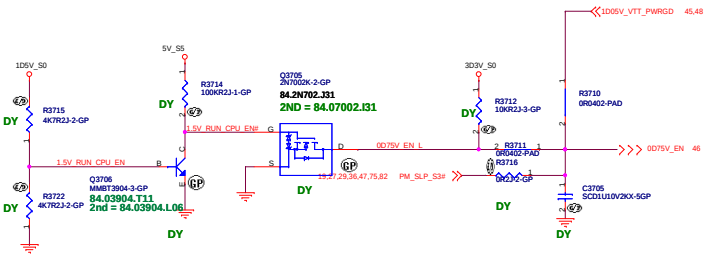


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

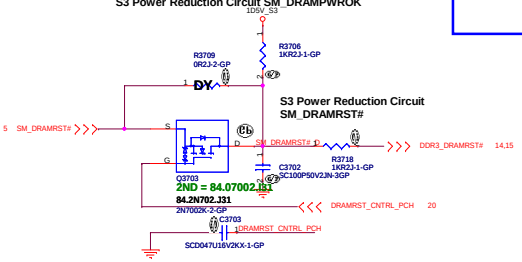


SB 1010 BACK IVB properties



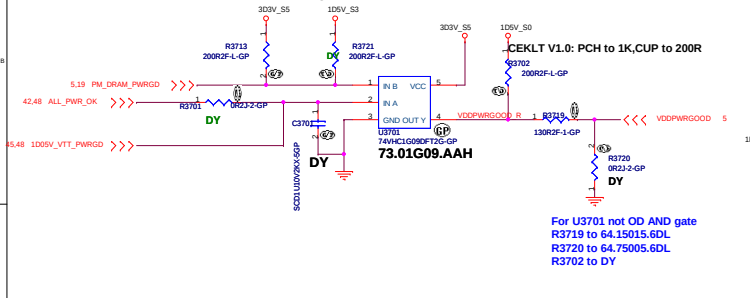


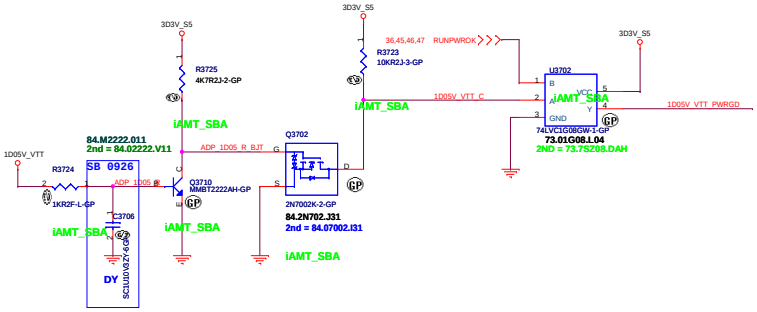
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

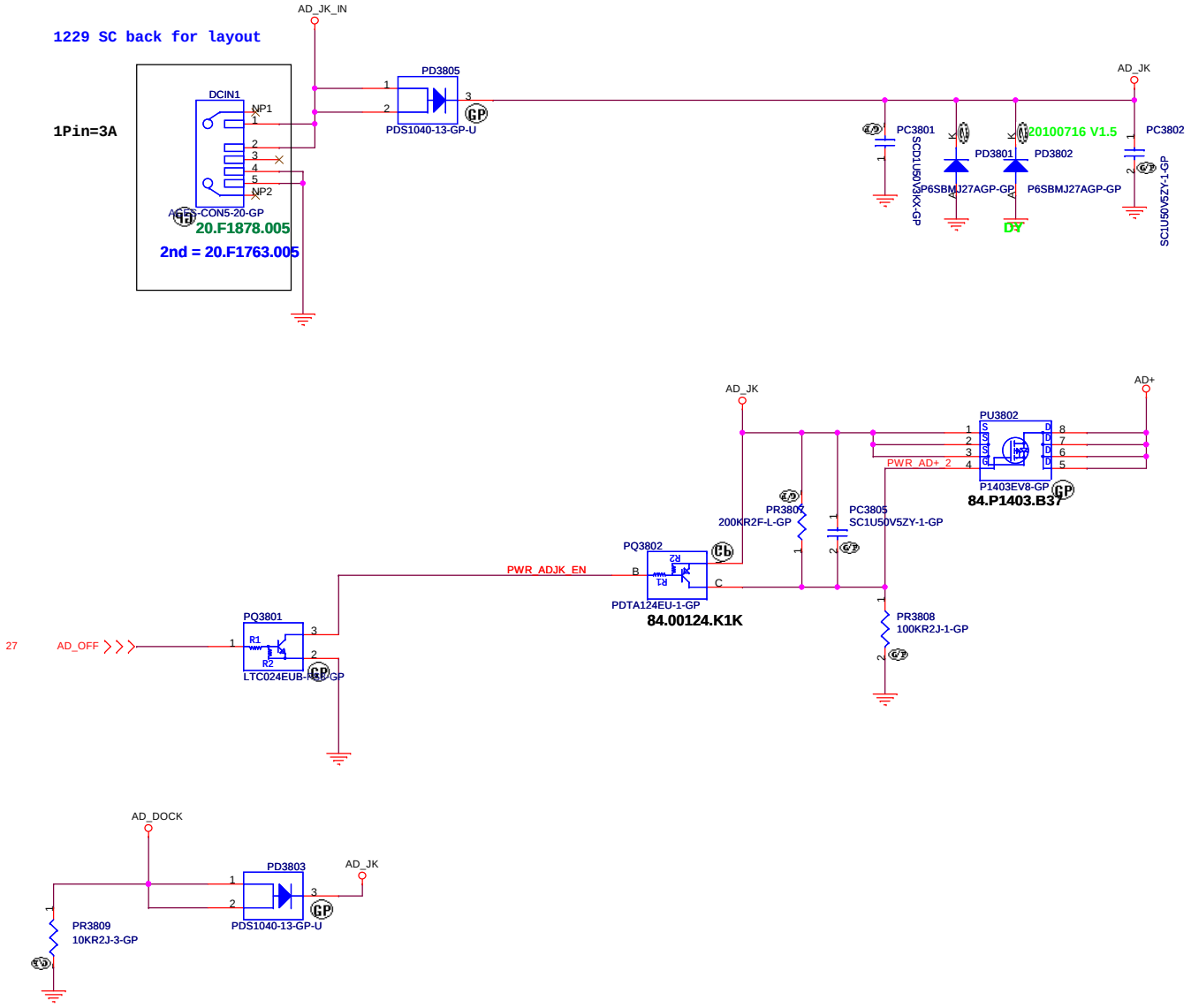
SB





HR PX
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER
Size: Custom | Document Number: BAD40_HC | Rev: 1
Date: Thursday, April 12, 2012 | Sheet 37 of 108



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DCIN JACK***

Size	Document Number	Rev
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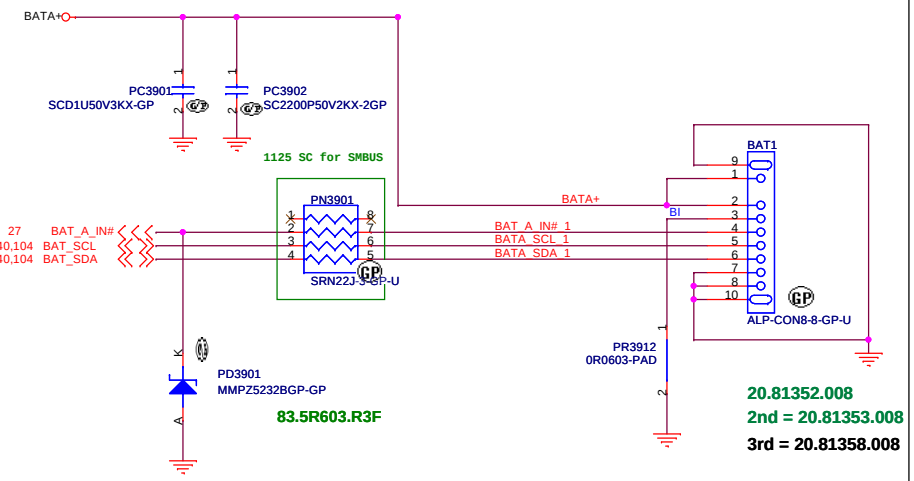
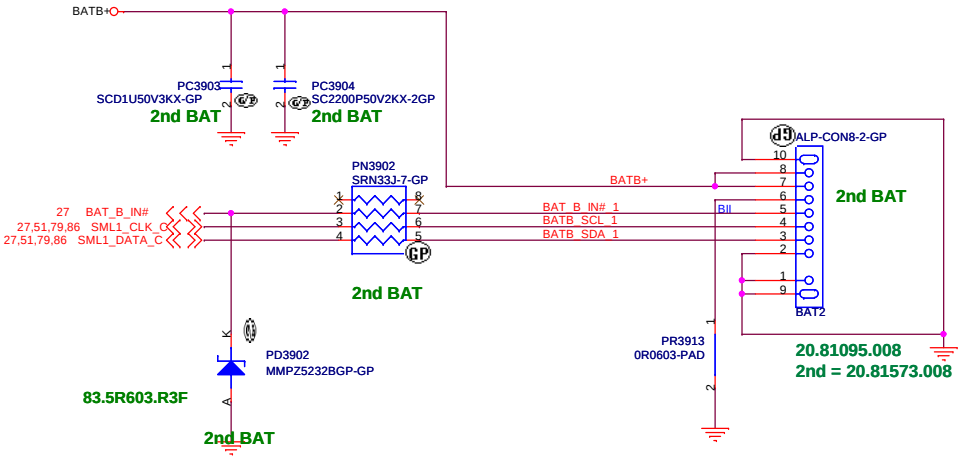
Date: Thursday, April 12, 2012 Sheet 38 of 108

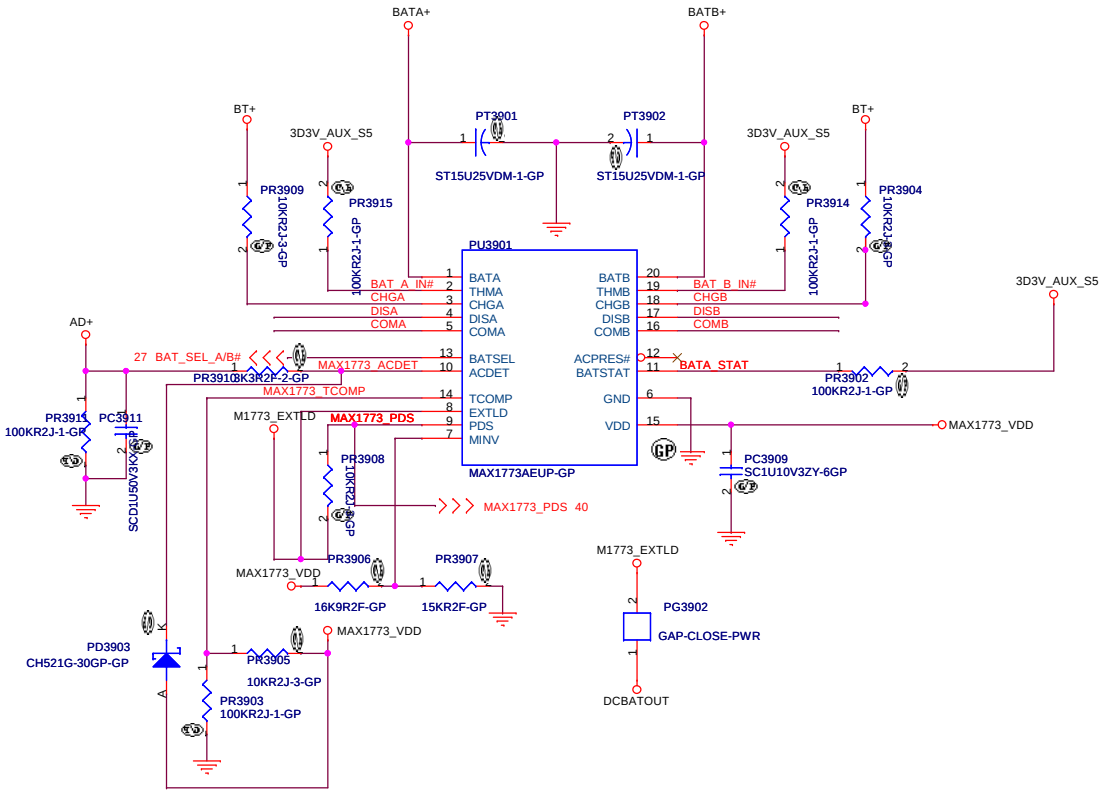
MAIN BATTERY CONNECTOR



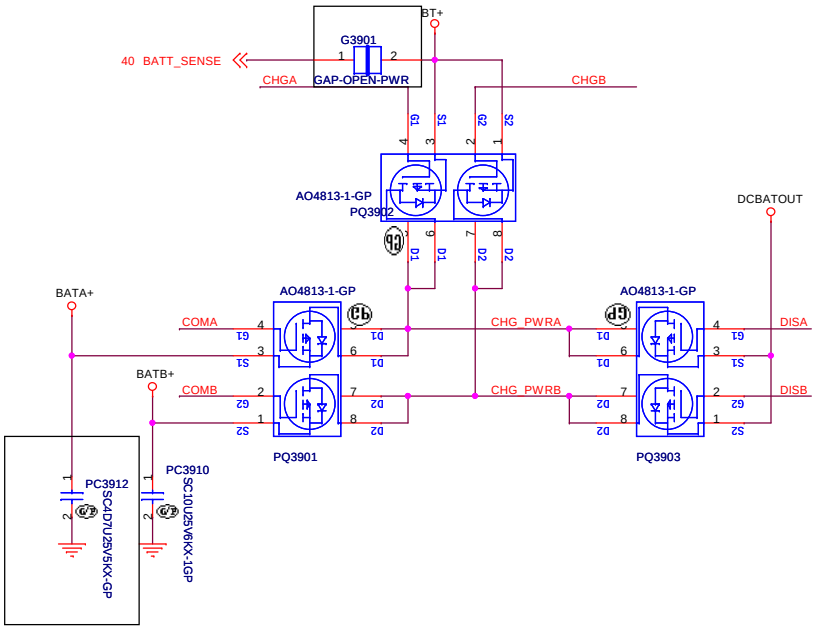
2nd BATTERY CONNECTOR



BATTERY SWITCH



1108 SC



0913 SB

HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT_CONN

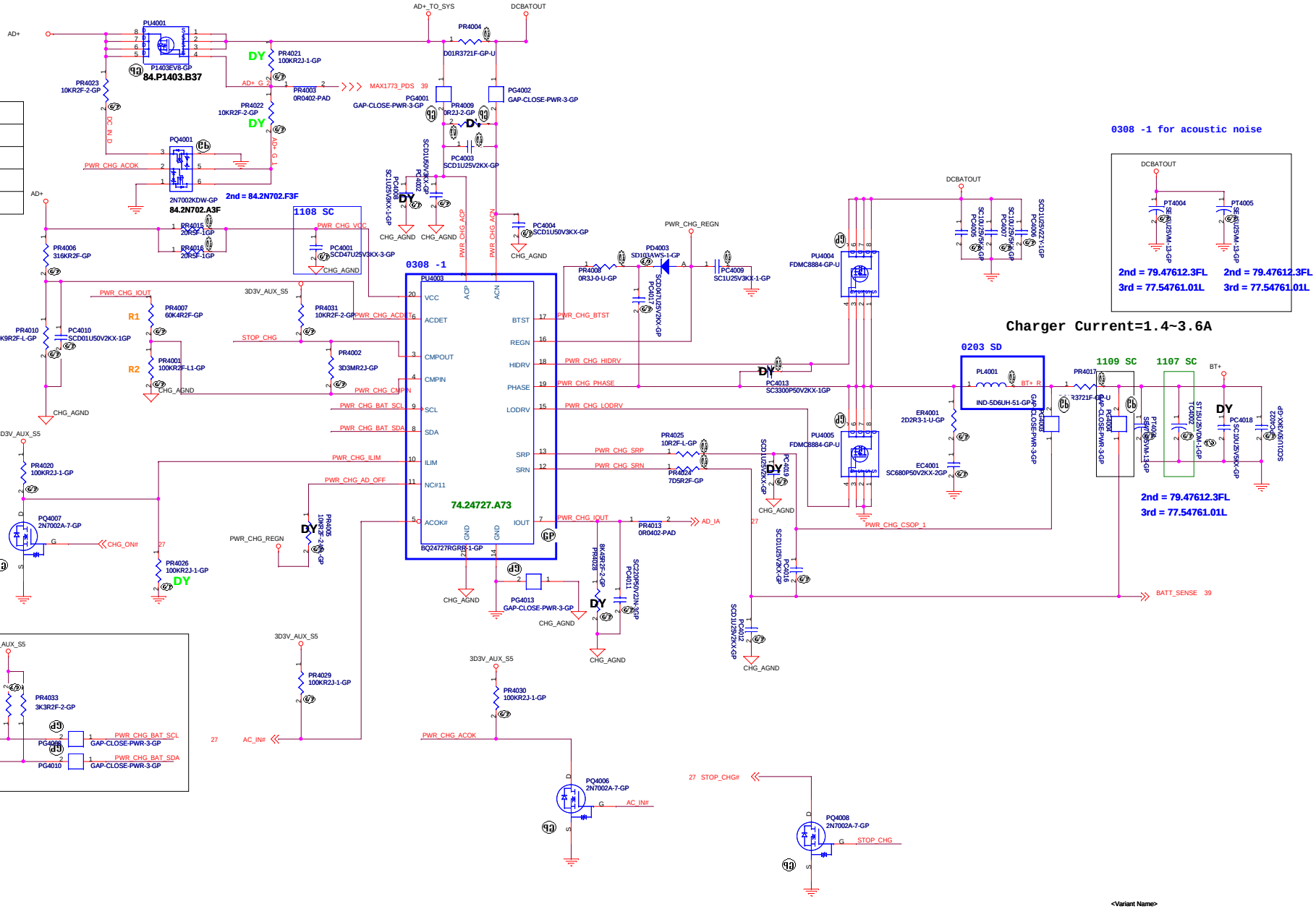
Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 39 of 108

SSID = Charger

A8(ANNIE/ASTRO)
PR4014,PR4016

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



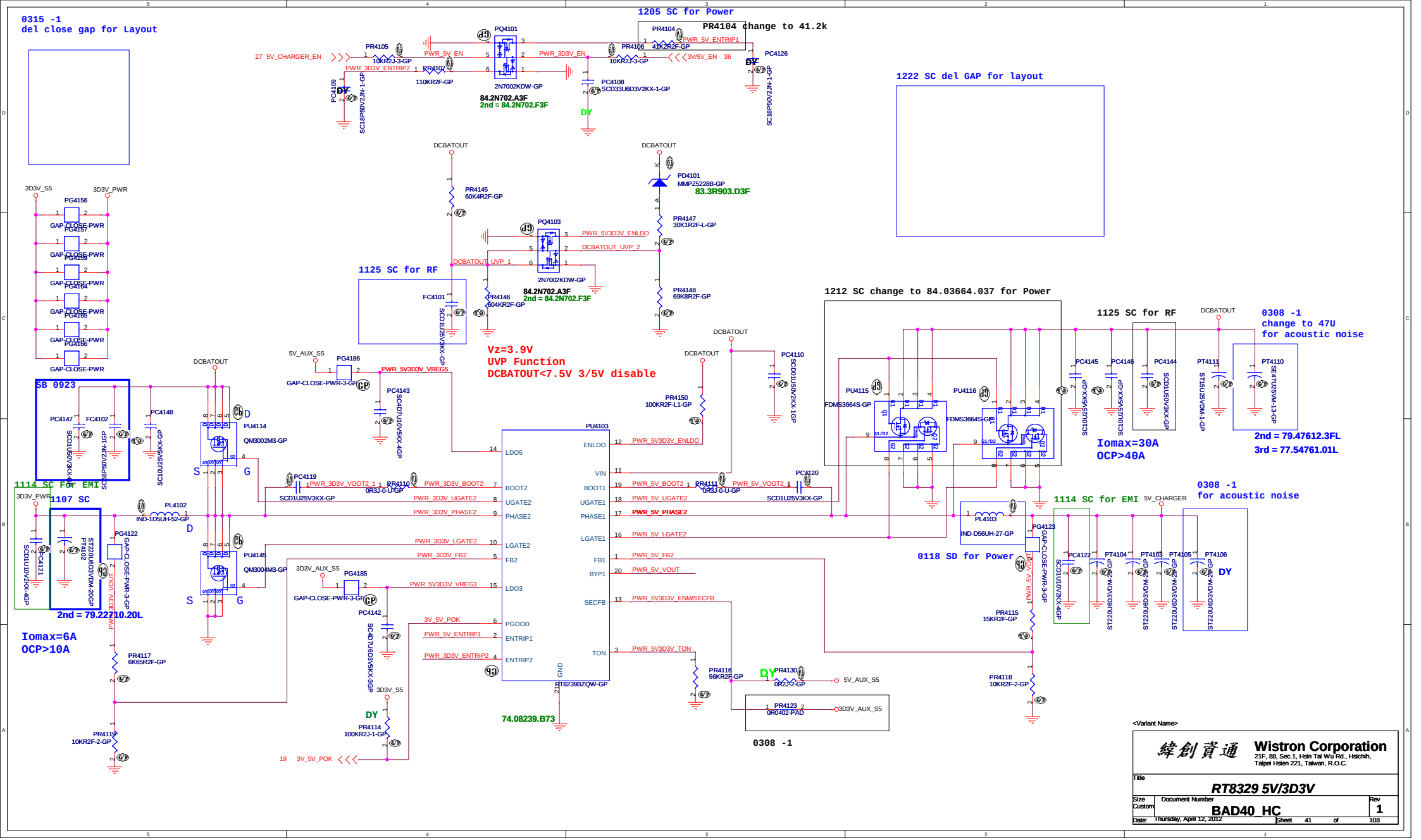
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24707A

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 40 of 108


0315 -1
del close gap for Layout
1205 SC for Power
PR4104 change to 41.2k
PQ4101
PR4105
10KR2J-3-GP
PR4102
110KR2F-GP
2N7002KDW-GP
PR4106
41K2R2F-GP
10KR2J-3-GP
PC4108
SCD33U6D3V2KX-1-GP
PC4109
SC18P50V2JN-1-GP
PC4126
SC18P50V2JN-1-GP
84.2N702.A3F
2nd = 84.2N702.F3F
DY
1222 SC del GAP for layout
DCBATOUT
PR4145
60K4R2F-GP
PD4101
MMPZ5228B-GP
83.3R903.D3F
PR4147
30K1R2F-L-GP
PR4148
69K8R2F-GP
PQ4103
PWR_5V3D3V_ENLDO
DCBATOUT_UVP_2
DCBATOUT_UVP_1
2N7002KDW-GP
84.2N702.A3F
2nd = 84.2N702.F3F
1125 SC for RF
FC4101
PR4146
604KR2F-GP
Vz=3.9V
UVP Function
DCBATOUT<7.5V 3/5V disable
1212 SC change to 84.03664.037 for Power
1125 SC for RF
0308 -1
change to 47U
for acoustic noise
2nd = 79.47612.3FL
3rd = 77.54761.01L
Iomax=30A
OCP>40A
PU4115
PU4116
FDMS3664S-GP
PC4145
PC4146
PC4144
PT4111
PT4110
3D3V_S5
3D3V_PWR
PG4156
GAP-CLOSE-PWR
PG4157
PG4159
PG4164
PG4165
PG4166
SB 0923
PC4147
FC4102
PC4148
PU4114
QM3002M3-GP
5V_AUX_S5
PG4186
GAP-CLOSE-PWR-3-GP
PWR_5V3D3V_VREG5
PC4143
SCD47U10V9KX-4GP
PC4110
PR4150
100KR2F-L1-GP
1114 SC For EMI
1107 SC
PC4119
PWR_3D3V_VOOT2_1
PR4110
0R3J-0-U-GP
PWR_3D3V_BOOT2
PWR_3D3V_UGATE2
PWR_3D3V_PHASE2
PWR_3D3V_LGATE2
PWR_3D3V_FB2
PWR_3D3V_VREG3
3V_5V_POK
PWR_5V_ENTRIP1
PWR_3D3V_ENTRIP2
PU4103
ENLDO
VIN
BOOT1
UGATE1
PHASE1
LGATE1
FB1
BYP1
SECFB
TON
PGOOD
ENTRIP1
ENTRIP2
LDO5
BOOT2
UGATE2
PHASE2
LGATE2
FB2
LDO3
RT8239BZQW-GP
PWR_5V_BOOT2
PWR_5V_UGATE2
PWR_5V_PHASE2
PWR_5V_LGATE2
PWR_5V_FB2
PWR_5V_VOUT
PWR_5V3D3V_ENLDO
PWR_5V3D3V_ENM/SECFB
PWR_5V3D3V_TON
PC4120
SCD1U25V3KX-GP
PL4102
IND-1D5UH-32-GP
PL4103
IND-D56UH-27-GP
PG4122
PG4123
PC4121
PT4102
ST220U6D3VDM-20GP
PC4122
PT4104
PT4103
PT4105
PT4106
ST220U6D3VDM-2GP
0118 SD for Power
0308 -1
for acoustic noise
1114 SC for EMI
5V_CHARGER
2nd = 79.22710.20L
Iomax=6A
OCP>10A
PR4117
6K65R2F-GP
PR4119
10KR2F-2-GP
PU4145
QM3004M3-GP
3D3V_AUX_S5
PG4185
PC4142
SC47U6D3V5KX-3GP
PR4114
100KR2J-1-GP
3V_5V_POK
19
PR4116
56KR2F-GP
PR4130
0R2J-2-GP
5V_AUX_S5
PR4123
0R0402-PAD
3D3V_AUX_S5
74.08239.B73
0308 -1
PR4115
15KR2F-GP
PR4118
10KR2F-2-GP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8329 5V/3D3V
Size
Custom
Document Number
BAD40_HC
Rev
1
Date: Thursday, April 12, 2012
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SSID = CPU.Regulator

0207 SD
for DC S5 leakage

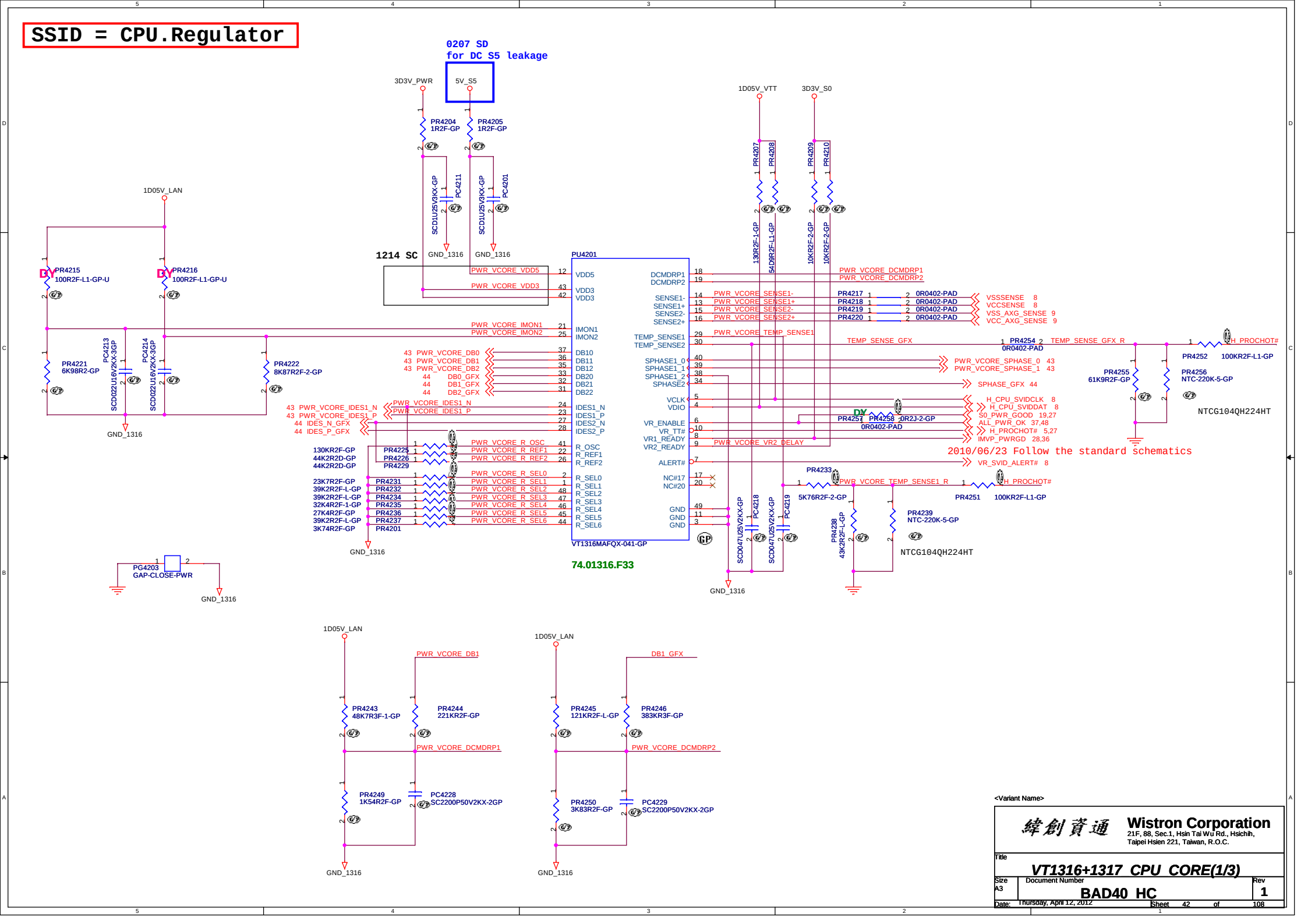
1214 SC

PU4201

VT1316MAFQX-041-GP

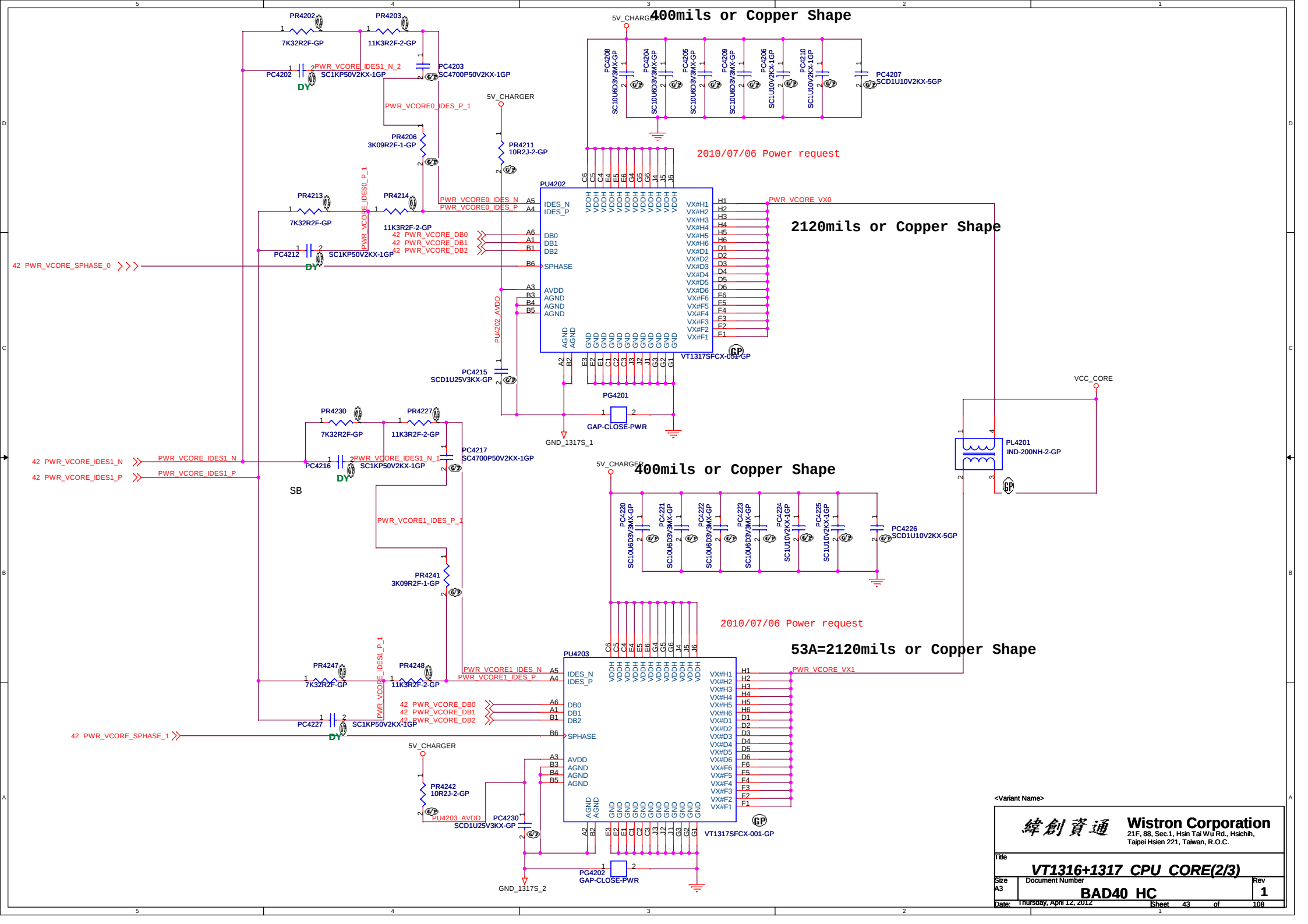
74.01316.F33

2010/06/23 Follow the standard schematics



<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	VT1316+1317 CPU CORE(1/3)	
Size A3	Document Number BAD40 HC	Rev 1
Date: Thursday, April 12, 2012	Sheet 42 of 108	



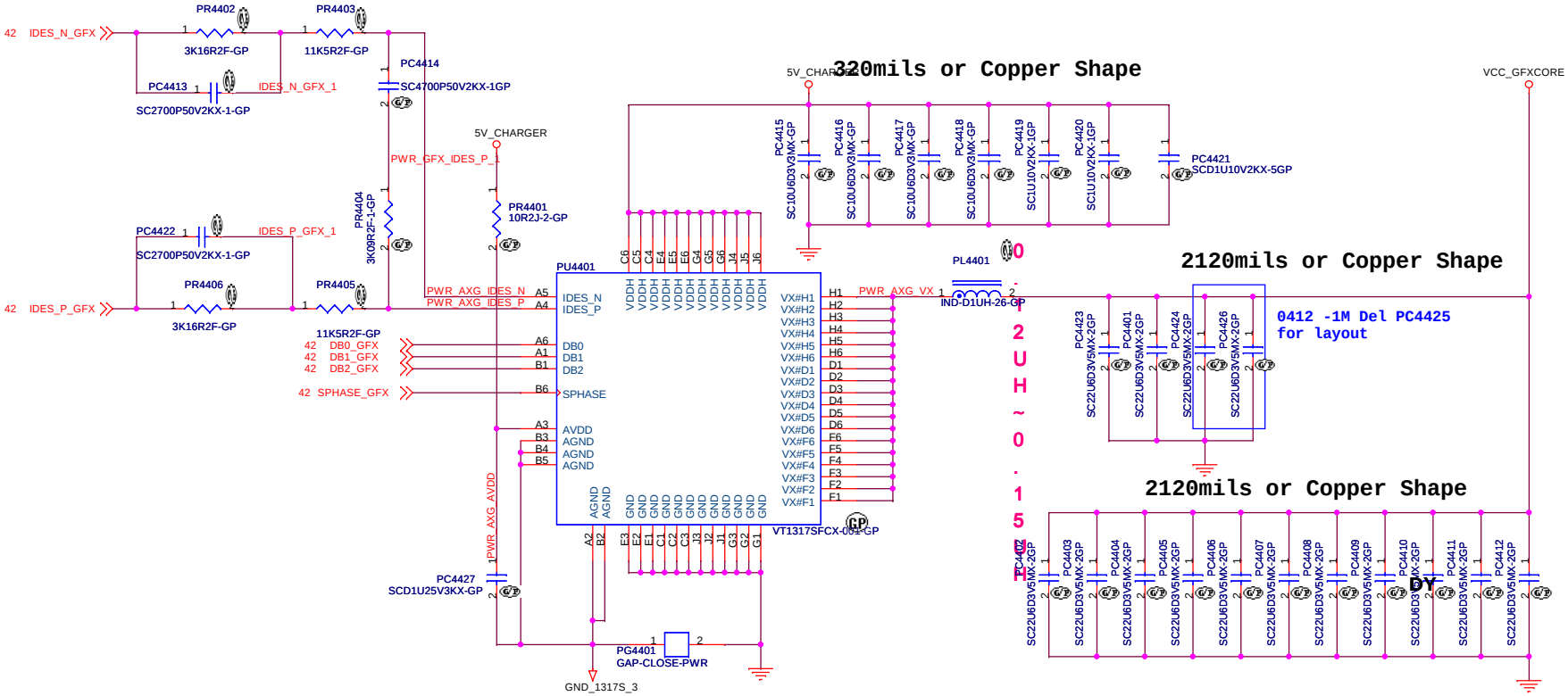
<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1317 CPU CORE(2/3)

Size	Document Number	Rev
A3	BAD40 HC	1

Date: Thursday, April 12, 2012 Sheet 43 of 108



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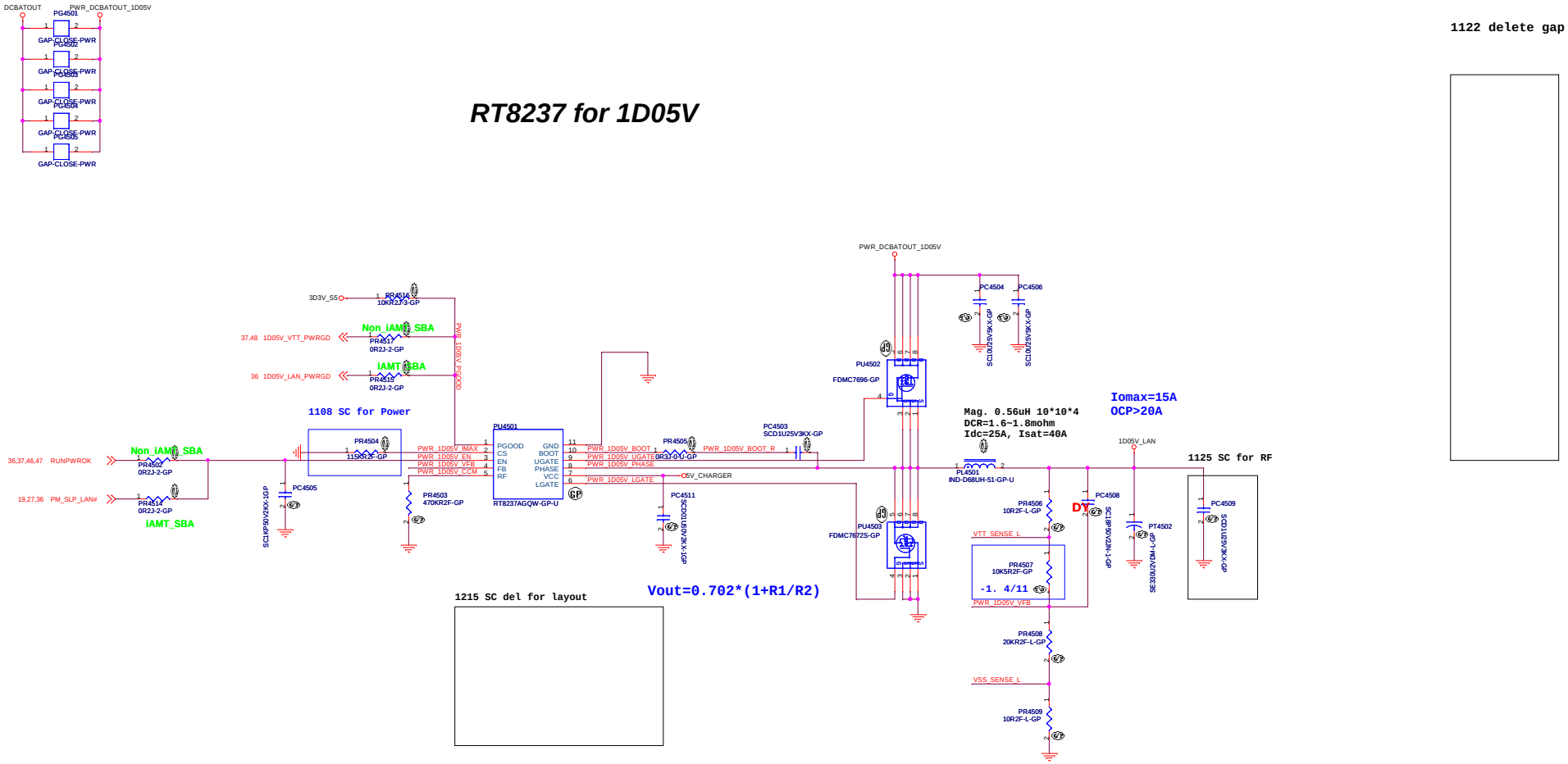
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	VT1316+1317 CPU CORE(3/3)	
Size A3	Document Number BAD40 HC	Rev 1
Date: Thursday, April 12, 2012	Sheet 44 of 108	

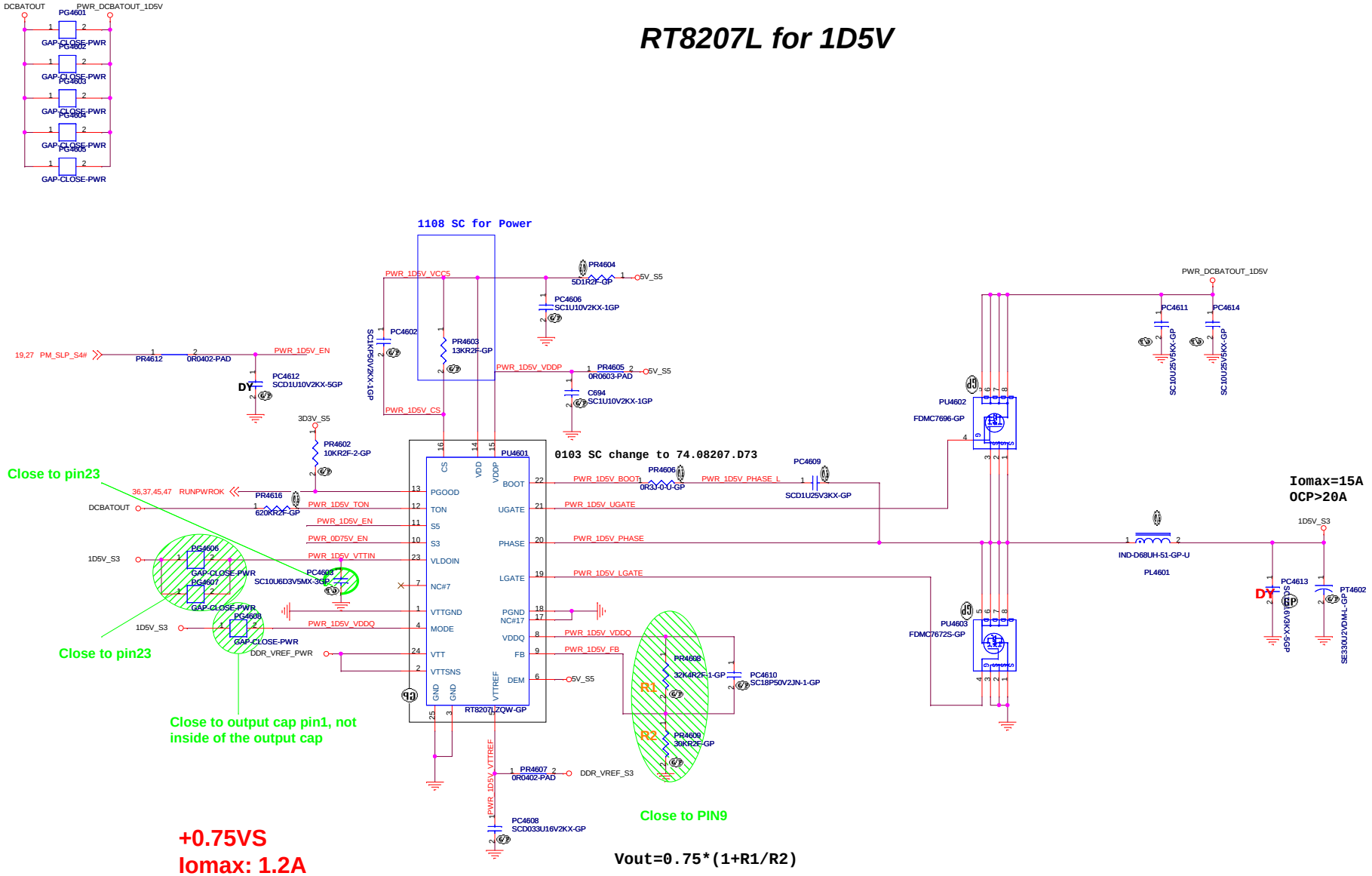


<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DC to DC 1D05V(RT8237)		
Size: A2	Document Number: BAD40_HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 45 of 108	

SSID = PWR.Plane.Regulator_1p5v0p75v

RT8207L for 1D5V



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

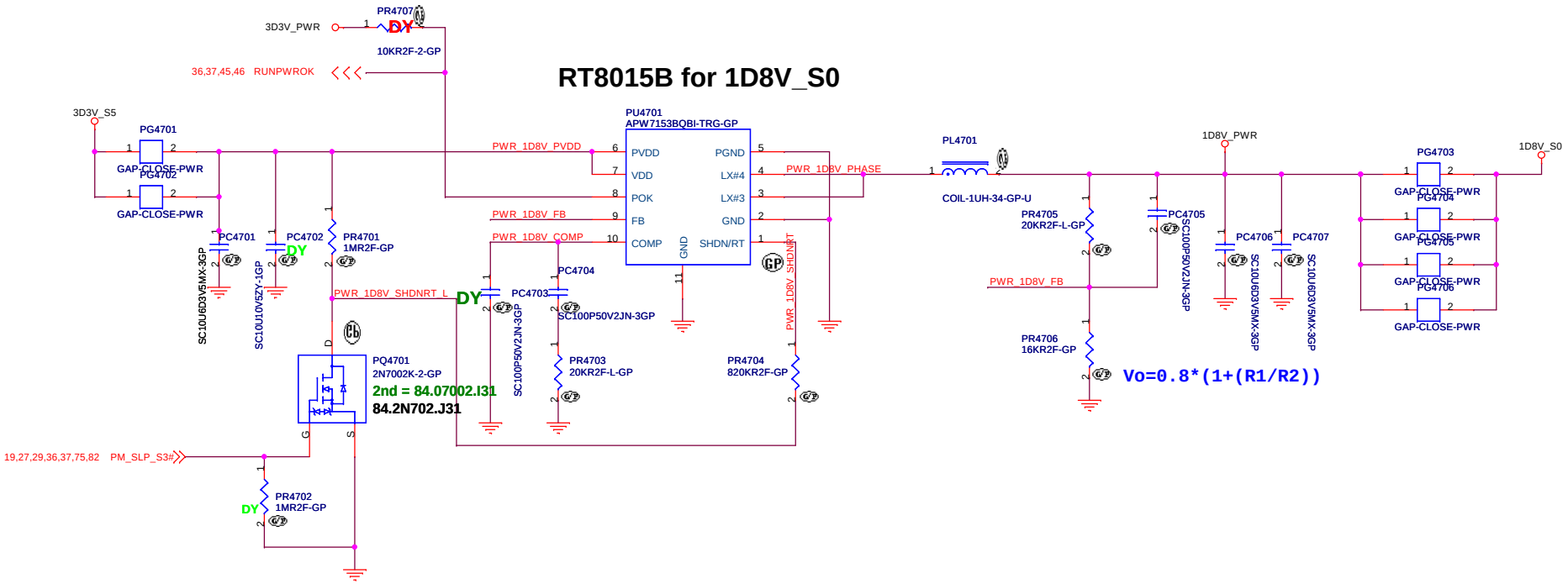
<Variant Name>

Title: RT8207L_+1.5V_SUS

Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 46 of 108

SSID = PWR.Plane.Regulator_1p8v



<Variant Name>

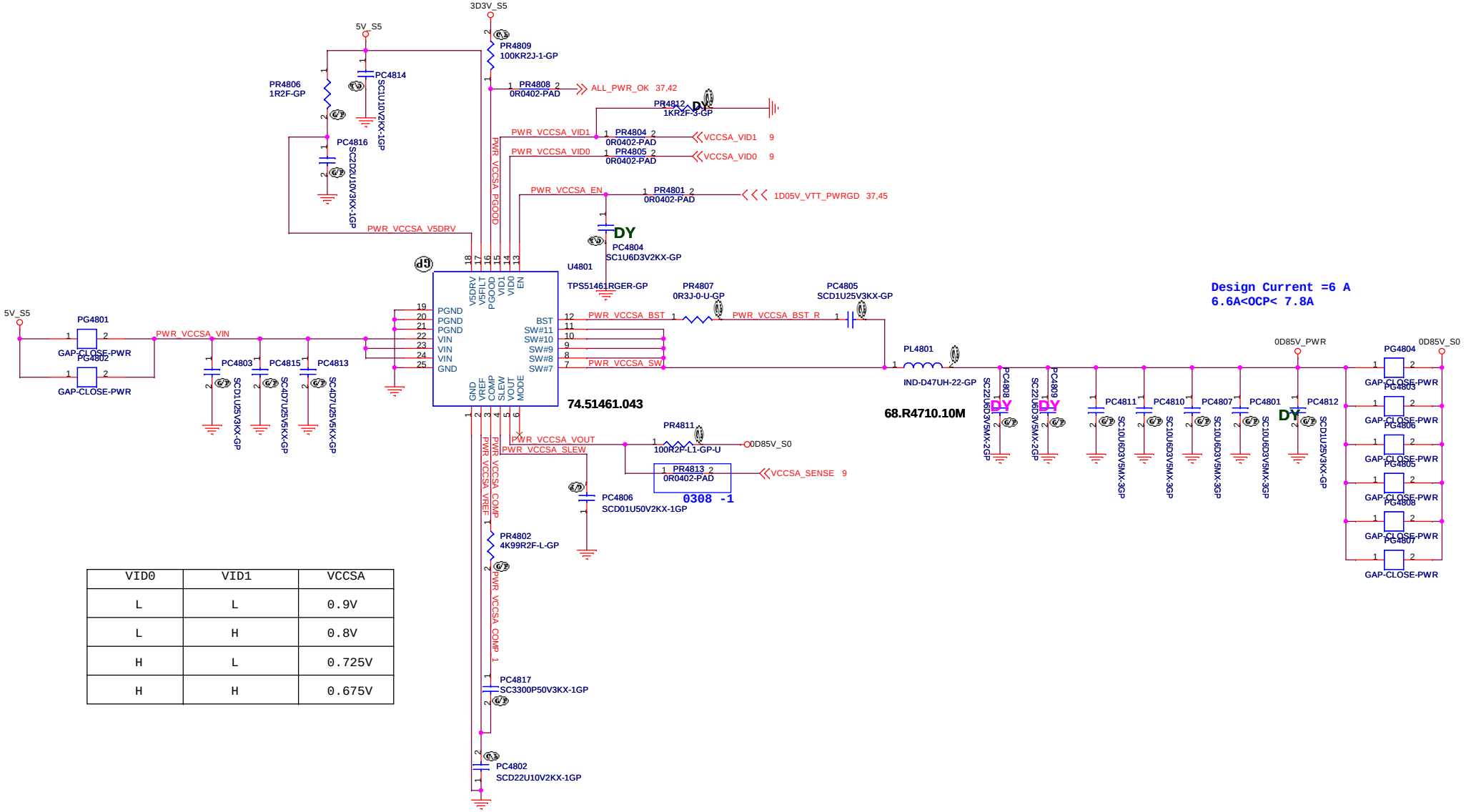
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC CONVERTER 1D8V(RT8015A)

Size: A3 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 47 of 108

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC CONVERTER VCCSA(TPS51461)

Size	Document Number	Rev
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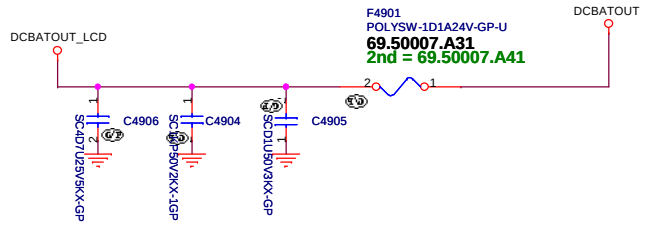
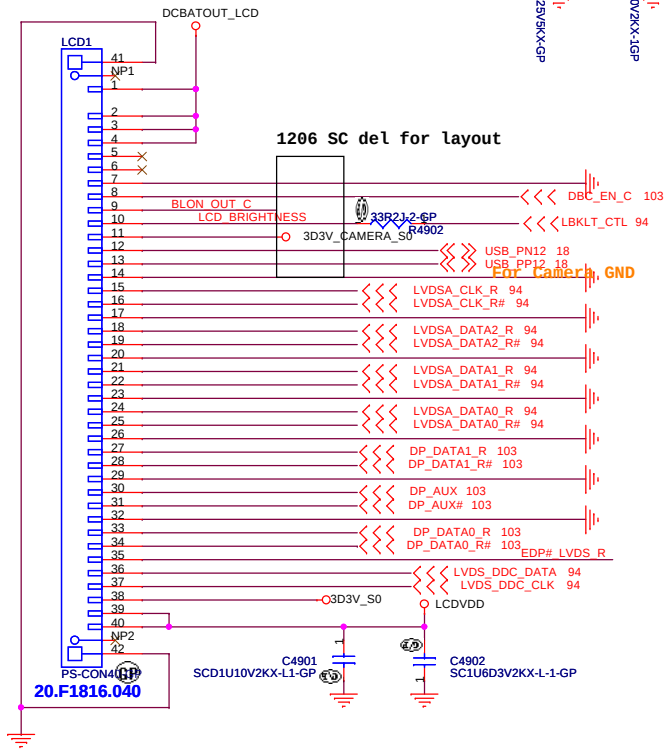
SSID = VIDEO

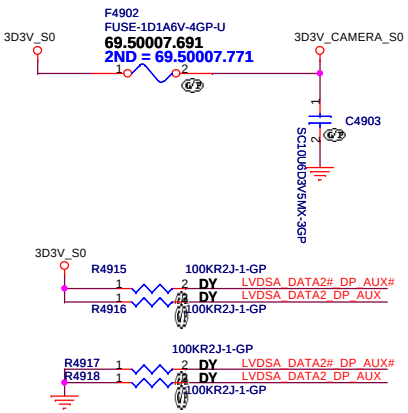
INVERTER POWER



LVDS CONNECTOR

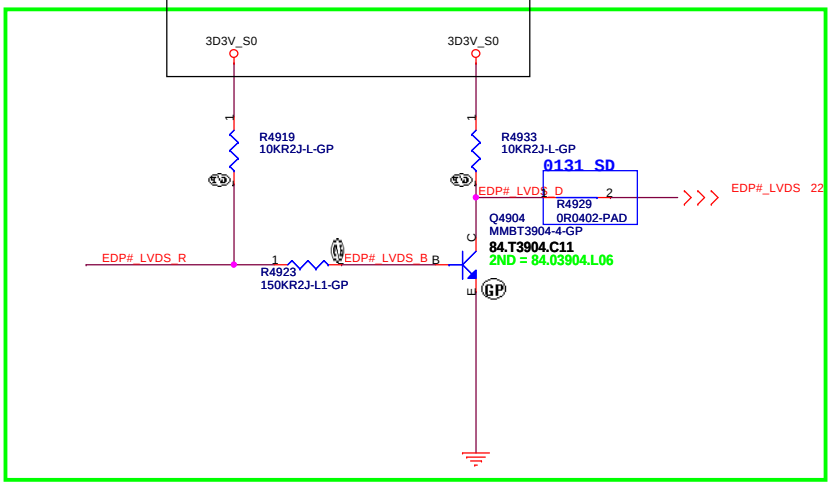


Camera Power



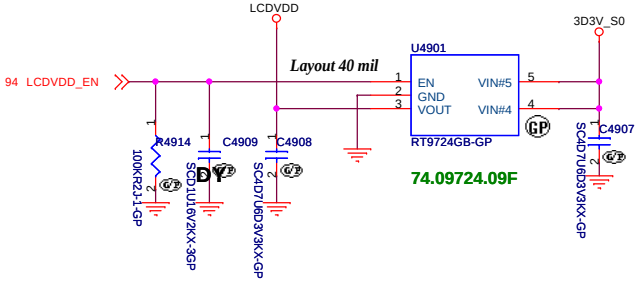
1122 SC del EDP&LVDS colay

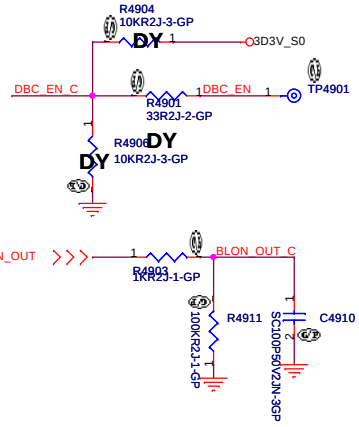
1121 SC



SSID = VIDEO

LCD POWER for ANNIE





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

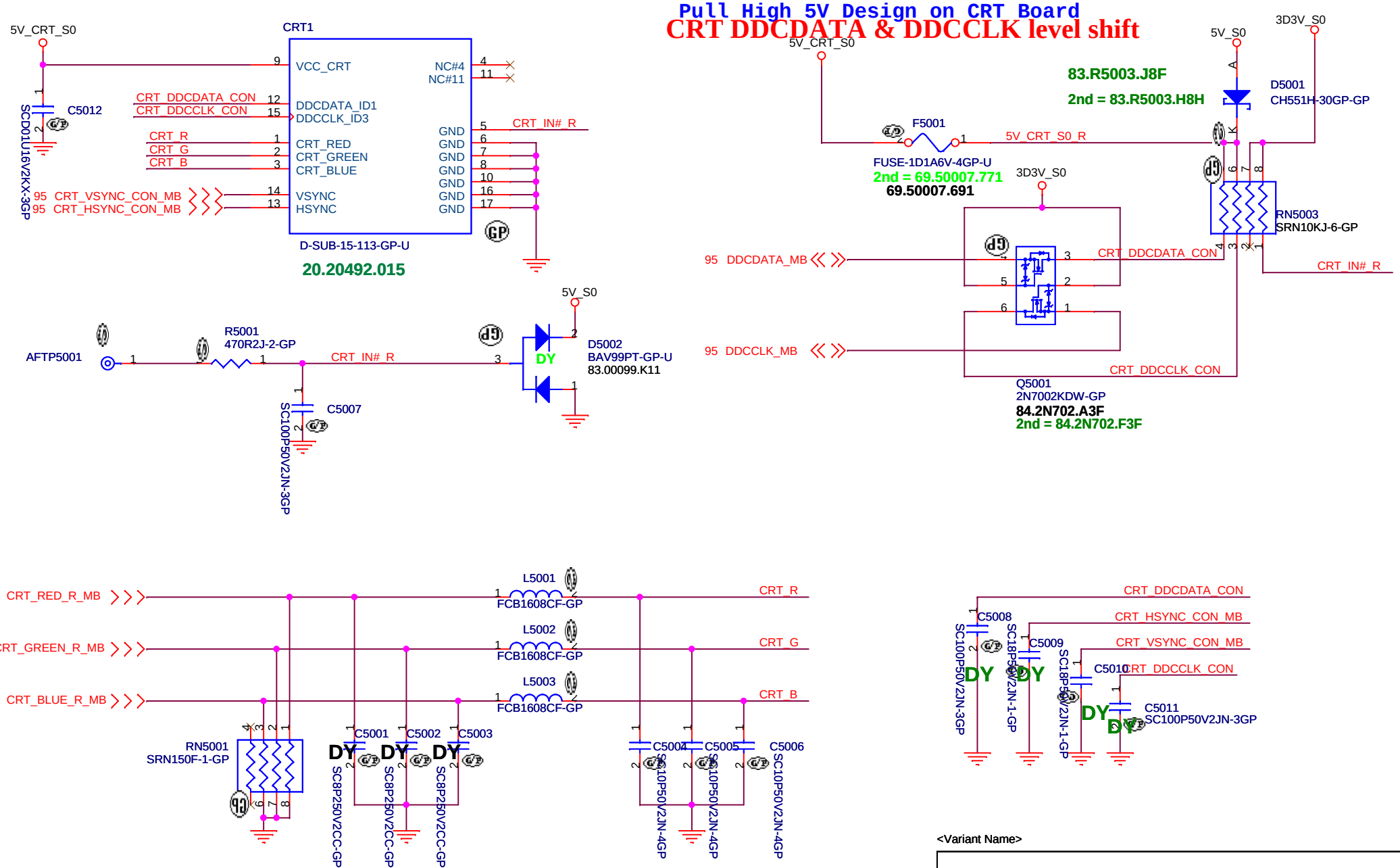
Title: LCD Connector

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 49 of 108

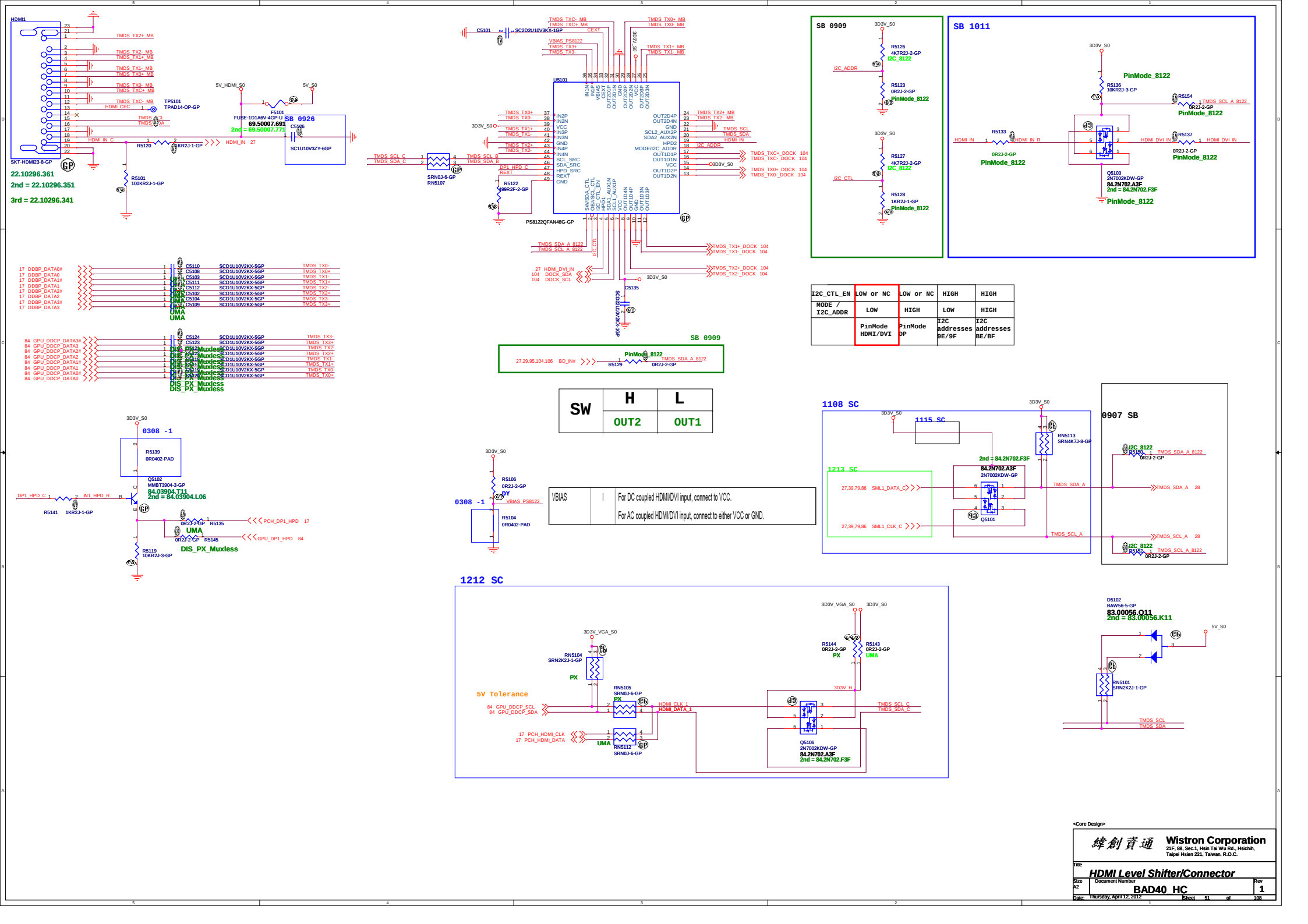
Pull High 5V Design on CRT Board

CRT DDCDATA & DDCCLK level shift



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CRT Connector***
Size: A4	Document Number: **BAD40_HC** Rev: **1**
Date: Thursday, April 12, 2012	Sheet 50 of 108



I2C_CTL_EN	LOW or NC	LOW or NC	HIGH	HIGH
MODE / I2C_ADDR	LOW	HIGH	LOW	HIGH
	PinMode HDMI/DVI	PinMode DP	I2C addresses 9E/9F	I2C addresses BE/BF

SW	H	L
	OUT2	OUT1

VBIAS	I	For DC coupled HDMI/DVI input, connect to VCC. For AC coupled HDMI/DVI input, connect to either VCC or GND.

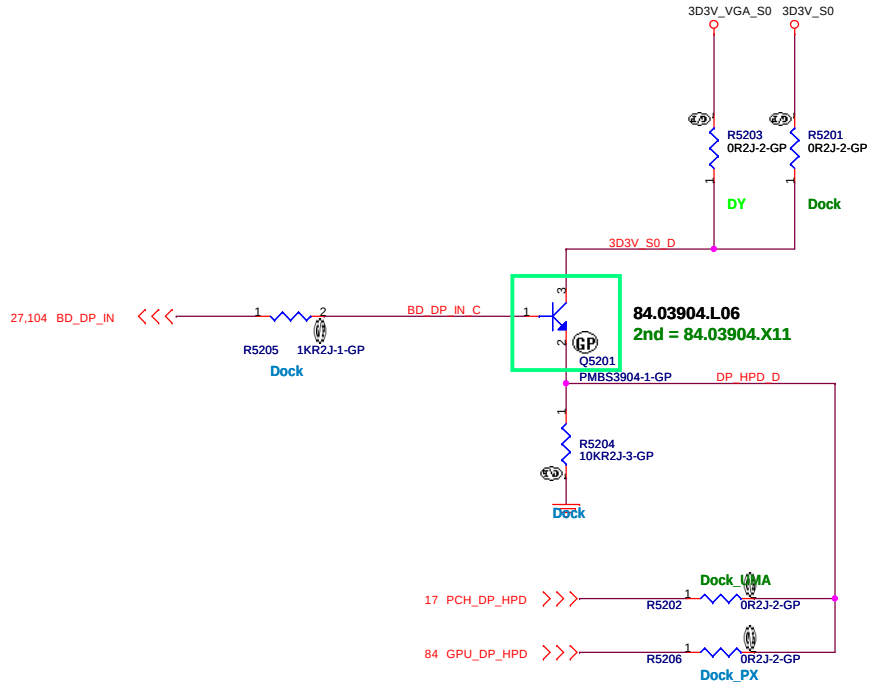
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

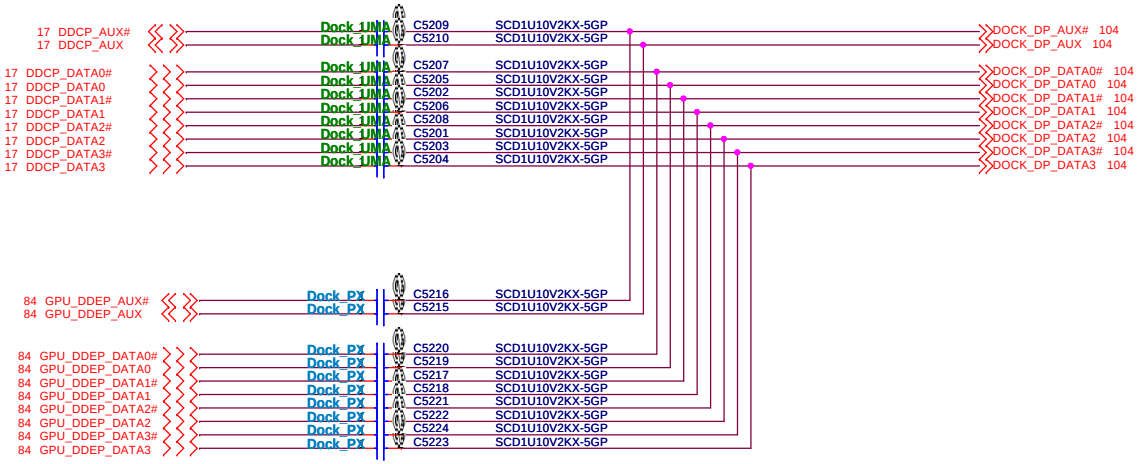
Title: **HDMI Level Shifter/Connector**

Size: A2 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 51 of 108

DP





HR PX

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Display Port***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 52 of 108

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *S-VIDEO*

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 53 of 108

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

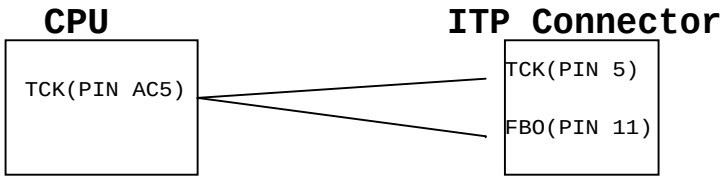
Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 54 of 108

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close ITP connector 500 mil (max), others place near CPU side.



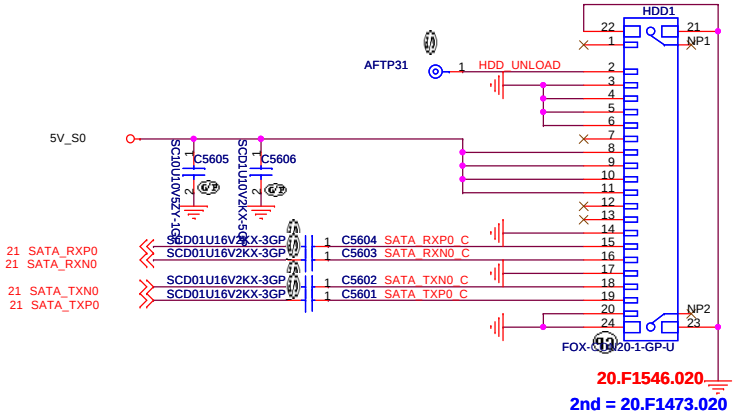
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

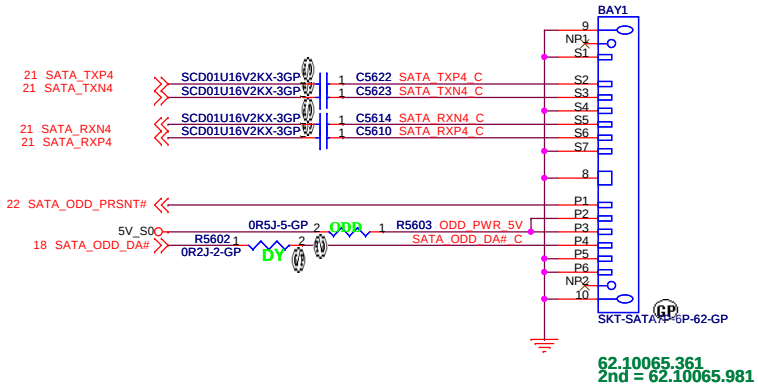
Title: ITP		
Size: A4	Document Number: BAD40_HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 55 of 108	

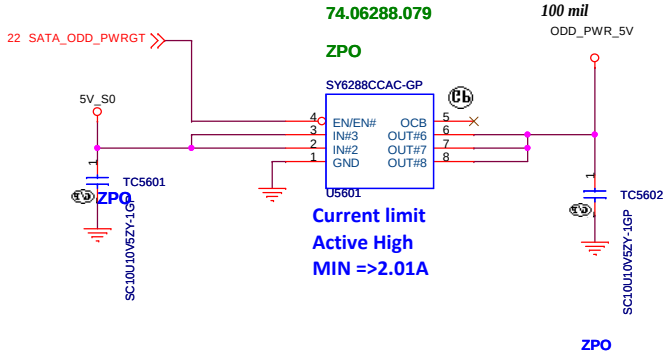
SSID = SATA

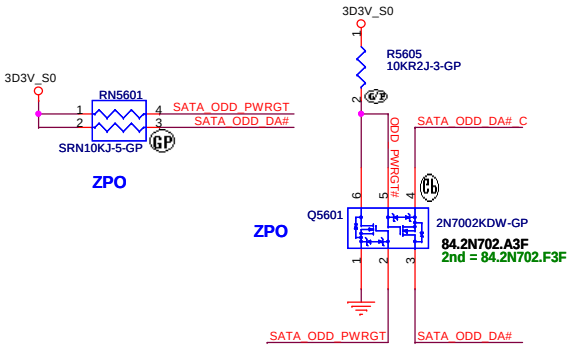
SATA HDD Connector



ODD Connector







<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 56 of 108

reserved

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

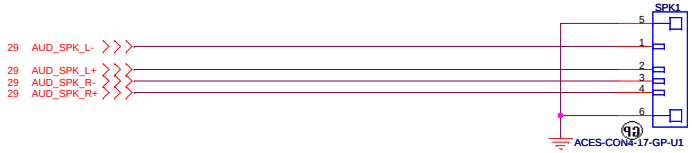
Title: ***E-SATA/USB CHARGER***

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 57 of 108

SSID = AUDIO

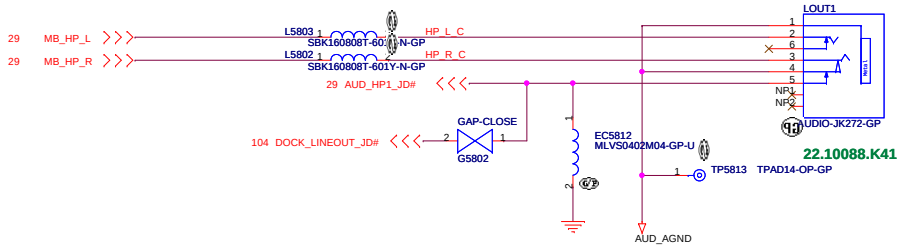
Speaker Connector



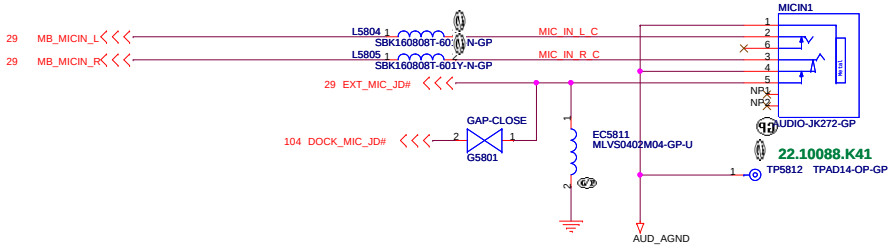
20.F1621.004

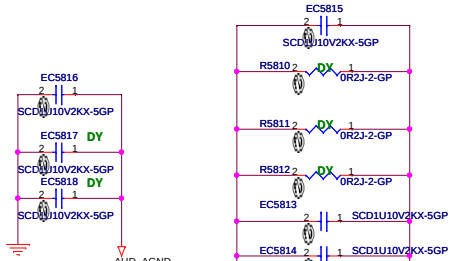
2nd = 20.F1937.004

LINE OUT

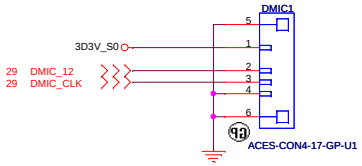


MIC IN





Internal Microphone

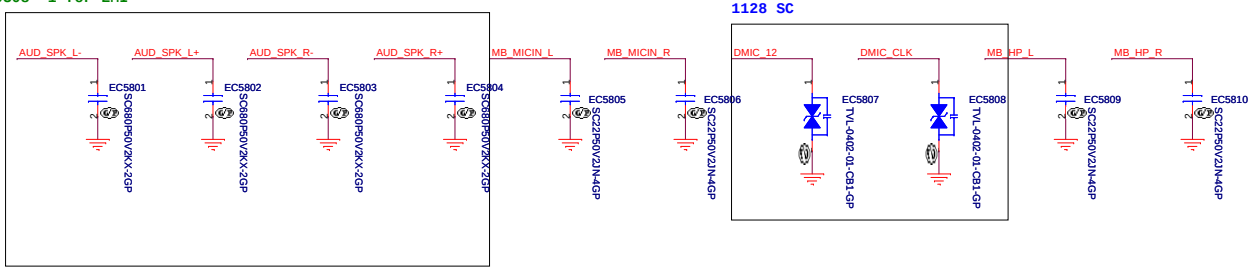


20.F1621.004

2nd = 20.F1937.004

0308 -1 for EMI

1128 SC



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

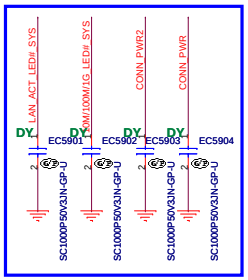
Title: Audio Jack

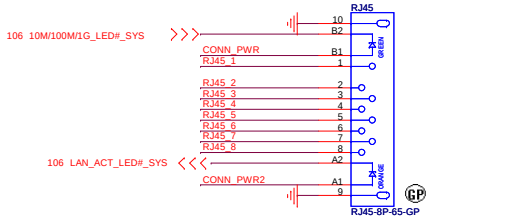
Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 58 of 108

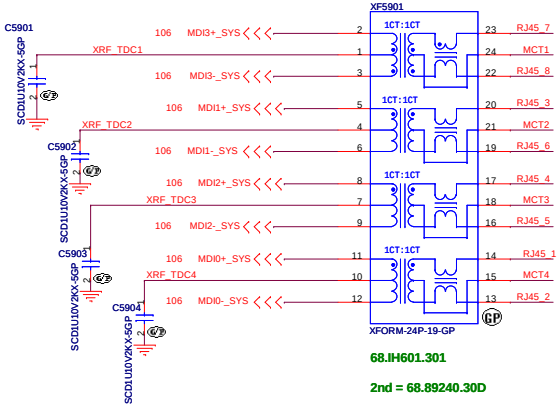
SSID = LOM

SB 0922

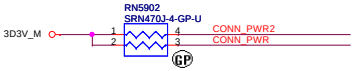


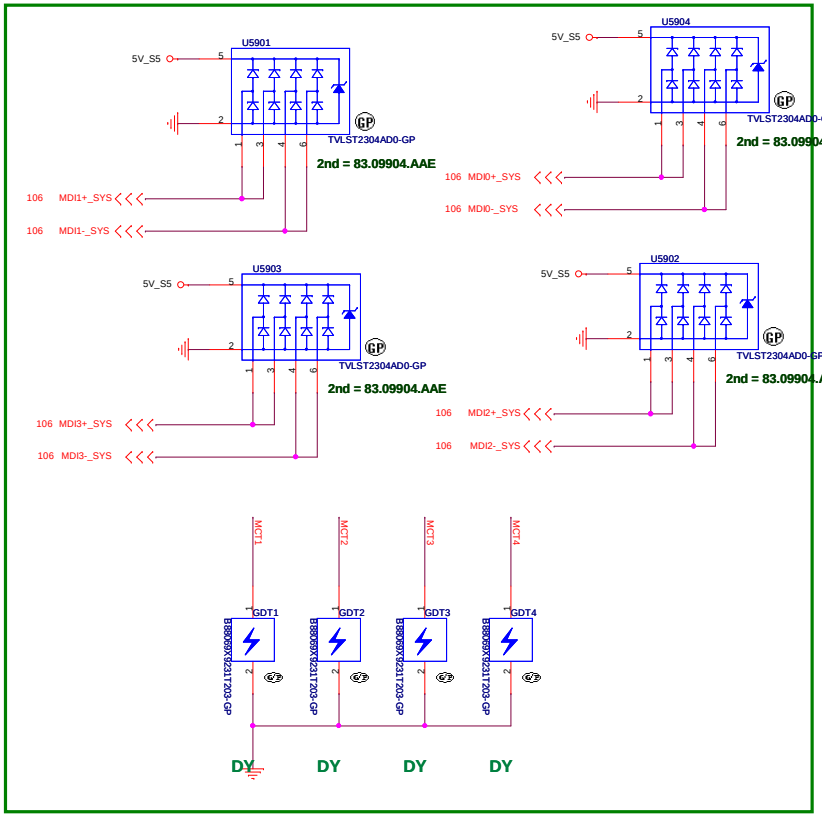


22.10177.J21
2nd = 22.10177.J51

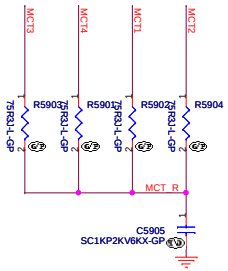


68.IH601.301
2nd = 68.89240.30D





2nd = 83.09904.AAE



<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONNECTOR**

Size	Document Number	Rev
Custom	BAD40_HC	1

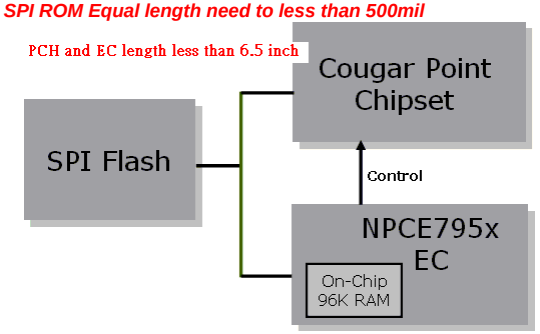
Date: Thursday, April 12, 2012 Sheet 59 of 108

SPI FLASH ROM (8M byte) for PCH

SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch



1212 SC

1216 SC

64MB:72.25640.D01,72.25Q64.B01
32MB:72.25Q32.A01, 72.25320.C01

SYSTEM SPI ROM

3D3V_S5

R6011 4K7R2J-2-GP
R6016 4K7R2J-2-GP
R6017 4K7R2J-2-GP

C6002 SCD1U10V2KX-6GP
C6003 SCD1U10V2KX-6GP

SPI_HOLD_0#

21 SPI_CS0#_R
21 SPI_SO_R

R6001 33R2J-2-GP

SPI_SO_0
SPI_WP#_0

U6001
CE# VDD
SO HOLD#
WP# SCK
VSS SI

SST25VF032B-80-4I-S2AF-GP
72.25032.D01

SPI_CLK_R_0
SPI_SI_R_0

R6012 33R2J-2-GP
R6013 33R2J-2-GP

SPI_CLK_R_21
SPI_SI_R_21

R6008 4K7R2J-2-GP
R6009 4K7R2J-2-GP
R6010 4K7R2J-2-GP

DUAL ROM

21 SPI_CS1#_R
21 SPI_SO_R

R6007 33R2J-2-GP

SPI_SO_1
SPI_WP#_1

U6003
SST25VF032B-80-4I-S2AF-GP
72.25032.D01

SPI_HOLD_1#
SPI_CLK_R_1
SPI_SI_R_1

R6014 33R2J-2-GP
R6015 33R2J-2-GP

SPI_CLK_R_C
SPI_SI_R_C

1230 SC

RN6001 4RN0J-6-GP

SPI_CLK_R_21
SPI_SI_R_21

SSID = RBATT

3D3V_AUX_S5

D6001 BAS16-6-GP

83.00016.K11
2nd = 83.00016.M11

DY

+RTC_PWR_R

R6002 1KR2J-1-GP

20.F1639.002
2nd = 20.F1804.002

RTC_AUX_S5

Q6001 CH715FGP-GP-U

RTC_PWR

R6006 510R2J-1-GP

+RTC_PWR

RTC1

ACES-88242-20-GP

Width=20mils

83.R0304.D81
2nd = 83.R2004.G81

EC BIOS Flash ROM

256KB

3D3V_AUX_S5

for ENE FAE suggest,SPICS# is push-pull pin,
don't need to pull high

R6005 10KR2J-3-GP
R6004 DY 10KR2J-3-GP

SPI_HOLD#

27 SPICS#
27 SPIDI
27 SPI_WP2#

150R2F-1-GP

ER6001

SPI_DI
SPI_WP2#

R6003 10KR2J-3-GP

U6002
CE# VCC
SO HOLD#
WP# SCK
GND SIO

PM25LD020C-SCE-GP
72.25020.E01
2nd = 72.25020.00D

SPI_3D3V_VCC
SPI_HOLD#
SPICLK_1
SPI_DO

150R2F-1-GP

ER6004 0R0603-PAD
C6004 SCD22U16V3KX-2-GP
ER6003
ER6002

SPICLK 27
SPIDO 27

SPICLK_1
SPI_DO
SPIDI

EC6004 SC4D7P50V2CN-1GP DY
EC6005 SC4D7P50V2CN-1GP DY
EC6006 SC4D7P50V2CN-1GP DY

HR PX

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 60 of 108

SSID = USB

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 61 of 108

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
USB 3.0 Port

Size	Document Number	Rev
A3	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 62 of 108

SSID = User.Interface

Bluetooth Module conn.

reserved 1216

<Variant Name>

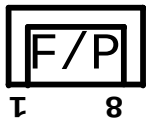
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Bluetooth*

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 63 of 108

Finger printer



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

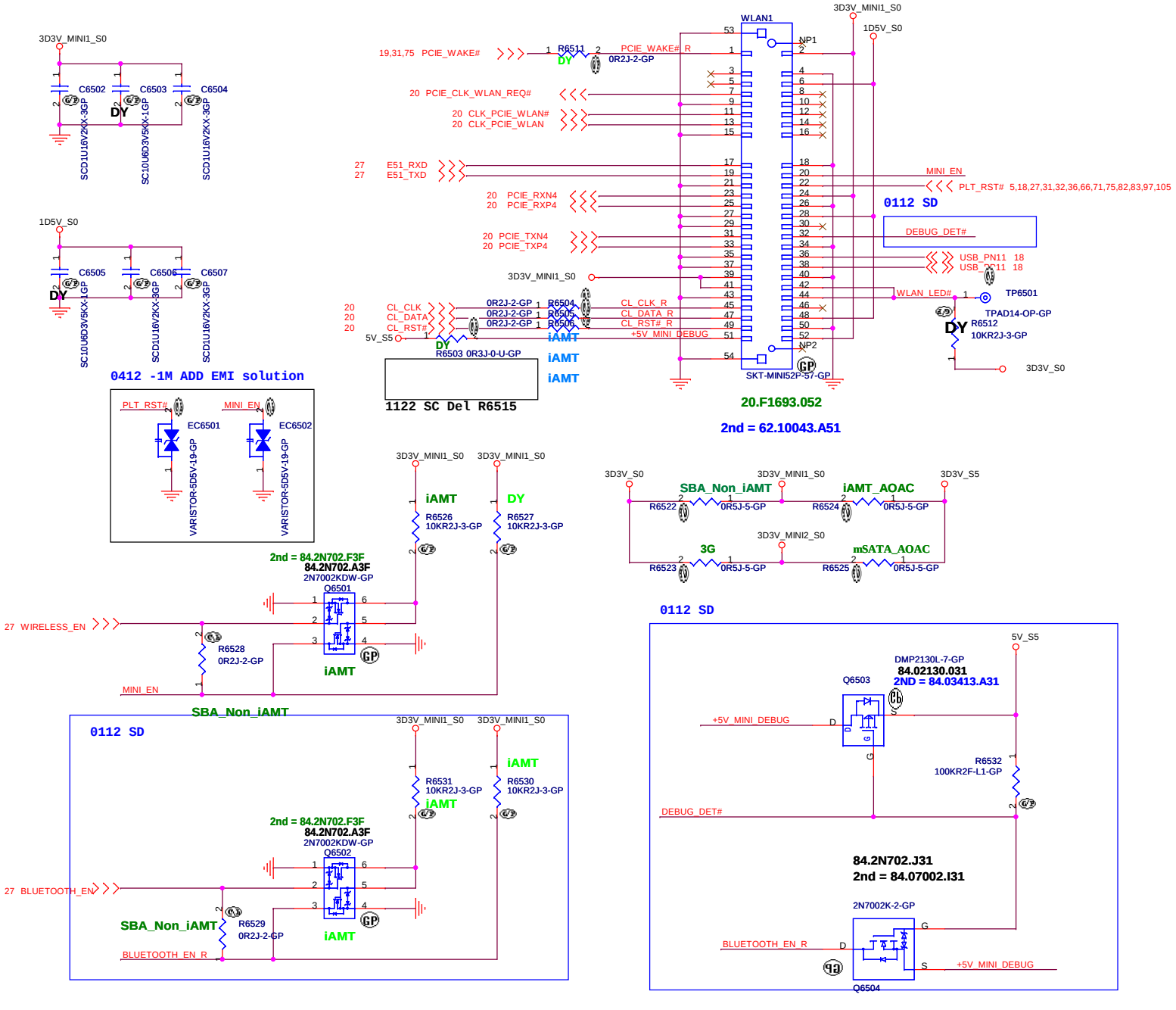
Title
RESERVED

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 64 of 108

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



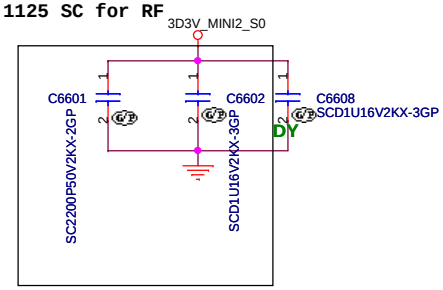
<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINICARD(WLAN)/ITP CONN		
Size: A3	Document Number: BAD40_HC	Rev: 1
Date: Thursday, April 12, 2012	Sheet 65 of 108	

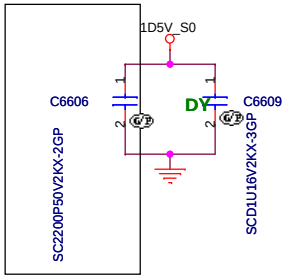
SSID = Wireless

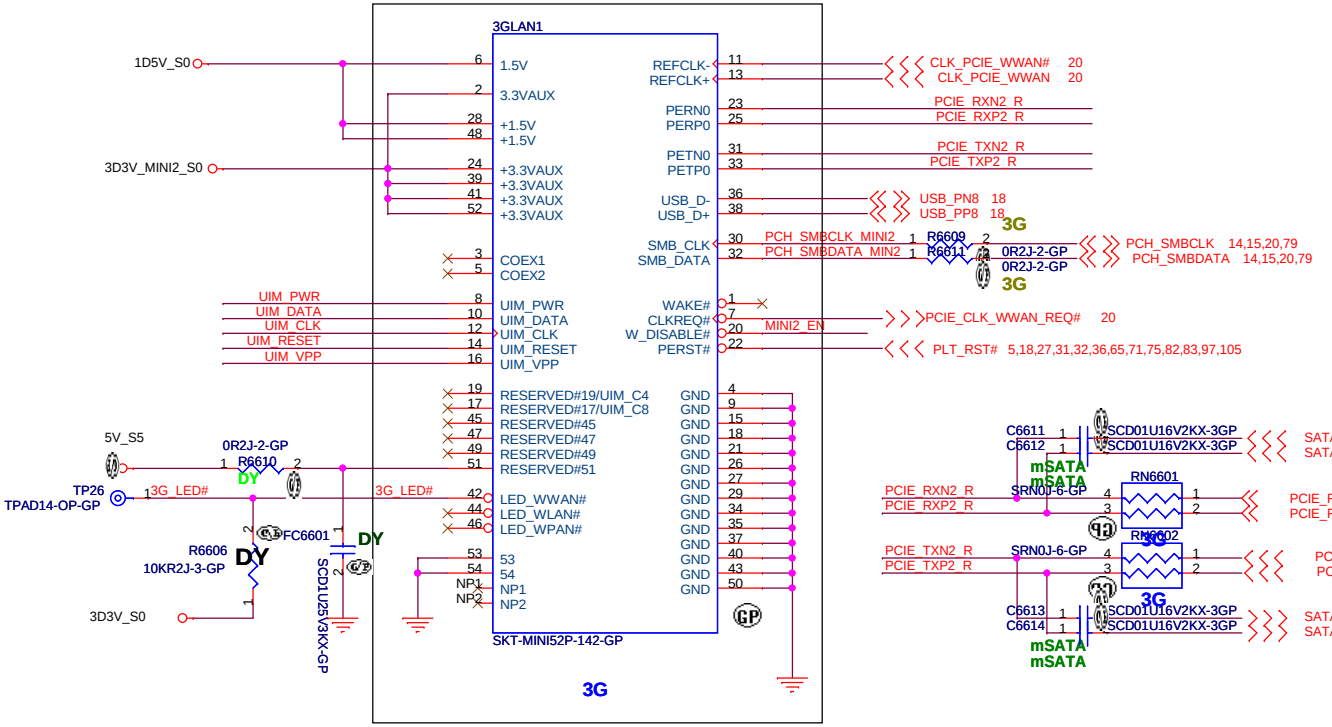
Mini Card Connector(3GLAN)

1125 SC for RF

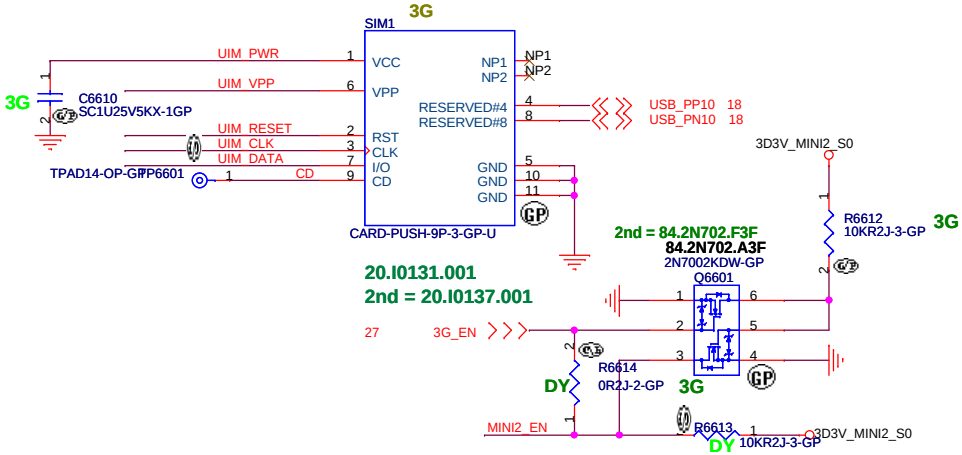


1125 SC for RF





0103 SC change to 62.10043.H61



<Variant Name>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	3G
Size: Custom	Document Number: BAD40_HC
Rev	1
Date: Thursday, April 12, 2012	Sheet 66 of 108

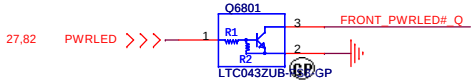
reserved

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***mSATA***		
Size: A4	Document Number: **BAD40_HC**	Rev: **1**
Date: Thursday, April 12, 2012	Sheet 67 of 108	

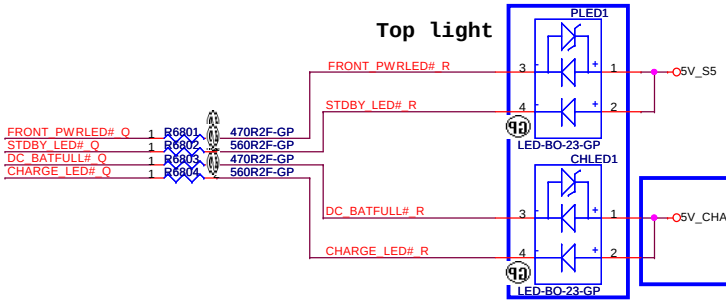
Power button LED



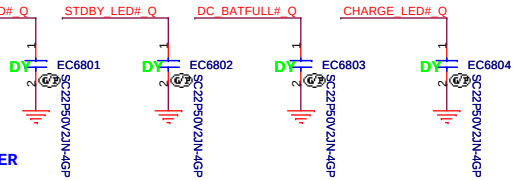
84.00043.011
2nd = 84.05143.011

0130 SD change PN

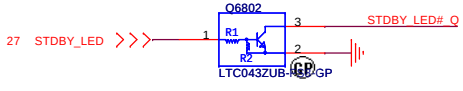
Top light



0130 SD change to 5V_CHARGER

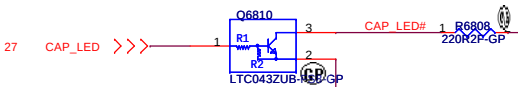


Power STDBY_LED



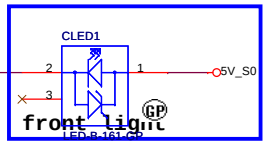
84.00043.011
2nd = 84.05143.011

Caps Lock LED

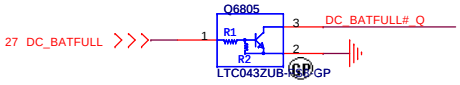


84.00043.011
2nd = 84.05143.011

0202 SD

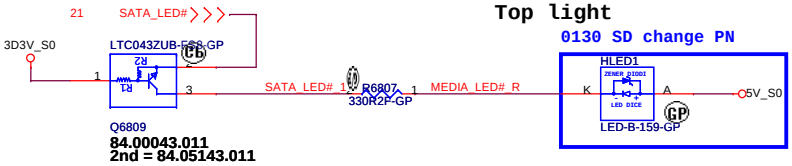


Battery LED2(DC_BATFULL)



84.00043.011
2nd = 84.05143.011

SATA HDD LED

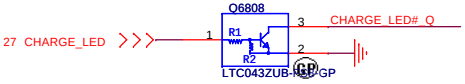


84.00043.011
2nd = 84.05143.011

Top light

0130 SD change PN

Battery LED1(CHARGE)



84.00043.011
2nd = 84.05143.011

0302 -1 Del PWR BTN

1107 SC Del BXD PWR LED

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

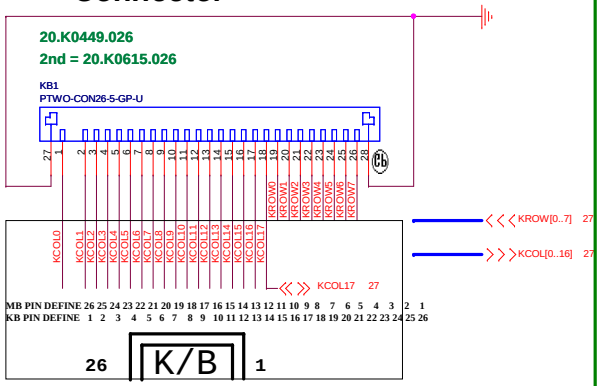
Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 68 of 108

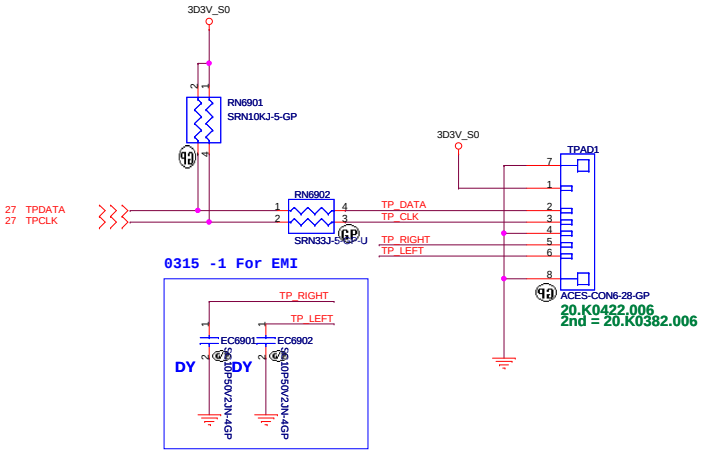
SSID = KBC

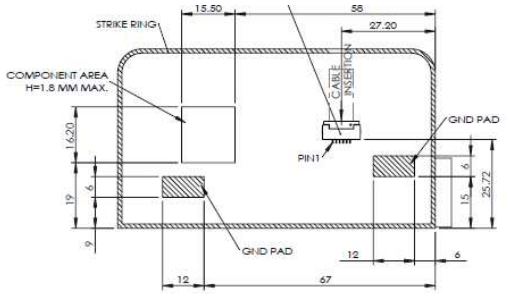
SB 0919 change PN for Layout

Internal KeyBoard Connector



TOUCH PAD 1.0 pitch



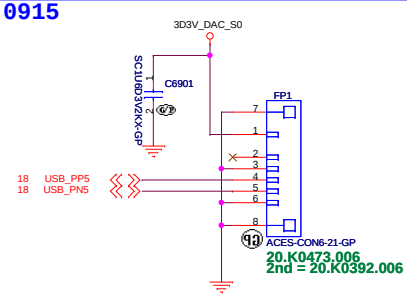


COMPONENT - BOTTOM VIEW

J1 PIN ASSIGNMENT:
PIN1 : TP_L
PIN2 : TP_R
PIN3 : GND
PIN4 : PS2_CLK
PIN5 : PS2_DAT
PIN6 : VDD

Finger Printer 0.5 pitch

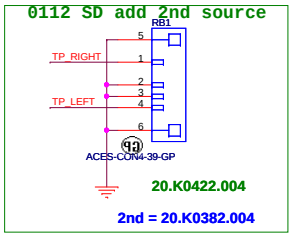
SB 0915



Pin No.	Define
1	ESD ground
2	USB D- Signal
3	USB D+ Signal
4	GND
5	NC
6	3.3V Power pin

Rubber Dome 1.0 pitch

0909 SB
0112 SD add 2nd source



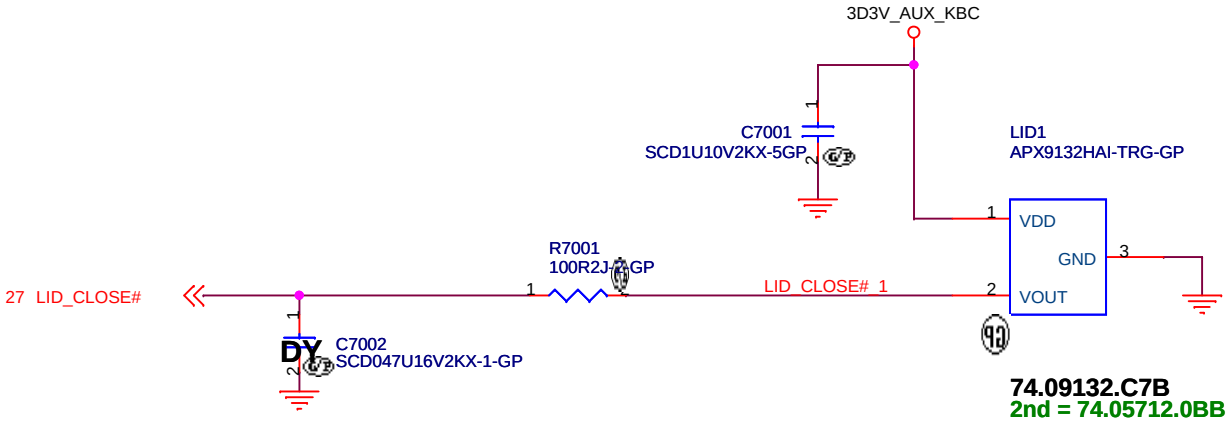
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size: Custom | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 69 of 108



<Variant Name>

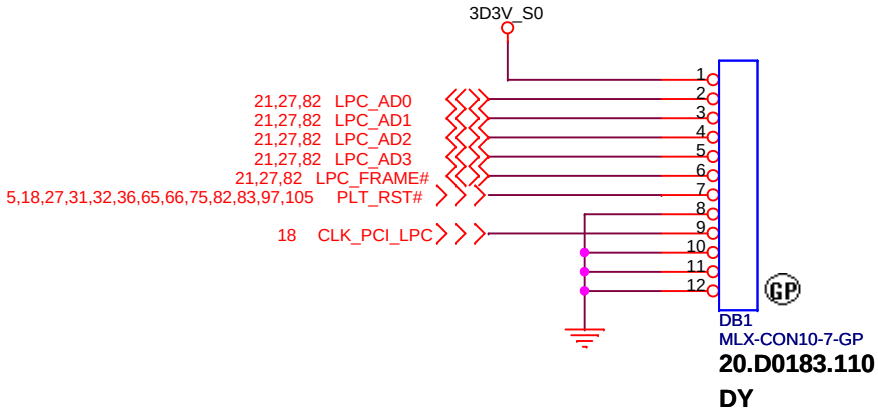
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 70 of 108

SB modify to test pad



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 71 of 108

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	BAD40_HC	1

(Blanking)

<Variant Name>

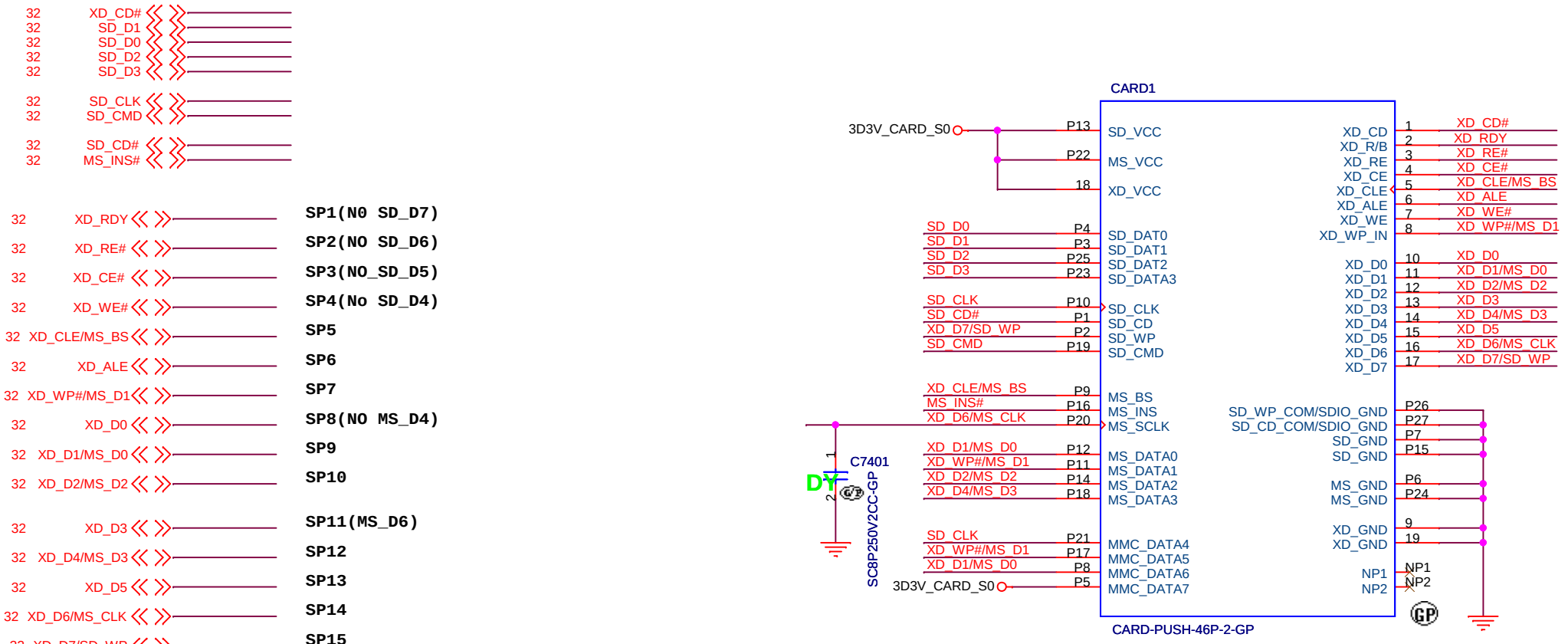
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	BAD40_HC	1

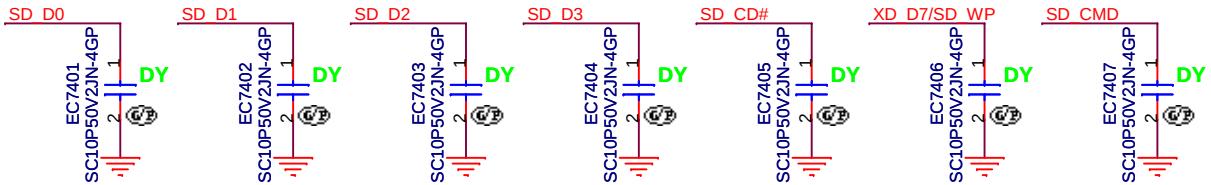
SD/XD/MS Card Reader

SSID = SDIO



20.I0135.001

2nd = 20.I0129.001



<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	BAD40_HC	1

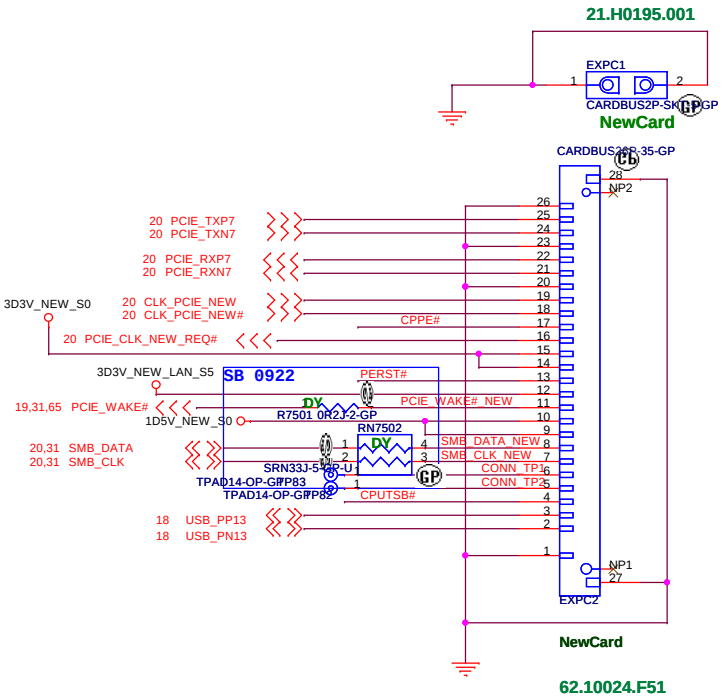
Date: Thursday, April 12, 2012 Sheet 74 of 108

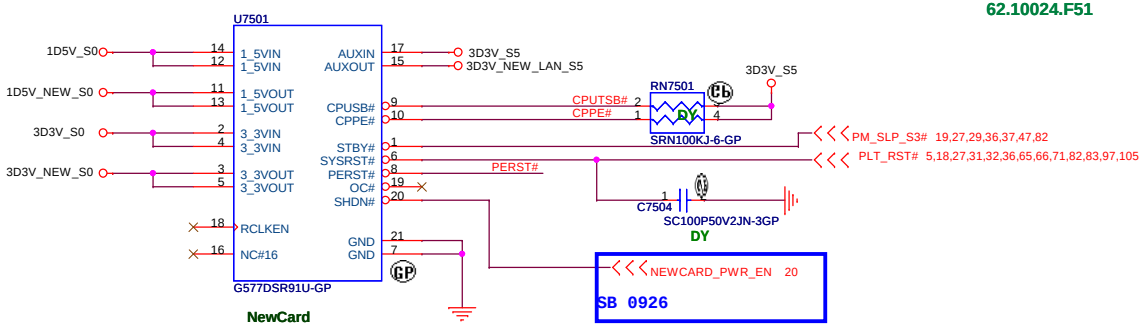
SSID = ExpressCard

DIP階 For Expresscard socket

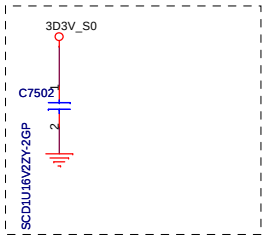
21.H0195.001

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

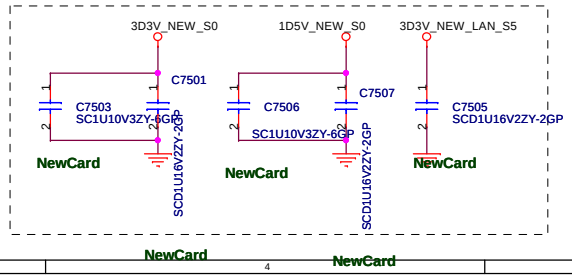




Place them Near to Chip



Place them Near to Connector



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***New Card***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 75 of 108

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 76 of 108

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 77 of 108

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

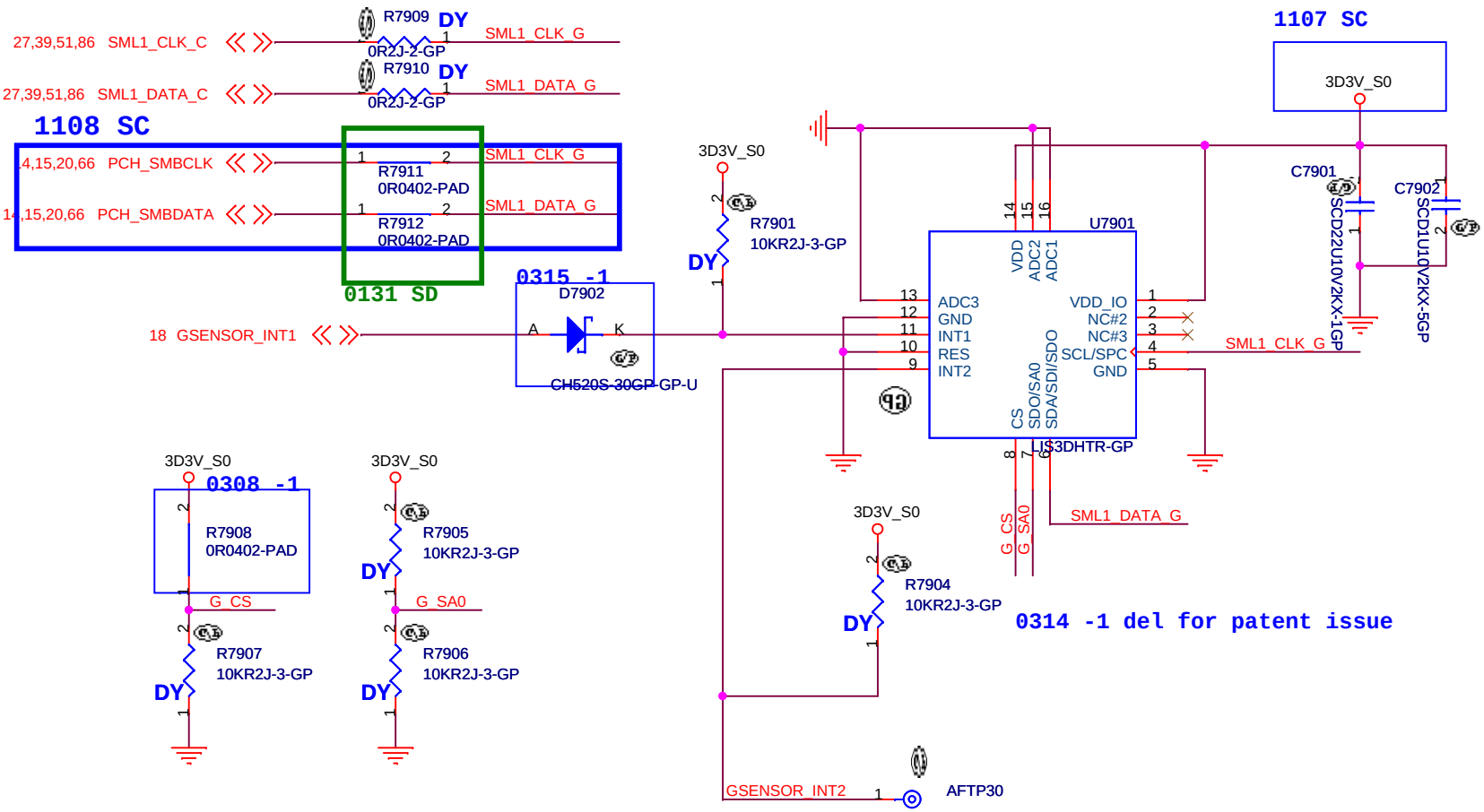
Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 78 of 108

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 79 of 108

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 80 of 108

<Variant Name>

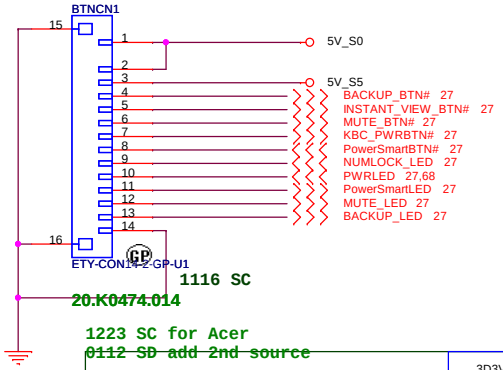
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	**BAD40_HC**	1

Date: Thursday, April 12, 2012 Sheet 81 of 108

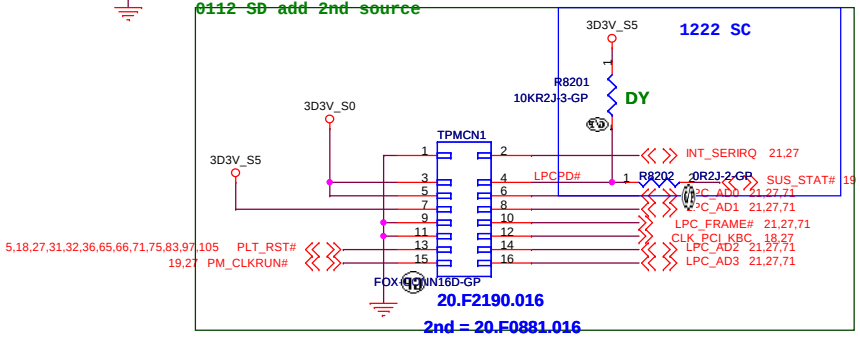


1116 SC

20.K0474.014

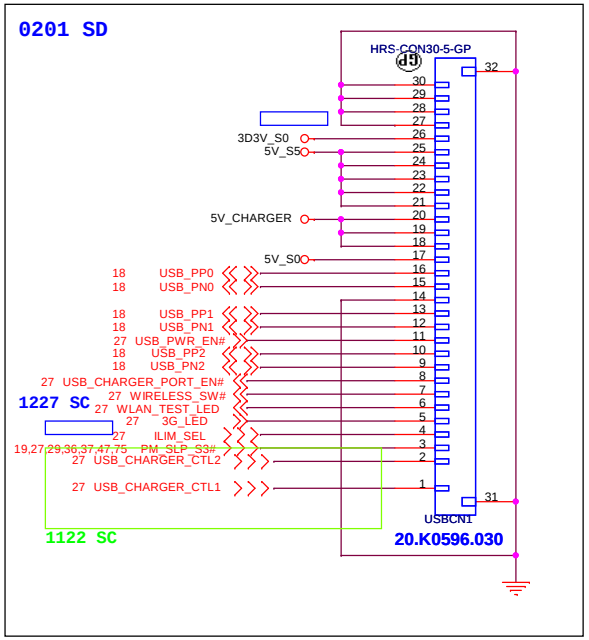
1223 SC for Acer

0112 SD add 2nd source

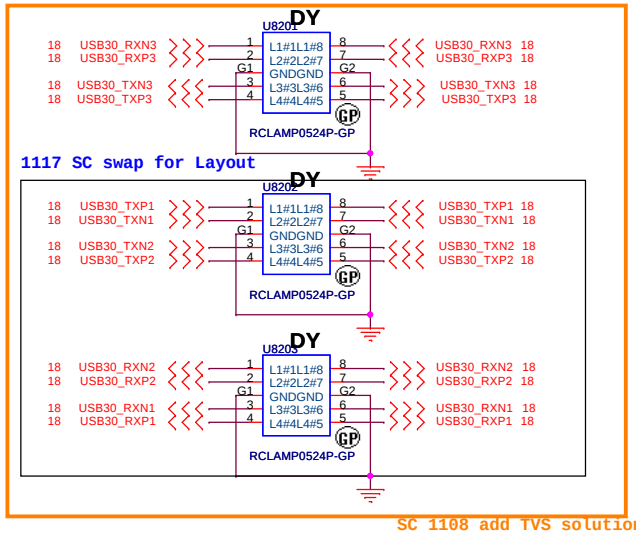


20.F2190.016

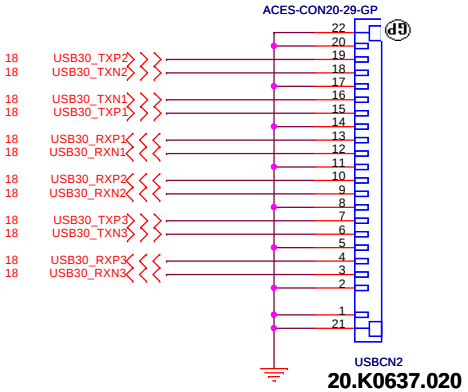
2nd = 20.F0881.016



20.K0596.030



SC 1108 add TVS solution



20.K0637.020

<Variant Name>

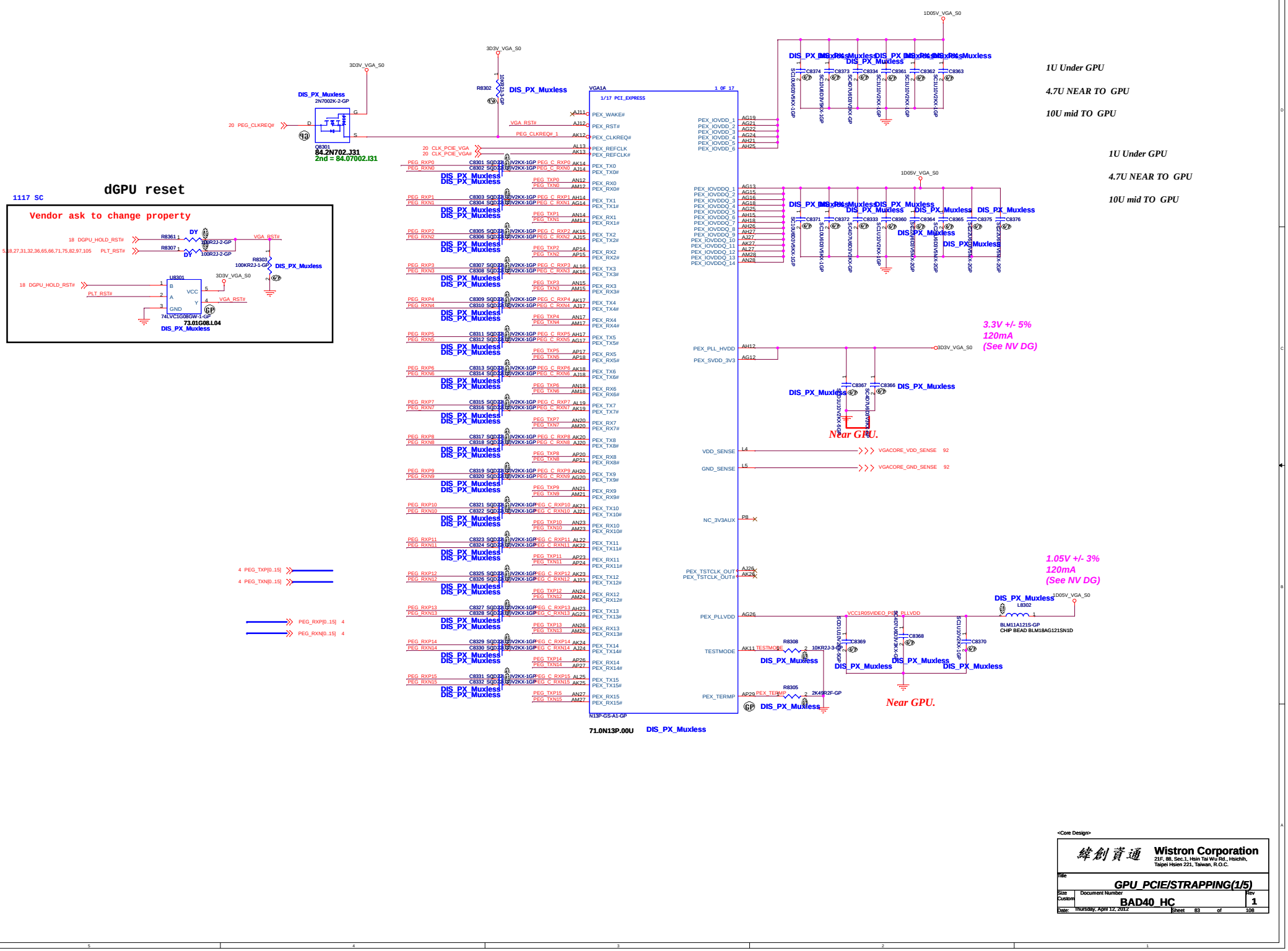
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 82 of 108


dGPU reset
1117 SC
Vendor ask to change property
DGPU_HOLD_RST#
PLT_RST#
VGA_RST#
DY
R8361
R8307
R8303
100R2J-2-GP
100KR2J-1-GP
DIS_PX_Muxless
U8301
74LVC1G08GW-1-GP
73.01G08.L04
3D3V_VGA_S0
PEG_CLKREQ#
2N7002K-2-GP
Q8301
84.2N702.J31
2nd = 84.07002.I31
R8302
10KR2J-3-GP
VGA_RST#
PEG_CLKREQ# 1
CLK_PCIE_VGA
CLK_PCIE_VGA#
VGA1A
1/17 PCI_EXPRESS
1 OF 17
PEX_WAKE#
PEX_RST#
PEX_CLKREQ#
PEX_REFCLK
PEX_REFCLK#
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
PEX_RX4#
PEX_TX5
PEX_TX5#
PEX_RX5
PEX_RX5#
PEX_TX6
PEX_TX6#
PEX_RX6
PEX_RX6#
PEX_TX7
PEX_TX7#
PEX_RX7
PEX_RX7#
PEX_TX8
PEX_TX8#
PEX_RX8
PEX_RX8#
PEX_TX9
PEX_TX9#
PEX_RX9
PEX_RX9#
PEX_TX10
PEX_TX10#
PEX_RX10
PEX_RX10#
PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
PEX_RX12#
PEX_TX13
PEX_TX13#
PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#
N13P-GS-A1-GP
71.0N13P.00U
PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5
PEX_IOVDD_6
PEX_IOVDDQ_1
PEX_IOVDDQ_2
PEX_IOVDDQ_3
PEX_IOVDDQ_4
PEX_IOVDDQ_5
PEX_IOVDDQ_6
PEX_IOVDDQ_7
PEX_IOVDDQ_8
PEX_IOVDDQ_9
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
PEX_PLL_HVDD
PEX_SVDD_3V3
VDD_SENSE
GND_SENSE
NC_3V3AUX
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PEX_PLLVDD
TESTMODE
PEX_TERMP
VGACORE_VDD_SENSE 92
VGACORE_GND_SENSE 92
1D05V_VGA_S0
3D3V_VGA_S0
4 PEG_TXP[0..15]
4 PEG_TXN[0..15]
PEG_RXP[0..15] 4
PEG_RXN[0..15] 4
1U Under GPU
4.7U NEAR TO GPU
10U mid TO GPU
3.3V +/- 5%
120mA
(See NV DG)
Near GPU.
1.05V +/- 3%
120mA
(See NV DG)
L8302
BLM11A121S-GP
CHIP BEAD BLM18AG121SN1D
R8308
10KR2J-3-GP
R8305
2K49R2F-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU_PCIE/STRAPPING(1/5)
Size
Custom
Document Number
BAD40_HC
Rev
1
Date: Thursday, April 12, 2012
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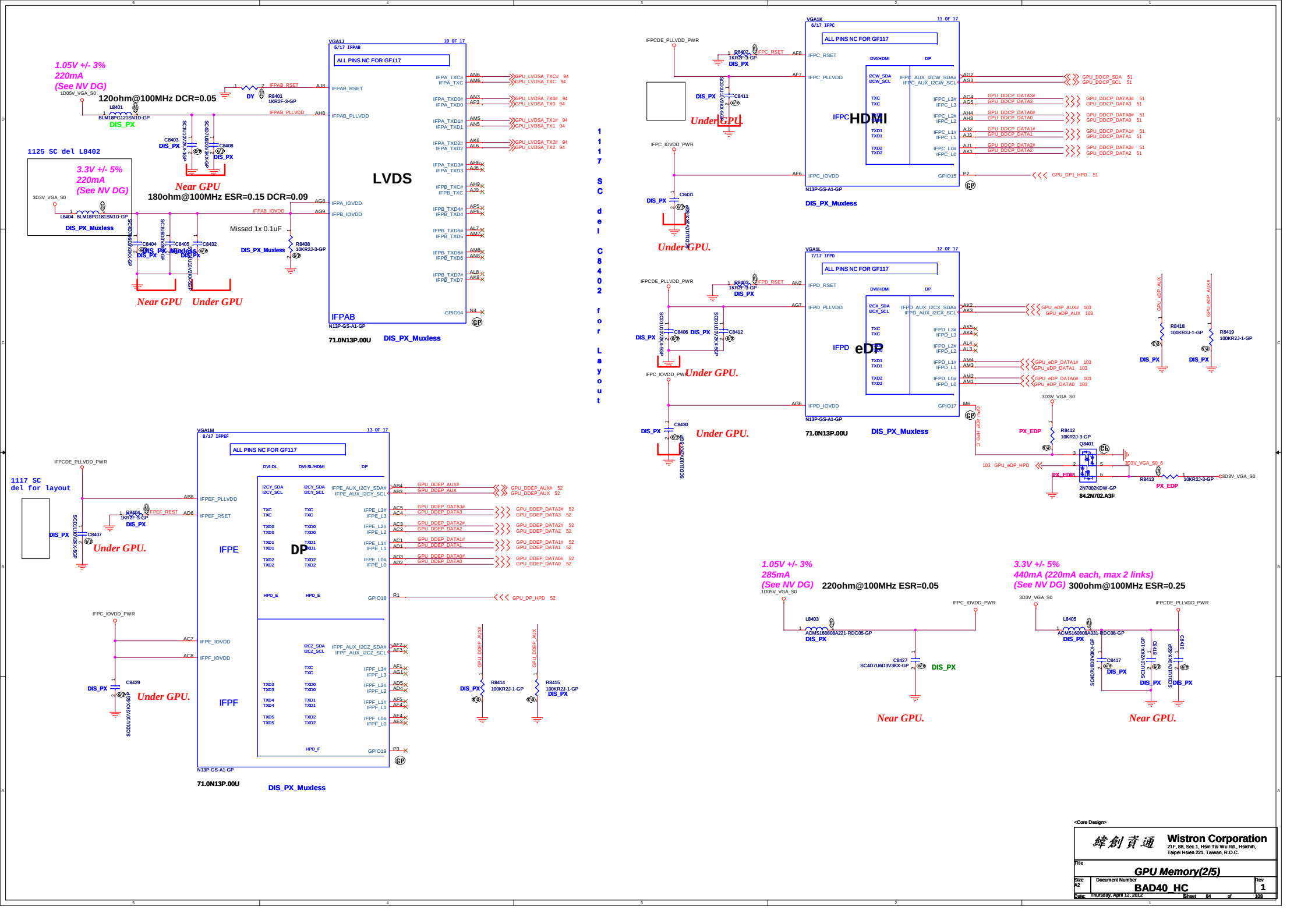


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size: A2 | Document Number: BAD40_HC | Rev: 1

Date: Thursday, April 12, 2012 | Sheet 84 of 108

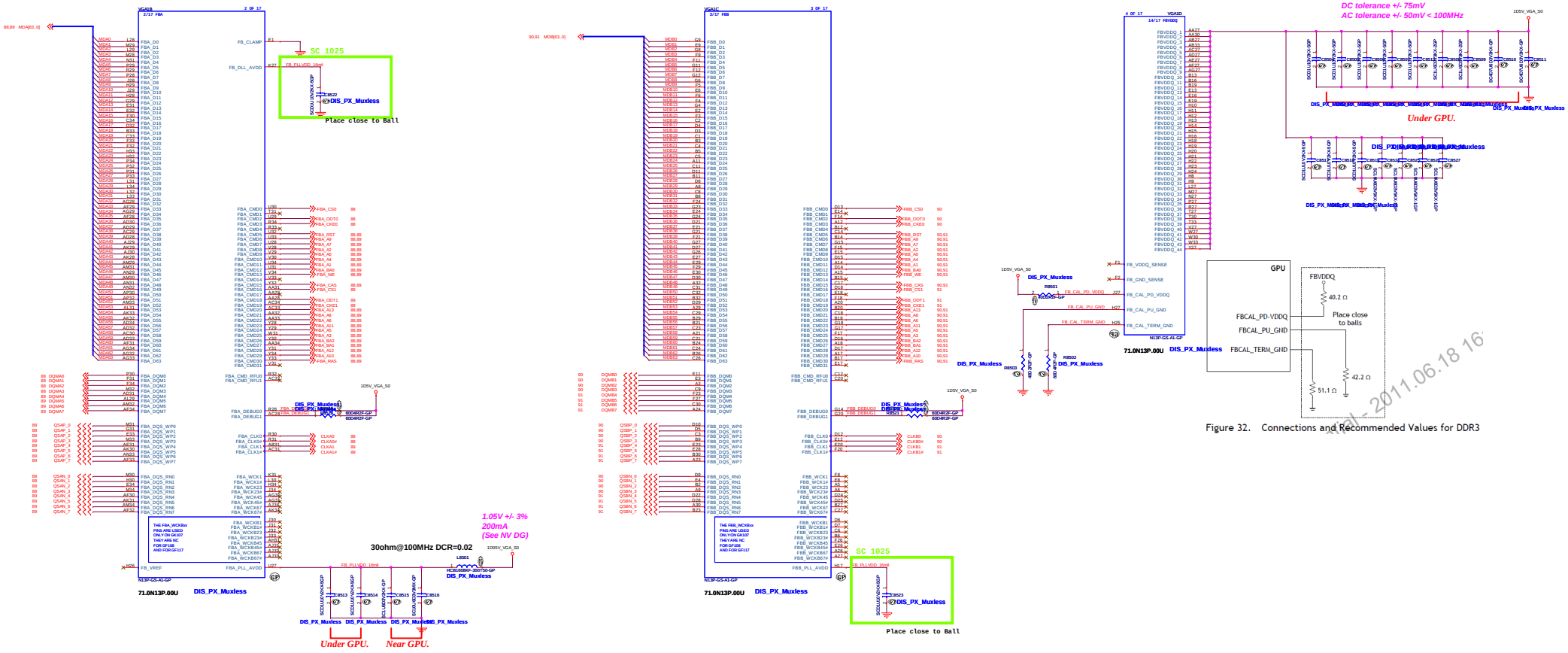
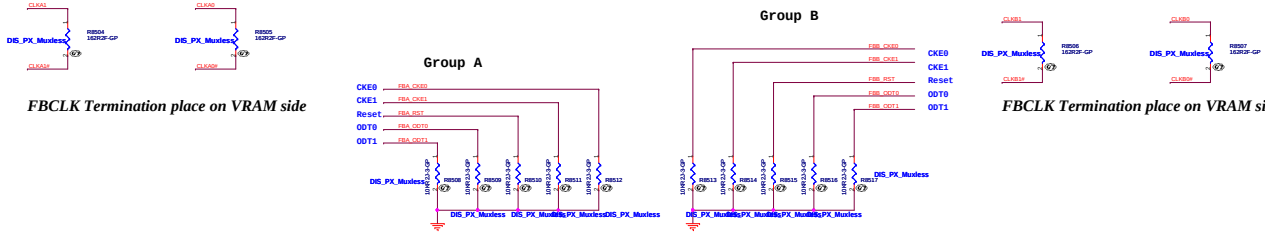


Figure 32. Connections and Recommended Values for DDR3



FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: GPU_DP/LVDS/CRT/GPIO(3/5)	
Size: Custom	Document Number: BAD40_HC
Rev: 1	
Date: Thursday, April 14, 2011	Sheet 85 of 108

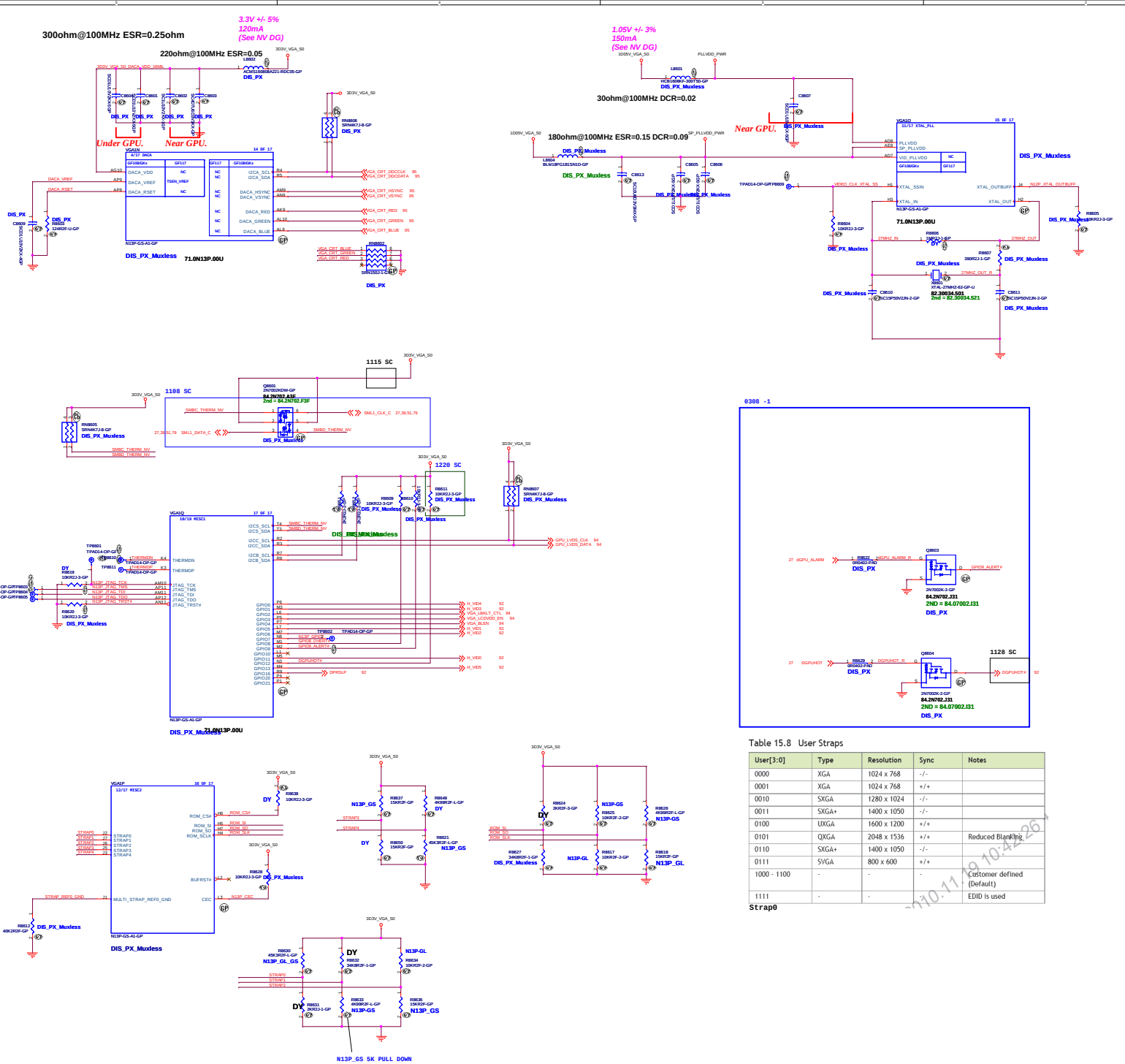


Table 15.8 User Straps

User[3:0]	Type	Resolution	Sync	Notes
0000	XGA	1024 x 768	-/-	
0001	XGA	1024 x 768	+/+	
0010	SXGA	1280 x 1024	-/-	
0011	SXGA+	1400 x 1050	-/-	
0100	UXGA	1600 x 1200	+/+	
0101	QXGA	2048 x 1536	+/+	Reduced Blanking
0110	SXGA+	1400 x 1050	-/-	
0111	SVGA	800 x 600	+/+	
1000 - 1100	-	-	-	Customer defined (Default)
1111	-	-	-	EDID is used

Strap0

Table 15.3 Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD	Pull-down to GND
5k	1000	0000
10k	1001	0001
15k	1010	0010
20k	1011	0011
25k	1100	0100
30k	1101	0101
35k	1110	0110
45k	1111	0111

25Kohm	5Kohm	10Kohm	30Kohm
64.24925.6DL	64.49915.6DL	64.10025.6DL	64.30025.6DL

NVIDIA TABLE

	Hynix 2G 0110 128M*16*8 900MHZ	Hynix 1G 0010 64M*16*8 900MHZ	Samsung 1G 0011 64M*16*8 900MHZ	Samsung 2G 0111 128M*16*8 900MHZ
ROM_SI	34.8Kohm 64.34825.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

Table 111. Display Link to SORx_EXPOSED Bit Mapping

Displays		DVI/HDMI/DP	LVDS	eDP	Not in Use
Dual Link Mode	IFPA/B		SOR0_EXPOSED = 0		SOR0_EXPOSED = 0
	IFPC	SOR1_EXPOSED = 1			SOR1_EXPOSED = 0
	IFPD	SOR2_EXPOSED = 1		SOR2_EXPOSED = 0	SOR2_EXPOSED = 0
	IFPE/F	SOR3_EXPOSED = 1			SOR3_EXPOSED = 0
Split Mode	IFPA/B				
	IFPC	SOR1_EXPOSED = 1			SOR1_EXPOSED = 0
	IFPD	SOR2_EXPOSED = 1		SOR2_EXPOSED = 0	SOR2_EXPOSED = 0
	IFPE	SOR3_EXPOSED = 1			SOR3_EXPOSED = 0
	IFPF	SOR0_EXPOSED = 1			SOR0_EXPOSED = 0

Strap3

	DEVID	ROM-SCLK		strap2	
N13P-GL-A1	0x0DE9	0010	PD 15K	1001	PU 10K
N13P-GS-ES-A1	0x0FD8	1000	PU 4.99K	1011	PU 20K
N13P-GS-A1	0x0FD2	1000	PU 4.99K	0010	PD 15K

For N13P-GS-A1 0x0FD2

Strap Pin Nmae	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0	
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TER_ST	
	1	0	0	0	5K ohm pull-up
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]	
Hynix 2G	0	1	1	0	35K ohm pull-down
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	
	1	0	0	1	10K ohm pull-up
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	
	1	1	1	1	45K ohm pull-up
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	
	0	0	0	0	5K ohm pull-down
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	
	0	0	1	0	15K ohm pull-down
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	
	1	0	1	0	15K ohm pull-up
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	
	0	1	1	1	45K ohm pull-down

<Core Design>

Wistron Corporation
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Title: GPU_POWER(4/5)

Size: A3 | Document Number: BAD40_HC | Rev: 1

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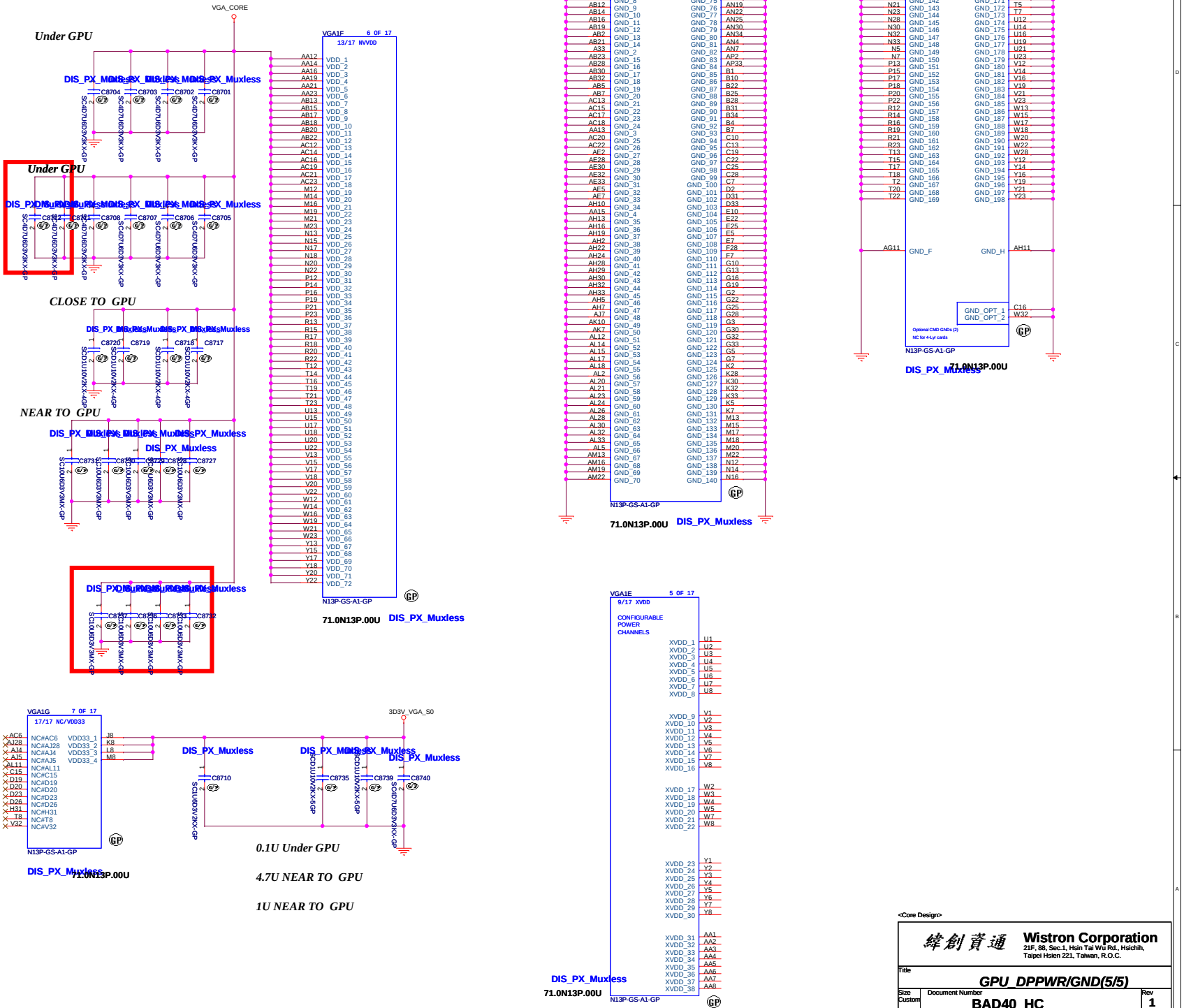
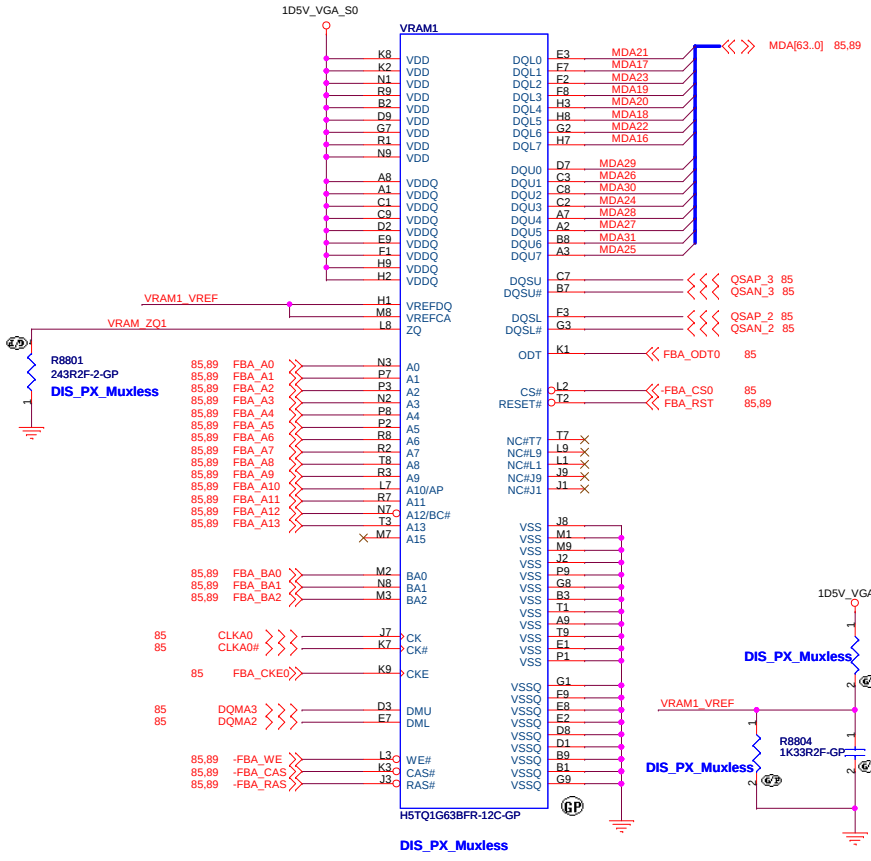
EDP 50A
(TDP 37W)

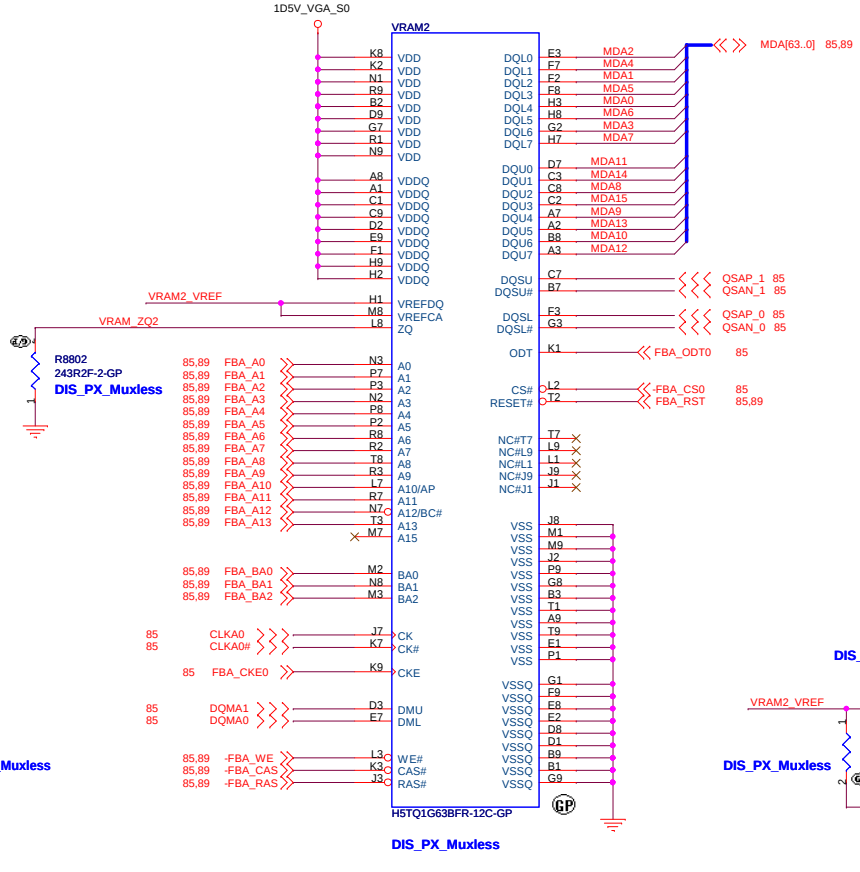


Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
Custom	BAD40_HC	1

Date: Thursday, April 12, 2012 Sheet 87 of 108





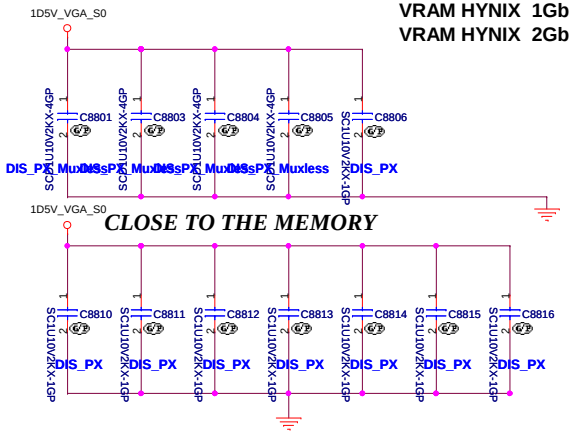
Hy2GX8_VR.2GB0G.001,Sam1GX8_VR.1GB0B.006,,Hy1GX8_72.51G63.C0U,Sam512X4_VR.1GB0B.006,Sam2GX8

VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

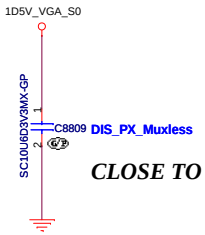
FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



CLOSE TO THE MEMORY



CLOSE TO THE MEMORY

<Core Design>

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Title: ***GPU-VRAM1,2 (1/4)***

Size	Document Number	Rev
Custom	BAD40_HC	1

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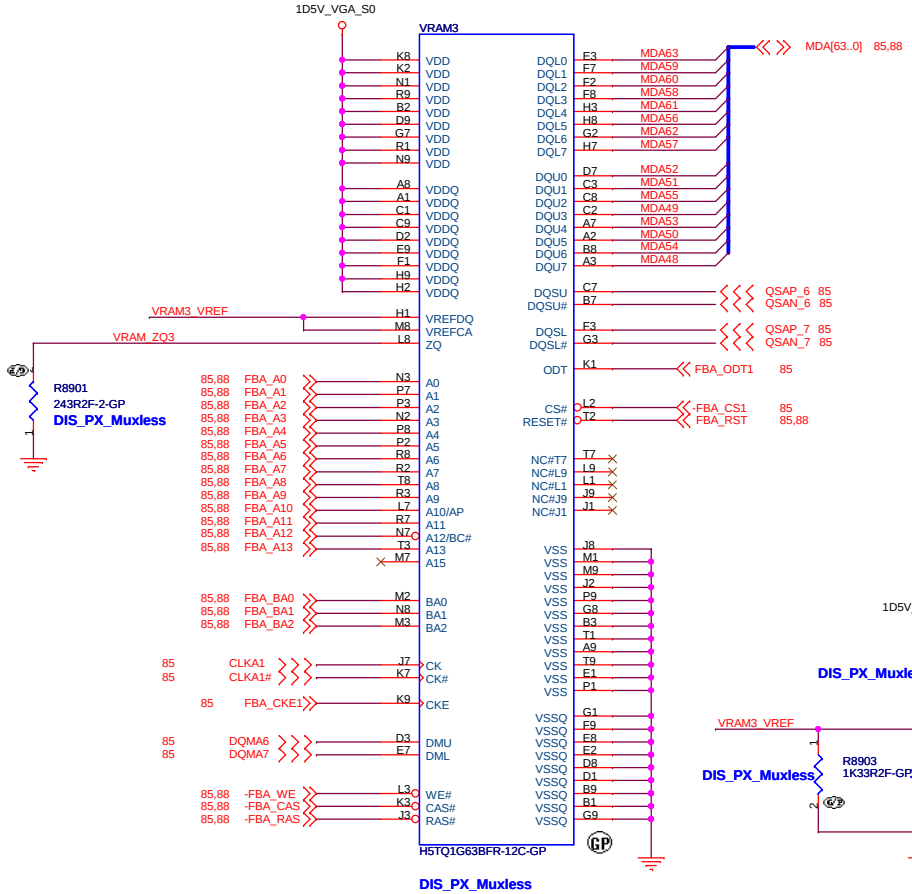
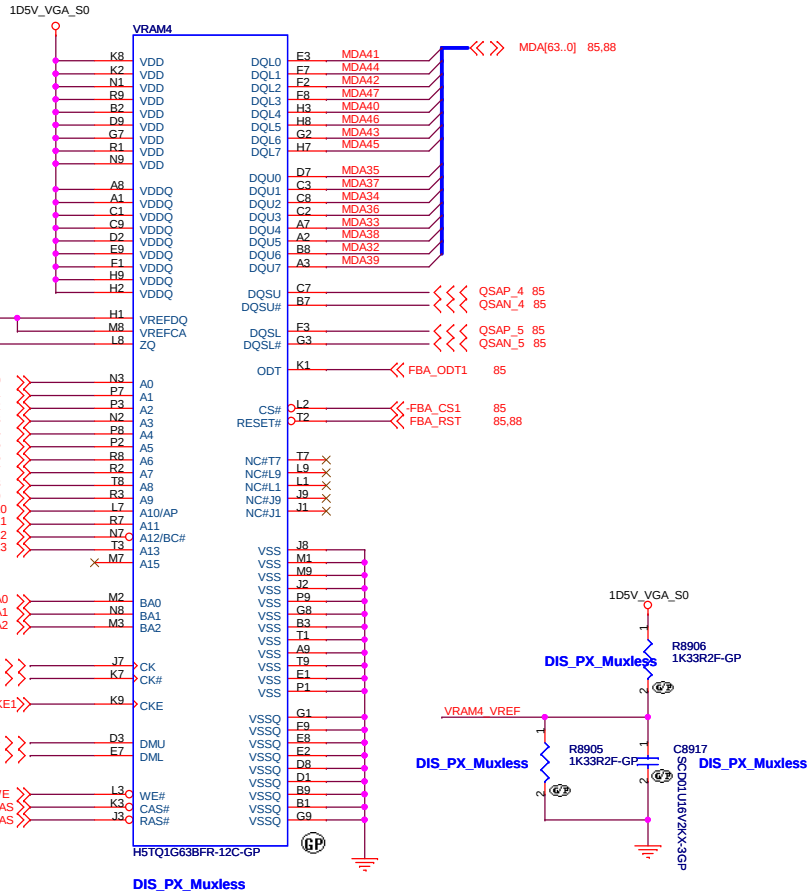


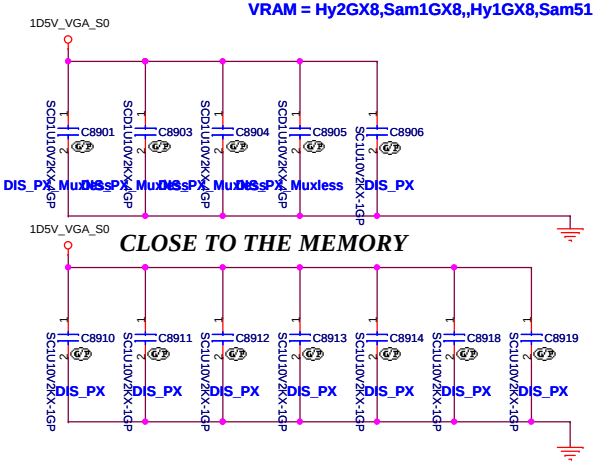
VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8



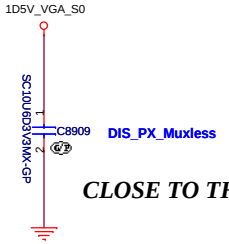
VRAM = Hy2GX8,Sam1GX8,,Hy1GX8,Sam512X4,Sam2Gx8

FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



CLOSE TO THE MEMORY



CLOSE TO THE MEMORY

<core_design>
<Core Design>

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Title: ***GPU-VRAM3,4 (2/4)***

Size: Custom | Document Number: **BAD40_HC** | Rev: **1**

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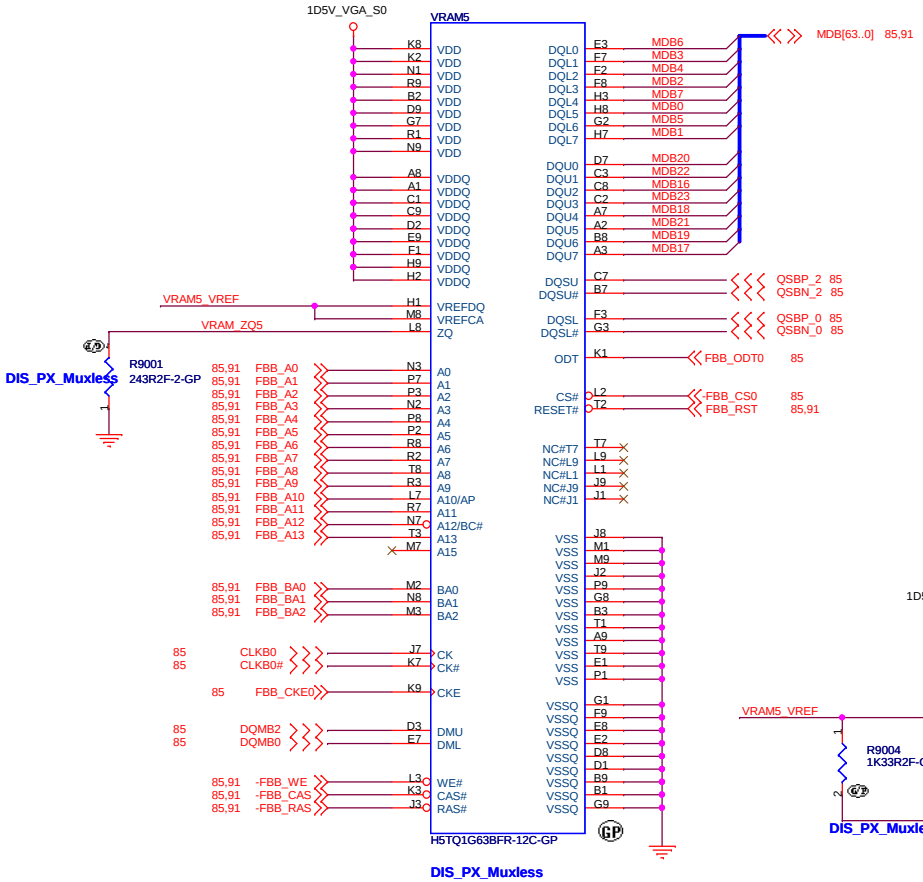
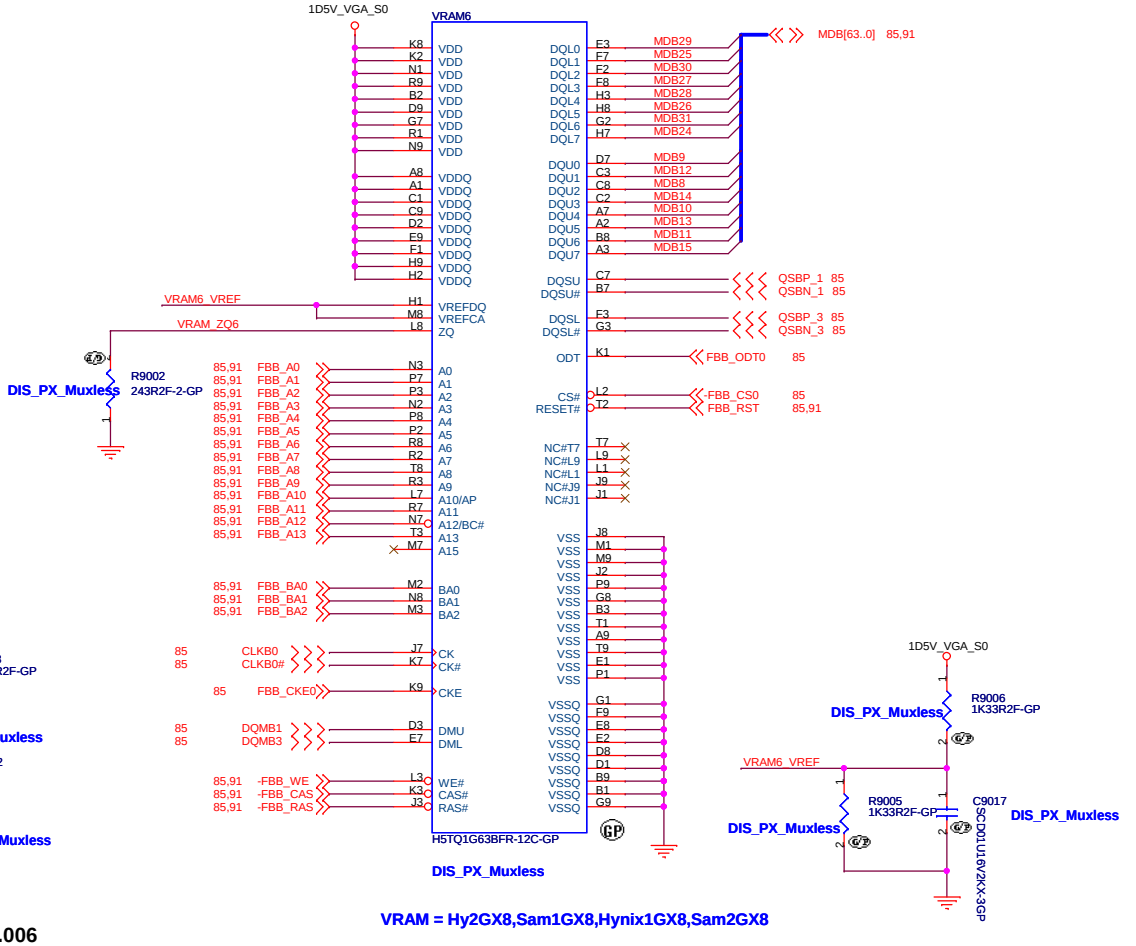
</core_design>



DIS_PX_Muxless

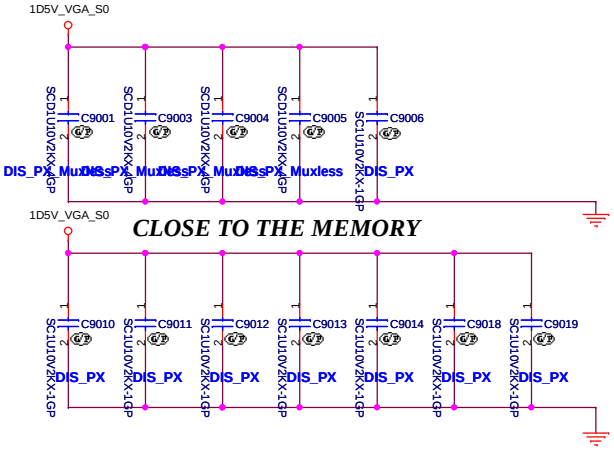
VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8



DIS_PX_Muxless

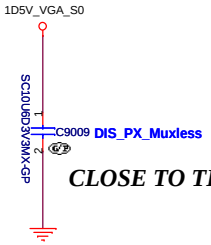
VRAM = Hy2GX8,Sam1GX8,Hynix1GX8,Sam2GX8

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



CLOSE TO THE MEMORY

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



CLOSE TO THE MEMORY

<Variant Name>

緯創資通 **Wistron Corporation**
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Title: **GPU-VRAM5,6 (3/4)**

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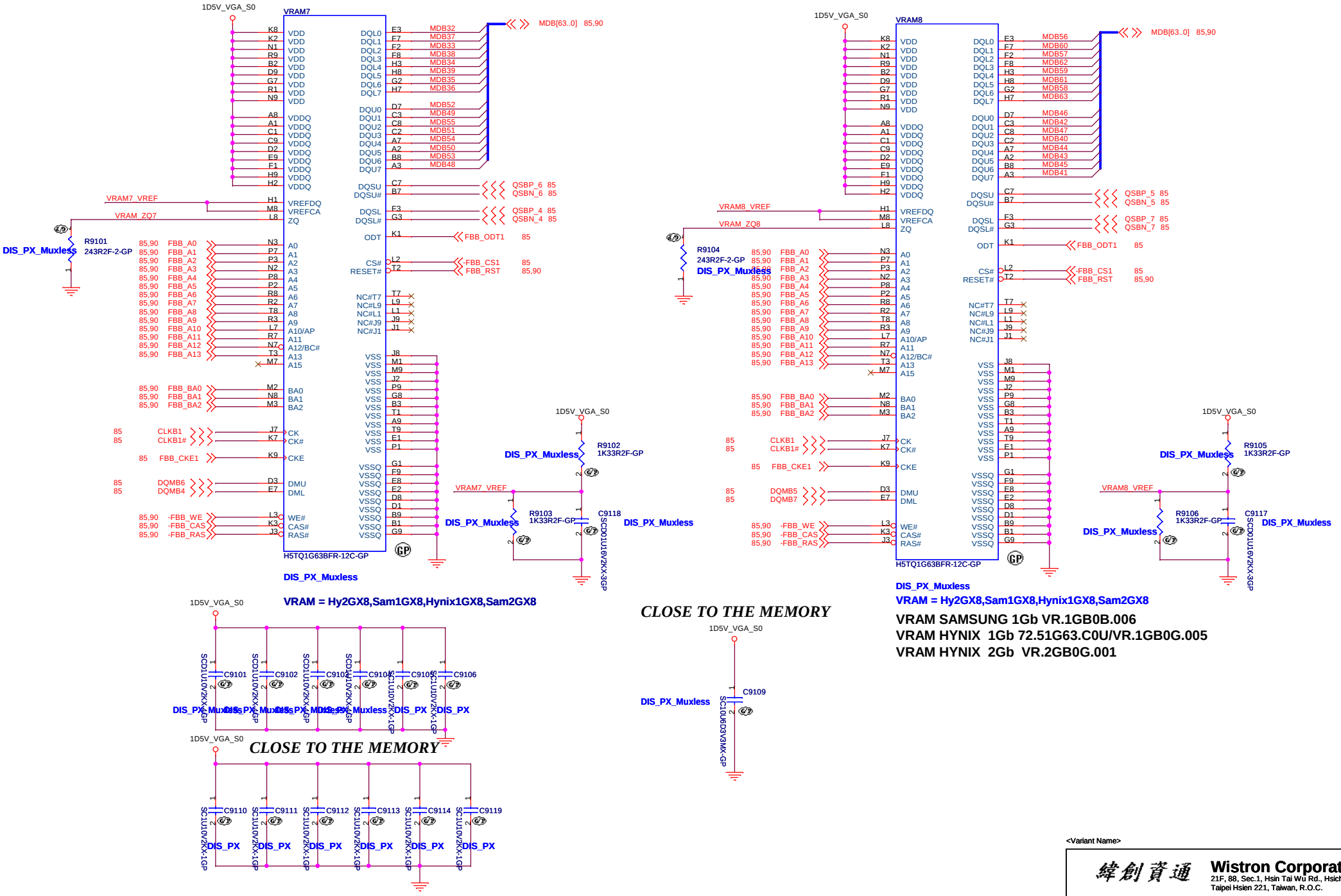

<Variant Name>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GPU-VRAM7,8 (4/4)
Size: Custom	Document Number: BAD40_HC
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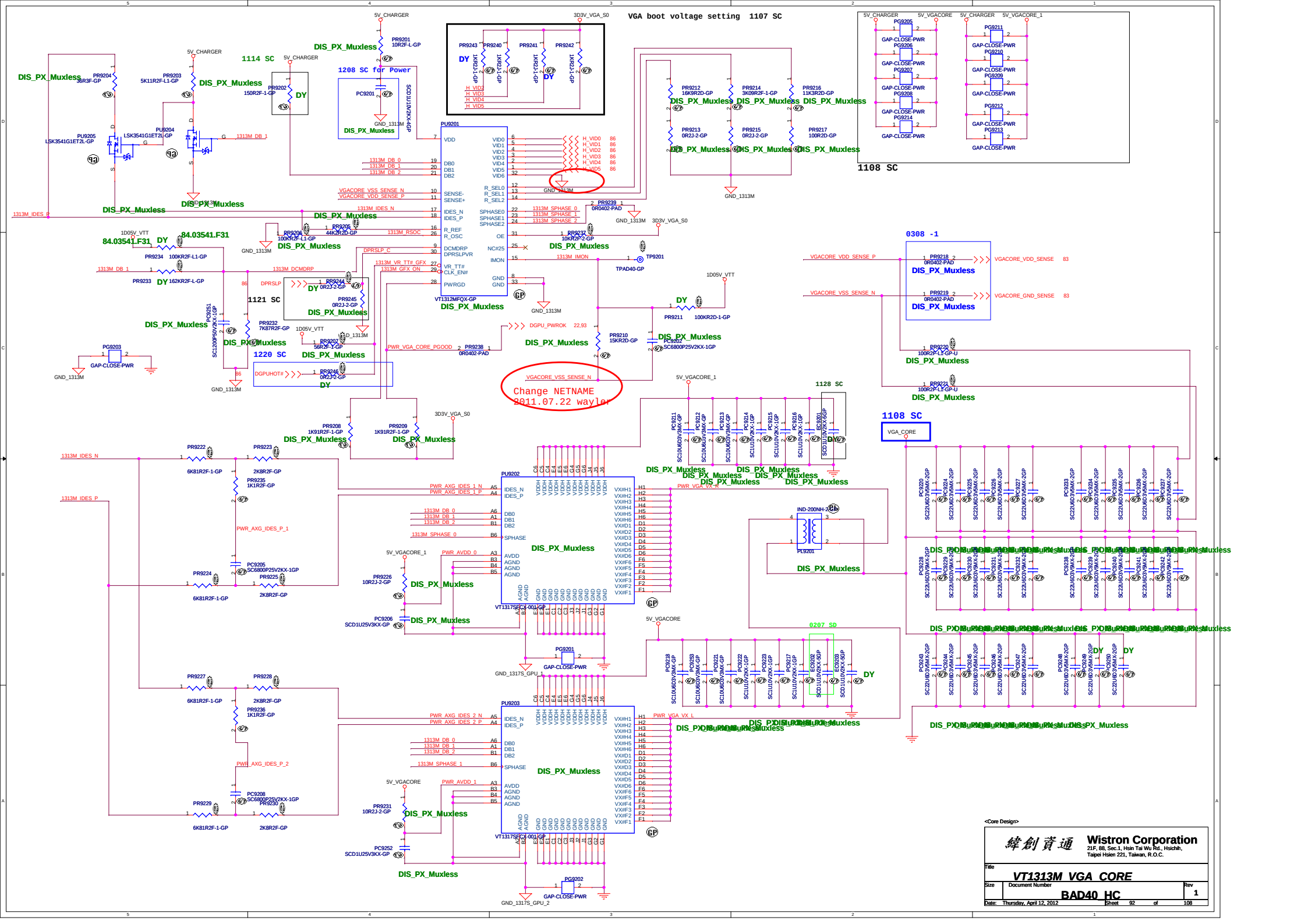
VGA boot voltage setting 1107 SC
Change NETNAME
2011.07.22 wayler
1108 SC
1114 SC
1208 SC for Power
1121 SC
1220 SC
1128 SC
0308 -1
0207 SD
VT1312MFQX-GP
VT1317SFCX-001-GP
DIS_PX_Muxless
DY
GAP-CLOSE-PWR
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VT1313M VGA CORE
BAD40_HC
Rev 1
Thursday, April 12, 2012
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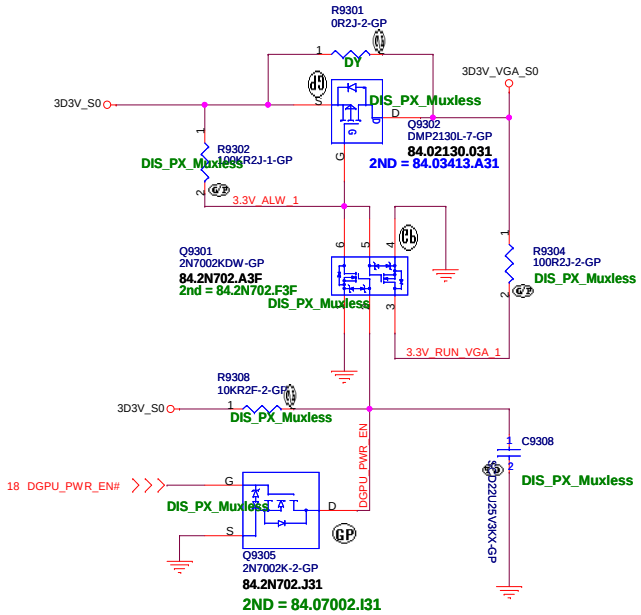
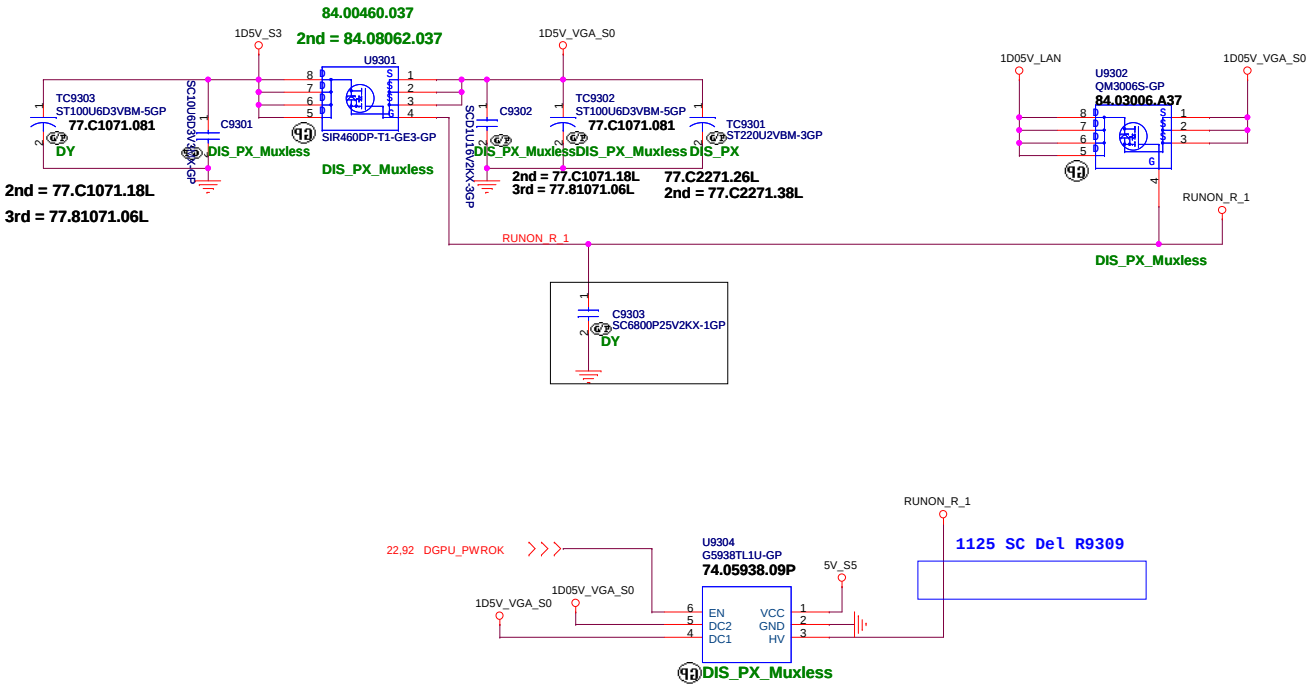
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0



1D8V_S0 to 1D8V_VGA_S0

1125 SC Del Q9306

1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

<Variant Name>

緯創資通 **Wistron Corporation**
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Title: ***DISCRETE VGA POWER***

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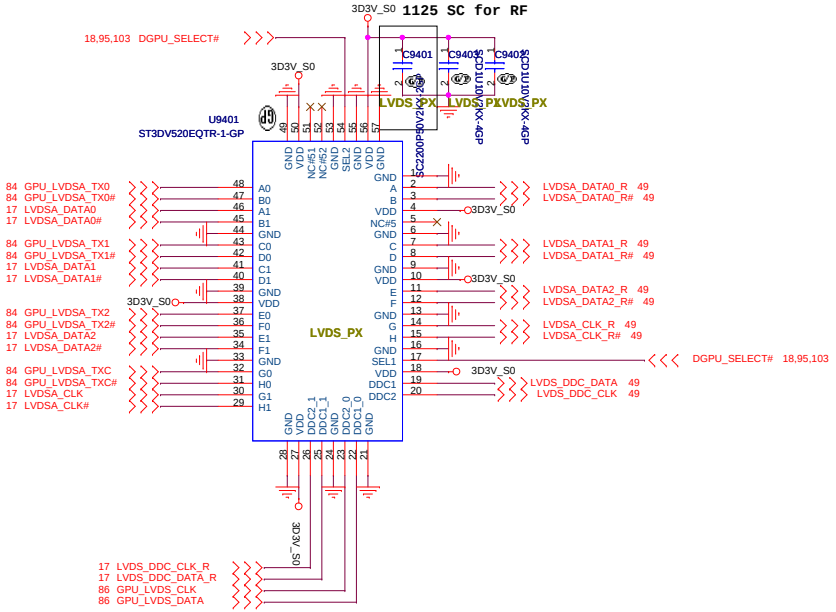
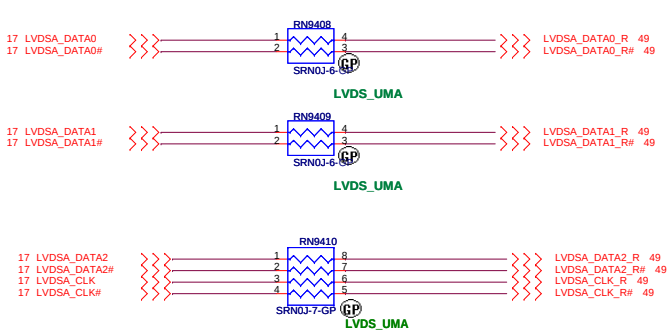
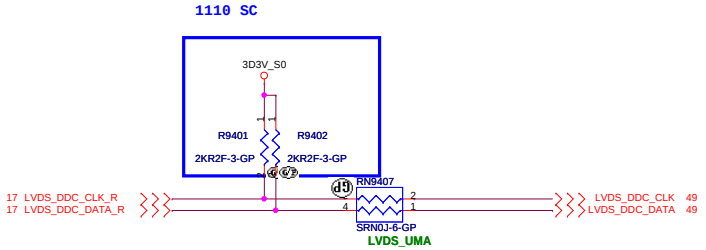
LVDS

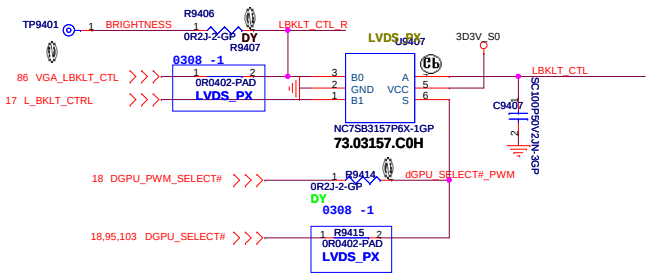




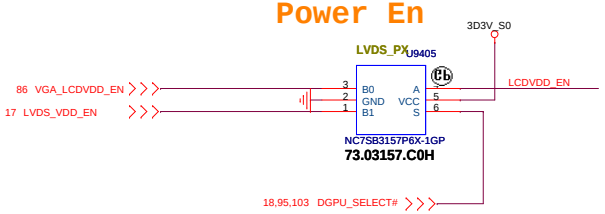
SEL->L(X=nX0),H(X=nX1)
SEL1 Control A~H
SEL2 Control DDC1,DDC2



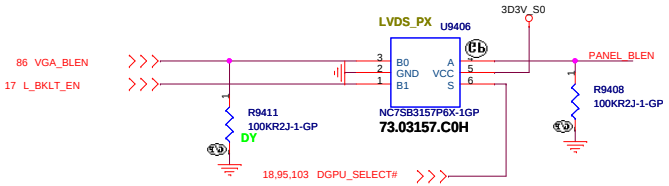
Panel BL brightness



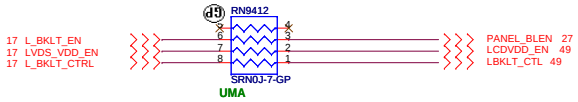
Power En



BL En



Panel BL brightness/Power En/BL En



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *LVDS_Switch*

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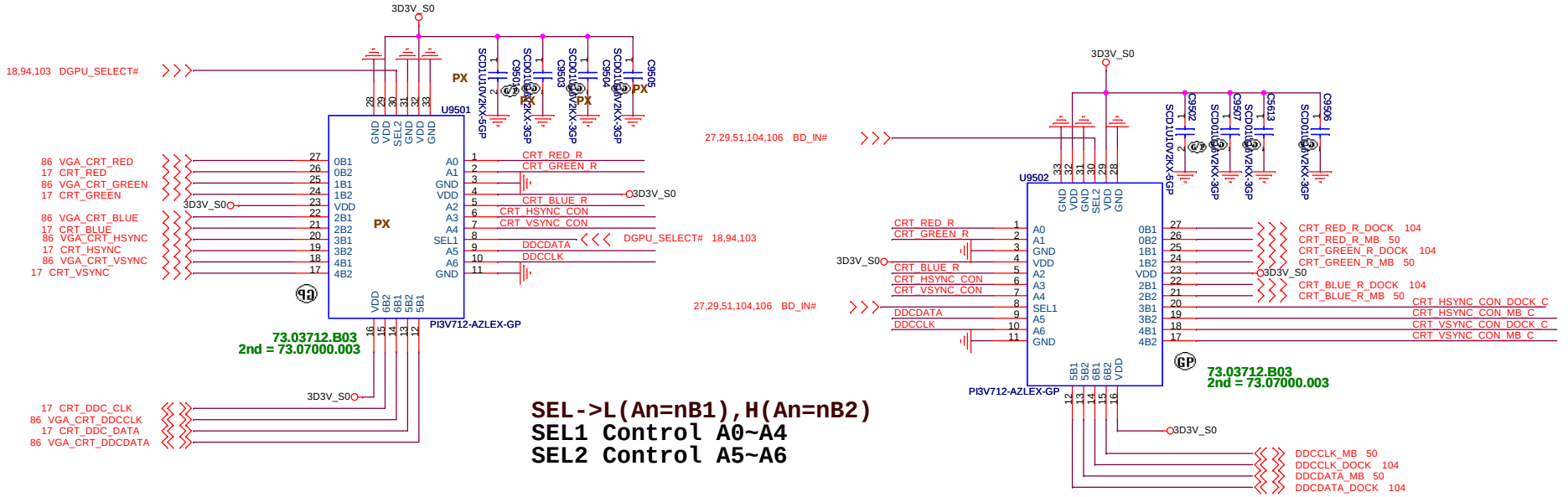
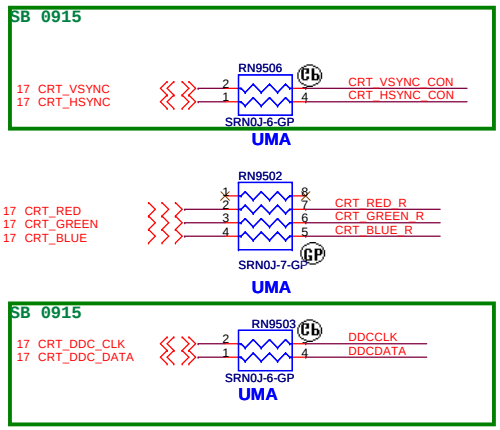
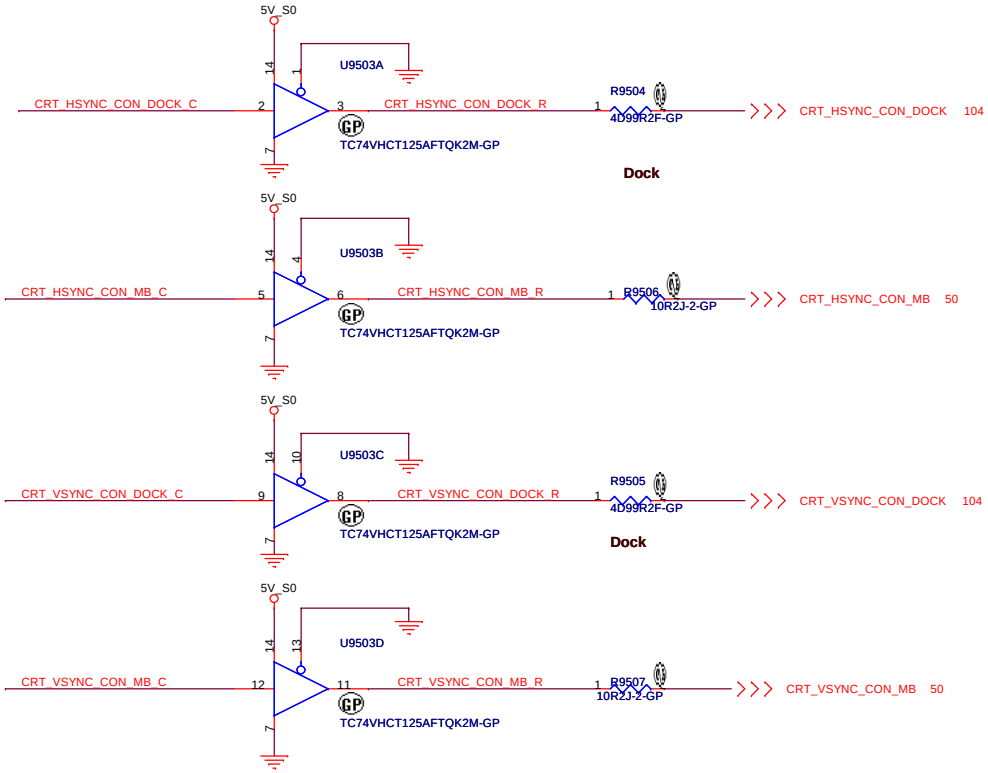
CRT DDCDATA & DDCCLK



SEL->L(An=nB1),H(An=nB2)
SEL1 Control A0~A4
SEL2 Control A5~A6





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT_Switch**

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SSID = SDIO

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TOUCH PANEL***

Size	Document Number	Rev
A2	BAD40_HC	1

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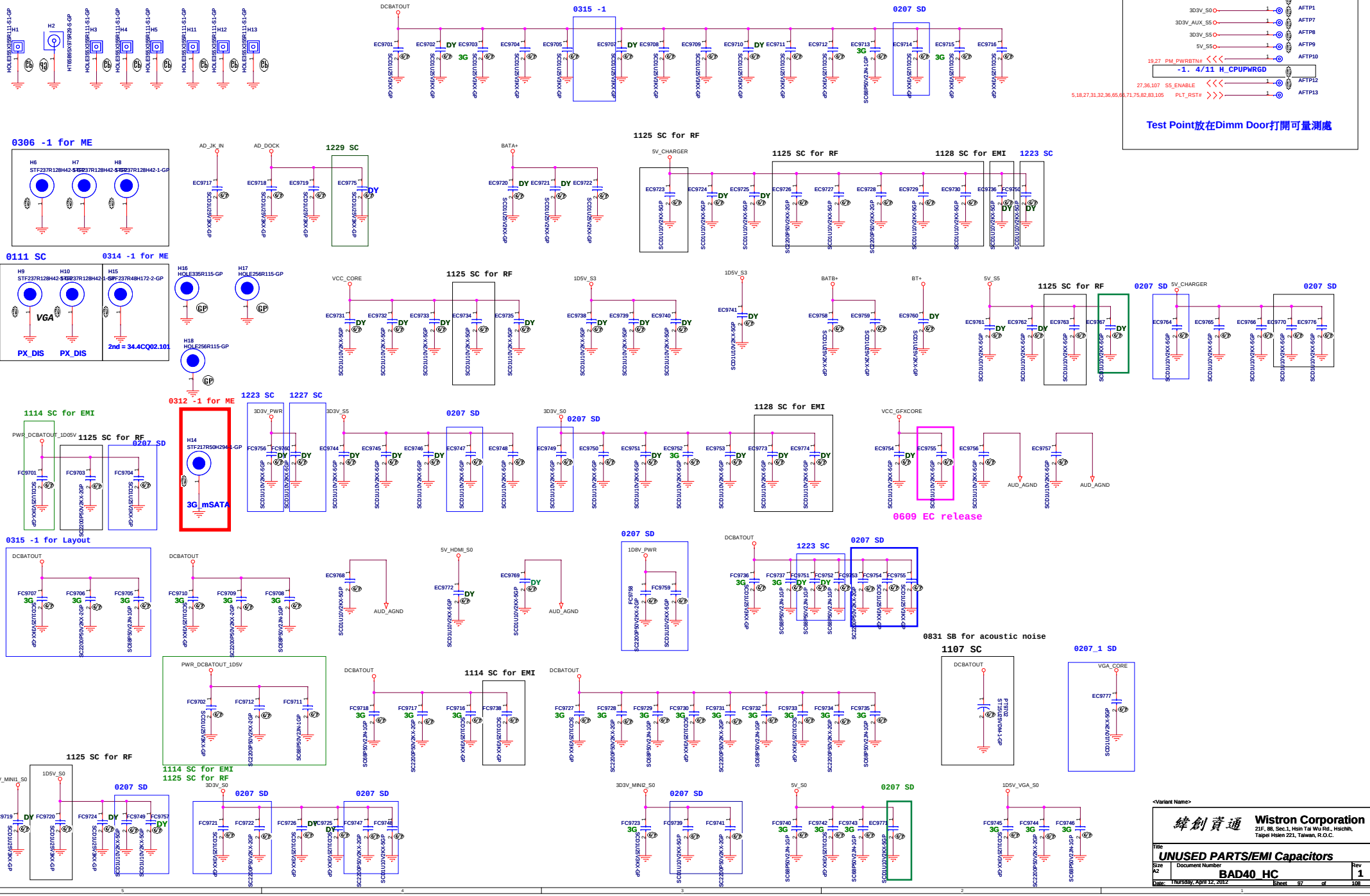
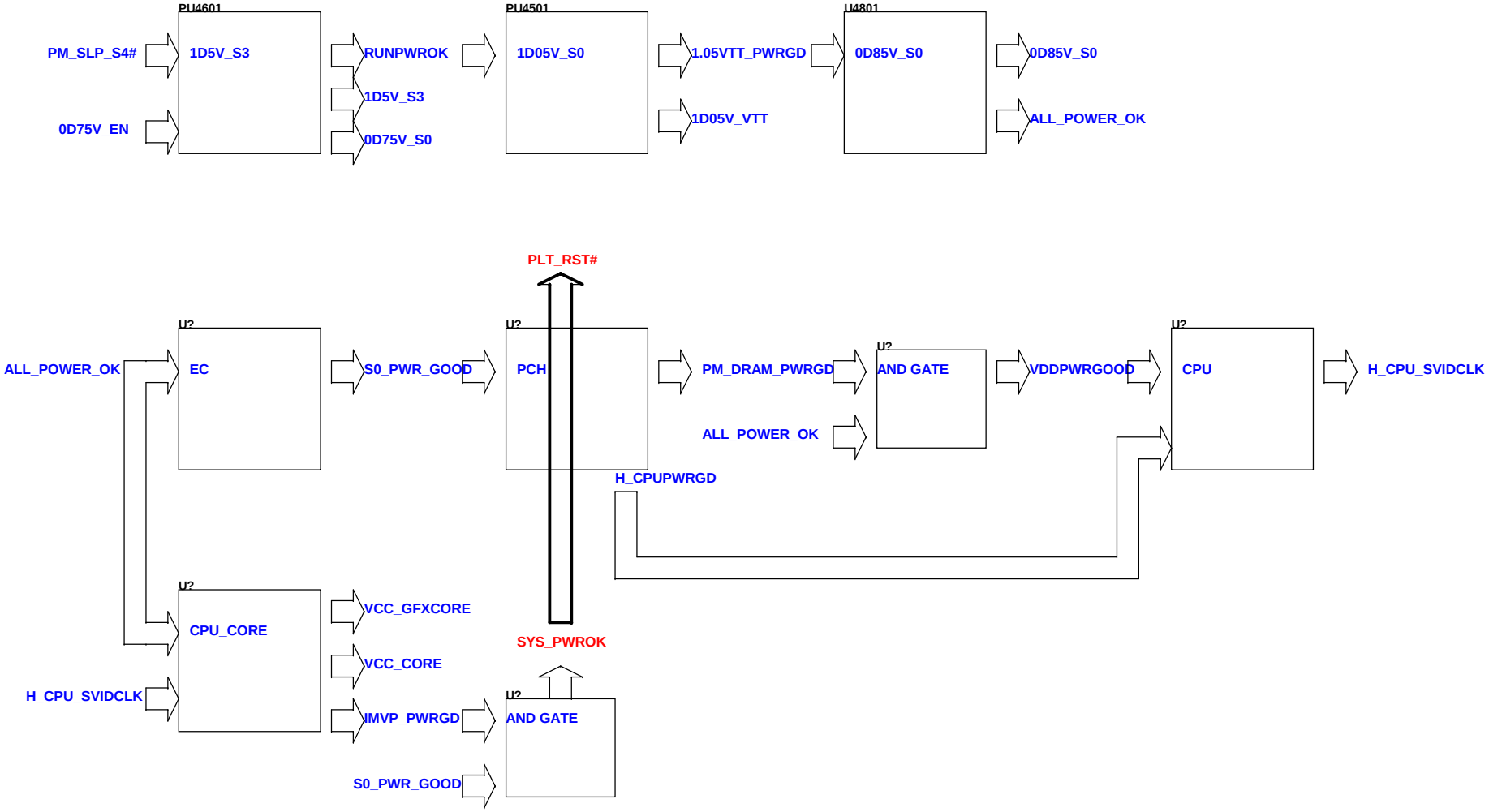

Check test point
3D3V_S0
3D3V_AUX_S5
3D3V_S5
5V_S5
19,27 PM_PWRBTN#
-1. 4/11 H_CPUPWRGD
27,36,107 S5_ENABLE
5,18,27,31,32,36,65,66,71,75,82,83,105 PLT_RST#
AFTP1
AFTP7
AFTP8
AFTP9
AFTP10
AFTP12
AFTP13
Test Point放在Dimm Door打開可量測處
0315 -1
0207 SD
0306 -1 for ME
1125 SC for RF
1128 SC for EMI
1223 SC
1229 SC
0111 SC
0314 -1 for ME
VGA
PX_DIS
2nd = 34.4CQ02.101
1125 SC for RF
1125 SC for RF
1207 SD
0312 -1 for ME
1223 SC
1227 SC
1114 SC for EMI
1125 SC for RF
0207 SD
1128 SC for EMI
3G_mSATA
0609 EC release
0315 -1 for Layout
0207 SD
1223 SC
0207 SD
0831 SB for acoustic noise
1107 SC
0207_1 SD
1125 SC for RF
1114 SC for EMI
1125 SC for RF
0207 SD
0207 SD
0207 SD
0207 SD
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
UNUSED PARTS/EMI Capacitors
Size A2
Document Number
BAD40_HC
Rev 1
Date: Thursday, April 12, 2012
Sheet 97 of 108

Power Sequence



<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Change History***

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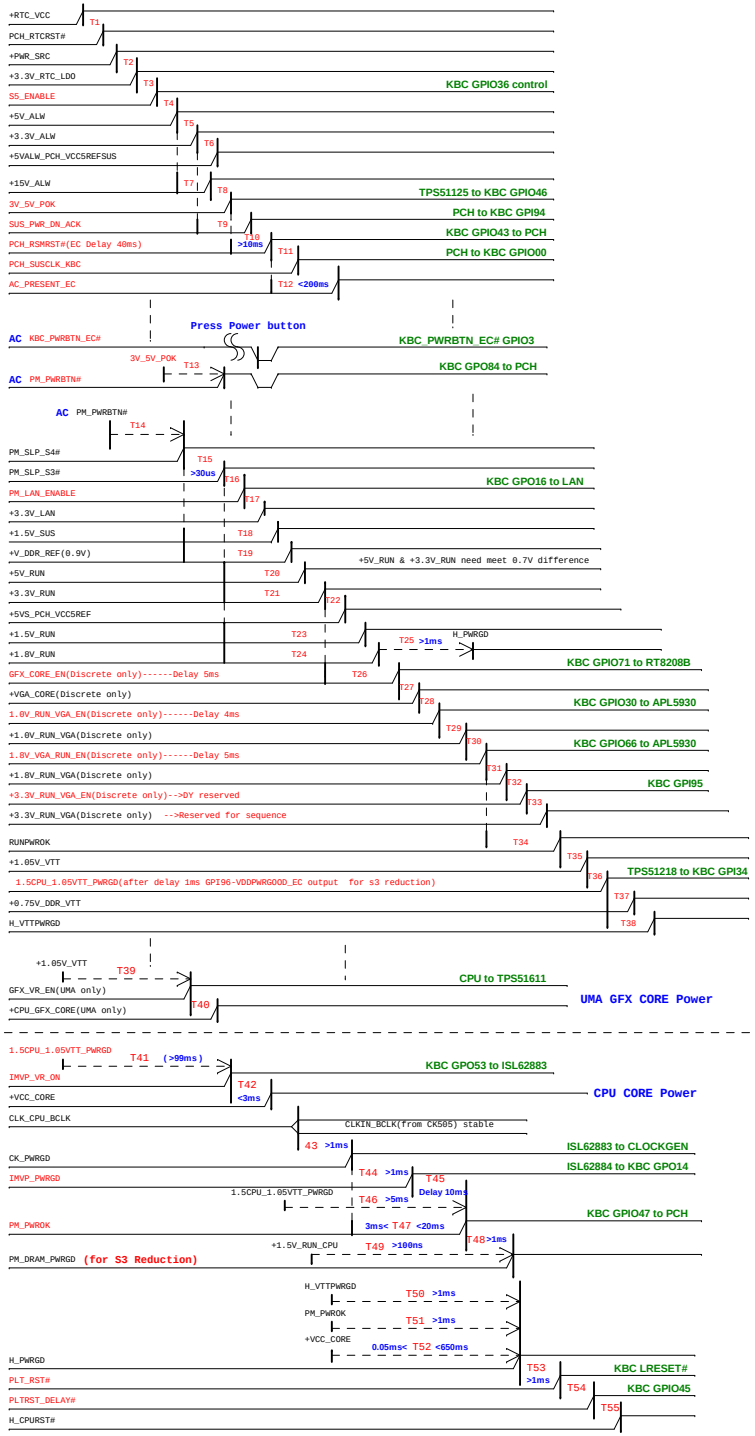
Intel-Power Up Sequence

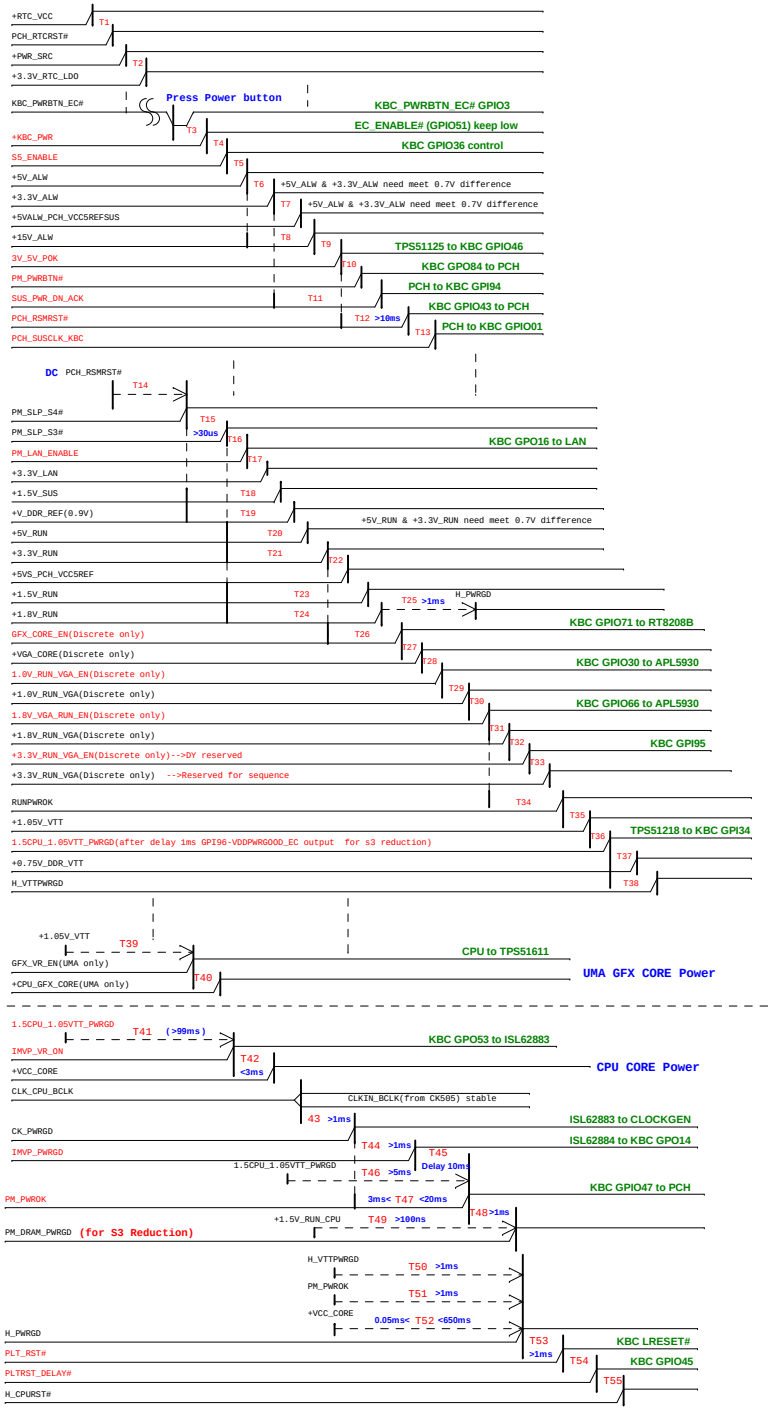
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



Wistron Corporation			
Title: Power Sequence			
Size: A3	Document Number: BAD40_HC		Rev: 1
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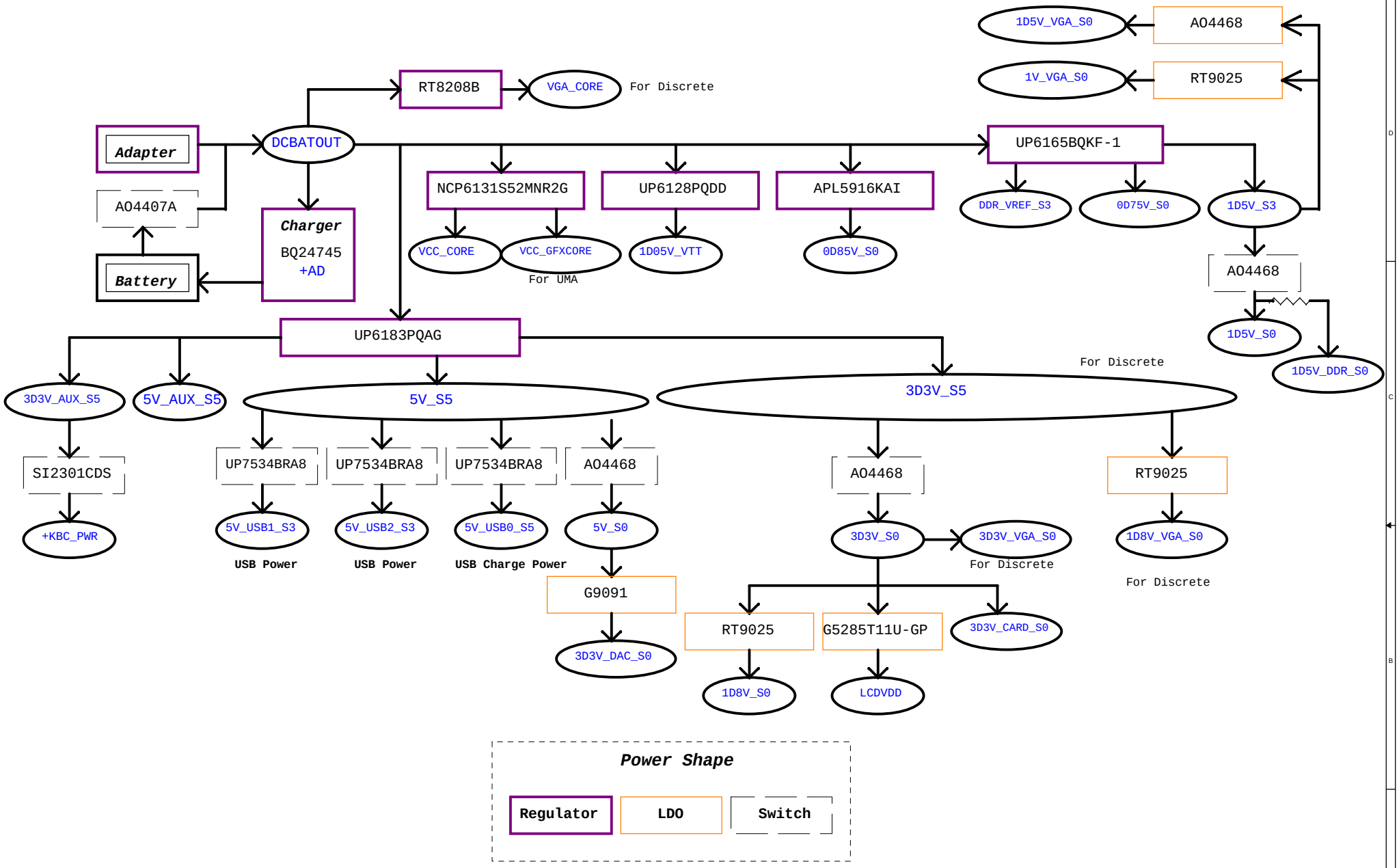

HR PX

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
A3	BAD40 HC	1

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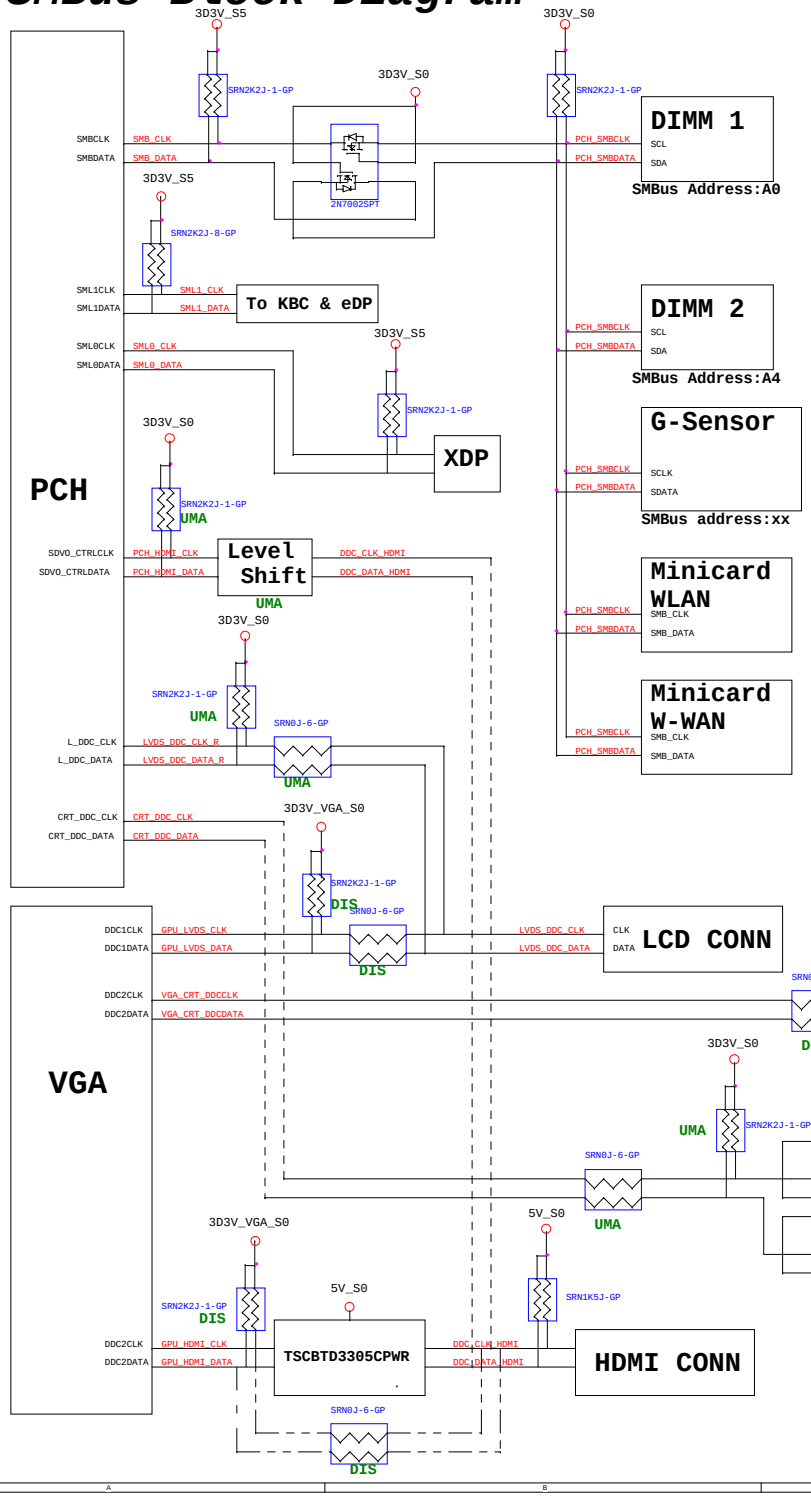
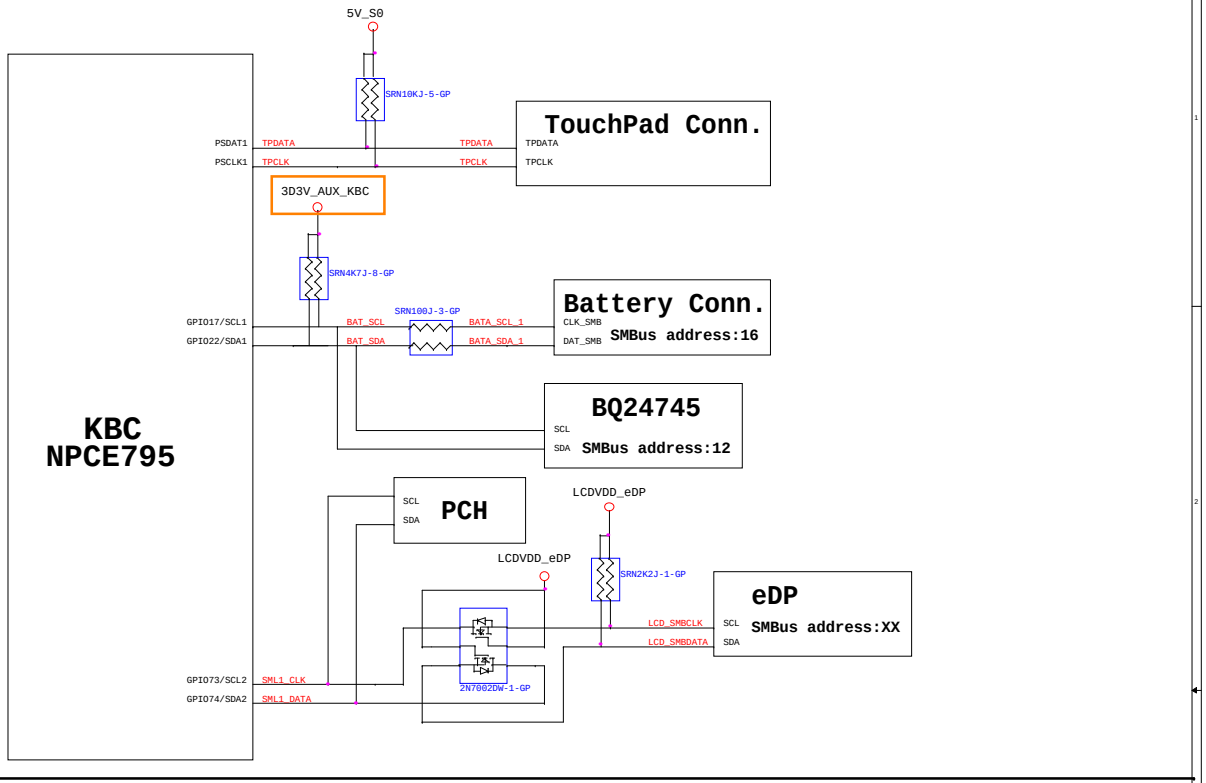
PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	BAD40_HC	1

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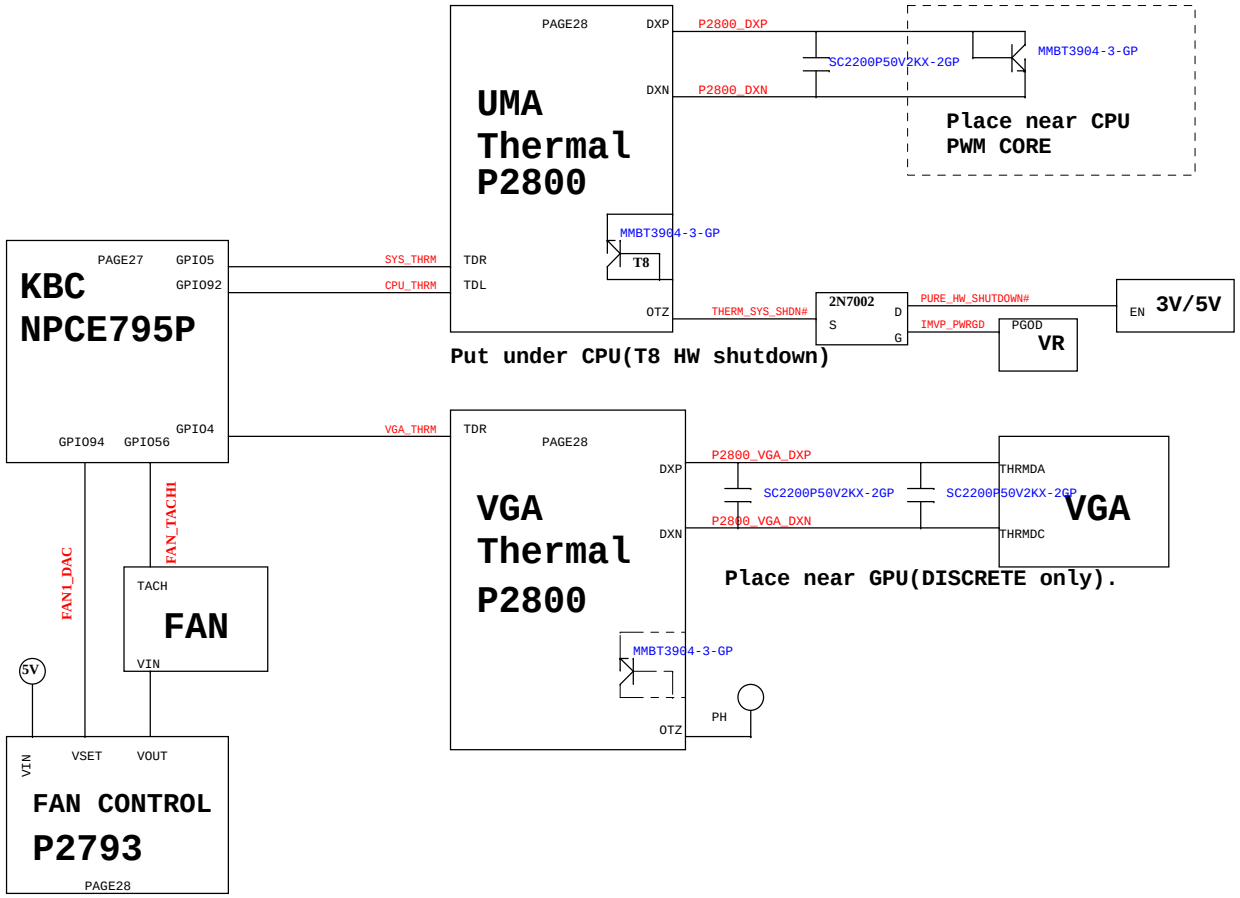
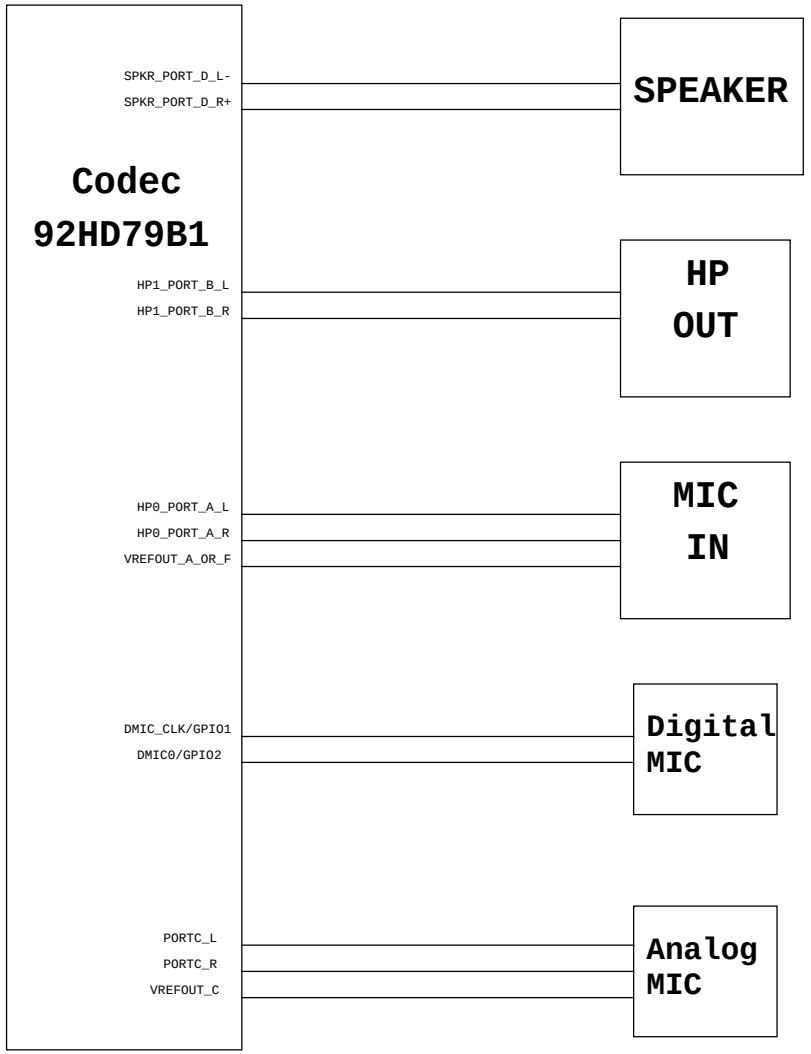
Thermal Block Diagram



Audio Block Diagram



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

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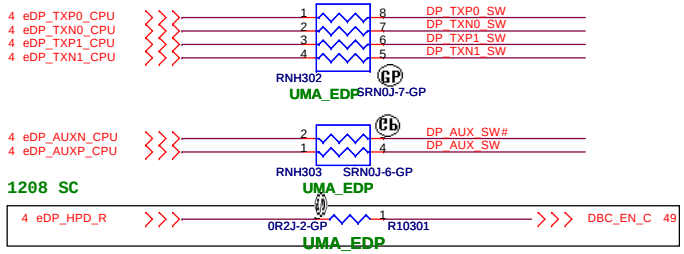
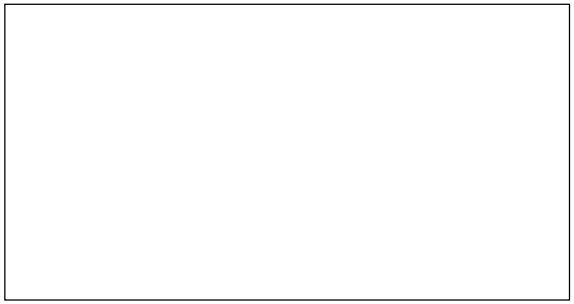
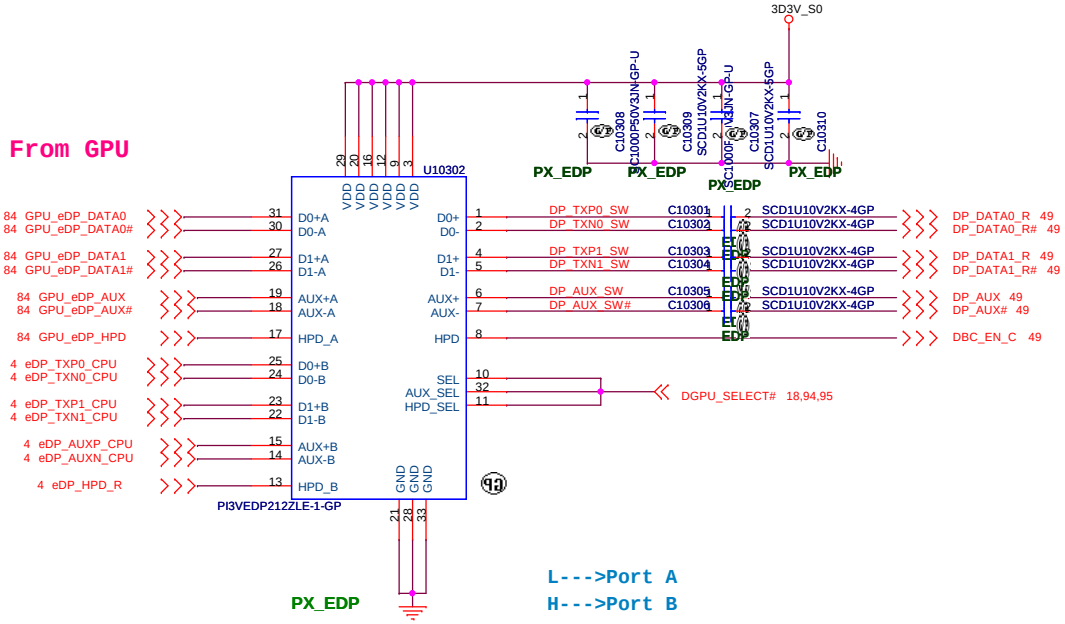


1117 SC del eDP SMBUS





<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Switch GFX DP*		
Size: A3	Document Number: BAD40 HC	Rev: 1
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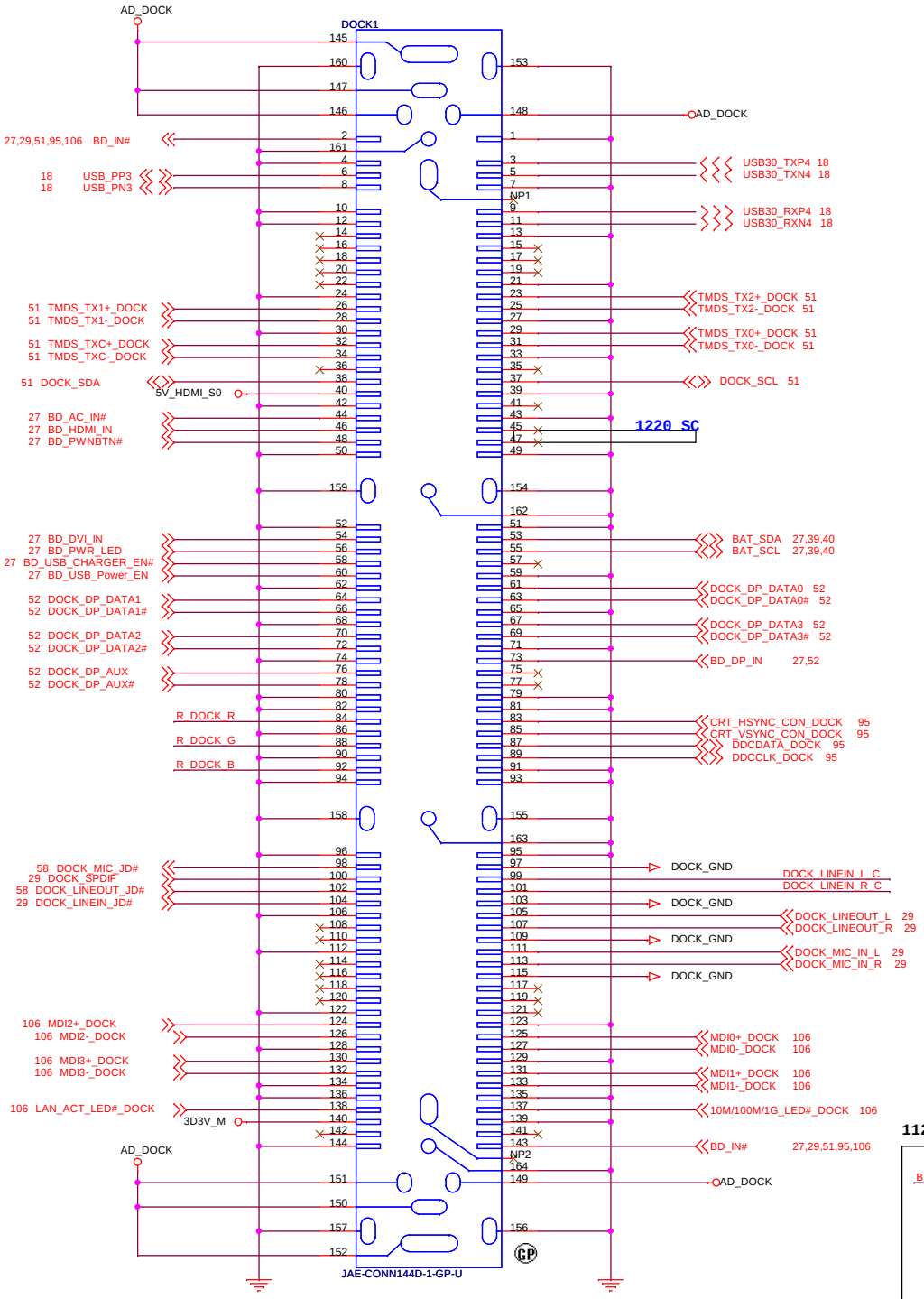
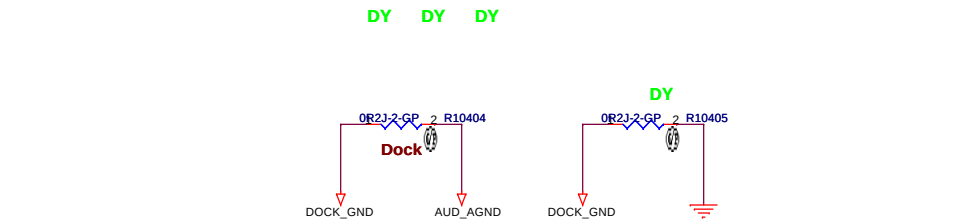
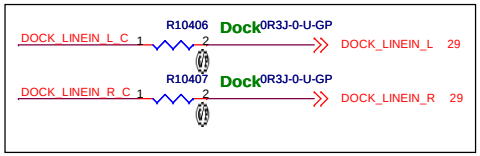
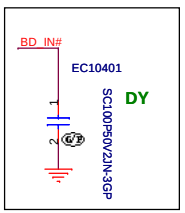




1128 SC for EMI



1128 SC for EMI



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BOTTOM DOCKING		
Size: A3	Document Number: BAD40_HC	Rev: 1
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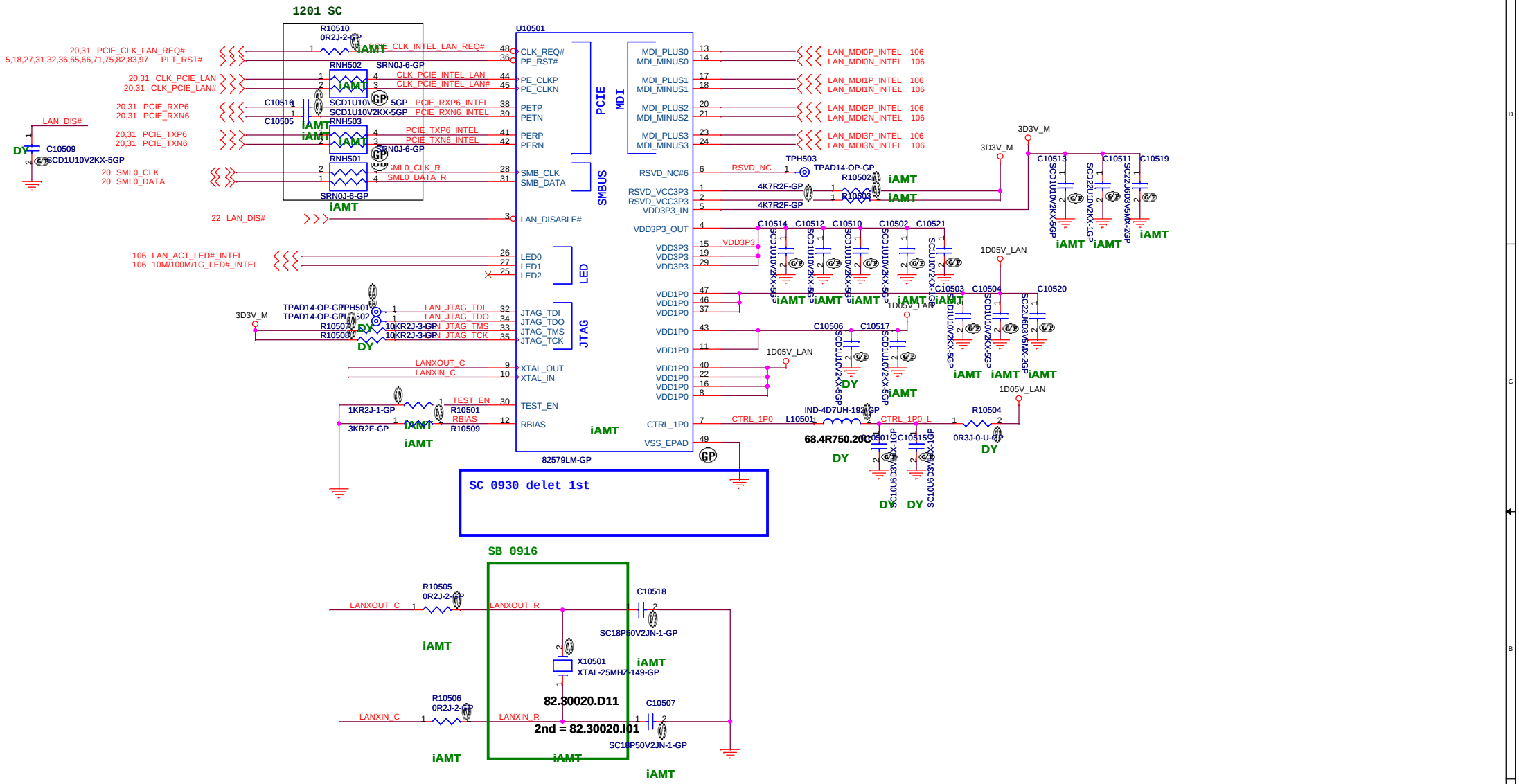

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LAN INTEL 82579
Size A3	Document Number BAD40 HC
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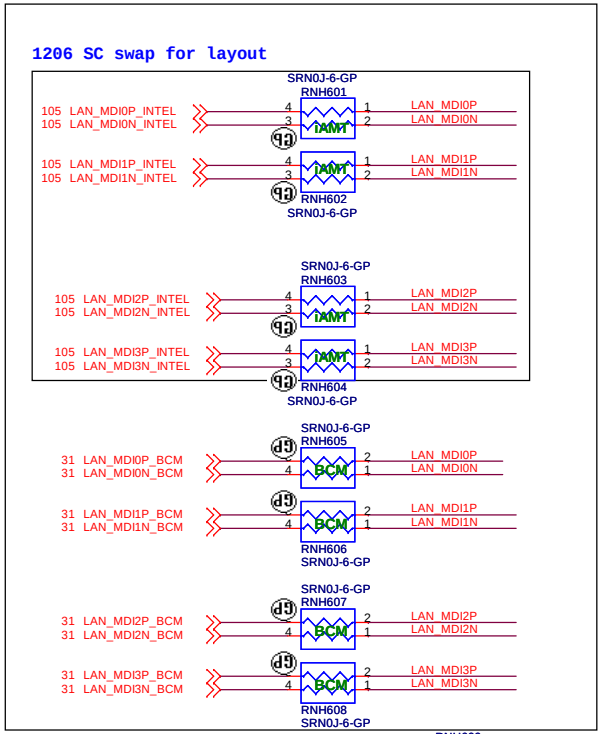
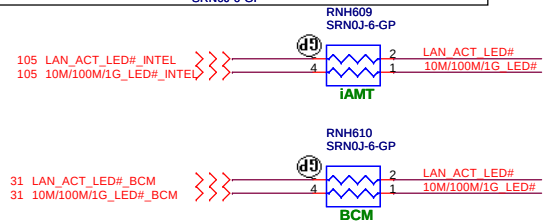
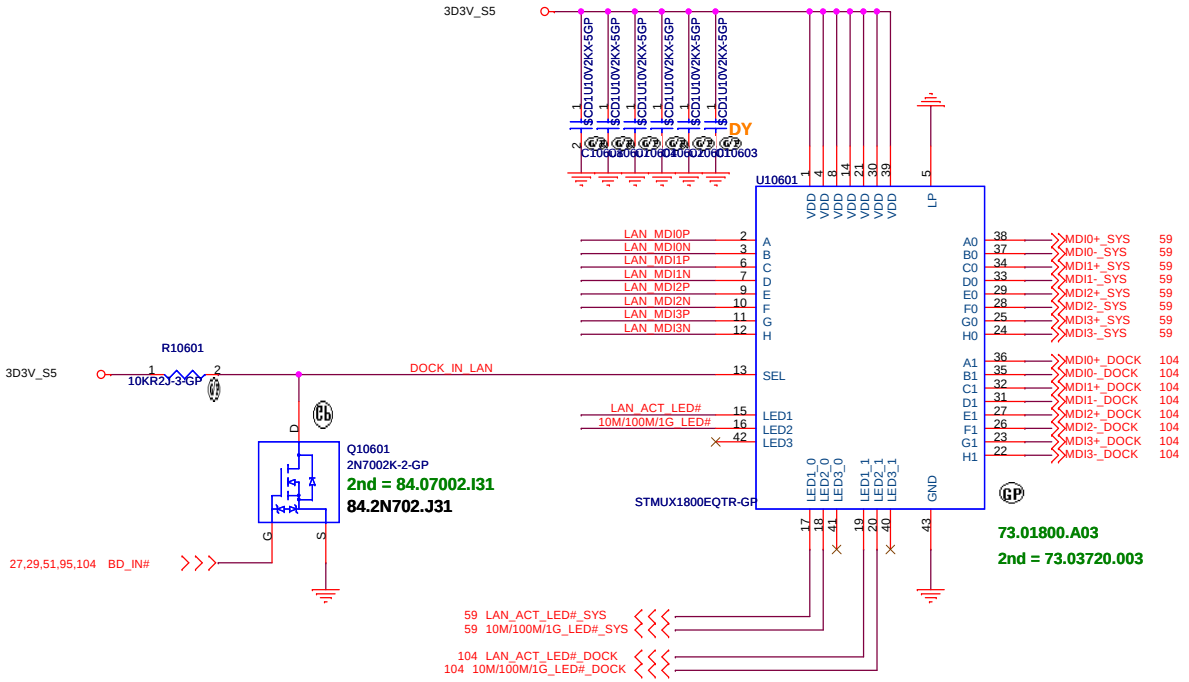
1201 SC

1206 SC swap for layout





LAN switch



Function	SEL	
to X0	L	SYSTEM
to X1	H	DOCK

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN SWITCH

Size	Document Number	Rev
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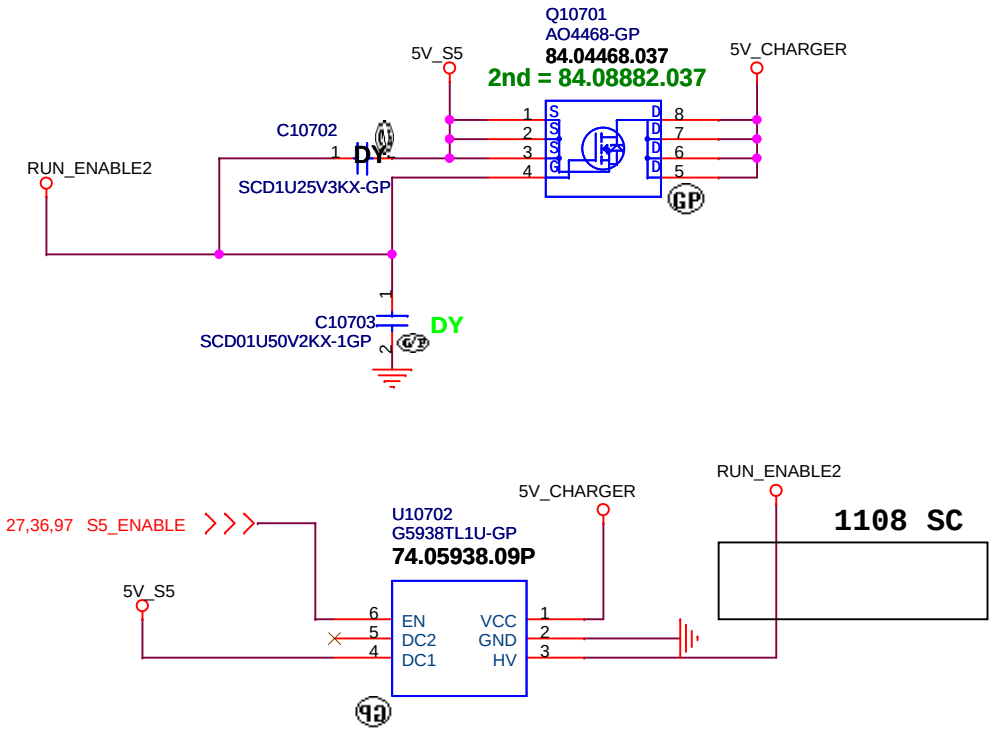

USB charger @ USB30 BD

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***USB Charger/ 5V_S5***	
Size A4	Document Number **BAD40_HC**	Rev **1**
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reserve

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB2 HUB AU6256**

Size	Document Number	Rev
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