

Compal Confidential

Huayra UMA (QCL51) Schematics Document

AMD Comal Platform

AMD Trinity APU / Hudson FCH / ATI Thames XT M2

Muxless/UMA / PX 5.0

2012-01-04

LA-8714P REV: 0.3

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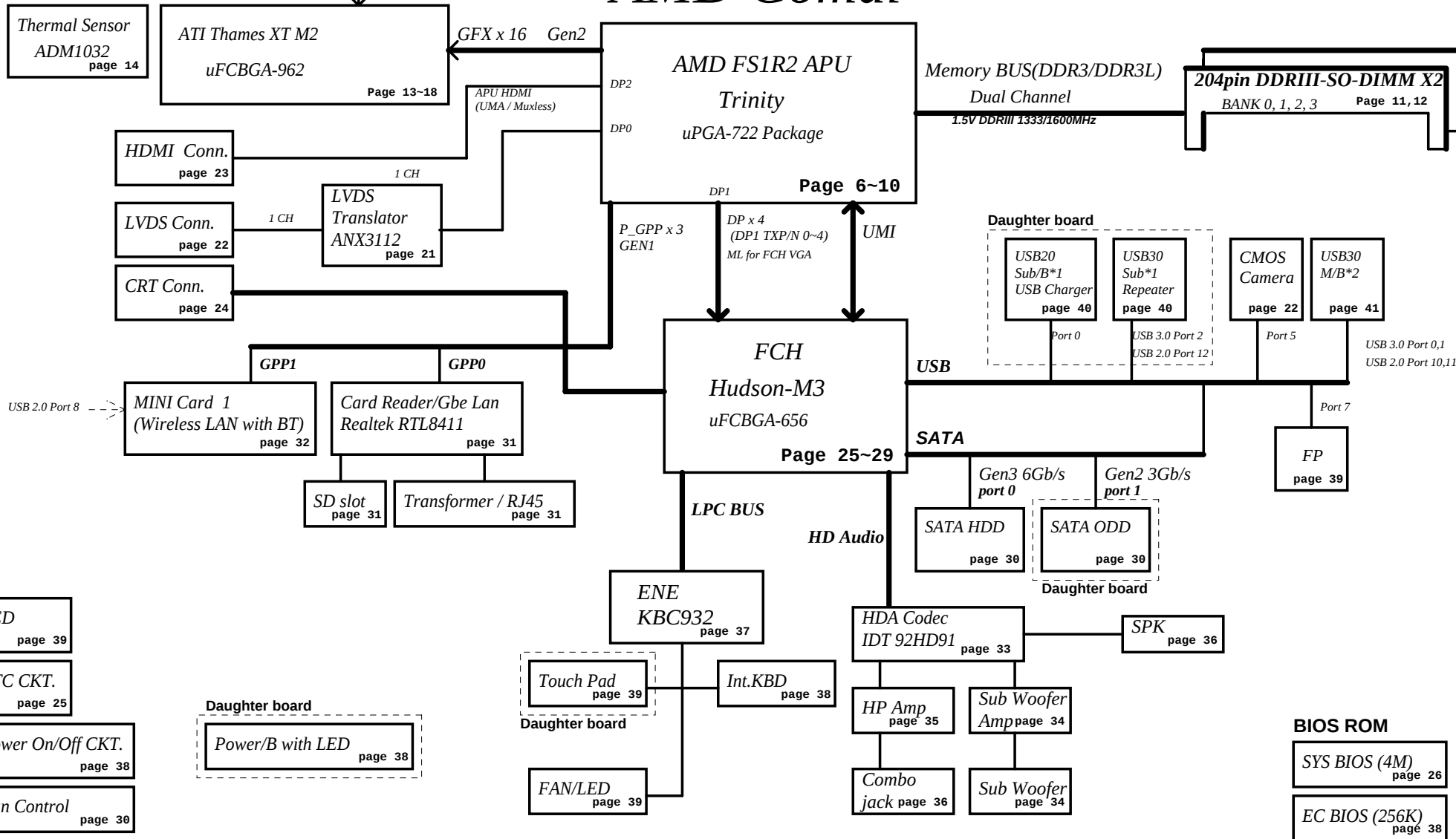
Model Name : QCL51 AMD

Board Name : LA-8712P

64M x16
128M x 16
VRAM DDR3
page 19, 20

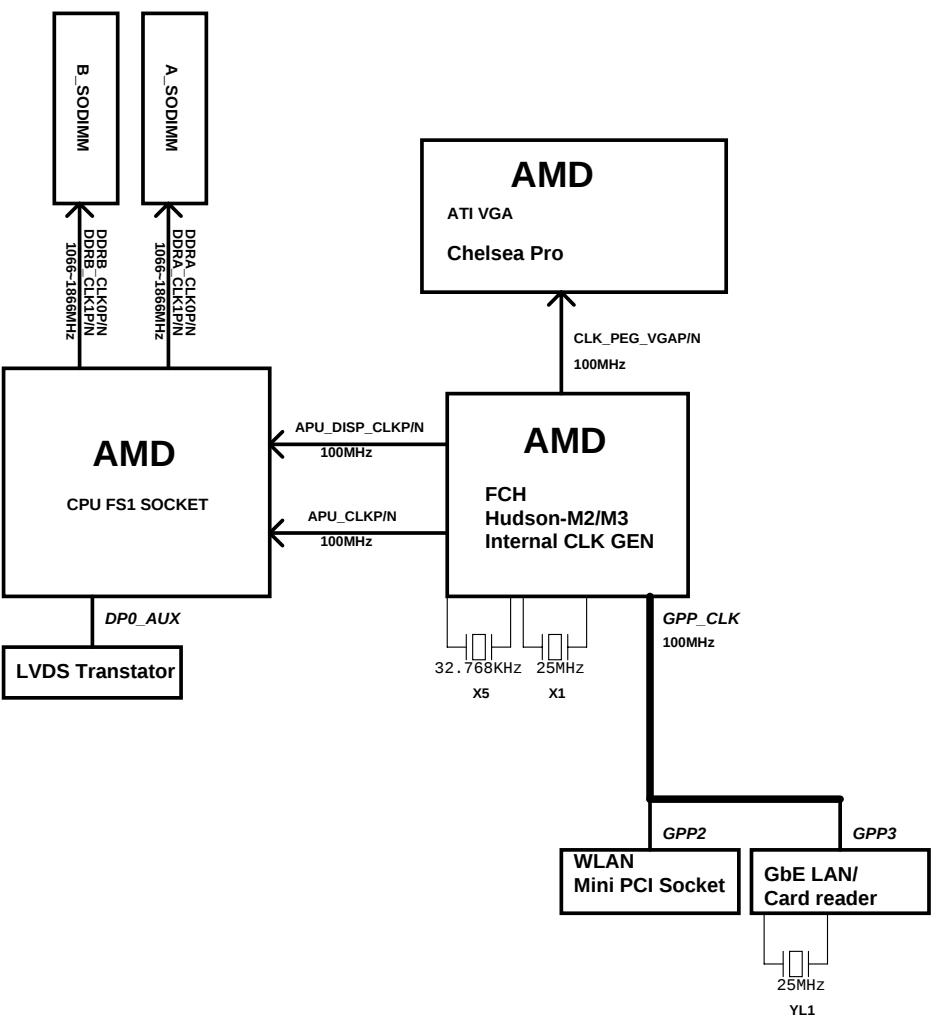
DDR3

AMD Comal

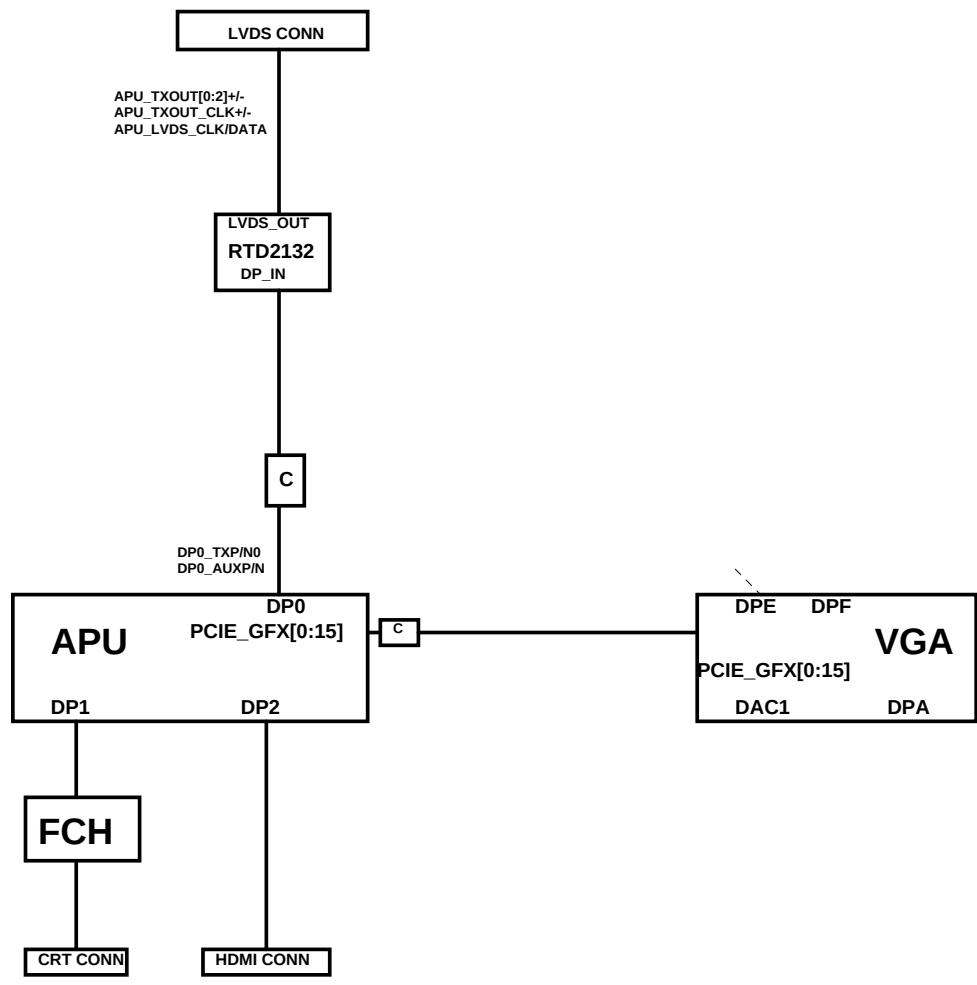


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CLOCK DISTRIBUTION



DISPLAY OUTPUT



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+0.935VGS	0.935V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5V_PCIE	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_VDD_3V3	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is writtee cmd.

External PCI Devices			
Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (GPU)	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			LVDS TR	1010 100X b	A8H
			VGA Internal Thermal	1000 001X b	82H

FCH (S0) SM Bus 0 address			FCH (S0~S5) SM Bus 1 address		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000X b	A0	Touch pad		
DDR DIMM2	1010 001X b	A2			
Amplifier					

STATE	SIGNAL							
	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

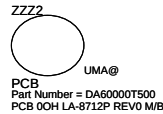
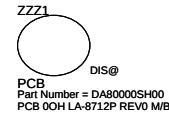
Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rb	100K +/- 5%			
Board ID	Ra / Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOM Option Table

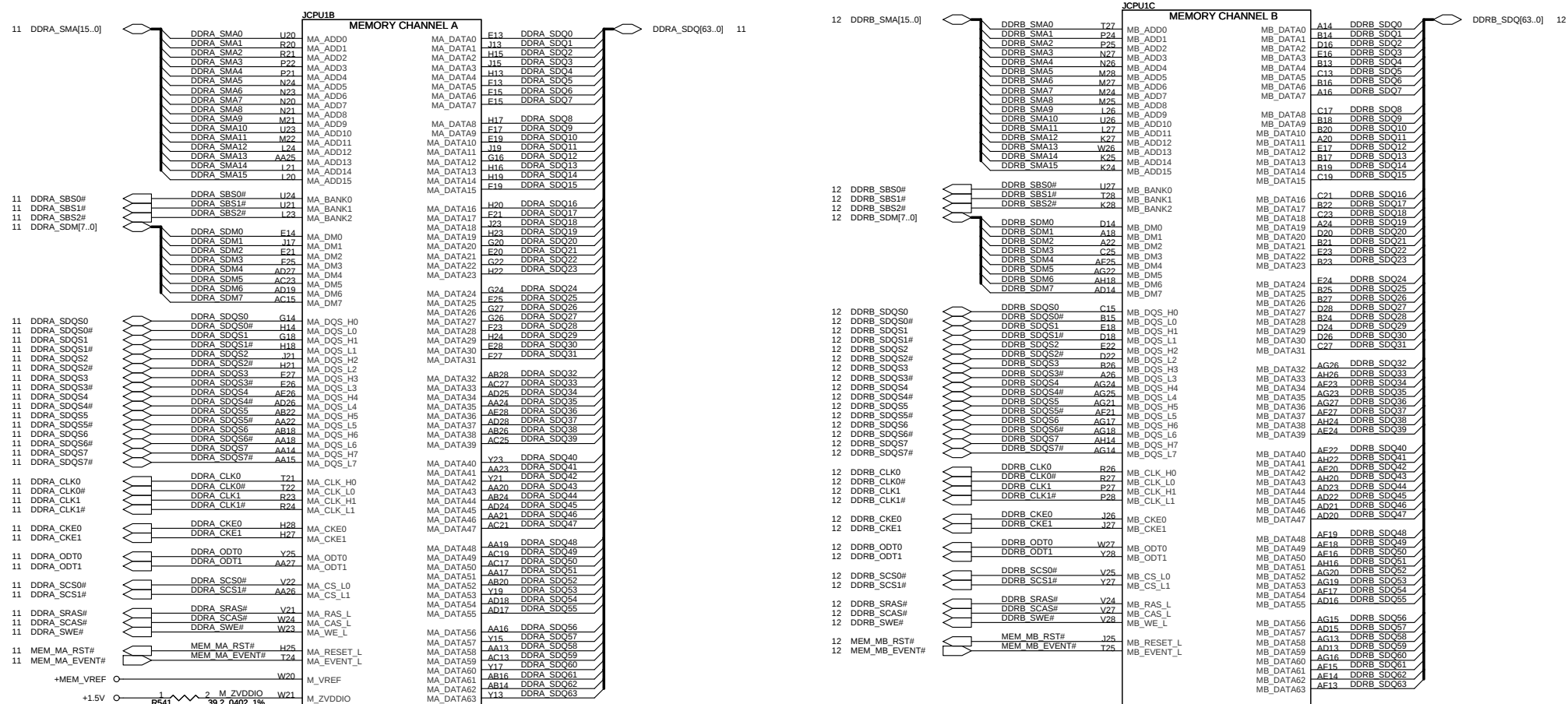
BOM Structure	Description	DIS	PX@ DIS@ Tha@
PX@	PX function	UMA	UMA@
DIS@			
UMA@			
Tha@			

BOM Config



BOARD ID Table

Board ID	PCB Revision
0	DB
1	SI



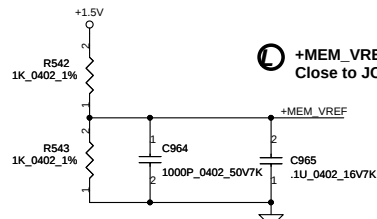
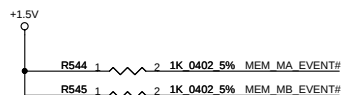
1 M_ZVDDIO W/S=8/12 mil, <1000mil

LOTES ACA-ZIF-109-P12-A_FS1R2 CONN@

0.75V reference voltage

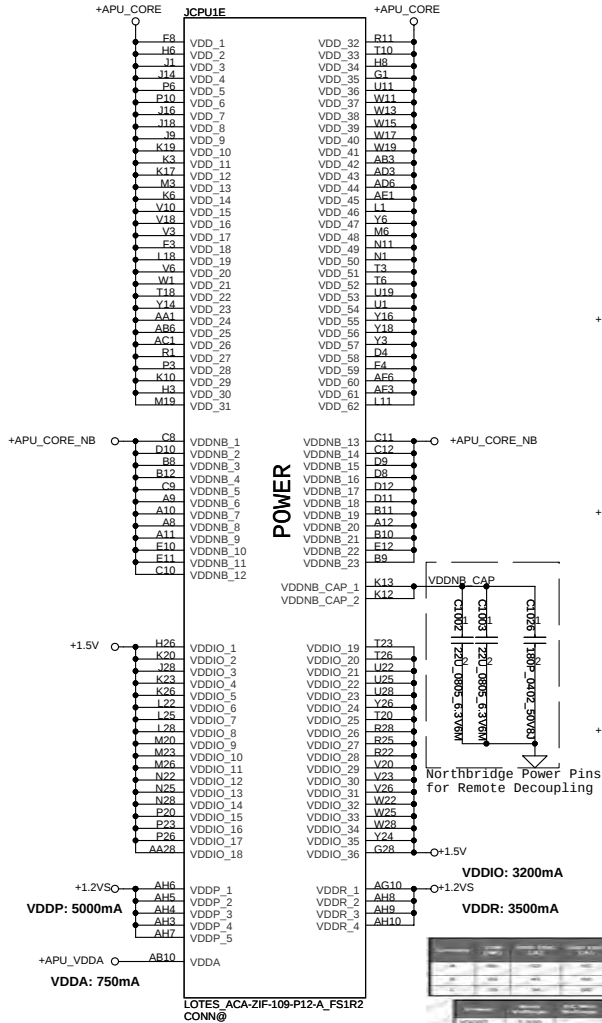
+MEM_VREF 15mil Close to JCPU1

EVENT# pull high



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Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	37A
VDDIO	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.75A



Decoupling Caps.	Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF	1nF	180pF
Pumori 2.0		0	19/11	7	5	17	3	1	1 / 1	13/3		
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2	
P5WS5	7 / 2	1	1	13	3	19	3	1	4	16		

+CPU_CORE_NB Decoupling

330uF x2
22uF x2 @ x2
10uF x1
0.22uF x2
180pF x3

+1.5V / VDDIO Decoupling

330uF x1
22uF x4
4.7uF x4
0.22uF x6
180pF x1 @x1

VDDR Decoupling
Close JCPU1.AG10,AH8,AH9,AH10

10uF x3
0.22uF x2
1000pF x1
180pF x2

VDDP Decoupling
Close JCPU1.AH3-7

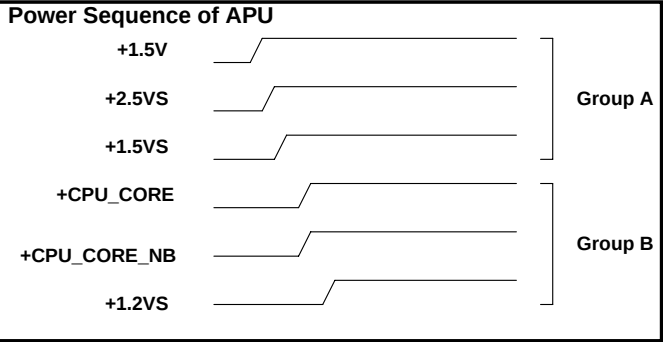
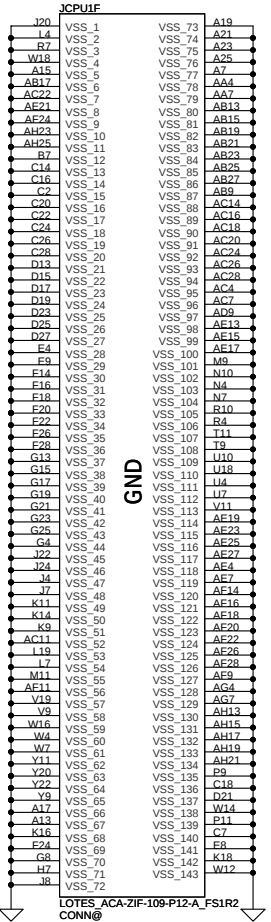
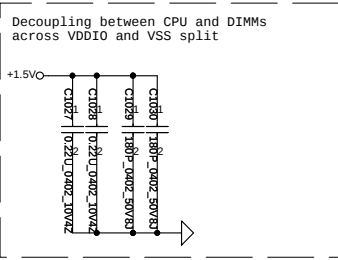
22uF x1
10uF x3
0.22uF x2
1000pF @x1
180pF x2

VDDA Decoupling

47uF x1
0.22uF x1
3300pF x1
180pF x1

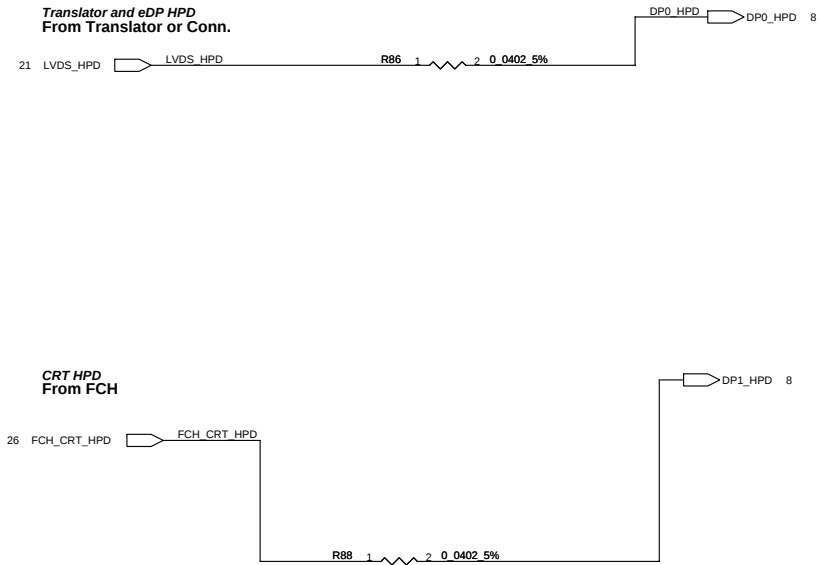
+CPU_CORE Decoupling

330uF x4 @ x1
22uF x10
0.22uF x2
0.01uF x3
180pF x2 @ x1

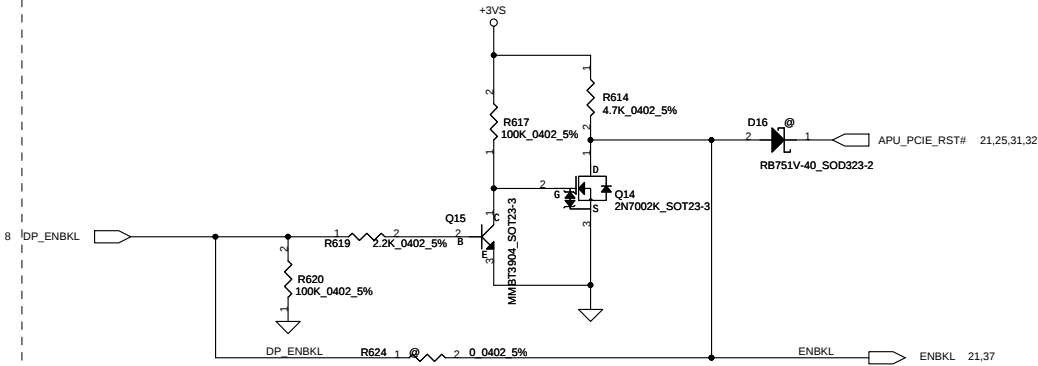


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HPD

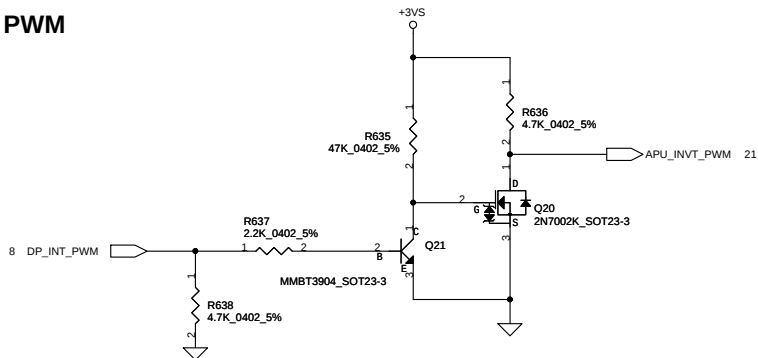


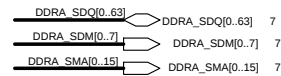
Panel ENBKL



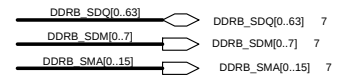
eDP Panel ENVDD

Panel PWM





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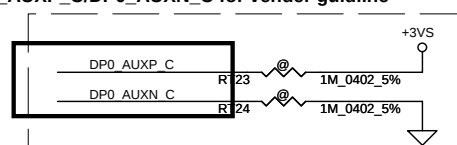
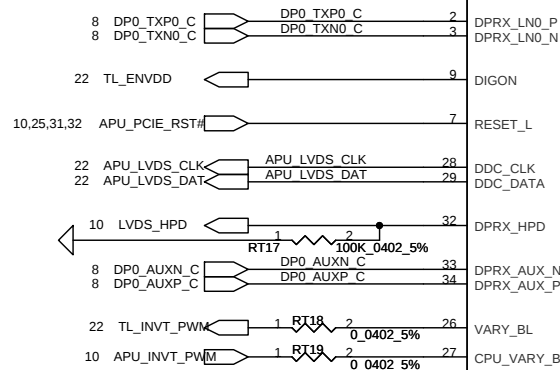
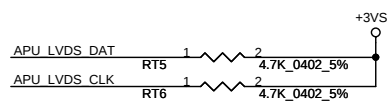
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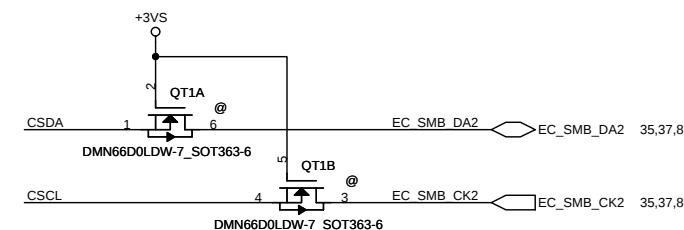
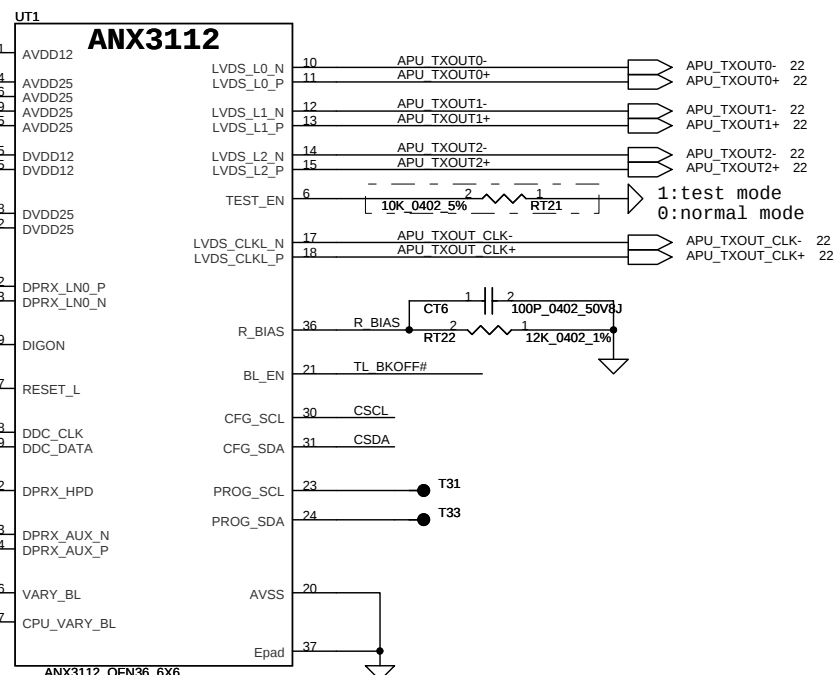
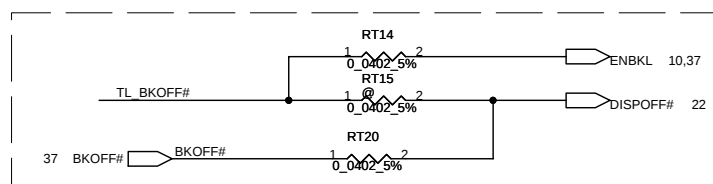
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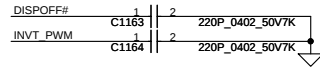
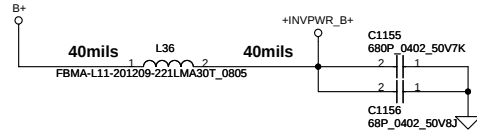
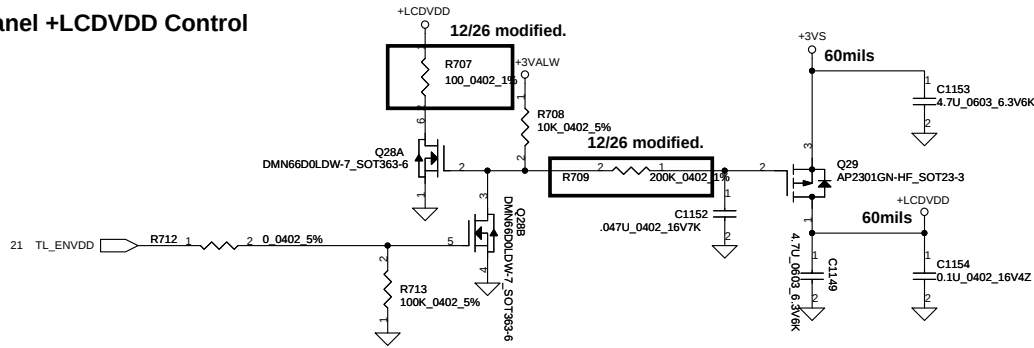


Place via on each trace bus and let resistor very close the via

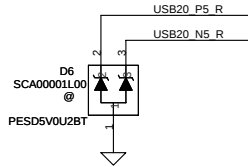
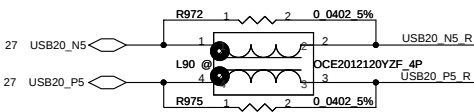
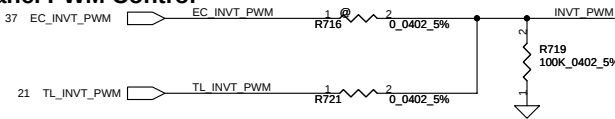


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Panel +LCDVDD Control

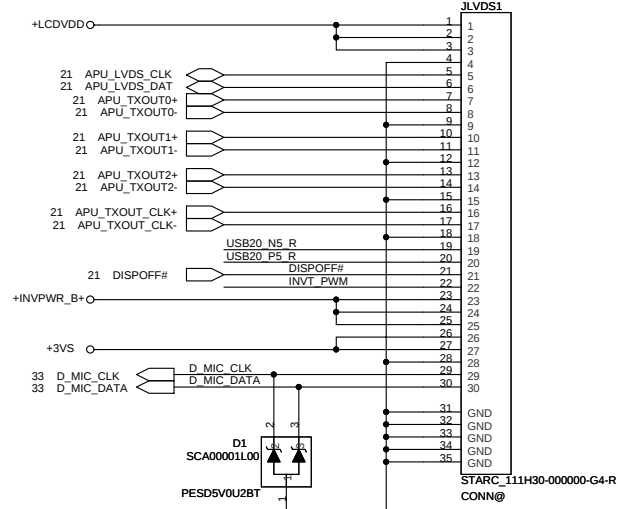


Panel PWM Control



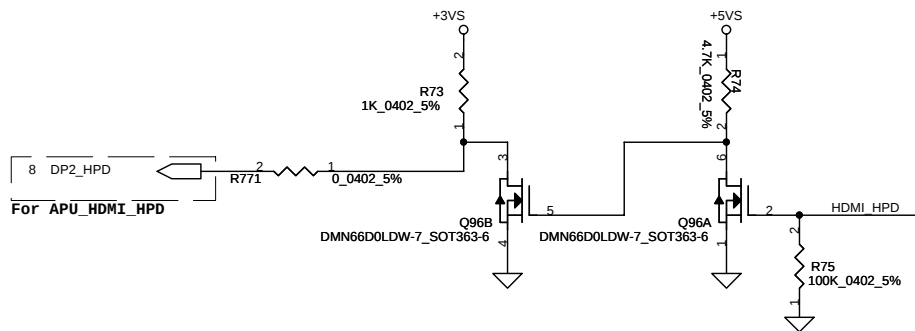
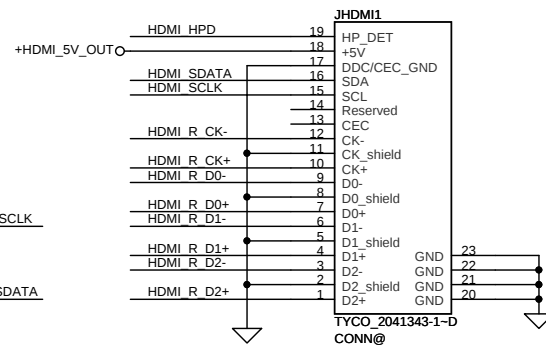
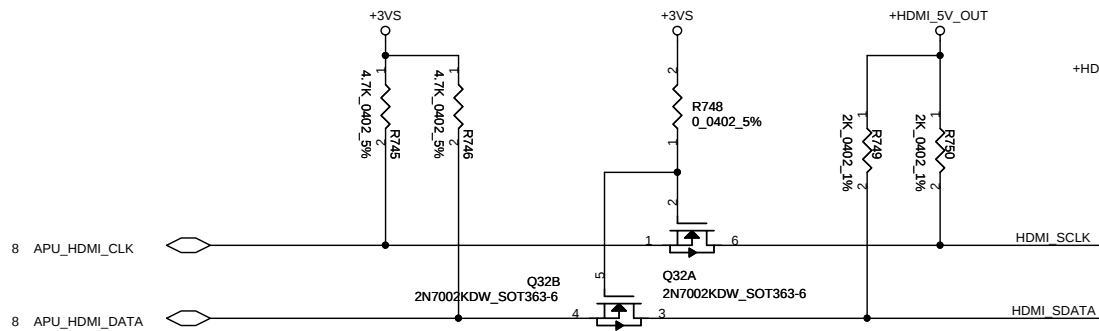
<Translator LVDS Output>

LVDS Connector

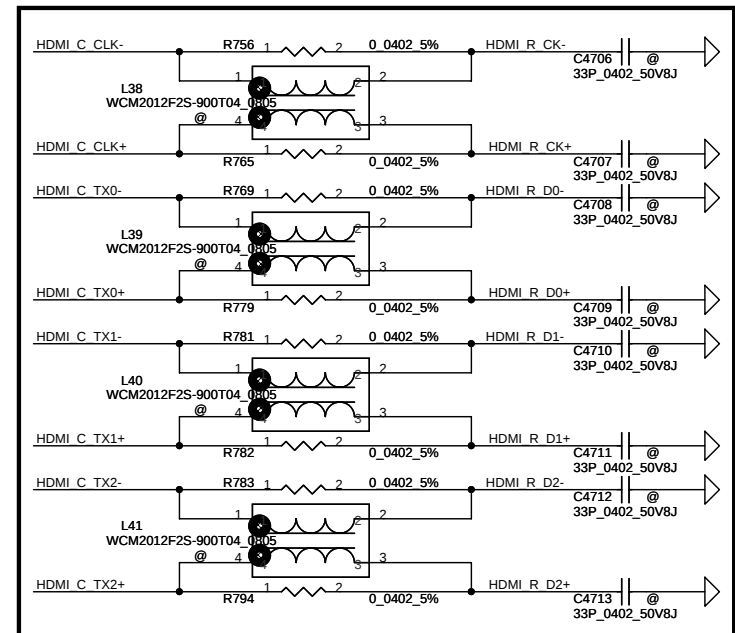


no updated.
11/10 follow QCL50

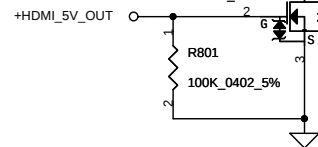
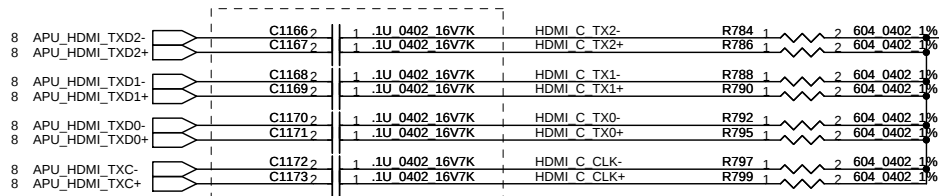
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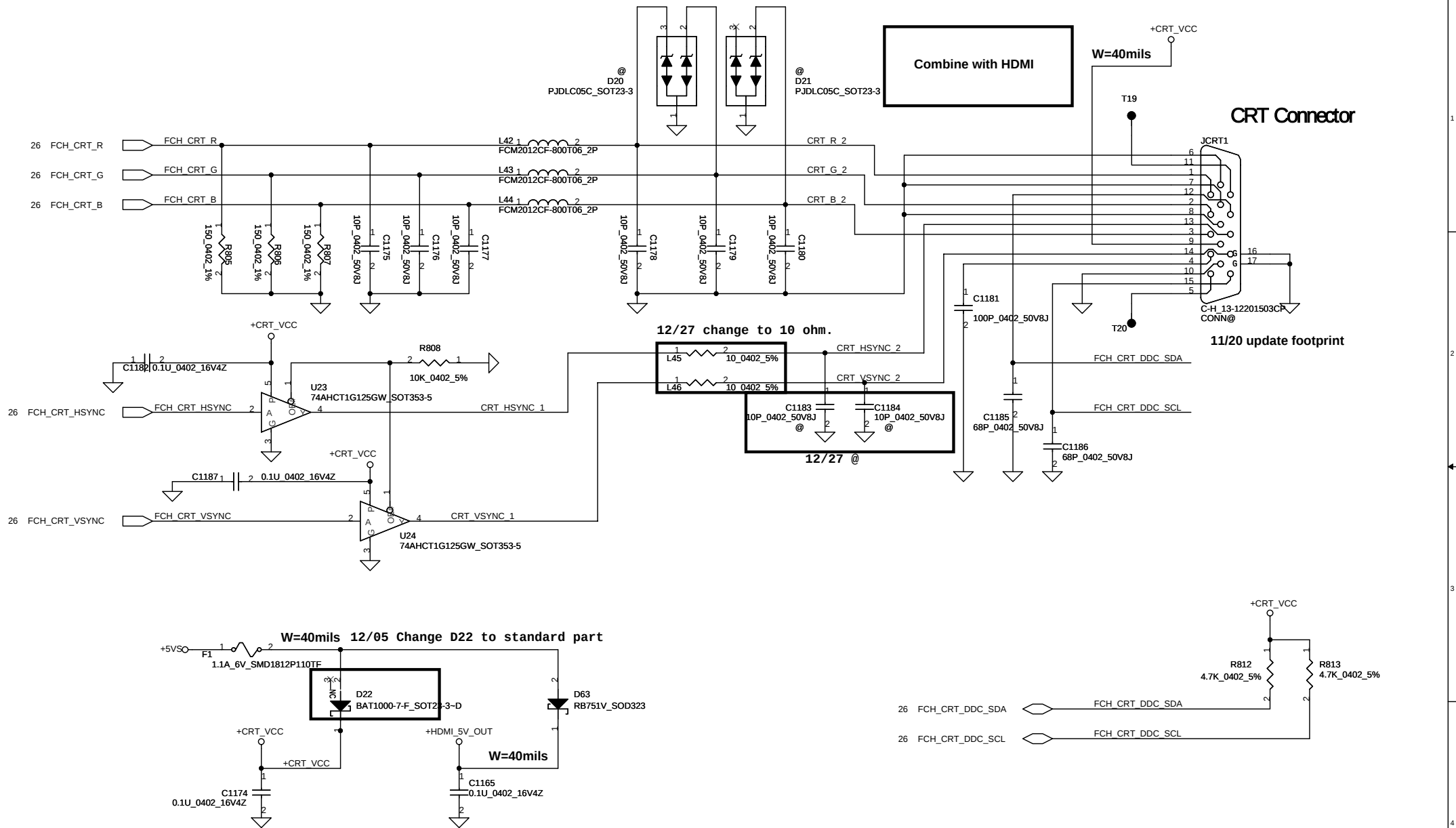
12/7 Swap signals for routing smoothly



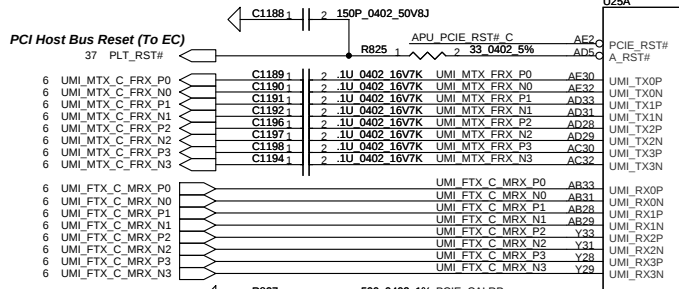
Close to HDMI conn



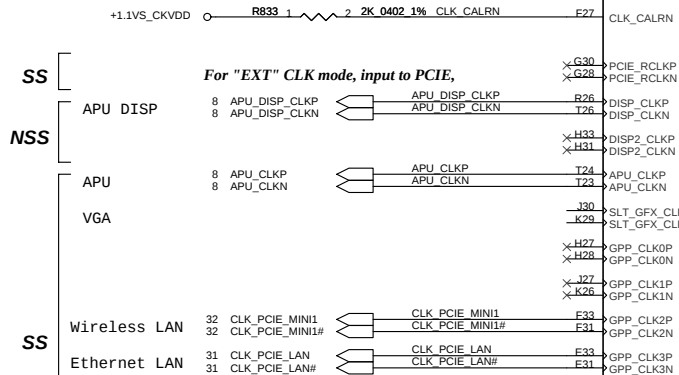
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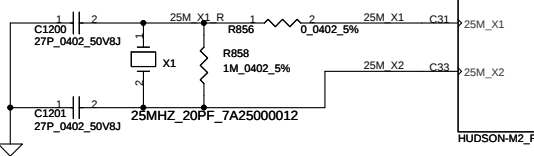
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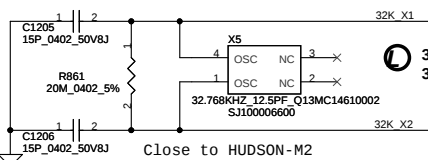
PCI_CALRP R=50ohm, 4mil, <1000mil
PCI_CALRN R=50ohm, 4mil, <1000mil



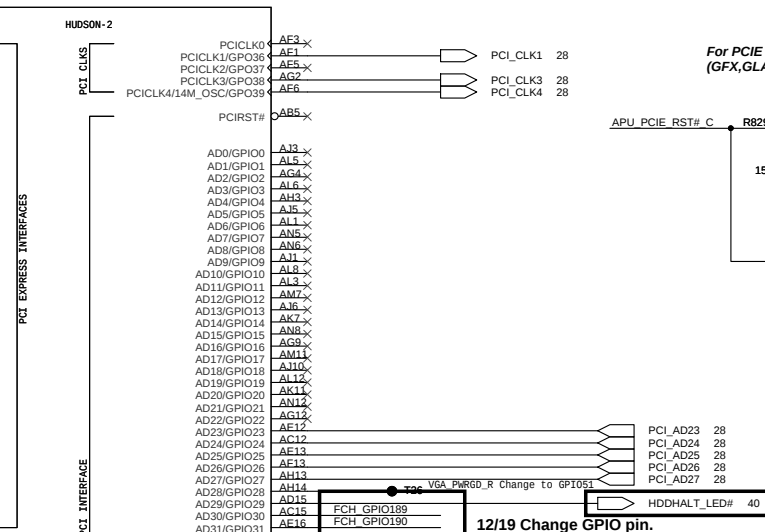
25M_X1 and 25M_X1 R=50ohm, 4mil
25M_X2=50ohm, 4mil



C1205, C1206
Change for G3
RTC timing issue
<improve amplitude>



32K_X1=50ohm, 4mil, <1500mil
32K_X2=50ohm, 4mil, <1500mil

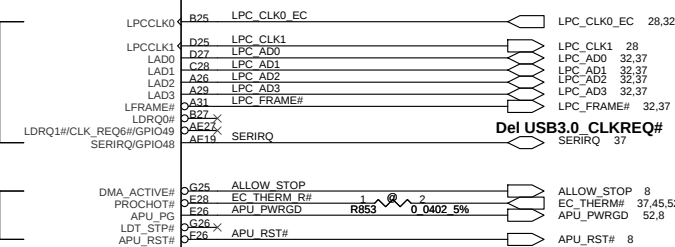


12/19 Change GPIO pin.

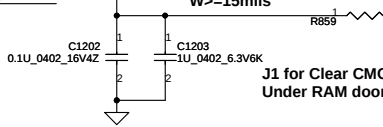
Del USB3.0_CLKREQ# PH.

12/19 add PH to +3VS.

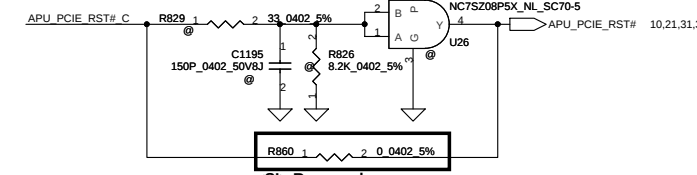
12/01 change to INTH for BIOS request



RTC_CLK R=50ohm, 4mil
RTC_CLK=50ohm, 4mil

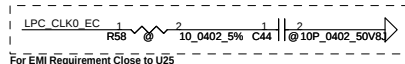


For PCIe device reset on FS1
(GFX, GLAN, WLAN, LVDS Travis)

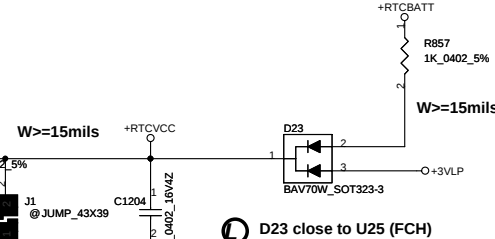
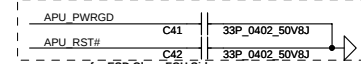


Project SKU ID	L(N)	H(Y)
GPIO189 (use VGA)	R44	R43
GPIO190 (use PX)	R46	R45

DIS is High
DIS is High

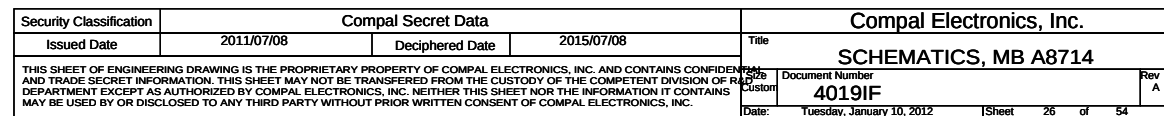


APU PG/APU_RST#/LDT_STP# : OD pin
DMA_ACTIVE# : INOD, 0.8V threshold
PROCHOT# : IN, 0.8V threshold
LDT_STP# : No use, NC
DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.



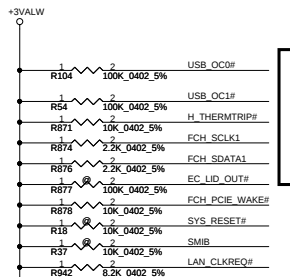
D23 close to U25 (FCH)

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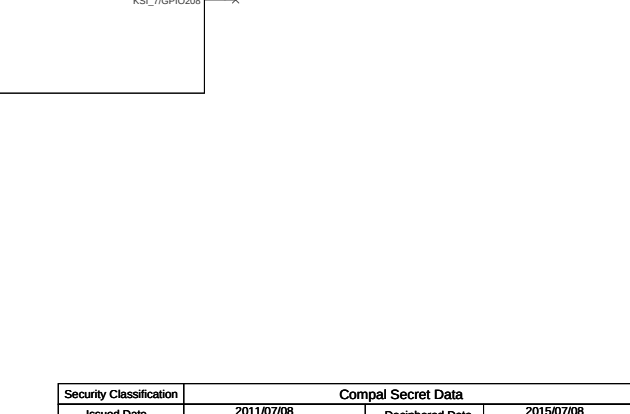


THERMTRIP:
Need level shift from +3VALW to +1.5V
Note: Ensure FCH internal pull-up resistor
to +3.3V S5 is disabled to prevent leakage
when APU is powered down.

FCH GEVENT (S5 domain)
with isolation circuit to avoid leakage



1	2	TEST0
R887	2.2K_0402_5%	
1	2	TEST1
R889	2.2K_0402_5%	
1	2	TEST2
R890	2.2K_0402_5%	



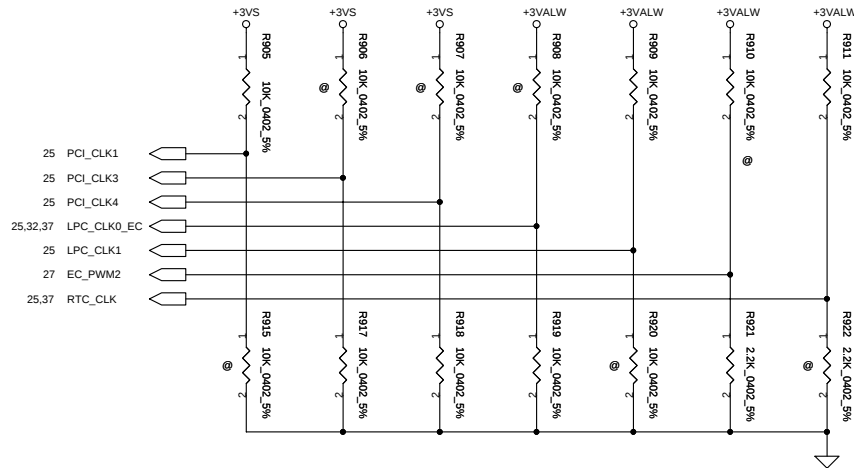
SB 3.0 port(Left.

	Title

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				Date	Revision	By
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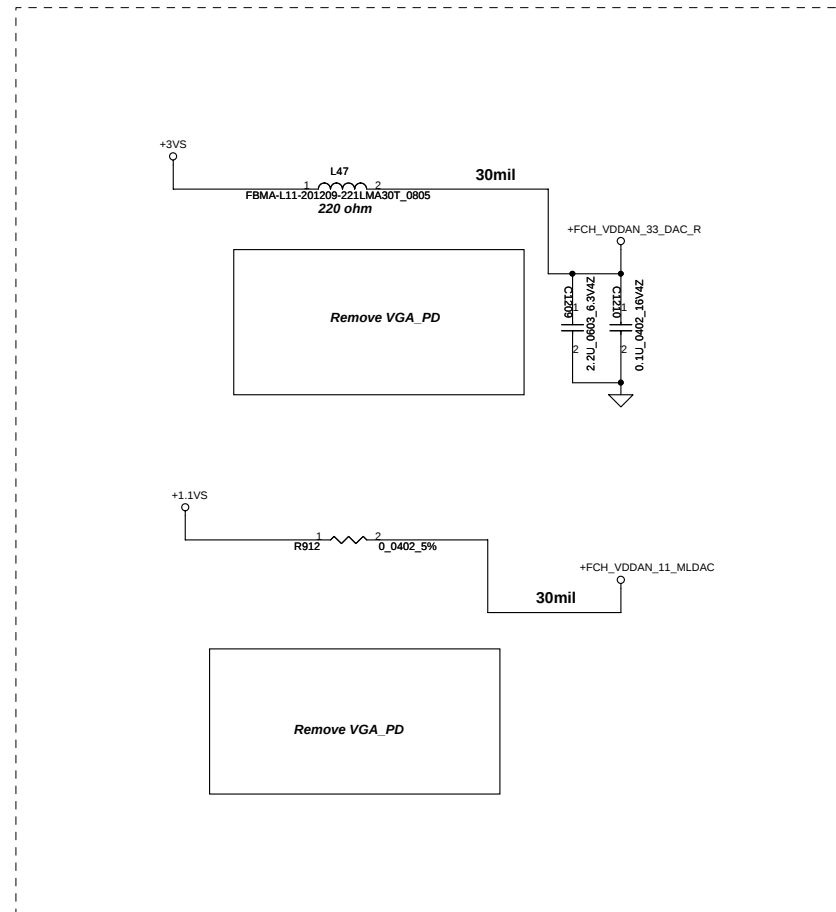
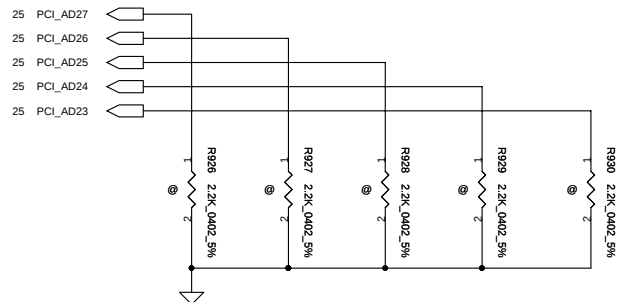
Change to SPI

PULL HIGH	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

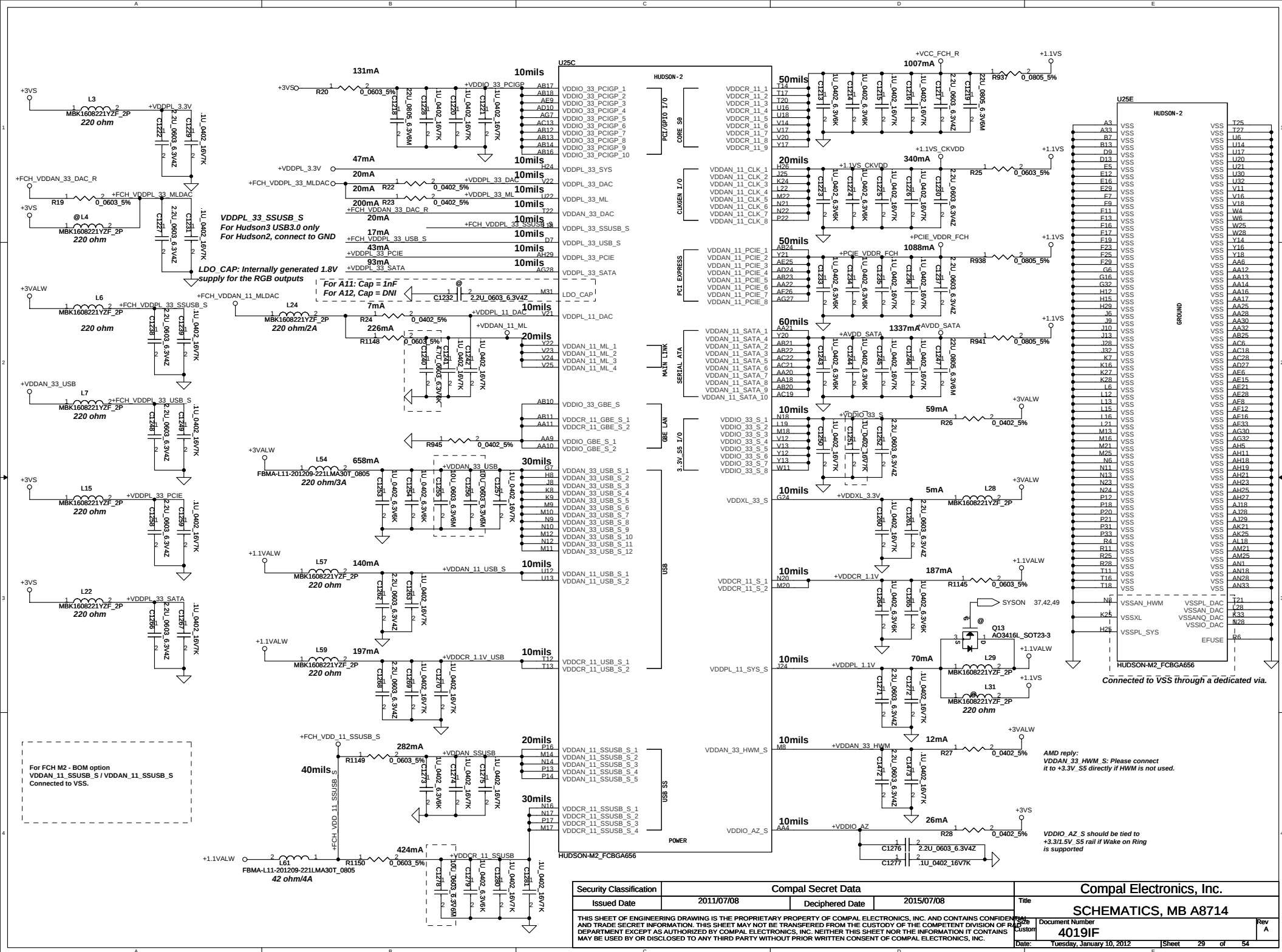


FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23
No external R	USE PCI PLL DEFAULT	Normal REFCLK termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	Inverted REFCLK termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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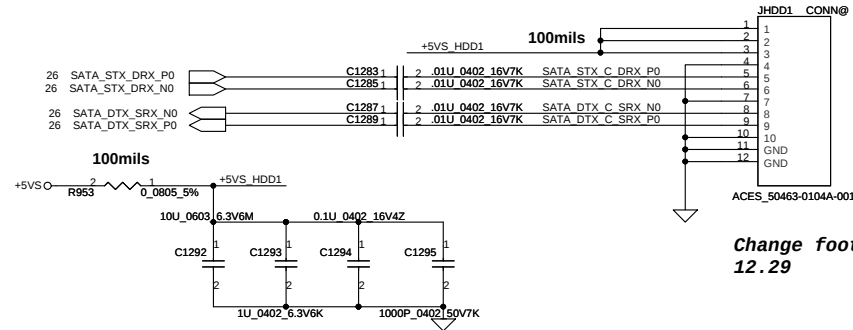


AMD reply:
VDDAN_33_HWM_S: Please connect
it to +3.3V_S5 directly if HWM is not used.

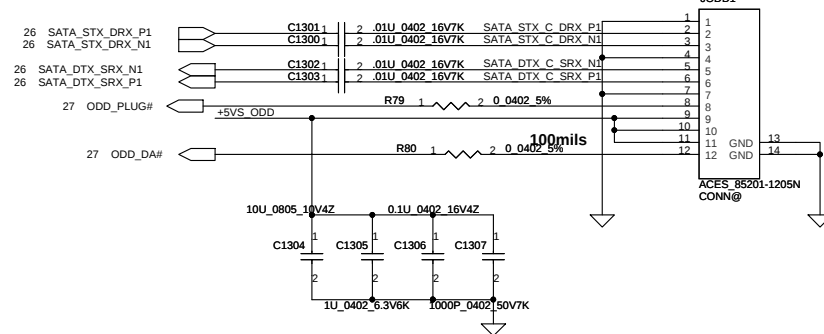
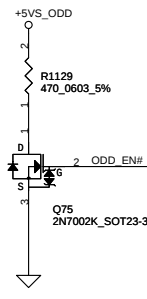
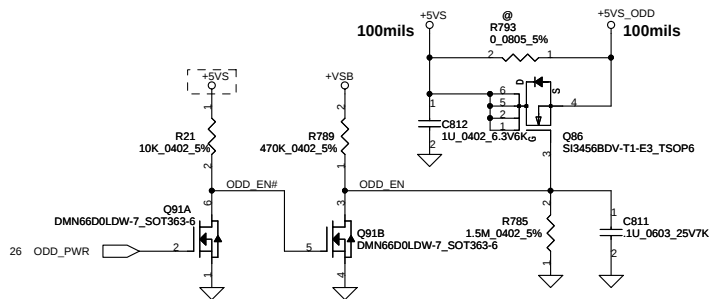
VDDIO_AZ_S should be tied to
+3.3V_S5 rail if Wake on Ring
is supported

Connected to VSS through a dedicated via.

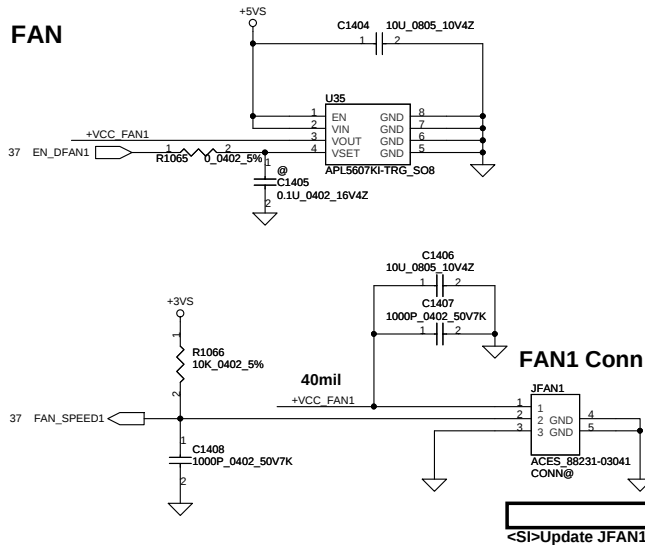
SATA HDD1 Conn.



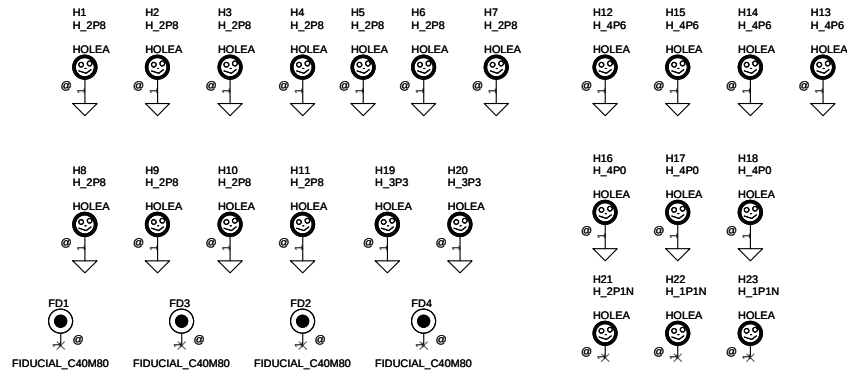
Change footprint to Starconn (PAD is bigger)
12.29



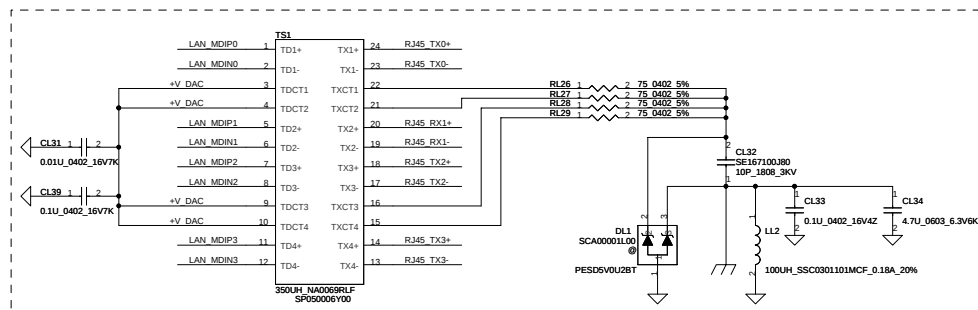
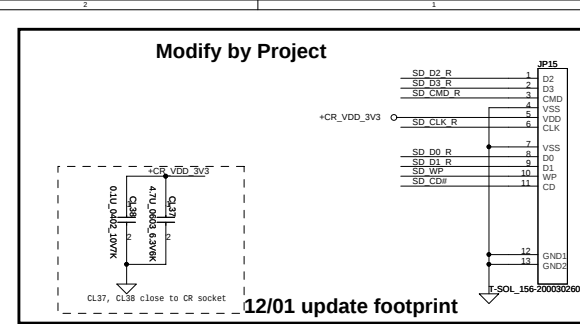
FAN



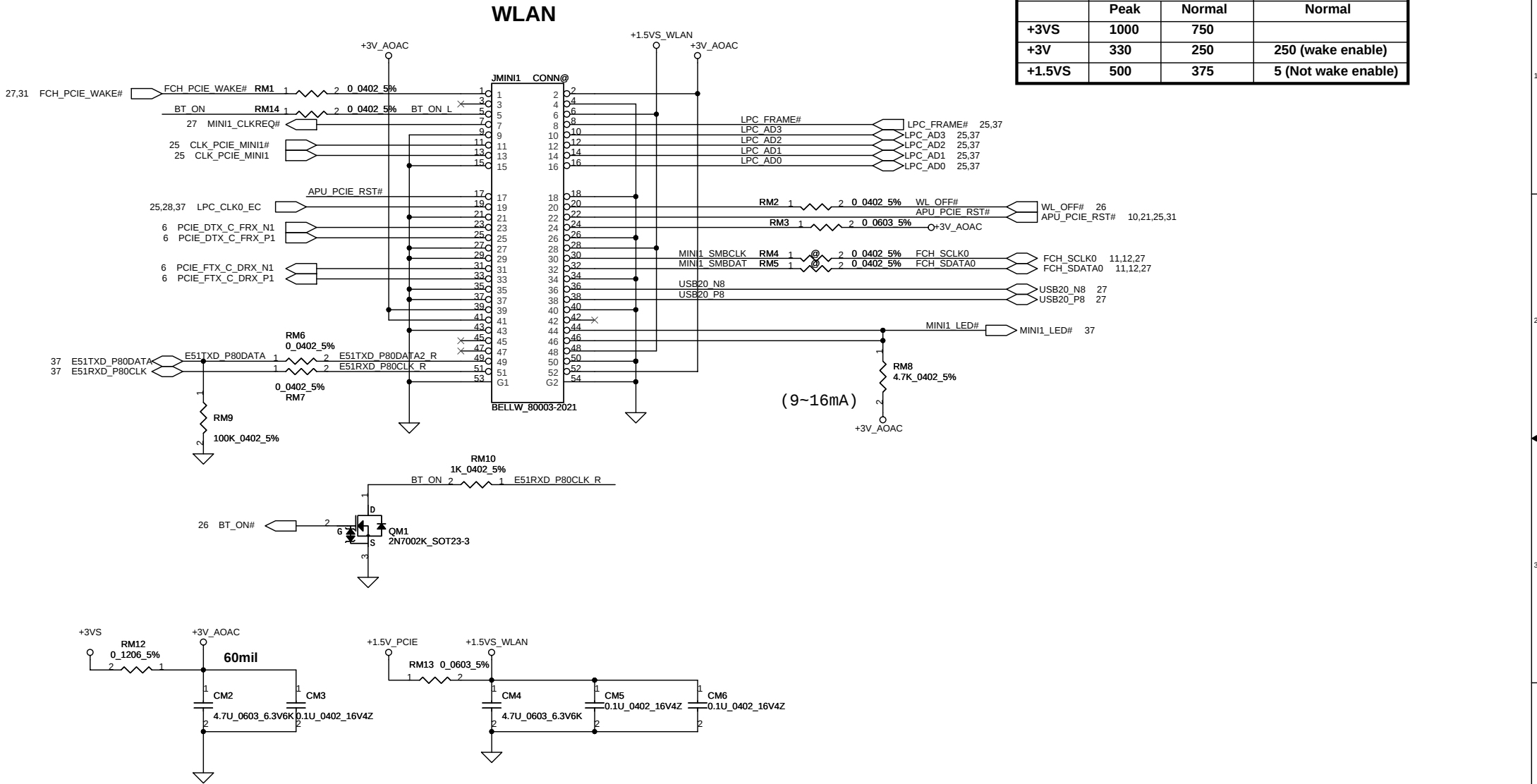
Screw Hole



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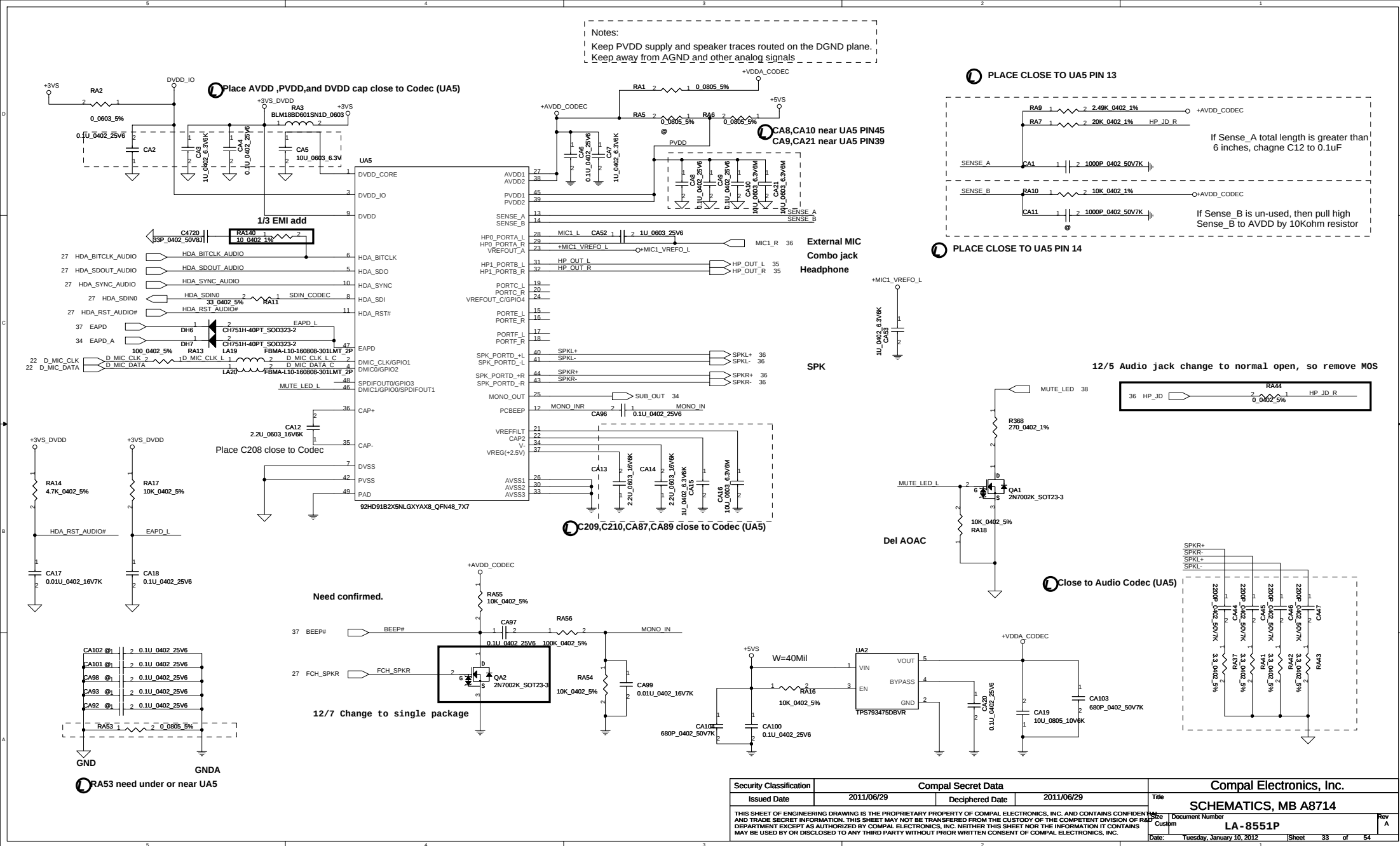


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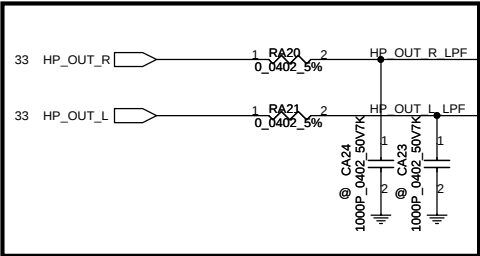
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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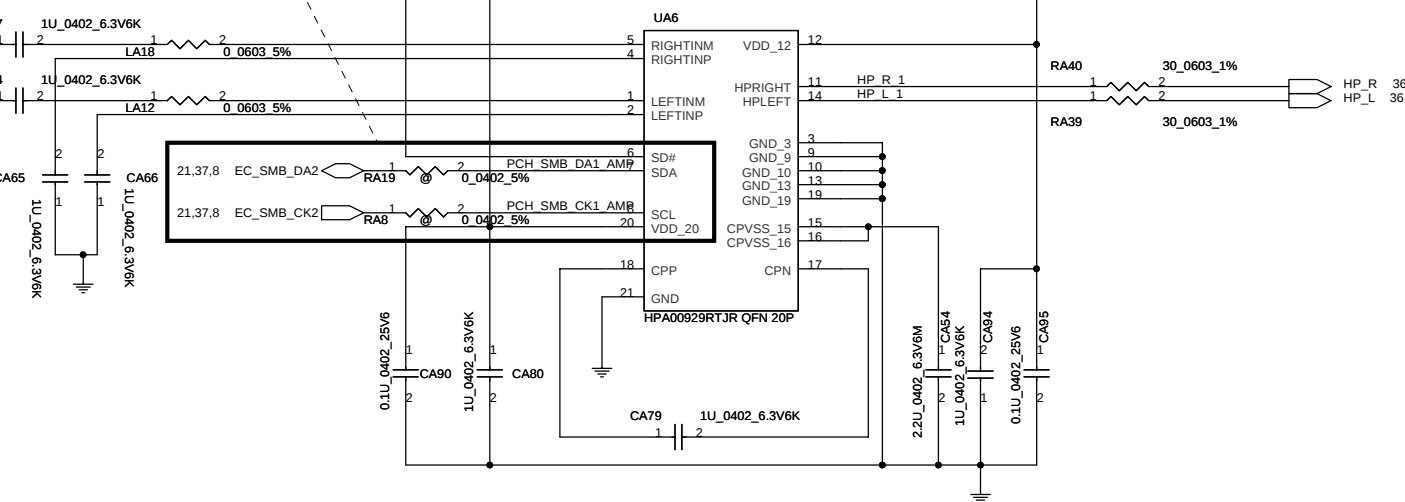
Headphone amplifier

12/05 Add LPF for HP requirement

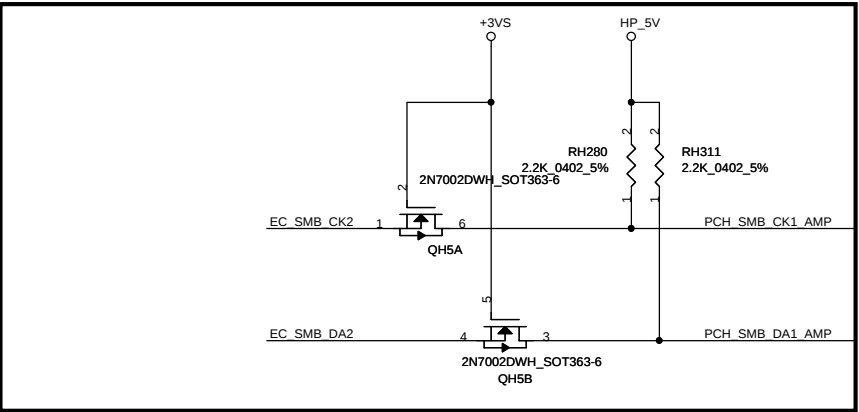


<SI> BOM update :RA20,RA21 4.7K-->0
CA24,CA23 SMT-->@

12/05 Connect HP AMP SMBus to EC

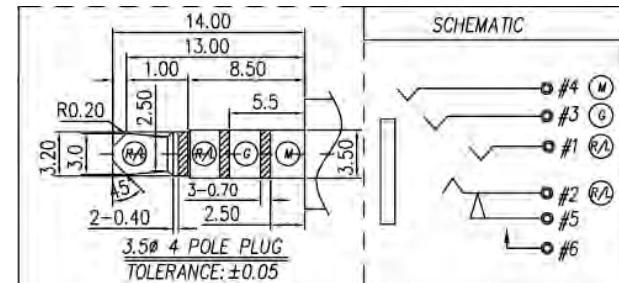
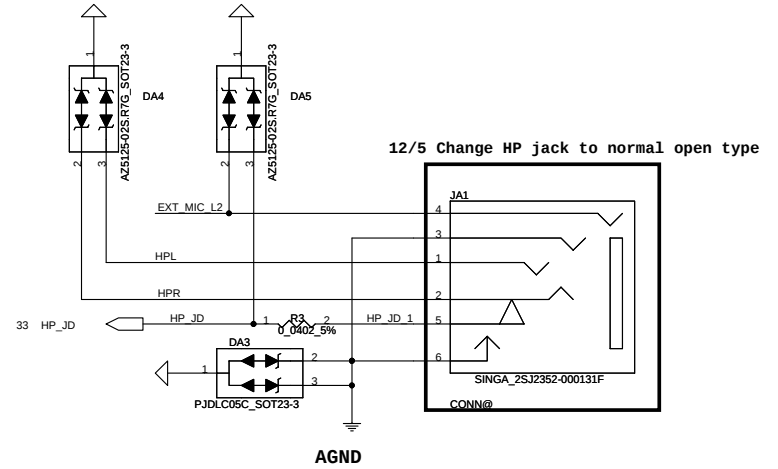
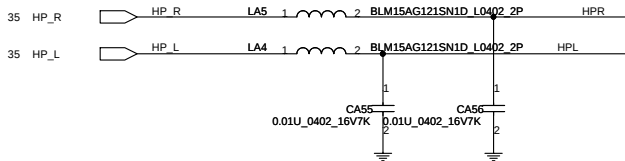
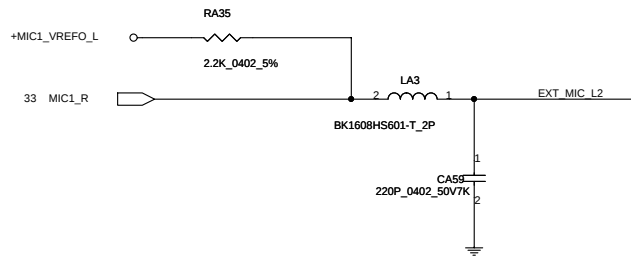
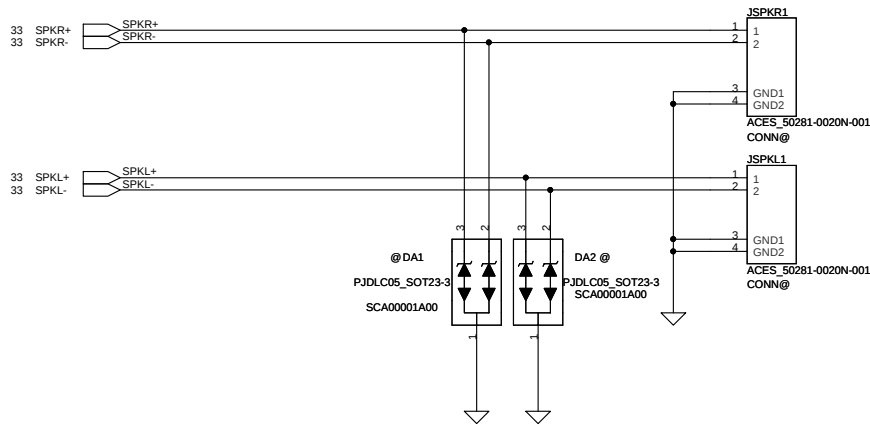


12/05 Reserve level shift Connect to EC

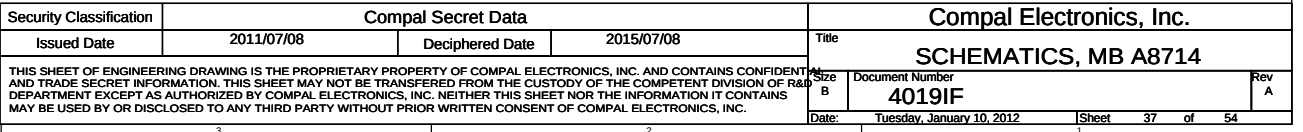


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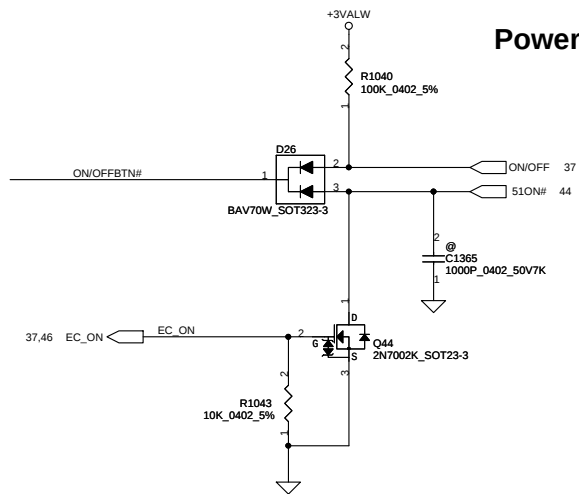
SPK conn



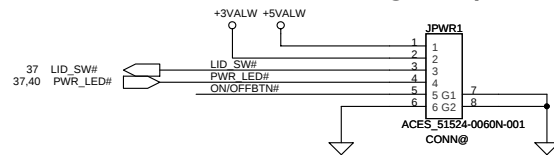
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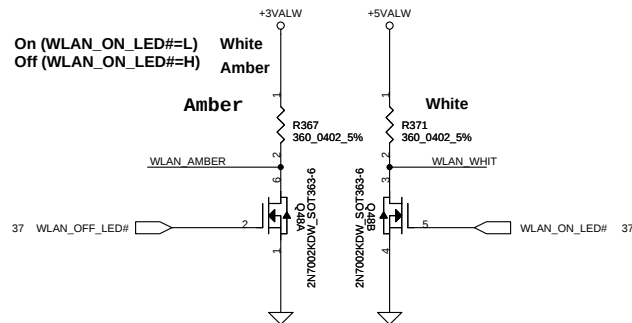
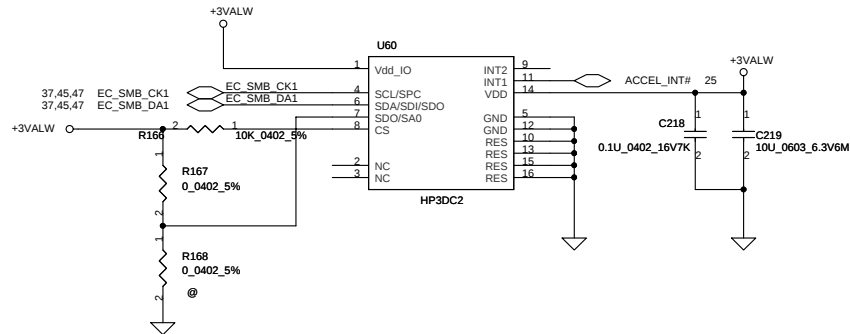
Power Button



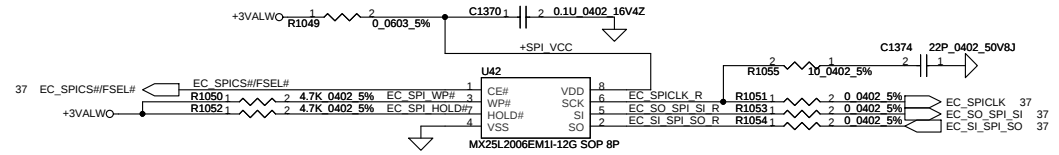
POWER/B



ACCELEROMETER

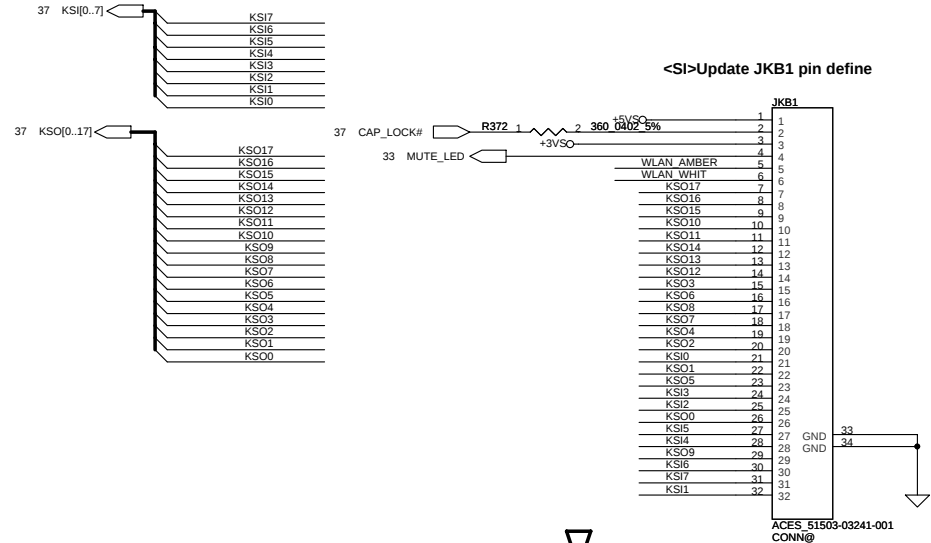


EC BIOS ROM

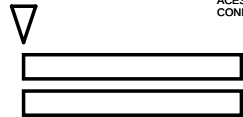


KB conn

<SI>Update JKB1 pin define

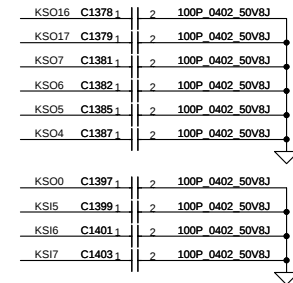
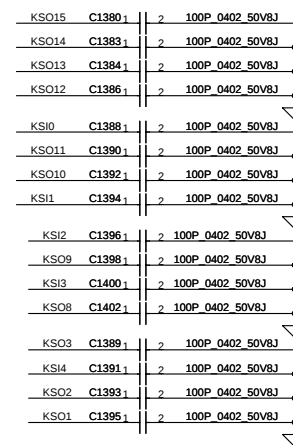


Membrane
Down contact



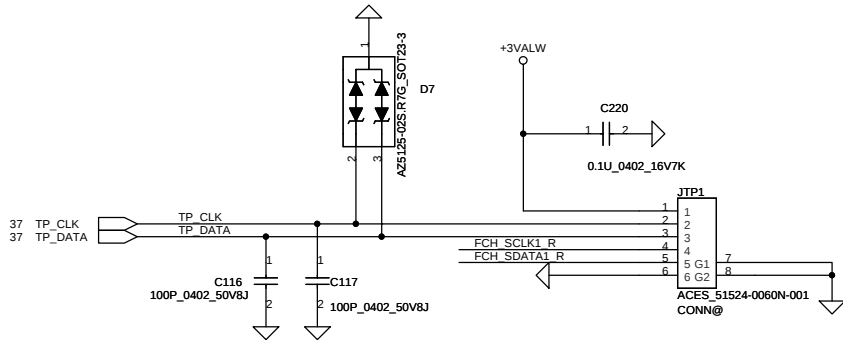
Conn footprint
Down contact

The KB pin define must opposite



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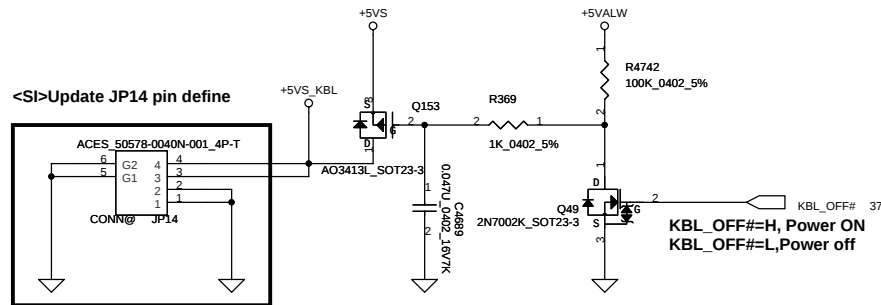
TP Conn



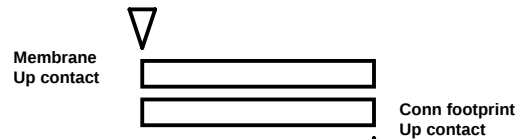
27 FCH_SCLK1 R190 @ 2 0.0402 5% FCH_SCLK1_R
27 FCH_SDAT1A1 R210 @ 2 0.0402 5% FCH_SDAT1A1_R

For multi-touch function

Keyboard backlight Conn



12/06 Change keyboard back light conn



The JP14 pin define must opposite

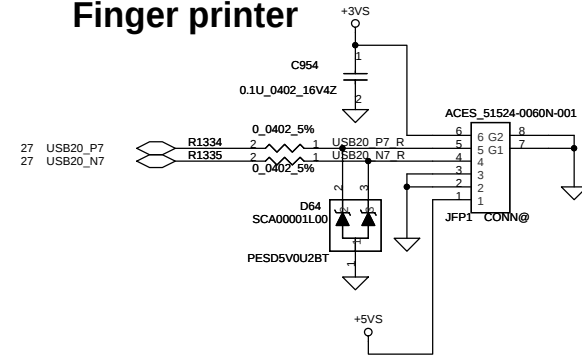
T/P On/Off LED



EC pin

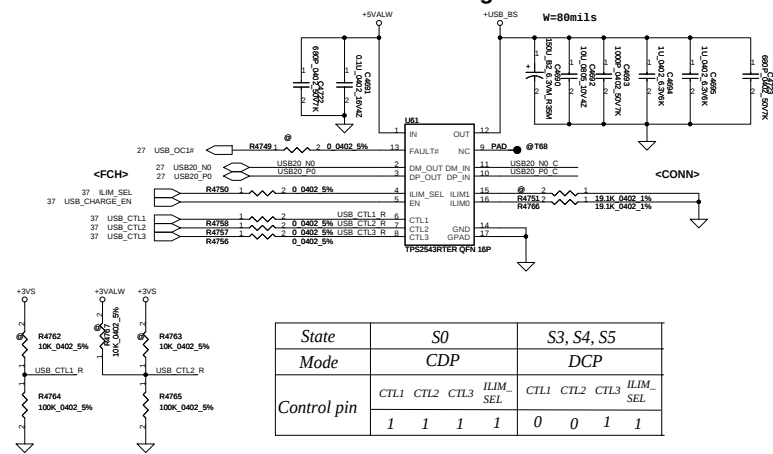
Finger printer

12/06 Change FPR pin define



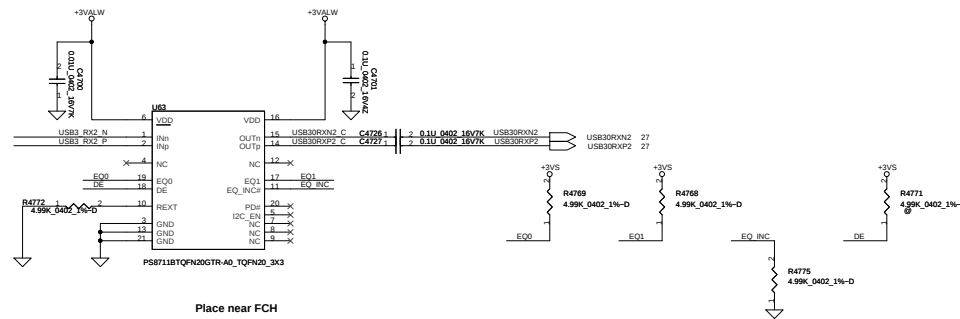
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USB Charger

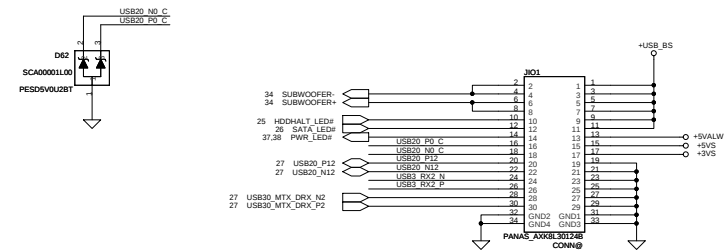


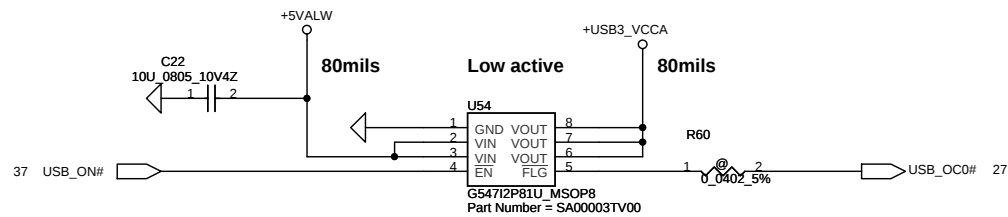
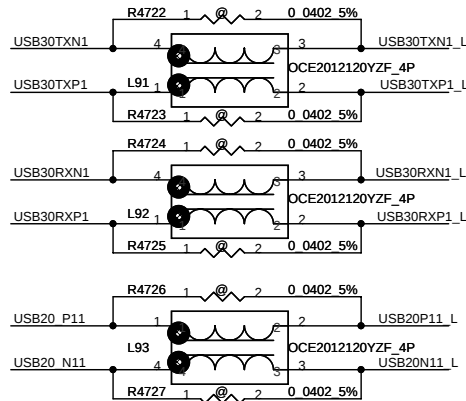
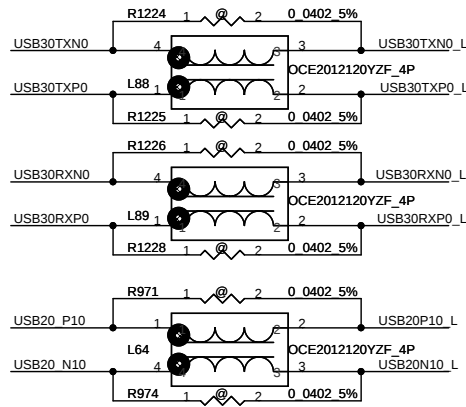
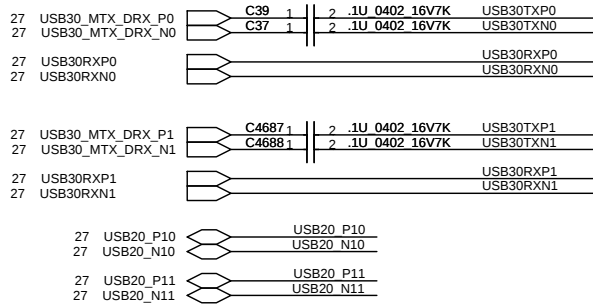
<i>State</i>	<i>S0</i>				<i>S3, S4, S5</i>			
<i>Mode</i>	<i>CDP</i>				<i>DCP</i>			
<i>Control pin</i>	<i>CTL1</i>	<i>CTL2</i>	<i>CTL3</i>	<i>ILIM-SEL</i>	<i>CTL1</i>	<i>CTL2</i>	<i>CTL3</i>	<i>ILIM-SEL</i>
	1	1	1	1	0	0	1	1

USB3.0 Repeater

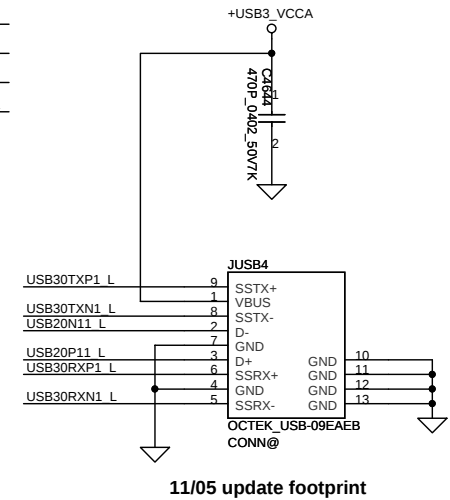
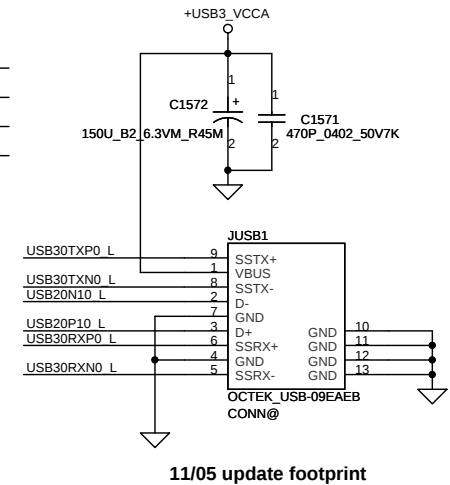
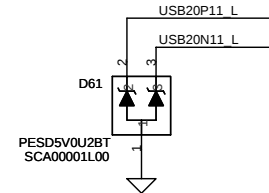
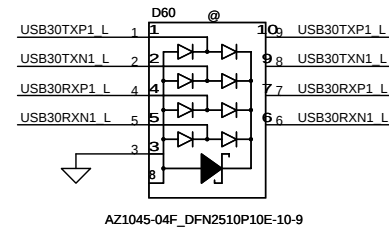
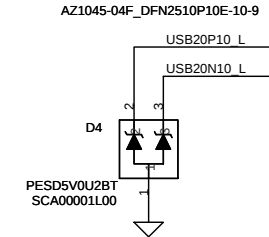
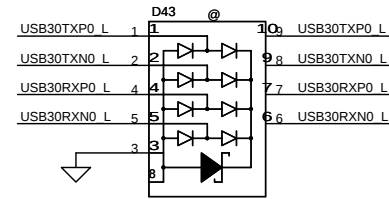


Place near FCH



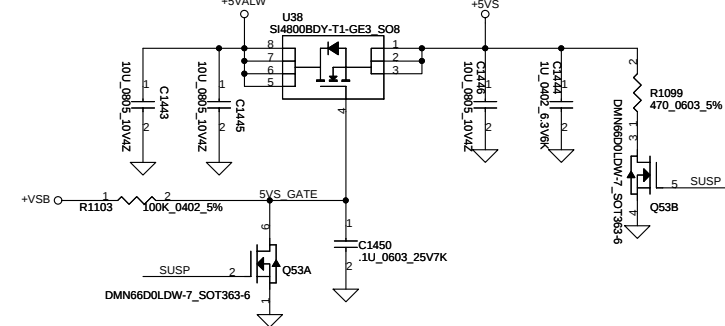


For ESD request

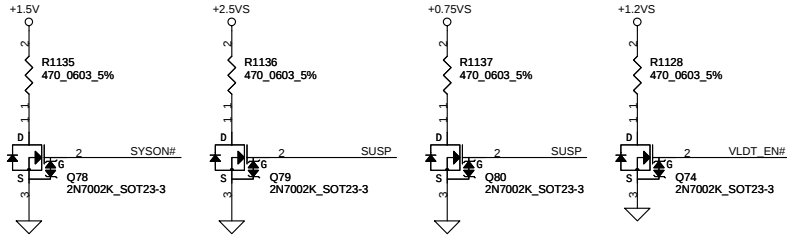
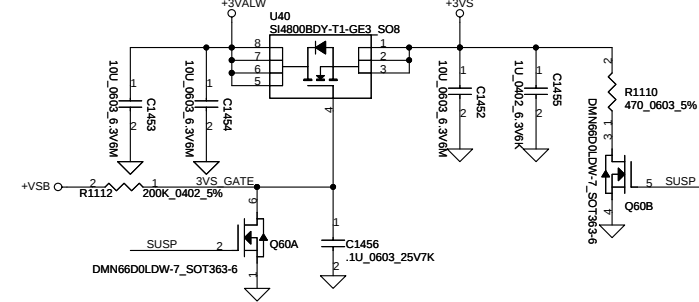


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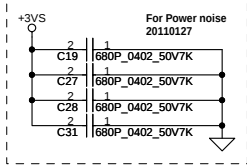
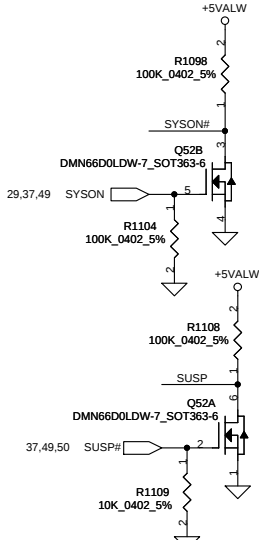
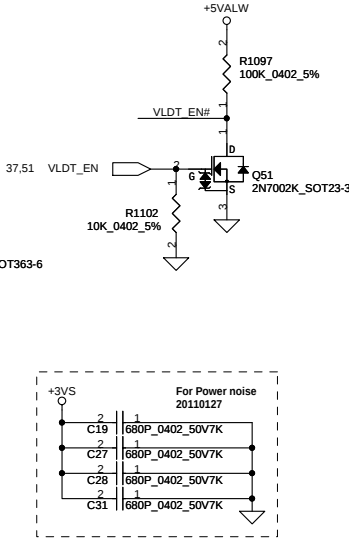
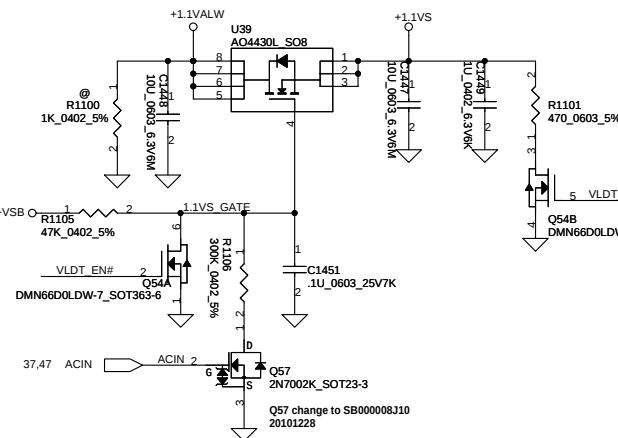
+5VALW TO +5VS (5A)



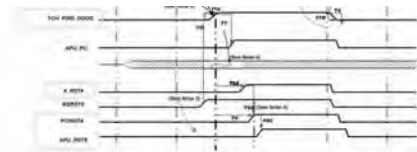
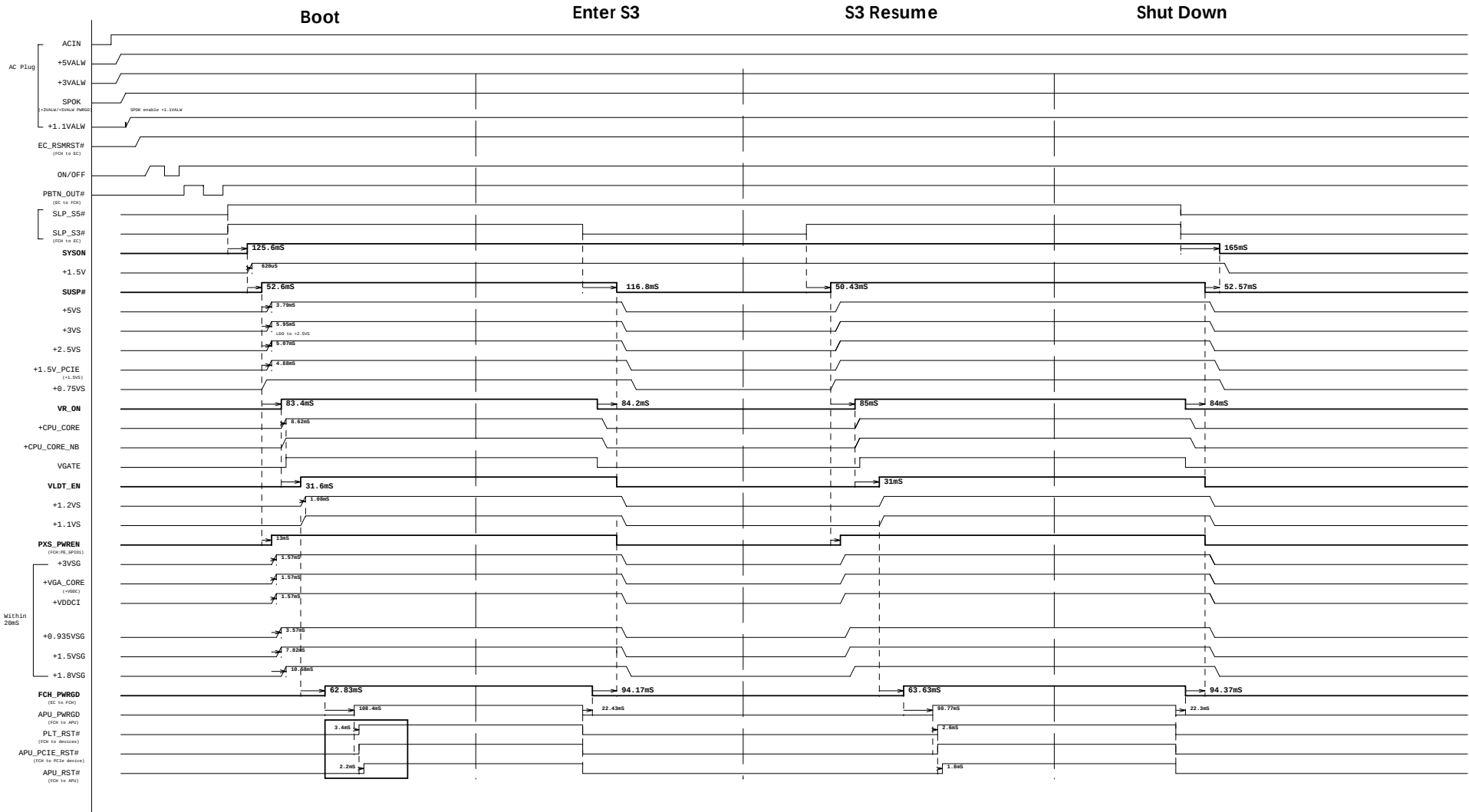
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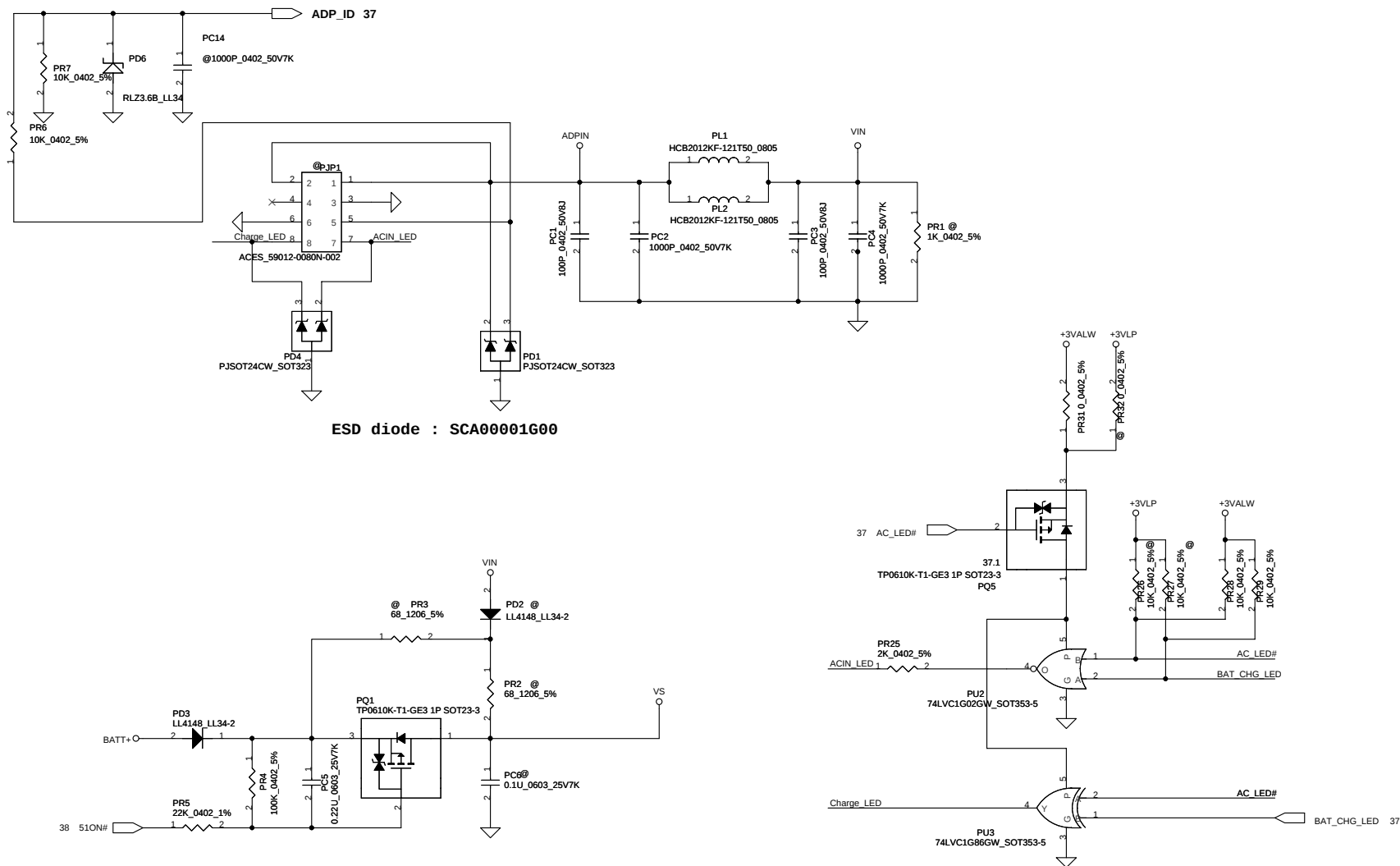
+1.1VALW TO +1.1VS (1.1A)



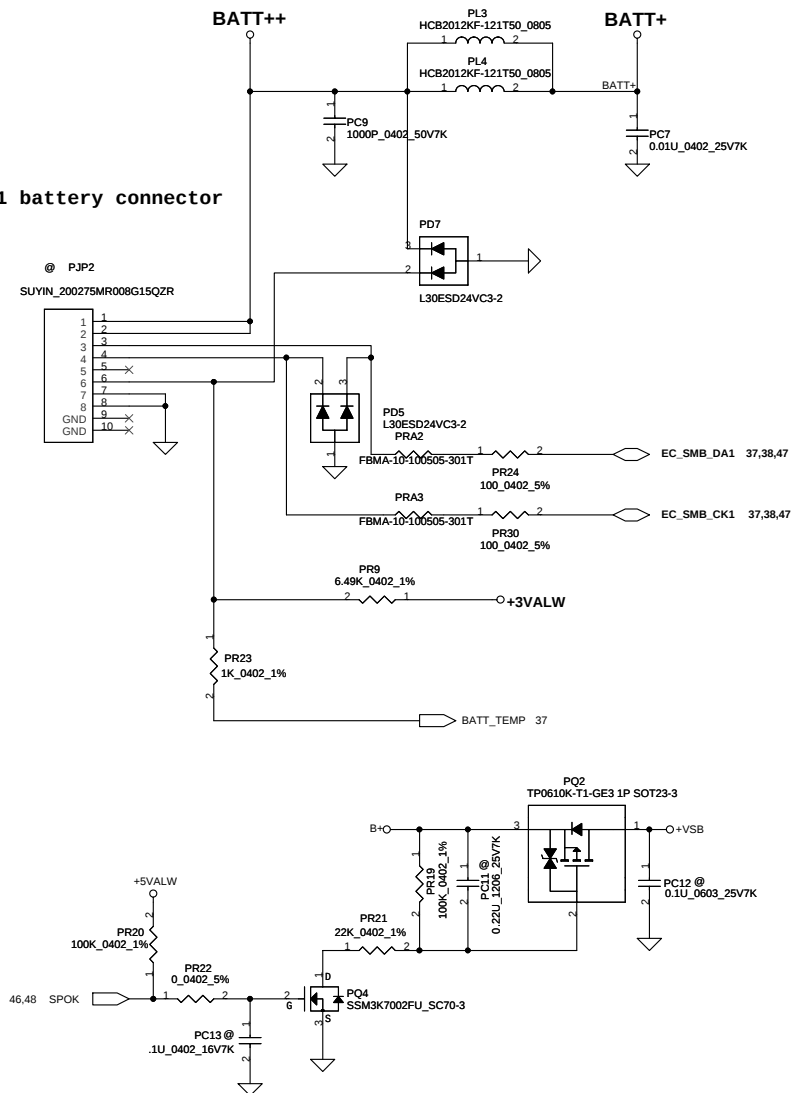
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Doc	4019IF	Rev	1	Rev	1
Rev	1	Rev	1	Rev	1



PJPB1 battery connector



For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

PH1 under CPU bottom side :
CPU thermal protection at 90 +/- 3 degree C
Recovery at 56 +/- 3 degree C

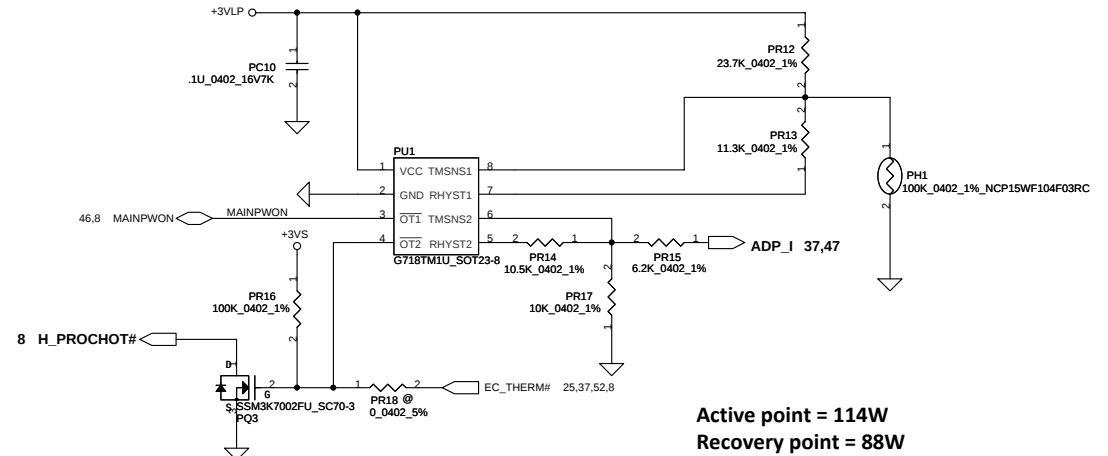
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

$$R_{tmh} \text{ at } 90C = 7.8K, R_{tml} \text{ at } 56C = 26.1K$$

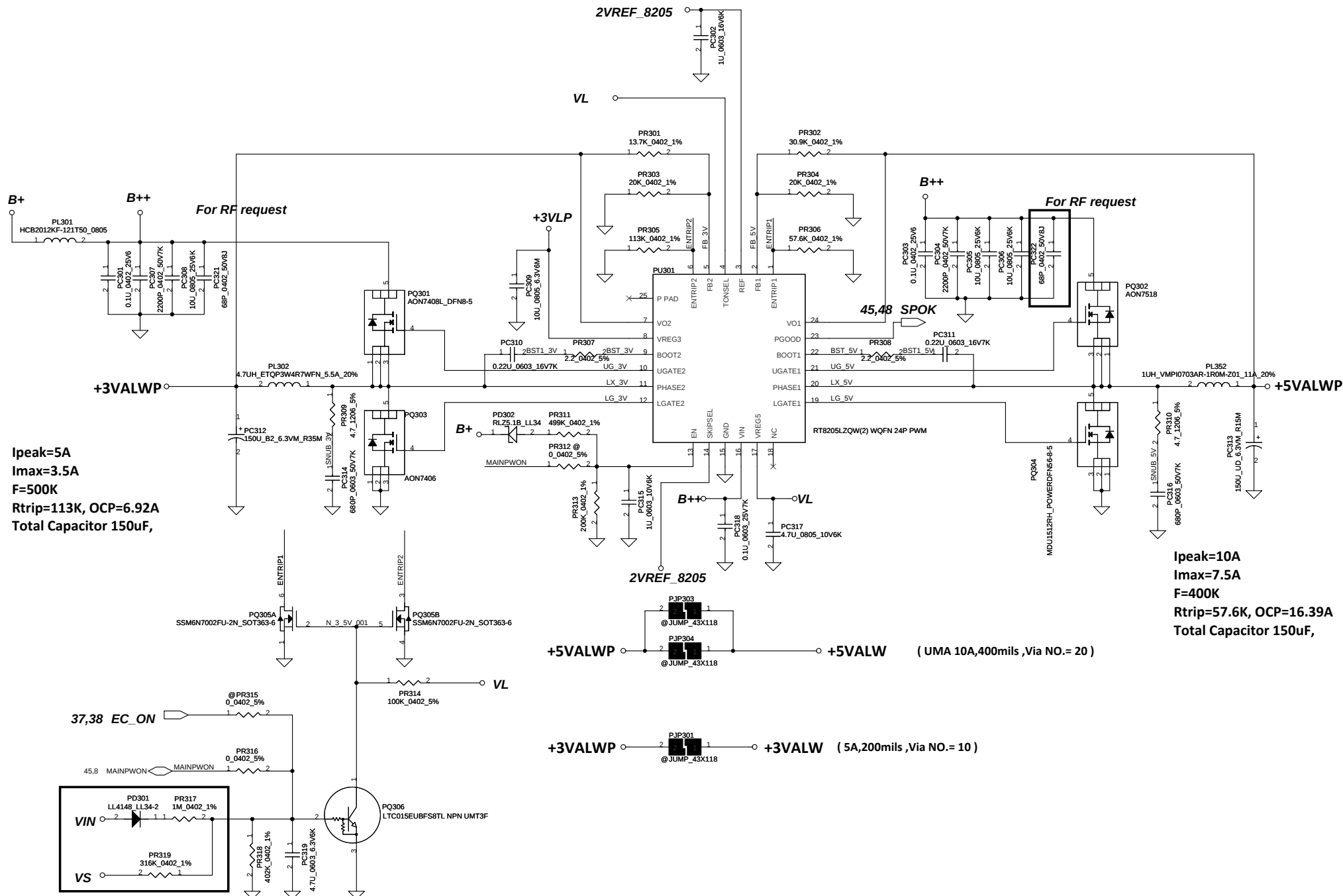
$$R_{set} = 3 * 7.8K = 23.4K \Rightarrow 23.7K$$

$$R_{hyst} = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K \Rightarrow 11.3K$$



Active point = 114W
Recovery point = 88W

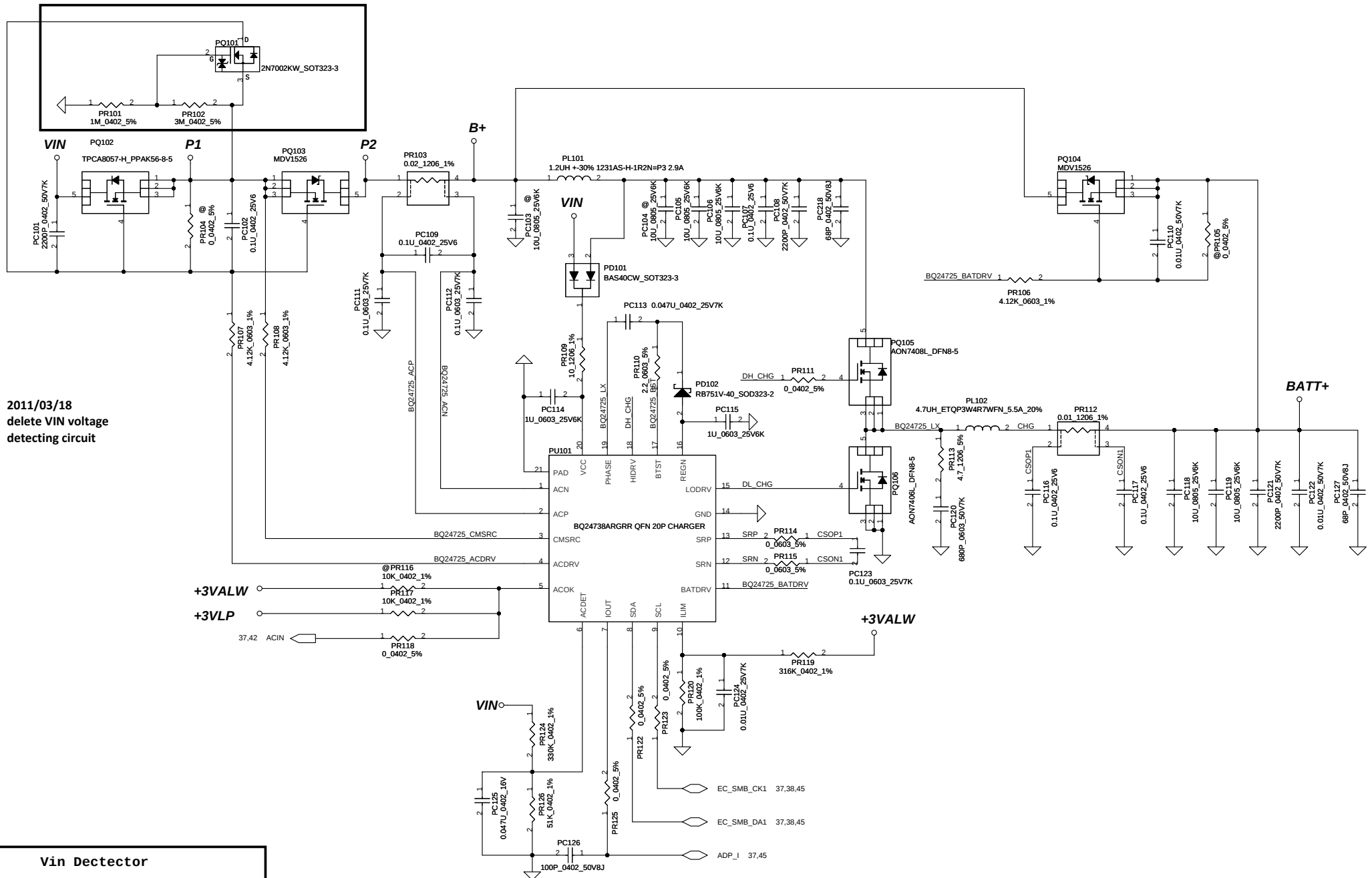
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For KB930 --> Keep PD301, PR317, PR319

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for reverse input protection



2011/03/18
delete VIN voltage
detecting circuit

Vin Dectector

	Min.	Typ	Max.
H-->L		17.33V	
L-->H		16.98V	

ILIM and external DPM
4.36A

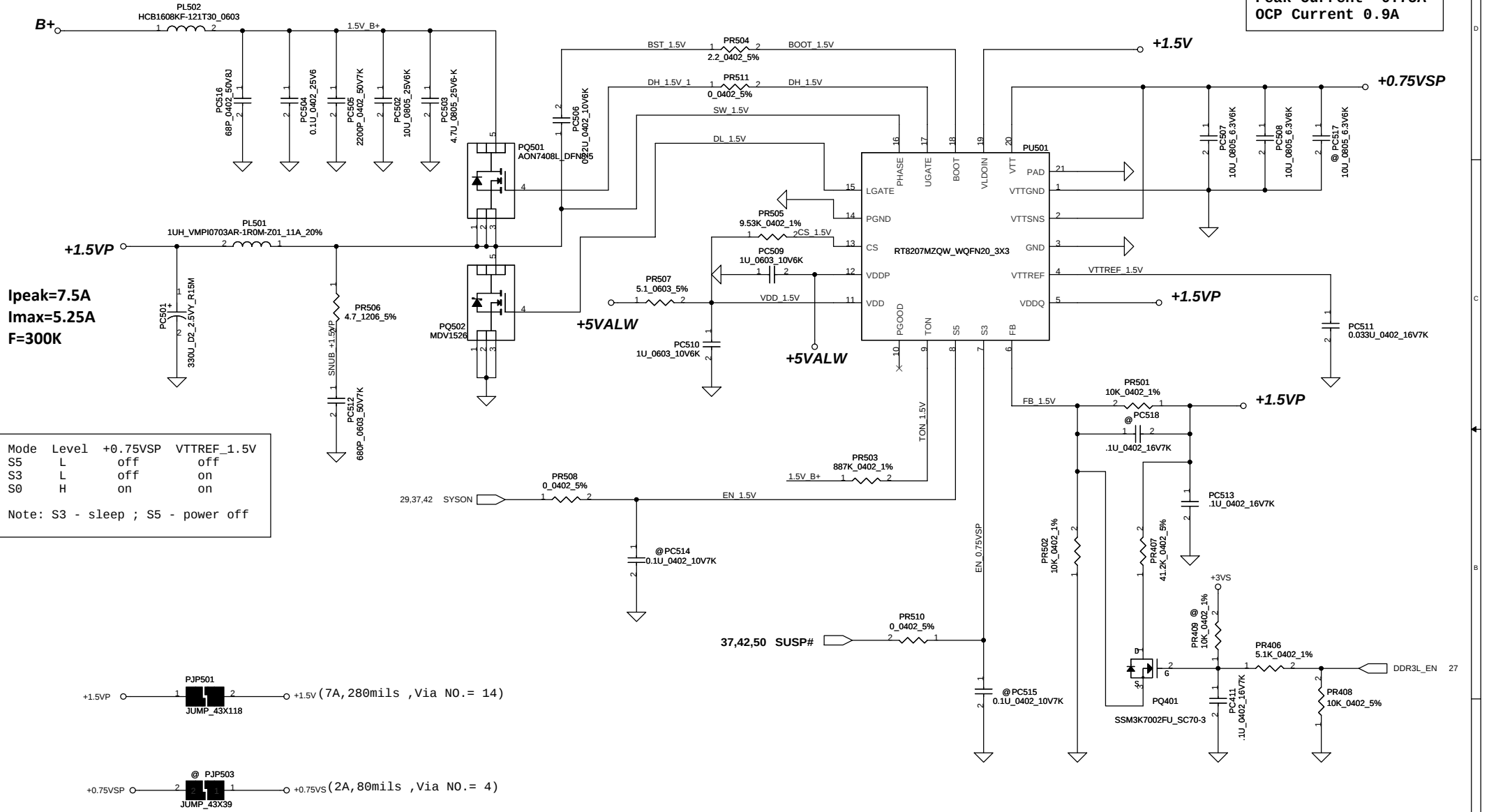
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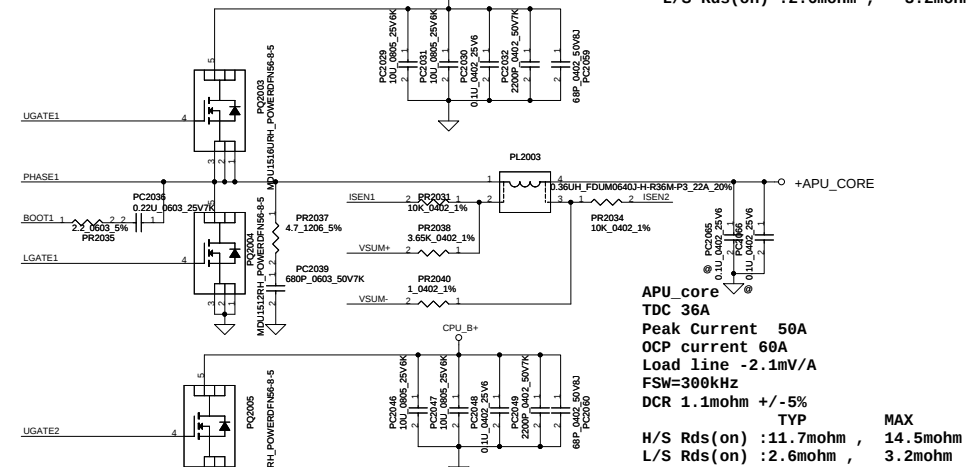
I_{peak}=7.5A
I_{max}=5.25A
F=300K

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

0.75V_{olt} +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A

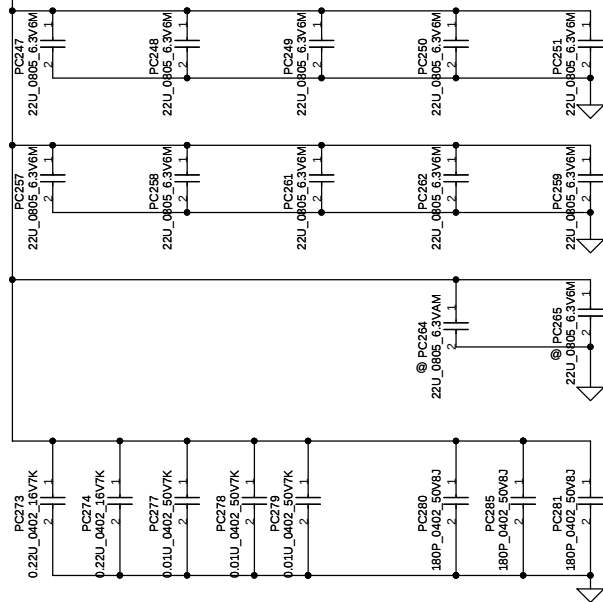




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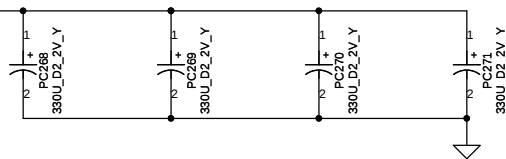
+APU_CORE

+APU_CORE



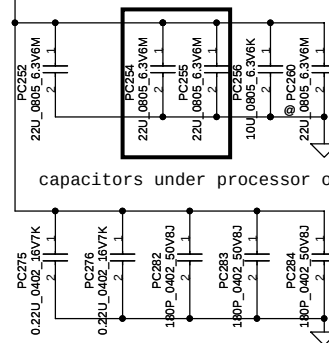
+APU_CORE

Local



+APU_CORE_NB

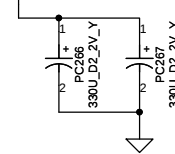
+APU_CORE_NB



capacitors under processor on bottom side of board

+APU_CORE_NB

Local



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NO	DATE	PAGE	MODIFICATION LIST		PURPOSE
DB-2(12/2)		P44-PWR-DCIN / Vin Detector	Change to PJP1 pine define		DC-IN jack buy and sale define does not change
DB-2(12/8)		P45-PWR-BATTERY CONN	Pin 7 power source change +3VLP to +3VALW		EC command
DB-2(12/8)		P52-PWR-+1.5VPCIE/0.935V	PC11506 loaction change to PC1156		CIC SMT command
DB-2(12/12)		P52-PWR-+1.5VPCIE/1V	Change PR9352 11.3K to 13.3K (0.935V to 1V)		HW comand
DB-2(12/13)		P50-PWR-1.1VALWP	Add PR803 =10K		SY8809 enbale pin issue

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2005/06/01		2006/06/01		SCHEMATICS, MB A8714	
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