CZC Digital technologies Co.,LTD

Board name: Mother Board Schematic

Project name: **CPL S01 (R48)**

Version: VerC

Start Date:JAN 6,2010

VerA Release Data:

1. System Block Diagram & Schematic page description;
2. Power Block Diagram & Discription;
3. Annotations & information;
4. Schematic modify Item and history;
5. Power on & off Sequence;
6. ACPI Mode Switch Timings;
7. Power On Sequence Map;
8. CLOCK Distribution;

Hardware drawing by: _____

Hardware check by: _____

EMI Check by: _____

Power drawing by: _____

Power check by: _____

Manager Sign by: _____

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Title <Title>			
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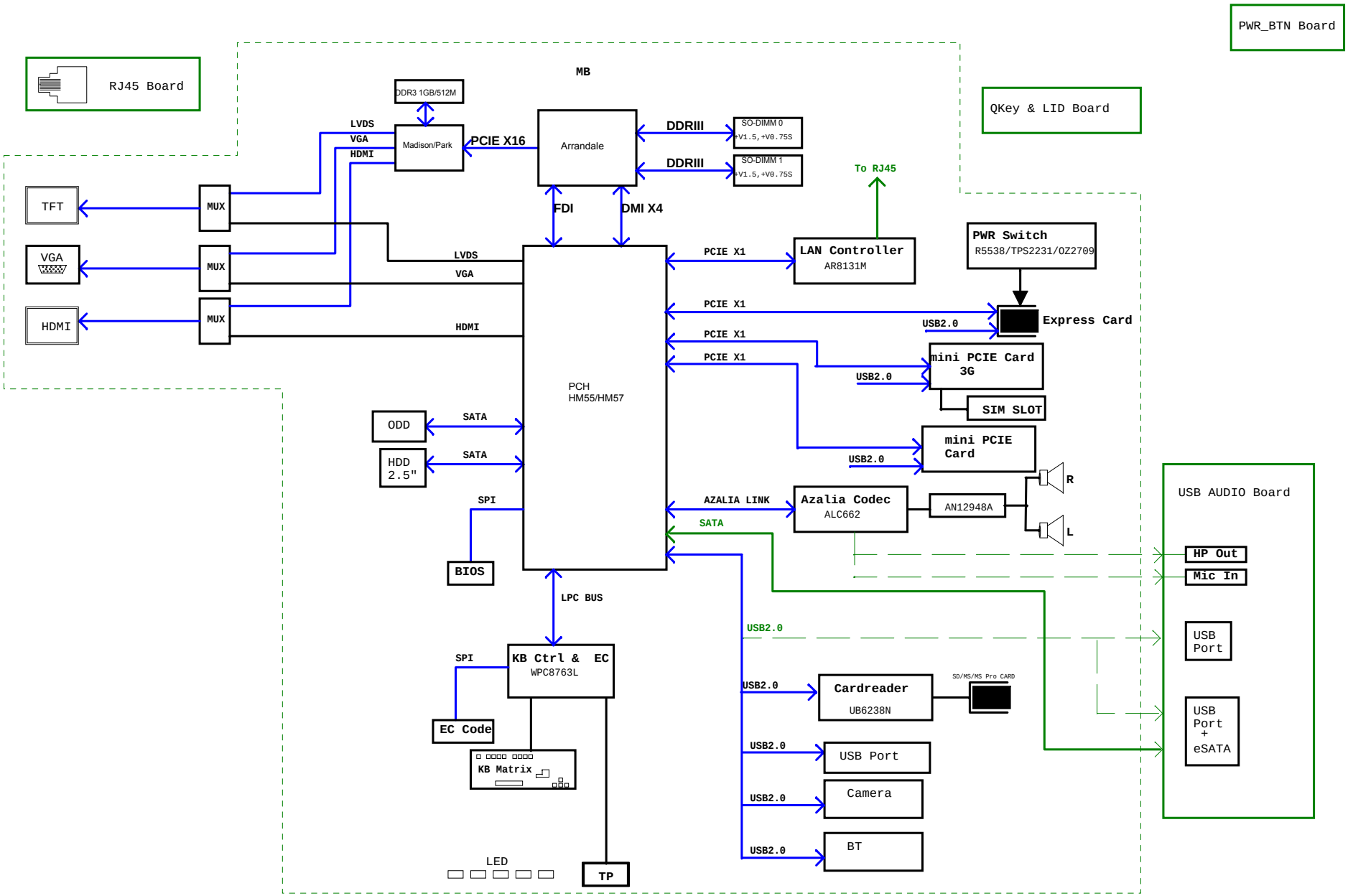
S45 System Block Ver:A



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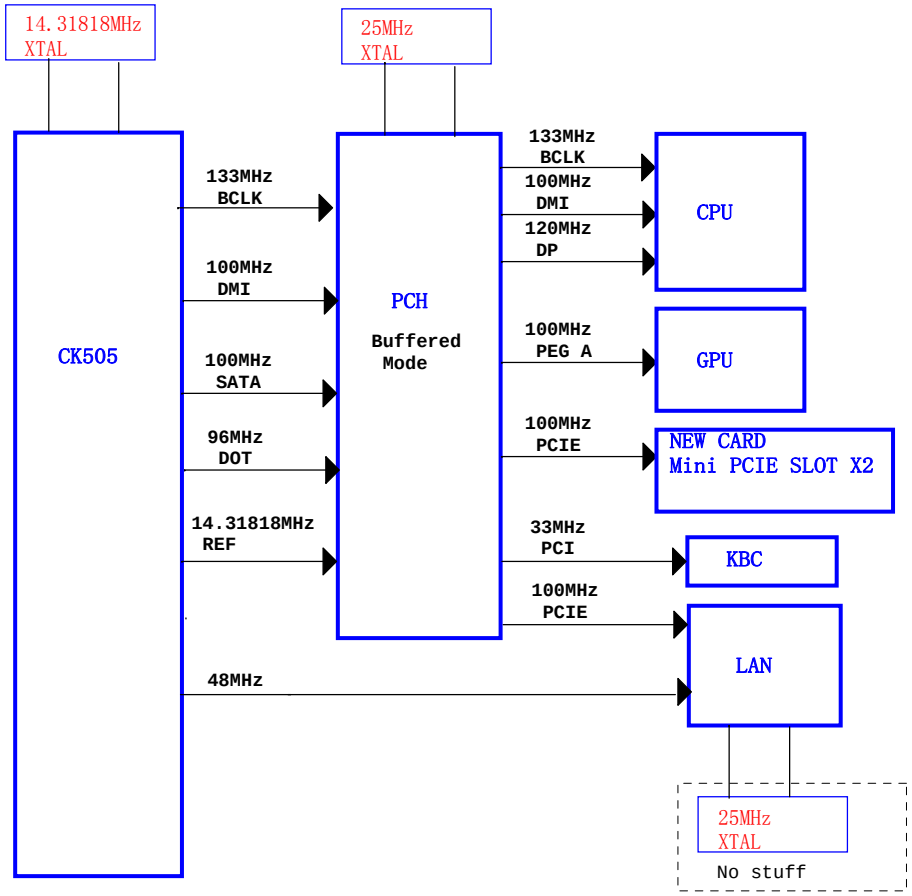
POWER RAIL	AC Mode					Battery Mode				
	S0	S1	S3	S4	S5	S0	S1	S3	S4	S5
+V3.3AUX	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF
+V5AUX	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF
+V1.5	ON	ON	ON	OFF	OFF	ON	ON	ON	OFF	OFF
+V0.75S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+V5S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+V3.3S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+V1.5S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+V1.8S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+V1.5S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+V1.1S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+Vcore	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
GFXCORE	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF



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Voltage Rails

+Vcore:0.75V-1.1V

+VDC	Primary DC system power supply(9V-12V)
+VCC_core	Core/VTT voltage for processor
+V1.8S	1.8V For PCH CPU
+V1.1S	1.05V /1.1V For PCH CPU GPU
+V0.75S	0.75V DDRIII Termination voltage
+V1.5S	1.5V for system power
+V1.5	1.5V power rail for DDRIII
+V3.3AUX	3.3V always on power rail
+V3.3S	3.3V main power rail
+V5AUX	5V always on power rail
+V5S	5V main power rail

I2C SMB Address

Device	Address	Hex(W/R)	Bus	Master
Clock Generator	1101 001x	D2H/D3H	SMB_CLK/DATA	PCH
SO-DIMM0	1010 000x	0xA0		
SO-DIMM1	1010 010x	0xA4		
OZ8805LN	0001 011x	16H/17H	EC_I2C_CLK2/DATA2	EC
Thermal Diode G781	1001 100x	98H/99H	EC_I2C_CLK/DATA	

Board stack up description

PCB Layers	
Top(Signal1)	Trace Impedence:50ohm +/-15%
Ground	
Signal2	
Signal3	
Power	
Signal4	
Ground	
Bottom(Signal5)	

PCB Layer Difference signal Impedence list

USB signal difference impedence 85ohm
LVDS signal difference impedence 85ohm
DDRIII signal difference impedence 85ohm
DDRIII CLK signal difference impedence 68ohm

Power States

state \ signal	PM_SLP_S4#	PM_SLP_S3#	+V*AUX	+V*	+V*S	CLOCKS
Full ON		HIGH	ON	ON	ON	ON
S1M(Power On Suspend)		HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)	HIGH	LOW	ON	ON	OFF	OFF
S4(Suspend to DISK)	LOW	LOW	ON	OFF	OFF	OFF
S5/Soft Off With AC IN	LOW	LOW	ON	OFF	OFF	OFF
G3 With Battery	LOW	LOW	OFF	OFF	OFF	OFF

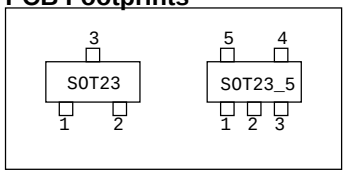
Wake up Events

Wake Events	State Supported(AC)
LID switch from EC	S3 support
Power Button from EC	S3,S4,S5 support
Keyboard from EC	No
USB device	No

[Option]:ns -- Component marked "ns" is not stuff

[Use State]:new --Component Marked "new" is new Materiel.

PCB Footprints



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Title <Title>

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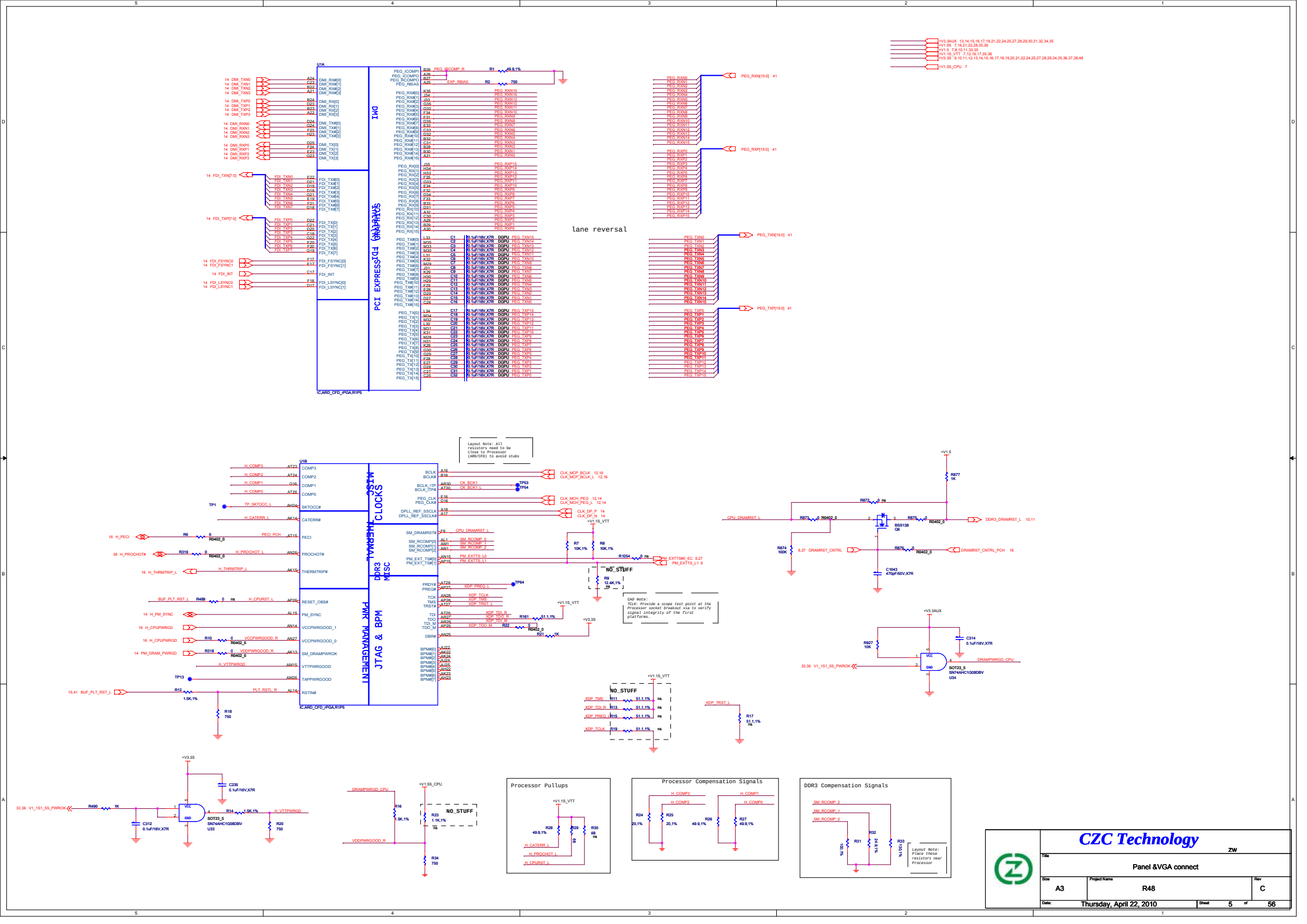
U1A
DMI
PCI EXPRESS* GRAPHICS
lane reversal
U1B
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
Layout Note: All resistors need to be close to Processor (ARD/CFD) to avoid stubs
NO_STUFF
CAD Note: TCLK: Provide a scope test point at the Processor socket breakout via to verify signal integrity of the first platforms.
SOT23_5 SN74AHC1G08DBV U34
SOT23_5 SN74AHC1G08DBV U33
Processor Pullups
Processor Compensation Signals
DDR3 Compensation Signals
Layout Note: Place these resistors near Processor
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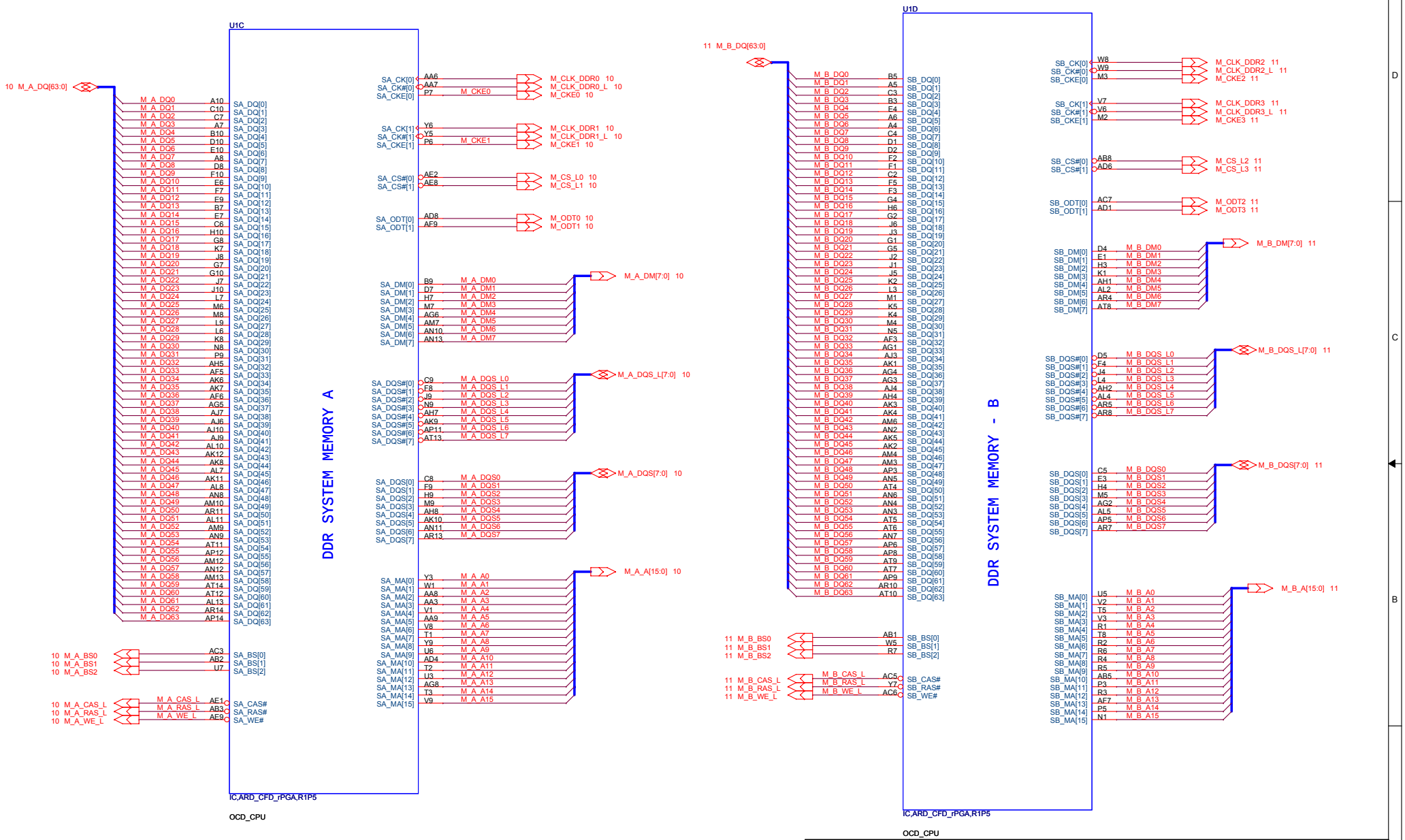

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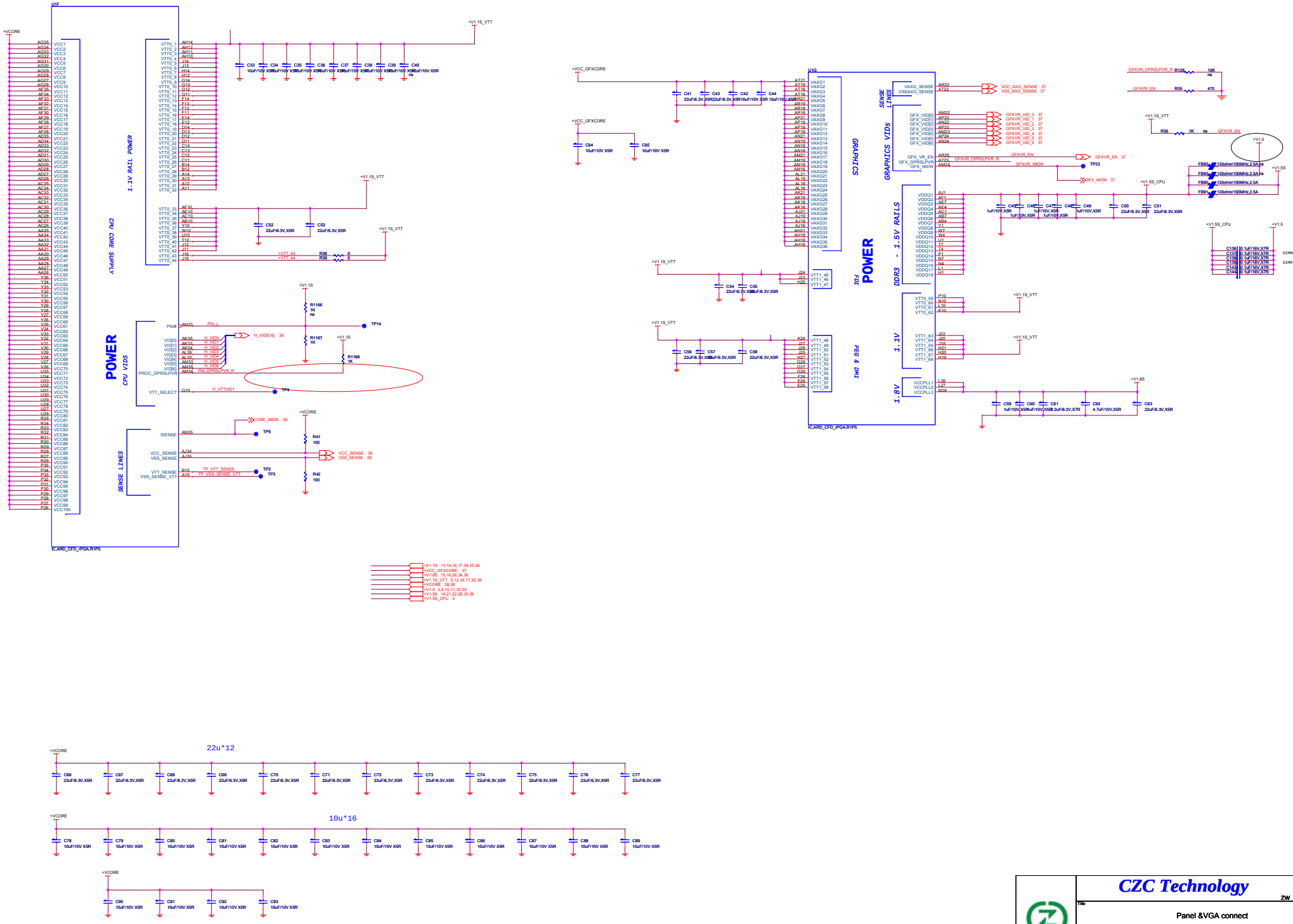

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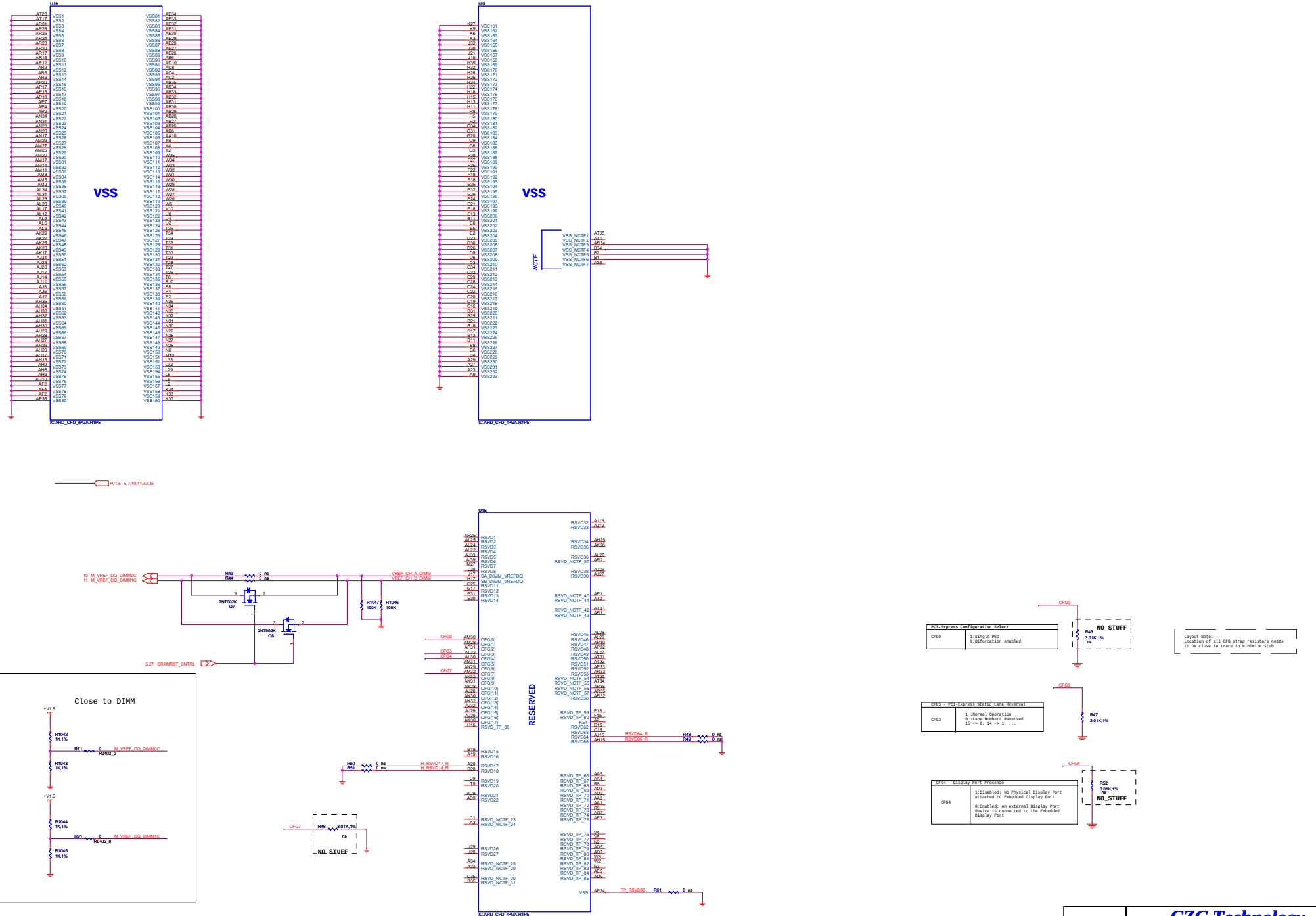

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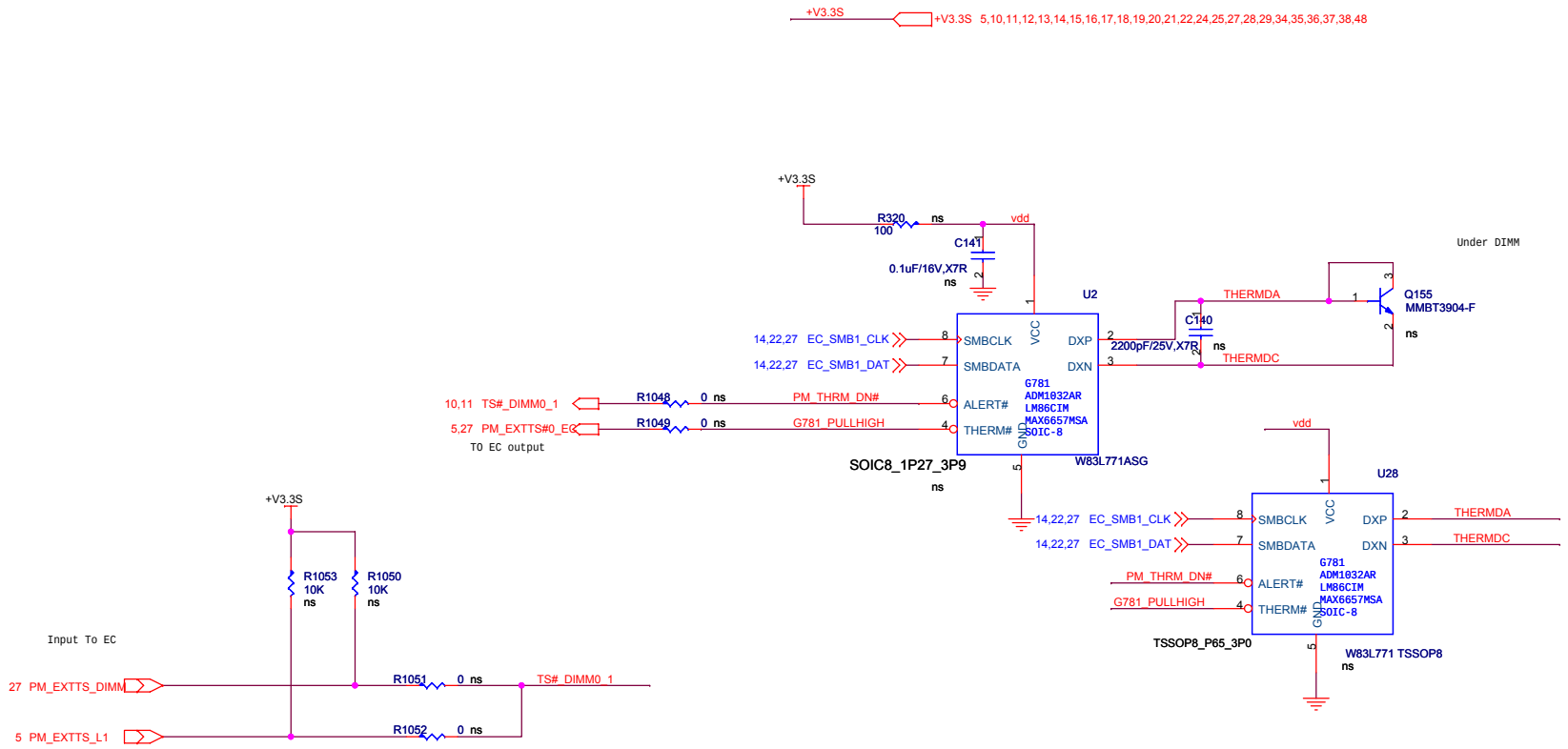

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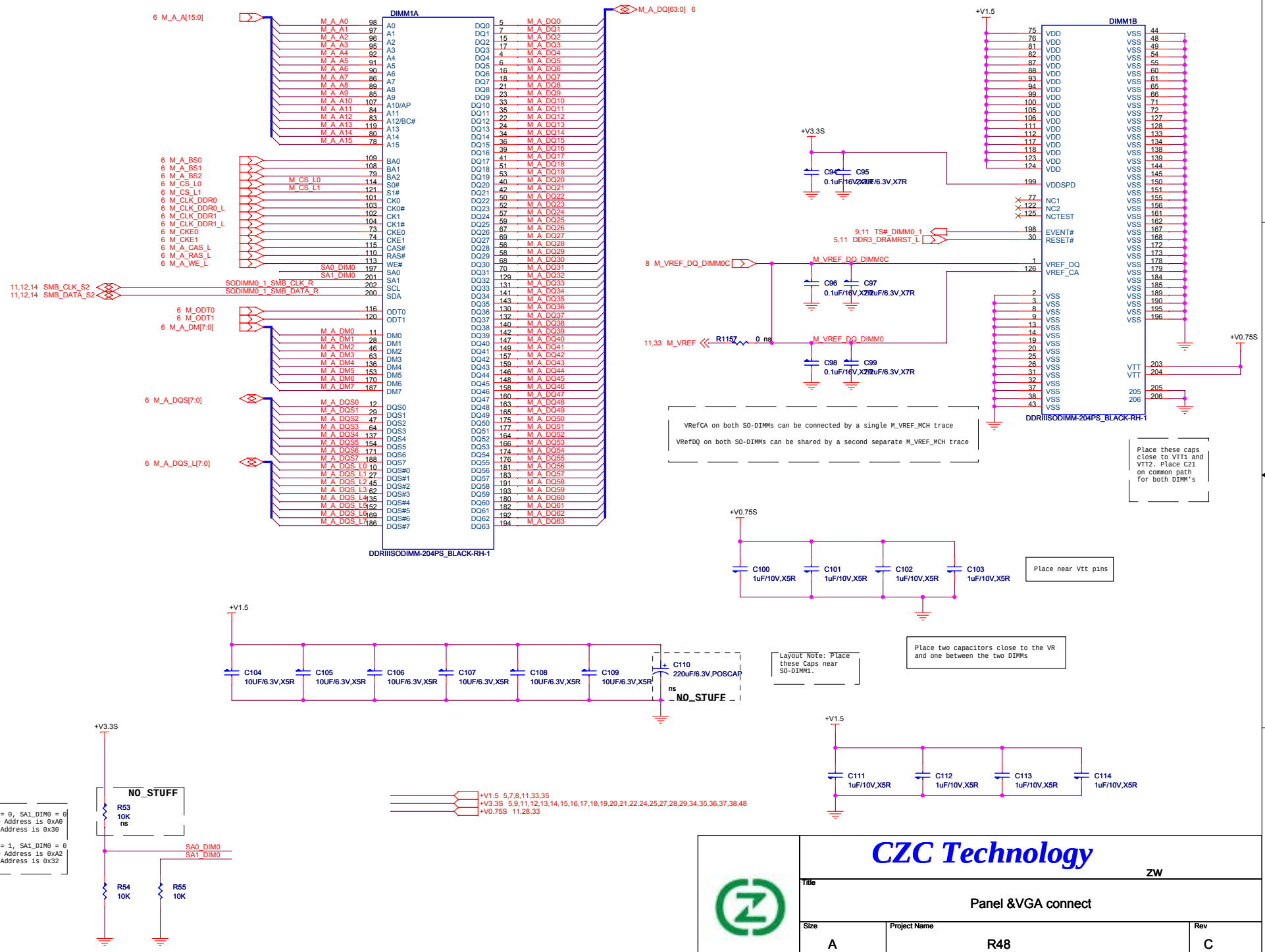
Channel A High :9.2mm



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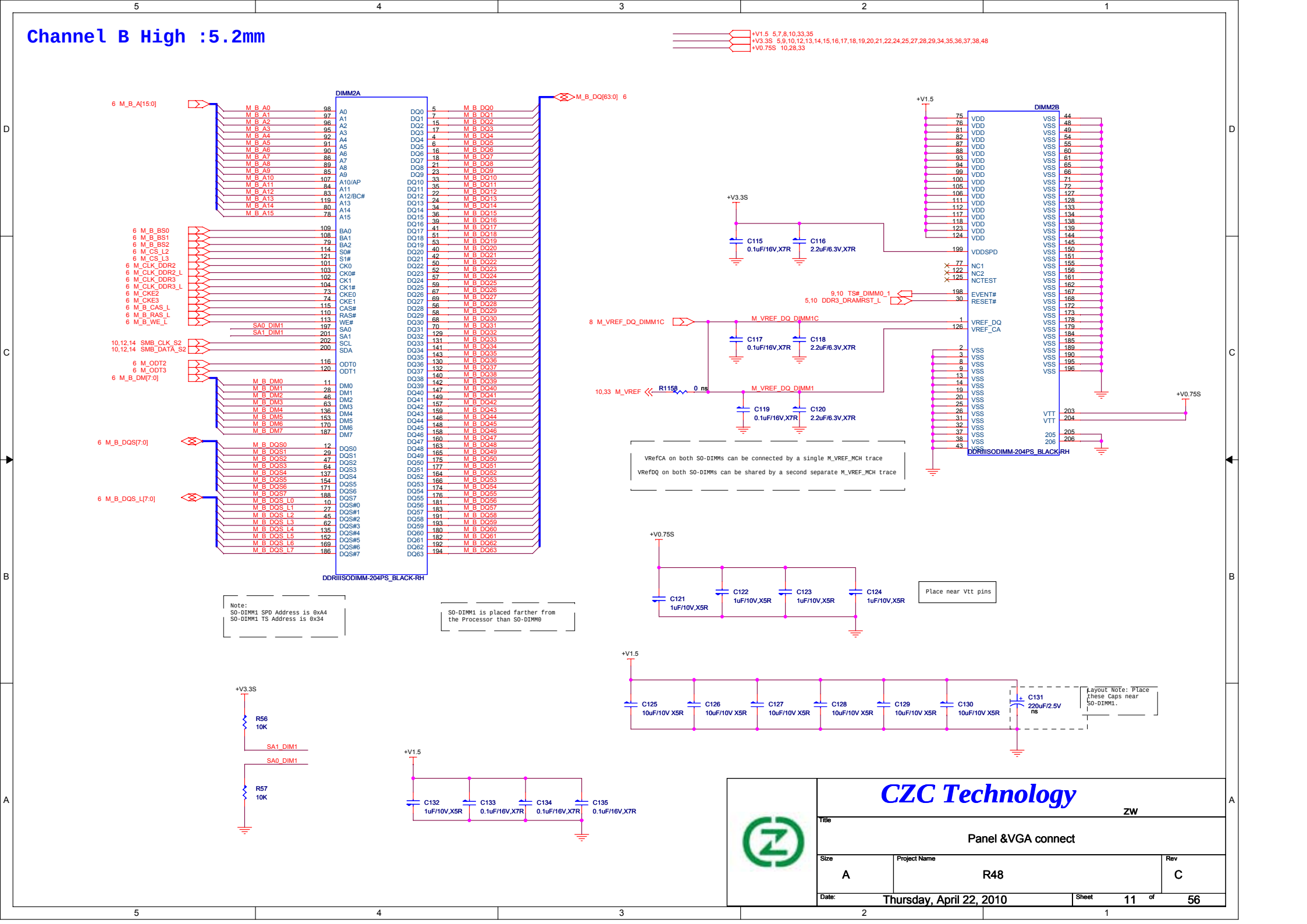
Channel B High :5.2mm



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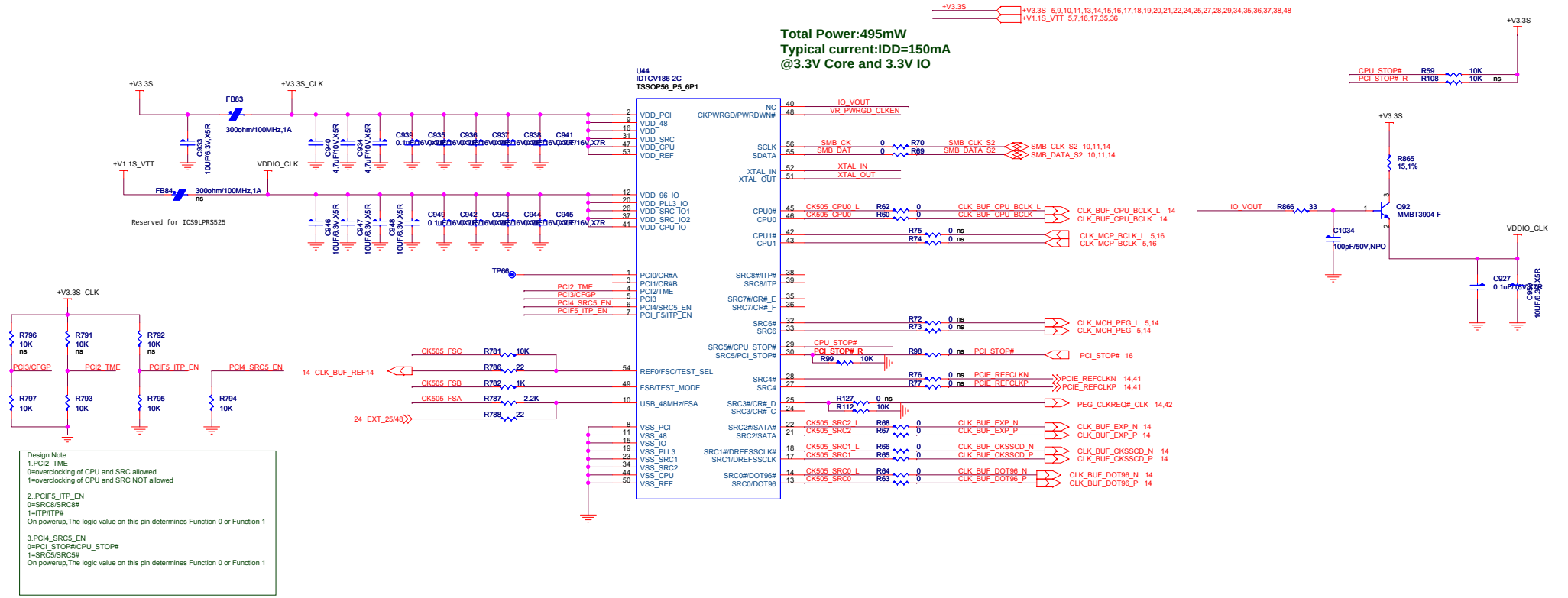
Total Power:495mW
Typical current:IDD=150mA
@3.3V Core and 3.3V IO



Design Note:
1.PCI2_TME
0=overclocking of CPU and SRC allowed
1=overclocking of CPU and SRC NOT allowed

2..PCIF5_ITP_EN
0=SRC8/SRC8#
1=ITP/ITP#
On powerup,The logic value on this pin determines Function 0 or Function 1

3.PCI4_SRC5_EN
0=PCI_STOP#/CPU_STOP#
1=SRC5/SRC5#
On powerup,The logic value on this pin determines Function 0 or Function 1

FSC BSEL2	FSB BSEL1	FSA BSEL0	Host Clock frequency MHz
1	0	1	100
0	0	1	133
0	1	1	166
0	1	0	200
0	0	0	266
1	0	0	333
1	1	0	400
1	1	1	Reserved

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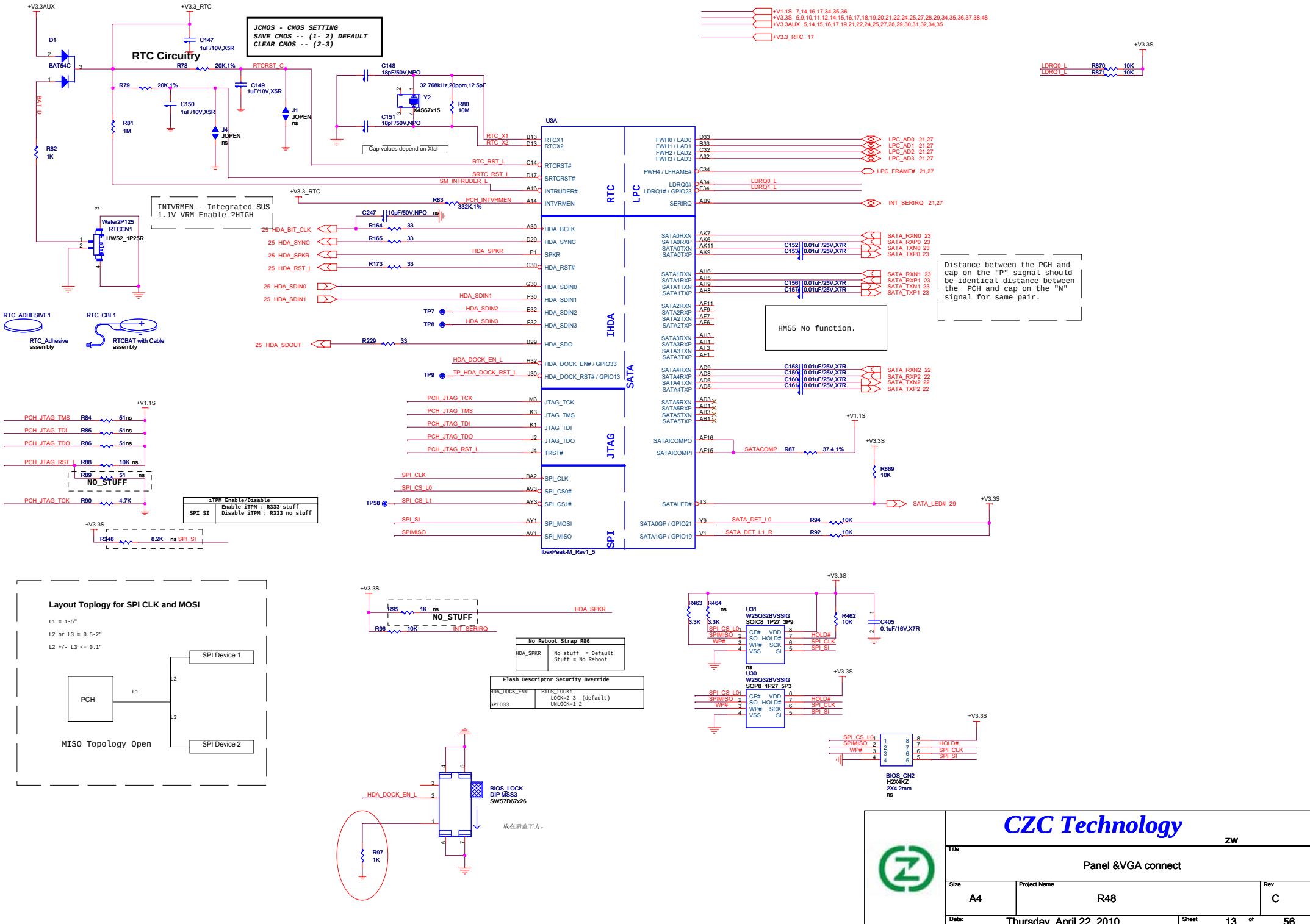
RTC Circuitry
JCMOS - CMOS SETTING
SAVE CMOS -- (1- 2) DEFAULT
CLEAR CMOS -- (2-3)
INTVRMEN - Integrated SUS 1.1V VRM Enable ?HIGH
Cap values depend on Xtal
Distance between the PCH and cap on the "P" signal should be identical distance between the PCH and cap on the "N" signal for same pair.
HM55 No function.
NO_STUFF
iTPM Enable/Disable
Enable iTPM : R333 stuff
Disable iTPM : R333 no stuff
No Reboot Strap R86
HDA_SPKR
No stuff = Default
Stuff = No Reboot
Flash Descriptor Security Override
HDA_DOCK_EN#
GPIO33
BIOS_LOCK:
LOCK=2-3 (default)
UNLOCK=1-2
Layout Toplogy for SPI CLK and MOSI
L1 = 1-5"
L2 or L3 = 0.5-2"
L2 +/- L3 <= 0.1"
PCH
SPI Device 1
SPI Device 2
MISO Topology Open
U3A
RTC
LPC
IHDA
SATA
JTAG
SPI
IbexPeak-M_Rev1_5
U31
W25Q32BVSSIG
SOIC8_1P27_3P9
U30
W25Q32BVSSIG
SOP8_1P27_5P3
BIOS_CN2
H2X4KZ
2X4 2mm
BIOS_LOCK
DIP MSS3
SWS7D67x26
放在后盖下方。
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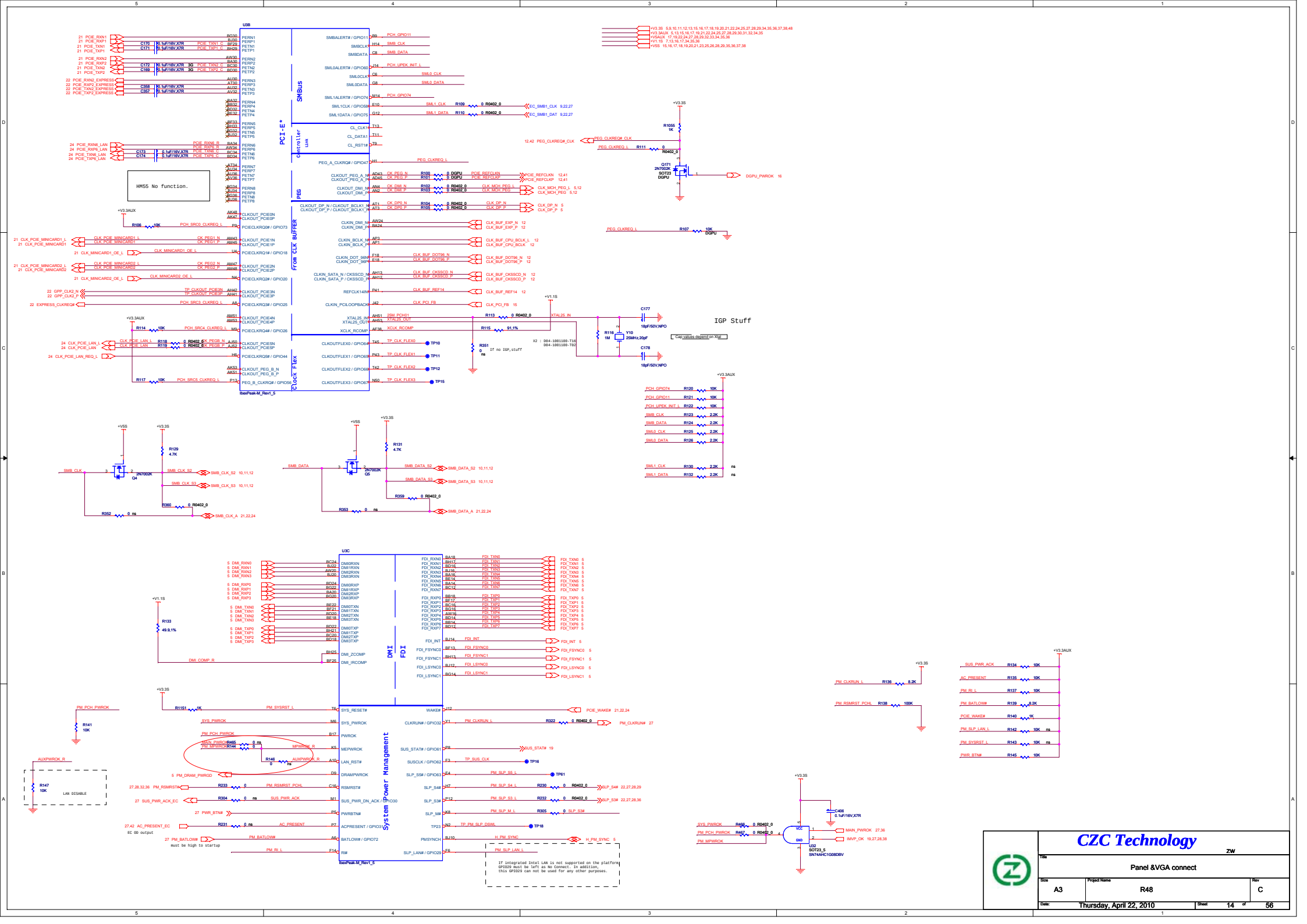
U3B
PCI-E*
SMBus
LAN Controller
PEG
From CLK BUFFER
Clock Flex
HM55 No function.
IbexPeak-M_Rev1_5
U3C
DMI
FDI
System Power Management
If integrated Intel LAN is not supported on the platform, GPIO29 must be left as No Connect. In addition, this GPIO29 can not be used for any other purposes.
IGP Stuff
Cap values depend on Xtal
LAN DISABLE
EC OD output
must be high to startup
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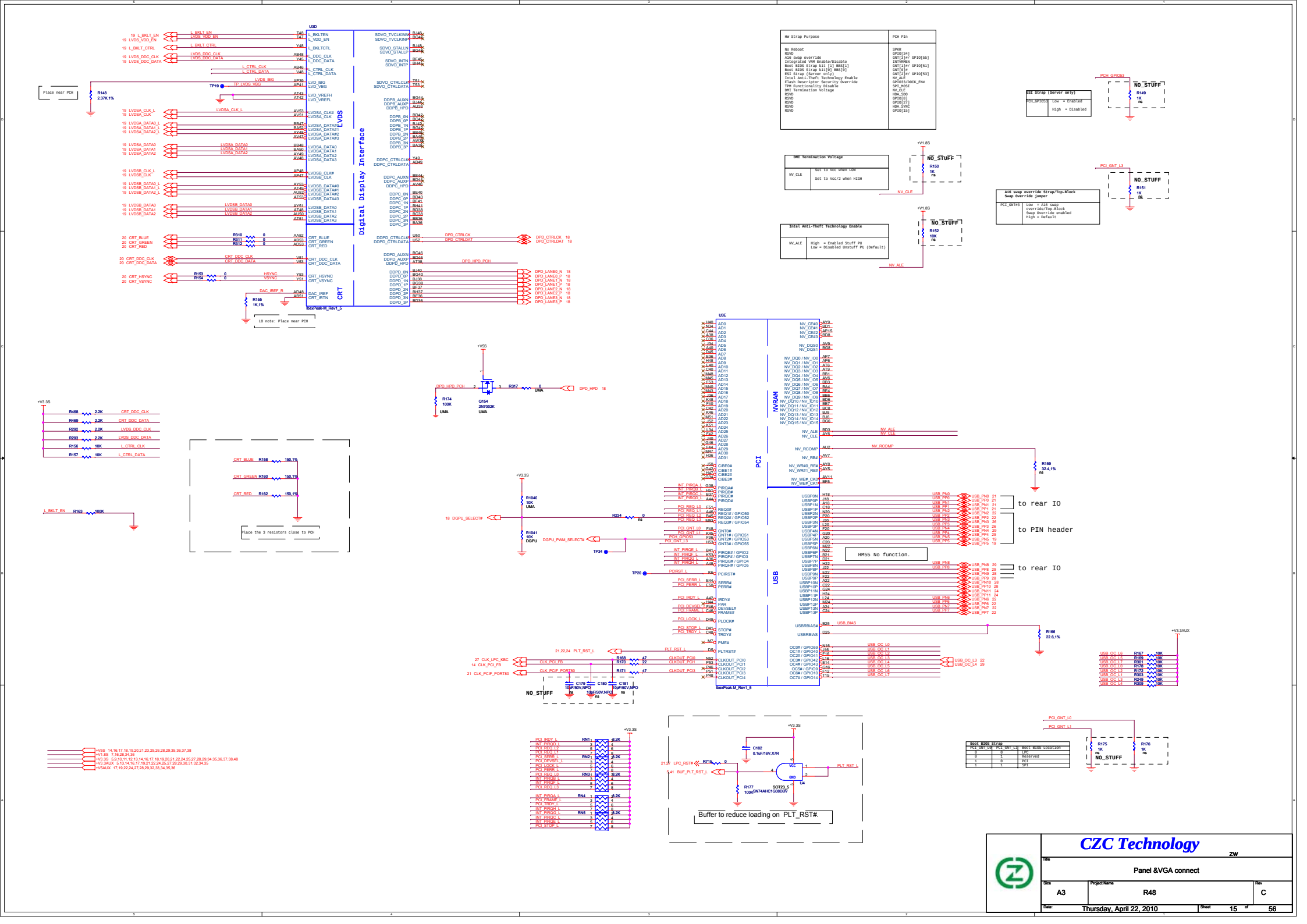

Company	CZC Technology
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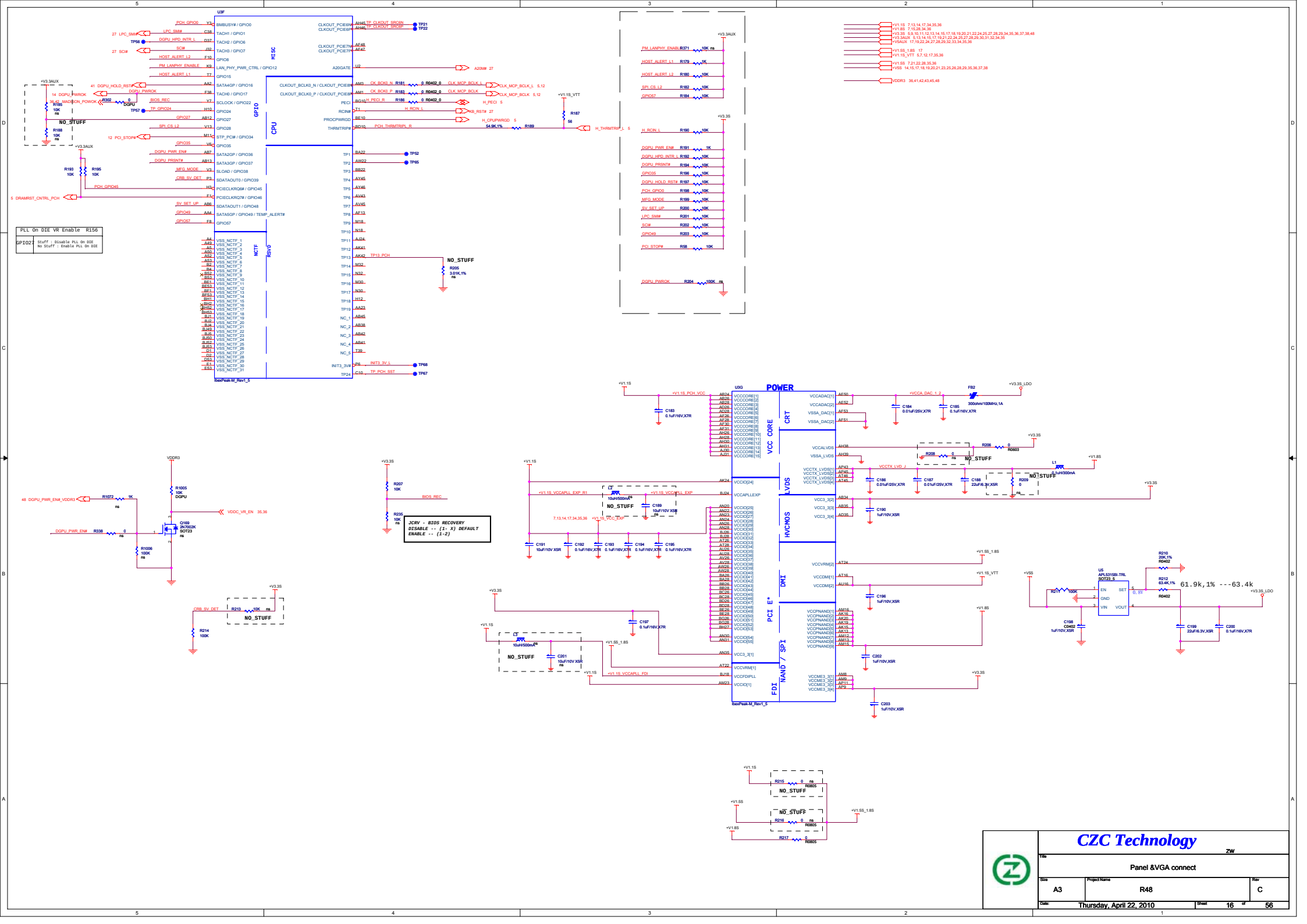
U3F
CPU
GPIO
MISC
NCTF
RSVD
PLL On DIE VR Enable R156
GPIO27 Stuff : Disable PLL On DIE
No Stuff : Enable PLL On DIE
NO_STUFF
BIOS_REC
JCRV - BIOS RECOVERY
DISABLE -- (1- X) DEFAULT
ENABLE -- (1-2)
U3G
POWER
VCC CORE
CRT
LVDS
HVCMOS
PCI E*
DMI
NAND / SPI
FDI
IbexPeak-M_Rev1_5
U5
APL5315BI-TRL
SOT23_5
61.9k,1% ---63.4k
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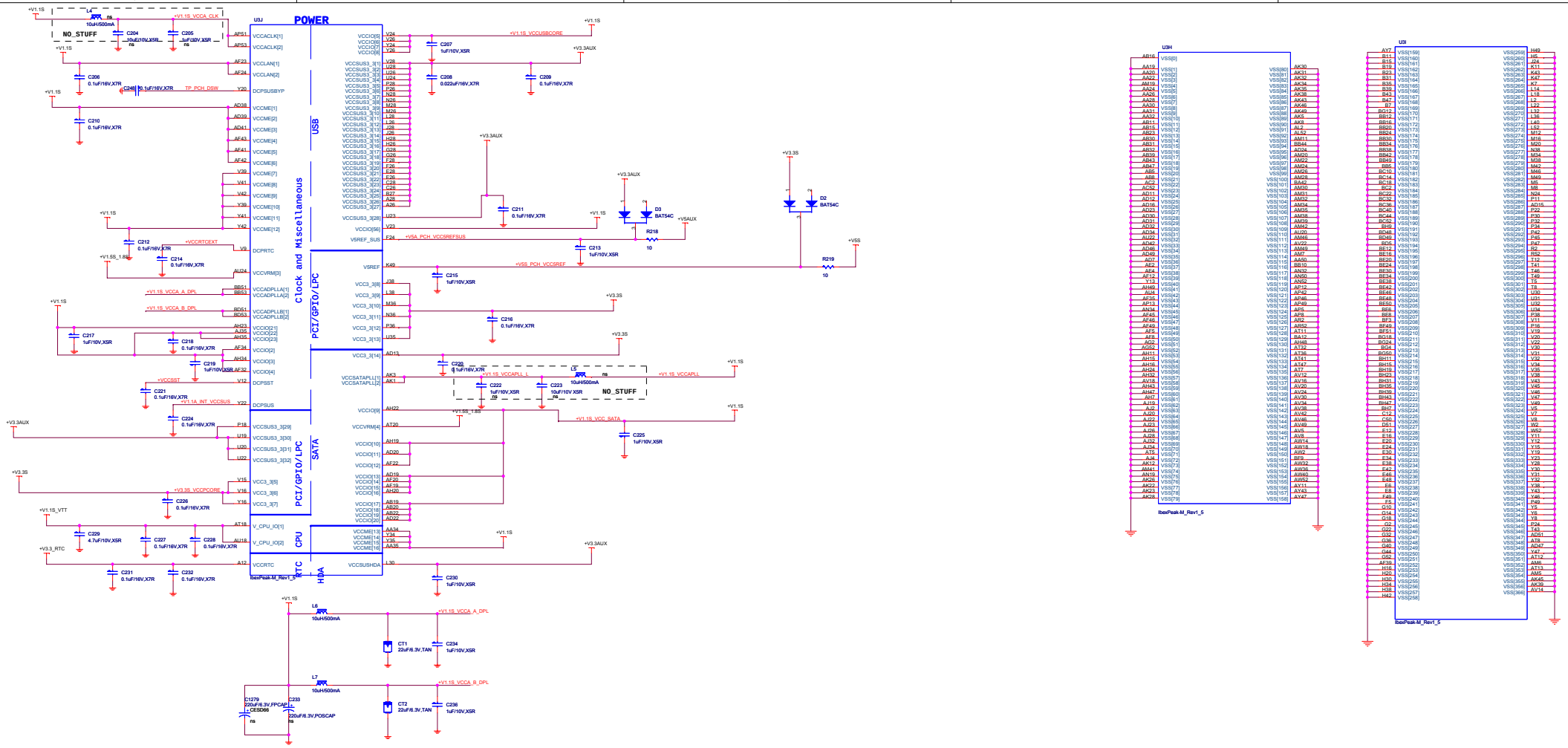

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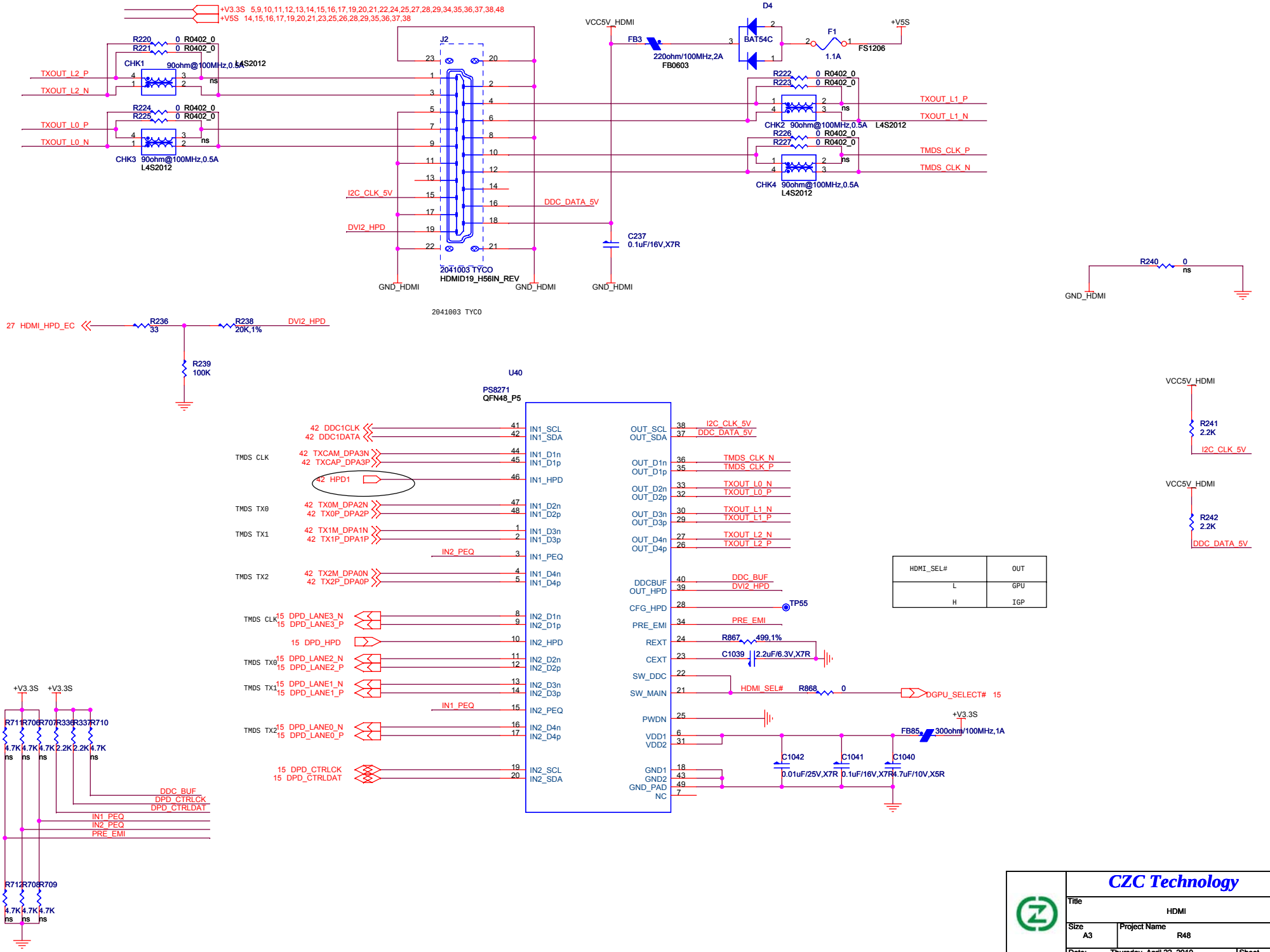
+V3.3S 5,9,10,11,12,13,14,15,16,17,19,20,21,22,24,25,27,28,29,34,35,36,37,38,48
+V5S 14,15,16,17,19,20,21,23,25,26,28,29,35,36,37,38
R220 0 R0402_0
R221 0 R0402_0
CHK1 90ohm@100MHz,0.5A L4S2012
TXOUT_L2_P
TXOUT_L2_N
R224 0 R0402_0
R225 0 R0402_0
TXOUT_L0_P
TXOUT_L0_N
CHK3 90ohm@100MHz,0.5A L4S2012
J2
I2C_CLK_5V
DVI2_HPD
DDC_DATA_5V
2041003 TYCO
HDMID19_H56IN_REV
GND_HDMI
VCC5V_HDMI
FB3
220ohm/100MHz,2A
FB0603
D4
BAT54C
F1
1.1A
FS1206
+V5S
R222 0 R0402_0
R223 0 R0402_0
TXOUT_L1_P
TXOUT_L1_N
CHK2 90ohm@100MHz,0.5A L4S2012
R226 0 R0402_0
R227 0 R0402_0
TMDS_CLK_P
TMDS_CLK_N
CHK4 90ohm@100MHz,0.5A L4S2012
C237
0.1uF/16V,X7R
R240 0 ns
27 HDMI_HPD_EC
R236 33
R238 20K,1%
R239 100K
U40
PS8271
QFN48_P5
42 DDC1CLK
42 DDC1DATA
TMDS CLK
42 TXCAM_DPA3N
42 TXCAP_DPA3P
42 HPD1
TMDS TX0
42 TX0M_DPA2N
42 TX0P_DPA2P
TMDS TX1
42 TX1M_DPA1N
42 TX1P_DPA1P
IN2_PEQ
TMDS TX2
42 TX2M_DPA0N
42 TX2P_DPA0P
15 DPD_LANE3_N
15 DPD_LANE3_P
15 DPD_HPD
15 DPD_LANE2_N
15 DPD_LANE2_P
15 DPD_LANE1_N
15 DPD_LANE1_P
IN1_PEQ
15 DPD_LANE0_N
15 DPD_LANE0_P
15 DPD_CTRLCK
15 DPD_CTRLDAT
IN1_SCL
IN1_SDA
IN1_D1n
IN1_D1p
IN1_HPD
IN1_D2n
IN1_D2p
IN1_D3n
IN1_D3p
IN1_PEQ
IN1_D4n
IN1_D4p
IN2_D1n
IN2_D1p
IN2_HPD
IN2_D2n
IN2_D2p
IN2_D3n
IN2_D3p
IN2_PEQ
IN2_D4n
IN2_D4p
IN2_SCL
IN2_SDA
OUT_SCL
OUT_SDA
I2C_CLK_5V
DDC_DATA_5V
OUT_D1n
OUT_D1p
TMDS_CLK_N
TMDS_CLK_P
OUT_D2n
OUT_D2p
TXOUT_L0_N
TXOUT_L0_P
OUT_D3n
OUT_D3p
TXOUT_L1_N
TXOUT_L1_P
OUT_D4n
OUT_D4p
TXOUT_L2_N
TXOUT_L2_P
DDCBUF
OUT_HPD
DDC_BUF
DVI2_HPD
CFG_HPD
TP55
PRE_EMI
REXT
R867 499,1%
CEXT
C1039 2.2uF/6.3V,X7R
SW_DDC
SW_MAIN
HDMI_SEL#
R868 0
DGPU_SELECT# 15
PWDN
VDD1
VDD2
GND1
GND2
GND_PAD
NC
FB85 300ohm/100MHz,1A
C1042 0.01uF/25V,X7R
C1041 0.1uF/16V,X7R
C1040 4.7uF/10V,X5R
HDMI_SEL# | OUT
L | GPU
H | IGP
VCC5V_HDMI
R241 2.2K
I2C_CLK_5V
R242 2.2K
DDC_DATA_5V
+V3.3S
R711 4.7K ns
R706 4.7K ns
R707 4.7K ns
R336 2.2K
R337 2.2K
R710 4.7K ns
DDC_BUF
DPD_CTRLCK
DPD_CTRLDAT
IN1_PEQ
IN2_PEQ
PRE_EMI
R712 4.7K ns
R708 4.7K ns
R709 4.7K ns
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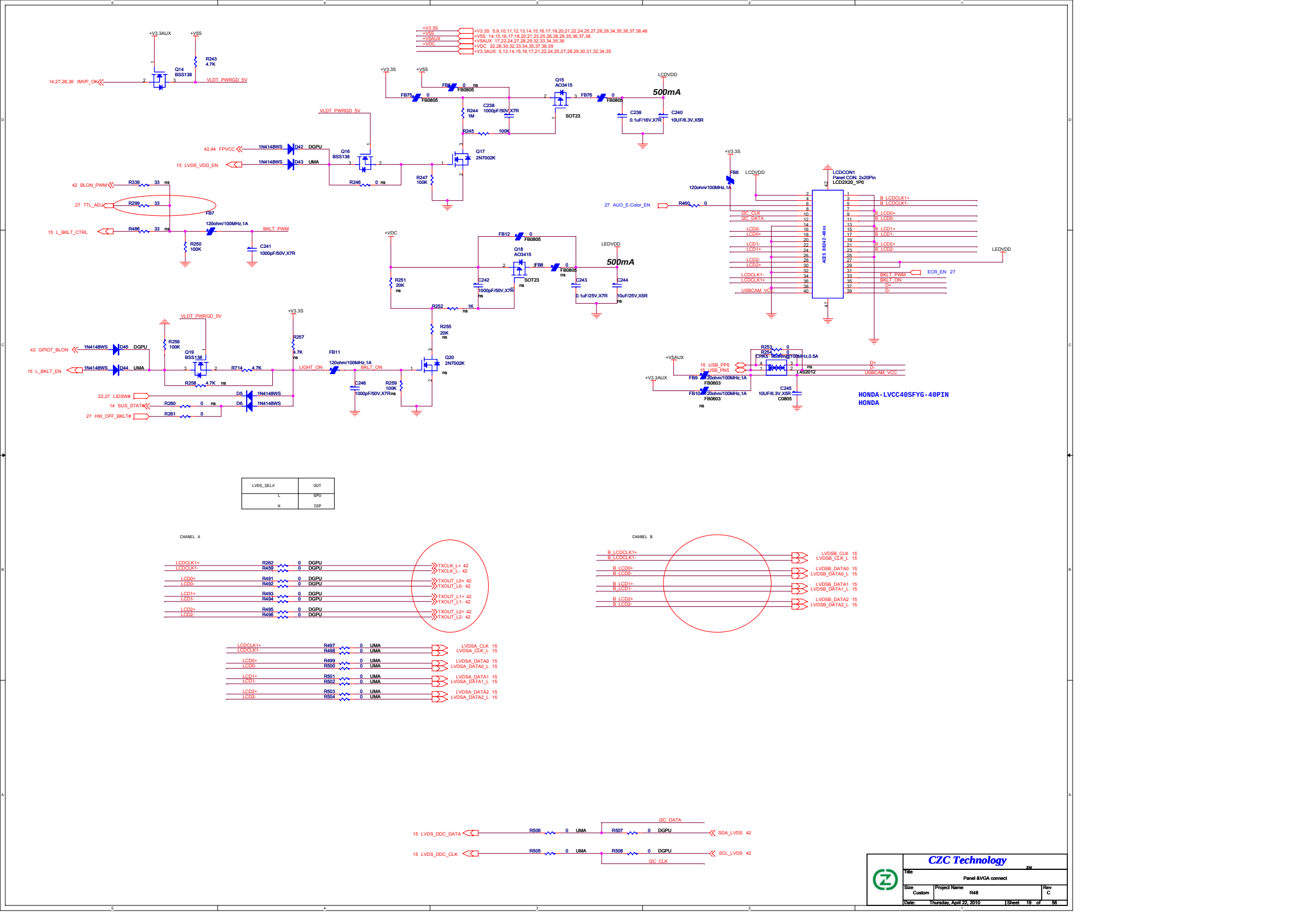
+V3.3AUX
+V5S
Q14
BSS138
R243
4.7K
14,27,28,38 IMVP_OK
VLDT_PWRGD_5V
+V3.3S
+V5S
+V5AUX
+VDC
+V3.3S 5,9,10,11,12,13,14,15,16,17,18,20,21,22,24,25,27,28,29,34,35,36,37,38,48
+V5S 14,15,16,17,18,20,21,23,25,26,28,29,35,36,37,38
+V5AUX 17,22,24,27,28,29,32,33,34,35,36
+VDC 22,28,30,32,33,34,35,37,38,39
+V3.3AUX 5,13,14,15,16,17,21,22,24,25,27,28,29,30,31,32,34,35
FB74 0 ns FB0805
FB75 0 FB0805
Q15
AO3415
SOT23
FB76 0 FB0805
LCDVDD
500mA
C238
1000pF/50V,X7R
R244
1M
R245
100K
C239
0.1uF/16V,X7R
C240
10UF/6.3V,X5R
42,44 FPVCC
1N4148WS D42 DGPU
1N4148WS D43 UMA
15 LVDS_VDD_EN
Q16
BSS138
Q17
2N7002K
R246 0 ns
R247
100K
42 BLON_PWM
R339 33 ns
27 TTL_ADJ
R299 33
FB7
15 L_BKLT_CTRL
R486 33 ns
120ohm/100MHz,1A
BKLT_PWM
R250
100K
C241
1000pF/50V,X7R
+VDC
FB12 0 FB0805
Q18
AO3415
FB8 0 FB0805 ns
LEDVDD
500mA
R251
20K
ns
C242
1000pF/50V,X7R
ns
C243
0.1uF/25V,X7R
C244
10uF/25V,X5R
ns
R252 1K ns
R255
20K
ns
+V3.3AUX
FB6
LCDVDD
120ohm/100MHz,1A
27 AUO_E-Color_EN
R460 0
LCDCON1
Panel CON, 2x20Pin
LCD2X20_1P0
I2C_CLK
I2C_DATA
LCD0-
LCD0+
LCD1-
LCD1+
LCD2-
LCD2+
LCDCLK1-
LCDCLK1+
USBCAM_VCC
B_LCDCLK1+
B_LCDCLK1-
B_LCD0+
B_LCD0-
B_LCD1+
B_LCD1-
B_LCD2+
B_LCD2-
BKLT_PWM
BKLT_ON
D+
D-
ECR_EN 27
ACES 88042-40Axx
VLDT_PWRGD_5V
+V3.3S
42 GPIO7_BLON
15 L_BKLT_EN
1N4148WS D45 DGPU
1N4148WS D44 UMA
R256
100K
Q19
BSS138
R257
4.7K
ns
R714 4.7K
R258 4.7K ns
LIGHT_ON
FB11
120ohm/100MHz,1A
BKLT_ON
Q20
2N7002K
ns
C246
1000pF/50V,X7R
ns
R259
100K
ns
22,27 LIDSW#
14 SUS_STAT#
27 HW_OFF_BKLT#
D5 1N4148WS
D6 1N4148WS
R260 0 ns
R261 0
+V5AUX
+V3.3AUX
15 USB_PP5
15 USB_PN5
R253 0
R254 0
CHRG 1608mg/100MHz,0.5A
FB9 120ohm/100MHz,1A FB0603
FB10 120ohm/100MHz,1A FB0603
ns
C245
10UF/6.3V,X5R
C0805
1.5A/2012
D+
D-
USBCAM_VCC
HONDA-LVCC40SFYG-40PIN
HONDA
LVDS_SEL#
OUT
L
GPU
H
IGP
CHANEL A
LCDCLK1+
LCDCLK1-
LCD0+
LCD0-
LCD1+
LCD1-
LCD2+
LCD2-
R462 0 DGPU
R463 0 DGPU
R491 0 DGPU
R492 0 DGPU
R493 0 DGPU
R494 0 DGPU
R495 0 DGPU
R496 0 DGPU
TXCLK_L+ 42
TXCLK_L- 42
TXOUT_L0+ 42
TXOUT_L0- 42
TXOUT_L1+ 42
TXOUT_L1- 42
TXOUT_L2+ 42
TXOUT_L2- 42
CHANEL B
B_LCDCLK1+
B_LCDCLK1-
B_LCD0+
B_LCD0-
B_LCD1+
B_LCD1-
B_LCD2+
B_LCD2-
LVDSB_CLK 15
LVDSB_CLK_L 15
LVDSB_DATA0 15
LVDSB_DATA0_L 15
LVDSB_DATA1 15
LVDSB_DATA1_L 15
LVDSB_DATA2 15
LVDSB_DATA2_L 15
R497 0 UMA
R498 0 UMA
R499 0 UMA
R500 0 UMA
R501 0 UMA
R502 0 UMA
R503 0 UMA
R504 0 UMA
LVDSA_CLK 15
LVDSA_CLK_L 15
LVDSA_DATA0 15
LVDSA_DATA0_L 15
LVDSA_DATA1 15
LVDSA_DATA1_L 15
LVDSA_DATA2 15
LVDSA_DATA2_L 15
15 LVDS_DDC_DATA
15 LVDS_DDC_CLK
R506 0 UMA
R505 0 UMA
R507 0 DGPU
R508 0 DGPU
I2C_DATA
I2C_CLK
SDA_LVDS 42
SCL_LVDS 42
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RGB_SEL#	OUT
L	GPU
H	IGP

15 CRT_VSYNC — R510 0 UMA — R511 0 DGPU — VSYNC# — VSYNC_DAC1 42,48

15 CRT_HSYNC — R509 0 UMA — R512 0 DGPU — HSYNC# — HSYNC_DAC1 42,48

42 R_DAC1 — 15 CRT_RED — R519 0 DGPU / R518 0 UMA — R

42 G_DAC1 — 15 CRT_GREEN — R521 0 DGPU / R520 0 UMA — G

42 B_DAC1 — 15 CRT_BLUE — R523 0 DGPU / R522 0 UMA — B

15 CRT_DDC_DATA — R514 0 UMA — R515 0 DGPU — DAC_SDAT — DDC6DATA 42

15 CRT_DDC_CLK — R513 0 UMA — R516 0 DGPU — DAC_SCL — DDC6CLK 42

+V3.3S — R264 10K — R406 0 — CRT_DET# 27

+5VCRT — D9 BAT54SPT — D10 BAT54SPT — D11 BAT54SPT — RED_1 — GREEN_1 — BLUE_1 — GND_CRT

+V5S — F2 1.1A FS1206 — D8 BAT54C — FB15 220ohm/100MHz,2A — R267 100K — C260 0.1uF/16V,X7R

1N4148WS D65 — D66 1N4148WS — D12 BAT54SPT — D13 BAT54SPT — R265 4.7K — R266 4.7K

R — G — B — L8 82nH/100Mhz — L9 82nH/100Mhz — L10 82nH/100Mhz — RED_1 — GREEN_1 — BLUE_1

R269 150,1% — R270 150,1% — R271 150,1%

C261 10pF/50V,NPO — C262 10pF/50V,NPO — C263 10pF/50V,NPO — C264 10pF/50V,NPO — C265 10pF/50V,NPO — C266 10pF/50V,NPO

VGA1 — dsub15C-F — VGA2F15H12IN_REV_NB

R268 0 R0402_0 — SPDAT1_5V — DAC_SDAT — Q21 2N7002K

R272 0 R0402_0 — SPCLK1_5V — DAC_SCL — Q22 2N7002K

U11 74AHCT1G125 — VSYNC# — CRT_VS — R274 27 — CRT_VS_1

U12 74AHCT1G125 — HSYNC# — CRT_HS — R275 27 — CRT_HS_1

C267 0.1uF/16V,X7R — C268 0.1uF/16V,X7R

D14 BAT54SPT — D15 BAT54SPT

C269 10pF/50V,NPO — C270 10pF/50V,NPO

R273 0 ns

H24 BOSS MH24X40X80 ns

+V3.3S — +V5S 14,15,16,17,18,19,21,23,25,26,28,29,35,36,37,38

+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,21,22,24,25,27,28,29,34,35,36,37,38,48

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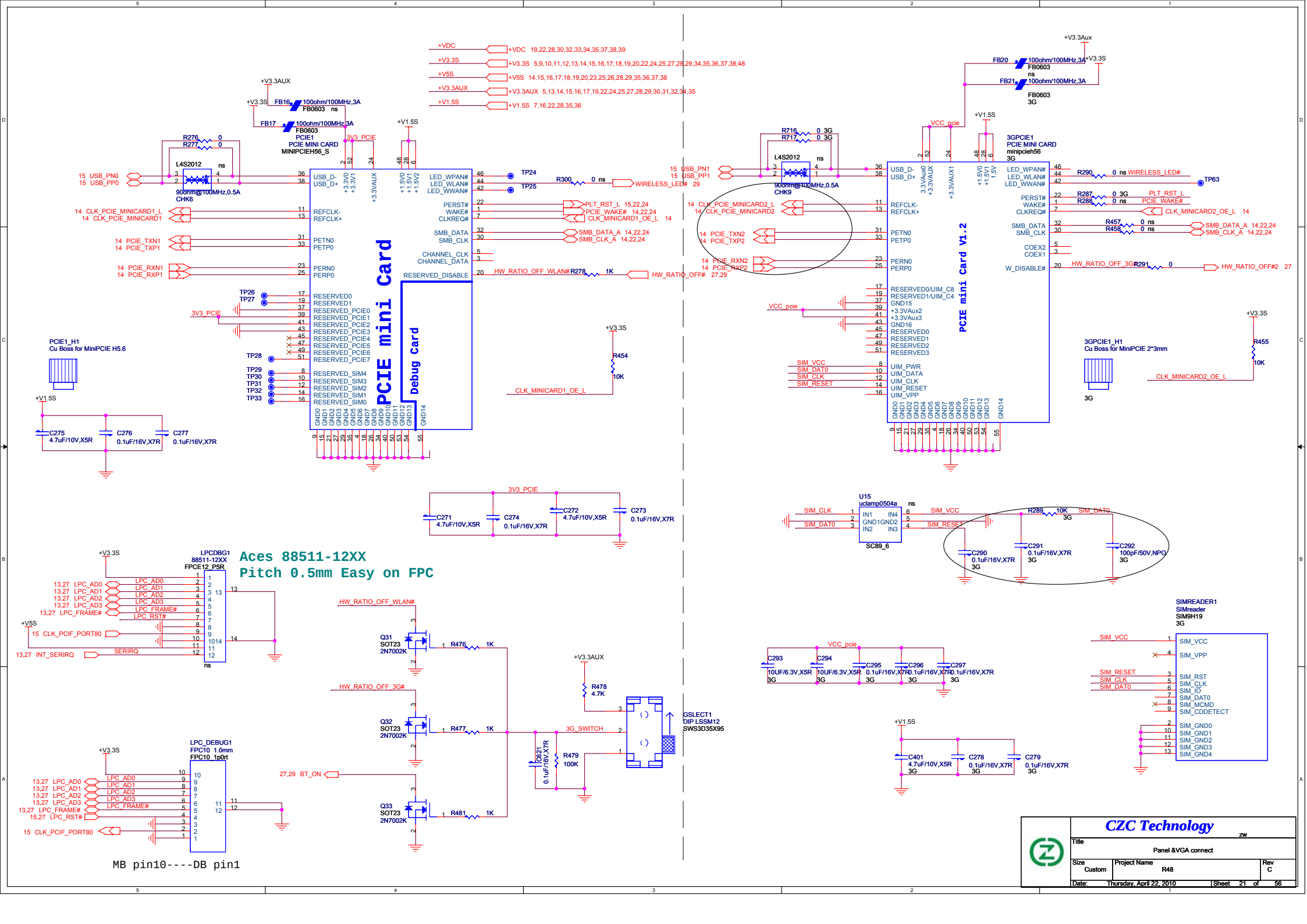
PCIE mini Card
Debug Card
PCIE mini Card V1.2
3GPCIE1
PCIE MINI CARD
minipcieh56
3G
PCIE1
PCIE MINI CARD
MINIPCIEH56_S
PCIE1_H1
Cu Boss for MiniPCIE H5.6
3GPCIE1_H1
Cu Boss for MiniPCIE 2*3mm
LPCDBG1
88511-12XX
FPCE12_P5R
Aces 88511-12XX
Pitch 0.5mm Easy on FPC
LPC_DEBUG1
FPC10 1.0mm
FPC10 1p0rt
U15
uclamp0504a
SC89_6
SIMREADER1
SIMreader
SIM9H19
3G
GSLECT1
DIP LSSM12
SWS3D35X95
Q31
SOT23
2N7002K
Q32
SOT23
2N7002K
Q33
SOT23
2N7002K
CHK6
CHK9
MB pin10----DB pin1
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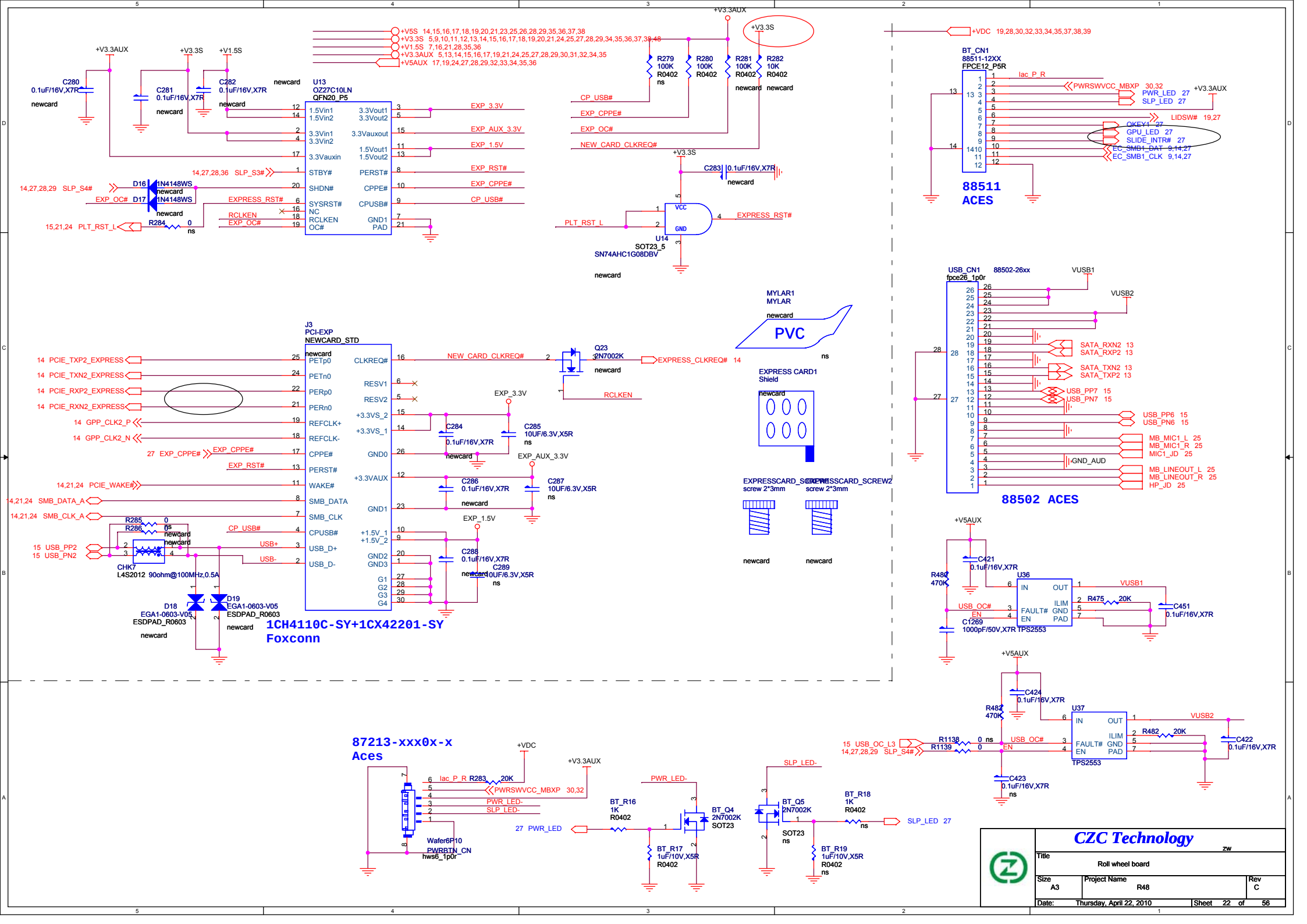
+V5S 14,15,16,17,18,19,20,21,23,25,26,28,29,35,36,37,38
+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,24,25,27,28,29,34,35,36,37,38,48
+V1.5S 7,16,21,28,35,36
+V3.3AUX 5,13,14,15,16,17,19,21,24,25,27,28,29,30,31,32,34,35
+V5AUX 17,19,24,27,28,29,32,33,34,35,36
+V3.3AUX
+V3.3S
+V1.5S
C280 0.1uF/16V,X7R newcard
C281 0.1uF/16V,X7R newcard
C282 0.1uF/16V,X7R newcard
U13
OZ27C10LN
QFN20_P5
1.5Vin1
1.5Vin2
3.3Vin1
3.3Vin2
3.3Vauxin
STBY#
SHDN#
SYSRST#
NC
RCLKEN
OC#
3.3Vout1
3.3Vout2
3.3Vauxout
1.5Vout1
1.5Vout2
PERST#
CPPE#
CPUSB#
GND1
PAD
EXP_3.3V
EXP_AUX_3.3V
EXP_1.5V
EXP_RST#
EXP_CPPE#
CP_USB#
14,27,28,36 SLP_S3#
14,27,28,29 SLP_S4#
EXP_OC#
D16 1N4148WS newcard
D17 1N4148WS newcard
EXPRESS_RST#
RCLKEN
15,21,24 PLT_RST_L
R284 0 ns
R279 100K R0402 ns
R280 100K R0402
R281 100K R0402 newcard
R282 10K R0402 newcard
CP_USB#
EXP_CPPE#
EXP_OC#
NEW_CARD_CLKREQ#
C283 0.1uF/16V,X7R newcard
U14
SOT23_5
SN74AHC1G08DBV
VCC
GND
PLT_RST_L
EXPRESS_RST#
newcard
+VDC 19,28,30,32,33,34,35,37,38,39
BT_CN1
88511-12XX
FPCE12_P5R
lac_P_R
PWRSWVCC_MBXP 30,32
PWR_LED 27
SLP_LED 27
LIDSW# 19,27
OKEY1 27
GPU_LED 27
SLIDE_INTR# 27
EC_SMB1_DAT 9,14,27
EC_SMB1_CLK 9,14,27
88511
ACES
J3
PCI-EXP
NEWCARD_STD
14 PCIE_TXP2_EXPRESS
14 PCIE_TXN2_EXPRESS
14 PCIE_RXP2_EXPRESS
14 PCIE_RXN2_EXPRESS
14 GPP_CLK2_P
14 GPP_CLK2_N
27 EXP_CPPE#
EXP_RST#
14,21,24 PCIE_WAKE#
14,21,24 SMB_DATA_A
14,21,24 SMB_CLK_A
PETp0
PETn0
PERp0
PERn0
REFCLK+
REFCLK-
CPPE#
PERST#
WAKE#
SMB_DATA
SMB_CLK
CPUSB#
USB_D+
USB_D-
CLKREQ#
RESV1
RESV2
+3.3VS_2
+3.3VS_1
GND0
+3.3VAUX
GND1
+1.5V_1
+1.5V_2
GND2
GND3
G1
G2
G3
G4
NEW_CARD_CLKREQ#
EXPRESS_CLKREQ# 14
RCLKEN
Q23
2N7002K
newcard
C284 0.1uF/16V,X7R newcard
C285 10UF/6.3V,X5R ns
C286 0.1uF/16V,X7R newcard
C287 10UF/6.3V,X5R ns
C288 0.1uF/16V,X7R newcard
C289 10UF/6.3V,X5R ns
EXP_3.3V
EXP_AUX_3.3V
EXP_1.5V
R285 0 ns newcard
R286 newcard
15 USB_PP2
15 USB_PN2
CP_USB#
USB+
USB-
CHK7
L4S2012 90ohm@100MHz,0.5A
D18 EGA1-0603-V05 ESDPAD_R0603 newcard
D19 EGA1-0603-V05 ESDPAD_R0603 newcard
1CH4110C-SY+1CX42201-SY
Foxconn
MYLAR1
MYLAR
newcard
PVC
ns
EXPRESS CARD1
Shield
newcard
EXPRESSCARD_SCREW1
EXPRESSCARD_SCREW2
screw 2*3mm
newcard
USB_CN1
88502-26xx
fpce26_1p0r
VUSB1
VUSB2
SATA_RXN2 13
SATA_RXP2 13
SATA_TXN2 13
SATA_TXP2 13
USB_PP7 15
USB_PN7 15
USB_PP6 15
USB_PN6 15
MB_MIC1_L 25
MB_MIC1_R 25
MIC1_JD 25
GND_AUD
MB_LINEOUT_L 25
MB_LINEOUT_R 25
HP_JD 25
88502 ACES
+V5AUX
C421 0.1uF/16V,X7R
R480 470K
U36
IN
OUT
ILIM
FAULT#
GND
EN
PAD
USB_OC#
R475 20K
C1269 1000pF/50V,X7R
TPS2553
C451 0.1uF/16V,X7R
C424 0.1uF/16V,X7R
R482 470K
U37
R482 20K
C423 0.1uF/16V,X7R ns
C422 0.1uF/16V,X7R
15 USB_OC_L3
14,27,28,29 SLP_S4#
R1138 0 ns
R1139 0
87213-xxx0x-x
Aces
+VDC
+V3.3AUX
lac_P_R R283 20K
PWRSWVCC_MBXP 30,32
PWR_LED-
SLP_LED-
Wafer6P10
PWRBTN_CN
hws6_1p0r
27 PWR_LED
BT_R16 1K R0402
BT_Q4 2N7002K SOT23
BT_R17 1uF/10V,X5R R0402
BT_Q5 2N7002K SOT23 ns
BT_R18 1K R0402 ns
BT_R19 1uF/10V,X5R R0402 ns
SLP_LED 27
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+V5S
+V3.3S
+V5S 14,15,16,17,18,19,20,21,25,26,28,29,35,36,37,38
+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,22,24,25,27,28,29,34,35,36,37,38,48

C16619

SATA1
13 SATA_TXP0
13 SATA_TXN0
13 SATA_RXN0
13 SATA_RXP0
C298 0.01uF/25V,X7R
C299 0.01uF/25V,X7R
T1 ns V3.3_SATA
V_HDD0
S2 TX
S3 TX#
S5 RX#
S6 RX
P1 VCC3_0
P2 VCC3_1
P3 VCC3_2
P7 VCC5_0
P8 VCC5_1
P9 VCC5_2
P11 RESVE
P13 VCC12_0
P14 VCC12_1
P15 VCC12_2
GND0 GND1 GND2 GND3 GND4 GND5 GND6 GND7
S1 S4 S7 P4 P5 P6 P10 P12
NC0 NC1 1 2
SATACN
SATA22R_REV

+V5S
FB24
Average 1A,Peak 1.5A
V_HDD0
100ohm/100MHz,3A
FB0603
C300 4.7uF/10V,X5R C0603
C301 4.7uF/10V,X5R C0603
C302 0.1uF/16V,X7R C0402
C303 0.1uF/16V,X7R C0402

VerB: ADD HDD2 Option

FFC 1x10
SATA2
ns
SATA_TXP R721 0 ns
SATA_TXN R722 0 ns
SATA_RXN1 C420 0.01uF/25V,X7R ns
SATA_RXP1 C425 0.01uF/25V,X7R ns
V_HDD1
10 9 8 7 6 5 4 3 2 1
10 9 8 12 7 6 5 4 3 11 2 1
12 11
fpce10_1p0r

ACES 88502

+V5S
FB25
Average 1A,Peak 1.8A
V_HDD1
100ohm/100MHz,3A
FB0603
C304 4.7uF/10V,X5R C0603
C305 4.7uF/10V,X5R C0603
C306 0.1uF/16V,X7R C0402
C307 0.1uF/16V,X7R C0402

ODDCN1
13 SATA_TXP1
13 SATA_TXN1
13 SATA_RXN1
13 SATA_RXP1
R723 0
R724 0
C308 0.01uF/25V,X7R
C309 0.01uF/25V,X7R
T2 ns Device_present
V_HDD1
S2 TX
S3 TX#
S5 RX#
S6 RX
P1 DP
P2 VCC5_1
P3 VCC5_2
1 NC0
GND0 GND1 GND2 MD GND4 GND5 NC1
S1 S4 S7 P4 P5 P6 2
ODD_SATA CONN
SATAS13RIN_REV

LN21133-D407-9F

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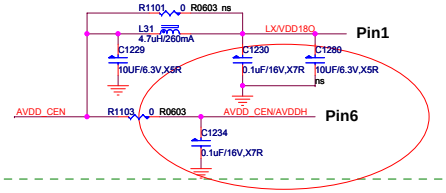
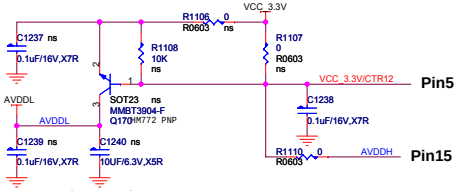
AR8131/M, 8121 GigaBit Lan
AR8132/M, 8114 10M/100M Lan

Close to U26

For AR8131/M, 8132/M: remove R348, C325. C337=0.1uF
For AR8121/8114: remove L9, C306, R322. C337=1uF. C325 close to Pin1





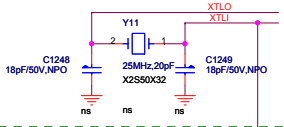
For AR8131/M, 8132/M:
option1: remove R328, R327, R349, R334, C302, C342, C311, Q7.
option2: remove R328, R327, R349, R339, C302, C342, C311, Q7.

For AR8121/8114: remove C320, R339
Q7 close to Pin8

Clock Resource

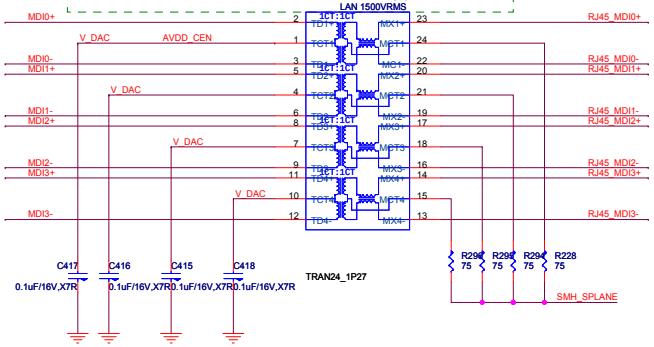
For AR8121/8114 : Remove R336
For AR8131/M, 8132/M Input 25M: Remove R336, C339
For AR8131/M, 8132/M Input 48M: Stuff R336. Remove C339

25MHz Crystal



External clock

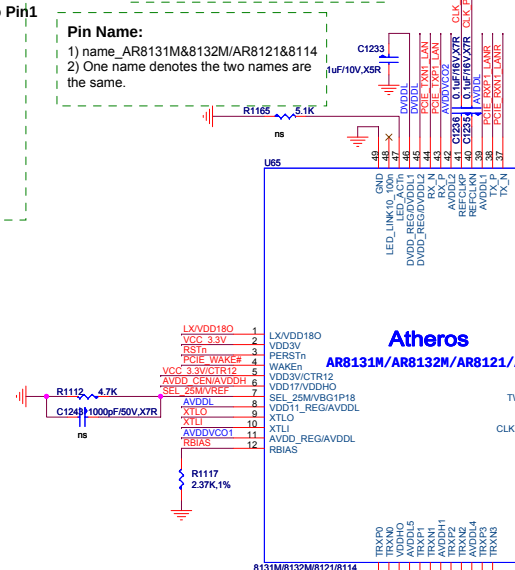
For AR8121/8114 : Remove C322
For AR8131/M, 8132/M intertnal clock: Remove C322
For AR8131/M, 8132/M external clock: Remove Y4, C687, C688
If the external clock is swing from 0 to 0.8V, EXT_25/48 can be connected to XTLI directly.



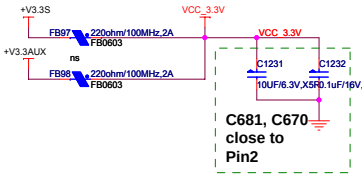
For AR8131/M, 8132/M: C675=1uF
For AR8121/8114: C675=0.1uF

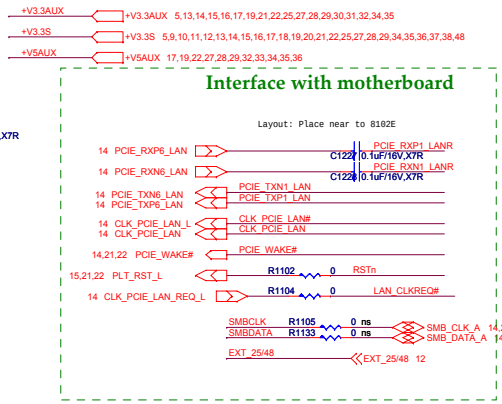
Pin Name:

1) name_AR8131M&8132M/AR8121&8114
2) One name denotes the two names are the same.



C683 close to Pin30
For AR8131/8132: Remove C683

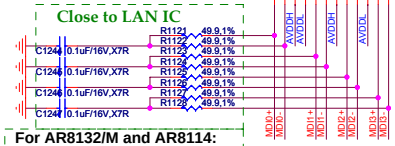




For AR8121/8114: Remove R335
CLKREQn/PNP_PWR_SEL R1109 0 LAN_CLKREQ#

For AR8121/8114: Pin27 power-on strapping (internal pull- up for input)
If R341 and R343 are removed, Q1 collector connects 3.3V and remove R327.
If R341 is removed ,and R343 is stuffed, Q1 collector connects 1.8V and remove R328.

Close to LAN IC



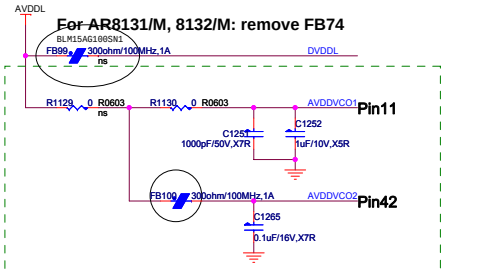
For AR8132/M and AR8114:
R549,R550,R551,R554,C731 and C732 can be removed.

R6,R8,R13 and R14 are pull-up resistors, which might not be necessary due to existence on motherboard.

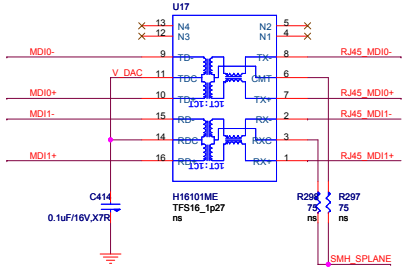
C684, C685 close to Pin8

For AR8131M/8132M: R340=0 ohm. Remove U12, C301, R344.
For AR8131/8132 eeprom application, reserve TWSI circuit.

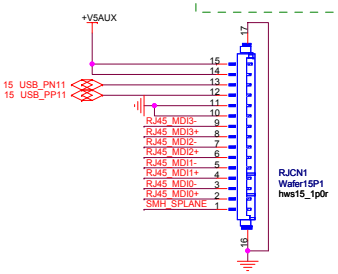
Pin6 AVDD_CEN/AVDDH R1120 0 R0603 ns AVDDH
For AR8131/M, AR8132/M: Remove R342



If overclocking, R332, FB75 stuffed and R330 removed.
If not overclocking, R330, FB75 stuffed and R332 removed.
For AR8131/M, AR8132/M: FB75 can be 0 ohm



87213-xxx0x-x
ACES



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Title: LAN
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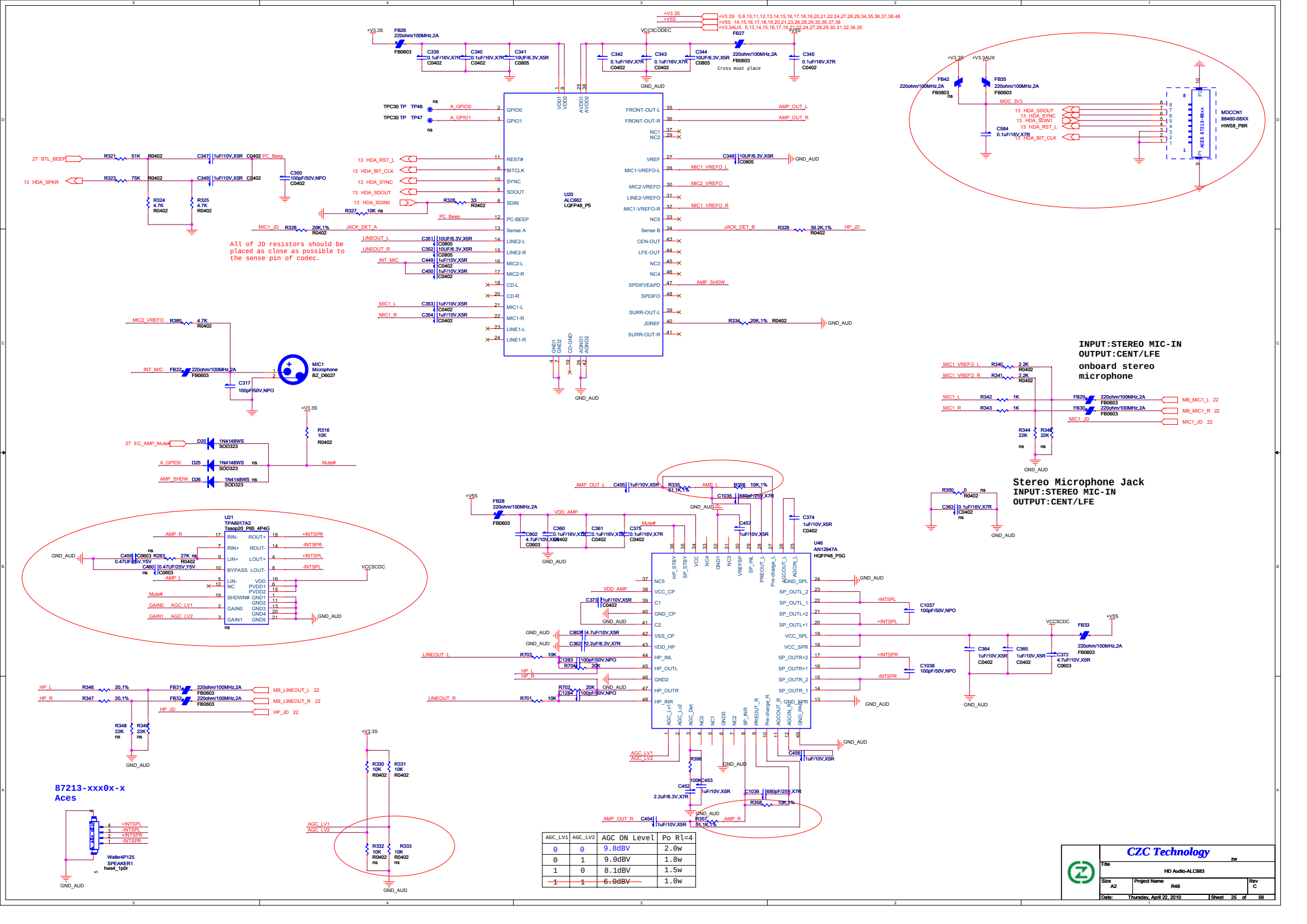
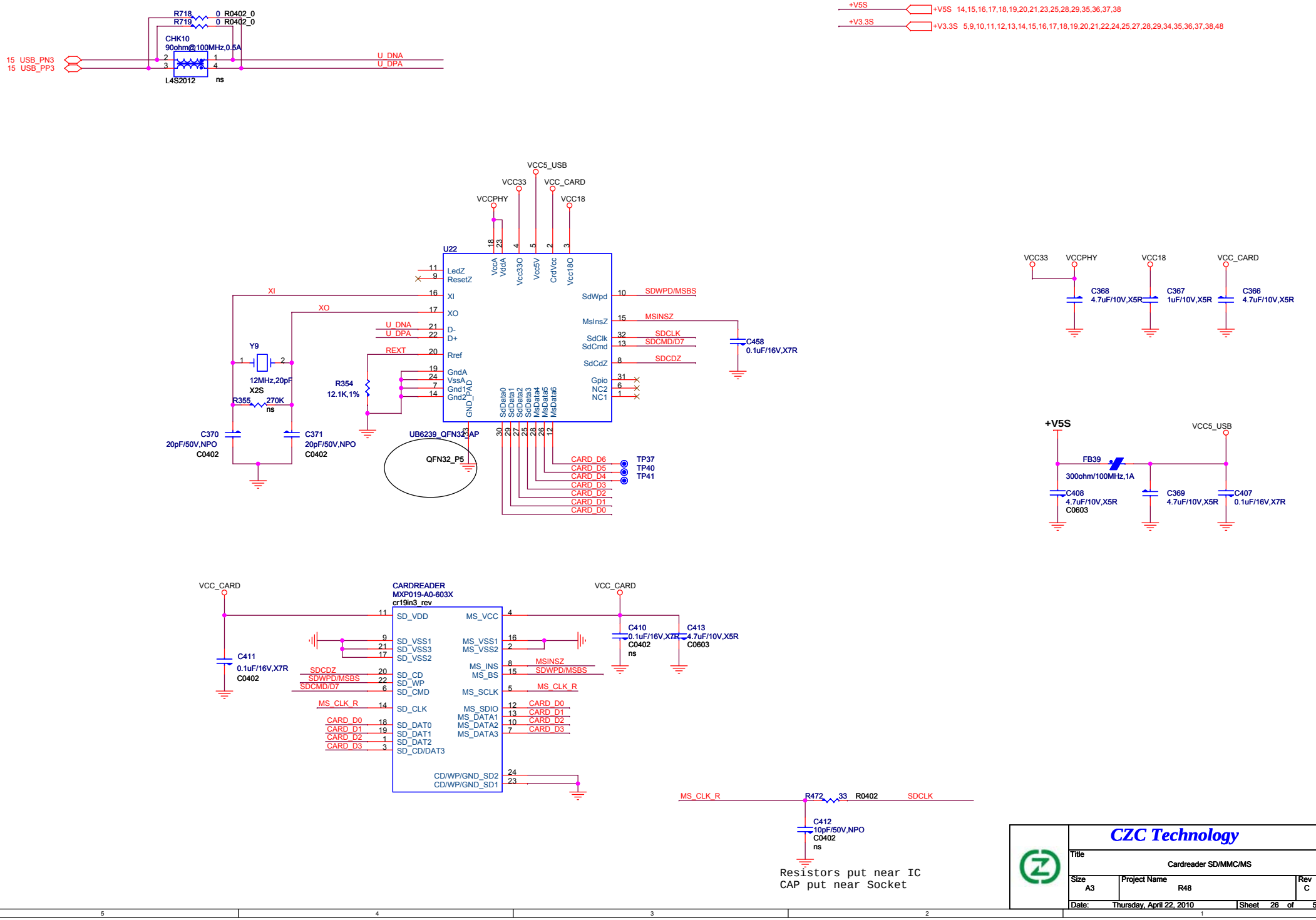


AGC_LV1	AGC_LV2	AGC ON Level	Po Rl=4
0	0	9.8dBV	2.0w
0	1	9.0dBV	1.8w
1	0	8.1dBV	1.5w
1	1	6.0dBV	1.0w

CZC Technology		zw
Title	HD Audio-ALC883	
Size: A2	Project Name: R48	Rev: C
Date: Thursday, April 22, 2010	Sheet 25 of 58	


R718 0 R0402_0
R719 0 R0402_0
CHK10
90ohm@100MHz,0.5A
15 USB_PN3
15 USB_PP3
U_DNA
U_DPA
L4S2012
ns
+V5S
+V5S 14,15,16,17,18,19,20,21,23,25,28,29,35,36,37,38
+V3.3S
+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,22,24,25,27,28,29,34,35,36,37,38,48
VCC5_USB
VCC33
VCC_CARD
VCCPHY
VCC18
U22
LedZ
ResetZ
XI
XO
U_DNA
U_DPA
REXT
Y9
12MHz,20pF
X2S
R355 270K
ns
R354
12.1K,1%
C370
20pF/50V,NPO
C0402
C371
20pF/50V,NPO
C0402
UB6239_QFN32AP
QFN32_P5
SdWpd
MsInsZ
SdClk
SdCmd
SdCdZ
Gpio
NC2
NC1
SDWPD/MSBS
MSINSZ
SDCLK
SDCMD/D7
SDCDZ
C458
0.1uF/16V,X7R
SdData0
SdData1
SdData2
SdData3
MsData4
MsData5
MsData6
CARD_D6
CARD_D5
CARD_D4
CARD_D3
CARD_D2
CARD_D1
CARD_D0
TP37
TP40
TP41
C368
4.7uF/10V,X5R
C367
1uF/10V,X5R
C366
4.7uF/10V,X5R
+V5S
FB39
300ohm/100MHz,1A
C408
4.7uF/10V,X5R
C0603
C369
4.7uF/10V,X5R
C407
0.1uF/16V,X7R
CARDREADER
MXP019-A0-603X
cr19in3_rev
SD_VDD
SD_VSS1
SD_VSS3
SD_VSS2
SD_CD
SD_WP
SD_CMD
SD_CLK
SD_DAT0
SD_DAT1
SD_DAT2
SD_CD/DAT3
MS_VCC
MS_VSS1
MS_VSS2
MS_INS
MS_BS
MS_SCLK
MS_SDIO
MS_DATA1
MS_DATA2
MS_DATA3
CD/WP/GND_SD2
CD/WP/GND_SD1
C411
0.1uF/16V,X7R
C0402
C410
0.1uF/16V,X7R
C0402
ns
C413
4.7uF/10V,X5R
C0603
MS_CLK_R
R472 33 R0402
SDCLK
C412
10pF/50V,NPO
C0402
ns
Resistors put near IC
CAP put near Socket
CZC Technology
Title
Cardreader SD/MMC/MS
Size A3
Project Name R48
Rev C
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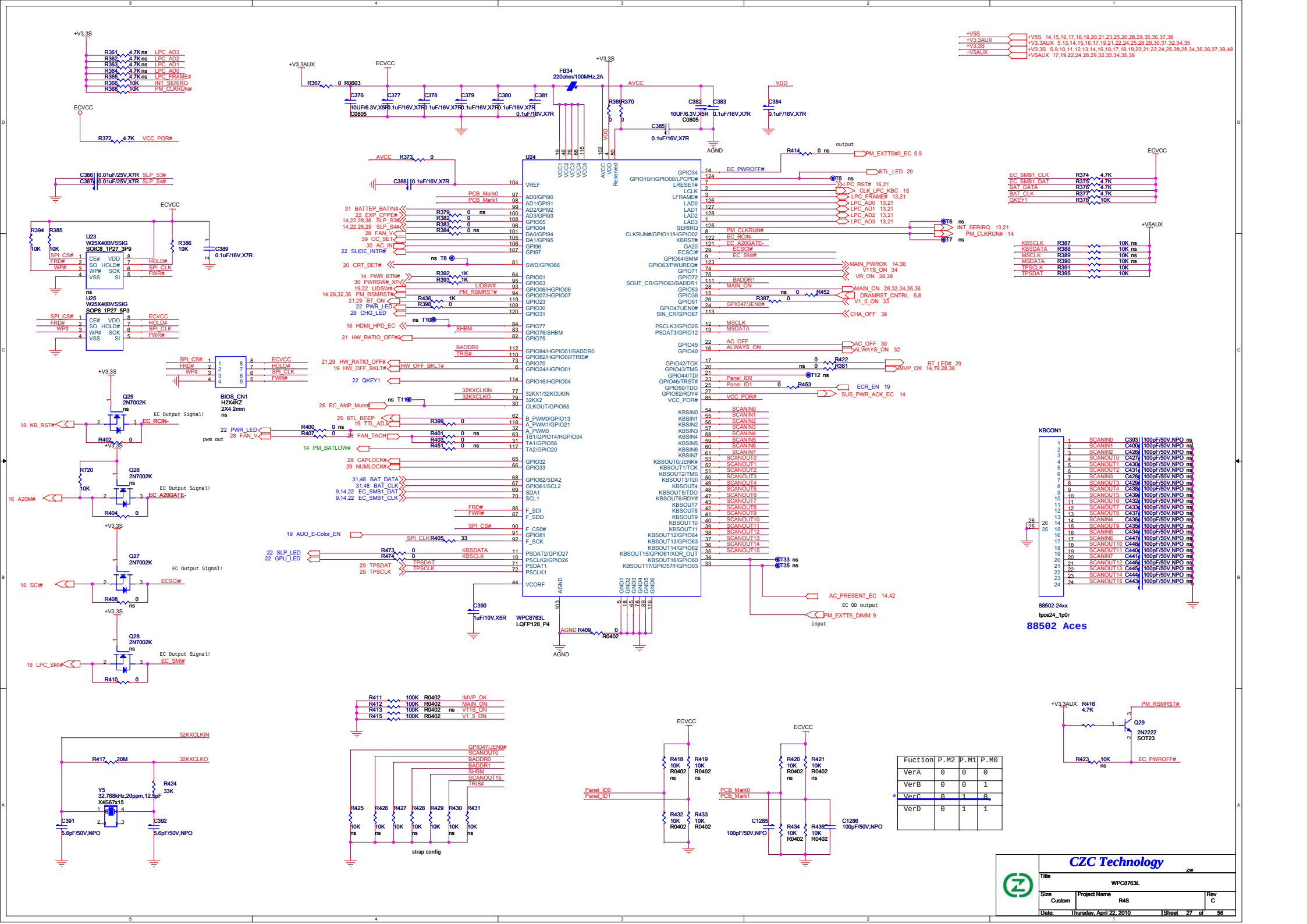
U24
WPC8763L
LQFP128_P4
U23
W25X40BVSSIG
SOIC8_1P27_3P9
U25
W25X40BVSSIG
SOP8_1P27_5P3
BIOS_CN1
H2X4KZ
2X4 2mm
KBCON1
88502-24xx
fpce24_1p0r
88502 Aces
strap config
Y5
32.768kHz,20ppm,12.5pF
X4S67x15
Fuction | P.M2 | P.M1 | P.M0
VerA | 0 | 0 | 0
VerB | 0 | 0 | 1
VerC | 0 | 1 | 0
VerD | 0 | 1 | 1
CZC Technology
zw
WPC8763L
Custom
R48
C
Thursday, April 22, 2010
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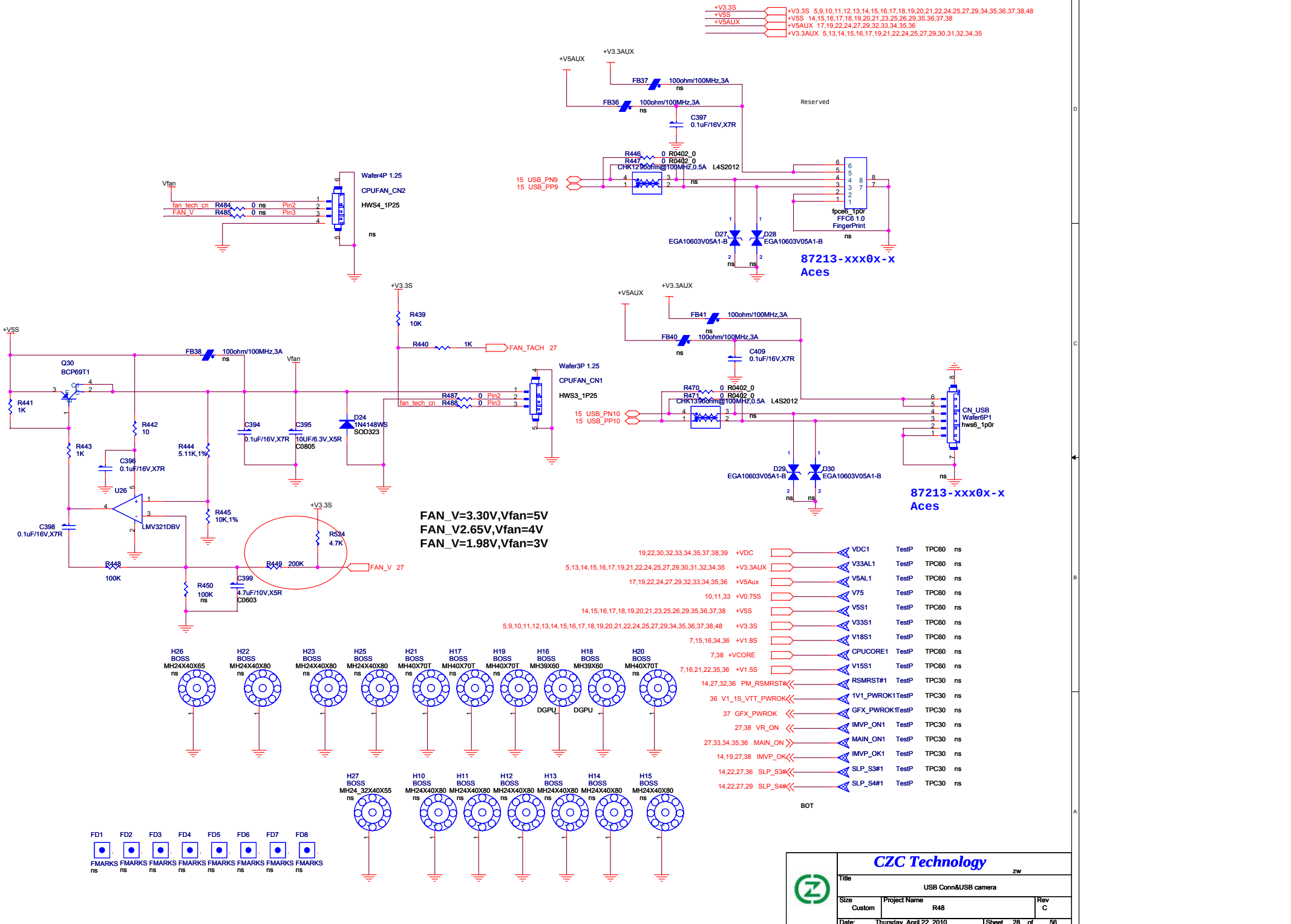
+V3.3S +V5S +V5AUX
+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,22,24,25,27,29,34,35,36,37,38,48
+V5S 14,15,16,17,18,19,20,21,23,25,26,29,35,36,37,38
+V5AUX 17,19,22,24,27,29,32,33,34,35,36
+V3.3AUX 5,13,14,15,16,17,19,21,22,24,25,27,29,30,31,32,34,35
+V5AUX
+V3.3AUX
FB37 100ohm/100MHz,3A
FB36 100ohm/100MHz,3A
Reserved
C397 0.1uF/16V,X7R
R446 0 R0402_0
R447 0 R0402_0
CHK1290ohm@100MHz,0.5A L4S2012
15 USB_PN9
15 USB_PP9
fpce6_1p0r
FFC6 1.0
FingerPrint
D27 EGA10603V05A1-B
D28 EGA10603V05A1-B
87213-xxx0x-x
Aces
Vfan
fan_tech_cn R484 0 ns Pin2
FAN_V R485 0 ns Pin3
Wafer4P 1.25
CPUFAN_CN2
HWS4_1P25
+V3.3S
+V5S
Q30
BCP69T1
FB38 100ohm/100MHz,3A
R439 10K
R440 1K
FAN_TACH 27
R441 1K
R442 10
R443 1K
R444 5.11K,1%
C394 0.1uF/16V,X7R
C395 10UF/6.3V,X5R C0805
C396 0.1uF/16V,X7R
D24 1N4148WS SOD323
R487 0 Pin2
fan_tech_cn R488 0 Pin3
Wafer3P 1.25
CPUFAN_CN1
HWS3_1P25
U26
LMV321DBV
R445 10K,1%
C398 0.1uF/16V,X7R
R448 100K
R450 100K ns
C399 4.7uF/10V,X5R C0603
R524 4.7K
R449 200K
FAN_V 27
FAN_V=3.30V,Vfan=5V
FAN_V2.65V,Fan=4V
FAN_V=1.98V,Vfan=3V
FB41 100ohm/100MHz,3A
FB40 100ohm/100MHz,3A
C409 0.1uF/16V,X7R
R470 0 R0402_0
R471 0 R0402_0
CHK1390ohm@100MHz,0.5A L4S2012
15 USB_PN10
15 USB_PP10
CN_USB
Wafer6P1
hws6_1p0r
D29 EGA10603V05A1-B
D30 EGA10603V05A1-B
87213-xxx0x-x
Aces
19,22,30,32,33,34,35,37,38,39 +VDC
5,13,14,15,16,17,19,21,22,24,25,27,29,30,31,32,34,35 +V3.3AUX
17,19,22,24,27,29,32,33,34,35,36 +V5Aux
10,11,33 +V0.75S
14,15,16,17,18,19,20,21,23,25,26,29,35,36,37,38 +V5S
5,9,10,11,12,13,14,15,16,17,18,19,20,21,22,24,25,27,29,34,35,36,37,38,48 +V3.3S
7,15,16,34,36 +V1.8S
7,38 +VCORE
7,16,21,22,35,36 +V1.5S
14,27,32,36 PM_RSMRST#
36 V1_1S_VTT_PWROK
37 GFX_PWROK
27,38 VR_ON
27,33,34,35,36 MAIN_ON
14,19,27,38 IMVP_OK
14,22,27,36 SLP_S3#
14,22,27,29 SLP_S4#
VDC1 TestP TPC60 ns
V33AL1 TestP TPC60 ns
V5AL1 TestP TPC60 ns
V75 TestP TPC60 ns
V5S1 TestP TPC60 ns
V33S1 TestP TPC60 ns
V18S1 TestP TPC60 ns
CPUCORE1 TestP TPC60 ns
V15S1 TestP TPC60 ns
RSMRST#1 TestP TPC30 ns
1V1_PWROK1 TestP TPC30 ns
GFX_PWROK1 TestP TPC30 ns
IMVP_ON1 TestP TPC30 ns
MAIN_ON1 TestP TPC30 ns
IMVP_OK1 TestP TPC30 ns
SLP_S3#1 TestP TPC30 ns
SLP_S4#1 TestP TPC30 ns
BOT
H26 BOSS MH24X40X65 ns
H22 BOSS MH24X40X80 ns
H23 BOSS MH24X40X80 ns
H25 BOSS MH24X40X80 ns
H21 BOSS MH40X70T ns
H17 BOSS MH40X70T ns
H19 BOSS MH40X70T ns
H16 BOSS MH39X60 ns
H18 BOSS MH39X60 ns
H20 BOSS MH40X70T ns
DGPU
DGPU
H27 BOSS MH24_32X40X55 ns
H10 BOSS MH24X40X80 ns
H11 BOSS MH24X40X80 ns
H12 BOSS MH24X40X80 ns
H13 BOSS MH24X40X80 ns
H14 BOSS MH24X40X80 ns
H15 BOSS MH24X40X80 ns
FD1 FMARKS ns
FD2 FMARKS ns
FD3 FMARKS ns
FD4 FMARKS ns
FD5 FMARKS ns
FD6 FMARKS ns
FD7 FMARKS ns
FD8 FMARKS ns
CZC Technology
zw
Title
USB Conn&USB camera
Size Custom
Project Name R48
Rev C
Date: Thursday, April 22, 2010
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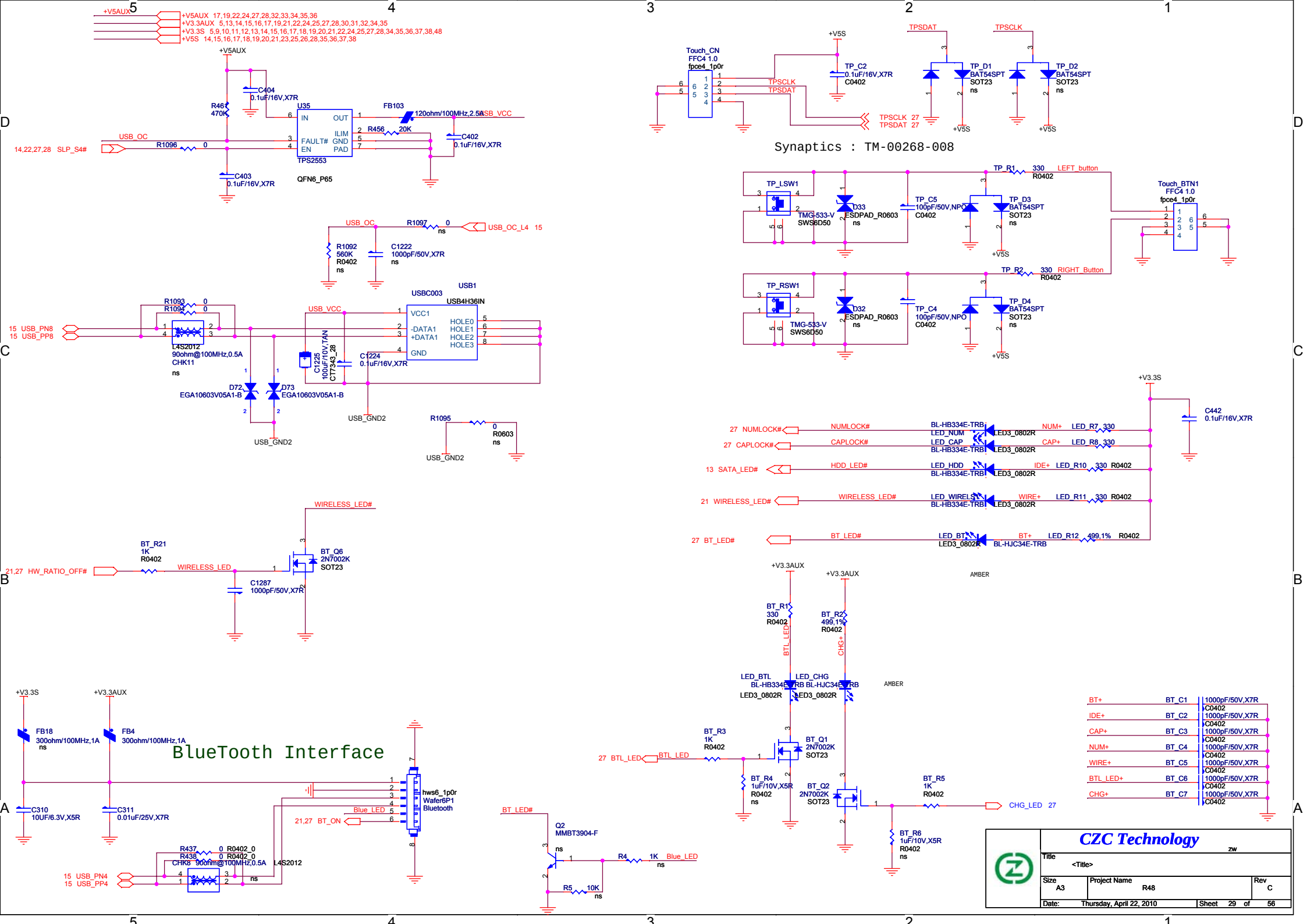
+V5AUX 17,19,22,24,27,28,32,33,34,35,36
+V3.3AUX 5,13,14,15,16,17,19,21,22,24,25,27,28,30,31,32,34,35
+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,22,24,25,27,28,34,35,36,37,38,48
+V5S 14,15,16,17,18,19,20,21,23,25,26,28,35,36,37,38
+V5AUX
C404 0.1uF/16V,X7R
R467 470K
U35
IN OUT
FAULT# ILIM
EN GND
PAD
TPS2553
QFN6_P65
FB103 120ohm/100MHz,2.5A
R456 20K
C402 0.1uF/16V,X7R
C403 0.1uF/16V,X7R
USB_OC
R1096 0
14,22,27,28 SLP_S4#
USB_VCC
USB_OC
R1097 0 ns
USB_OC_L4 15
R1092 560K R0402 ns
C1222 1000pF/50V,X7R ns
USB1
USBC003
USB4H36IN
VCC1
-DATA1
+DATA1
GND
HOLE0
HOLE1
HOLE2
HOLE3
R1093 0
R1094 0
15 USB_PN8
15 USB_PP8
L4S2012
90ohm@100MHz,0.5A
CHK11
ns
C1225 100uF/10V,TAN C7343_28
C1224 0.1uF/16V,X7R
D72 EGA10603V05A1-B
D73 EGA10603V05A1-B
USB_GND2
R1095 0 R0603 ns
WIRELESS_LED#
BT_R21 1K R0402
21,27 HW_RATIO_OFF#
WIRELESS_LED
BT_Q6 2N7002K SOT23
C1287 1000pF/50V,X7R
+V3.3S
+V3.3AUX
FB18 300ohm/100MHz,1A ns
FB4 300ohm/100MHz,1A
BlueTooth Interface
C310 10UF/6.3V,X5R
C311 0.01uF/25V,X7R
hws6_1p0r Wafer6P1 Bluetooth
Blue_LED
21,27 BT_ON
R437 0 R0402_0
R438 0 R0402_0
CHK8 90ohm@100MHz,0.5A
L4S2012
ns
15 USB_PN4
15 USB_PP4
Touch_CN FFC4 1.0 fpce4_1p0r
TPSCLK
TPSDAT
TP_C2 0.1uF/16V,X7R C0402
TP_D1 BAT54SPT SOT23 ns
TP_D2 BAT54SPT SOT23 ns
TPSCLK 27
TPSDAT 27
+V5S
Synaptics : TM-00268-008
TP_LSW1
TMG-533-V SWS6D50
D33 ESDPAD_R0603 ns
TP_C5 100pF/50V,NPO C0402
TP_D3 BAT54SPT SOT23 ns
TP_R1 330 R0402
LEFT_button
TP_RSW1
D32 ESDPAD_R0603 ns
TP_C4 100pF/50V,NPO C0402
TP_D4 BAT54SPT SOT23 ns
TP_R2 330 R0402
RIGHT_Button
Touch_BTN1 FFC4 1.0 fpce4_1p0r
+V3.3S
C442 0.1uF/16V,X7R
27 NUMLOCK#
NUMLOCK#
BL-HB334E-TRB
LED_NUM
LED3_0802R
NUM+
LED_R7 330
27 CAPLOCK#
CAPLOCK#
LED_CAP
CAP+
LED_R8 330
13 SATA_LED#
HDD_LED#
LED_HDD
IDE+
LED_R10 330 R0402
21 WIRELESS_LED#
WIRELESS_LED#
LED_WIRELESS
WIRE+
LED_R11 330 R0402
27 BT_LED#
BT_LED#
LED_BT
BT+
LED_R12 499,1% R0402
BL-HJC34E-TRB
+V3.3AUX
AMBER
BT_R1 330 R0402
BT_R2 499,1% R0402
BTL_LED
CHG+
LED_BTL
LED_CHG
BL-HJC34E-TRB
27 BTL_LED
BT_R3 1K R0402
BT_Q1 2N7002K SOT23
BT_R4 1uF/10V,X5R R0402 ns
BT_Q2 2N7002K SOT23
BT_R5 1K R0402
BT_R6 1uF/10V,X5R R0402 ns
CHG_LED 27
BT_LED#
Q2 MMBT3904-F
R4 1K Blue_LED ns
R5 10K ns
BT+ BT_C1 1000pF/50V,X7R C0402
IDE+ BT_C2 1000pF/50V,X7R C0402
CAP+ BT_C3 1000pF/50V,X7R C0402
NUM+ BT_C4 1000pF/50V,X7R C0402
WIRE+ BT_C5 1000pF/50V,X7R C0402
BTL_LED+ BT_C6 1000pF/50V,X7R C0402
CHG+ BT_C7 1000pF/50V,X7R C0402
CZC Technology
zw
Title
<Title>
Size A3
Project Name R48
Rev C
Date: Thursday, April 22, 2010
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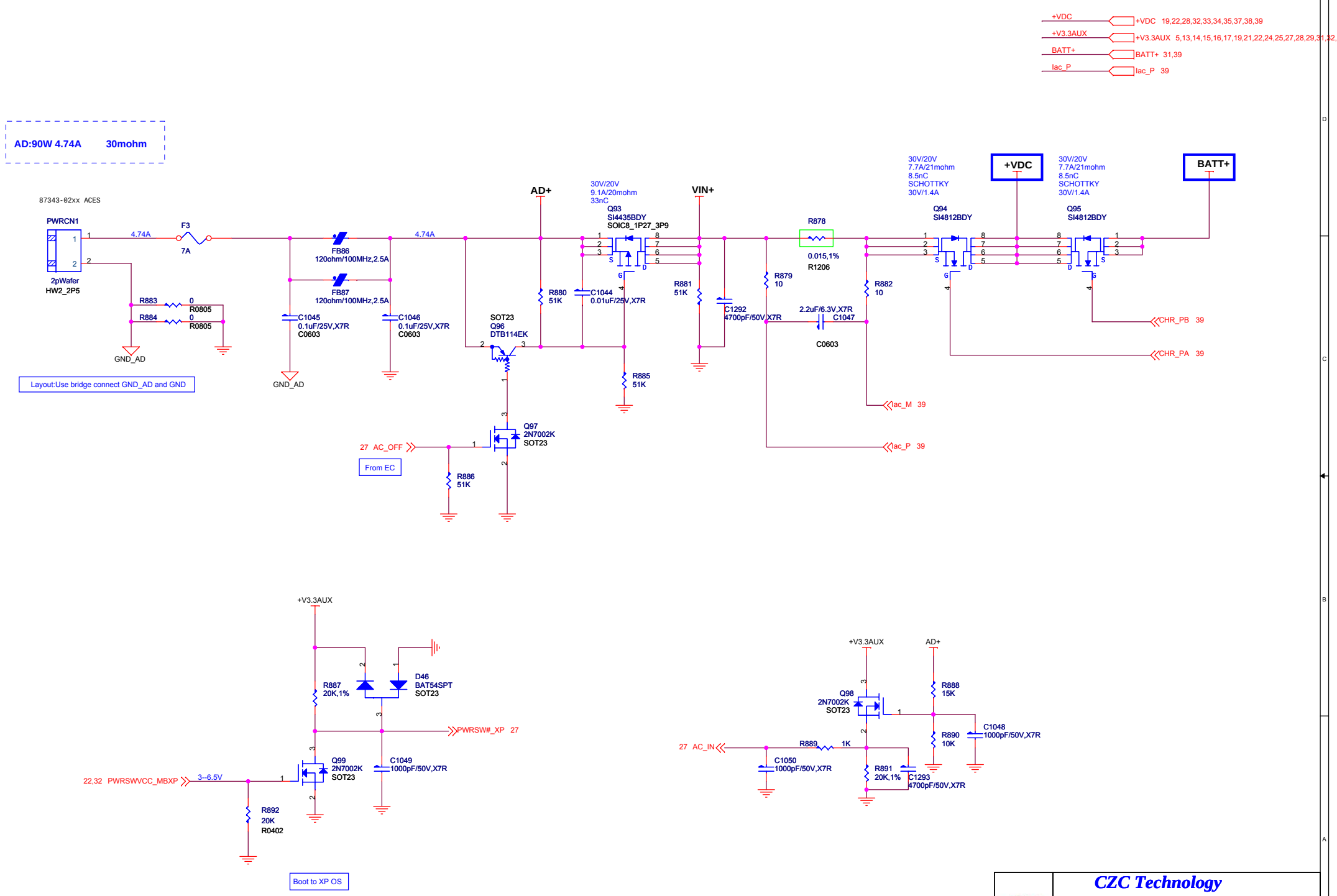

CZC Technology

Title		
Size A3	Project Name R48	Rev C
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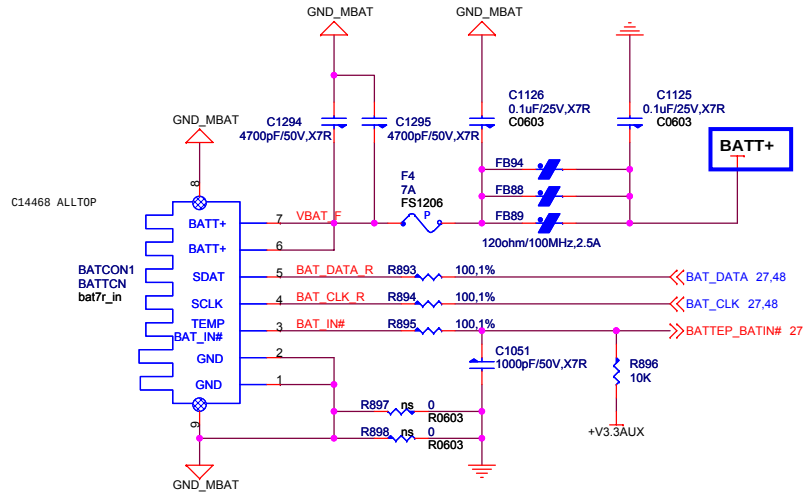
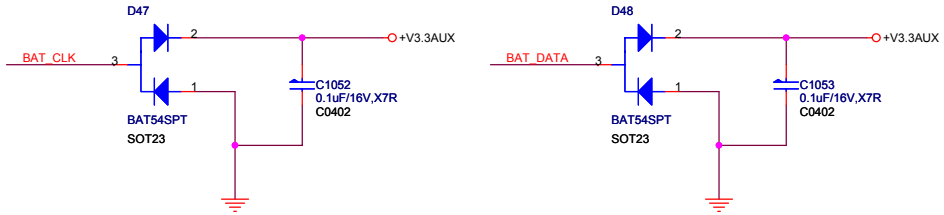
BATT+ BATT+ 30,39

+V3.3AUX +V3.3AUX 5,13,14,15,16,17,19,21,22,24,25,27,28,29,30,32,34

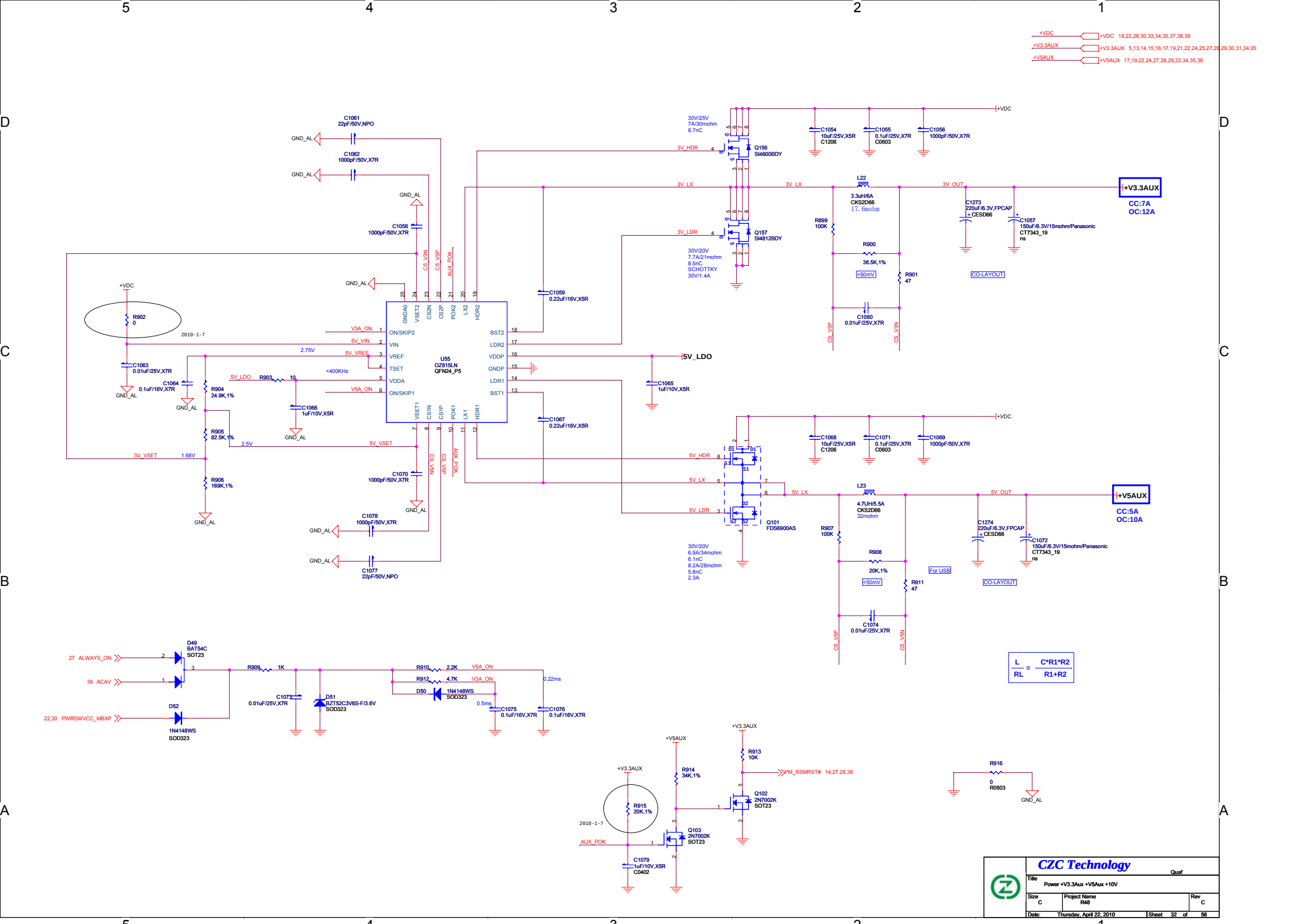


BATTEP_BATIN#	
0.5-2.5V	Battery OK
<0.5V or >2.5V	Battery Fail

Use bridge connect GND_MBAT and GND



CZC Technology			
Title			
Size A3	Project Name R48		Rev C
Date: Thursday, April 22, 2010		Sheet 31 of 56	


+VDC +VDC 19,22,28,30,33,34,35,37,38,39
+V3.3AUX +V3.3AUX 5,13,14,15,16,17,19,21,22,24,25,27,28,29,30,31,34,35
+V5AUX +V5AUX 17,19,22,24,27,28,29,33,34,35,36
C1061 22pF/50V,NPO
C1062 1000pF/50V,X7R
C1058 1000pF/50V,X7R
C1059 0.22uF/16V,X5R
C1063 0.01uF/25V,X7R
C1064 0.1uF/16V,X7R
C1065 1uF/10V,X5R
C1066 1uF/10V,X5R
C1067 0.22uF/16V,X5R
C1070 1000pF/50V,X7R
C1077 22pF/50V,NPO
C1078 1000pF/50V,X7R
R902 0
R903 10
R904 24.9K,1%
R905 82.5K,1%
R906 169K,1%
U55 OZ815LN QFN24_P5
ON/SKIP2
VIN
VREF
TSET
VDDA
ON/SKIP1
BST2
LDR2
VDDP
GNDP
LDR1
BST1
V3A_ON
5V_VIN
5V_VREF
5V_LDO
V5A_ON
3V_VSET
5V_VSET
2.75V
2.5V
1.68V
<400KHz
2010-1-7
30V/25V 7A/30mohm 8.7nC
Q156 SI4800BDY
3V_HDR
3V_LX
3V_LDR
30V/20V 7.7A/21mohm 8.5nC SCHOTTKY 30V/1.4A
Q157 SI4812BDY
C1054 10uF/25V,X5R C1206
C1055 0.1uF/25V,X7R C0603
C1056 1000pF/50V,X7R
L22 3.3uH/6A CKS2D66 17.6mohm
3V_OUT
+V3.3AUX
CC:7A OC:12A
C1273 220uF/6.3V,FPCAP +CESD66
C1057 150uF/6.3V/15mohm/Panasonic CT7343_19 ns
R899 100K
R900 36.5K,1%
R901 47
C1060 0.01uF/25V,X7R
<50mV
CO-LAYOUT
CS_V3P
CS_V3N
30V/20V 6.9A/34mohm 6.1nC 8.2A/28mohm 5.8nC 2.3A
Q101 FDS6900AS
5V_HDR
5V_LX
5V_LDR
C1068 10uF/25V,X5R C1206
C1071 0.1uF/25V,X7R C0603
C1069 1000pF/50V,X7R
L23 4.7UH/5.5A CKS2D66 32mohm
5V_OUT
+V5AUX
CC:5A OC:10A
C1274 220uF/6.3V,FPCAP +CESD66
C1072 150uF/6.3V/15mohm/Panasonic CT7343_19 ns
R907 100K
R908 20K,1%
R911 47
C1074 0.01uF/25V,X7R
For USB
CO-LAYOUT
CS_V5P
CS_V5N
L / RL = C*R1*R2 / R1+R2
27 ALWAYS_ON
39 ACAV
22,30 PWRSWVCC_MBXP
D49 BAT54C SOT23
D52 1N4148WS SOD323
R909 1K
C1073 0.01uF/25V,X7R
D51 BZT52C3V6S-F/3.6V SOD323
R910 2.2K
R912 4.7K
D50 1N4148WS SOD323
V5A_ON
V3A_ON
0.22ms
0.5ms
C1075 0.1uF/16V,X7R
C1076 0.1uF/16V,X7R
R913 10K
R914 34K,1%
R915 20K,1%
Q102 2N7002K SOT23
Q103 2N7002K SOT23
PM_RSMRST# 14,27,28,36
AUX_POK
C1079 1uF/10V,X5R C0402
R916 0 R0603
CZC Technology
Quaf
Power +V3.3Aux +V5Aux +10V
Size C
Project Name R48
Rev C
Date: Thursday, April 22, 2010
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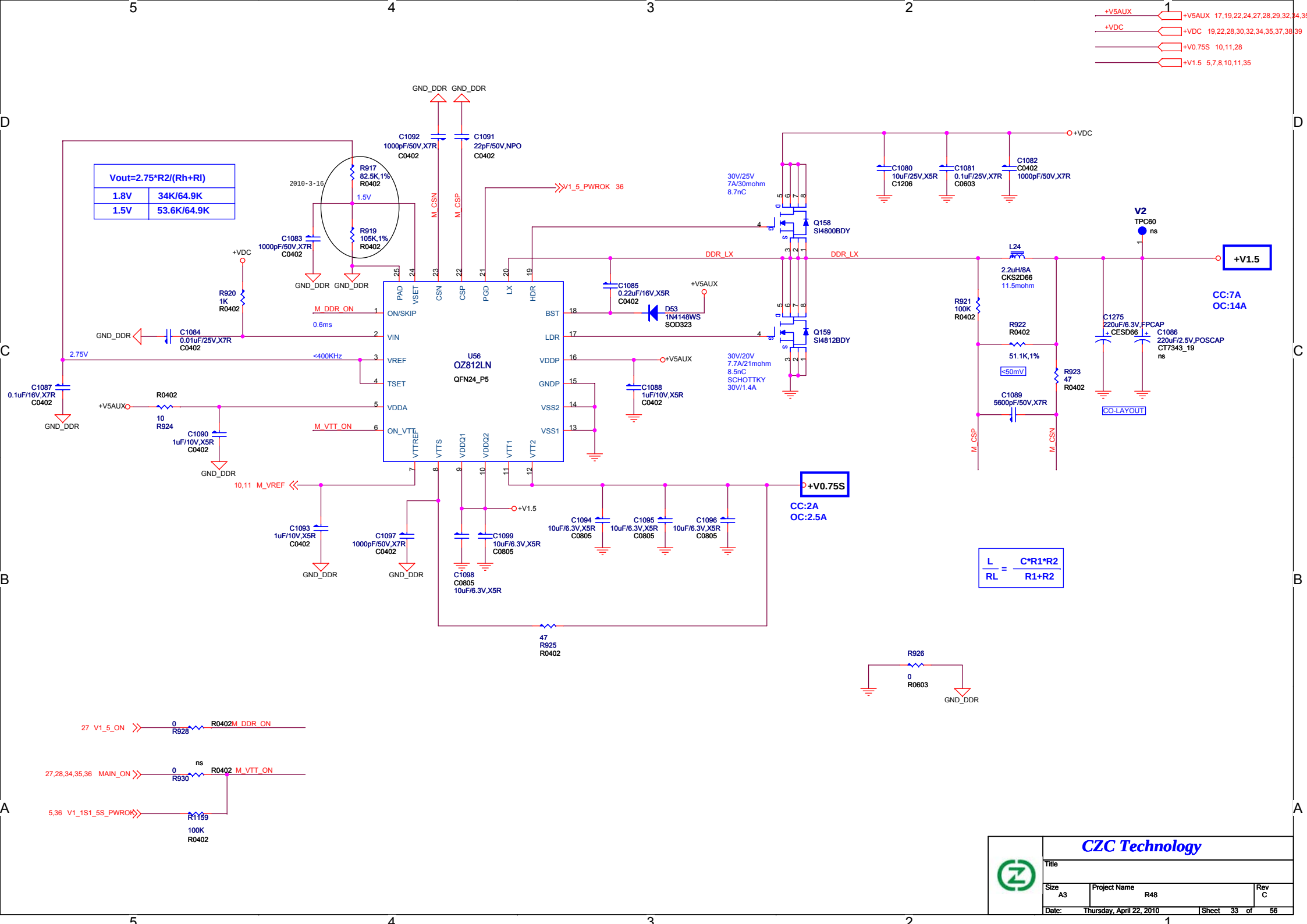
+V5AUX +V5AUX 17,19,22,24,27,28,29,32,34,35
+VDC +VDC 19,22,28,30,32,34,35,37,38,39
+V0.75S 10,11,28
+V1.5 5,7,8,10,11,35
Vout=2.75*R2/(Rh+Rl)
1.8V 34K/64.9K
1.5V 53.6K/64.9K
2010-3-16
R917 82.5K,1% R0402
R919 105K,1% R0402
C1083 1000pF/50V,X7R C0402
C1092 1000pF/50V,X7R C0402
C1091 22pF/50V,NPO C0402
GND_DDR
M_CSN
M_CSP
V1_5_PWROK 36
U56
OZ812LN
QFN24_P5
PAD VSET CSN CSP PGD LX HDR
ON/SKIP VIN VREF TSET VDDA ON_VTT
BST LDR VDDP GNDP VSS2 VSS1
VTTREF VTTS VDDQ1 VDDQ2 VTT1 VTT2
R920 1K R0402
M_DDR_ON
0.6ms
C1084 0.01uF/25V,X7R C0402
2.75V
<400KHz
C1087 0.1uF/16V,X7R C0402
+V5AUX
R0402
10 R924
C1090 1uF/10V,X5R C0402
M_VTT_ON
10,11 M_VREF
C1085 0.22uF/16V,X5R C0402
D53 1N4148WS SOD323
C1088 1uF/10V,X5R C0402
30V/25V 7A/30mohm 8.7nC
Q158 SI4800BDY
30V/20V 7.7A/21mohm 8.5nC SCHOTTKY 30V/1.4A
Q159 SI4812BDY
DDR_LX
C1080 10uF/25V,X5R C1206
C1081 0.1uF/25V,X7R C0603
C1082 C0402 1000pF/50V,X7R
L24 2.2uH/8A CKS2D66 11.5mohm
R921 100K R0402
R922 R0402 51.1K,1%
<50mV
R923 47 R0402
C1089 5600pF/50V,X7R
C1275 220uF/6.3V,FPCAP CESD66
C1086 220uF/2.5V,POSCAP CT7343_19 ns
CO-LAYOUT
V2 TPC60 ns
+V1.5
CC:7A OC:14A
+V0.75S
CC:2A OC:2.5A
C1093 1uF/10V,X5R C0402
C1097 1000pF/50V,X7R C0402
C1098 C0805 10uF/6.3V,X5R
C1099 10uF/6.3V,X5R C0805
C1094 10uF/6.3V,X5R C0805
C1095 10uF/6.3V,X5R C0805
C1096 10uF/6.3V,X5R C0805
47 R925 R0402
L/RL = C*R1*R2/(R1+R2)
R926 0 R0603
27 V1_5_ON
0 R928
R0402 M_DDR_ON
27,28,34,35,36 MAIN_ON
0 R930
ns
R0402 M_VTT_ON
5,36 V1_1S1_5S_PWROK
R1139 100K R0402
CZC Technology
Title
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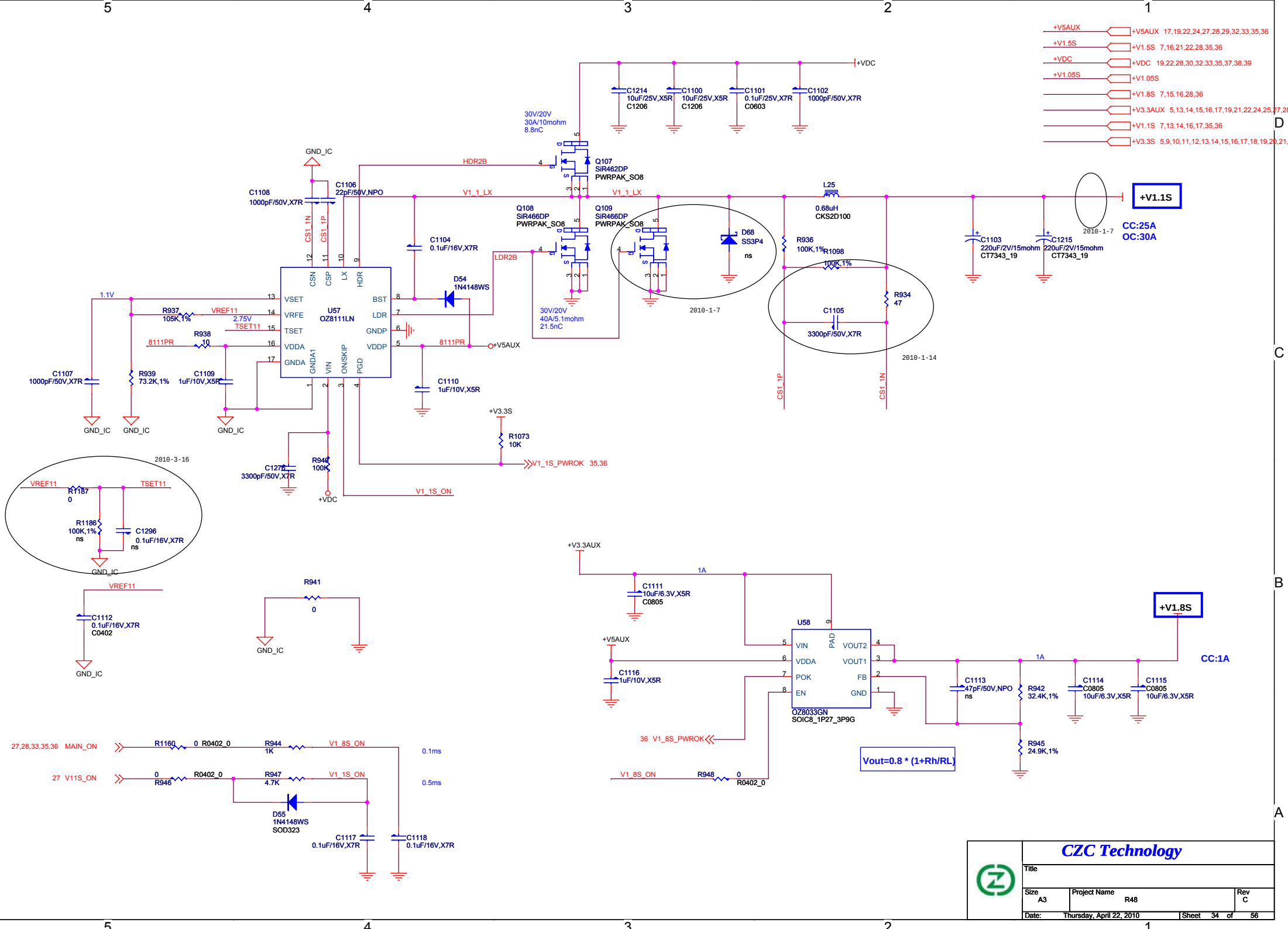

CZC Technology			
Title			
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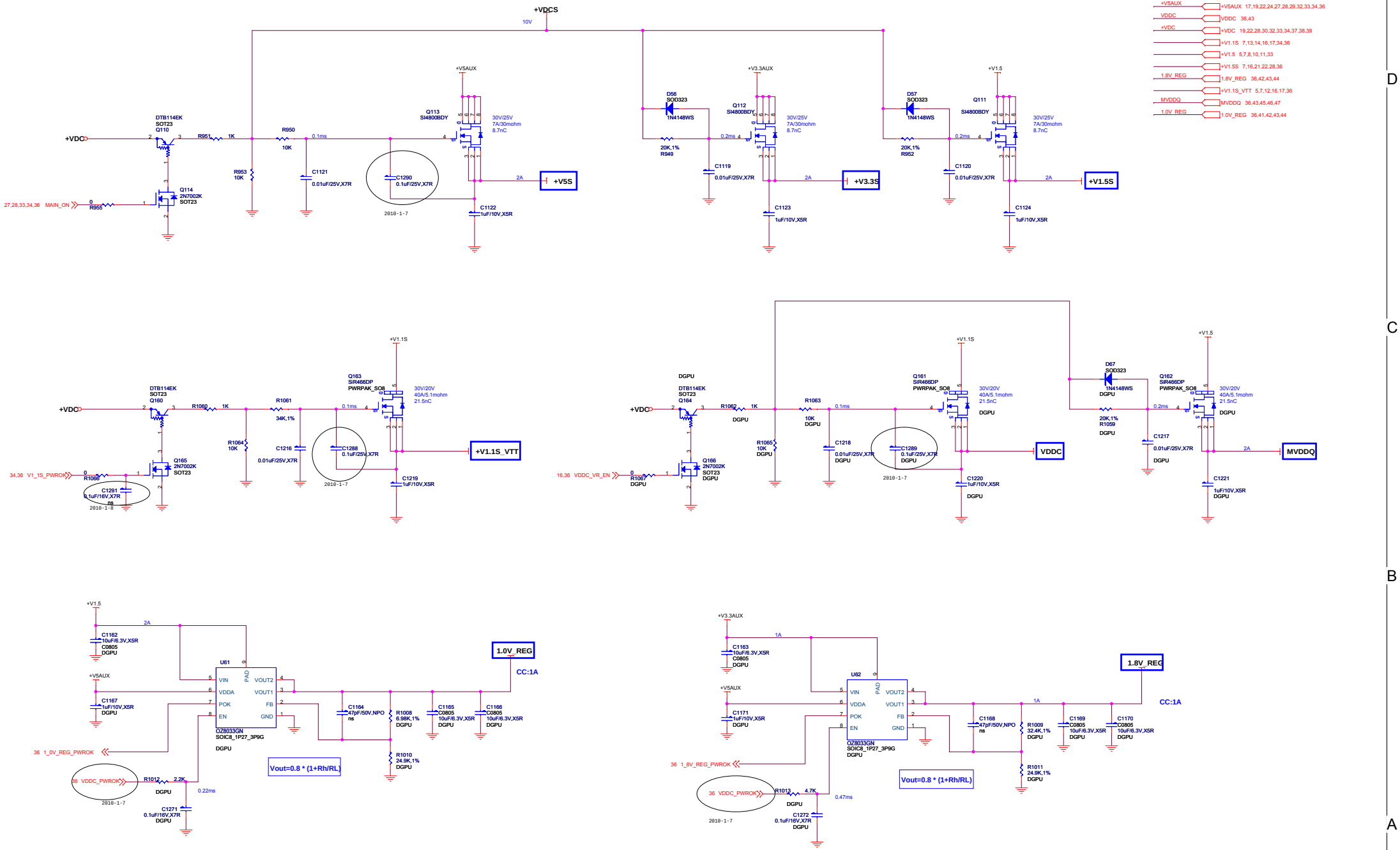
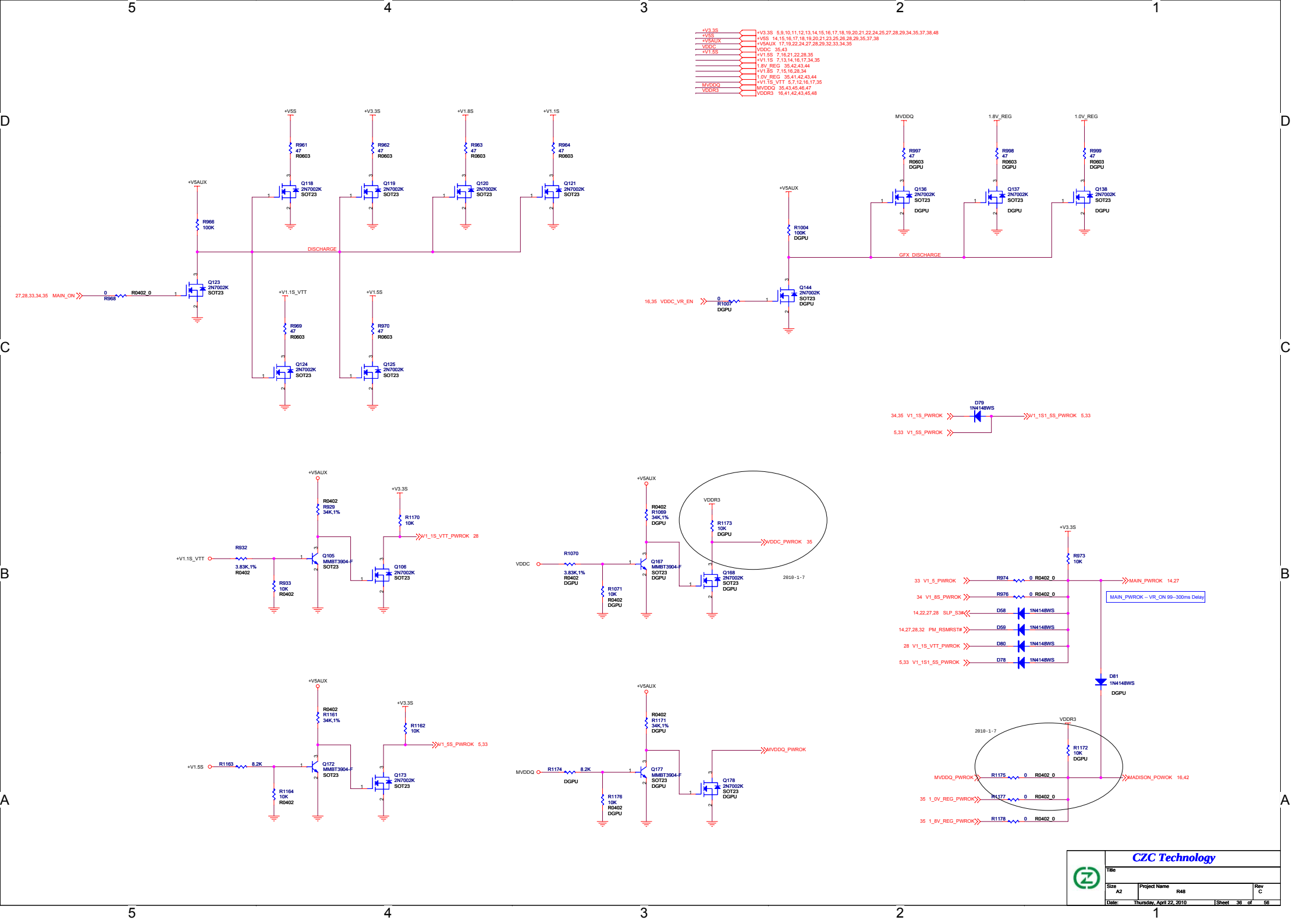


CZC Technology			
Title			
Size: A2	Project Name: R48		Rev: C
Date: Thursday, April 22, 2010		Sheet 35 of 58	


+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,22,24,25,27,28,29,34,35,37,38,48
+V5S 14,15,16,17,18,19,20,21,23,25,26,28,29,35,37,38
+V5AUX 17,19,22,24,27,28,29,32,33,34,35
VDDC 35,43
+V1.5S 7,16,21,22,28,35
+V1.1S 7,13,14,16,17,34,35
1.8V_REG 35,42,43,44
+V1.8S 7,15,16,28,34
1.0V_REG 35,41,42,43,44
+V1.1S_VTT 5,7,12,16,17,35
MVDDQ 35,43,45,46,47
VDDR3 16,41,42,43,45,48
R961 47 R0603
R962 47 R0603
R963 47 R0603
R964 47 R0603
Q118 2N7002K SOT23
Q119 2N7002K SOT23
Q120 2N7002K SOT23
Q121 2N7002K SOT23
R966 100K
Q123 2N7002K SOT23
27,28,33,34,35 MAIN_ON
R968
R0402_0
DISCHARGE
R969 47 R0603
R970 47 R0603
Q124 2N7002K SOT23
Q125 2N7002K SOT23
R997 47 R0603 DGPU
R998 47 R0603 DGPU
R999 47 R0603 DGPU
Q136 2N7002K SOT23 DGPU
Q137 2N7002K SOT23 DGPU
Q138 2N7002K SOT23 DGPU
R1004 100K DGPU
Q144 2N7002K SOT23 DGPU
16,35 VDDC_VR_EN
R1007 DGPU
GFX_DISCHARGE
D79 1N4148WS
34,35 V1_1S_PWROK
5,33 V1_5S_PWROK
V1_1S1_5S_PWROK 5,33
R0402 R929 34K,1%
R1170 10K
R932 3.83K,1% R0402
R933 10K R0402
Q105 MMBT3904-F SOT23
Q106 2N7002K SOT23
V1_1S_VTT_PWROK 28
R0402 R1069 34K,1% DGPU
R1173 10K DGPU
R1070 3.83K,1% R0402 DGPU
R1071 10K R0402 DGPU
Q167 MMBT3904-F SOT23 DGPU
Q168 2N7002K SOT23 DGPU
VDDC_PWROK 35
2010-1-7
R973 10K
R974 0 R0402_0
R976 0 R0402_0
D58 1N4148WS
D59 1N4148WS
D80 1N4148WS
D78 1N4148WS
33 V1_5_PWROK
34 V1_8S_PWROK
14,22,27,28 SLP_S3#
14,27,28,32 PM_RSMRST#
28 V1_1S_VTT_PWROK
5,33 V1_1S1_5S_PWROK
MAIN_PWROK 14,27
MAIN_PWROK -- VR_ON 99--300ms Delay
D81 1N4148WS DGPU
R0402 R1161 34K,1%
R1162 10K
R1163 8.2K
R1164 10K R0402
Q172 MMBT3904-F SOT23
Q173 2N7002K SOT23
V1_5S_PWROK 5,33
R0402 R1171 34K,1% DGPU
R1174 8.2K DGPU
R1176 10K R0402 DGPU
Q177 MMBT3904-F SOT23 DGPU
Q178 2N7002K SOT23 DGPU
MVDDQ_PWROK
R1172 10K DGPU
R1175 0 R0402_0
R1177 0 R0402_0
R1178 0 R0402_0
35 1_0V_REG_PWROK
35 1_8V_REG_PWROK
MADISON_POWOK 16,42
CZC Technology
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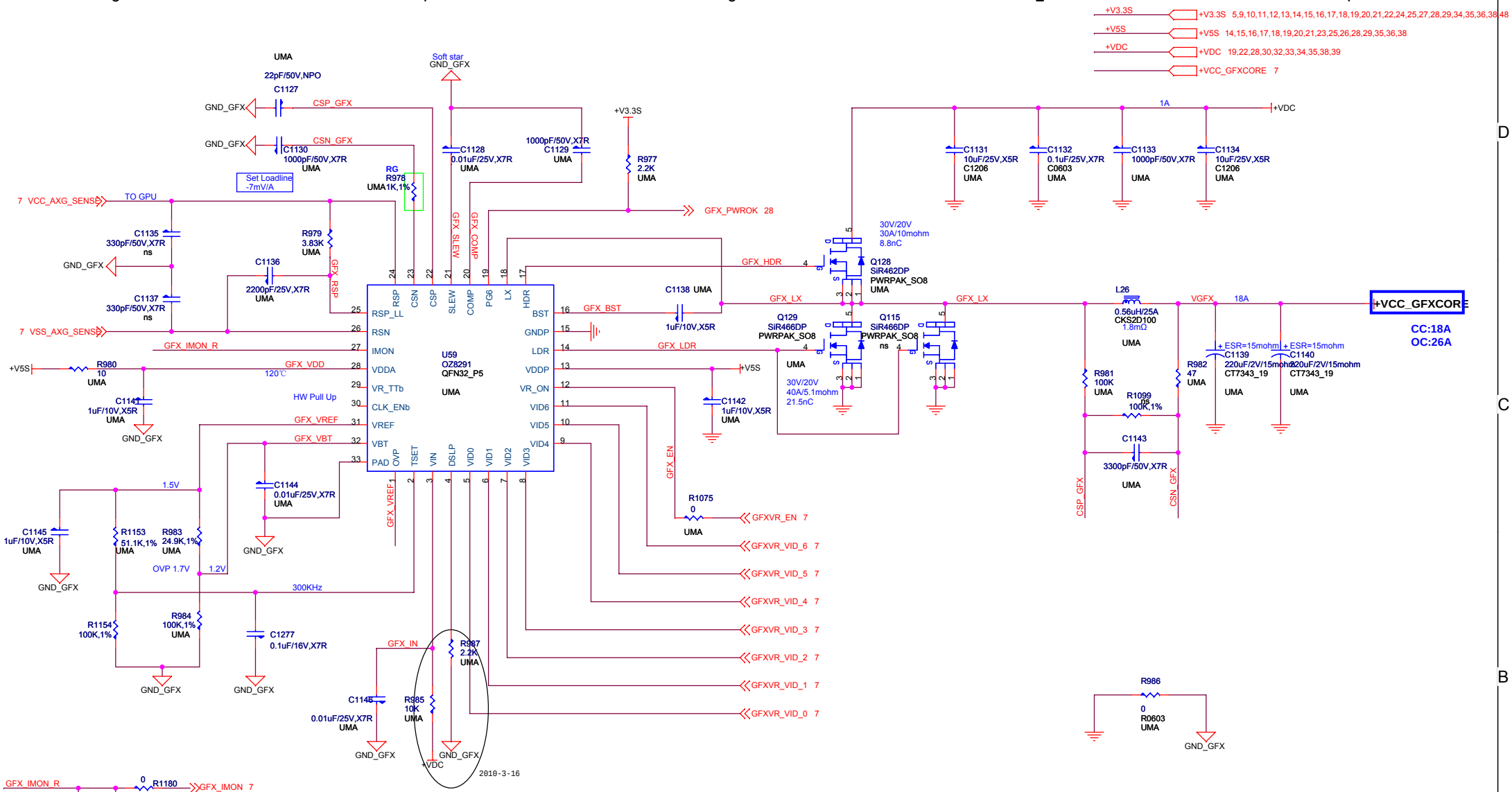

GFX CORE Debug

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vout
0	0	1	1	0	0	0	1.2000V
0	1	1	0	0	0	0	0.9000V

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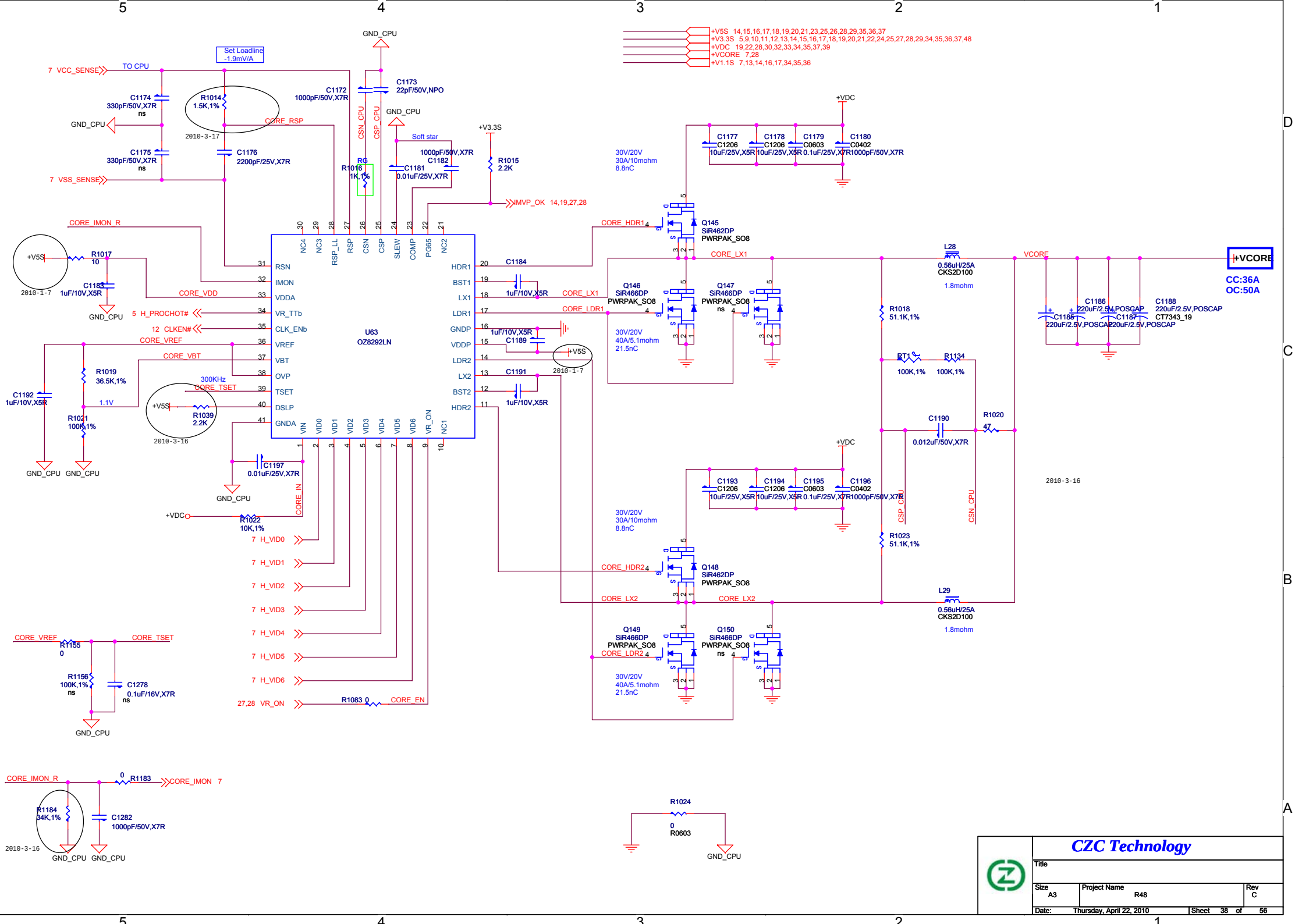
U63
OZ8292LN
Set Loadline
-1.9mV/A
TO CPU
7 VCC_SENSE
7 VSS_SENSE
CORE_RSP
CORE_IMON_R
CORE_VDD
CORE_VREF
CORE_VBT
CORE_TSET
CORE_IN
CORE_LX1
CORE_LX2
CORE_LDR1
CORE_LDR2
CORE_HDR1
CORE_HDR2
CORE_EN
IMVP_OK 14,19,27,28
5 H_PROCHOT#
12 CLKEN#
7 H_VID0
7 H_VID1
7 H_VID2
7 H_VID3
7 H_VID4
7 H_VID5
7 H_VID6
27,28 VR_ON
+V5S
+V3.3S
+VDC
+VCORE
CC:36A
OC:50A
30V/20V
30A/10mohm
8.8nC
30V/20V
40A/5.1mohm
21.5nC
1.8mohm
300KHz
1.1V
2010-1-7
2010-3-16
2010-3-17
GND_CPU
+5S 14,15,16,17,18,19,20,21,23,25,26,28,29,35,36,37
+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,22,24,25,27,28,29,34,35,36,37,48
+VDC 19,22,28,30,32,33,34,35,37,39
+VCORE 7,28
+V1.1S 7,13,14,16,17,34,35,36
CZC Technology
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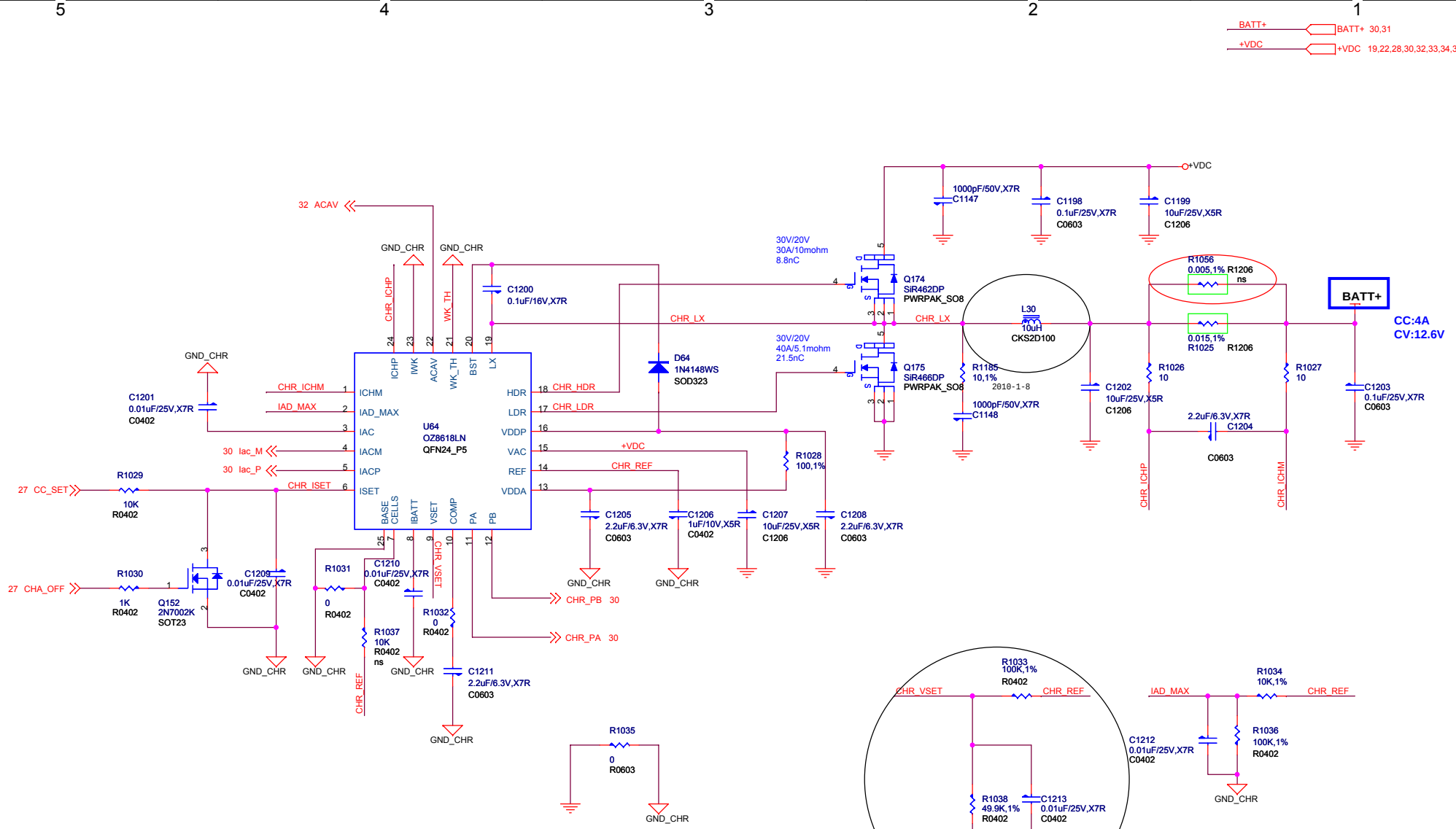

CC_SET	Charge Current	SystemState	Cells
3.0V	4.17A	S3,S4,S5	6Cells
2.0V	2.78A	S0	6Cells
1.5V	2.08A	S0,S3,S4,S5	3Cells
0.375V	521mA	PreCharge	3Cells/6Cells
<0.15V	=CHA_OFF		3Cells/6Cells

State	CELLS
Hi_Z	2
LOW	3

CZC Technology

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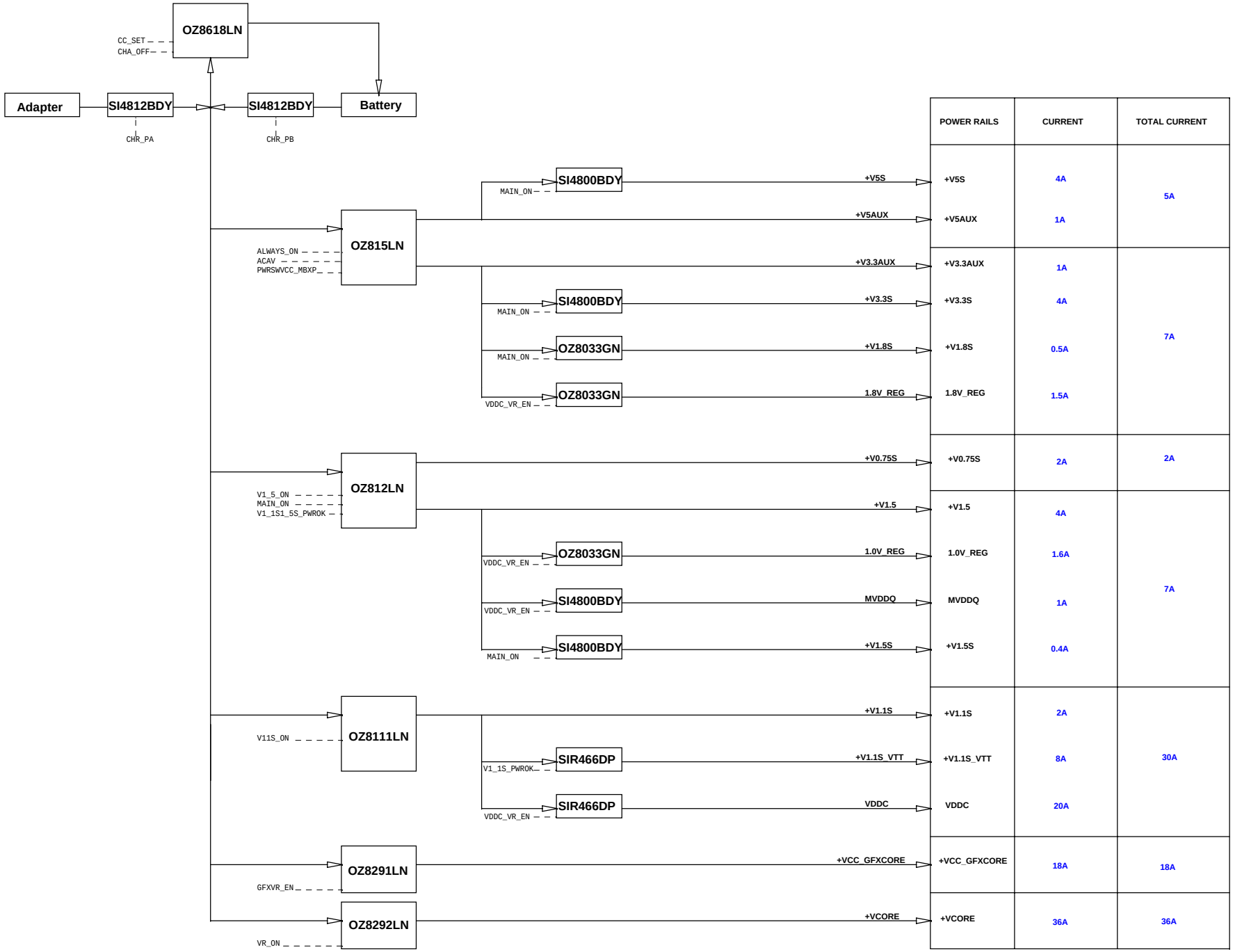

POWER RAILS	CURRENT	TOTAL CURRENT
+V5S	4A	5A
+V5AUX	1A	
+V3.3AUX	1A	7A
+V3.3S	4A	
+V1.8S	0.5A	
1.8V_REG	1.5A	
+V0.75S	2A	2A
+V1.5	4A	7A
1.0V_REG	1.6A	
MVDDQ	1A	
+V1.5S	0.4A	
+V1.1S	2A	30A
+V1.1S_VTT	8A	
VDDC	20A	
+VCC_GFXCORE	18A	18A
+VCORE	36A	36A

CZC Technology

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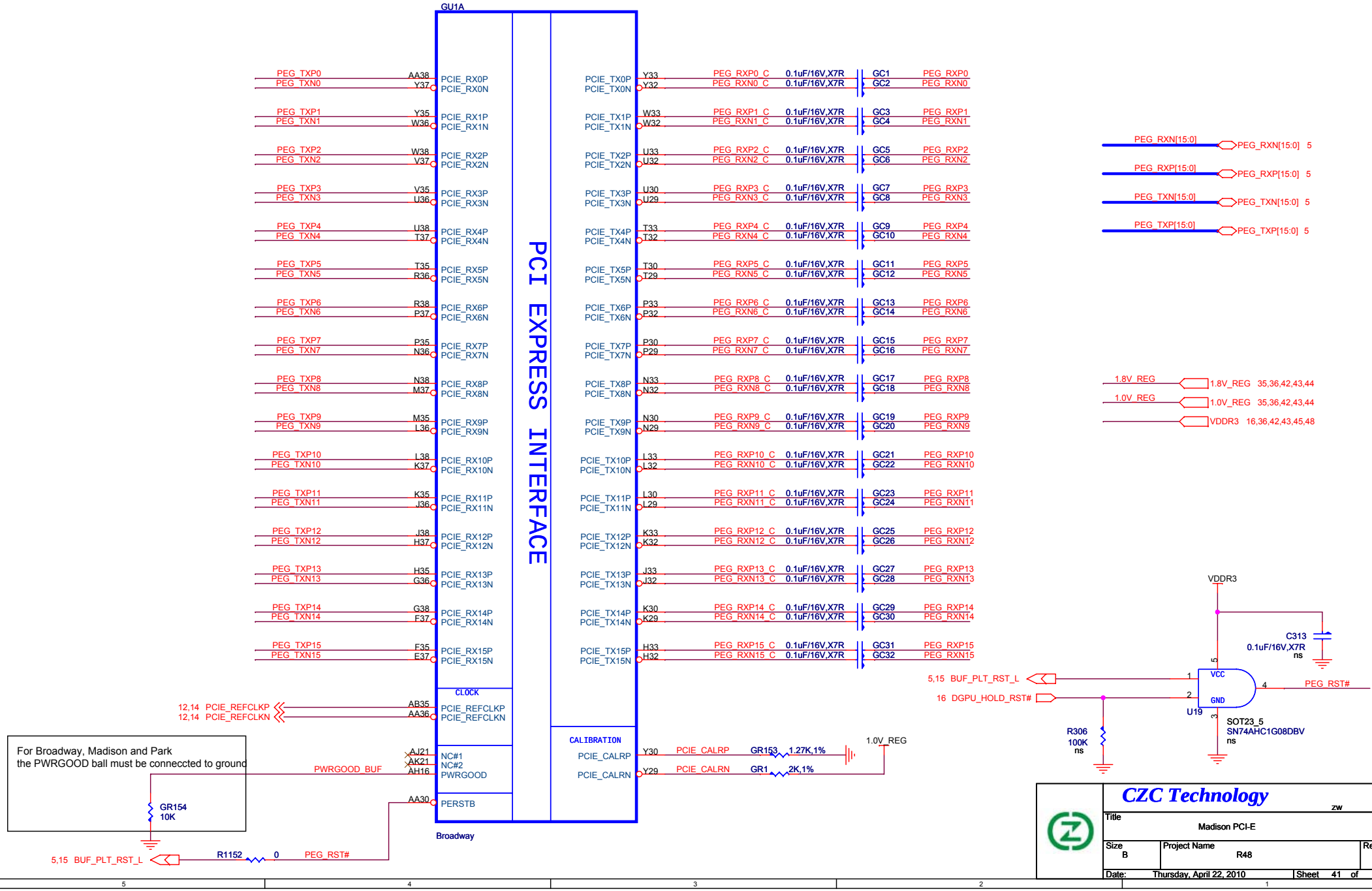
GU1A
PCI EXPRESS INTERFACE
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
CLOCK
PCIE_REFCLKP
PCIE_REFCLKN
NC#1
NC#2
PWRGOOD
PERSTB
CALIBRATION
PCIE_CALRP
PCIE_CALRN
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
Broadway
PEG_RXN[15:0] PEG_RXN[15:0] 5
PEG_RXP[15:0] PEG_RXP[15:0] 5
PEG_TXN[15:0] PEG_TXN[15:0] 5
PEG_TXP[15:0] PEG_TXP[15:0] 5
1.8V_REG 1.8V_REG 35,36,42,43,44
1.0V_REG 1.0V_REG 35,36,42,43,44
VDDR3 16,36,42,43,45,48
VDDR3
C313
0.1uF/16V,X7R
ns
5,15 BUF_PLT_RST_L
16 DGPU_HOLD_RST#
PEG_RST#
U19
VCC
GND
SOT23_5
SN74AHC1G08DBV
ns
R306
100K
ns
12,14 PCIE_REFCLKP
12,14 PCIE_REFCLKN
PWRGOOD_BUF
For Broadway, Madison and Park
the PWRGOOD ball must be connecctd to ground
GR154
10K
5,15 BUF_PLT_RST_L
R1152
0
PEG_RST#
1.0V_REG
PCIE_CALRP
GR153
1.27K,1%
PCIE_CALRN
GR1
2K,1%
PEG_RXP0_C
PEG_RXN0_C
PEG_RXP1_C
PEG_RXN1_C
PEG_RXP2_C
PEG_RXN2_C
PEG_RXP3_C
PEG_RXN3_C
PEG_RXP4_C
PEG_RXN4_C
PEG_RXP5_C
PEG_RXN5_C
PEG_RXP6_C
PEG_RXN6_C
PEG_RXP7_C
PEG_RXN7_C
PEG_RXP8_C
PEG_RXN8_C
PEG_RXP9_C
PEG_RXN9_C
PEG_RXP10_C
PEG_RXN10_C
PEG_RXP11_C
PEG_RXN11_C
PEG_RXP12_C
PEG_RXN12_C
PEG_RXP13_C
PEG_RXN13_C
PEG_RXP14_C
PEG_RXN14_C
PEG_RXP15_C
PEG_RXN15_C
0.1uF/16V,X7R
CZC Technology
zw
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Madison PCI-E
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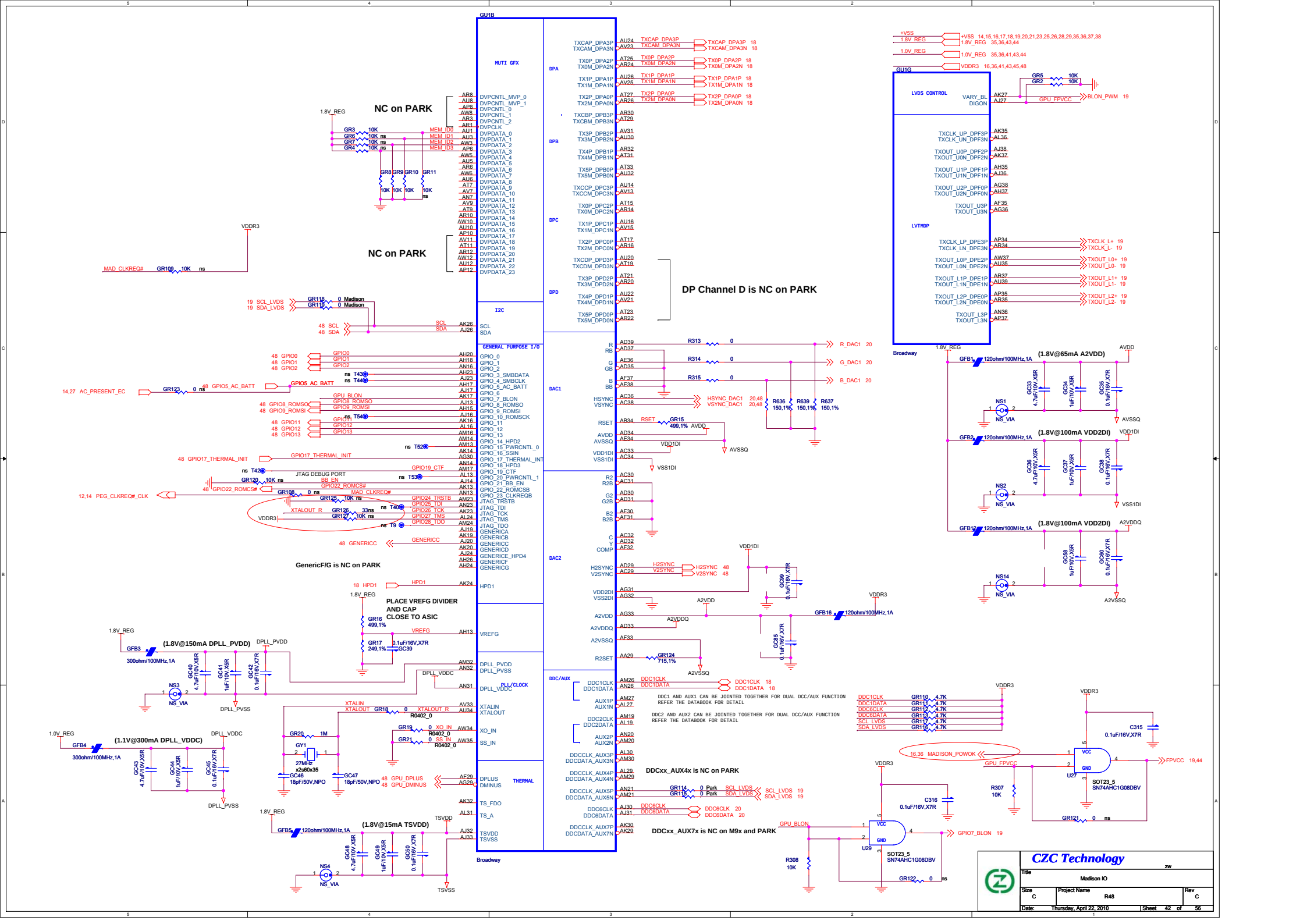
GU1B
MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
DDC/AUX
THERMAL
Broadway
NC on PARK
NC on PARK
DP Channel D is NC on PARK
GenericF/G is NC on PARK
PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC
(1.8V@150mA DPLL_PVDD)
(1.1V@300mA DPLL_VDDC)
(1.8V@15mA TSVDD)
(1.8V@65mA A2VDD)
(1.8V@100mA VDD2DI)
(1.8V@100mA VDD2DI)
DDCxx_AUX4x is NC on PARK
DDCxx_AUX7x is NC on M9x and PARK
DDC1 AND AUX1 CAN BE JOINTED TOGETHER FOR DUAL DCC/AUX FUNCTION
REFER THE DATABOOK FOR DETAIL
DDC2 AND AUX2 CAN BE JOINTED TOGETHER FOR DUAL DCC/AUX FUNCTION
REFER THE DATABOOK FOR DETAIL
LVDS CONTROL
LVTMDP
GU1G
Broadway
CZC Technology
Madison IO
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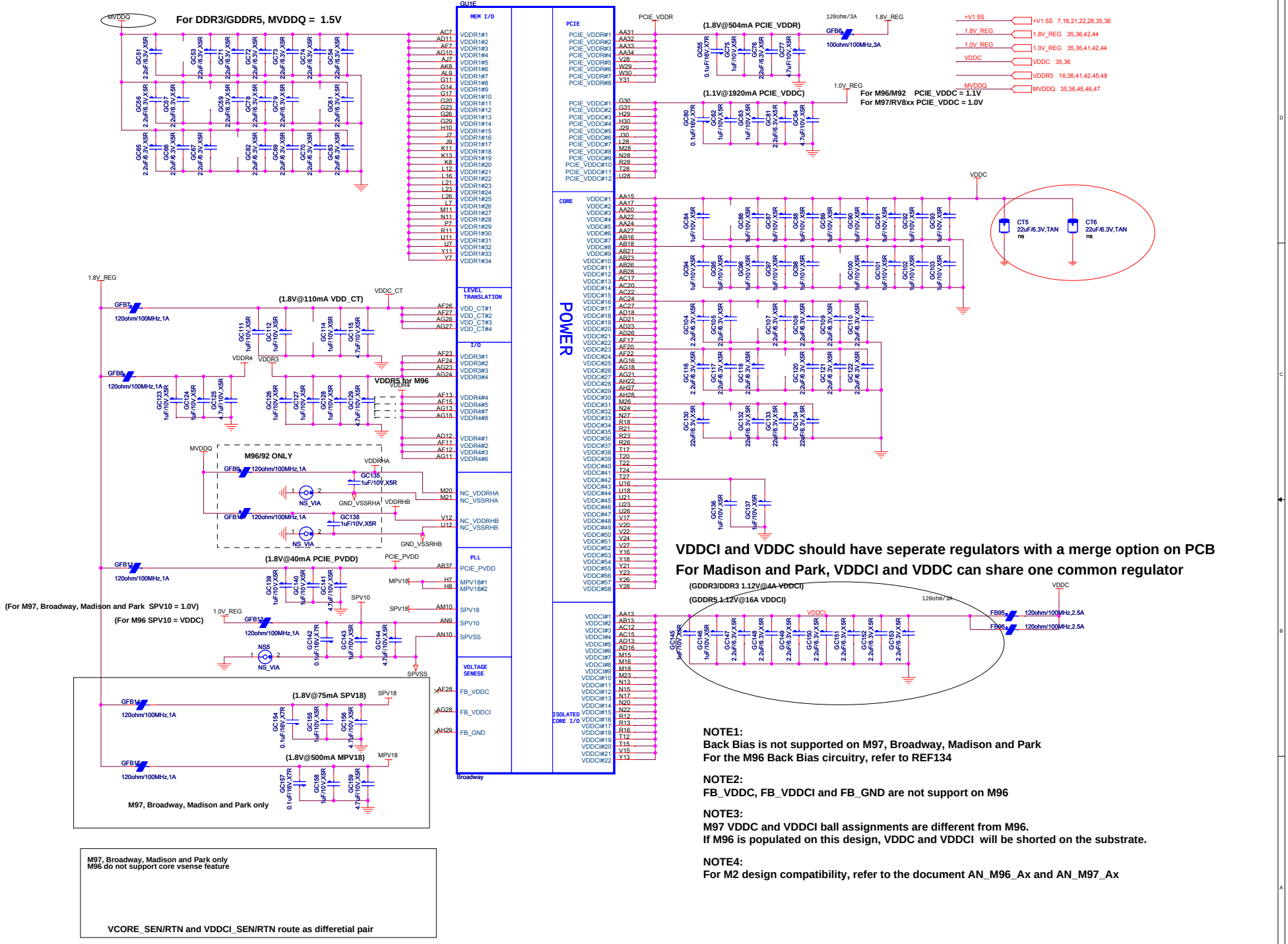
For DDR3/GDDR5, MVDDQ = 1.5V
MVDDQ
GU1E
MEM I/O
PCIE
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
POWER
CORE
ISOLATED CORE I/O
Broadway
PCIE_VDDR
(1.8V@504mA PCIE_VDDR)
(1.1V@1920mA PCIE_VDDC)
For M96/M92 PCIE_VDDC = 1.1V
For M97/RV8xx PCIE_VDDC = 1.0V
VDDC
CT5 22uF/6.3V,TAN ns
CT6 22uF/6.3V,TAN ns
1.8V_REG
(1.8V@110mA VDD_CT)
VDDC_CT
VDDR5 for M96
M96/92 ONLY
(1.8V@40mA PCIE_PVDD)
PCIE_PVDD
(For M97, Broadway, Madison and Park SPV10 = 1.0V)
(For M96 SPV10 = VDDC)
1.0V_REG
(1.8V@75mA SPV18)
(1.8V@500mA MPV18)
M97, Broadway, Madison and Park only
VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator
(GDDR3/DDR3 1.12V@4A VDDCI)
(GDDR5 1.12V@16A VDDCI)
VDDCI
NOTE1:
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134
NOTE2:
FB_VDDC, FB_VDDCI and FB_GND are not support on M96
NOTE3:
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.
NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax
M97, Broadway, Madison and Park only
M96 do not support core vsense feature
VCORE_SEN/RTN and VDDCI_SEN/RTN route as differetial pair
CZC Technology
Madison Power
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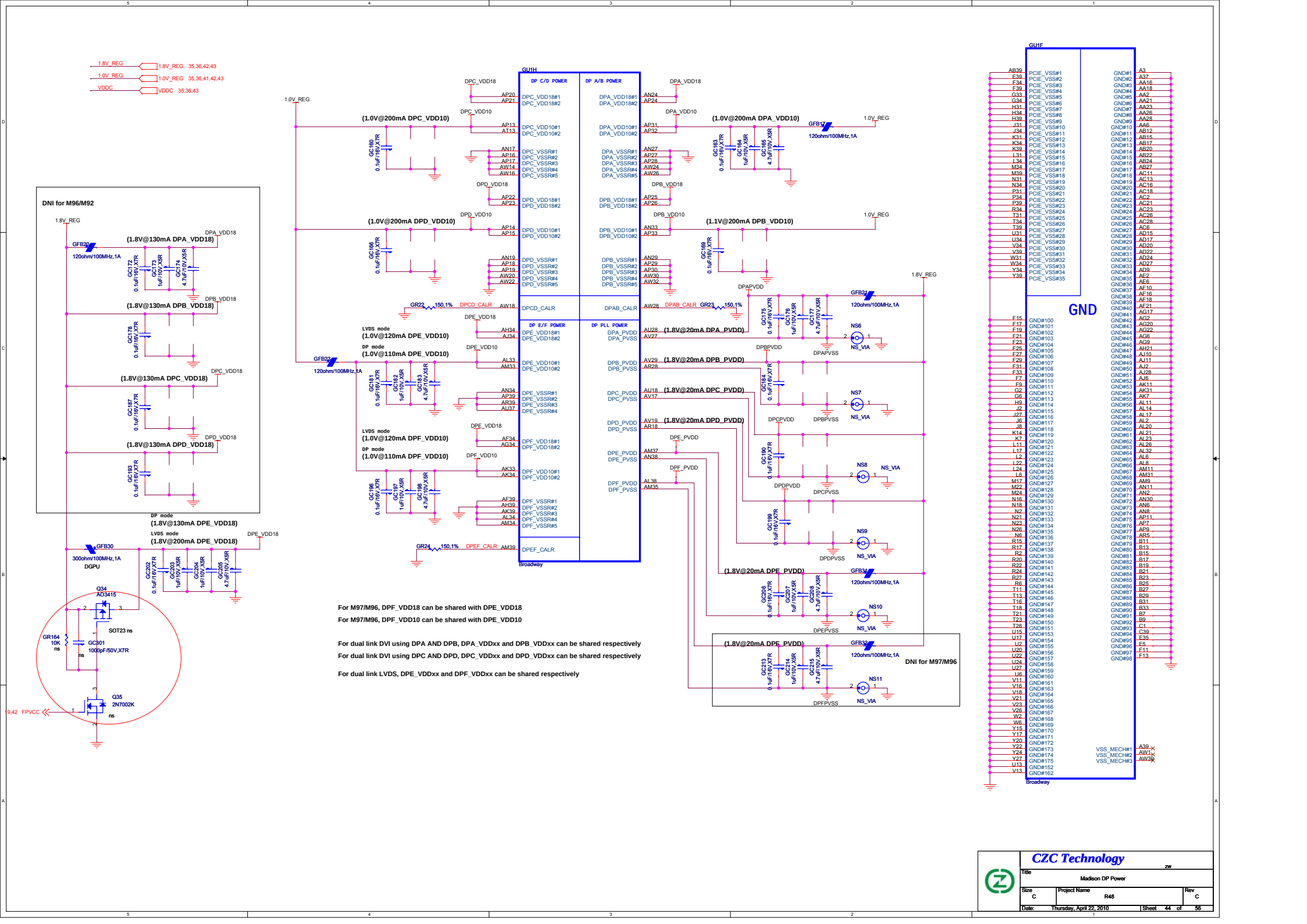
1.8V_REG 1.8V_REG 35,36,42,43
1.0V_REG 1.0V_REG 35,36,41,42,43
VDDC VDDC 35,36,43
DNI for M96/M92
1.8V_REG
(1.8V@130mA DPA_VDD18)
DPA_VDD18
GFB30
120ohm/100MHz,1A
(1.8V@130mA DPB_VDD18)
DPB_VDD18
(1.8V@130mA DPC_VDD18)
DPC_VDD18
(1.8V@130mA DPD_VDD18)
DPD_VDD18
DP mode
(1.8V@130mA DPE_VDD18)
LVDS mode
(1.8V@200mA DPE_VDD18)
DPE_VDD18
GFB30
300ohm/100MHz,1A
DGPU
Q34
AO3415
SOT23 ns
GR164
10K
ns
GC301
1000pF/50V,X7R
Q35
2N7002K
19,42 FPVCC
1.0V_REG
GU1H
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
DPC_VDD18
DPC_VDD10
(1.0V@200mA DPC_VDD10)
DPD_VDD18
DPD_VDD10
(1.0V@200mA DPD_VDD10)
DPE_VDD18
LVDS mode
(1.0V@120mA DPE_VDD10)
DP mode
(1.0V@110mA DPE_VDD10)
DPF_VDD18
LVDS mode
(1.0V@120mA DPF_VDD10)
DP mode
(1.0V@110mA DPF_VDD10)
DPCD_CALR
DPAB_CALR
DPEF_CALR
GR22 150,1% DPCD_CALR
GR23 150,1% DPAB_CALR
GR24 150,1% DPEF_CALR
GFB23
120ohm/100MHz,1A
DPA_VDD18
DPA_VDD10
(1.0V@200mA DPA_VDD10)
DPB_VDD18
DPB_VDD10
(1.1V@200mA DPB_VDD10)
(1.8V@20mA DPA_PVDD)
(1.8V@20mA DPB_PVDD)
(1.8V@20mA DPC_PVDD)
(1.8V@20mA DPD_PVDD)
(1.8V@20mA DPE_PVDD)
(1.8V@20mA DPF_PVDD)
DPAPVDD
DPBPVDD
DPCPVDD
DPDPVDD
DPEPVDD
DPFPVDD
DPAPVSS
DPBPVSS
DPCPVSS
DPDPVSS
DPEPVSS
DPFPVSS
NS6
NS7
NS8
NS9
NS10
NS11
NS_VIA
GFB24
GFB31
GFB32
GFB33
GFB34
120ohm/100MHz,1A
GFB17
120ohm/100MHz,1A
Broadway
For M97/M96, DPF_VDD18 can be shared with DPE_VDD18
For M97/M96, DPF_VDD10 can be shared with DPE_VDD10
For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively
For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively
For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively
DNI for M97/M96
GU1F
GND
VSS_MECH#1
VSS_MECH#2
VSS_MECH#3
Broadway
CZC Technology
zw
Title
Madison DP Power
Size
C
Project Name
R48
Rev
C
Date: Thursday, April 22, 2010
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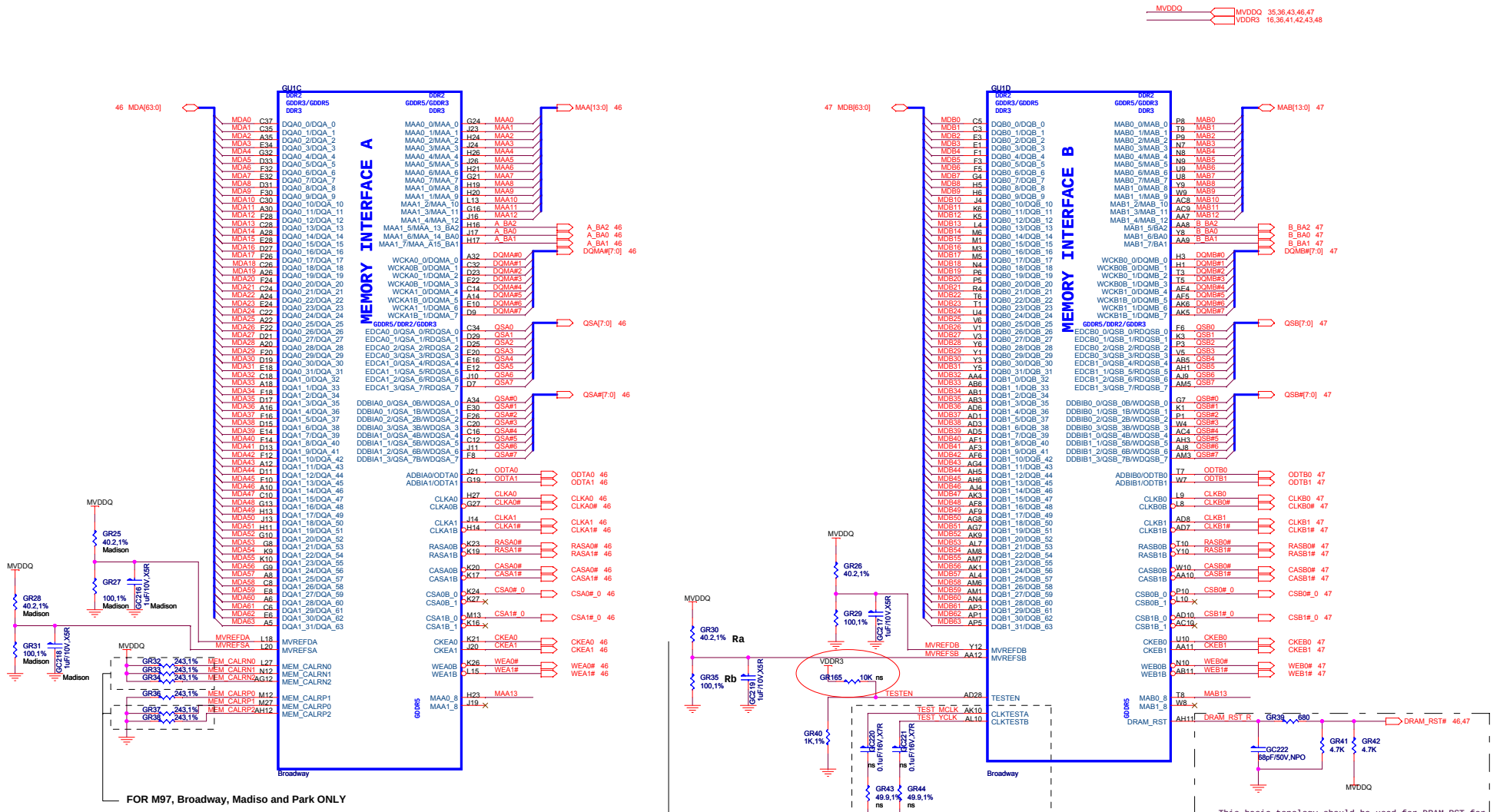

DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	0R/Short	680R
R_MEM_3	DNI	DNI
C_MEM	2.2nF	68pF

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zw

Title: Madison Memory

Size: C | Project Name: R48 | Rev: C

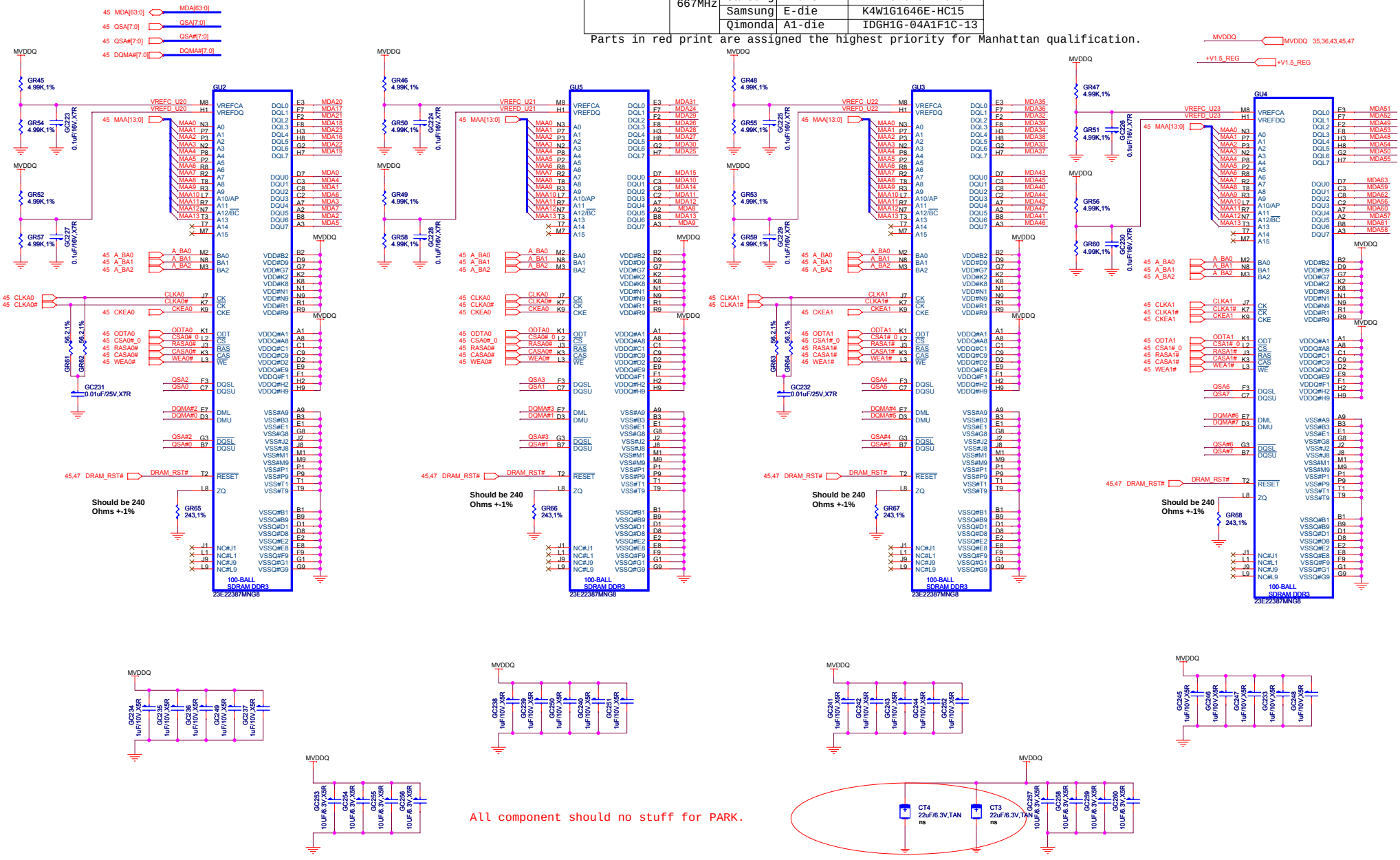
Date: Thursday, April 22, 2010 | Sheet 45 of 56

CHANNEL A: 256MB/512MB DDR3

Size per Part	Configuration	Row x Col x Bank bits
1024 Mbit	8 M x 16 x 8	13 x 10 x 3

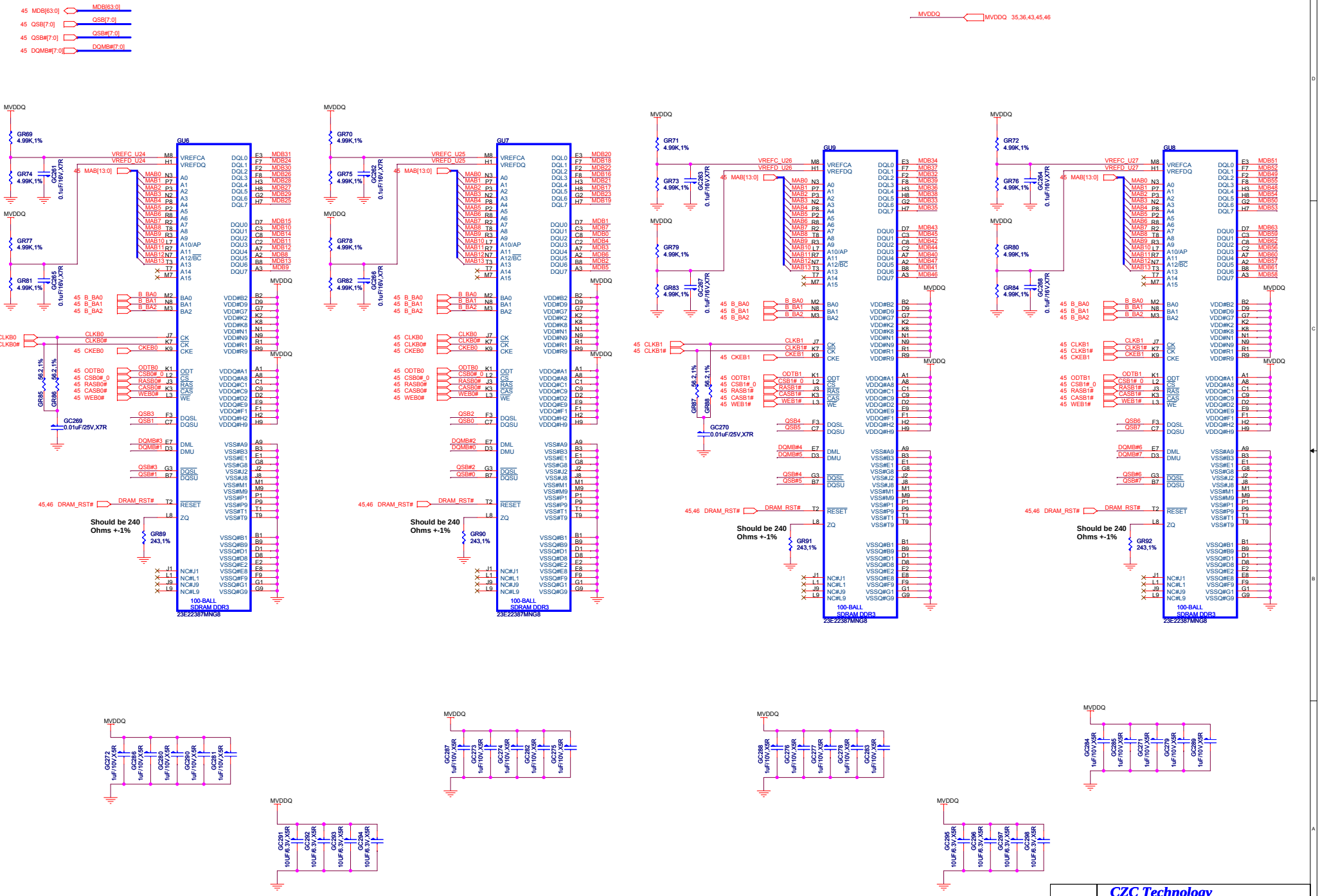
DDR3 64M X 16bit	1GHz	Samsung	E-die	K4W1G1646E-HC1A
	900MHz	Qimonda	A1-die	IDGH1G-04A1F1C-18
		Samsung	E-die	K4W1G1646E-HC11
	800MHz	Hynix	Orion-die	H5TQ1G63BFR-12C
		Qimonda	A1-die	IDGH1G-04A1F1C-16
		Samsung	E-die	K4W1G1646E-HC12
	700MHz	Hynix	Tiva-die	H5TQ1G63AFR-14C
		Hynix	Orion-die	H5TS1G63BFR-1
	667MHz	Samsung	D-die	K4W1G1646D-EC15
		Samsung	E-die	K4W1G1646E-HC15
		Qimonda	A1-die	IDGH1G-04A1F1C-13

Parts in red print are assigned the highest priority for Manhattan qualification.



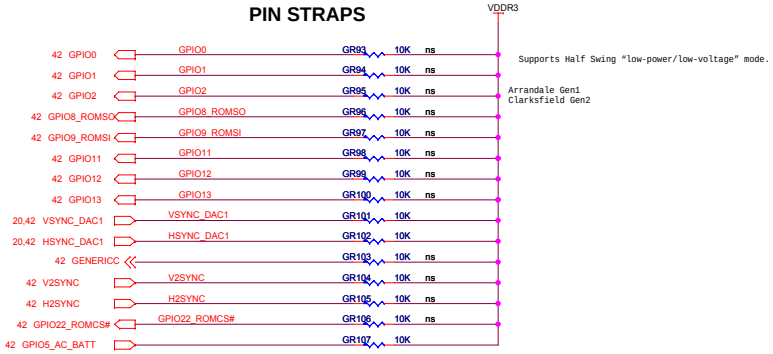
CZC Technology			zw
Title	Madison Memory DDR3 Channel A		
Size C	Project Name R48		Rev C
Date: Thursday, April 22, 2010	Sheet 46 of 56		

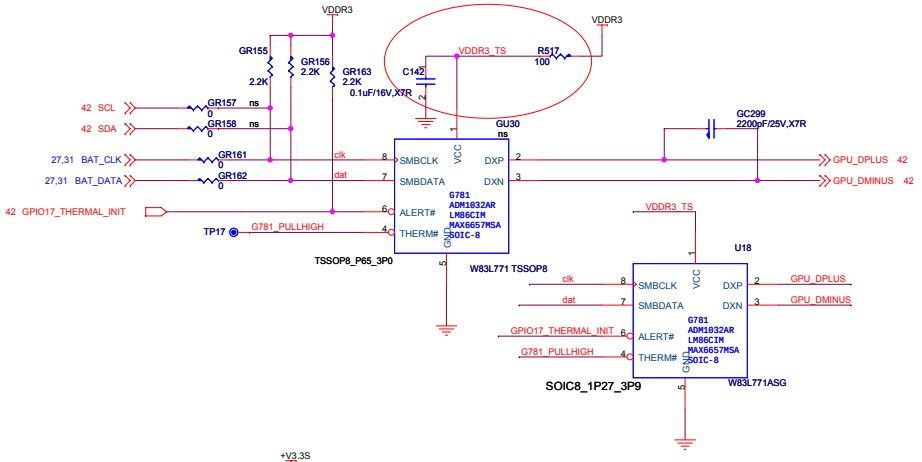
CHANNEL B: 256MB/512MB DDR3

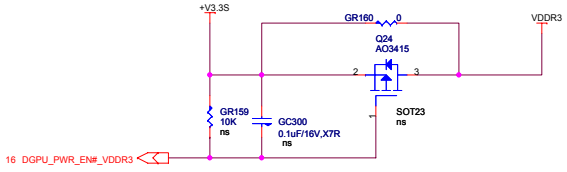


+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,22,24,25,27,28,29,34,35,36,37,38
VDDR3 16,36,41,42,43,45

PIN STRAPS







CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9_ROMSI	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO22_ROMCS#	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0
AUD[1]	HSYNC_DAC1	built-in HDMI connector	1
AUD[0]	VSYNC_DAC1	Audio functiuon present	1

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GPIO21_BB_EN

CZC Technology zw

Title: Madison Thermal Straps

Size: C | Project Name: R48 | Rev: C

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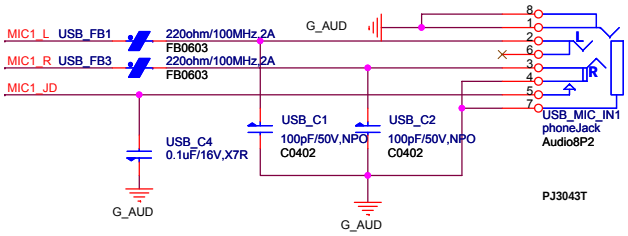
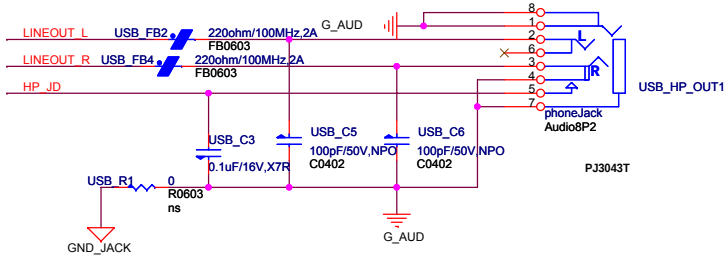
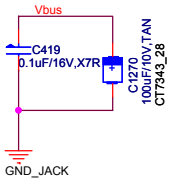
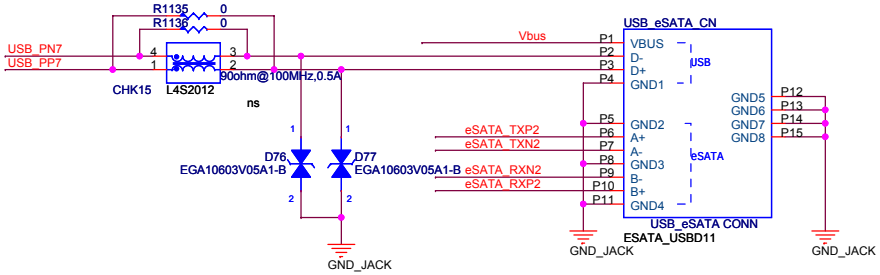
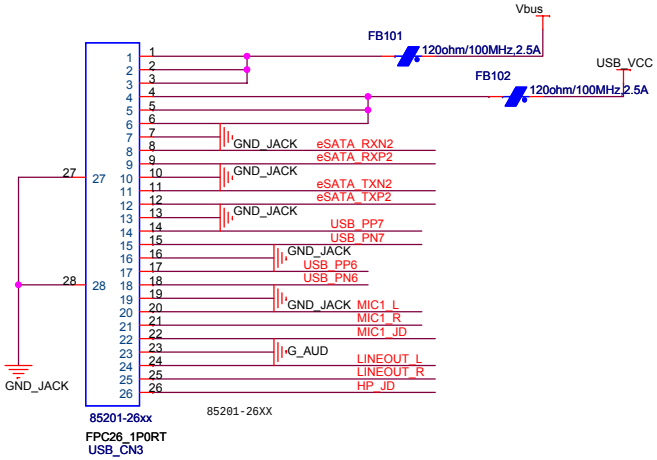


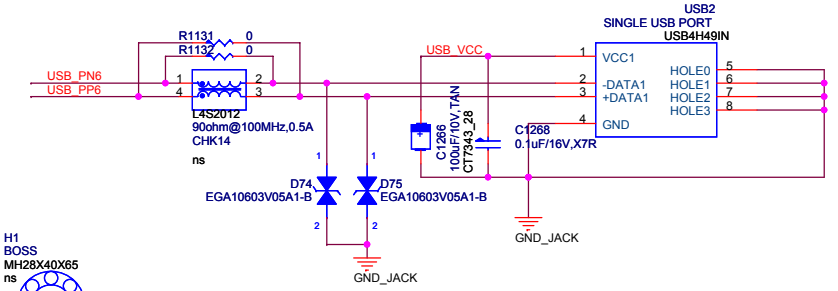


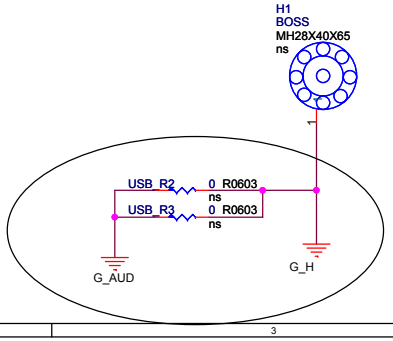




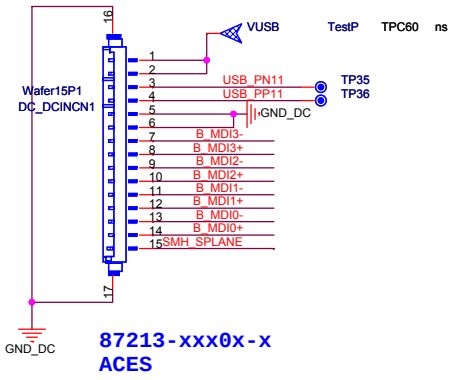
C10756-10403-L

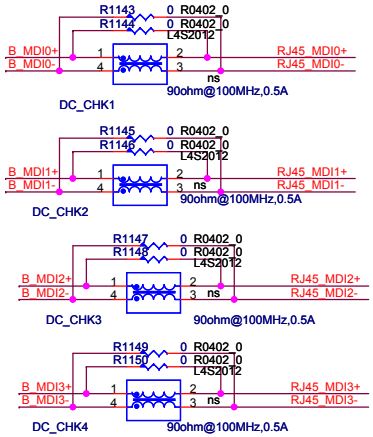


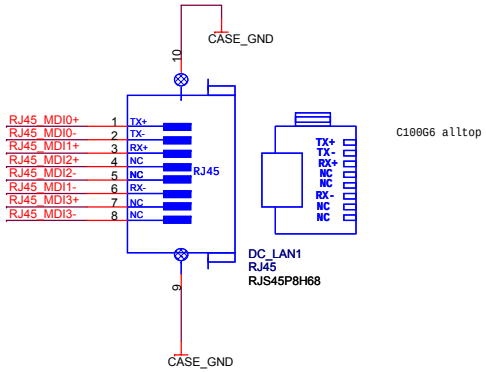


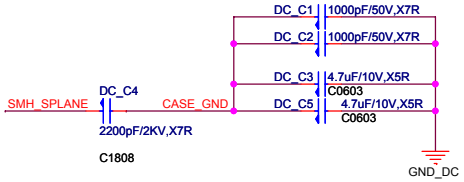


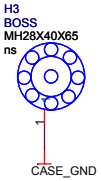
CZC Technology		zw
Title: USB AUDIO board		
Size: A3	Project Name: R48	Rev: C
Date: Thursday, April 22, 2010	Sheet 49 of 56	



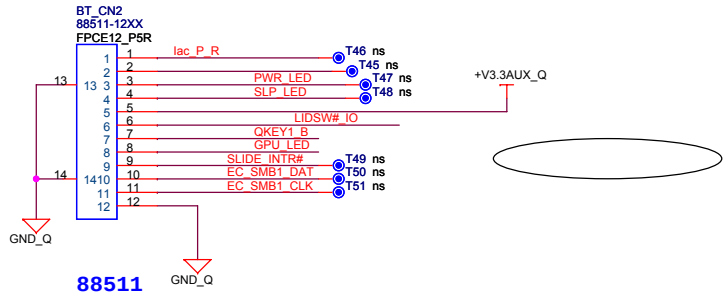


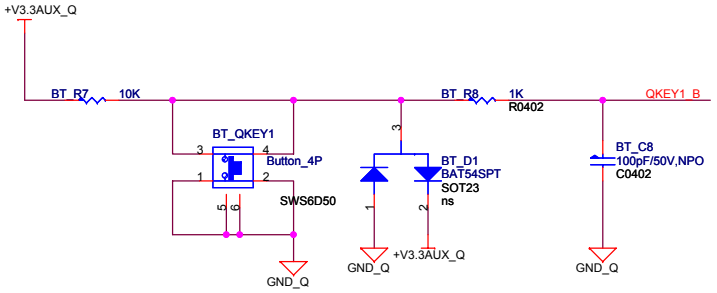


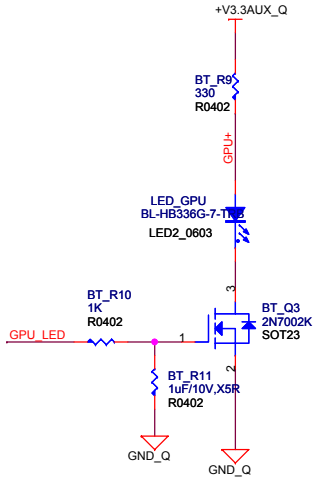


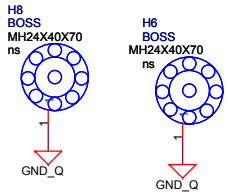


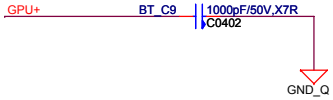
CZC Technology		
Title: RJ45		
Size: A3	Project Name: R48	Rev: C
Date: Thursday, April 22, 2010	Sheet 50 of 56	

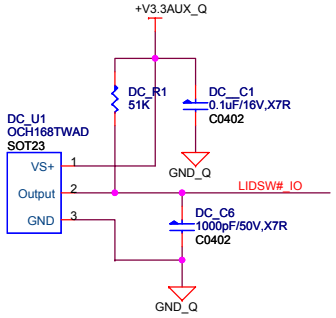












CZC Technology

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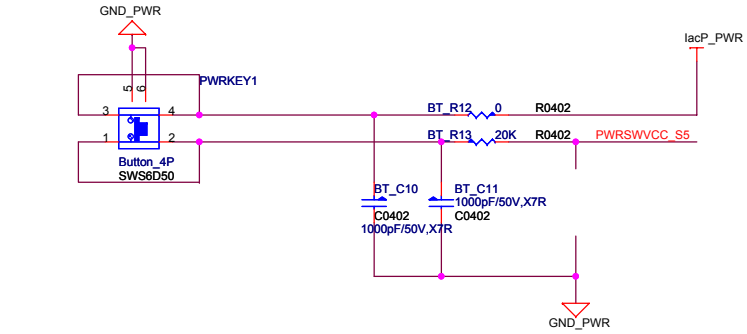
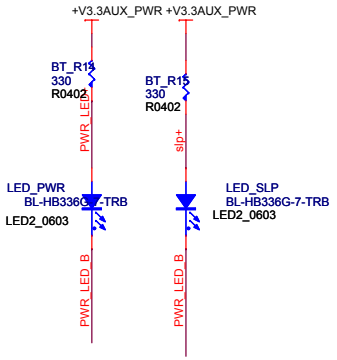
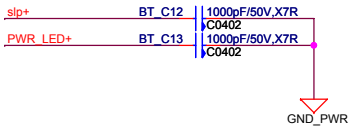
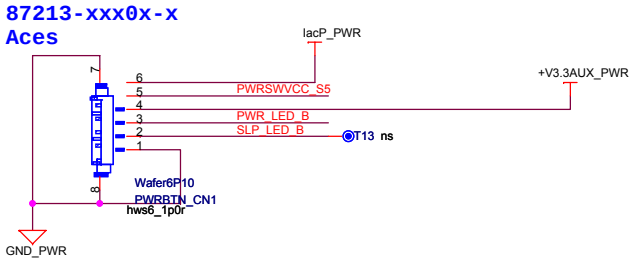
Title	QKey LID Board	
Size A3	Project Name R48	Rev C
Date: Thursday, April 22, 2010	Sheet 51 of 56	

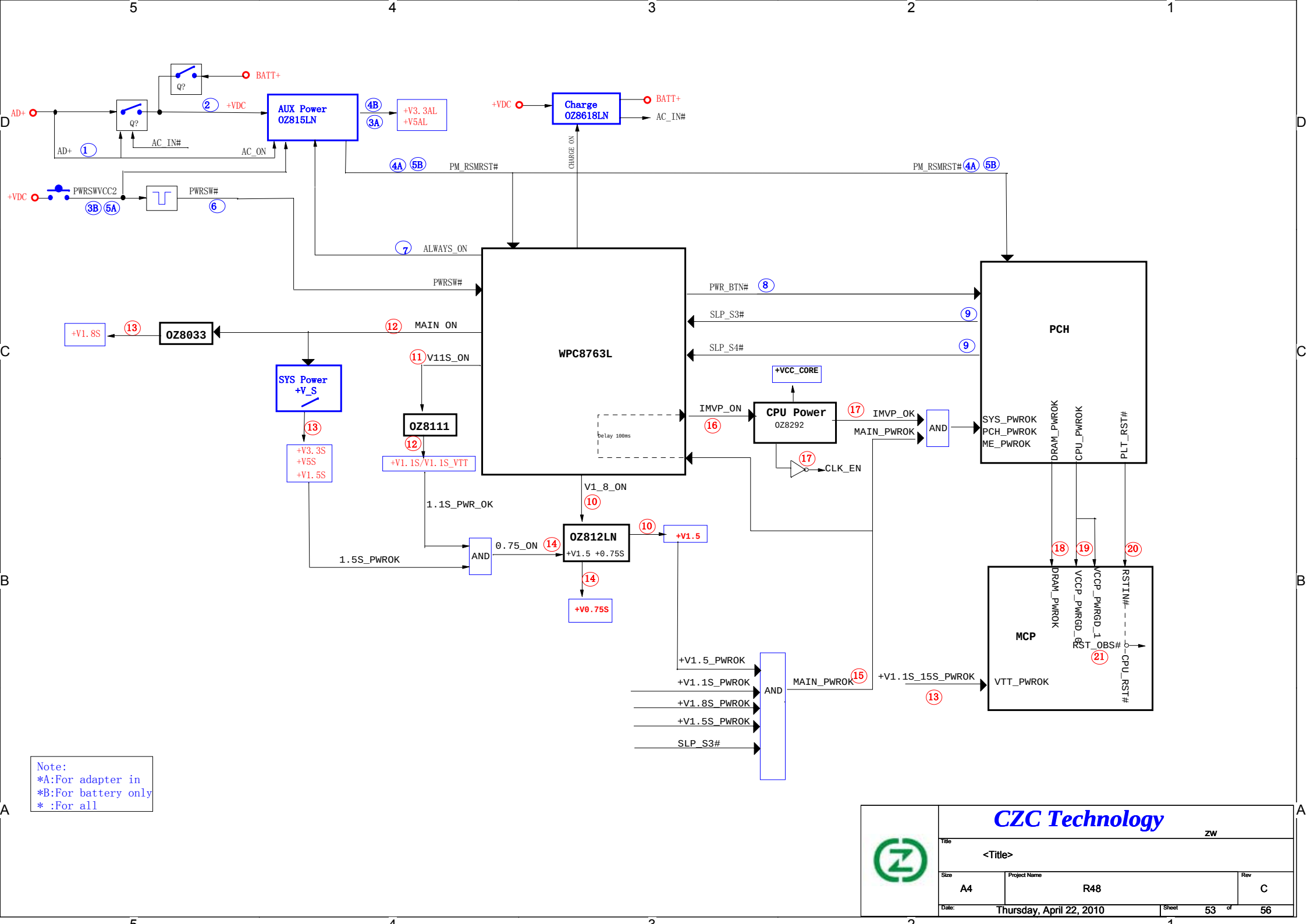








CZC Technology		zw
Title: PWR_BTN Board		
Size: A3	Project Name: R48	Rev: C
Date: Thursday, April 22, 2010	Sheet 52 of 56	



Note:
*A:For adapter in
*B:For battery only
* :For all

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ZW

Title: <Title>		
Size: A4	Project Name: R48	Rev: C
Date: Thursday, April 22, 2010	Sheet 53 of 56	

4. Schematic modify Item and history;

2009-12-03:
1. first Release and generate netfile.

2010-01-08:
1. P13 stuff R97。
2. P14 Add R359 R360
3. P16 Change R1005 pull high to VDDR3.
   No stuff R204
4. P19 Change D62 to R299
   Correct channel A/B connection of GPU LVDS.
5. P21 ns R457 R458
6. P22 Change NEW_CARD_CLKREQ# pull high to +V3.3S(R282)
7. P25 Add MDCCN1
   ns D26
7. P27 Add R436 1K,
   Add BT_LED# to EC
8. P29 change wifi LED connection,Touchpad CONN connection.
9. P42 Add GR125 GR126 GR127 for the Ver A11 of PARK. U27.1 change to Madison_pwrok.
10. P43 Add CT5 CT6 reserved.
11. P44 Add Q34 Q35 GR164 GC301
12. P45 Add GR165 for the Ver A11 of PARK.
13. P46 Add CT3 CT4 reserved.
14. P30-P40 change refer to SCH.

VerC change list:
hw:
1, 修改部分0ohm电阻封装为R0402_0
2,ns thermal sensor for DIMM(P09)
3,ADD BIOS_LOCK SWITCH。(P13)
4, ns MiniPCIE slot for 3G.(P21)
5,ns C1280 C1230 C1234(P24)
6,Reserved TPA6017A2,adjust amp out(p25)
7,add R524,change R449 to 200K,for fan(p28)
8,ns U19,stuff R1152(p41)
9,add R517 (P48)
10,del BT_Z1 (P52)

pwr:
1、更改R917 R919阻值，设定DDR3电源1.54V
2、1.1S电源增加R1187 R1186 C1296频率调整电路
3、更改R939 R937阻值，调整1.1S电源为1.129V
4、去掉电阻R1179 0ohm电阻，去掉D69续流二极管，更改R978 1K 5%为1K 1%，
5、R1153，R1154，C1277更改value设定GFX电源频率在350KHz
6、OZ8291 DSLP pin改成2.2Kohm下拉到地
7、R1181阻值更改以满足IMONITOR
8、去掉OZ8291 VID 测试电路
9、更改R1014阻值以满足cpucore的loadline，更改R1016 1K 5%为1K 1%，去掉R1182 0ohm电阻
10、OZ8292 DSLP pin接2.2K电阻上拉到5VS以满足imvp6.5
11、更改R1184阻值以满足IMONITOR,去掉D70 D71续流二极管，去掉OZ8292 VID 测试电路

CZC Technology			ZW
Title: <Title>			
Size: A4	Project Name: R48		Rev: C
Date: Thursday, April 22, 2010		Sheet 56 of 56	