1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
			2010-07-22

SCHEM,MLB DVT,K99

07/22/10

Page	(.csa)	Contents	Sync	Date
1	1	Table of Contents		
2	2	System Block Diagram	K6_MLB	12/11/2009
3	3	Power Block Diagram	K6_MLB	12/11/2009
4	4	K99 BOM Variants	K6_MLB	12/11/2009
5	5	BOM Configuration	K24_MLB	07/20/2009
6	6	Revision History	K24_MLB	01/19/2009
7	7	FUNCTIONAL TEST	K6_MLB	12/11/2009
8	8	Power Aliases	K6_MLB	12/11/2009
9	9	SIGNAL ALIAS	K6_MLB	12/11/2009
10	10	CPU FSB	K16_MLB	07/07/2010
11	11	CPU Power & Ground	K16_MLB	07/07/2010
12	12	CPU Decoupling & VID	K16_MLB	03/24/2010
13	13	eXtended Debug Port (Micro-XDP)	K16_MLB	07/07/2010
14	14	MCP CPU Interface	K16_MLB	07/07/2010
15	15	MCP Memory Interface	K16_MLB	07/07/2010
16	16	MCP PCIe Interfaces	K16_MLB	07/07/2010
17	17	MCP Graphics	K16_MLB	07/07/2010
18	18	MCP SATA, USB & Ethernet	K16_MLB	07/07/2010
19	19	MCP HDA, LPC & MISC	K16_MLB	07/07/2010
20	20	MCP Power & Ground	K16_MLB	07/07/2010
21	23	MCP89 Memory Rail Gating	K16_MLB	07/07/2010
22	24	MCP89 GFX Core Rail Gating	K16_MLB	07/07/2010
23	25	MCP Standard Decoupling	K16_MLB	07/07/2010
24	26	MCP Graphics Support	K16_MLB	07/07/2010
25	28	SB Misc	K6_MLB	12/11/2009
26	31	DDR3 DRAM Channel A (0-31)	K16_MLB	07/07/2010
27	32	DDR3 DRAM Channel A (32-63)	K16_MLB	07/07/2010
28	33	DDR3 DRAM Channel B (0-31)	K16_MLB	07/07/2010
29	34	DDR3 DRAM Channel B (32-63)	K16_MLB	07/07/2010
30	35	DDR BYPASSING 1	K16_MLB	07/07/2010
31	36	DDR BYPASSING 2	K16_MLB	07/07/2010
32	37	Memory Active Termination	K16_MLB	07/07/2010
33	39	FSB/DDR3 Vref Margining	K16_MLB	07/07/2010
34	40	X21 WIRELESS CONNECTOR	K16_MLB	07/07/2010
35	45	SATA CONNECTOR	K16_MLB	07/07/2010
36	46	External USB Connectors	K16_MLB	07/07/2010
37	47	LIO CONNECTORS	N/A	N/A
38	49	SMC	K16_MLB	07/07/2010
39	50	SMC Support	K16_MLB	07/07/2010
40	51	LPC+SPI Debug Connector	K16_MLB	07/07/2010
41	52	K16/K99 SMus Connections	K16_MLB	07/07/2010
42	53	Voltage & Current Sensing	K16_MLB	07/07/2010
43	54	Current Sensing	K16_MLB	07/07/2010
44	55	Thermal Sensors	K16_MLB	07/07/2010
45	56	Fan	K16_MLB	07/07/2010
46	57	WELLSPRING 1	K16_MLB	07/07/2010
47	61	SPI ROM	K16_MLB	07/07/2010
48	66	AUDI0: SPEAKER AMP	AUDIO	02/09/2010
49	69	DC-In & Battery Connectors	K84_MLB	11/09/2009
50	70	PBus Supply & Battery Charger	K6_MLB	11/09/2009
51	72	5V / 3.3V Power Supply	K16_MLB	07/07/2010
52	73	1.5V/1.35V LVDDR3 Supply	K16_MLB	07/07/2010
53	74	IMVP6 CPU VCore Regulator	POWER	07/13/2005
54	75	MCP VCore Regulator	K6_MLB	12/11/2009
55	76	CPUVTT (1.05V) Power Supply	K16_MLB	07/07/2010
56	77	Misc Power Supplies	K16_MLB	07/07/2010
57	78	Power Sequencing	K16_MLB	07/07/2010
58	79	Power FETs	K16_MLB	07/07/2010
59	90	Internal DisplayPort Connector	K16_MLB	07/07/2010
60	93	External DisplayPort Support	K16_MLB	07/07/2010
61	94	DisplayPort Connector	K16_MLB	07/07/2010
62	97	LCD Backlight Driver	K16_MLB	03/31/2010
63	98	LCD Backlight Support	K16_MLB	07/07/2010
64	99	Additional CPU/GPU Decoupling	K16_MLB	07/07/2010
65	100	CPU/FSB Constraints	K16_MLB	07/07/2010
66	101	Memory Constraints	K16_MLB	07/07/2010
67	102	MCP Constraints 1	K16_MLB	07/07/2010
68	103	MCP Constraints 2	K16_MLB	07/07/2010
69	104	Ethernet Constraints	K16_MLB	07/07/2010
70	106	SMC Constraints	K16_MLB	07/07/2010
71	108	K16/K99 Specific Constraints	K16_MLB	07/07/2010
72	109	K99 RULE DEFINITIONS	K16_MLB	07/07/2010
73	110	Acoustic Cap BOM Config Tables	K16_MLB	07/07/2010

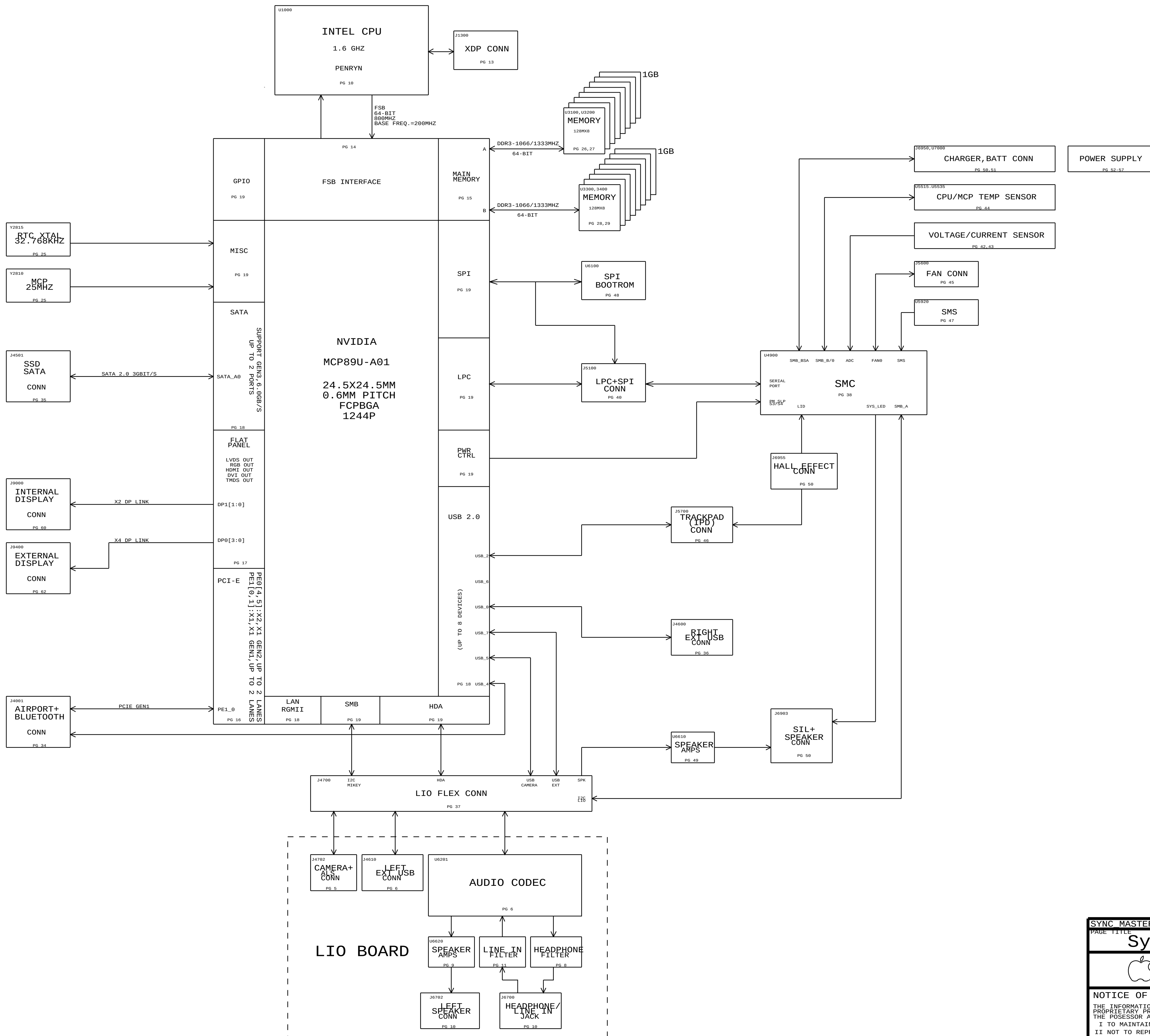
Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8379	1	SCHEM,MLB,K99	SCH	CRITICAL	
820-2796	1	PCBF,MLB,K99	PCB	CRITICAL	

DRAWING TITLE
SCHEM,MLB,K99

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D
REVISION 4.4.0
BRANCH
PAGE 1 OF 110
SHEET 1 OF 73



SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE

System Block Diagram

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DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

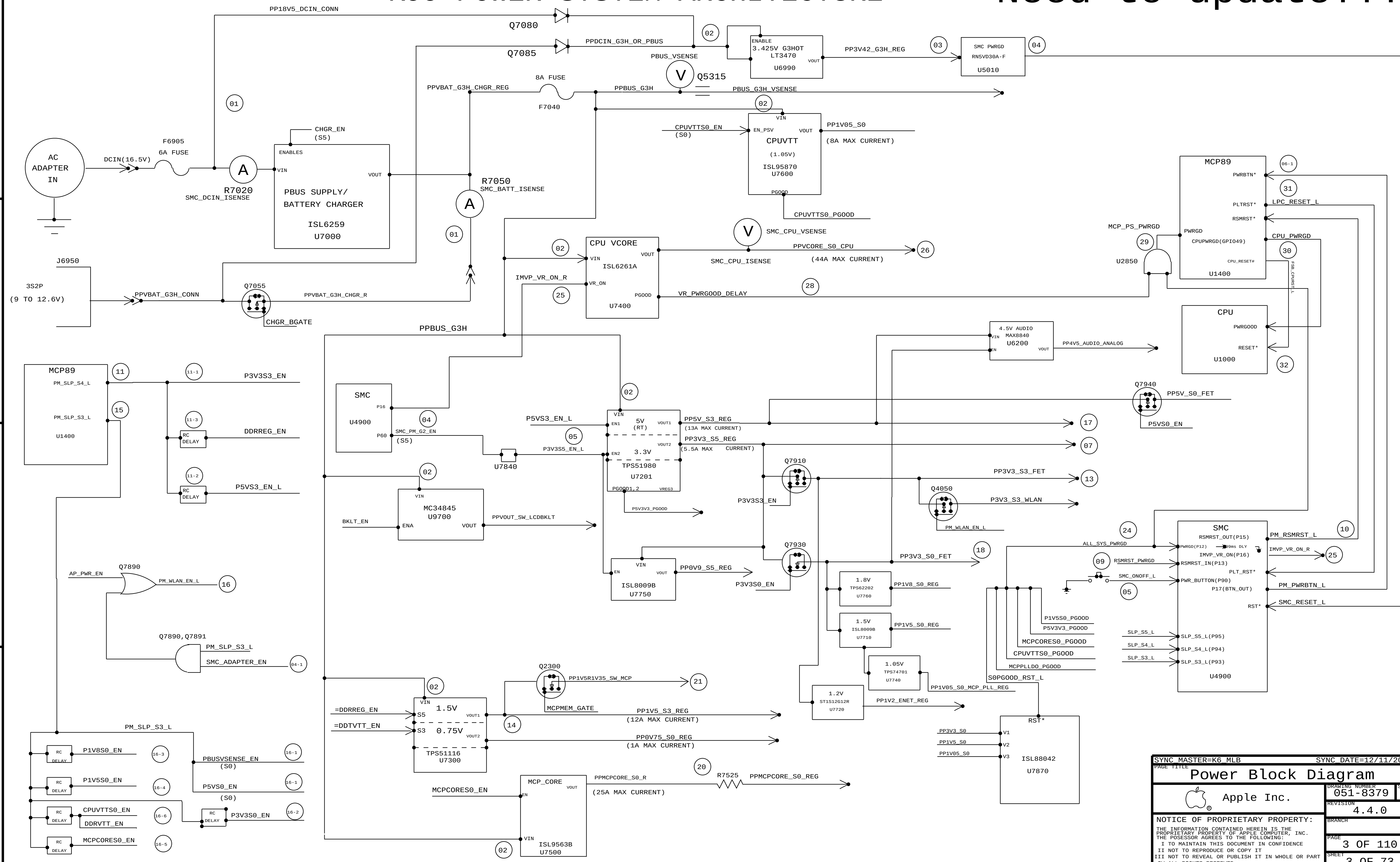
BRANCH

PAGE 2 OF 110

SHEET 2 OF 73

K99 POWER SYSTEM ARCHITECTURE

Need to update!!!



SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE: Power Block Diagram

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DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

NOTICE OF PROPRIETARY PROPERTY:

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0651	PCBA,MLB,HY 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DX7,DDR3:HYNIX_2GB,CAPS:SS
639-1055	PCBA,MLB,HY 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD15,DDR3:HYNIX_2GB,CAPS:MU
639-1048	PCBA,MLB,HY 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0X,DDR3:HYNIX_2GB,CAPS:TY
639-1043	PCBA,MLB,HY 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0Q,DDR3:HYNIX_4GB,CAPS:SS
639-1044	PCBA,MLB,HY 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0R,DDR3:HYNIX_4GB,CAPS:MU
639-1039	PCBA,MLB,HY 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0L,DDR3:HYNIX_4GB,CAPS:TY
639-1045	PCBA,MLB,SA 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0T,DDR3:SAMSUNG_2GB,CAPS:SS
639-1054	PCBA,MLB,SA 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD14,DDR3:SAMSUNG_2GB,CAPS:MU
639-1049	PCBA,MLB,SA 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0Y,DDR3:SAMSUNG_2GB,CAPS:TY
639-1052	PCBA,MLB,SA 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD12,DDR3:SAMSUNG_4GB,CAPS:SS
639-1046	PCBA,MLB,SA 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0V,DDR3:SAMSUNG_4GB,CAPS:MU
639-1040	PCBA,MLB,SA 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0M,DDR3:SAMSUNG_4GB,CAPS:TY
639-1042	PCBA,MLB,MI 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0P,DDR3:MICRON_2GB,CAPS:SS
639-1053	PCBA,MLB,MI 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD13,DDR3:MICRON_2GB,CAPS:MU
639-1047	PCBA,MLB,MI 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0W,DDR3:MICRON_2GB,CAPS:TY
639-1051	PCBA,MLB,MI 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD11,DDR3:MICRON_4GB,CAPS:SS
639-1041	PCBA,MLB,MI 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0N,DDR3:MICRON_4GB,CAPS:MU
639-1050	PCBA,MLB,MI 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD10,DDR3:MICRON_4GB,CAPS:TY
639-1446	PCBA,MLB,1.6GHZ,EL 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4Q,DDR3:ELPIDA_2GB,CAPS:SS
639-1438	PCBA,MLB,1.6GHZ,EL 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4G,DDR3:ELPIDA_2GB,CAPS:MU
639-1444	PCBA,MLB,1.6GHZ,EL 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4N,DDR3:ELPIDA_2GB,CAPS:TY
639-1449	PCBA,MLB,1.6GHZ,EL 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4V,DDR3:ELPIDA_4GB,CAPS:SS
639-1448	PCBA,MLB,1.6GHZ,EL 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4T,DDR3:ELPIDA_4GB,CAPS:MU
639-1445	PCBA,MLB,1.6GHZ,EL 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4P,DDR3:ELPIDA_4GB,CAPS:TY
607-6999	CMN PTS,PCBA,MLB,K99	K99_COMMON
085-1121	K99 MLB DEVELOPMENT BOM	K99_DEVEL:ENG
639-1355	PCBA,MLB,1.4GHZ,HY 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8L,DDR3:HYNIX_2GB,CAPS:SS
639-1341	PCBA,MLB,1.4GHZ,HY 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF83,DDR3:HYNIX_2GB,CAPS:MU
639-1353	PCBA,MLB,1.4GHZ,HY 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8J,DDR3:HYNIX_2GB,CAPS:TY
639-1350	PCBA,MLB,1.4GHZ,HY 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8F,DDR3:HYNIX_4GB,CAPS:SS
639-1356	PCBA,MLB,1.4GHZ,HY 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8M,DDR3:HYNIX_4GB,CAPS:MU
639-1348	PCBA,MLB,1.4GHZ,HY 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8C,DDR3:HYNIX_4GB,CAPS:TY
639-1349	PCBA,MLB,1.4GHZ,SA 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8D,DDR3:SAMSUNG_2GB,CAPS:SS
639-1351	PCBA,MLB,1.4GHZ,SA 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8G,DDR3:SAMSUNG_2GB,CAPS:MU
639-1357	PCBA,MLB,1.4GHZ,SA 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8N,DDR3:SAMSUNG_2GB,CAPS:TY
639-1344	PCBA,MLB,1.4GHZ,SA 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF86,DDR3:SAMSUNG_4GB,CAPS:SS
639-1352	PCBA,MLB,1.4GHZ,SA 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8H,DDR3:SAMSUNG_4GB,CAPS:MU
639-1354	PCBA,MLB,1.4GHZ,SA 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8K,DDR3:SAMSUNG_4GB,CAPS:TY
639-1342	PCBA,MLB,1.4GHZ,MI 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF84,DDR3:MICRON_2GB,CAPS:SS
639-1346	PCBA,MLB,1.4GHZ,MI 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF88,DDR3:MICRON_2GB,CAPS:MU
639-1343	PCBA,MLB,1.4GHZ,MI 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF85,DDR3:MICRON_2GB,CAPS:TY
639-1347	PCBA,MLB,1.4GHZ,MI 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF89,DDR3:MICRON_4GB,CAPS:SS
639-1345	PCBA,MLB,1.4GHZ,MI 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF87,DDR3:MICRON_4GB,CAPS:MU
639-1340	PCBA,MLB,1.4GHZ,MI 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF82,DDR3:MICRON_4GB,CAPS:TY
639-1442	PCBA,MLB,1.4GHZ,EL 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4L,DDR3:ELPIDA_2GB,CAPS:SS
639-1443	PCBA,MLB,1.4GHZ,EL 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4M,DDR3:ELPIDA_2GB,CAPS:MU
639-1447	PCBA,MLB,1.4GHZ,EL 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4R,DDR3:ELPIDA_2GB,CAPS:TY
639-1441	PCBA,MLB,1.4GHZ,EL 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4K,DDR3:ELPIDA_4GB,CAPS:SS
639-1439	PCBA,MLB,1.4GHZ,EL 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4H,DDR3:ELPIDA_4GB,CAPS:MU
639-1440	PCBA,MLB,1.4GHZ,EL 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4J,DDR3:ELPIDA_4GB,CAPS:TY

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7557	1	LABEL,MLB,K16/K99	[EEE_DX7]	CRITICAL	EEE:DX7
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0L]	CRITICAL	EEE:DD0L
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0M]	CRITICAL	EEE:DD0M
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0N]	CRITICAL	EEE:DD0N
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0P]	CRITICAL	EEE:DD0P
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0Q]	CRITICAL	EEE:DD0Q
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0R]	CRITICAL	EEE:DD0R
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0T]	CRITICAL	EEE:DD0T
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0V]	CRITICAL	EEE:DD0V
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0W]	CRITICAL	EEE:DD0W
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0X]	CRITICAL	EEE:DD0X
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0Y]	CRITICAL	EEE:DD0Y
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD10]	CRITICAL	EEE:DD10
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD11]	CRITICAL	EEE:DD11
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD12]	CRITICAL	EEE:DD12
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD13]	CRITICAL	EEE:DD13
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD14]	CRITICAL	EEE:DD14
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD15]	CRITICAL	EEE:DD15
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF82]	CRITICAL	EEE:DF82
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF83]	CRITICAL	EEE:DF83
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF84]	CRITICAL	EEE:DF84
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF85]	CRITICAL	EEE:DF85
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF86]	CRITICAL	EEE:DF86
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF87]	CRITICAL	EEE:DF87
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF88]	CRITICAL	EEE:DF88
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF89]	CRITICAL	EEE:DF89
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8C]	CRITICAL	EEE:DF8C
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8D]	CRITICAL	EEE:DF8D
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8F]	CRITICAL	EEE:DF8F
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8G]	CRITICAL	EEE:DF8G
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8H]	CRITICAL	EEE:DF8H
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8J]	CRITICAL	EEE:DF8J
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8K]	CRITICAL	EEE:DF8K
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8L]	CRITICAL	EEE:DF8L
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8M]	CRITICAL	EEE:DF8M
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8N]	CRITICAL	EEE:DF8N
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4G]	CRITICAL	EEE:DG4G
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4H]	CRITICAL	EEE:DG4H
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4J]	CRITICAL	EEE:DG4J
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4K]	CRITICAL	EEE:DG4K
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4M]	CRITICAL	EEE:DG4M
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4N]	CRITICAL	EEE:DG4N
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4P]	CRITICAL	EEE:DG4P
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4Q]	CRITICAL	EEE:DG4Q
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4R]	CRITICAL	EEE:DG4R
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4L]	CRITICAL	EEE:DG4L
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4T]	CRITICAL	EEE:DG4T
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4V]	CRITICAL	EEE:DG4V

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
2GB	0
4GB	1

DIE REV	CFG 3
A	0
B	1

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1121	1	K99 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-6999	1	CMN PTS,PCBA,MLB,K99	CMNPTS	CRITICAL	K99_CMNPTS

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE

K99 BOM Variants

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DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC:BLANK
341T0261	1	IC ASSY,SMC EXTERNAL,K99	U4900	CRITICAL	SMC:PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM:BLANK
341T0262	1	IC ASSY,EFI UNLOCKED,K99	U6100	CRITICAL	BOOTROM:UNLOCKED
341T0263	1	IC ASSY,EFI,LOCKED,K99	U6100	CRITICAL	BOOTROM:LOCKED

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0681	138S0638		ALL	TAIYO YUDEN AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
353S2987	353S2988	HVDDLDO:FIXED	ALL	TPS71725DCK AS ALTERNATE FOR U2590
104S0023	104S0018		ALL	CYNTEC/DALE AS ALTERNATES
107S0139	107S0075		ALL	CYNCTEC AS ALTERNATE
138S0671	138S0673		ALL	TAIYO AS ALTERNATE
155S0578	155S0367		ALL	TAIYO AS ALTERNATE
376S0926	376S0610		ALL	FAIRCHILD AS ALTERNATE
155S0457	155S0329		ALL	MAGLAYERS AS ALTERNATE
377S0107	377S0066		ALL	ONSEMI AS ALTERNATE

BOM Groups

BOM GROUP	BOM OPTIONS
K99_COMMON	COMMON,ALTERNATE,PROJ:K99,K99_MISC,MCP89U:A03,K99_DEBUG:ENG,K99_PROGPARTS,SPI:41MHZ,LVDDR3:YES,WLAN_PCTL:HW,IPD_5V:S5_INT,IPD_3V3:S5
K99_MISC	DP_ESD,DP_PWR:SMC,VFRQ:SLPS3,HVDDLDO:FIXED,MCPHVDD:P2V5,MCPPLL_R:REG,S0PGOOD_BJT,ISL6259_SCREENED:YES,DPI2C:SMC
K99_PROGPARTS	BOOTROM:UNLOCKED,SMC:PROG
K99_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,LPCPLUS,VREFMRGN:YES,EFI_DEBUG,S0PGOOD_ISL,MCPPLL_LDO,S3_S0_LED
K99_DEVEL:PVT	LPCPLUS
K99_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG:YES,XDP
K99_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
K99_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_2GB	DRAM_CFG0:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_2GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_4GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:MICRON_4GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB
CAPS:SS	SS_CAP_2_2UF,SS_CAP_10UF,SS_CAP_1UF,SS_CAP_22UF
CAPS:MU	MU_CAP_2_2UF,MU_CAP_10UF,MU_CAP_1UF,MU_CAP_22UF
CAPS:TY	TY_CAP_2_2UF,TY_CAP_10UF,TY_CAP_1UF,TY_CAP_22UF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3792	1	CDC,QKWH,QS,1,2,10W,800,R0,1M,BGA	U1000	CRITICAL	CPU:1.2GHZ
337S3947	1	PDC,SLGFN,PRQ,1,6,10W,R0,3M,BGA	U1000	CRITICAL	CPU:1.6GHZ
337S3954	1	PDC,SLGAK,PRQ,1,4,10W,R0,3M,BGA	U1000	CRITICAL	CPU:1.4GHZ
337S3820	1	IC,MCP89U-A01,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A01
337S3868	1	IC,MCP89U-A02,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A02
337S3939	1	IC,MCP89U-A03,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A03
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,9X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,9X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,9X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,9X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_4GB
353S2392	1	IC,ISL6259,BATCHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6259_SCREENED:NO
353S2929	1	IC,ISL6259,BATCHARGER,3%,4C4MM,QFN28	U7000	CRITICAL	ISL6259_SCREENED:YES
607-6811	1	ASSEMBLY,SUBASSY,PCBA HALL EFFECT, K99	J6955	CRITICAL	

SYNC_MASTER=K24_MLB SYNC_DATE=07/20/2009

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

BRANCH

Revision History NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

03/05/2010: RELEASE 0.41.0 (MAJOR)-
- PAGE 9: ADDED Z0920 (OMIT) APN 998-3068 METAL TAB SYMBOL FOR MDP CONNECTOR
- PAGE 19: ADDED 10K R1954 APN 117S0007 PD ON MLB_RAM_CFG0 AS THERE IS NO INTERNAL PD ON GPIO 48
- PAGE 72: RENAMED =P5VS3_EN_L TO =P5VS3_EN AND =P3V3S5_EN_L TO =P3V3S5_EN
- PAGE 78: MOVED P3V3S5_EN_L NET FROM PIN 4 TO PIN 3 (NON-INVERTING) AND RENAMED IT TO P3V3S5_EN AS IT IS ACTIVE HIGH SIGNAL. LEFT PIN 4 NC
- PAGE 78: NO STUFF C7801
- PAGE 78: ALIASED =P0V9S5_EN TO CONNECT TO =PP3V3_S5_P0V0S5
- PAGE 78: DELETED Q7891 (PINS 3,4,5) SYMBOL AS P5VS3_EN_L IS ACTIVE HIGH SIGNAL (SO NO NEED TO INVERT) AND RENAMED IT TO P5VS3_EN. ALSO, CONNECTED IT TO PM_SLP_S4_L VIA RC NETWORK - R7813 & C7813
- PAGE 78: REPLACED R7813 WITH 0 OHMS APN 117S0002 FOR NOW

03/05/2010: RELEASE 0.42.0 (MAJOR)-
- PAGE 4: ADDED DRAM_CFG0:L TO RAM TABLES NOT CALLING OUT DRAM_CFG0:H, AND REMOVED DRAM_CFG1:H AS IT IS NO LONGER NEEDED
- PAGE 4: DELETED MODULE TABLE ENTRY FOR ZS0907 AS POR SYMBOL IS READY
- PAGE 4: ADDED MODULE TABLE ENTRY FOR Z0920 MLB STIFFENER: 806-1176
- PAGE 9: REPLACED ZS0907 WITH POR APN 870-1938 AND DELETED OMIT ATTRIBUTE
- PAGE 9: REPLACED POGO PIN ZS0906 WITH APN 870-1938 PER PD
- PAGE 19: REMOVED R1955 PULL-UP ON MLB_RAM_CFG1 (INTERNAL PULL-UP)
- PAGE 19: CHANGED R1956 PULL-DOWN TO 470 OHMS (STRONGER PD VS 8.5K PU) APN 117S0103
- PAGE 19: REPLACED R1957 WITH 10K APN 117S0007 TO BE CONSISTENT
- PAGE 78: ADDED BYPASS PROPERTIES TO C7895 AND C7896
- PAGE 78: CHANGED BASE NET FOR PM_SLP_S4_DLY_L PER WILL

03/05/2010: RELEASE 0.43.0 (MAJOR)-
- PAGE 2: REPLACED THIS PAGE WITH QUANTA'S UPDATED ONE
- PAGE 4: SWITCHED BOM TABLE TO USE SCREENED ISL6259 PART
- PAGE 4: ADDED APN 376S0895 UNDER MODULE PART TABLE FOR Q7220 & Q7225 PER DAYU FOR PART SUPPLY ISSUE
- PAGE 4: MOVED SMS_YES BOM OPTION FROM K99_MISC TO DEVEL_BOM
- PAGE 4: UPDATED MICRON 2GB APN 333S0557 IN THE BOM TABLE
- PAGE 9: FIXED MCPCOREISNS SIGNALS ALIASES PER WILL'S CHANGES ON K16
- PAGE 39: REMOVED CRITICAL ATTRIBUTE FROM THE BOM TABLE AS IT IS NOT NEEDED
- PAGE 70: NO STUFF Q7080, D7005,Q7055 AND F7040 FOR NON-FUNCTIONAL BOARD
- PAGE 72: ADDED OMIT BOM OPTION TO Q7220 & Q7225 AS SYMBOL IS NOT READY
- PAGE 72: CHANGED R7246 AND R7247 TO 1.69K, 1% APN 118S0134 PER VENDOR
- PAGE 72: CHANGED R7216 AND R7256 TO 4.02K, 1% APN 118S0354 PER VENDOR
- PAGE 72: CHANGED C7237 AND C7239 TO 1000PF, 10% APN 132S0122 PER VENDOR
- PAGE 76: CHANGED OCP TEXT NOTE PAR VENDOR
- PAGE 76: CHANGED R7641 AND R7642 TO 1.78K, 1% APN 118S0144 PER VENDOR
- PAGE 78: ADDED NC SYMBOL TO PIN 5 OF U7896

03/07/2010: PROTO1 NON-FUNCTIONAL AGILE RELEASE 1.0.0 (FAB)-
- NON-FUNCTIONAL PROTO 1 OK2FAB RELEASE!!!

3/19/2010: RELEASE 1.1.0 (MAJOR)-
- PAGE 4: REMOVED SMS_YES BOM OPTION FROM K99 DEVEL:ENG BOM GROUP. INSTEAD, ADDED SMS:NO TO K99_MISC [ALSO SEE BELOW CHANGES FOR PAGES 50,59]
- PAGE 50: ADDED BOM OPTION ATTRIBUTE SMS:NO TO R5093 PU ON SMS_INT_L. IDEA IS TO PULL THIS NET TO S5 RAIL WHEN SMS IN NOT STUFFED, ELSE PU TO S3 RAIL (PAGE 59) PER RADAR 7765442
- PAGE 52: CONNECTED SMC 0 SMBUS INTERFACE TO THE TCON-A CHIP IN THE INTERNAL DISPLAY. ALSO, PROVIDED 0 OHMS STUFFING OPTIONS TO BE DRIVEN FROM MCP89 0 SMBUS [R5240-R5243 APN 117S0002] PER RADAR 7749046
- PAGE 59: REPLACED BOM OPTION SMS_YES WITH SMS:YES
- PAGE 59: ADDED 10K R5924 PU ON SMS_INT_L TO =PP3V3_S3_SMS WITH BOM OPTION ATTRIBUTE SMS:YES PER RADAR 7765442
- PAGE 70: STUFF BACK Q7080, D7005,Q7055 AND F7040
- PAGE 75: REPLACED L7560 WITH 10X10X3MM APN 152S1236 PER RADAR 7769386
- PAGE 90: ROUTED NEWLY ADDED =I2C_TCON_SDA/SCL TO PINS 1 & 30 OF J9000 RESPECTIVELY PER RADAR 7749046
- PAGE 93: ADDED 3300PF APN 132S0241 C9302 CAP ON DP_CA_DET TO GND PER RADAR 7742010
- PAGE 108: ADDED SMBUS_SMC_0_S0_SCL/SDA_R CONSTRAINTS SET

03/24/2010: Release 1.2.0 (MAJOR)-
- Text sizes have been fixed - safe to sync
- Page 8: Renamed PP3V3_S5_LCD to PP3V3_S0_LCD
- Page 8: Moved PP3V3_S0_LCD & PP3V3_S5_DP_PORT_PWR to S5 rail
- Page 7: Added =I2_TCON_SCL/SDA FCTs under INT_DP_FUNC_TEST group
- Page 12: After syncing from K16, deleted C1273 as it NA to K99
- Page 90: After syncing, renamed PP3V3_S5_LCD to PP3V3_S0_LCD

Sync'ed ALL but pages 1-9,28,47,69,70,74,75 and 97 from K16
*Please NOTE that some of the below changes were already part of 1.1 release. Below list depicts all the changes since 3/1 K16 release *

- Page 12: Fixed invisible pins on CPU bypass caps. Also changed all OMITs to OMIT_TABLEs and performed other cleanup
- Page 14: Swapped BCLK_IN_N/P after library symbol refresh
- Page 17: Added CKPLUS_WAIVE properties to VDD_IFPx pins that are legally grounded on K16
- Page 19: Removed PM_SLP_S5_L alias. Other cleanup to make all CRefs visible
- Page 19: Removed pull-up on MLB_RAM_CFG1 (internal pull-up), changed pull-down to 470 ohms. Added pull-down on MLB_RAM_CFG0, made both pull-up and pull-down 10K
- Page 25: Added MCPHVDD LDO, SC-70 version. Added 1uF 0201 input cap and 10K pull-up resistor, BOMOPTIONed same as LDO. L2590 retained with MCPHVDD:P3V3 BOMOPTION
- Page 25: Added voltage divider for HVDD LDO. OMIT_TABLE'd U2590, added tables for fixed (2.5V Intersil) and adjustable (TI) regulators
- Page 39: Removed CRITICAL flag from 0-ohm resistor table
- Page 49: PB3 changed from SMC_DRAM_S3_PWRDN to SMC_SLPS5_L. P74 changed from PM_SLP_S4_L to SMC_DP_HPD_L. P75 changed from PM_SLP_S5_L to PM_SLP_S4_L
- Page 49: C4902 changed from 0805 to 0603 to free up some layout space for MCP VCore regulator
- Page 50: Added SMS:NO BOMOPTION to SMS_INT_L pull-up. Other cleanup including deleting unused alias for SMC_PB3
- Page 50: Added 2 resistors to control DP_PWR and one to connect DP_EXT_HPD_L to SMC. Updated netname on R5090 and added BOMOPTION of DP_PWR:S0
- Page 52: Added TCON I2C block and R's to connect to SMC 0 and MCP 0
- Page 53: Removed PP prefix from non-power nets. Added OMIT_TABLE to buses. Other cosmetic cleanup including grid compliance C5310 for vendor control
- Page 59: Sync'ed with K99 (adds R5924, S3 pull-up on SMS_INT_L), plus lots of cleanup including removing PP prefix from signal net, correcting BYPASS & PLACE_NEAR properties, correcting offpages, etc
- Page 72: Changed Q7220 & Q7225 to 376S0895 per Dayu's request. Fixed netnames on switcher enables, removing _L suffixes since they are active-high
- Page 72: Value changes to C7237/C7239/R7216/R7246/R7247/R7256 per Dayu. Changed C7288 to match C7218. Removed alias that was serving no purpose and was incorrect since it lacked a MAKE_BASE anyhow
- Page 76: Value changes to R7641/R7642 and OCP note correction per Dayu
- Page 78: Removed RAM power-down circuit, reconnecting =DDRREG_EN to original net
- Page 78: Disconnected half of Q7891 from 5V S3 power sequencing, gate left indicated as unused. Removed inverter from P5VS3_EN and reconnected P3V3S5_EN to be non-inverted. R7813 changed from pull-up to series R (0-ohms). P0V9S5_EN changed to alias to 3.3V S5 rail. Cleaned up page including fixing grid issues. Added BYPASS properties to C7895 and C7896. Changed base net for PM_SLP_S4_DLY_L
- Page 93: Added RC between DP_CA_DET and DDC bypass FETs. Also cleaned up page, adding offpages, fixed grid issues, made power nets convention-compliant and added note about DP_CA_DET pull-up / FET Vgs reqirements
- Page 93: Added RC between DP_CA_DET and DDC bypass FETs. Also cleaned up page, adding offpages, fixed grid issues, made power nets convention-compliant and added note about DP_CA_DET pull-up / FET Vgs reqirements
- Page 93: Added CKPLUS_WAIVE properties to _P nets connecting to FET DRAIN pins
- Page 94: Renamed DP_PWR nets to indicate 'SW' state instead of 'S0'. Switch input changed from PM_SLP_S3_L to =DP_PWR_EN. HPD_L netname changed, offpage added and pull-up changed to DP_PWR. Other cleanup including removing PLACE_NEARs that should be handled via constraints, OMIT_TABLEs for caps, CRITICAL flags on common-mode chokes and cosmetic changes
- Page 108: Added net constraints for diffpairs reported by diffpNoPhysNet report (except for 4 false errors). Other cleanup including removing some unnecessary net properties

03/25/2010: Release 1.3.0 (MAJOR)-
- Page 4: Fixed DRAM CFG table - swapped CFG 1 and 0 columns
- Page 4: Updated EEE numbers
- Page 4: Pulled new 607-XXXX APN and added K99_CMNPTS BOM option corresponding to this new sub-BOM consisting of common parts between 18 BOMs
- Page 4: Replaced K99_COMMON with K99_CMNPTS in the BOM variant table
- Page 4: Replaced K99_SS/MU/TY_CAP BOM option with better nomenclature - CAPS:SS/MU/TY
- Page 4: Removed K99_ prefix from K99_DDR3_ BOM Group
- Page 4: Deleted 376S0895 APN module parts table entry as it is already duplicated on page 72
- Page 4: Deleted module table entry for 806-1176 as actual symbol has been added
- Page 9: Replaced Z0920 with POR stiffener symbol for APN 806-1176 and deleted OMIT
- Page 46: Replaced Q4690 with single port switch APN 353S1930 (Higher DCR) to fix USB short issue
- Page 46: Changed BOM attribute OMIT to OMIT_TABLE for C4690 & C4695
- Page 54: Changed R5418 to 4.53K 0201 APN 118S0384
- Page 54: Changed R5471 to 4.53K 0402 APN 114S0281
- Page 72: Changed R7246, R7247 to 1.87K, 1% APN 118S0159 per Dayu
- Page 72: Changed R7216, R7256 to 3.16K, 1% APN 118S0289 per Dayu
- Page 72: Changed C7236, C7238 to 0.01uF, 10% APN 132S0097 per Dayu
- Page 72: Changed C7237, C7239 to 100pF, 10% APN 131S0287 per Dayu
- Page 97: Replaced U9701 with new improved E00 version APN 353S2967
- Page 97: Changed R9704 to 33 ohms APN 117S0080 per Kiran
- Page 97: Stuffed C9704 per Kiran

3/26/2010: Release 1.4.0 (MAJOR)-
- Page 4: Added 376S0895 as an alternate for 376S0749 per Dayu
- Page 4: Added 138S0681 as an alternate for 138S0638 per GSM
- Page 4: Added 138S0676 as an alternate for 138S0635 per GSM
- Page 4: Removed alternates that were NA to K99
- Page 72: Deleted OMIT_TABLE attribute from Q7220 & Q7225. Also deleted the BOM table. Plan is to use 376S0895 as alternate instead

03/30/2010: Release 1.5.0 (MAJOR)-
- Page 4: Deleted 376S0895 alternate part entry to avoid mixing of vendors between high & low side FETs per Dayu
- Page 4: Deleted DPI2C:SMC BOM OPTION as eDP I2C Bus won't be routed on Proto 1
- Page 4: Changed BOM OPTION SPI:25MHz to 62MHz
- Page 9: Changed BOM OPTION attribute of ZS0904 to OMIT_TABLE
- Page 10-11: Changed BOM OPTION attribute of U1000 to OMIT_TABLE
- Page 14-20: Changed BOM OPTION attribute of U1400 to OMIT_TABLE
- Page 25: Changed BOM OPTION attribute of C2600 to OMIT_TABLE
- Page 31-34: Changed BOM OPTION attribute of U3100-U3430 to OMIT_TABLE
- Page 35-36: Changed BOM OPTION attribute of all caps to OMIT_TABLE
- Page 49: Changed BOM OPTION attribute of U4900 to OMIT_TABLE
- Page 52: Changed R5290 & R5291 to 2K APN 118S0174 per RADAR# 7810865
- Page 61: Changed BOM OPTION attribute of U6100 to OMIT_TABLE
- Page 69: Changed R6905 to 10 Ohms APN 101S0089 & C6990 to 2.2uF APN 138S0672 to improve noise immunity & reduce inrush stress, per Dayu
- Page 69: Changed BOM OPTION attribute of U6955 to OMIT_TABLE
- Page 69: Changed BOM OPTION attribute of C6999 to OMIT_TABLE
- Page 70: Changed BOM OPTION attribute of U7000 to OMIT_TABLE
- Page 72: Replaced Q7220 & Q7225 with APN 376S0895 (RJK03E0) per Dayu
- Page 72: Changed R7220 to 41.2K APN 118S0360 to boost 5V, per Dayu
- Page 73: Replaced Q7330 with APN 376S0749 (SIS426) per Dayu
- Page 76: Replaced Q7630 & Q7635 with APN 376S0895 (RJK03E0) per Dayu
- Page 77: Changed R7751 to 2.55K APN 118S0234 & R7752 to 20K APN 118S0175 to improve noise immunity & reduce inrush stress, per Dayu

03/31/2010 - Proto 1 Agile Release 2.0.0 (FAB)
- Proto 1 Ok2FAB Agile Release!!!

3/31/2010: Proto 1+ Release 2.1.0 (MAJOR)
- Page 4: Activated PROJ:K99 BOMOPTION to select proper APN for U9701
- Page 97: Changed BOM OPTION attribute of C9797 to OMIT_TABLE after syncing from K16

Sync'ed from K16
-Page 90: Added Q9090 isolation FET to support LCD panel power-down per radar 7761747
-Page 97: Reversed previous change, U9701 back to 353S2896, handled via a table now to support/clarify different values for K16/K99
-Page 108: Added constraints for new nets on page90, I2C_TCON_SCL/SDA_CONN per radar 7761747

3/31/2010: Proto 1+ Release 2.2.0 (MAJOR)
- Page 97: Swapped pins of R9700 to match original orientation before syncing with K16
- Page 97: Deleted OMIT_TABLE BOM option attribute from C9797 and replaced it with actual POR APN 138S0673 symbol. Also, deleted it from BOM table as it is no longer required

5/12/2010: Proto 1+ Agile Release 3.0.0 (FAB)
- Proto 1+ OK2FAB Agile Release!!!

5/17/2010: Release 3.1.0 (Major)-
<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V
- Page 4: Added APNs 353S2987 & 353S2988 as alternates for 353S2986

<rdar://problem/7964678> K99 MLB BOM: Change MCP APN to A03 version
- Page 4: Added MCP89U:A03 BOM table. Changed K99_Common to call out A03

<rdar://problem/7861271> K99 MLB: Set SPI operating frequency to 42MHz
<rdar://problem/7851979> K16/K99: Set SPI operating frequency to 42MHz
- Page 4: Changed SPI:62Mhz to SPI:41MHZ BOM option

<rdar://problem/7838450> K99 MLB: WoW / WoL power control architecture change
- Page 4: Added WLAN_PCTL:HW to K99_Common

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
<rdar://problem/7953783> K99 IPD power regulator new design
- Page 4: Added IPD_PWR:S5 to K99_Common
- Page 8: Aliased =PPBUS_5V_S5 to PPBUS_G3H signal

<rdar://problem/7825507> K99 MLB BOM: Change label P/N
- Page 4: Replaced label APN 826-4393 with 825-7557

<rdar://problem/7749046> K99 MLB: Connect SMBUS to internal display connector
- Page 7: Renamed PP3V3_LCDVDD_SW_F to PP3V3_SW_LCD to match page 90, making it convention compliant power net

<rdar://problem/7779132> K99 MLB: Implement deeper sleep S4 state
- Page 7: Renamed PP3V3_S0_DPPWR to PP3V3_SW_DPPWR to match page 94 changes, making it convention compliant power net

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 7: Removed SYS_LED_ANODE_R
- Page 8: Removed =PP3V3_S5_PWRCTL alias

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 8: Added =PP3V3_S5_TPAD to PP3V3_S5 net

<rdar://problem/7963570> K99 MLB: Remove SMS circuit from layout
- Page 59: Deleted csa page as SMS is no longer POR

<rdar://problem/7795028> K99 MLB: 5V/3V3 power supply BOM changes per characterization
- Page 74: Changed C7451/C7452 to same APN 131S0287 as C7237/C7239 for BOM consolidation

<rdar://problem/7993241> K99 MLB: Cleanup of CheckPlus warnings/errors
- Page 4: Deleted ZS0904 entry from the module parts table as symbol is ready
- Page 9: Renamed stiffener Z0920 to MT0900, similar to K16
- Page 9: Tagged POGOS and MT0900 as CRITICAL
- Page 9: Replaced ZS0904 with actual symbol for APN 870-1940 and deleted OMIT_TABLE
- Page 9: Cleaned-up TP/NC P27 errors
- Page 74: Renamed VSNS nets to VSEN to match page 100 constraints and deleted these nets from constraints table on the same page
- Page 79: Changed OMIT associated with C7980 to OMIT_TABLE
- Page 99: Changed OMIT associated with all caps to OMIT_TABLE

<rdar://problem/7935301> K99 MLB BOM: Change BOM per CE request
- Page 75: Added Critical attribute to R7560
- Page 97: Added Critical attribute to R9700

Synced ALL but pages 1-9,12,28,47,69,70,74,75 and 97 from K16
** Didn't sync pages 79 & 99 as K16 need to sync it first from K99 to fix OMIT_TABLE attribute as mentioned above**

<rdar://problem/7749046> K99 MLB: Connect SMBUS to internal display connector
- Page 52: Added notes about I2C addresses on panel, may not be 100% accurate yet

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 13: Changed XDP SMBus nets to =I2C_XDP_* for new aliases on page52
- Page 52: Added XDP to MCP_0 SMBus diagram
- Page 76: Cleaned-up page, including correcting application of two PLACE_NEAR properties and changing an OMIT to OMIT_TABLE

<rdar://problem/7779132> K99 MLB: Implement deeper sleep S4 state
- Page 50: Added PLACE_NEAR property on R5022 to ensure no stub in fallback case.

<rdar://problem/7794868> K99 MLB: Change to single USB port power switch
- Page 46: Corrected Refdes from Q4690 to U4690

<rdar://problem/7993278> K99 MLB: Schematic sync with K16 MLB
- Page 26: Sync'ed with K16, OMIT changed to OMIT_TABLE
- Page 73: Sync'ed with K16, OMITs changed to OMIT_TABLE and cosmetic clean-up

<rdar://problem/7994057> K99 MLB: Need to add Need_TP=True property to CPU
- Page 10: Added Need_TP=True attribute to pin E37 & D40

<rdar://problem/7871167> K99 MLB: Change RC on CPUVCORE PMON output
- Page 54: Changed R5471 from 4.53K to 15K for higher PMON pin sink capability
- Page 54: Changed C5470 from 0.22UF to 68nF 10%. Only one in the library

<rdar://problem/7934374> K99 MLB BOM: Replace 376S0868 with 376S0912
- Page 23: Changed Q2300 from 376S0868 to 376S0912

<rdar://problem/7838450> K99 MLB: WoW / WoL power control architecture change
- Page 78: Swapped unused gate to Q7890 and SMC_Adapter_En fet to Q7891.
- Page 78: Added BOM Options WLAN_PCTL:HW to Q7891 both halves
- Page 78: Added R7891 0 ohm 5%
- Page 78: Added Bom option WLAN_PCTL:SW to R7891

<rdar://problem/7871918> K99 MLB: Investigate larger replacement for LCD backlight fuse
- Page 98: Changed F9800 to 0603 package APN 740S0115

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
<rdar://problem/7953783> K99 IPD power regulator new design
- Page 57: L5720.2 now connects to PP5V_S5_LDO
- Page 77: Added U7760 and surrounding circuits. BOM table need to replace later
- Page 77: Added R7760 for switching capability
- Page 77: Added min line and neck width properties to PP5V_S5_LDO
- Page 78: Aliased =PP5V_S5_LDO to =P5V3V3_REG_EN
- Page 78: Added R7848 and C7848 0ohm 0.47F (NO STUFF) stuffing options

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 57: Added U5730 & R5731 for power switch on PP3V3_TPAD
- Page 57: Added U5750 USB Mux
- Page 57: Added R5751 (NO STUFF) to bypass U5750 MUX
- Page 78: Added =USB_TPAD_MUX_EN to DDRREG_EN

<rdar://problem/7935301> K99 MLB BOM: Change BOM per CE request
- Page 39: Added Critical attribute to Q3920, U3940
- Page 54: Added Critical attribute to Q5401,U5413
- Page 77: Removed Critical from C7710, C7715
- Page 98: Added Critical attribute toF9800

5/19/2010: Release 3.2.0 (Major)-
<rdar://problem/8006037> K99 MLB: Change RC Filter Values on AMON and BMON
- Page 54: Changed R5481 to 150K APN 118S0106 and C5487 to 0.0068uF APN 132S0009
- Page 54: Changed R5401 to 300K APN 118S0276 and C5490 to 0.0033uF APN 132S0049

<rdar://problem/7986457> K99 MLB: Change LIO Flex connector J4700 to accommodate new LIO Flex
- Page 47: Replaced J4700 with new POR connector APN 516S0862

<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V
- Page 4: Deleted APN 353S2988 entry from the alternate table
- Page 4: Replaced APN 353S2987 entry with APN 353S3047 (TI) as an alternate
- Page 25: Replaced U2590 with 2.85V LDO APN 353S3048 (MICREL)
- Page 25: Replaced APN 353S2986 with 353S3048 in the BOM table too for HVDDLDO:FIXED

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 57: Connected a new PME signal SMC_PME_S4_L to pin 2

<rdar://problem/8004981> K99 MLB: Connect eDP SMBUS interface to SMC SMBUS 0
- Page 4: Added BOM option DPI2C:SMC to stuff R5242 & R5243

<rdar://problem/7963570> K99 MLB: Remove SMS circuit from layout
- Page 4: Deleted SMS:NO BOM option as SMS has been removed
- Page 50: Deleted BOM option SMS:NO from R5093
- Page 52: Deleted Accelerometer block from the SMBUS page

<rdar://problem/8007333> K99 MLB: Stuff R7872 to enable output connection of ISL power monitor to ALL_S_PWRGD
- Page 78: Added BOM option S0PGOOD_ISL to R7872

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 8: Added =PP3V3_S5_DBGLEDS alias to =PP3V3_S3_FET for debug LEDS (like K16)
- Page 60: Changed PP3V3_S3_TPAD_CONN to PP3V3_TPAD_CONN
- Page 69: Renamed PP3V3_S3 going to debug LEDs to =PP3V3_S5_DBGLEDS

<rdar://problem/8007524> K99 MLB: Stuff C9799 to provide better phase margin
- Page 97: Stuff C9799

<rdar://problem/8007560> K99 MLB: Change min neck width to meet layout requirements
- Page 4: Changed min neck width of PP3V3_S3 to 0.2mm
- Page 8: Changed min neck width of PP5V_S3 to 0.2mm
- Page 74: Deleted PPVPS_CS_P/N nets from the constraints set as the bottom of the page
- Page 97: Changed min neck width of PPBUS_SW_BKL to 0.25mm

05/19/2010: Release 3.3.0 (Major)-
<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 69: Fixed name =PP3V3_S3_DBGLEDS (= sign was missing)

05/21/2010: Release 3.4.0 (Major)-
<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 2: Updated CPU block to reflect 1.6GHz

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
- Page 77: Changed IPD_PWR:S5 to IPD_5V:S5 LDO BOM option to use internal LDO of 5V/3.3V switcher for IPD 5V supply

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 4: Added IPD_3V3:S5 BOM option under K99_COMMON to select 3.3V S5 power supply
- Page 8: Renamed =PP3V3_S3_TPAD_CONN and =PP5V_S3_TPAD to PP5V_S3_TPAD_FILT
- Page 8: Added =PP3V3_SMC_PME alias to PP3V3_S5

<rdar://problem/8009884> K99 MLB: Add new CPU APN for U1000
- Page 4: Added new CPU APN [illegible] to the module part table. And, updated BOM variant table to call out this new APN

<rdar://problem/8011930> K99 MLB: Remove SIL BOM option as SIL is not POR
- Page 4: Removed SIL BOM option from the development BOM

<rdar://problem/8007560> K99 MLB: Change min neck width to meet layout requirements
- Page 8: Changed min neck width of PP3V3_S3 to 0.3mm
- Page 46: Fixed line/neck width attributes from =PP3V3_S3_WLAN as duplicates

<rdar://problem/7825507> K99 MLB BOM: Change label P/N
- Fixed typo in APN (first column)

<rdar://problem/7986457> K99 MLB: Change LIO Flex connector J4700 to accommodate new LIO Flex
- Page 47: Connected pin 38 to GND

<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V
- Page 4: Added APN 353S2986 (MICREL) as an alternate for 353S2986
- Page 4: Added APN 353S2987 (TI) as an alternate for 353S2986
- Page 4: Deleted 353S3047 entry from the alternate table
- Page 25: Reverted U2590 back to the 2.5 LDO APN 353S2988
- Page 25: Replaced APN 353S3048 with 353S2986 in the BOM table for U2590 as primary for HVDDLDO:FIXED

Synced ALL but pages 1-9,12,28,47,69,70,74,75 and 97 from K16 - changes below
** Didn't sync page 8 as K16 need to sync it first from K99 to remove Accelerometer**
** Didn't sync page 25 as K16 needs to sync it first from K99 to revert to 2.5 LDO
** Didn't sync page 40 as K16 needs to sync it first from K99 for above change**

<rdar://problem/8007560> K99 MLB: Change min neck width to meet layout requirements
- Page 24: Changed PPVCORE_SW_MCP_GFX min neck width to 0.12mm for routing

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
- Page 77: Changed IPD_PWR:S3 to IPD_5V:S3 BOM option
- Page 77: Changed IPD_PWR:S5 to IPD_5V:S5 BOM option
- Page 77: Added R7761 BOM bypass option to use internal LDO of 5V/3.3V switcher for IPD 5V supply. Added BOM option for R7761
- Page 77: Added place near [illegible] to R7761 to avoid long stub

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 50: Changed R5076 to a PU to =PP3V3_SMC_PME. And, renamed SMC_BS_ALERT_L to SMC_PME_S4_L
- Page 57: Changed IPD_PWR:S5 to IPD_3V3:S5 BOM option
- Page 57: Changed IPD_PWR:S3 to IPD_3V3:S3 BOM option
- Page 57: Removed Q5750, R5751,R5759 and C5750 USB IPD Debug Mux as it is not needed
- Page 57: Renamed pins 5 & 6 to USB_TPAD_CONN_P/N as before
- Page 57: Renamed pin 10 to PP5V_TPAD_FILT
- Page 78: Removed =USB_TPAD_MUX_EN alias to DDREG_EN as MUX has been removed

<rdar://problem/7779132> K99 MLB: Implement deeper sleep S4 state
- Page 49: Added alias for PM_SLP_S4_L to PM_SLP_S4
- Page 49: Changed port P84 from SMC_DP_HPD_L to PM_SLP_S4_L
- Page 49: Changed port P85 from PM_SLP_S5_L to SMC_DP_HPD_L
- Page 50: Removed R5095 PU resistor on SMC_PB6

05/26/2010: Release 3.5.0 (Major)-
Synced ALL but pages 1-9,12,28,47,69,70,74,75 and 97 from K16 - changes below
** Didn't sync page 8 as K16 need to sync it first from K99 to remove Accelerometer**
** Didn't sync page 46 as K16 needs to sync it first from K99 to remove neck width from PP3V3_S3_WLAN**

<rdar://problem/8033353> K99 MLB: Change to dual USB port power switch
- Page 46: Changed USB port power switch U4690 back to dual port TPS2052B APN 353S2298

<rdar://problem/7744955> K99 Proto0 Task: Characterize Voltage/Current/Temperature Sensors
- Page 53: For IZDP, change U5360 to INA210 (APN : 353S2873)
- Page 53: Changed R5324 to 118 Ohms, APN : 114S0227

<rdar://problem/8033256> K99 MLB: Implement 3V3 S5 bleed resistor to satisfy IPD Cumulus power sequencing on shutdown
- Page 77: Added R7899, [illegible] 0603 (value to be confirmed later) pull-up to =PP3V3_S5_REG and connected R7890 to pin [illegible] of Q7890 whose gate tied to P3V3S5_EN_L, Q7890.4 to GND and Q7840 output to P3V3S5_EN_L

<rdar://problem/8007560> K99 MLB: Change min neck width to meet layout requirements
- Page 108: Changed Therm, Sense, Audio line-to-line spacing to 1:1 instead of 2:1

05/28/2010: Release 3.6.0 (Major)-
<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V (not POR)
- Page 4: Removed MIC5366 from alternate BOM table as it is primary now and replaced 353S2986 with 353S2988 making it its alternate
<rdar://problem/8036805> K99 MLB BOM: Implement MCP VCORE characterization changes
- [illegible] table as it's been replaced per GSM(see below)
- [illegible]

Synced ALL but pages 1-9,12,28,47,69,70,74,75 and 97 from K16 - changes below

<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V (not POR)
- Page 25: Changed BOM table from ISL 353S2986 to MIC5366 353S2988, as Intersil is NOT POR

<rdar://problem/8027047> K99 MLB BOM: Swap 132s0247 w/132s0257, 138s0621 w/138s0653, 138s0635 w/138s0654
- Page 39,34,35,49: Swapped 132s0247 w/132s0257 per GSM
- Page 39,34: Swapped 138s0621 w/138s0653 per GSM
- Page 49,72: Swapped 138s0635 w/138s0654 as per GSM

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
- Page 77: Fixed BOM table attribute to attach BOM option value to TBL_BOMOPTION

6/4/2010: EVT Agile Release 4.0.0 (FAB)-
*** EVT OK2FAB Agile Release ***
- No changes since last release 3.6.0
- This release matches Quanta's official BOM for EVT build
- Upcoming changes (Acoustic, Alternates) will be reflected in 4.1 major release, which will match Quanta's deviations for EVT

06/06/2010: Release 4.1.0 (MAJOR)-
<rdar://problem/8065425> K99 MLB: Add new CPU APN for U1000 - SU9400
- Page 4: Added 4 new K99_XXXX BOMs corresponding to 1.4GHz SU9400 CPU
- Page 4: Added SU9400 as a new EEEE corresponding to the new BOMs
- Page 5: Added SU9400 1.4GHz APN 337S3954 to the BOM module parts table

<rdar://problem/8065431> K99 MLB: Add new Elpida 1Gb memory APN - 333S0565
- Page 4: Added new DDR3:ELPIDA_2GB BOM group and set appropriate CFG bits
- Page 4: Added Elpida DRAM to the CFG table
- Page 5: Added Elpida 1Gb APN 333S0565 to the BOM module parts table with DRAM_TYPE: ELPIDA_2GB BOM option

<rdar://problem/8066033> K99 MLB BOM: Change CPU VCORE 0603 bypass caps for acoustics
- Page 4: Added new BOM options CAP_22UF_MU, CAP_22UF_TY & CAP_22UF BOM options for corresponding vendor BOM group
- Page 49: Added OMIT_TABLE BOM option to C4902
- Page 73: Added OMIT_TABLE BOM option to C7360 & C7361
- Page 78: Added OMIT_TABLE BOM option to C7840
- page 110: Added BOM config tables for 22uF caps for three vendors - Samsung (138S0635), Murata (138S0676) and Taiyo (138S0688). Also assigned C1200-C1231, C4902, C7360, C7361 and C9480 to these groups
- Page 110: Removed C1200-C1231 from 10uF caps BOM config table

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 6: Deleted revision history and replaced it with BOM module parts, Programmable parts and Alternate parts tables as space was limited

<rdar://problem/8065429> K99 MLB: Add alternates per GSM
- Page 5: Added APN 107S0133 as an alternate for APN 118S0018 per GSM/CE
- Page 5: Added APN 118S0065 as an alternate for APN 118S0075 per GSM/CE
- Page 5: Added APN 155S0456 as an alternate for APN 155S0367 per GSM/CE
- Page 5: Added APN 155S0530 as an alternate for APN 155S0453 per GSM/CE
- Page 5: Added APN 376S0757 as an alternate for APN 376S0604 per GSM/CE

<rdar://problem/8064296> K99 MLB: Change pull-up values for SMC 0 SMBus for TCON I2C
- Page 52: Changed R5250 & R5251 with 2K APN 117S0052 to reduce rise time

07/07/2010: Release 4.2.0 (MAJOR)-
<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Moved BOM group table on page 4 to page 5 for space limitations

<rdar://problem/8065425> K99 MLB: Add new CPU APN for U1000 - SU9400
- Page 4: Updated SU9400 BOMs with correct EEEEs (Elpida's still pending)
- Page 4: Updated Label table with correct EEEEs for SU9400 configs

<rdar://problem/8151087> K99 MLB BOM: Add new Elpida 2Gb memory
- Page 4: Added 12 new BOMs corresponding to Elpida 2GB and 4GB configs
- Page 5: Added DDR3:ELPIDA_4GB BOM group
- Page 5: Added DRAM_TYPE:ELPIDA_4GB BOM option to the Module Parts table (2Gb APN is not ready yet- using 2Gb Micron APN as a placeholder)

<rdar://problem/8168390> K99 MLB BOM: Swap 155S0556-> 155S0578, fix 0402 pad with 0603
- Page 5: Changed 155S0556 to 155S0578 to address the 0603 0402 mismatch alternate parts

<rdar://problem/8151651> K99 MLB BOM: Reduce CPU VCORE 0603 bypass caps
- Page 12: Changed BOM option attribute of C1200,C1201,C1202,C1203,C1204, C1205,C1206,C1207,C1208,C1209,C1211,C1212,C1213,C1215,C1216, C1219, C1220,C1221,C1222,C1224,C1225,C1228,C1229,C1231 from OMIT_TABLE to NOSTUFF

Synced ALL but pages 1-9,12,28,47,69,70,74,75 and 97 from K16

<rdar://problem/8118512> K99 MLB BOM: Swap 155S0423 -> 155S0559, Supply Constraint (TDK)
- Page 90: Changed FL9000, FL9001 from 155S0423 to 155S0559
- Page 94: Changed FL9400-FL9403 from 155S0423 to 155S0559

<rdar://problem/8151651> K99 MLB BOM: Reduce CPU VCORE 0603 bypass caps
- Page 110: Removed caps listed above on page 12 from the BOM table as these would get NOSTUFF'ed

7/12/2010: Release 4.3.0 (MAJOR)-
<rdar://problem/8151087> K99 MLB BOM: Add new Elpida 2Gb memory
- Page 4: Updated BOM options table with correct EEEEs for Elpida configs
- Page 4: Added label table with correct EEEEs for Elpida configs
- Page 5: Updated Elpida 2Gb configs with correct APN 333S0566

<rdar://problem/8180364> K99 MLB BOM: Remove 806-1176 stiffener
- Page 9: Deleted CRITICAL attribute from MT0900 and NOSTUFF'ed it

7/22/2010: Release 4.4.0 (MAJOR)-
<rdar://problem/8175202> K99 MLB: Move MCP Temp Sensor to SMC B SMBUS
- Page 52: Move MCP_TEMP_I2C connections to SMC B Bus
- Page 52: NOSTUFF'ed R5250 & R5251
- Page 52: Changed MCP_TEMP I2C address note to reflect 0XD8/0XD9
- Page 55: Changed R5536 to 15K APN 118S0105 to set ADDR = 0XD8/0XD9. Updated schematic note too for address

<rdar://problem/8141673> K99 MLB: Change eDP connector J9000 pinout
- Page 90: Changed pine 2 to NC and connected pin 4 to PPVOUT_SW_LCDBKLT

<rdar://problem/8224515> K99 MLB: Remove Q9090 isolation FET
- Page 90: Removed Q9090 FET and directly connected TCON I2C bus J9000
- Page 90: Deleted =I2C_TCON_SCL/SDA_CONN net names and kept =I2C_TCON_SCL/SDA

<rdar://problem/8224857> K99 MLB: Replace APN 155S0559 with 155S0423 (incompatible pad sizes)
- Page 90: Changed FL9000 and FL9001 back to the original APN 155S0423
- Page 94: Changed FL9400-FL9403back to the original APN 155S0423

<rdar://problem/8224921> K99 MLB: Change R9714 (BKLT_ISET) resistor to 18.2K 1% APN 118S0155
- Page 97: Change R9714 to 18.2K 1% APN 118S0155

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 97: Fixed schematic note - I_LED=369/Riset

SYNC_MASTER=K24_MLB	SYNC_DATE=01/19/2009
PAGE TITLE	Revision History
Apple Inc.	DRAWING NUMBER 051-8379 SIZE D
	REVISION 4.4.0
NOTICE OF PROPRIETARY PROPERTY:	BRANCH
	PAGE 6 OF 110
	SHEET 6 OF 73

Functional Test Points

Fan Connectors

TRUE	PP5V_S0	7 8 57	
TRUE	FAN_RT_PWM	45	
TRUE	FAN_RT_TACH	45	

(NEED TO ADD 1 GND TP)

SPEAKER FUNC_TEST

TRUE	SPKRAMP_R_N_OUT	48 49
TRUE	SPKRAMP_R_P_OUT	48 49

INT DP FUNC_TEST

TRUE	PP3V3_SW_LCD	7 59	(NEED 2 TP)
TRUE	PPVOUT_SW_LCDBKLT	7 42 59 62	(NEED 2 TP)
TRUE	DP_INT_ML_F_N<0>	59 71	
TRUE	DP_INT_ML_F_P<0>	59 71	
TRUE	DP_INT_ML_F_N<1>	59 71	
TRUE	DP_INT_ML_F_P<1>	59 71	
TRUE	DP_INT_AUX_CH_C_N	59 71	
TRUE	DP_INT_AUX_CH_C_P	59 71	
TRUE	DP_INT_HPD_CONN	59	
TRUE	LED_RETURN_1	59 62	
TRUE	LED_RETURN_2	59 62	
TRUE	LED_RETURN_3	59 62	
TRUE	LED_RETURN_4	59 62	
TRUE	LED_RETURN_5	59 62	
TRUE	LED_RETURN_6	59 62	
TRUE	=I2C_TCON_SCL	41 59	
TRUE	=I2C_TCON_SDA	41 59	

(NEED TO ADD 5 GND TP)

HALL EFFECT CONN (PLACEHOLDER)

TRUE	SMC_LID_R	49
TRUE	=PP3V42_G3H_HALL	8 49

SATA HDD

TRUE	PP3V3_S0_HDD_R	7 35	(NEED 5 TP)
TRUE	SATA_HDD_R2D_P	35 67	
TRUE	SATA_HDD_R2D_N	35 67	
TRUE	SATA_HDD_D2R_C_P	35 67	
TRUE	SATA_HDD_D2R_C_N	35 67	
TRUE	SMC_HDD_OOB_TEMP	35 38	
TRUE	SMC_HDD_TEMP_CTL	35 38	

(NEED TO ADD 6 GND TP)

BATT POWER CONN

TRUE	SMBUS_SMC_BSA_SCL	41 70	
TRUE	SMBUS_SMC_BSA_SDA	41 70	
TRUE	SYS_DETECT_L	49	
TRUE	PPVBAT_G3H_CONN	49 50	(NEED 4 TP)

(NEED TO ADD 4 GND TP NEAR J6950 AND 1 FOR SHIELD)

LIO CONNECTOR

TRUE	=PP3V3_S0_AUDIO	37 8	(NEED 2 TP)
TRUE	=PP3V42_G3H_ONEWIRE	8 37	
TRUE	SMC_BC_ACOK	9 37 38 39	
TRUE	SYS_ONEWIRE	37 38	
TRUE	=USB_PWR_EN	36 37 57	
TRUE	USB_EXTD_OC_L	18 37	
TRUE	USB_CAMERA_P	18 37 68	
TRUE	USB_CAMERA_N	18 37 68	
TRUE	USB_EXTD_P	18 37 68	
TRUE	USB_EXTD_N	18 37 68	
TRUE	=PP1V8R1V5_S0_AUDIO	8 37	
TRUE	=I2C_LIO_SDA	37 41	
TRUE	=I2C_LIO_SCL	37 41	
TRUE	AUD_GPIO_3	37 48	
TRUE	AUD_I2C_INT_L	19 37	
TRUE	=I2C_MIKEY_SDA	37 41	
TRUE	=I2C_MIKEY_SCL	37 41	
TRUE	AUD_IP_PERIPHERAL_DET	17 37	
TRUE	SPKRAMP_INR_P	37 48 71	
TRUE	SPKRAMP_INR_N	37 48 71	
TRUE	HDA_SDIN0	19 37 68	
TRUE	HDA_SDOUT	19 37 68	
TRUE	HDA_BIT_CLK	19 37 68	
TRUE	HDA_SYNC	19 37 68	
TRUE	HDA_RST_L	19 37 68	
TRUE	AUD_IPHS_SWITCH_EN	19 37	

(NEED TO ADD 5 GND TP)

AIRPORT / BT

TRUE	PCIE_AP_R2D_P	34 67	
TRUE	PCIE_AP_R2D_N	34 67	
TRUE	PCIE_AP_D2R_P	16 34 67	
TRUE	PCIE_AP_D2R_N	16 34 67	
TRUE	PCIE_CLK100M_AP_P	16 34 67	
TRUE	PCIE_CLK100M_AP_N	16 34 67	
TRUE	USB_BT_P	18 34 68	
TRUE	USB_BT_N	18 34 68	
TRUE	WIFI_EVENT_L	34 38 39	
TRUE	=PP3V3_S3_BT	8 34	
TRUE	PP3V3_WLAN_F	7 34 39	(NEED 6 TP)
TRUE	PCIE_WAKE_L	16 34	
TRUE	AP_RESET_CONN_L	34	
TRUE	AP_CLKREQ_Q_L	34	

(NEED TO ADD 8 GND TP)

IPD_FLEX_CONN

TRUE	SMC_TPAD_RST_L	39 46
TRUE	SMC_LID	38 39 46 49
TRUE	SMC_ONOFF_L	38 39 46
TRUE	=I2C_TPAD_SCL	41 46
TRUE	=I2C_TPAD_SDA	41 46
TRUE	=PP3V42_G3H_TPAD	8 46
TRUE	PP3V3_TPAD_CONN	46
TRUE	PP5V_TPAD_FILT	46
TRUE	USB_TPAD_CONN_N	46 71
TRUE	USB_TPAD_CONN_P	46 71

(NEED TO ADD 5 GND TP)

LCP + SPI CONN

TRUE	=PP3V3_S5_LPCPLUS	8 40
TRUE	=PP5V_S0_LPCPLUS	8 40
TRUE	LPC_AD<3..0>	19 38 40 68
TRUE	SPI_ALT_MOSI	40 68
TRUE	SPI_ALT_MISO	40 68
TRUE	LPC_FRAME_L	19 38 40 68
TRUE	PM_CLKRUN_L	19 38 40
TRUE	SMC_TMS	38 39 40
TRUE	LPCPLUS_RESET_L	25 40
TRUE	SMC_TDO	38 39 40
TRUE	SMC_TRST_L	38 40
TRUE	SMC_MD1	38 40
TRUE	SMC_TX_L	36 38 39 40
TRUE	LPC_CLK33M_LPCPLUS	25 40 68
TRUE	SPIROM_USE_MLB	19 40 47
TRUE	SPI_ALT_CLK	40 68
TRUE	SPI_ALT_CS_L	40 68
TRUE	LPC_SERIRQ	19 38 40
TRUE	LPC_PWRDWN_L	19 38 40
TRUE	SMC_TDI	38 39 40
TRUE	SMC_TCK	38 39 40
TRUE	SMC_RESET_L	38 39 40 50
TRUE	SMC_NMI	38 40
TRUE	SMC_RX_L	36 38 39 40
TRUE	LPCPLUS_GPIO	19 40

(NEED TO ADD 6 GND TP)

DC POWER CONN

TRUE	=PP18V5_DCIN_CONN	8 49	(NEED 6 TP)
TRUE	=PP5V_S3_LIO_CONN	8 49	

(NEED TO ADD 6 GND TP)

DEBUG VOLTAGE

TRUE	PPVCORE_S0_CPU	8 42
TRUE	PPVCORE_S0_MCP	8 42
TRUE	PP1V05_S0	8 57
TRUE	PP1V5_S0	8 57 71
TRUE	PP3V3_S0	8 57 71
TRUE	PP5V_S0	7 8 57
TRUE	PP3V3_S3	8
TRUE	PP5V_S3	8
TRUE	PP0V9_S5	8
TRUE	PP3V3_S5	8 57 71
TRUE	PP3V42_G3H	8
TRUE	PPBUS_G3H	8 42 49
TRUE	PP3V3_WLAN_F	7 34 39
TRUE	PP3V3_S0_HDD_R	7 35
TRUE	PPDCIN_S5_S5	8
TRUE	PPVOUT_SW_LCDBKLT	7 42 59 62
TRUE	PP3V3_SW_LCD	7 59
TRUE	PP1V5R1V35_S3	8 71
TRUE	SMC_PM_G2_EN	38 57
TRUE	PM_SLP_S4_L	19 38 57
TRUE	PM_SLP_S3_L	19 38 39 57
TRUE	PP0V9_ENET	8
TRUE	PP1V05_S0_MCP_PLL_UF	8
TRUE	PP3V3_ENET	8
TRUE	PP3V3_SW_DPPWR	61
TRUE	PP5V_S3_RTUSB_A_F	36
TRUE	PPBUS_G3H_ISNS	8

(NEED TO ADD 27 GND TP)

FSB SIGNALS WITH NOTEST

NO_TEST=TRUE	FSB_A_L<35..3>	10 14 65
NO_TEST=TRUE	FSB_ADS_L	10 14 65
NO_TEST=TRUE	FSB_ADSTB_L<1..0>	10 14 65
NO_TEST=TRUE	FSB_D_L<63..0>	10 14 65
NO_TEST=TRUE	FSB_DINV_L<3..0>	10 14 65
NO_TEST=TRUE	FSB_DSTB_L_N<3..0>	10 14 65
NO_TEST=TRUE	FSB_DSTB_L_P<3..0>	10 14 65
NO_TEST=TRUE	FSB_HIT_L	10 14 65
NO_TEST=TRUE	FSB_HITM_L	10 14 65
NO_TEST=TRUE	FSB_LOCK_L	10 14 65
NO_TEST=TRUE	FSB_REQ_L<4..0>	10 14 65

8 7 6 5 4 3 2 1

"S0,S0M" RAILS

53 =PPVCORE_S0_CPU_REG 18 A
PPVCORE_S0_CPU 7 42
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU 11 12 64

55 =PPCPUVTT_S0_REG 9.40 A
PP1V05_S0 7 57
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU 10 11 12
=PP1V05_S0_MCP_FSB 14 20 23
=PP1V05_S0_MCP_AVDD_UF 23
=PP1V05_S0_MCP_SATA_DVDD 20 23
=PP1V05_S0_MCP_PLL_UF_R 56
=PP1V05_SW_MCP_FSB 20 23
=PP1V05_S0_MCP_PE_DVDD 20 23
=PP1V05_S0_MCP_M2CLK_DLL 15 23
=PP1V05_S0_MCP_DP0_VDD 17 24
=PP1V05_S0_XDP 13

54 =PPMCPCORE_S0_REG (MCP_VCORE AFTER SENSE RES) 23.8 A
PPVCORE_S0_MCP 7 42
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP 20 23
=PPVCORE_S0_MCPGFXFET 22

LVDDR VRef/VTT (0.75V/0.675V) Rails

52 =PPVTT_S0_DDR_LDO 1.20 A
PPDDRVTT_S0
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PPDDRVTT_S0_MEM_A 32
=PPDDRVTT_S0_MEM_B 32

52 33 =PPVTT_S3_DDR_BUF
PPDDRVREF_S3
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

56 =PP1V5_S0_REG .210 A
PP1V5_S0 7 57 71
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU 11 12
=PP1V5_S0_MCP_PLL_VLDO 56
=PP1V8R1V5_S0_AUDIO 7 37
=PP3V3R1V5_S0_MCP_HDA 19 23

56 =PP1V05_S0_MCP_PLL_OR
PP1V05_S0_MCP_PLL_UF 7
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_MCP_PLL_UF 23

58 =PP5V_S0_FET 0.100 A
PP5V_S0 7 57
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_LPCPLUS 7 40
=PP5V_S0_FAN 45
=PP5V_S0_CPU_IMVP 53
=PP5VR3V3_S0_DPCADET 61
=PP5V_S0_CPUVTTS0 55
=PP5V_S0_BKL 62
=PP5V_S0_MCPREG 54
=PP5V_S0_MCPFSBFET 22

58 =PP3V3_S0_FET 3.30 A
PP3V3_S0 7 57 71
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_XDP 13
=PP3V3_S0_MCP 20 23
=PP3V3_S0_P1V5S0 56
=PP3V3_S0_DEBUGROM 40
=PP3V3_S0_SMBUS_SMC_0_S0 41
=PP3V3_S0_SMBUS_SMC_B_S0 41
=PP3V3_S0_SMBUS_MCP_0 41
=PP3V3_S0_FAN 45
=PP3V3_S0_AUDIO 7 37
=PP3V3_S0_IMVP 53
=PP3V3_S0_MCP_GPIO 17 18 19
=PP3V3_S0_MCP_PLL_UF 23
=PP3V3_S0_MCP_HVDD 20 23
=PP3V3_S0_SMC 39
=PP3V3_S0_MCPTHMSNS 44
=PP3V3_S0_CPUTHMSNS 44
=PP3V3_S0_PWRCTL 57
=PP3V3_S0_SMBUS_MCP_1 41
=PP3V3_S0_HDD 35
=PP3V3_S0_MCP_PLL_VLDO 56
=PP3V3_S0_MCPCOREISNS 43
=PP3V3_S0_MCPDDRISNS 43
=PP3V3_S0_BKLTISNS 42
=PP3V3_S0_CSREGISNS 43
=PP3V3_S0_BKL_VDDIO 62
=PP3V3_S0_DPCONN 61
=PP3V3_S0_HDDISNS 42

"ENET" RAILS

9 =PP3V3_ENET_FET_R 400mA
PP3V3_ENET 7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
300mA =PP3V3_ENET_MCP_RMGT 18 20 23
~100mA =PP3V3_ENET_MCP_PLL_MAC 23

58 =PP0V9_ENET_FET
PP0V9_ENET 7
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V9_ENET_MCP_RMGT 20 23

"S3" RAILS

LVDDR (1.5V/1.35V) Rails

52 =PPDDR_S3_REG 11.30 A
PP1V5R1V35_S3 7 71
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE (OR 1.35V)
=PPLVDDR_S3_MEM_A 26 27 30
=PPLVDDR_S3_MEM_B 28 29 31
0 mA =PP1V5R1V35_S3_MCP_MEM 15
4250 mA =PP1V5R1V35_S0_MCPDDRFET 21
=PPVIN_S0_DDRREG_LDO 52

58 =PP3V3_S3_FET 1.274 A
PP3V3_S3 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_SMBUS_SMC_A_S3 41
=PP3V3_S3_PDCISENS 52
=PP3V3_S3_VREFMRGN 33
=PP3V3_S3_MCP_GPIO 19
=PP3V3_S3_SMS
=PP3V3_S3_1V5S3ISNS 42
=PP3V3_S3_WLANISNS 42
=PP3V3_S3_DBGLEDS 49
=PP3V3_S3_BT 7 34
=PP3V3_S3_WLAN 34
=PP3V3_S3_TPAD 46

51 =PP5V_S3_REG 5.40 A
PP5V_S3 7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_MCPDDRFET 21
=PP5V_S3_SYSLED 39
=PP5V_S3_TPAD 46
=PP5V_S3_DDRREG 52
=PP5V_S3_AUDIO_AMP 48
=PP5V_S3_P5VS0FET 58
=PP5V_S3_RTUSB 36
=PP5V_S3_LIO_CONN 7 49

"S5" RAILS

57 51 =PP3V3_S5_REG 1.07 A + S3 + S0
PP3V3_S5 7 57 71
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_GPIO 18 19
=PP3V3_S5_ROM 47
=PP3V3_S5_MCP 20 23
=PP3V3_S5_MCPPWRGD 25
=PP3V3_S5_P3V3S3FET 58
=PP3V3_S5_P3V3S0FET 58
=PP3V3_S5_P3V3ENETFET 58
=PP3V3_S5_P0V9S5 56 57
=PP3V3_S5_VMON 57
=PP3V3_S5_SMBUS_SMC_MGMT 41
=PP3V3_S5_P0V9ENETFET 58
=PP3V3_S5_TPAD 46
=PP3V3_S5_DP_PORT_PWR 61
=PP3V3_S0_LCD 59
=PP3V3_SMC_PME 39

56 =PP0V9_S5_REG 0.290 A
PP0V9_S5 7
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
105 mA/241 mA =PP0V9_S5_MCP_VDD_AUXC 20 23
=PP0V9_ENET_P0V9ENETFET 58

"G3H" RAILS

49 =PP3V42_G3H_REG 0.064
PP3V42_G3H 7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PPVIN_S5_SMCVREF 39
=PP3V42_G3H_SMBUS_SMC_BSA 41
=PP3V42_G3H_PWRCTL 57
=PP3V42_G3H_CHGR 50 57
=PP3V42_G3H_SMCUSBMUX 36
=PP3V42_G3H_TPAD 7 46
=PP3V42_G3H_HALL 7 49
=PP3V3_S5_SMC 38 39
=PP3V3_S5_LPCPLUS 7 40
=PP3V42_G3H_BMON_ISNS 43
=PP3V42_G3H_ONEWIRE 7 37
PP3V3_G3_RTC 19 20 23

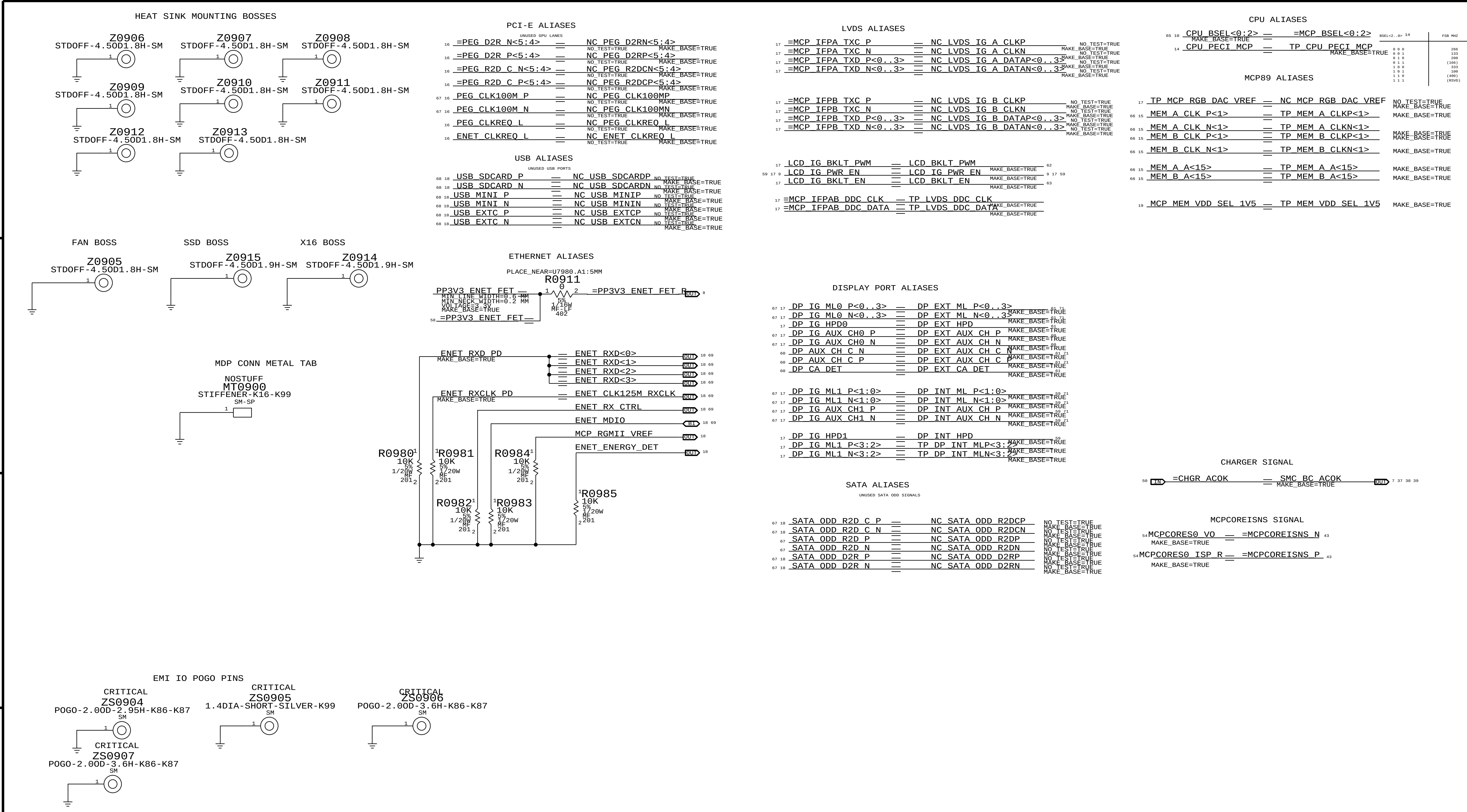
49 7 =PP18V5_DCIN_CONN
PPDCIN_S5_S5 7
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPDCIN_S5_CHGR 50

50 =PPBUS_G3H
PPBUS_G3H 7 42 49
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
=PPBUS_S0_LCDBKLT 63
=PPVIN_S5_P5VP3V3 51
=PPBUS_G3H_R_IN 43
=PPBUS_5V_S5 56

43 =PPBUS_G3H_R_OUT
PPBUS_G3H_ISNS 7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=8.4V
MAKE_BASE=TRUE
=PPVIN_S0_CPUVTTS0 55
=PPVIN_S5_CPU_IMVP 53
=PPVIN_S0_MCPCORE 54
=PPVIN_S3_DDRREG 52

SYNC_MASTER=K6_MLB	SYNC_DATE=12/11/2009
PAGE TITLE	Power Aliases
Apple Inc.	DRAWING NUMBER 051-8379 SIZE D
	REVISION 4.4.0
	BRANCH
	PAGE 8 OF 110
	SHEET 8 OF 73

8 7 6 5 4 3 2 1



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PAGE TITLE

SIGNAL ALIAS

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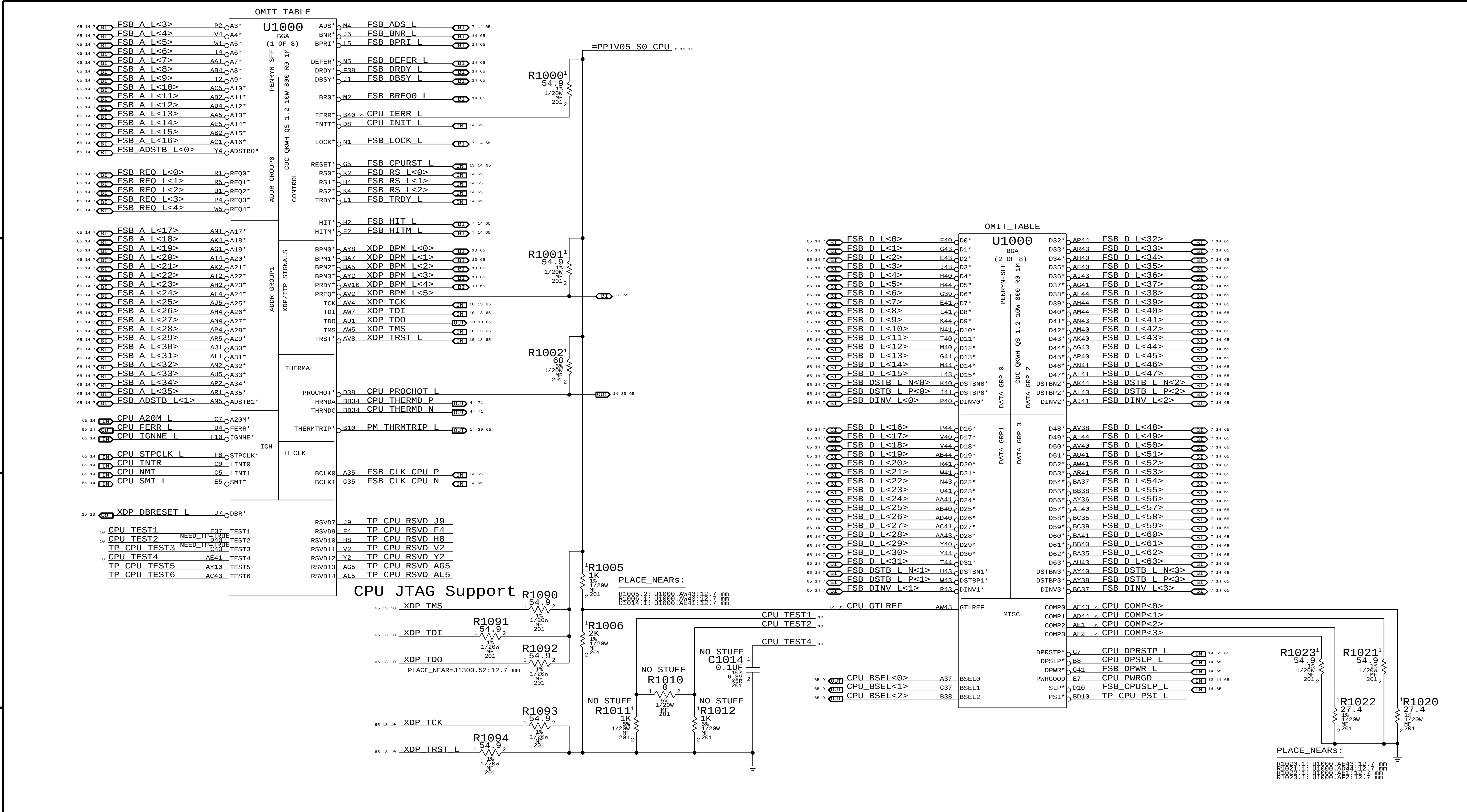

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

CPU FSB

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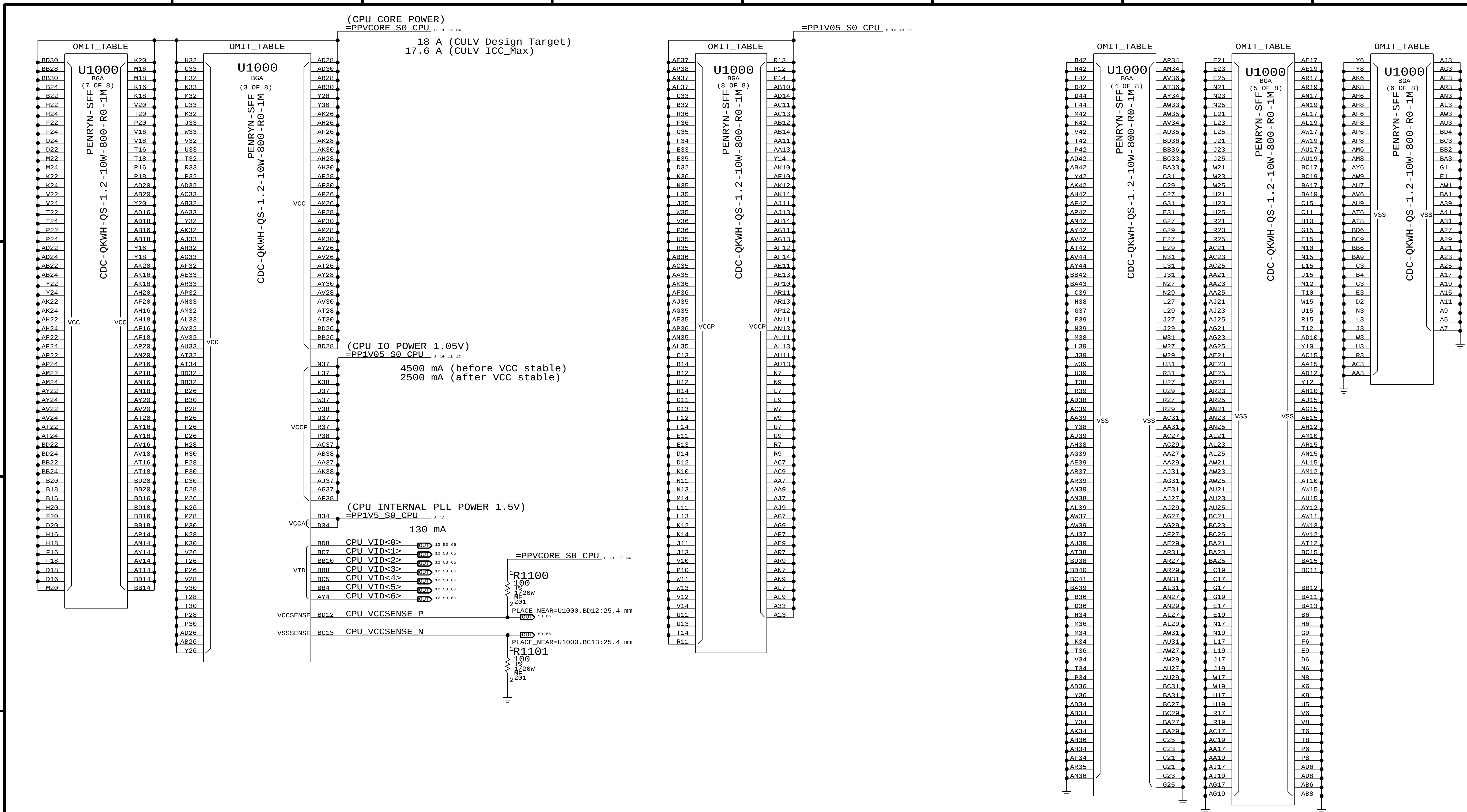

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

CPU Power & Ground

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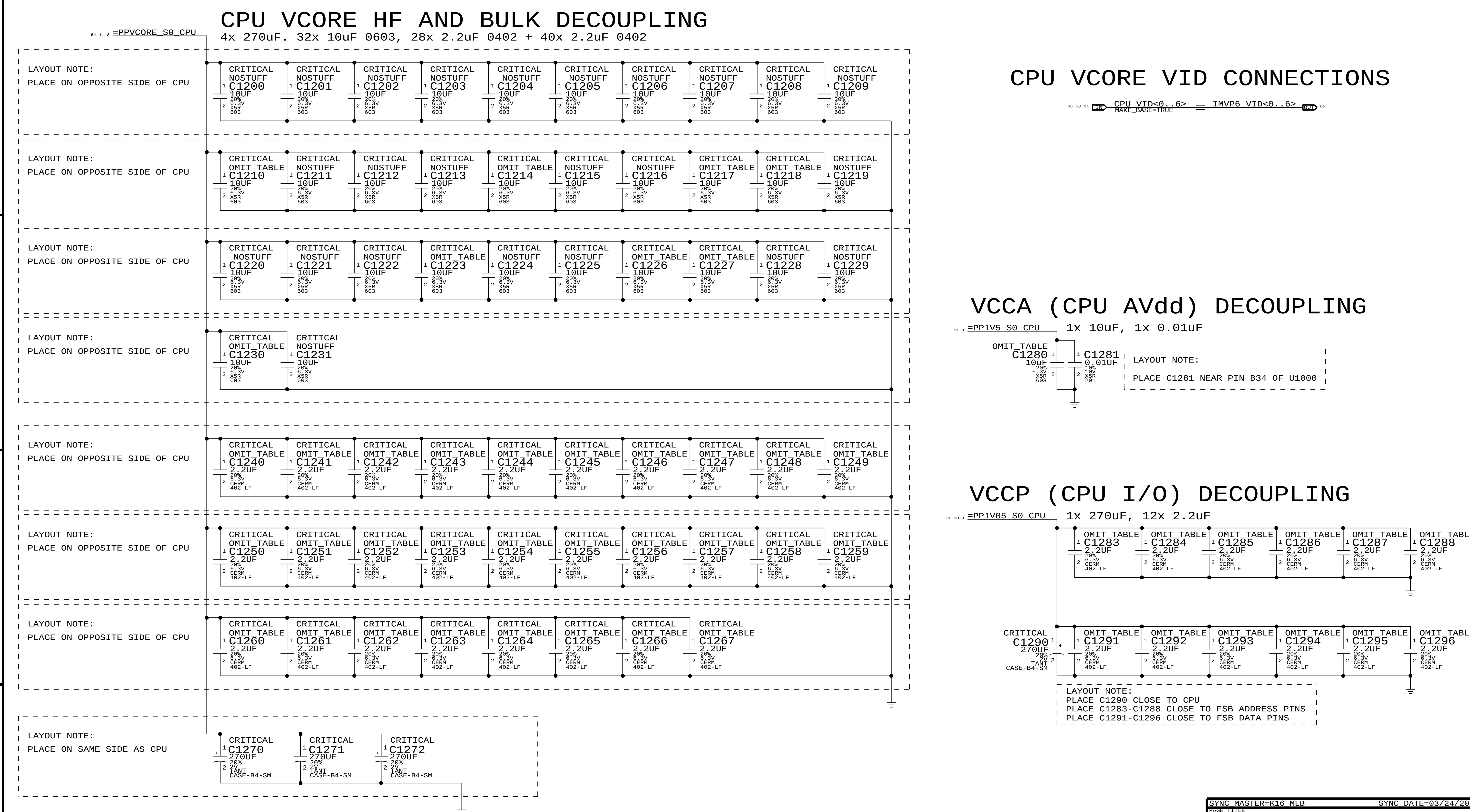


SYNC_MASTER=K16_MLB SYNC_DATE=03/24/2010

PAGE TITLE
CPU Decoupling & VID

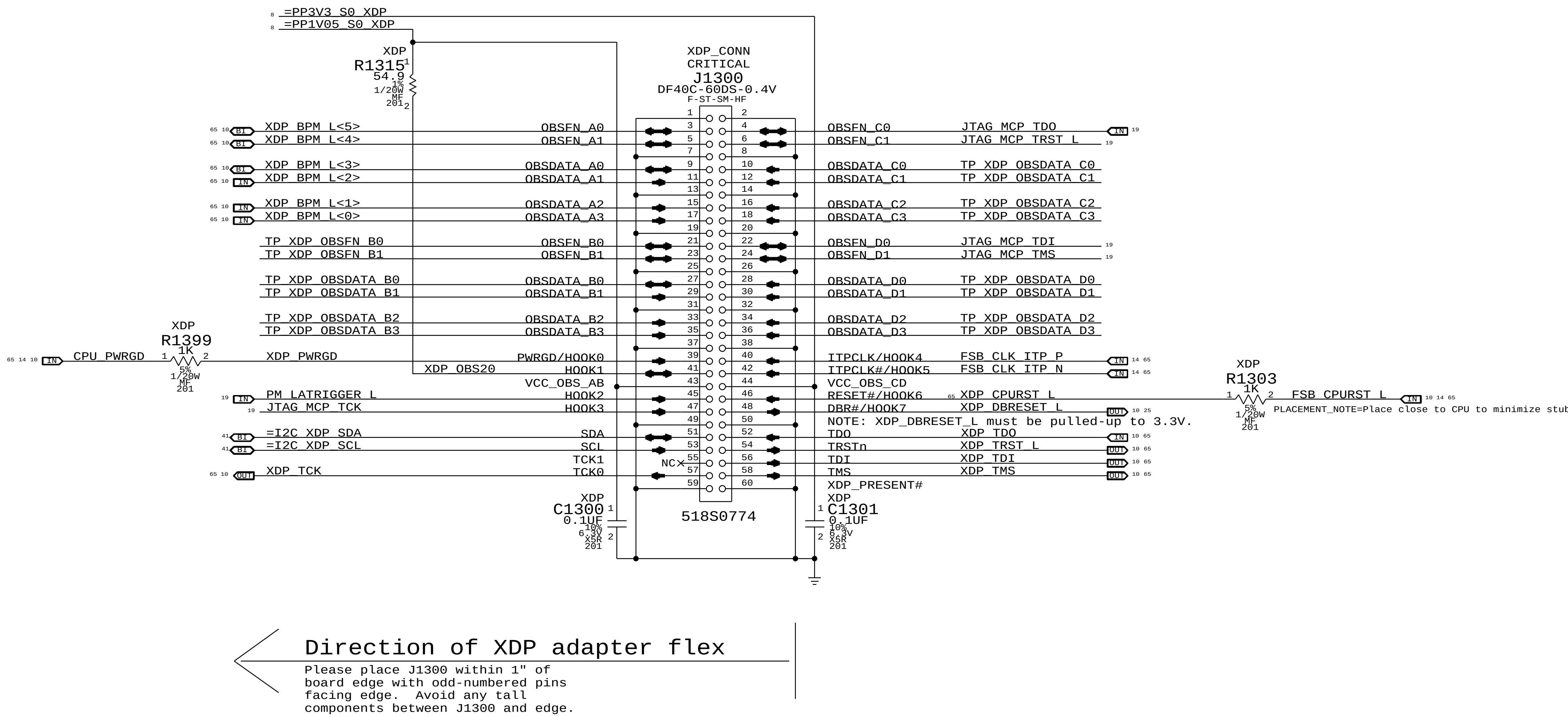
Apple Inc.

DRAWING NUMBER	051-8379
SIZE	D
REVISION	4.4.0
BRANCH	
PAGE	12 OF 110
SHEET	12 OF 73

Micro2-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0782 Adapter Flex to support chipset debug.



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

eXtended Debug Port (Micro-XDP)

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DRAWING NUMBER	SIZE
051-8379	D

REVISION 4.4.0

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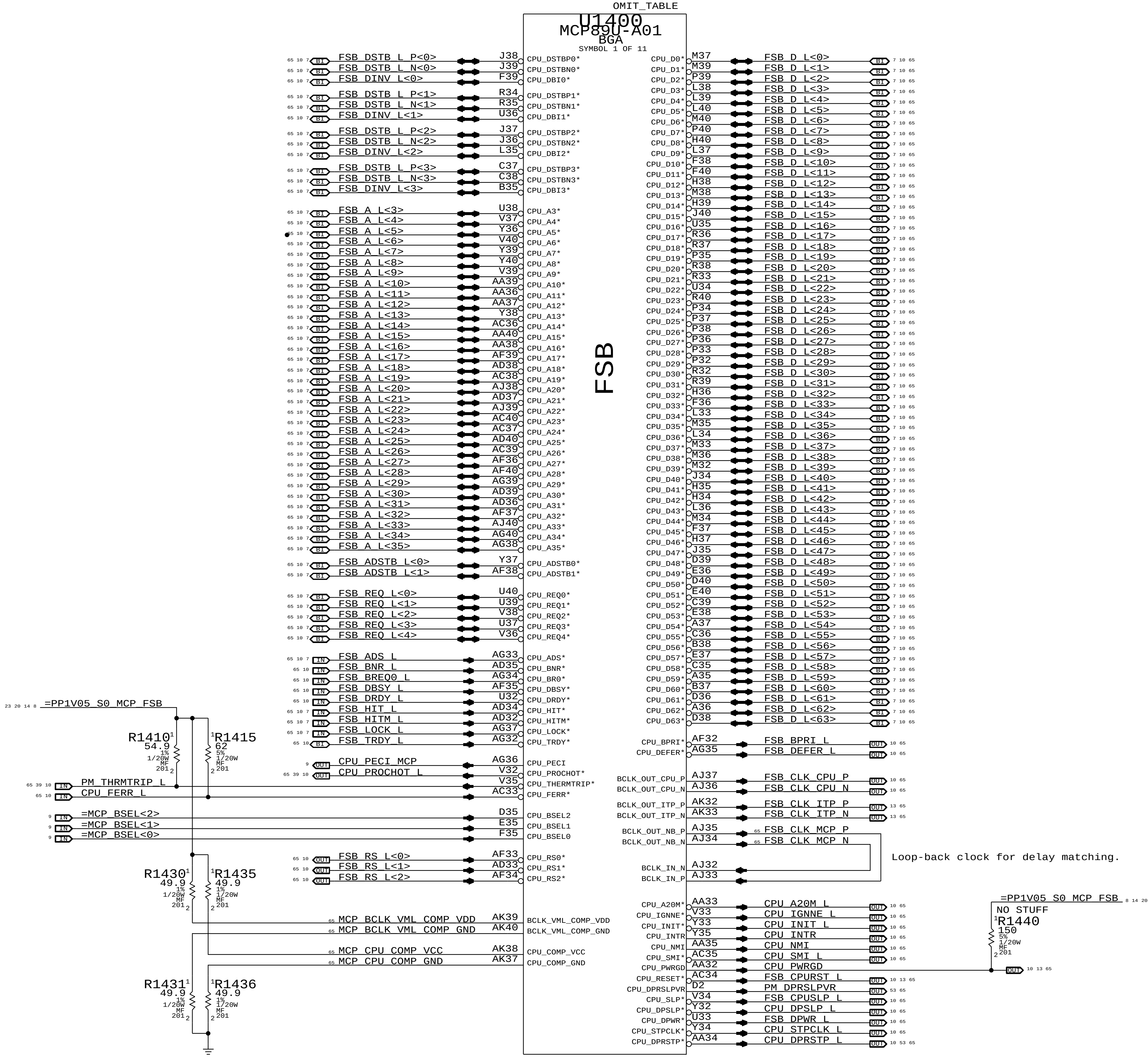

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

MCP CPU Interface

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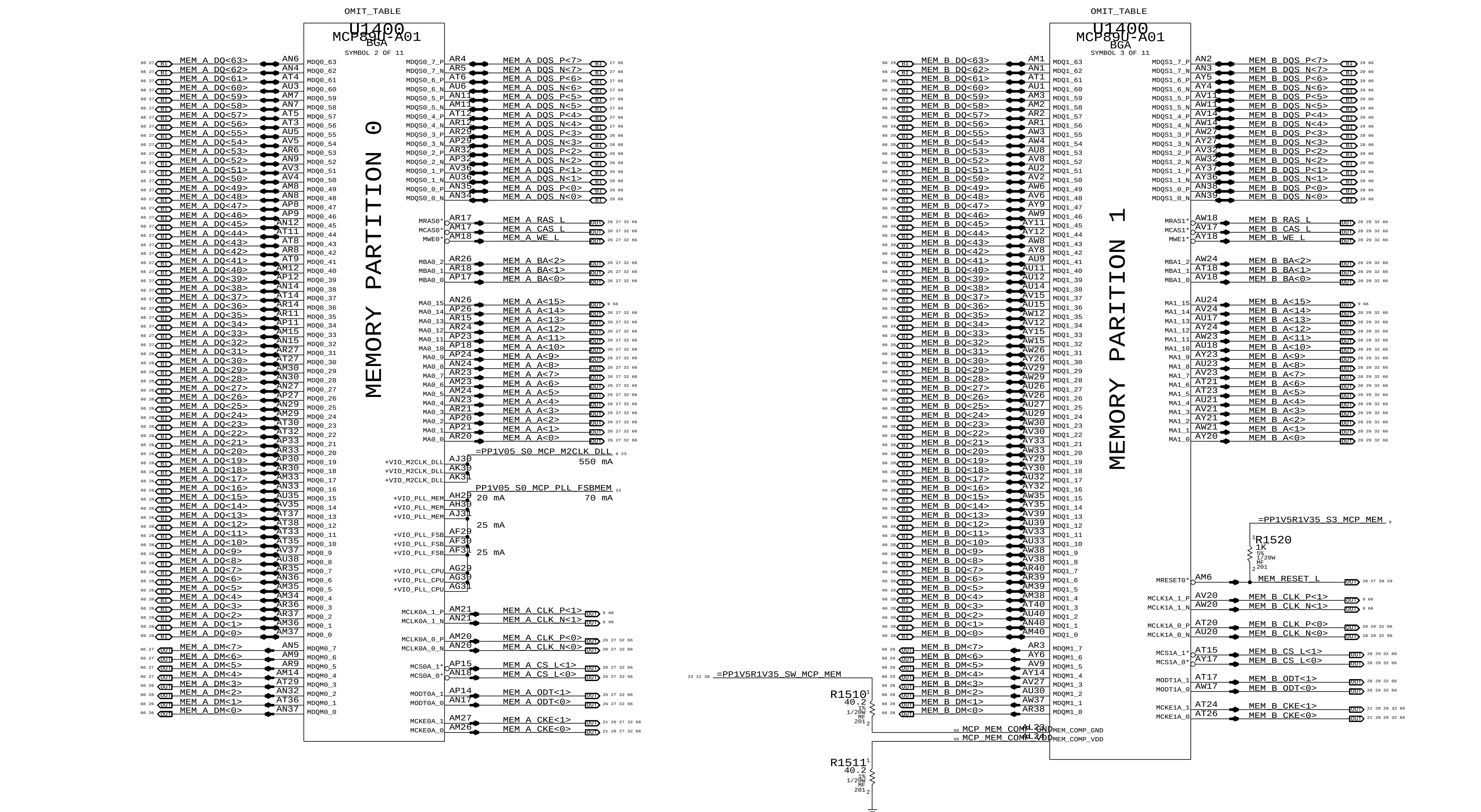

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

MCP Memory Interface

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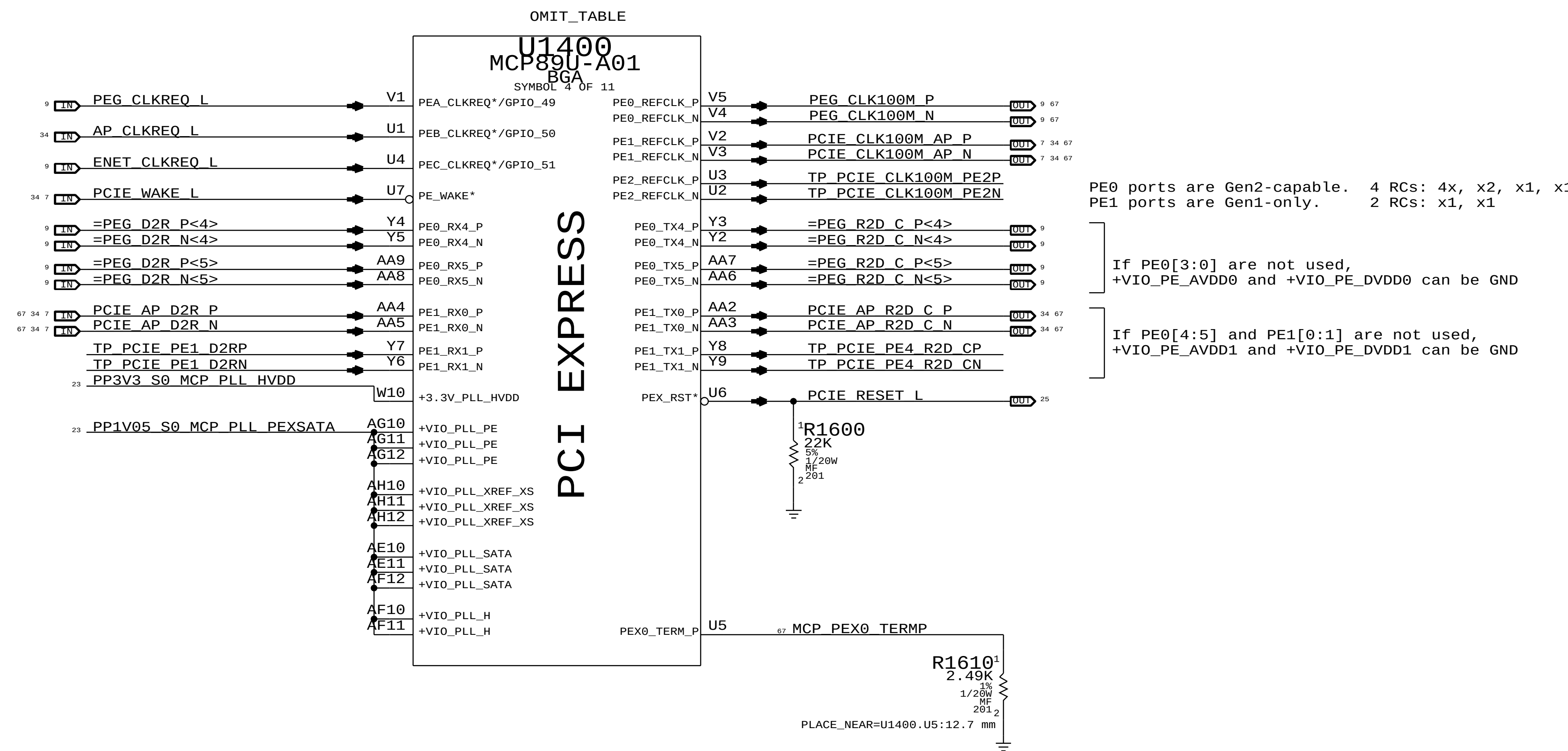

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB	SYNC_DATE=07/07/2010
PAGE TITLE: MCP PCIe Interfaces	
Apple Inc.	DRAWING NUMBER 051-8379, SIZE D
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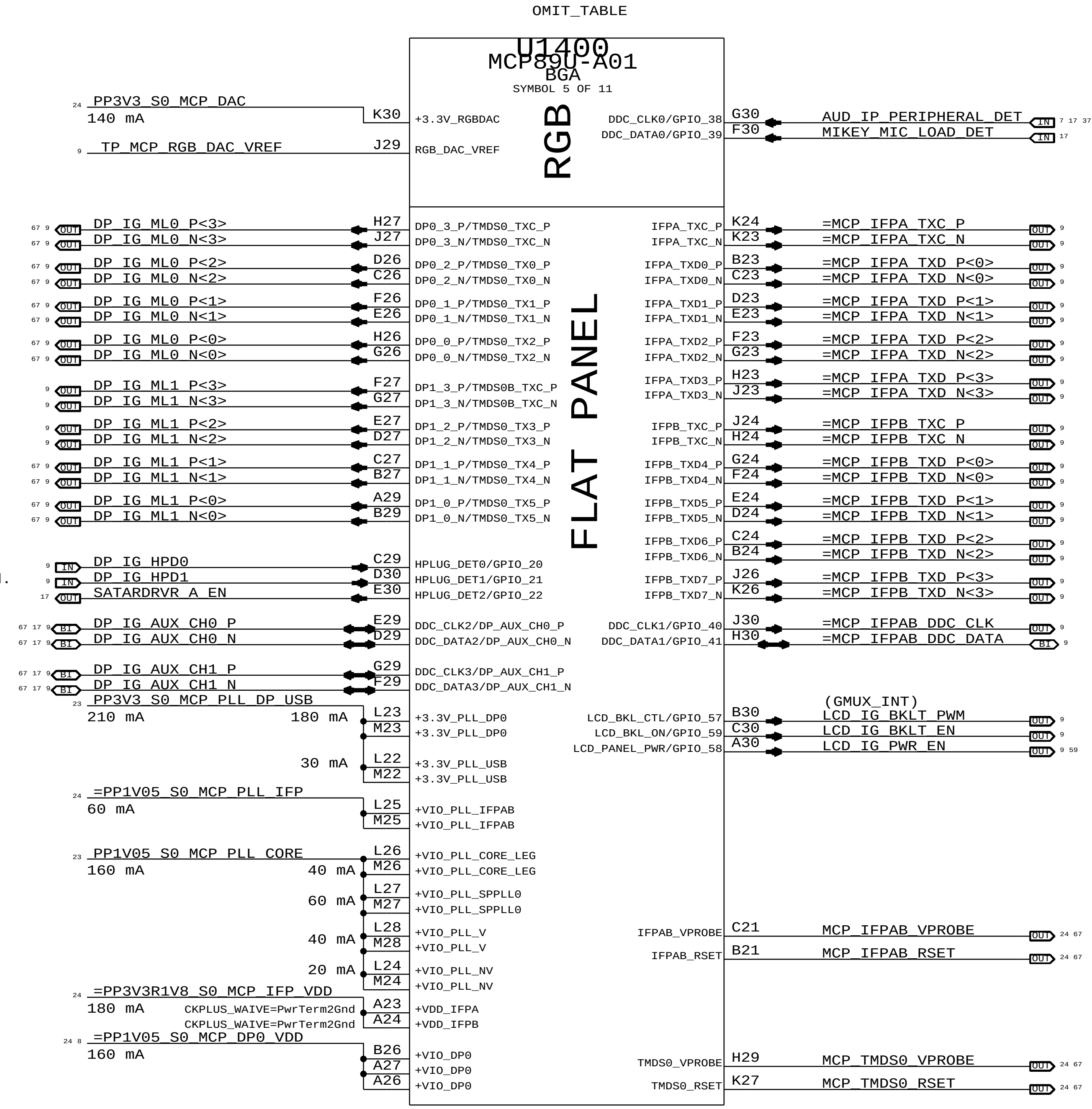
	SHEET 16 OF 73



RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
Connect +3.3V_RGBDAC pin to GND.

NOTE: No Composite/S-Video/Component Video support on MCP89

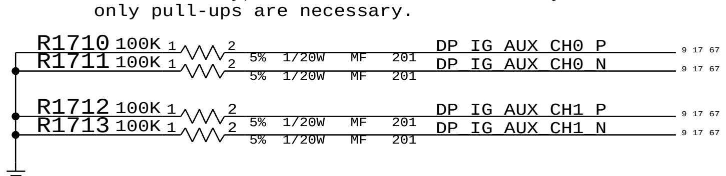
Interface Mode

MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

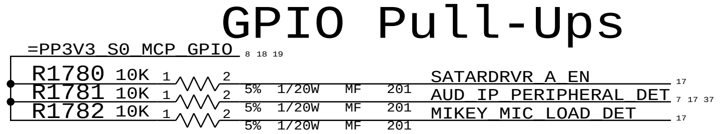
LVDS: Power +VDD_IFPx at 1.8V
TMDS: Power +VDD_IFPx at 3.3V

DDC Mode Pull-downs

NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.



GPIO Pull-Ups



Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: MCP Graphics

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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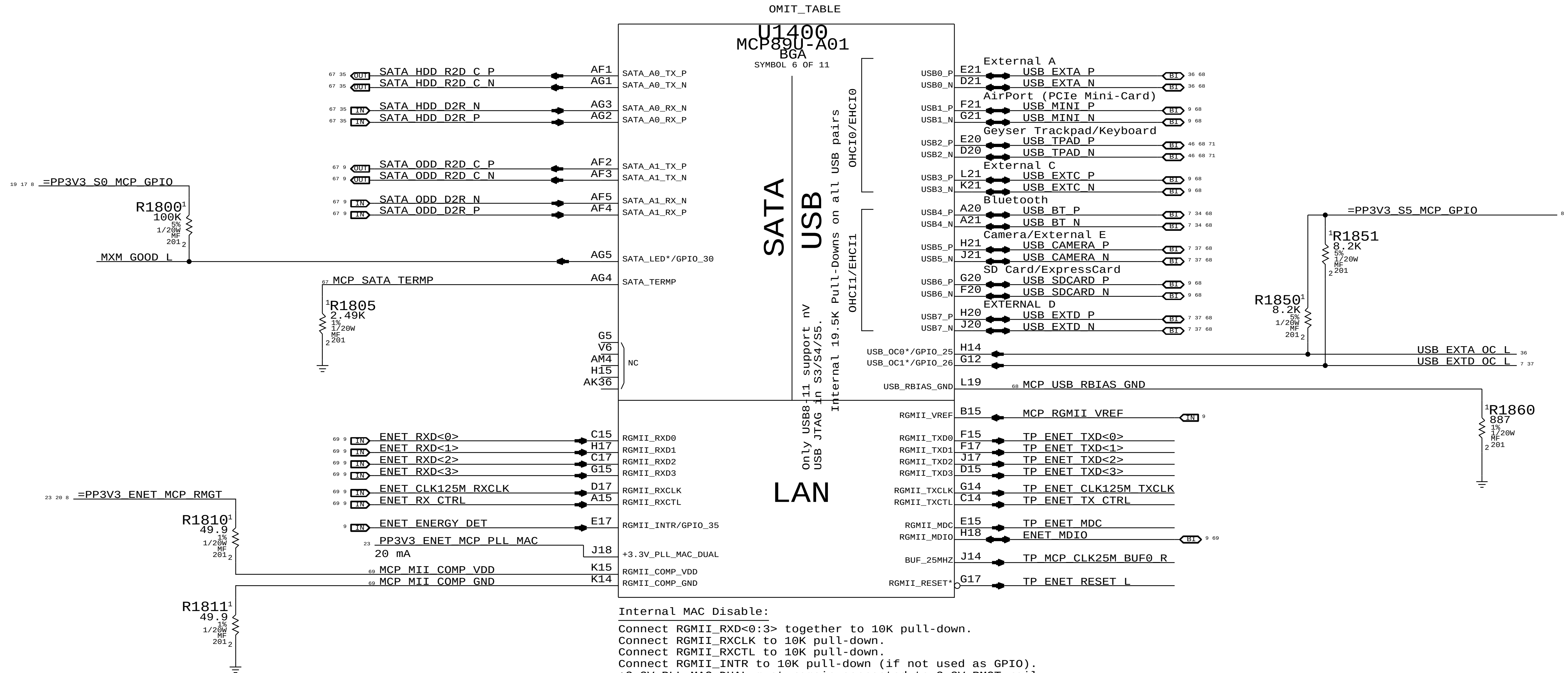

Internal MAC Disable:

Connect RGMII_RXD<0:3> together to 10K pull-down.
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
RGMII_COMP_VDD/_GND must remain connected as shown.
Connect RGMII_VREF to 10K pull-down.
Connect RGMII_MDIO to 10K pull-down.
All other pins can be left TP or NC.

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
MCP SATA, USB & Ethernet

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DRAWING NUMBER 051-8379 SIZE D

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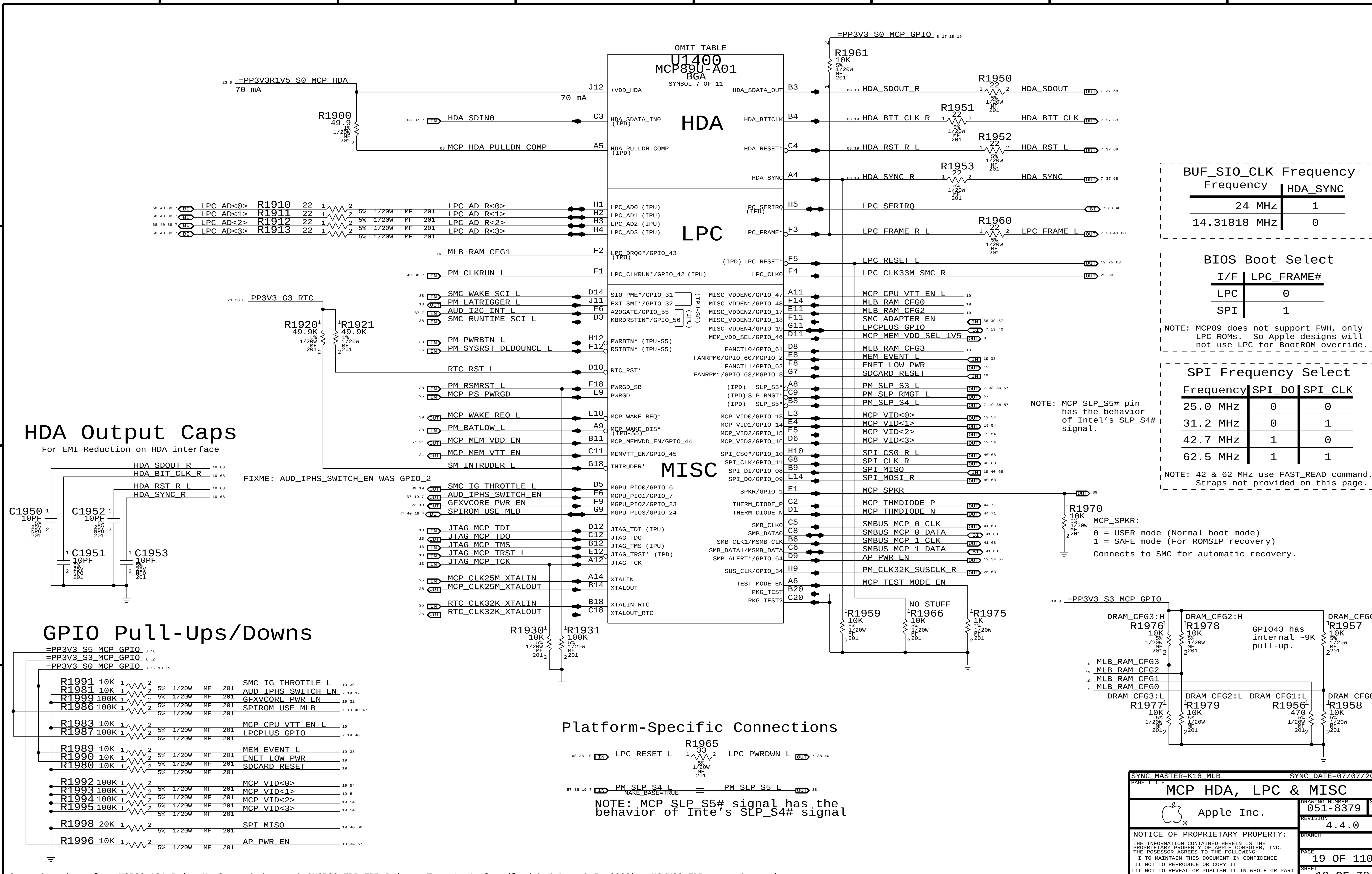

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select

I/F	LPC_FRAME#
LPC	0
SPI	1

NOTE: MCP89 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command. Straps not provided on this page.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: MCP HDA, LPC & MISC

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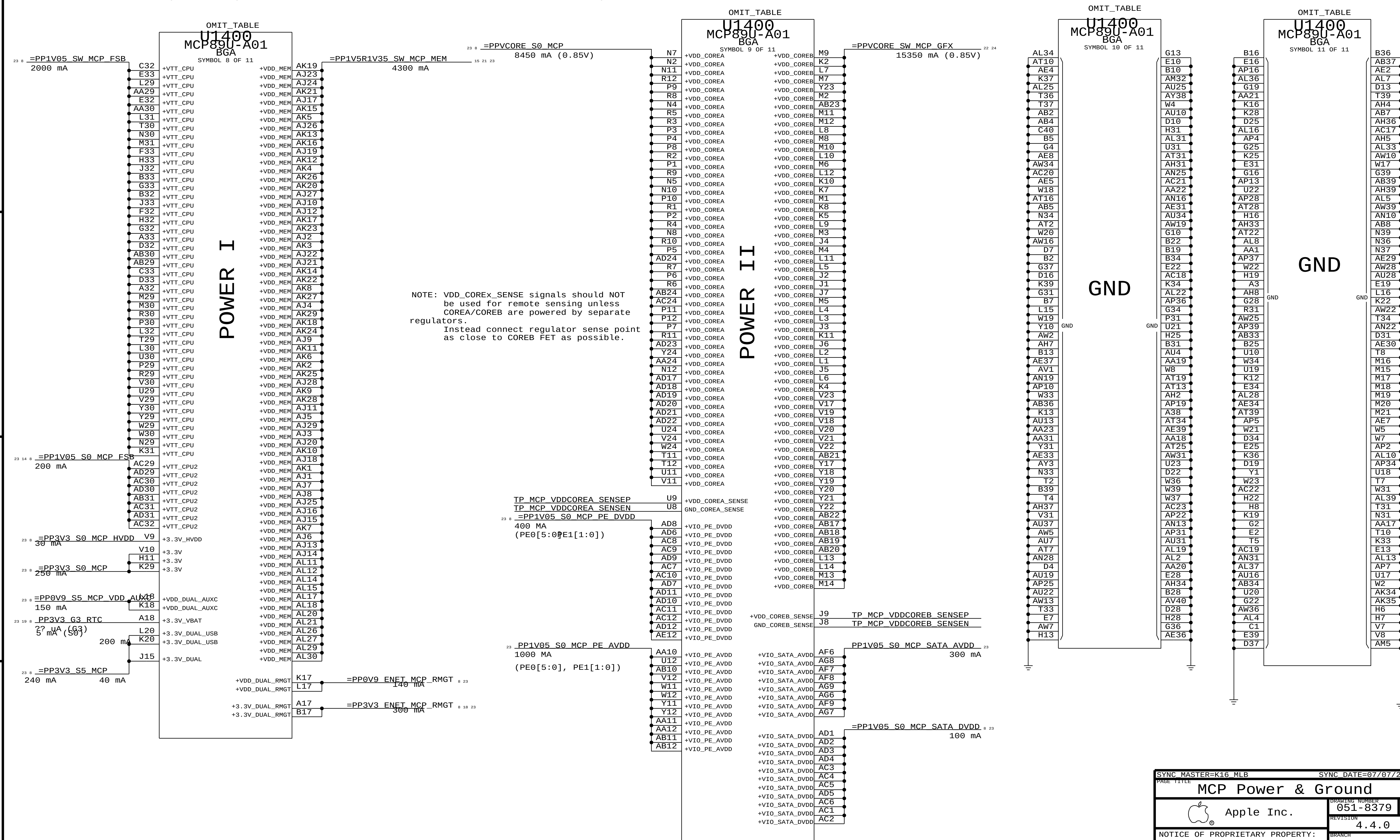
NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.



Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

MCP Power & Ground

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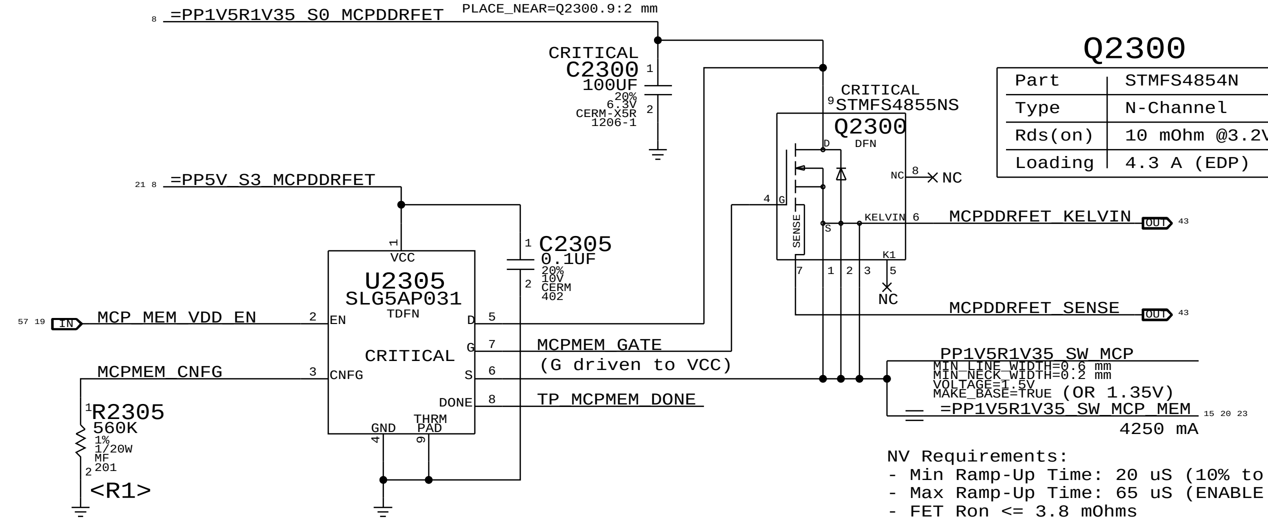
C2300 helps reduce input rail
droop during Q2300 turn-on.



Q2300

Part	STMFS4854N
Type	N-Channel
Rds(on)	10 mOhm @3.2V
Loading	4.3 A (EDP)

Approx. Ramp Time (EN to 1.35V, uS): 7.91 + 0.0678 * R1(Kohms)

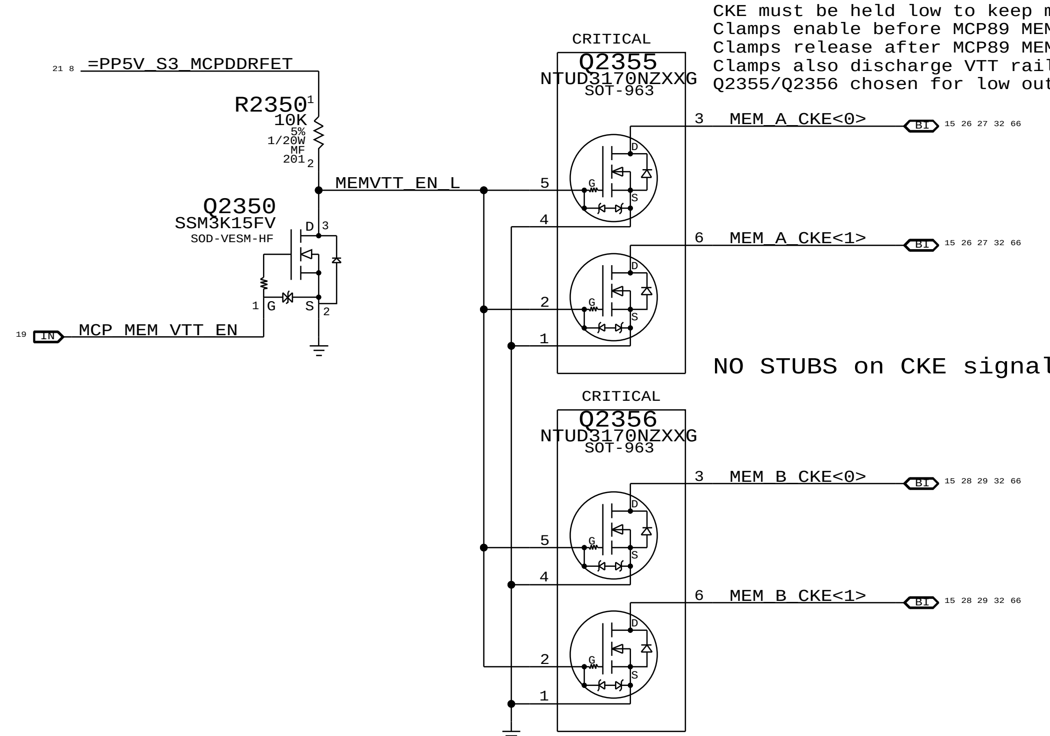
NV Requirements:
- Min Ramp-Up Time: 20 uS (10% to 90%)
- Max Ramp-Up Time: 65 uS (ENABLE to 90%)
- FET Ron <= 3.8 mOhms

NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.

Gated Rail Savings: 120mW

DIMM CKE Clamps

CKE must be held low to keep memory in self-refresh.
Clamps enable before MCP89 MEMVDD rail switched off.
Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.
Clamps also discharge VTT rail via termination resistor on each CKE signal on DIMM.
Q2355/Q2356 chosen for low output capacitance.



NO STUBS on CKE signals!

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: MCP89 Memory Rail Gating

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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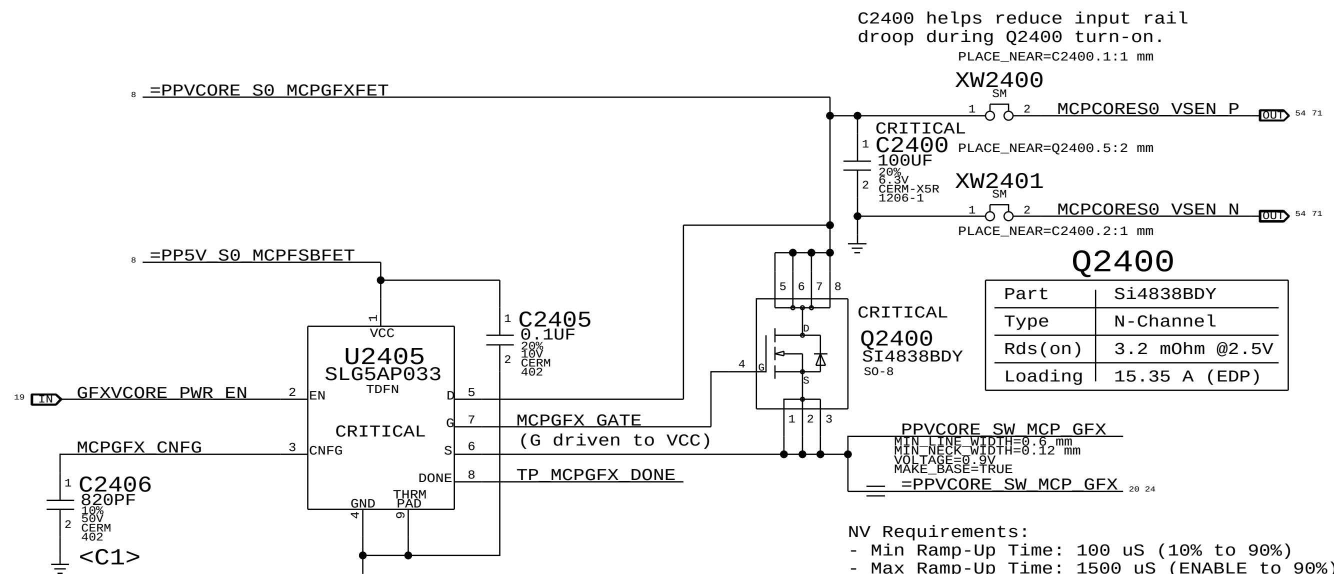

Q2400

Part	Si4838BDY
Type	N-Channel
Rds(on)	3.2 mOhm @2.5V
Loading	15.35 A (EDP)

NV Requirements:
- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET Ron <= 2.5 mOhms

Approx. Ramp Time (EN to 1V, uS): 43.9 + 0.6943 * C1(pF)

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

Gated Rail Savings: 860mW

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

MCP89 GFX Core Rail Gating

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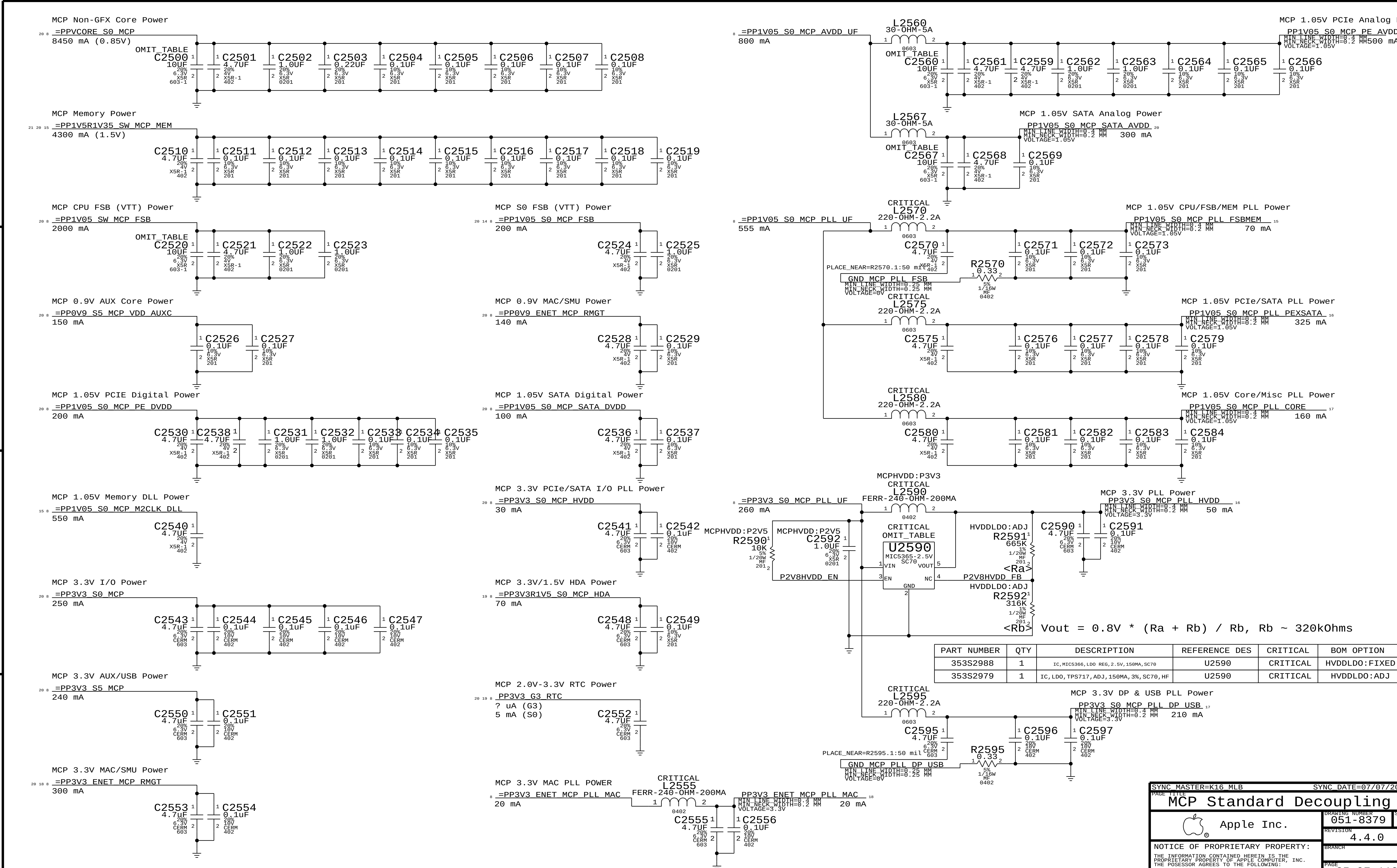

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2988	1	IC,MIC5366,LDO REG,2.5V,150MA,SC70	U2590	CRITICAL	HVDDLDO:FIXED
353S2979	1	IC,LDO,TPS717,ADJ,150MA,3%,SC70,HF	U2590	CRITICAL	HVDDLDO:ADJ

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

MCP Standard Decoupling

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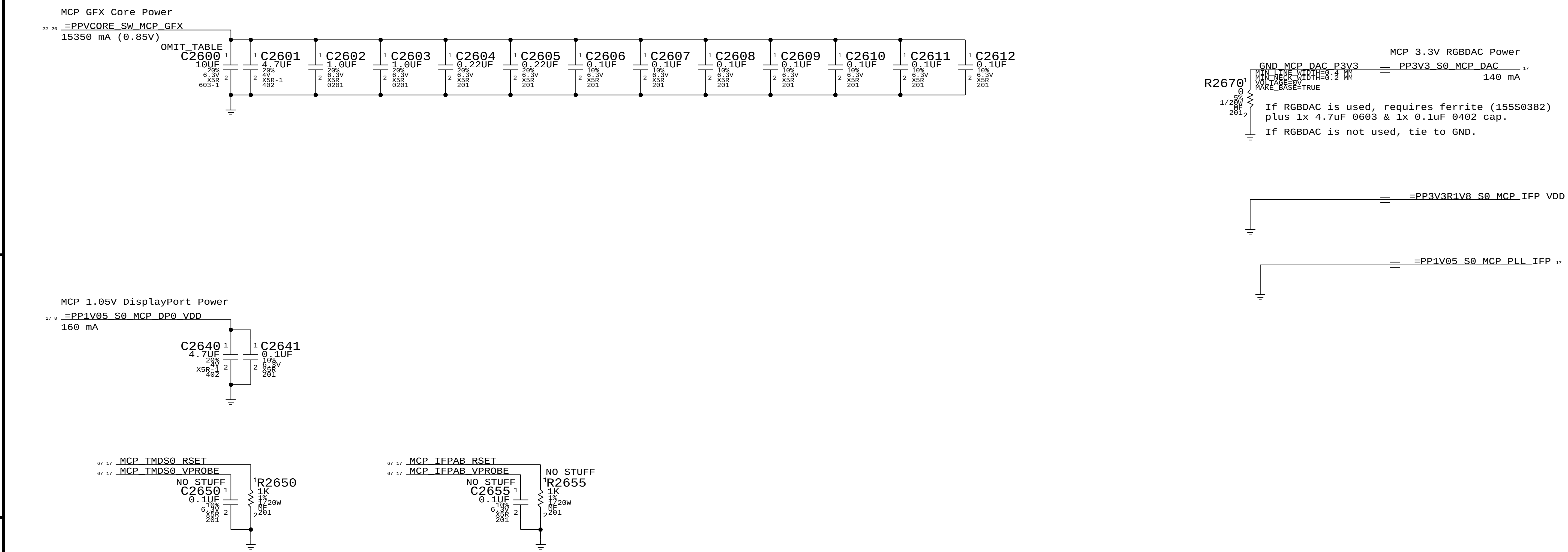
Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.



Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

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PAGE TITLE

MCP Graphics Support

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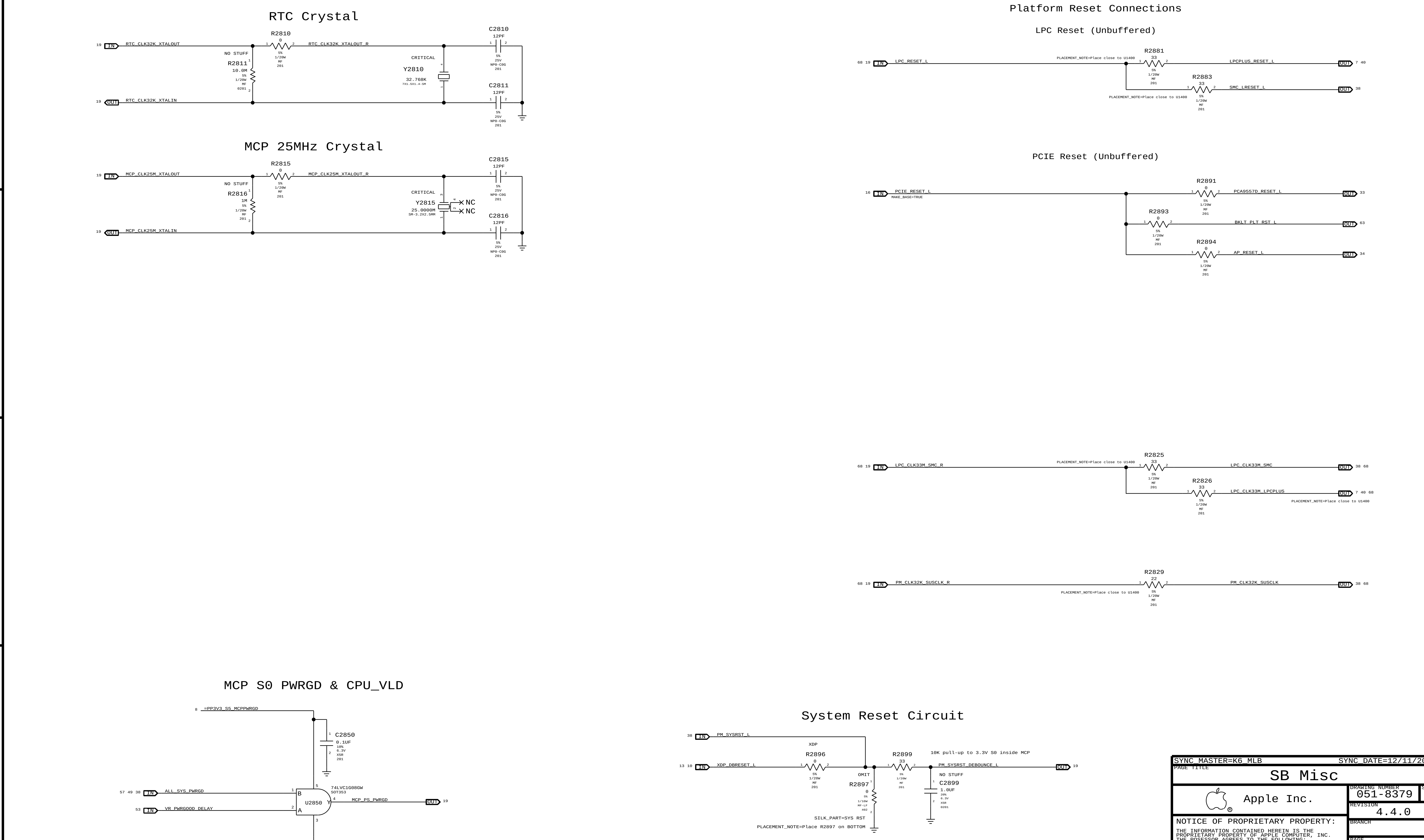

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE

SB Misc

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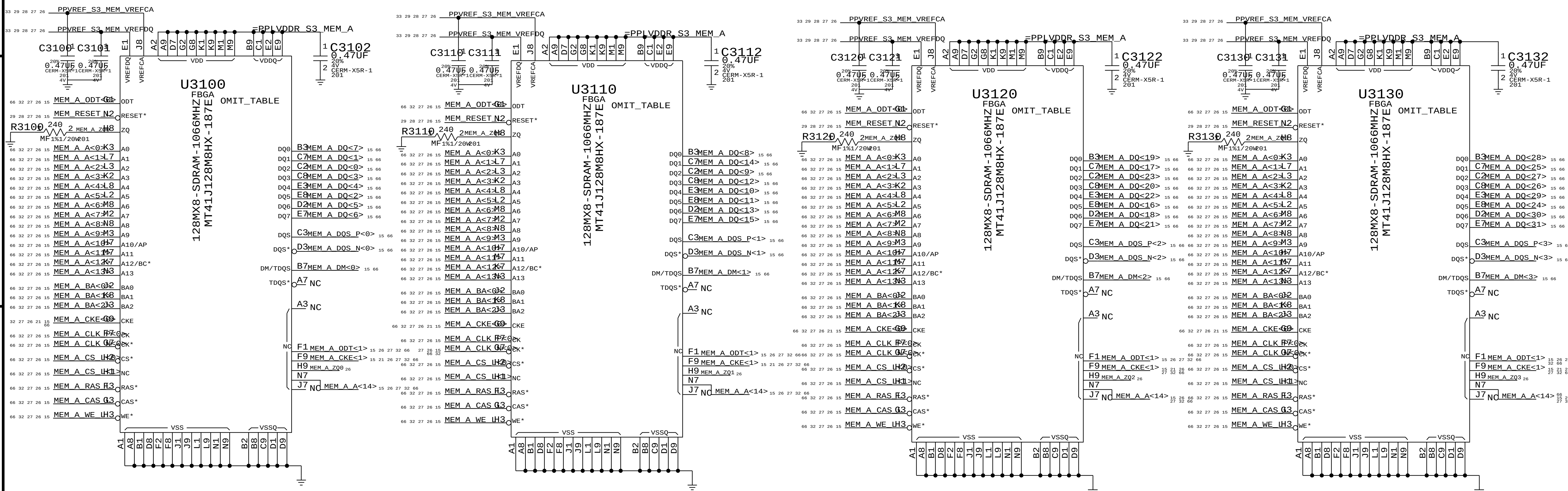

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

DDR3 DRAM Channel A (0-31)

Apple Inc.

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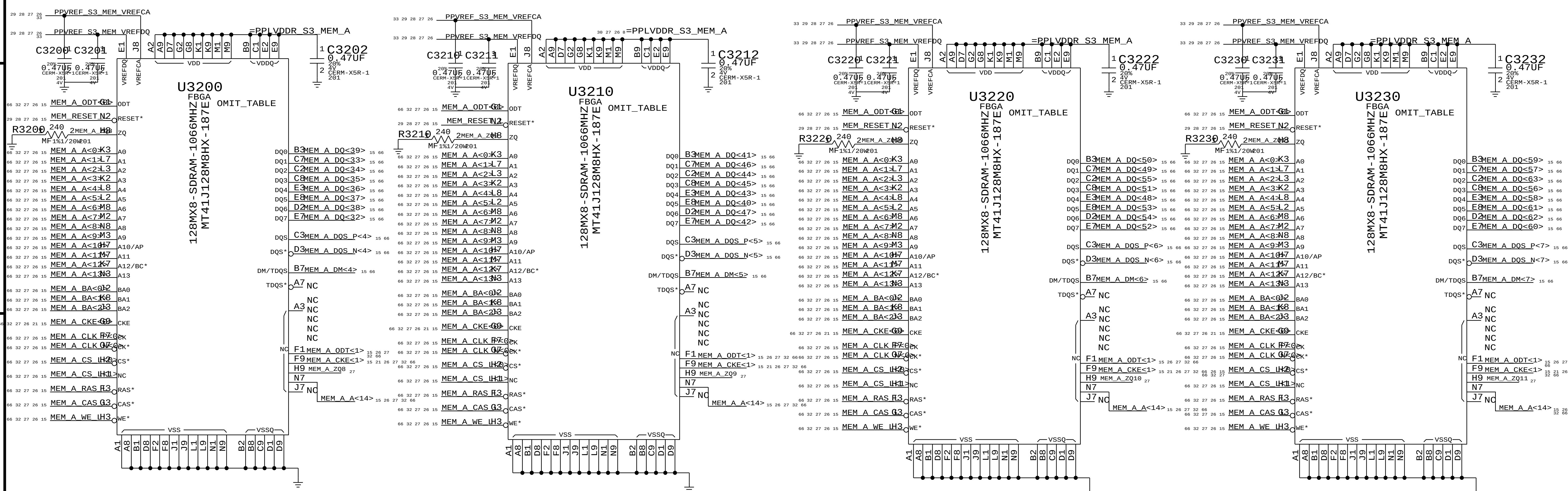
PAGE 31 OF 110

SHEET 26 OF 73



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
DDR3 DRAM Channel A (32-63)

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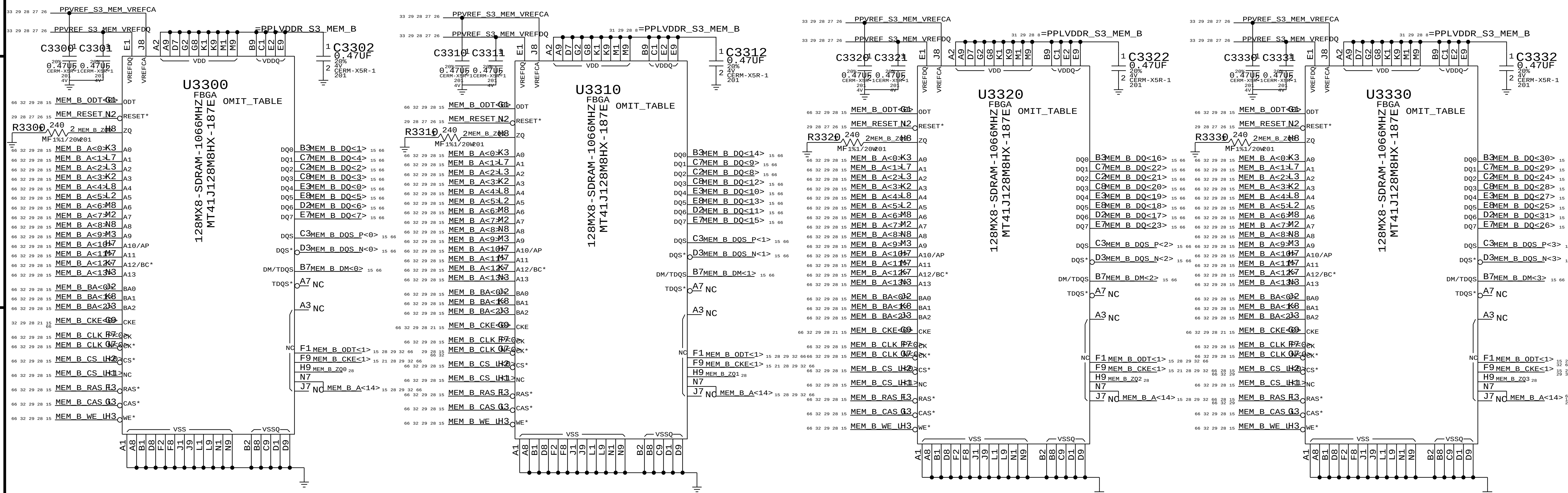

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

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PAGE TITLE
DDR3 DRAM Channel B (0-31)

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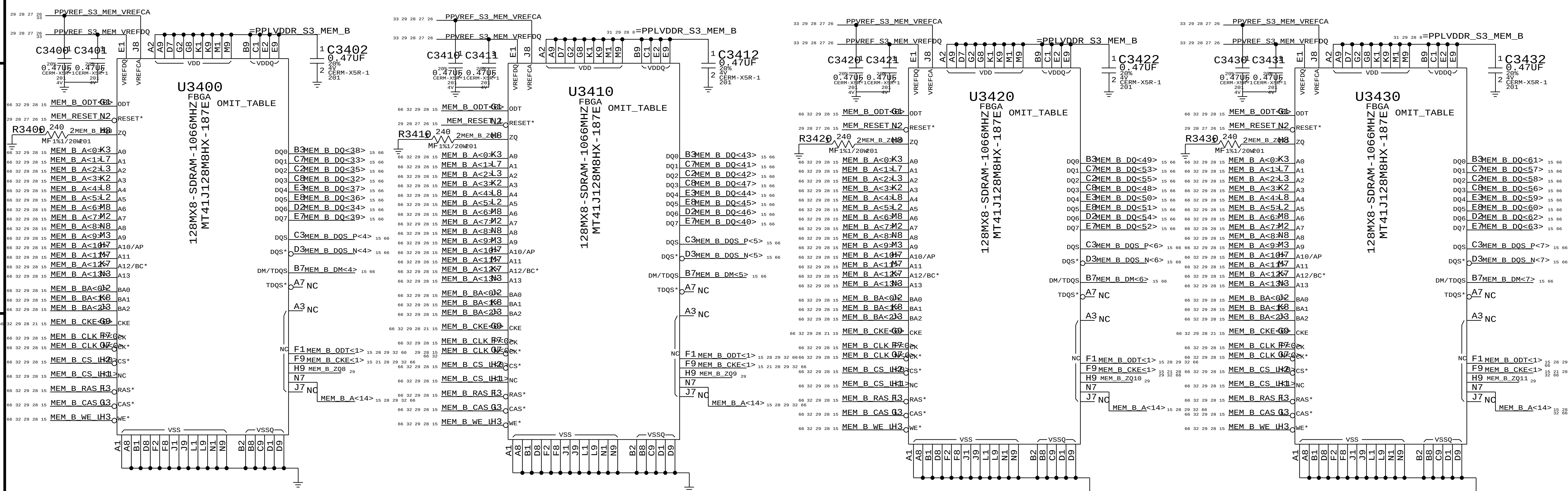

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

DDR3 DRAM Channel B (32-63)

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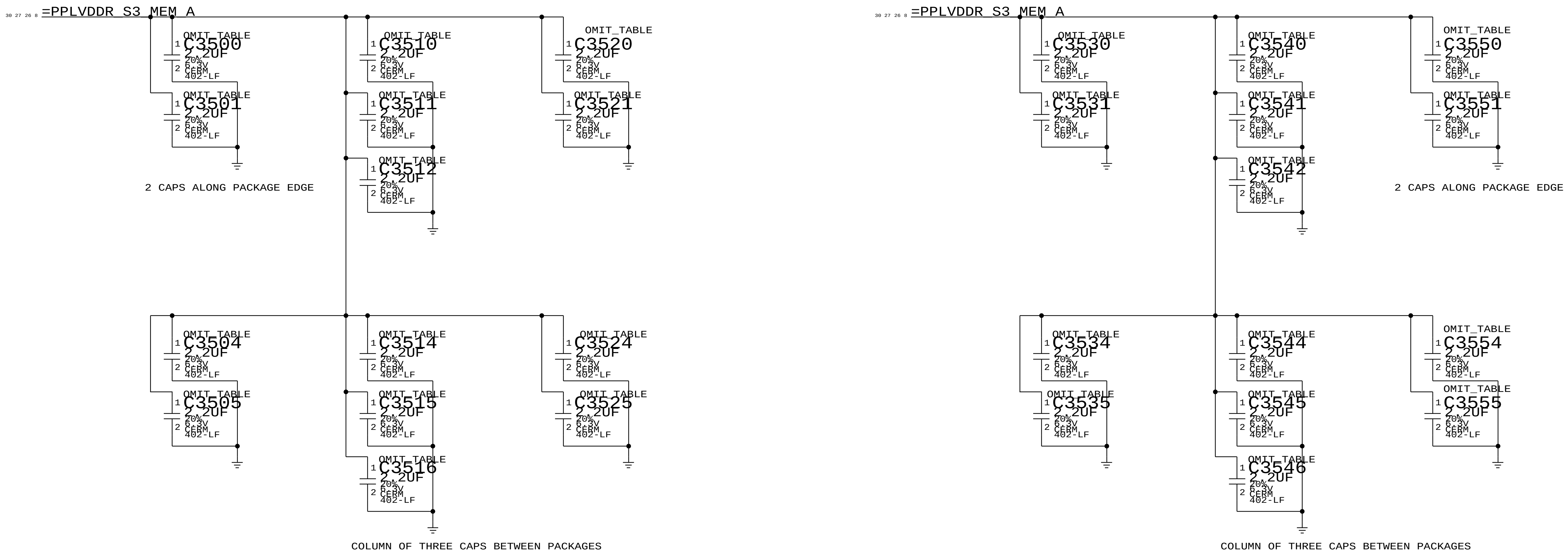

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

DDR BYPASSING 1

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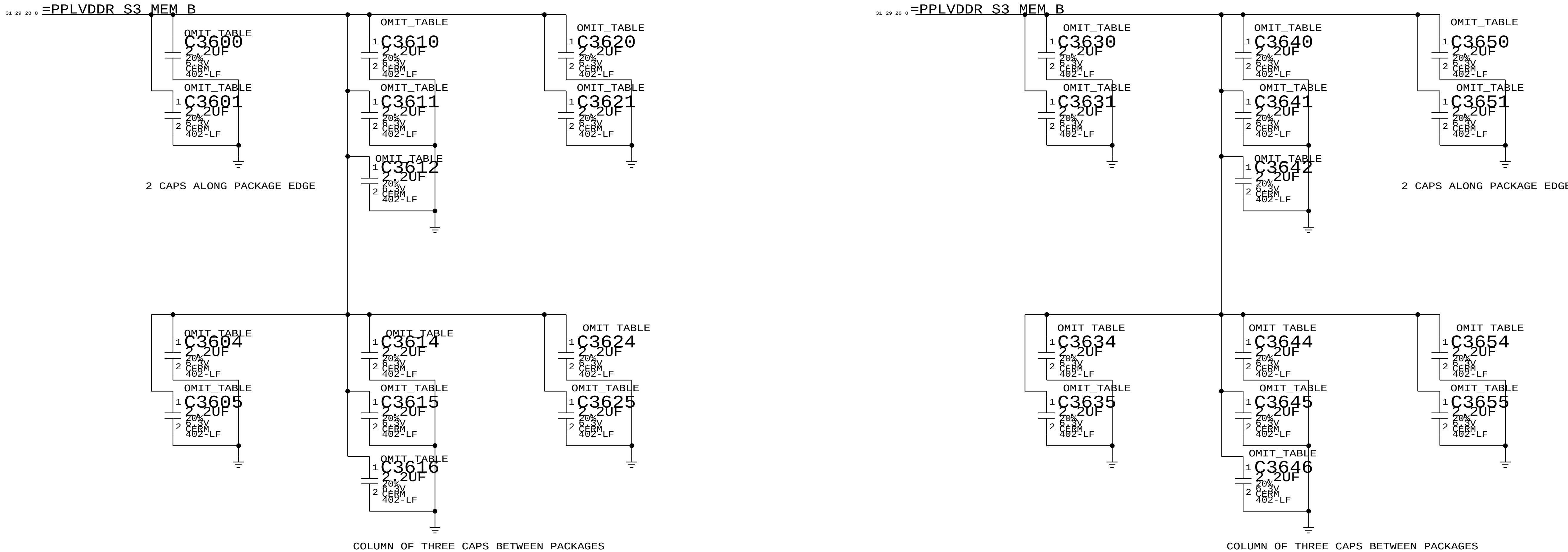
PAGE 35 OF 110

SHEET 30 OF 73



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

DDR BYPASSING 2

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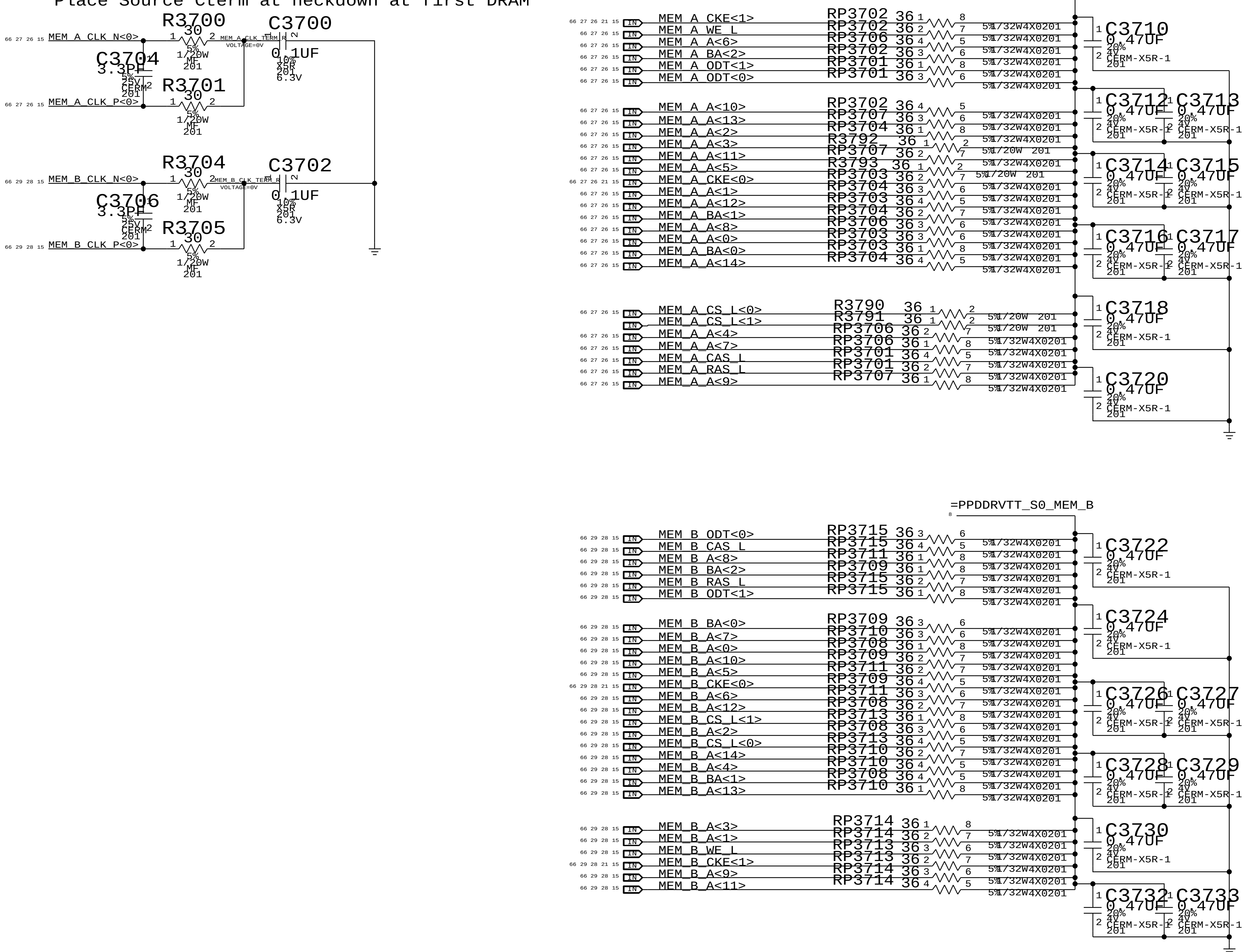
PAGE 36 OF 110

SHEET 31 OF 73

MEM CLOCK TERMINATION

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

Memory Active Termination

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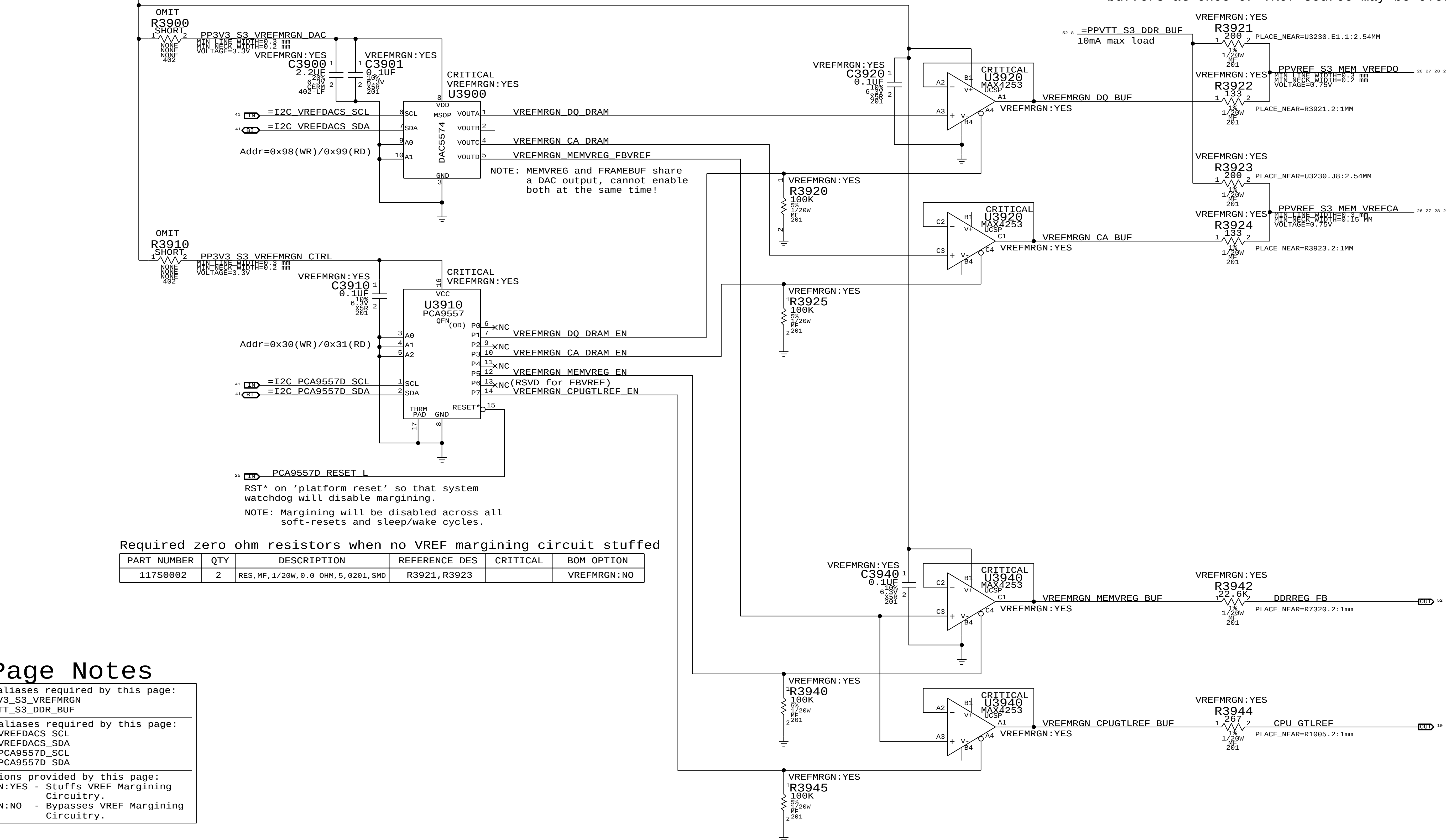
PAGE 37 OF 110

SHEET 32 OF 73

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3921,R3923		VREFMRGN:NO

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN:YES - Stuffs VREF Margining Circuitry.
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM VREF DQ	MEM VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	C	D	D
PCA9557D Pin:	1	3	5	7
Nominal value	0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)		1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
VRef current:	+3.4mA - -3.4mA (- = sourced)		+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:	7.69mV / step @ output		8.59mV / step @ output	9.24mV / step @ output

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
FSB/DDR3 Vref Margining

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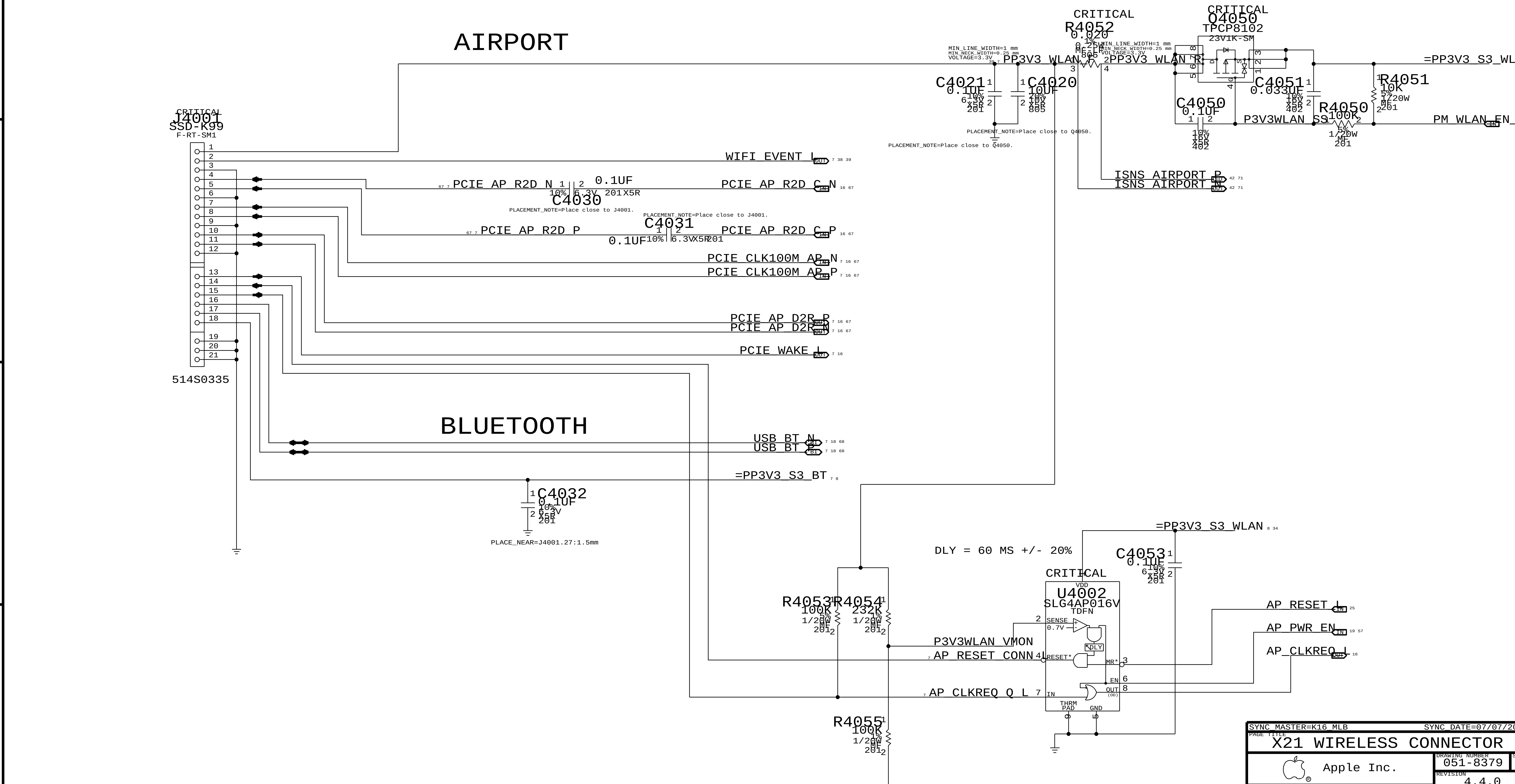
3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)



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PAGE TITLE

X21 WIRELESS CONNECTOR

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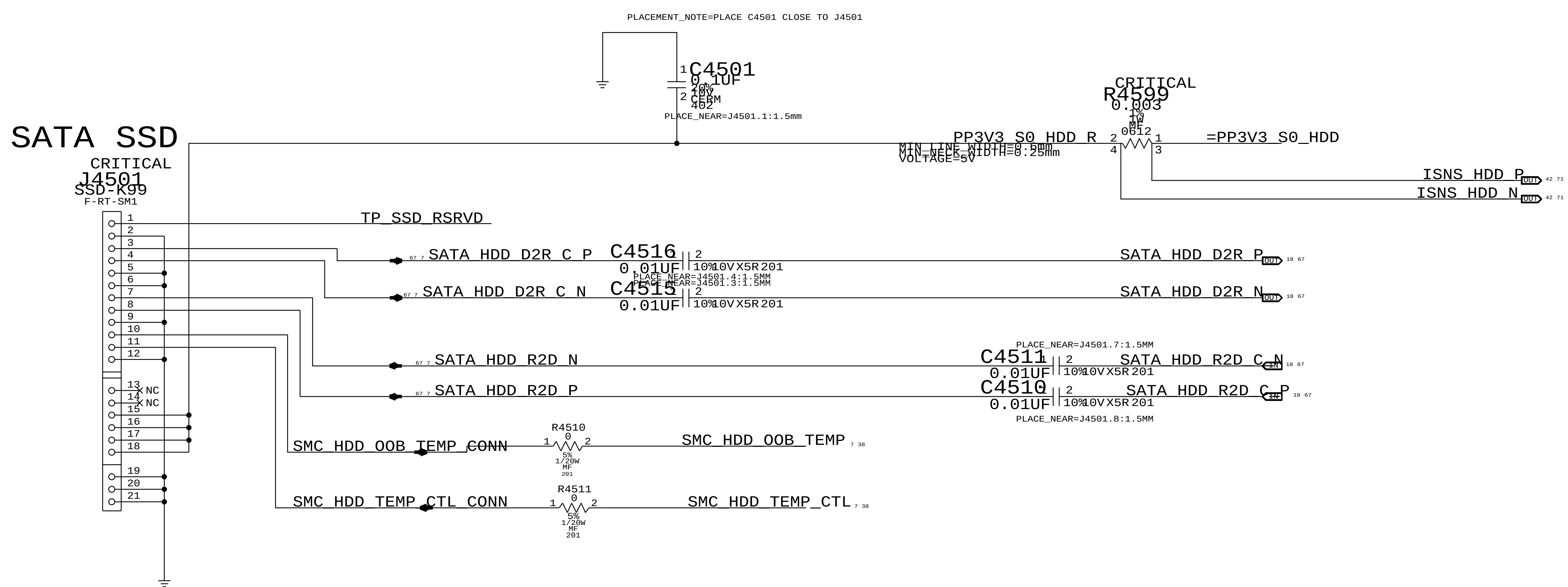

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PAGE TITLE

SATA CONNECTOR

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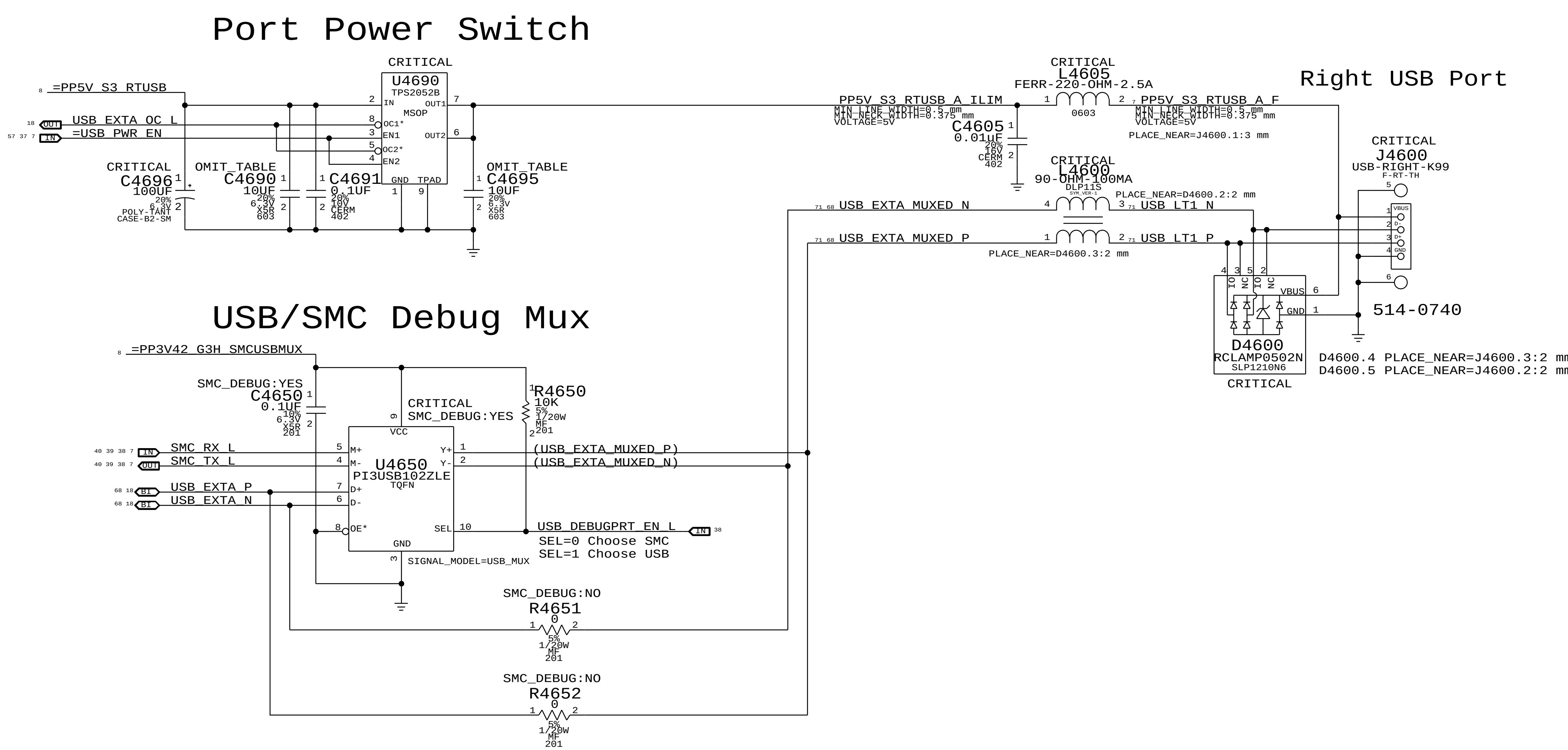
SHEET 35 OF 73



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

External USB Connectors

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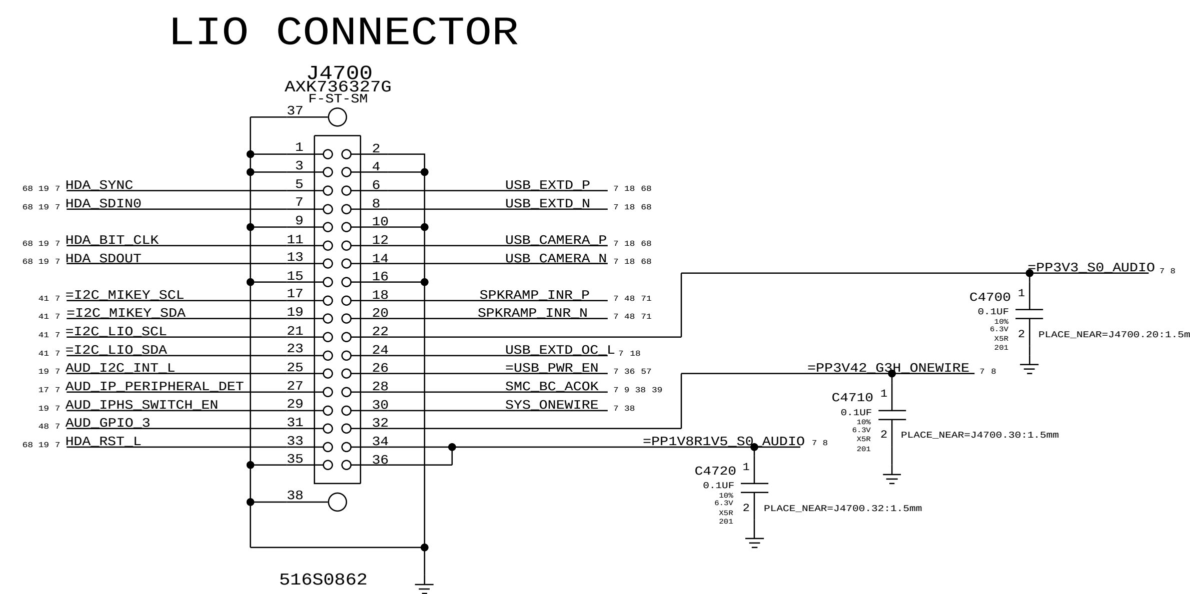

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

LIO CONNECTORS

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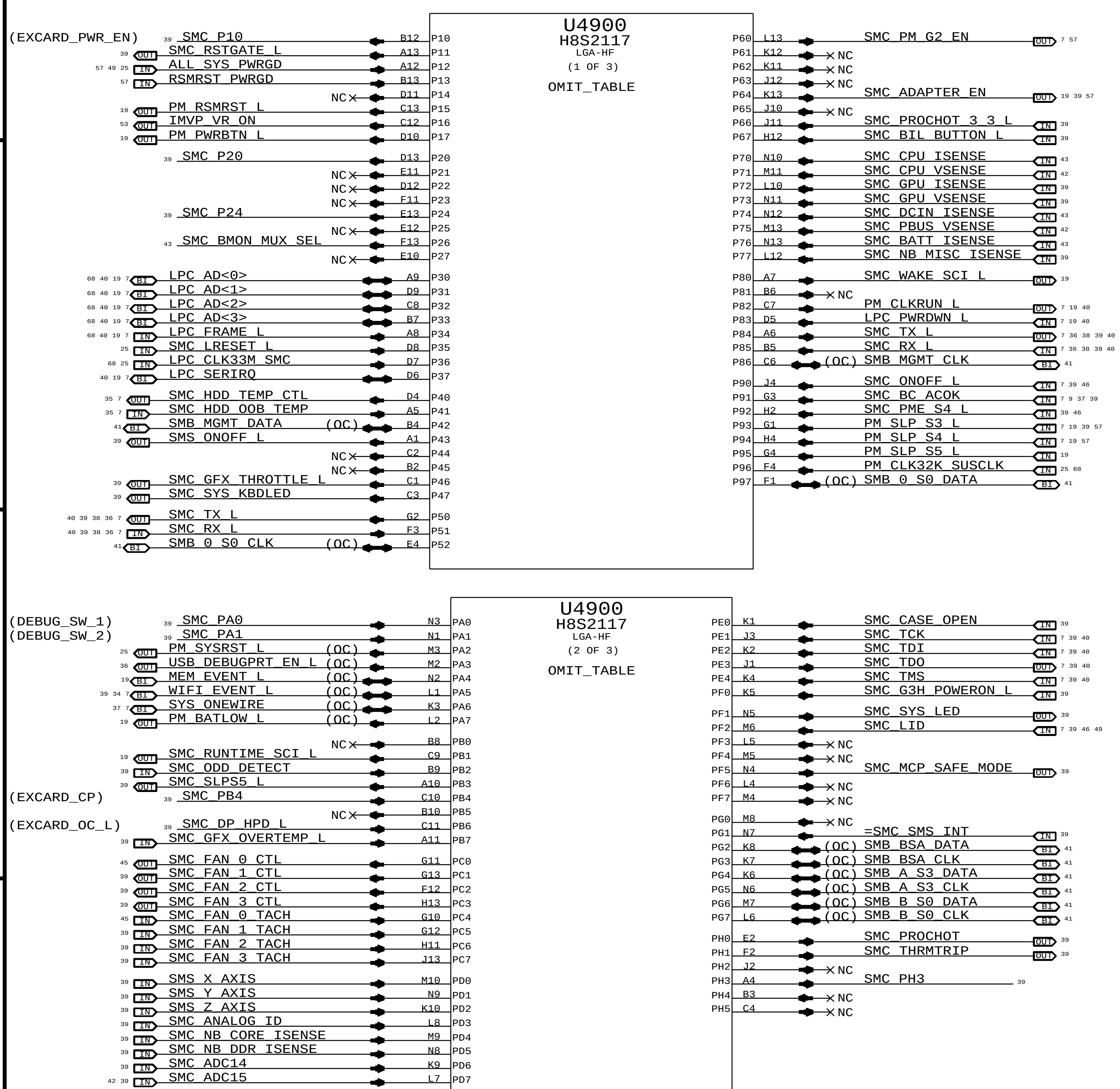
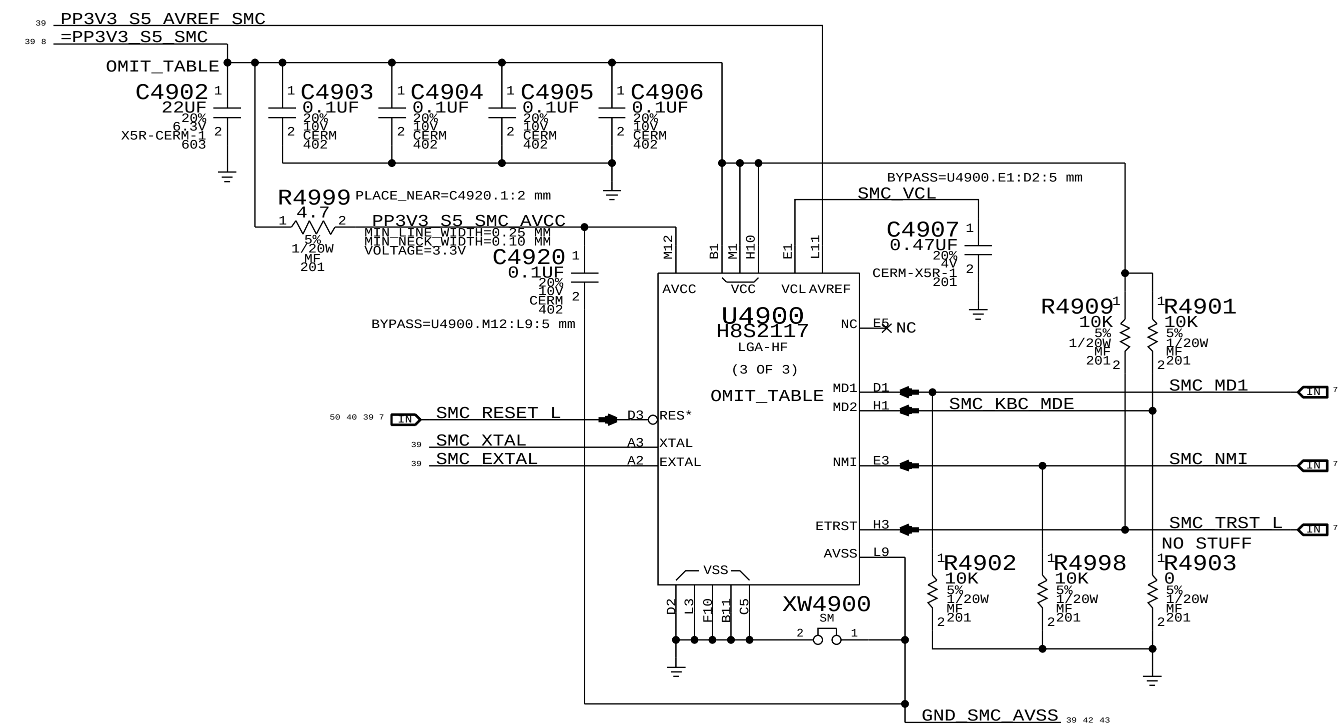
NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)

SYNC_MASTER=K16_MLB	SYNC_DATE=07/07/2010
PAGE TITLE	SMC
Apple Inc.	DRAWING NUMBER 051-8379 SIZE D
	REVISION 4.4.0
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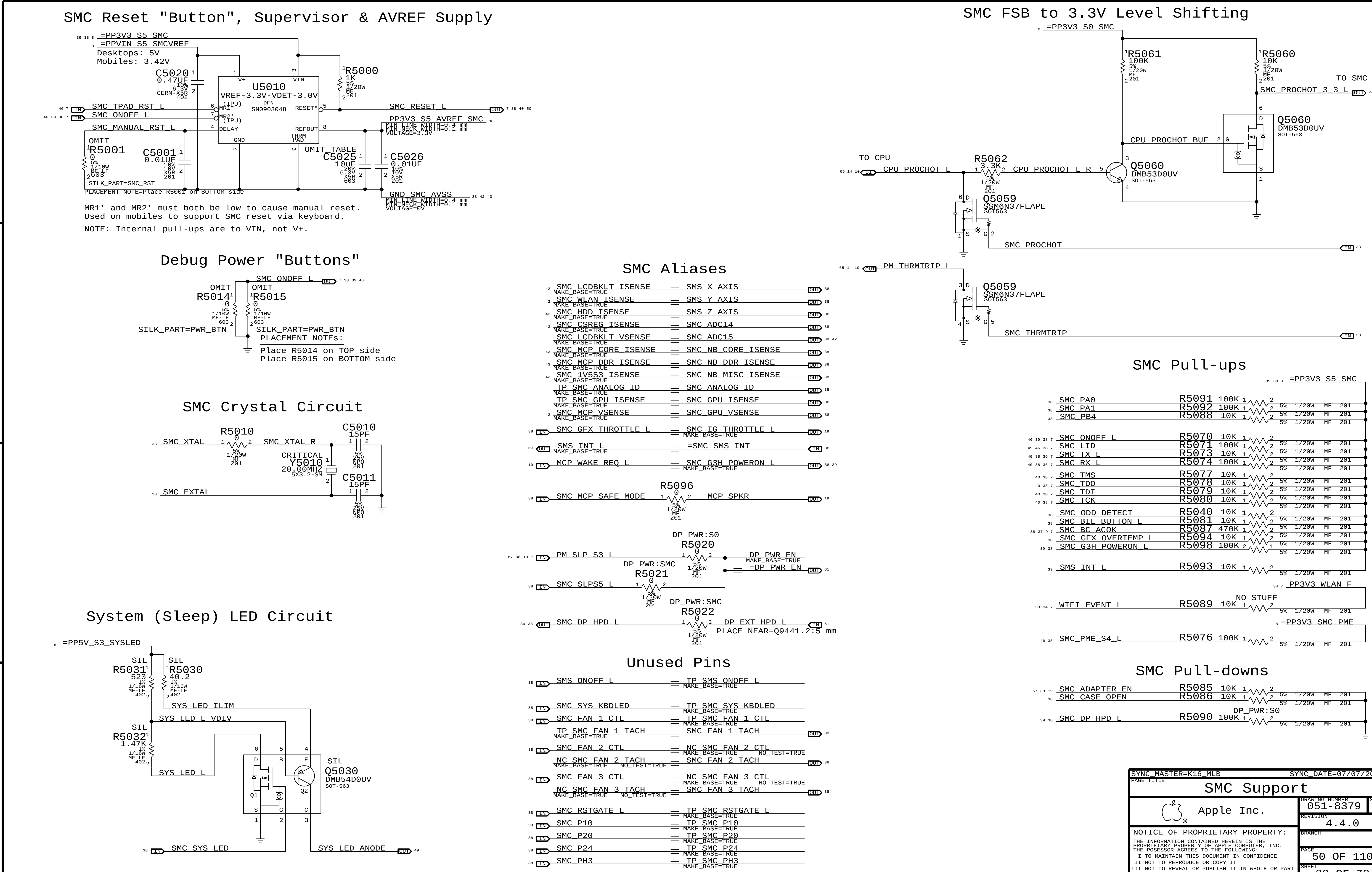
	PAGE 49 OF 110
	SHEET 38 OF 73



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: SMC Support

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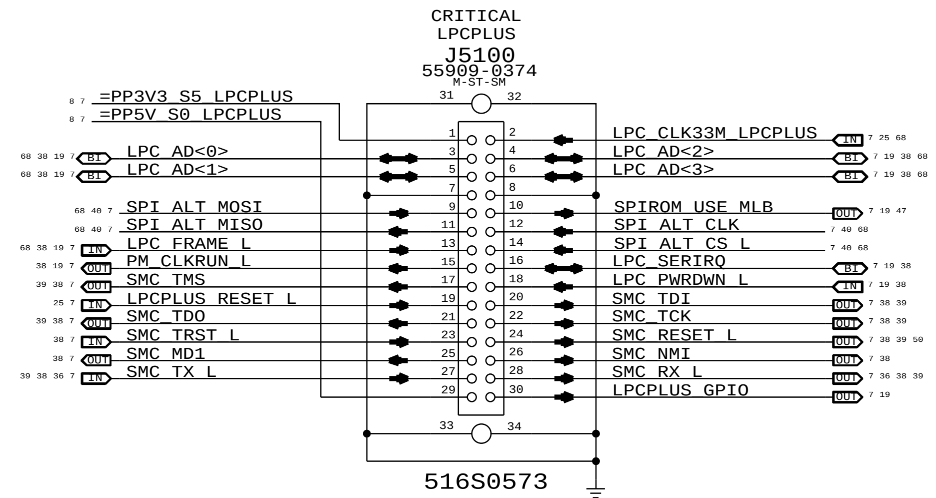
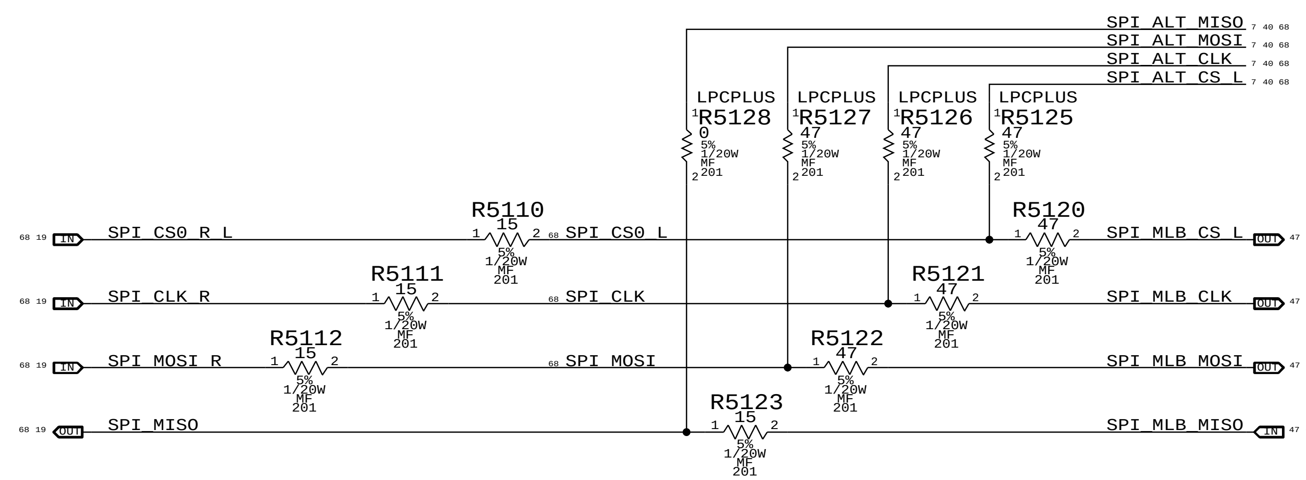
PAGE: 50 OF 110

SHEET: 39 OF 73

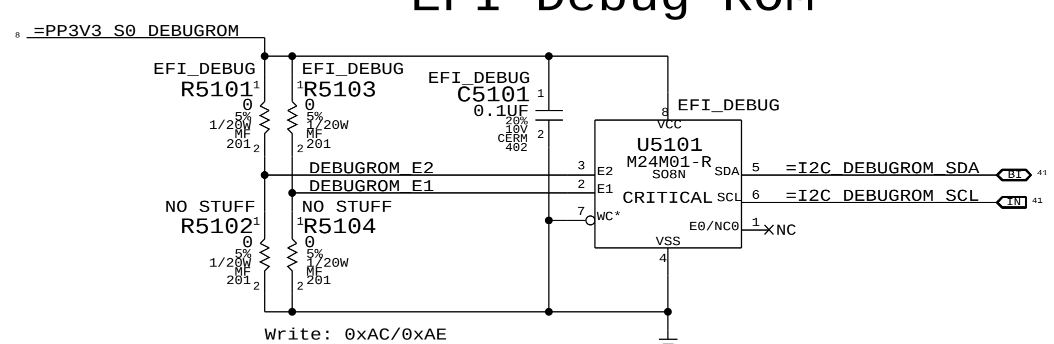
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: LPC+SPI Debug Connector

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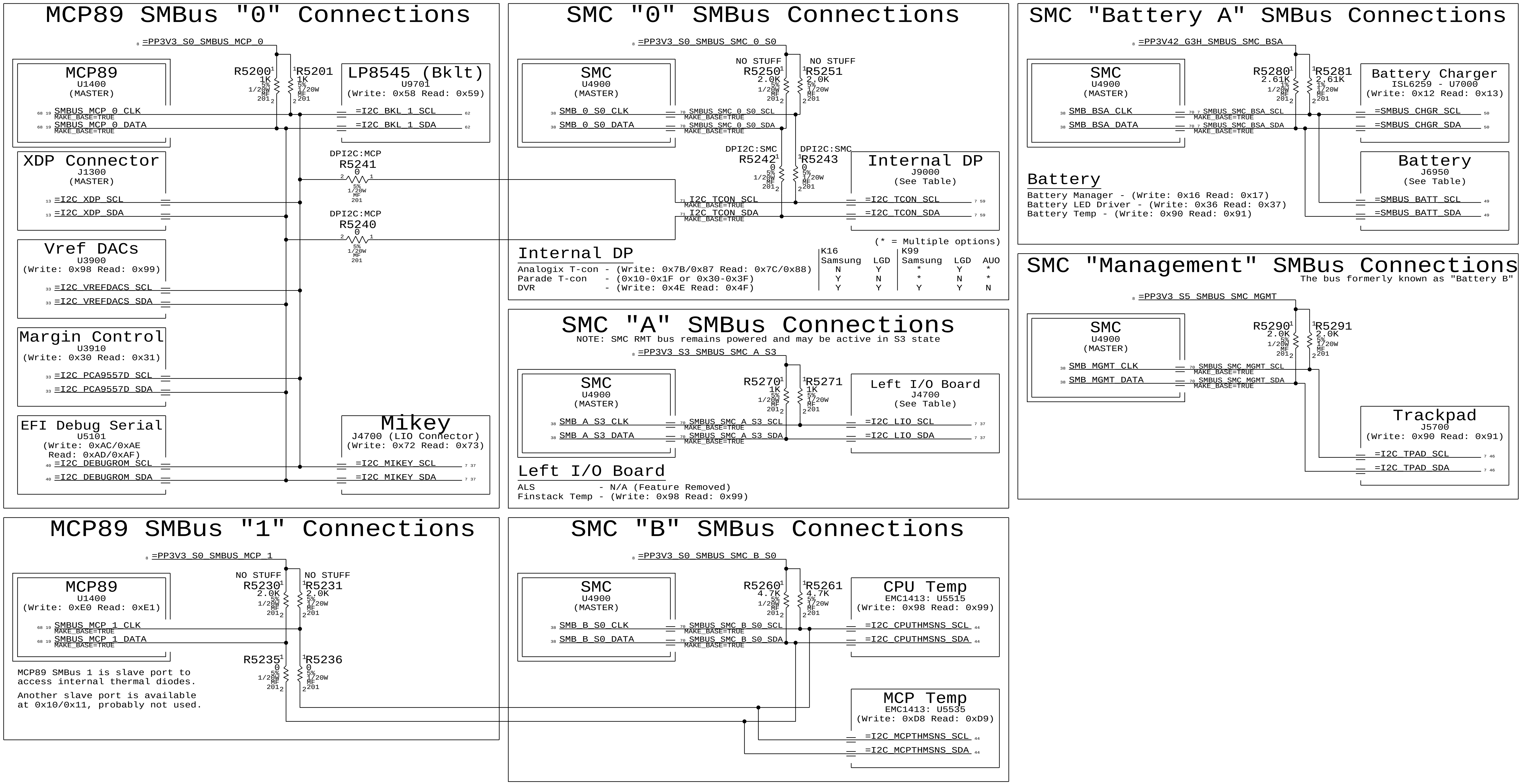

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
K16/K99 SMus Connections

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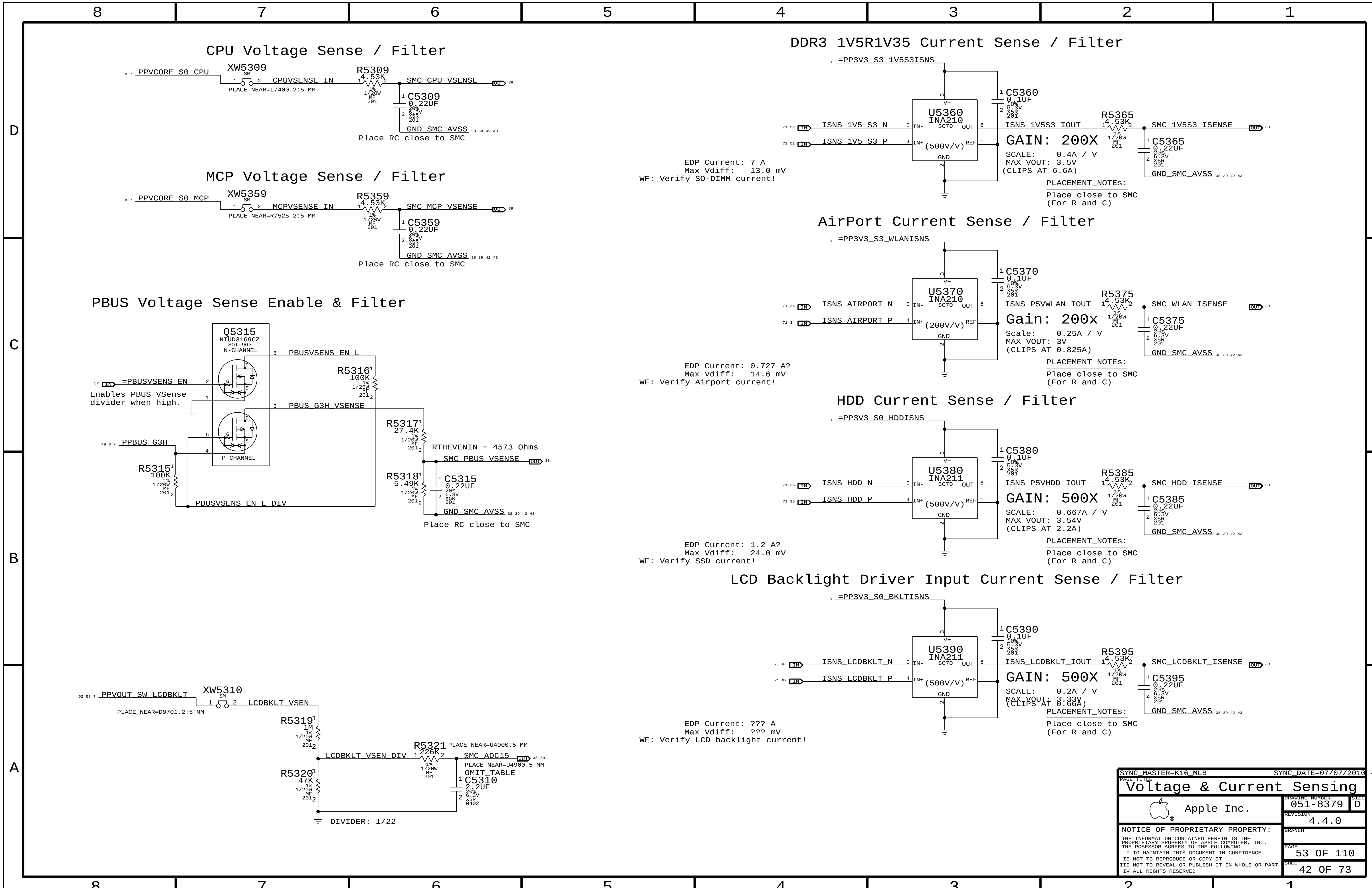
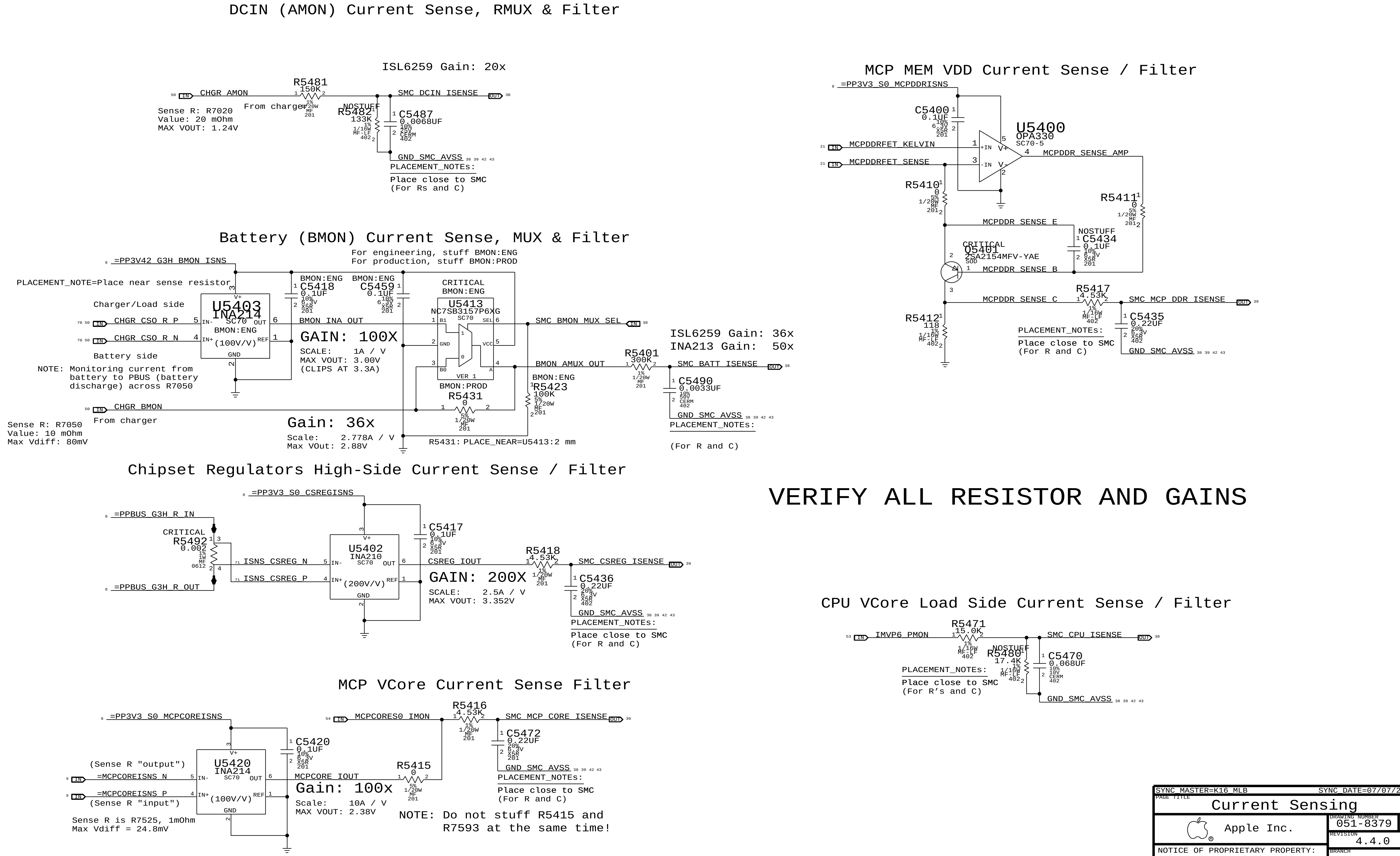

CPU Voltage Sense / Filter
PPVCORE_S0_CPU
XW5309
SM
CPUVSENSE_IN
PLACE_NEAR=L7400.2:5 MM
R5309
4.53K
1%
1/20W
MF
201
SMC_CPU_VSENSE
C5309
0.22UF
20%
6.3V
X5R
201
GND_SMC_AVSS
Place RC close to SMC
MCP Voltage Sense / Filter
PPVCORE_S0_MCP
XW5359
MCPVSENSE_IN
PLACE_NEAR=R7525.2:5 MM
R5359
4.53K
SMC_MCP_VSENSE
C5359
0.22UF
GND_SMC_AVSS
Place RC close to SMC
PBUS Voltage Sense Enable & Filter
Q5315
NTUD3169CZ
SOT-963
N-CHANNEL
P-CHANNEL
PBUSVSENS_EN_L
R5316
100K
=PBUSVSENS_EN
Enables PBUS VSense
divider when high.
PBUS_G3H_VSENSE
R5317
27.4K
RTHEVENIN = 4573 Ohms
PPBUS_G3H
SMC_PBUS_VSENSE
R5315
100K
R5318
5.49K
C5315
0.22UF
PBUSVSENS_EN_L_DIV
GND_SMC_AVSS
Place RC close to SMC
PPVOUT_SW_LCDBKLT
XW5310
LCDBKLT_VSEN
PLACE_NEAR=D9701.2:5 MM
R5319
1M
R5321
226K
PLACE_NEAR=U4900:5 MM
LCDBKLT_VSEN_DIV
SMC_ADC15
PLACE_NEAR=U4900:5 MM
OMIT_TABLE
C5310
2.2UF
0402
R5320
47K
DIVIDER: 1/22
DDR3 1V5R1V35 Current Sense / Filter
=PP3V3_S3_1V5S3ISNS
C5360
0.1UF
U5360
INA210
SC70
ISNS_1V5_S3_N
ISNS_1V5_S3_P
(500V/V)
ISNS_1V5S3_IOUT
R5365
4.53K
SMC_1V5S3_ISENSE
GAIN: 200X
SCALE: 0.4A / V
MAX VOUT: 3.5V
(CLIPS AT 6.6A)
C5365
0.22UF
GND_SMC_AVSS
EDP Current: 7 A
Max Vdiff: 13.0 mV
WF: Verify SO-DIMM current!
PLACEMENT_NOTES:
Place close to SMC
(For R and C)
AirPort Current Sense / Filter
=PP3V3_S3_WLANISNS
C5370
0.1UF
U5370
INA210
ISNS_AIRPORT_N
ISNS_AIRPORT_P
(200V/V)
ISNS_P5VWLAN_IOUT
R5375
4.53K
SMC_WLAN_ISENSE
Gain: 200x
Scale: 0.25A / V
MAX VOUT: 3V
(CLIPS AT 0.825A)
C5375
0.22UF
GND_SMC_AVSS
EDP Current: 0.727 A?
Max Vdiff: 14.6 mV
WF: Verify Airport current!
PLACEMENT_NOTES:
Place close to SMC
(For R and C)
HDD Current Sense / Filter
=PP3V3_S0_HDDISNS
C5380
0.1UF
U5380
INA211
ISNS_HDD_N
ISNS_HDD_P
(500V/V)
ISNS_P5VHDD_IOUT
R5385
4.53K
SMC_HDD_ISENSE
GAIN: 500X
SCALE: 0.667A / V
MAX VOUT: 3.54V
(CLIPS AT 2.2A)
C5385
0.22UF
GND_SMC_AVSS
EDP Current: 1.2 A?
Max Vdiff: 24.0 mV
WF: Verify SSD current!
PLACEMENT_NOTES:
Place close to SMC
(For R and C)
LCD Backlight Driver Input Current Sense / Filter
=PP3V3_S0_BKLTISNS
C5390
0.1UF
U5390
INA211
ISNS_LCDBKLT_N
ISNS_LCDBKLT_P
(500V/V)
ISNS_LCDBKLT_IOUT
R5395
4.53K
SMC_LCDBKLT_ISENSE
GAIN: 500X
SCALE: 0.2A / V
MAX VOUT: 3.33V
(CLIPS AT 0.66A)
C5395
0.22UF
GND_SMC_AVSS
EDP Current: ??? A
Max Vdiff: ??? mV
WF: Verify LCD backlight current!
PLACEMENT_NOTES:
Place close to SMC
(For R and C)
SYNC_MASTER=K16_MLB
SYNC_DATE=07/07/2010
Voltage & Current Sensing
Apple Inc.
DRAWING NUMBER 051-8379
SIZE D
REVISION 4.4.0
PAGE 53 OF 110
SHEET 42 OF 73



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: Current Sensing

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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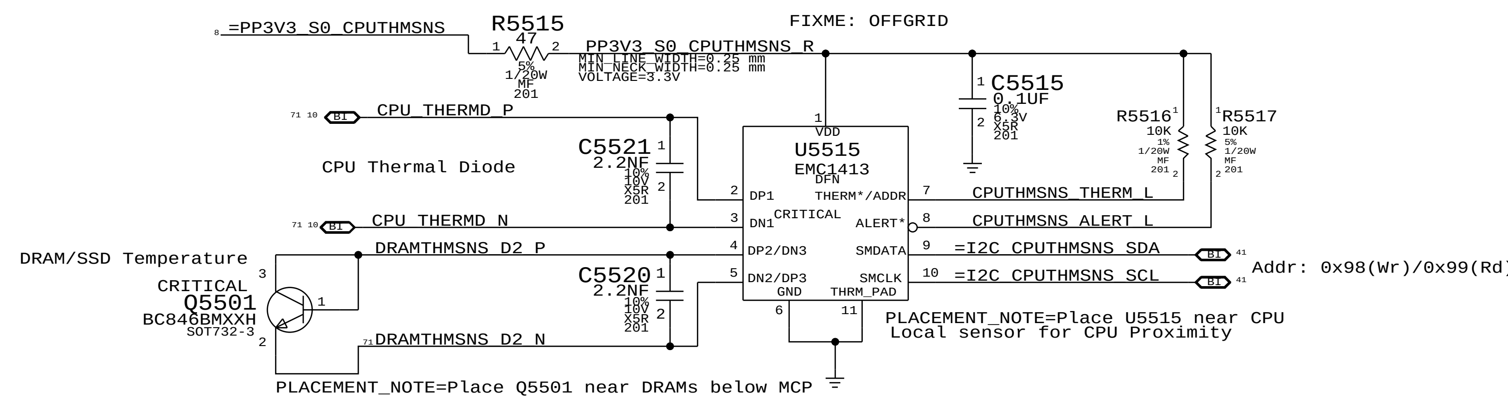
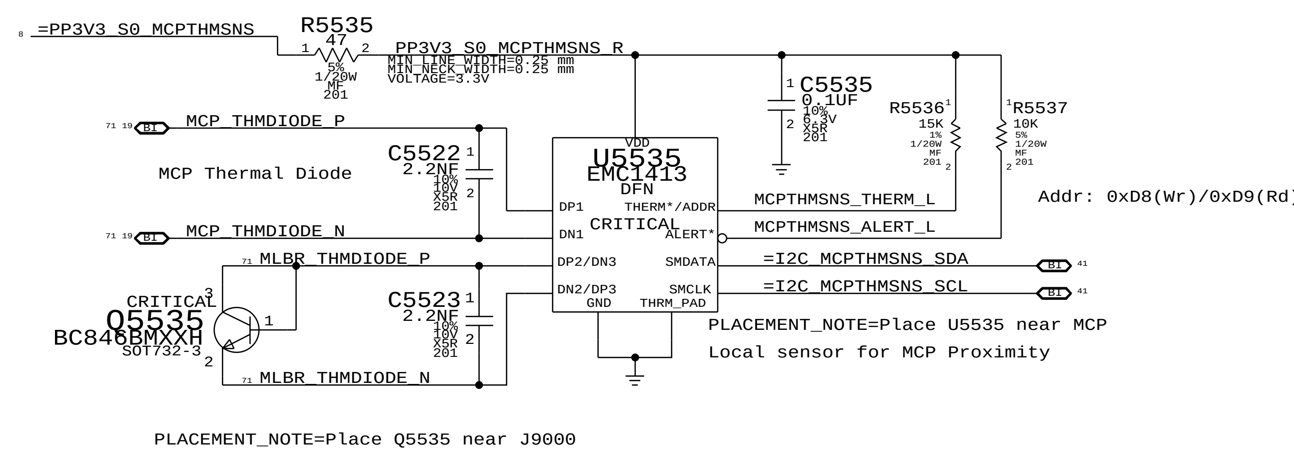
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

Thermal Sensors

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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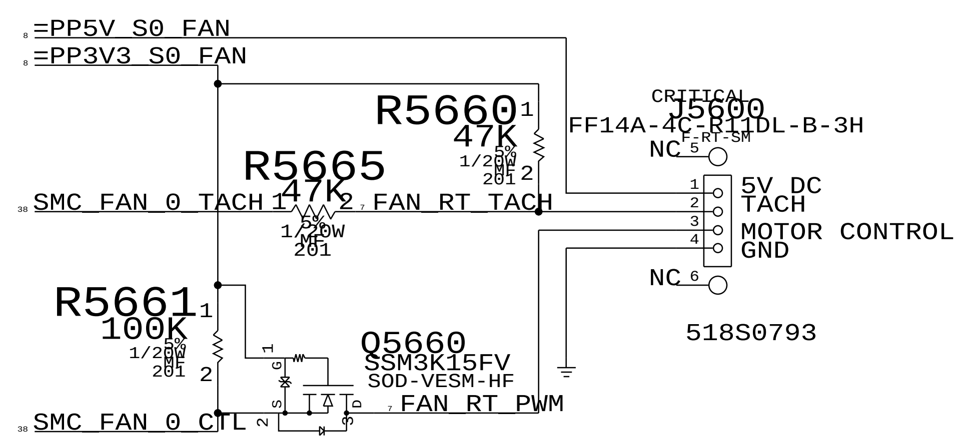
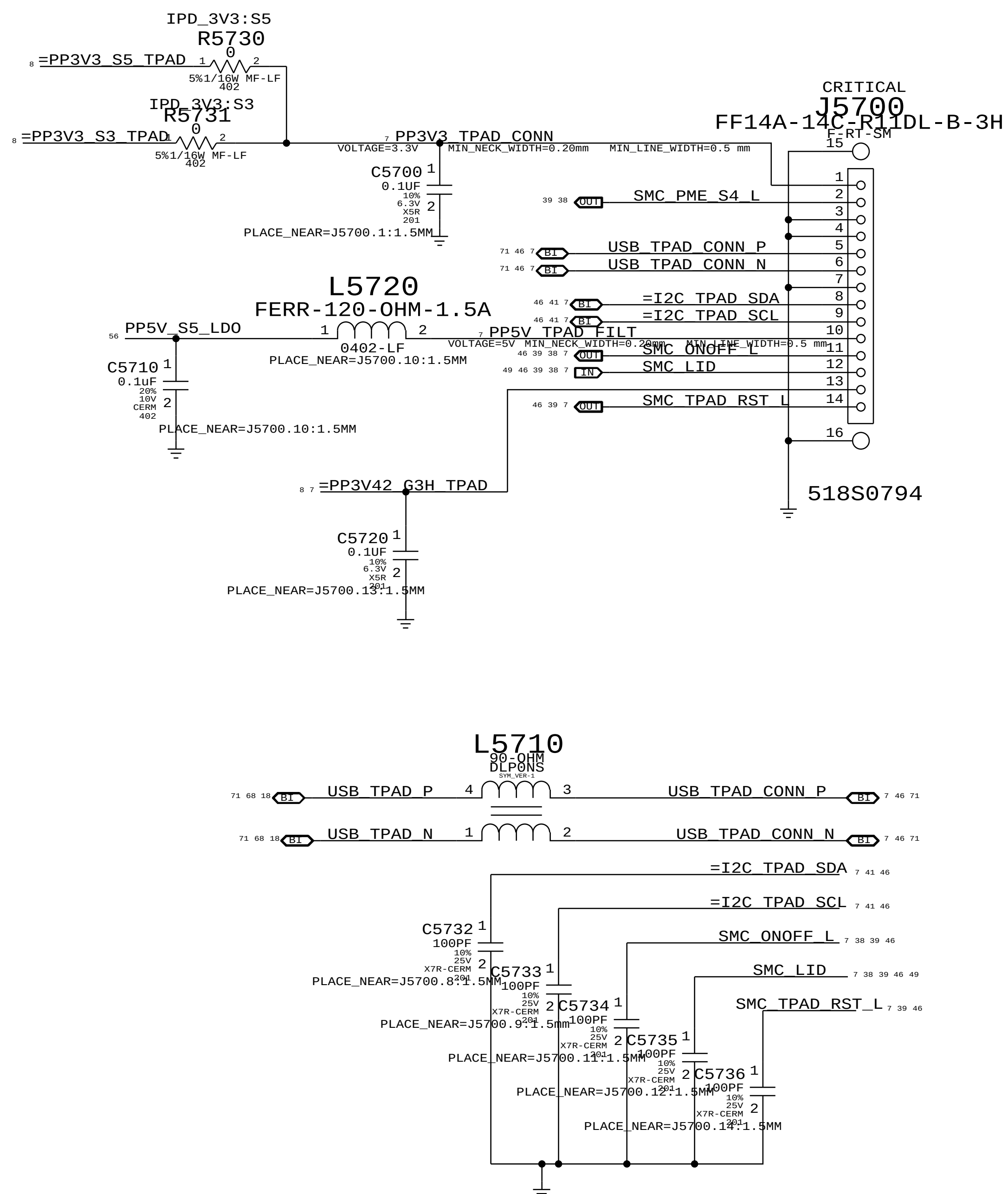
FAN CONNECTOR



IPD Flex Connector



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

WELLSPRING 1

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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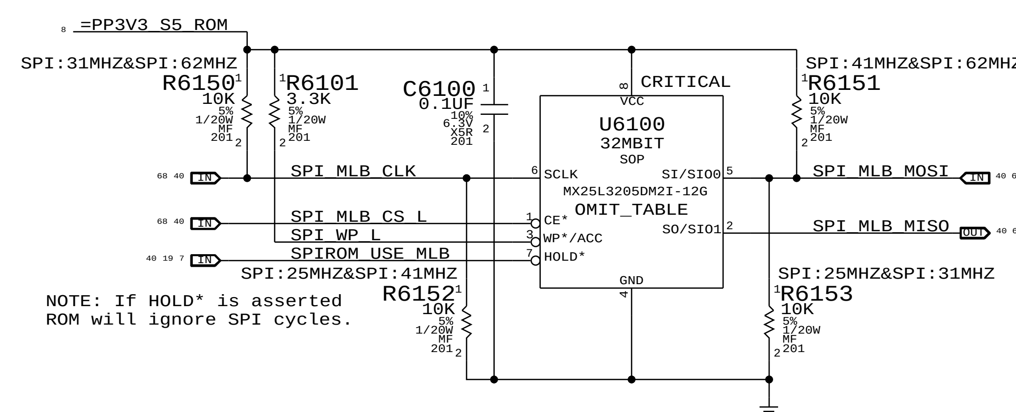

MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
SPI ROM

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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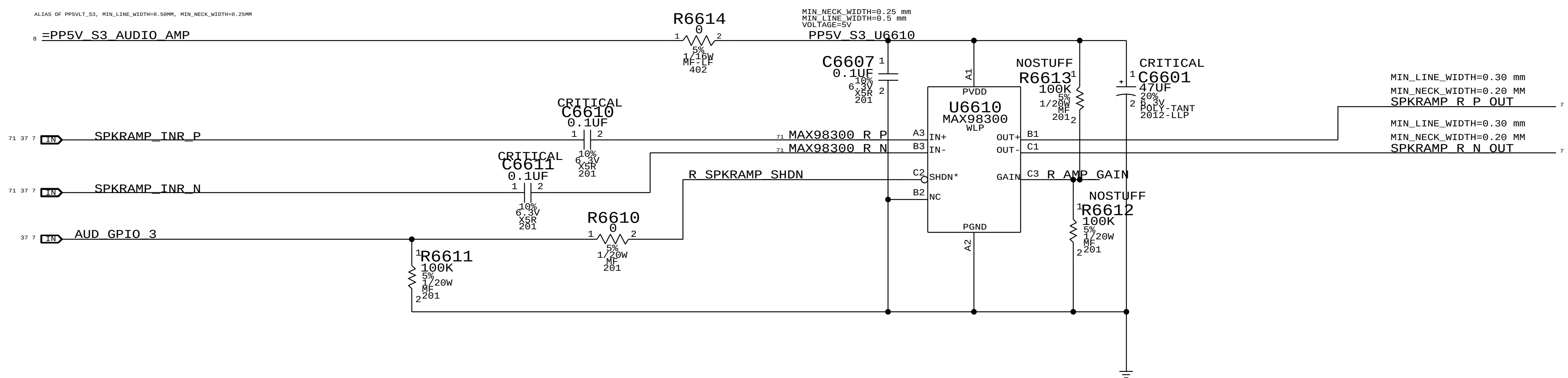
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



SYNC_MASTER=AUDIO	SYNC_DATE=02/09/2010
PAGE TITLE: AUDIO: SPEAKER AMP	
Apple Inc.	DRAWING NUMBER: 051-8379 SIZE: D
	REVISION: 4.4.0
NOTICE OF PROPRIETARY PROPERTY:	BRANCH
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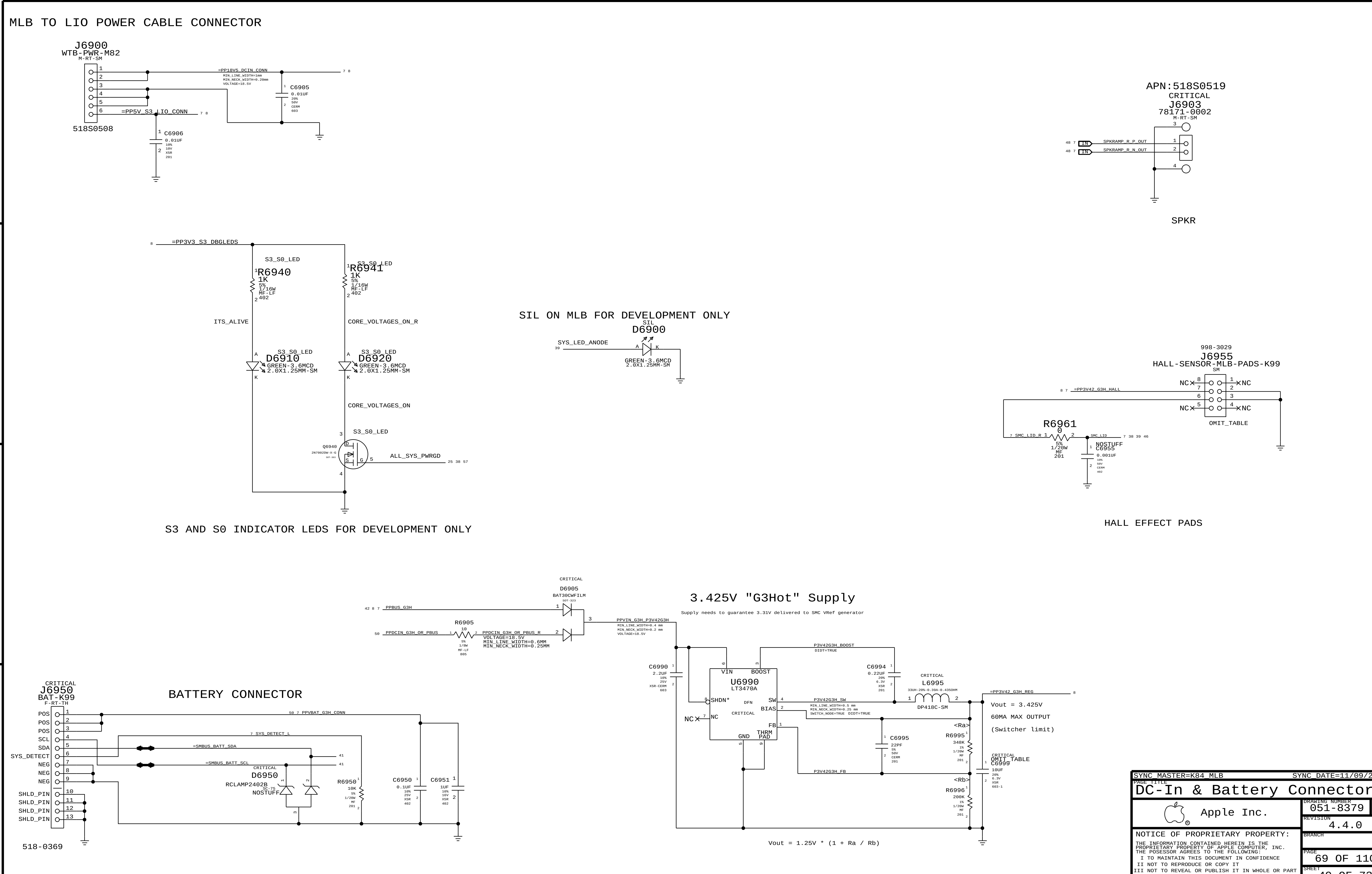
	SHEET: 48 OF 73



SYNC_MASTER=K84_MLB SYNC_DATE=11/09/2009

PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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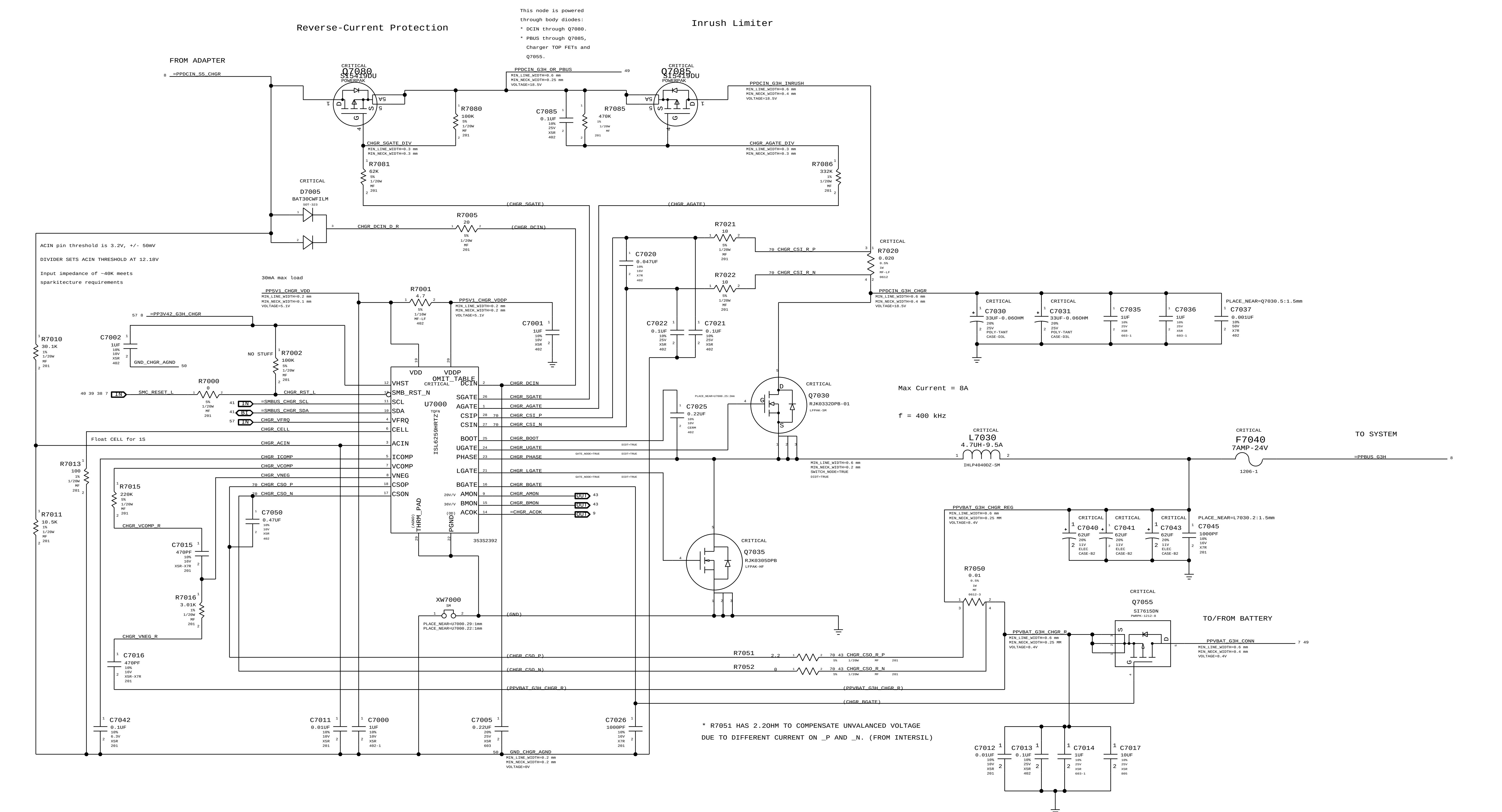
PAGE 69 OF 110

SHEET 49 OF 73



K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT

SYNC_MASTER=K6_MLB SYNC_DATE=11/09/2009

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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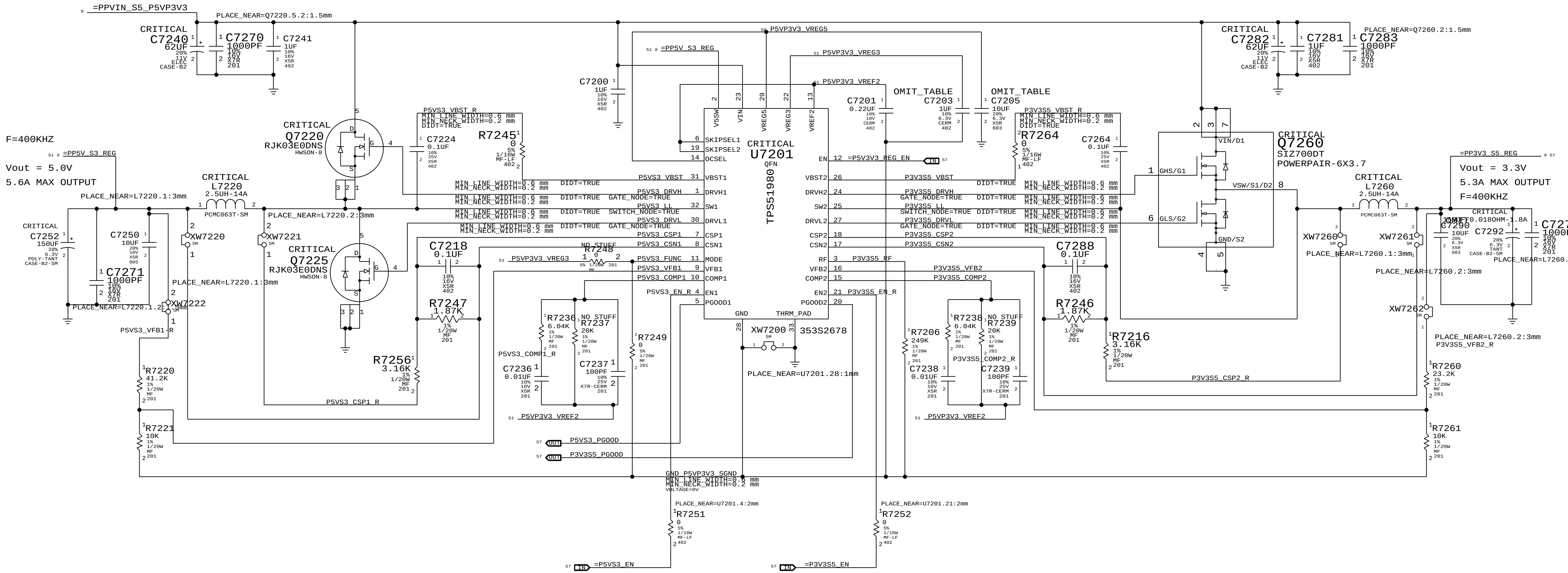
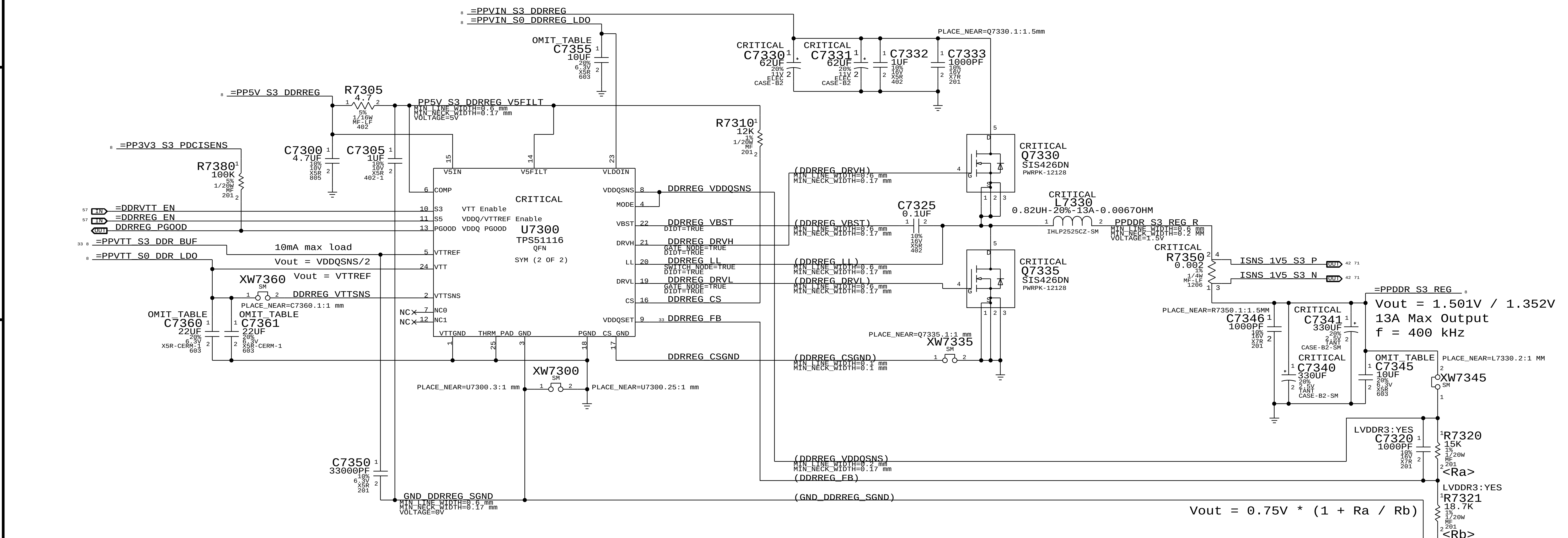


SYNC_MASTER=K16_MLB	SYNC_DATE=07/07/2010
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER 051-8379 SIZE D
	REVISION 4.4.0
	BRANCH
	PAGE 72 OF 110
	SHEET 51 OF 73

NOTICE OF PROPRIETARY PROPERTY:



Use LVDDR3:YES for fixed 1.35V operation or LVDDR3:NO for fixed 1.5V operation.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0331	1	RES,15K,1%,1/16W,MF-LF,0402	R7321		LVDDR3:NO

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

1.5V/1.35V LVDDR3 Supply

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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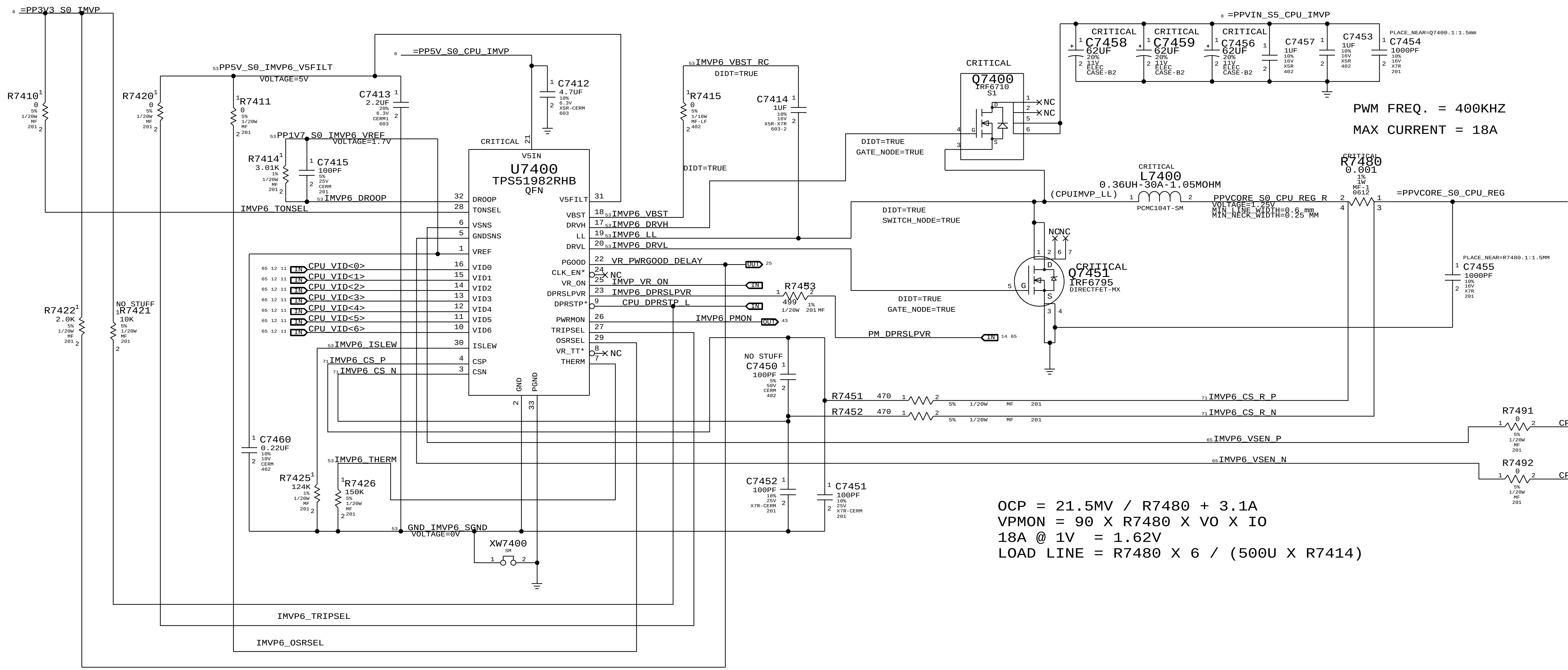
IMVP6 CPU VCORE REGULATOR



	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_THERM	0.25 MM	0.20 MM
IMVP6_ISLEW	0.25 MM	0.20 MM
PP1V7_S0_IMVP6_VREF	0.25 MM	0.20 MM
PP5V_S0_IMVP6_V5FILT	0.25 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_LL	1.5 MM	0.20 MM
IMVP6_VBST	0.25 MM	0.20 MM
IMVP6_DRVH	1.5 MM	0.20 MM
IMVP6_DRVL	1.5 MM	0.20 MM
IMVP6_VBST_RC	1.5 MM	0.20 MM

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

PAGE TITLE: IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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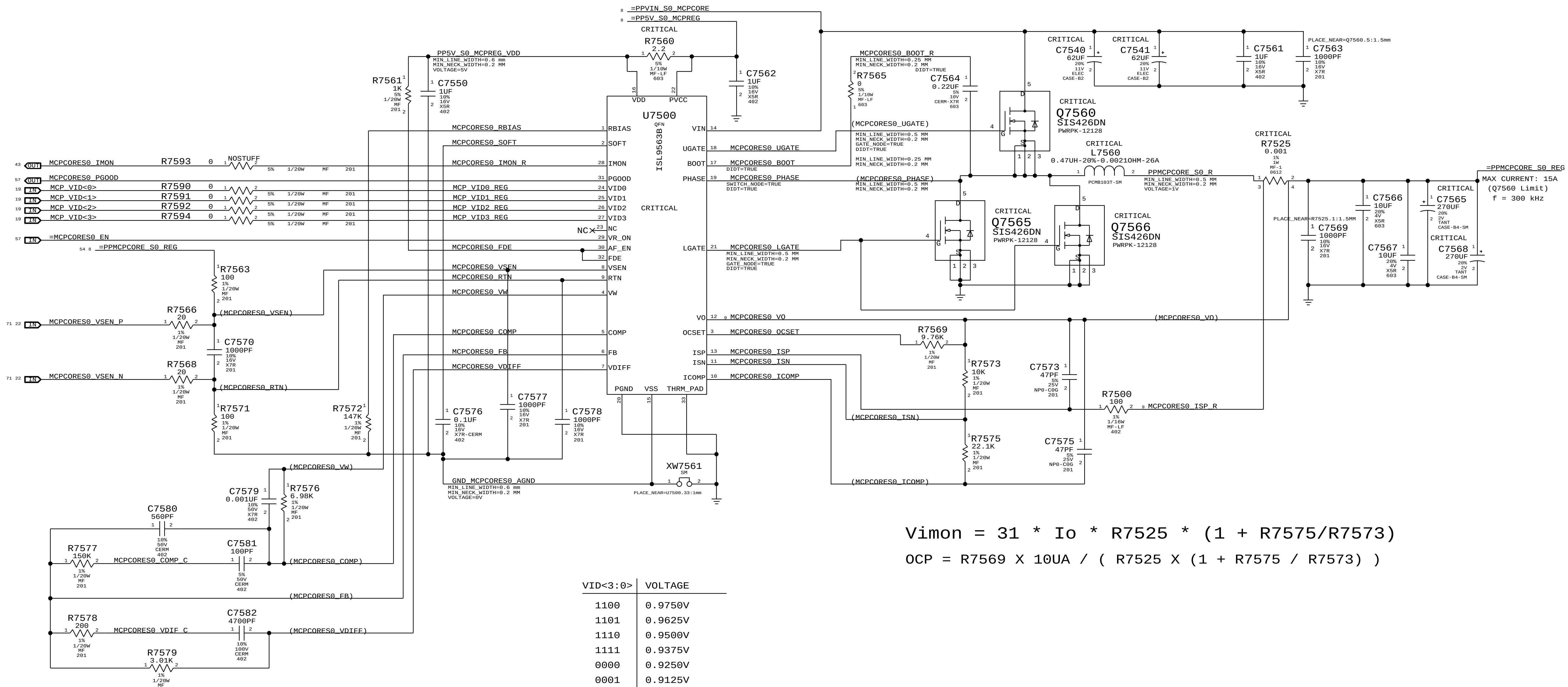

Vimon = 31 * Io * R7525 * (1 + R7575/R7573)

OCP = R7569 X 10UA / (R7525 X (1 + R7575 / R7573))

VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE

MCP VCore Regulator

Apple Inc.

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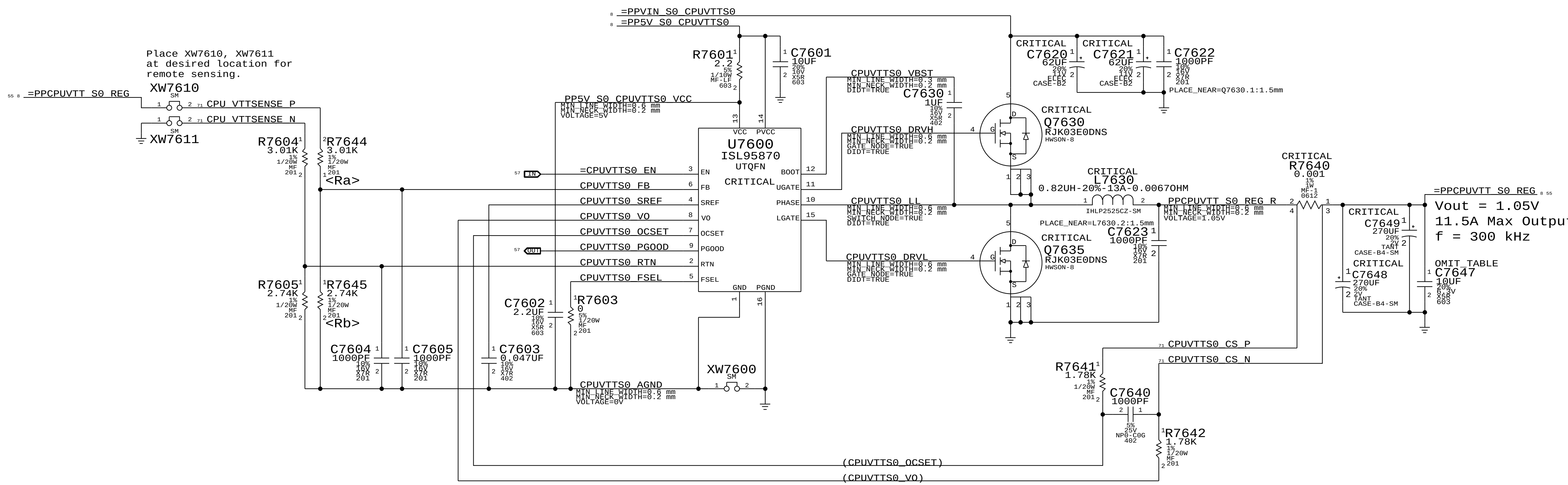

OCP = R7641 x 8.5uA / R7640
Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
CPUVTT (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D
REVISION 4.4.0
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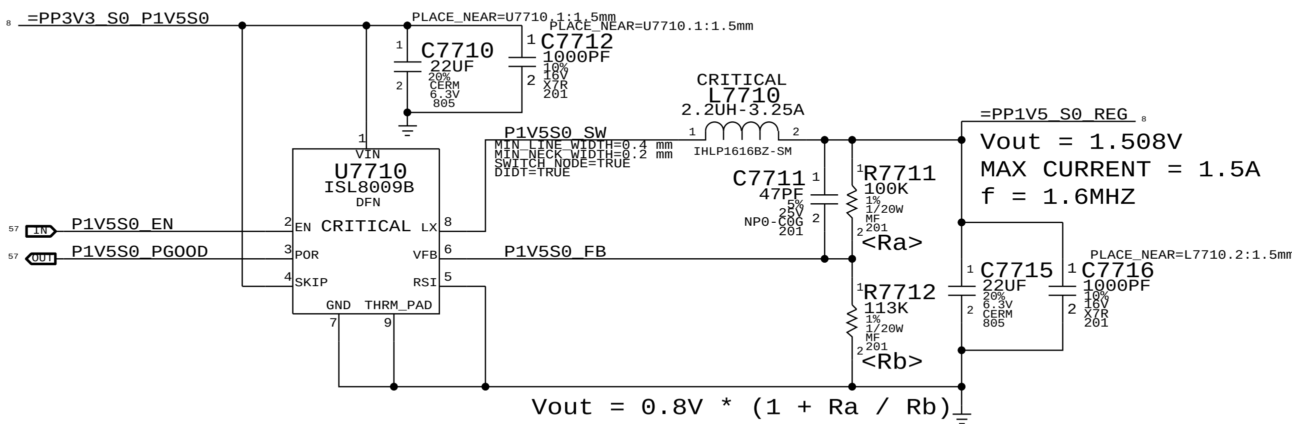
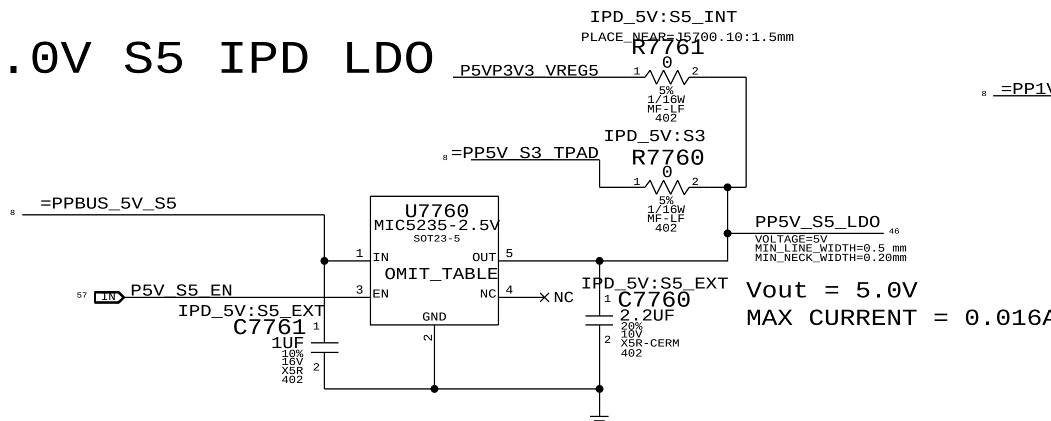
1.5V S0 Regulator

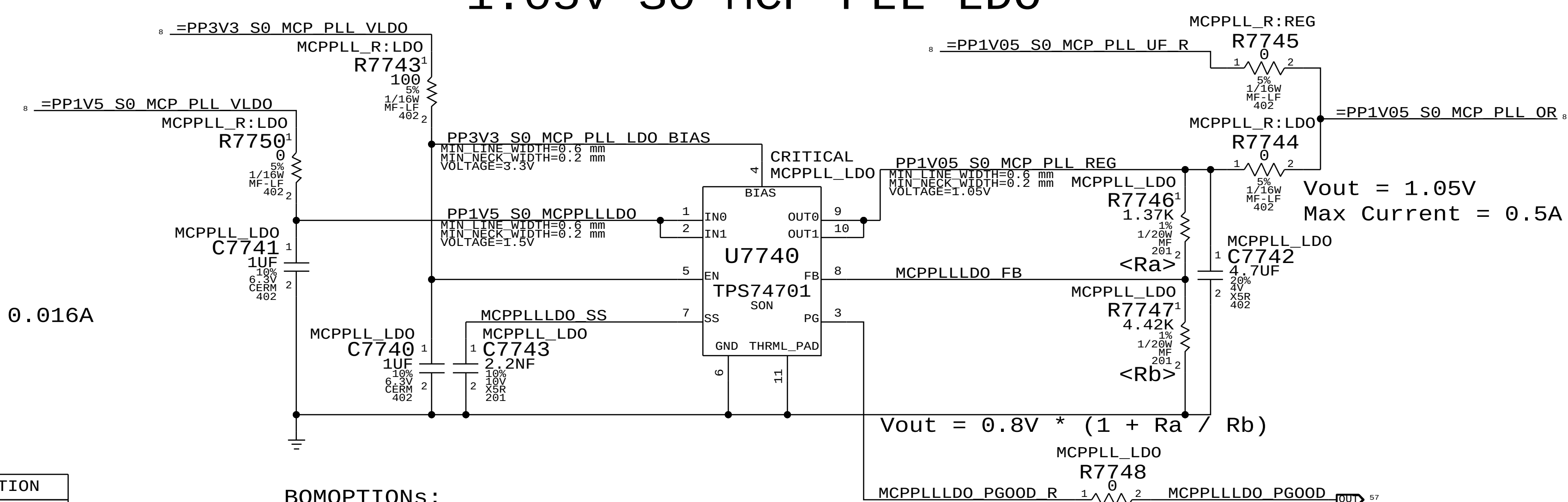


5.0V S5 IPD LDO



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3034	1	IC,LDO,MIC5235,5V,1%,150MA,SOT23-5	U7760		IPD_5V:S5_EXT

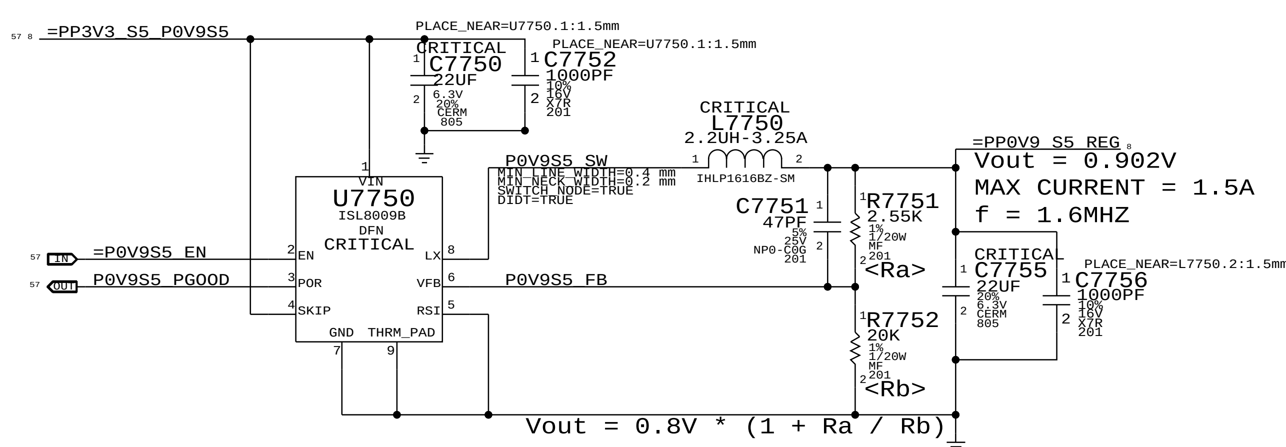
1.05V S0 MCP PLL LDO



BOMOPTIONs:

MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

MCP 0.9V S5 (AUXC) Switcher



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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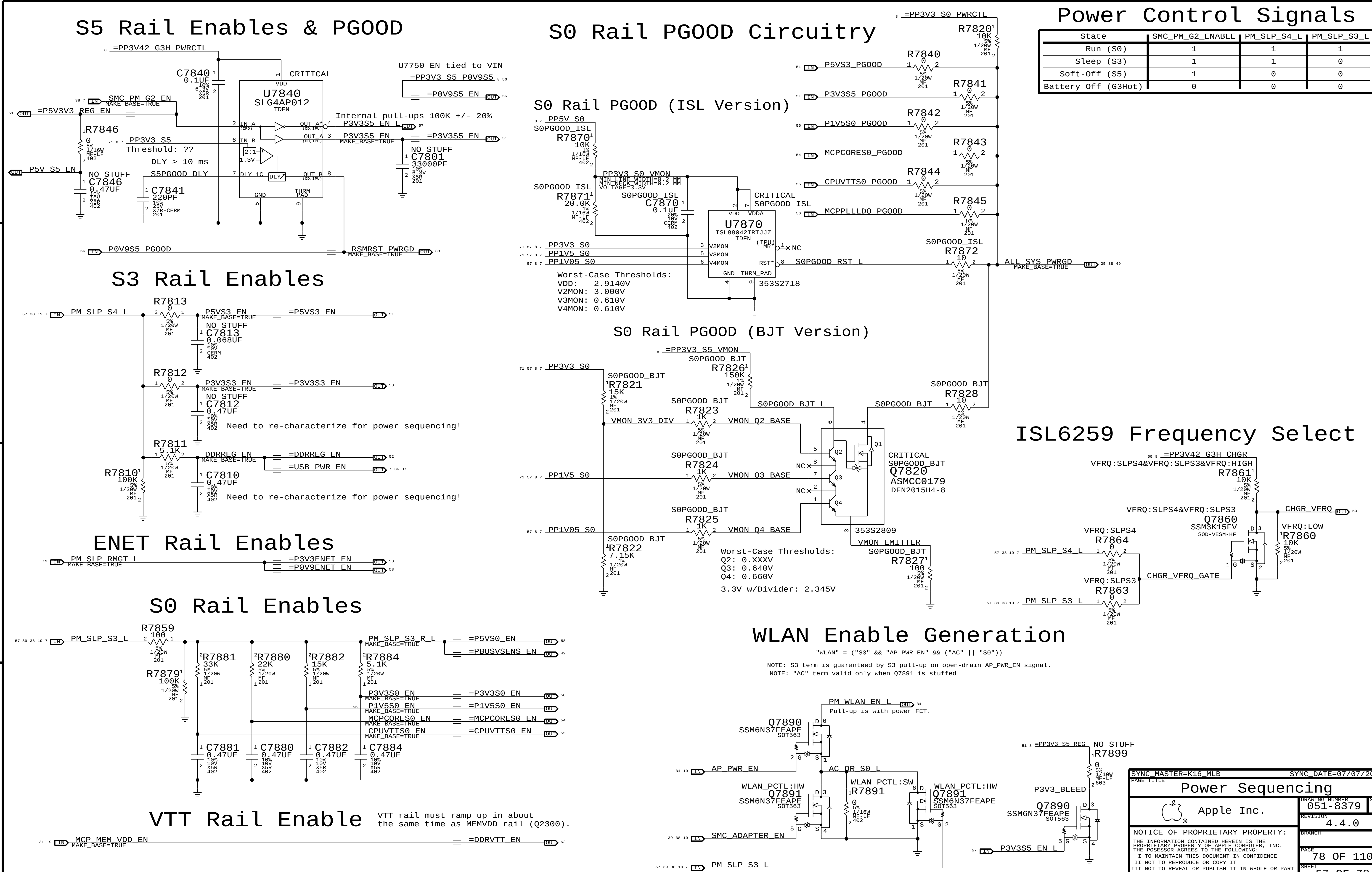

Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: Power Sequencing

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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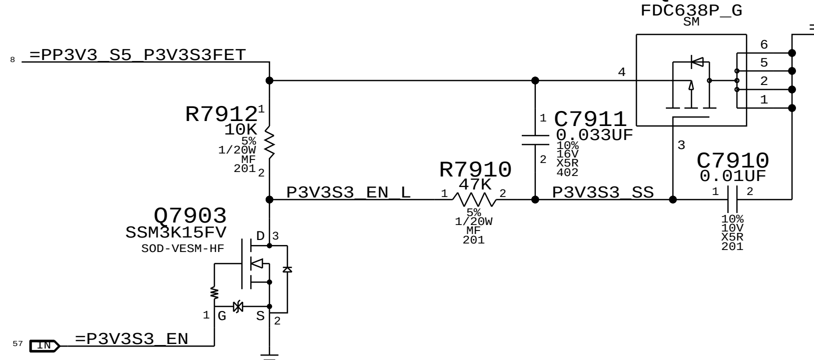
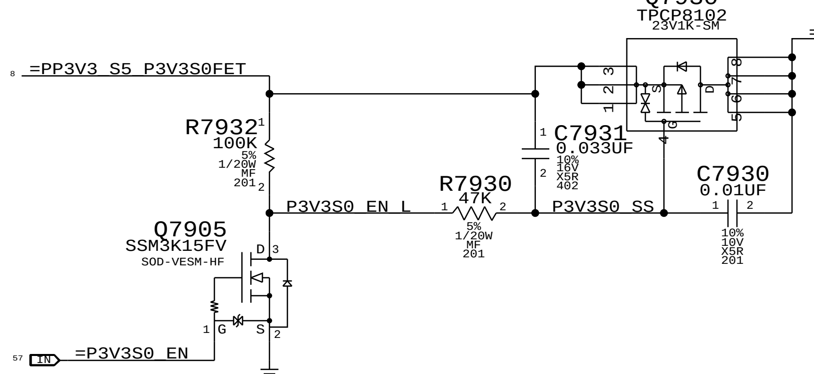
3.3V S3 FET



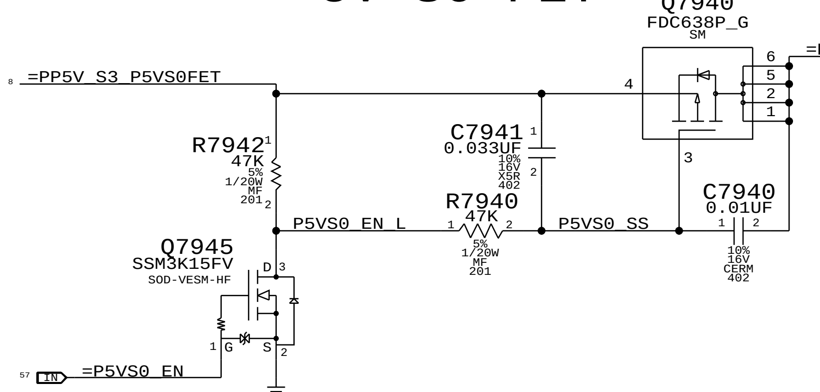
Q7910	
MOSFET	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	1.274 A (EDP)

3.3V S0 FET



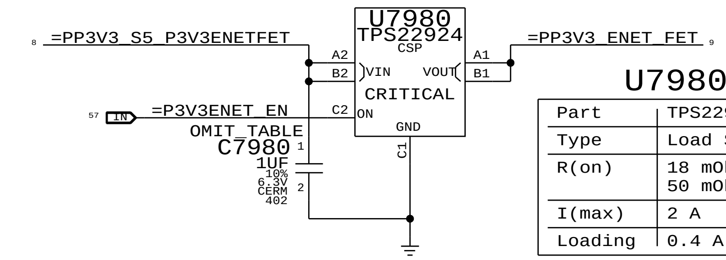
Q7930	
MOSFET	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
ID(max)	7.2 A @85C
Loading	3.294 A (EDP)

5V S0 FET



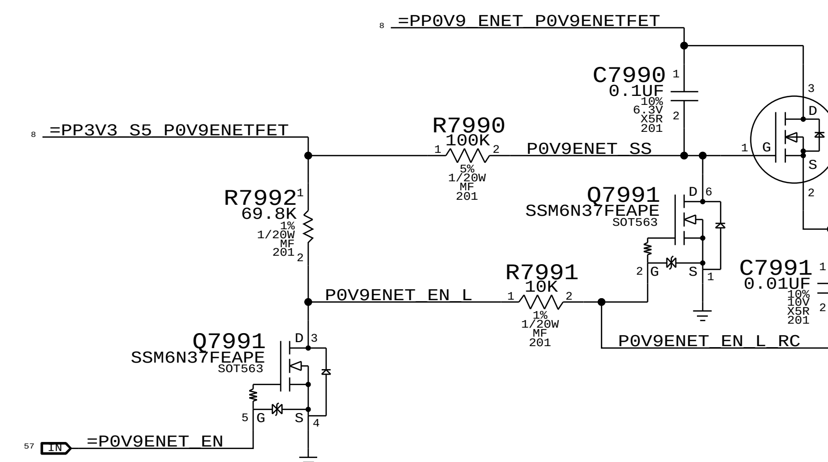
Q7940	
Part	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	0.100 A (EDP)

3.3V ENET Switch



U7980	
Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max
I(max)	2 A
Loading	0.4 A (EDP)

0.9V ENET FET



Q7990	
MOSFET	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85C
Loading	0.140 A (EDP)

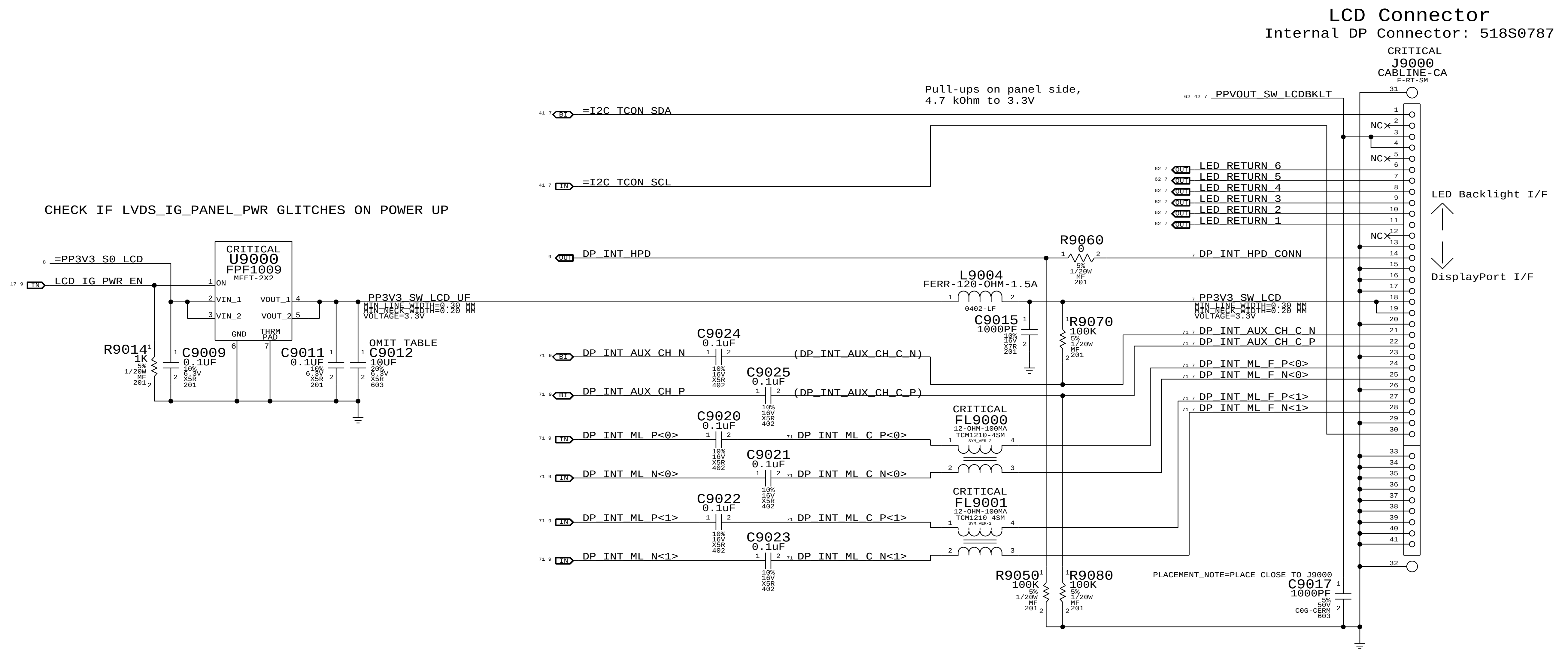
SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

Internal DisplayPort Connector

Apple Inc.

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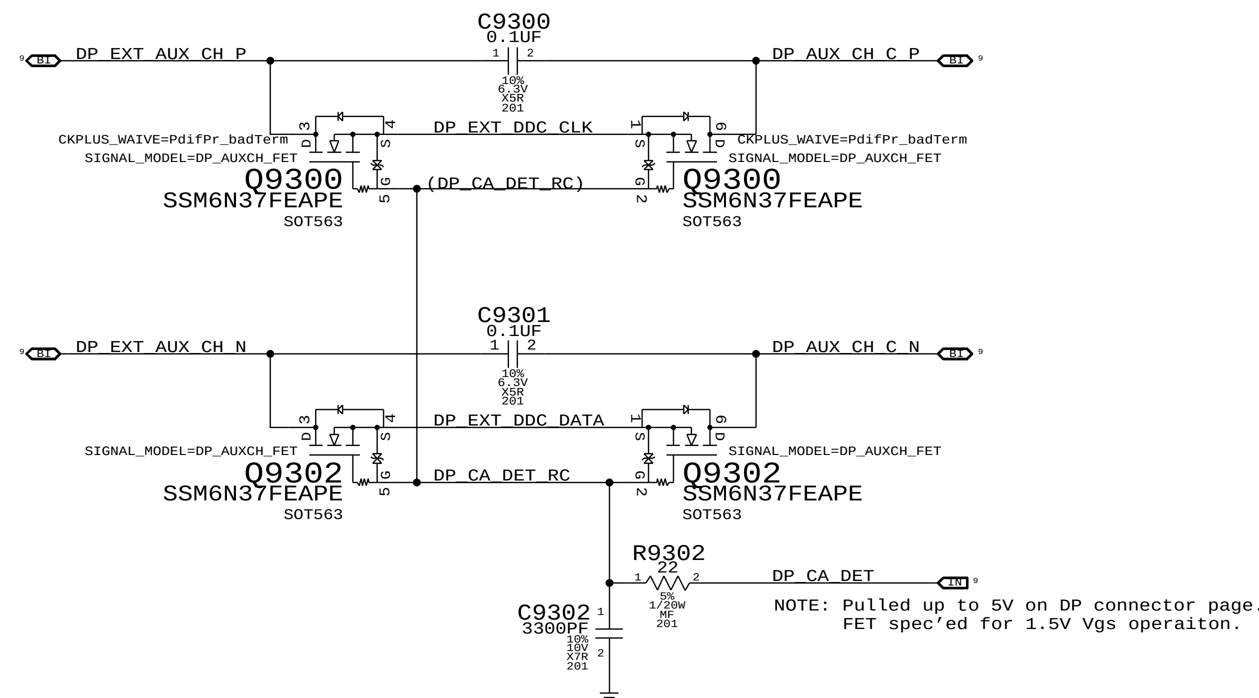


SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

External DisplayPort Support

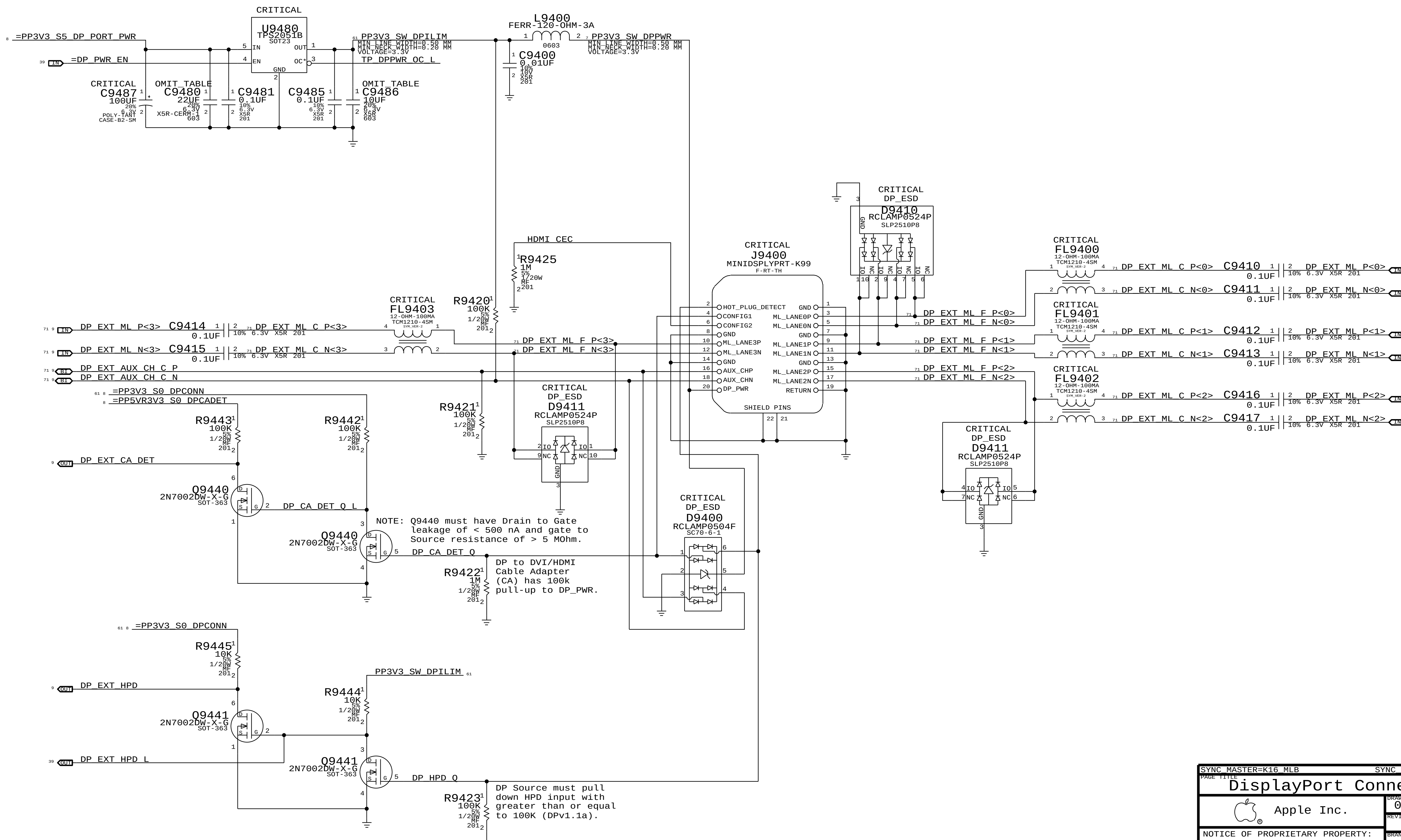
Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

BRANCH

Port Power Switch



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: DisplayPort Connector

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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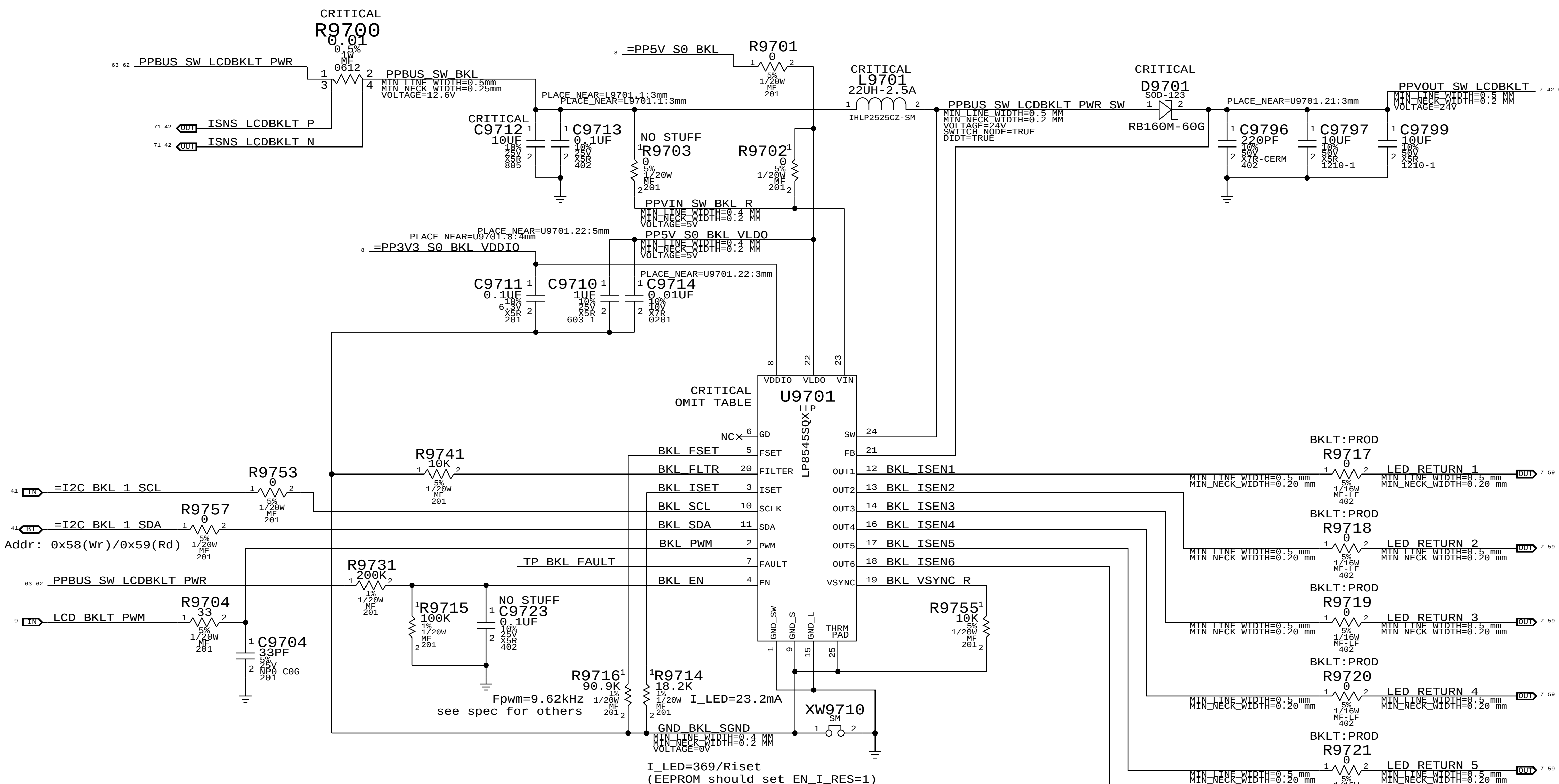
*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



FOR LP8543:
STUFF R9741
NO STUFF R9740, C9740, C9741, R9754

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
353S2896	1	IC,LP8545,LED BKLT CTRLR,PRODUCTIO,LLP24	U9701	CRITICAL	PROJ:K16
353S2967	1	IC,LP8545,LED BKLT CTRLR,LLP24,K99 VER	U9701	CRITICAL	PROJ:K99

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=K16_MLB SYNC_DATE=03/31/2010
PAGE TITLE
LCD Backlight Driver
Apple Inc.
DRAWING NUMBER 051-8379 SIZE D
REVISION 4.4.0
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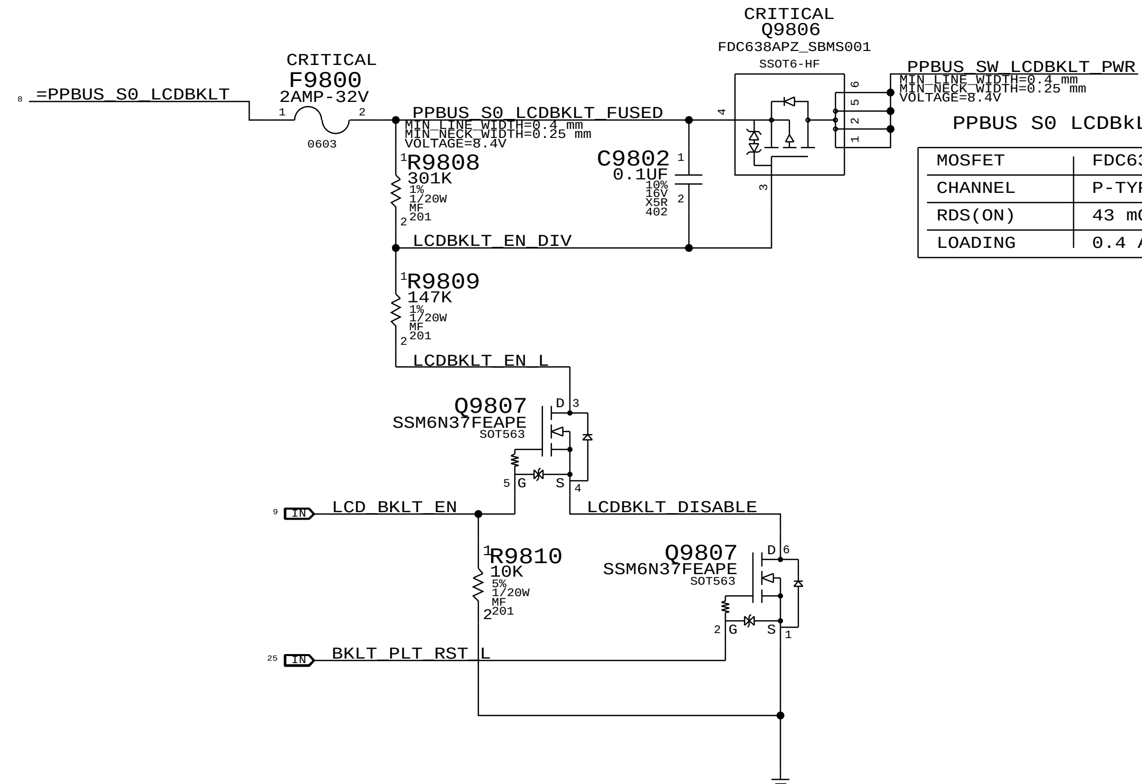

PPBUS S0 LCDBKLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

LCD Backlight Support

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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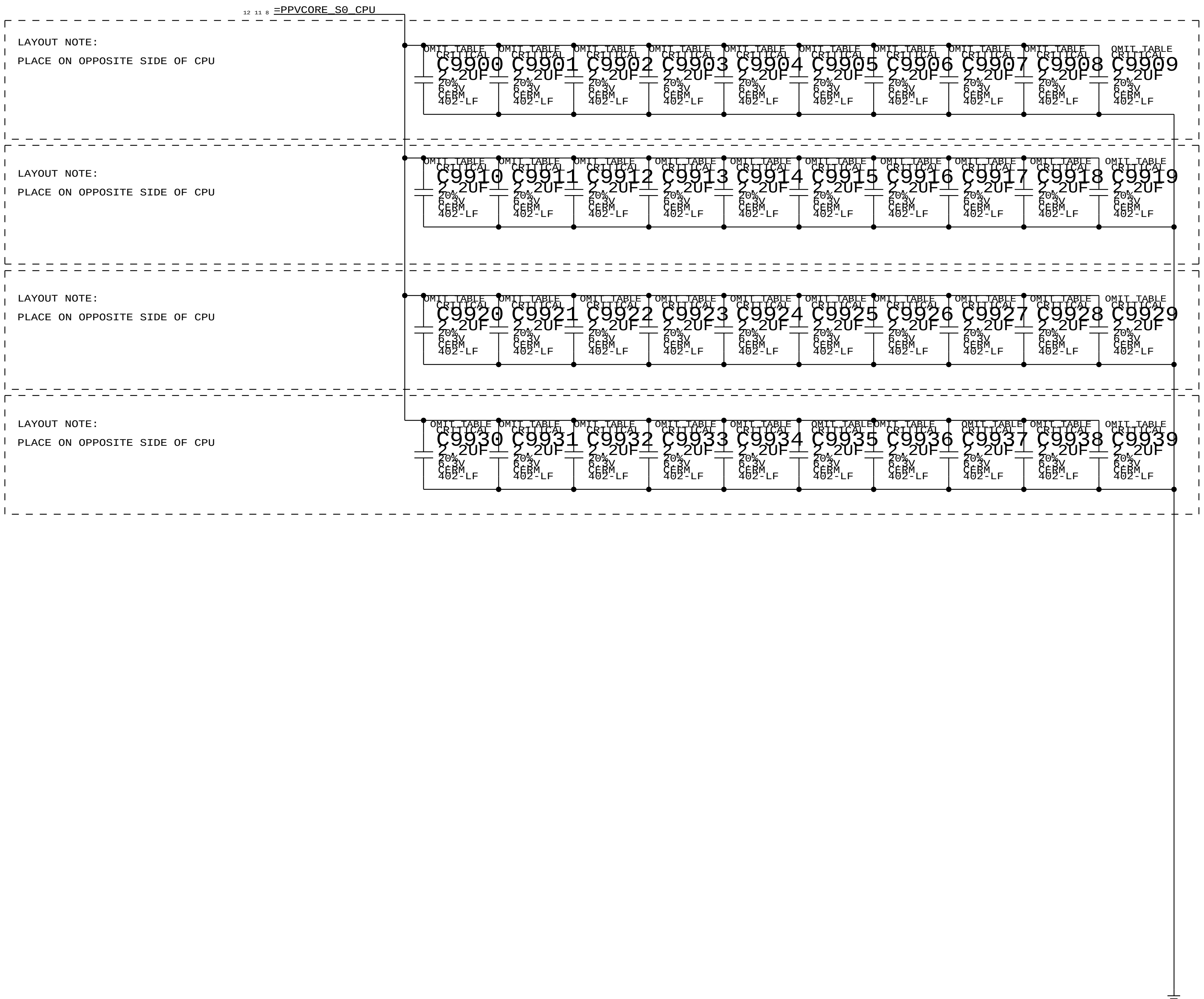
ADDITIONAL CPU VCORE HF DECOUPLING

40x 1uF 0402



FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

Group	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	Net	Pages
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
	FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_55S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_55S	FSB_1X	FSB_BREQ0_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_DBSY_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_DRDY_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_55S	FSB_1X	FSB_CPURST_L	10 13 14
	FSB_1X	FSB_55S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_55S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_55S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_55S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU_INTR	10 14
	CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU_NMI	10 14
	CPU_PROCHOT_L	CPU_55S	CPU_AGTL	CPU_PROCHOT_L	10 14 39
	CPU_PWRGD	CPU_55S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_55S	CPU_8MIL	PM_THRMTRIP_L	10 14 39
	FSB_CPUSLP_L	CPU_55S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_55S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_55S	CPU_AGTL	CPU_DPRSTP_L	10 14 53
	CPU_ASYNC	CPU_55S	CPU_AGTL	FSB_DPWR_L	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_55S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_55S	CPU_AGTL	PM_DPRSLPVR	14 53
	(See above)	CPU_55S	CPU_AGTL	IMVP_DPRSLPVR	
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 33
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
	XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
	XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
	XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
	XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
	XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	13
		CPU_55S	CPU_8MIL	CPU_VID<6..0>	11 12 53
		CPU_55S	CPU_8MIL	IMVP6_VID<6..0>	12
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 53
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 53
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	53
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	53

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: CPU/FSB Constraints

Apple Inc.

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REVISION: 4.4.0

BRANCH

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
MEM_CLK2MEM	*	=4:1_SPACING	?	NV DG says 3x inner, 4x outer
MEM_CTRL2CTRL	*	=2:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CTRL2MEM	*	=2.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2CMD	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2DATA	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DQS2MEM	*	=3:1_SPACING	?	NV DG says 4x inner, 5x outer
MEM_2OTHER	*	25 MIL	?	

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 360 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
CMD/CTRL signals should be matched within 150 ps.
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

MEM_A/B_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_P<5..0>	9 15 26 27 32
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_N<5..0>	9 15 26 27 32
MEM_A_CKE	MEM_50S	MEM_CTRL	MEM_A_CKE<3..0>	15 21 26 27 32
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_CS_L<3..0>	15 26 27 32
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_ODT<3..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_A<15..0>	9 15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_BA<2..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_RAS_L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_CAS_L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_WE_L	15 26 27 32
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DM<0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DM<1>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DM<2>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DM<3>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 26
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 26
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_P<5..0>	9 15 28 29 32
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_N<5..0>	9 15 28 29 32
MEM_B_CKE	MEM_50S	MEM_CTRL	MEM_B_CKE<3..0>	15 21 28 29 32
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_CS_L<3..0>	15 28 29 32
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_ODT<3..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_A<15..0>	9 15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_BA<2..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_RAS_L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_CAS_L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_WE_L	15 28 29 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	
	PCIE_90D	PCIE	PCIE_AP_R2D_P	7 34
	PCIE_90D	PCIE	PCIE_AP_R2D_N	7 34
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE_AP_R2D_C_P	16 34
	PCIE_90D	PCIE	PCIE_AP_R2D_C_N	16 34
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE_AP_D2R_P	7 16 34
	PCIE_90D	PCIE	PCIE_AP_D2R_N	7 16 34
	PCIE_90D	PCIE	PCIE_ENET_R2D_P	
	PCIE_90D	PCIE	PCIE_ENET_R2D_N	
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE_ENET_R2D_C_P	
	PCIE_90D	PCIE	PCIE_ENET_R2D_C_N	
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE_ENET_D2R_P	
	PCIE_90D	PCIE	PCIE_ENET_D2R_N	
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_P	
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_90D	PCIE	PCIE_FW_R2D_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_N	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9 16
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9 16
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_P	7 16 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_N	7 16 34
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX0_TERMP	16
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	
DP_INT_ML	DP_90D	DISPLAYPORT	DP_IG_ML1_P<1..0>	9 17
DP_INT_ML	DP_90D	DISPLAYPORT	DP_IG_ML1_N<1..0>	9 17
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH1_P	9 17
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH1_N	9 17
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML0_P<3..0>	9 17
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML0_N<3..0>	9 17
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH0_P	9 17
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH0_N	9 17
MCP_TMDS0_RSET	MCP_DV_COMP		MCP_TMDS0_RSET	17 24
MCP_TMDS0_VPROBE			MCP_TMDS0_VPROBE	17 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17 24
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	18 35
	SATA_90D	SATA	SATA_HDD_R2D_C_N	18 35
	SATA_90D	SATA	SATA_HDD_R2D_P	7 35
	SATA_90D	SATA	SATA_HDD_R2D_N	7 35
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	18 35
	SATA_90D	SATA	SATA_HDD_D2R_N	18 35
	SATA_90D	SATA	SATA_HDD_D2R_C_P	7 35
	SATA_90D	SATA	SATA_HDD_D2R_C_N	7 35
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	9 18
	SATA_90D	SATA	SATA_ODD_R2D_C_N	9 18
	SATA_90D	SATA	SATA_ODD_R2D_P	9
	SATA_90D	SATA	SATA_ODD_R2D_N	9
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	9 18
	SATA_90D	SATA	SATA_ODD_D2R_N	9 18
	SATA_90D	SATA	SATA_ODD_D2R_C_P	
	SATA_90D	SATA	SATA_ODD_D2R_C_N	
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	18

8 7 6 5 4 3 2 1

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	7 19 38 40
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	7 19 38 40
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	25 38
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	7 25 40
USB_EXTA	USB_90D	USB	USB_EXTA_P	18 36
	USB_90D	USB	USB_EXTA_N	18 36
	USB_90D	USB	USB_EXTA_MUXED_P	36 71
	USB_90D	USB	USB_EXTA_MUXED_N	36 71
USB_MINI	USB_90D	USB	USB_MINI_P	9 18
	USB_90D	USB	USB_MINI_N	9 18
USB_EXTD	USB_90D	USB	USB_EXTD_P	7 18 37
	USB_90D	USB	USB_EXTD_N	7 18 37
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 18 37
	USB_90D	USB	USB_CAMERA_N	7 18 37
USB_BT	USB_90D	USB	USB_BT_P	7 18 34
	USB_90D	USB	USB_BT_N	7 18 34
USB_TPAD	USB_90D	USB	USB_TPAD_P	18 46 71
	USB_90D	USB	USB_TPAD_N	18 46 71
USB_IR	USB_90D	USB	USB_IR_P	
	USB_90D	USB	USB_IR_N	
USB_EXTB	USB_90D	USB	USB_EXTB_P	
	USB_90D	USB	USB_EXTB_N	
USB_T57	USB_90D	USB	USB_T57_P	
	USB_90D	USB	USB_T57_N	
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 18
	USB_90D	USB	USB_EXTC_N	9 18
USB_SDCARD	USB_90D	USB	USB_SDCARD_P	9 18
	USB_90D	USB	USB_SDCARD_N	9 18
USB_WM	USB_90D	USB	USB_WM_P	
	USB_90D	USB	USB_WM_N	
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	18
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	19 41
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	19 41
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS_MCP_1_CLK	19 41
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS_MCP_1_DATA	19 41
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	7 19 37
	HDA_55S	HDA	HDA_BIT_CLK_R	19
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	7 19 37
	HDA_55S	HDA	HDA_SYNC_R	19
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	19
	HDA_55S	HDA	HDA_RST_L	7 19 37
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	7 19 37
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	7 19 37
	HDA_55S	HDA	HDA_SDOUT_R	19
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	19
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	19 25
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	25 38
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	19 40
	SPI_55S	SPI	SPI_CLK	40
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	19 40
	SPI_55S	SPI	SPI_MOSI	40
SPI_MISO	SPI_55S	SPI	SPI_MISO	19 40
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	19 40
	SPI_55S	SPI	SPI_CS0_L	40
	SPI_55S	SPI	SPI_MLB_CLK	40 47
	SPI_55S	SPI	SPI_MLB_MOSI	40 47
	SPI_55S	SPI	SPI_MLB_MISO	40 47
	SPI_55S	SPI	SPI_MLB_CS_L	40 47
	SPI_55S	SPI	SPI_ALT_CLK	7 40
	SPI_55S	SPI	SPI_ALT_MOSI	7 40
	SPI_55S	SPI	SPI_ALT_MISO	7 40
	SPI_55S	SPI	SPI_ALT_CS_L	7 40

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PAGE TITLE
MCP Constraints 2

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

BRANCH

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

SD Card Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

RGMII Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	9 18
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	9 18
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<0>	9 18
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	9 18
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	9 18
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	
	ENET_MII_55S	ENET_MII	ENET_RESET_L	

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET
SD_DATA	SD_55S	SD_INTERFACE	SD_D<4..0>
	SD_55S	SD_INTERFACE	SDCONN_DATA<4..0>
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<4>
SD_DATA_R	SD_55S	SD_INTERFACE	SD_D<7..5>
	SD_55S	SD_INTERFACE	SDCONN_DATA<7..5>
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<7..5>
SD_CLK	SD_55S	SD_INTERFACE	SD_CLK
	SD_55S	SD_INTERFACE	SD_CLK_R
	SD_55S	SD_INTERFACE	SDCONN_CLK
SD_CMD	SD_55S	SD_INTERFACE	SD_CMD
	SD_55S	SD_INTERFACE	SDCONN_CMD
	SD_55S	SD_INTERFACE	BCM57765_CR_CMD

NOTE: SD_D<7..5> are different to support BCM5764M/BCM57765 co-layout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	41
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	41
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	41
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	41
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	41
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	41
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	7 41
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	7 41
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	41
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	41

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	50
	1TO1_DIFFPAIR		CHGR_CSI_N	50
	1TO1_DIFFPAIR		CHGR_CSI_R_P	50
	1TO1_DIFFPAIR		CHGR_CSI_R_N	50
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	50
	1TO1_DIFFPAIR		CHGR_CSO_N	50
	1TO1_DIFFPAIR		CHGR_CSO_R_P	43 50
	1TO1_DIFFPAIR		CHGR_CSO_R_N	43 50

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PAGE TITLE

SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=1:1_SPACING	?
AUDIO	*	=1:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SD CARD READER LAYOUT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S OVERRIDE	* OVERRIDE	OVERRIDE	=STANDARD OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_P	36 68
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_N	36 68
(USB_EXTA)	USB_90D	USB	USB_LT1_P	36
(USB_EXTA)	USB_90D	USB	USB_LT1_N	36
(USB_TPAD)	USB_90D	USB	USB_TPAD_P	18 46 68
(USB_TPAD)	USB_90D	USB	USB_TPAD_N	18 46 68
(USB_TPAD)	USB_90D	USB	USB_TPAD_CONN_P	7 46
(USB_TPAD)	USB_90D	USB	USB_TPAD_CONN_N	7 46
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	I2C_SMC_SMS_SDA_R	
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	I2C_SMC_SMS_SCL_R	
	SMB_55S	SMB	I2C_TCON_SCL	41
	SMB_55S	SMB	I2C_TCON_SDA	41
	SMB_55S	SMB	I2C_TCON_SCL_CONN	
	SMB_55S	SMB	I2C_TCON_SDA_CONN	

Graphics Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
	DP_90D	DISPLAYPORT	DP_INT_ML_P<1..0>	9 59
	DP_90D	DISPLAYPORT	DP_INT_ML_N<1..0>	9 59
	DP_90D	DISPLAYPORT	DP_INT_ML_C_P<1..0>	59
	DP_90D	DISPLAYPORT	DP_INT_ML_C_N<1..0>	59
	DP_90D	DISPLAYPORT	DP_INT_ML_F_P<1..0>	7 59
	DP_90D	DISPLAYPORT	DP_INT_ML_F_N<1..0>	7 59
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_C_P	7 59
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_C_N	7 59
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_P	9 59
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_N	9 59
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP_EXT_ML_P<3..0>	9 61
	DP_90D	DISPLAYPORT	DP_EXT_ML_N<3..0>	9 61
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_P<3..0>	61
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_N<3..0>	61
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_P<3..0>	61
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_N<3..0>	61
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_P	9 61
	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_N	9 61

Power Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
CPUTHMSNS_D2	THERM_1TO1_55S	THERM	DRAMTHMSNS_D2_P	44
	THERM_1TO1_55S	THERM	DRAMTHMSNS_D2_N	44
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 44
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 44
MCPTHMSNS_D2	THERM_1TO1_55S	THERM	MLBR_THMDIODE_P	44
	THERM_1TO1_55S	THERM	MLBR_THMDIODE_N	44
MCP_THMDIODE	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	19 44
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	19 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	42 52
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	42 52
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	34 42
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	34 42
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CSREG_P	43
	SENSE_1TO1_55S	SENSE	ISNS_CSREG_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	35 42
	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	35 42
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	42 62
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	42 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_P	55
	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_N	55
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	IMVP6_CS_P	53
	SENSE_1TO1_55S	SENSE	IMVP6_CS_N	53
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	IMVP6_CS_R_P	53
	SENSE_1TO1_55S	SENSE	IMVP6_CS_R_N	53
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VTTSENSE_P	55
	SENSE_1TO1_55S	SENSE	CPU_VTTSENSE_N	55
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_P	22 54
	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_N	22 54
		MEM_POWER	PP1V5R1V35_S3	7 8
		SB_POWER	PP3V3_S5	7 8 57
		SB_POWER	PP3V3_S0	7 8 57
		SB_POWER	PP1V5_S0	7 8 57
		GND	GND	

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P	7 37 48
	DIFFPAIR	AUDIO	SPKRAMP_INR_N	7 37 48
MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_P	48
	DIFFPAIR	AUDIO	MAX98300_R_N	48

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PAGE TITLE
K16/K99 Specific Constraints

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K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL3,ISL10	Y	0.250 MM	0.250 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.250 MM	0.250 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.140 MM	0.140 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.090 MM	0.090 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.076 MM	0.076 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.125 MM	0.125 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
75_OHM_DIFF	TOP,BOTTOM	Y	0.160 MM	0.160 MM		0.160 MM	0.160 MM
75_OHM_DIFF	ISL3,ISL10	Y	0.120 MM	0.120 MM		0.140 MM	0.140 MM
75_OHM_DIFF	ISL4,ISL9	Y	0.140 MM	0.140 MM		0.140 MM	0.140 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
95_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
95_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL3,ISL10	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM
100_OHM_DIFF	ISL4,ISL9	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
1.5X_DIELECTRIC	*	0.105 MM	?
5X_DIELECTRIC	*	0.350 MM	?

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PAGE TITLE

K99 RULE DEFINITIONS

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

BRANCH

1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	SS_CAP_1UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0628	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	MU_CAP_1UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0630	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	SS_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1283,C1284,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3540,C3541	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3600,C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3640,C3641	CRITICAL	SS_CAP_2_2UF
138S0632	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655,C5810	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	MU_CAP_2_2UF
138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1283,C1284,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3540,C3541	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3600,C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3640,C3641	CRITICAL	MU_CAP_2_2UF
138S0633	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655,C5810	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	TY_CAP_2_2UF
138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1283,C1284,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3540,C3541	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3600,C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3640,C3641	CRITICAL	TY_CAP_2_2UF
138S0634	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655,C5810	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C7647	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9486,C2500,C2520,C2560,C2567,C2600,C6999	CRITICAL	SS_CAP_10UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0625	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C7647	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9486,C2500,C2520,C2560,C2567,C2600,C6999	CRITICAL	MU_CAP_10UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0627	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C7647	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9486,C2500,C2520,C2560,C2567,C2600,C6999	CRITICAL	TY_CAP_10UF

22UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0635	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	SS_CAP_22UF
138S0635	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	SS_CAP_22UF
138S0635	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	SS_CAP_22UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0676	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	MU_CAP_22UF
138S0676	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	MU_CAP_22UF
138S0676	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	MU_CAP_22UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0688	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	TY_CAP_22UF
138S0688	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	TY_CAP_22UF
138S0688	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	TY_CAP_22UF

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PAGE TITLE
Acoustic Cap BOM Config Tables

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