1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-07-22

SCHEM,MLB DVT,K99

07/22/10

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32	Memory Active Termination	K16_MLB 07/07/2010
33	FSB/DDR3 Vref Margining	K16_MLB 07/07/2010
34	X21 WIRELESS CONNECTOR	K16_MLB 07/07/2010
35	SATA CONNECTOR	K16_MLB 07/07/2010
36	External USB Connectors	K16_MLB 07/07/2010
37	LIO CONNECTORS	N/A N/A
38	SMC	K16_MLB 07/07/2010
39	SMC Support	K16_MLB 07/07/2010
40	LPC+SPI Debug Connector	K16_MLB 07/07/2010
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43	Current Sensing	K16_MLB 07/07/2010
44	Thermal Sensors	K16_MLB 07/07/2010
45	Fan	K16_MLB 07/07/2010
46	WELLSPRING 1	K16_MLB 07/07/2010
47	SPI ROM	K16_MLB 07/07/2010
48	AUDI0: SPEAKER AMP	AUDIO 02/09/2010
49	DC-In & Battery Connectors	K84_MLB 11/09/2009
50	PBus Supply & Battery Charger	K6_MLB 11/09/2009
51	5V / 3.3V Power Supply	K16_MLB 07/07/2010
52	1.5V/1.35V LVDDR3 Supply	K16_MLB 07/07/2010
53	IMVP6 CPU VCore Regulator	POWER 07/13/2005
54	MCP VCore Regulator	K6_MLB 12/11/2009
55	CPUVTT (1.05V) Power Supply	K16_MLB 07/07/2010
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8379	1	SCHEM,MLB,K99	SCH	CRITICAL	
820-2796	1	PCBF,MLB,K99	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,K99

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

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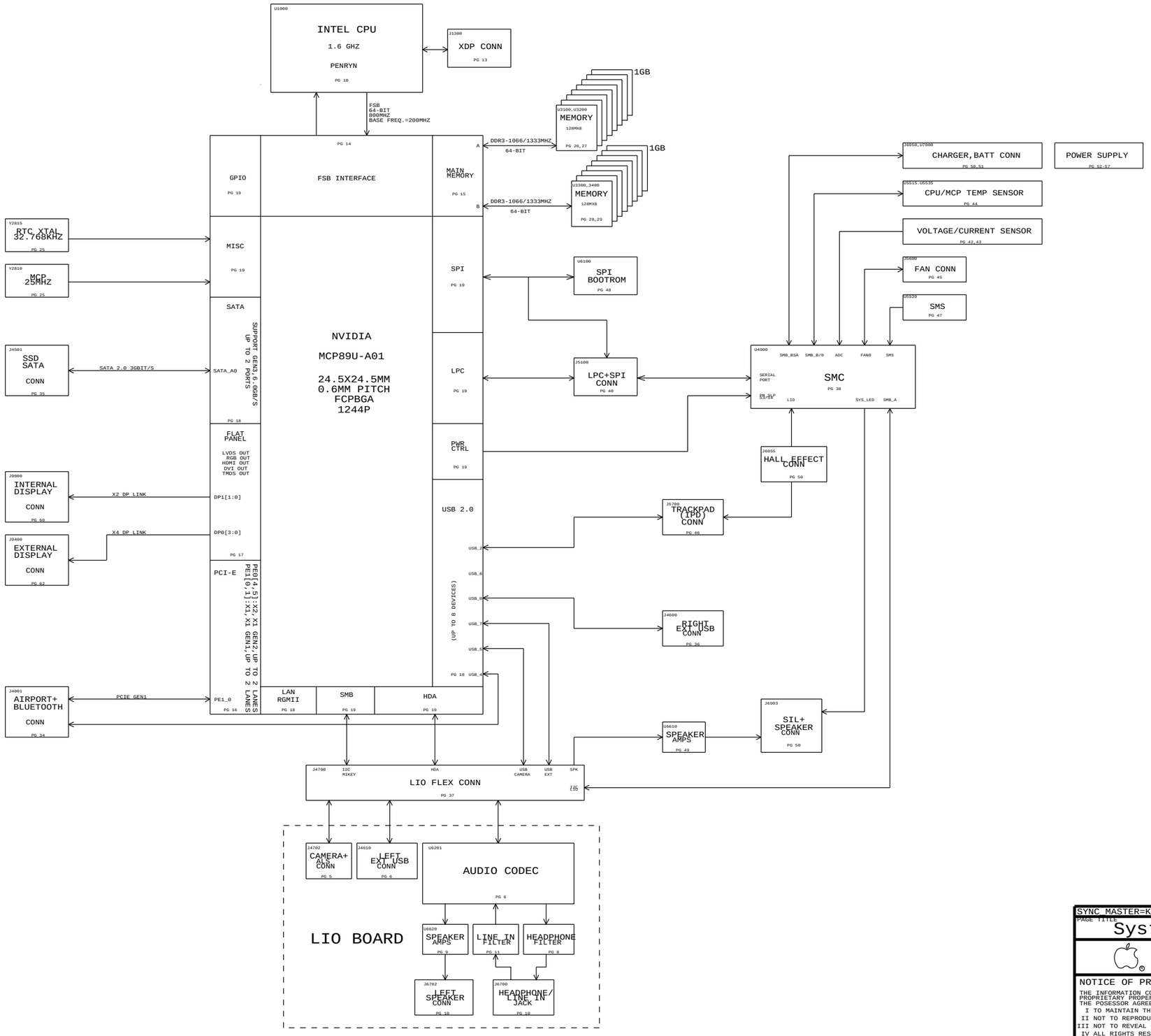

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PAGE TITLE

System Block Diagram

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K99 POWER SYSTEM ARCHITECTURE

Need to update!!!

PP18V5_DCIN_CONN
Q7080
Q7085
PPDCIN_G3H_OR_PBUS
PBUS_VSENSE
ENABLE
3.425V G3HOT
LT3470
U6990
VOUT
PP3V42_G3H_REG
SMC PWRGD
RN5VD30A-F
U5010
Q5315
8A FUSE
F7040
PPVBAT_G3H_CHGR_REG
PPBUS_G3H
PBUS_G3H_VSENSE
AC
ADAPTER
IN
DCIN(16.5V)
F6905
6A FUSE
R7020
SMC_DCIN_ISENSE
CHGR_EN
(S5)
ENABLES
VIN
VOUT
PBUS SUPPLY/
BATTERY CHARGER
ISL6259
U7000
R7050
SMC_BATT_ISENSE
CPUVTTS0_EN
(S0)
EN_PSV
CPUVTT
(1.05V)
ISL95870
U7600
PP1V05_S0
(8A MAX CURRENT)
PGOOD
CPUVTTS0_PGOOD
J6950
3S2P
(9 TO 12.6V)
PPVBAT_G3H_CONN
Q7055
PPVBAT_G3H_CHGR_R
CHGR_BGATE
CPU VCORE
ISL6261A
IMVP_VR_ON_R
VR_ON
PGOOD
U7400
SMC_CPU_VSENSE
SMC_CPU_ISENSE
PPVCORE_S0_CPU
(44A MAX CURRENT)
VR_PWRGOOD_DELAY
MCP89
PWRBTN*
PLTRST*
RSMRST*
PWRGD
CPUPWRGD(GPIO49)
CPU_RESET#
U1400
MCP_PS_PWRGD
U2850
LPC_RESET_L
CPU_PWRGD
PCH_DPWROK_L
CPU
PWRGOOD
RESET*
U1000
4.5V AUDIO
MAX8840
U6200
PP4V5_AUDIO_ANALOG
PPBUS_G3H
MCP89
PM_SLP_S4_L
PM_SLP_S3_L
U1400
P3V3S3_EN
DDRREG_EN
P5VS3_EN_L
RC DELAY
SMC
U4900
SMC_PM_G2_EN
(S5)
P5VS3_EN_L
U7840
5V
(RT)
3.3V
TPS51980
U7201
PP5V_S3_REG
(13A MAX CURRENT)
PP3V3_S5_REG
(5.5A MAX CURRENT)
P3V3S5_EN_L
PGOOD1,2
VREG3
P5V3V3_PGOOD
Q7940
PP5V_S0_FET
P5VS0_EN
Q7910
PP3V3_S3_FET
P3V3S3_EN
Q4050
P3V3_S3_WLAN
PM_WLAN_EN_L
MC34845
U9700
BKLT_EN
ENA
PPVOUT_SW_LCDBKLT
Q7890
AP_PWR_EN
PM_WLAN_EN_L
Q7890,Q7891
PM_SLP_S3_L
SMC_ADAPTER_EN
Q7930
PP0V9_S5_REG
P3V3S0_EN
ISL8009B
U7750
PP3V3_S0_FET
1.8V
TPS62202
U7760
PP1V8_S0_REG
1.5V
ISL8009B
U7710
PP1V5_S0_REG
1.05V
TPS74701
U7740
PP1V05_S0_MCP_PLL_REG
1.2V
ST1S12G12R
U7720
PP1V2_ENET_REG
SMC
RSMRST_OUT(P15)
PWRGD(P12)
IMVP_VR_ON(P16)
RSMRST_IN(P13)
PLT_RST*
PWR_BUTTON(P90)
P17(BTN_OUT)
RST*
U4900
PM_RSMRST_L
IMVP_VR_ON_R
PM_PWRBTN_L
SMC_RESET_L
ALL_SYS_PWRGD
RSMRST_PWRGD
SMC_ONOFF_L
P1V5S0_PGOOD
P5V3V3_PGOOD
MCPCORES0_PGOOD
CPUVTTS0_PGOOD
MCPPLLDO_PGOOD
S0PGOOD_RST_L
SLP_S5_L
SLP_S4_L
SLP_S3_L
Q2300
PP1V5R1V35_SW_MCP
MCPMEM_GATE
=DDRREG_EN
=DDTVTT_EN
1.5V
0.75V
TPS51116
U7300
PP1V5_S3_REG
(12A MAX CURRENT)
PP0V75_S0_REG
(1A MAX CURRENT)
MCP_CORE
ISL9563B
U7500
PPMCPCORE_S0_R
(25A MAX CURRENT)
MCPCORES0_EN
R7525
PPMCPCORE_S0_REG
PM_SLP_S3_L
P1V8S0_EN
P1V5S0_EN
CPUVTTS0_EN
DDRVTT_EN
MCPCORES0_EN
PBUSVSENSE_EN
(S0)
P5VS0_EN
(S0)
P3V3S0_EN
PP3V3_S0
PP1V5_S0
PP1V05_S0
RST*
ISL88042
U7870
V1
V2
V3

SYNC_MASTER=K6_MLB	SYNC_DATE=12/11/2009
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0651	PCBA,MLB,HY 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DX7,DDR3:HYNIX_2GB,CAPS:SS
639-1055	PCBA,MLB,HY 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD15,DDR3:HYNIX_2GB,CAPS:MU
639-1048	PCBA,MLB,HY 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0X,DDR3:HYNIX_2GB,CAPS:TY
639-1043	PCBA,MLB,HY 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0Q,DDR3:HYNIX_4GB,CAPS:SS
639-1044	PCBA,MLB,HY 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0R,DDR3:HYNIX_4GB,CAPS:MU
639-1039	PCBA,MLB,HY 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0L,DDR3:HYNIX_4GB,CAPS:TY
639-1045	PCBA,MLB,SA 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0T,DDR3:SAMSUNG_2GB,CAPS:SS
639-1054	PCBA,MLB,SA 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD14,DDR3:SAMSUNG_2GB,CAPS:MU
639-1049	PCBA,MLB,SA 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0Y,DDR3:SAMSUNG_2GB,CAPS:TY
639-1052	PCBA,MLB,SA 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD12,DDR3:SAMSUNG_4GB,CAPS:SS
639-1046	PCBA,MLB,SA 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0V,DDR3:SAMSUNG_4GB,CAPS:MU
639-1040	PCBA,MLB,SA 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0M,DDR3:SAMSUNG_4GB,CAPS:TY
639-1042	PCBA,MLB,MI 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0P,DDR3:MICRON_2GB,CAPS:SS
639-1053	PCBA,MLB,MI 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD13,DDR3:MICRON_2GB,CAPS:MU
639-1047	PCBA,MLB,MI 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0W,DDR3:MICRON_2GB,CAPS:TY
639-1051	PCBA,MLB,MI 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD11,DDR3:MICRON_4GB,CAPS:SS
639-1041	PCBA,MLB,MI 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD0N,DDR3:MICRON_4GB,CAPS:MU
639-1050	PCBA,MLB,MI 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DD10,DDR3:MICRON_4GB,CAPS:TY
639-1446	PCBA,MLB,1.6GHZ,EL 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4Q,DDR3:ELPIDA_2GB,CAPS:SS
639-1438	PCBA,MLB,1.6GHZ,EL 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4G,DDR3:ELPIDA_2GB,CAPS:MU
639-1444	PCBA,MLB,1.6GHZ,EL 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4N,DDR3:ELPIDA_2GB,CAPS:TY
639-1449	PCBA,MLB,1.6GHZ,EL 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4V,DDR3:ELPIDA_4GB,CAPS:SS
639-1448	PCBA,MLB,1.6GHZ,EL 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4T,DDR3:ELPIDA_4GB,CAPS:MU
639-1445	PCBA,MLB,1.6GHZ,EL 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.6GHZ,EEE:DG4P,DDR3:ELPIDA_4GB,CAPS:TY
607-6999	CMN PTS,PCBA,MLB,K99	K99_COMMON
085-1121	K99 MLB DEVELOPMENT BOM	K99_DEVEL:ENG
639-1355	PCBA,MLB,1.4GHZ,HY 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8L,DDR3:HYNIX_2GB,CAPS:SS
639-1341	PCBA,MLB,1.4GHZ,HY 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF83,DDR3:HYNIX_2GB,CAPS:MU
639-1353	PCBA,MLB,1.4GHZ,HY 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8J,DDR3:HYNIX_2GB,CAPS:TY
639-1350	PCBA,MLB,1.4GHZ,HY 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8F,DDR3:HYNIX_4GB,CAPS:SS
639-1356	PCBA,MLB,1.4GHZ,HY 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8M,DDR3:HYNIX_4GB,CAPS:MU
639-1348	PCBA,MLB,1.4GHZ,HY 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8C,DDR3:HYNIX_4GB,CAPS:TY
639-1349	PCBA,MLB,1.4GHZ,SA 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8D,DDR3:SAMSUNG_2GB,CAPS:SS
639-1351	PCBA,MLB,1.4GHZ,SA 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8G,DDR3:SAMSUNG_2GB,CAPS:MU
639-1357	PCBA,MLB,1.4GHZ,SA 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8N,DDR3:SAMSUNG_2GB,CAPS:TY
639-1344	PCBA,MLB,1.4GHZ,SA 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF86,DDR3:SAMSUNG_4GB,CAPS:SS
639-1352	PCBA,MLB,1.4GHZ,SA 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8H,DDR3:SAMSUNG_4GB,CAPS:MU
639-1354	PCBA,MLB,1.4GHZ,SA 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF8K,DDR3:SAMSUNG_4GB,CAPS:TY
639-1342	PCBA,MLB,1.4GHZ,MI 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF84,DDR3:MICRON_2GB,CAPS:SS
639-1346	PCBA,MLB,1.4GHZ,MI 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF88,DDR3:MICRON_2GB,CAPS:MU
639-1343	PCBA,MLB,1.4GHZ,MI 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF85,DDR3:MICRON_2GB,CAPS:TY
639-1347	PCBA,MLB,1.4GHZ,MI 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF89,DDR3:MICRON_4GB,CAPS:SS
639-1345	PCBA,MLB,1.4GHZ,MI 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF87,DDR3:MICRON_4GB,CAPS:MU
639-1340	PCBA,MLB,1.4GHZ,MI 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DF82,DDR3:MICRON_4GB,CAPS:TY
639-1442	PCBA,MLB,1.4GHZ,EL 2GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4L,DDR3:ELPIDA_2GB,CAPS:SS
639-1443	PCBA,MLB,1.4GHZ,EL 2GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4M,DDR3:ELPIDA_2GB,CAPS:MU
639-1447	PCBA,MLB,1.4GHZ,EL 2GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4R,DDR3:ELPIDA_2GB,CAPS:TY
639-1441	PCBA,MLB,1.4GHZ,EL 4GB,SS CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4K,DDR3:ELPIDA_4GB,CAPS:SS
639-1439	PCBA,MLB,1.4GHZ,EL 4GB,MU CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4H,DDR3:ELPIDA_4GB,CAPS:MU
639-1440	PCBA,MLB,1.4GHZ,EL 4GB,TY CAP,K99	K99_CMNPTS,CPU:1.4GHZ,EEE:DG4J,DDR3:ELPIDA_4GB,CAPS:TY

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7557	1	LABEL,MLB,K16/K99	[EEE_DX7]	CRITICAL	EEE:DX7
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0L]	CRITICAL	EEE:DD0L
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0M]	CRITICAL	EEE:DD0M
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0N]	CRITICAL	EEE:DD0N
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0P]	CRITICAL	EEE:DD0P
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0Q]	CRITICAL	EEE:DD0Q
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0R]	CRITICAL	EEE:DD0R
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0T]	CRITICAL	EEE:DD0T
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0V]	CRITICAL	EEE:DD0V
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0W]	CRITICAL	EEE:DD0W
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0X]	CRITICAL	EEE:DD0X
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD0Y]	CRITICAL	EEE:DD0Y
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD10]	CRITICAL	EEE:DD10
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD11]	CRITICAL	EEE:DD11
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD12]	CRITICAL	EEE:DD12
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD13]	CRITICAL	EEE:DD13
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD14]	CRITICAL	EEE:DD14
825-7557	1	LABEL,MLB,K16/K99	[EEE_DD15]	CRITICAL	EEE:DD15
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF82]	CRITICAL	EEE:DF82
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF83]	CRITICAL	EEE:DF83
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF84]	CRITICAL	EEE:DF84
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF85]	CRITICAL	EEE:DF85
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF86]	CRITICAL	EEE:DF86
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF87]	CRITICAL	EEE:DF87
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF88]	CRITICAL	EEE:DF88
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF89]	CRITICAL	EEE:DF89
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8C]	CRITICAL	EEE:DF8C
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8D]	CRITICAL	EEE:DF8D
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8F]	CRITICAL	EEE:DF8F
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8G]	CRITICAL	EEE:DF8G
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8H]	CRITICAL	EEE:DF8H
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8J]	CRITICAL	EEE:DF8J
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8K]	CRITICAL	EEE:DF8K
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8L]	CRITICAL	EEE:DF8L
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8M]	CRITICAL	EEE:DF8M
825-7557	1	LABEL,MLB,K16/K99	[EEE_DF8N]	CRITICAL	EEE:DF8N
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4G]	CRITICAL	EEE:DG4G
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4H]	CRITICAL	EEE:DG4H
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4J]	CRITICAL	EEE:DG4J
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4K]	CRITICAL	EEE:DG4K
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4M]	CRITICAL	EEE:DG4M
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4N]	CRITICAL	EEE:DG4N
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4P]	CRITICAL	EEE:DG4P
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4Q]	CRITICAL	EEE:DG4Q
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4R]	CRITICAL	EEE:DG4R
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4L]	CRITICAL	EEE:DG4L
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4T]	CRITICAL	EEE:DG4T
825-7557	1	LABEL,MLB,K16/K99	[EEE_DG4V]	CRITICAL	EEE:DG4V

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
2GB	0
4GB	1

DIE REV	CFG 3
A	0
B	1

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1121	1	K99 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-6999	1	CMN PTS,PCBA,MLB,K99	CMNPTS	CRITICAL	K99_CMNPTS

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE: K99 BOM Variants

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

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Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC:BLANK
341T0261	1	IC ASSY,SMC EXTERNAL,K99	U4900	CRITICAL	SMC:PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM:BLANK
341T0262	1	IC ASSY,EFI UNLOCKED,K99	U6100	CRITICAL	BOOTROM:UNLOCKED
341T0263	1	IC ASSY,EFI,LOCKED,K99	U6100	CRITICAL	BOOTROM:LOCKED

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0681	138S0638		ALL	TAIYO YUDEN AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
353S2987	353S2988	HVDDLDO:FIXED	ALL	TPS71725DCK AS ALTERNATE FOR U2500
104S0023	104S0018		ALL	CYNTEC/DALE AS ALTERNATES
107S0139	107S0075		ALL	CYNCTEC AS ALTERNATE
138S0671	138S0673		ALL	TAIYO AS ALTERNATE
155S0578	155S0367		ALL	TAIYO AS ALTERNATE
376S0926	376S0610		ALL	FAIRCHILD AS ALTERNATE
155S0457	155S0329		ALL	MAGLAYERS AS ALTERNATE
377S0107	377S0066		ALL	ONSEMI AS ALTERNATE

BOM Groups

BOM GROUP	BOM OPTIONS
K99_COMMON	COMMON,ALTERNATE,PROJ:K99,K99_MISC,MCP89U:A03,K99_DEBUG:ENG,K99_PROGPARTS,SPI:41MHZ,LVDDR3:YES,WLAN_PCTL:HW,IPD_5V:S5_INT,IPD_3V3:S5
K99_MISC	DP_ESD,DP_PWR:SMC,VFRQ:SLPS3,HVDDLDO:FIXED,MCPHVDD:P2V5,MCPPLL_R:REG,S0PGOOD_BJT,ISL6259_SCREENED:YES,DPI2C:SMC
K99_PROGPARTS	BOOTROM:UNLOCKED,SMC:PROG
K99_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,LPCPLUS,VREFMRGN:YES,EFI_DEBUG,S0PGOOD_ISL,MCPPLL_LDO,S3_S0_LED
K99_DEVEL:PVT	LPCPLUS
K99_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG:YES,XDP
K99_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
K99_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_2GB	DRAM_CFG0:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_2GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_4GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:MICRON_4GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB
CAPS:SS	SS_CAP_2_2UF,SS_CAP_10UF,SS_CAP_1UF,SS_CAP_22UF
CAPS:MU	MU_CAP_2_2UF,MU_CAP_10UF,MU_CAP_1UF,MU_CAP_22UF
CAPS:TY	TY_CAP_2_2UF,TY_CAP_10UF,TY_CAP_1UF,TY_CAP_22UF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3792	1	CDC,QX6H,QS,1.2,10W,800,R0.1M,BGA	U1000	CRITICAL	CPU:1.2GHZ
337S3947	1	PDC,SLGFN,PBQ,1.6,10W,R0.3M,BGA	U1000	CRITICAL	CPU:1.6GHZ
337S3954	1	PDC,SLGAK,PBQ,1.4,10W,R0.3M,BGA	U1000	CRITICAL	CPU:1.4GHZ
337S3820	1	IC,MCP89U-A01,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A01
337S3868	1	IC,MCP89U-A02,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A02
337S3939	1	IC,MCP89U-A03,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A03
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,9X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,9X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,9X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,9X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_4GB
353S2392	1	IC,ISL6259,BATCHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6259_SCREENED:NO
353S2929	1	IC,ISL6259,BATCHARGER,3%,4C4MM,QFN28	U7000	CRITICAL	ISL6259_SCREENED:YES
607-6811	1	ASSEMBLY,SUBASSY,PCBA HALL EFFECT, K99	J6955	CRITICAL	

SYNC_MASTER=K24_MLB SYNC_DATE=07/20/2009

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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Revision History NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

03/05/2010: RELEASE 0.41.0 (MAJOR)-
- PAGE 9: ADDED Z0920 (OMIT) APN 998-3068 METAL TAB SYMBOL FOR MDP CONNECTOR
- PAGE 19: ADDED 10K R1954 APN 117S0007 PD ON MLB_RAM_CFG0 AS THERE IS NO INTERNAL PD ON GPIO 48
- PAGE 72: RENAMED =P5VS3_EN_L TO =P5VS3_EN AND =P3V3S5_EN_L TO =P3V3S5_EN
- PAGE 78: MOVED P3V3S5_EN_L NET FROM PIN 4 TO PIN 3 (NON-INVERTING) AND RENAMED IT TO P3V3S5_EN AS IT IS ACTIVE HIGH SIGNAL. LEFT PIN 4 NC
- PAGE 78: NO STUFF C7801
- PAGE 78: ALIASED =P0V9S5_EN TO CONNECT TO =PP3V3_S5_P0V0S5
- PAGE 78: DELETED Q7891 (PINS 3,4,5) SYMBOL AS P5VS3_EN_L IS ACTIVE HIGH SIGNAL (SO NO NEED TO INVERT) AND RENAMED IT TO P5VS3_EN. ALSO, CONNECTED IT TO PM_SLP_S4_L VIA RC NETWORK - R7813 & C7813
- PAGE 78: REPLACED R7813 WITH 0 OHMS APN 117S0002 FOR NOW

03/05/2010: RELEASE 0.42.0 (MAJOR)-
- PAGE 4: ADDED DRAM_CFG0:L TO RAM TABLES NOT CALLING OUT DRAM_CFG0:H, AND REMOVED DRAM_CFG1:H AS IT IS NO LONGER NEEDED
- PAGE 4: DELETED MODULE TABLE ENTRY FOR ZS0907 AS POR SYMBOL IS READY
- PAGE 4: ADDED MODULE TABLE ENTRY FOR Z0920 MLB STIFFENER: 806-1176
- PAGE 9: REPLACED ZS0907 WITH POR APN 870-1938 AND DELETED OMIT ATTRIBUTE
- PAGE 9: REPLACED POGO PIN ZS0906 WITH APN 870-1938 PER PD
- PAGE 19: REMOVED R1955 PULL-UP ON MLB_RAM_CFG1 (INTERNAL PULL-UP)
- PAGE 19: CHANGED R1956 PULL-DOWN TO 470 OHMS (STRONGER PD VS 8.5K PU) APN 117S0103
- PAGE 19: REPLACED R1957 WITH 10K APN 117S0007 TO BE CONSISTENT
- PAGE 78: ADDED BYPASS PROPERTIES TO C7895 AND C7896
- PAGE 78: CHANGED BASE NET FOR PM_SLP_S4_DLY_L PER WILL

03/05/2010: RELEASE 0.43.0 (MAJOR)-
- PAGE 2: REPLACED THIS PAGE WITH QUANTA'S UPDATED ONE
- PAGE 4: SWITCHED BOM TABLE TO USE SCREENED ISL6259 PART
- PAGE 4: ADDED APN 376S0895 UNDER MODULE PART TABLE FOR Q7220 & Q7225 PER DAYU FOR PART SUPPLY ISSUE
- PAGE 4: MOVED SMS_YES BOM OPTION FROM K99_MISC TO DEVEL_BOM
- PAGE 4: UPDATED MICRON 2GB APN 333S0557 IN THE BOM TABLE
- PAGE 9: FIXED MCPCOREISNS SIGNALS ALIASES PER WILL'S CHANGES ON K16
- PAGE 39: REMOVED CRITICAL ATTRIBUTE FROM THE BOM TABLE AS IT IS NOT NEEDED
- PAGE 70: NO STUFF Q7080, D7005,Q7055 AND F7040 FOR NON-FUNCTIONAL BOARD
- PAGE 72: ADDED OMIT BOM OPTION TO Q7220 & Q7225 AS SYMBOL IS NOT READY
- PAGE 72: CHANGED R7246 AND R7247 TO 1.69K, 1% APN 118S0134 PER VENDOR
- PAGE 72: CHANGED R7216 AND R7256 TO 4.02K, 1% APN 118S0354 PER VENDOR
- PAGE 72: CHANGED C7237 AND C7239 TO 1000PF, 10% APN 132S0122 PER VENDOR
- PAGE 76: CHANGED OCP TEXT NOTE PAR VENDOR
- PAGE 76: CHANGED R7641 AND R7642 TO 1.78K, 1% APN 118S0144 PER VENDOR
- PAGE 78: ADDED NC SYMBOL TO PIN 5 OF U7896

03/07/2010: PROTO1 NON-FUNCTIONAL AGILE RELEASE 1.0.0 (FAB)-
- NON-FUNCTIONAL PROTO 1 OK2FAB RELEASE!!!

3/19/2010: RELEASE 1.1.0 (MAJOR)-
- PAGE 4: REMOVED SMS_YES BOM OPTION FROM K99_DEVEL:ENG BOM GROUP. INSTEAD, ADDED SMS:NO TO K99_MISC [ALSO SEE BELOW CHANGES FOR PAGES 50,59]
- PAGE 50: ADDED BOM OPTION ATTRIBUTE SMS:NO TO R5093 PU ON SMS_INT_L. IDEA IS TO PULL THIS NET TO S5 RAIL WHEN SMS IN NOT STUFFED, ELSE PU TO S3 RAIL (PAGE 59) PER RADAR 7765442
- PAGE 52: CONNECTED SMC 0 SMBUS INTERFACE TO THE TCON-A CHIP IN THE INTERNAL DISPLAY. ALSO, PROVIDED 0 OHMS STUFFING OPTIONS TO BE DRIVEN FROM MCP89 0 SMBUS [R5240-R5243 APN 117S0002] PER RADAR 7749046
- PAGE 59: REPLACED BOM OPTION SMS_YES WITH SMS:YES
- PAGE 59: ADDED 10K R5924 PU ON SMS_INT_L TO =PP3V3_S3_SMS WITH BOM OPTION ATTRIBUTE SMS:YES PER RADAR 7765442
- PAGE 70: STUFF BACK Q7080, D7005,Q7055 AND F7040
- PAGE 75: REPLACED L7560 WITH 10X10X3MM APN 152S1236 PER RADAR 7769386
- PAGE 90: ROUTED NEWLY ADDED =I2C_TCON_SDA/SCL TO PINS 1 & 30 OF J9000 RESPECTIVELY PER RADAR 7749046
- PAGE 93: ADDED 3300PF APN 132S0241 C9302 CAP ON DP_CA_DET TO GND PER RADAR 7742010
- PAGE 108: ADDED SMBUS_SMC_0_S0_SCL/SDA_R CONSTRAINTS SET

03/24/2010: Release 1.2.0 (MAJOR)-
- Text sizes have been fixed - safe to sync
- Page 8: Renamed PP3V3_S5_LCD to PP3V3_S0_LCD
- Page 8: Moved PP3V3_S0_LCD & PP3V3_S5_DP_PORT_PWR to S5 rail
- Page 7: Added =I2C_TCON_SCL/SDA FCTs under INT_DP_FUNC_TEST group
- Page 12: After syncing from K16, deleted C1273 as it NA to K99
- Page 90: After syncing, renamed PP3V3_S5_LCD to PP3V3_S0_LCD

Sync'ed ALL but pages 1-9,28,47,69,70,74,75 and 97 from K16
*Please NOTE that some of the below changes were already part of 1.1 release. Below list depicts all the changes since 3/1 K16 release *

- Page 12: Fixed invisible pins on CPU bypass caps. Also changed all OMITs to OMIT_TABLEs and performed other cleanup
- Page 14: Swapped BCLK_IN_N/P after library symbol refresh
- Page 17: Added CKPLUS_WAIVE properties to VDD_IFPx pins that are legally grounded on K16
- Page 19: Removed PM_SLP_S5_L alias. Other cleanup to make all CRefs visible
- Page 19: Removed pull-up on MLB_RAM_CFG1 (internal pull-up), changed pull-down to 470 ohms. Added pull-down on MLB_RAM_CFG0, made both pull-up and pull-down 10K
- Page 25: Added MCPHVDD LDO, SC-70 version. Added 1uF 0201 input cap and 10K pull-up resistor. BOMOPTIONed same as LDO. L2590 retained with MCPHVDD:P3V3 BOMOPTION
- Page 25: Added voltage divider for HVDD LDO. OMIT_TABLE'd U2590, added tables for fixed (2.5V Intersil) and adjustable (TI) regulators
- Page 39: Removed CRITICAL flag from 0-ohm resistor table
- Page 49: PB3 changed from SMC_DRAM_S3_PWRDN to SMC_SLPS5_L. P74 changed from PM_SLP_S4_L to SMC_DP_HPD_L. P75 changed from PM_SLP_S5_L to PM_SLP_S4_L
- Page 49: C4902 changed from 0805 to 0603 to free up some layout space for MCP VCore regulator
- Page 50: Added SMS:NO BOMOPTION to SMS_INT_L pull-up. Other cleanup including deleting unused alias for SMC_PB3
- Page 50: Added 2 resistors to control DP_PWR and one to connect DP_EXT_HPD_L to SMC. Updated netname on R5090 and added BOMOPTION of DP_PWR:S0
- Page 52: Added TCON I2C block and R's to connect to SMC 0 and MCP 0
- Page 53: Removed PP prefix from non-power nets. Added OMIT_TABLE to buses. Other cosmetic cleanup including grid compliance C5310 for vendor control
- Page 59: Sync'ed with K99 (adds R5924, S3 pull-up on SMS_INT_L), plus lots of cleanup including removing PP prefix from signal net, correcting BYPASS & PLACE_NEAR properties, correcting offpages, etc
- Page 72: Changed Q7220 & Q7225 to 376S0895 per Dayu's request. Fixed netnames on switcher enables, removing _L suffixes since they are active-high
- Page 72: Value changes to C7237/C7239/R7216/R7246/R7247/R7256 per Dayu. Changed C7288 to match C7218. Removed alias that was serving no purpose and was incorrect since it lacked a MAKE_BASE anyhow
- Page 76: Value changes to R7641/R7642 and OCP note correction per Dayu
- Page 78: Removed RAM power-down circuit, reconnecting =DDRREG_EN to original net
- Page 78: Disconnected half of Q7891 from 5V S3 power sequencing, gate left indicated as unused. Removed inverter from P5VS3_EN and reconnected P3V3S5_EN to be non-inverted. R7813 changed from pull-up to series R (0-ohms). P0V9S5_EN changed to alias to 3.3V S5 rail. Cleaned up page including fixing grid issues. Added BYPASS properties to C7895 and C7896. Changed base net for PM_SLP_S4_DLY_L
- Page 93: Added RC between DP_CA_DET and DDC bypass FETs. Also cleaned up page, adding offpages, fixed grid issues, made power nets convention-compliant and added note about DP_CA_DET pull-up / FET Vgs reqirements
- Page 93: Added RC between DP_CA_DET and DDC bypass FETs. Also cleaned up page, adding offpages, fixed grid issues, made power nets convention-compliant and added note about DP_CA_DET pull-up / FET Vgs reqirements
- Page 93: Added CKPLUS_WAIVE properties to _P nets connecting to FET DRAIN pins
- Page 94: Renamed DP_PWR nets to indicate 'SW' state instead of 'S0'. Switch input changed from PM_SLP_S3_L to =DP_PWR_EN. HPD_L netname changed, offpage added and pull-up changed to DP_PWR. Other cleanup including removing PLACE_NEARs that should be handled via constraints, OMIT_TABLEs for caps, CRITICAL flags on common-mode chokes and cosmetic changes
- Page 108: Added net constraints for diffpairs reported by diffpNoPhysNet report (except for 4 false errors). Other cleanup including removing some unnecessary net properties

03/25/2010: Release 1.3.0 (MAJOR)-
- Page 4: Fixed DRAM_CFG table - swapped CFG 1 and 0 columns
- Page 4: Updated EEE numbers
- Page 4: Pulled new 607-XXXX APN and added K99_CMNPTS BOM option corresponding to this new sub-BOM consisting of common parts between 18 BOMs
- Page 4: Replaced K99_COMMON with K99_CMNPTS in the BOM variant table
- Page 4: Replaced K99_SS/MU/TY_CAP BOM option with better nomenclature - CAPS:SS/MU/TY
- Page 4: Removed K99_ prefix from K99_DDR3_ BOM Group
- Page 4: Deleted 376S0895 APN module parts table entry as it is already duplicated on page 72
- Page 4: Deleted module table entry for 806-1176 as actual symbol has been added
- Page 9: Replaced Z0920 with POR stiffener symbol for APN 806-1176 and deleted OMIT
- Page 46: Replaced Q4690 with single port switch APN 353S1930 (Higher DCR) to fix USB short issue
- Page 46: Changed BOM attribute OMIT to OMIT_TABLE for C4690 & C4695
- Page 54: Changed R5418 to 4.53K 0201 APN 118S0384
- Page 54: Changed R5471 to 4.53K 0402 APN 114S0281
- Page 72: Changed R7246, R7247 to 1.87K, 1% APN 118S0159 per Dayu
- Page 72: Changed R7216, R7256 to 3.16K, 1% APN 118S0289 per Dayu
- Page 72: Changed C7236, C7238 to 0.01uF, 10% APN 132S0097 per Dayu
- Page 72: Changed C7237, C7239 to 100pF, 10% APN 131S0287 per Dayu
- Page 97: Replaced U9701 with new improved E00 version APN 353S2967
- Page 97: Changed R9704 to 33 ohms APN 117S0080 per Kiran
- Page 97: Stuffed C9704 per Kiran

3/26/2010: Release 1.4.0 (MAJOR)-
- Page 4: Added 376S0895 as an alternate for 376S0749 per Dayu
- Page 4: Added 138S0681 as an alternate for 138S0638 per GSM
- Page 4: Added 138S0676 as an alternate for 138S0635 per GSM
- Page 4: Removed alternates that were NA to K99
- Page 72: Deleted OMIT_TABLE attribute from Q7220 & Q7225. Also deleted the BOM table. Plan is to use 376S0895 as alternate instead

03/30/2010: Release 1.5.0 (MAJOR)-
- Page 4: Deleted 376S0895 alternate part entry to avoid mixing of vendors between high & low side FETs, per Dayu
- Page 4: Deleted DPI2C:SMC BOM OPTION as eDP I2C Bus won't be routed on Proto 1
- Page 4: Changed BOM OPTION SPI:25MHz to 62MHz
- Page 9: Changed BOM OPTION attribute of ZS0904 to OMIT_TABLE
- Page 10-11: Changed BOM OPTION attribute of U1000 to OMIT_TABLE
- Page 14-20: Changed BOM OPTION attribute of U1400 to OMIT_TABLE
- Page 25: Changed BOM OPTION attribute of C2600 to OMIT_TABLE
- Page 31-34: Changed BOM OPTION attribute of U3100-U3430 to OMIT_TABLE
- Page 35-36: Changed BOM OPTION attribute of all caps to OMIT_TABLE
- Page 49: Changed BOM OPTION attribute of U4900 to OMIT_TABLE
- Page 52: Changed R5290 & R5291 to 2K APN 118S0174 per RADAR# 7810865
- Page 61: Changed BOM OPTION attribute of U6100 to OMIT_TABLE
- Page 69: Changed R6905 to 10 Ohms APN 101S0089 & C6990 to 2.2uF APN 138S0672 to improve noise immunity & reduce inrush stress, per Dayu
- Page 69: Changed BOM OPTION attribute of U6955 to OMIT_TABLE
- Page 69: Changed BOM OPTION attribute of C6999 to OMIT_TABLE
- Page 70: Changed BOM OPTION attribute of U7000 to OMIT_TABLE
- Page 72: Replaced Q7220 & Q7225 with APN 376S0895 (RJK03E0) per Dayu
- Page 72: Changed R7220 to 41.2K APN 118S0360 to boost 5V, per Dayu
- Page 73: Replaced Q7330 with APN 376S0749 (SIS426) per Dayu
- Page 76: Replaced Q7630 & Q7635 with APN 376S0895 (RJK03E0) per Dayu
- Page 77: Changed R7751 to 2.55K APN 118S0234 & R7752 to 20K APN 118S0175 to improve noise immunity & reduce inrush stress, per Dayu

03/31/2010 - Proto 1 Agile Release 2.0.0 (FAB)
- Proto 1 Ok2FAB Agile Release!!!

3/31/2010: Proto 1+ Release 2.1.0 (MAJOR)
- Page 4: Activated PROJ:K99 BOMOPTION to select proper APN for U9701
- Page 97: Changed BOM OPTION attribute of C9797 to OMIT_TABLE after syncing from K16

Sync'ed from K16
- Page 90: Added Q9090 isolation FET to support LCD panel power-down per radar 7761747
- Page 97: Reversed previous change, U9701 back to 353S2896, handled via a table now to support/clarify different values for K16/K99
- Page 108: Added constraints for new nets on page90, I2C_TCON_SCL/SDA_CONN per radar 7761747

3/31/2010: Proto 1+ Release 2.2.0 (MAJOR)
- Page 97: Swapped pins of R9700 to match original orientation before syncing with K16
- Page 97: Deleted OMIT_TABLE BOM option attribute from C9797 and replaced it with actual POR APN 138S0673 symbol. Also, deleted it from BOM table as it is no longer required

5/12/2010: Proto 1+ Agile Release 3.0.0 (FAB)
- Proto 1+ OK2FAB Agile Release!!!

5/17/2010: Release 3.1.0 (Major)-
<rdar://problem/7992365> K99_MLB: Change MCP HVDD_PLL rail to 2.85V
- Page 4: Added APNs 353S2987 & 353S2988 as alternates for 353S2986

<rdar://problem/7964678> K99 MLB BOM: Change MCP APN to A03 version
- Page 4: Added MCP89U:A03 BOM table. Changed K99_Common to call out A03

<rdar://problem/7861271> K99 MLB: Set SPI operating frequency to 42MHz
<rdar://problem/7851979> K16/K99: Set SPI operating frequency to 42Mhz
- Page 4: Changed SPI:62Mhz to SPI:41MHZ BOM option

<rdar://problem/7838450> K99 MLB: WoW / WoL power control architecture change
- Page 4: Added WLAN_PCTL:HW to K99_Common

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
<rdar://problem/7953783> K99 IPD power regulator new design
- Page 4: Added IPD_PWR:S5 to K99_Common
- Page 8: Aliased =PPBUS_5V_S5 to PPBUS_G3H signal

<rdar://problem/7825507> K99 MLB BOM: Change label P/N
- Page 4: Replaced label APN 826-4393 with 825-7557

<rdar://problem/7749046> K99 MLB: Connect SMBUS to internal display connector
- Page 7: Renamed PP3V3_LCDVDD_SW_F to PP3V3_SW_LCD to match page 90, making it convention compliant power net

<rdar://problem/7779132> K99 MLB: Implement deeper sleep S4 state
- Page 7: Renamed PP3V3_S0_DPPWR to PP3V3_SW_DPPWR to match page 94 changes, making it convention compliant power net

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 7: Removed SYS_LED_ANODE_R
- Page 8: Removed =PP3V3_S5_PWRCTL alias

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 8: Added =PP3V3_S5_TPAD to PP3V3_S5 net

<rdar://problem/7963570> K99 MLB: Remove SMS circuit from layout
- Page 59: Deleted csa page as SMS is no longer POR

<rdar://problem/7795028> K99 MLB: 5V/3V3 power supply BOM changes per characterization
- Page 74: Changed C7451/C7452 to same APN 131S0287 as C7237/C7239 for BOM consolidation

<rdar://problem/7993241> K99 MLB: Cleanup of CheckPlus warnings/errors
- Page 4: Deleted ZS0904 entry from the module parts table as symbol is ready
- Page 9: Renamed stiffener Z0920 to MT0900, similar to K16
- Page 9: Tagged POGOS and MT0900 as CRITICAL
- Page 9: Replaced ZS0904 with actual symbol for APN 870-1940 and deleted OMIT_TABLE
- Page 9: Cleaned-up TP/NC _P/_N errors
- Page 74: Renamed VSNS nets to VSEN to match page 100 constraints and deleted these nets from constraints table on the same page
- Page 79: Changed OMIT associated with C7980 to OMIT_TABLE
- Page 99: Changed OMIT associated with all caps to OMIT_TABLE

<rdar://problem/7935301> K99 MLB BOM: Change BOM per CE request
- Page 75: Added Critical attribute to R7560
- Page 97: Added Critical attribute to R9700

Synced ALL but pages 1-9,12,28,47,69,70,74,75 and 97 from K16
** Didn't sync pages 79 & 99 as K16 need to sync it first from K99 to fix OMIT_TABLE attribute as mentioned above**

<rdar://problem/7749046> K99 MLB: Connect SMBUS to internal display connector
- Page 52: Added notes about I2C addresses on panel, may not be 100% accurate yet

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 13: Changed XDP SMBus nets to =I2C_XDP_* for new aliases on page52
- Page 52: Added XDP to MCP_0 SMBus diagram
- Page 76: Cleaned-up page, including correcting application of two PLACE_NEAR properties and changing an OMIT to OMIT_TABLE

<rdar://problem/7779132> K99 MLB: Implement deeper sleep S4 state
- Page 50: Added PLACE_NEAR property on R5022 to ensure no stub in fallback case.

<rdar://problem/7794868> K99 MLB: Change to single USB port power switch
- Page 46: Corrected Refdes from Q4690 to U4690

<rdar://problem/7993278> K99 MLB: Schematic sync with K16 MLB
- Page 26: Sync'ed with K16, OMIT changed to OMIT_TABLE
- Page 73: Sync'ed with K16, OMITs changed to OMIT_TABLE and cosmetic clean-up

<rdar://problem/7994057> K99 MLB: Need to add Need_TP=True property to CPU
- Page 10: Added Need_TP=True attribute to pin E37 & D40

<rdar://problem/7871167> K99 MLB: Change RC on CPUVCORE PMON output
- Page 54: Changed R5471 from 4.53K to 15k for higher PMON pin sink capability
- Page 54: Changed C5470 from 0.22UF to 68nF 10%. Only one in the library

<rdar://problem/7934374> K99 MLB BOM: Replace 376S0868 with 376S0912
- Page 23: Changed Q2300 from 376S0868 to 376S0912

<rdar://problem/7838450> K99 MLB: WoW / WoL power control architecture change
- Page 78: Swapped unused gate to Q7890 and SMC_Adapter_En fet to Q7891.
- Page 78: Added BOM Options WLAN_PCTL:HW to Q7891 both halves
- Page 78: Added R7891 0 ohm 5%
- Page 78: Added Bom option WLAN_PCTL:SW to R7891

<rdar://problem/7871918> K99 MLB: Investigate larger replacement for LCD backlight fuse
- Page 98: Changed F9800 to 0603 package APN 740S0115

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
<rdar://problem/7953783> K99 IPD power regulator new design
- Page 57: L5720.2 now connects to PP5V_S5_LDO
- Page 77: Added U7760 and surrounding circuits. BOM table need to replace later
- Page 77: Added R7760 for switching capability
- Page 77: Added min line and neck width properties to PP5V_S5_LDO
- Page 78: Aliased =P5V_S5_EN to =P5V3V3_REG_EN
- Page 78: Added R7846 and C7846 0ohm 0.47F (NO STUFF) stuffing options

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 57: Added R5730 & R5731 for power switch on PP3V3_TPAD
- Page 57: Added U5750 USB Mux
- Page 57: Added R5751 (NO STUFF) to bypass U5750 MUX
- Page 78: Added =USB_TPAD_MUX_EN to DDRREG_EN

<rdar://problem/7935301> K99 MLB BOM: Change BOM per CE request
- Page 39: Added Critical attribute to U3920, U3940
- Page 54: Added Critical attribute to Q5401,U5413
- Page 77: Removed Critical from C7710, C7715
- Page 98: Added Critical attribute toF9800

5/19/2010: Release 3.2.0 (Major)-
<rdar://problem/8006037> K99 MLB: Change RC Filter Values on AMON, and BMON
- Page 54: Changed R5481 to 150K APN 118S0106 and C5487 to 0.0068uF APN 132S0009
- Page 54: Changed R5401 to 300K APN 118S0276 and C5490 to 0.0033uF APN 132S0049

<rdar://problem/7986457> K99 MLB: Change LIO Flex connector J4700 to accommodate new LIO Flex
- Page 47: Replaced J4700 with new POR connector APN 516S0862

<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V
- Page 4: Deleted APN 353S2988 entry from the alternate table
- Page 4: Replaced APN 353S2987 entry with APN 353S3047 (TI) as an alternate
- Page 25: Replaced U2590 with 2.85V LDO APN 353S3048 (MICREL)
- Page 25: Replaced APN 353S2986 with 353S3048 in the BOM table too for HVDDLDO:FIXED

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 57: Connected a new PME signal SMC_PME_S4_L to pin 2

<rdar://problem/8004981> K99 MLB: Connect eDP SMBUS interface to SMC SMBUS 0
- Page 4: Added BOM option DPI2C:SMC to stuff R5242 & R5243

<rdar://problem/7963570> K99 MLB: Remove SMS circuit from layout
- Page 4: Deleted SMS:NO BOM option as SMS has been removed
- Page 50: Deleted BOM option SMS:NO from R5093
- Page 52: Deleted Accelerometer block from the SMBUS page

<rdar://problem/8007333> K99 MLB: Stuff R7872 to enable output connection of ISL power monitor to ALL_SYS_PWRGD
- Page 78: Added BOM option S0PGOOD_ISL to R7872

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 8: Added =PP3V3_S3_DBGLEDS alias to =PP3V3_S3_FET for debug LEDS (like K16)
- Page 57: Changed PP3V3_S5_TPAD_CONN to PP3V3_TPAD_CONN
- Page 69: Renamed PP3V3_S3 going to debug LEDs to =PP3V3_S3_DBGLEDS

<rdar://problem/8007524> K99 MLB: Stuff C9799 to provide better phase margin
- Page 97: Stuff C9799

<rdar://problem/8007560> K99 MLB: Change min neck width to meet layout requirements
- Page 8: Changed min neck width of PP3V3_S3 to 0.1mm
- Page 8: Changed min neck width of PP5V3_S3 to 0.2mm
- Page 74: Deleted IMVP6_CS_P/N & IMVP6_CS_R_P/N nets from the constraints set as the bottom of the page
- Page 97: Changed min neck width of PPBUS_SW_BKL to 0.25mm

05/19/2010: Release 3.3.0 (Major)-
<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 69: Fixed netname =PP3V3_S3_DBGLEDS (= sign was missing)

05/21/2010: Release 3.4.0 (Major)-
<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 2: Updated CPU block to reflect 1.6GHz

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
- Page 4: Changed IPD_PWR:S5 to IPD_5V:S5_INT BOM option to use internal LDO of 5V/3.3V switcher for IPD 5V supply

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 4: Added IPD_3V3:S5 BOM option under K99_COMMON to select 3.3V S5 power supply
- Page 7: Renamed =PP3V3_S3_TPAD to PP3V3_TPAD_CONN and =PP5V_S3_TPAD TO PP5V_TPAD_FILT
- Page 8: Added =PP3V3_SMC_PME alias to PP3V3_S5

<rdar://problem/8009884> K99 MLB: Add new CPU APN for U1000
- Page 4: Added SU9600 CPU APN 337S3947 1.6GHz to the module part table. And, updated BOM variant table to call out this new APN

<rdar://problem/8011930> K99 MLB: Remove SIL BOM option as SIL is not POR
- Page 4: Removed SIL BOM option from the development BOM

<rdar://problem/8007560> K99 MLB: Change min neck width to meet layout requirements
- Page 8: Changed min neck width of PP3V3_S3 to 0.1mm
- Page 40: Deleted line/neck width attributes from =PP3V3_S3_WLAN as duplicates

<rdar://problem/7825507> K99 MLB BOM: Change label P/N
- Fixed typo in APN (first column)

<rdar://problem/7986457> K99 MLB: Change LIO Flex connector J4700 to accommodate new LIO Flex
- Page 47: Connected pin 38 to GND

<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V
- Page 4: Added APN 353S2988 (MICREL) as an alternate for 353S2986
- Page 4: Added APN 353S2987 (TI) as an alternate for 353S2986
- Page 4: Deleted APN 353S3047 entry from the alternate table
- Page 25: Reverted U2590 back to the 2.5 LDO APN 353S2988
- Page 25: Replaced APN 353S3048 with 353S2986 in the BOM table for U2590 as primary for HVDDLDO:FIXED

Synced ALL but pages 1-9,12,28,47,69,70,74,75 and 97 from K16 - changes below
** Didn't sync page 52 as K16 need to sync it first from K99 to remove accelerometer**
** Didn't sync page 25 as K16 need to sync it first from K99 to revert to 2.5 LDO**
** Didn't sync page 40 as K16 needs to sync it first from K99 for above change**

<rdar://problem/8007560> K99 MLB: Change min neck width to meet layout requirements
- Page 24: Changed PPVCORE_SW_MCP_GFX min neck width to 0.12mm for routing

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
- Page 77: Changed IPD_PWR:S5 to IPD_5V:S5_EXT BOM option
- Page 77: Changed IPD_PWR:S3 to IPD_5V:S3 BOM option
- Page 77: Added R7761 0 ohm bypass option to use internal LDO of 5V/3.3V switcher for IPD 5V supply. Added BOM option IPD_5V:S5_INT to R7761
- Page 77: Added place near J5700.10:1.5mm to R7761 to avoid long stub

<rdar://problem/7978044> K99 MLB: Modify IPD interface for deeper sleep
- Page 49: Changed port P92 from SMC_BS_ALRT_L to SMC_PME_S4_L
- Page 50: Changed R5076 to a PU to =PP3V3_SMC_PME. And, renamed SMC_BS_ALERT_L to SMC_PME_S4_L
- Page 57: Changed IPD_PWR:S5 to IPD_3V3:S5 BOM option
- Page 57: Changed IPD_PWR:S3 to IPD_3V3:S3 BOM option
- Page 57: Removed U5750, R5751,R5750 and C5750 USB IPD Debug Mux as it is not needed
- Page 57: Renamed pins 5 & 6 to USB_TPAD_CONN_P/N as before
- Page 57: Renamed pin 10 to PP5V_TPAD_FILT
- Page 78: Removed =USB_TPAD_MUX_EN alias to DDREG_EN as MUX has been removed

<rdar://problem/7779132> K99 MLB: Implement deeper sleep S4 state
- Page 19: Added alias for PM_SLP_S4_L to PM_SLP_S5_L
- Page 49: Changed port P94 from SMC_DP_HPD_L to PM_SLP_S4_L
- Page 49: Changed port P95 from PM_SLP_S4_L to PM_SLP_S5_L
- Page 49: Changed port PB6 from SMC_PB6 to SMC_DP_HPD_L
- Page 50: Removed R5095 PU resistor on SMC_PB6

05/26/2010: Release 3.5.0 (Major)-
Synced ALL but pages 1-9,12,28,47,69,70,74,75 and 97 from K16 - changes below
** Didn't sync page 52 as K16 need to sync it first from K99 to remove accelerometer**
** Didn't sync page 40 as K16 needs to sync it first from K99 to remove neck width from PP3V3_S3_WLAN**

<rdar://problem/8033353> K99 MLB: Change to dual USB port power switch
- Page 46: Changed USB port power switch U4690 back to dual port TPS2052B APN 353S2298

<rdar://problem/7744955> K99 Proto0 Task: Characterize Voltage/Current/Temperature Sensors
- Page 53: For IZDM, change U5360 to INA210 (APN : 353S2073)
- Page 54: For IN1C, change R5412 to 118 Ohms, APN : 114S0127

<rdar://problem/8033256> K99 MLB: Implement 3V3 S5 bleed resistor to satisfy IPD Cumulus power sequencing on shutdown
- Page 78: Added R7899 0ohm 0603 (will change later) pull-up to =PP3V3_S5_REG and connected R7899 to pin 3 of Q7890, Q7890.5 gate tied to P3V3S5_EN_L; Q7890.4 to GND and, U7840.4 output to P3V3S5_EN_L

<rdar://problem/8007560> K99 MLB: Change min neck width to meet layout requirements
- Page 108: Changed Therm, Sense, Audio line-to-line spacing to 1:1 instead of 2:1

05/28/2010: Release 3.6.0 (Major)-
<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V (not POR)
- Page 4: Removed MIC5366 from alternate BOM table as it is primary now and replaced 353S2986 with 353S2988, making TI its alternate
- Page 4: Deleted 138S0635 from alternate table as it's been replaced per GSM(see below)
<rdar://problem/8036605> K99 MLB BOM: Implement MCP VCORE characterization changes
- Page 75: Changed C7580 to 560pF APN 132S4001 per Intersil FAE

Synced ALL but pages 1-9,12,28,47,69,70,74,75 and 97 from K16 - changes below

<rdar://problem/7992365> K99 MLB: Change MCP HVDD_PLL rail to 2.85V (not POR)
- Page 25: Changed BOM table from ISL 353S2986 to MIC5366 353S2988, as Intersil is NOT POR

<rdar://problem/8027047> K99 MLB BOM: Swap 132s0247 w/132s0257, 138s0621 w/138s0653, 138s0635 w/138s0654
- Page 25,26: Swapped 138s0621 w/138s0653 as per GSM
- Page 31-34,37,49: Swapped 132s0247 w/132s0257 as per GSM
- Page 49,73: Swapped 138s0635 w/138s0654 as per GSM

<rdar://problem/7968723> K99 MLB: Implement 5V LDO for IPD
- Page 77: Fixed BOM table attribute to attach BOM option value to TBL_BOMOPTION

6/4/2010: EVT Agile Release 4.0.0 (FAB)-
*** EVT OK2FAB Agile Release ***
- No changes since last release 3.6.0
- This release matches Quanta's official BOM for EVT build
- Upcoming changes (Acoustic, Alternates) will be reflected in 4.1 major release, which will match Quanta's deviations for EVT

06/06/2010: Release 4.1.0 (MAJOR)-
<rdar://problem/8065425> K99 MLB: Add new CPU APN for U1000 - SU9400
- Page 4: Added 18 new 639-XXXX BOMS corresponding to 1.4GHz SU9400 CPU
- Page 4: Added 18 new EEEs corresponding to new BOMs
- Page 5: Added SU9400 1.4GHz APN 337S33954 to the BOM module parts table

<rdar://problem/8065431> K99 MLB: Add new Elpida 1Gb memory APN - 333S0565
- Page 4: Added DDR3:ELPIDA_2GB BOM group and set appropriate CFG bits
- Page 4: Added Elpida DRAM to the CFG table
- Page 5: Added Elpida 1Gb APN 333S0565 to the BOM module parts table with DRAM_TYPE: ELPIDA_2GB BOM option

<rdar://problem/8066033> K99 MLB BOM: Change CPU VCORE 0603 bypass caps for acoustics
- Page 4: Added SS_CAP_22uF, MU_CAP_22uF and TY_CAP_22uF BOM options for corresponding vendor BOM group
- Page 49: Added OMIT_TABLE BOM option to C4902
- Page 73: Added OMIT_TABLE BOM option to C7360 & C7361
- Page 94: Added OMIT_TABLE BOM option to C9480
- page 110: Added BOM config table for 22uF caps for three vendors - Samsung (138S0635), Murata (138S0676) and Taiyo (138S0688). Also assigned C1200-C1231, C4902, C7360, C7361 and C9480 to these groups
- Page 110: Removed C1200-C1231 from 10uF caps BOM config table

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 5: Deleted revision history and replaced it with BOM module parts, Programmable parts and Alternate parts tables as space was limited

<rdar://problem/8065428> K99 MLB: Add alternates per GSM
- Page 5: Added APN 104S0023 as an alternate for APN 104S0018 per GSM/CE
- Page 5: Added APN 107S0139 as an alternate for APN 104S0075 per GSM/CE
- Page 5: Added APN 138S0671 as an alternate for APN 138S0673 per GSM/CE
- Page 5: Added APN 155S0556 as an alternate for APN 155S0367 per GSM/CE
- Page 5: Added APN 376S0926 as an alternate for APN 376S0610 per GSM/CE
- Page 5: Added APN 155S0457 as an alternate for APN 155S0329 per GSM/CE
- Page 5: Added APN 377S0107 as an alternate for APN 377S0066 per GSM/CE

<rdar://problem/8064296> K99 MLB: Change pull-up values for SMC 0 SMBus for TCON I2C
- Page 52: Changed R5250 & R5251 with 2K APN 117S0052 to reduce rise time

07/07/2010: Release 4.2.0 (MAJOR)-
<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Moved BOM group table on page 4 to page 5 for space limitations

<rdar://problem/8065425> K99 MLB: Add new CPU APN for U1000 - SU9400
- Page 4: Updated SU9400 BOMs with correct EEEEs (Elpida's still pending)
- Page 4: Updated Label table with correct EEEEs for SU9400 configs

<rdar://problem/8151087> K99 MLB BOM: Add new Elpida 2Gb memory
- Page 4: Added 12 new BOMs corresponding to Elpida 2GB and 4GB configs
- Page 5: Added DDR3:ELPIDA_4GB BOM group
- Page 5: Added DRAM_TYPE:ELPIDA_4GB BOM option to the Module Parts table (2Gb APN is not ready yet- using 2Gb Micron APN as a placeholder)

<rdar://problem/8168390> K99 MLB BOM: Swap 155S0556-> 155S0578, fix 0402 pad with 0603
- Page 5: Changed 155S0556 to 155S0578 to address the 0603 0402 mismatch alternate parts

<rdar://problem/8151651> K99 MLB BOM: Reduce CPU VCORE 0603 bypass caps
- Page 12: Changed BOM option attribute of C1200,C1201,C1202,C1203,C1204, C1205,C1206,C1207,C1208,C1209,C1211,C1212,C1213,C1215,C1216, C1219, C1220,C1221,C1222,C1224,C1225,C1228,C1229,C1231 from OMIT_TABLE to NOSTUFF

Synced ALL but pages 1-9,12,28,47,69,70,74,75 and 97 from K16

<rdar://problem/8118512> K99 MLB BOM: Swap 155S0423 -> 155S0559, Supply Constraint (TDK)
- Page 90: Changed FL9000, FL9001 from 155S0423 to 155S0559
- Page 94: Changed FL9400-FL9403 from 155S0423 to 155S0559

<rdar://problem/8151651> K99 MLB BOM: Reduce CPU VCORE 0603 bypass caps
- Page 110: Removed caps listed above on page 12 from the BOM table as these would get NOSTUFF'ed

7/12/2010: Release 4.3.0 (MAJOR)-
<rdar://problem/8151087> K99 MLB BOM: Add new Elpida 2Gb memory
- Page 4: Updated BOM options table with correct EEEEs for Elpida configs
- Page 4: Added label table with correct EEEEs for Elpida configs
- Page 5: Updated Elpida 2Gb configs with correct APN 333S0566

<rdar://problem/8180364> K99 MLB BOM: Remove 806-1176 stiffener
- Page 9: Deleted CRITICAL attribute from MT0900 and NOSTUFF'ed it

7/22/2010: Release 4.4.0 (MAJOR)-
<rdar://problem/8175202> K99 MLB: Move MCP Temp Sensor to SMC B SMBUS
- Page 52: Move MCP_TEMP_I2C connections to SMC B Bus
- Page 52: NOSTUFF'ed R5250 & R5251
- Page 52: Changed MCP_TEMP I2C address note to reflect 0XD8/0XD9
- Page 55: Changed R5536 to 15K APN 118S0105 to set ADDR = 0XD8/0XD9. Updated schematic note too for address

<rdar://problem/8141673> K99 MLB: Change eDP connector J9000 pinout
- Page 90: Changed pine 2 to NC and connected pin 4 to PPVOUT_SW_LCDBKLT

<rdar://problem/8224515> K99 MLB: Remove Q9090 isolation FET
- Page 90: Removed Q9090 FET and directly connected TCON I2C bus J9000
- Page 90: Deleted =I2C_TCON_SCL/SDA_CONN net names and kept =I2C_TCON_SCL/SDA

<rdar://problem/8224857> K99 MLB: Replace APN 155S0559 with 155S0423 (incompatible pad sizes)
- Page 90: Changed FL9000 and FL9001 back to the original APN 155S0423
- Page 94: Changed FL9400-FL9403back to the original APN 155S0423

<rdar://problem/8224921> K99 MLB: Change R9714 (BKLT_ISET) resistor to 18.2K 1% APN 118S0155
- Page 97: Change R9714 to 18.2K 1% APN 118S0155

<rdar://problem/7993210> K99 MLB: Cosmetic updates
- Page 97: Fixed schematic note - I_LED=369/Riset

SYNC_MASTER=K24_MLB SYNC_DATE=01/19/2009

PAGE TITLE: Revision History

Apple Inc.

DRAWING NUMBER	SIZE
051-8379	D

REVISION: 4.4.0

BRANCH:

Functional Test Points

Fan Connectors

J3700	TRUE	PP5V_S0	7 8 57
J3701	TRUE	FAN_RT_PWM	45
J3702	TRUE	FAN_RT_TACH	45

(NEED TO ADD 1 GND TP)

SPEAKER FUNC_TEST

TP_SPKRAMP_R_N_OUT	TRUE	SPKRAMP_R_N_OUT	48 49
TP_SPKRAMP_R_P_OUT	TRUE	SPKRAMP_R_P_OUT	48 49

INT DP FUNC_TEST

J3900	TRUE	PP3V3_SW_LCD	7 59 (NEED 2 TP)
J3901	TRUE	PPVOUT_SW_LCDBKLT	7 42 59 62 (NEED 2 TP)
J3902	TRUE	DP_INT_ML_F_N<0>	59 71
J3903	TRUE	DP_INT_ML_F_P<0>	59 71
J3904	TRUE	DP_INT_ML_F_N<1>	59 71
J3905	TRUE	DP_INT_ML_F_P<1>	59 71
J3906	TRUE	DP_INT_AUX_CH_C_N	59 71
J3907	TRUE	DP_INT_AUX_CH_C_P	59 71
J3908	TRUE	DP_INT_HPD_CONN	59
J3909	TRUE	LED_RETURN_1	59 62
J3910	TRUE	LED_RETURN_2	59 62
J3911	TRUE	LED_RETURN_3	59 62
J3912	TRUE	LED_RETURN_4	59 62
J3913	TRUE	LED_RETURN_5	59 62
J3914	TRUE	LED_RETURN_6	59 62
J3915	TRUE	=I2C_TCON_SCL	41 59
J3916	TRUE	=I2C_TCON_SDA	41 59

(NEED TO ADD 5 GND TP)

HALL EFFECT CONN (PLACEHOLDER)

J4700	TRUE	SMC_LID_R	49
J4701	TRUE	=PP3V42_G3H_HALL	8 49

SATA HDD

J3600	TRUE	PP3V3_S0_HDD_R	7 35 (NEED 5 TP)
J3601	TRUE	SATA_HDD_R2D_P	35 67
J3602	TRUE	SATA_HDD_R2D_N	35 67
J3603	TRUE	SATA_HDD_D2R_C_P	35 67
J3604	TRUE	SATA_HDD_D2R_C_N	35 67
J3605	TRUE	SMC_HDD_OOB_TEMP	35 38
J3606	TRUE	SMC_HDD_TEMP_CTL	35 38

(NEED TO ADD 6 GND TP)

BATT POWER CONN

J3207	TRUE	SMBUS_SMC_BSA_SCL	41 70
J3208	TRUE	SMBUS_SMC_BSA_SDA	41 70
J3209	TRUE	SYS_DETECT_L	49
J3205	TRUE	PPVBAT_G3H_CONN	49 50 (NEED 4 TP)

(NEED TO ADD 4 GND TP NEAR J6950 AND 1 FOR SHIELD)

LIO CONNECTOR

J3800	TRUE	=PP3V3_S0_AUDIO	37 (NEED 2 TP)
J3801	TRUE	=PP3V42_G3H_ONEWIRE	8 37
J3802	TRUE	SMC_BC_ACOK	9 37 38 39
J3803	TRUE	SYS_ONEWIRE	37 38
J3804	TRUE	=USB_PWR_EN	36 37 57
J3805	TRUE	USB_EXTD_OC_L	18 37
J3806	TRUE	USB_CAMERA_P	18 37 68
J3807	TRUE	USB_CAMERA_N	18 37 68
J3808	TRUE	USB_EXTD_P	18 37 68
J3809	TRUE	USB_EXTD_N	18 37 68
J3810	TRUE	=PP1V8R1V5_S0_AUDIO	8 37
J3811	TRUE	=I2C_LIO_SDA	37 41
J3812	TRUE	=I2C_LIO_SCL	37 41
J3813	TRUE	AUD_GPIO_3	37 48
J3814	TRUE	AUD_I2C_INT_L	19 37
J3815	TRUE	=I2C_MIKEY_SDA	37 41
J3816	TRUE	=I2C_MIKEY_SCL	37 41
J3817	TRUE	AUD_IP_PERIPHERAL_DET	17 37
J3818	TRUE	SPKRAMP_INR_P	37 48 71
J3819	TRUE	SPKRAMP_INR_N	37 48 71
J3820	TRUE	HDA_SDIN0	19 37 68
J3821	TRUE	HDA_SDOUT	19 37 68
J3822	TRUE	HDA_BIT_CLK	19 37 68
J3823	TRUE	HDA_SYNC	19 37 68
J3824	TRUE	HDA_RST_L	19 37 68
J3825	TRUE	AUD_IPHS_SWITCH_EN	19 37

(NEED TO ADD 5 GND TP)

AIRPORT / BT

J3400	TRUE	PCIE_AP_R2D_P	34 67
J3401	TRUE	PCIE_AP_R2D_N	34 67
J3402	TRUE	PCIE_AP_D2R_P	16 34 67
J3403	TRUE	PCIE_AP_D2R_N	16 34 67
J3404	TRUE	PCIE_CLK100M_AP_P	16 34 67
J3405	TRUE	PCIE_CLK100M_AP_N	16 34 67
J3406	TRUE	USB_BT_P	18 34 68
J3407	TRUE	USB_BT_N	18 34 68
J3408	TRUE	WIFI_EVENT_L	34 38 39
J3409	TRUE	=PP3V3_S3_BT	8 34
J3410	TRUE	PP3V3_WLAN_F	7 34 39 (NEED 6 TP)
J3411	TRUE	PCIE_WAKE_L	16 34
J3412	TRUE	AP_RESET_CONN_L	34
J3413	TRUE	AP_CLKREQ_Q_L	34

(NEED TO ADD 8 GND TP)

IPD_FLEX_CONN

J3100	TRUE	SMC_TPAD_RST_L	39 46
J3101	TRUE	SMC_LID	38 39 46 49
J3102	TRUE	SMC_ONOFF_L	38 39 46
J3103	TRUE	=I2C_TPAD_SCL	41 46
J3104	TRUE	=I2C_TPAD_SDA	41 46
J3105	TRUE	=PP3V42_G3H_TPAD	8 46
J3106	TRUE	PP3V3_TPAD_CONN	46
J3107	TRUE	PP5V_TPAD_FILT	46
J3108	TRUE	USB_TPAD_CONN_N	46 71
J3109	TRUE	USB_TPAD_CONN_P	46 71

(NEED TO ADD 5 GND TP)

LCP + SPI CONN

J3500	TRUE	=PP3V3_S5_LPCPLUS	8 40
J3501	TRUE	=PP5V_S0_LPCPLUS	8 40
J3502	TRUE	LPC_AD<3..0>	19 38 40 68
J3503	TRUE	SPI_ALT_MOSI	40 68
J3504	TRUE	SPI_ALT_MISO	40 68
J3505	TRUE	LPC_FRAME_L	19 38 40 68
J3506	TRUE	PM_CLKRUN_L	19 38 40
J3507	TRUE	SMC_TMS	38 39 40
J3508	TRUE	LPCPLUS_RESET_L	25 40
J3509	TRUE	SMC_TDO	38 39 40
J3510	TRUE	SMC_TRST_L	38 40
J3511	TRUE	SMC_MD1	38 40
J3512	TRUE	SMC_TX_L	36 38 39 40
J3513	TRUE	LPC_CLK33M_LPCPLUS	25 40 68
J3514	TRUE	SPIROM_USE_MLB	19 40 47
J3515	TRUE	SPI_ALT_CLK	40 68
J3516	TRUE	SPI_ALT_CS_L	40 68
J3517	TRUE	LPC_SERIRQ	19 38 40
J3518	TRUE	LPC_PWRDWN_L	19 38 40
J3519	TRUE	SMC_TDI	38 39 40
J3520	TRUE	SMC_TCK	38 39 40
J3521	TRUE	SMC_RESET_L	38 39 40 50
J3522	TRUE	SMC_NMI	38 40
J3523	TRUE	SMC_RX_L	36 38 39 40
J3524	TRUE	LPCPLUS_GPIO	19 40

(NEED TO ADD 6 GND TP)

DC POWER CONN

J3000	TRUE	=PP18V5_DCIN_CONN	8 49 (NEED 6 TP)
J3001	TRUE	=PP5V_S3_LIO_CONN	8 49

(NEED TO ADD 6 GND TP)

DEBUG VOLTAGE

J3300	TRUE	PPVCORE_S0_CPU	8 42
J3301	TRUE	PPVCORE_S0_MCP	8 42
J3302	TRUE	PP1V05_S0	8 57
J3303	TRUE	PP1V5_S0	8 57 71
J3304	TRUE	PP3V3_S0	8 57 71
J3305	TRUE	PP5V_S0	7 8 57
J3306	TRUE	PP3V3_S3	8
J3307	TRUE	PP5V_S3	8
J3308	TRUE	PP0V9_S5	8
J3309	TRUE	PP3V3_S5	8 57 71
J3310	TRUE	PP3V42_G3H	8
J3311	TRUE	PPBUS_G3H	8 42 49
J3312	TRUE	PP3V3_WLAN_F	7 34 39
J3313	TRUE	PP3V3_S0_HDD_R	7 35
J3314	TRUE	PPDCIN_S5_S5	8
J3315	TRUE	PPVOUT_SW_LCDBKLT	7 42 59 62
J3316	TRUE	PP3V3_SW_LCD	7 59
J3317	TRUE	PP1V5R1V35_S3	8 71
J3318	TRUE	SMC_PM_G2_EN	38 57
J3319	TRUE	PM_SLP_S4_L	19 38 57
J3320	TRUE	PM_SLP_S3_L	19 38 39 57
J3321	TRUE	PP0V9_ENET	8
J3322	TRUE	PP1V05_S0_MCP_PLL_UF	8
J3323	TRUE	PP3V3_ENET	8
J3324	TRUE	PP3V3_SW_DPPWR	61
J3325	TRUE	PP5V_S3_RTUSB_A_F	36
J3326	TRUE	PPBUS_G3H_ISNS	8

(NEED TO ADD 27 GND TP)

FSB SIGNALS WITH NOTEST

J3200	NO_TEST=TRUE	FSB_A_L<35..3>	10 14 65
J3201	NO_TEST=TRUE	FSB_ADS_L	10 14 65
J3202	NO_TEST=TRUE	FSB_ADSTB_L<1..0>	10 14 65
J3203	NO_TEST=TRUE	FSB_D_L<63..0>	10 14 65
J3204	NO_TEST=TRUE	FSB_DINV_L<3..0>	10 14 65
J3205	NO_TEST=TRUE	FSB_DSTB_L_N<3..0>	10 14 65
J3206	NO_TEST=TRUE	FSB_DSTB_L_P<3..0>	10 14 65
J3207	NO_TEST=TRUE	FSB_HIT_L	10 14 65
J3208	NO_TEST=TRUE	FSB_HITM_L	10 14 65
J3209	NO_TEST=TRUE	FSB_LOCK_L	10 14 65
J3210	NO_TEST=TRUE	FSB_REQ_L<4..0>	10 14 65

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE: FUNCTIONAL TEST

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

BRANCH:

PAGE: 7 OF 110

SHEET: 7 OF 73

"S0,S0M" RAILS

=PPVCORE_S0_CPU_REG (53) — 18 A
PPVCORE_S0_CPU (7 42)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU (11 12 64)

=PPCPUVTT_S0_REG (55) — 9.40 A
PP1V05_S0 (7 57)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU (10 11 12)
=PP1V05_S0_MCP_FSB (14 20 23)
=PP1V05_S0_MCP_AVDD_UF (23)
=PP1V05_S0_MCP_SATA_DVDD (20 23)
=PP1V05_S0_MCP_PLL_UF_R (56)
=PP1V05_SW_MCP_FSB (20 23)
=PP1V05_S0_MCP_PE_DVDD (20 23)
=PP1V05_S0_MCP_M2CLK_DLL (15 23)
=PP1V05_S0_MCP_DP0_VDD (17 24)
=PP1V05_S0_XDP (13)

=PPMCPCORE_S0_REG (54) — (MCP VCORE AFTER SENSE RES) 23.8 A
PPVCORE_S0_MCP (7 42)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP (20 23)
=PPVCORE_S0_MCPGFXFET (22)

LVDDR VRef/VTT (0.75V/0.675V) Rails

=PPVTT_S0_DDR_LDO (52) — 1.20 A
PPDDRVTT_S0
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PPDDRVTT_S0_MEM_A (32)
=PPDDRVTT_S0_MEM_B (32)

=PPVTT_S3_DDR_BUF (52 33)
PPDDRVREF_S3
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

=PP1V5_S0_REG (56) — .210 A
PP1V5_S0 (7 57 71)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU (11 12)
=PP1V5_S0_MCP_PLL_VLDO (56)
=PP1V8R1V5_S0_AUDIO (7 37)
=PP3V3R1V5_S0_MCP_HDA (19 23)

=PP1V05_S0_MCP_PLL_OR (56)
PP1V05_S0_MCP_PLL_UF (7)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_MCP_PLL_UF (23)

=PP5V_S0_FET (58) — 0.100 A
PP5V_S0 (7 57)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_LPCPLUS (7 40)
=PP5V_S0_FAN (45)
=PP5V_S0_CPU_IMVP (53)
=PP5VR3V3_S0_DPCADET (61)
=PP5V_S0_CPUVTTS0 (55)
=PP5V_S0_BKL (62)
=PP5V_S0_MCPREG (54)
=PP5V_S0_MCPFSBFET (22)

=PP3V3_S0_FET (58) — 3.30 A
PP3V3_S0 (7 57 71)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_XDP (13)
=PP3V3_S0_MCP (20 23)
=PP3V3_S0_P1V5S0 (56)
=PP3V3_S0_DEBUGROM (40)
=PP3V3_S0_SMBUS_SMC_0_S0 (41)
=PP3V3_S0_SMBUS_SMC_B_S0 (41)
=PP3V3_S0_SMBUS_MCP_0 (41)
=PP3V3_S0_FAN (45)
=PP3V3_S0_AUDIO (7 37)
=PP3V3_S0_IMVP (53)
=PP3V3_S0_MCP_GPIO (17 18 19)
=PP3V3_S0_MCP_PLL_UF (23)
=PP3V3_S0_MCP_HVDD (20 23)
=PP3V3_S0_SMC (39)
=PP3V3_S0_MCPTHMSNS (44)
=PP3V3_S0_CPUTHMSNS (44)
=PP3V3_S0_PWRCTL (57)
=PP3V3_S0_SMBUS_MCP_1 (41)
=PP3V3_S0_HDD (35)
=PP3V3_S0_MCP_PLL_VLDO (56)
=PP3V3_S0_MCPCOREISNS (43)
=PP3V3_S0_MCPDDRISNS (43)
=PP3V3_S0_BKLTISNS (42)
=PP3V3_S0_CSREGISNS (43)
=PP3V3_S0_BKL_VDDIO (62)
=PP3V3_S0_DPCONN (61)
=PP3V3_S0_HDDISNS (42)

"S3" RAILS

LVDDR (1.5V/1.35V) Rails

=PPDDR_S3_REG (52) — 11.30 A
PP1V5R1V35_S3 (7 71)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE (OR 1.35V)
=PPLVDDR_S3_MEM_A (26 27 30)
=PPLVDDR_S3_MEM_B (28 29 31)
0 mA =PP1V5R1V35_S3_MCP_MEM (15)
4250 mA =PP1V5R1V35_S0_MCPDDRFET (21)
=PPVIN_S0_DDRREG_LDO (52)

=PP3V3_S3_FET (58) — 1.274 A
PP3V3_S3 (7)
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_SMBUS_SMC_A_S3 (41)
=PP3V3_S3_PDCISENS (52)
=PP3V3_S3_VREFMRGN (33)
=PP3V3_S3_MCP_GPIO (19)
=PP3V3_S3_SMS (41)
=PP3V3_S3_1V5S3ISNS (42)
=PP3V3_S3_WLANISNS (42)
=PP3V3_S3_DBGLEDS (49)
=PP3V3_S3_BT (7 34)
=PP3V3_S3_WLAN (34)
=PP3V3_S3_TPAD (46)

=PP5V_S3_REG (51) — 5.40 A
PP5V_S3 (7)
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_MCPDDRFET (21)
=PP5V_S3_SYSLED (39)
=PP5V_S3_TPAD (56)
=PP5V_S3_DDRREG (52)
=PP5V_S3_AUDIO_AMP (48)
=PP5V_S3_P5VS0FET (58)
=PP5V_S3_RTUSB (36)
=PP5V_S3_LIO_CONN (7 49)

"G3H" RAILS

=PP3V42_G3H_REG (49) — 0.064
PP3V42_G3H (7)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PPVIN_S5_SMCVREF (39)
=PP3V42_G3H_SMBUS_SMC_BSA (41)
=PP3V42_G3H_PWRCTL (57)
=PP3V42_G3H_CHGR (50 57)
=PP3V42_G3H_SMCUSBMUX (36)
=PP3V42_G3H_TPAD (7 46)
=PP3V42_G3H_HALL (7 49)
=PP3V3_S5_SMC (38 39)
=PP3V3_S5_LPCPLUS (7 40)
=PP3V42_G3H_BMON_ISNS (43)
=PP3V42_G3H_ONEWIRE (7 37)
PP3V3_G3_RTC (19 20 23)

=PP18V5_DCIN_CONN (49 7)
PPDCIN_S5_S5 (7)
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPDCIN_S5_CHGR (50)

=PPBUS_G3H (50)
PPBUS_G3H (7 42 49)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPBUS_S0_LCDBKLT (63)
=PPVIN_S5_P5VP3V3 (51)
=PPBUS_G3H_R_IN (43)
=PPBUS_5V_S5 (56)

=PPBUS_G3H_R_OUT (43)
PPBUS_G3H_ISNS (7)
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=8.4V
MAKE_BASE=TRUE
=PPVIN_S0_CPUVTTS0 (55)
=PPVIN_S5_CPU_IMVP (53)
=PPVIN_S0_MCPCORE (54)
=PPVIN_S3_DDRREG (52)

"ENET" RAILS

=PP3V3_ENET_FET_R (9) — 400mA
PP3V3_ENET (7)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
300mA =PP3V3_ENET_MCP_RMGT (18 20 23)
~100mA =PP3V3_ENET_MCP_PLL_MAC (23)

=PP0V9_ENET_FET (58)
PP0V9_ENET (7)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V9_ENET_MCP_RMGT (20 23)

"S5" RAILS

=PP3V3_S5_REG (57 51) — 1.07 A + S3 + S0
PP3V3_S5 (7 57 71)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_GPIO (18 19)
=PP3V3_S5_ROM (47)
=PP3V3_S5_MCP (20 23)
=PP3V3_S5_MCPPWRGD (25)
=PP3V3_S5_P3V3S3FET (58)
=PP3V3_S5_P3V3S0FET (58)
=PP3V3_S5_P3V3ENETFET (58)
=PP3V3_S5_P0V9S5 (56 57)
=PP3V3_S5_VMON (57)
=PP3V3_S5_SMBUS_SMC_MGMT (41)
=PP3V3_S5_P0V9ENETFET (58)
=PP3V3_S5_TPAD (46)
=PP3V3_S5_DP_PORT_PWR (61)
=PP3V3_S0_LCD (59)
=PP3V3_SMC_PME (39)

=PP0V9_S5_REG (56) — 0.290 A
PP0V9_S5 (7)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
105 mA/241 mA =PP0V9_S5_MCP_VDD_AUXC (20 23)
=PP0V9_ENET_P0V9ENETFET (58)

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE: Power Aliases

Apple Inc.

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HEAT SINK MOUNTING BOSSES

Z0906 STDOFF-4.5OD1.8H-SM
Z0907 STDOFF-4.5OD1.8H-SM
Z0908 STDOFF-4.5OD1.8H-SM
Z0909 STDOFF-4.5OD1.8H-SM
Z0910 STDOFF-4.5OD1.8H-SM
Z0911 STDOFF-4.5OD1.8H-SM
Z0912 STDOFF-4.5OD1.8H-SM
Z0913 STDOFF-4.5OD1.8H-SM

FAN BOSS

Z0905 STDOFF-4.5OD1.8H-SM

SSD BOSS

Z0915 STDOFF-4.5OD1.9H-SM

X16 BOSS

Z0914 STDOFF-4.5OD1.9H-SM

MDP CONN METAL TAB

NOSTUFF
MT0900 STIFFENER-K16-K99
SM-SP

EMI IO POGO PINS

CRITICAL ZS0904 POGO-2.0OD-2.95H-K86-K87 SM
CRITICAL ZS0905 1.4DIA-SHORT-SILVER-K99 SM
CRITICAL ZS0906 POGO-2.0OD-3.6H-K86-K87 SM
CRITICAL ZS0907 POGO-2.0OD-3.6H-K86-K87 SM

PCI-E ALIASES

UNUSED GPU LANES

16	=PEG_D2R_N<5:4>	NC_PEG_D2RN<5:4>	NO_TEST=TRUE, MAKE_BASE=TRUE
16	=PEG_D2R_P<5:4>	NC_PEG_D2RP<5:4>	NO_TEST=TRUE, MAKE_BASE=TRUE
16	=PEG_R2D_C_N<5:4>	NC_PEG_R2DCN<5:4>	NO_TEST=TRUE, MAKE_BASE=TRUE
16	=PEG_R2D_C_P<5:4>	NC_PEG_R2DCP<5:4>	NO_TEST=TRUE, MAKE_BASE=TRUE
67 16	PEG_CLK100M_P	NC_PEG_CLK100MP	NO_TEST=TRUE, MAKE_BASE=TRUE
67 16	PEG_CLK100M_N	NC_PEG_CLK100MN	NO_TEST=TRUE, MAKE_BASE=TRUE
16	PEG_CLKREQ_L	NC_PEG_CLKREQ_L	NO_TEST=TRUE, MAKE_BASE=TRUE
16	ENET_CLKREQ_L	NC_ENET_CLKREQ_L	NO_TEST=TRUE, MAKE_BASE=TRUE

USB ALIASES

UNUSED USB PORTS

68 18	USB_SDCARD_P	NC_USB_SDCARDP	NO_TEST=TRUE, MAKE_BASE=TRUE
68 18	USB_SDCARD_N	NC_USB_SDCARDN	NO_TEST=TRUE, MAKE_BASE=TRUE
68 19	USB_MINI_P	NC_USB_MINIP	NO_TEST=TRUE, MAKE_BASE=TRUE
68 19	USB_MINI_N	NC_USB_MININ	NO_TEST=TRUE, MAKE_BASE=TRUE
68 19	USB_EXTC_P	NC_USB_EXTCP	NO_TEST=TRUE, MAKE_BASE=TRUE
68 19	USB_EXTC_N	NC_USB_EXTCN	NO_TEST=TRUE, MAKE_BASE=TRUE

ETHERNET ALIASES

PLACE_NEAR=U7980.A1:5MM
R0911 0 5% 1/16W MF-LF 402 1 2
PP3V3_ENET_FET — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
=PP3V3_ENET_FET 58
=PP3V3_ENET_FET_R OUT 8

ENET_RXD_PD (MAKE_BASE=TRUE)	ENET_RXD<0>	OUT 18 69
	ENET_RXD<1>	OUT 18 69
	ENET_RXD<2>	OUT 18 69
	ENET_RXD<3>	OUT 18 69
ENET_RXCLK_PD (MAKE_BASE=TRUE)	ENET_CLK125M_RXCLK	OUT 18 69
	ENET_RX_CTRL	OUT 18 69
	ENET_MDIO	BI 18 69
	MCP_RGMII_VREF	OUT 18
	ENET_ENERGY_DET	OUT 18

R0980 10K 5% 1/20W MF 201
R0981 10K 5% 1/20W MF 201
R0982 10K 5% 1/20W MF 201
R0983 10K 5% 1/20W MF 201
R0984 10K 5% 1/20W MF 201
R0985 10K 5% 1/20W MF 201

GND

VOLTAGE=0V
MIN_LINE_WIDTH=0.58MM
MIN_NECK_WIDTH=0.20MM

LVDS ALIASES

17	=MCP_IFPA_TXC_P	NC_LVDS_IG_A_CLKP	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPA_TXC_N	NC_LVDS_IG_A_CLKN	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPA_TXD_P<0..3>	NC_LVDS_IG_A_DATAP<0..3>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPA_TXD_N<0..3>	NC_LVDS_IG_A_DATAN<0..3>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPB_TXC_P	NC_LVDS_IG_B_CLKP	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPB_TXC_N	NC_LVDS_IG_B_CLKN	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPB_TXD_P<0..3>	NC_LVDS_IG_B_DATAP<0..3>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	=MCP_IFPB_TXD_N<0..3>	NC_LVDS_IG_B_DATAN<0..3>	NO_TEST=TRUE, MAKE_BASE=TRUE
17	LCD_IG_BKLT_PWM	LCD_BKLT_PWM	62
59 17 9	LCD_IG_PWR_EN	LCD_IG_PWR_EN	MAKE_BASE=TRUE, 9 17 59
17	LCD_IG_BKLT_EN	LCD_BKLT_EN	MAKE_BASE=TRUE, 63
17	=MCP_IFPAB_DDC_CLK	TP_LVDS_DDC_CLK	MAKE_BASE=TRUE
17	=MCP_IFPAB_DDC_DATA	TP_LVDS_DDC_DATA	MAKE_BASE=TRUE

DISPLAY PORT ALIASES

67 17	DP_IG_ML0_P<0..3>	DP_EXT_ML_P<0..3>	61 71, MAKE_BASE=TRUE
67 17	DP_IG_ML0_N<0..3>	DP_EXT_ML_N<0..3>	61 71, MAKE_BASE=TRUE
17	DP_IG_HPD0	DP_EXT_HPD	MAKE_BASE=TRUE
67 17	DP_IG_AUX_CH0_P	DP_EXT_AUX_CH_P	MAKE_BASE=TRUE
67 17	DP_IG_AUX_CH0_N	DP_EXT_AUX_CH_N	MAKE_BASE=TRUE
66	DP_AUX_CH_C_N	DP_EXT_AUX_CH_C_N	61 71, MAKE_BASE=TRUE
66	DP_AUX_CH_C_P	DP_EXT_AUX_CH_C_P	61 71, MAKE_BASE=TRUE
66	DP_CA_DET	DP_EXT_CA_DET	MAKE_BASE=TRUE
67 17	DP_IG_ML1_P<1:0>	DP_INT_ML_P<1:0>	59 71, MAKE_BASE=TRUE
67 17	DP_IG_ML1_N<1:0>	DP_INT_ML_N<1:0>	59 71, MAKE_BASE=TRUE
67 17	DP_IG_AUX_CH1_P	DP_INT_AUX_CH_P	59 71, MAKE_BASE=TRUE
67 17	DP_IG_AUX_CH1_N	DP_INT_AUX_CH_N	59 71, MAKE_BASE=TRUE
17	DP_IG_HPD1	DP_INT_HPD	59, MAKE_BASE=TRUE
17	DP_IG_ML1_P<3:2>	TP_DP_INT_MLP<3:2>	MAKE_BASE=TRUE
17	DP_IG_ML1_N<3:2>	TP_DP_INT_MLN<3:2>	MAKE_BASE=TRUE

SATA ALIASES

UNUSED SATA ODD SIGNALS

67 18	SATA_ODD_R2D_C_P	NC_SATA_ODD_R2DCP	NO_TEST=TRUE, MAKE_BASE=TRUE
67 18	SATA_ODD_R2D_C_N	NC_SATA_ODD_R2DCN	NO_TEST=TRUE, MAKE_BASE=TRUE
67	SATA_ODD_R2D_P	NC_SATA_ODD_R2DP	NO_TEST=TRUE, MAKE_BASE=TRUE
67	SATA_ODD_R2D_N	NC_SATA_ODD_R2DN	NO_TEST=TRUE, MAKE_BASE=TRUE
67 18	SATA_ODD_D2R_P	NC_SATA_ODD_D2RP	NO_TEST=TRUE, MAKE_BASE=TRUE
67 18	SATA_ODD_D2R_N	NC_SATA_ODD_D2RN	NO_TEST=TRUE, MAKE_BASE=TRUE

CPU ALIASES

65 10	CPU_BSEL<0:2>	=MCP_BSEL<0:2>	MAKE_BASE=TRUE
14	CPU_PECI_MCP	TP_CPU_PECI_MCP	MAKE_BASE=TRUE

BSEL<2..0> 14

	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

MCP89 ALIASES

17	TP_MCP_RGB_DAC_VREF	NC_MCP_RGB_DAC_VREF	NO_TEST=TRUE, MAKE_BASE=TRUE
66 15	MEM_A_CLK_P<1>	TP_MEM_A_CLKP<1>	MAKE_BASE=TRUE
66 15	MEM_A_CLK_N<1>	TP_MEM_A_CLKN<1>	MAKE_BASE=TRUE
66 15	MEM_B_CLK_P<1>	TP_MEM_B_CLKP<1>	MAKE_BASE=TRUE
66 15	MEM_B_CLK_N<1>	TP_MEM_B_CLKN<1>	MAKE_BASE=TRUE
66 15	MEM_A_A<15>	TP_MEM_A_A<15>	MAKE_BASE=TRUE
66 15	MEM_B_A<15>	TP_MEM_B_A<15>	MAKE_BASE=TRUE
19	MCP_MEM_VDD_SEL_1V5	TP_MEM_VDD_SEL_1V5	MAKE_BASE=TRUE

CHARGER SIGNAL

50 IN =CHGR_ACOK — SMC_BC_ACOK (MAKE_BASE=TRUE) OUT 7 37 38 39

MCPCOREISNS SIGNAL

54 MCPCORES0_VO — =MCPCOREISNS_N 43 (MAKE_BASE=TRUE)
54 MCPCORES0_ISP_R — =MCPCOREISNS_P 43 (MAKE_BASE=TRUE)

SYNC_MASTER=K6_MLB	SYNC_DATE=12/11/2009
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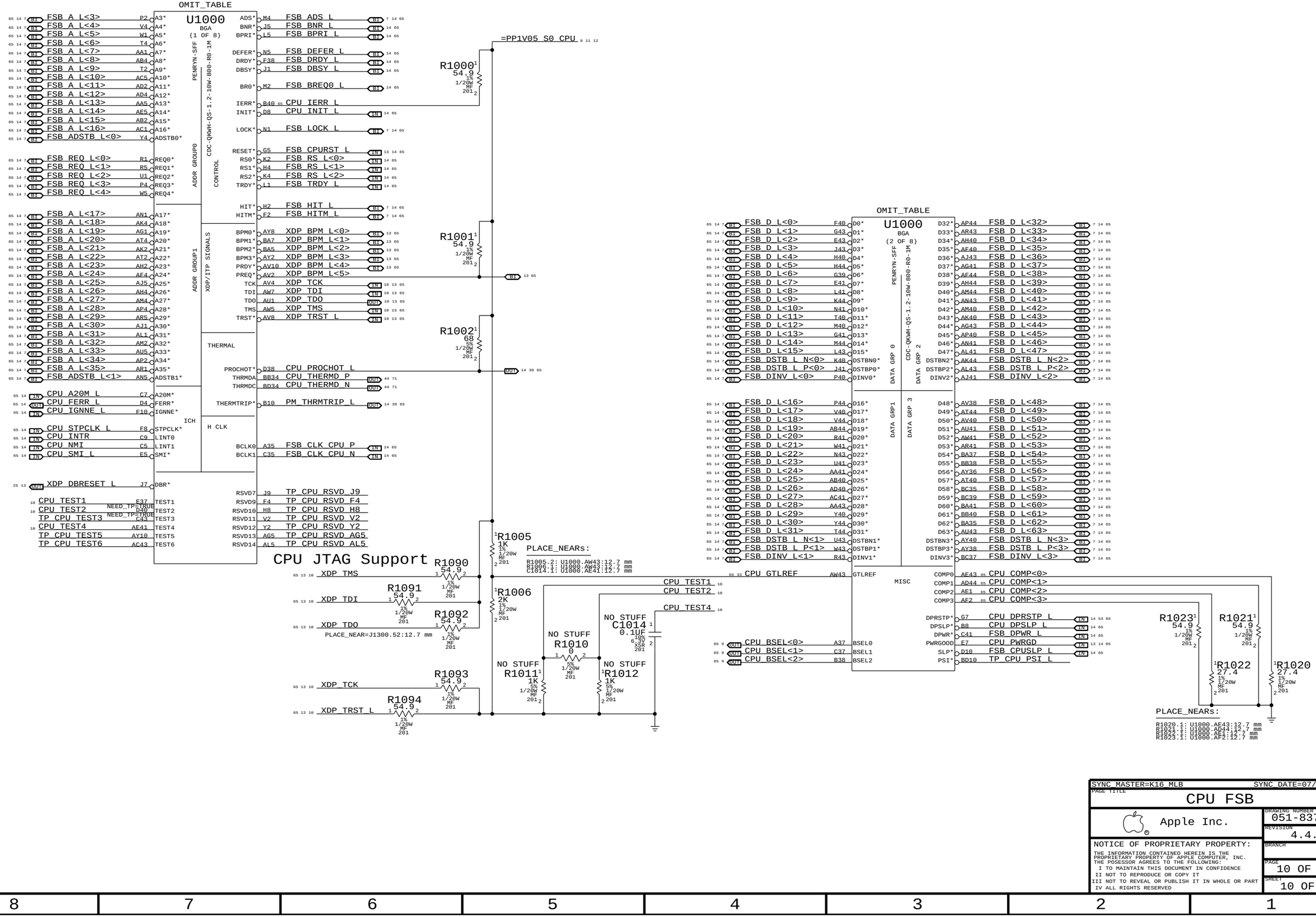

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: CPU FSB

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

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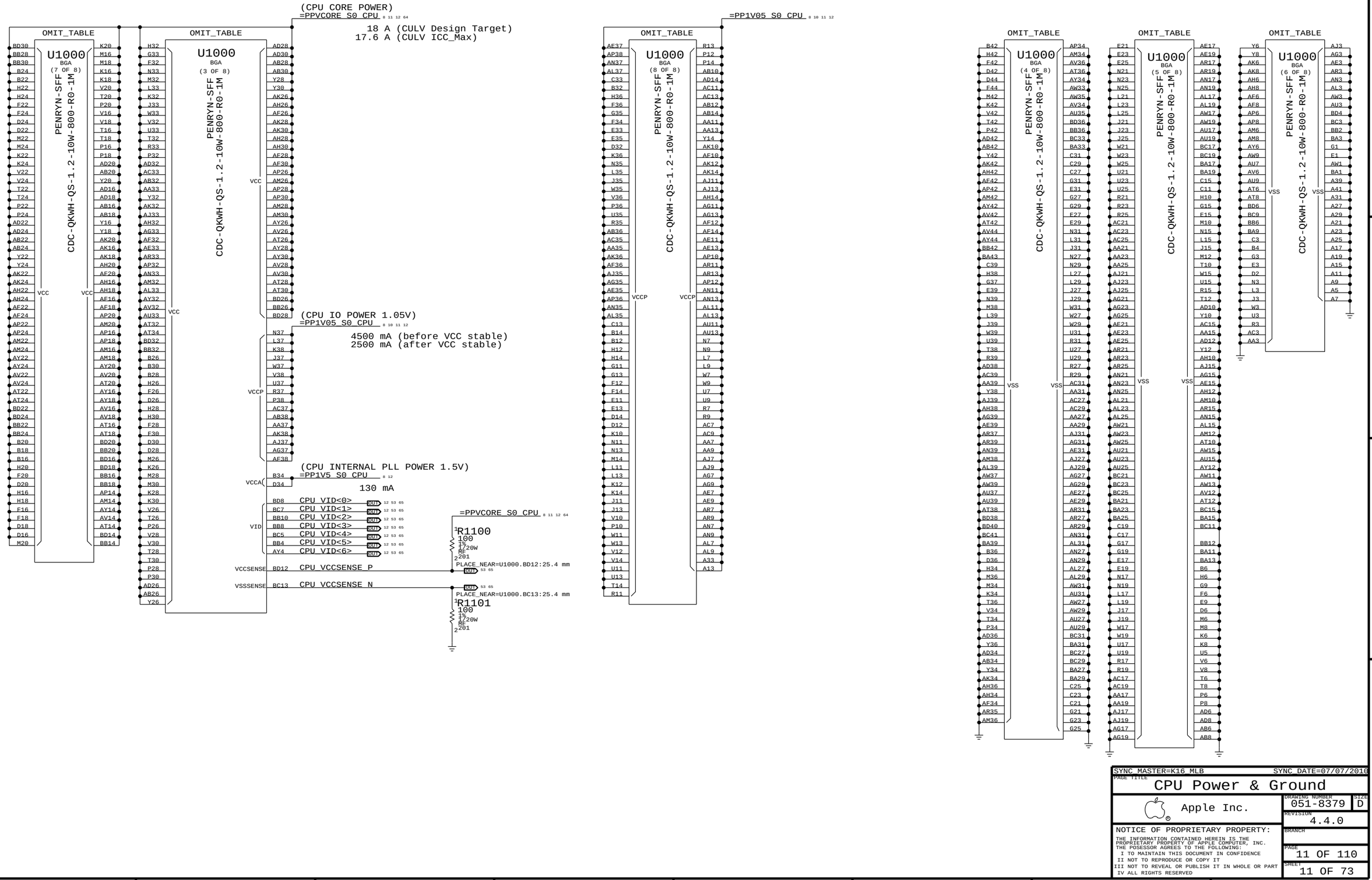

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: CPU Power & Ground

Apple Inc.

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CPU VCORE HF AND BULK DECOUPLING

4x 270uF. 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

64 11 8 =PPVCORE_S0_CPU

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL NOSTUFF C1200 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1201 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1202 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1203 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1204 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1205 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1206 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1207 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1208 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1209 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1210 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1211 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1212 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1213 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1214 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1215 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1216 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1217 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1218 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1219 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL NOSTUFF C1220 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1221 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1222 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1223 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1224 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1225 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1226 10UF 20% 6.3V X5R 603
CRITICAL OMIT_TABLE C1227 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1228 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1229 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1230 10UF 20% 6.3V X5R 603
CRITICAL NOSTUFF C1231 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1240 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1241 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1242 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1243 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1244 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1245 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1246 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1247 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1248 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1249 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1250 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1251 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1252 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1253 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1254 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1255 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1256 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1257 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1258 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1259 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1260 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1261 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1262 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1263 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1264 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1265 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1266 2.2UF 20% 6.3V CERM 402-LF
CRITICAL OMIT_TABLE C1267 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

CRITICAL C1270 270UF 20% 2V TANT CASE-B4-SM
CRITICAL C1271 270UF 20% 2V TANT CASE-B4-SM
CRITICAL C1272 270UF 20% 2V TANT CASE-B4-SM

CPU VCORE VID CONNECTIONS

65 53 11 IN CPU_VID<0..6> = IMVP6_VID<0..6> OUT 65
MAKE_BASE=TRUE

VCCA (CPU AVdd) DECOUPLING

11 8 =PP1V5_S0_CPU 1x 10uF, 1x 0.01uF

OMIT_TABLE C1280 10UF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V X5R 201

LAYOUT NOTE:
PLACE C1281 NEAR PIN B34 OF U1000

VCCP (CPU I/O) DECOUPLING

11 10 8 =PP1V05_S0_CPU 1x 270uF, 12x 2.2uF

OMIT_TABLE C1283 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1284 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1285 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1286 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1287 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1288 2.2UF 20% 6.3V CERM 402-LF

CRITICAL C1290 270UF 20% 2V TANT CASE-B4-SM
OMIT_TABLE C1291 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1292 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1293 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1294 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1295 2.2UF 20% 6.3V CERM 402-LF
OMIT_TABLE C1296 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE C1290 CLOSE TO CPU
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

SYNC_MASTER=K16_MLB SYNC_DATE=03/24/2010

PAGE TITLE
CPU Decoupling & VID

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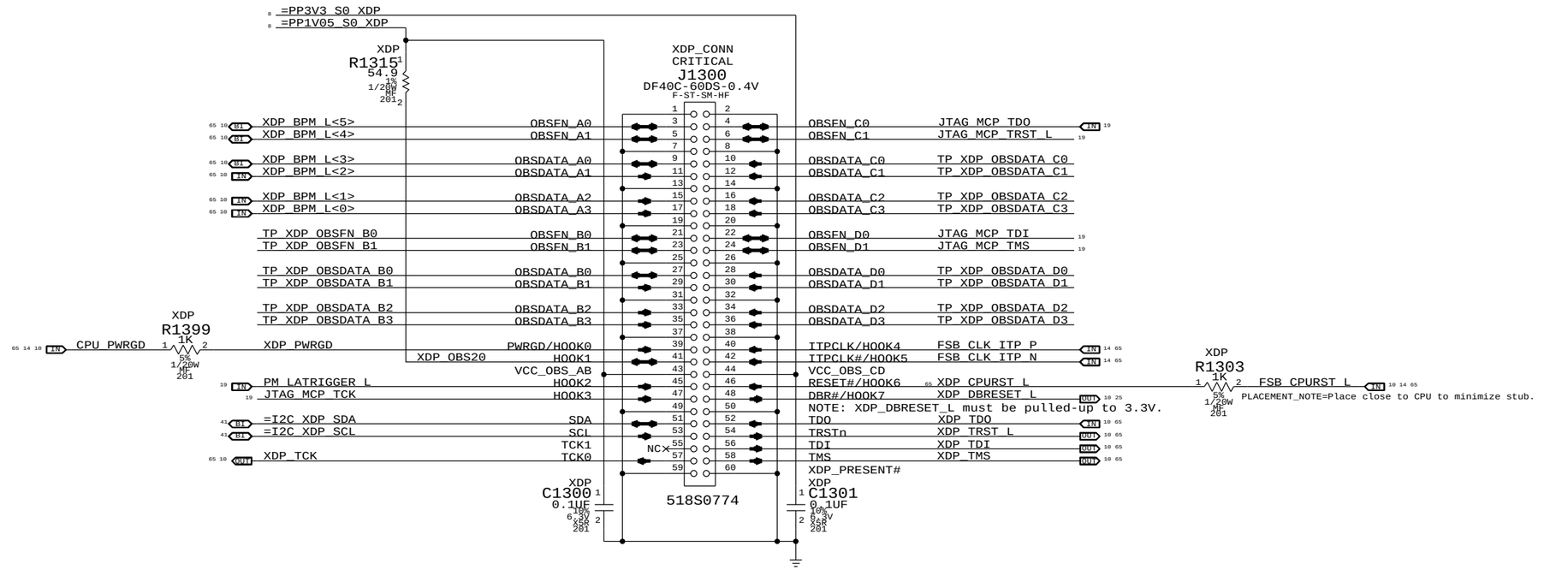
Micro2-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0782 Adapter Flex to support chipset debug.



Direction of XDP adapter flex

Please place J1300 within 1" of
board edge with odd-numbered pins
facing edge. Avoid any tall
components between J1300 and edge.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
eXtended Debug Port (Micro-XDP)

Apple Inc.

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OMIT_TABLE

U1400
MCP89U-A01
BGA

SYMBOL 1 OF 11

FSB

FSB_DSTB_L_P<0>	J38	CPU_DSTBP0*	
FSB_DSTB_L_N<0>	J39	CPU_DSTBN0*	
FSB_DINV_L<0>	F39	CPU_DBI0*	
FSB_DSTB_L_P<1>	R34	CPU_DSTBP1*	
FSB_DSTB_L_N<1>	R35	CPU_DSTBN1*	
FSB_DINV_L<1>	U36	CPU_DBI1*	
FSB_DSTB_L_P<2>	J37	CPU_DSTBP2*	
FSB_DSTB_L_N<2>	J36	CPU_DSTBN2*	
FSB_DINV_L<2>	L35	CPU_DBI2*	
FSB_DSTB_L_P<3>	C37	CPU_DSTBP3*	
FSB_DSTB_L_N<3>	C38	CPU_DSTBN3*	
FSB_DINV_L<3>	B35	CPU_DBI3*	
FSB_A_L<3>	U38	CPU_A3*	
FSB_A_L<4>	V37	CPU_A4*	
FSB_A_L<5>	Y36	CPU_A5*	
FSB_A_L<6>	V40	CPU_A6*	
FSB_A_L<7>	Y39	CPU_A7*	
FSB_A_L<8>	Y40	CPU_A8*	
FSB_A_L<9>	V39	CPU_A9*	
FSB_A_L<10>	AA39	CPU_A10*	
FSB_A_L<11>	AA36	CPU_A11*	
FSB_A_L<12>	AA37	CPU_A12*	
FSB_A_L<13>	Y38	CPU_A13*	
FSB_A_L<14>	AC36	CPU_A14*	
FSB_A_L<15>	AA40	CPU_A15*	
FSB_A_L<16>	AA38	CPU_A16*	
FSB_A_L<17>	AF39	CPU_A17*	
FSB_A_L<18>	AD38	CPU_A18*	
FSB_A_L<19>	AC38	CPU_A19*	
FSB_A_L<20>	AJ38	CPU_A20*	
FSB_A_L<21>	AD37	CPU_A21*	
FSB_A_L<22>	AJ39	CPU_A22*	
FSB_A_L<23>	AC40	CPU_A23*	
FSB_A_L<24>	AC37	CPU_A24*	
FSB_A_L<25>	AD40	CPU_A25*	
FSB_A_L<26>	AC39	CPU_A26*	
FSB_A_L<27>	AF36	CPU_A27*	
FSB_A_L<28>	AF40	CPU_A28*	
FSB_A_L<29>	AG39	CPU_A29*	
FSB_A_L<30>	AD39	CPU_A30*	
FSB_A_L<31>	AD36	CPU_A31*	
FSB_A_L<32>	AF37	CPU_A32*	
FSB_A_L<33>	AJ40	CPU_A33*	
FSB_A_L<34>	AG40	CPU_A34*	
FSB_A_L<35>	AG38	CPU_A35*	
FSB_ADSTB_L<0>	Y37	CPU_ADSTB0*	
FSB_ADSTB_L<1>	AF38	CPU_ADSTB1*	
FSB_REQ_L<0>	U40	CPU_REQ0*	
FSB_REQ_L<1>	U39	CPU_REQ1*	
FSB_REQ_L<2>	V38	CPU_REQ2*	
FSB_REQ_L<3>	U37	CPU_REQ3*	
FSB_REQ_L<4>	V36	CPU_REQ4*	
FSB_ADS_L	AG33	CPU_ADS*	
FSB_BNR_L	AD35	CPU_BNR*	
FSB_BREQ0_L	AG34	CPU_BR0*	
FSB_DBSY_L	AF35	CPU_DBSY*	
FSB_DRDY_L	U32	CPU_DRDY*	
FSB_HIT_L	AD34	CPU_HIT*	
FSB_HITM_L	AD32	CPU_HITM*	
FSB_LOCK_L	AG37	CPU_LOCK*	
FSB_TRDY_L	AG32	CPU_TRDY*	
CPU_PECI_MCP	AG36	CPU_PECI	
CPU_PROCHOT_L	V32	CPU_PROCHOT*	
	V35	CPU_THERMTRIP*	
PM_THRMTRIP_L	AC33	CPU_FERR*	
CPU_FERR_L			
=MCP_BSEL<2>	D35	CPU_BSEL2	
=MCP_BSEL<1>	E35	CPU_BSEL1	
=MCP_BSEL<0>	F35	CPU_BSEL0	
FSB_RS_L<0>	AF33	CPU_RS0*	
FSB_RS_L<1>	AD33	CPU_RS1*	
FSB_RS_L<2>	AF34	CPU_RS2*	
MCP_BCLK_VML_COMP_VDD	AK39	BCLK_VML_COMP_VDD	
MCP_BCLK_VML_COMP_GND	AK40	BCLK_VML_COMP_GND	
MCP_CPU_COMP_VCC	AK38	CPU_COMP_VCC	
MCP_CPU_COMP_GND	AK37	CPU_COMP_GND	

CPU_D0*	M37	FSB_D_L<0>	
CPU_D1*	M39	FSB_D_L<1>	
CPU_D2*	P39	FSB_D_L<2>	
CPU_D3*	L38	FSB_D_L<3>	
CPU_D4*	L39	FSB_D_L<4>	
CPU_D5*	L40	FSB_D_L<5>	
CPU_D6*	M40	FSB_D_L<6>	
CPU_D7*	P40	FSB_D_L<7>	
CPU_D8*	H40	FSB_D_L<8>	
CPU_D9*	L37	FSB_D_L<9>	
CPU_D10*	F38	FSB_D_L<10>	
CPU_D11*	F40	FSB_D_L<11>	
CPU_D12*	H38	FSB_D_L<12>	
CPU_D13*	M38	FSB_D_L<13>	
CPU_D14*	H39	FSB_D_L<14>	
CPU_D15*	J40	FSB_D_L<15>	
CPU_D16*	U35	FSB_D_L<16>	
CPU_D17*	R36	FSB_D_L<17>	
CPU_D18*	R37	FSB_D_L<18>	
CPU_D19*	P35	FSB_D_L<19>	
CPU_D20*	R38	FSB_D_L<20>	
CPU_D21*	R33	FSB_D_L<21>	
CPU_D22*	U34	FSB_D_L<22>	
CPU_D23*	R40	FSB_D_L<23>	
CPU_D24*	P34	FSB_D_L<24>	
CPU_D25*	P37	FSB_D_L<25>	
CPU_D26*	P38	FSB_D_L<26>	
CPU_D27*	P36	FSB_D_L<27>	
CPU_D28*	P33	FSB_D_L<28>	
CPU_D29*	P32	FSB_D_L<29>	
CPU_D30*	R32	FSB_D_L<30>	
CPU_D31*	R39	FSB_D_L<31>	
CPU_D32*	H36	FSB_D_L<32>	
CPU_D33*	F36	FSB_D_L<33>	
CPU_D34*	L33	FSB_D_L<34>	
CPU_D35*	M35	FSB_D_L<35>	
CPU_D36*	L34	FSB_D_L<36>	
CPU_D37*	M33	FSB_D_L<37>	
CPU_D38*	M36	FSB_D_L<38>	
CPU_D39*	M32	FSB_D_L<39>	
CPU_D40*	J34	FSB_D_L<40>	
CPU_D41*	H35	FSB_D_L<41>	
CPU_D42*	H34	FSB_D_L<42>	
CPU_D43*	L36	FSB_D_L<43>	
CPU_D44*	M34	FSB_D_L<44>	
CPU_D45*	F37	FSB_D_L<45>	
CPU_D46*	H37	FSB_D_L<46>	
CPU_D47*	J35	FSB_D_L<47>	
CPU_D48*	D39	FSB_D_L<48>	
CPU_D49*	E36	FSB_D_L<49>	
CPU_D50*	D40	FSB_D_L<50>	
CPU_D51*	E40	FSB_D_L<51>	
CPU_D52*	C39	FSB_D_L<52>	
CPU_D53*	E38	FSB_D_L<53>	
CPU_D54*	A37	FSB_D_L<54>	
CPU_D55*	C36	FSB_D_L<55>	
CPU_D56*	B38	FSB_D_L<56>	
CPU_D57*	E37	FSB_D_L<57>	
CPU_D58*	C35	FSB_D_L<58>	
CPU_D59*	A35	FSB_D_L<59>	
CPU_D60*	B37	FSB_D_L<60>	
CPU_D61*	D36	FSB_D_L<61>	
CPU_D62*	A36	FSB_D_L<62>	
CPU_D63*	D38	FSB_D_L<63>	
CPU_BPRI*	AF32	FSB_BPRI_L	
CPU_DEFER*	AG35	FSB_DEFER_L	
BCLK_OUT_CPU_P	AJ37	FSB_CLK_CPU_P	
BCLK_OUT_CPU_N	AJ36	FSB_CLK_CPU_N	
BCLK_OUT_ITP_P	AK32	FSB_CLK_ITP_P	
BCLK_OUT_ITP_N	AK33	FSB_CLK_ITP_N	
BCLK_OUT_NB_P	AJ35	FSB_CLK_MCP_P	
BCLK_OUT_NB_N	AJ34	FSB_CLK_MCP_N	
BCLK_IN_N	AJ32		
BCLK_IN_P	AJ33		
CPU_A20M*	AA33	CPU_A20M_L	
CPU_IGNNE*	V33	CPU_IGNNE_L	
CPU_INIT*	Y33	CPU_INIT_L	
CPU_INTR	Y35	CPU_INTR	
CPU_NMI	AA35	CPU_NMI	
CPU_SMI*	AC35	CPU_SMI_L	
CPU_PWRGD	AA32	CPU_PWRGD	
CPU_RESET*	AC34	FSB_CPURST_L	
CPU_DPRSLPVR	D2	PM_DPRSLPVR	
CPU_SLP*	V34	FSB_CPUSLP_L	
CPU_DPSLP*	Y32	CPU_DPSLP_L	
CPU_DPWR*	U33	FSB_DPWR_L	
CPU_STPCLK*	Y34	CPU_STPCLK_L	
CPU_DPRSTP*	AA34	CPU_DPRSTP_L	

Loop-back clock for delay matching.

=PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/20W MF 201

R1415 62 5% 1/20W MF 201

R1430 49.9 1% 1/20W MF 201

R1435 49.9 1% 1/20W MF 201

R1431 49.9 1% 1/20W MF 201

R1436 49.9 1% 1/20W MF 201

=PP1V05_S0_MCP_FSB

NO STUFF

R1440 150 5% 1/20W MF 201

SYNC_MASTER=K16_MLB	SYNC_DATE=07/07/2010
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MEM_A_DQ<63>	AN6	MDQ0_63	MDQS0_7_P	AR4	MEM_A_DQS_P<7>
MEM_A_DQ<62>	AN4	MDQ0_62	MDQS0_7_N	AR5	MEM_A_DQS_N<7>
MEM_A_DQ<61>	AT4	MDQ0_61	MDQS0_6_P	AT6	MEM_A_DQS_P<6>
MEM_A_DQ<60>	AU3	MDQ0_60	MDQS0_6_N	AU6	MEM_A_DQS_N<6>
MEM_A_DQ<59>	AM7	MDQ0_59	MDQS0_5_P	AN11	MEM_A_DQS_P<5>
MEM_A_DQ<58>	AN7	MDQ0_58	MDQS0_5_N	AM11	MEM_A_DQS_N<5>
MEM_A_DQ<57>	AT5	MDQ0_57	MDQS0_4_P	AT12	MEM_A_DQS_P<4>
MEM_A_DQ<56>	AT3	MDQ0_56	MDQS0_4_N	AR12	MEM_A_DQS_N<4>
MEM_A_DQ<55>	AU5	MDQ0_55	MDQS0_3_P	AR29	MEM_A_DQS_P<3>
MEM_A_DQ<54>	AV5	MDQ0_54	MDQS0_3_N	AP29	MEM_A_DQS_N<3>
MEM_A_DQ<53>	AR6	MDQ0_53	MDQS0_2_P	AR32	MEM_A_DQS_P<2>
MEM_A_DQ<52>	AN9	MDQ0_52	MDQS0_2_N	AP32	MEM_A_DQS_N<2>
MEM_A_DQ<51>	AV3	MDQ0_51	MDQS0_1_P	AV36	MEM_A_DQS_P<1>
MEM_A_DQ<50>	AV4	MDQ0_50	MDQS0_1_N	AU36	MEM_A_DQS_N<1>
MEM_A_DQ<49>	AM8	MDQ0_49	MDQS0_0_P	AN35	MEM_A_DQS_P<0>
MEM_A_DQ<48>	AN8	MDQ0_48	MDQS0_0_N	AN34	MEM_A_DQS_N<0>
MEM_A_DQ<47>	AP8	MDQ0_47			
MEM_A_DQ<46>	AP9	MDQ0_46			
MEM_A_DQ<45>	AN12	MDQ0_45			
MEM_A_DQ<44>	AT11	MDQ0_44			
MEM_A_DQ<43>	AT8	MDQ0_43			
MEM_A_DQ<42>	AR8	MDQ0_42			
MEM_A_DQ<41>	AT9	MDQ0_41			
MEM_A_DQ<40>	AM12	MDQ0_40			
MEM_A_DQ<39>	AP12	MDQ0_39			
MEM_A_DQ<38>	AN14	MDQ0_38			
MEM_A_DQ<37>	AT14	MDQ0_37			
MEM_A_DQ<36>	AR14	MDQ0_36			
MEM_A_DQ<35>	AR11	MDQ0_35			
MEM_A_DQ<34>	AP11	MDQ0_34			
MEM_A_DQ<33>	AM15	MDQ0_33			
MEM_A_DQ<32>	AN15	MDQ0_32			
MEM_A_DQ<31>	AR27	MDQ0_31			
MEM_A_DQ<30>	AT27	MDQ0_30			
MEM_A_DQ<29>	AM30	MDQ0_29			
MEM_A_DQ<28>	AN30	MDQ0_28			
MEM_A_DQ<27>	AN27	MDQ0_27			
MEM_A_DQ<26>	AP27	MDQ0_26			
MEM_A_DQ<25>	AN29	MDQ0_25			
MEM_A_DQ<24>	AM29	MDQ0_24			
MEM_A_DQ<23>	AT30	MDQ0_23			
MEM_A_DQ<22>	AT32	MDQ0_22			
MEM_A_DQ<21>	AP33	MDQ0_21			
MEM_A_DQ<20>	AR33	MDQ0_20			
MEM_A_DQ<19>	AP30	MDQ0_19			
MEM_A_DQ<18>	AR30	MDQ0_18			
MEM_A_DQ<17>	AM33	MDQ0_17			
MEM_A_DQ<16>	AN33	MDQ0_16			
MEM_A_DQ<15>	AU35	MDQ0_15			
MEM_A_DQ<14>	AV35	MDQ0_14			
MEM_A_DQ<13>	AT37	MDQ0_13			
MEM_A_DQ<12>	AT38	MDQ0_12			
MEM_A_DQ<11>	AT33	MDQ0_11			
MEM_A_DQ<10>	AT35	MDQ0_10			
MEM_A_DQ<9>	AV37	MDQ0_9			
MEM_A_DQ<8>	AU38	MDQ0_8			
MEM_A_DQ<7>	AR35	MDQ0_7			
MEM_A_DQ<6>	AN36	MDQ0_6			
MEM_A_DQ<5>	AM35	MDQ0_5			
MEM_A_DQ<4>	AM34	MDQ0_4			
MEM_A_DQ<3>	AR36	MDQ0_3			
MEM_A_DQ<2>	AR37	MDQ0_2			
MEM_A_DQ<1>	AM36	MDQ0_1			
MEM_A_DQ<0>	AM37	MDQ0_0			
MEM_A_DM<7>	AN5	MDQM0_7			
MEM_A_DM<6>	AM9	MDQM0_6			
MEM_A_DM<5>	AR9	MDQM0_5			
MEM_A_DM<4>	AM14	MDQM0_4			
MEM_A_DM<3>	AT29	MDQM0_3			
MEM_A_DM<2>	AN32	MDQM0_2			
MEM_A_DM<1>	AT36	MDQM0_1			
MEM_A_DM<0>	AN37	MDQM0_0			

MRAS0*	AR17	MEM_A_RAS_L	26 27 32 66
MCAS0*	AM17	MEM_A_CAS_L	26 27 32 66
MWE0*	AM18	MEM_A_WE_L	26 27 32 66
MBA0_2	AR26	MEM_A_BA<2>	26 27 32 66
MBA0_1	AR18	MEM_A_BA<1>	26 27 32 66
MBA0_0	AP17	MEM_A_BA<0>	26 27 32 66
MA0_15	AN26	MEM_A_A<15>	9 66
MA0_14	AP26	MEM_A_A<14>	26 27 32 66
MA0_13	AR15	MEM_A_A<13>	26 27 32 66
MA0_12	AR24	MEM_A_A<12>	26 27 32 66
MA0_11	AP23	MEM_A_A<11>	26 27 32 66
MA0_10	AP18	MEM_A_A<10>	26 27 32 66
MA0_9	AP24	MEM_A_A<9>	26 27 32 66
MA0_8	AN24	MEM_A_A<8>	26 27 32 66
MA0_7	AR23	MEM_A_A<7>	26 27 32 66
MA0_6	AM23	MEM_A_A<6>	26 27 32 66
MA0_5	AM24	MEM_A_A<5>	26 27 32 66
MA0_4	AN23	MEM_A_A<4>	26 27 32 66
MA0_3	AR21	MEM_A_A<3>	26 27 32 66
MA0_2	AP20	MEM_A_A<2>	26 27 32 66
MA0_1	AP21	MEM_A_A<1>	26 27 32 66
MA0_0	AR20	MEM_A_A<0>	26 27 32 66

=PP1V05_S0_MCP_M2CLK_DLL 8 23

+VIO_M2CLK_DLL	AJ30	550 mA
+VIO_M2CLK_DLL	AK30	
+VIO_M2CLK_DLL	AK31	

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+VIO_PLL_MEM	AH29	20 mA
+VIO_PLL_MEM	AH30	70 mA
+VIO_PLL_MEM	AJ31	
+VIO_PLL_FSB	AF29	25 mA
+VIO_PLL_FSB	AF30	
+VIO_PLL_FSB	AF31	25 mA
+VIO_PLL_CPU	AG29	
+VIO_PLL_CPU	AG30	
+VIO_PLL_CPU	AG31	

MCLK0A_1_P	AM21	MEM_A_CLK_P<1>	9 66
MCLK0A_1_N	AN21	MEM_A_CLK_N<1>	9 66
MCLK0A_0_P	AM20	MEM_A_CLK_P<0>	26 27 32 66
MCLK0A_0_N	AN20	MEM_A_CLK_N<0>	26 27 32 66
MCS0A_1*	AP15	MEM_A_CS_L<1>	26 27 32 66
MCS0A_0*	AN18	MEM_A_CS_L<0>	26 27 32 66
MODT0A_1	AP14	MEM_A_ODT<1>	26 27 32 66
MODT0A_0	AN17	MEM_A_ODT<0>	26 27 32 66
MCKE0A_1	AM27	MEM_A_CKE<1>	21 26 27 32 66
MCKE0A_0	AM26	MEM_A_CKE<0>	21 26 27 32 66

OMIT_TABLE

U1400 MCP89U-A01 BGA — SYMBOL 3 OF 11 — MEMORY PARTITION 1

MEM_B_DQ<63>	AM1	MDQ1_63	MDQS1_7_P	AN2	MEM_B_DQS_P<7>
MEM_B_DQ<62>	AN1	MDQ1_62	MDQS1_7_N	AN3	MEM_B_DQS_N<7>
MEM_B_DQ<61>	AT1	MDQ1_61	MDQS1_6_P	AY5	MEM_B_DQS_P<6>
MEM_B_DQ<60>	AU1	MDQ1_60	MDQS1_6_N	AY4	MEM_B_DQS_N<6>
MEM_B_DQ<59>	AM3	MDQ1_59	MDQS1_5_P	AV11	MEM_B_DQS_P<5>
MEM_B_DQ<58>	AM2	MDQ1_58	MDQS1_5_N	AW11	MEM_B_DQS_N<5>
MEM_B_DQ<57>	AR2	MDQ1_57	MDQS1_4_P	AV14	MEM_B_DQS_P<4>
MEM_B_DQ<56>	AR1	MDQ1_56	MDQS1_4_N	AW14	MEM_B_DQS_N<4>
MEM_B_DQ<55>	AW3	MDQ1_55	MDQS1_3_P	AW27	MEM_B_DQS_P<3>
MEM_B_DQ<54>	AW4	MDQ1_54	MDQS1_3_N	AY27	MEM_B_DQS_N<3>
MEM_B_DQ<53>	AU8	MDQ1_53	MDQS1_2_P	AV32	MEM_B_DQS_P<2>
MEM_B_DQ<52>	AV8	MDQ1_52	MDQS1_2_N	AW32	MEM_B_DQS_N<2>
MEM_B_DQ<51>	AU2	MDQ1_51	MDQS1_1_P	AY32	MEM_B_DQS_P<1>
MEM_B_DQ<50>	AV2	MDQ1_50	MDQS1_1_N	AY36	MEM_B_DQS_N<1>
MEM_B_DQ<49>	AW6	MDQ1_49	MDQS1_0_P	AN38	MEM_B_DQS_P<0>
MEM_B_DQ<48>	AV6	MDQ1_48	MDQS1_0_N	AN39	MEM_B_DQS_N<0>
MEM_B_DQ<47>	AY9	MDQ1_47			
MEM_B_DQ<46>	AW9	MDQ1_46			
MEM_B_DQ<45>	AY11	MDQ1_45			
MEM_B_DQ<44>	AY12	MDQ1_44			
MEM_B_DQ<43>	AW8	MDQ1_43			
MEM_B_DQ<42>	AY8	MDQ1_42			
MEM_B_DQ<41>	AU9	MDQ1_41			
MEM_B_DQ<40>	AU11	MDQ1_40			
MEM_B_DQ<39>	AU12	MDQ1_39			
MEM_B_DQ<38>	AU14	MDQ1_38			
MEM_B_DQ<37>	AV15	MDQ1_37			
MEM_B_DQ<36>	AU15	MDQ1_36			
MEM_B_DQ<35>	AW12	MDQ1_35			
MEM_B_DQ<34>	AV12	MDQ1_34			
MEM_B_DQ<33>	AY15	MDQ1_33			
MEM_B_DQ<32>	AW15	MDQ1_32			
MEM_B_DQ<31>	AW26	MDQ1_31			
MEM_B_DQ<30>	AY26	MDQ1_30			
MEM_B_DQ<29>	AV29	MDQ1_29			
MEM_B_DQ<28>	AW29	MDQ1_28			
MEM_B_DQ<27>	AU26	MDQ1_27			
MEM_B_DQ<26>	AV26	MDQ1_26			
MEM_B_DQ<25>	AU27	MDQ1_25			
MEM_B_DQ<24>	AU29	MDQ1_24			
MEM_B_DQ<23>	AW30	MDQ1_23			
MEM_B_DQ<22>	AV30	MDQ1_22			
MEM_B_DQ<21>	AY33	MDQ1_21			
MEM_B_DQ<20>	AW33	MDQ1_20			
MEM_B_DQ<19>	AY29	MDQ1_19			
MEM_B_DQ<18>	AY30	MDQ1_18			
MEM_B_DQ<17>	AU32	MDQ1_17			
MEM_B_DQ<16>	AY32	MDQ1_16			
MEM_B_DQ<15>	AW35	MDQ1_15			
MEM_B_DQ<14>	AY35	MDQ1_14			
MEM_B_DQ<13>	AV39	MDQ1_13			
MEM_B_DQ<12>	AU39	MDQ1_12			
MEM_B_DQ<11>	AV33	MDQ1_11			
MEM_B_DQ<10>	AU33	MDQ1_10			
MEM_B_DQ<9>	AW38	MDQ1_9			
MEM_B_DQ<8>	AV38	MDQ1_8			
MEM_B_DQ<7>	AR40	MDQ1_7			
MEM_B_DQ<6>	AR39	MDQ1_6			
MEM_B_DQ<5>	AM39	MDQ1_5			
MEM_B_DQ<4>	AM38	MDQ1_4			
MEM_B_DQ<3>	AT40	MDQ1_3			
MEM_B_DQ<2>	AU40	MDQ1_2			
MEM_B_DQ<1>	AN40	MDQ1_1			
MEM_B_DQ<0>	AM40	MDQ1_0			
MEM_B_DM<7>	AR3	MDQM1_7			
MEM_B_DM<6>	AY6	MDQM1_6			
MEM_B_DM<5>	AV9	MDQM1_5			
MEM_B_DM<4>	AY14	MDQM1_4			
MEM_B_DM<3>	AV27	MDQM1_3			
MEM_B_DM<2>	AU30	MDQM1_2			
MEM_B_DM<1>	AW37	MDQM1_1			
MEM_B_DM<0>	AR38	MDQM1_0			

MRAS1*	AW18	MEM_B_RAS_L	28 29 32 66
MCAS1*	AV17	MEM_B_CAS_L	28 29 32 66
MWE1*	AY18	MEM_B_WE_L	28 29 32 66
MBA1_2	AW24	MEM_B_BA<2>	28 29 32 66
MBA1_1	AT18	MEM_B_BA<1>	28 29 32 66
MBA1_0	AV18	MEM_B_BA<0>	28 29 32 66
MA1_15	AU24	MEM_B_A<15>	9 66
MA1_14	AV24	MEM_B_A<14>	28 29 32 66
MA1_13	AU17	MEM_B_A<13>	28 29 32 66
MA1_12	AY24	MEM_B_A<12>	28 29 32 66
MA1_11	AW23	MEM_B_A<11>	28 29 32 66
MA1_10	AU18	MEM_B_A<10>	28 29 32 66
MA1_9	AY23	MEM_B_A<9>	28 29 32 66
MA1_8	AU23	MEM_B_A<8>	28 29 32 66
MA1_7	AV23	MEM_B_A<7>	28 29 32 66
MA1_6	AT21	MEM_B_A<6>	28 29 32 66
MA1_5	AT23	MEM_B_A<5>	28 29 32 66
MA1_4	AU21	MEM_B_A<4>	28 29 32 66
MA1_3	AV21	MEM_B_A<3>	28 29 32 66
MA1_2	AY21	MEM_B_A<2>	28 29 32 66
MA1_1	AW21	MEM_B_A<1>	28 29 32 66
MA1_0	AY20	MEM_B_A<0>	28 29 32 66

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R1520 1K 5% 1/20W MF 201

MRESET0*	AM6	MEM_RESET_L	26 27 28 29
MCLK1A_1_P	AV20	MEM_B_CLK_P<1>	9 66
MCLK1A_1_N	AW20	MEM_B_CLK_N<1>	9 66
MCLK1A_0_P	AT20	MEM_B_CLK_P<0>	28 29 32 66
MCLK1A_0_N	AU20	MEM_B_CLK_N<0>	28 29 32 66
MCS1A_1*	AT15	MEM_B_CS_L<1>	28 29 32 66
MCS1A_0*	AY17	MEM_B_CS_L<0>	28 29 32 66
MODT1A_1	AT17	MEM_B_ODT<1>	28 29 32 66
MODT1A_0	AW17	MEM_B_ODT<0>	28 29 32 66
MCKE1A_1	AT24	MEM_B_CKE<1>	21 28 29 32 66
MCKE1A_0	AT26	MEM_B_CKE<0>	21 28 29 32 66

23 21 20 =PP1V5R1V35_SW_MCP_MEM

R1510 40.2 1% 1/20W MF 201

R1511 40.2 1% 1/20W MF 201

MCP_MEM_COMP_GND	AL23	MEM_COMP_GND
MCP_MEM_COMP_VDD	AL24	MEM_COMP_VDD

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

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Apple Inc.

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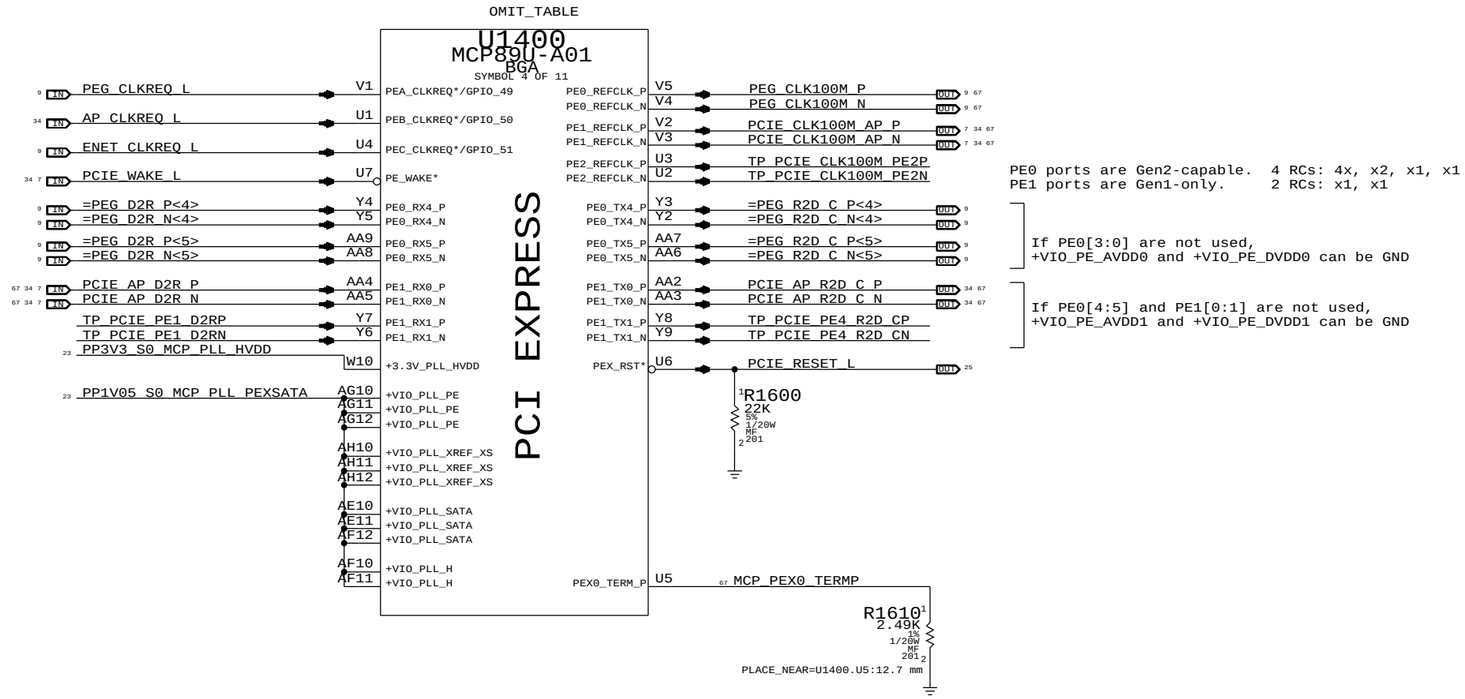
Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.



Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

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OMIT_TABLE

U1400
MCP89U-A01
BGA
SYMBOL 5 OF 11

RGB

24 PP3V3_S0_MCP_DAC 140 mA	K30	+3.3V_RGBDAC	DDC_CLK0/GPIO_38	G30	AUD_IP_PERIPHERAL_DET (IN) 7 17 37
9 TP_MCP_RGB_DAC_VREF	J29	RGB_DAC_VREF	DDC_DATA0/GPIO_39	F30	MIKEY_MIC_LOAD_DET (IN) 17

FLAT PANEL

67 9 OUT DP_IG_ML0_P<3>	H27	DP0_3_P/TMDS0_TXC_P	IFPA_TXC_P	K24	=MCP_IFPA_TXC_P (OUT) 9
67 9 OUT DP_IG_ML0_N<3>	J27	DP0_3_N/TMDS0_TXC_N	IFPA_TXC_N	K23	=MCP_IFPA_TXC_N (OUT) 9
67 9 OUT DP_IG_ML0_P<2>	D26	DP0_2_P/TMDS0_TX0_P	IFPA_TXD0_P	B23	=MCP_IFPA_TXD_P<0> (OUT) 9
67 9 OUT DP_IG_ML0_N<2>	C26	DP0_2_N/TMDS0_TX0_N	IFPA_TXD0_N	C23	=MCP_IFPA_TXD_N<0> (OUT) 9
67 9 OUT DP_IG_ML0_P<1>	F26	DP0_1_P/TMDS0_TX1_P	IFPA_TXD1_P	D23	=MCP_IFPA_TXD_P<1> (OUT) 9
67 9 OUT DP_IG_ML0_N<1>	E26	DP0_1_N/TMDS0_TX1_N	IFPA_TXD1_N	E23	=MCP_IFPA_TXD_N<1> (OUT) 9
67 9 OUT DP_IG_ML0_P<0>	H26	DP0_0_P/TMDS0_TX2_P	IFPA_TXD2_P	F23	=MCP_IFPA_TXD_P<2> (OUT) 9
67 9 OUT DP_IG_ML0_N<0>	G26	DP0_0_N/TMDS0_TX2_N	IFPA_TXD2_N	G23	=MCP_IFPA_TXD_N<2> (OUT) 9
9 OUT DP_IG_ML1_P<3>	F27	DP1_3_P/TMDS0B_TXC_P	IFPA_TXD3_P	H23	=MCP_IFPA_TXD_P<3> (OUT) 9
9 OUT DP_IG_ML1_N<3>	G27	DP1_3_N/TMDS0B_TXC_N	IFPA_TXD3_N	J23	=MCP_IFPA_TXD_N<3> (OUT) 9
9 OUT DP_IG_ML1_P<2>	E27	DP1_2_P/TMDS0_TX3_P	IFPB_TXC_P	J24	=MCP_IFPB_TXC_P (OUT) 9
9 OUT DP_IG_ML1_N<2>	D27	DP1_2_N/TMDS0_TX3_N	IFPB_TXC_N	H24	=MCP_IFPB_TXC_N (OUT) 9
67 9 OUT DP_IG_ML1_P<1>	C27	DP1_1_P/TMDS0_TX4_P	IFPB_TXD4_P	G24	=MCP_IFPB_TXD_P<0> (OUT) 9
67 9 OUT DP_IG_ML1_N<1>	B27	DP1_1_N/TMDS0_TX4_N	IFPB_TXD4_N	F24	=MCP_IFPB_TXD_N<0> (OUT) 9
67 9 OUT DP_IG_ML1_P<0>	A29	DP1_0_P/TMDS0_TX5_P	IFPB_TXD5_P	E24	=MCP_IFPB_TXD_P<1> (OUT) 9
67 9 OUT DP_IG_ML1_N<0>	B29	DP1_0_N/TMDS0_TX5_N	IFPB_TXD5_N	D24	=MCP_IFPB_TXD_N<1> (OUT) 9
			IFPB_TXD6_P	C24	=MCP_IFPB_TXD_P<2> (OUT) 9
			IFPB_TXD6_N	B24	=MCP_IFPB_TXD_N<2> (OUT) 9
9 IN DP_IG_HPD0	C29	HPLUG_DET0/GPIO_20	IFPB_TXD7_P	J26	=MCP_IFPB_TXD_P<3> (OUT) 9
9 IN DP_IG_HPD1	D30	HPLUG_DET1/GPIO_21	IFPB_TXD7_N	K26	=MCP_IFPB_TXD_N<3> (OUT) 9
17 OUT SATARDRVR_A_EN	E30	HPLUG_DET2/GPIO_22			
67 17 9 BI DP_IG_AUX_CH0_P	E29	DDC_CLK2/DP_AUX_CH0_P	DDC_CLK1/GPIO_40	J30	=MCP_IFPAB_DDC_CLK (OUT) 9
67 17 9 BI DP_IG_AUX_CH0_N	D29	DDC_DATA2/DP_AUX_CH0_N	DDC_DATA1/GPIO_41	H30	=MCP_IFPAB_DDC_DATA (BI) 9
67 17 9 BI DP_IG_AUX_CH1_P	G29	DDC_CLK3/DP_AUX_CH1_P			
67 17 9 BI DP_IG_AUX_CH1_N	F29	DDC_DATA3/DP_AUX_CH1_N			
23 PP3V3_S0_MCP_PLL_DP_USB 210 mA	L23	+3.3V_PLL_DP0	LCD_BKL_CTL/GPIO_57	B30	(GMUX_INT) LCD_IG_BKLT_PWM (OUT) 9
180 mA	M23	+3.3V_PLL_DP0	LCD_BKL_ON/GPIO_59	C30	LCD_IG_BKLT_EN (OUT) 9
30 mA	L22	+3.3V_PLL_USB	LCD_PANEL_PWR/GPIO_58	A30	LCD_IG_PWR_EN (OUT) 9 59
	M22	+3.3V_PLL_USB			
24 =PP1V05_S0_MCP_PLL_IFP 60 mA	L25	+VIO_PLL_IFPAB			
	M25	+VIO_PLL_IFPAB			
23 PP1V05_S0_MCP_PLL_CORE 160 mA	L26	+VIO_PLL_CORE_LEG			
40 mA	M26	+VIO_PLL_CORE_LEG			
	L27	+VIO_PLL_SPPLL0			
60 mA	M27	+VIO_PLL_SPPLL0			
	L28	+VIO_PLL_V	IFPAB_VPROBE	C21	MCP_IFPAB_VPROBE (OUT) 24 67
40 mA	M28	+VIO_PLL_V	IFPAB_RSET	B21	MCP_IFPAB_RSET (OUT) 24 67
	L24	+VIO_PLL_NV			
20 mA	M24	+VIO_PLL_NV			
24 =PP3V3R1V8_S0_MCP_IFP_VDD 180 mA CKPLUS_WAIVE=PwrTerm2Gnd	A23	+VDD_IFPA			
CKPLUS_WAIVE=PwrTerm2Gnd	A24	+VDD_IFPB			
24 8 =PP1V05_S0_MCP_DP0_VDD 160 mA	B26	+VIO_DP0			
	A27	+VIO_DP0	TMDS0_VPROBE	H29	MCP_TMDS0_VPROBE (OUT) 24 67
	A26	+VIO_DP0	TMDS0_RSET	K27	MCP_TMDS0_RSET (OUT) 24 67

NOTE: 100K pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
Connect +3.3V_RGBDAC pin to GND.

NOTE: No Composite/S-Video/Component Video support on MCP89

Interface Mode

MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

LVDS: Power +VDD_IFPx at 1.8V
TMDS: Power +VDD_IFPx at 3.3V

DDC Mode Pull-downs

NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.

R1710	100K	1	2	5%	1/20W	MF	201	DP_IG_AUX_CH0_P 9 17 67
R1711	100K	1	2	5%	1/20W	MF	201	DP_IG_AUX_CH0_N 9 17 67
R1712	100K	1	2	5%	1/20W	MF	201	DP_IG_AUX_CH1_P 9 17 67
R1713	100K	1	2	5%	1/20W	MF	201	DP_IG_AUX_CH1_N 9 17 67

GPIO Pull-Ups

=PP3V3_S0_MCP_GPIO 8 18 19

R1780	10K	1	2	5%	1/20W	MF	201	SATARDRVR_A_EN 17
R1781	10K	1	2	5%	1/20W	MF	201	AUD_IP_PERIPHERAL_DET 7 17 37
R1782	10K	1	2	5%	1/20W	MF	201	MIKEY_MIC_LOAD_DET 17

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: MCP Graphics

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D
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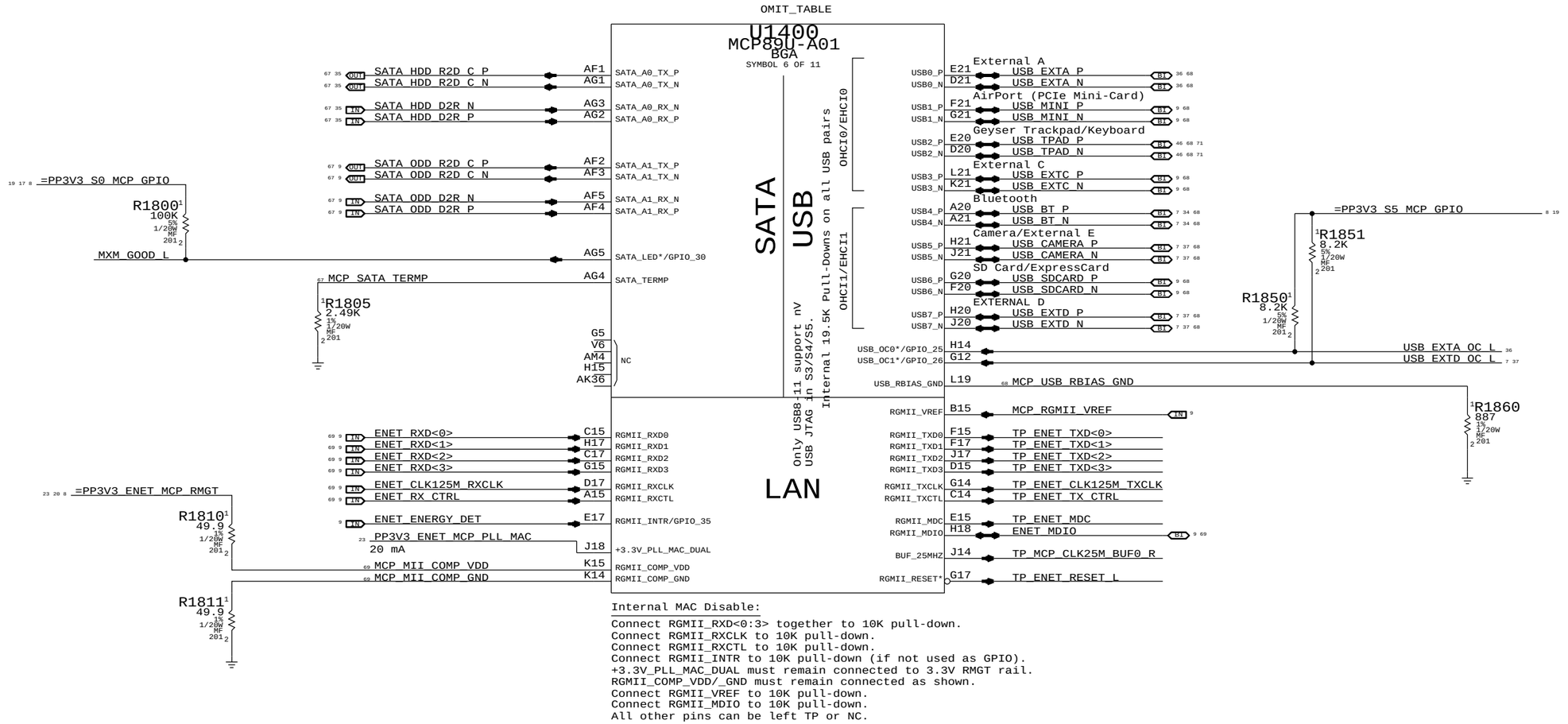

Internal MAC Disable:

Connect RGMII_RXD<0:3> together to 10K pull-down.
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
RGMII_COMP_VDD/_GND must remain connected as shown.
Connect RGMII_VREF to 10K pull-down.
Connect RGMII_MDIO to 10K pull-down.
All other pins can be left TP or NC.

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: MCP SATA, USB & Ethernet

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D
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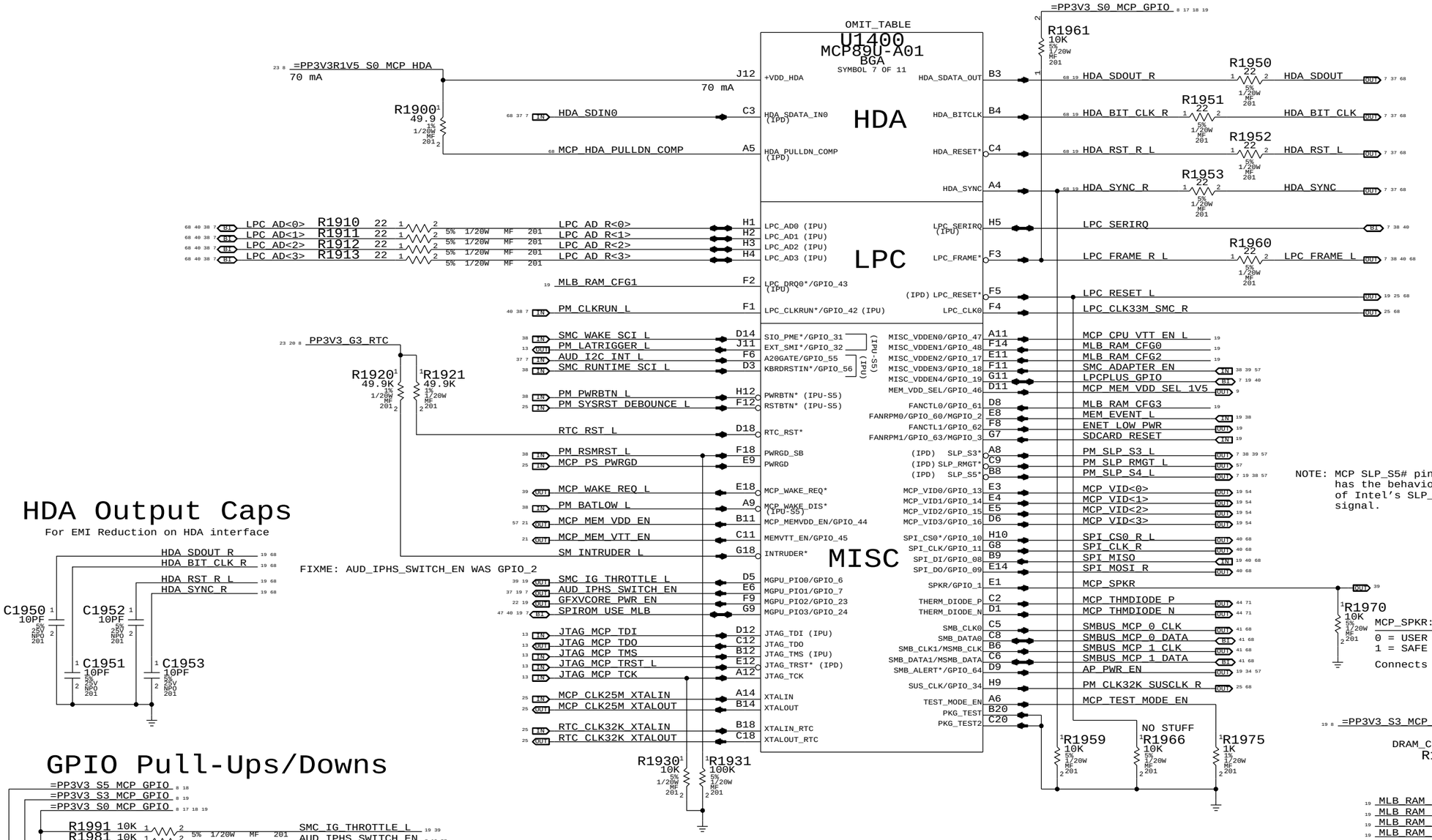

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: MCP HDA, LPC & MISC

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.

=PP1V05_SW_MCP_FSB
2000 mA

OMIT_TABLE
U1400
MCP89U-A01
BGA
SYMBOL 8 OF 11
POWER I

C32	+VTT_CPU	+VDD_MEM	AK19
E33	+VTT_CPU	+VDD_MEM	AJ23
L29	+VTT_CPU	+VDD_MEM	AJ24
AA29	+VTT_CPU	+VDD_MEM	AK21
E32	+VTT_CPU	+VDD_MEM	AJ17
AA30	+VTT_CPU	+VDD_MEM	AK15
L31	+VTT_CPU	+VDD_MEM	AK5
T30	+VTT_CPU	+VDD_MEM	AJ26
N30	+VTT_CPU	+VDD_MEM	AK13
M31	+VTT_CPU	+VDD_MEM	AK16
F33	+VTT_CPU	+VDD_MEM	AJ19
H33	+VTT_CPU	+VDD_MEM	AK12
J32	+VTT_CPU	+VDD_MEM	AK4
B33	+VTT_CPU	+VDD_MEM	AK26
G33	+VTT_CPU	+VDD_MEM	AK20
B32	+VTT_CPU	+VDD_MEM	AJ27
J33	+VTT_CPU	+VDD_MEM	AJ10
F32	+VTT_CPU	+VDD_MEM	AJ12
H32	+VTT_CPU	+VDD_MEM	AK17
G32	+VTT_CPU	+VDD_MEM	AK23
A33	+VTT_CPU	+VDD_MEM	AJ2
D32	+VTT_CPU	+VDD_MEM	AK3
AB30	+VTT_CPU	+VDD_MEM	AJ22
AB29	+VTT_CPU	+VDD_MEM	AJ21
C33	+VTT_CPU	+VDD_MEM	AK14
D33	+VTT_CPU	+VDD_MEM	AK22
A32	+VTT_CPU	+VDD_MEM	AK8
M29	+VTT_CPU	+VDD_MEM	AK27
M30	+VTT_CPU	+VDD_MEM	AJ4
R30	+VTT_CPU	+VDD_MEM	AK29
P30	+VTT_CPU	+VDD_MEM	AK18
L32	+VTT_CPU	+VDD_MEM	AK24
T29	+VTT_CPU	+VDD_MEM	AJ9
L30	+VTT_CPU	+VDD_MEM	AK11
U30	+VTT_CPU	+VDD_MEM	AK6
P29	+VTT_CPU	+VDD_MEM	AK2
R29	+VTT_CPU	+VDD_MEM	AK25
V30	+VTT_CPU	+VDD_MEM	AJ28
U29	+VTT_CPU	+VDD_MEM	AK9
V29	+VTT_CPU	+VDD_MEM	AK28
Y30	+VTT_CPU	+VDD_MEM	AJ11
Y29	+VTT_CPU	+VDD_MEM	AJ5
W29	+VTT_CPU	+VDD_MEM	AJ29
W30	+VTT_CPU	+VDD_MEM	AJ3
N29	+VTT_CPU	+VDD_MEM	AJ20
K31	+VTT_CPU	+VDD_MEM	AK10
		+VDD_MEM	AJ18
AC29	+VTT_CPU2	+VDD_MEM	AK1
AD29	+VTT_CPU2	+VDD_MEM	AJ1
AC30	+VTT_CPU2	+VDD_MEM	AJ7
AD30	+VTT_CPU2	+VDD_MEM	AJ8
AB31	+VTT_CPU2	+VDD_MEM	AJ25
AC31	+VTT_CPU2	+VDD_MEM	AJ16
AD31	+VTT_CPU2	+VDD_MEM	AJ15
AC32	+VTT_CPU2	+VDD_MEM	AK7
		+VDD_MEM	AJ6
V9	+3.3V_HVDD	+VDD_MEM	AJ13
V10	+3.3V	+VDD_MEM	AJ14
H11	+3.3V	+VDD_MEM	AL11
K29	+3.3V	+VDD_MEM	AL12
		+VDD_MEM	AL14
		+VDD_MEM	AL15
AU18	+VDD_DUAL_AUXC	+VDD_MEM	AL17
K18	+VDD_DUAL_AUXC	+VDD_MEM	AL18
		+VDD_MEM	AL20
A18	+3.3V_VBAT	+VDD_MEM	AL21
		+VDD_MEM	AL26
L20	+3.3V_DUAL_USB	+VDD_MEM	AL27
K20	+3.3V_DUAL_USB	+VDD_MEM	AL29
		+VDD_MEM	AL30
J15	+3.3V_DUAL		

=PP3V3_S0_MCP_HVDD
30 mA

=PP3V3_S0_MCP
250 mA

=PP0V9_S5_MCP_VDD_AUXC
150 mA

=PP3V3_G3_RTC
2? uA (G3)
5 mA (S0)

=PP3V3_S5_MCP
240 mA 40 mA

=PP1V05_S0_MCP_FSB
200 mA

=PP1V5R1V35_SW_MCP_MEM
4300 mA

K17	+VDD_DUAL_RMGT	=PP0V9_ENET_MCP_RMGT	8 23
L17	+VDD_DUAL_RMGT	140 mA	
A17	+3.3V_DUAL_RMGT	=PP3V3_ENET_MCP_RMGT	8 18 23
B17	+3.3V_DUAL_RMGT	300 mA	

=PPVCORE_S0_MCP
8450 mA (0.85V)

NOTE: VDD_COREx_SENSE signals should NOT be used for remote sensing unless COREA/COREB are powered by separate regulators.
Instead connect regulator sense point as close to COREB FET as possible.

OMIT_TABLE
U1400
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SYMBOL 9 OF 11
POWER II

N7	+VDD_COREA	+VDD_COREB	M9
N2	+VDD_COREA	+VDD_COREB	K2
N11	+VDD_COREA	+VDD_COREB	L7
R12	+VDD_COREA	+VDD_COREB	M7
P9	+VDD_COREA	+VDD_COREB	Y23
R8	+VDD_COREA	+VDD_COREB	M2
N4	+VDD_COREA	+VDD_COREB	AB23
R5	+VDD_COREA	+VDD_COREB	M11
R3	+VDD_COREA	+VDD_COREB	M12
P3	+VDD_COREA	+VDD_COREB	L8
P4	+VDD_COREA	+VDD_COREB	M8
P8	+VDD_COREA	+VDD_COREB	M10
R2	+VDD_COREA	+VDD_COREB	L10
P1	+VDD_COREA	+VDD_COREB	M6
R9	+VDD_COREA	+VDD_COREB	L12
N5	+VDD_COREA	+VDD_COREB	K10
N10	+VDD_COREA	+VDD_COREB	K7
P10	+VDD_COREA	+VDD_COREB	M1
R1	+VDD_COREA	+VDD_COREB	K8
P2	+VDD_COREA	+VDD_COREB	K5
R4	+VDD_COREA	+VDD_COREB	L9
N8	+VDD_COREA	+VDD_COREB	M3
R10	+VDD_COREA	+VDD_COREB	J4
P5	+VDD_COREA	+VDD_COREB	M4
AD24	+VDD_COREA	+VDD_COREB	L11
R7	+VDD_COREA	+VDD_COREB	L5
P6	+VDD_COREA	+VDD_COREB	J2
R6	+VDD_COREA	+VDD_COREB	J1
AB24	+VDD_COREA	+VDD_COREB	J7
AC24	+VDD_COREA	+VDD_COREB	M5
P11	+VDD_COREA	+VDD_COREB	L4
P12	+VDD_COREA	+VDD_COREB	L3
P7	+VDD_COREA	+VDD_COREB	J3
R11	+VDD_COREA	+VDD_COREB	K11
AD23	+VDD_COREA	+VDD_COREB	J6
Y24	+VDD_COREA	+VDD_COREB	L2
AA24	+VDD_COREA	+VDD_COREB	L1
N12	+VDD_COREA	+VDD_COREB	J5
AD17	+VDD_COREA	+VDD_COREB	L6
AD18	+VDD_COREA	+VDD_COREB	K4
AD19	+VDD_COREA	+VDD_COREB	V23
AD20	+VDD_COREA	+VDD_COREB	V17
AD21	+VDD_COREA	+VDD_COREB	V19
AD22	+VDD_COREA	+VDD_COREB	V18
U24	+VDD_COREA	+VDD_COREB	V20
V24	+VDD_COREA	+VDD_COREB	V21
W24	+VDD_COREA	+VDD_COREB	V22
T11	+VDD_COREA	+VDD_COREB	AB21
T12	+VDD_COREA	+VDD_COREB	Y17
U11	+VDD_COREA	+VDD_COREB	Y18
V11	+VDD_COREA	+VDD_COREB	Y19
		+VDD_COREB	Y20
U9	+VDD_COREA_SENSE	+VDD_COREB	Y21
U8	GND_COREA_SENSE	+VDD_COREB	Y22
		+VDD_COREB	AB22
AD8	+VIO_PE_DVDD	+VDD_COREB	AB17
AD6	+VIO_PE_DVDD	+VDD_COREB	AB18
AC8	+VIO_PE_DVDD	+VDD_COREB	AB19
AC9	+VIO_PE_DVDD	+VDD_COREB	AB20
AD9	+VIO_PE_DVDD	+VDD_COREB	L13
AC7	+VIO_PE_DVDD	+VDD_COREB	L14
AC10	+VIO_PE_DVDD	+VDD_COREB	M13
AD7	+VIO_PE_DVDD	+VDD_COREB	M14
AD11	+VIO_PE_DVDD		
AD10	+VIO_PE_DVDD		
AC11	+VIO_PE_DVDD		
AC12	+VIO_PE_DVDD		
AD12	+VIO_PE_DVDD		
AE12	+VIO_PE_DVDD		
AA10	+VIO_PE_AVDD		
U12	+VIO_PE_AVDD		
AB10	+VIO_PE_AVDD		
V12	+VIO_PE_AVDD		
W11	+VIO_PE_AVDD		
W12	+VIO_PE_AVDD		
Y11	+VIO_PE_AVDD		
Y12	+VIO_PE_AVDD		
AA11	+VIO_PE_AVDD		
AA12	+VIO_PE_AVDD		
AB11	+VIO_PE_AVDD		
AB12	+VIO_PE_AVDD		

TP_MCP_VDDCOREA_SENSEP
TP_MCP_VDDCOREA_SENSEN

=PP1V05_S0_MCP_PE_DVDD
400 MA
(PE0[5:0], PE1[1:0])

PP1V05_S0_MCP_PE_AVDD
1000 MA
(PE0[5:0], PE1[1:0])

J9	+VDD_COREB_SENSE	TP_MCP_VDDCOREB_SENSEP	
J8	GND_COREB_SENSE	TP_MCP_VDDCOREB_SENSEN	

AF6	+VIO_SATA_AVDD	PP1V05_S0_MCP_SATA_AVDD	
AG8	+VIO_SATA_AVDD	300 mA	
AF7	+VIO_SATA_AVDD		
AF8	+VIO_SATA_AVDD		
AG9	+VIO_SATA_AVDD		
AG6	+VIO_SATA_AVDD		
AF9	+VIO_SATA_AVDD		
AG7	+VIO_SATA_AVDD		
AD1	+VIO_SATA_DVDD	=PP1V05_S0_MCP_SATA_DVDD	8 23
AD2	+VIO_SATA_DVDD	100 mA	
AD3	+VIO_SATA_DVDD		
AD4	+VIO_SATA_DVDD		
AC3	+VIO_SATA_DVDD		
AC4	+VIO_SATA_DVDD		
AC5	+VIO_SATA_DVDD		
AD5	+VIO_SATA_DVDD		
AC6	+VIO_SATA_DVDD		
AC1	+VIO_SATA_DVDD		
AC2	+VIO_SATA_DVDD		

=PPVCORE_SW_MCP_GFX
15350 mA (0.85V)

OMIT_TABLE
U1400
MCP89U-A01
BGA
SYMBOL 10 OF 11
GND

AL34	GND	G13	GND
AT10		E10	
AE4		B10	
K37		AM32	
AL25		AU25	
T36		AY38	
T37		W4	
AB2		AU10	
AB4		D10	
C40		H31	
B5		AL31	
G4		U31	
AE8		AT31	
AW34		AH31	
AC20		AN25	
AE5		AC21	
W18		AA22	
AT16		AN16	
AB5		AE31	
N34		AU34	
AT2		AW19	
W20		G10	
AW16		B22	
D7		B19	
B2		B34	
G37		E22	
D16		AC18	
K39		K34	
G31		AL22	
B7		AP36	
L15		G34	
W19		P31	
Y10		U21	
AW2		H25	
AH7		B31	
B13		AU4	
AE37		AA19	
AV1		W8	
AN19		AT19	
AP10		AT13	
W33		AH2	
AB36		AP19	
K13		A38	
AU13		AT34	
AA23		AE39	
AA31		AA18	
Y31		AT25	
AE33		AW31	
AY3		U23	
N33		D22	
T2		W36	
B39		W39	
T4		W37	
AH37		AC23	
V31		AP22	
AU37		AN13	
AW5		AP31	
AU7		AU31	
AT7		AL19	
AN28		AL2	
D4		AA20	
AU19		E28	
AP25		AH34	
AU22		B28	
AW13		AV40	
T33		D28	
E7		H28	
AW7		G36	
H13		AE36	

OMIT_TABLE
U1400
MCP89U-A01
BGA
SYMBOL 11 OF 11
GND

B16	GND	B36	GND
E16		AB37	
AP16		AE2	
AL36		AL7	
G19		D13	
AA21		T39	
K16		AH4	
K28		AB7	
D25		AH36	
AL16		AC17	
AP4		AH5	
G25		AL33	
K25		AW10	
E31		W17	
G16		G39	
AP13		AB39	
U22		AH39	
AP28		AL5	
AT28		AW39	
H16		AN10	
AH33		AB8	
AT22		N39	
AL8		N36	
AA1		N37	
AP37		AE29	
W22		AW28	
H19		AU28	
A3		E19	
AH8		L16	
G28		K22	
R31		AW22	
AW25		T34	
AP39		AN22	
AB33		D31	
B25		AE30	
U10		T8	
W34		M16	
U19		M15	
K12		M17	
E34		M18	
AL28		M19	
AE34		M20	
AT39		M21	
AP5		AE7	
W21		W5	
D34		W7	
E25		AP2	
K36		AL10	
D19		AP34	
Y1		U18	
W23		T7	
AC22		W31	
H22		AL39	
H8		T31	
K19		N31	
G2		AA17	
E2		T10	
T5		K33	
AC19		E13	
AN31		AL13	
AL37		AP7	
AU16		U17	
AB34		W2	
U20		AK34	
G22		AK35	
AW36		H6	
AL4		H7	
C1		V7	
E39		V8	
D37		AM5	

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: MCP Power & Ground

Apple Inc.

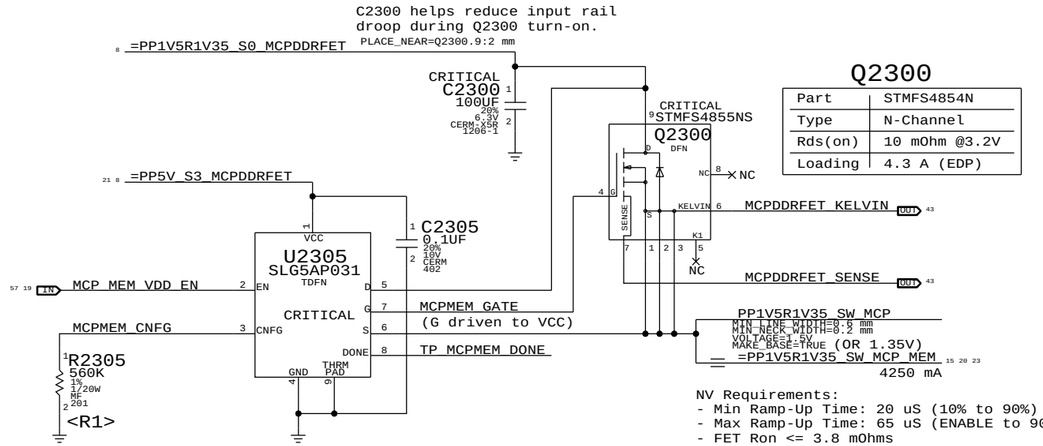
DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

BRANCH:

PAGE: 20 OF 110

SHEET: 20 OF 73



Q2300

Part	STMFS4854N
Type	N-Channel
Rds(on)	10 mOhm @3.2V
Loading	4.3 A (EDP)

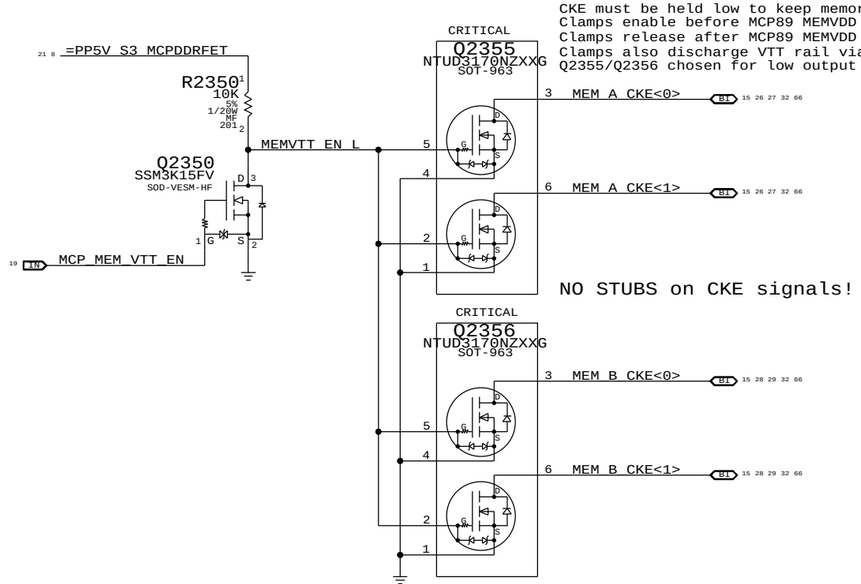
NV Requirements:
- Min Ramp-Up Time: 20 uS (10% to 90%)
- Max Ramp-Up Time: 65 uS (ENABLE to 90%)
- FET Ron <= 3.8 mOhms

NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.

Gated Rail Savings: 120mW

DIMM CKE Clamps

CKE must be held low to keep memory in self-refresh.
Clamps enable before MCP89 MEMVDD rail switched off.
Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.
Clamps also discharge VTT rail via termination resistor on each CKE signal on DIMM.
Q2355/Q2356 chosen for low output capacitance.



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2016

PAGE TITLE
MCP89 Memory Rail Gating

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D
REVISION 4.4.0
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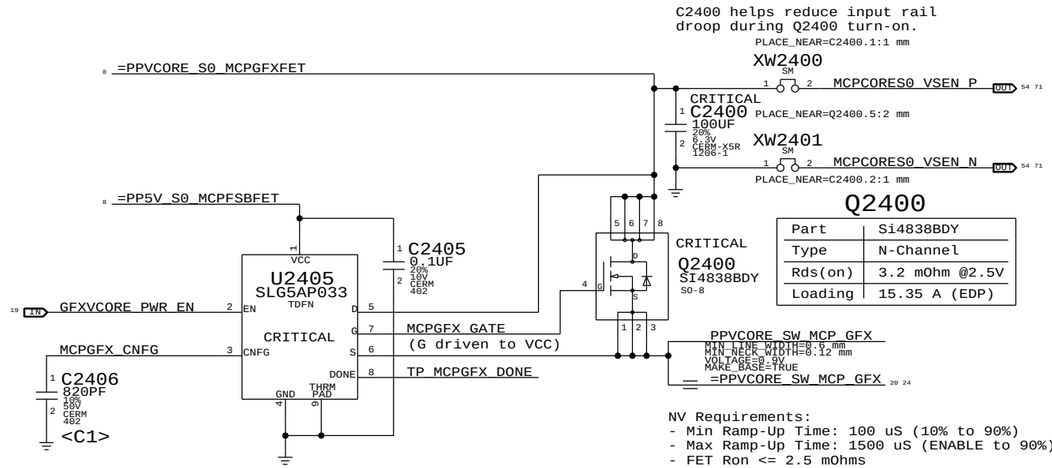

Approx. Ramp Time (EN to 1V, uS): 43.9 + 0.6943 * C1(pF)

Q2400

Part	Si4838BDY
Type	N-Channel
Rds(on)	3.2 mOhm @2.5V
Loading	15.35 A (EDP)

NV Requirements:
- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET Ron <= 2.5 mOhms

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

Gated Rail Savings: 860mW

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
MCP89 GFX Core Rail Gating

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D
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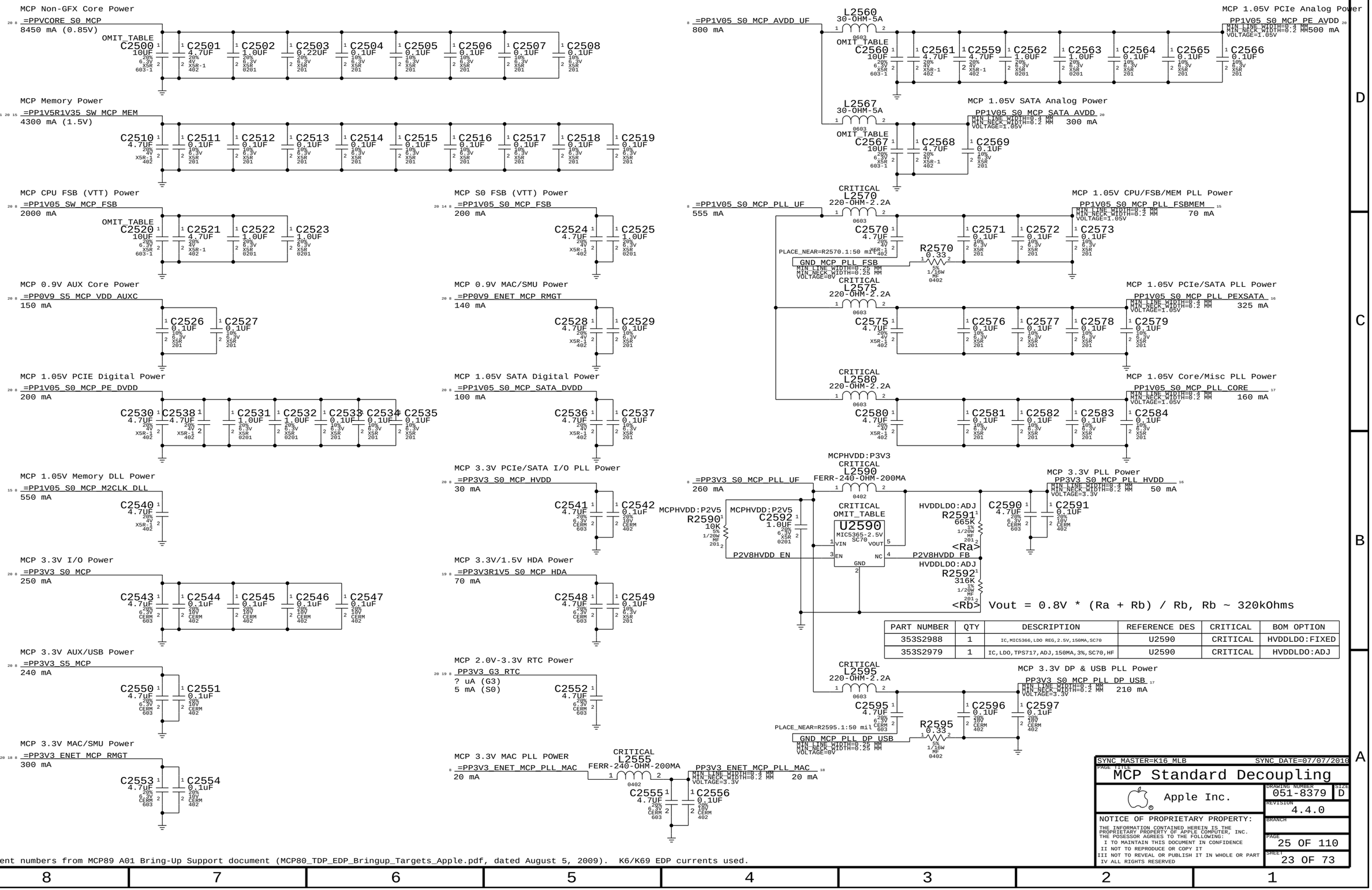
MCP Non-GFX Core Power
=PPVCORE_S0_MCP
8450 mA (0.85V)
OMIT_TABLE
C2500 10UF 20% 6.3V X5R 603-1
C2501 4.7UF 20% 4V X5R-1 402
C2502 1.0UF 20% 6.3V X5R 0201
C2503 0.22UF 20% 6.3V X5R 201
C2504 0.1UF 10% 6.3V X5R 201
C2505 0.1UF 10% 6.3V X5R 201
C2506 0.1UF 10% 6.3V X5R 201
C2507 0.1UF 10% 6.3V X5R 201
C2508 0.1UF 10% 6.3V X5R 201
MCP Memory Power
=PP1V5R1V35_SW_MCP_MEM
4300 mA (1.5V)
C2510 4.7UF 20% 4V X5R-1 402
C2511 0.1UF 10% 6.3V X5R 201
C2512 0.1UF 10% 6.3V X5R 201
C2513 0.1UF 10% 6.3V X5R 201
C2514 0.1UF 10% 6.3V X5R 201
C2515 0.1UF 10% 6.3V X5R 201
C2516 0.1UF 10% 6.3V X5R 201
C2517 0.1UF 10% 6.3V X5R 201
C2518 0.1UF 10% 6.3V X5R 201
C2519 0.1UF 10% 6.3V X5R 201
MCP CPU FSB (VTT) Power
=PP1V05_SW_MCP_FSB
2000 mA
OMIT_TABLE
C2520 10UF 20% 6.3V X5R 603-1
C2521 4.7UF 20% 4V X5R-1 402
C2522 1.0UF 20% 6.3V X5R 0201
C2523 1.0UF 20% 6.3V X5R 0201
MCP S0 FSB (VTT) Power
=PP1V05_S0_MCP_FSB
200 mA
C2524 4.7UF 20% 4V X5R-1 402
C2525 1.0UF 20% 6.3V X5R 0201
MCP 0.9V AUX Core Power
=PP0V9_S5_MCP_VDD_AUXC
150 mA
C2526 0.1UF 10% 6.3V X5R 201
C2527 0.1UF 10% 6.3V X5R 201
MCP 0.9V MAC/SMU Power
=PP0V9_ENET_MCP_RMGT
140 mA
C2528 4.7UF 20% 4V X5R-1 402
C2529 0.1UF 10% 6.3V X5R 201
MCP 1.05V PCIE Digital Power
=PP1V05_S0_MCP_PE_DVDD
200 mA
C2530 4.7UF 20% 4V X5R-1 402
C2538 4.7UF 20% 4V X5R-1 402
C2531 1.0UF 20% 6.3V X5R 0201
C2532 1.0UF 20% 6.3V X5R 0201
C2533 0.1UF 10% 6.3V X5R 201
C2534 0.1UF 10% 6.3V X5R 201
C2535 0.1UF 10% 6.3V X5R 201
MCP 1.05V SATA Digital Power
=PP1V05_S0_MCP_SATA_DVDD
100 mA
C2536 4.7UF 20% 4V X5R-1 402
C2537 0.1UF 10% 6.3V X5R 201
MCP 1.05V Memory DLL Power
=PP1V05_S0_MCP_M2CLK_DLL
550 mA
C2540 4.7UF 20% 4V X5R-1 402
MCP 3.3V PCIe/SATA I/O PLL Power
=PP3V3_S0_MCP_HVDD
30 mA
C2541 4.7UF 20% 6.3V CERM 603
C2542 0.1UF 20% 10V CERM 402
MCP 3.3V I/O Power
=PP3V3_S0_MCP
250 mA
C2543 4.7UF 20% 6.3V CERM 603
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
MCP 3.3V/1.5V HDA Power
=PP3V3R1V5_S0_MCP_HDA
70 mA
C2548 4.7UF 20% 6.3V CERM 603
C2549 0.1UF 10% 6.3V X5R 201
MCP 3.3V AUX/USB Power
=PP3V3_S5_MCP
240 mA
C2550 4.7UF 20% 6.3V CERM 603
C2551 0.1UF 20% 10V CERM 402
MCP 2.0V-3.3V RTC Power
=PP3V3_G3_RTC
? uA (G3)
5 mA (S0)
C2552 4.7UF 20% 6.3V CERM 603
MCP 3.3V MAC/SMU Power
=PP3V3_ENET_MCP_RMGT
300 mA
C2553 4.7UF 20% 6.3V CERM 603
C2554 0.1UF 20% 10V CERM 402
MCP 3.3V MAC PLL POWER
=PP3V3_ENET_MCP_PLL_MAC
20 mA
CRITICAL
L2555 FERR-240-OHM-200MA 0402
C2555 4.7UF 20% 6.3V CERM 603
C2556 0.1UF 20% 10V CERM 402
PP3V3_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
20 mA
MCP 1.05V PCIe Analog Power
=PP1V05_S0_MCP_AVDD_UF
800 mA
L2560 30-OHM-5A 0603
OMIT_TABLE
C2560 10UF 20% 6.3V X5R 603-1
C2561 4.7UF 20% 4V X5R-1 402
C2559 4.7UF 20% 4V X5R-1 402
C2562 1.0UF 20% 6.3V X5R 0201
C2563 1.0UF 20% 6.3V X5R 0201
C2564 0.1UF 10% 6.3V X5R 201
C2565 0.1UF 10% 6.3V X5R 201
C2566 0.1UF 10% 6.3V X5R 201
PP1V05_S0_MCP_PE_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
500 mA
MCP 1.05V SATA Analog Power
L2567 30-OHM-5A 0603
OMIT_TABLE
C2567 10UF 20% 6.3V X5R 603-1
C2568 4.7UF 20% 4V X5R-1 402
C2569 0.1UF 10% 6.3V X5R 201
PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
300 mA
MCP 1.05V CPU/FSB/MEM PLL Power
=PP1V05_S0_MCP_PLL_UF
555 mA
CRITICAL
L2570 220-OHM-2.2A 0603
C2570 4.7UF 20% 4V X5R-1 402
PLACE_NEAR=R2570.1:50 mil
GND_MCP_PLL_FSB
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=0V
R2570 0.33 5% 1/16W MF 0402
C2571 0.1UF 10% 6.3V X5R 201
C2572 0.1UF 10% 6.3V X5R 201
C2573 0.1UF 10% 6.3V X5R 201
PP1V05_S0_MCP_PLL_FSBMEM
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
70 mA
MCP 1.05V PCIe/SATA PLL Power
CRITICAL
L2575 220-OHM-2.2A 0603
C2575 4.7UF 20% 4V X5R-1 402
C2576 0.1UF 10% 6.3V X5R 201
C2577 0.1UF 10% 6.3V X5R 201
C2578 0.1UF 10% 6.3V X5R 201
C2579 0.1UF 10% 6.3V X5R 201
PP1V05_S0_MCP_PLL_PEXSATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
325 mA
MCP 1.05V Core/Misc PLL Power
CRITICAL
L2580 220-OHM-2.2A 0603
C2580 4.7UF 20% 4V X5R-1 402
C2581 0.1UF 10% 6.3V X5R 201
C2582 0.1UF 10% 6.3V X5R 201
C2583 0.1UF 10% 6.3V X5R 201
C2584 0.1UF 10% 6.3V X5R 201
PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
160 mA
MCP 3.3V PLL Power
MCPHVDD:P3V3
CRITICAL
L2590 FERR-240-OHM-200MA 0402
=PP3V3_S0_MCP_PLL_UF
260 mA
MCPHVDD:P2V5
R2590 10K 5% 1/20W MF 201
MCPHVDD:P2V5
C2592 1.0UF 20% 6.3V X5R 0201
P2V8HVDD_EN
CRITICAL
OMIT_TABLE
U2590 MIC5365-2.5V SC70
VIN VOUT EN NC GND
HVDDLDO:ADJ
R2591 665K 1% 1/20W MF 201
<Ra>
P2V8HVDD_FB
HVDDLDO:ADJ
R2592 316K 1% 1/20W MF 201
<Rb>
C2590 4.7UF 20% 6.3V CERM 603
C2591 0.1UF 20% 10V CERM 402
PP3V3_S0_MCP_PLL_HVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
50 mA
Vout = 0.8V * (Ra + Rb) / Rb, Rb ~ 320kOhms
PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION
353S2988 | 1 | IC,MIC5366,LDO REG,2.5V,150MA,SC70 | U2590 | CRITICAL | HVDDLDO:FIXED
353S2979 | 1 | IC,LDO,TPS717,ADJ,150MA,3%,SC70,HF | U2590 | CRITICAL | HVDDLDO:ADJ
MCP 3.3V DP & USB PLL Power
CRITICAL
L2595 220-OHM-2.2A 0603
C2595 4.7UF 20% 6.3V CERM 603
PLACE_NEAR=R2595.1:50 mil
GND_MCP_PLL_DP_USB
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=0V
R2595 0.33 5% 1/16W MF 0402
C2596 0.1UF 20% 10V CERM 402
C2597 0.1UF 20% 10V CERM 402
PP3V3_S0_MCP_PLL_DP_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
210 mA
Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.
SYNC_MASTER=K16_MLB
SYNC_DATE=07/07/2010
PAGE TITLE
MCP Standard Decoupling
Apple Inc.
DRAWING NUMBER 051-8379
SIZE D
REVISION 4.4.0
BRANCH
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MCP GFX Core Power

=PPVCORE_SW_MCP_GFX
15350 mA (0.85V)

OMIT_TABLE

C2600 10UF 20% 6.3V X5R 603-1
C2601 4.7UF 20% 4V X5R-1 402
C2602 1.0UF 20% 6.3V X6S 0201
C2603 1.0UF 20% 6.3V X6S 0201
C2604 0.22UF 20% 6.3V X5R 201
C2605 0.22UF 20% 6.3V X5R 201
C2606 0.1UF 10% 6.3V X5R 201
C2607 0.1UF 10% 6.3V X5R 201
C2608 0.1UF 10% 6.3V X5R 201
C2609 0.1UF 10% 6.3V X5R 201
C2610 0.1UF 10% 6.3V X5R 201
C2611 0.1UF 10% 6.3V X5R 201
C2612 0.1UF 10% 6.3V X5R 201

MCP 3.3V RGBDAC Power

GND_MCP_DAC_P3V3
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
MAKE_BASE=TRUE

R2670 0 5% 1/20W MF 201

PP3V3_S0_MCP_DAC
140 mA

If RGBDAC is used, requires ferrite (155S0382)
plus 1x 4.7uF 0603 & 1x 0.1uF 0402 cap.

If RGBDAC is not used, tie to GND.

=PP3V3R1V8_S0_MCP_IFP_VDD

=PP1V05_S0_MCP_PLL_IFP

MCP 1.05V DisplayPort Power

=PP1V05_S0_MCP_DP0_VDD
160 mA

C2640 4.7UF 20% 4V X5R-1 402
C2641 0.1UF 10% 6.3V X5R 201

MCP_TMDS0_RSET
MCP_TMDS0_VPROBE

NO STUFF
C2650 0.1UF 10% 6.3V X5R 201
R2650 1K 1% 1/20W MF 201

MCP_IFPAB_RSET
MCP_IFPAB_VPROBE

NO STUFF
C2655 0.1UF 10% 6.3V X5R 201
NO STUFF
R2655 1K 1% 1/20W MF 201

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
MCP Graphics Support

Apple Inc.

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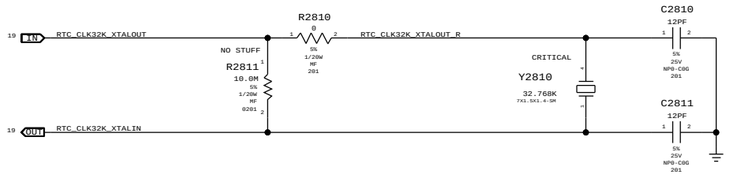
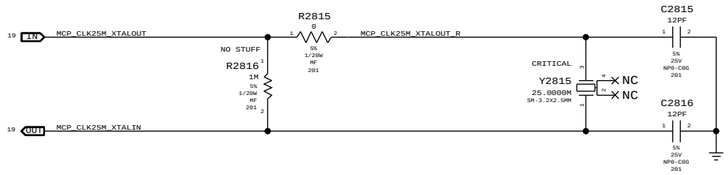
RTC Crystal

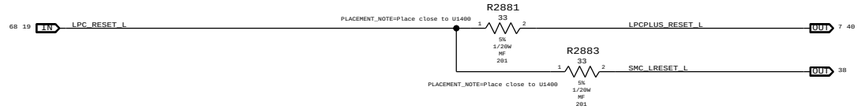


MCP 25MHz Crystal

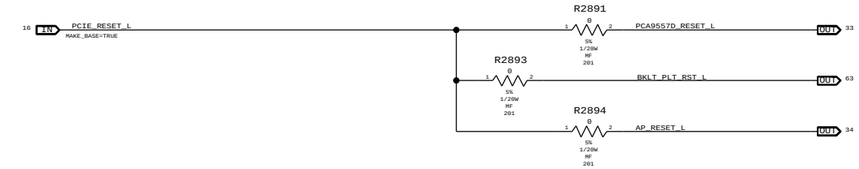


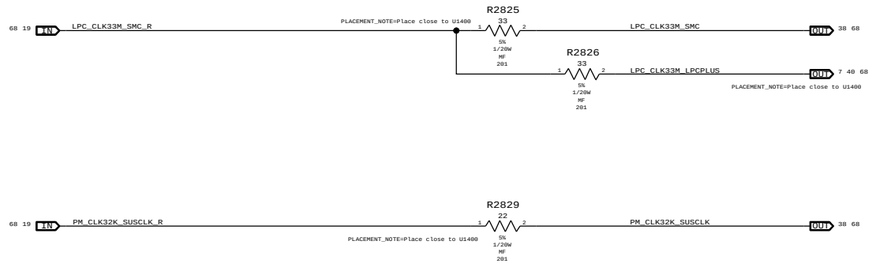
Platform Reset Connections

LPC Reset (Unbuffered)

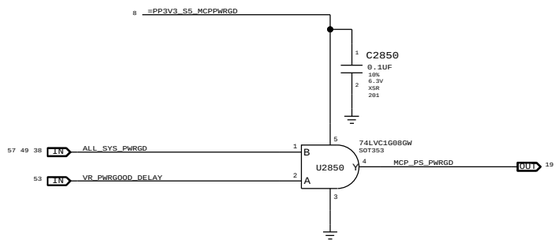


PCIE Reset (Unbuffered)

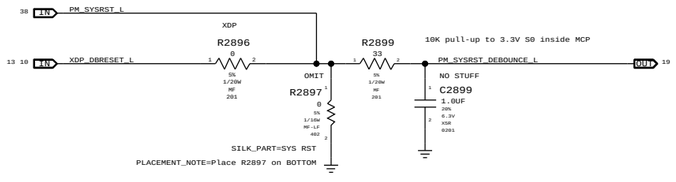




MCP S0 PWRGD & CPU_VLD



System Reset Circuit



SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE

SB Misc

Apple Inc.

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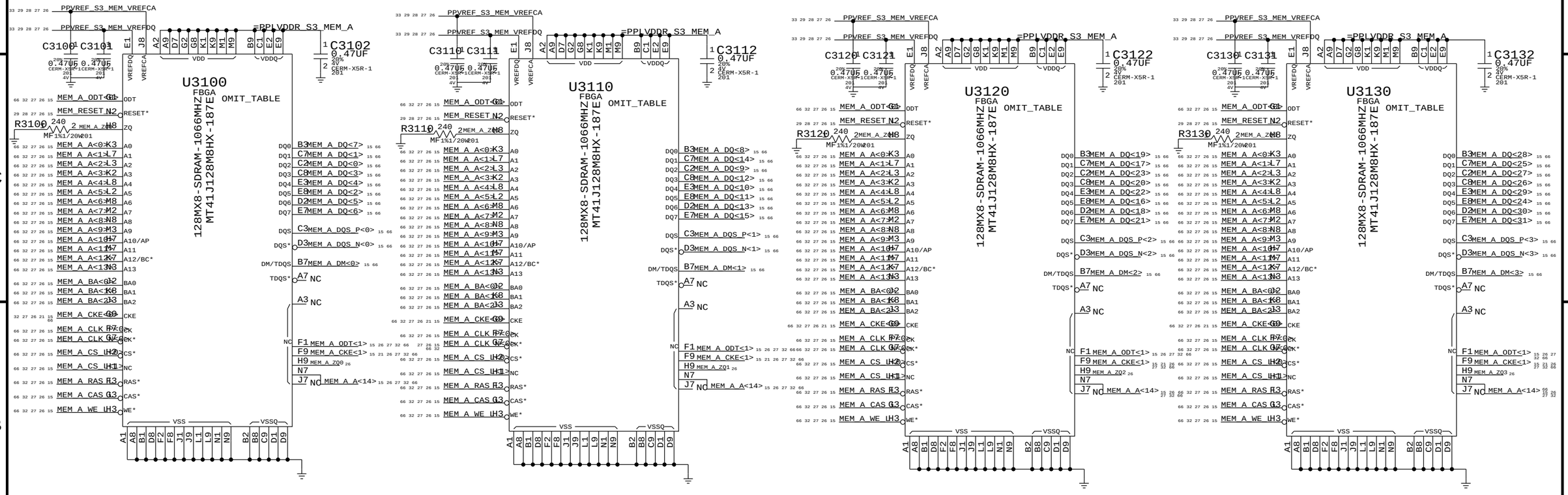

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
DDR3 DRAM Channel A (0-31)

Apple Inc.

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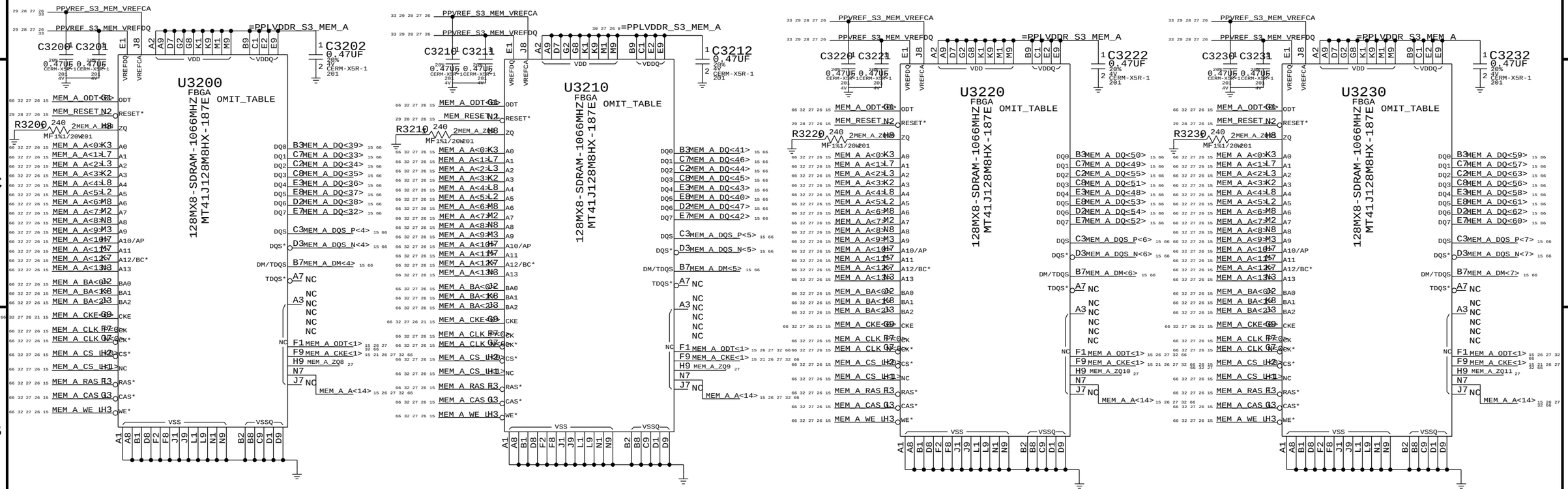

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
DDR3 DRAM Channel A (32-63)

Apple Inc.

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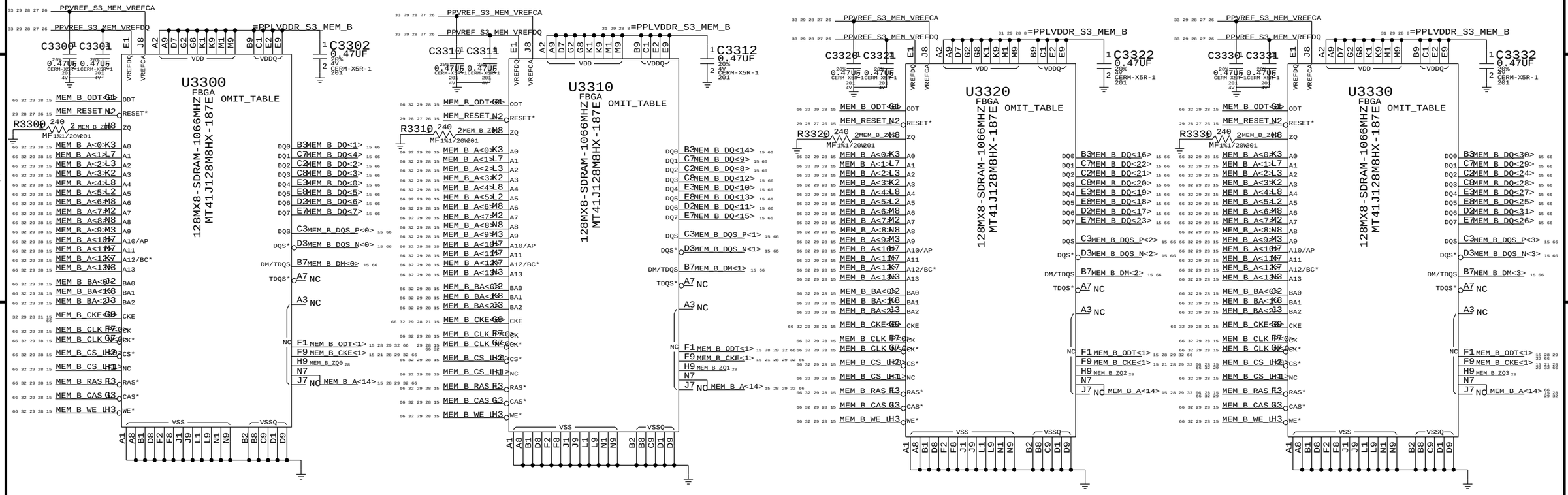

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
DDR3 DRAM Channel B (0-31)

Apple Inc.

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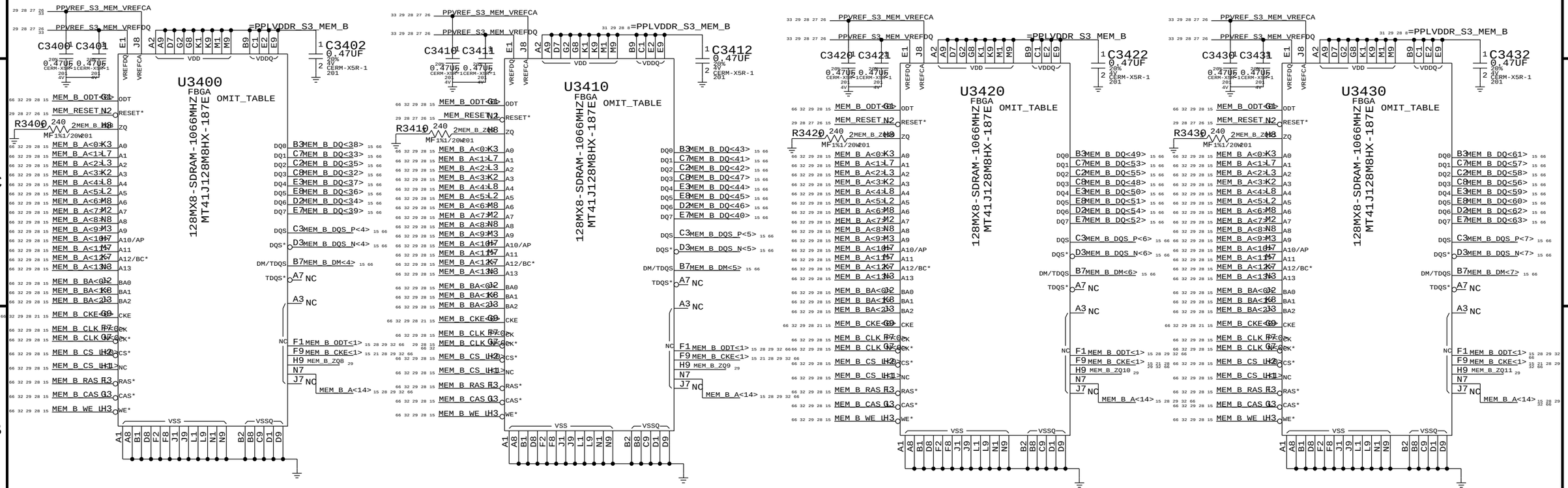

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
DDR3 DRAM Channel B (32-63)

Apple Inc.

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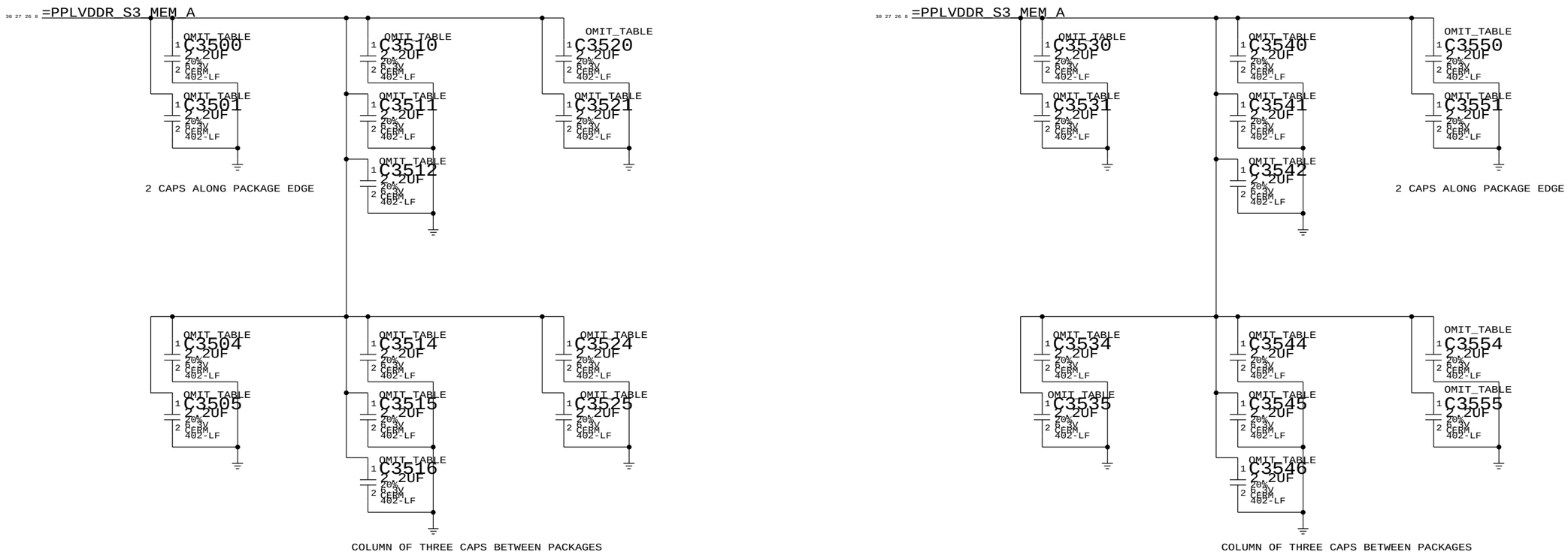

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

DDR BYPASSING 1

Apple Inc.

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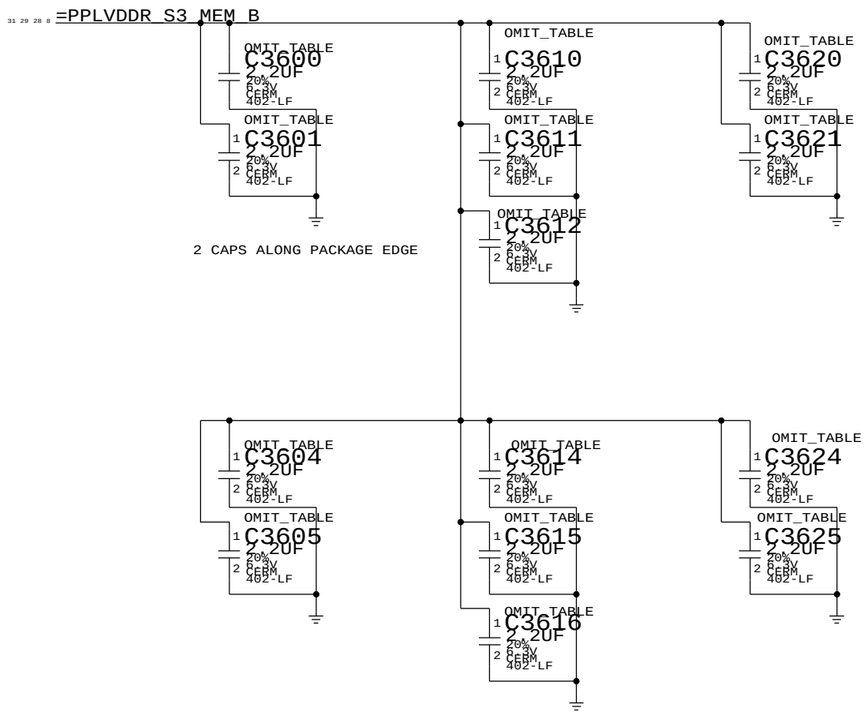

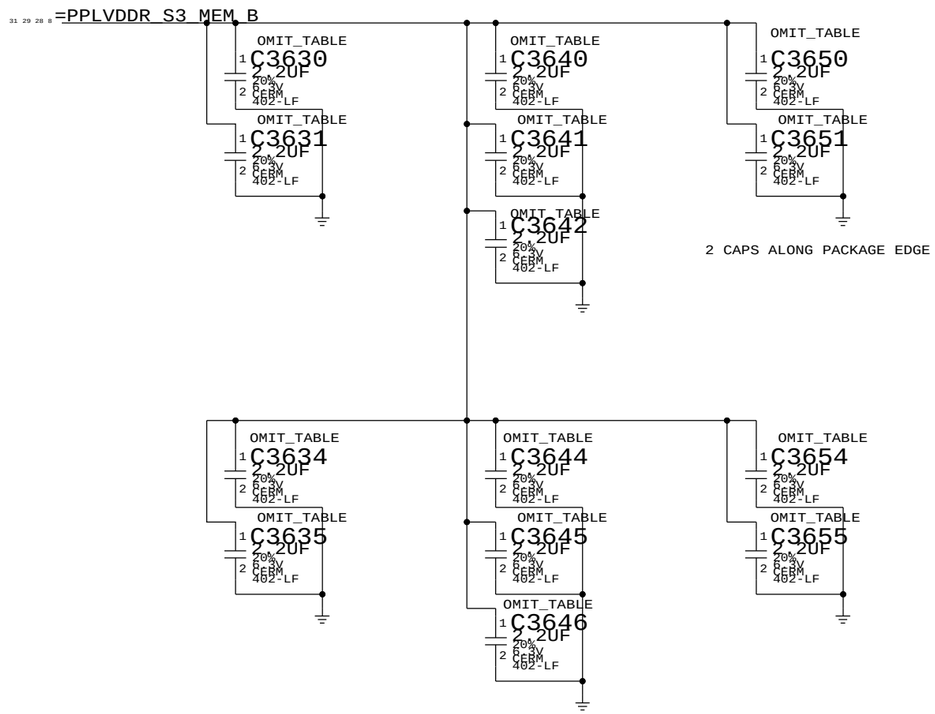

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

DDR BYPASSING 2

Apple Inc.

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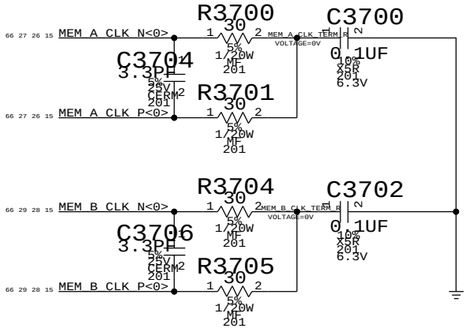
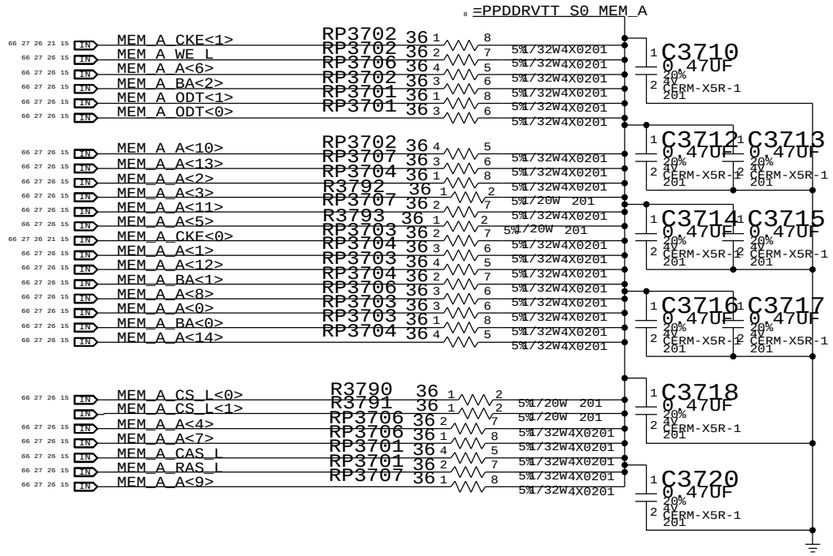
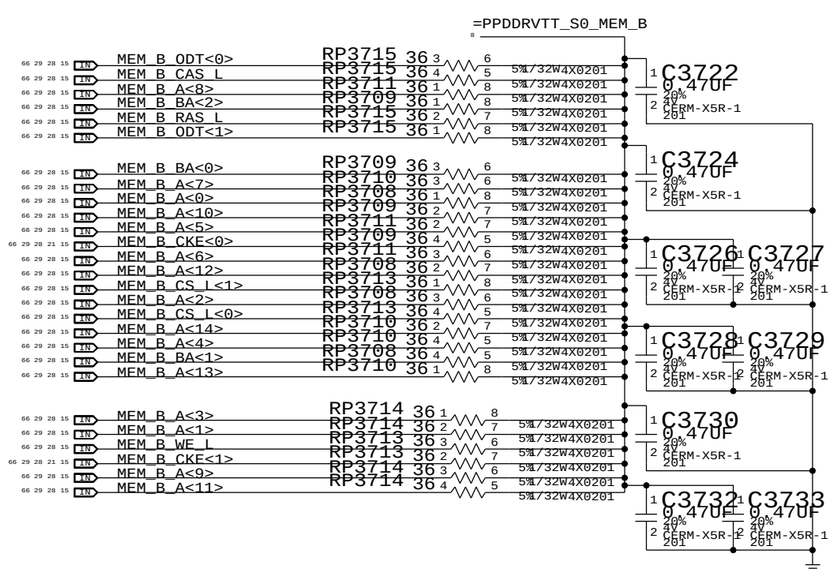
MEM CLOCK TERMINATION

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2016

PAGE TITLE
Memory Active Termination

Apple Inc.

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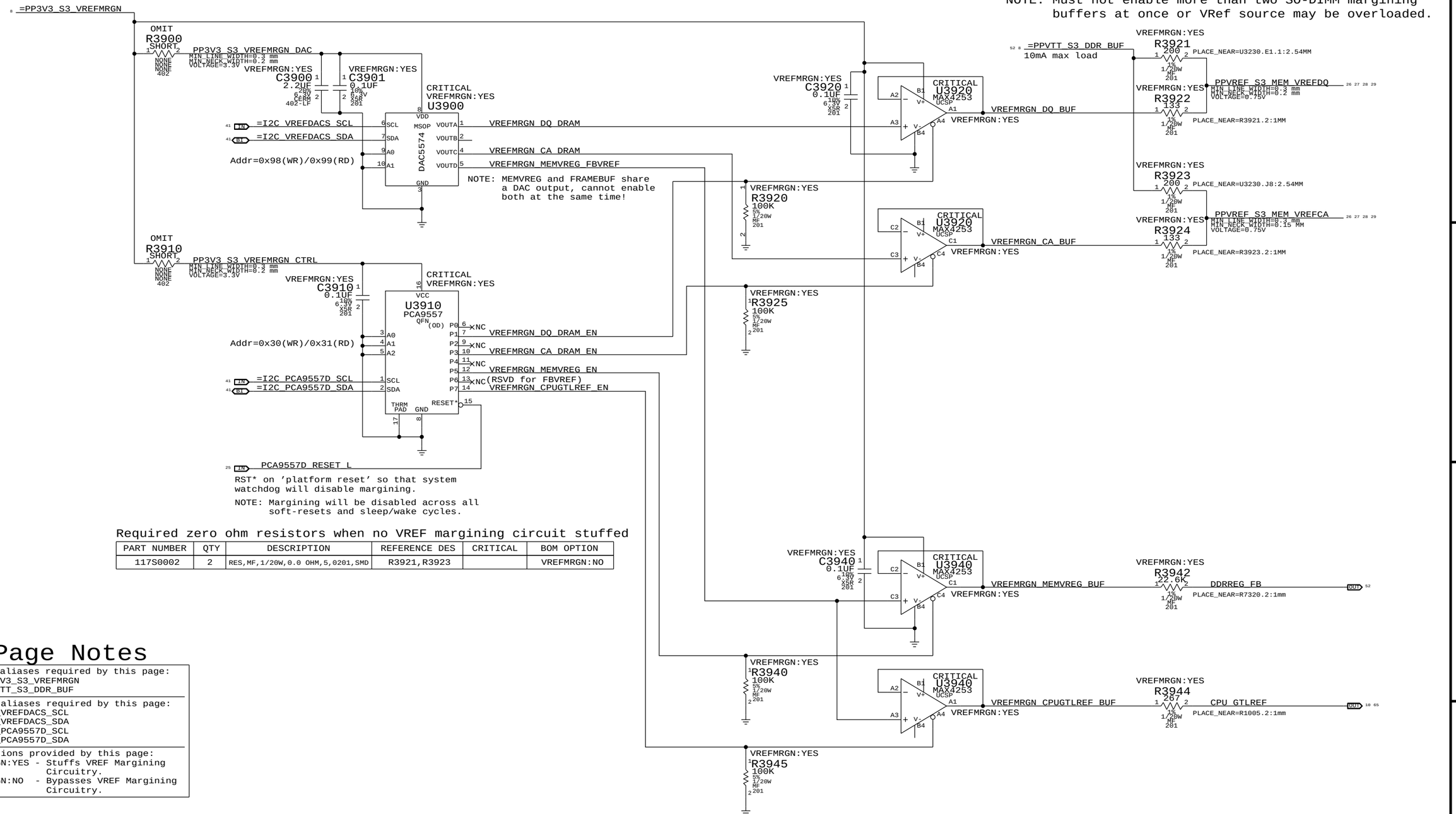

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3921,R3923		VREFMRGN:NO

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN:YES - Stuffs VREF Margining Circuitry.
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM VREF DQ	MEM VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	C	D	D
PCA9557D Pin:	1	3	5	7
Nominal value		0.75V (DAC: 0x3A)	1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)	1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
VRef current:		+3.4mA - -3.4mA (- = sourced)	+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output	8.59mV / step @ output	9.24mV / step @ output

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2016

PAGE TITLE: FSB/DDR3 Vref Margining

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AIRPORT

CRITICAL
J4001
SSD-K99
F-RT-SM1

514S0335

WIFI_EVENT_L
PCIE_AP_R2D_N
PCIE_AP_R2D_C_N
PCIE_AP_R2D_P
PCIE_AP_R2D_C_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N
PCIE_WAKE_L

C4030 0.1UF 10% 6.3V 201X5R
PLACEMENT_NOTE=Place close to J4001.

C4031 0.1UF 10% 6.3V X5R 201
PLACEMENT_NOTE=Place close to J4001.

BLUETOOTH

USB_BT_N
USB_BT_P

=PP3V3_S3_BT

C4032 0.1UF 10% 6.3V 25R 201
PLACE_NEAR=J4001.27:1.5mm

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)

CRITICAL
R4052 0.020 1% 0.25W MF 805
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
=PP3V3_WLAN_F
=PP3V3_WLAN_R

CRITICAL
Q4050 TPCP8102 23V1K-SM

C4021 0.1UF 10% 6.3V X5R 201
C4020 10UF 20% 10V X5R 805
PLACEMENT_NOTE=Place close to Q4050.

C4050 0.1UF 10% 10V X5R 402
C4051 0.033UF 10% 16V X5R 402
R4050 100K 5% 1/20W MF 201
R4051 10K 5% 1/20W MF 201
P3V3WLAN_SS
=PP3V3_S3_WLAN
PM_WLAN_EN_L

ISNS_AIRPORT_P
ISNS_AIRPORT_N

DLY = 60 MS +/- 20%

C4053 0.1UF 10% 6.3V X5R 201

CRITICAL
U4002
SLG4AP016V
TDFN
VDD
SENSE
0.7V
DLY
RESET*
MR*
EN
IN
OUT (OD)
THRM PAD
GND

R4053 100K 1% 1/20W MF 201
R4054 232K 1% 1/20W MF 201
P3V3WLAN_VMON
AP_RESET_CONN_L
AP_CLKREQ_Q_L

R4055 100K 1% 1/20W MF 201

AP_RESET_L
AP_PWR_EN
AP_CLKREQ_L

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
X21 WIRELESS CONNECTOR

Apple Inc.

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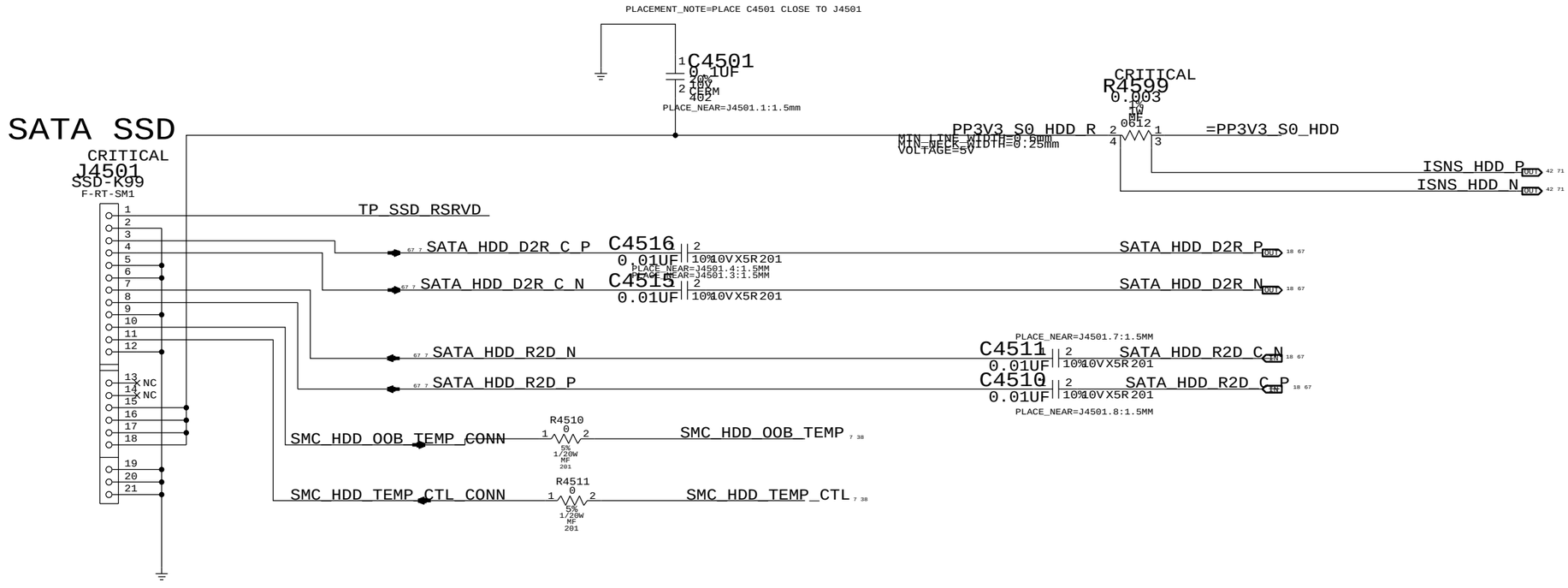

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

SATA CONNECTOR

Apple Inc.

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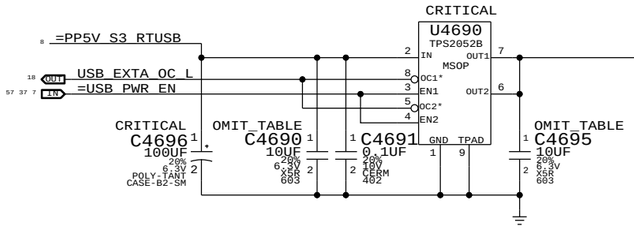
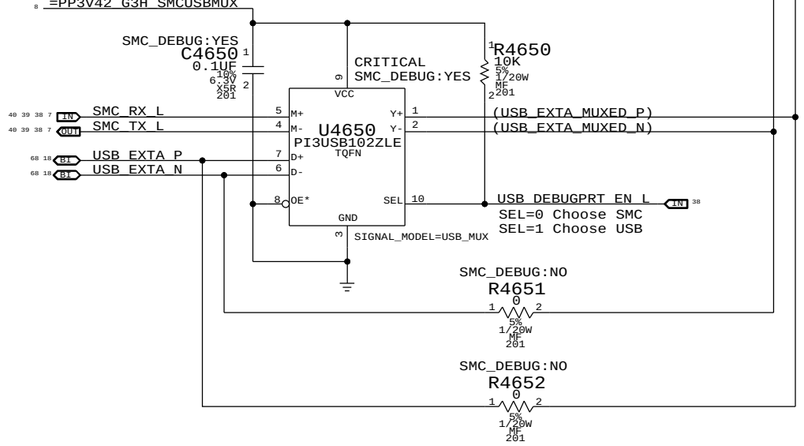
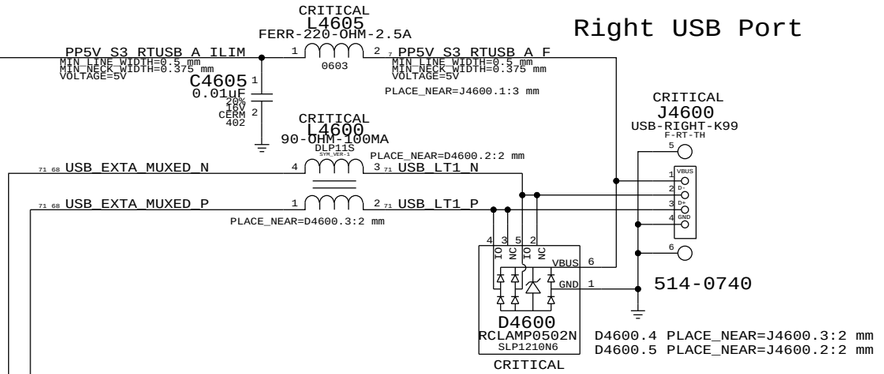
Port Power Switch



USB/SMC Debug Mux



Right USB Port



SYNC_MASTER=K16_MLB	SYNC_DATE=07/07/2010
PAGE TITLE	External USB Connectors
Apple Inc.	DRAWING NUMBER 051-8379 · SIZE D
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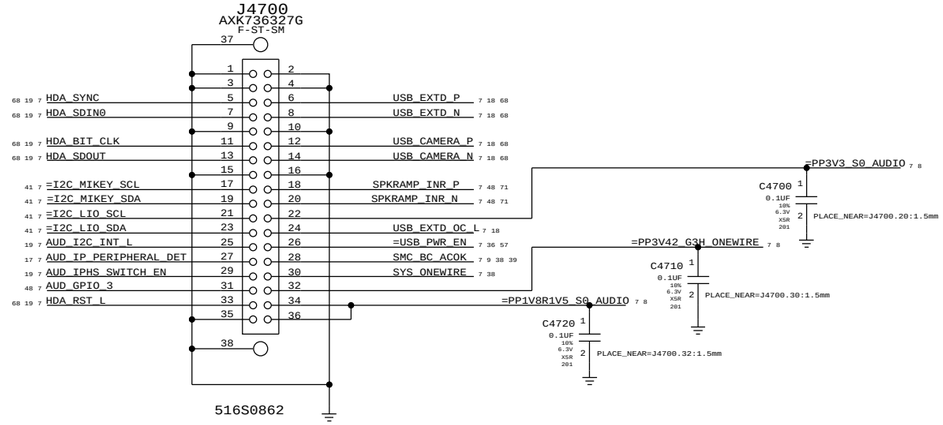
LIO CONNECTOR



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
LIO CONNECTORS

Apple Inc.

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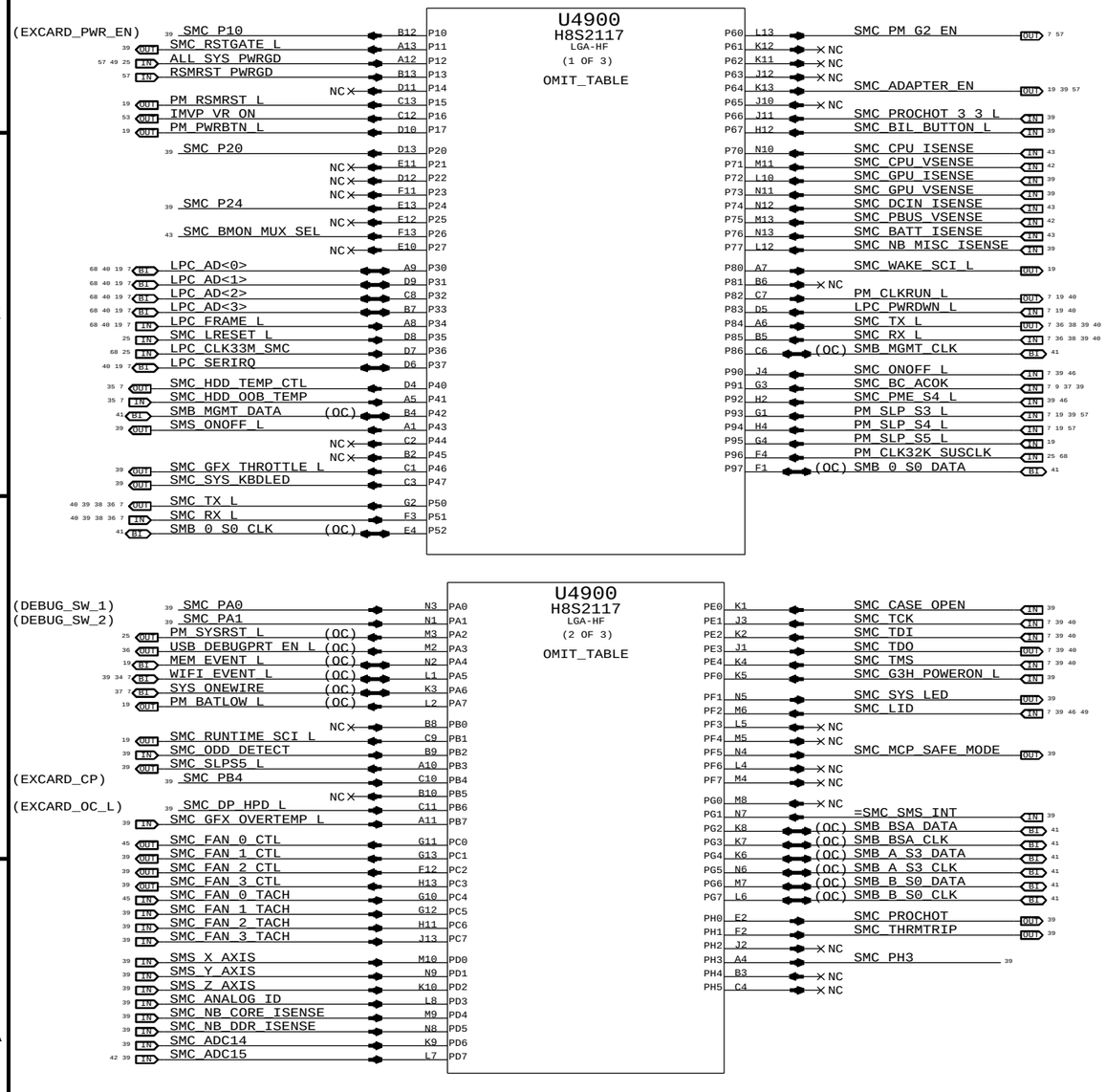
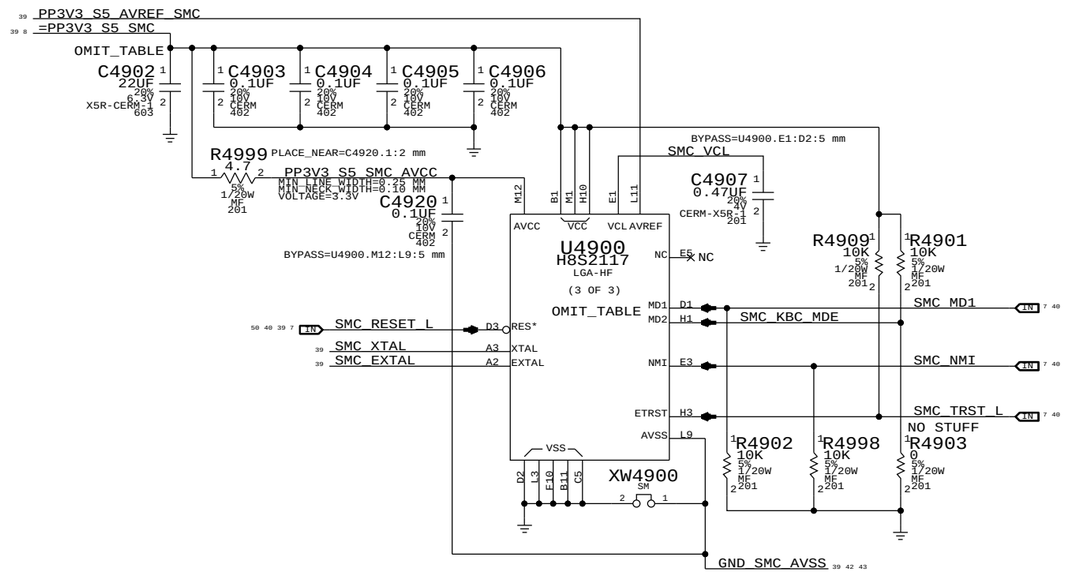
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

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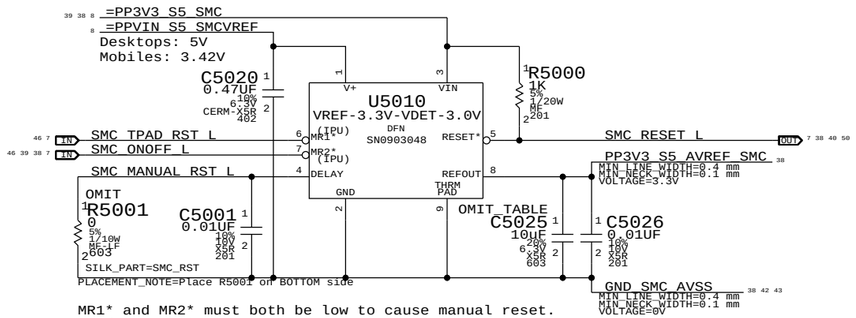
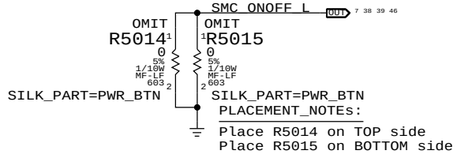
SMC Reset "Button", Supervisor & AVREF Supply



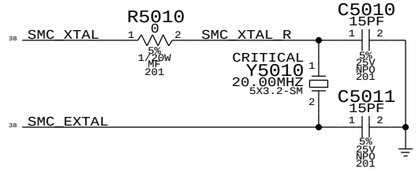
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

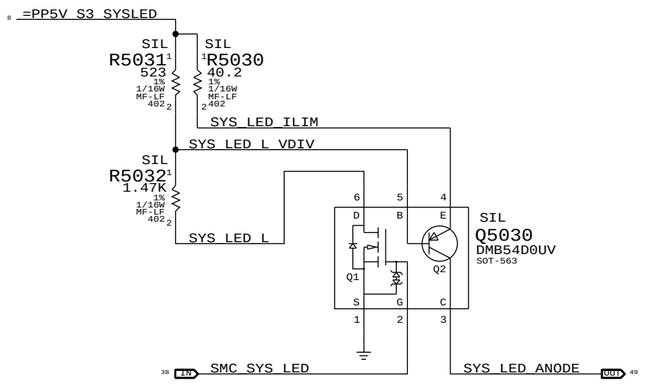
Debug Power "Buttons"



SMC Crystal Circuit



System (Sleep) LED Circuit



SMC Aliases

SMC_LCDBKLT_ISENSE	MAKE_BASE=TRUE	SMS_X_AXIS
SMC_WLAN_ISENSE	MAKE_BASE=TRUE	SMS_Y_AXIS
SMC_HDD_ISENSE	MAKE_BASE=TRUE	SMS_Z_AXIS
SMC_CSREG_ISENSE	MAKE_BASE=TRUE	SMC_ADC14
SMC_LCDBKLT_VSENSE	MAKE_BASE=TRUE	SMC_ADC15
SMC_MCP_CORE_ISENSE	MAKE_BASE=TRUE	SMC_NB_CORE_ISENSE
SMC_MCP_DDR_ISENSE	MAKE_BASE=TRUE	SMC_NB_DDR_ISENSE
SMC_1V5S3_ISENSE	MAKE_BASE=TRUE	SMC_NB_MISC_ISENSE
TP_SMC_ANALOG_ID	MAKE_BASE=TRUE	SMC_ANALOG_ID
TP_SMC_GPU_ISENSE	MAKE_BASE=TRUE	SMC_GPU_ISENSE
SMC_MCP_VSENSE	MAKE_BASE=TRUE	SMC_GPU_VSENSE
SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	SMC_IG_THROTTLE_L
SMS_INT_L	MAKE_BASE=TRUE	=SMC_SMS_INT
MCP_WAKE_REQ_L	MAKE_BASE=TRUE	SMC_G3H_POWERON_L

R5096 0
SMC_MCP_SAFE_MODE — MCP_SPKR

DP_PWR:S0
R5020 0
PM_SLP_S3_L — DP_PWR_EN (MAKE_BASE=TRUE) =DP_PWR_EN

DP_PWR:SMC
R5021 0
SMC_SLPS5_L

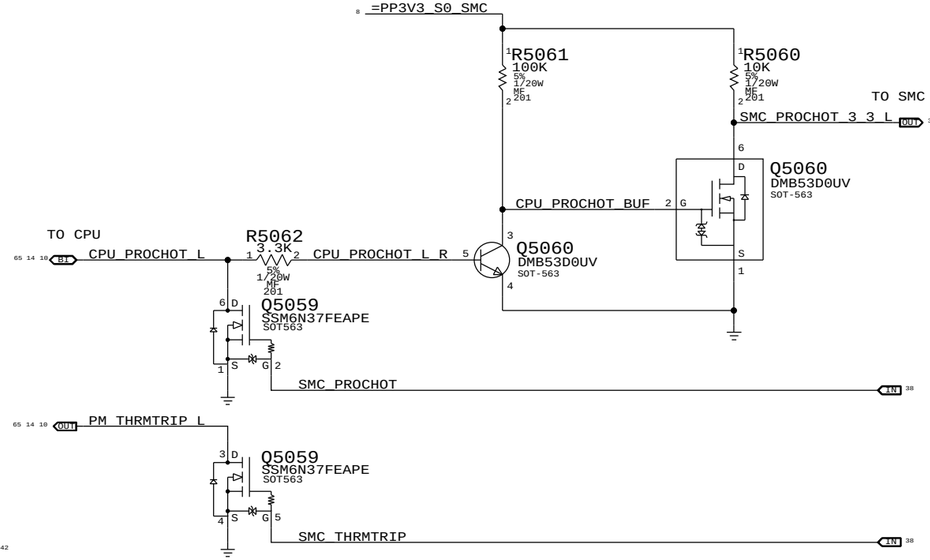
DP_PWR:SMC
R5022 0
SMC_DP_HPD_L — DP_EXT_HPD_L
PLACE_NEAR=Q9441.2:5 mm

Unused Pins

SMS_ONOFF_L	TP_SMS_ONOFF_L
SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED
SMC_FAN_1_CTL	TP_SMC_FAN_1_CTL
TP_SMC_FAN_1_TACH	SMC_FAN_1_TACH
SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL
NC_SMC_FAN_2_TACH	SMC_FAN_2_TACH
SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL
NC_SMC_FAN_3_TACH	SMC_FAN_3_TACH
SMC_RSTGATE_L	TP_SMC_RSTGATE_L
SMC_P10	TP_SMC_P10
SMC_P20	TP_SMC_P20
SMC_P24	TP_SMC_P24
SMC_PH3	TP_SMC_PH3

(MAKE_BASE=TRUE; NO_TEST=TRUE where noted)

SMC FSB to 3.3V Level Shifting



SMC Pull-ups

SMC_PA0	R5091	100K
SMC_PA1	R5092	100K
SMC_PB4	R5088	10K
SMC_ONOFF_L	R5070	10K
SMC_LID	R5071	100K
SMC_TX_L	R5073	10K
SMC_RX_L	R5074	100K
SMC_TMS	R5077	10K
SMC_TDO	R5078	10K
SMC_TDI	R5079	10K
SMC_TCK	R5080	10K
SMC_ODD_DETECT	R5040	10K
SMC_BIL_BUTTON_L	R5081	10K
SMC_BC_ACOK	R5087	470K
SMC_GFX_OVERTEMP_L	R5094	10K
SMC_G3H_POWERON_L	R5098	100K
SMS_INT_L	R5093	10K

(5% 1/20W MF 201)

PP3V3_WLAN_F
NO STUFF
WIFI_EVENT_L — R5089 10K

=PP3V3_SMC_PME
SMC_PME_S4_L — R5076 100K

SMC Pull-downs

SMC_ADAPTER_EN	R5085	10K
SMC_CASE_OPEN	R5086	10K
SMC_DP_HPD_L	R5090	100K

(5% 1/20W MF 201)

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: SMC Support

Apple Inc.

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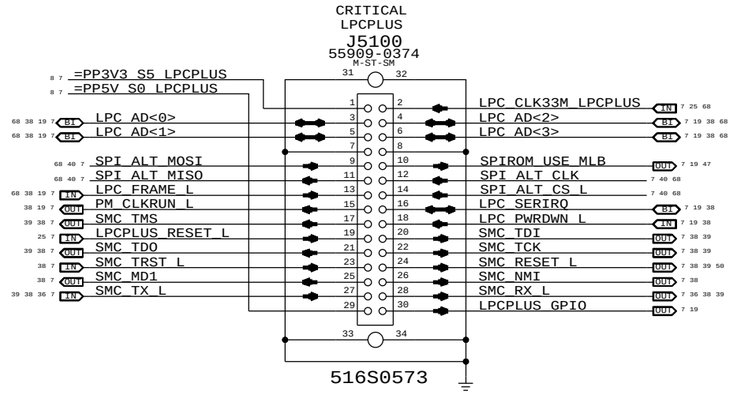
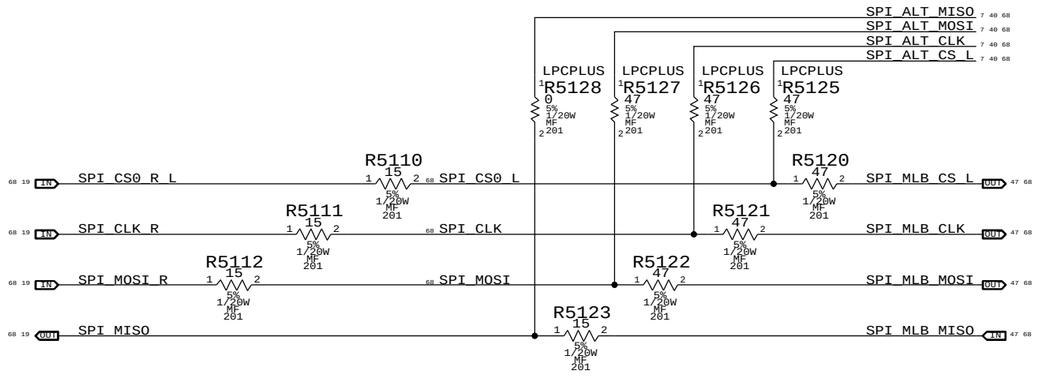
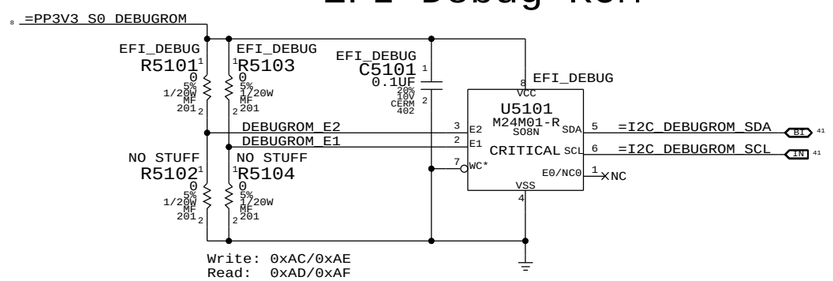
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: LPC+SPI Debug Connector

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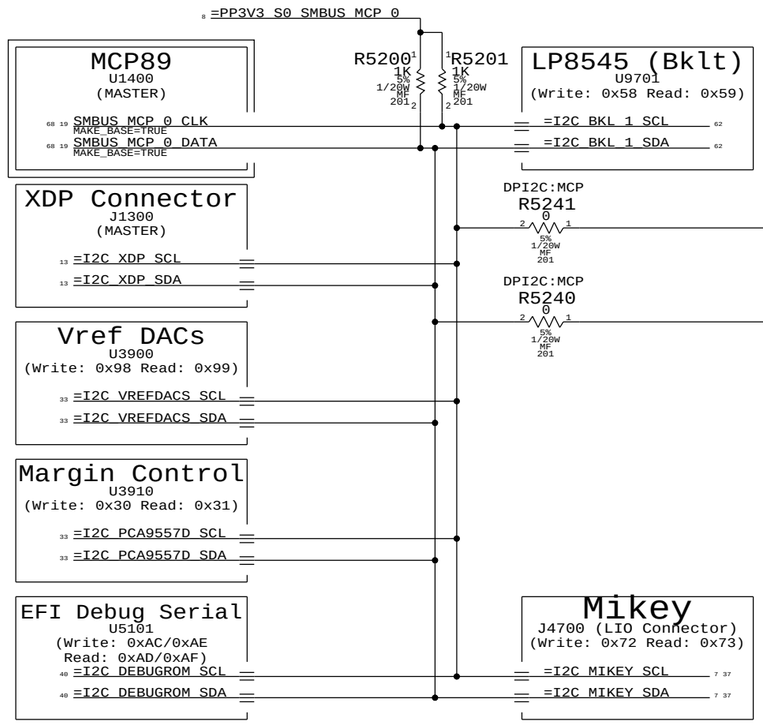
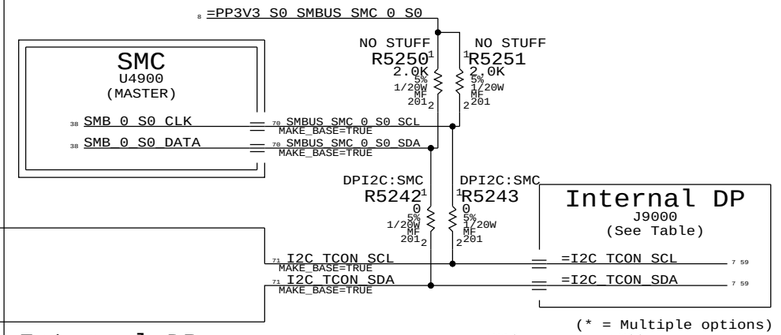
MCP89 SMBus "0" Connections



SMC "0" SMBus Connections



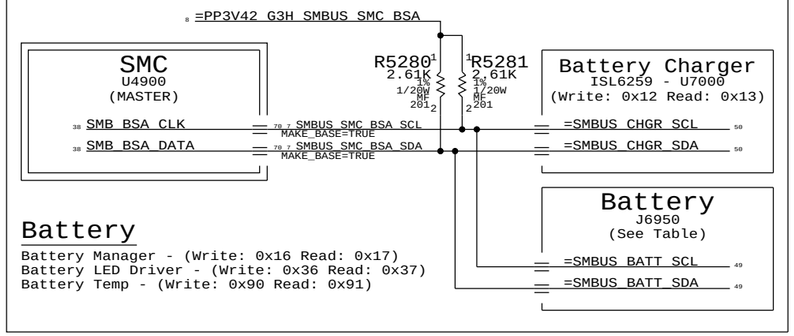
Internal DP

Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)
Parade T-con - (0x10-0x1F or 0x30-0x3F)
DVR - (Write: 0x4E Read: 0x4F)

(* = Multiple options)

K16		K99		
Samsung	LGD	Samsung	LGD	AUO
N	Y	*	Y	*
Y	N	*	N	*
Y	Y	Y	Y	N

SMC "Battery A" SMBus Connections

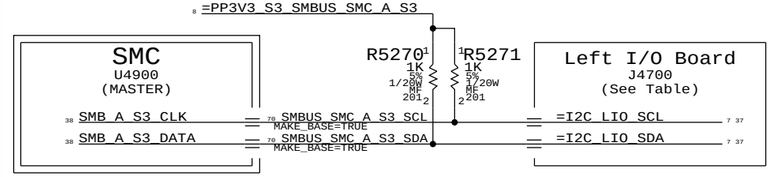


Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

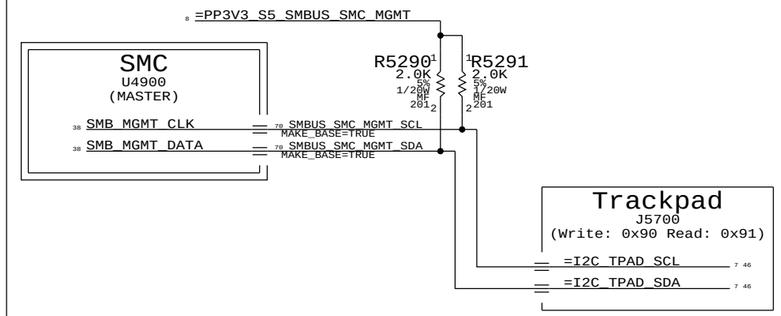


Left I/O Board

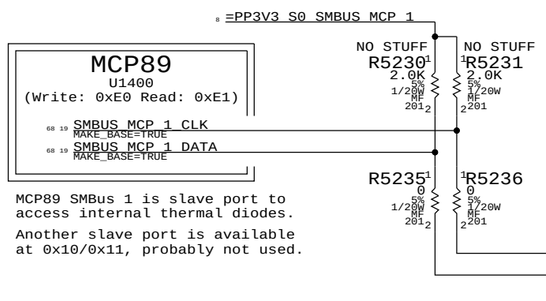
ALS - N/A (Feature Removed)
Finstack Temp - (Write: 0x98 Read: 0x99)

SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



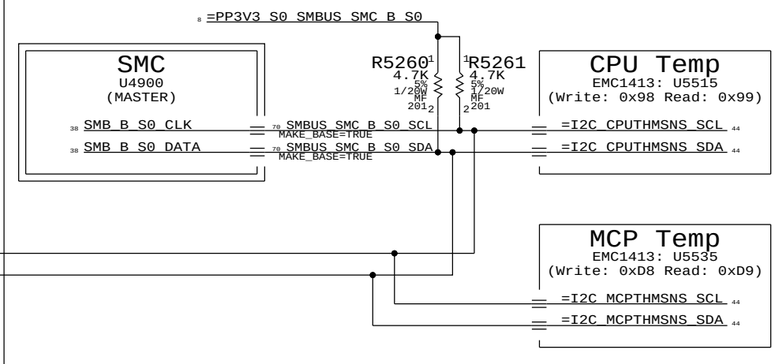
MCP89 SMBus "1" Connections



MCP89 SMBus 1 is slave port to access internal thermal diodes.

Another slave port is available at 0x10/0x11, probably not used.

SMC "B" SMBus Connections



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
K16/K99 SMus Connections

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D
REVISION 4.4.0
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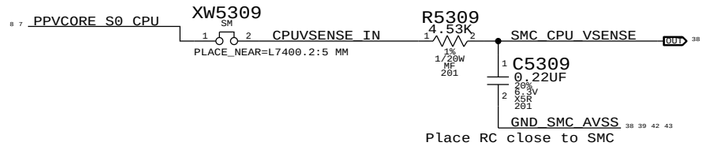
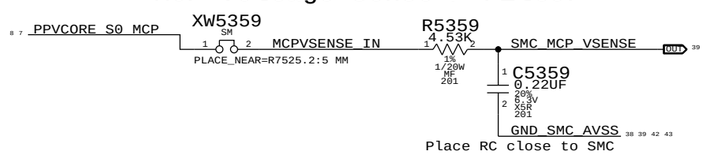
CPU Voltage Sense / Filter



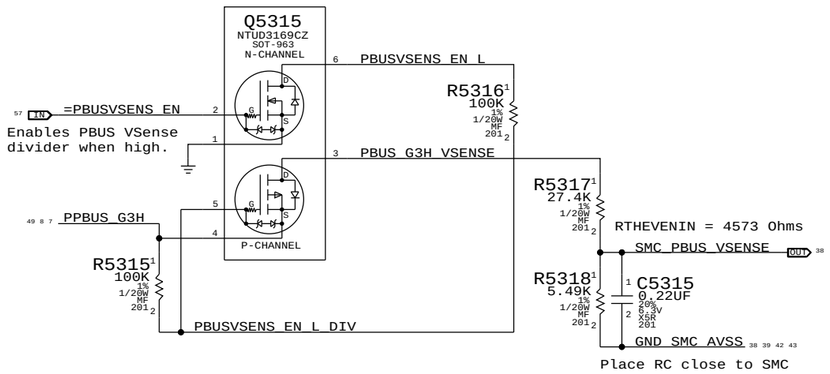
Place RC close to SMC

MCP Voltage Sense / Filter

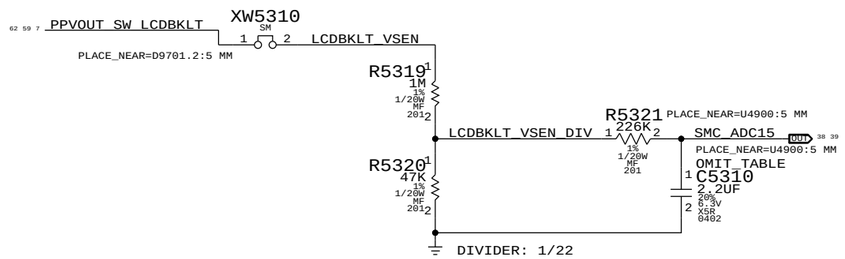


Place RC close to SMC

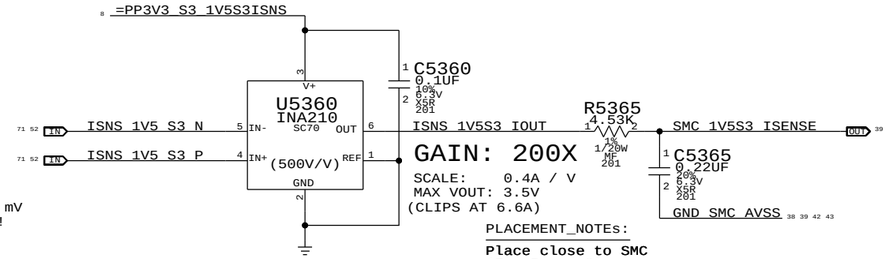
PBUS Voltage Sense Enable & Filter



Place RC close to SMC



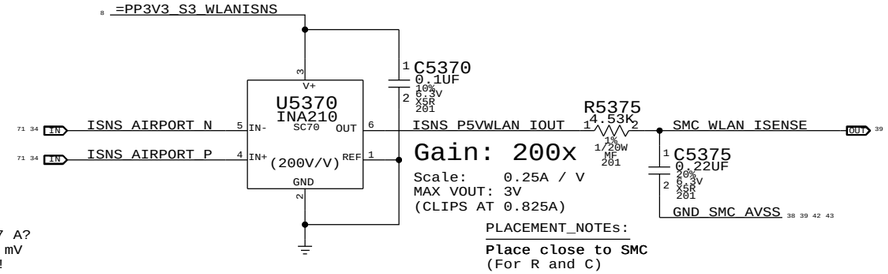
DDR3 1V5R1V35 Current Sense / Filter



EDP Current: 7 A
Max Vdiff: 13.0 mV
WF: Verify SO-DIMM current!

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

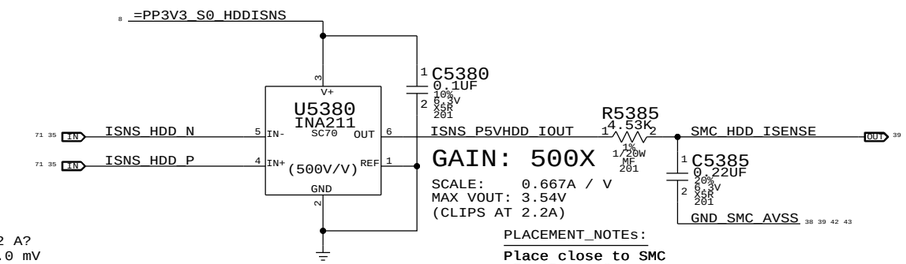
AirPort Current Sense / Filter



EDP Current: 0.727 A?
Max Vdiff: 14.6 mV
WF: Verify Airport current!

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

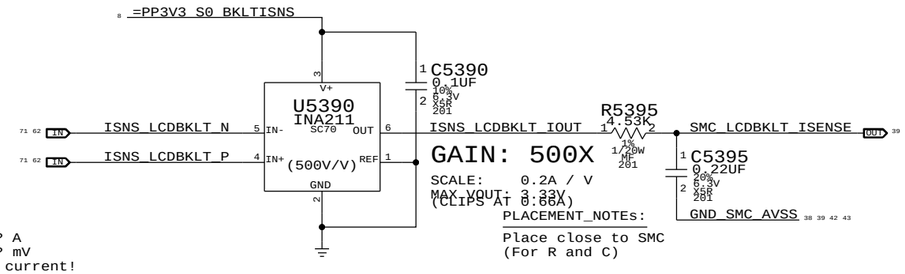
HDD Current Sense / Filter



EDP Current: 1.2 A?
Max Vdiff: 24.0 mV
WF: Verify SSD current!

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

LCD Backlight Driver Input Current Sense / Filter



EDP Current: ??? A
Max Vdiff: ??? mV
WF: Verify LCD backlight current!

PLACEMENT_NOTES:
Place close to SMC
(For R and C)

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
Voltage & Current Sensing

Apple Inc.

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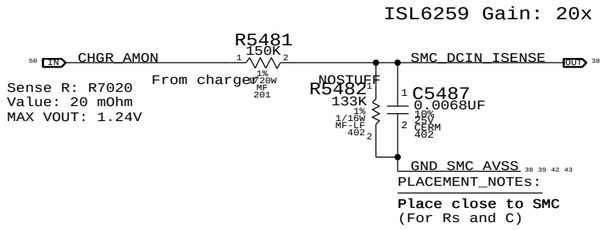
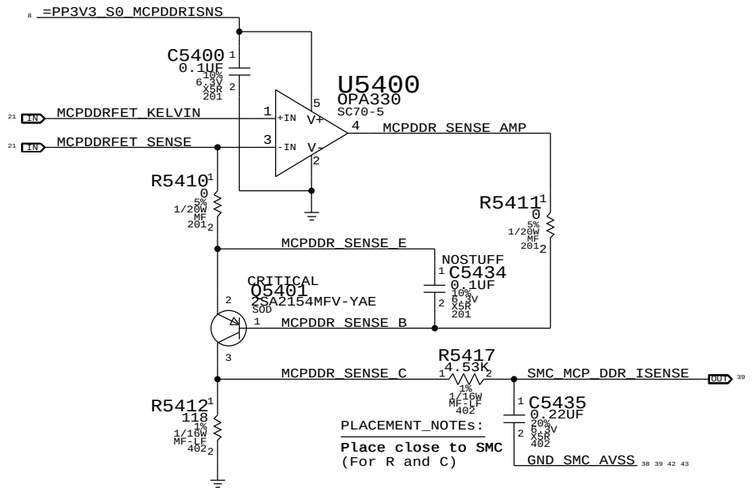
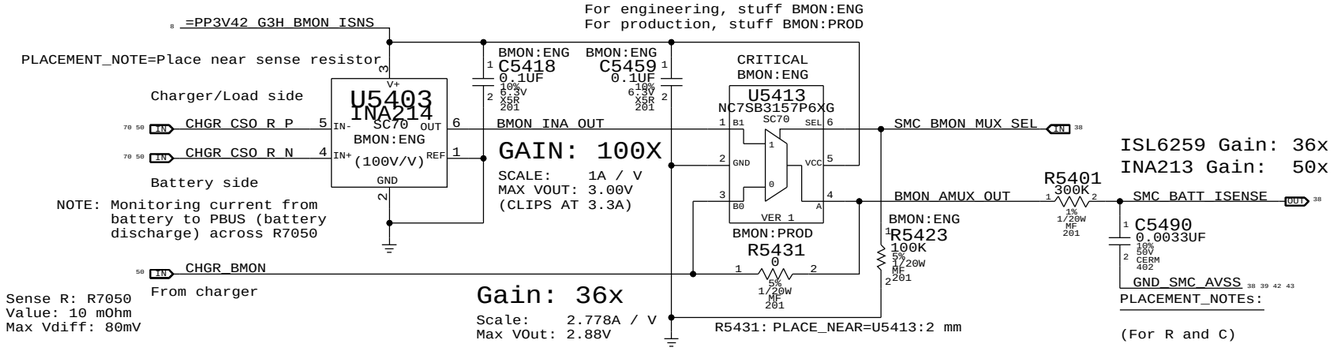
DCIN (AMON) Current Sense, RMUX & Filter



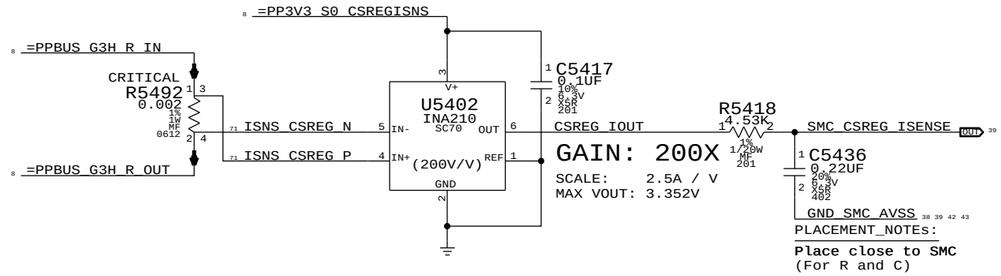
MCP MEM VDD Current Sense / Filter



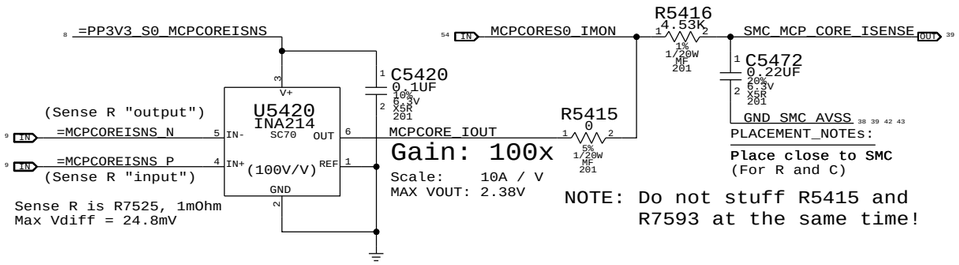
Battery (BMON) Current Sense, MUX & Filter



Chipset Regulators High-Side Current Sense / Filter

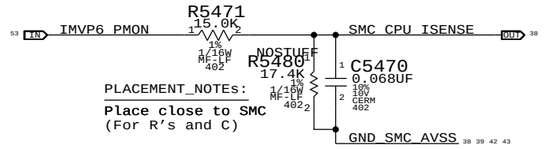


MCP VCore Current Sense Filter



VERIFY ALL RESISTOR AND GAINS

CPU VCore Load Side Current Sense / Filter



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: Current Sensing

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

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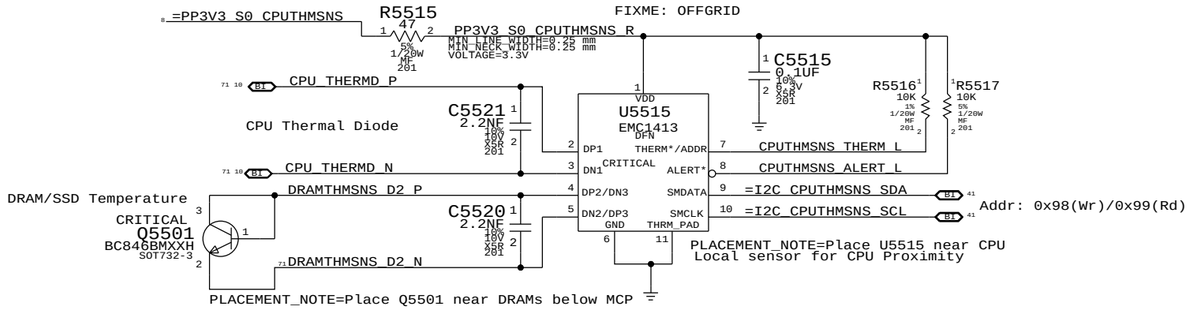
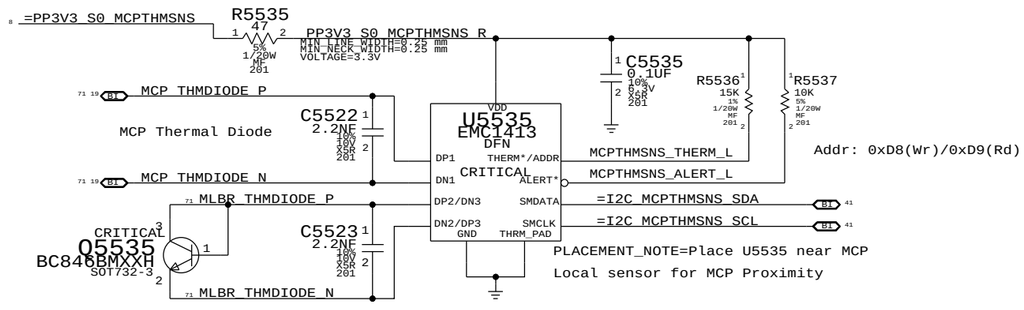
CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

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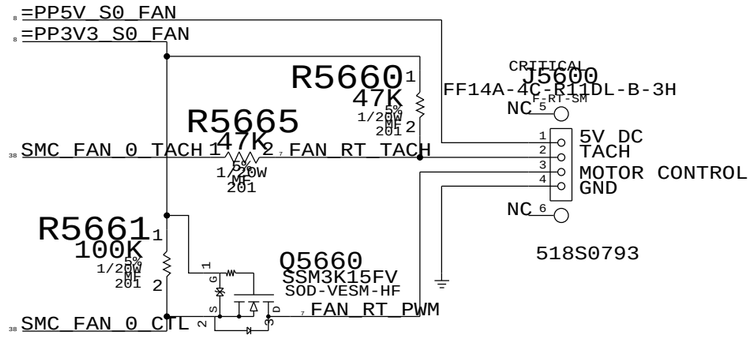
FAN CONNECTOR



SYNC_MASTER=K16_MLB	SYNC_DATE=07/07/2010
PAGE TITLE: Fan	
Apple Inc.	DRAWING NUMBER: 051-8379 SIZE: D
	REVISION: 4.4.0
	BRANCH:
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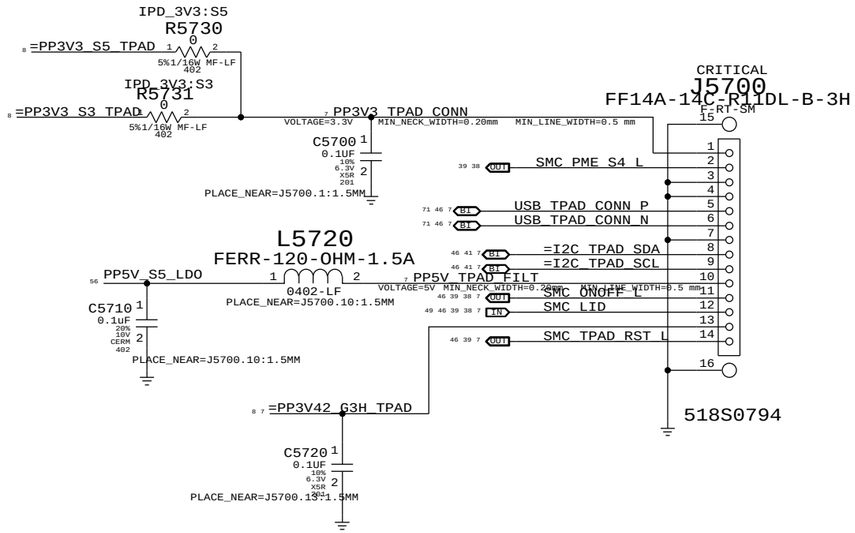
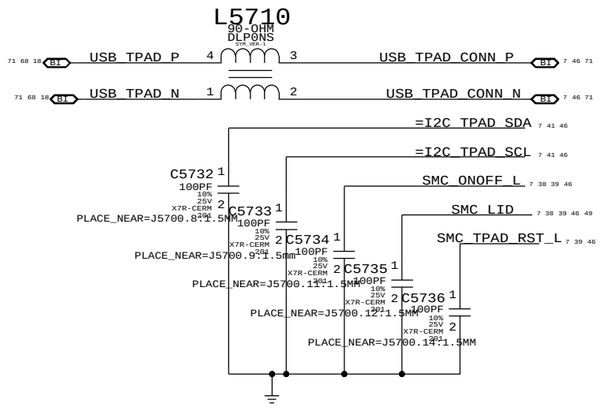
IPD Flex Connector





SYNC_MASTER=K16_MLB	SYNC_DATE=07/07/2010
PAGE TITLE: WELLSPRING 1	
Apple Inc.	DRAWING NUMBER: 051-8379 · SIZE: D
	REVISION: 4.4.0
	BRANCH:
	PAGE: 57 OF 110
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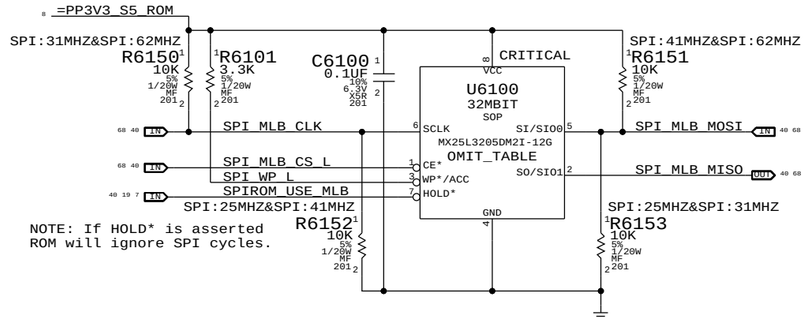

MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command.

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: SPI ROM

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

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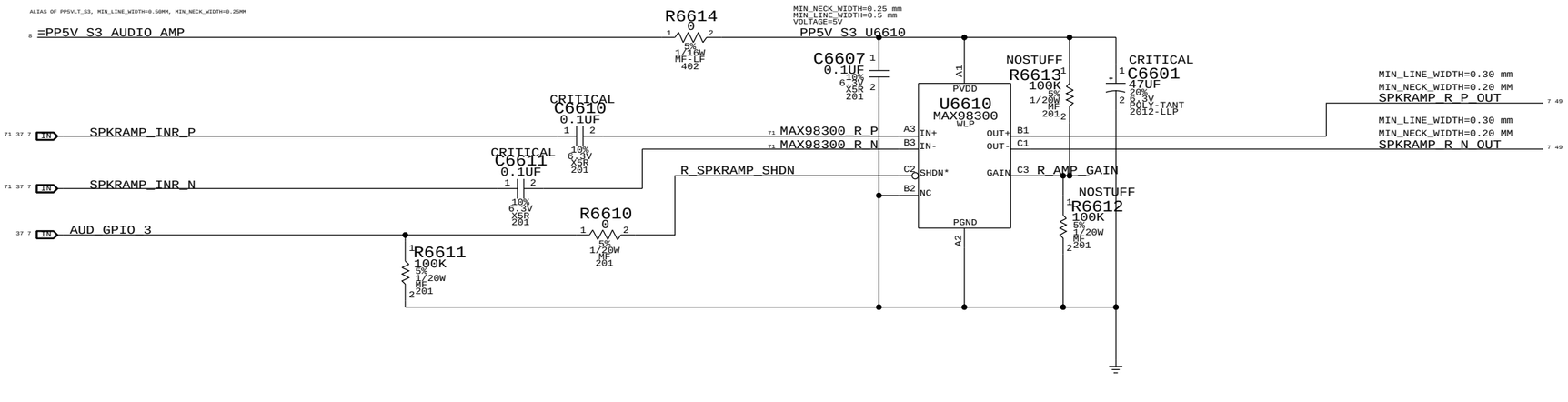
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



SYNC_MASTER=AUDIO SYNC_DATE=02/09/2010

PAGE TITLE

AUDI0: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

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MLB TO LIO POWER CABLE CONNECTOR

J6900
WTB-PWR-M82
M-RT-SM

=PP1V8_DCIN_CONN
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=18.5V

=PP5V_S3_LIO_CONN

C6905 0.01UF 20% 50V CERM 603

C6906 0.01UF 10% 10V X5R 201

518S0508

APN:518S0519
CRITICAL
J6903
78171-0002
M-RT-SM

SPKRAMP_R_P_OUT
SPKRAMP_R_N_OUT

SPKR

=PP3V3_S3_DBGLEDS

S3_S0_LED
R6940 1K 5% 1/16W MF-LF 402

S3_S0_LED
R6941 1K 5% 1/16W MF-LF 402

ITS_ALIVE

CORE_VOLTAGES_ON_R

S3_S0_LED
D6910 GREEN-3.6MCD 2.0X1.25MM-SM

S3_S0_LED
D6920 GREEN-3.6MCD 2.0X1.25MM-SM

CORE_VOLTAGES_ON

S3_S0_LED
Q6940 2N7002DW-X-G SOT-363

ALL_SYS_PWRGD

S3 AND S0 INDICATOR LEDS FOR DEVELOPMENT ONLY

SIL ON MLB FOR DEVELOPMENT ONLY

SIL
D6900
SYS_LED_ANODE
GREEN-3.6MCD 2.0X1.25MM-SM

998-3029
J6955
HALL-SENSOR-MLB-PADS-K99
SM

=PP3V42_G3H_HALL

NC NC NC NC

OMIT_TABLE

R6961 0 5% 1/20W MF 201

SMC_LID

NOSTUFF C6955 0.001UF 10% 50V CERM 402

HALL EFFECT PADS

CRITICAL
J6950
BAT-K99
F-RT-TH

POS POS POS SCL SDA SYS_DETECT NEG NEG NEG SHLD_PIN SHLD_PIN SHLD_PIN SHLD_PIN

PPVBAT_G3H_CONN

SYS_DETECT_L

=SMBUS_BATT_SDA

=SMBUS_BATT_SCL

CRITICAL
D6950 RCLAMP2402B SC-75 NOSTUFF

R6950 10K 5% 1/20W MF 201

C6950 0.1UF 10% 25V X5R 402

C6951 1UF 10% 16V X5R 402

518-0369

BATTERY CONNECTOR

CRITICAL
D6905
BAT30CWFILM
SOT-323

PPBUS_G3H

R6905 10 5% 1/8W MF-LF 805

PPDCIN_G3H_OR_PBUS

PPDCIN_G3H_OR_PBUS_R
VOLTAGE=18.5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

C6990 2.2UF 10% 25V X5R-CERM 603

U6990
LT3470A
DFN
CRITICAL
VIN BOOST SHDN* SW BIAS NC NC FB GND THRM PAD

P3V42G3H_BOOST
DIDT=TRUE

C6994 0.22UF 20% 6.3V X5R 201

L6995 33UH-20%-0.39A-0.435OHM DP418C-SM

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE DIDT=TRUE

=PP3V42_G3H_REG

Vout = 3.425V
60MA MAX OUTPUT
(Switcher limit)

C6995 22PF 5% 50V CERM 201

R6995 348K 1% 1/20W MF 201

OMIT_TABLE
C6999 10UF 20% 6.3V X5R 603-1

P3V42G3H_FB

R6996 200K 1% 1/20W MF 201

Vout = 1.25V * (1 + Ra / Rb)

SYNC_MASTER=K84_MLB SYNC_DATE=11/09/2009

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

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Reverse-Current Protection

Inrush Limiter

FROM ADAPTER

8 =PPDCIN_S5_CHGR

CRITICAL Q7080 SI5415DU POWERPAK

PPDCIN_G3H_OR_PBUS MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=18.5V 49

CRITICAL Q7085 SI5415DU POWERPAK

PPDCIN_G3H_INRUSH MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=18.5V

R7080 100K 5% 1/20W MF 201

C7085 0.1UF 10% 25V X5R 402

R7085 470K 1% 1/20W MF 201

CHGR_SGATE_DIV MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.3 mm

CHGR_AGATE_DIV MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.3 mm

R7081 62K 5% 1/20W MF 201

R7086 332K 1% 1/20W MF 201

CRITICAL D7005 BAT30CWFILM SOT-323

CHGR_DCIN_D_R

R7005 20 5% 1/20W MF 201

(CHGR_DCIN)

(CHGR_SGATE)

(CHGR_AGATE)

ACIN pin threshold is 3.2V, +/- 50mV

DIVIDER SETS ACIN THRESHOLD AT 12.18V

Input impedance of ~40K meets sparkitecture requirements

30mA max load

_P5V1_CHGR_VDD MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.1 mm VOLTAGE=5.1V

R7001 4.7 5% 1/10W MF-LF 402

_P5V1_CHGR_VDDP MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=5.1V

C7001 1UF 10% 10V X5R 402

57 8 =PP3V42_G3H_CHGR

R7010 30.1K 1% 1/20W MF 201

C7002 1UF 10% 10V X5R 402

GND_CHGR_AGND 50

NO STUFF

R7002 100K 5% 1/20W MF 201

R7000 0 5% 1/20W MF 201

40 39 38 7 IN SMC_RESET_L

CHGR_RST_L

VDD VDDP

OMIT_TABLE

CRITICAL U7000 ISL6259HRTZ TQFN 7X7

VHST	12	DCIN	2 CHGR_DCIN
SMB_RST_N	13	SGATE	26 CHGR_SGATE
SCL	11	AGATE	1 CHGR_AGATE
SDA	10	CSIP	28 70 CHGR_CSI_P
VFRQ	4	CSIN	27 70 CHGR_CSI_N
CELL	6	BOOT	25 CHGR_BOOT
ACIN	3	UGATE	24 CHGR_UGATE
ICOMP	5	PHASE	23 CHGR_PHASE
VCOMP	7	LGATE	21 CHGR_LGATE
VNEG	8	BGATE	16 CHGR_BGATE
CSOP	18	AMON	9 CHGR_AMON
CSON	17	BMON	15 CHGR_BMON
THRM_PAD (AGND) 33		ACOK	14 =CHGR_ACOK
PGND 22			

41 IN =SMBUS_CHGR_SCL

41 BI =SMBUS_CHGR_SDA

57 IN CHGR_VFRQ

CHGR_CELL

Float CELL for 1S

CHGR_ACIN

CHGR_ICOMP

CHGR_VCOMP

CHGR_VNEG

70 CHGR_CSO_P

70 CHGR_CSO_N

R7013 100 1% 1/20W MF 201

R7011 10.5K 1% 1/20W MF 201

R7015 220K 1% 1/20W MF 201

CHGR_VCOMP_R

C7050 0.47UF 10% 16V X5R 402

C7015 470PF 10% 16V X5R-X7R 201

R7016 3.01K 1% 1/20W MF 201

CHGR_VNEG_R

C7016 470PF 10% 16V X5R-X7R 201

C7042 0.1UF 10% 6.3V X5R 201

C7011 0.01UF 10% 10V X5R 201

C7000 1UF 10% 10V X5R 402-1

C7005 0.22UF 20% 25V X5R 603

C7026 1000PF 10% 16V X7R 201

GND_CHGR_AGND MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V

35352392

XW7000 SM

PLACE_NEAR=U7000.29:1mm PLACE_NEAR=U7000.22:1mm

(GND)

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

R7051 2.2 5% 1/20W MF 201 70 43 CHGR_CSO_R_P

R7052 0 5% 1/20W MF 201 70 43 CHGR_CSO_R_N

* R7051 HAS 2.2OHM TO COMPENSATE UNVALANCED VOLTAGE DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

R7021 10 5% 1/20W MF 201

R7022 10 5% 1/20W MF 201

C7020 0.047UF 10% 16V X7R 402

C7022 0.1UF 10% 25V X5R 402

C7021 0.1UF 10% 25V X5R 402

70 CHGR_CSI_R_P

70 CHGR_CSI_R_N

CRITICAL R7020 0.020 0.5% 1W MF-LF 0612

PPDCIN_G3H_CHGR MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=18.5V

CRITICAL C7030 33UF-0.06OHM 20% 25V POLY-TANT CASE-D3L

CRITICAL C7031 33UF-0.06OHM 20% 25V POLY-TANT CASE-D3L

C7035 1UF 10% 25V X5R 603-1

C7036 1UF 10% 25V X5R 603-1

C7037 0.001UF 10% 50V X7R 402

PLACE_NEAR=Q7030.5:1.5mm

CRITICAL Q7030 RJK0332DPB-01 LFPAK-SM

PLACE_NEAR=Q7000.21:2mm

C7025 0.22UF 10% 10V CER 402

MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm SWITCH_NODE=TRUE DIDT=TRUE

Max Current = 8A

f = 400 kHz

CRITICAL L7030 4.7UH-9.5A IHLP4040DZ-5M

CRITICAL F7040 7AMP-24V 1206-1

TO SYSTEM

=PPBUS_G3H 8

PPVBAT_G3H_CHGR_REG MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 MM VOLTAGE=8.4V

CRITICAL C7040 62UF 20% 11V ELEC CASE-B2

CRITICAL C7041 62UF 20% 11V ELEC CASE-B2

CRITICAL C7043 62UF 20% 11V ELEC CASE-B2

PLACE_NEAR=L7030.2:1.5mm

C7045 1000PF 10% 16V X7R 201

R7050 0.01 0.5% 1W MF 0612-3

CRITICAL Q7035 RJK0305DPB LFPAK-HF

CRITICAL Q7055 SI7615DN PWRPAK-1212-8

TO/FROM BATTERY

PPVBAT_G3H_CHGR_R MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 MM VOLTAGE=8.4V

PPVBAT_G3H_CONN MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=8.4V 7 49

C7012 0.01UF 10% 10V X5R 201

C7013 0.1UF 10% 25V X5R 402

C7014 1UF 10% 25V X5R 603-1

C7017 10UF 10% 25V X5R 805

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT

SYNC_MASTER=K6_MLB SYNC_DATE=11/09/2009

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

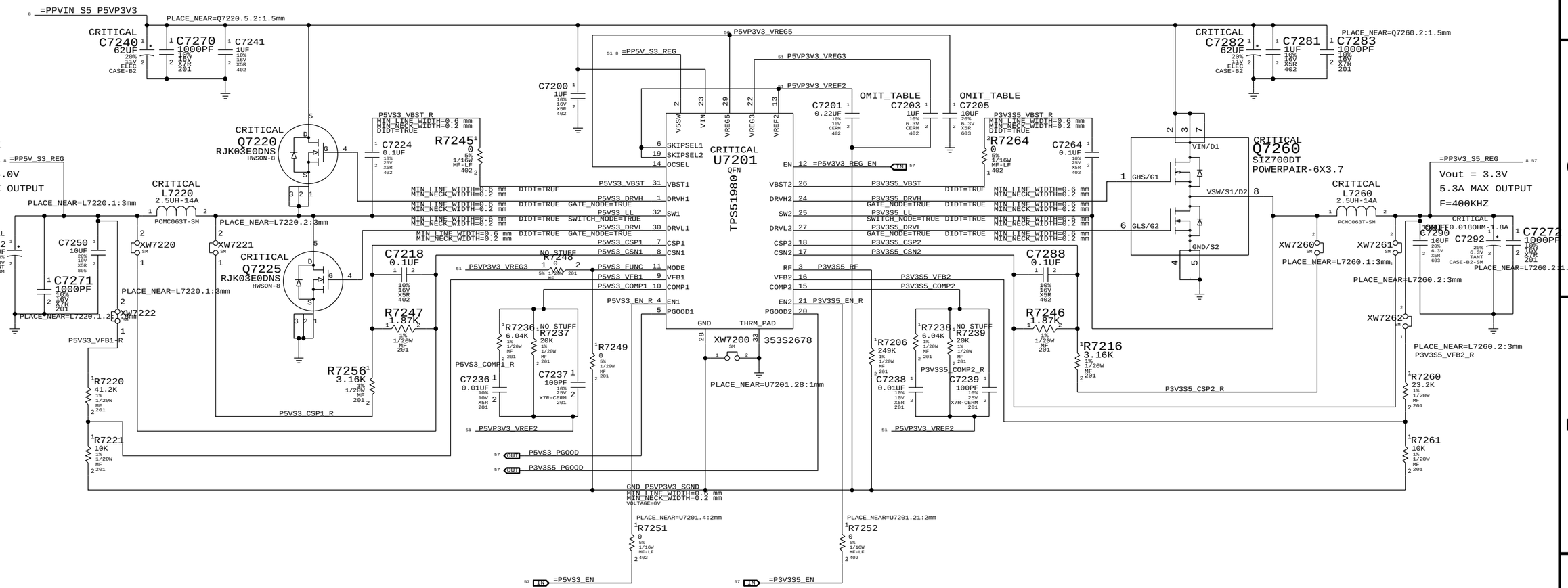
DRAWING NUMBER 051-8379 SIZE D

REVISION 4.4.0

BRANCH

PAGE 70 OF 110

SHEET 50 OF 73



SYNC_MASTER=K16_MLB	SYNC_DATE=07/07/2016
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER 051-8379 · SIZE D
	REVISION 4.4.0
	BRANCH
	PAGE 72 OF 110
	SHEET 51 OF 73

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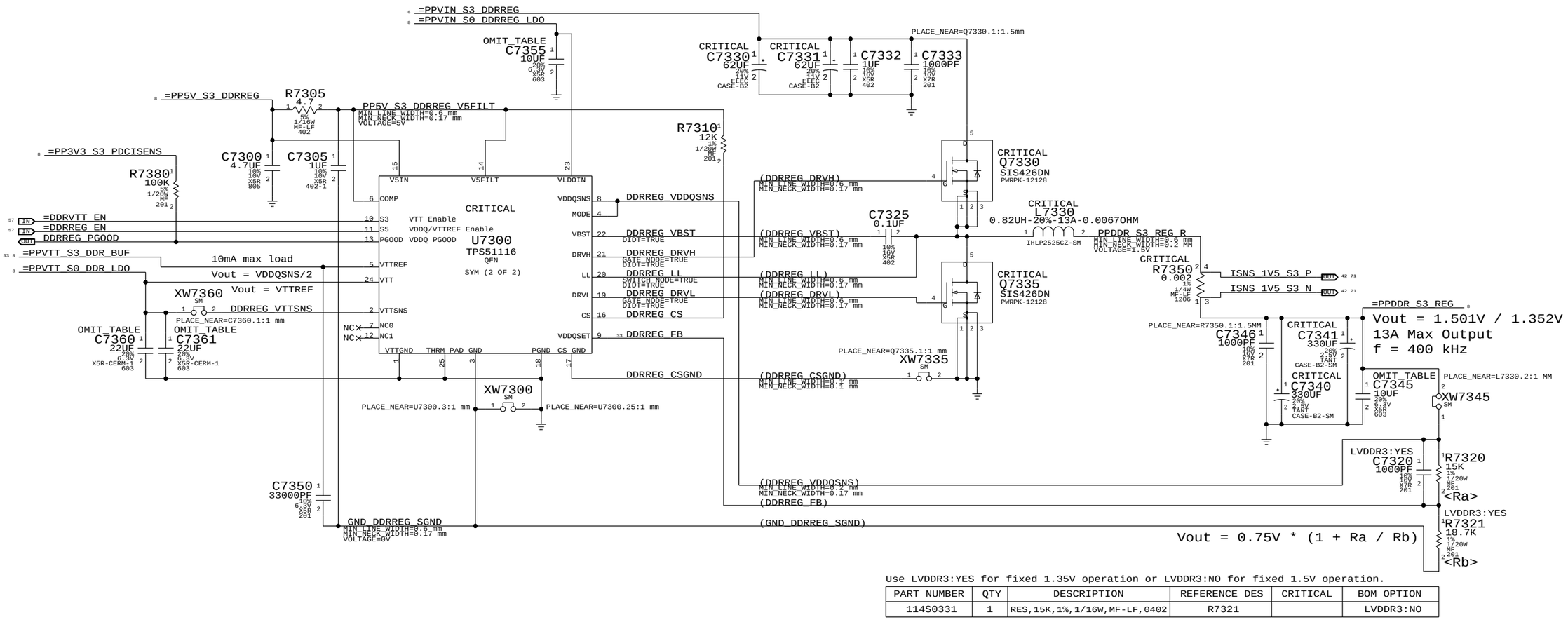

Use LVDDR3:YES for fixed 1.35V operation or LVDDR3:NO for fixed 1.5V operation.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0331	1	RES,15K,1%,1/16W,MF-LF,0402	R7321		LVDDR3:NO

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: 1.5V/1.35V LVDDR3 Supply

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

REVISION: 4.4.0

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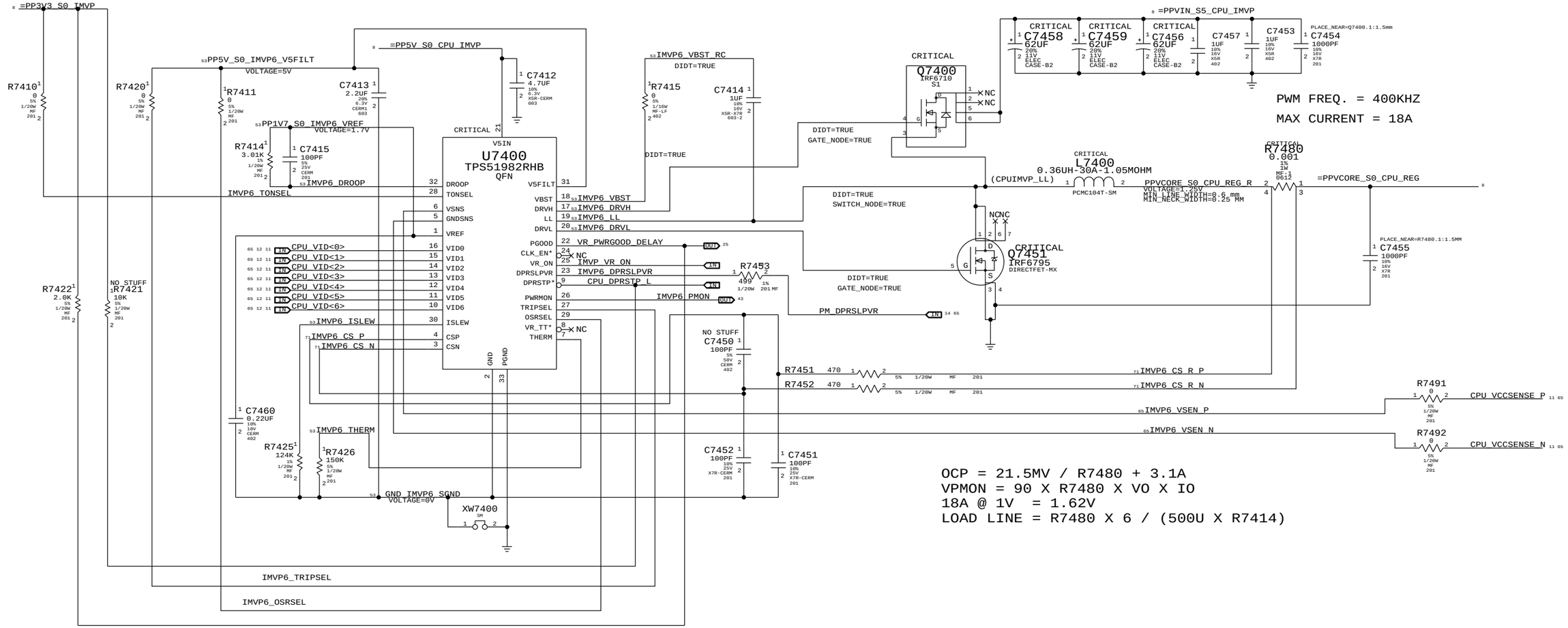
IMVP6 CPU VCORE REGULATOR



	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_LL	1.5 MM	0.20 MM
IMVP6_VBST	0.25 MM	0.20 MM
IMVP6_DRVH	1.5 MM	0.20 MM
IMVP6_DRVL	1.5 MM	0.20 MM
IMVP6_VBST_RC	1.5 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_THERM	0.25 MM	0.20 MM
IMVP6_ISLEW	0.25 MM	0.20 MM
PP1V7_S0_IMVP6_VREF	0.25 MM	0.20 MM
PP5V_S0_IMVP6_V5FILT	0.25 MM	0.20 MM

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

PAGE TITLE: IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

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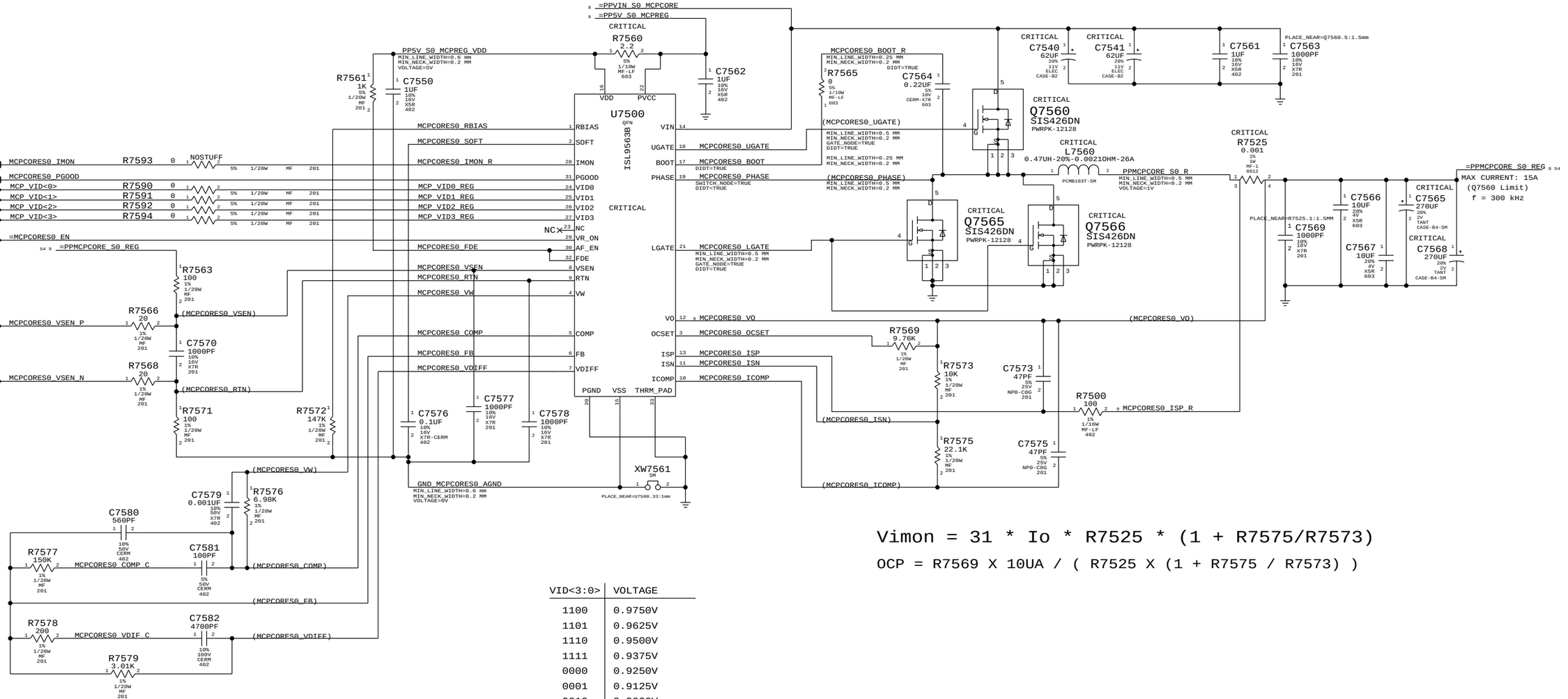

VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

Vimon = 31 * Io * R7525 * (1 + R7575/R7573)

OCP = R7569 X 10UA / (R7525 X (1 + R7575 / R7573))

K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE: MCP VCore Regulator

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

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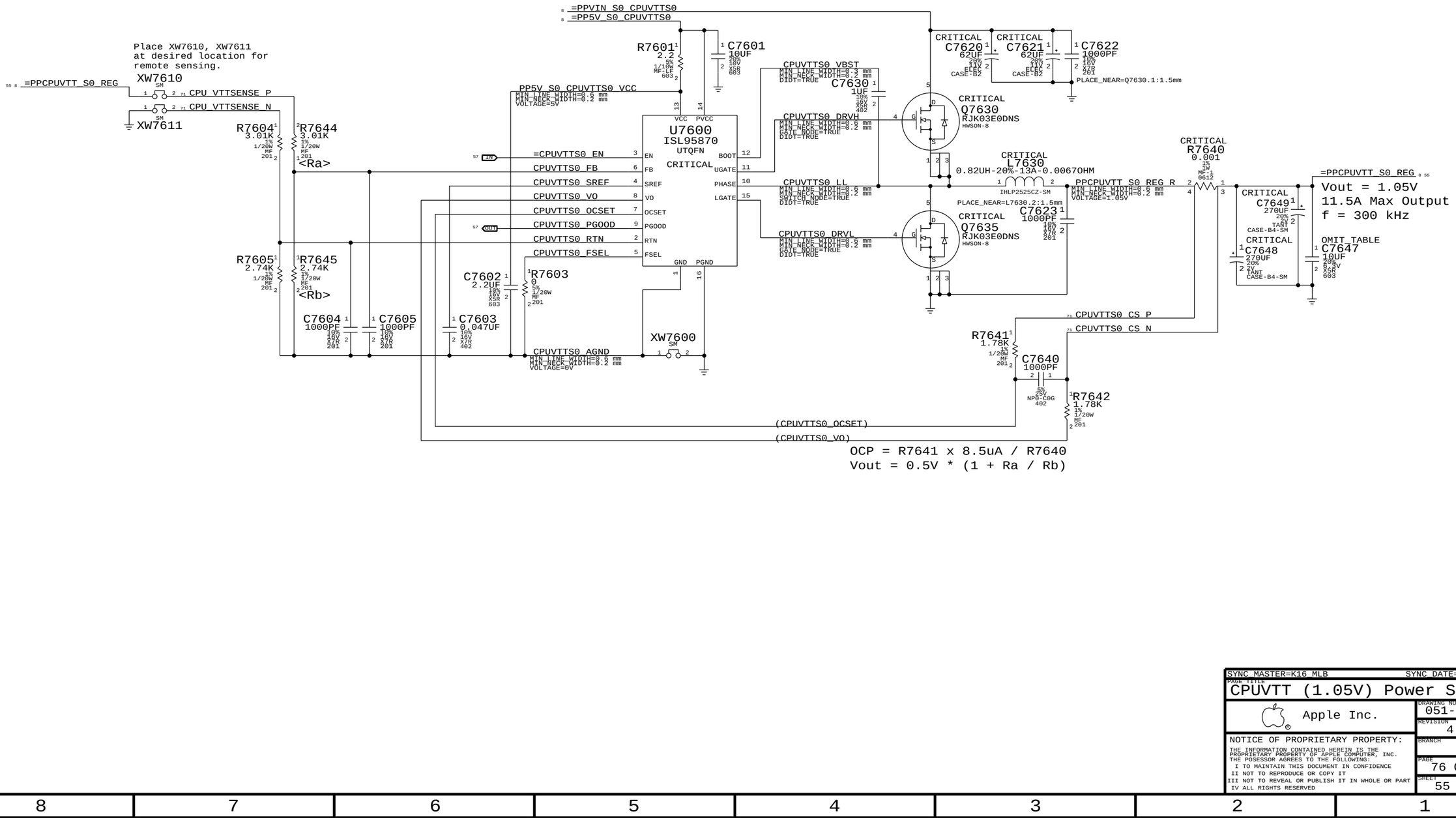

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2016

PAGE TITLE

CPUVTT (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER 051-8379 SIZE D

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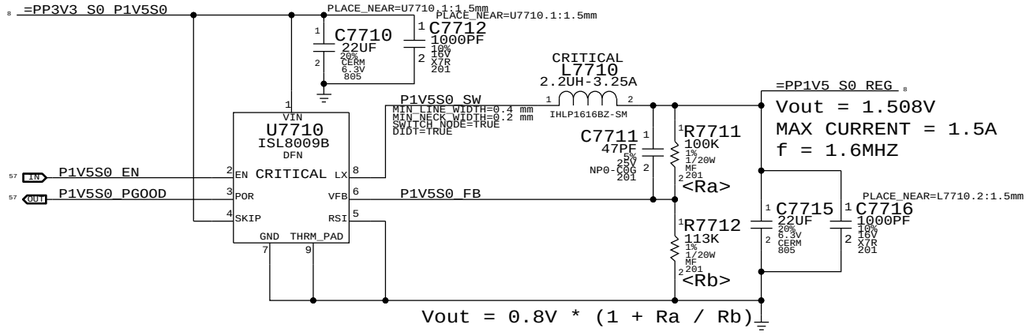
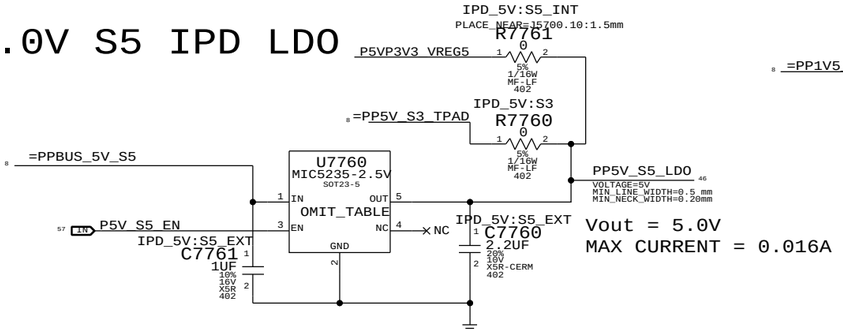
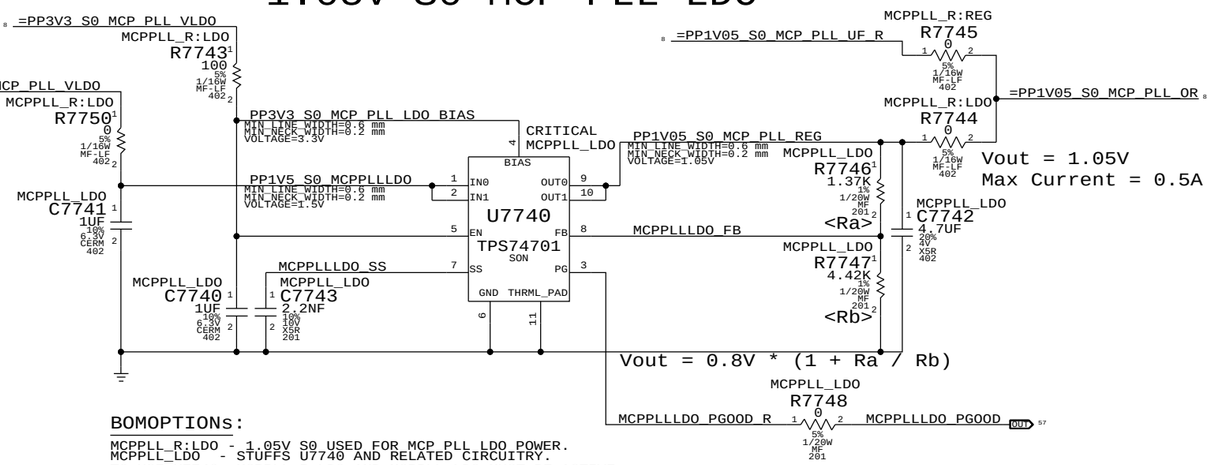
1.5V S0 Regulator



5.0V S5 IPD LDO



1.05V S0 MCP PLL LDO

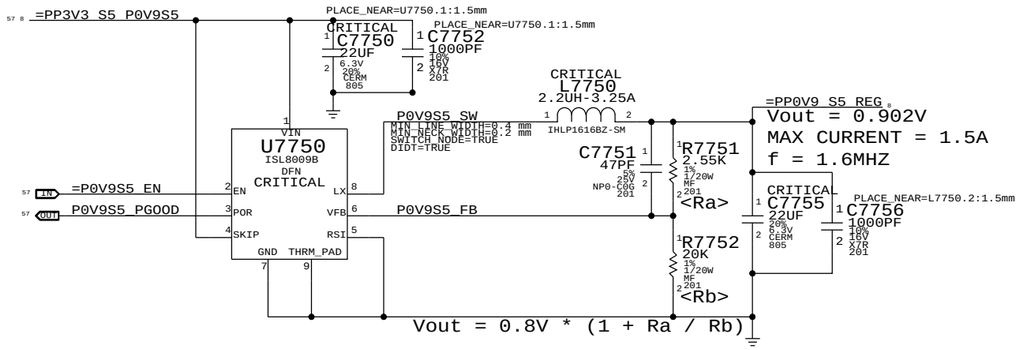


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3034	1	IC,LDO,MIC5235,5V,1%,150MA,SOT23-5	U7760		IPD_5V:S5_EXT

BOMOPTIONs:

MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

MCP 0.9V S5 (AUXC) Switcher



SYNC_MASTER=K16_MLB
SYNC_DATE=07/07/2010
PAGE TITLE: Misc Power Supplies
Apple Inc.
DRAWING NUMBER: 051-8379
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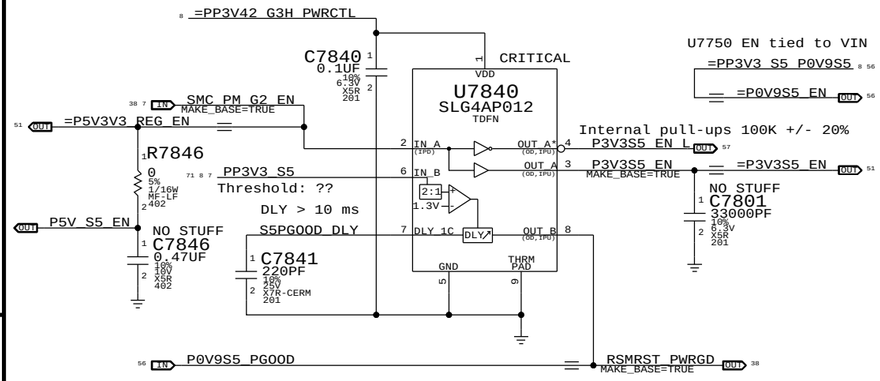
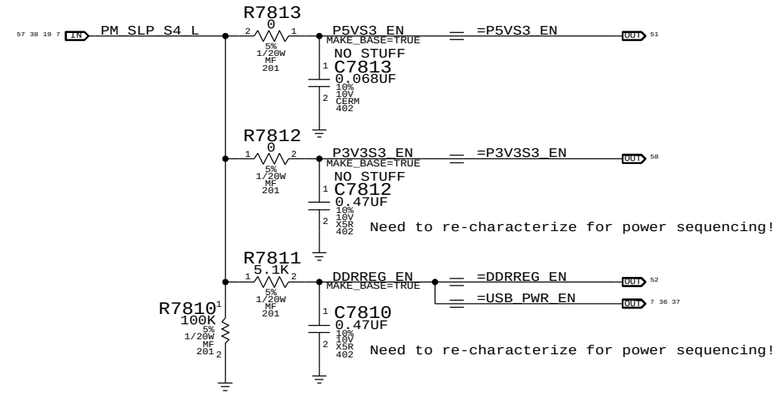
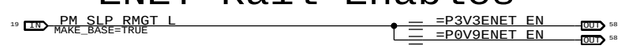
S5 Rail Enables & PGOOD



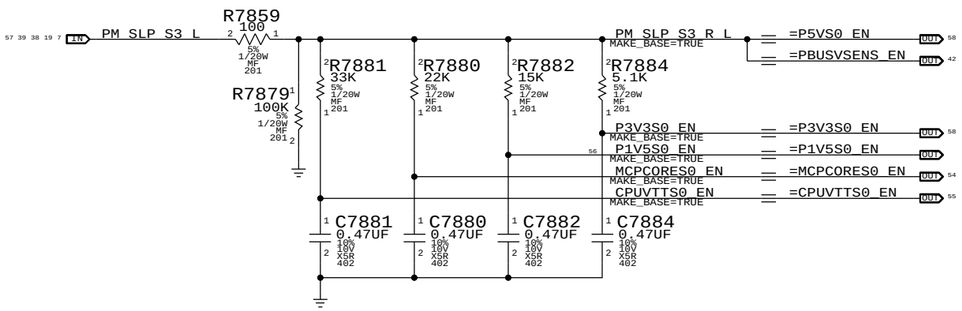
S3 Rail Enables



ENET Rail Enables



S0 Rail Enables

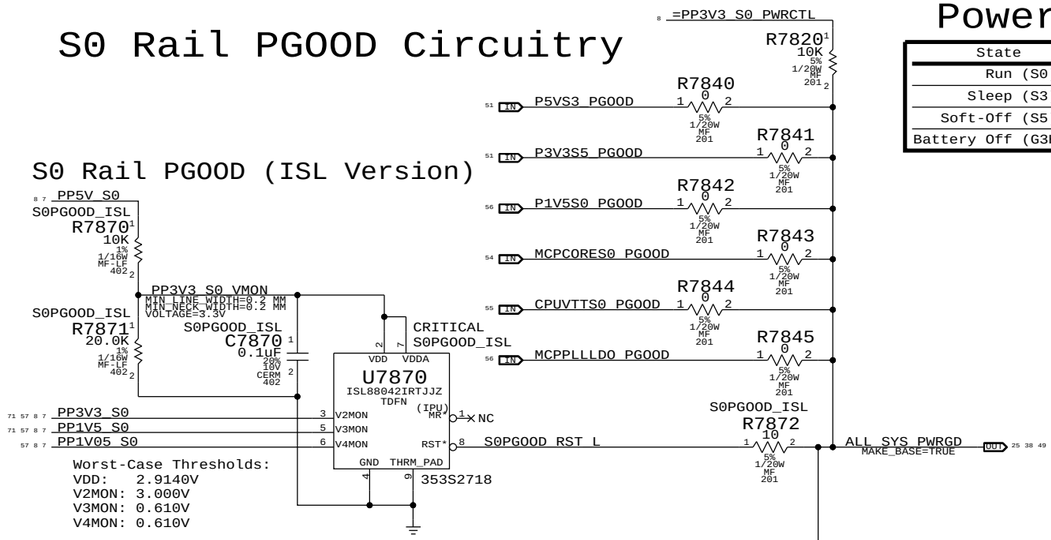


VTT Rail Enable

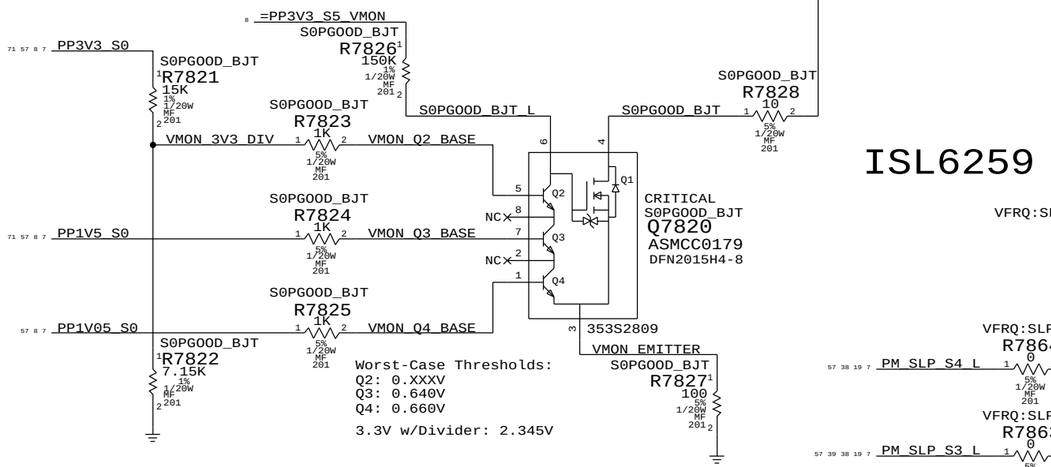
VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

S0 Rail PGOOD Circuitry

S0 Rail PGOOD (ISL Version)



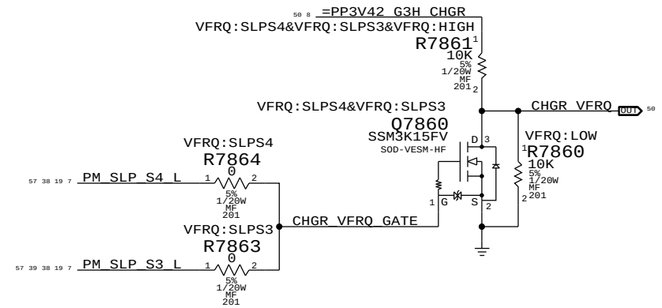
S0 Rail PGOOD (BJT Version)



Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

ISL6259 Frequency Select

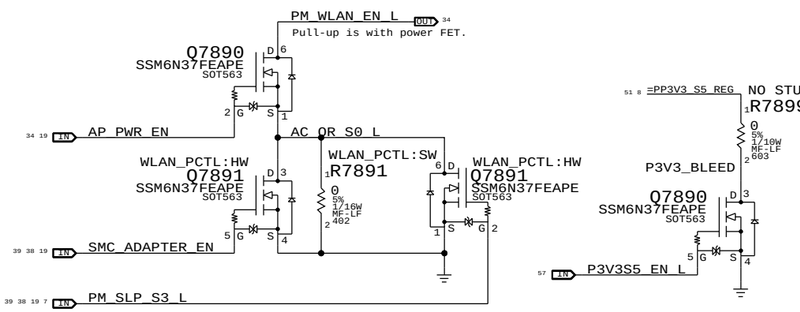


WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

NOTE: "AC" term valid only when Q7891 is stuffed



SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: Power Sequencing

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

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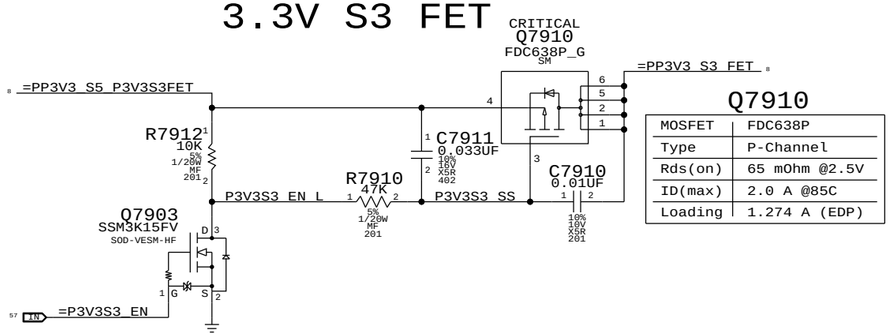
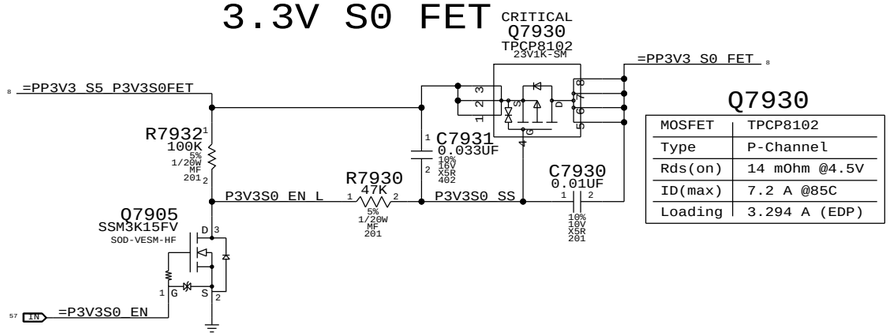
3.3V S3 FET



Q7910

MOSFET	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	1.274 A (EDP)

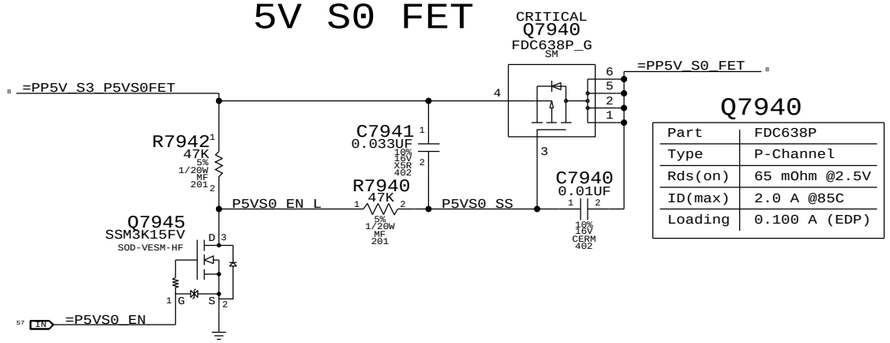
3.3V S0 FET



Q7930

MOSFET	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
ID(max)	7.2 A @85C
Loading	3.294 A (EDP)

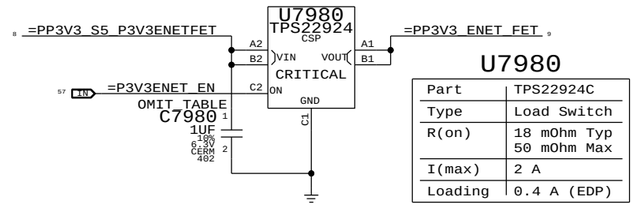
5V S0 FET



Q7940

Part	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	0.100 A (EDP)

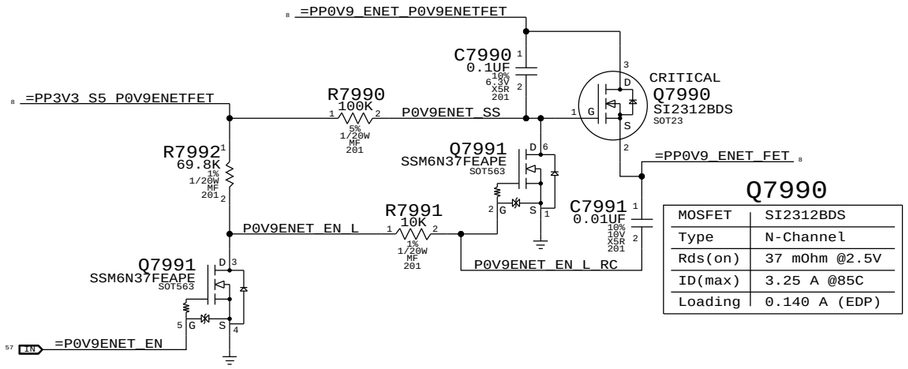
3.3V ENET Switch



U7980

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max
I(max)	2 A
Loading	0.4 A (EDP)

0.9V ENET FET



Q7990

MOSFET	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85C
Loading	0.140 A (EDP)

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: 051-8379 SIZE: D

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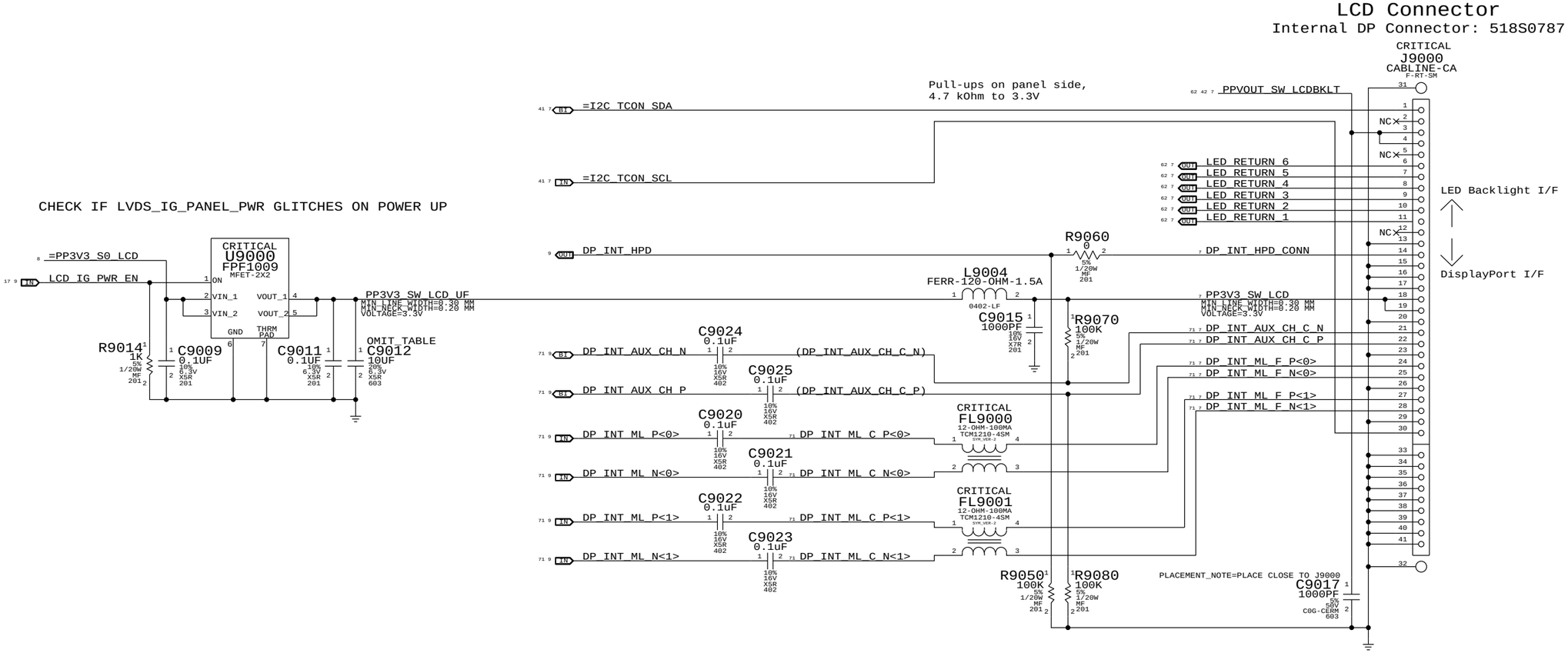

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

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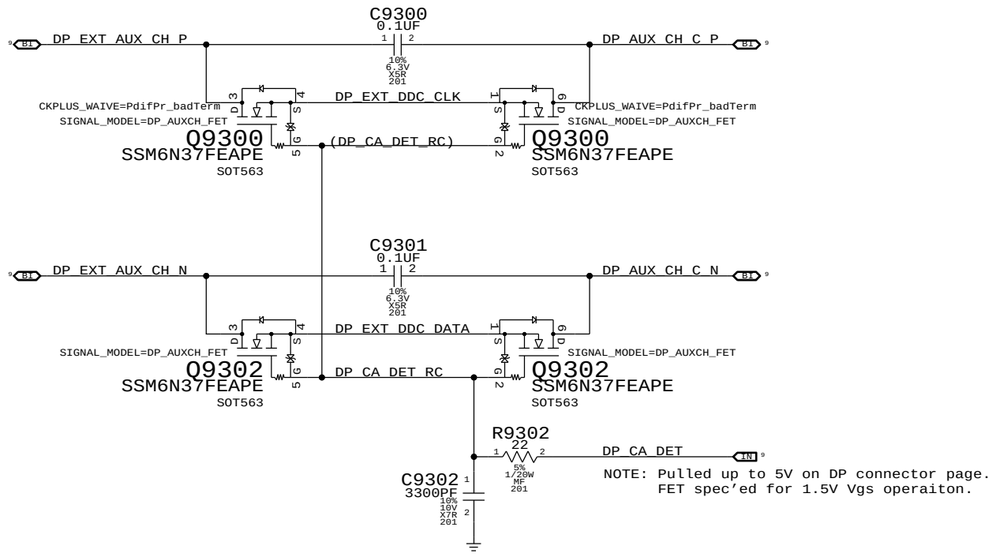

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE

External DisplayPort Support

Apple Inc.

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Port Power Switch

=PP3V3_S5_DP_PORT_PWR
=DP_PWR_EN
CRITICAL
U9480
TPS2051B
SOT23
IN
EN
GND
OUT
OC*
PP3V3_SW_DPILIM
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
TP_DPPWR_OC_L
L9400
FERR-120-OHM-3A
0603
PP3V3_SW_DPPWR
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
C9400 0.01UF 10% 16V X5R 201
CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-BZ-SM
OMIT_TABLE C9480 22UF 20% 6.3V X5R-CERM 1 603
C9481 0.1UF 10% 6.3V X5R 201
C9485 0.1UF 10% 6.3V X5R 201
OMIT_TABLE C9486 10UF 20% 6.3V X5R 603

HDMI_CEC
R9425 1M 5% 1/20W MF 201

CRITICAL
J9400
MINIDSPLYPRT-K99
F-RT-TH
HOT_PLUG_DETECT
CONFIG1
CONFIG2
GND
ML_LANE3P
ML_LANE3N
GND
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
GND
ML_LANE1P
ML_LANE1N
GND
ML_LANE2P
ML_LANE2N
RETURN
SHIELD PINS

CRITICAL
DP_ESD
D9410
RCLAMP0524P
SLP2510P8

CRITICAL
FL9403
12-OHM-100MA
TCM1210-4SM

R9420 100K 5% 1/20W MF 201

DP_EXT_ML_P<3> C9414 0.1UF 10% 6.3V X5R 201 DP_EXT_ML_C_P<3>
DP_EXT_ML_N<3> C9415 0.1UF 10% 6.3V X5R 201 DP_EXT_ML_C_N<3>
DP_EXT_ML_F_P<3>
DP_EXT_ML_F_N<3>
DP_EXT_AUX_CH_C_P
DP_EXT_AUX_CH_C_N

=PP3V3_S0_DPCONN
=PP5VR3V3_S0_DPCADET
R9443 100K 5% 1/20W MF 201
R9442 100K 5% 1/20W MF 201
DP_EXT_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q_L
NOTE: Q9440 must have Drain to Gate leakage of < 500 nA and gate to Source resistance of > 5 MOhm.
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q
R9422 1M 5% 1/20W MF 201
DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

R9421 100K 5% 1/20W MF 201
CRITICAL
DP_ESD
D9411
RCLAMP0524P
SLP2510P8

CRITICAL
DP_ESD
D9400
RCLAMP0504F
SC70-6-1

=PP3V3_S0_DPCONN
R9445 10K 5% 1/20W MF 201
DP_EXT_HPD
PP3V3_SW_DPILIM
R9444 10K 5% 1/20W MF 201
Q9441 2N7002DW-X-G SOT-363
DP_EXT_HPD_L
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q
R9423 100K 5% 1/20W MF 201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

CRITICAL
FL9400
12-OHM-100MA
TCM1210-4SM
DP_EXT_ML_C_P<0> C9410 0.1UF 10% 6.3V X5R 201 DP_EXT_ML_P<0>
DP_EXT_ML_C_N<0> C9411 0.1UF 10% 6.3V X5R 201 DP_EXT_ML_N<0>
DP_EXT_ML_F_P<0>
DP_EXT_ML_F_N<0>

CRITICAL
FL9401
12-OHM-100MA
TCM1210-4SM
DP_EXT_ML_C_P<1> C9412 0.1UF 10% 6.3V X5R 201 DP_EXT_ML_P<1>
DP_EXT_ML_C_N<1> C9413 0.1UF 10% 6.3V X5R 201 DP_EXT_ML_N<1>
DP_EXT_ML_F_P<1>
DP_EXT_ML_F_N<1>

CRITICAL
FL9402
12-OHM-100MA
TCM1210-4SM
DP_EXT_ML_C_P<2> C9416 0.1UF 10% 6.3V X5R 201 DP_EXT_ML_P<2>
DP_EXT_ML_C_N<2> C9417 0.1UF 10% 6.3V X5R 201 DP_EXT_ML_N<2>
DP_EXT_ML_F_P<2>
DP_EXT_ML_F_N<2>

CRITICAL
DP_ESD
D9411
RCLAMP0524P
SLP2510P8

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: DisplayPort Connector

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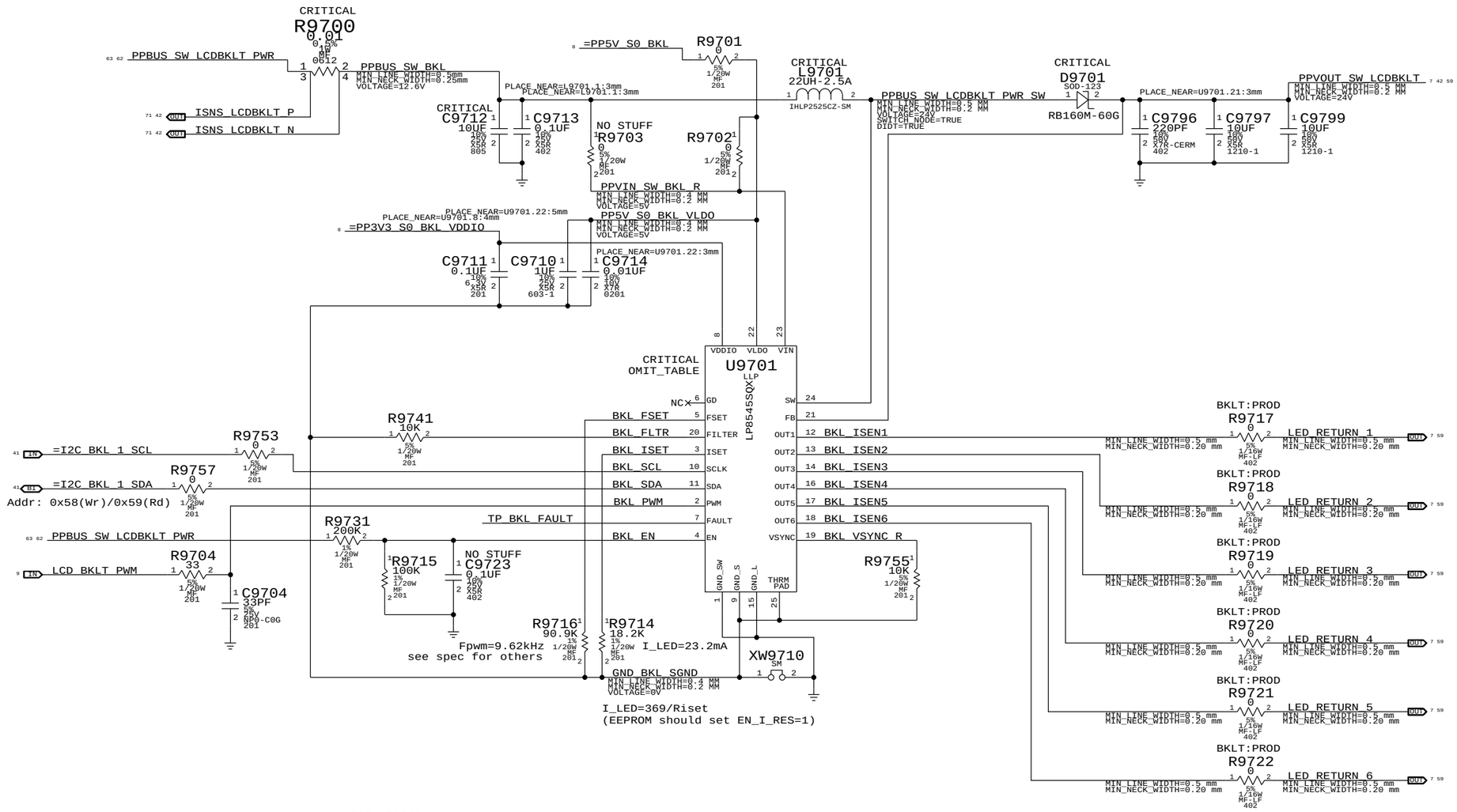
*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



FOR LP8543:
STUFF R9741
NO STUFF R9740, C9740, C9741, R9754

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
353S2896	1	IC,LP8545,LED BKLT CTRLR,PRODUCTIO,LLP24	U9701	CRITICAL	PROJ:K16
353S2967	1	IC,LP8545,LED BKLT CTRLR,LLP24,K99 VER	U9701	CRITICAL	PROJ:K99

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=K16_MLB SYNC_DATE=03/31/2010

PAGE TITLE
LCD Backlight Driver

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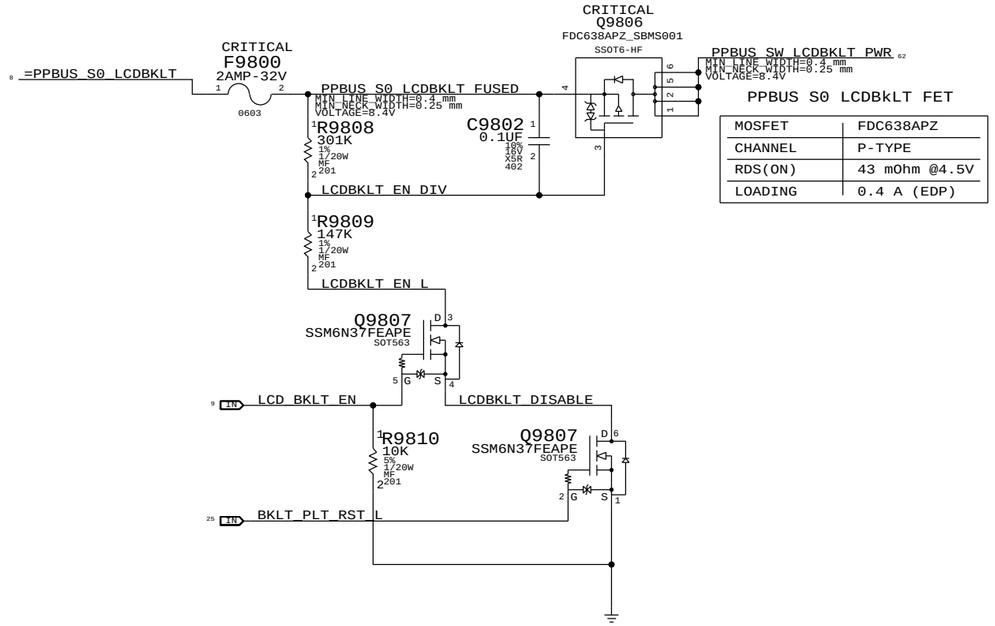

SYNC_MASTER=K16_MLB	SYNC_DATE=07/07/2010
PAGE TITLE: LCD Backlight Support	
Apple Inc.	DRAWING NUMBER: 051-8379 SIZE: D
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ADDITIONAL CPU VCORE HF DECOUPLING

40x 1uF 0402

12 11 8 =PPVCORE_S0_CPU

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT_TABLE CRITICAL C9900 C9901 C9902 C9903 C9904 C9905 C9906 C9907 C9908 C9909
2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT_TABLE CRITICAL C9910 C9911 C9912 C9913 C9914 C9915 C9916 C9917 C9918 C9919
2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT_TABLE CRITICAL C9920 C9921 C9922 C9923 C9924 C9925 C9926 C9927 C9928 C9929
2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT_TABLE CRITICAL C9930 C9931 C9932 C9933 C9934 C9935 C9936 C9937 C9938 C9939
2.2UF 20% 6.3V CERM 402-LF

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE
Additional CPU/GPU Decoupling

Apple Inc.

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
	FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_55S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_55S	FSB_1X	FSB_BREQ0_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_DBSY_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_DRDY_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_55S	FSB_1X	FSB_CPURST_L	10 13 14
	FSB_1X	FSB_55S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_55S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_55S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_55S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU_INTR	10 14
	CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU_NMI	10 14
	CPU_PROCHOT_L	CPU_55S	CPU_AGTL	CPU_PROCHOT_L	10 14 39
	CPU_PWRGD	CPU_55S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_55S	CPU_8MIL	PM_THRMTRIP_L	10 14 39
	FSB_CPUSLP_L	CPU_55S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_55S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_55S	CPU_AGTL	CPU_DPRSTP_L	10 14 53
	CPU_ASYNC	CPU_55S	CPU_AGTL	FSB_DPWR_L	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_55S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_55S	CPU_AGTL	PM_DPRSLPVR	14 53
	(See above)	CPU_55S	CPU_AGTL	IMVP_DPRSLPVR	
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 33
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
	XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
	XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
	XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
	XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
	XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	13
		CPU_55S	CPU_8MIL	CPU_VID<6..0>	11 12 53
		CPU_55S	CPU_8MIL	IMVP6_VID<6..0>	12
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 53
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 53
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	53
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	53

SYNC_MASTER=K16_MLB SYNC_DATE=07/07/2010

PAGE TITLE: CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
MEM_CLK2MEM	*	=4:1_SPACING	?	NV DG says 3x inner, 4x outer
MEM_CTRL2CTRL	*	=2:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CTRL2MEM	*	=2.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2CMD	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2DATA	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DQS2MEM	*	=3:1_SPACING	?	NV DG says 4x inner, 5x outer
MEM_2OTHER	*	25 MIL	?	

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 360 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
CMD/CTRL signals should be matched within 150 ps.
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

MEM_A/B_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_P<5..0>	9 15 26 27 32
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_N<5..0>	9 15 26 27 32
MEM_A_CKE	MEM_50S	MEM_CTRL	MEM_A_CKE<3..0>	15 21 26 27 32
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_CS_L<3..0>	15 26 27 32
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_ODT<3..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_A<15..0>	9 15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_BA<2..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_RAS_L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_CAS_L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_WE_L	15 26 27 32
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DM<0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DM<1>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DM<2>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DM<3>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 26
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 26
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_P<5..0>	9 15 28 29 32
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_N<5..0>	9 15 28 29 32
MEM_B_CKE	MEM_50S	MEM_CTRL	MEM_B_CKE<3..0>	15 21 28 29 32
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_CS_L<3..0>	15 28 29 32
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_ODT<3..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_A<15..0>	9 15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_BA<2..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_RAS_L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_CAS_L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_WE_L	15 28 29 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	
	PCIE_90D	PCIE	PCIE_AP_R2D_P	7 34
	PCIE_90D	PCIE	PCIE_AP_R2D_N	7 34
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE_AP_R2D_C_P	16 34
	PCIE_90D	PCIE	PCIE_AP_R2D_C_N	16 34
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE_AP_D2R_P	7 16 34
	PCIE_90D	PCIE	PCIE_AP_D2R_N	7 16 34
	PCIE_90D	PCIE	PCIE_ENET_R2D_P	
	PCIE_90D	PCIE	PCIE_ENET_R2D_N	
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE_ENET_R2D_C_P	
	PCIE_90D	PCIE	PCIE_ENET_R2D_C_N	
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE_ENET_D2R_P	
	PCIE_90D	PCIE	PCIE_ENET_D2R_N	
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_P	
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_90D	PCIE	PCIE_FW_R2D_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_N	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9 16
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9 16
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_P	7 16 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_N	7 16 34
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX0_TERMP	16
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	
DP_INT_ML	DP_90D	DISPLAYPORT	DP_IG_ML1_P<1..0>	9 17
DP_INT_ML	DP_90D	DISPLAYPORT	DP_IG_ML1_N<1..0>	9 17
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH1_P	9 17
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH1_N	9 17
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML0_P<3..0>	9 17
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML0_N<3..0>	9 17
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH0_P	9 17
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH0_N	9 17
MCP_TMDS0_RSET	MCP_DV_COMP		MCP_TMDS0_RSET	17 24
MCP_TMDS0_VPROBE			MCP_TMDS0_VPROBE	17 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17 24
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	18 35
	SATA_90D	SATA	SATA_HDD_R2D_C_N	18 35
	SATA_90D	SATA	SATA_HDD_R2D_P	7 35
	SATA_90D	SATA	SATA_HDD_R2D_N	7 35
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	18 35
	SATA_90D	SATA	SATA_HDD_D2R_N	18 35
	SATA_90D	SATA	SATA_HDD_D2R_C_P	7 35
	SATA_90D	SATA	SATA_HDD_D2R_C_N	7 35
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	9 18
	SATA_90D	SATA	SATA_ODD_R2D_C_N	9 18
	SATA_90D	SATA	SATA_ODD_R2D_P	9
	SATA_90D	SATA	SATA_ODD_R2D_N	9
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	9 18
	SATA_90D	SATA	SATA_ODD_D2R_N	9 18
	SATA_90D	SATA	SATA_ODD_D2R_C_P	
	SATA_90D	SATA	SATA_ODD_D2R_C_N	
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	18

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_55S	LPC	LPC AD<3..0>	7 19 38 40
LPC_FRAME_L	LPC_55S	LPC	LPC FRAME L	7 19 38 40
LPC_RESET_L	LPC_55S	LPC	LPC RESET L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R	19 25
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	25 38
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	7 25 40
USB_EXTA	USB_90D	USB	USB EXTA P	18 36
	USB_90D	USB	USB EXTA N	18 36
	USB_90D	USB	USB EXTA MUXED P	36 71
	USB_90D	USB	USB EXTA MUXED N	36 71
USB_MINI	USB_90D	USB	USB MINI P	9 18
	USB_90D	USB	USB MINI N	9 18
USB_EXTD	USB_90D	USB	USB EXTD P	7 18 37
	USB_90D	USB	USB EXTD N	7 18 37
USB_CAMERA	USB_90D	USB	USB CAMERA P	7 18 37
	USB_90D	USB	USB CAMERA N	7 18 37
USB_BT	USB_90D	USB	USB BT P	7 18 34
	USB_90D	USB	USB BT N	7 18 34
USB_TPAD	USB_90D	USB	USB TPAD P	18 46 71
	USB_90D	USB	USB TPAD N	18 46 71
USB_IR	USB_90D	USB	USB IR P	
	USB_90D	USB	USB IR N	
USB_EXTB	USB_90D	USB	USB EXTB P	
	USB_90D	USB	USB EXTB N	
USB_T57	USB_90D	USB	USB T57 P	
	USB_90D	USB	USB T57 N	
USB_EXTC	USB_90D	USB	USB EXTC P	9 18
	USB_90D	USB	USB EXTC N	9 18
USB_SDCARD	USB_90D	USB	USB SDCARD P	9 18
	USB_90D	USB	USB SDCARD N	9 18
USB_WM	USB_90D	USB	USB WM P	
	USB_90D	USB	USB WM N	
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP USB RBIAS GND	18
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP 0 CLK	19 41
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP 0 DATA	19 41
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP 1 CLK	19 41
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP 1 DATA	19 41
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK	7 19 37
	HDA_55S	HDA	HDA BIT CLK R	19
HDA_SYNC	HDA_55S	HDA	HDA SYNC	7 19 37
	HDA_55S	HDA	HDA SYNC R	19
HDA_RST_L	HDA_55S	HDA	HDA RST R L	19
	HDA_55S	HDA	HDA RST L	7 19 37
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0	7 19 37
	HDA_55S	HDA	HDA SDIN CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT	7 19 37
	HDA_55S	HDA	HDA SDOUT R	19
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP HDA PULLDN COMP	19
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK R	19 25
	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	25 38
SPI_CLK	SPI_55S	SPI	SPI CLK R	19 40
	SPI_55S	SPI	SPI CLK	40
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	19 40
	SPI_55S	SPI	SPI MOSI	40
SPI_MISO	SPI_55S	SPI	SPI MISO	19 40
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	19 40
	SPI_55S	SPI	SPI CS0 L	40
	SPI_55S	SPI	SPI MLB CLK	40 47
	SPI_55S	SPI	SPI MLB MOSI	40 47
	SPI_55S	SPI	SPI MLB MISO	40 47
	SPI_55S	SPI	SPI MLB CS L	40 47
	SPI_55S	SPI	SPI ALT CLK	7 40
	SPI_55S	SPI	SPI ALT MOSI	7 40
	SPI_55S	SPI	SPI ALT MISO	7 40
	SPI_55S	SPI	SPI ALT CS L	7 40

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

SD Card Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

RGMII Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD 18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND 18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO 9 18
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK 9 18
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<0> 9 18
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1> 9 18
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL 9 18
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL
	ENET_MII_55S	ENET_MII	ENET_RESET_L

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SD_DATA	SD_55S	SD_INTERFACE	SD_D<4..0>
	SD_55S	SD_INTERFACE	SDCONN_DATA<4..0>
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<4>
SD_DATA_R	SD_55S	SD_INTERFACE	SD_D<7..5>
	SD_55S	SD_INTERFACE	SDCONN_DATA<7..5>
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<7..5>
SD_CLK	SD_55S	SD_INTERFACE	SD_CLK
	SD_55S	SD_INTERFACE	SD_CLK_R
	SD_55S	SD_INTERFACE	SDCONN_CLK
SD_CMD	SD_55S	SD_INTERFACE	SD_CMD
	SD_55S	SD_INTERFACE	SDCONN_CMD
	SD_55S	SD_INTERFACE	BCM57765_CR_CMD

NOTE: SD_D<7..5> are different to support BCM5764M/BCM57765 co-layout.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	41
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	41
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	41
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	41
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	41
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	41
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	7 41
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	7 41
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	41
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	41

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	50
	1TO1_DIFFPAIR		CHGR_CSI_N	50
	1TO1_DIFFPAIR		CHGR_CSI_R_P	50
	1TO1_DIFFPAIR		CHGR_CSI_R_N	50
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	50
	1TO1_DIFFPAIR		CHGR_CSO_N	50
	1TO1_DIFFPAIR		CHGR_CSO_R_P	43 50
	1TO1_DIFFPAIR		CHGR_CSO_R_N	43 50

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=1:1_SPACING	?
AUDIO	*	=1:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SD CARD READER LAYOUT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*		=STANDARD				
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	5.8 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	*			0.25 MM	250 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_P	36 68
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_N	36 68
(USB_EXTA)	USB_90D	USB	USB_LT1_P	36
(USB_EXTA)	USB_90D	USB	USB_LT1_N	36
(USB_TPAD)	USB_90D	USB	USB_TPAD_P	18 46 68
(USB_TPAD)	USB_90D	USB	USB_TPAD_N	18 46 68
(USB_TPAD)	USB_90D	USB	USB_TPAD_CONN_P	7 46
(USB_TPAD)	USB_90D	USB	USB_TPAD_CONN_N	7 46
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	I2C_SMC_SMS_SDA_R	
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	I2C_SMC_SMS_SCL_R	
	SMB_55S	SMB	I2C_TCON_SCL	41
	SMB_55S	SMB	I2C_TCON_SDA	41
	SMB_55S	SMB	I2C_TCON_SCL_CONN	
	SMB_55S	SMB	I2C_TCON_SDA_CONN	

Graphics Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_90D	DISPLAYPORT	DP_INT_ML_P<1..0>	9 59
	DP_90D	DISPLAYPORT	DP_INT_ML_N<1..0>	9 59
	DP_90D	DISPLAYPORT	DP_INT_ML_C_P<1..0>	59
	DP_90D	DISPLAYPORT	DP_INT_ML_C_N<1..0>	59
	DP_90D	DISPLAYPORT	DP_INT_ML_F_P<1..0>	7 59
	DP_90D	DISPLAYPORT	DP_INT_ML_F_N<1..0>	7 59
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_C_P	7 59
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_C_N	7 59
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_P	9 59
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_N	9 59
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP_EXT_ML_P<3..0>	9 61
	DP_90D	DISPLAYPORT	DP_EXT_ML_N<3..0>	9 61
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_P<3..0>	61
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_N<3..0>	61
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_P<3..0>	61
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_N<3..0>	61
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_P	9 61
	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_N	9 61

Power Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPUTHMSNS_D2	THERM_1TO1_55S	THERM	DRAMTHMSNS_D2_P	44
	THERM_1TO1_55S	THERM	DRAMTHMSNS_D2_N	44
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 44
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 44
MCPTHMSNS_D2	THERM_1TO1_55S	THERM	MLBR_THMDIODE_P	44
	THERM_1TO1_55S	THERM	MLBR_THMDIODE_N	44
MCP_THMDIODE	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	19 44
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	19 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	42 52
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	42 52
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	34 42
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	34 42
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CSREG_P	43
	SENSE_1TO1_55S	SENSE	ISNS_CSREG_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	35 42
	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	35 42
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	42 62
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	42 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_P	55
	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_N	55
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	IMVP6_CS_P	53
	SENSE_1TO1_55S	SENSE	IMVP6_CS_N	53
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	IMVP6_CS_R_P	53
	SENSE_1TO1_55S	SENSE	IMVP6_CS_R_N	53
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VTTSENSE_P	55
	SENSE_1TO1_55S	SENSE	CPU_VTTSENSE_N	55
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_P	22 54
	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_N	22 54
		MEM_POWER	PP1V5R1V35_S3	7 8
		SB_POWER	PP3V3_S5	7 8 57
		SB_POWER	PP3V3_S0	7 8 57
		SB_POWER	PP1V5_S0	7 8 57
		GND	GND	

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P	7 37 48
	DIFFPAIR	AUDIO	SPKRAMP_INR_N	7 37 48
MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_P	48
	DIFFPAIR	AUDIO	MAX98300_R_N	48

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K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL3,ISL10	Y	0.250 MM	0.250 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.250 MM	0.250 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.140 MM	0.140 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.090 MM	0.090 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.076 MM	0.076 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.125 MM	0.125 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
75_OHM_DIFF	TOP,BOTTOM	Y	0.160 MM	0.160 MM		0.160 MM	0.160 MM
75_OHM_DIFF	ISL3,ISL10	Y	0.120 MM	0.120 MM		0.140 MM	0.140 MM
75_OHM_DIFF	ISL4,ISL9	Y	0.140 MM	0.140 MM		0.140 MM	0.140 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
95_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
95_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL3,ISL10	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM
100_OHM_DIFF	ISL4,ISL9	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
1.5X_DIELECTRIC	*	0.105 MM	?
5X_DIELECTRIC	*	0.350 MM	?

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1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	SS_CAP_1UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0628	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	MU_CAP_1UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0630	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	SS_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1284,C1285,C1286,C1287,C1289,C1291,C1292,C1293,C1294,C1295	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3536,C3537	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3600,C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3636,C3637	CRITICAL	SS_CAP_2_2UF
138S0632	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655,C3656	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	MU_CAP_2_2UF
138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1284,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3536,C3537	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3600,C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3636,C3637	CRITICAL	MU_CAP_2_2UF
138S0633	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655,C3656	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	TY_CAP_2_2UF
138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1284,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3536,C3537	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3600,C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3636,C3637	CRITICAL	TY_CAP_2_2UF
138S0634	9	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655,C3656	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C7360	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4912,C9486,C2500,C2520,C2560,C2567,C2600,C2651	CRITICAL	SS_CAP_10UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0625	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C7360	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4912,C9486,C2500,C2520,C2560,C2567,C2600,C2651	CRITICAL	MU_CAP_10UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0627	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C7360	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4912,C9486,C2500,C2520,C2560,C2567,C2600,C2651	CRITICAL	TY_CAP_10UF

22UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0635	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	SS_CAP_22UF
138S0635	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	SS_CAP_22UF
138S0635	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	SS_CAP_22UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0676	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	MU_CAP_22UF
138S0676	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	MU_CAP_22UF
138S0676	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	MU_CAP_22UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0688	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	TY_CAP_22UF
138S0688	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	TY_CAP_22UF
138S0688	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	TY_CAP_22UF

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