

8

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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M39 - DVT

11/16/05

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
06		400374	ENGINEERING RELEASED	09/16/05	06/22/04

PAGE	DRI	PDF	CIRCUIT	
1	JD	JD	1	TABLE OF CONTENTS
2	JD	JD	2	SYSTEM BLOCK DIAGRAM
3	RT	RT	3	POWER BLOCK DIAGRAM
4	JD	JD	4	TABLE ITEMS & REVISION HISTORY
5	JD	JD	5	FUNC TEST
6	RT	RT	6	POWER CONNECTOR / POWER ALIAS
(M42) 7	MS	JD	7	CPU - BUS INTERFACE
(M42) 8	MS	JD	8	CPU - PWR & GND
9	MS	JD	9	CPU - DECAPS
(M42) 10	MS	JD	10	CPU - THERMAL SENSOR
M42 11	MS	JD	11	CPU - ITP CONN
M1 12	PS	JH	12	NB - CPU INTERFACE
M1 13	PS	JH	13	NB - VIDEO INTERFACE
14	PS	JH	14	NB - MISC INTERFACES
M1 15	PS	JH	15	NB - DDR2 INTERFACE
M1 16	PS	JH	16	NB - POWER 1
M1 17	PS	JH	17	NB - POWER 2
M1 18	PS	JH	18	NB - GROUNDS
19	PS	JH	19	NB - DECAPS
M1 20	PS	JH	20	NB - CONFIG STRAPS
21	JD	JD	21	SB - RTC, LAN, AUDIO, ATA, CPU, LPC
22	JD	JD	22	SB - PCIE, SPI, USB, DMI, PCI
23	JD	JD	23	SB - SMB, GPIO, PM, CLKS
24	JD	JD	24	SB - POWERS AND GROUNDS
25	JD	JD	25	SB - DECAPS
26	JD	JD	26	SB - MISC
27	JD	JD	27	SB - SMB BUS CONNECTIONS
28	PS	JD	28	DDR2 - SO-DIMM CONN A
29	PS	JD	29	DDR2 - SO-DIMM CONN B (REVERSED)
30	PS	JD	30	DDR2 - TERMINATION
M1 31	RT	RT	31	DDR2 - VTT SUPPLY
M42 33	JD	JD	32	CLOCKS - GENERATOR
34	JD	JD	33	CLOCKS - TERMINATIONS
38	JD	JD	34	ATA (SATA AND IDE) CONN'S
(M42) 41	JD	JD	35	LAN - YUKON'S PCIE INTERFACE
42	JD	JD	36	LAN - YUKON'S PWR, MISC
43	JD	JD	37	LAN - CONN
44	JD	JD	38	FIREWIRE - FW323-06
45	JD	JD	39	FIREWIRE - DECAPS
46	JD	JD	40	FIREWIRE - CONN'S
47	JD	JD	41	USB - CONN'S
49	JD	JD	42	USB - FLASH CONN

PAGE	DRI	PDF	CIRCUIT	
53	JD	JD	43	PCI-E - AIRPORT MINI-PCIE CONN
54	JD	JD	44	PCI-E - UNUSED PORTS
58	MS	MS	45	SMC - H8S2116
59	MS	MS	46	SMC - SMB BUSSES, MISC
60	MS	MS	47	SMC - LPC+ CONN
61	JH	JH	48	SMC - GPU/NB THERMAL SENSOR
RX 63	MS	JD	49	SMC - SPI BOOTROM
65	MS	MS	50	SMC - FANS
66	MS	MS	51	SMC - FANS
67	JD	JD	52	SMC - TPM
SO 68	PT	JD	53	AUDIO - CODEC, VREG, MIC BIAS
SO 72	PT	JD	54	AUDIO - INTERNAL SPEAKER AMP
SO 73	PT	JD	55	AUDIO - I/O CONN'S, EMC
SO 74	PT	JD	56	AUDIO - DETECT TRANSLATORS
RP 75	RT	RT	57	VR - CPU CORE
RP 76	RT	RT	58	VR - CPU I-V SENSE CKT
RP 77	RT	RT	59	VR - "S0" 1.2V & 2.5V (GRAFIX)
RP 78	RT	RT	60	VR - "S0" 1.8V
RP 79	RT	RT	61	VR - "S3" 1.8V
RP 80	RT	RT	62	VR - "S0" 1.5V
RP 81	RT	RT	63	VR - "S0" 1.05V
RP 83	RT	RT	64	VR - "S3" 3.3V AND 5V
JH 84	JH	JH	65	GPU - M56 PCI-E
M1 85	JH	JH	66	GPU - VCORE SUPPLY
M1 86	JH	JH	67	GPU - M56 CORE PWR
M1 87	JH	JH	68	GPU - M56 FRAME BUFFER
M1 88	JH	JH	69	GPU - MISC
M1 89	JH	JH	70	GPU - GDDR SDRAM A
M1 90	JH	JH	71	GPU - GDDR SDRAM B
M1 91	JH	JH	72	GPU - M56 GPIO, DVO, MISC
M1 92	JH	JH	73	GPU - M56 CLOCKS
M1 93	JH	JH	74	GPU - M56 VIDEO INTERFACES
JH 94	JH	JH	75	GPU - INTERNAL DISPLAY CONN'S
JH 95	JH	JH	76	GPU - TP'S
JH 96	JH	JH	77	GPU - TMDS, INVERTER, EXT VGA
JH 97	JH	JH	78	GPU - EXTERNAL DISPLAY CONN'S

DIMENSIONS ARE IN MILLIMETERS

XX ± _____

X.XX ± _____

X.XXX ± _____

ANGLES ± _____

DO NOT SCALE DRAWING



THIRD ANGLE PROJECTION

METRIC

DRAFTER	DESIGN CK
ENG APPD	MFG APPD
QA APPD	DESIGNER
RELEASE	SCALE
MATERIAL/FINISH NOTED AS APPLICABLE	SIZE D

 Apple Computer Inc.

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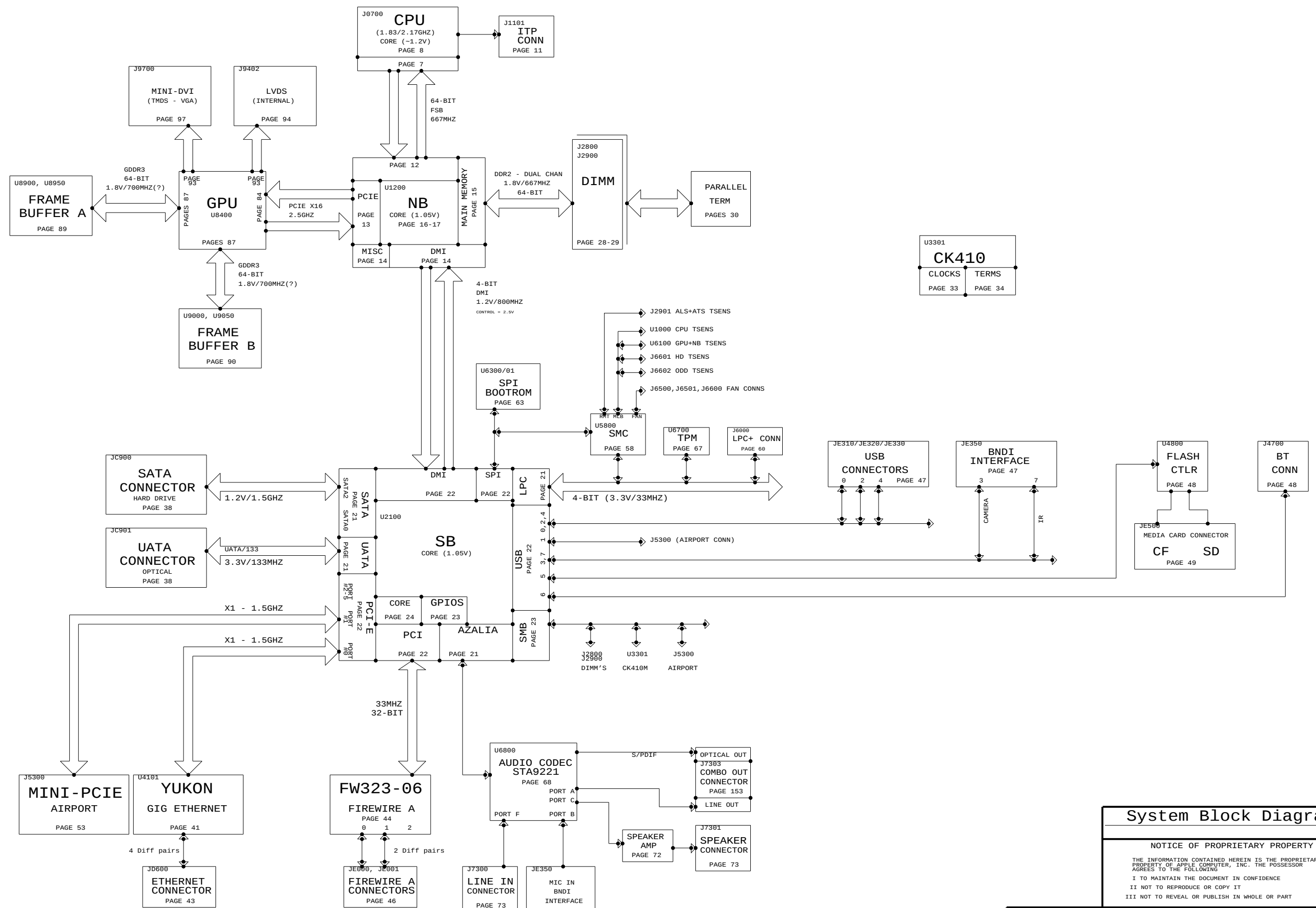
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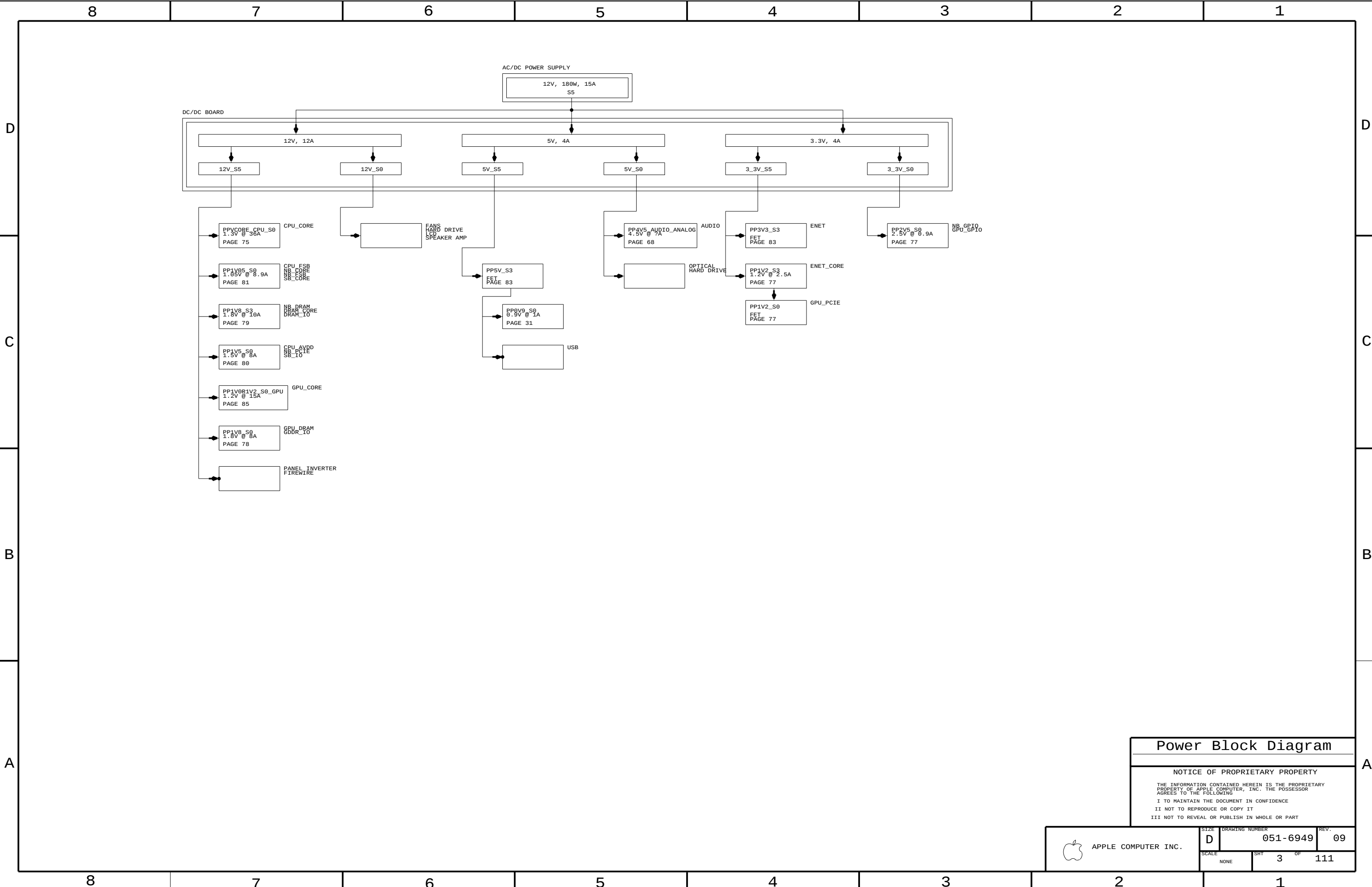
SCHEM, M39

DRAWING NUMBER 051-6950

REV. 06

SHT 1 OF 111





Power Block Diagram

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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	3	111

8765432

1

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC, CPU-SKT, 479BGA	J0700	CRITICAL	
338S0269	1	IC, 945GM, NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC, SB, 652BGA	U2100	CRITICAL	
742-0048	1	BAT, COIN, 3V, 220MAH, CR2032	BT2600	CRITICAL	
359S0101	1	IC, CY28445-5, CLK GEN, 68PIN QFN	U3301	CRITICAL	
338S0270	1	IC, BB8053, GIGABIT ENET XCVR, 64P QFN, NO	U4101	CRITICAL	
341S1797	1	IC, ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC, FW32306, 1394A LINK, TQFP	U4400	CRITICAL	
338S0274	1	IC, SMC, HS8/2116, BLANK	U5800	CRITICAL	
341S1789	1	IC, TPM, TSSOP, 28P	U6700	CRITICAL	LEMENU
352S1235	1	IC, CPU VREG, IMPV, TWO PHASE	U7500	CRITICAL	
338S0266	1	IC, ATI, M56P, GRAFAX CTLR, 880BGA, LF	U8400	CRITICAL	ATI_B24
338S0305	1	IC, ATI, M56P, GRAFAX CTLR, 880BGA, LF	U8400	CRITICAL	ATI_A24
128S0078	3	CAP, EL, AL, 330UF, 20%, 16V, 10X12.7MM, SMD, LF	C7517, C7518, C7910	CRITICAL	

M38

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-6949	1	PCB, SCHEM, MLB, M38	SCH1		17_INCH_LCD
820-1919	1	PCB, FAB, MLB, M38	MLB1		17_INCH_LCD
341T0003	1	EFI ROM, M38	U6301	CRITICAL	17_INCH_LCD
337S3241	1	M38/M39 LOW-SPEED CPU (QINY)	CPU	CRITICAL	CPU_M38
337S3242	1	M00-SPEED CPU (QINZ)	CPU	CRITICAL	CPU_M00

M39

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-6950	1	PCB, SCHEM, MLB, M39	SCH1		20_INCH_LCD
820-1888	1	PCB, FAB, MLB, M39	MLB1		20_INCH_LCD
341T0004	1	EFI ROM,M39	U6301	CRITICAL	20_INCH_LCD
337S3243	1	M39 HI-SPEED CPU (QHJJ)	CPU	CRITICAL	CPU_M39

M38 / M39

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136FBGA	U9000, U9050, U9000, U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136FBGA	U9000, U9050, U9000, U9050	CRITICAL	ATI_FB_128M_HYNIX

M39 - CT0

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136FBGA	U8900, U9550, U9000, U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136FBGA	U8900, U9550, U9000, U9050	CRITICAL	ATI_FB_256M_HYNIX

PART NUMBER	ALTERNATE PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
126S0096	126S0076		C7801	SANYO M16CE680KX 680UF 1F	LF
126S0086	126S0078		C699, C640, C1900, C1801, C1568	SANYO M6CE330F5 330UF 6.3V	LF
126S0080	126S0078		C7527, C7518, C7910	SANYO 165VP330M 330UF 16V	SHD LF
197S9177	197S9020		U4101	XTAL, 25MHZ, 50PPM, 15PF, 3.2X2.5	SHD, LF
338S0302	338S0266		U8400	IC, ATI, M360, GRAFIC CTLR, 8MB, 16V	LF

Table Items

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SCALE

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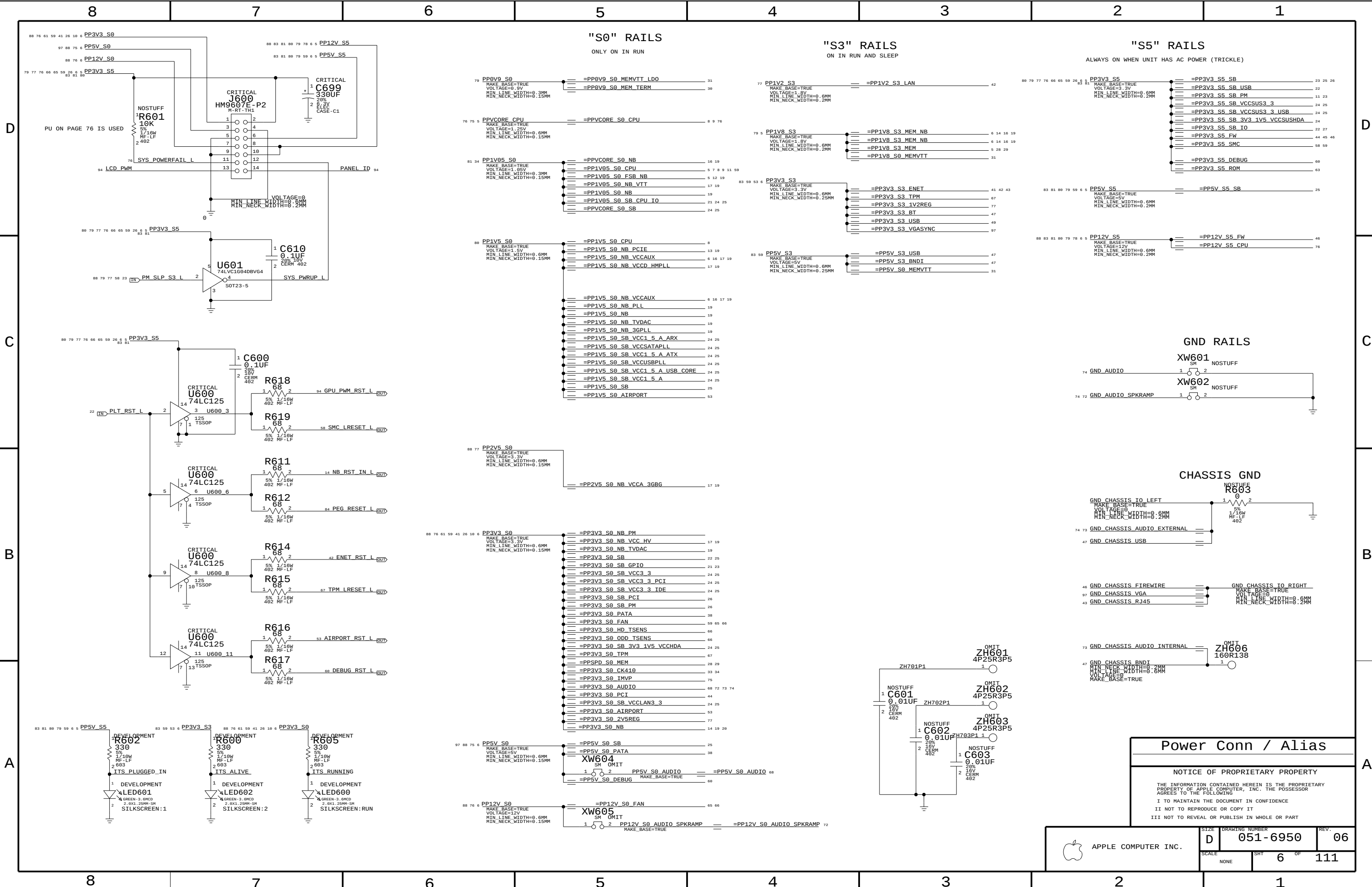
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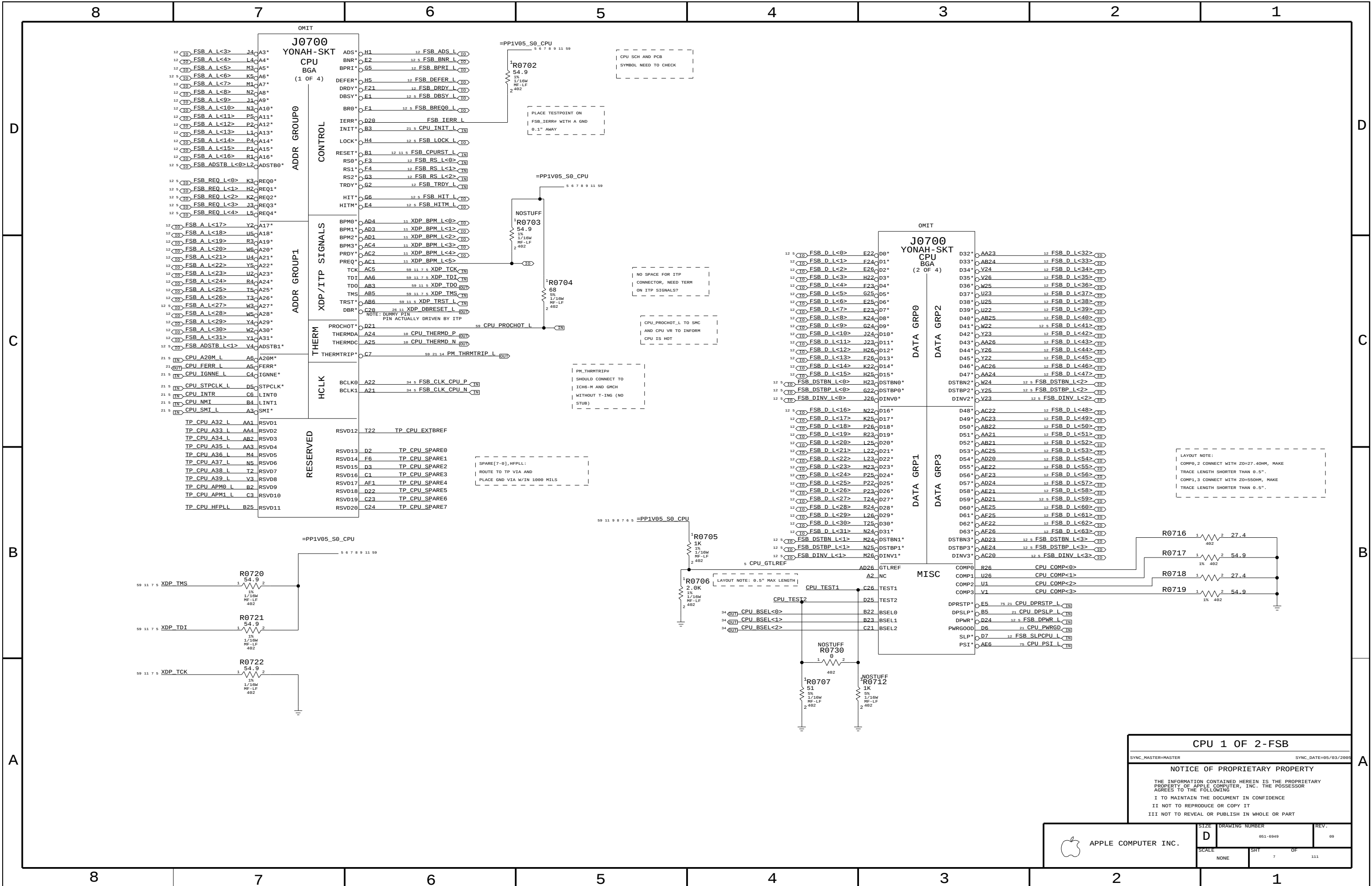
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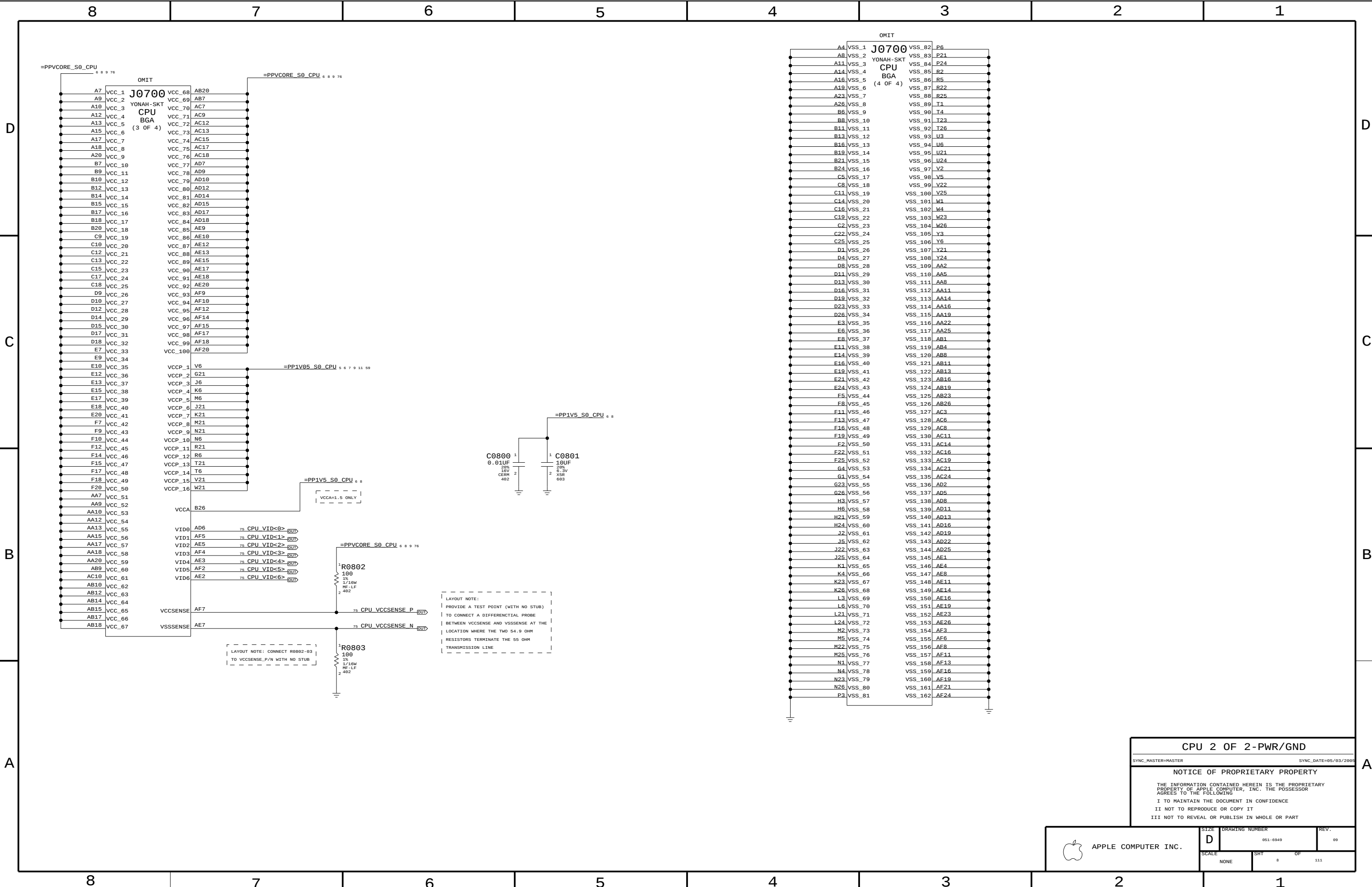
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Power Conn / Alias		
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D	051-6950	06
SCALE	SHT	6 OF 111
NONE		







CPU 2 OF 2-PWR/GND

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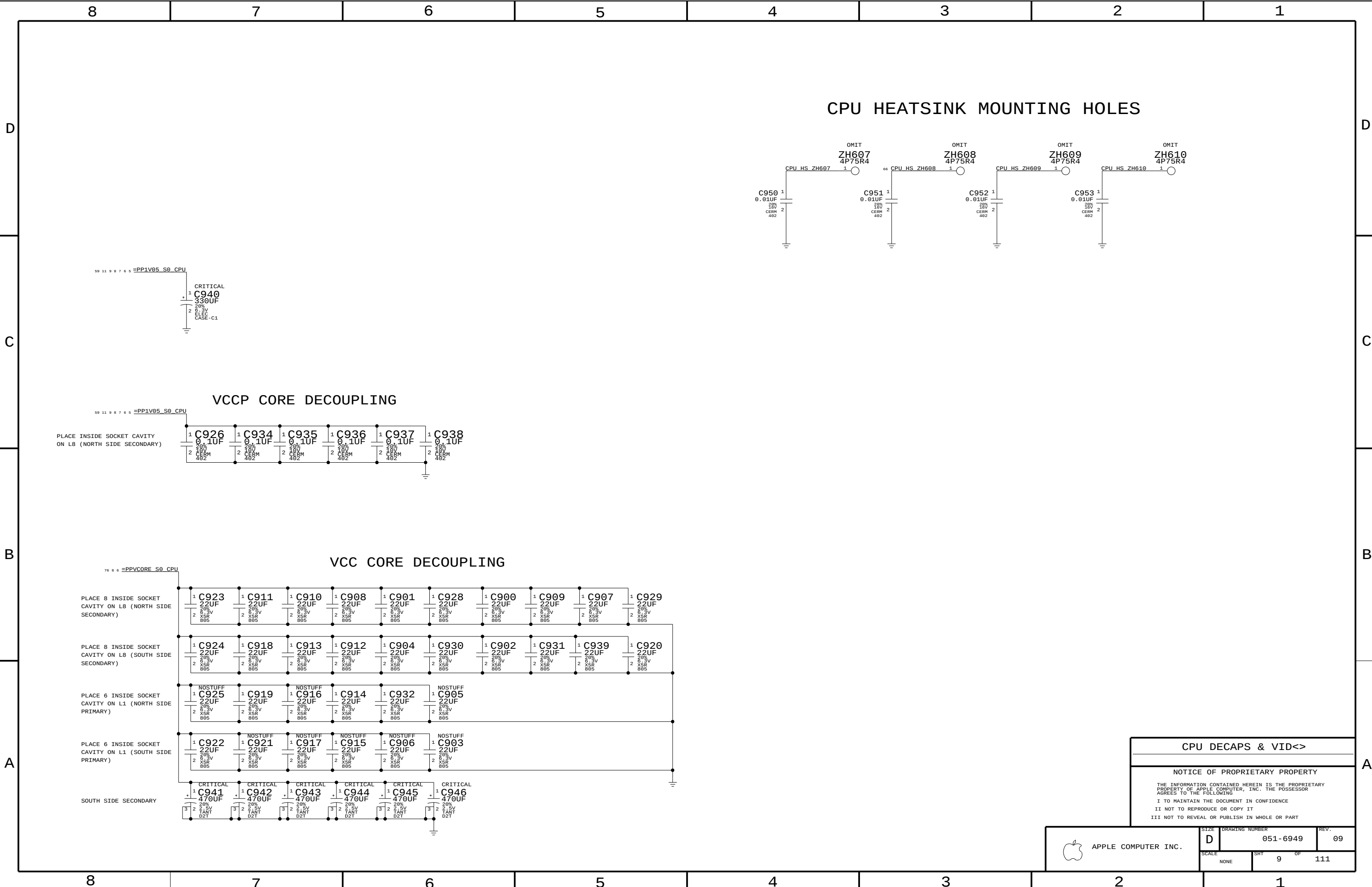
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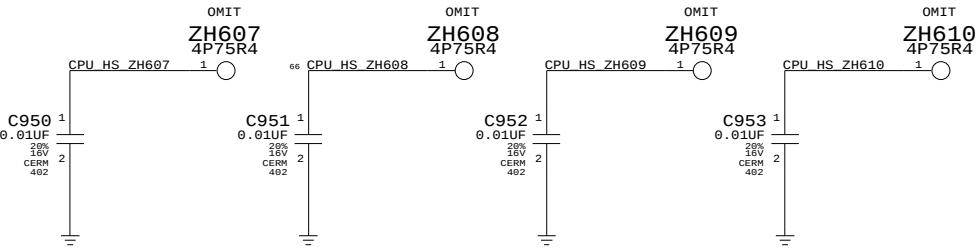
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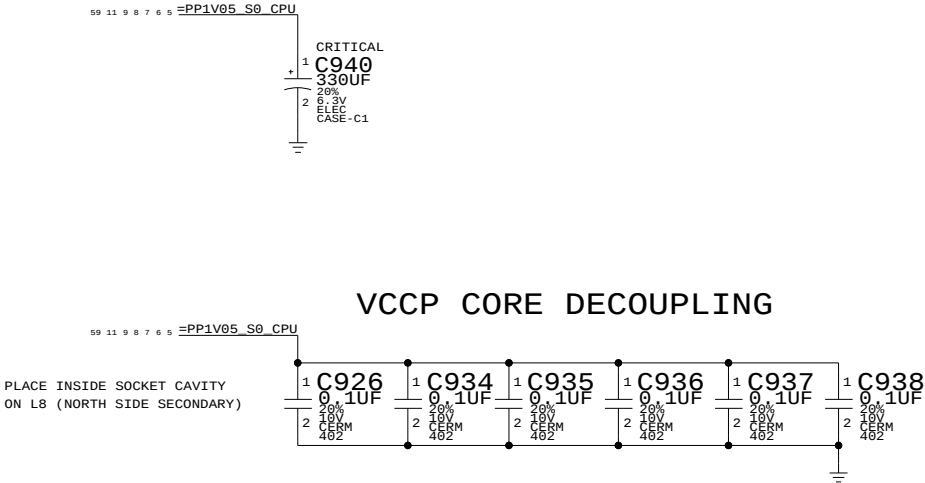
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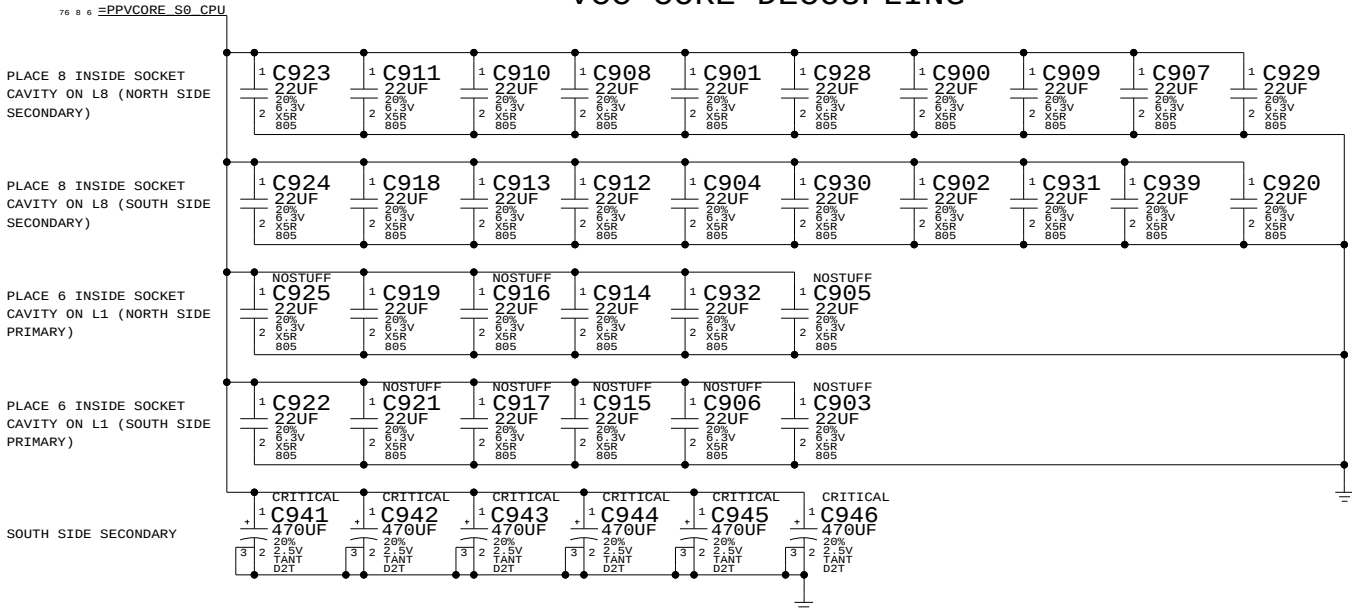
CPU HEATSINK MOUNTING HOLES



VCCP CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

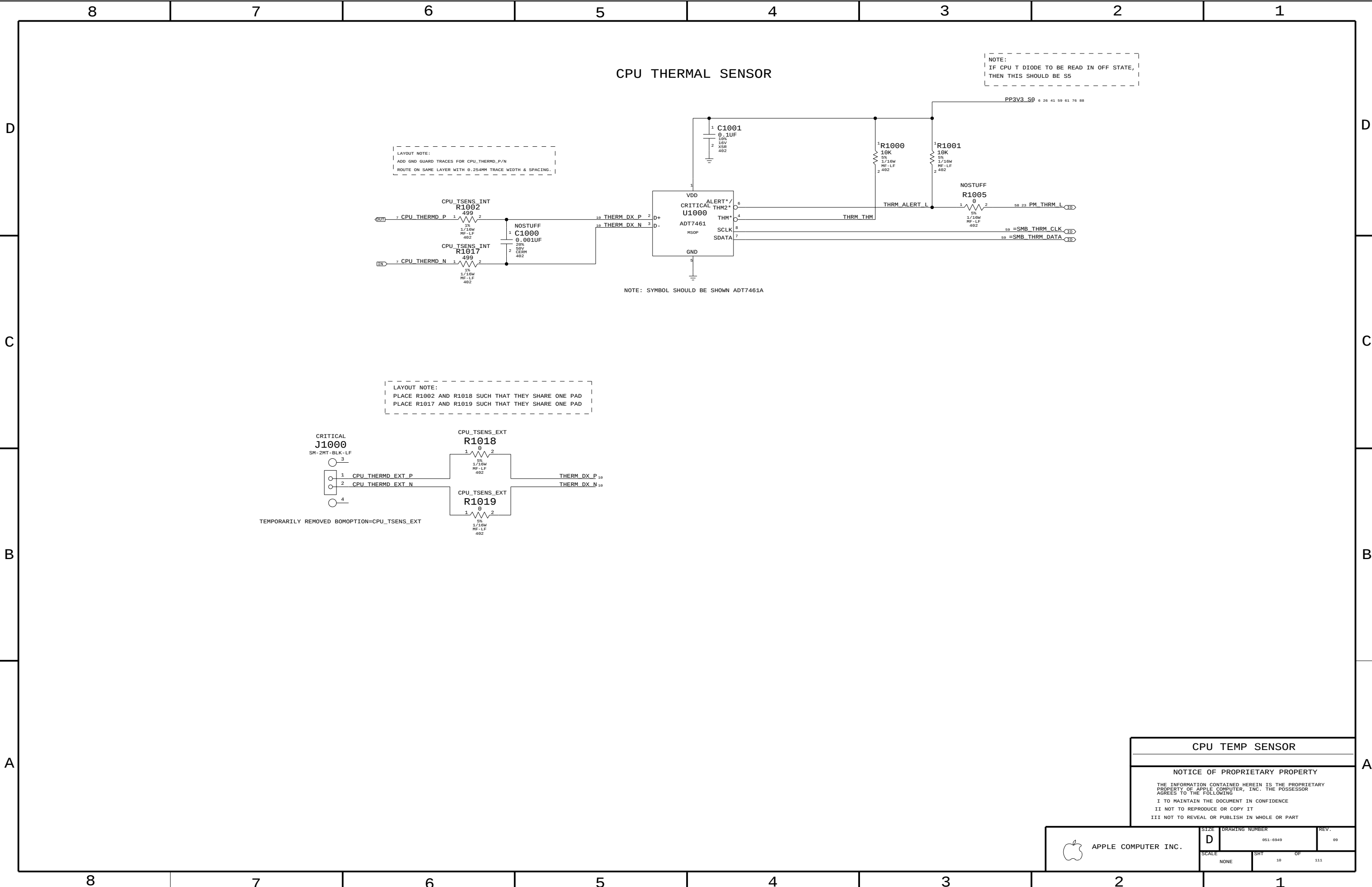
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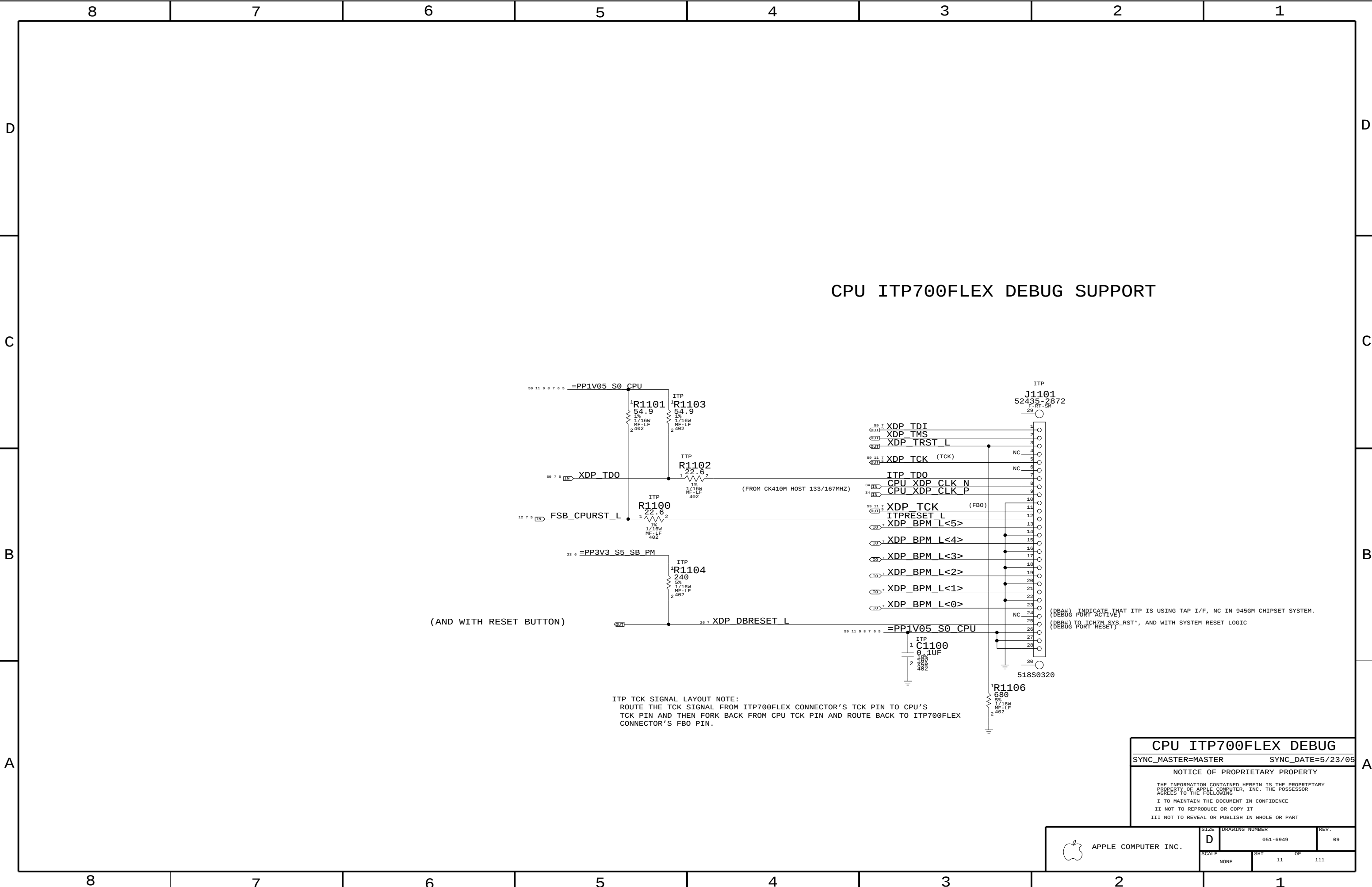
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NONE	9	111





CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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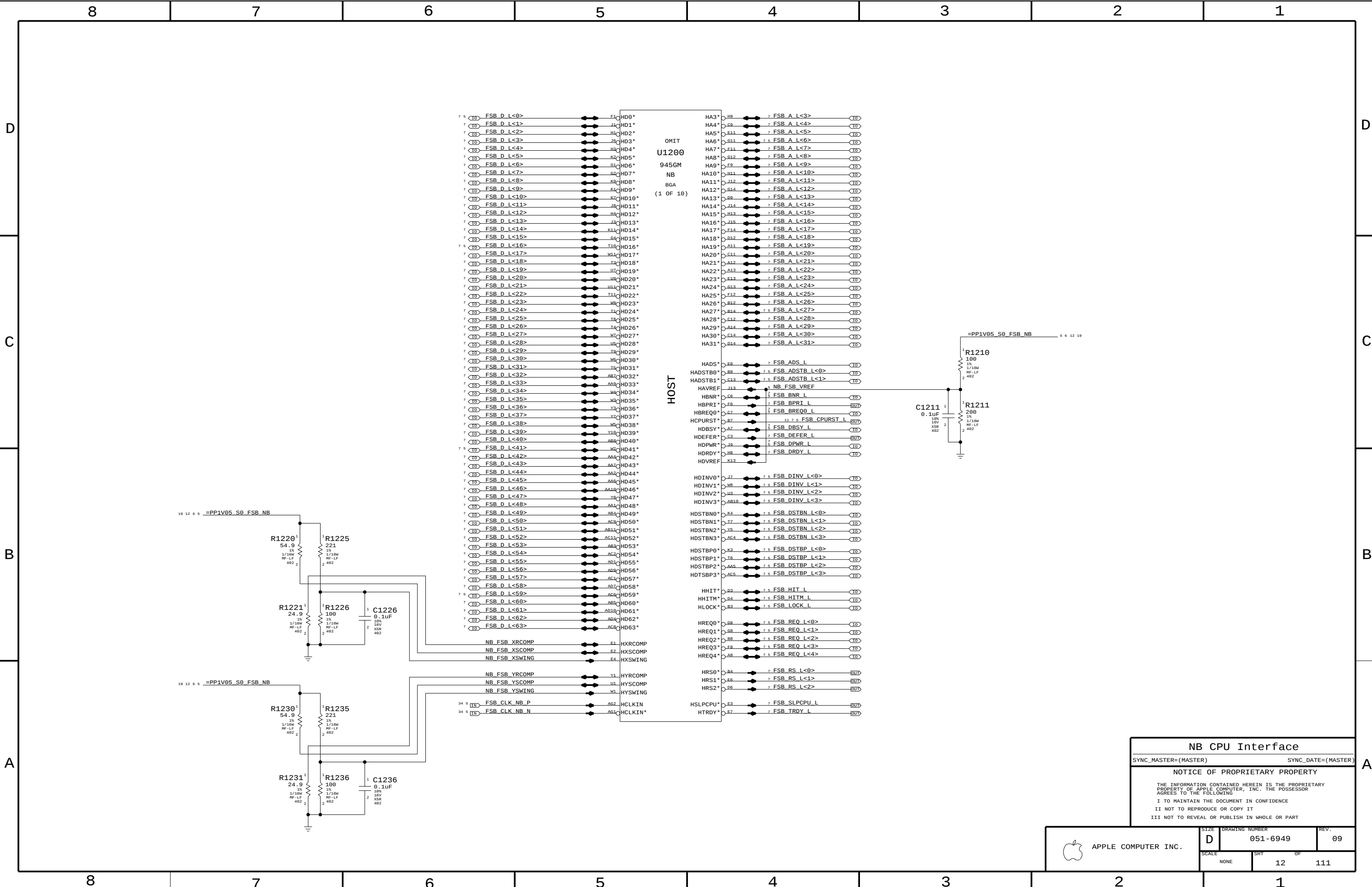
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NONE		11	111



NB CPU Interface

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SYNC_DATE=(MASTER)

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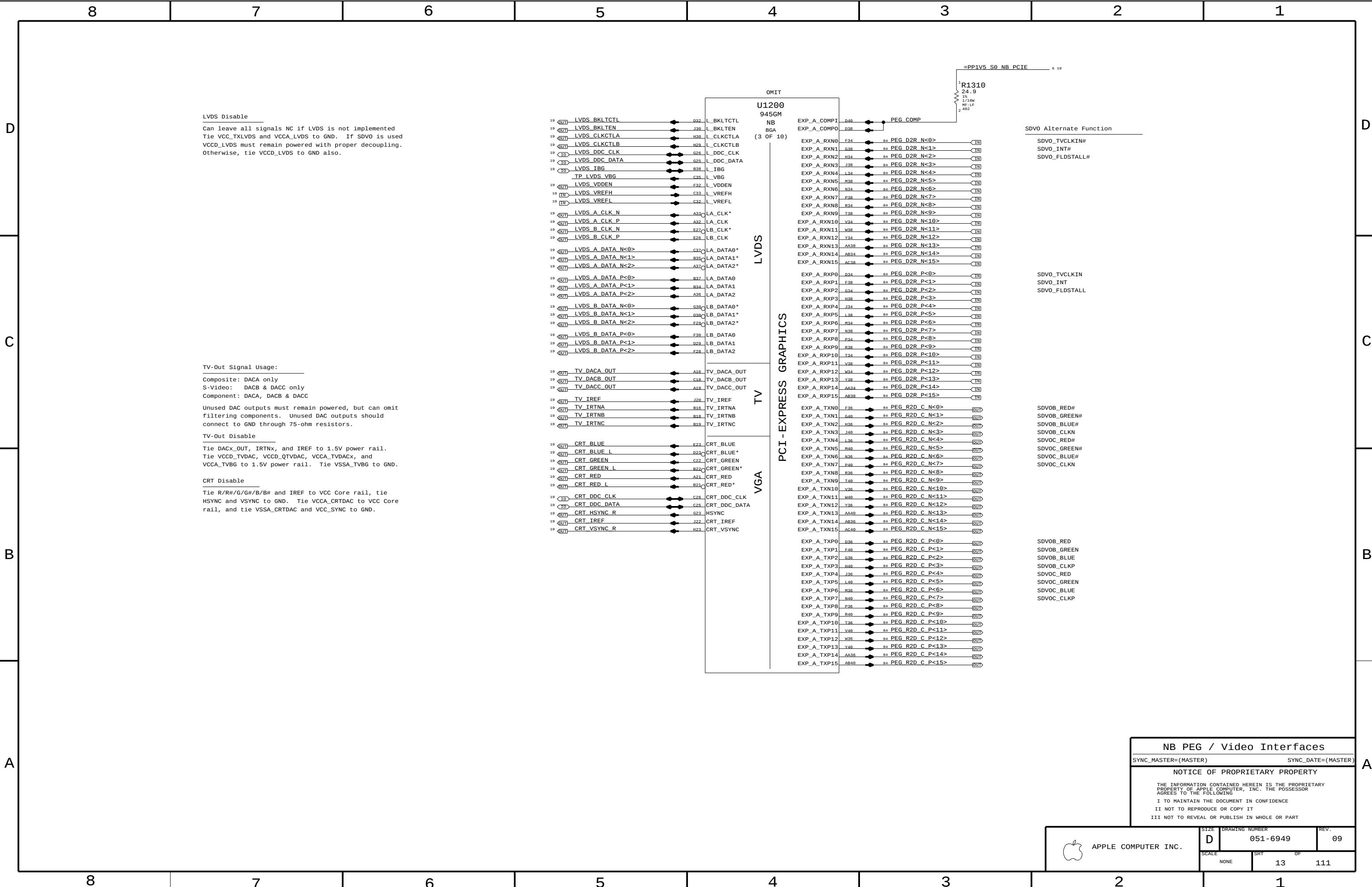
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REV. 09

SCALE NONE

SHT 12

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

NB PEG / Video Interfaces

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

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SIZE

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DRAWING NUMBER

051-6949

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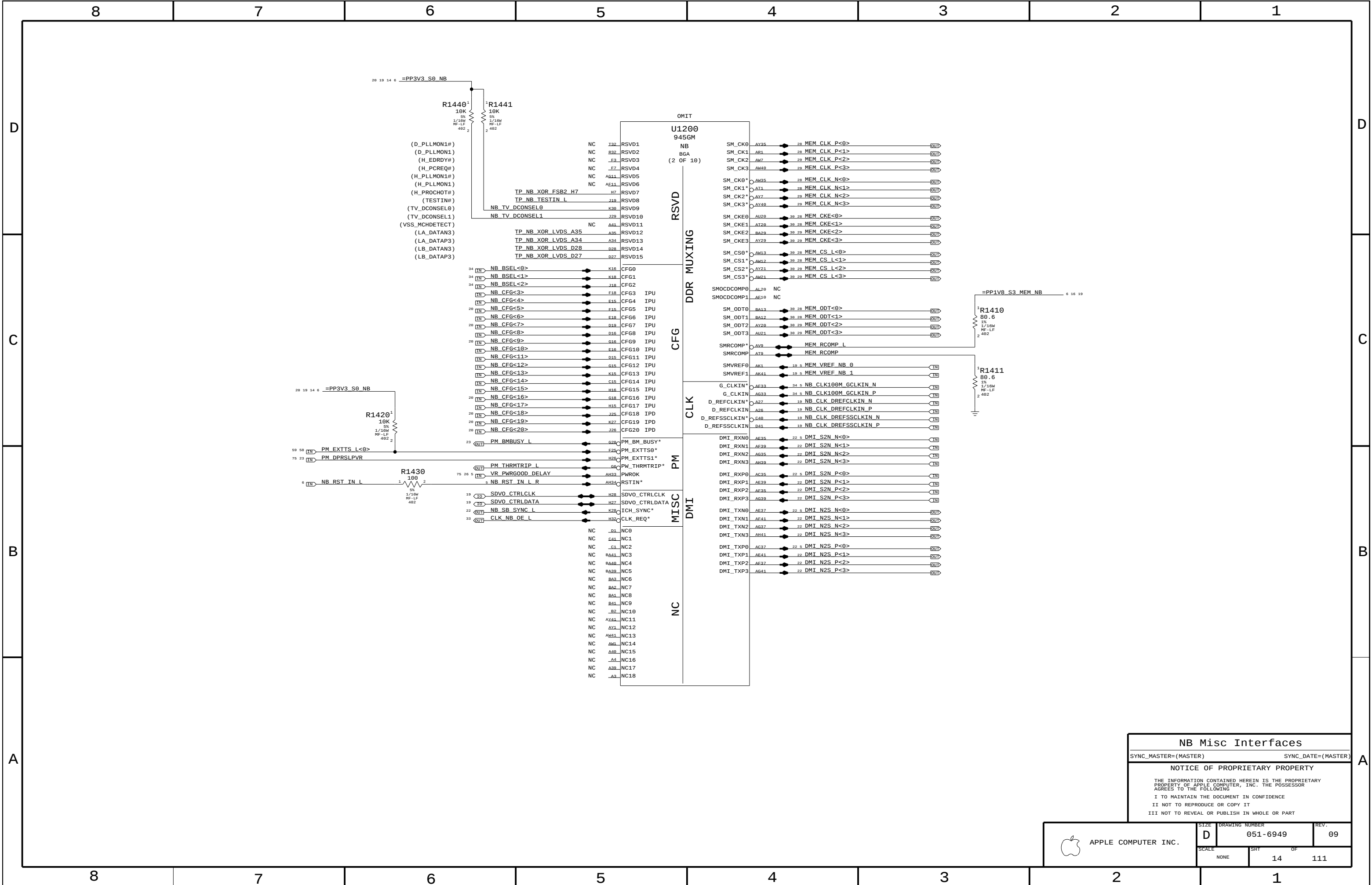
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111



NB Misc Interfaces

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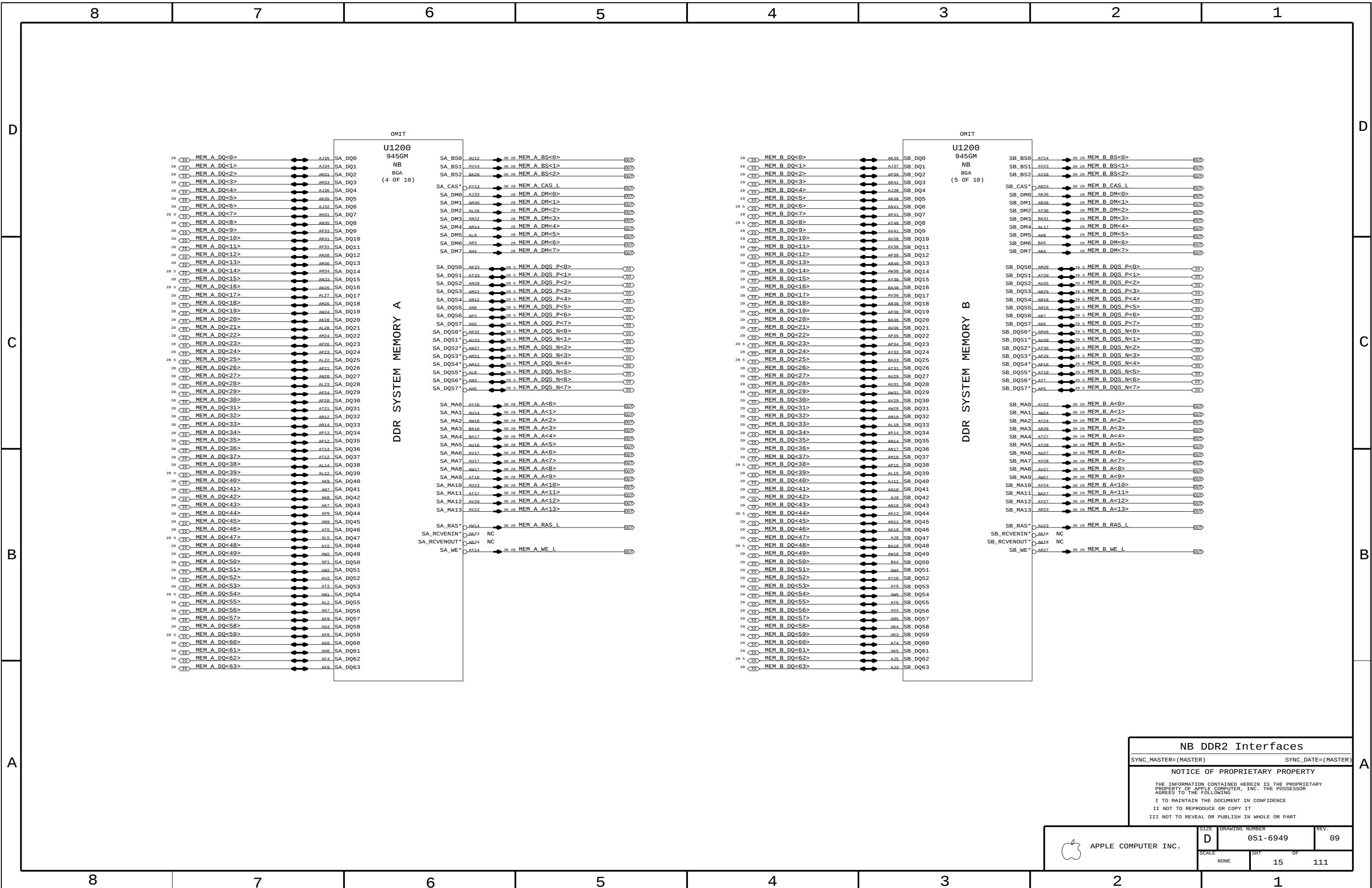
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NB DDR2 Interfaces

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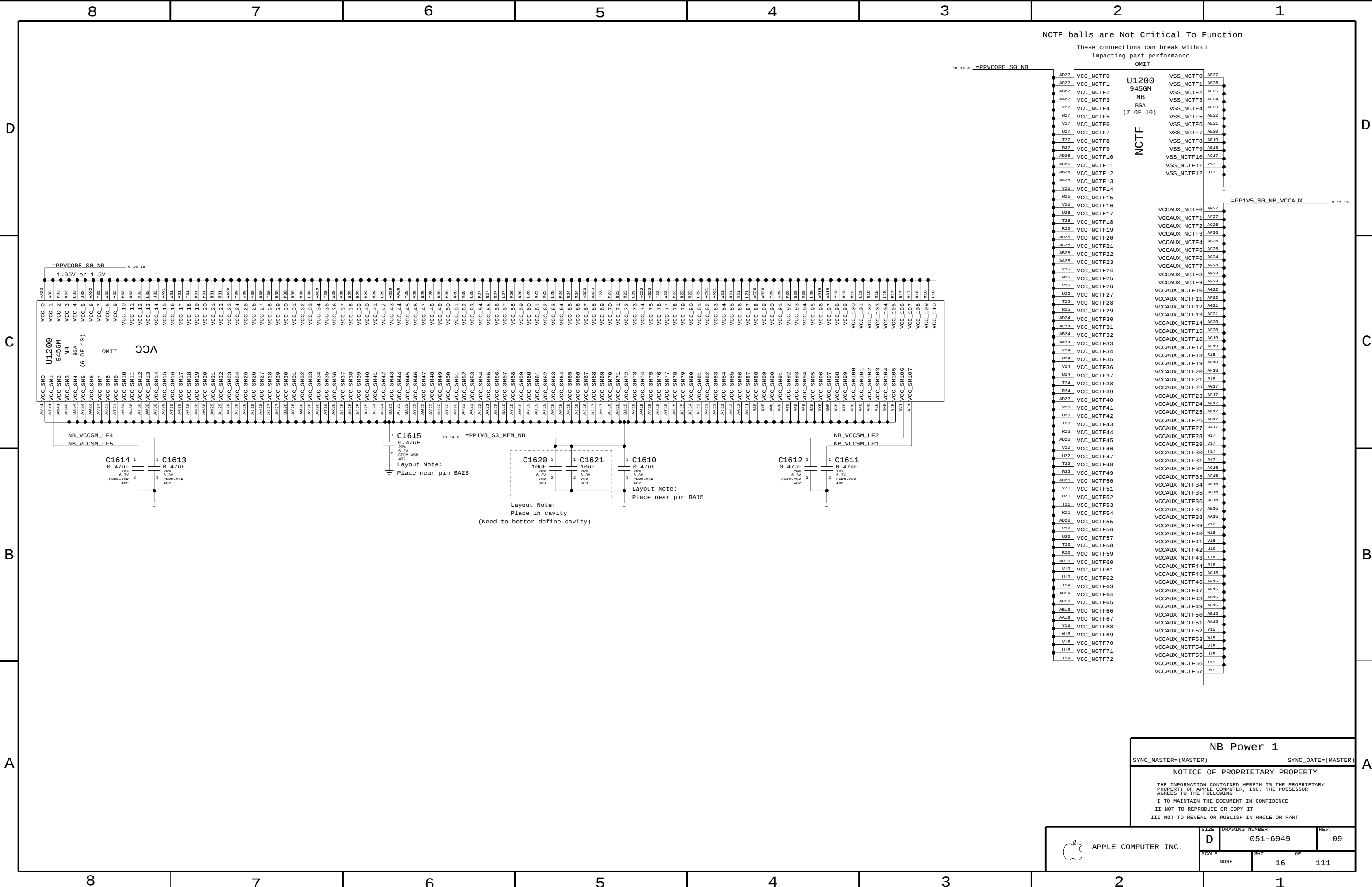
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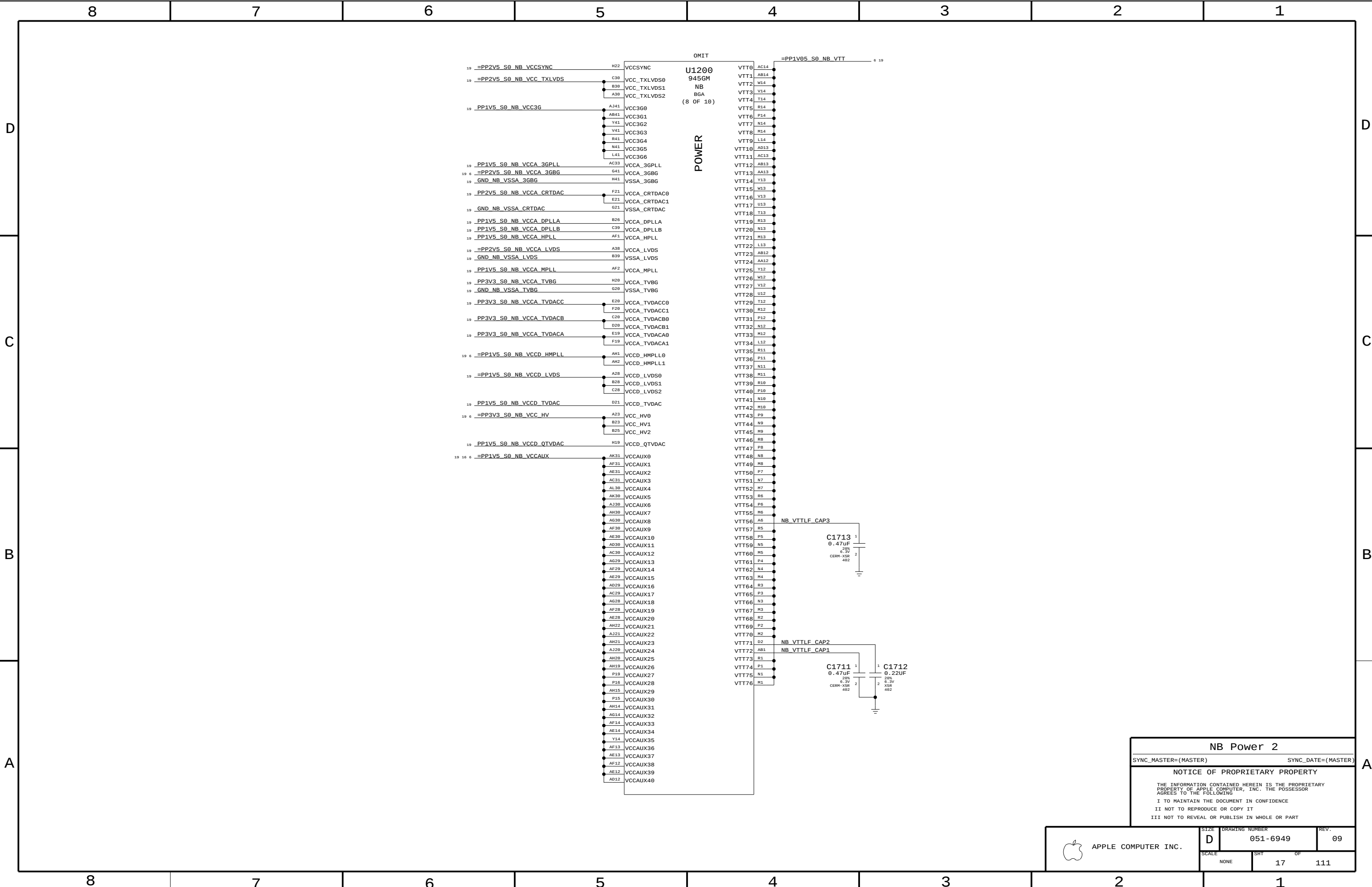
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NB Power 2

SYNC_MASTER=(MASTER)SYNC_DATE=(MASTER)

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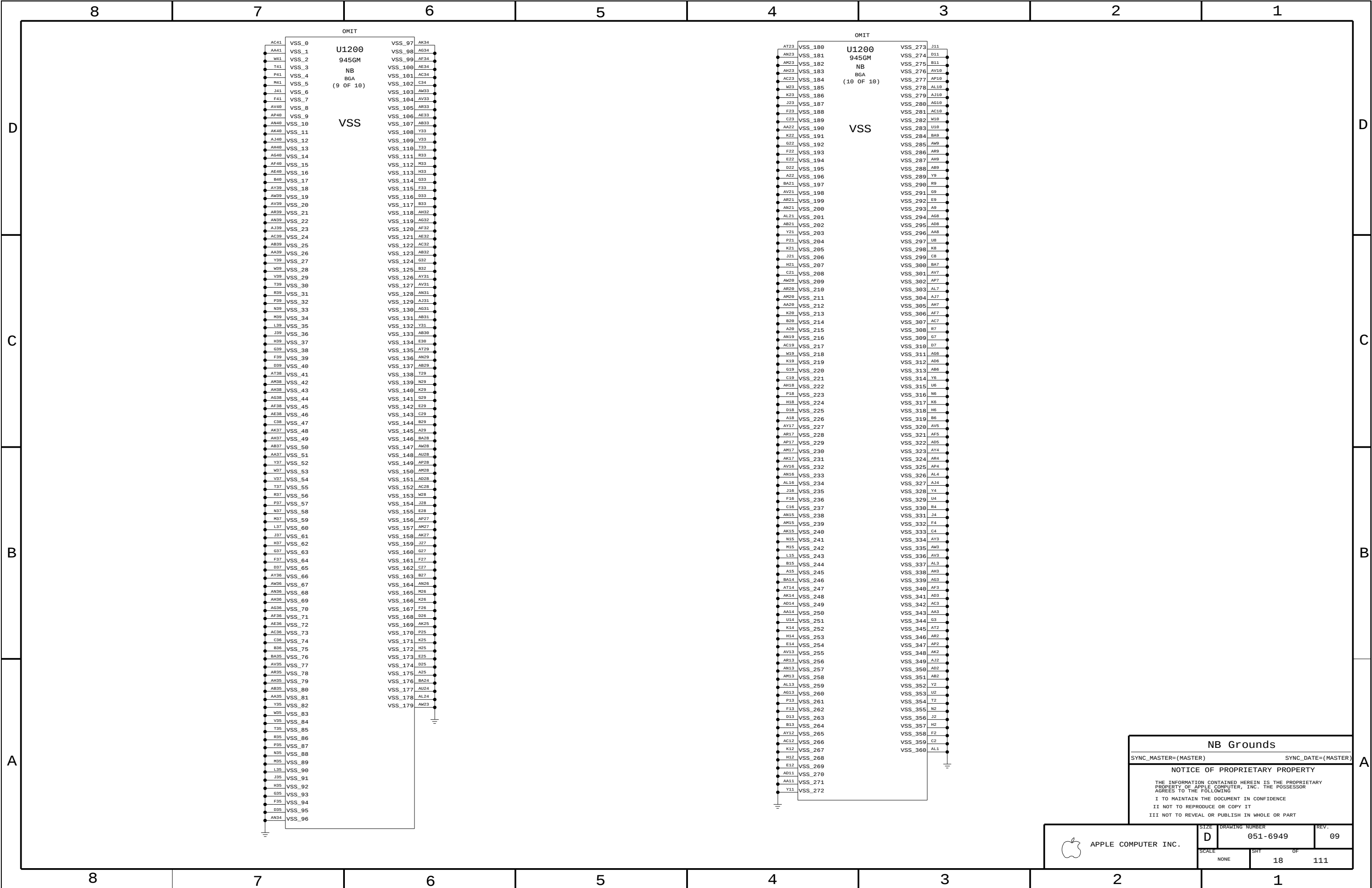
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	D	051-6949	09
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NONE		17	111



NB Grounds

SYNC_MASTER=(MASTER)

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APPLE COMPUTER INC.

SCALE
NONE

D

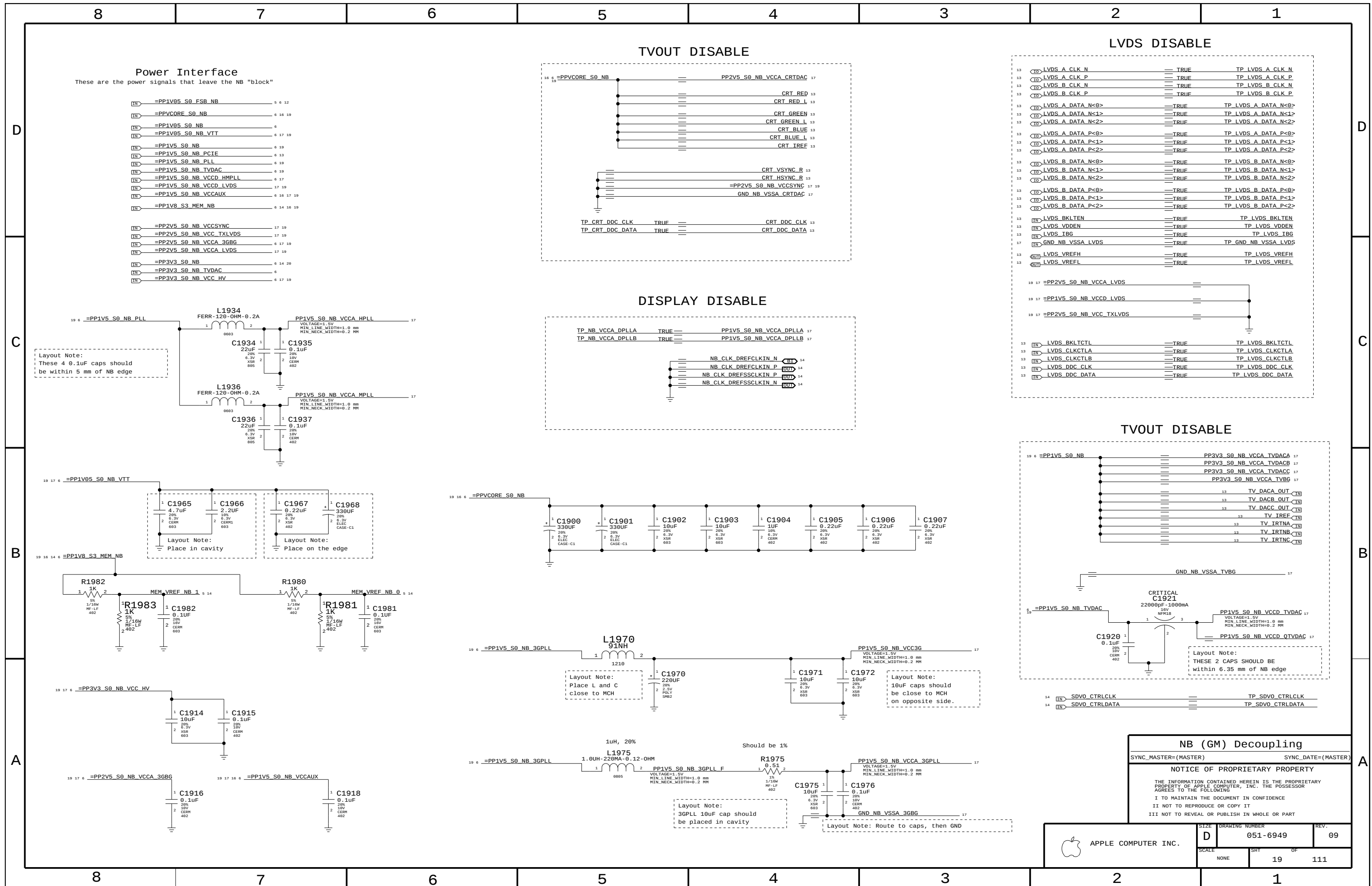
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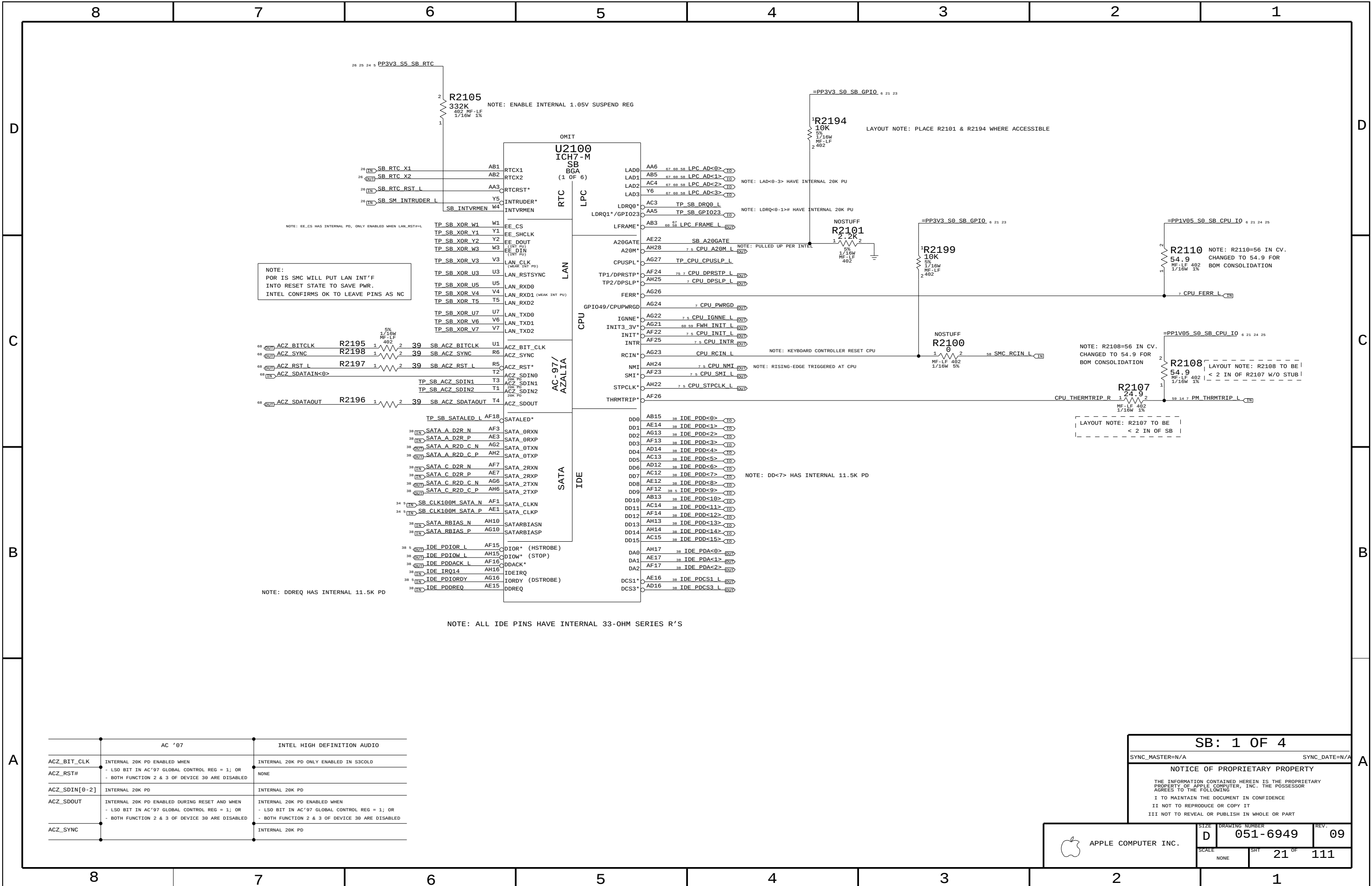
DRAWING NUMBER
051-6949

REV.
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NOTE:
POR IS SMC WILL PUT LAN INT'F
INTO RESET STATE TO SAVE PWR.
INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '97		INTEL HIGH DEFINITION AUDIO	
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR	INTERNAL 20K PD ONLY ENABLED IN S3COLD	
ACZ_RST#	- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE	
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD	
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR	
	- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	
ACZ_SYNC		INTERNAL 20K PD	

SB: 1 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

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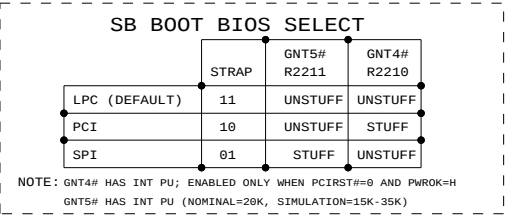
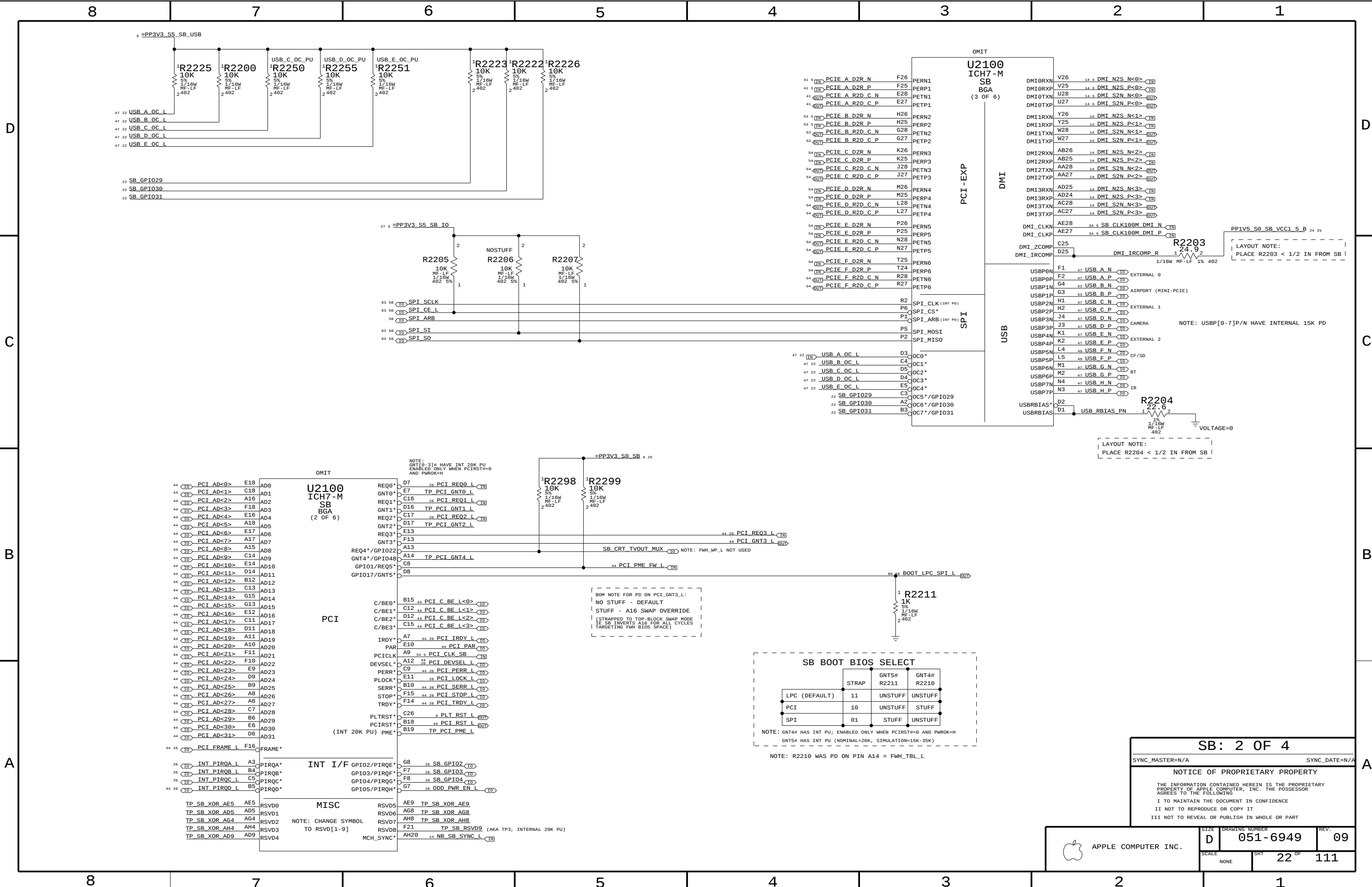
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SIZE: D DRAWING NUMBER: 051-6949 REV.: 09

SCALE: NONE SHY: 21 OF 111



SB: 2 OF 4

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SYNC_DATE=N/A

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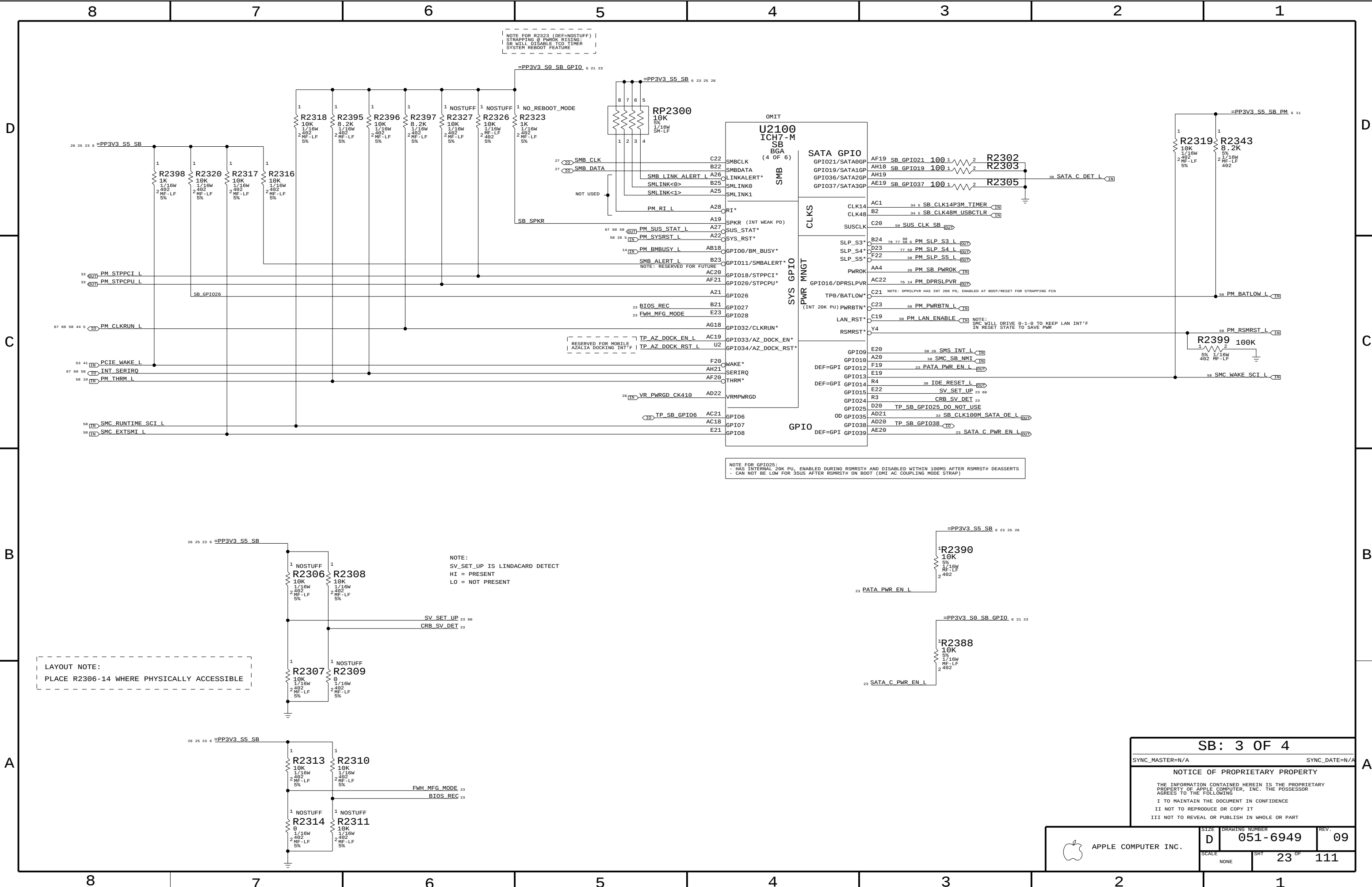
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SCALE

NONE

SHT

22 OF 111



NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (OWI AC COUPLING MODE STRAP)

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4

SYNC_MASTER=N/A

SYNC_DATE=N/A

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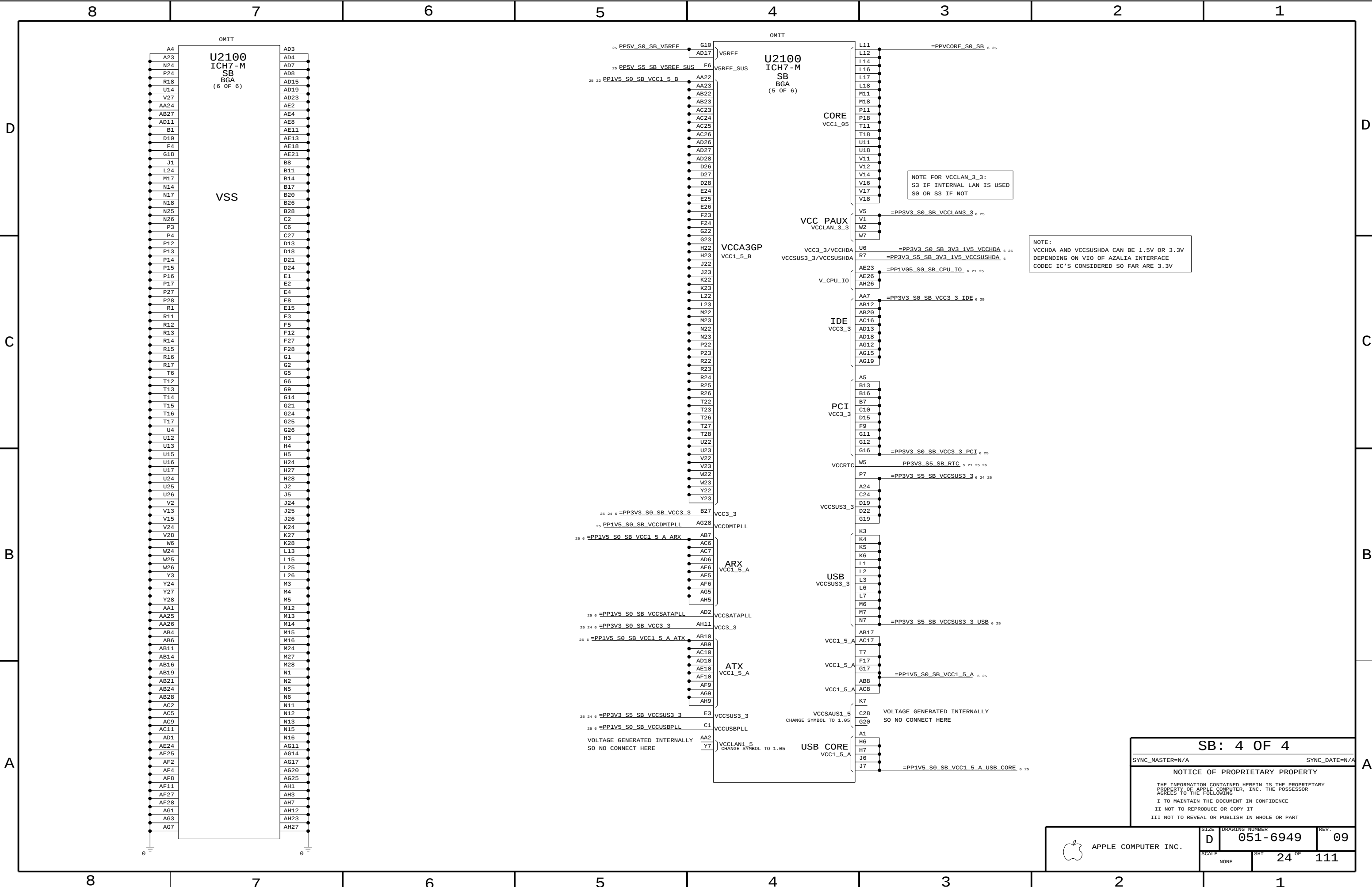
SIZE D

DRAWING NUMBER 051-6949

REV. 09

SCALE NONE

SHT 23 OF 111



SB: 4 OF 4

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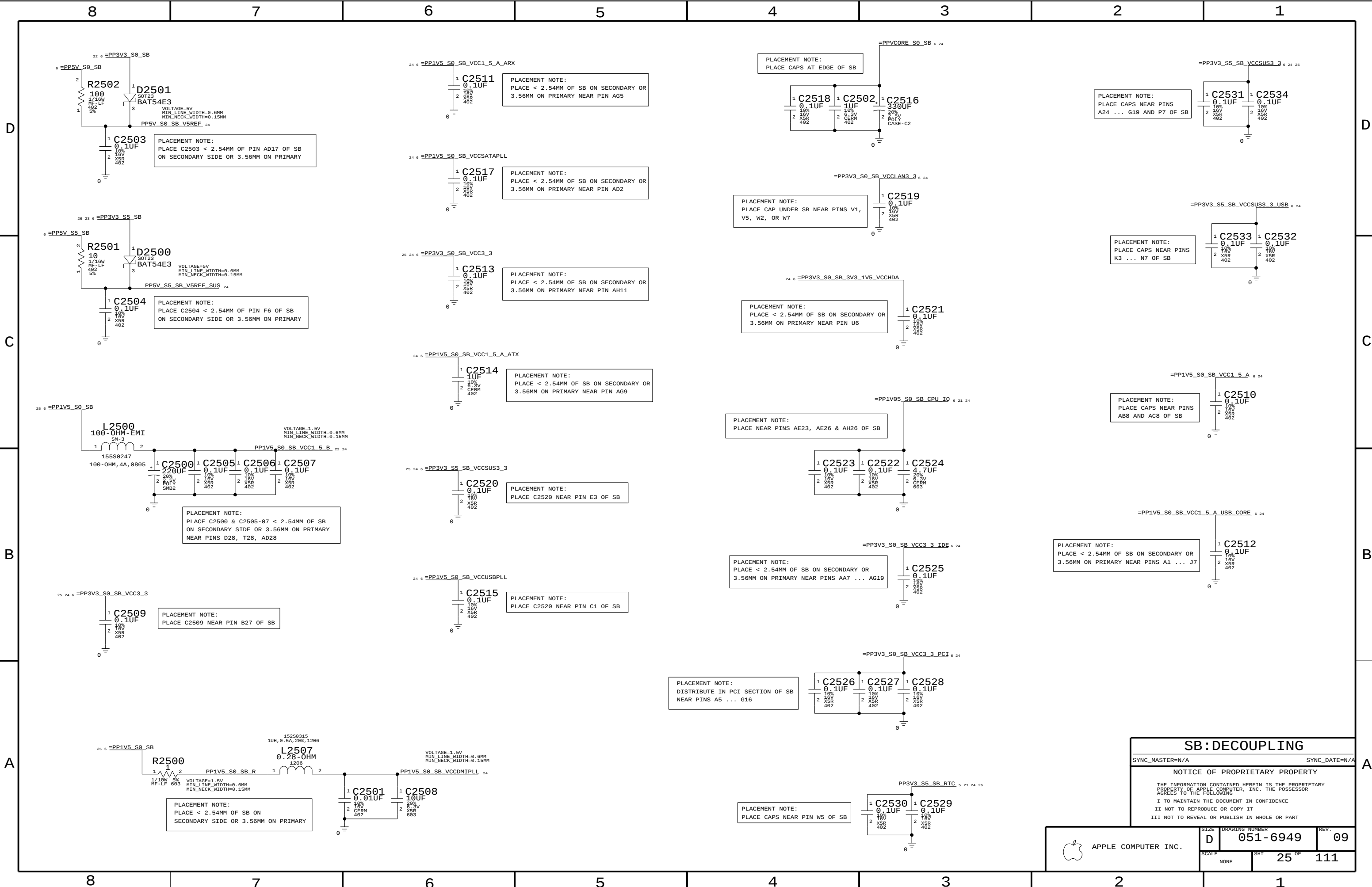
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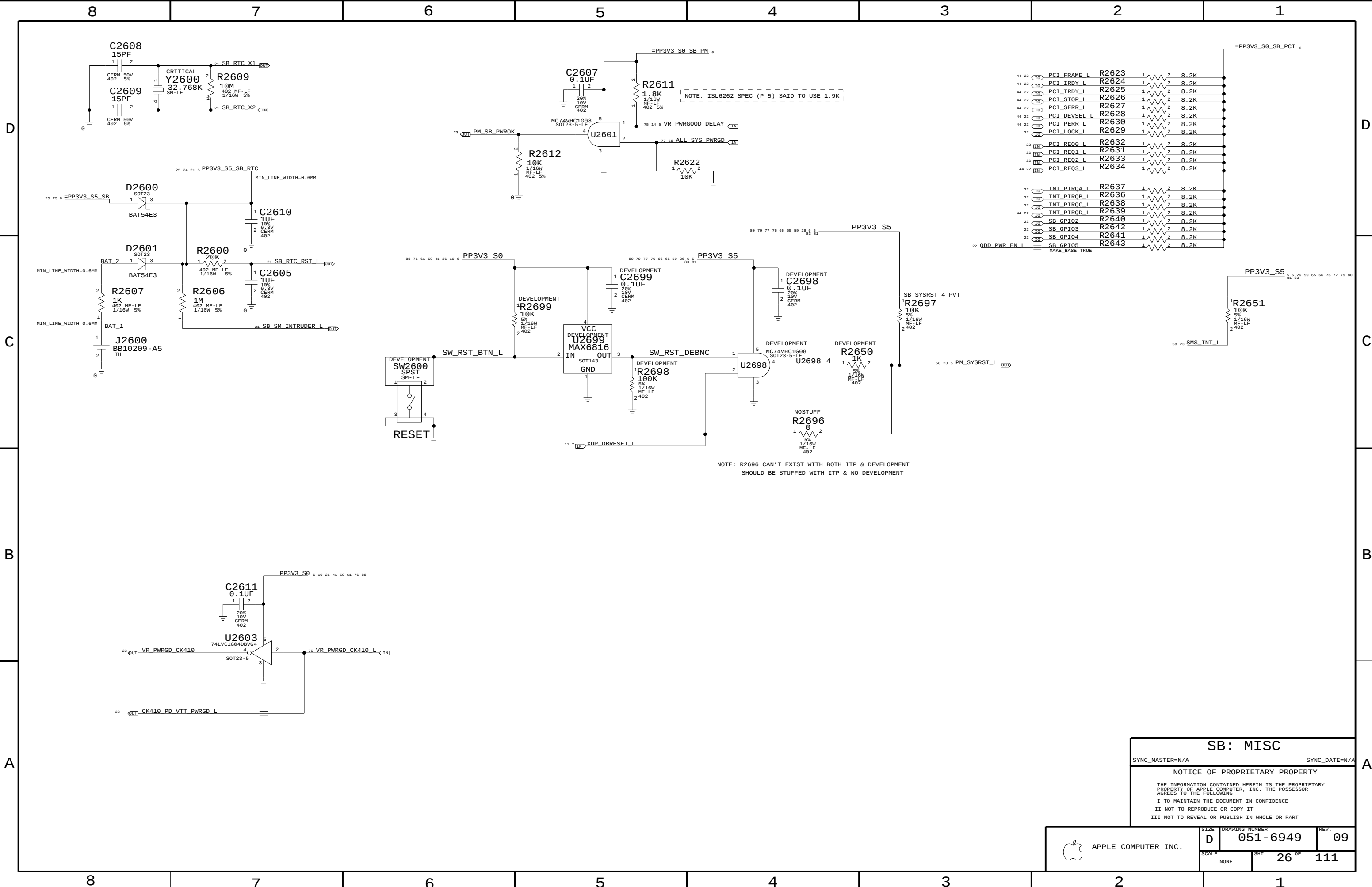
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE		SHY	24 OF 111
NONE			





SB: MISC

SYNC_MASTER=N/A

SYNC_DATE=N/A

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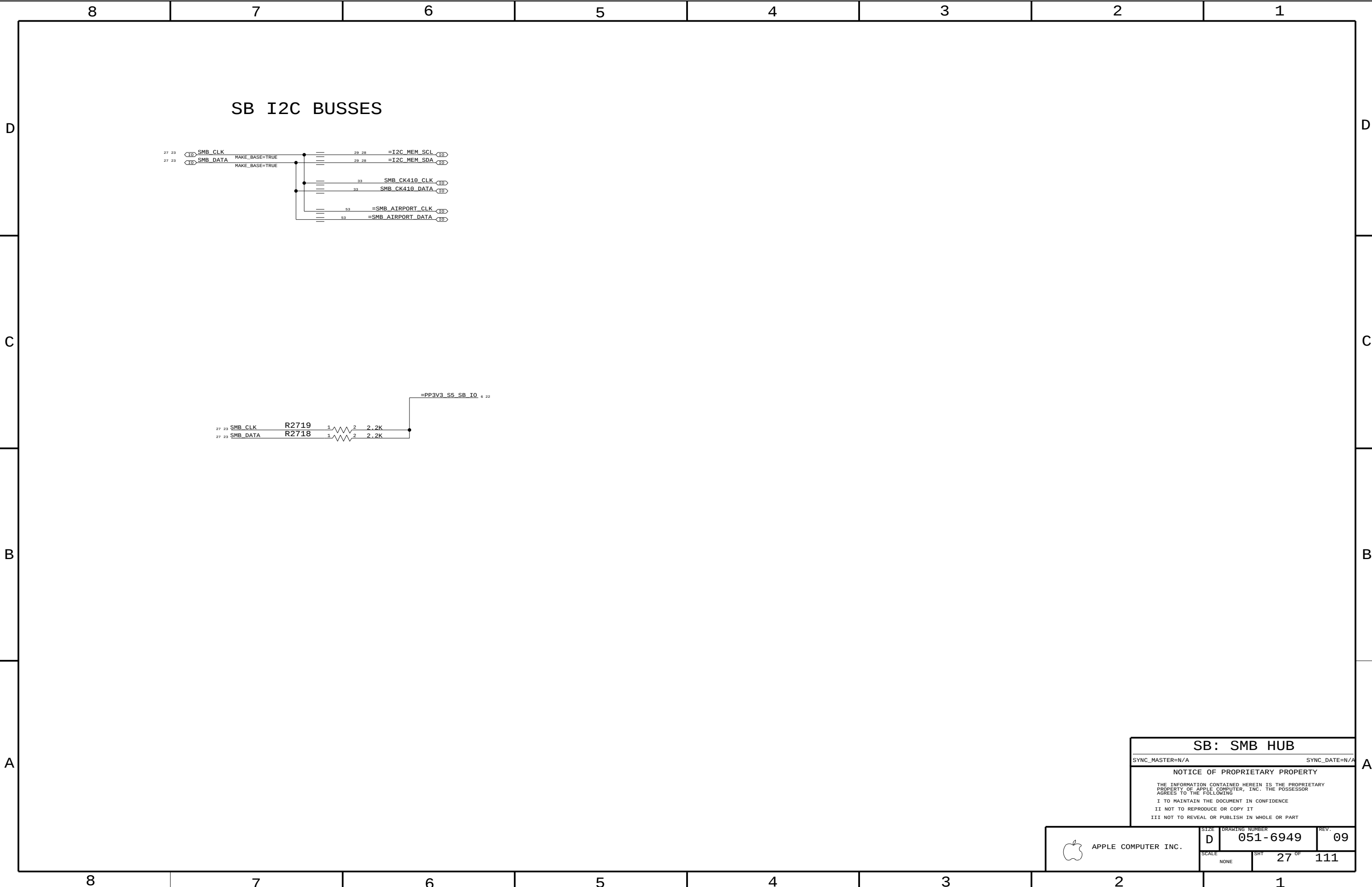
SCALE
NONE

D

DRAWING NUMBER
051-6949

SHT
26 OF 111

REV.
09



Power aliases required by this page:

- PP1V8_S3_MEM
- PPSPD_S0_MEM (2.5V ~ 3.3V)

Signal aliases required by this page:

- I2C_MEM_SCL
- I2C_MEM_SDA

BOM options provided by this page:

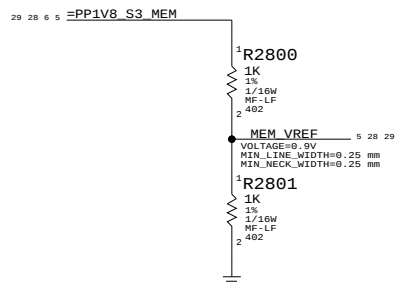
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Signal aliases required by this page:

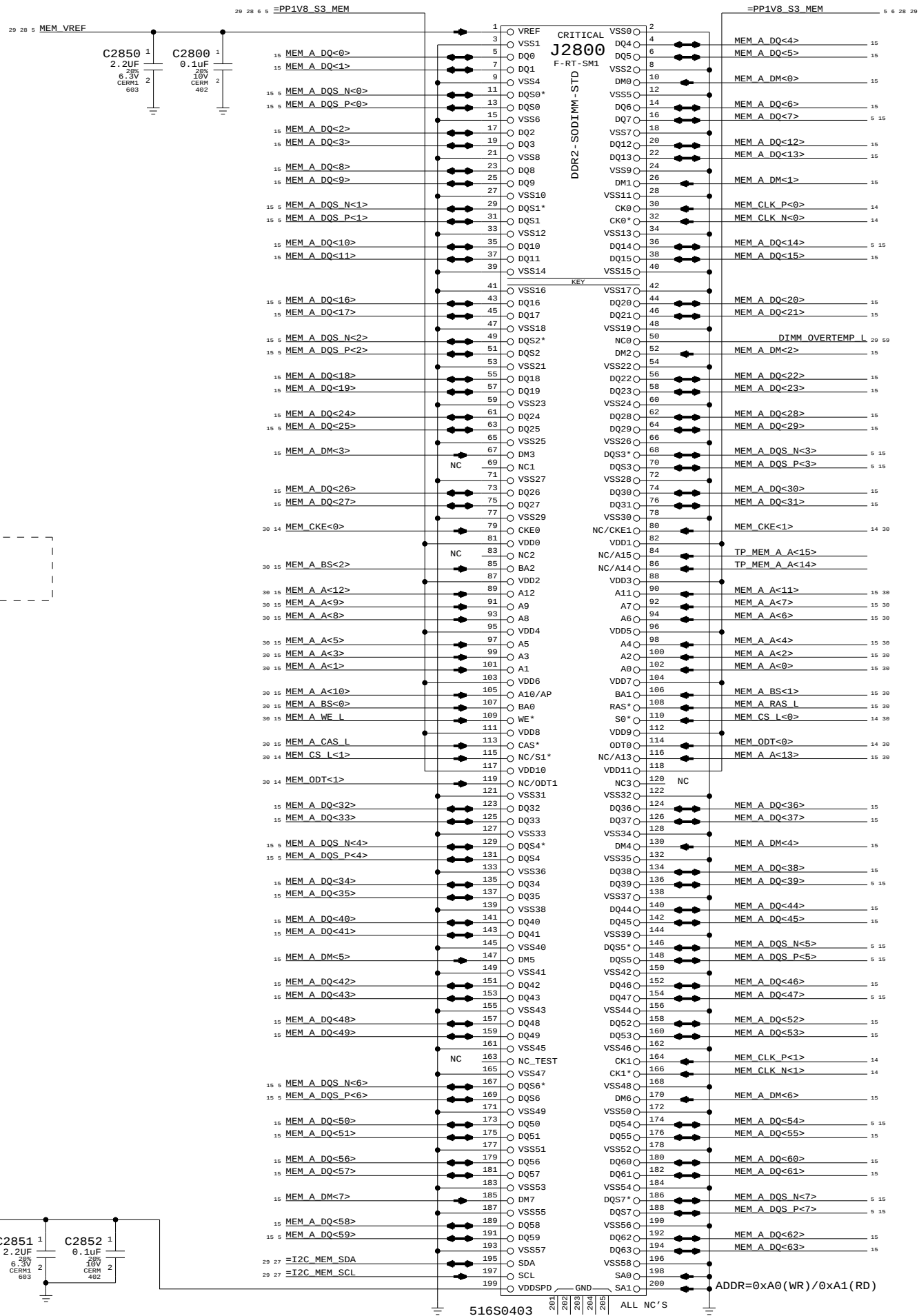
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

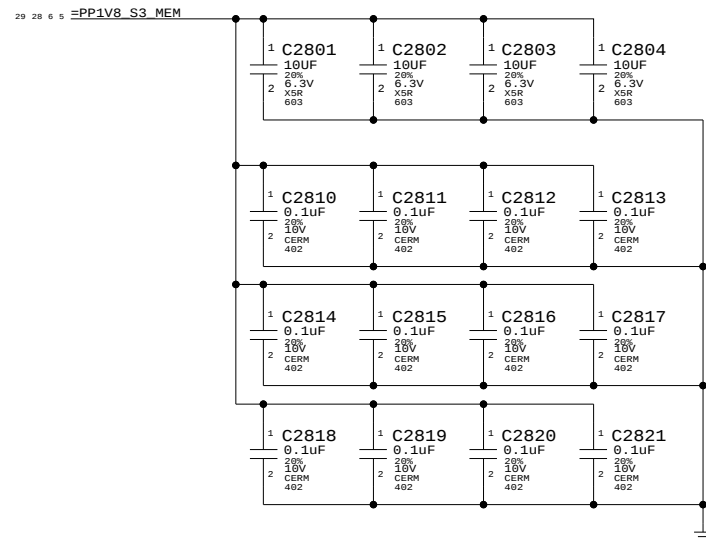
One 0.1uF per connector



Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)



(For return current)



SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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D	051-6949
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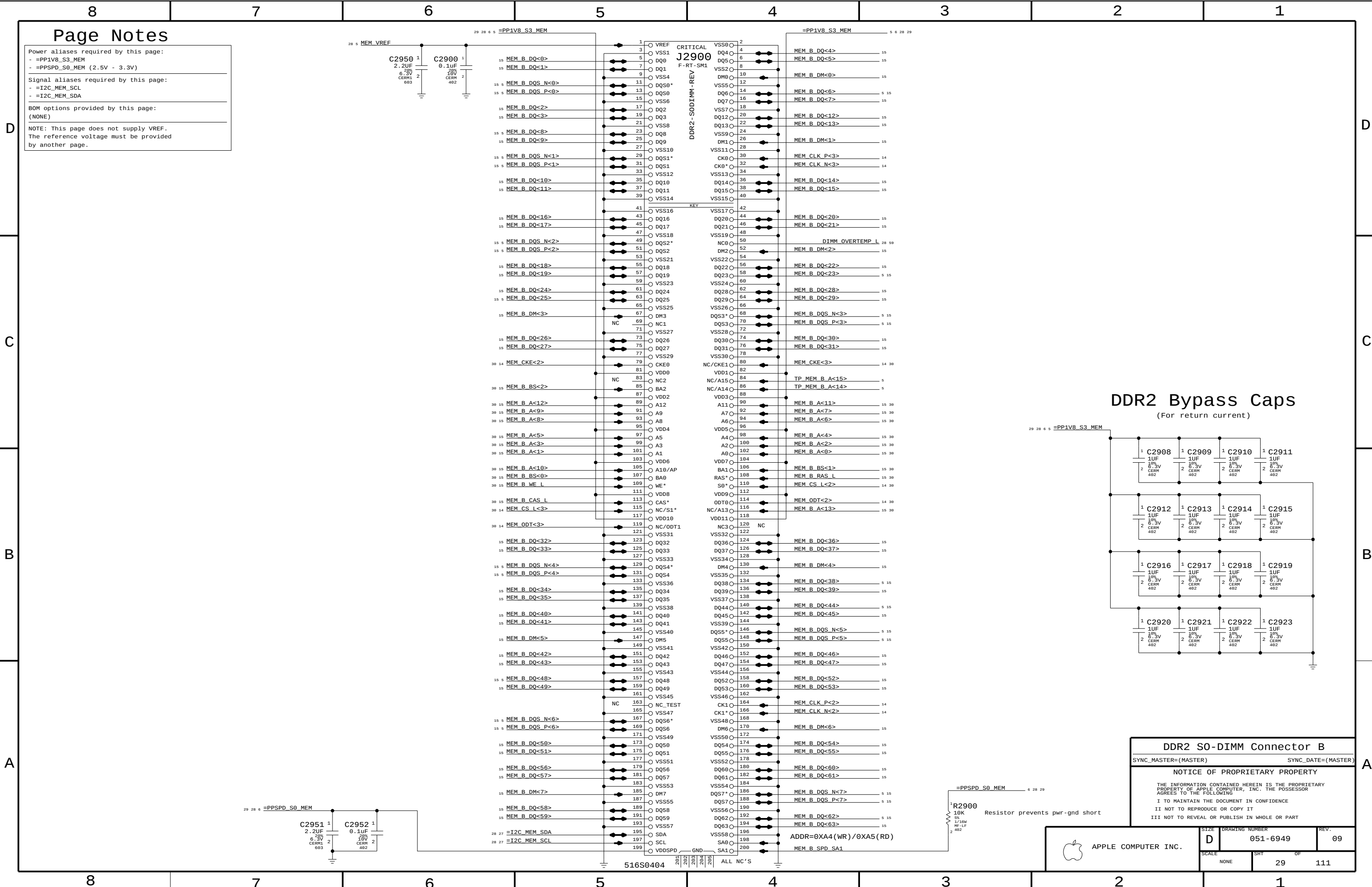
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SCALE	SHT
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NONE	28
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[illegible]

1



Page Notes

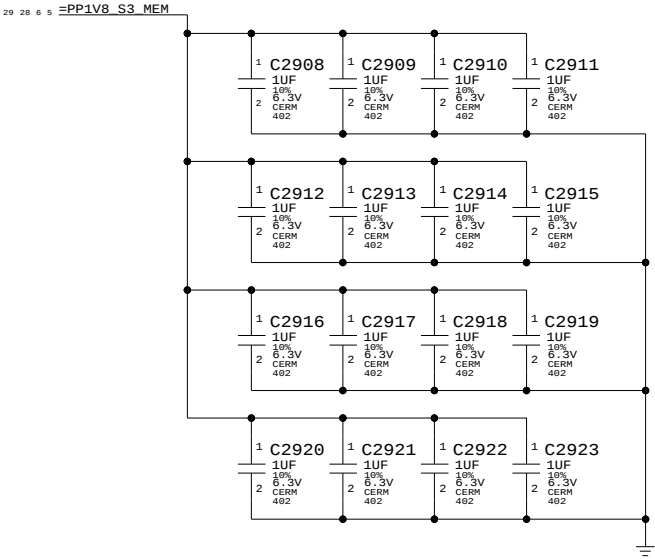
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- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
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- =I2C_MEM_SDA

BOM options provided by this page:
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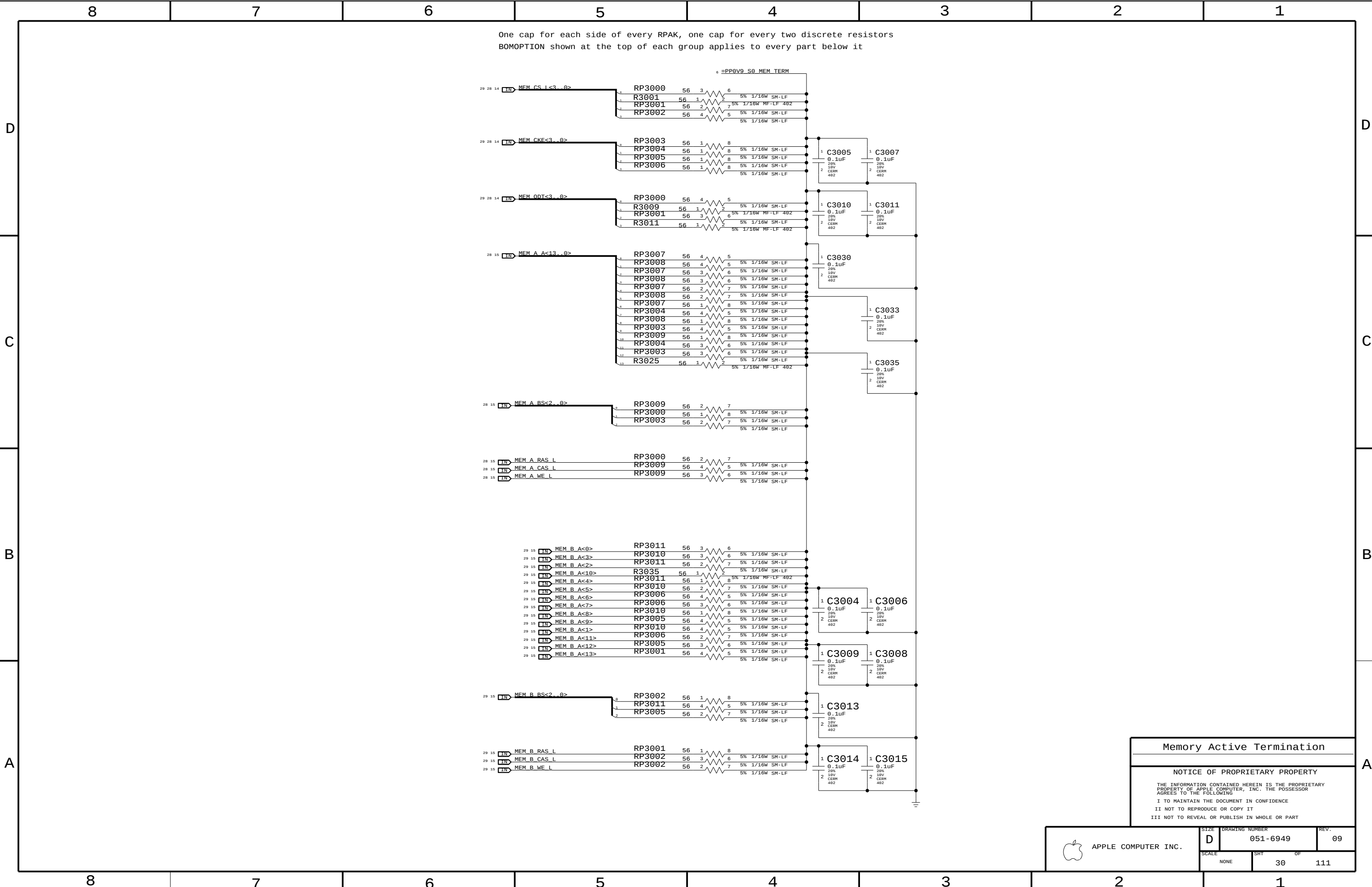
NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

DDR2 Bypass Caps (For return current)



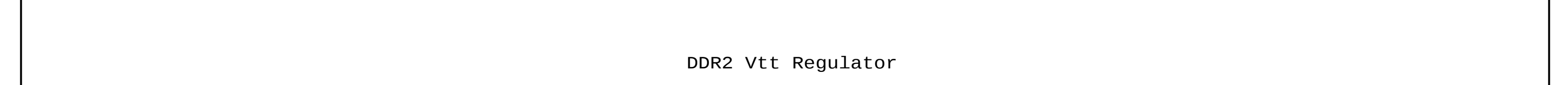
DDR2 S0-DIMM Connector B		
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APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	051-6949	09
SHT		29	111



8	7	6	5	4	3	2	1
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D		D
---	--	---



Timing diagram showing the relationship between MEMVTT_EN_PU and C3100. The signal MEMVTT_EN_PU transitions from low to high at approximately 1.5 ns, labeled as PP5V_S0_MEMVTT. The signal C3100 is shown as a constant high level.

The diagram illustrates the experimental setup. A participant is seated at a table, looking at a screen. The screen displays two stimuli, 'VDO' and 'VFC', arranged in a 2x2 grid. The participant is labeled 'Participant' and the screen is labeled 'Screen'.

[illegible]

7 VTT_IN VREF⁴ MEMVTT_VREF

[illegible]

Disable MERV11 in sleep.
Can SV be \$0 if 1V8 is S3?

==PP0V9_S0_MEMVTT_LDO



	POLY SNC - LF
--	------------------

B		B
---	--	---

[illegible]

	Memory	Vtt	Supply
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[illegible]

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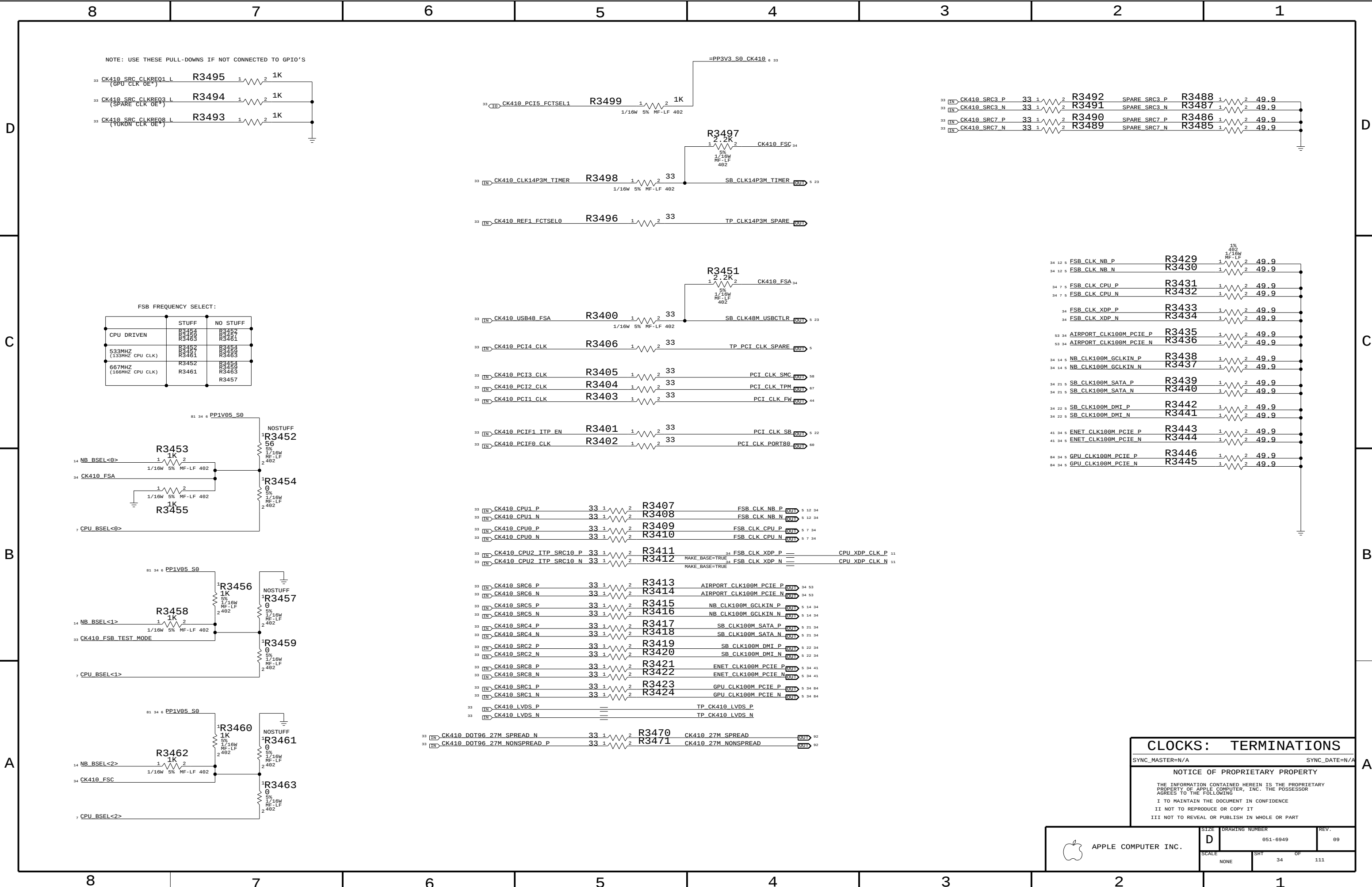
	III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
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 APPLE COMPUTER, INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
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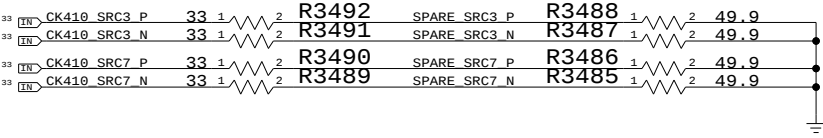
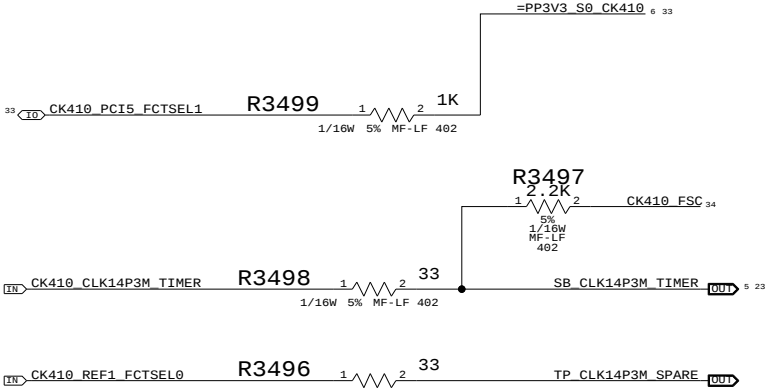
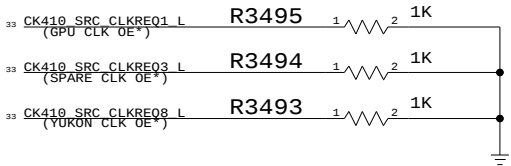
SCALE	STR	OF
NONE	31	111

8	7	6	5	4	3	2	1
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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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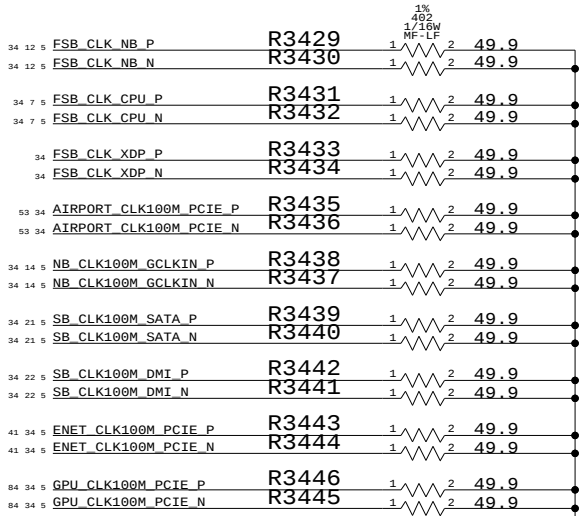
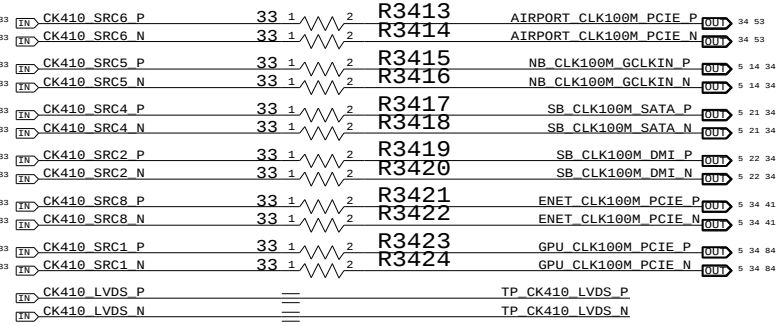
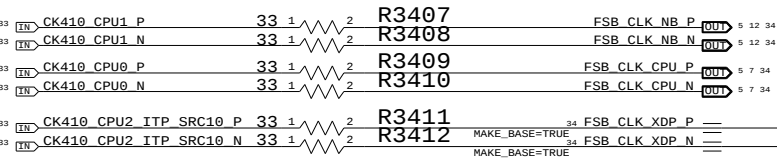
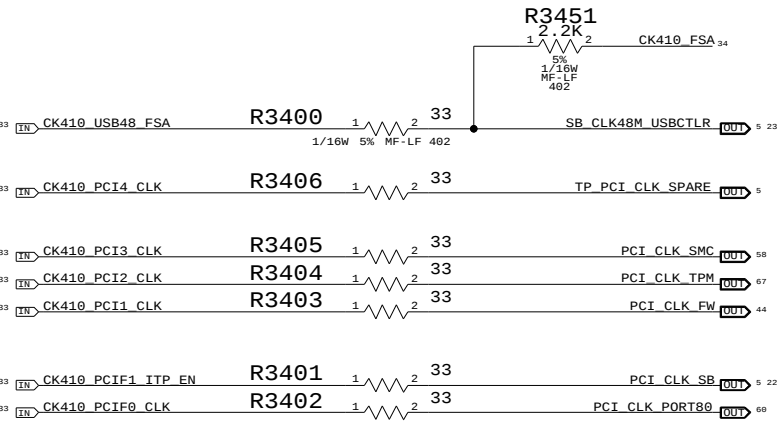
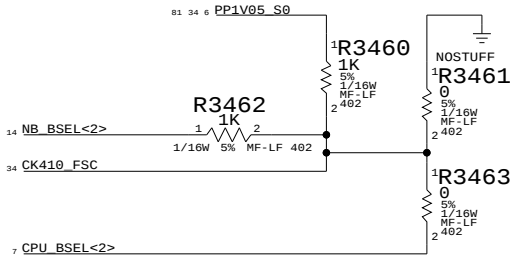
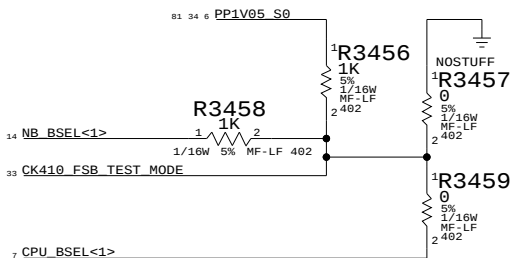
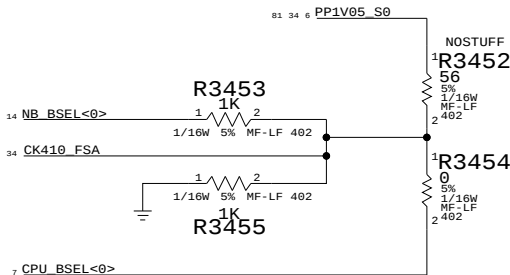


NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3455 R3456	R3452 R3453 R3457
533MHZ (133MHZ CPU CLK)	R3452 R3453 R3457	R3454 R3455 R3456
667MHZ (166MHZ CPU CLK)	R3452 R3453 R3457	R3454 R3455 R3456



CLOCKS: TERMINATIONS

SYNC_MASTER=N/A SYNC_DATE=N/A

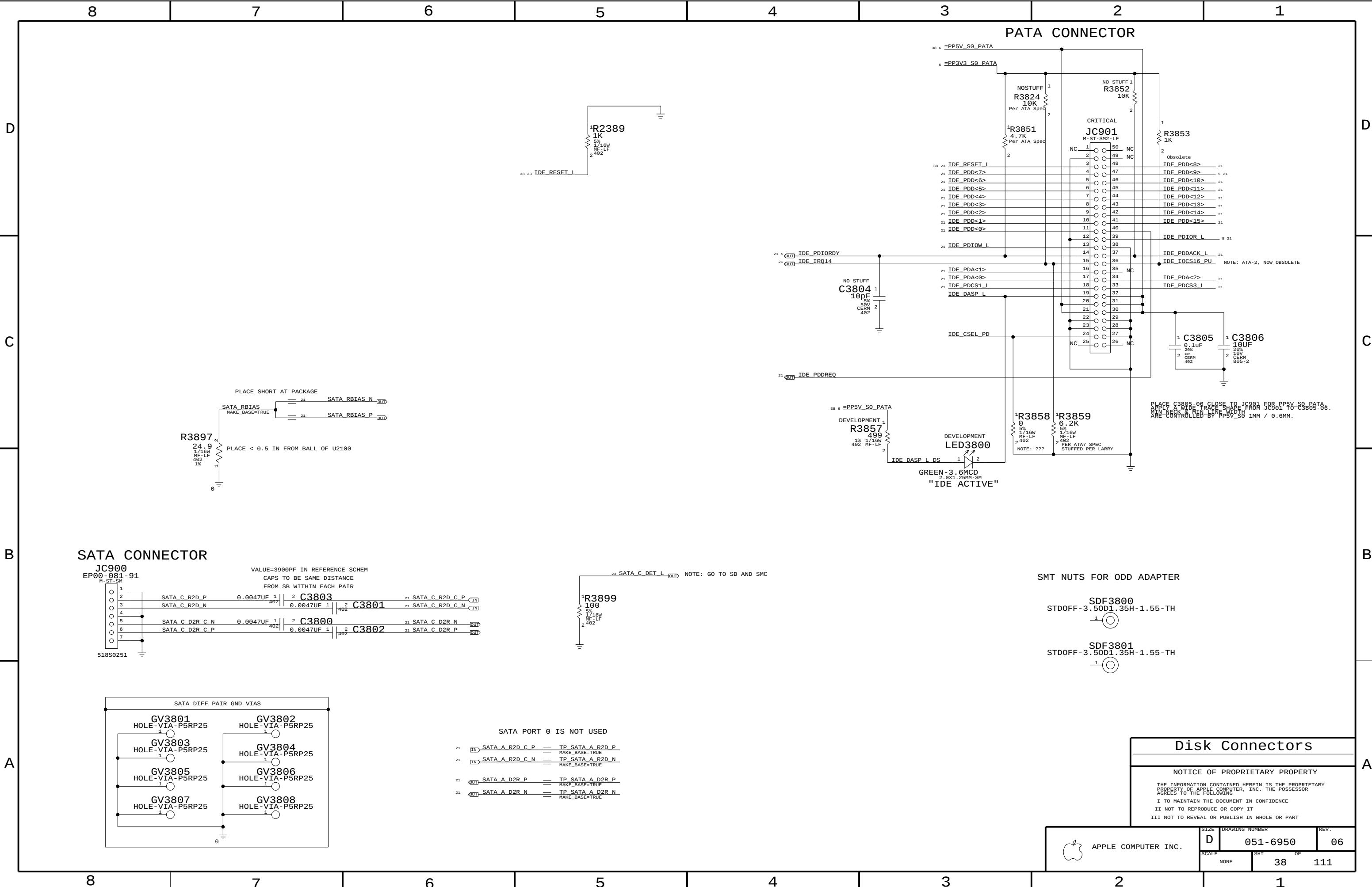
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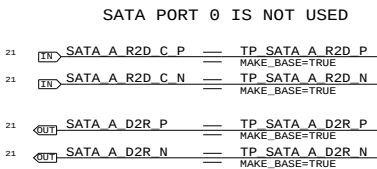
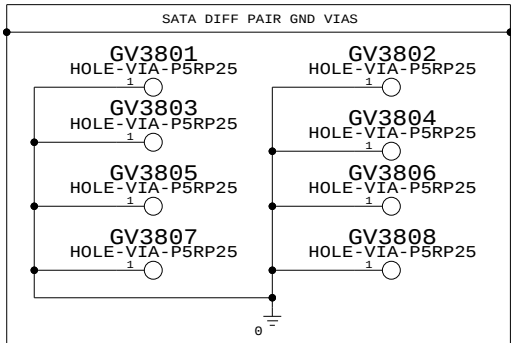
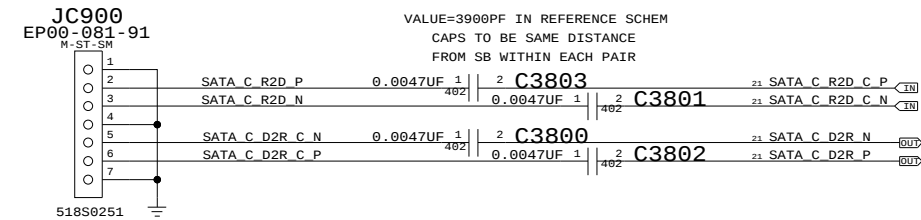


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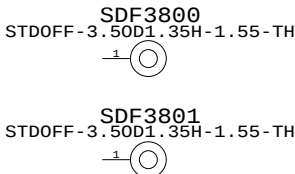
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT	OF
NONE	34	111



SATA CONNECTOR



SMT NUTS FOR ODD ADAPTER

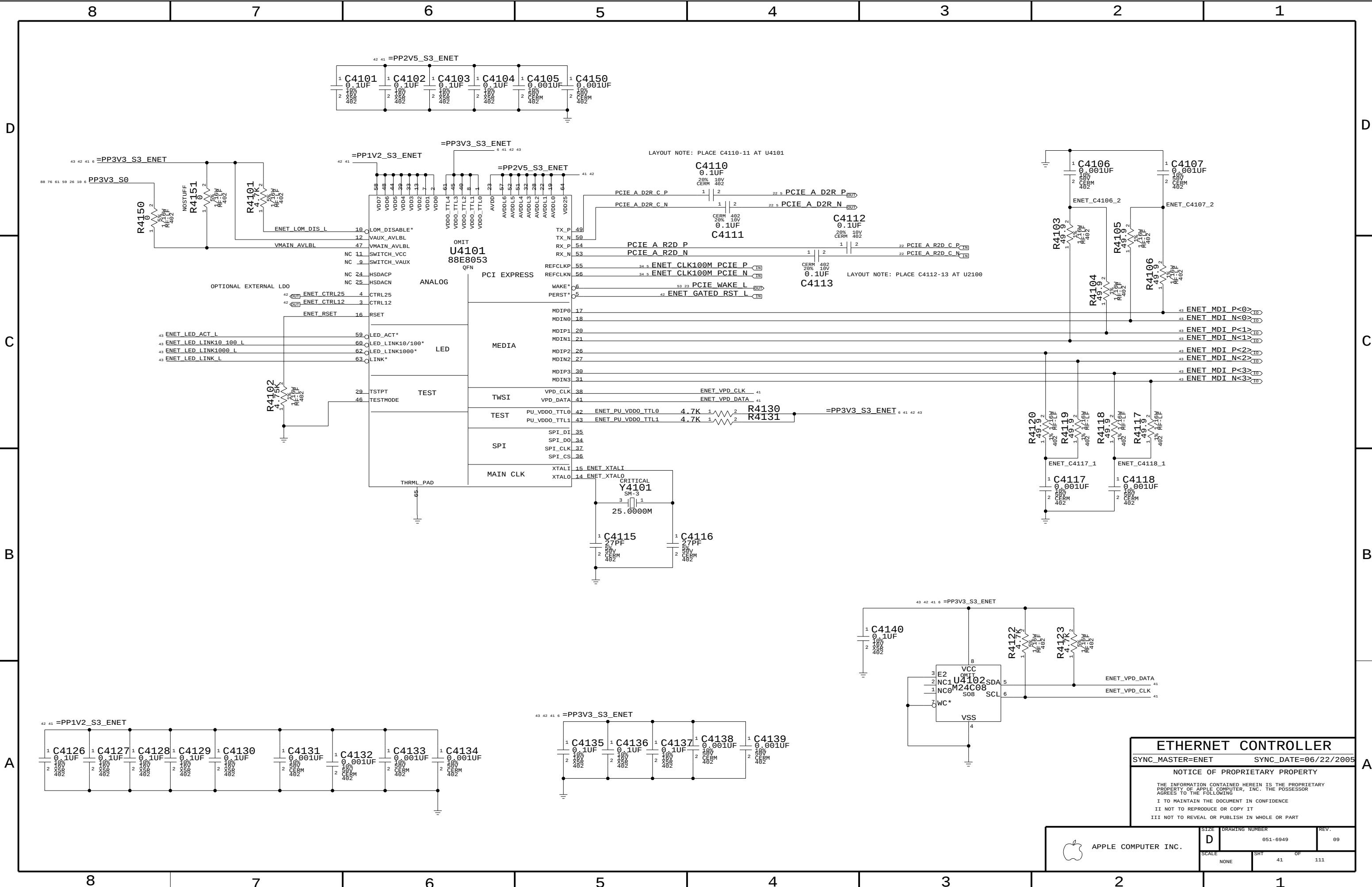


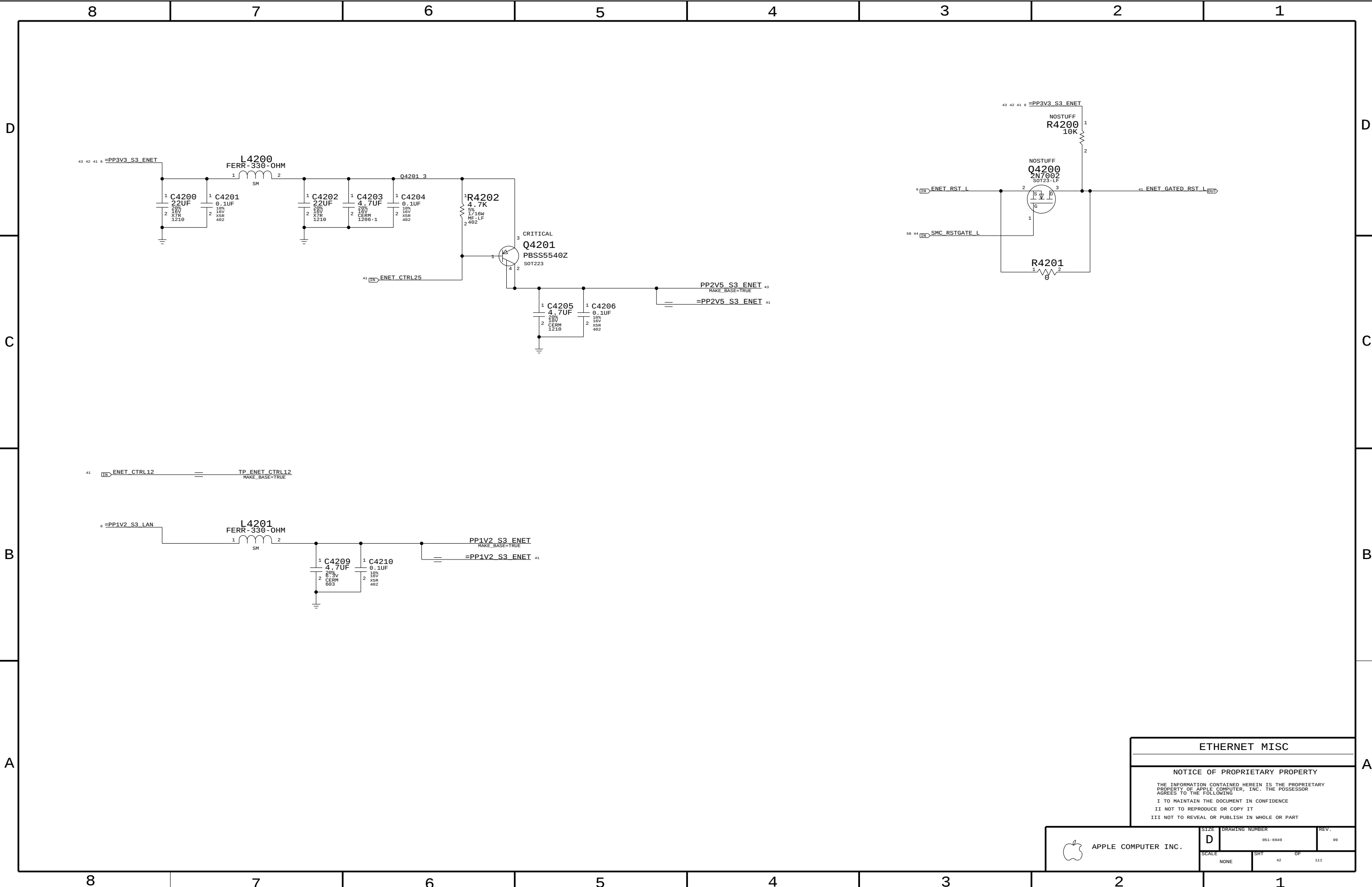
Disk Connectors

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	D	051-6950	06
SCALE	NONE	SHT	OF
		38	111





ETHERNET MISC

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SIZE

D

DRAWING NUMBER

001-0949

REV.

09

SCALE

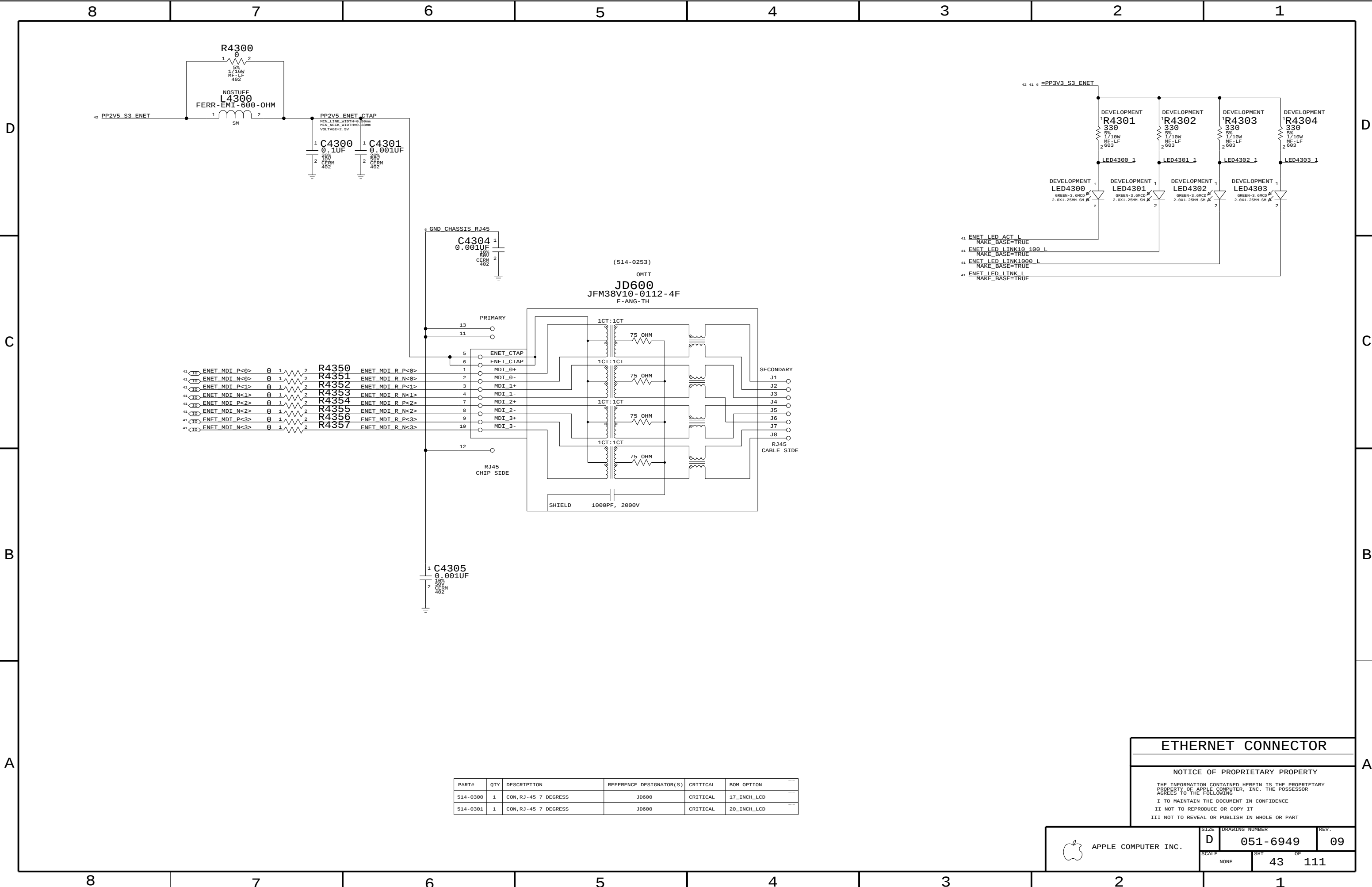
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SHT

42

OF

111



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0300	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0301	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

ETHERNET CONNECTOR

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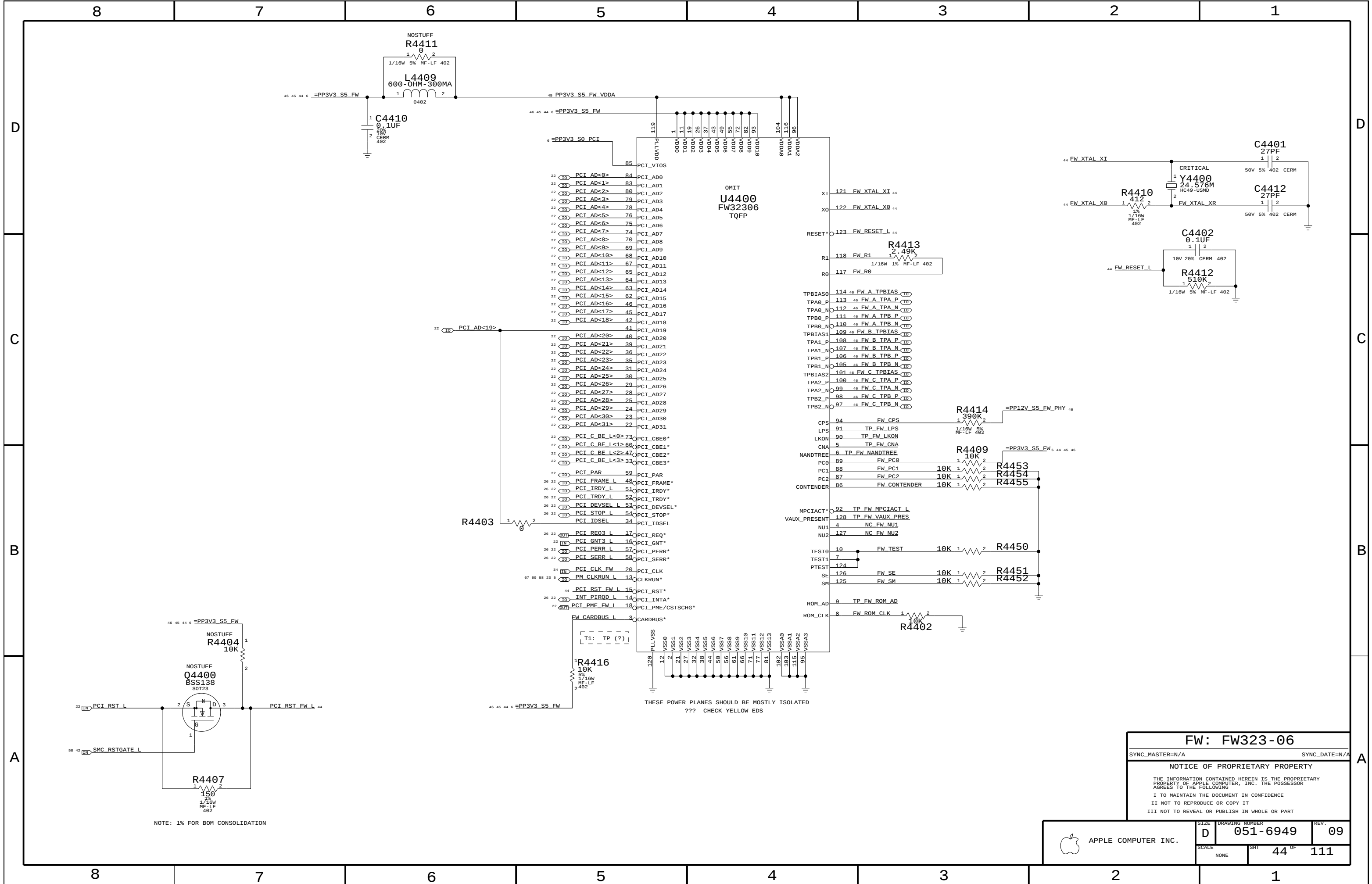
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43

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FW: FW323-06

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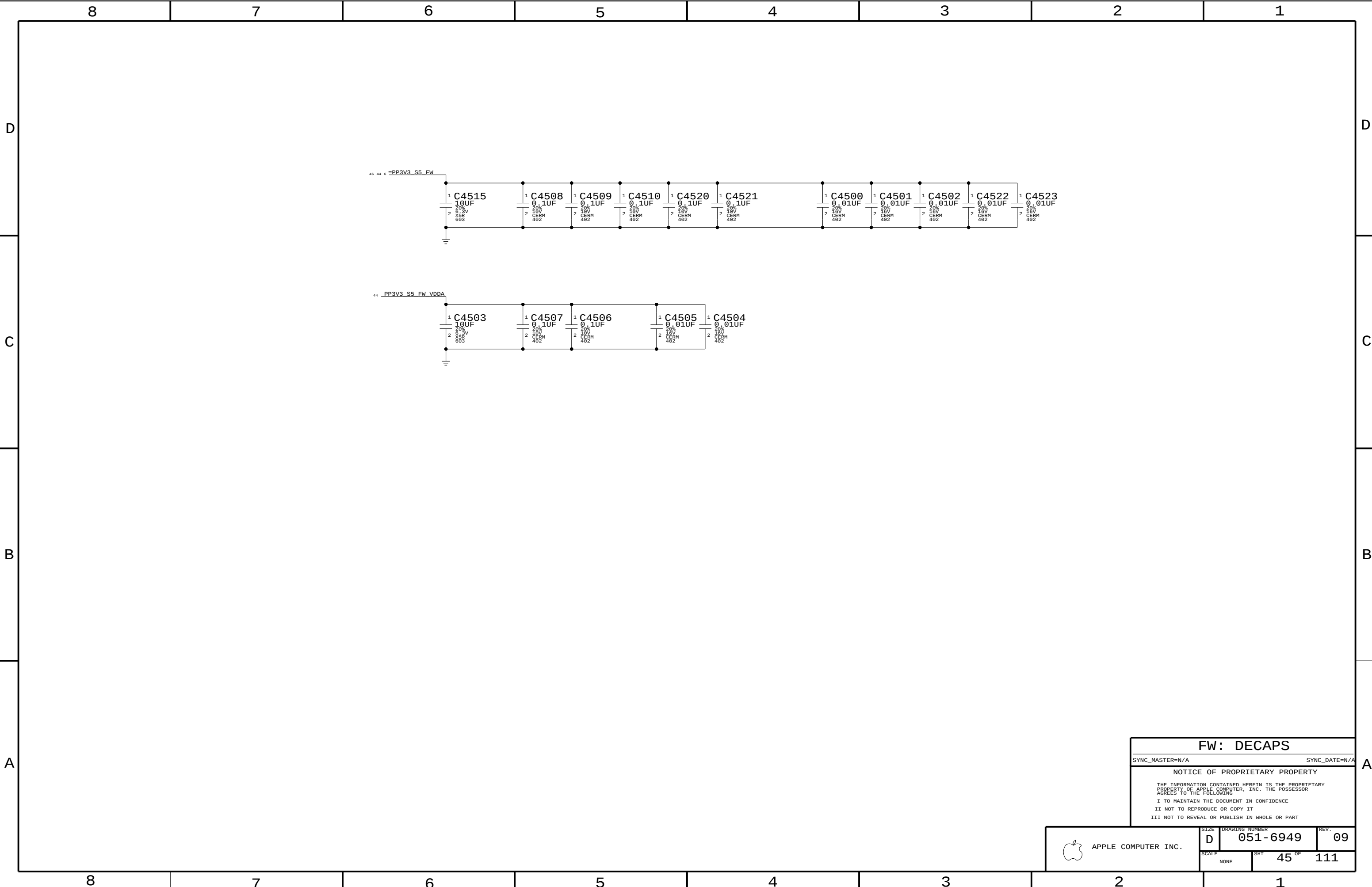
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	D	051-6949	09
SCALE	SHT		44 OF 111
	NONE		



FW: DECAPS

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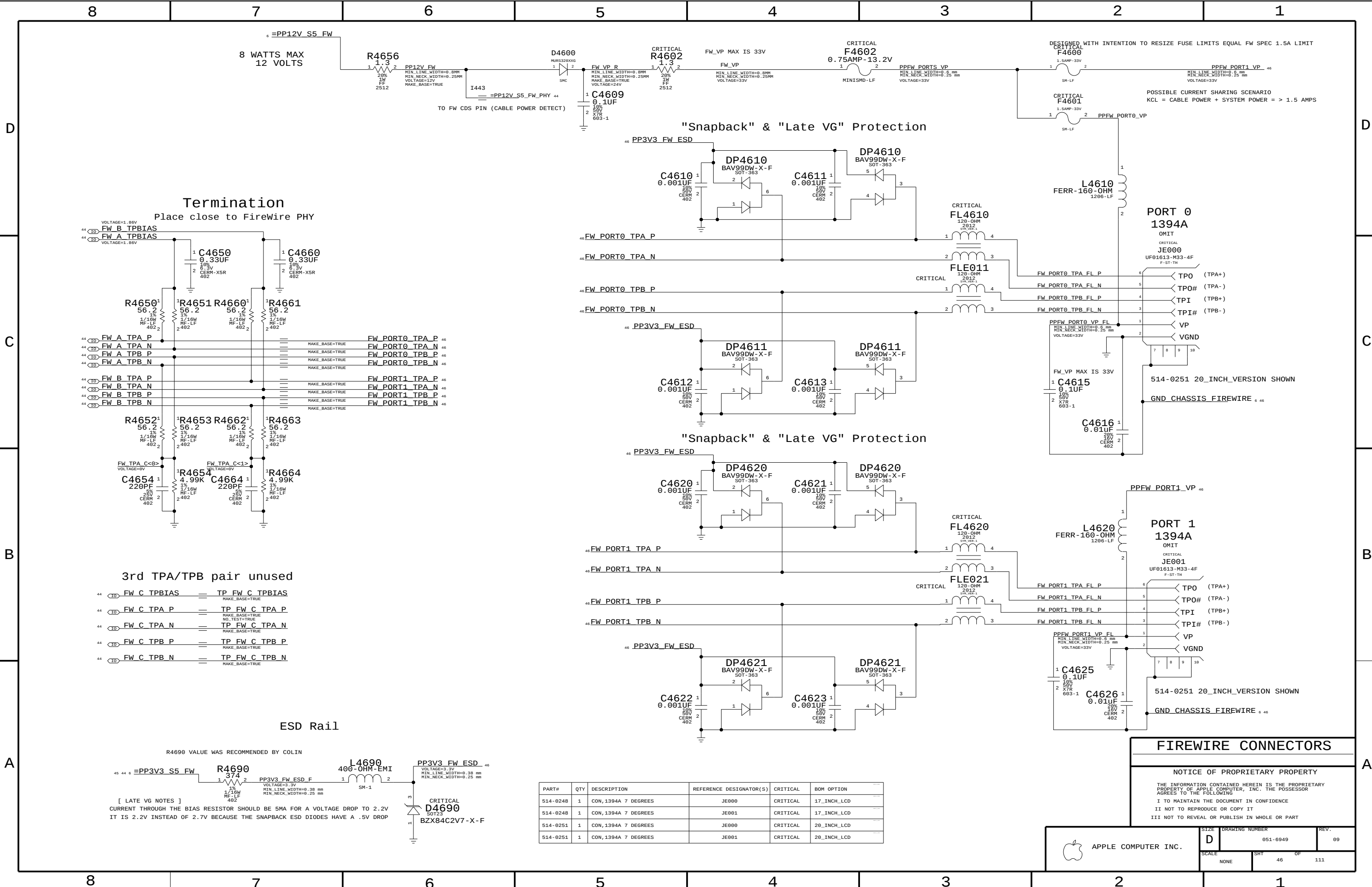
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT	45 OF 111
NONE		



Termination
Place close to FireWire PHY

"Snapback" & "Late VG" Protection

"Snapback" & "Late VG" Protection

3rd TPA/TPB pair unused

ESD Rail

FIREWIRE CONNECTORS

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON, 1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON, 1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON, 1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON, 1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

 APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-6949

REV.

09

SCALE

NONE

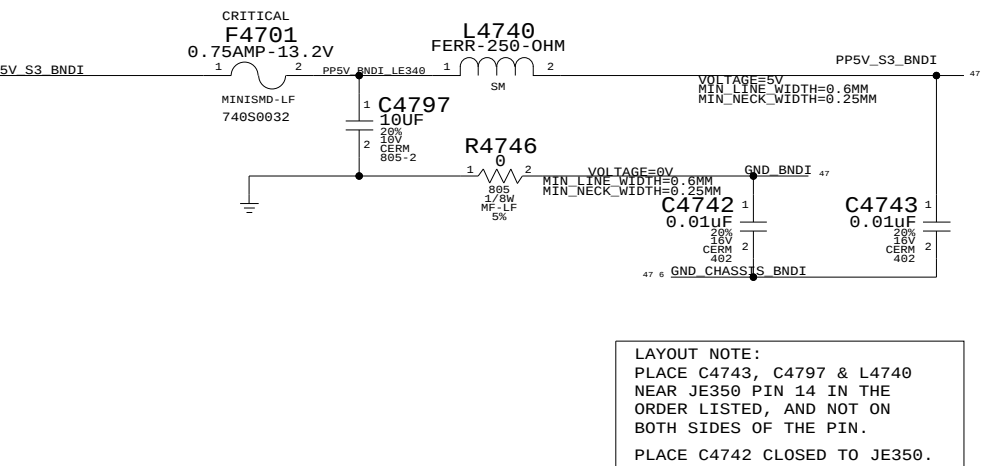
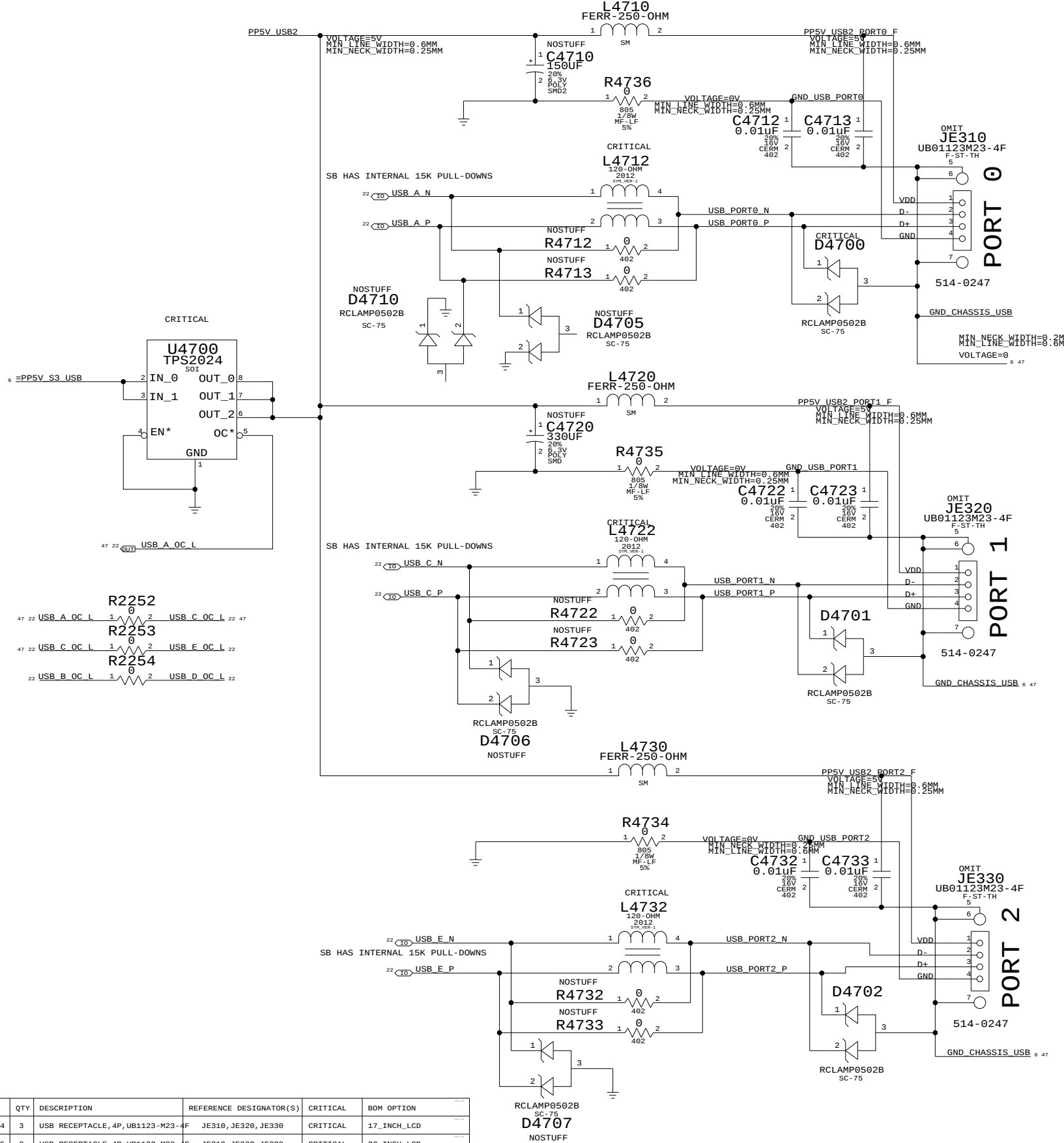
SHT

46

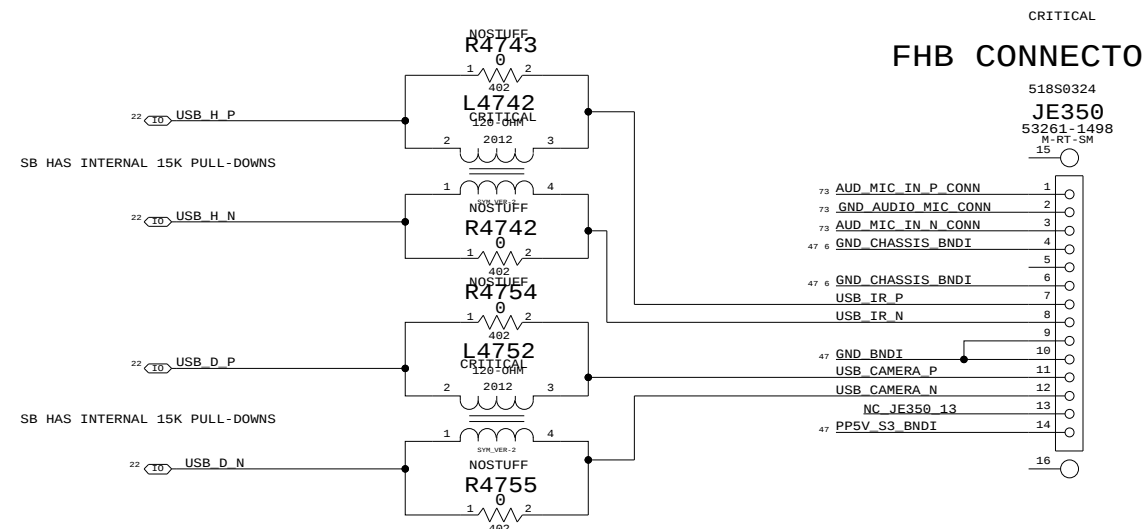
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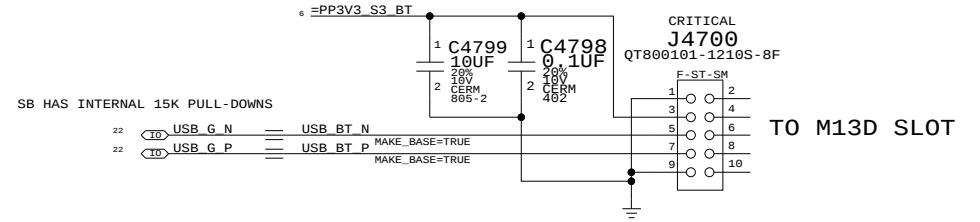
External USB Ports



LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR JE350 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.
PLACE C4742 CLOSED TO JE350.



BLUETOOTH



NOTE: STANDOFFS FOR J4700
SDF4700
STDOFF-40D4.5H-1.35-TH
SDF4701
STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0294	3	USB RECEPTACLE, 4P, UB1123-M23-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD
514-0295	3	USB RECEPTACLE, 4P, UB1123-M33-4F	JE310, JE320, JE330	CRITICAL	20_INCH_LCD

APPLE COMPUTER INC.

D

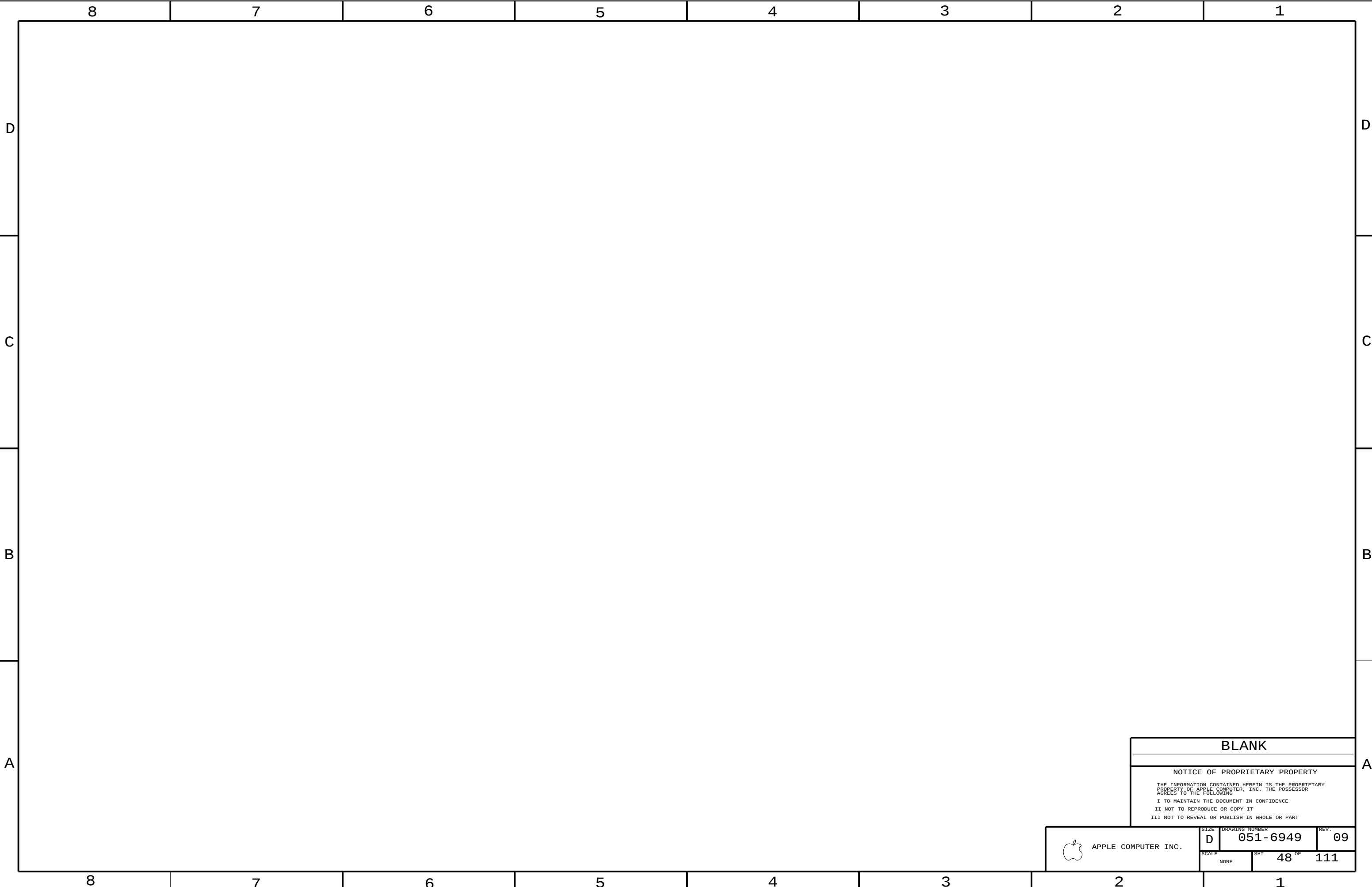
051-6950

06

NONE

47

111



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NOTICE OF PROPRIETARY PROPERTY

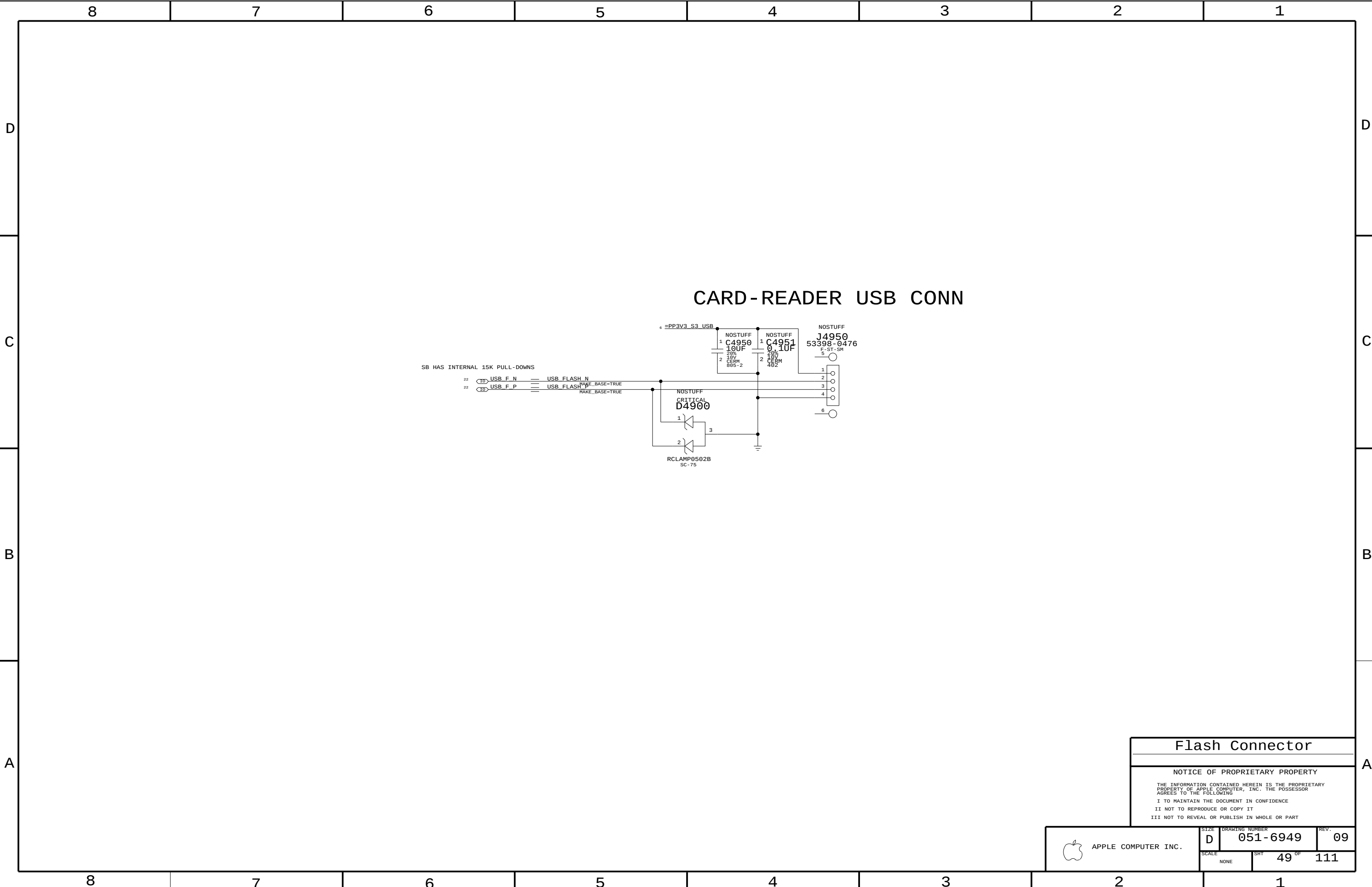
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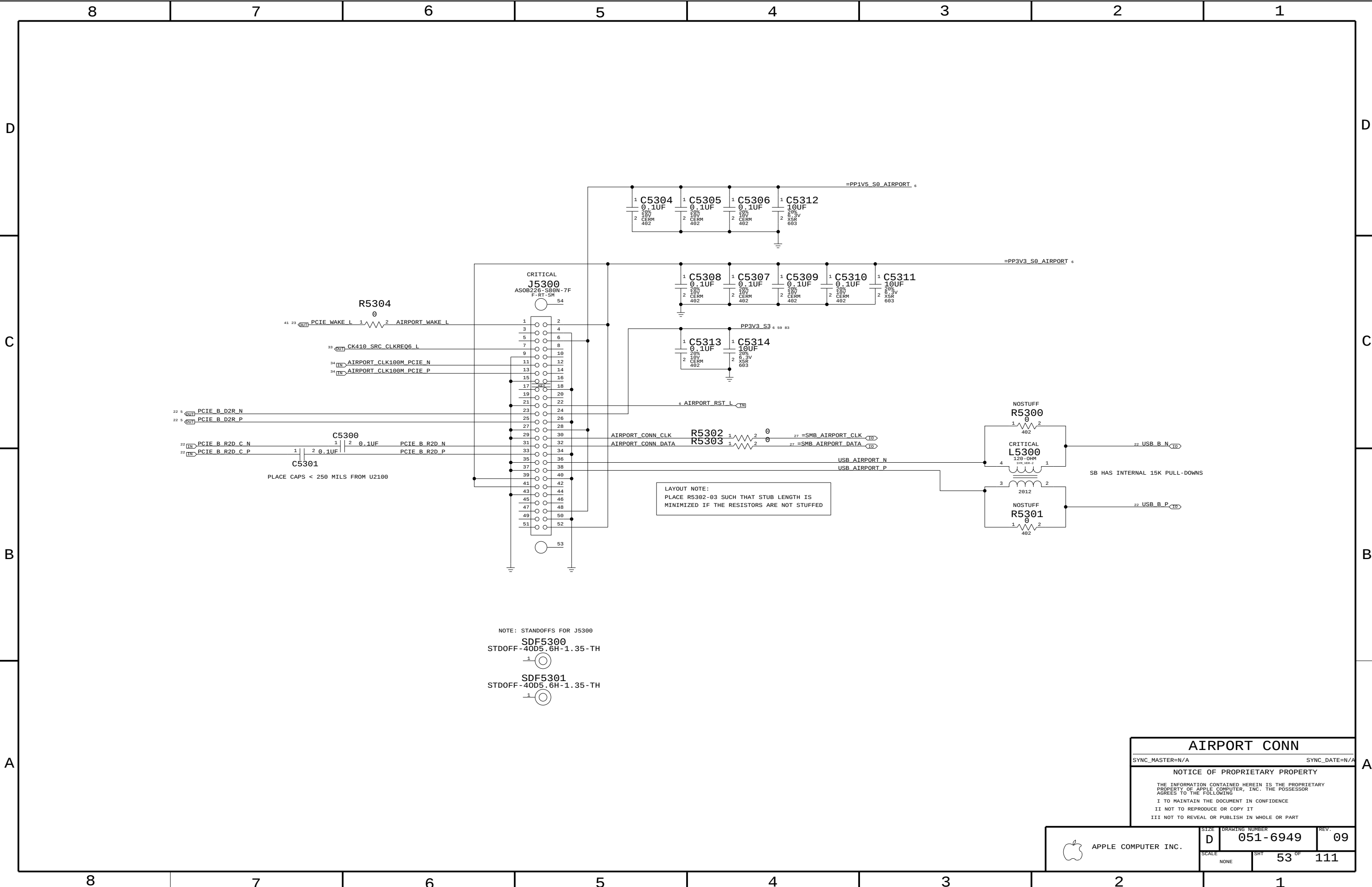
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
	SCALE NONE	SHT 48	OF 111





AIRPORT CONN

SYNC_MASTER=N/A

SYNC_DATE=N/A

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APPLE COMPUTER INC.

SCALE
NONE

D

SIZE

051-6949

DRAWING NUMBER

09

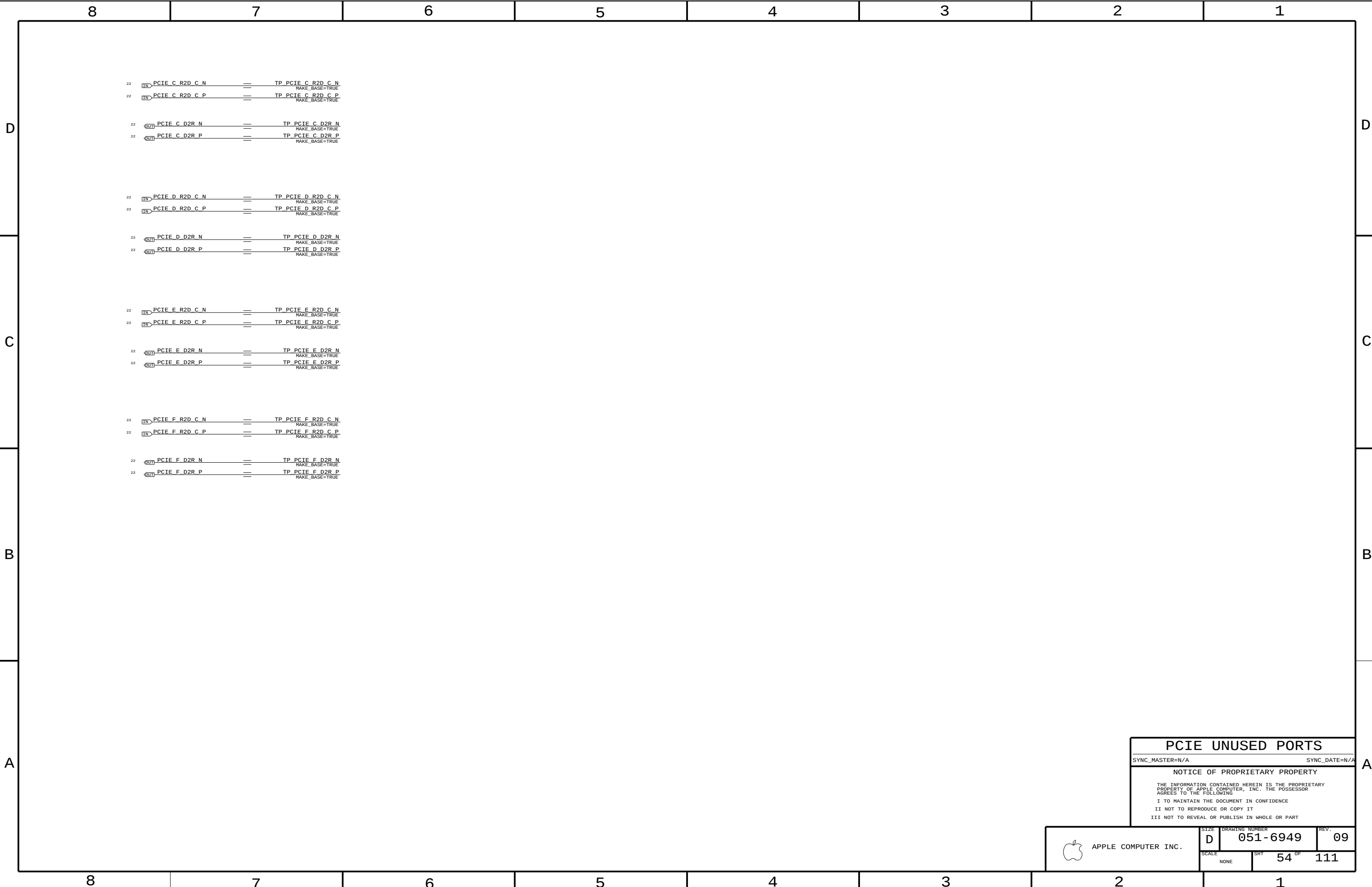
REV.

53

SHT

111

OF



PCIE UNUSED PORTS

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SYNC_DATE=N/A

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D

DRAWING NUMBER

051-6949

REV.

09

SCALE

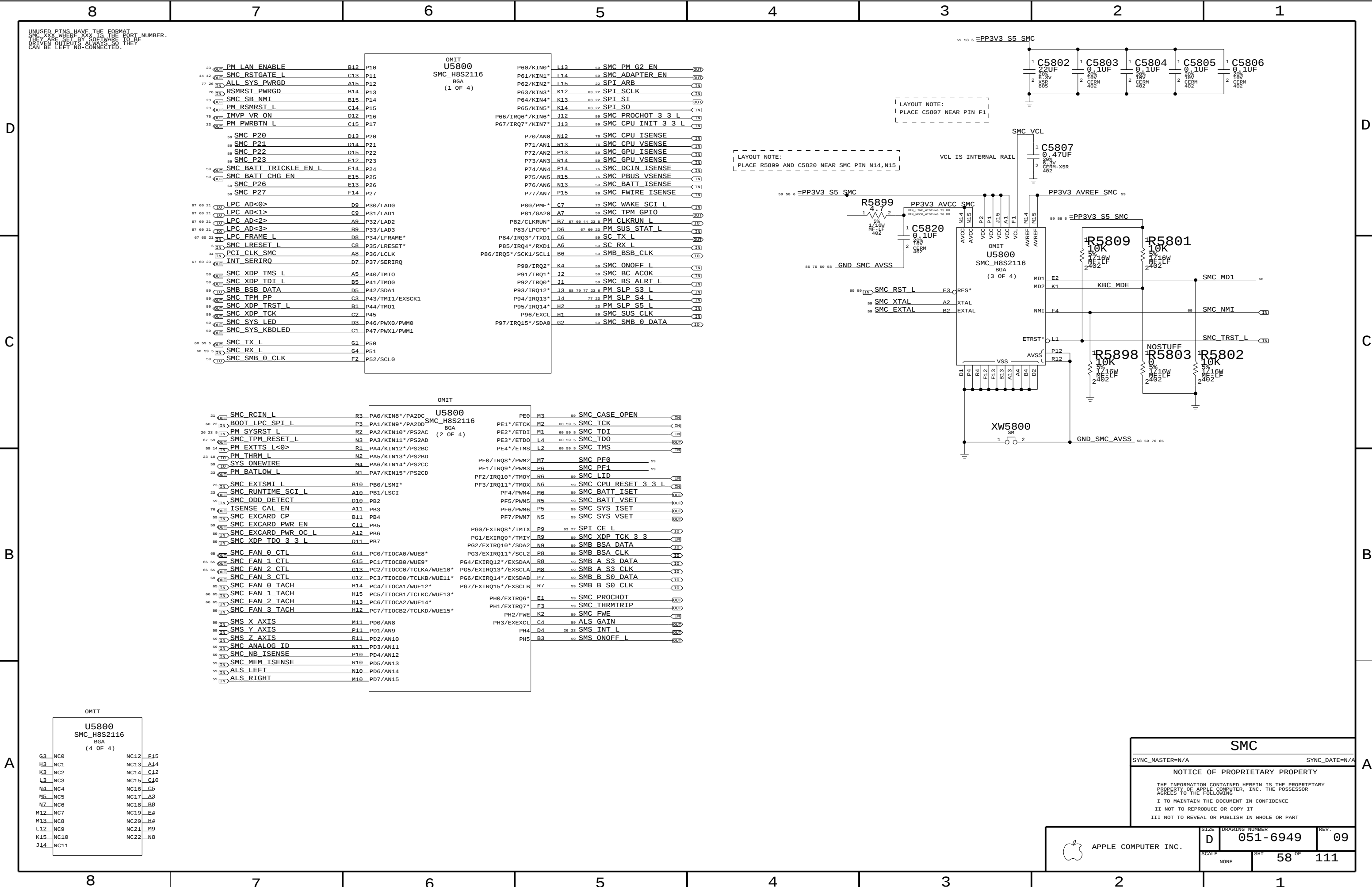
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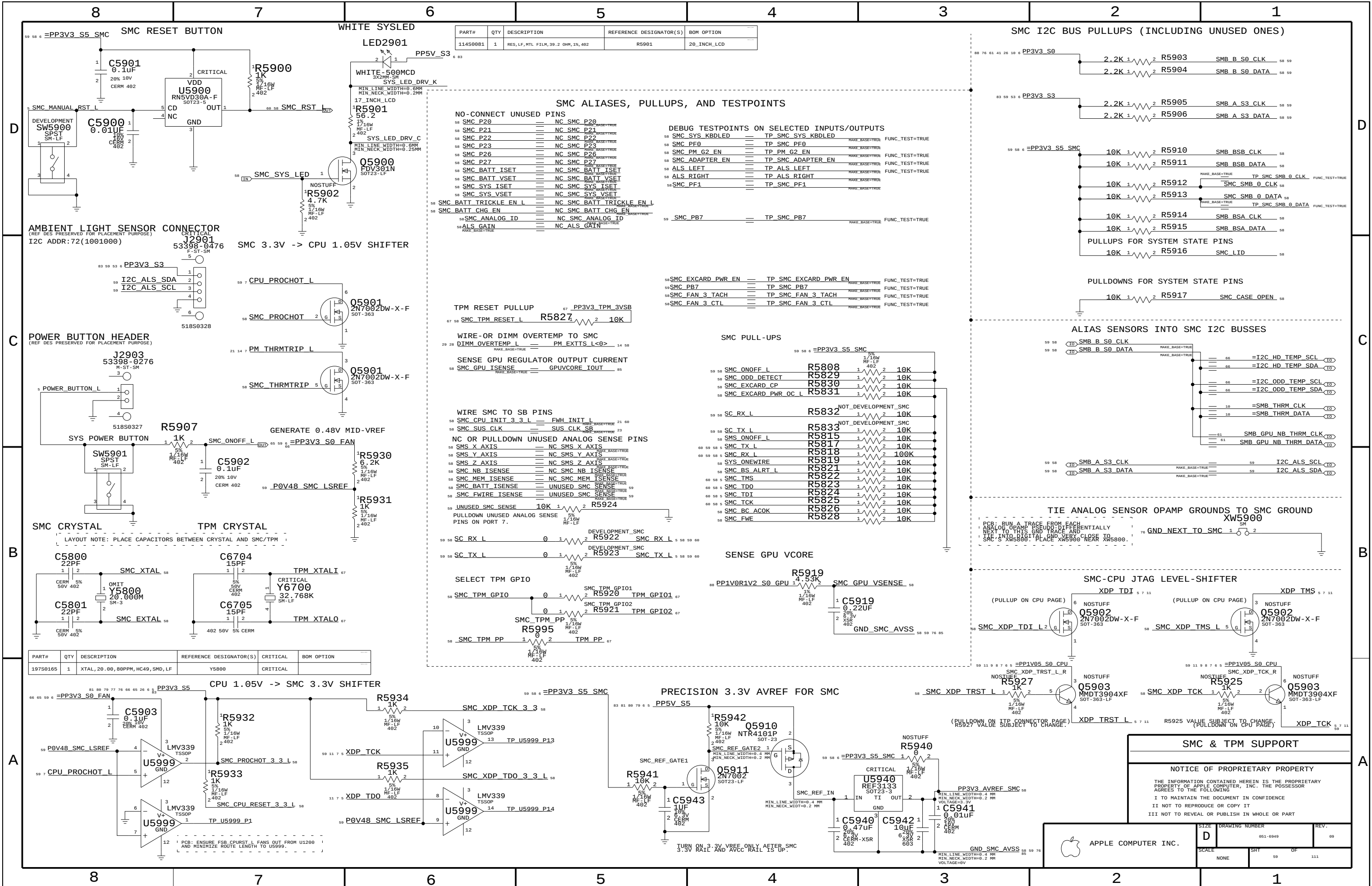
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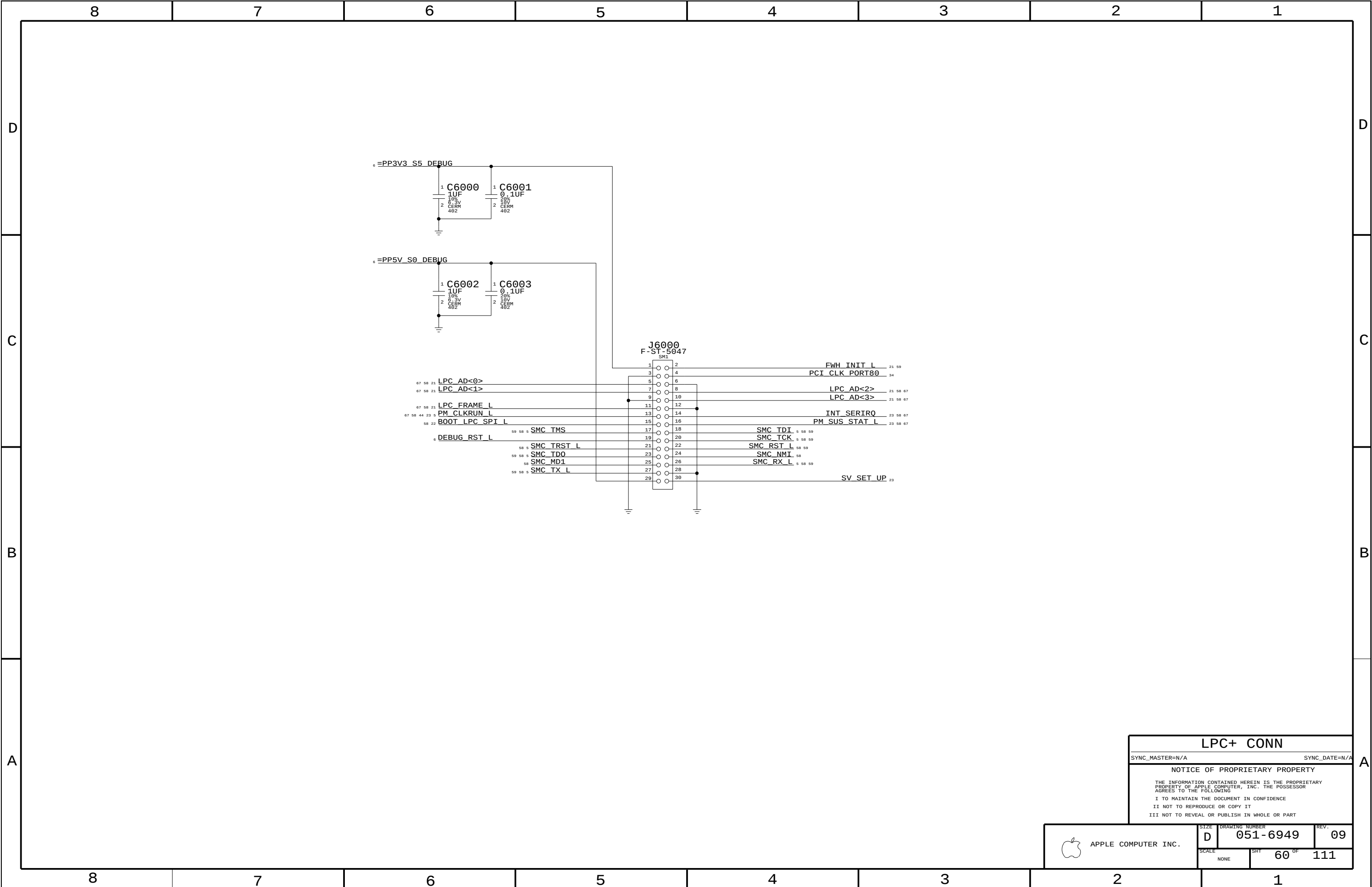
54

OF

111







LPC+ CONN

SYNC_MASTER=N/A

SYNC_DATE=N/A

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SIZE

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DRAWING NUMBER

051-6949

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09

SCALE

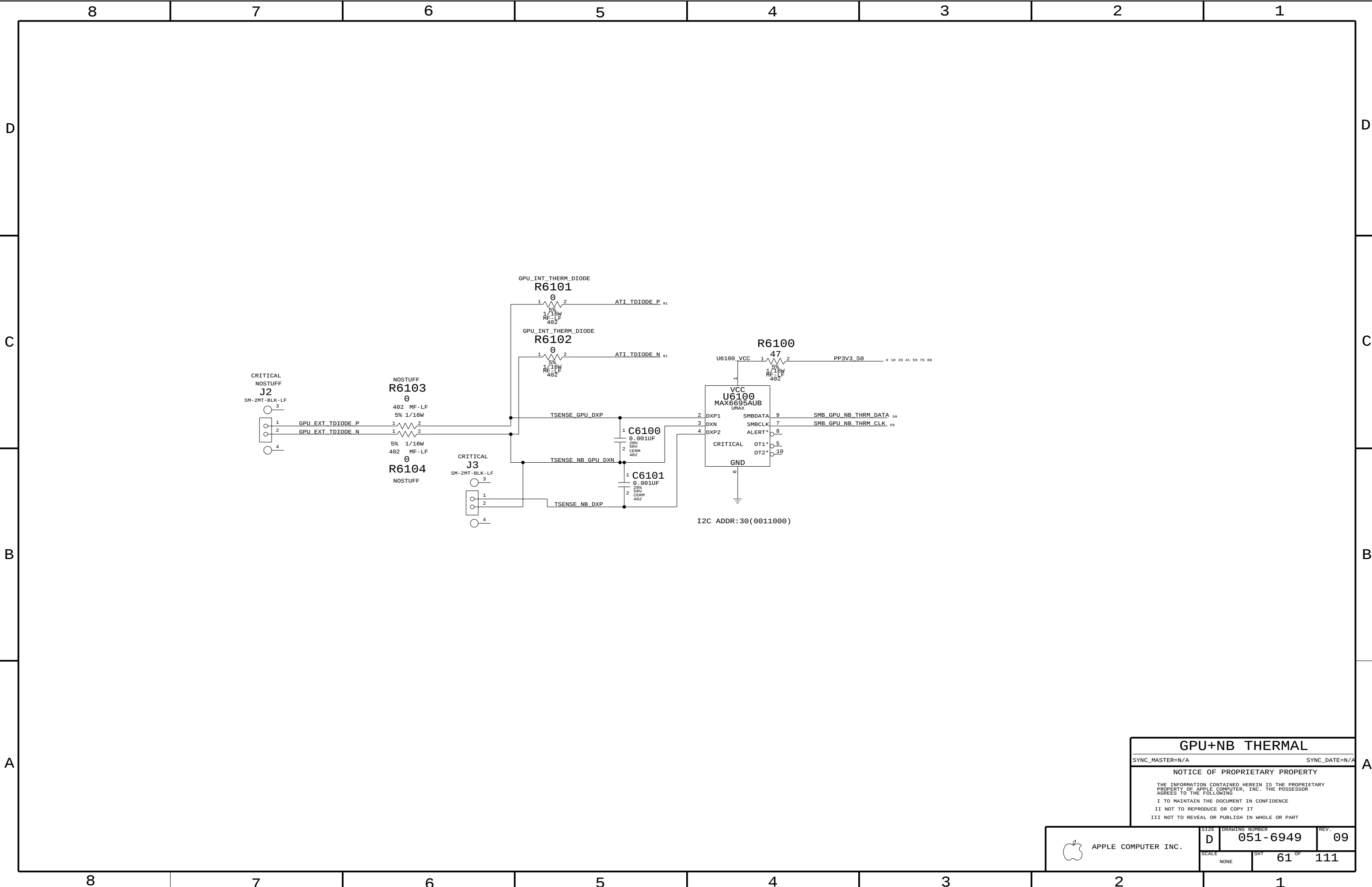
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SHT

60

OF

111



GPU+NB THERMAL

SYNC_MASTER=N/A

SYNC_DATE=N/A

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09

SCALE

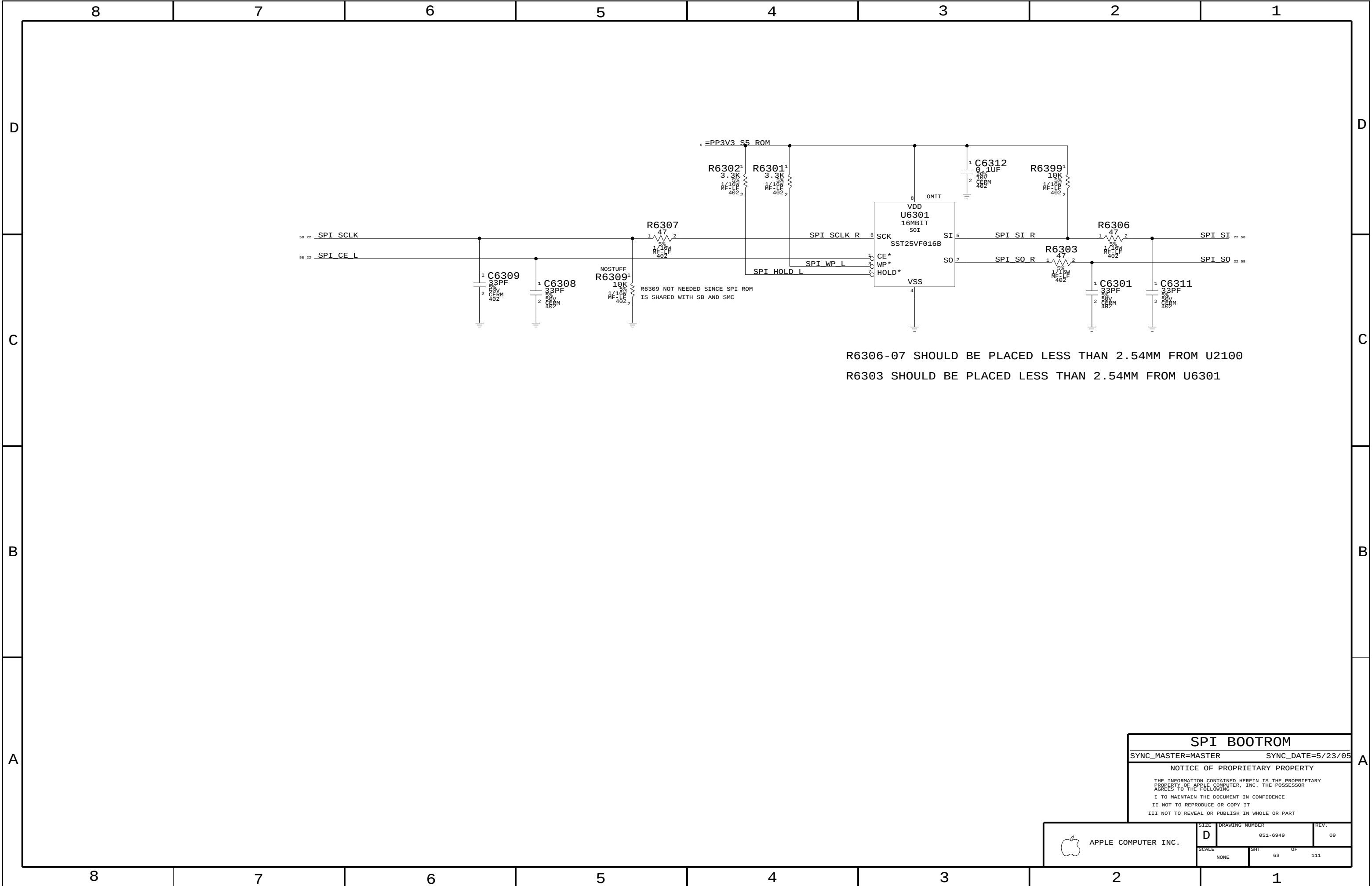
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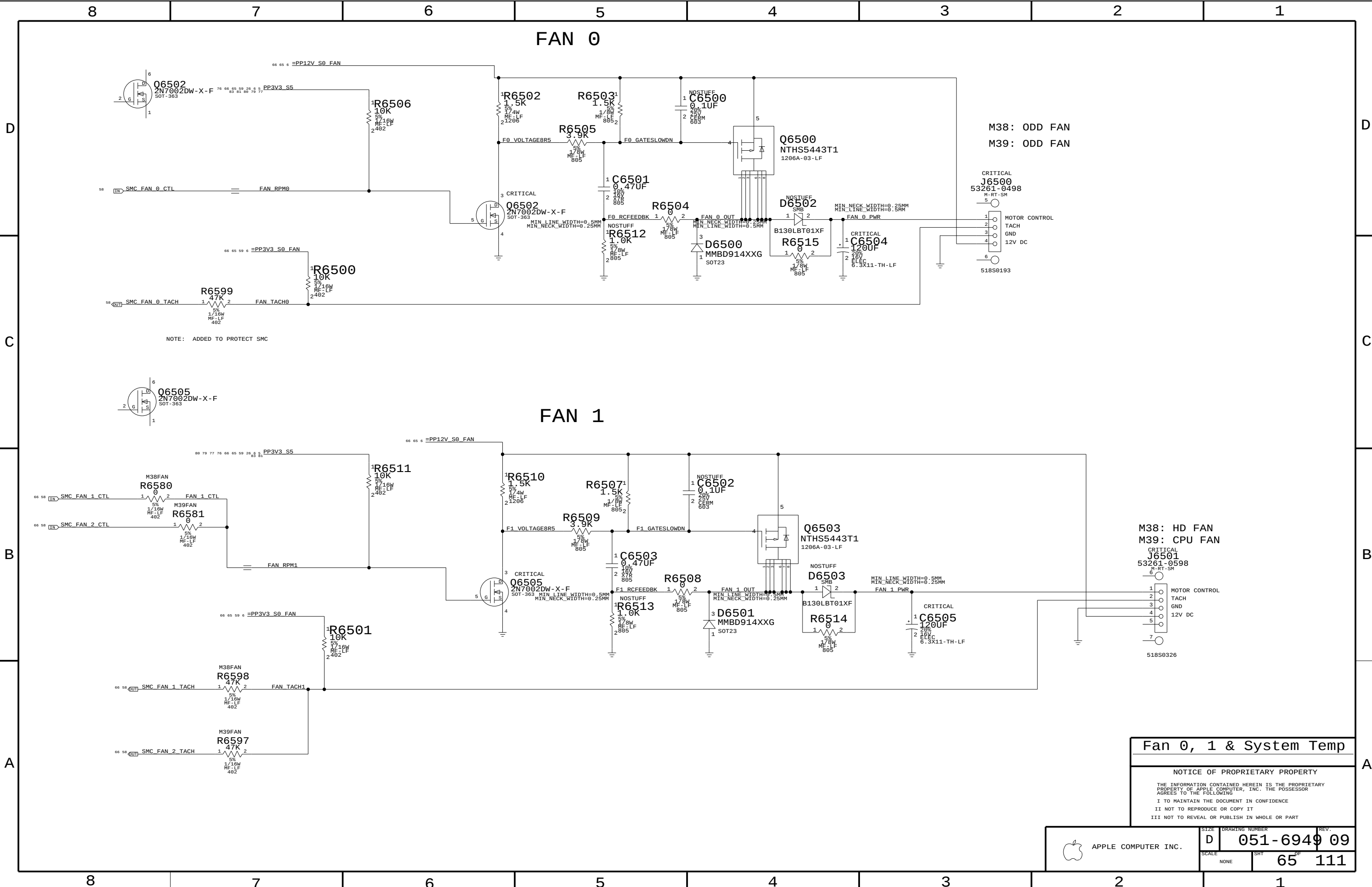
SHT

61

OF

111





Fan 0, 1 & System Temp

NOTICE OF PROPRIETARY PROPERTY

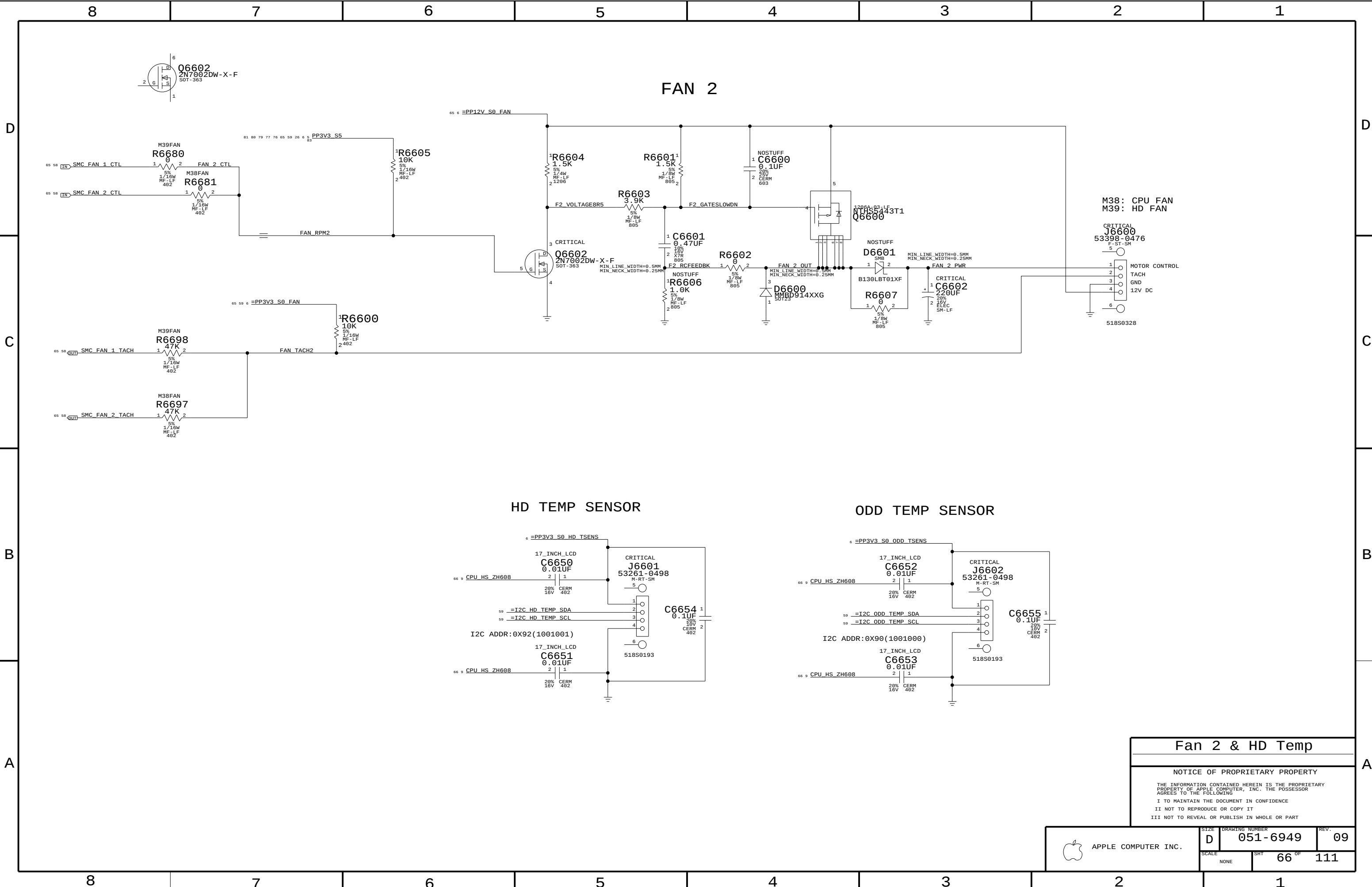
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	D	051-6949	09
SCALE	SHT		OF
	NONE		65 111



Fan 2 & HD Temp

NOTICE OF PROPRIETARY PROPERTY

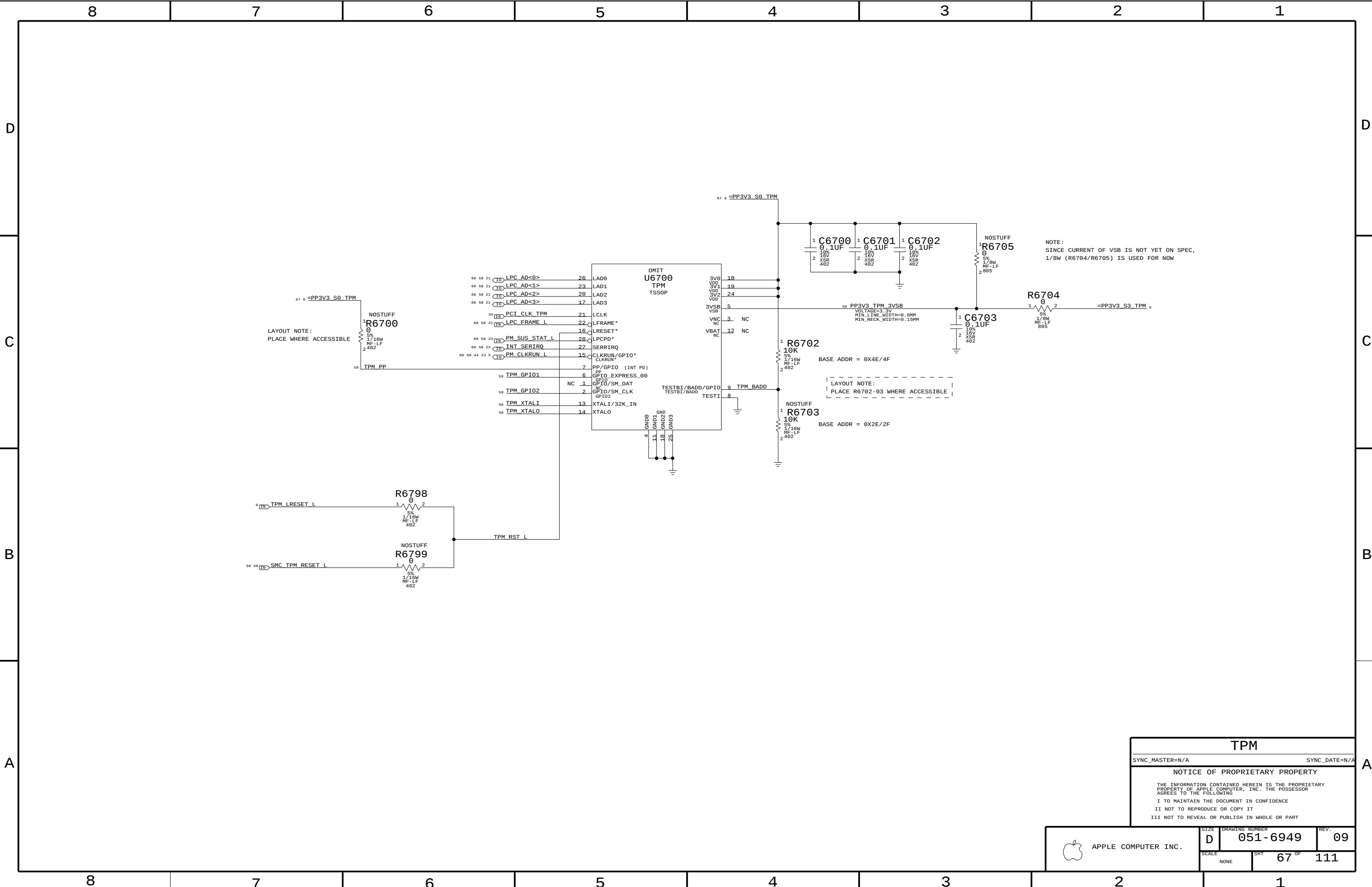
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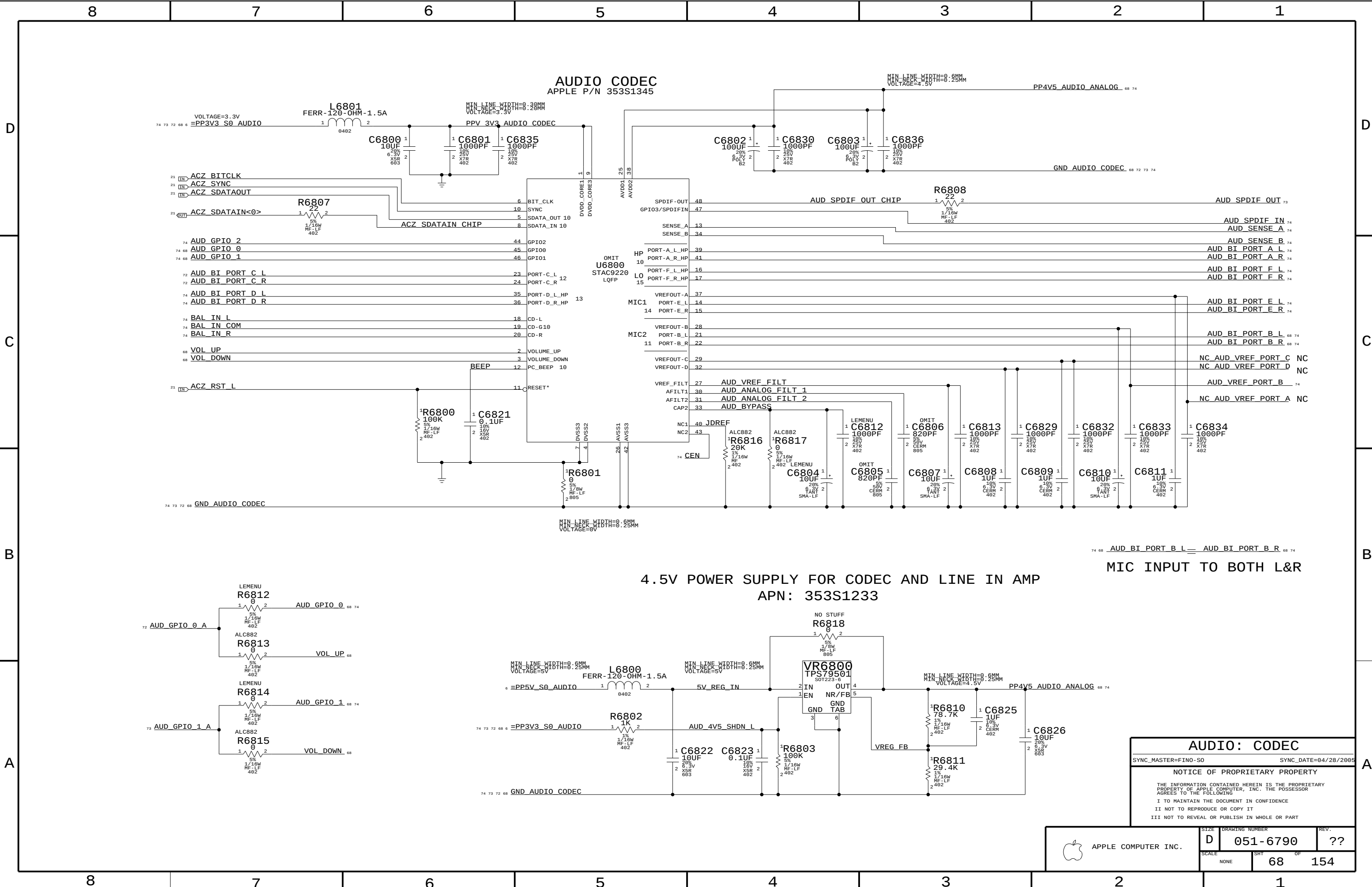
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE		SHT	66 OF 111
NONE			



TPM		
SYNC_MASTER=N/A		SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
SCALE		SHT	67 OF 111
NONE			



AUDIO CODEC
APPLE P/N 353S1345

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APN: 353S1233

AUDIO: CODEC

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

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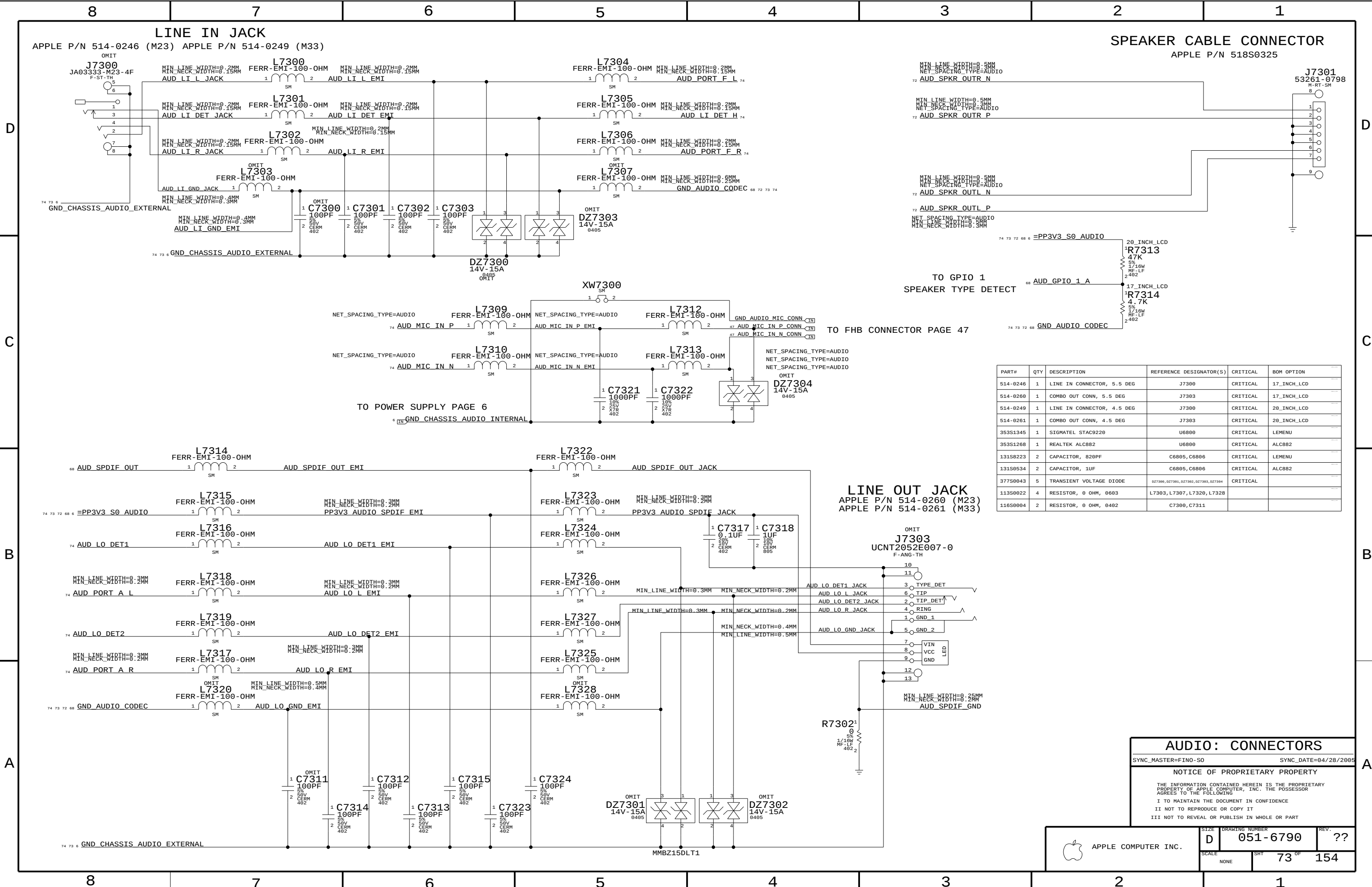


APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

D 051-6790 ??

SCALE NONE SHY OF 154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0246	1	LINE IN CONNECTOR, 5.5 DEG	J7300	CRITICAL	17_INCH_LCD
514-0260	1	COMBO OUT CONN, 5.5 DEG	J7303	CRITICAL	17_INCH_LCD
514-0249	1	LINE IN CONNECTOR, 4.5 DEG	J7300	CRITICAL	20_INCH_LCD
514-0261	1	COMBO OUT CONN, 4.5 DEG	J7303	CRITICAL	20_INCH_LCD
353S1345	1	SIGMATEL STAC9220	U6800	CRITICAL	LEMENU
353S1268	1	REALTEK ALC882	U6800	CRITICAL	ALC882
131S8223	2	CAPACITOR, 820PF	C6805,C6806	CRITICAL	LEMENU
131S0534	2	CAPACITOR, 1UF	C6805,C6806	CRITICAL	ALC882
377S0043	5	TRANSIENT VOLTAGE DIODE	DZ7300,DZ7301,DZ7302,DZ7303,DZ7304	CRITICAL	
113S0022	4	RESISTOR, 0 OHM, 0603	L7303,L7307,L7320,L7328		
116S0004	2	RESISTOR, 0 OHM, 0402	C7300,C7311		

AUDIO: CONNECTORS

SYNC_MASTER=F1N0-S0

SYNC_DATE=04/28/2005

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SCALE
NONE

D

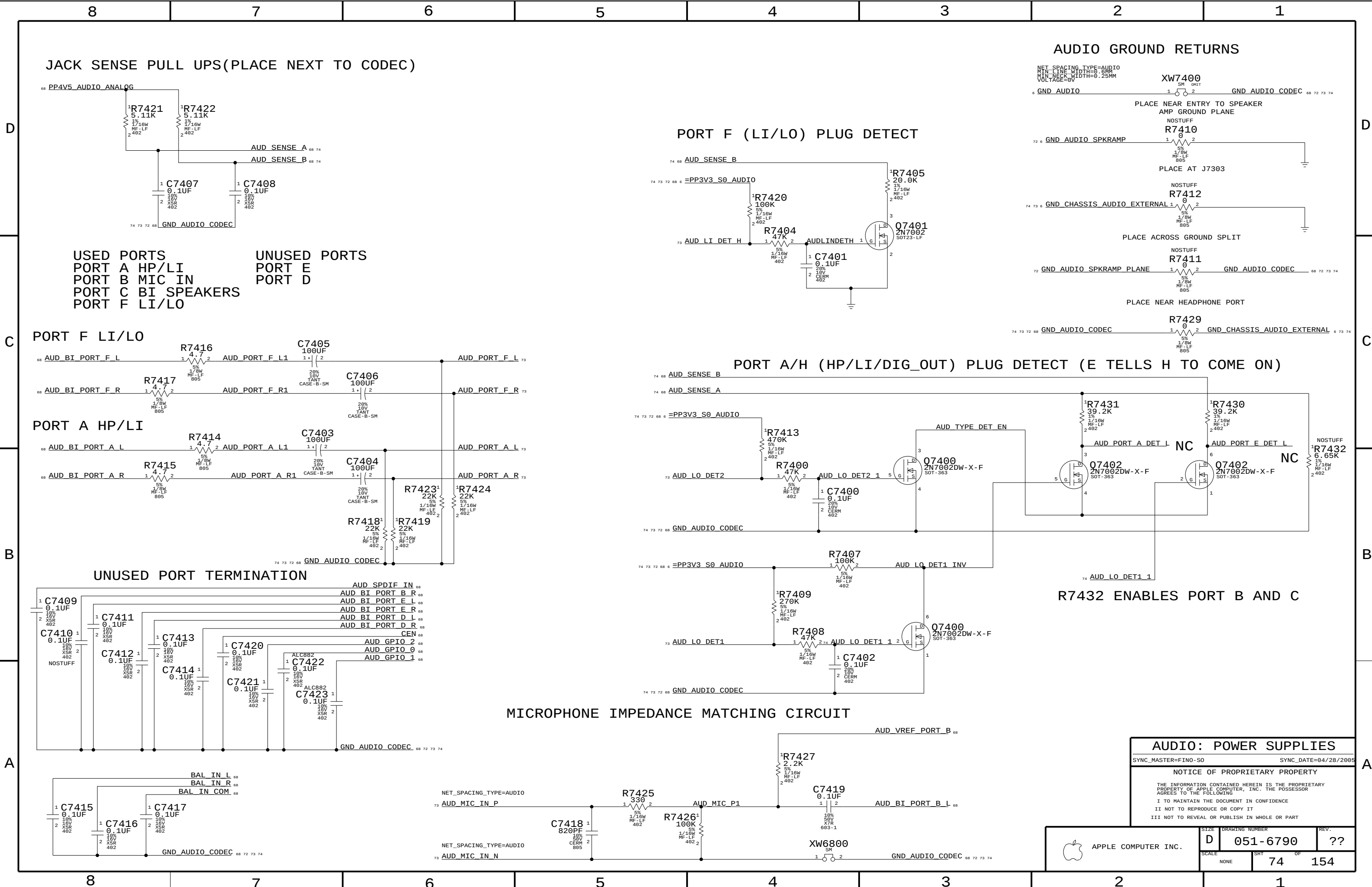
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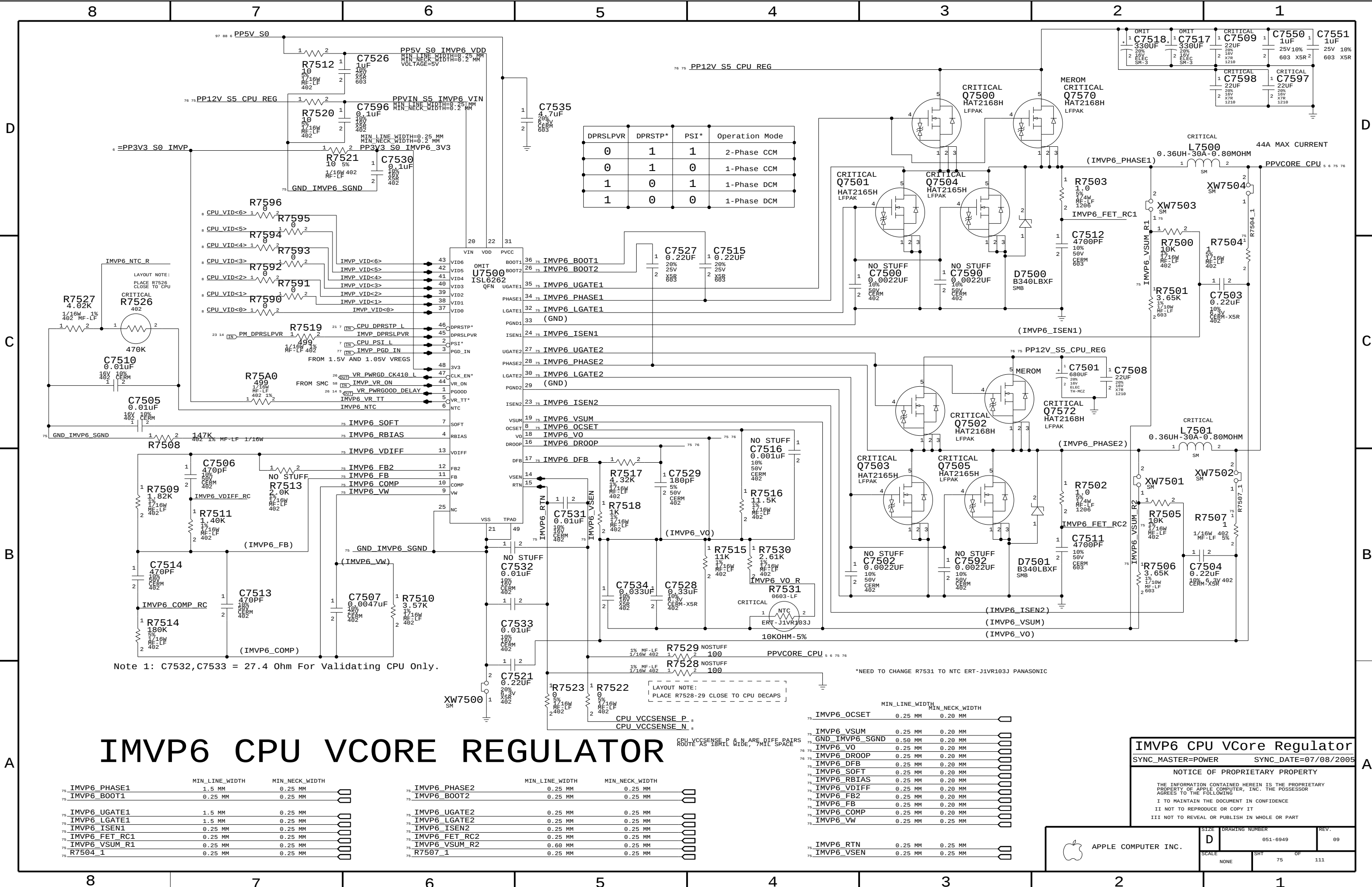
DRAWING NUMBER
051-6790

SHT
73

REV.
??

OF
154





IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DR00P	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
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IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

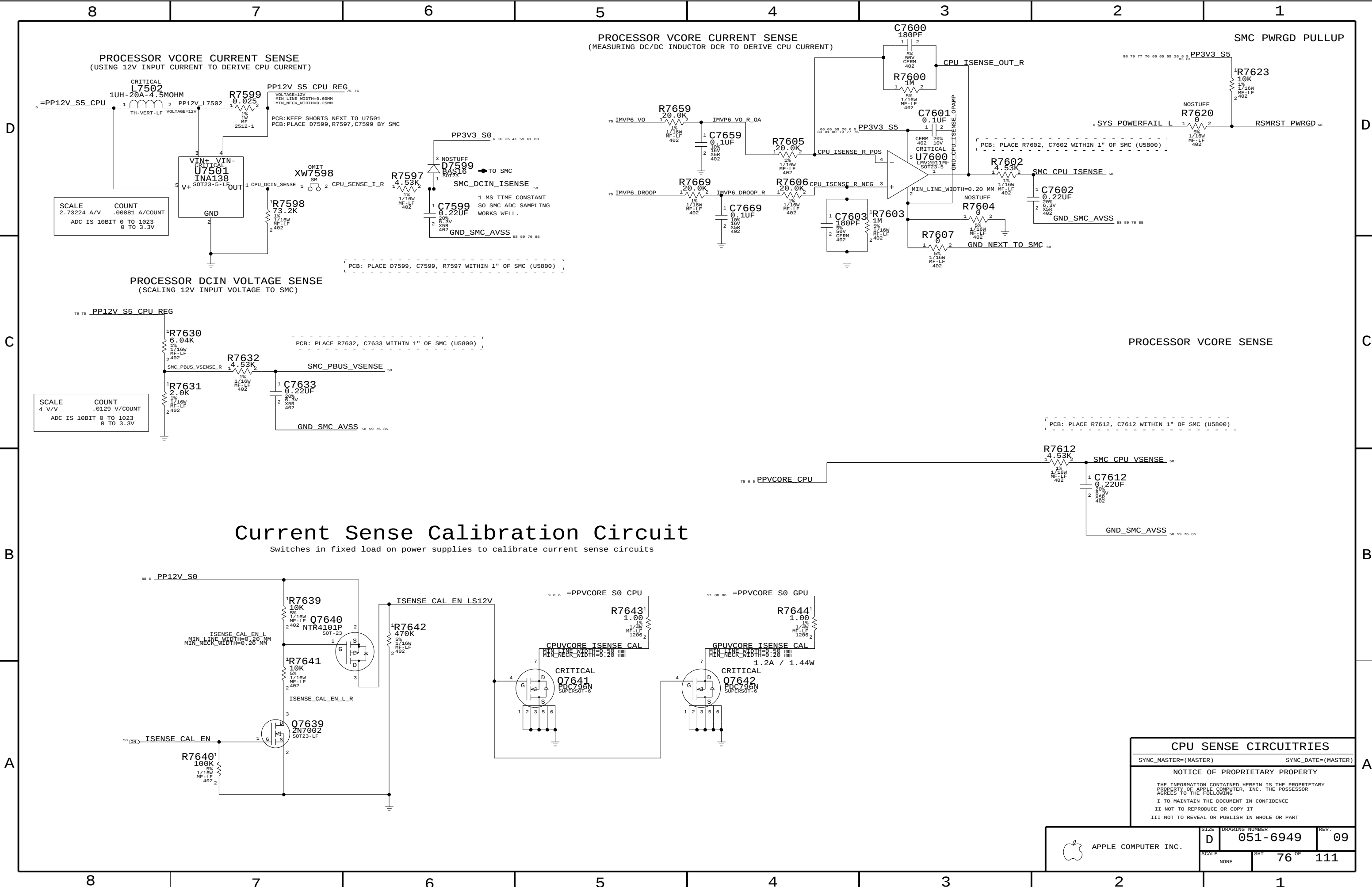
IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/08/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT	OF
NONE	75	111



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

CPU SENSE CIRCUITRIES

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

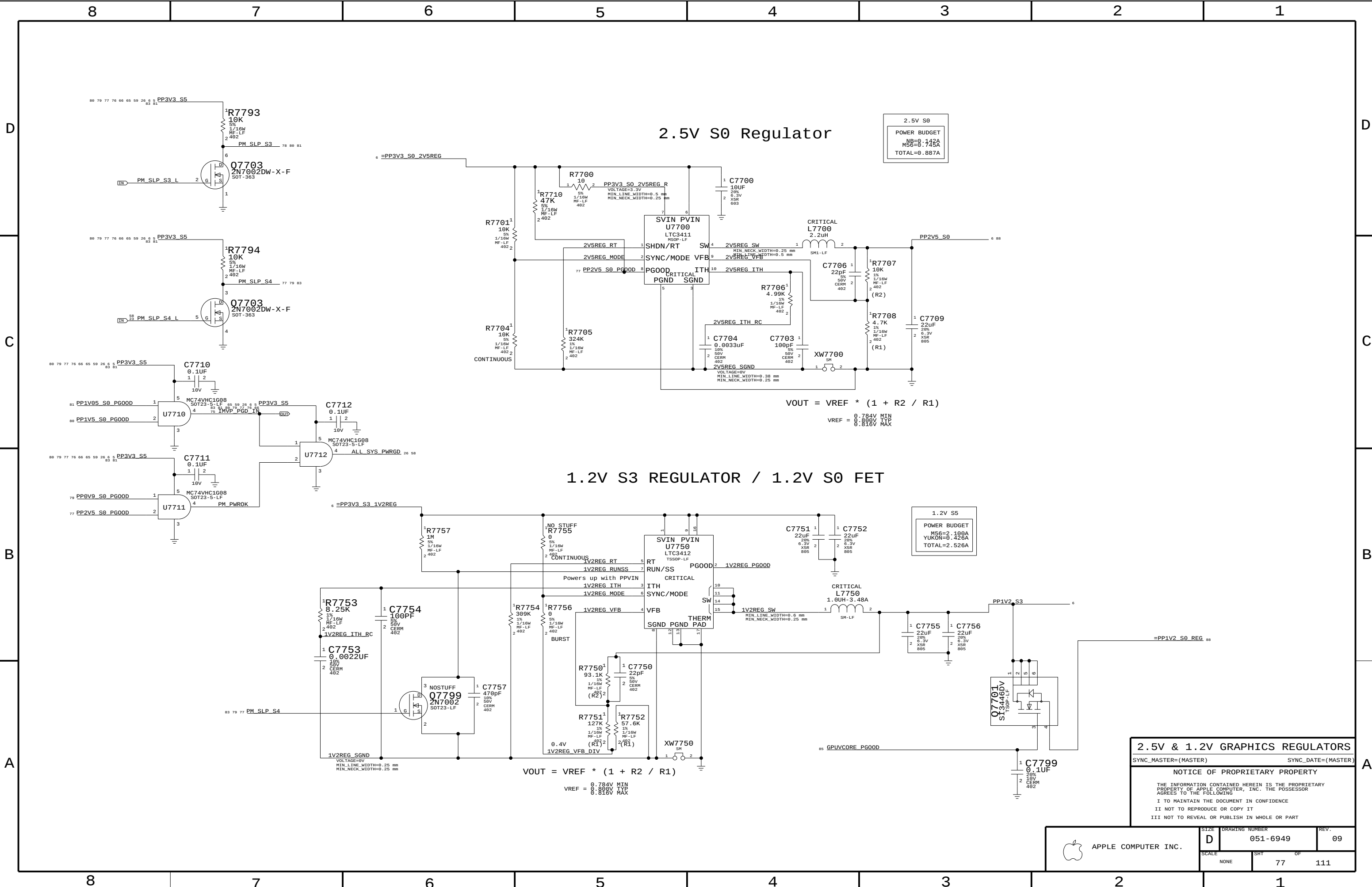
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	D	051-6949	09
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NONE			



2.5V & 1.2V GRAPHICS REGULATORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

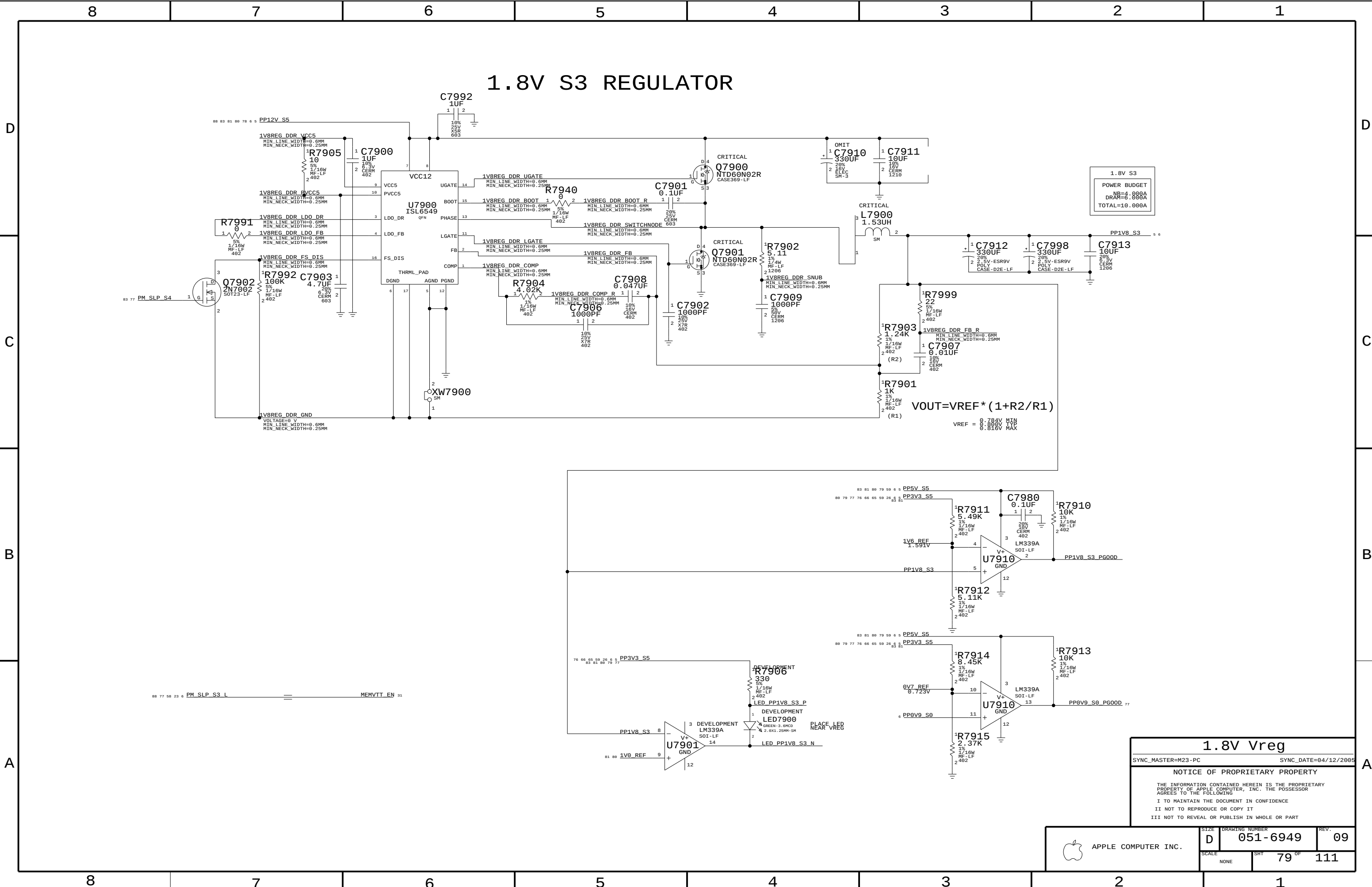
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	D	051-6949	09
SCALE	SHT		OF
	NONE		77 111



1.8V S3 REGULATOR

1.8V S3
POWER BUDGET
N=0.800A
DRA=0.800A
TOTAL=10.000A

$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

$$V_{REF} = 0.784V \text{ MIN}$$

$$0.800V \text{ TYP}$$

$$0.816V \text{ MAX}$$

1.8V Vreg
SYNC_MASTER=M23-PC
SYNC_DATE=04/12/2005
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	D	051-6949	09
SCALE		SHT	79 OF 111
NONE			

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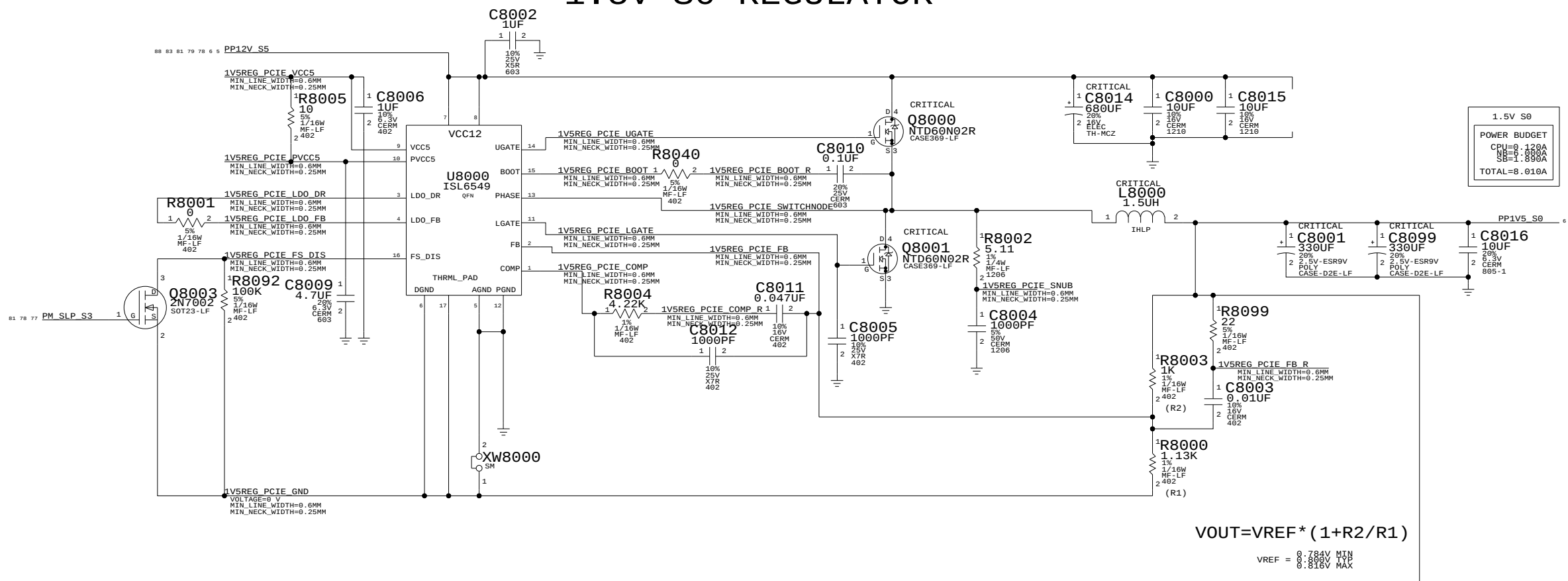
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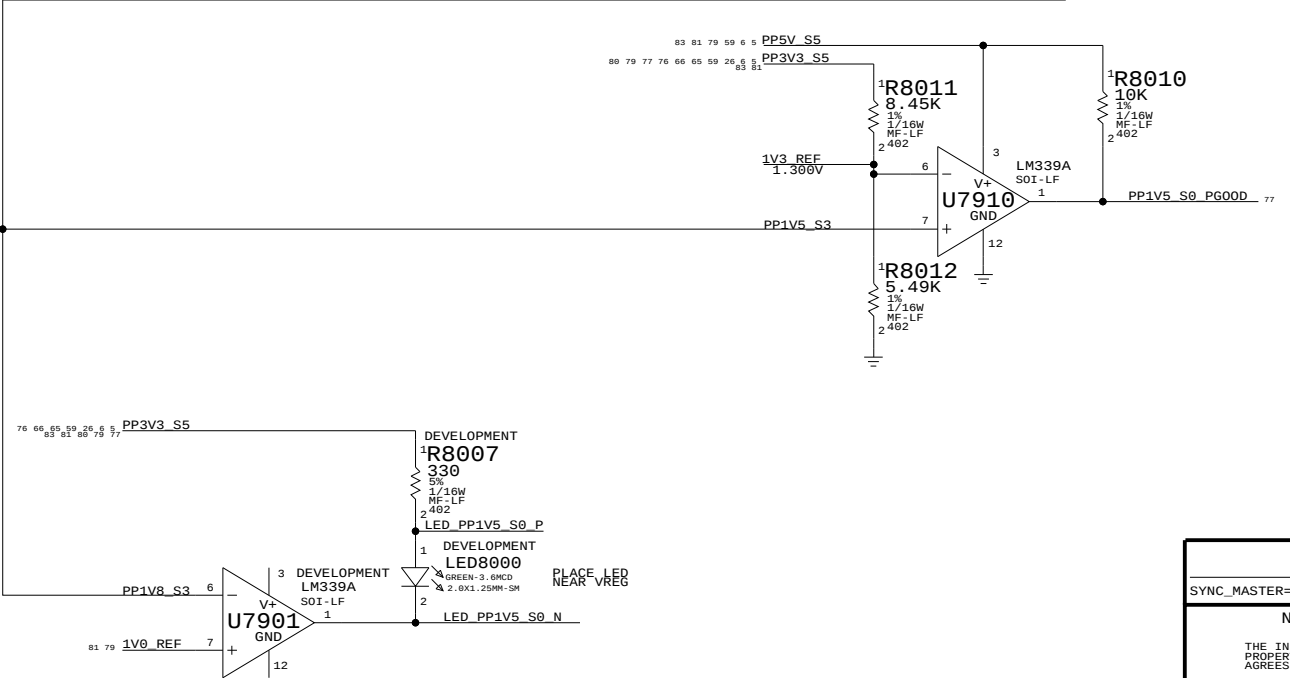
1.5V S0 REGULATOR



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

$$V_{REF} = 0.784V \text{ MIN}$$

$$0.816V \text{ MAX}$$



1.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

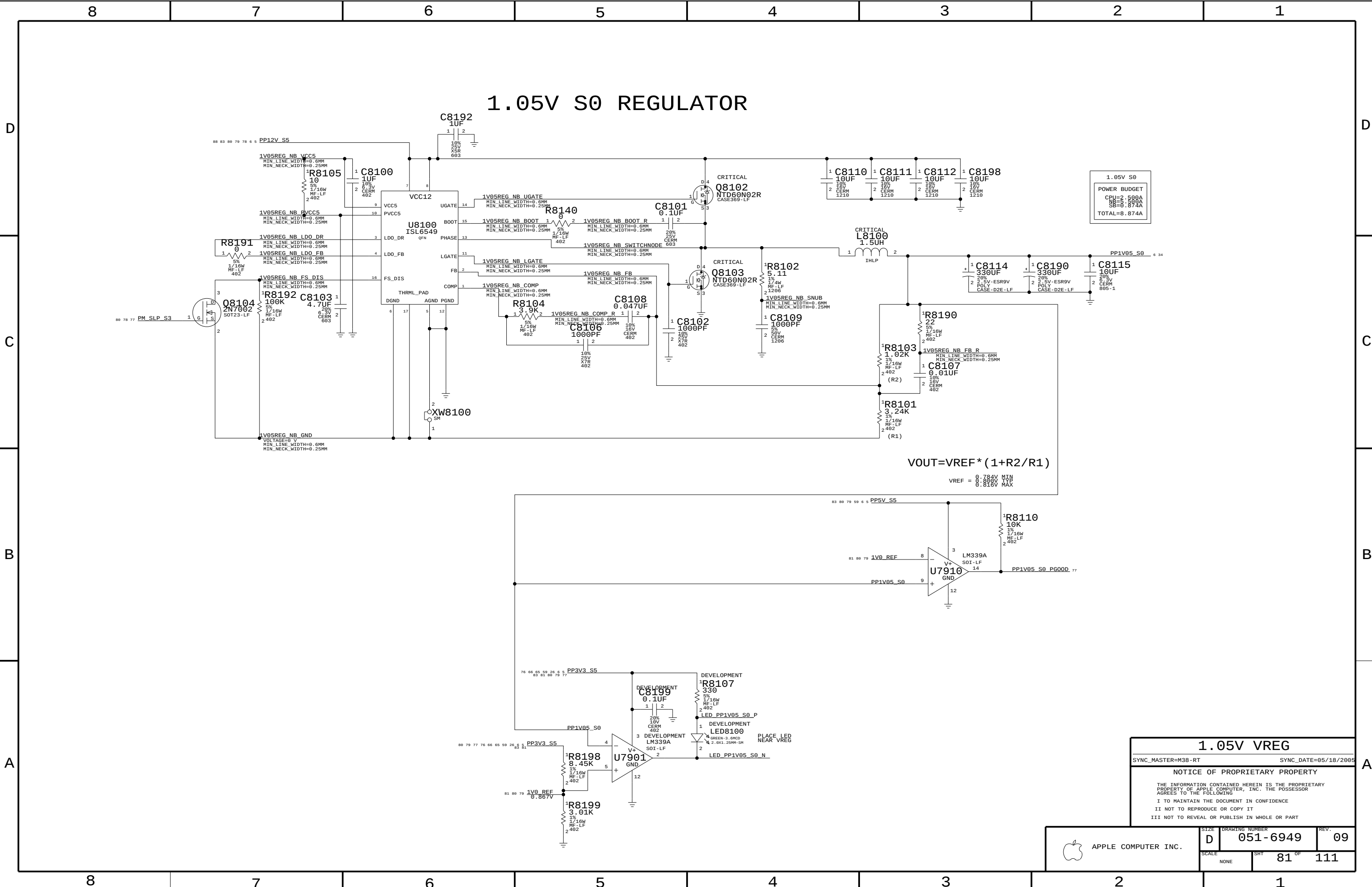
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	D	051-6950	06
SCALE		SHT	80 OF 111
NONE			



1.05V S0 REGULATOR

1.05V S0	
POWER BUDGET	
CPU=2.500A	
NB=5.890A	
SS=8.874A	
TOTAL=8.874A	

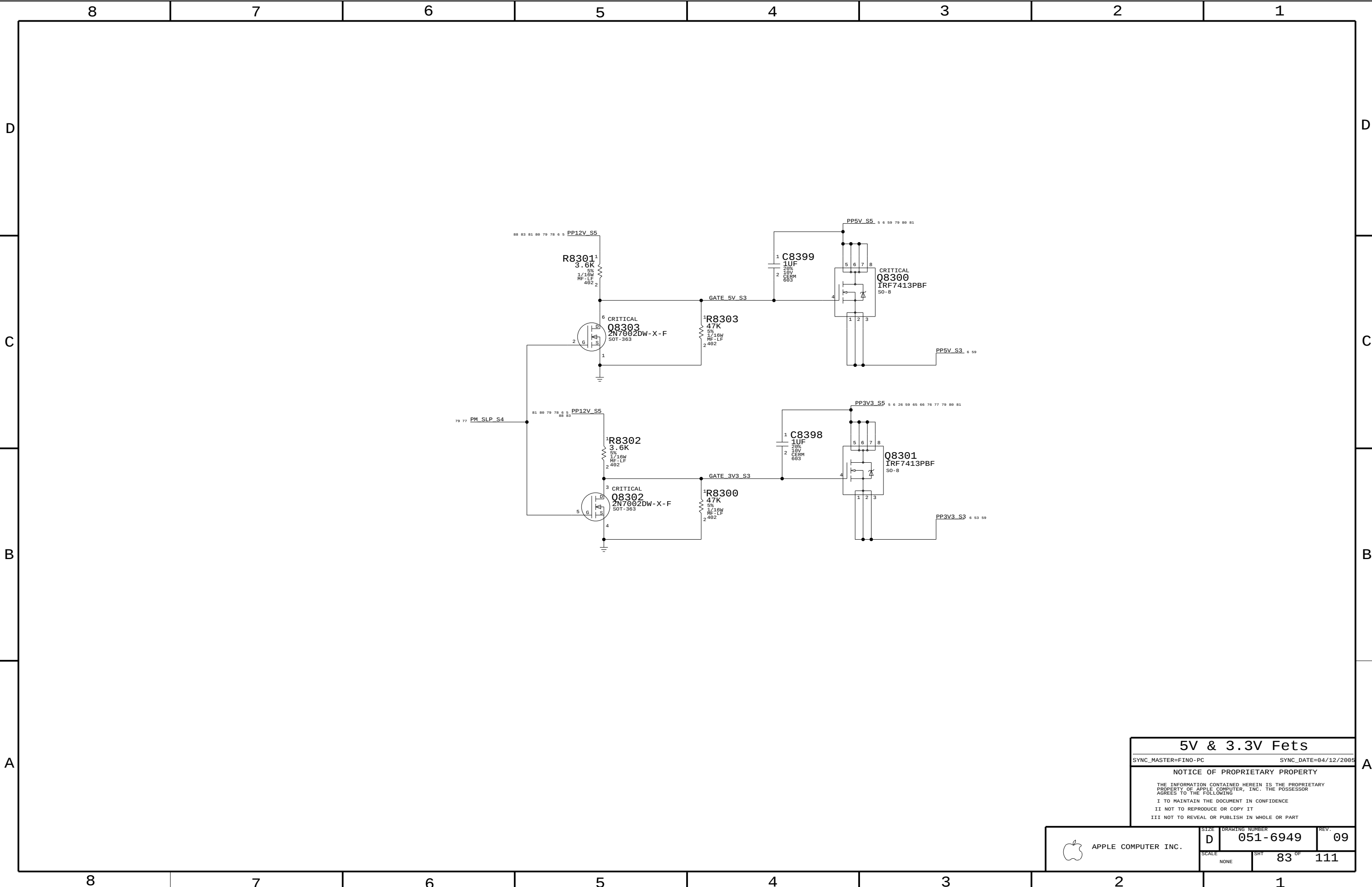
$$VOUT = VREF * (1 + R2/R1)$$

$$VREF = 0.784V \text{ MIN}$$

$$VREF = 0.816V \text{ MAX}$$

1.05V VREG		
SYNC_MASTER=M38-RT		SYNC_DATE=05/18/2005
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NONE			



5V & 3.3V Fets

SYNC_MASTER=FINO-PC

SYNC_DATE=04/12/2005

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SIZE

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DRAWING NUMBER

051-6949

REV.

09

SCALE

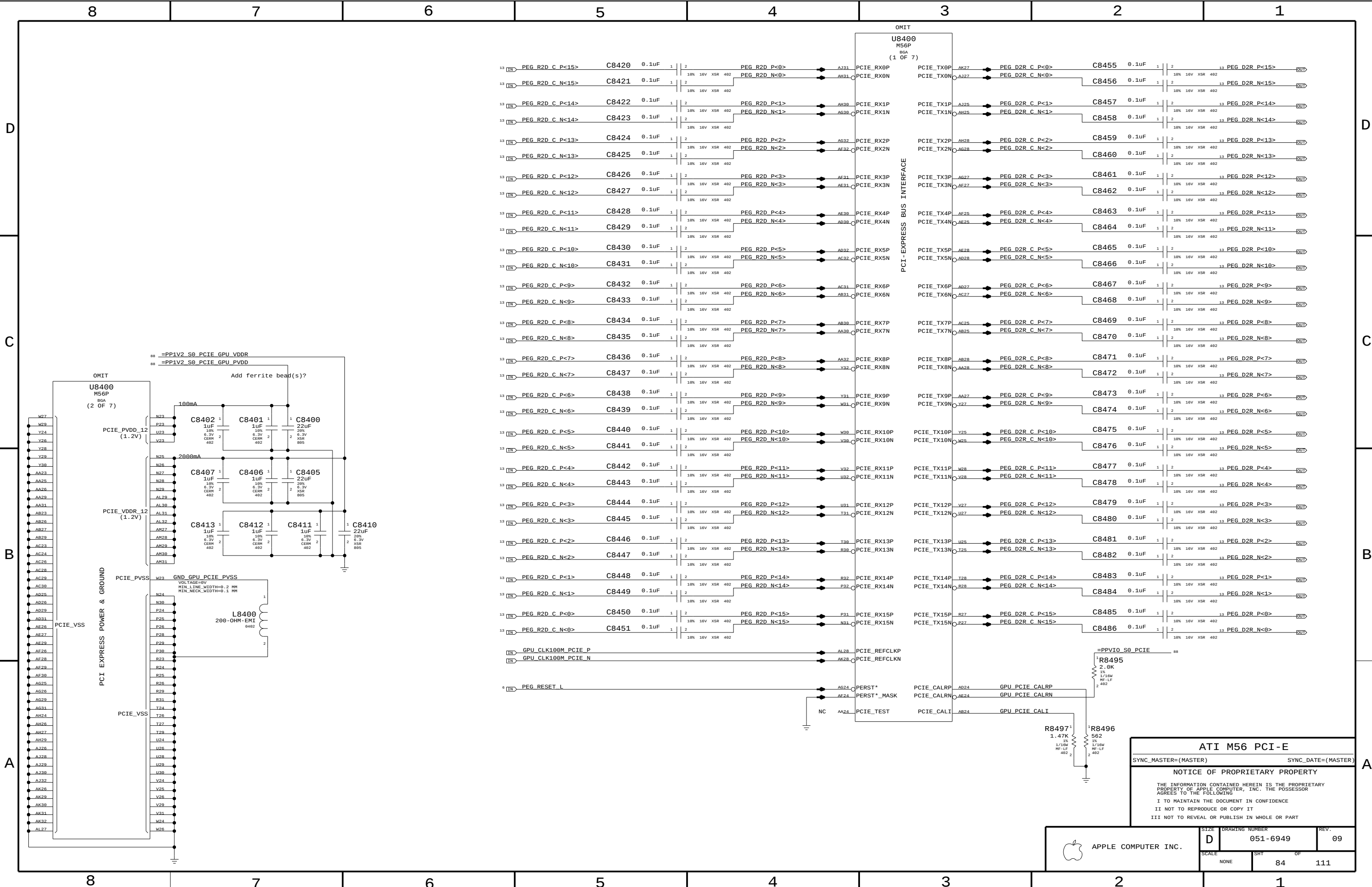
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SHT

83

OF

111



ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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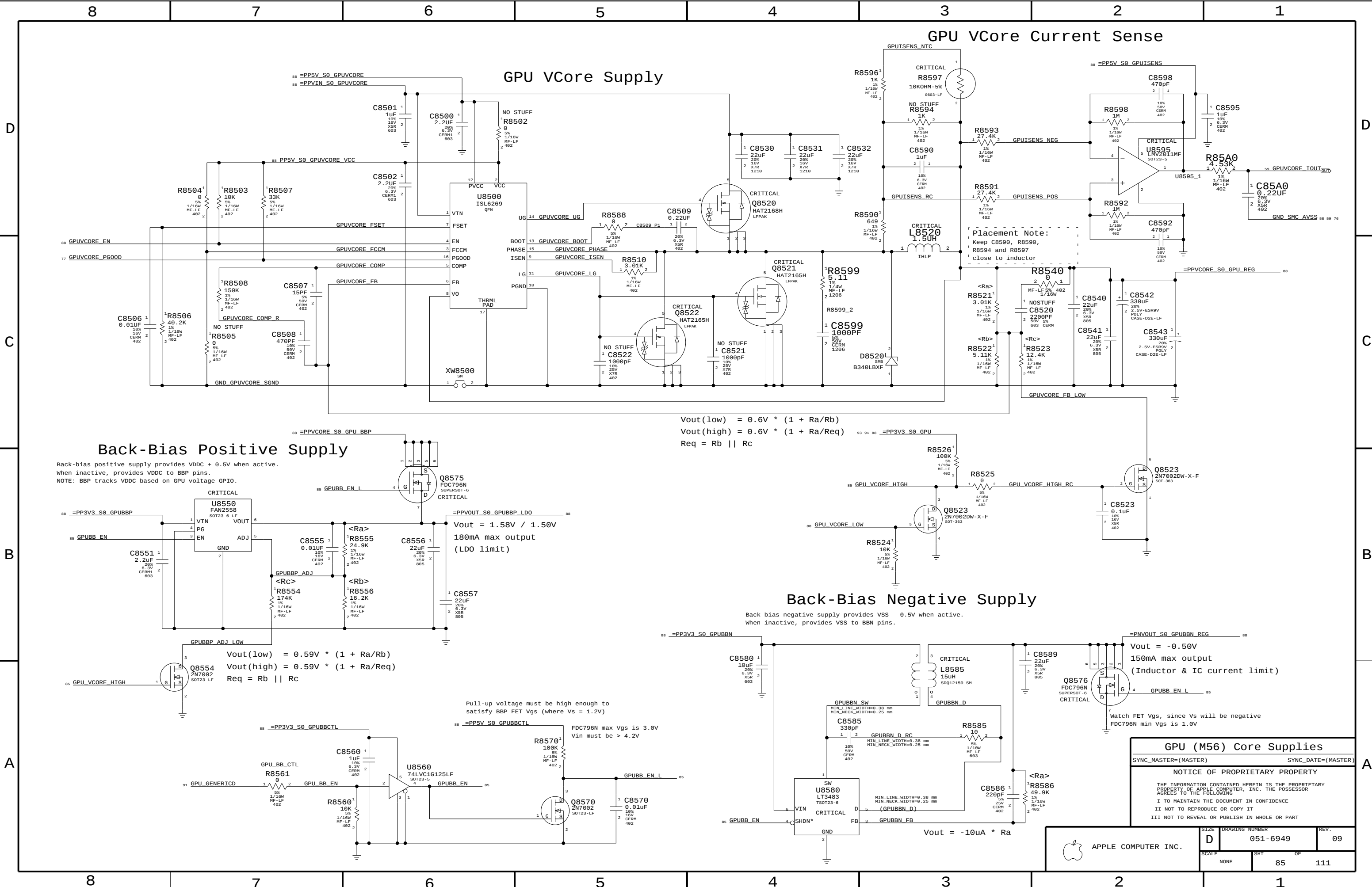
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
	SCALE	SHT OF	
	NONE	84	111



GPU VCore Supply

GPU VCore Current Sense

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active. When inactive, provides VDDC to BBP pins. NOTE: BBP tracks VDDC based on GPU voltage GPIO.

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.5V when active. When inactive, provides VSS to BBN pins.

$$V_{out(LOW)} = 0.6V \cdot (1 + R_a/R_b)$$
$$V_{out(HIGH)} = 0.6V \cdot (1 + R_a/R_{eq})$$
$$R_{eq} = R_b || R_c$$

$$V_{out(LOW)} = 0.59V \cdot (1 + R_a/R_b)$$
$$V_{out(HIGH)} = 0.59V \cdot (1 + R_a/R_{eq})$$
$$R_{eq} = R_b || R_c$$

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
FDC796N max Vgs is 3.0V
Vin must be > 4.2V

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER)

SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

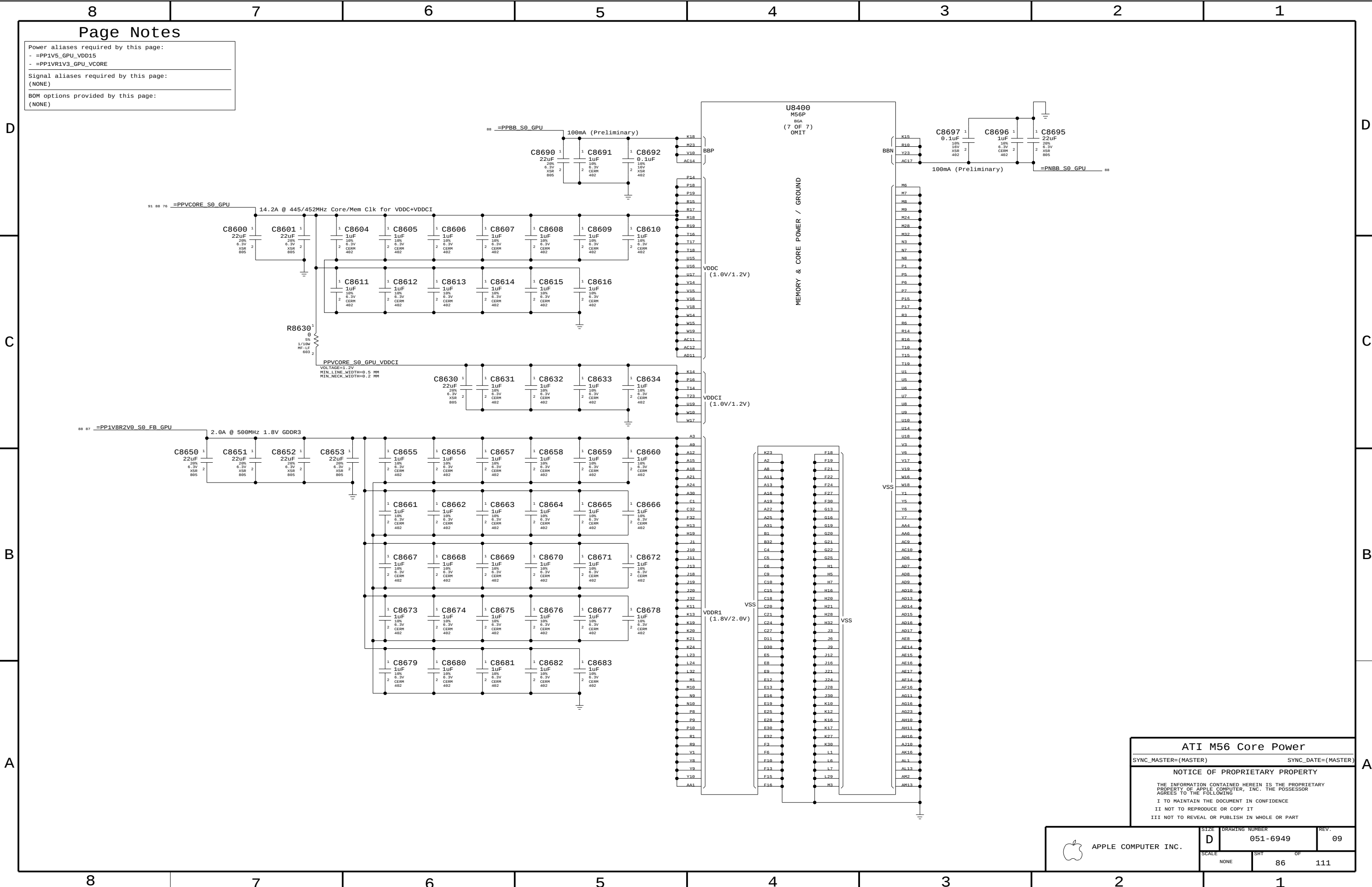
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	NONE		85 111



ATI M56 Core Power

SYNC_MASTER=(MASTER)SYNC_DATE=(MASTER)

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Page Notes

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- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
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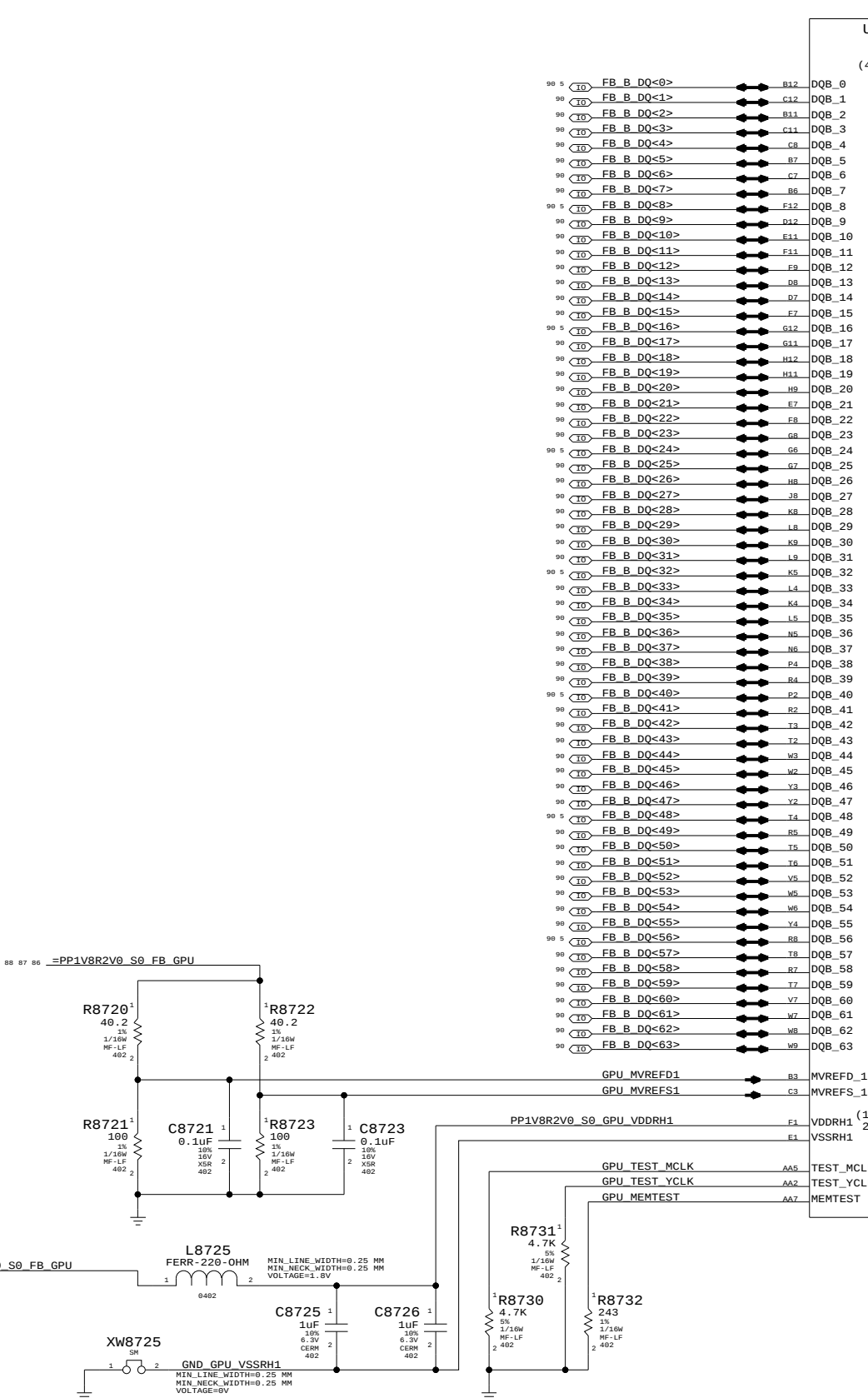
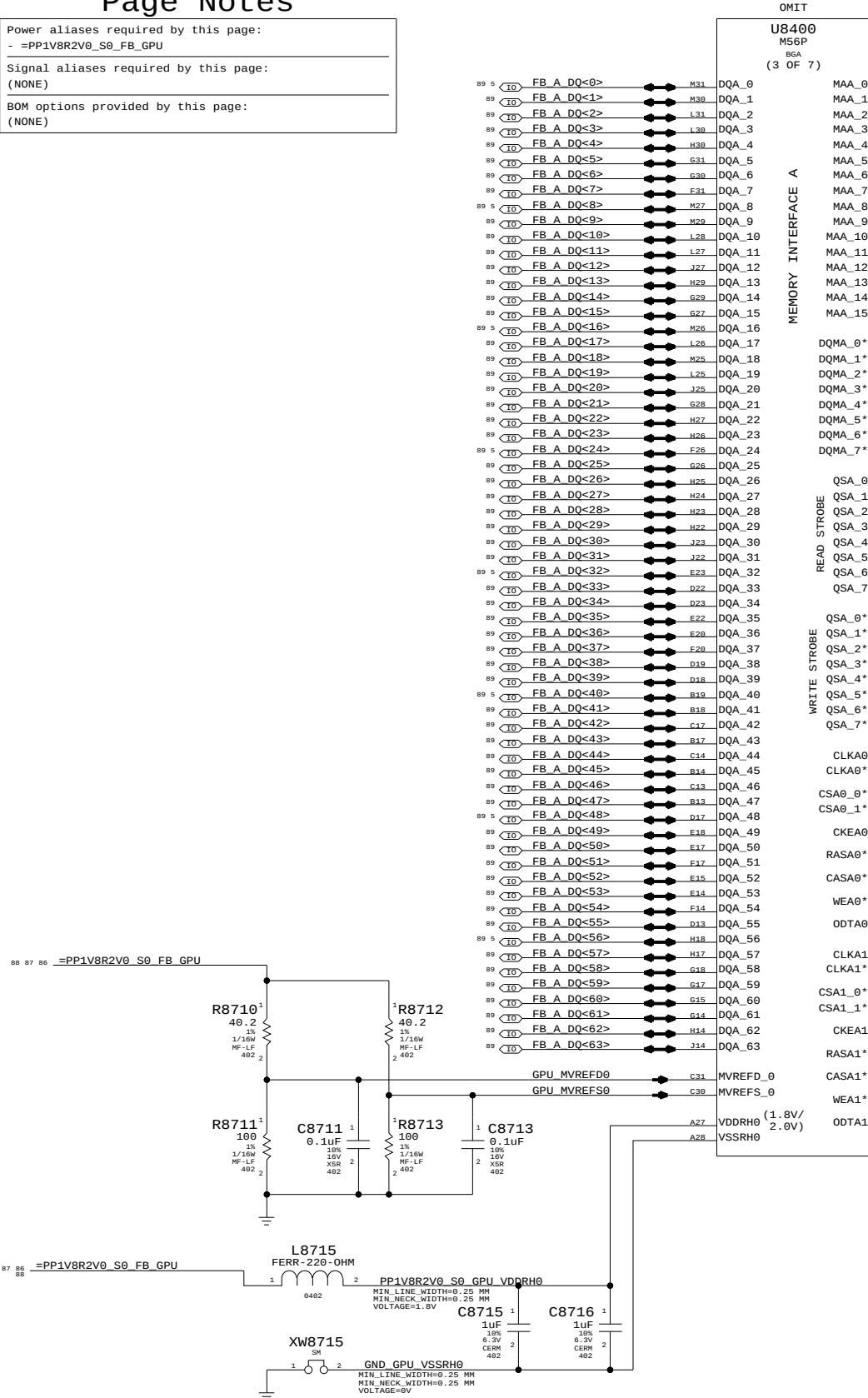
BOM options provided by this page:
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D

C

B

A

ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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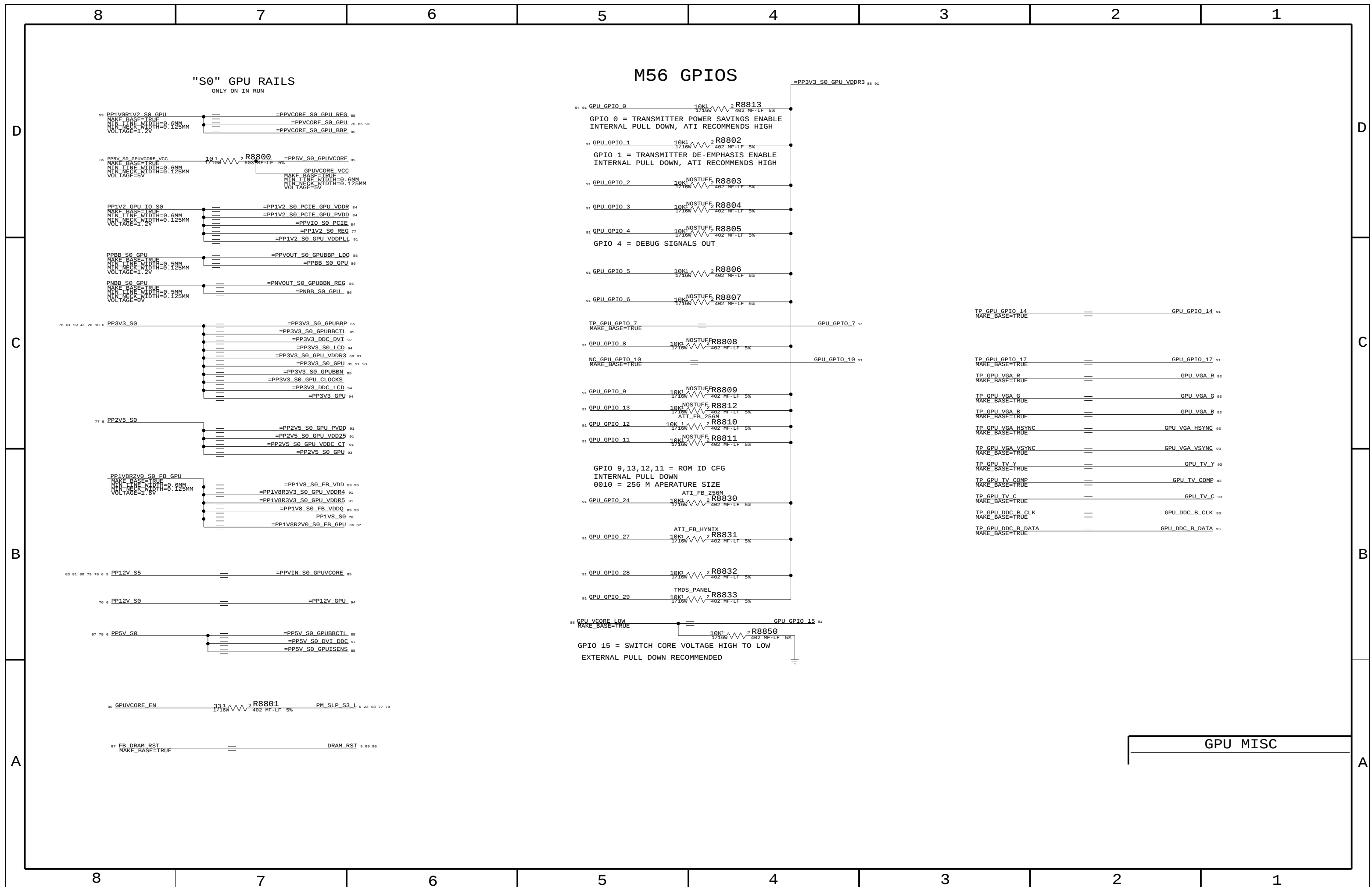
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-6949 REV. 09

SCALE NONE SHY OF 87 111



Power aliases required by this page:
 - =PP1V8_S0_FB_VDD
 - =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
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BOM options provided by this page:
 (NONE)

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

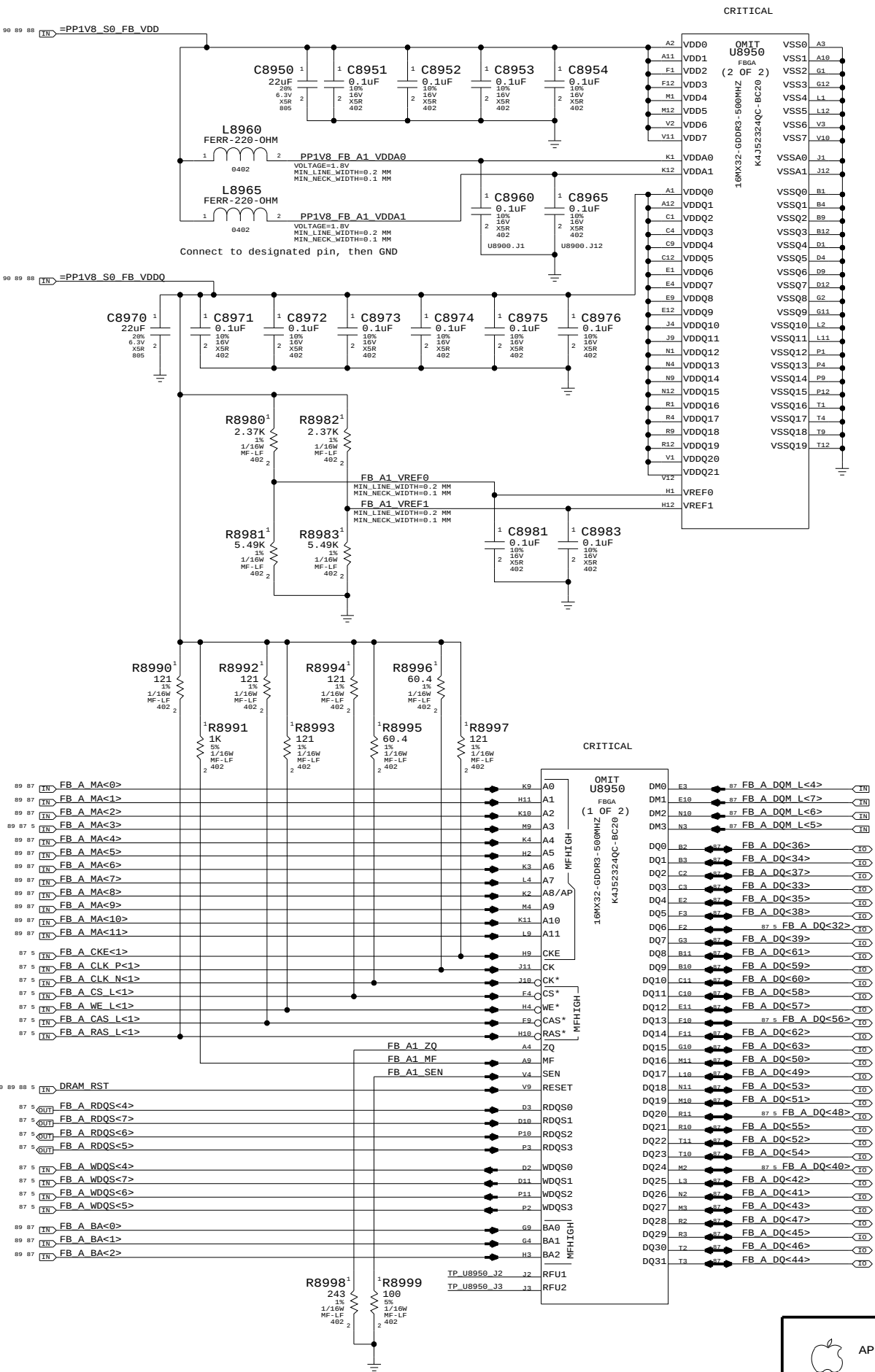
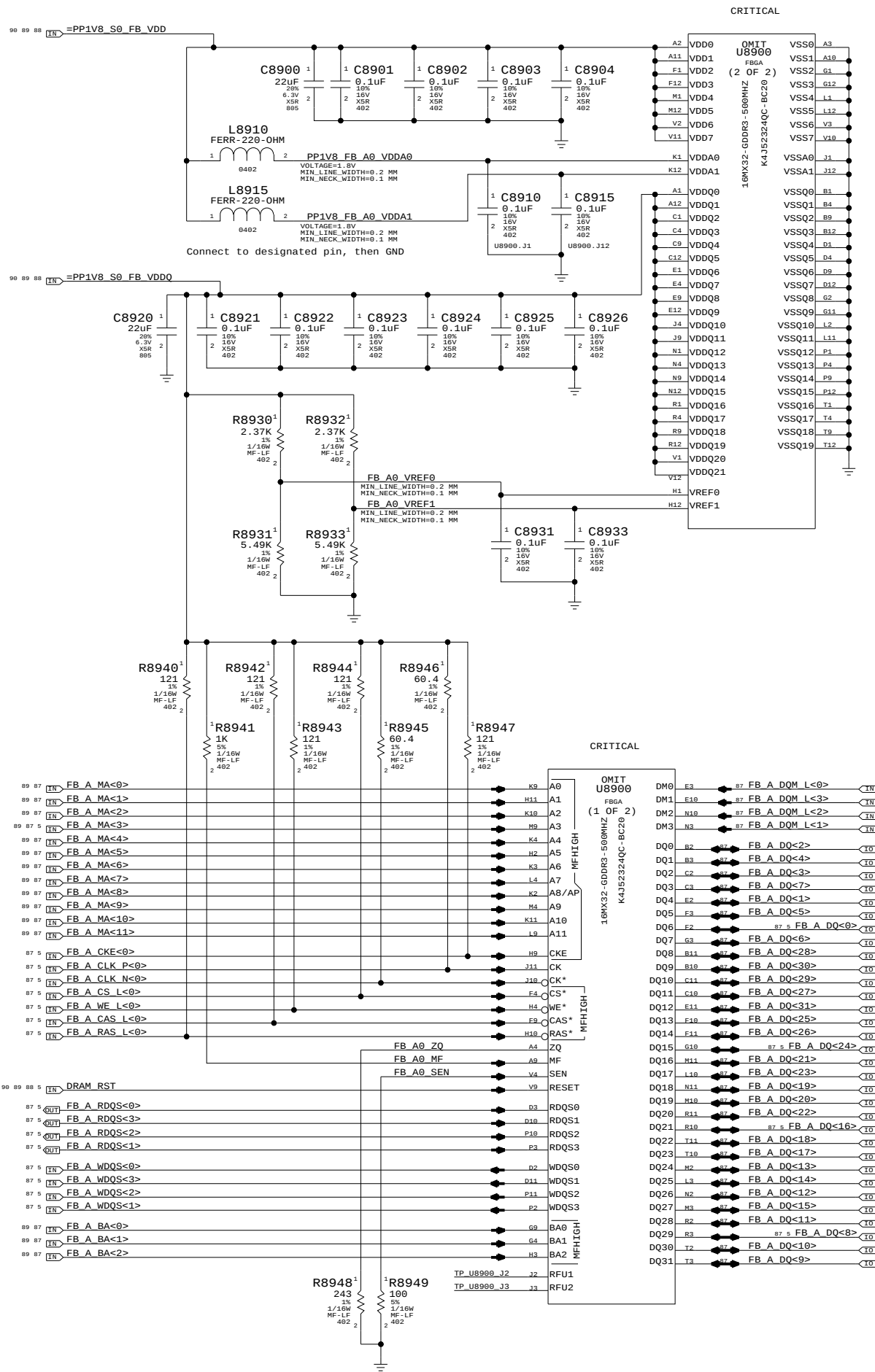
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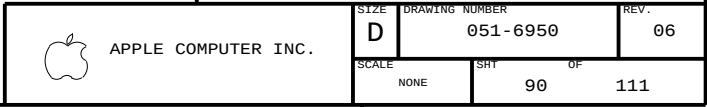
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SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT	OF
NONE	89	111





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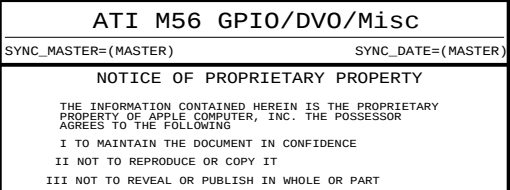
- PP3V3V3_GPU_GPIOS
- PP2V5_PVDD
- PP1V8_GPU_LVDS_PLL

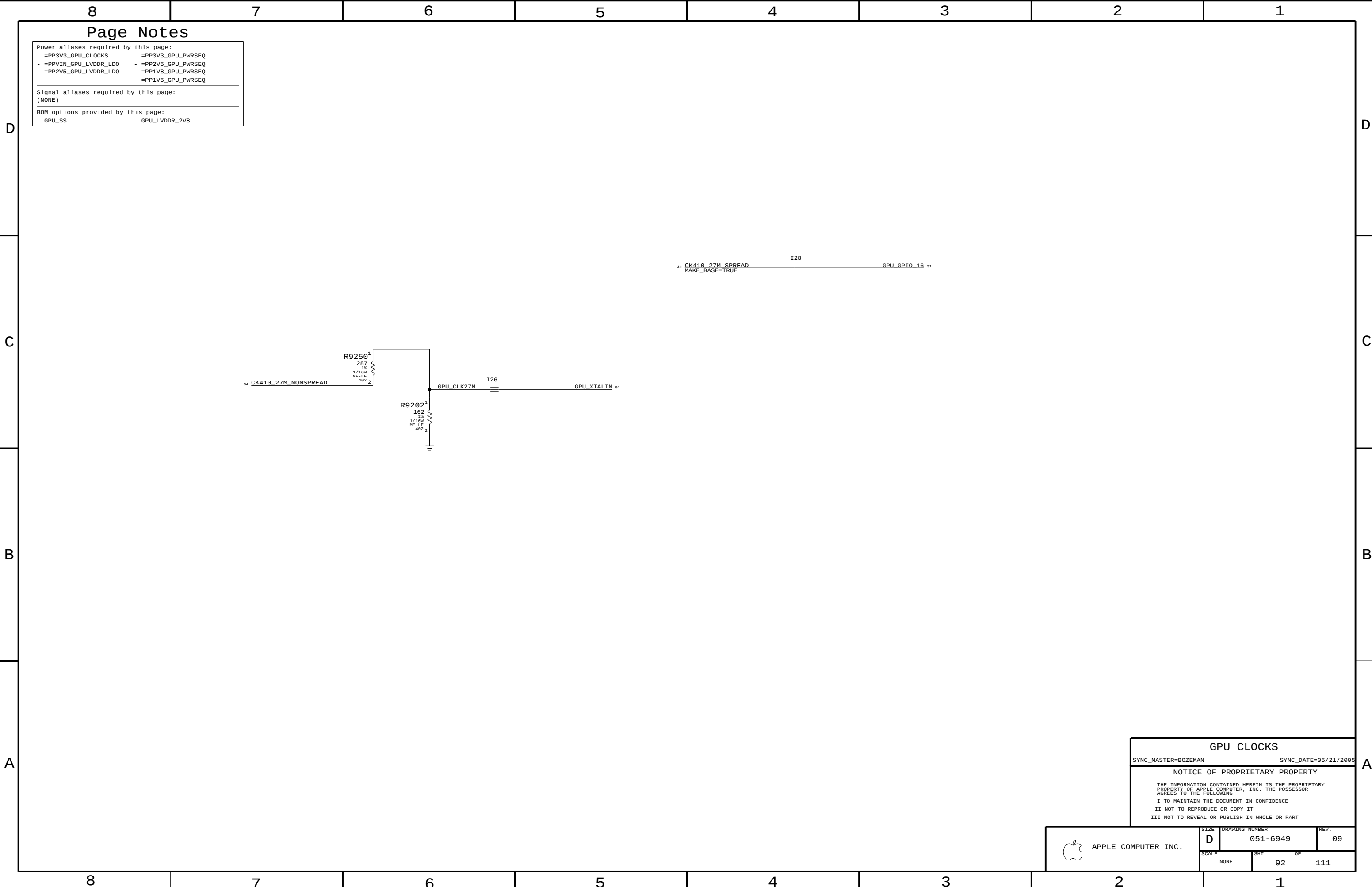
Signal aliases required by this page:

- I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:

(NONE)





Page Notes

Power aliases required by this page:

- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

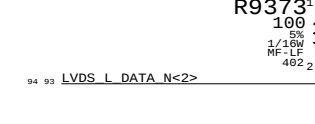
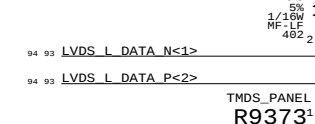
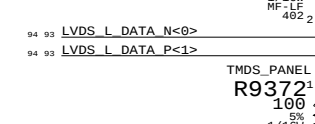
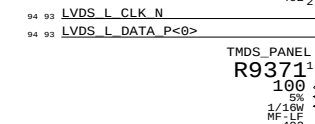
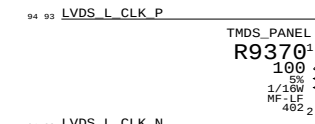
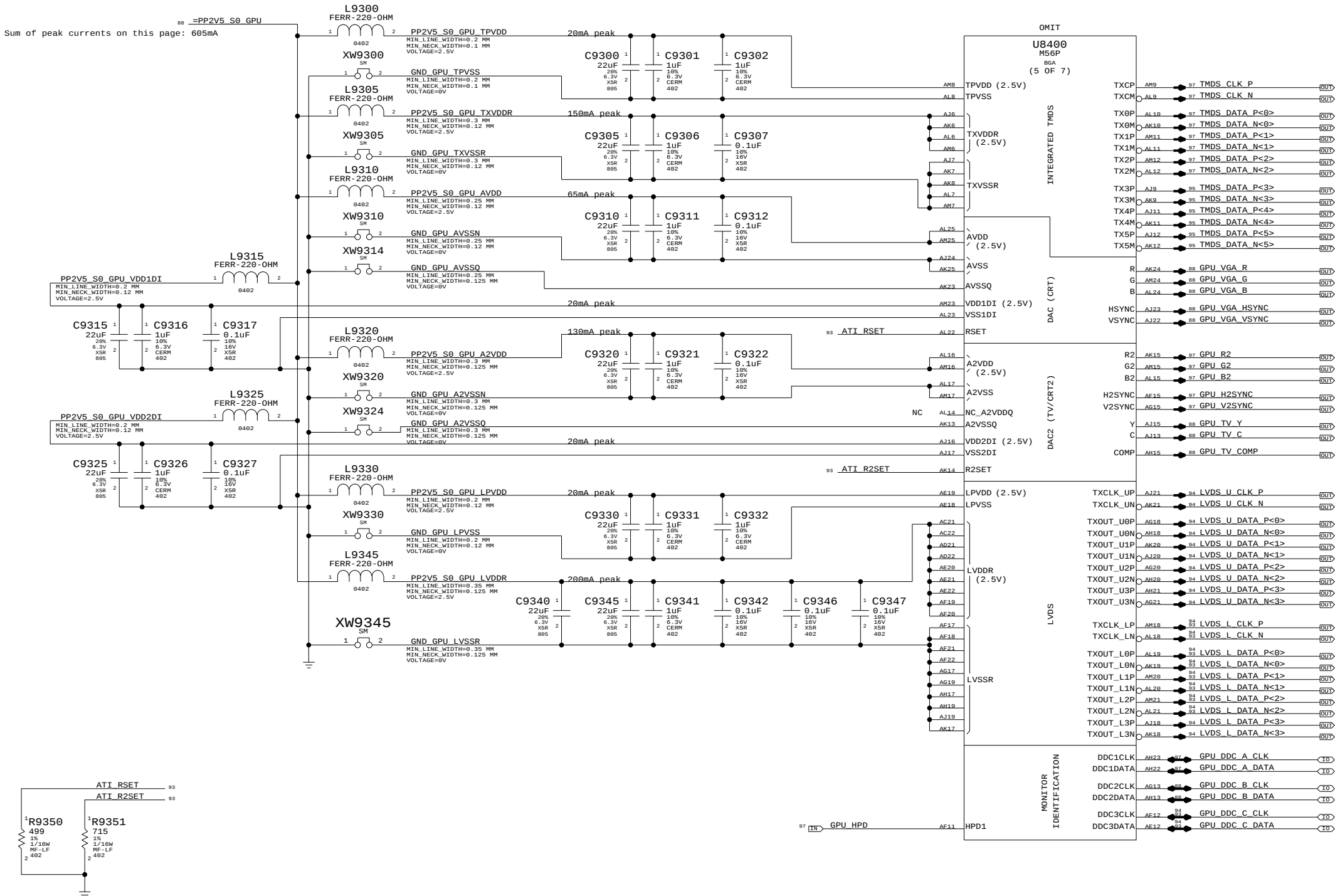
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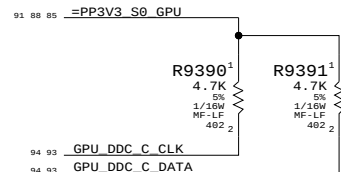
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TERMINATION FOR TMDS USAGE OF LVDS PINS
PLACE CLOSE TO GPU (U8400)



Composite/S-video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb



ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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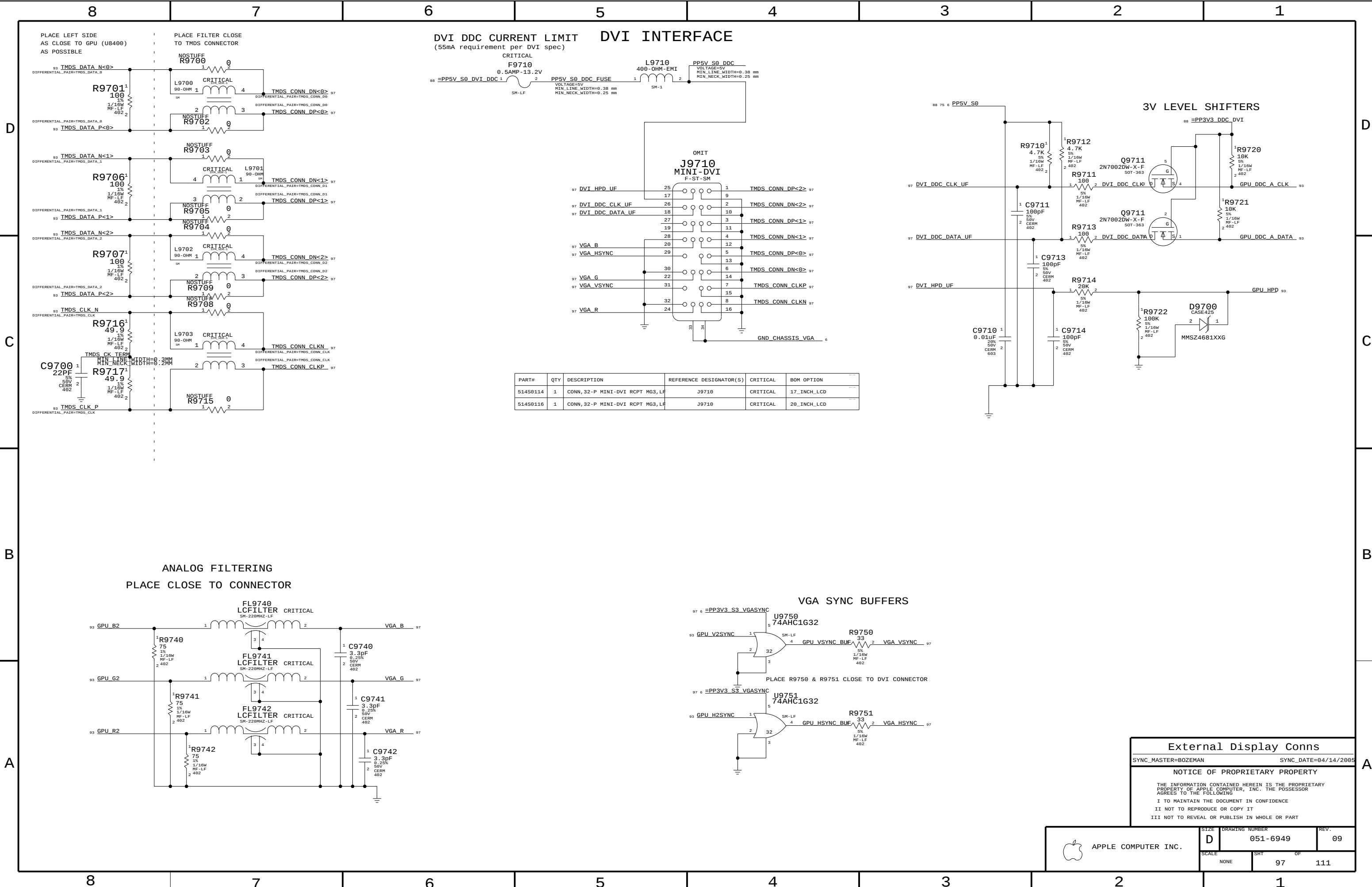
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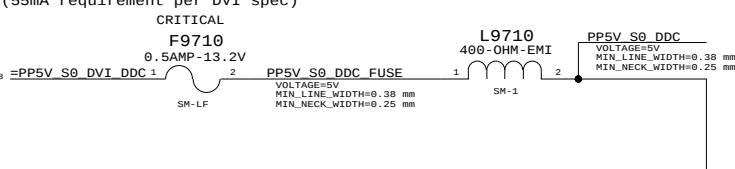
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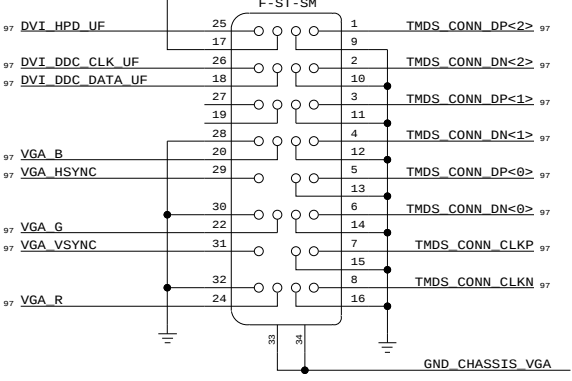
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DVI DDC CURRENT LIMIT DVI INTERFACE

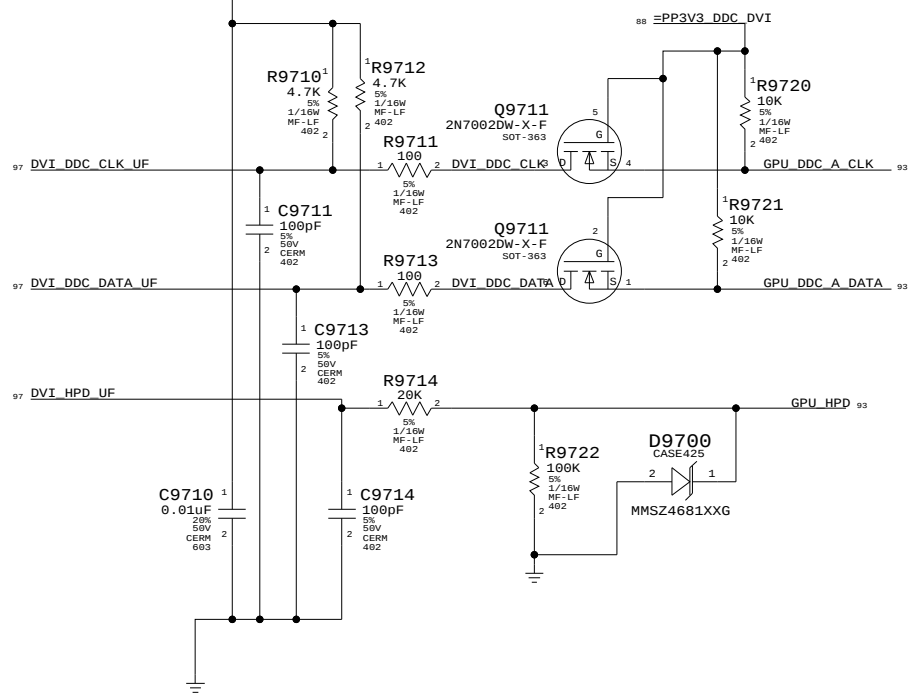


OMIT J9710 MINI-DVI F-ST-SM

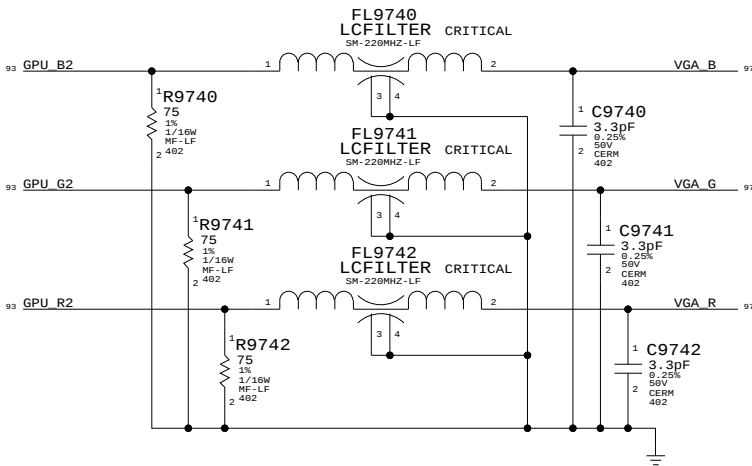


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0114	1	CONN, 32-P MINI-DVI RCPT MG3, LF	J9710	CRITICAL	17_INCH_LCD
514S0116	1	CONN, 32-P MINI-DVI RCPT MG3, LF	J9710	CRITICAL	20_INCH_LCD

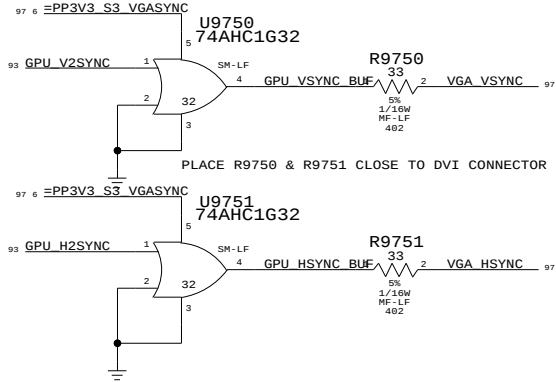
3V LEVEL SHIFTERS



ANALOG FILTERING PLACE CLOSE TO CONNECTOR



VGA SYNC BUFFERS



External Display Conns

SYNC_MASTER=BOZEMAN SYNC_DATE=04/14/2005

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	Q8575	TRA_FDC796N_SUPERSOT	m39[85B6]	R2317	RES_402	m39[23D7]	R3463	RES_402	m39[34A7]	R5828	RES_402	m39[5983]											
C	Q8576	TRA_FDC796N_SUPERSOT	m39[85A2]	R2318	RES_402	m39[23D7]	R3470	RES_402	m39[34A5]	R5829	RES_402	m39[59C3]											
	Q9400	TRA_SI3443DV_TSOP-LF	m39[94C7]	R2319	RES_402	m39[23D2]	R3471	RES_402	m39[34A5]	R5830	RES_402	m39[59C3]											
	Q9401	TRA_2N7002_S0T23-LF	m39[94C7]	R2320	RES_402	m39[23D7]	R3485	RES_402	m39[34D1]	R5831	RES_402	m39[59C3]											
	Q9711	TRA_2N7002DW_S0T-363	m39[97D2 97C2]	R2323	RES_402	m39[23D5]	R3486	RES_402	m39[34D1]	R5832	RES_402	m39[59C3]											
	R7500	RES_402	m39[75C7]	R2326	RES_402	m39[23D6]	R3487	RES_402	m39[34D1]	R5833	RES_402	m39[5983]											
	R8500	RES_402	m39[85D1]	R2327	RES_402	m39[23D6]	R3488	RES_402	m39[34D1]	R5898	RES_402	m39[58C2]											
	R600	RES_603	m39[6A7]	R2343	RES_402	m39[23D1]	R3489	RES_402	m39[34D2]	R5900	RES_402	m39[58D3]											
	R601	RES_402	m39[6D8]	R2388	RES_402	m39[23A3]	R3490	RES_402	m39[34D2]	R5900	RES_402	m39[59D7]											
	R602	RES_603	m39[6A7]	R2389	RES_402	m39[38D5]	R3491	RES_402	m39[34D2]	R5901	RES_402	m39[59D6]											
	R603	RES_402	m39[6B1]	R2390	RES_402	m39[2383]	R3492	RES_402	m39[34D2]	R5902	RES_402	m39[59D7]											
B	R605	RES_603	m39[6A7]	R2395	RES_402	m39[23D7]	R3493	RES_402	m39[34D7]	R5903	RES_402	m39[59D2]											
	R611	RES_402	m39[6B7]	R2396	RES_402	m39[23D6]	R3494	RES_402	m39[34D7]	R5904	RES_402	m39[59D2]											
	R612	RES_402	m39[6B7]	R2397	RES_402	m39[23D6]	R3495	RES_402	m39[34D7]	R5905	RES_402	m39[59D2]											
	R614	RES_402	m39[6B7]	R2398	RES_402	m39[23D8]	R3496	RES_402	m39[34C5]	R5906	RES_402	m39[59D2]											
	R615	RES_402	m39[6B7]	R2399	RES_402	m39[23C1]	R3497	RES_402	m39[34D4]	R5907	RES_402	m39[59B7]											
	R616	RES_402	m39[6A7]	R2500	RES_603	m39[25A8]	R3498	RES_402	m39[34D5]	R5910	RES_402	m39[59D2]											
	R617	RES_402	m39[6A7]	R2501	RES_402	m39[25C8]	R3499	RES_402	m39[34D5]	R5911	RES_402	m39[59D2]											
	R618	RES_402	m39[6C7]	R2502	RES_402	m39[25D8]	R3824	RES_402	m39[38D2]	R5912	RES_402	m39[59D2]											
	R619	RES_402	m39[6B7]	R2600	RES_402	m39[26C7]	R3851	RES_402	m39[38D3]	R5913	RES_402	m39[59D2]											
	R0702	RES_402	m39[7D6]	R2606	RES_402	m39[26C7]	R3852	RES_402	m39[38D2]	R5914	RES_402	m39[59C2]											
A	R0703	RES_402	m39[7C6]	R2607	RES_402	m39[26C8]	R3853	RES_402	m39[38D2]	R5915	RES_402	m39[59C2]											
	R0704	RES_402	m39[7C5]	R2609	RES_402	m39[26D7]	R3857	RES_402	m39[38B3]	R5916	RES_402	m39[59C2]											
	R0705	RES_402	m39[7B4]	R2611	RES_402	m39[26D5]	R3858	RES_402	m39[38B3]	R5917	RES_402	m39[59C2]											
	R0706	RES_402	m39[7A4]	R2612	RES_402	m39[26D5]	R3859	RES_402	m39[38B2]	R5919	RES_402	m39[59B4]											
	R0712	RES_402	m39[7A3]	R2622	RES_402	m39[26D4]	R3897	RES_402	m39[38B7]	R5920	RES_402	m39[59B5]											
	R0716	RES_402	m39[7B1]	R2623	RES_402	m39[26D2]	R3899	RES_402	m39[38B5]	R5921	RES_402	m39[59B5]											
	R0717	RES_402	m39[7B1]	R2624	RES_402	m39[26D2]	R4101	RES_402	m39[41D7]	R5922	RES_402	m39[59B5]											
	R0718	RES_402	m39[7B1]	R2625	RES_402	m39[26D2]	R4102	RES_402	m39[41C7]	R5923	RES_402	m39[59B5]											
	R0719	RES_402	m39[7B1]	R2626	RES_402	m39[26D2]	R4103	RES_402	m39[41C2]	R5924	RES_402	m39[59B5]											
	R0720	RES_402	m39[7B7]	R2627	RES_402	m39[26D2]	R4104	RES_402	m39[41C2]	R5925	RES_402	m39[59A1]											

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The image displays a PCB layout with a grid of dimensions (1-8) and a list of components. The components are organized into rows and columns, with their values and footprints listed. The components are:

Component	Value	Footprint
XW9330	SHORT_SM	m39[93B7]
XW9345	SHORT_SM	m39[93A7]
Y2600	CRYSTAL_4PIN_SM-LF	m39[26D8]
Y3301	CRYSTAL_5X3.2-SM	m39[33C7]
Y4101	CRYSTAL_4PIN_SM-3	m39[41B5]
Y4400	CRYSTAL_HC49-USMD	m39[44D2]
Y5800	CRYSTAL_SM-3	m39[59B8]
Y6700	CRYSTAL_4PIN_SM-LF	m39[59B7]
ZH500	HOLE_VIA	m39[5C1]
ZH501	HOLE_VIA	m39[5C1]
ZH502	HOLE_VIA	m39[5C1]
ZH503	HOLE_VIA	m39[5C1]
ZH504	HOLE_VIA	m39[5B1]
ZH505	HOLE_VIA	m39[5B1]
ZH506	HOLE_VIA	m39[5B1]
ZH507	HOLE_VIA	m39[5B1]
ZH508	HOLE_VIA	m39[5B1]
ZH509	HOLE_VIA	m39[5B1]
ZH510	HOLE_VIA	m39[5C1]
ZH511	HOLE_VIA	m39[5C1]
ZH512	HOLE_VIA	m39[5C1]
ZH513	HOLE_VIA	m39[5C1]
ZH514	HOLE_VIA	m39[5B1]
ZH515	HOLE_VIA	m39[5B1]
ZH516	HOLE_VIA	m39[5B1]
ZH517	HOLE_VIA	m39[5B1]
ZH518	HOLE_VIA	m39[5B1]
ZH519	HOLE_VIA	m39[5B1]
ZH520	HOLE_VIA	m39[5C1]
ZH521	HOLE_VIA	m39[5C1]
ZH522	HOLE_VIA	m39[5C1]
ZH523	HOLE_VIA	m39[5C1]
ZH524	HOLE_VIA	m39[5B1]
ZH525	HOLE_VIA	m39[5B1]
ZH526	HOLE_VIA	m39[5B1]
ZH527	HOLE_VIA	m39[5B1]
ZH528	HOLE_VIA	m39[5B1]
ZH529	HOLE_VIA	m39[5B1]
ZH601	MTGHOLE	m39[6A3]
ZH602	MTGHOLE	m39[6A3]
ZH603	MTGHOLE	m39[6A3]
ZH606	MTGHOLE	m39[6A1]
ZH607	MTGHOLE	m39[9D4]
ZH608	MTGHOLE	m39[9D3]
ZH609	MTGHOLE	m39[9D2]
ZH610	MTGHOLE	m39[9D2]