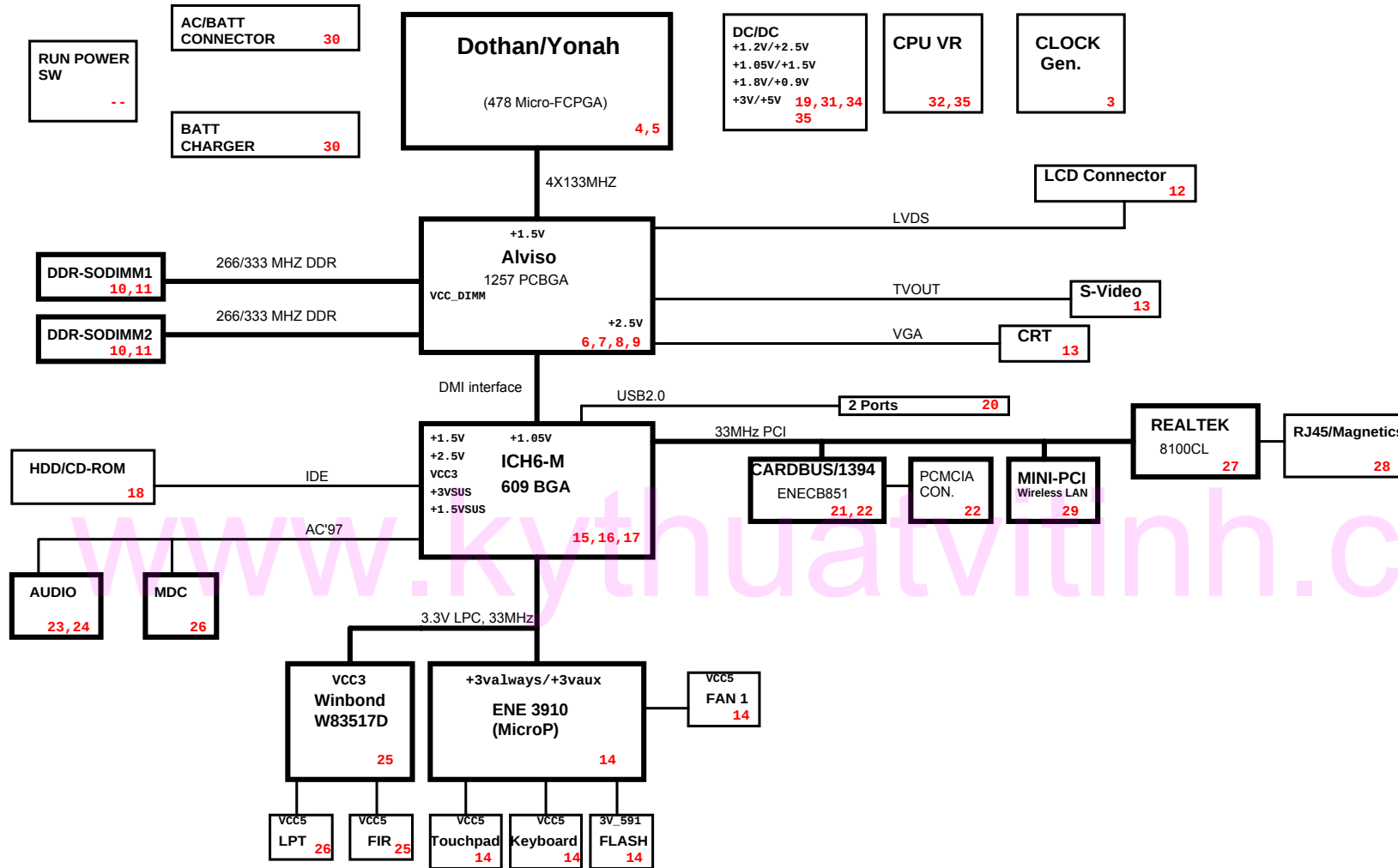




Page	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20
Rev.	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
Data	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21

Page	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
Rev.	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
Data	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21	2005/03/21

Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
12VOUT	X	X	X	X	
3V 591	X	X	X	X	
5VPSU	X	X	X	X	
+3V S5	X	X	X	X	SS ON
+1.8V S5	X	X	X	X	SS ON
+1.8V5US	X	X			SUSON
+3V5US	X	X			SUSON
+8V5US	X	X			SUSON
+0.9V5US	X	X			SUSON
DDR Termination voltage	X	X			SUSON
CPU CORE	X				VR ON
+0.8V	X				MAINON
+VCCP	X				MAINON
+1.8V	X				MAINON
+1.8V	X				MAINON
+2.5V	X				MAINON
+3V	X				MAINON
+5V	X				MAINON
+12V	X				MAINON

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus+1394	AD17	1	PIROD/C
Mini-PCI	AD19	2	PIROB/D
10/100M LAN	AD23	3	PIROB

EC SM Bus1 address

Device
Smart Battery
THERMAL SENSOR

ICH6-M SM Bus address

Device
SODIMM 1010 000X b
Clock Gen 1101 001x b

The region below of Clock Gen. need to place ground plane

Place these termination to close CK410M.

The Crystal must be 20PF =>
Close to IC chip

CLK_EN- use to invert VCCP ok
Must be the same length
at two targets(48MHz) =>

The region below of Clock Gen. need to place ground plane

12/07 PCI_LAN OFF

Iref=5mA,
Ioh=4*Iref

300mA (MAX.)

If power-up w/ V>2.0V
will enter to test
mode FSC , FSB

DOTHAN -B
SR153, R371
POP, R488,
R368 DEPOP

PULL HIGH
TO SET
PIN35,36
TO HOST
CLK

PULL LOW
TO SET
PIN17,18
TO 96M_SS
CLK

Place these termination to close
CK410M.(ICS954201/ICS954206)

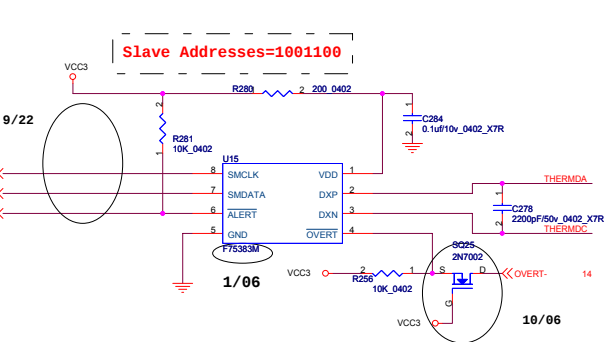
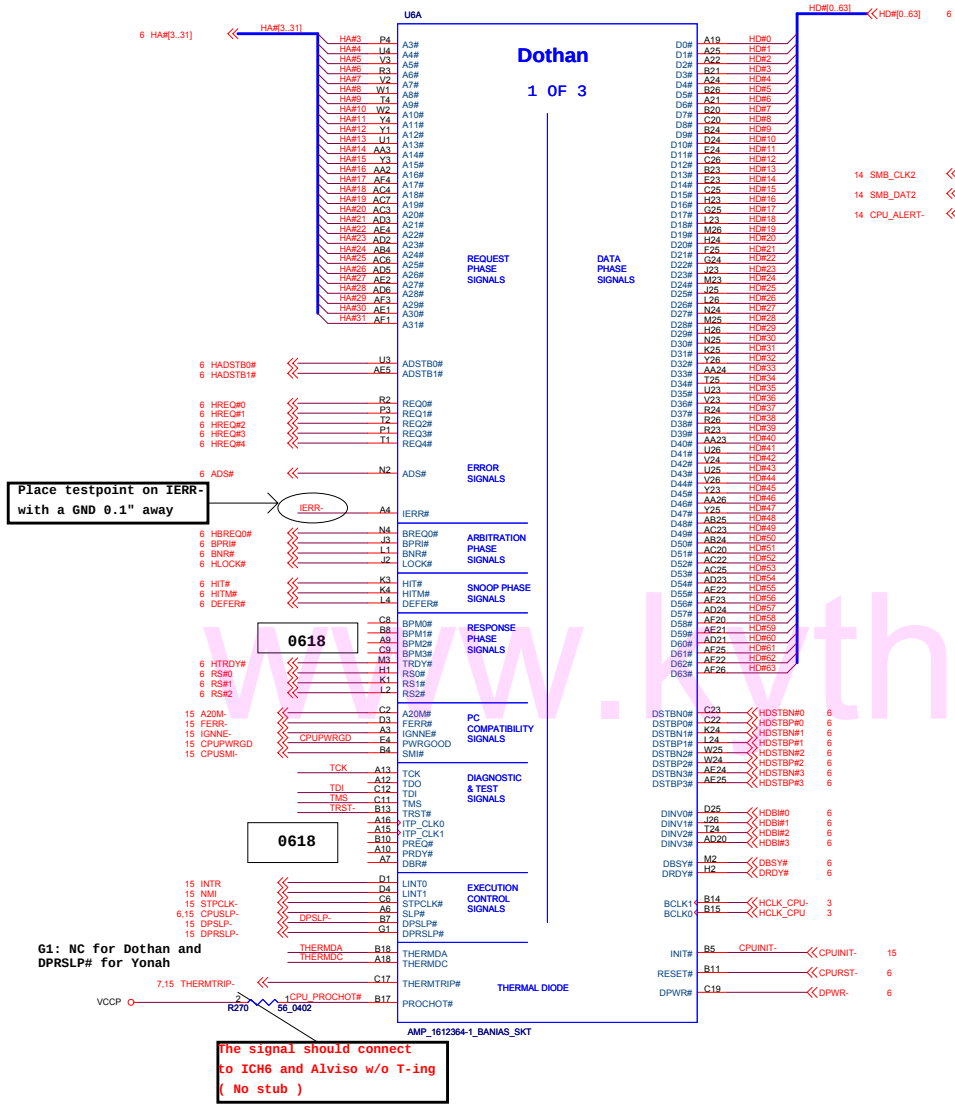
CHECK
16 PDAT_SMB << D S >> CGDAT_SMB 10

CHECK
16 PCLK_SMB << D S >> CGCLK_SMB 10

These are for backdrive issue

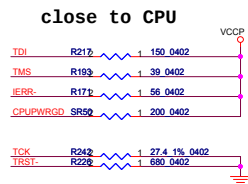
Voltage level shifter
SB(Vcc3_Sus)<->C.G. (Vcc3)

FSC	FSB	FSA	CPU	SRC	PCI	REF	
0	0	0	266	100	33	14.318	
0	0	1	133	100	33	14.318	DOTHAN 533
0	1	0	200	100	33	14.318	
0	1	1	166	100	33	14.318	
1	0	0	333	100	33	14.318	
1	0	1	100	100	33	14.318	DOTHAN 480
1	1	0	400	100	33	14.318	
1	1	1	RSVD	100	33	14.318	



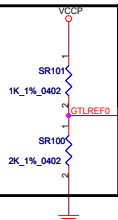
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TD0	Open	NC	Within 2.0" of the CPU

Del R682 because no ITP
Del R672 because no ITP

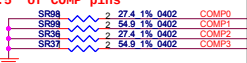


VCC_CORE
+VCCP
+1.8V

Place voltage
divider within
0.5" of GTLREF
pin

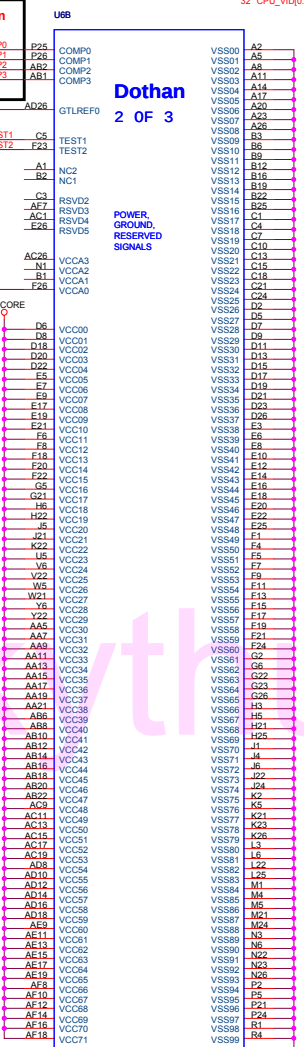


Place pulldown resistors within
0.5" of COMP pins



Dothan
2 OF 3

POWER,
GROUND,
RESERVED
SIGNALS



AMP_1612364_BANIAS_SKT

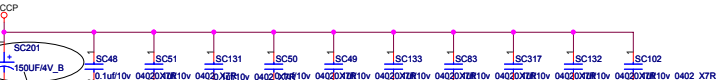
Dothan
3 OF 3

POWER, GROUND AND NC

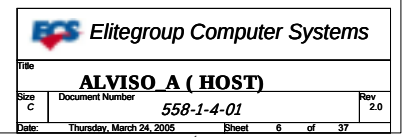
VID

DOOTHAN-A NC
DOOTHAN-B POP

Total caps = 2633 uF
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15



0628



MA_DAT0[7:0] 10,11

MADAT65..0

MADAT0	MADAT0 RP4407 33V4 0402 8	MA_DAT0
MADAT1	MADAT1 RP444C 33V4 0402 6	MA_DAT1
MADAT2	MADAT2 RP444A 33V4 0402 2	MA_DAT2
MADAT3	MADAT3 RP4481 33V4 0402 4	MA_DAT3
MADAT4		
MADAT5		
MADAT6		
MADAT7		
MADAT8	MADAT8 SRP128 33V4 0402 2	MA_DAT4
MADAT9	MADAT9 SRP128 33V4 0402 6	MA_DAT5
MADAT10	MADAT10 SRP128 33V4 0402 6	MA_DAT6
MADAT11	MADAT11 SRP128 33V4 0402 8	MA_DAT7
MADAT12		
MADAT13		
MADAT14	MADAT14 RP4007 33V4 0402 8	MA_DAT8
MADAT15	MADAT15 RP400C 33V4 0402 6	MA_DAT9
MADAT16	MADAT16 RP4081 33V4 0402 4	MA_DAT10
MADAT17	MADAT17 RP40A1 33V4 0402 2	MA_DAT11
MADAT18		
MADAT19		
MADAT20		
MADAT21	MADAT21 SRP138 33V4 0402 2	MA_DAT12
MADAT22	MADAT22 SRP138 33V4 0402 4	MA_DAT13
MADAT23	MADAT23 SRP138 33V4 0402 6	MA_DAT14
MADAT24	MADAT24 SRP138 33V4 0402 8	MA_DAT15
MADAT25		
MADAT26		
MADAT27		
MADAT28	MADAT28 RP390 33V4 0402 8	MA_DAT16
MADAT29	MADAT29 RP390 33V4 0402 6	MA_DAT17
MADAT30	MADAT30 RP398 33V4 0402 4	MA_DAT18
MADAT31	MADAT31 RP398 33V4 0402 2	MA_DAT19
MADAT32		
MADAT33		
MADAT34		
MADAT35	MADAT35 SRP11A 33V4 0402 2	MA_DAT20
MADAT36	MADAT36 SRP11B 33V4 0402 4	MA_DAT21
MADAT37	MADAT37 SRP11B 33V4 0402 6	MA_DAT22
MADAT38	MADAT38 SRP11B 33V4 0402 8	MA_DAT23
MADAT39		
MADAT40		
MADAT41	MADAT41 RP4307 33V4 0402 8	MA_DAT24
MADAT42	MADAT42 RP430C 33V4 0402 6	MA_DAT25
MADAT43	MADAT43 RP4381 33V4 0402 4	MA_DAT26
MADAT44	MADAT44 RP43A1 33V4 0402 2	MA_DAT27
MADAT45		
MADAT46		
MADAT47		
MADAT48		
MADAT49	MADAT49 SRP148 33V4 0402 2	MA_DAT28
MADAT50	MADAT50 SRP148 33V4 0402 4	MA_DAT29
MADAT51	MADAT51 SRP148 33V4 0402 6	MA_DAT30
MADAT52	MADAT52 SRP148 33V4 0402 8	MA_DAT31
MADAT53		
MADAT54		
MADAT55		
MADAT56		
MADAT57		
MADAT58		
MADAT59		
MADAT60		
MADAT61		
MADAT62		
MADAT63		
MADAT64		
MADAT65		

MADAT40	RP38C 33V4 0402 6	MA_DAT40
MADAT41	RP38C 33V4 0402 8	MA_DAT41
MADAT42	RP38C 33V4 0402 4	MA_DAT42
MADAT43	RP38C 33V4 0402 2	MA_DAT43
MADAT44		
MADAT45		

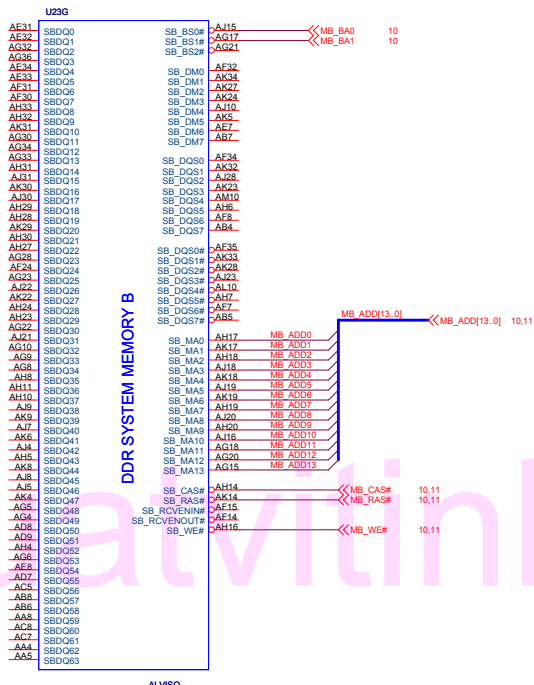
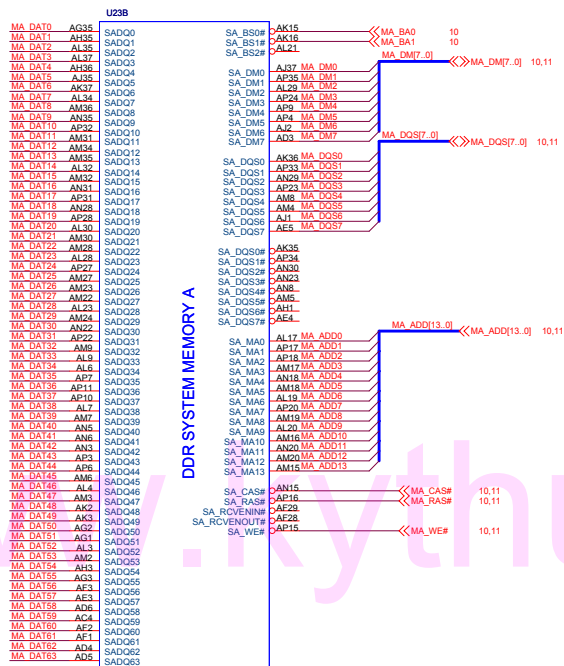
MADAT44	SRP8A 33V4 0402 2	MA_DAT44
MADAT45	SRP8B 33V4 0402 4	MA_DAT45
MADAT46	SRP8C 33V4 0402 6	MA_DAT46
MADAT47	SRP8D 33V4 0402 8	MA_DAT47
MADAT48		
MADAT49		

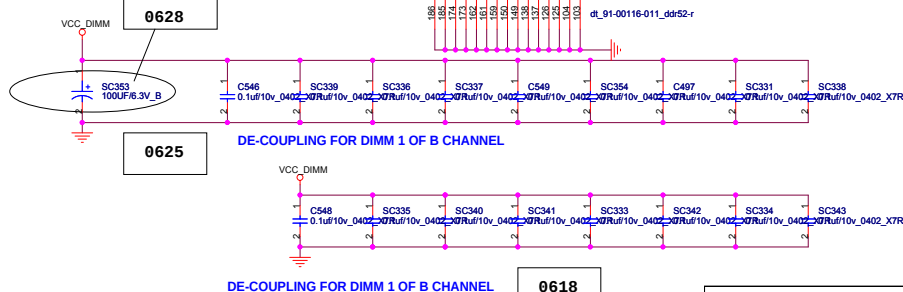
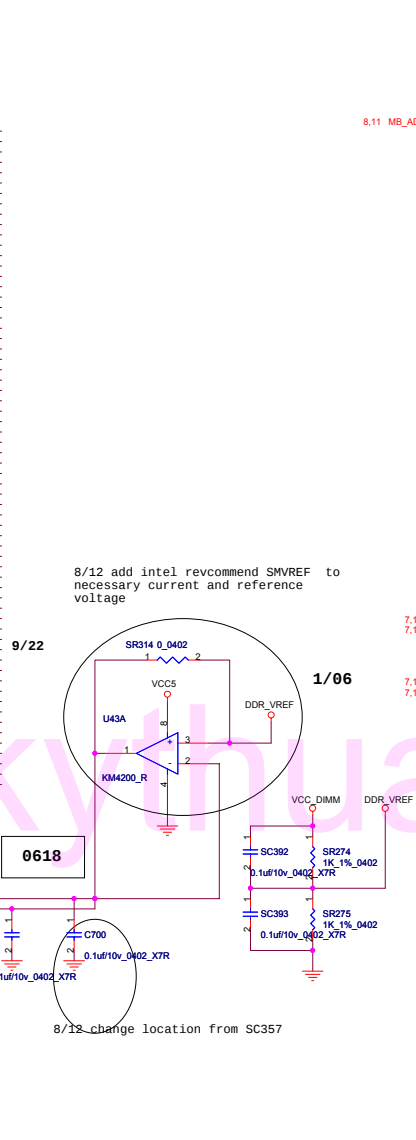
MADAT48	RP340 33V4 0402 8	MA_DAT48
MADAT49	RP340 33V4 0402 6	MA_DAT49
MADAT50	RP348 33V4 0402 4	MA_DAT50
MADAT51	RP34A 33V4 0402 2	MA_DAT51
MADAT52		
MADAT53		

MADAT52	SRP1A 33V4 0402 2	MA_DAT52
MADAT53	SRP1B 33V4 0402 4	MA_DAT53
MADAT54	SRP1C 33V4 0402 6	MA_DAT54
MADAT55	SRP1D 33V4 0402 8	MA_DAT55
MADAT56		
MADAT57		

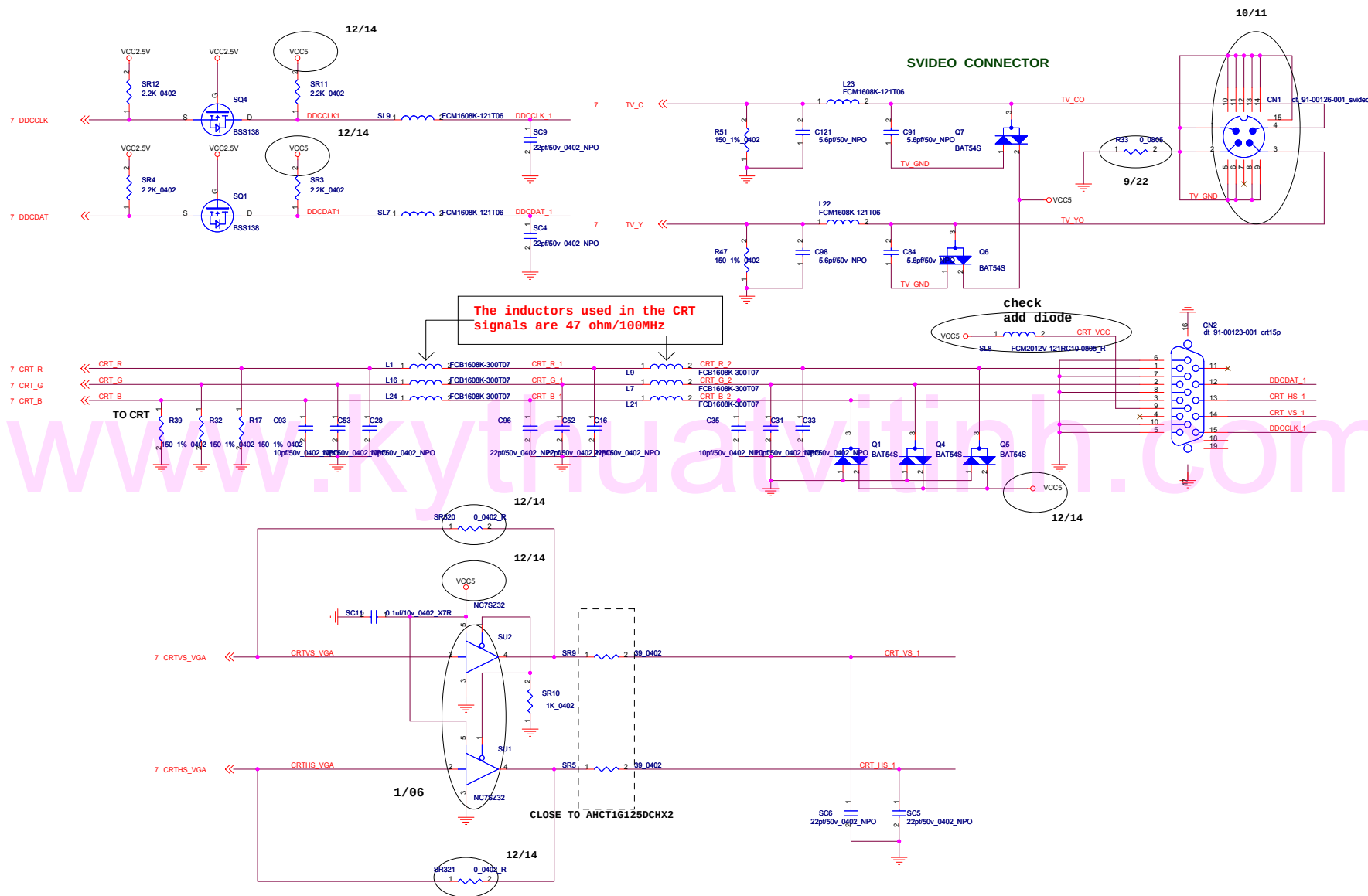
MADAT56	RP320 33V4 0402 8	MA_DAT56
MADAT57	RP320 33V4 0402 6	MA_DAT57
MADAT58	RP320 33V4 0402 4	MA_DAT58
MADAT59	RP32A 33V4 0402 2	MA_DAT59
MADAT60		
MADAT61		

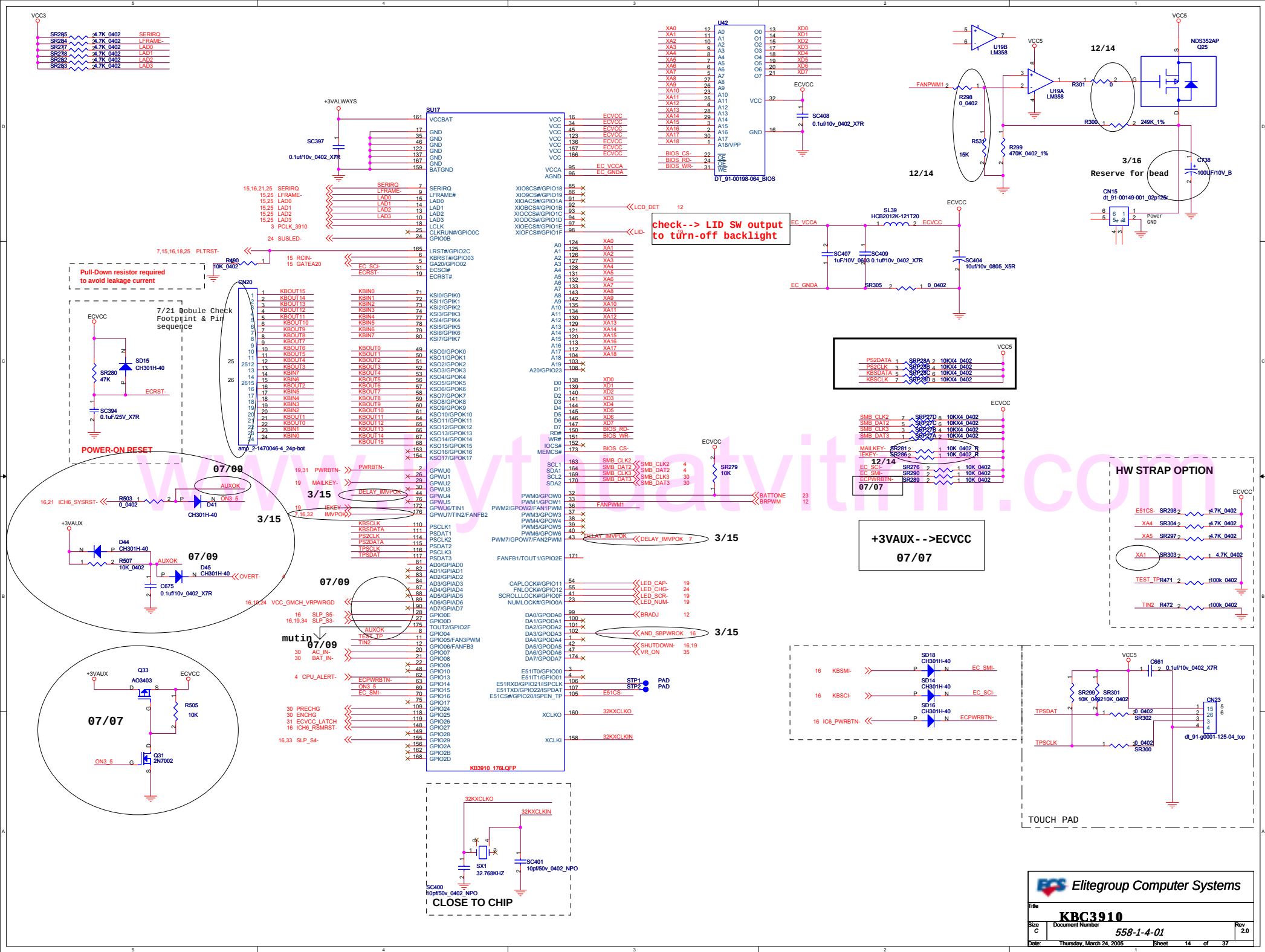
MADAT60	SRP10B 33V4 0402 2	MA_DAT60
MADAT61	SRP10B 33V4 0402 4	MA_DAT61
MADAT62	SRP10B 33V4 0402 6	MA_DAT62
MADAT63	SRP10B 33V4 0402 8	MA_DAT63
MADAT64		
MADAT65		

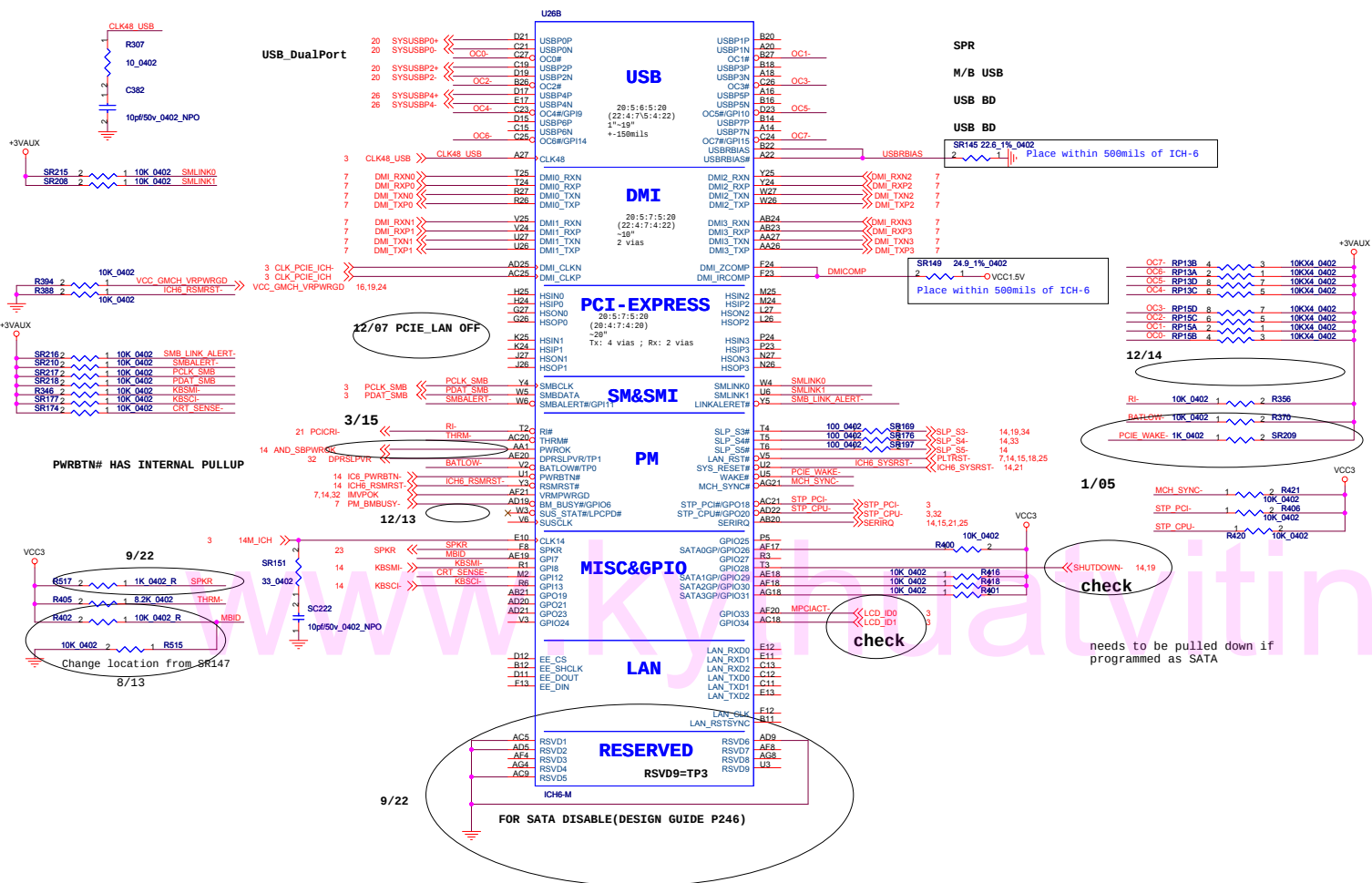




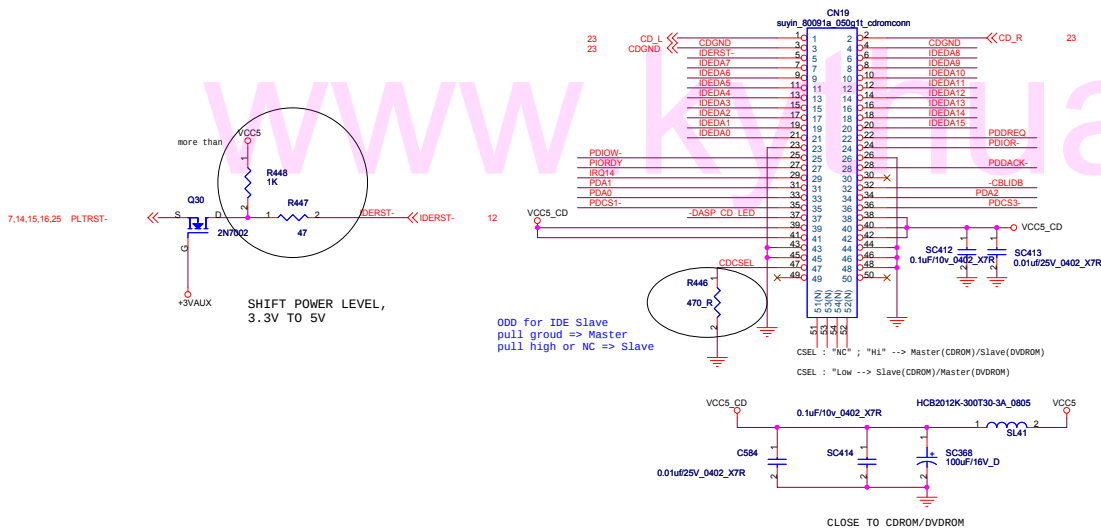
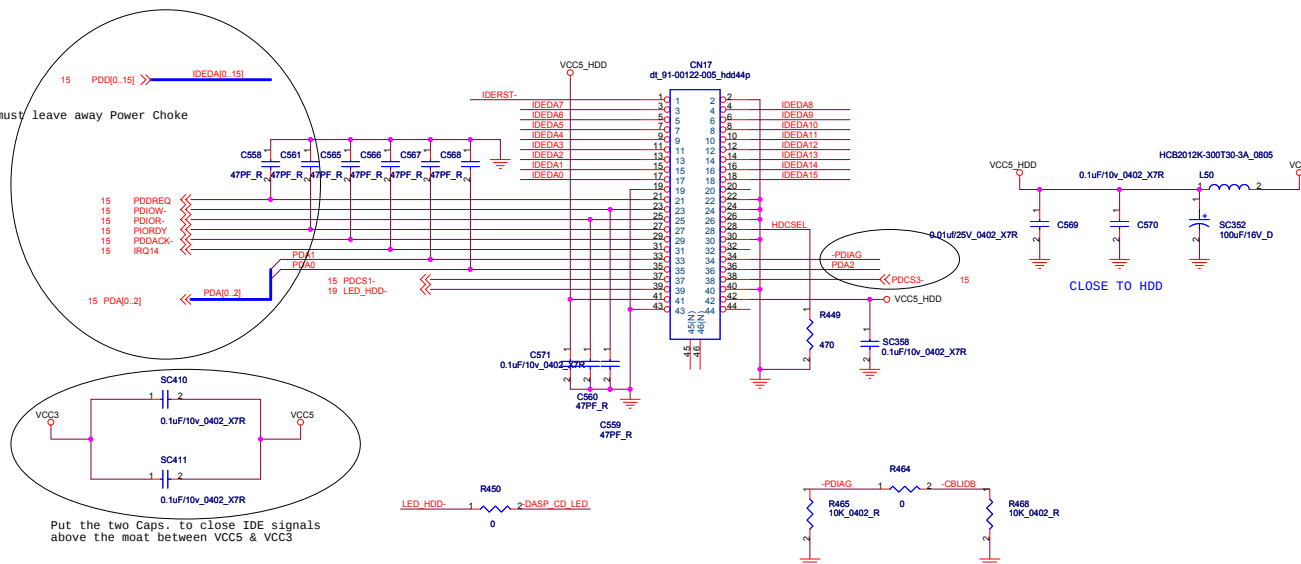


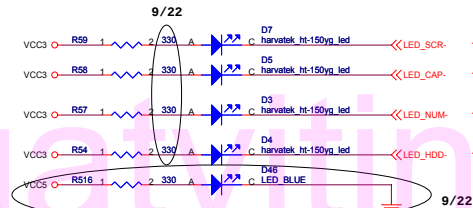
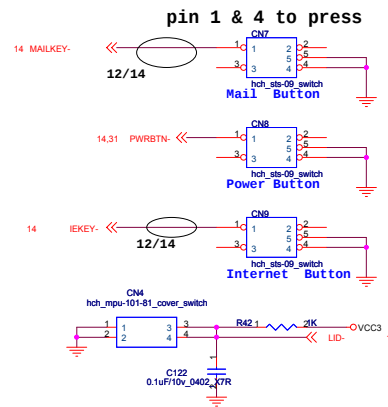
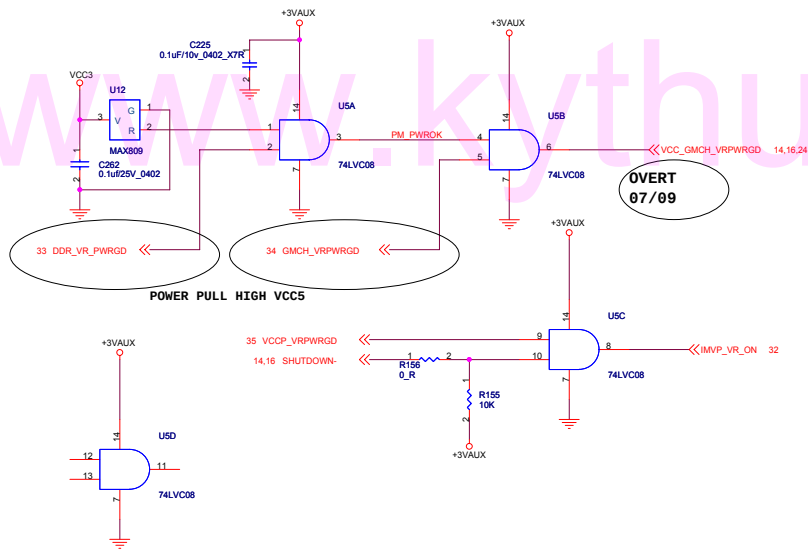
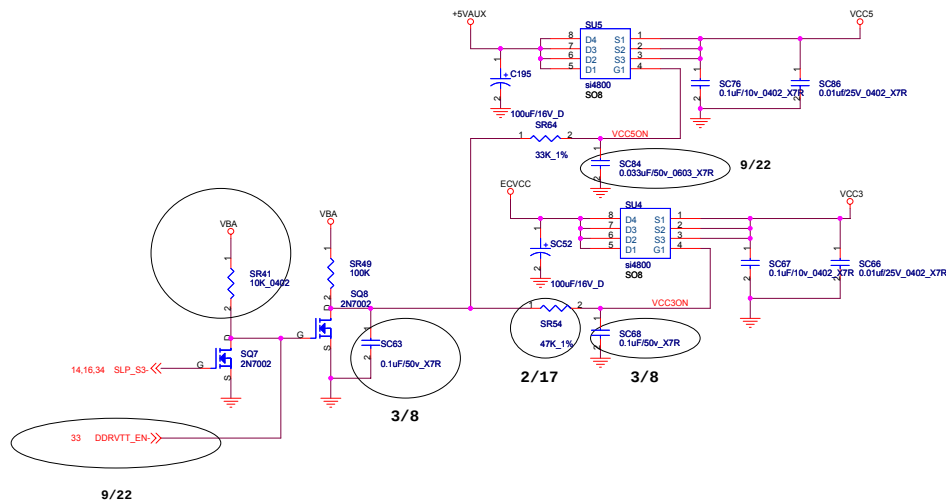






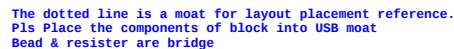
IDE signals must leave away Power Choke



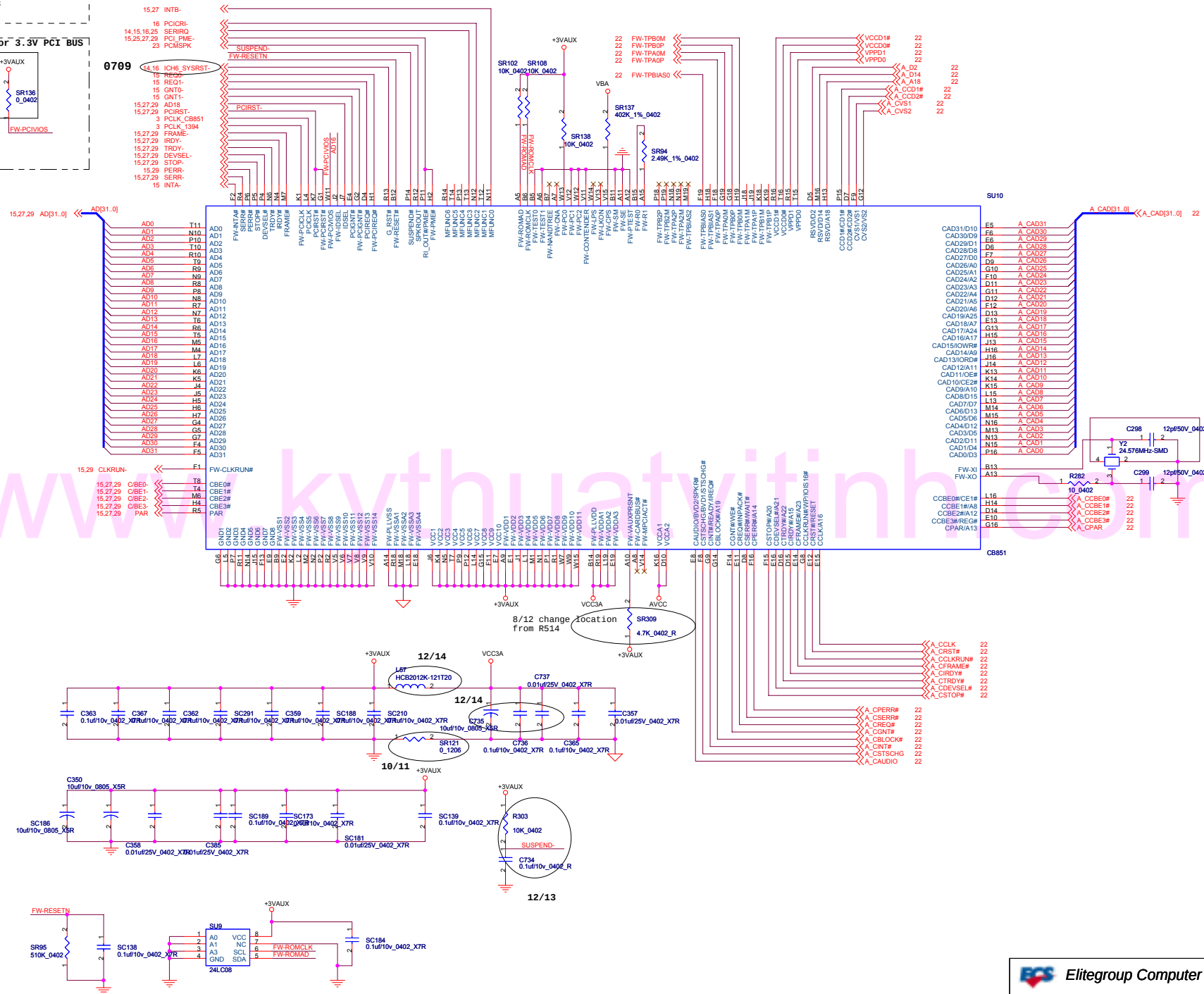


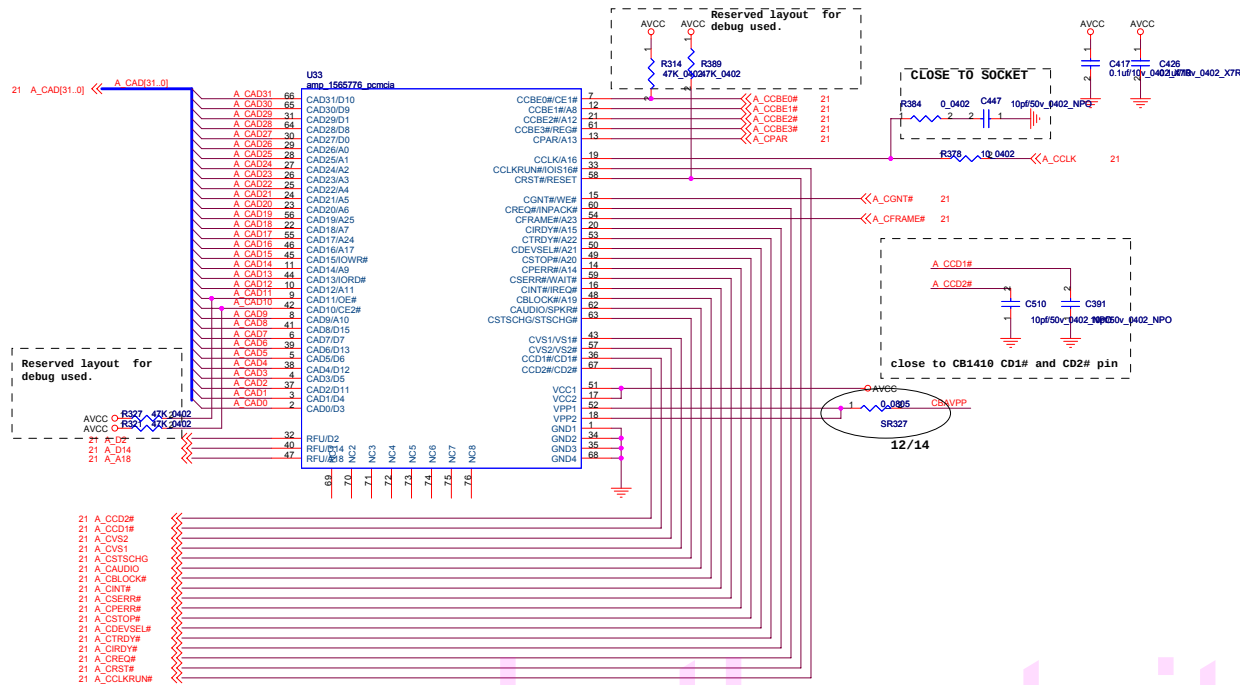
8/26 change F1 P/N: from
16-285-150370 to
16-200-150010

9/22

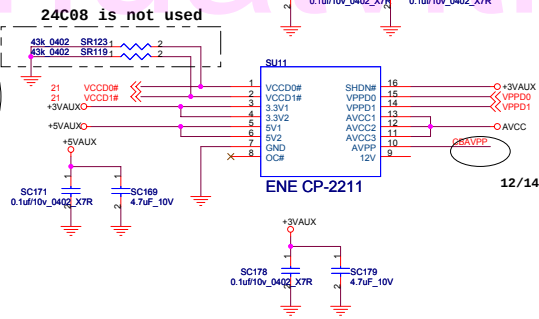
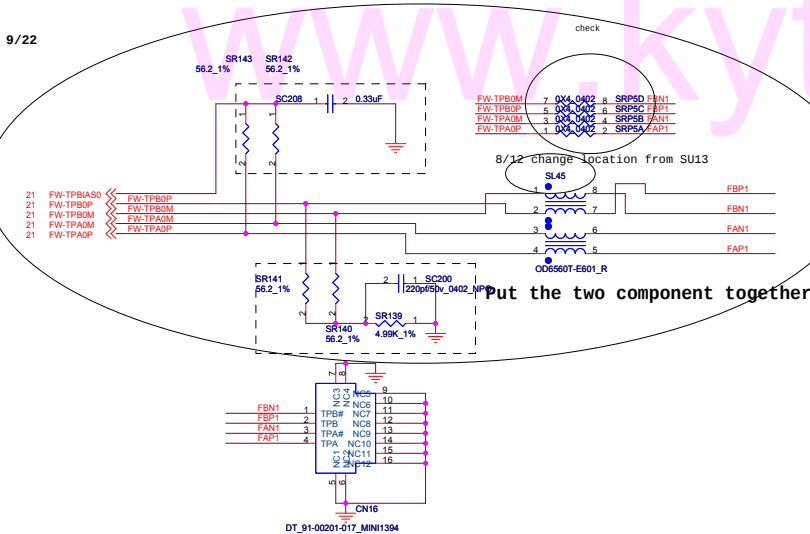


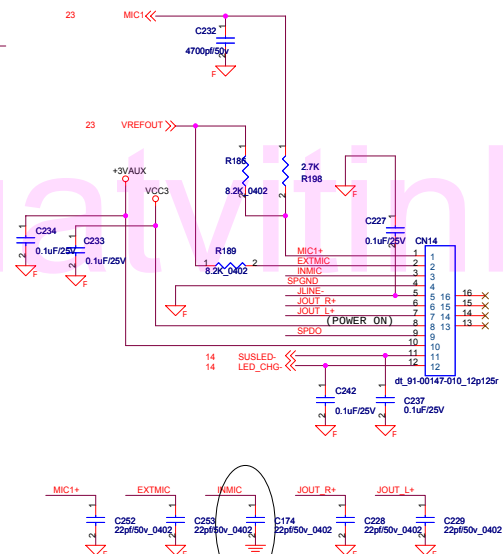
Use Plane to connecting & Rounting
(USB_GND1 <=> GND)



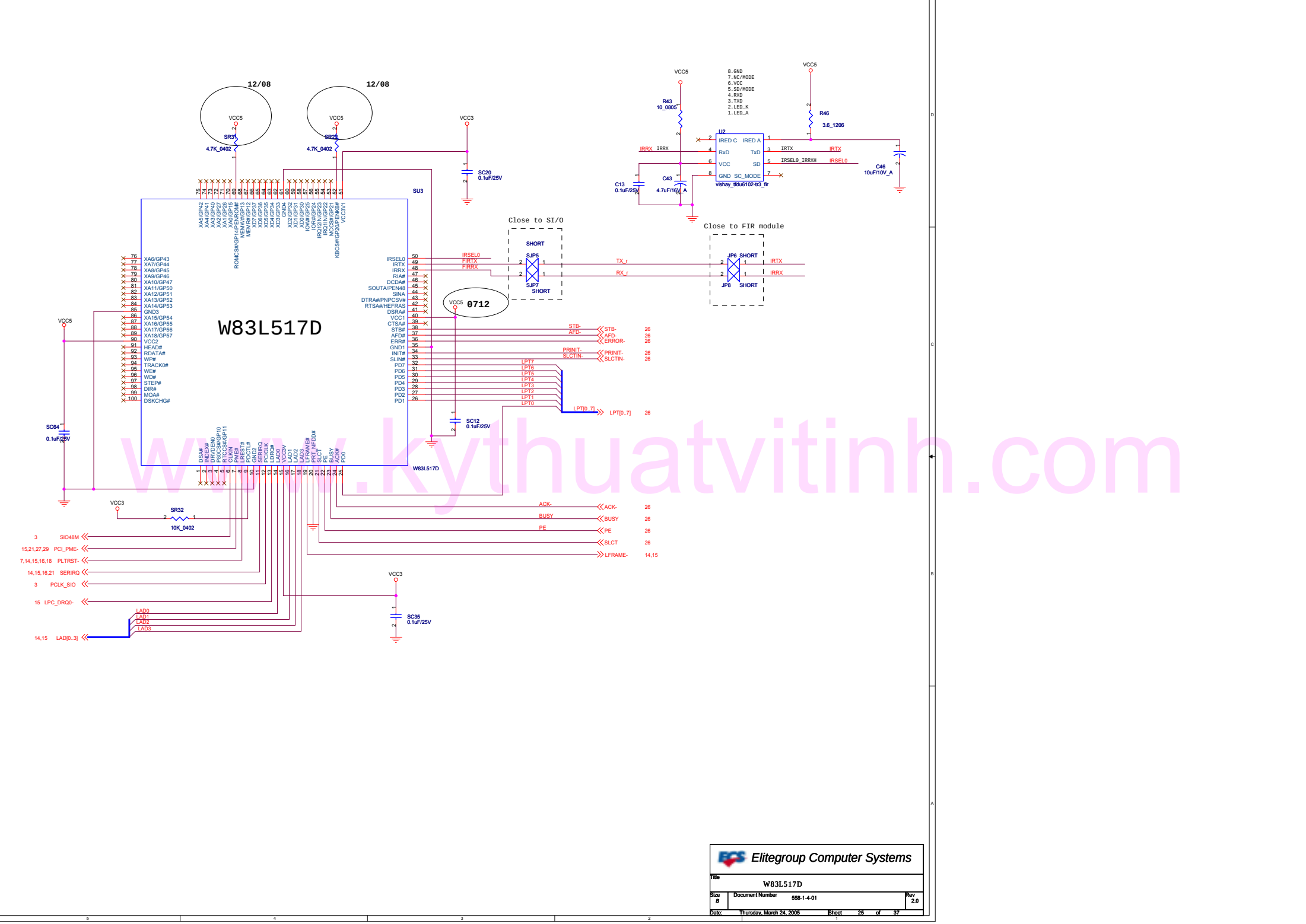


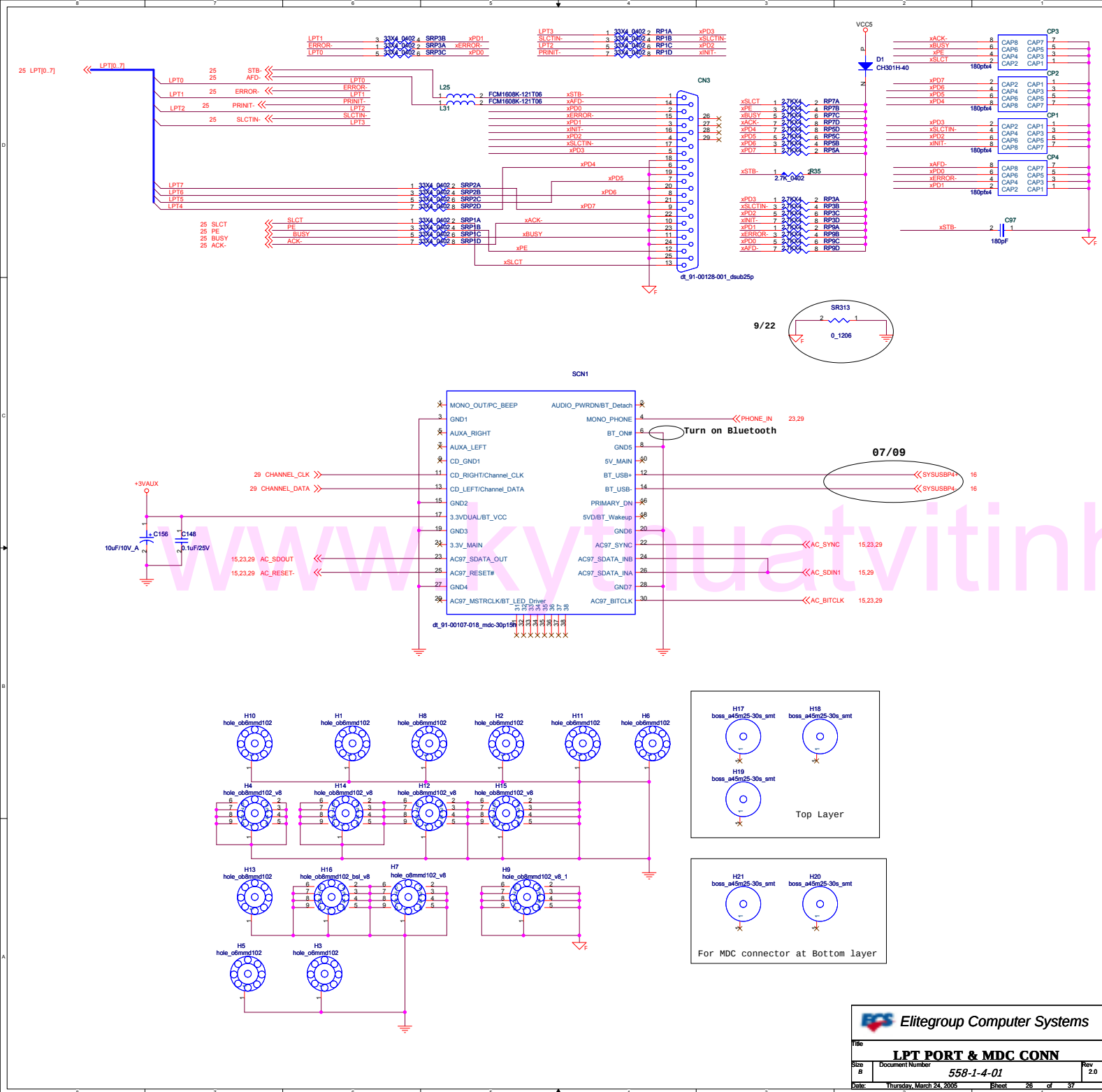
9/22

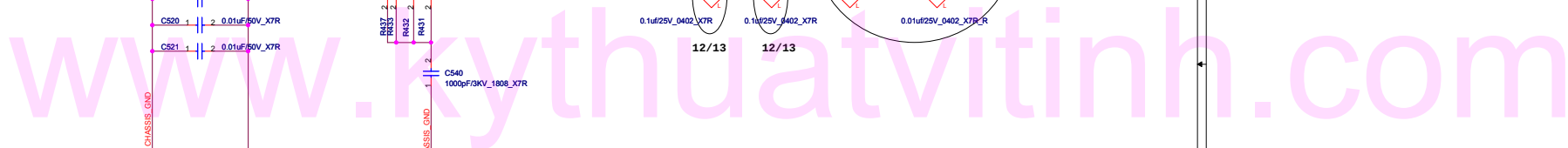




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File			
OPA & AUDIO JACK			
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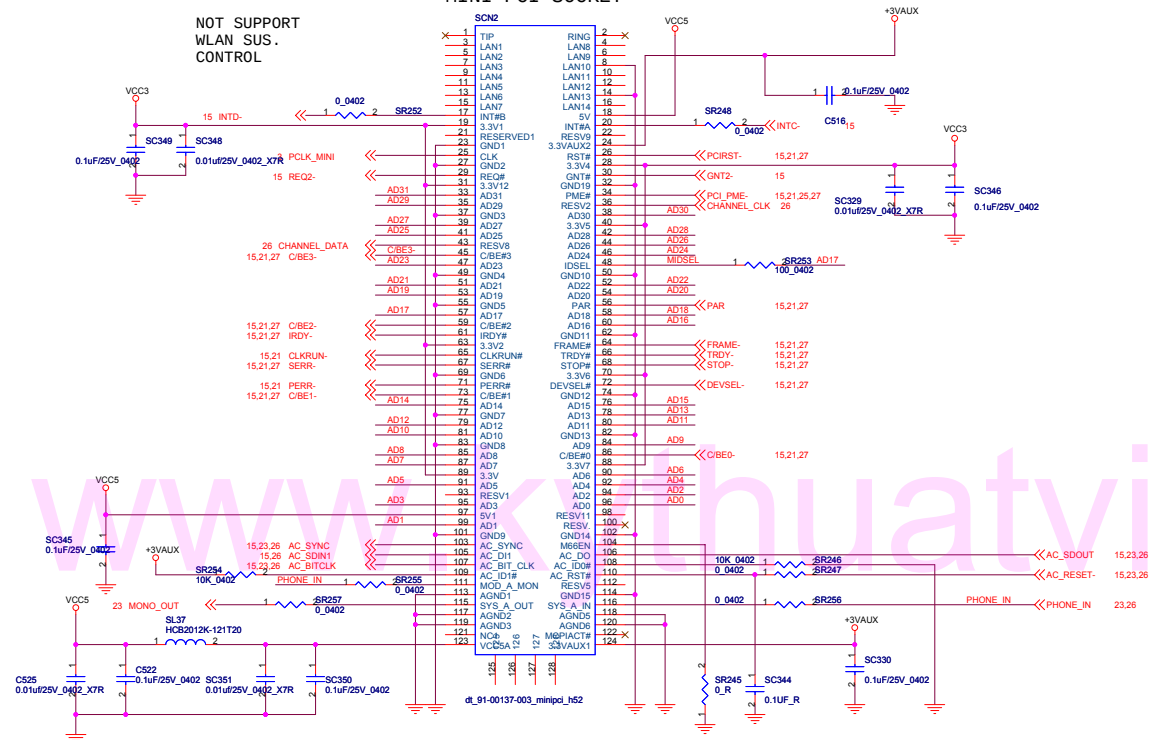


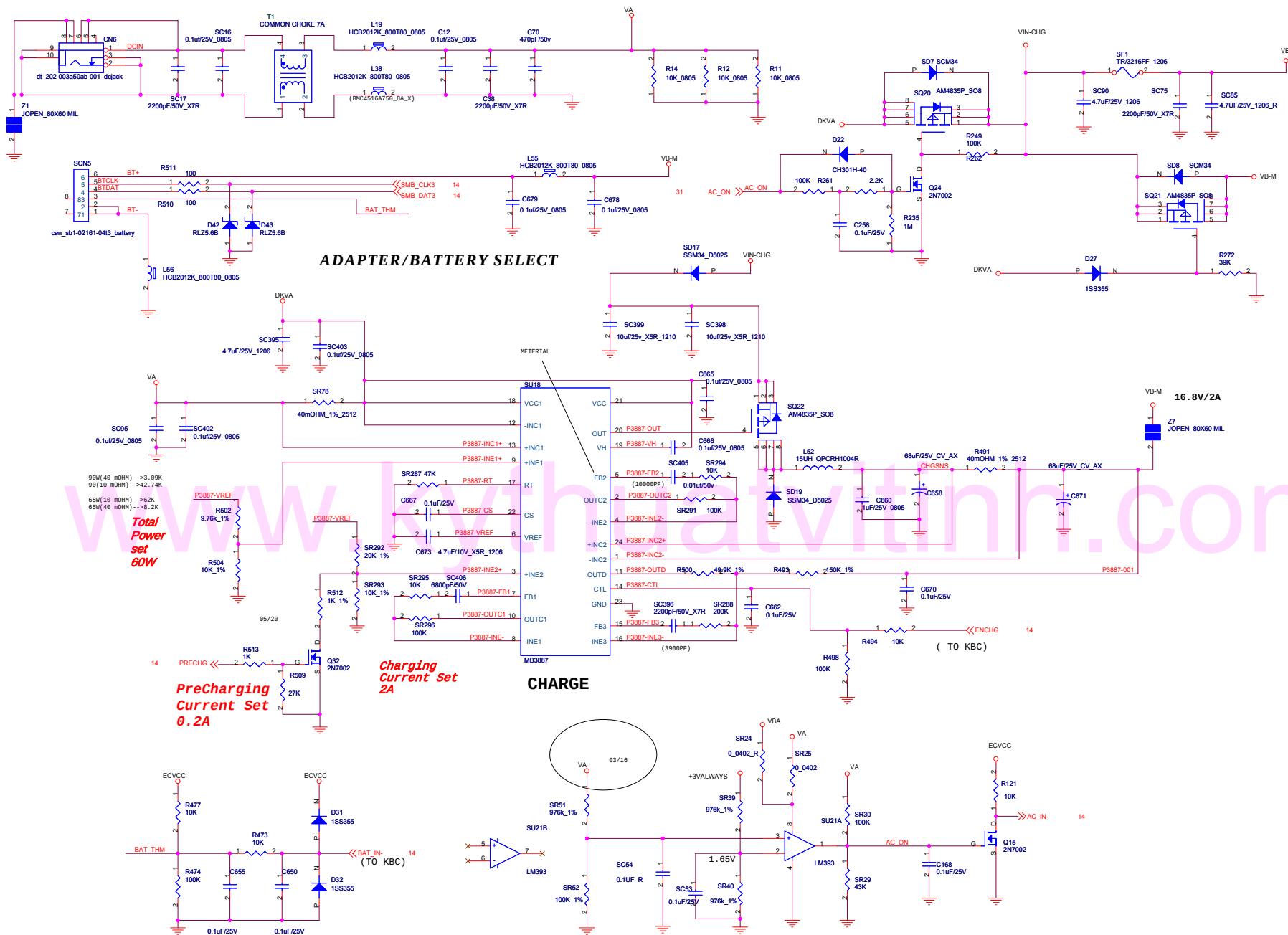
15,21,27 AD[0..31]

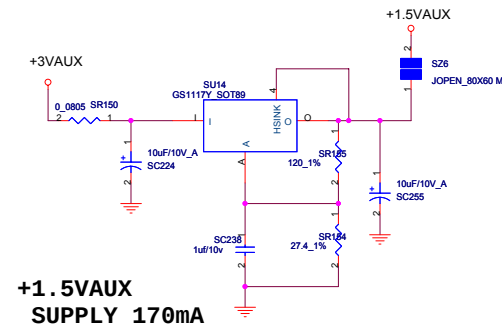
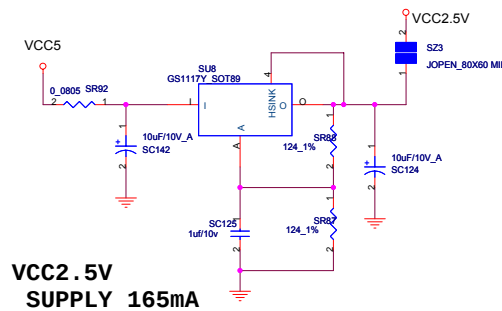
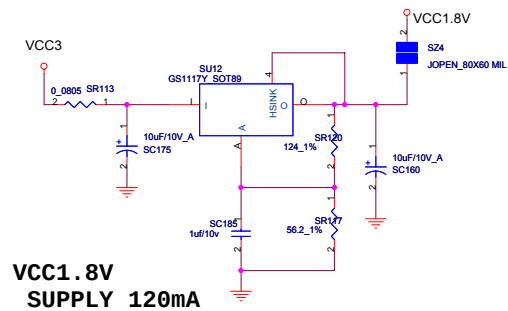
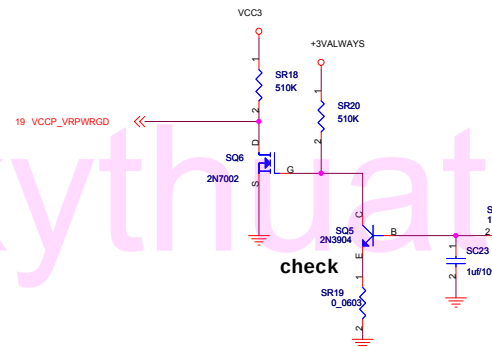
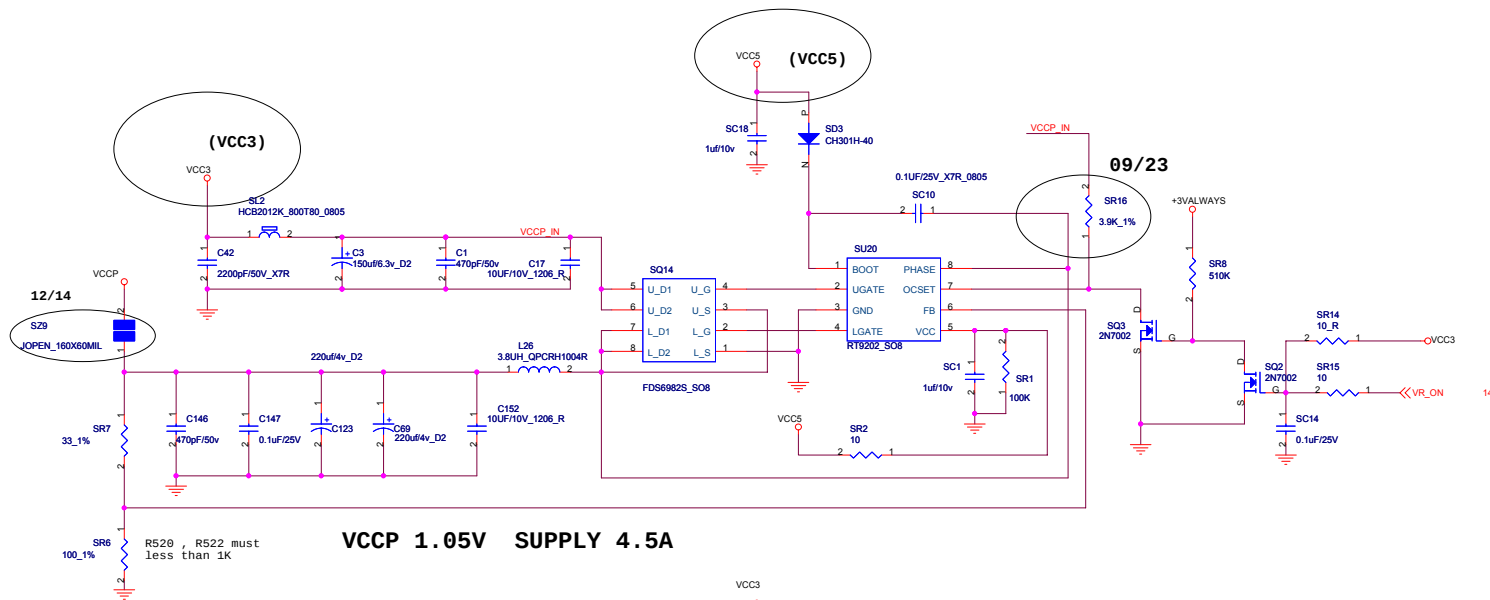
AD[0..31]

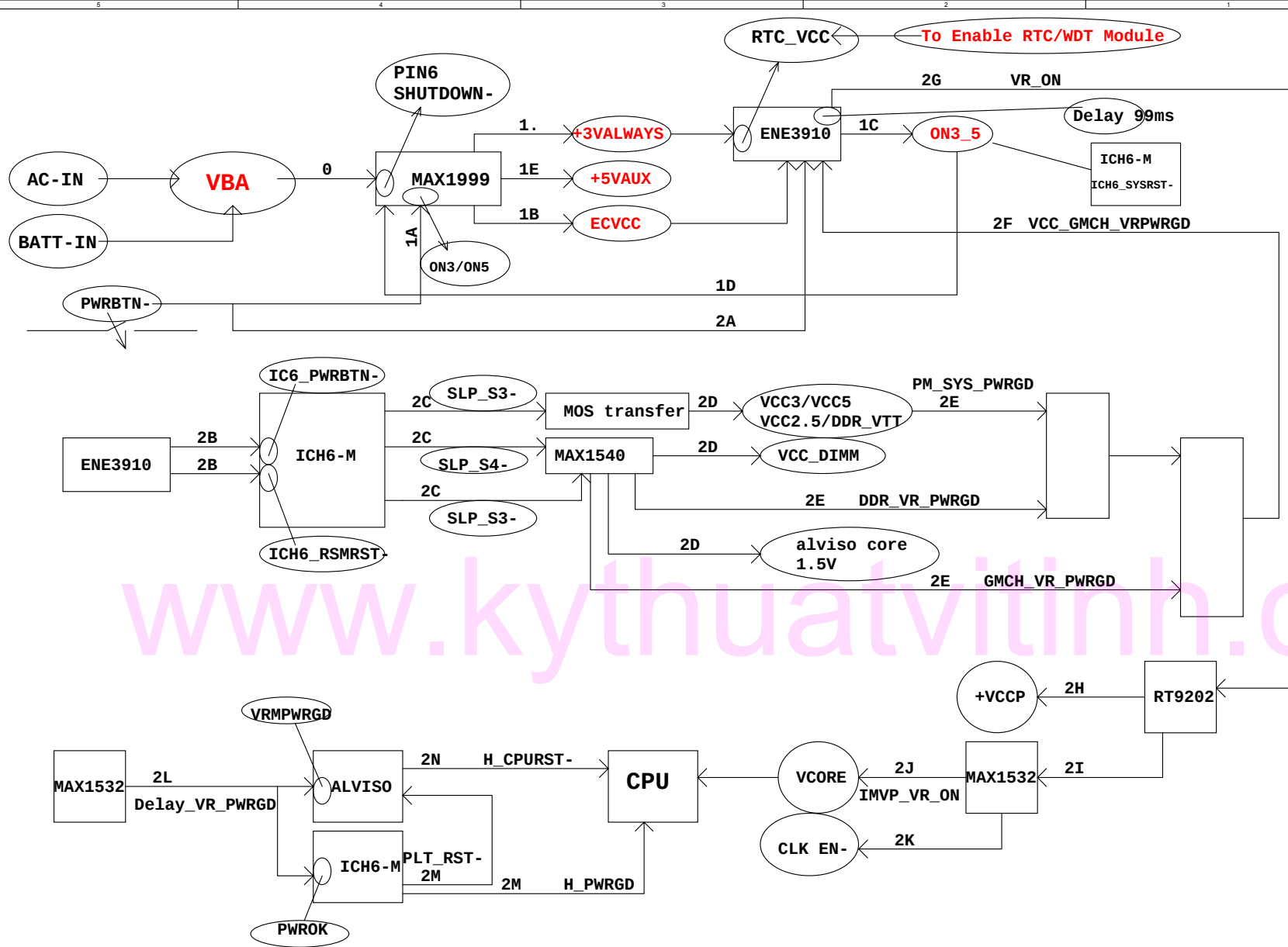
NOT SUPPORT
WLAN SUS.
CONTROL

MINI PCI SOCKET









V.A: Initial Release 2004/08/09	15-F55-010010
V.B: Initial Release 2004/10/13	15-F55-010020
V.C: Initial Release 2004/12/20	15-F55-010030
V.D: Initial Release 2005/01/06	15-F55-010040
V.1.0: Initial Release 2005/02/17	15-F55-011000
V.2.0: Initial Release 2005/03/21	15-F55-012000

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History		
Title		
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