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31	PCI (MS-DUO/MDC)						
32	PCI (PCMCIA)						
33	USB2.0						
34	LAN (1/2)						
35	LAN (2/2)						

PCB P/N: 1P-0075503-6010
1P-0075103-6010

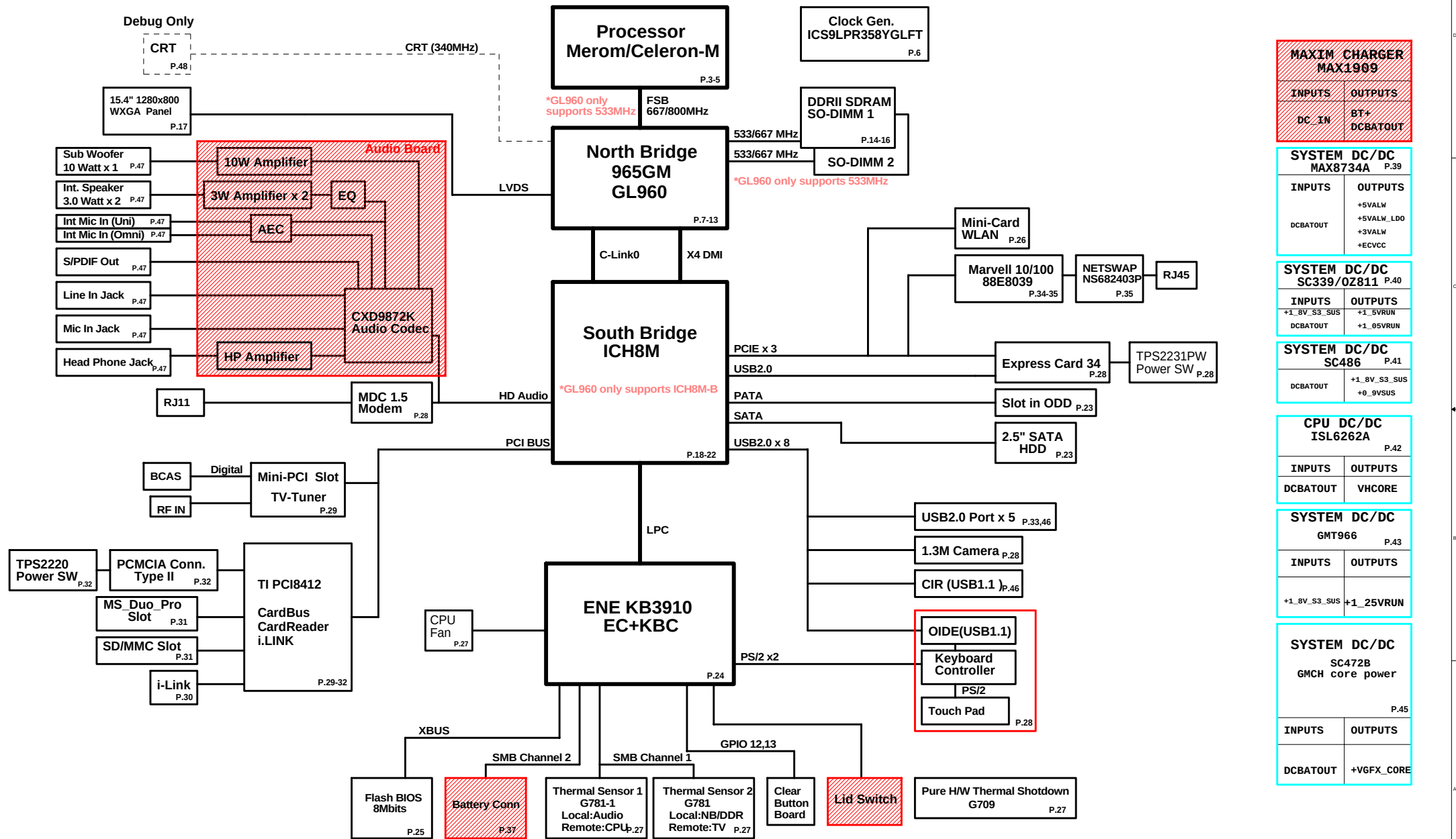
Project Code & Schematics Subject: M620 Main Board

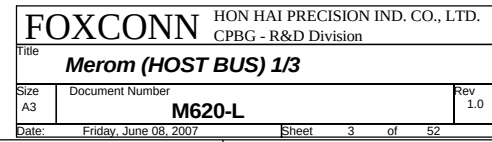
Value	M620GM	M620GML
NC_		

P. Leader	Check by	Design by

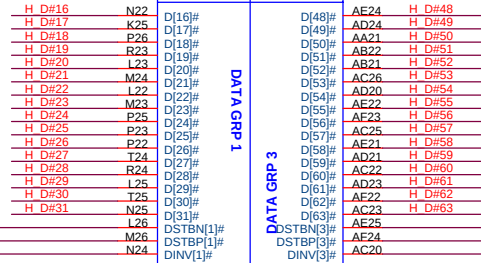
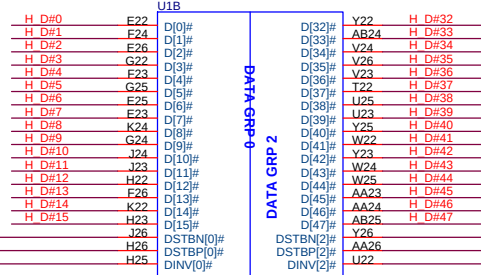
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
Index Page			
Size	Document Number	Rev	
Custom	M620-L	1.0	
Date:	Friday, June 08, 2007	Sheet	1 of 52

MBX-178 M620 Block Diagram (15.4" Wide Screen)

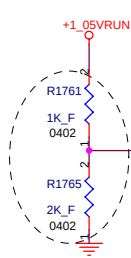




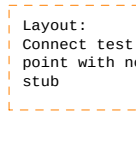
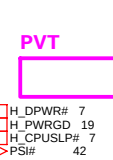
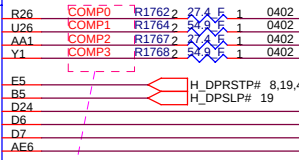
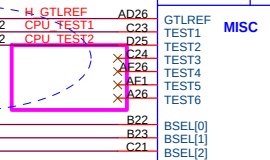
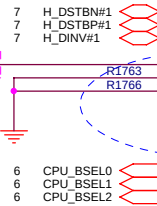
7 H_D#[63..0]



Place close to CPU



Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

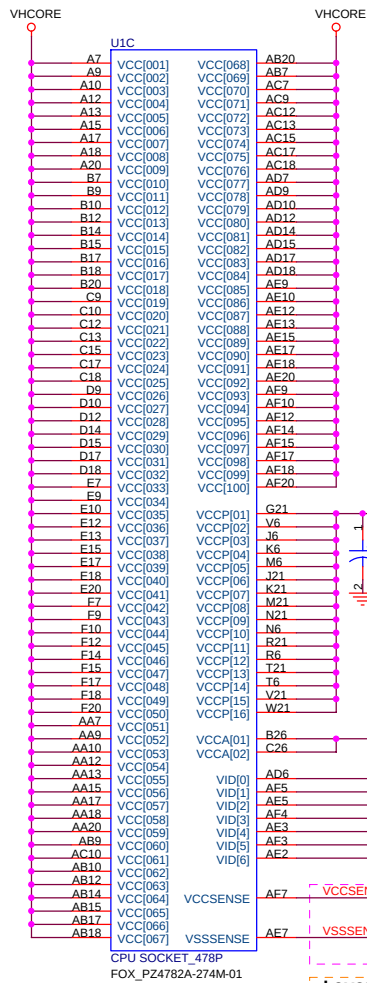
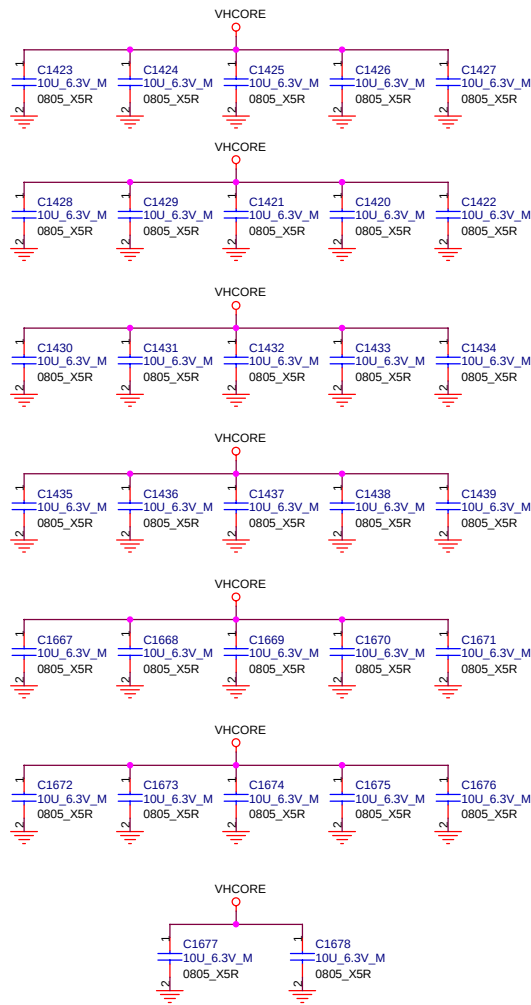


FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
LLL	266MHz
LLH	133MHz
LHH	166MHz
LHL	200MHz
HHL	400MHz
HHH	Reserve
HLL	100MHz
LLL	333MHz

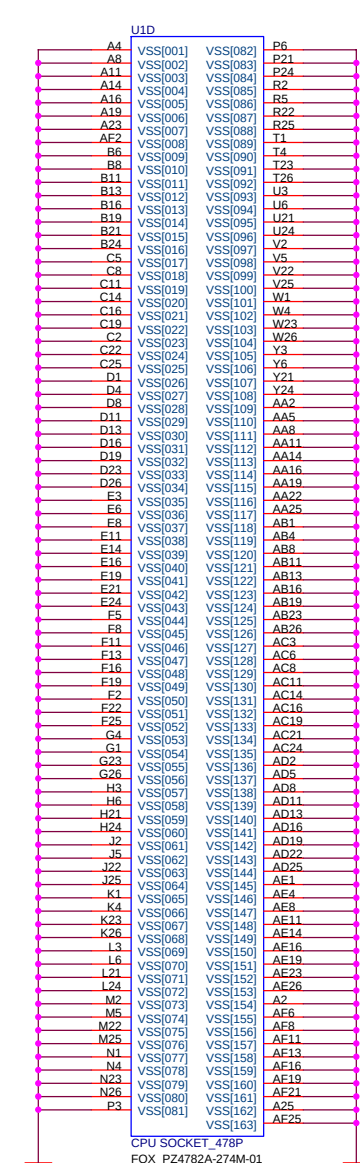
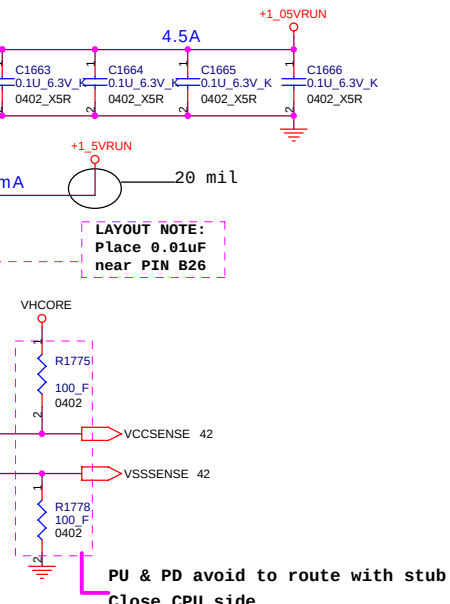
Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make
trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make
trace length shorter then 0.5".

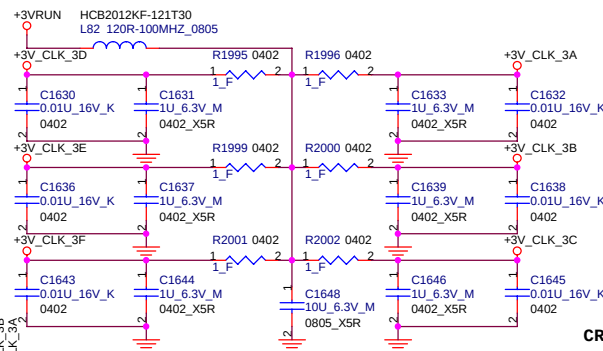
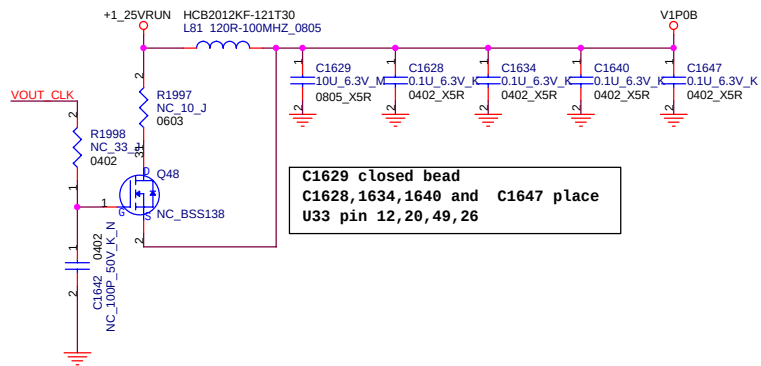
IMVP6 (ISL6262ACRZ-T)
cpu PSI# <-> ISL6262ACRZ-T PSI#
ISL6262ACRZ-T: VIHmin=0.315V
VILmax=0.735V
(ref. IMVP-6 NO:18904)



CPU_VCCA---->120mA
CPU_VCCP----->4.5A
CPU_VCC----->44A

Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of CPU.
width=18 mil
spacing=7 mil





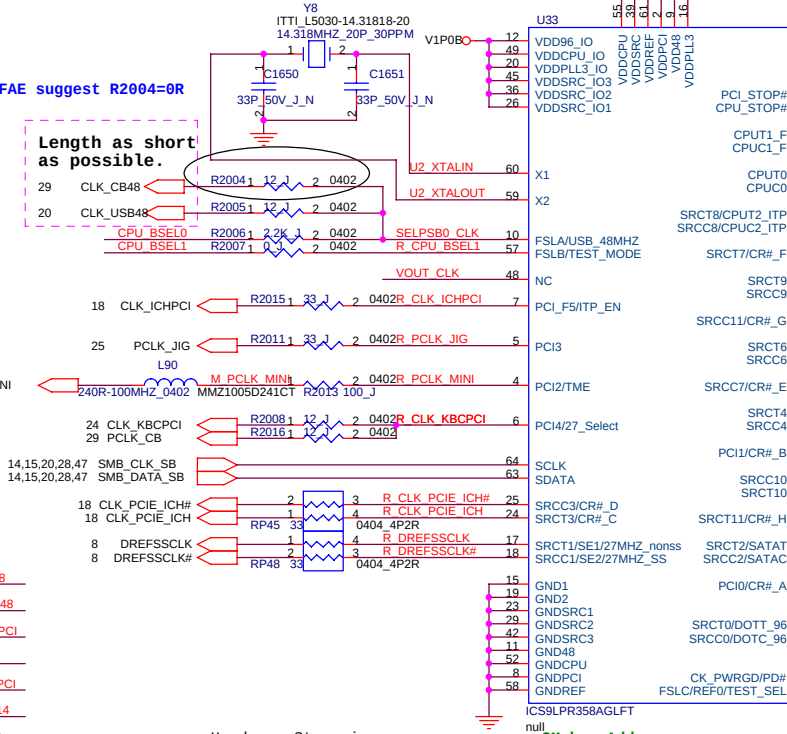
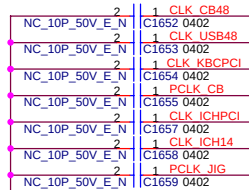
CR#_E/F/G/H pins control SRC output Table

CR#_E:Byte6:bit7=0, disable CR#_E; 1, enable CR#_E SRC6
 CR#_F:Byte6:bit6=0, disable CR#_F; 1, enable CR#_F SRC8
 CR#_G:Byte6:bit5=0, disable CR#_G; 1, enable CR#_G SRC9
 CR#_H:Byte6:bit4=0, disable CR#_H; 1, enable CR#_H SRC10

FAE suggest R2004=0R

Length as short as possible.

dual mode of PCI clock (pin3,4,6,7) should link to on-board device.



Hardware Strapping

SM bus Address : 1101001x(HEX:D2) (ICH8M)
 For clock generator

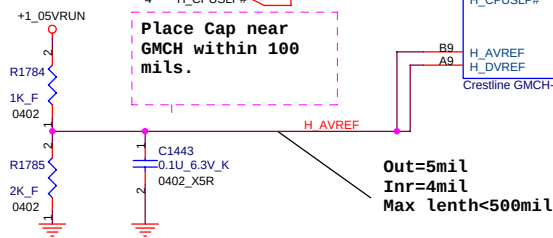
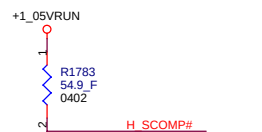
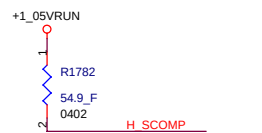
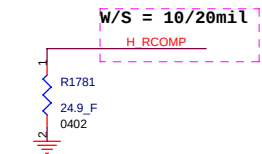
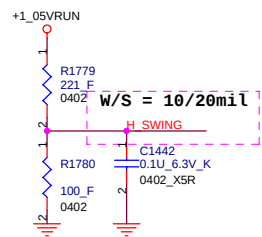
close to clk gen (For EMI)

FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

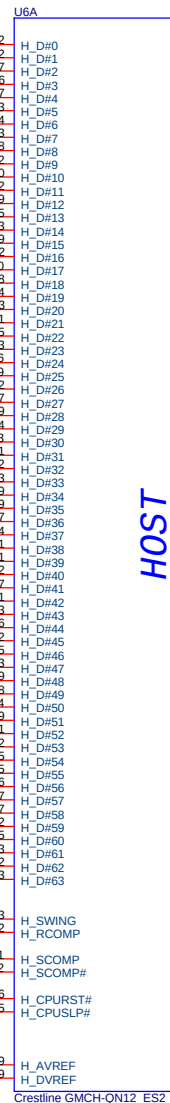
DVT

FAE suggest R2495=0R



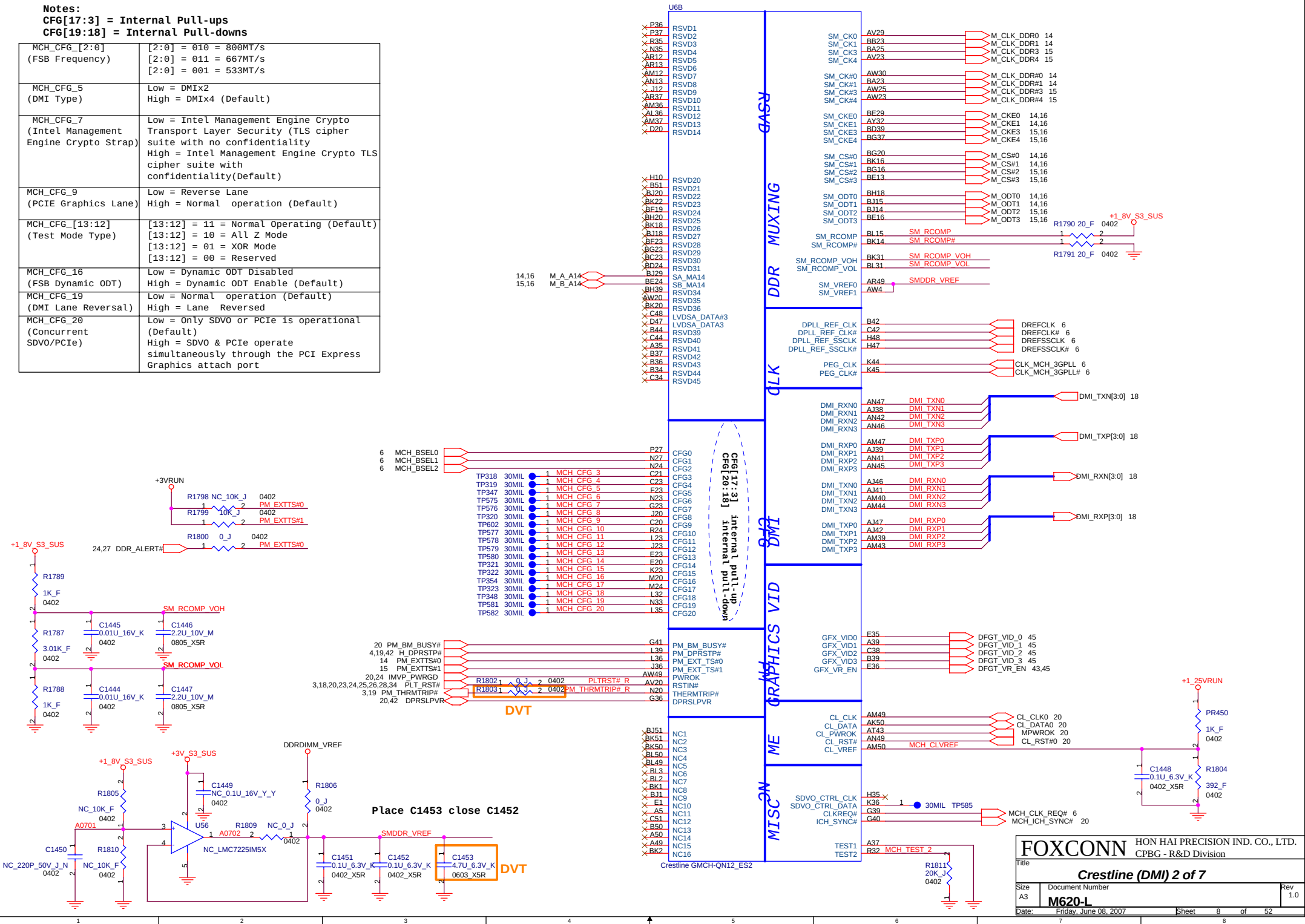
H_D#0	E2	H_D#0
H_D#1	G2	H_D#1
H_D#2	G7	H_D#2
H_D#3	M6	H_D#3
H_D#4	H7	H_D#4
H_D#5	H3	H_D#5
H_D#6	G4	H_D#6
H_D#7	F3	H_D#7
H_D#8	N8	H_D#8
H_D#9	H2	H_D#9
H_D#10	M10	H_D#10
H_D#11	N12	H_D#11
H_D#12	N9	H_D#12
H_D#13	H5	H_D#13
H_D#14	P13	H_D#14
H_D#15	K9	H_D#15
H_D#16	M2	H_D#16
H_D#17	W10	H_D#17
H_D#18	Y8	H_D#18
H_D#19	V4	H_D#19
H_D#20	M3	H_D#20
H_D#21	J11	H_D#21
H_D#22	N5	H_D#22
H_D#23	N3	H_D#23
H_D#24	W6	H_D#24
H_D#25	W9	H_D#25
H_D#26	N2	H_D#26
H_D#27	Y7	H_D#27
H_D#28	Y9	H_D#28
H_D#29	P4	H_D#29
H_D#30	W3	H_D#30
H_D#31	N1	H_D#31
H_D#32	AD12	H_D#32
H_D#33	AE3	H_D#33
H_D#34	AD9	H_D#34
H_D#35	AC9	H_D#35
H_D#36	AC7	H_D#36
H_D#37	AC14	H_D#37
H_D#38	AD11	H_D#38
H_D#39	AC11	H_D#39
H_D#40	AB2	H_D#40
H_D#41	AD7	H_D#41
H_D#42	AB1	H_D#42
H_D#43	Y3	H_D#43
H_D#44	AC6	H_D#44
H_D#45	AE2	H_D#45
H_D#46	AC5	H_D#46
H_D#47	AG3	H_D#47
H_D#48	AJ9	H_D#48
H_D#49	AH8	H_D#49
H_D#50	AJ14	H_D#50
H_D#51	AE9	H_D#51
H_D#52	AE11	H_D#52
H_D#53	AH12	H_D#53
H_D#54	AJ5	H_D#54
H_D#55	AH5	H_D#55
H_D#56	AJ6	H_D#56
H_D#57	AE7	H_D#57
H_D#58	AJ7	H_D#58
H_D#59	AJ2	H_D#59
H_D#60	AE5	H_D#60
H_D#61	AJ3	H_D#61
H_D#62	AH2	H_D#62
H_D#63	AH13	H_D#63

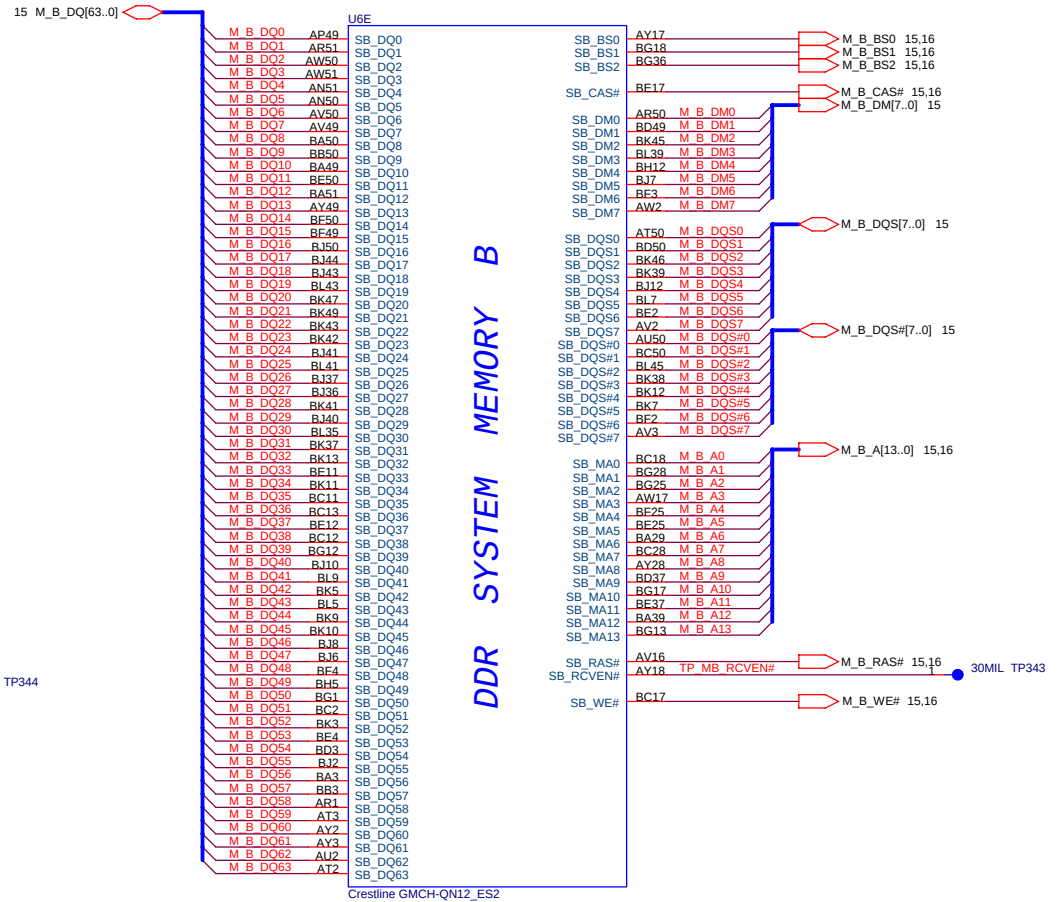
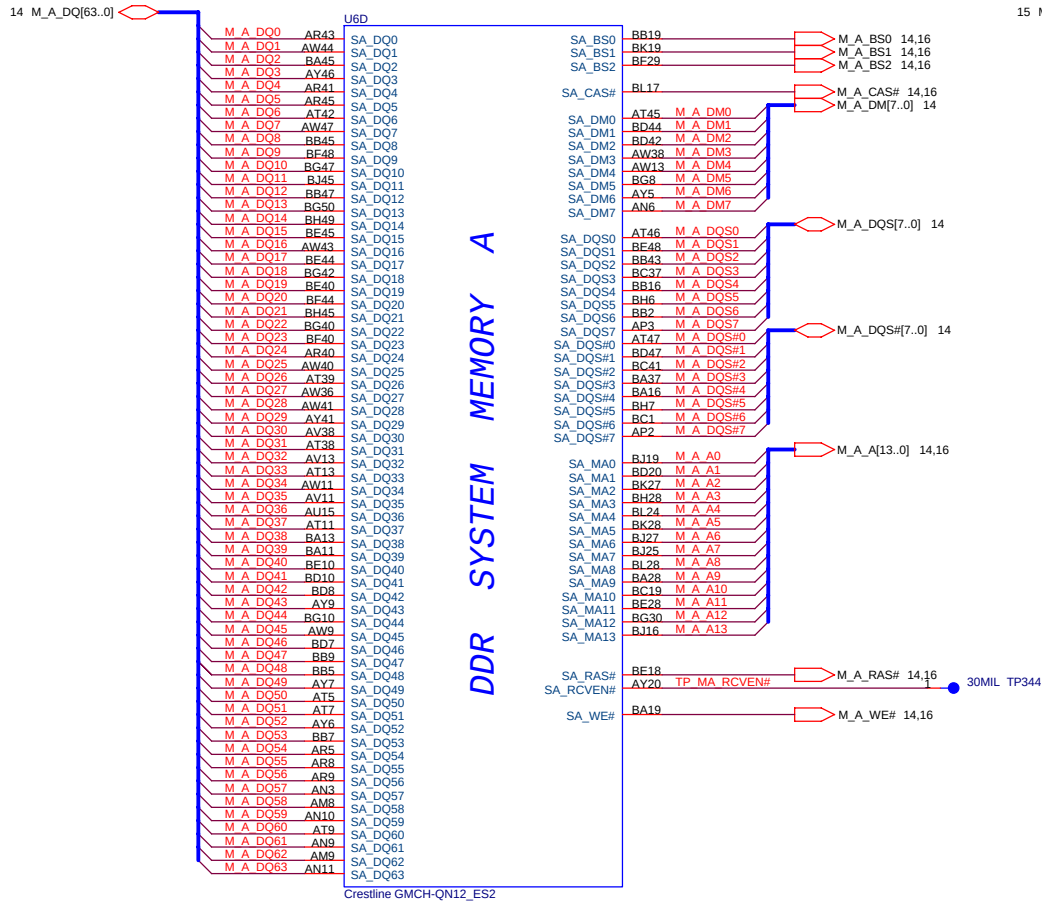
H_SWING	B3	H_SWING
H_RCOMP	C2	H_RCOMP
H_SCOMP	W1	H_SCOMP
H_SCOMP#	W2	H_SCOMP#
H_CPURST#	B6	H_CPURST#
H_CPUSLP#	E5	H_CPUSLP#
H_AVREF	B9	H_AVREF
H_DVREF	A9	H_DVREF

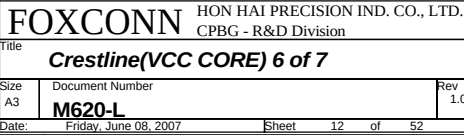


GM965=12-CRESTL1-ES03
GL960=12-CRESTL1-ES04

MCH_CFG_2[2:0] (FSB Frequency)	[2:0] = 010 = 800MT/s [2:0] = 011 = 667MT/s [2:0] = 001 = 533MT/s
MCH_CFG_5 (DMI Type)	Low = DMIx2 High = DMIx4 (Default)
MCH_CFG_7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality(Default)
MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation (Default)
MCH_CFG_13[13:12] (Test Mode Type)	[13:12] = 11 = Normal Operating (Default) [13:12] = 10 = All Z Mode [13:12] = 01 = XOR Mode [13:12] = 00 = Reserved
MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable (Default)
MCH_CFG_19 (DMI Lane Reversal)	Low = Normal operation (Default) High = Lane Reversed
MCH_CFG_20 (Concurrent SDVO/PCIE)	Low = Only SDVO or PCIE is operational (Default) High = SDVO & PCIE operate simultaneously through the PCI Express Graphics attach port

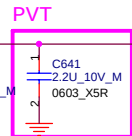








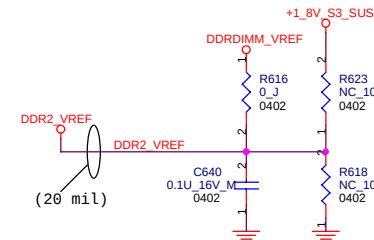
0.1 μ F and 2.2 μ F placed close to VREF pins



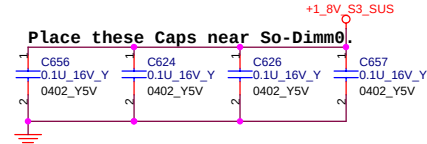
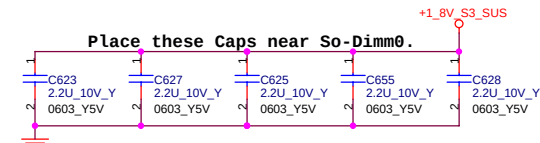
+1.8V S3_SUS

+1.8V S3_SUS

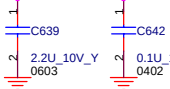
1.8V per DIMM=3.08A



Close to DIMM

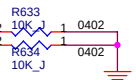


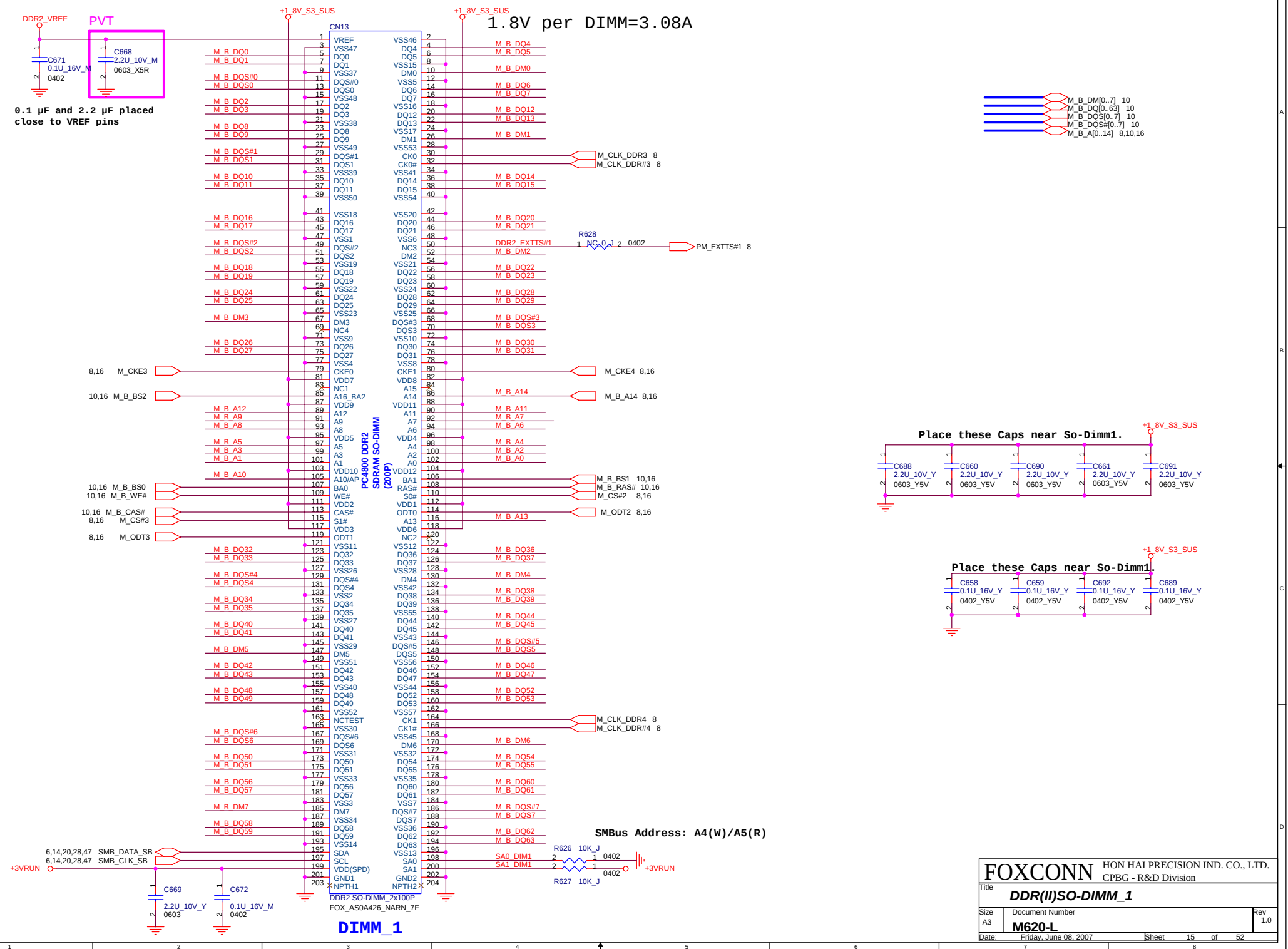
6,15,20,28,47 SMB_DATA_SB
6,15,20,28,47 SMB_CLK_SB
+3VRUN

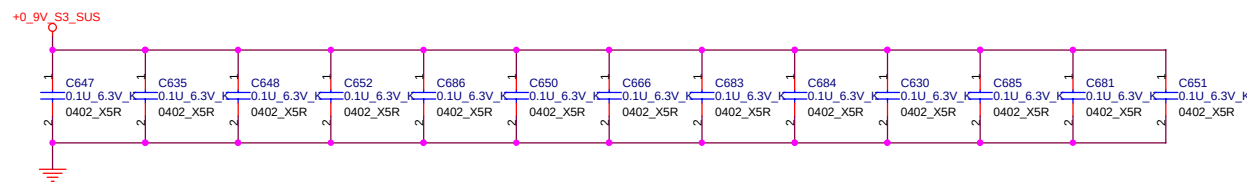


DDR2 SO-DIMM_2x100P
FOX_AS0A426_N2RN_7F
DIMM_0

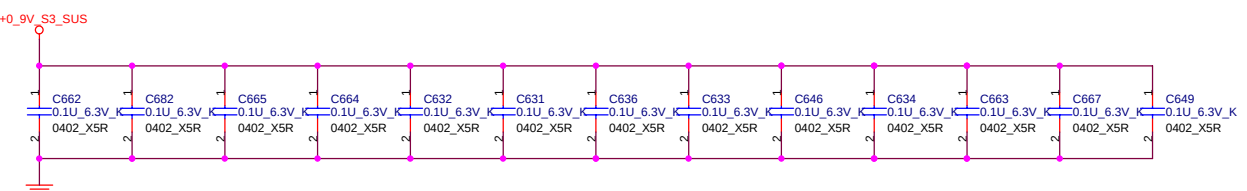
SMBus Address: A0(W)/A1(R)



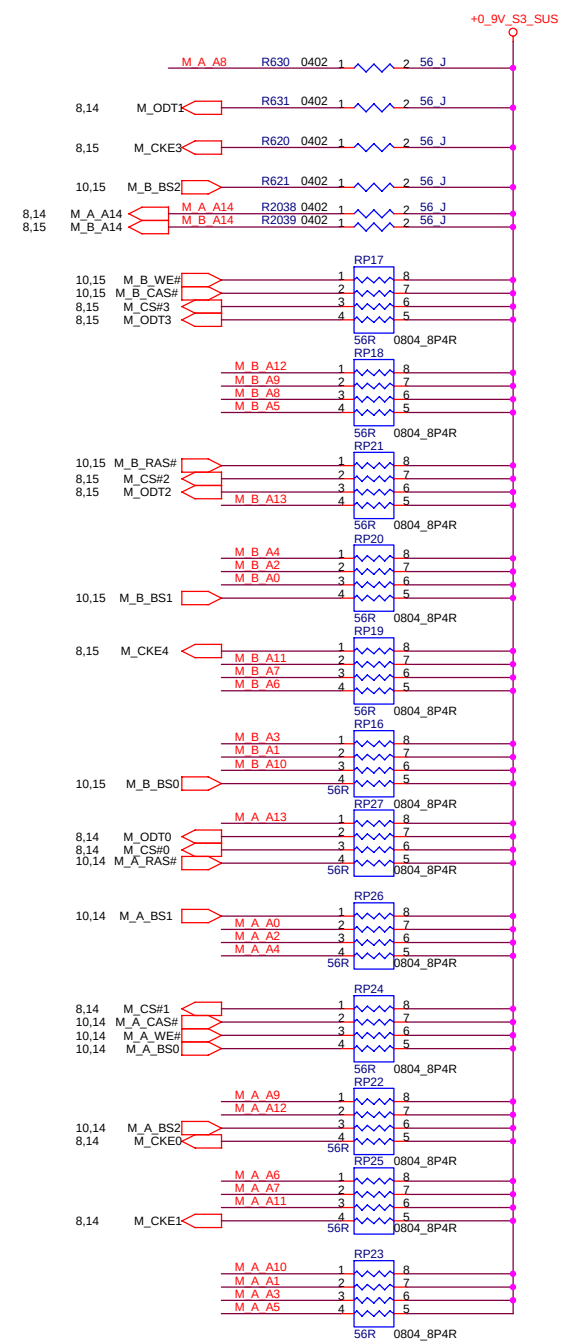




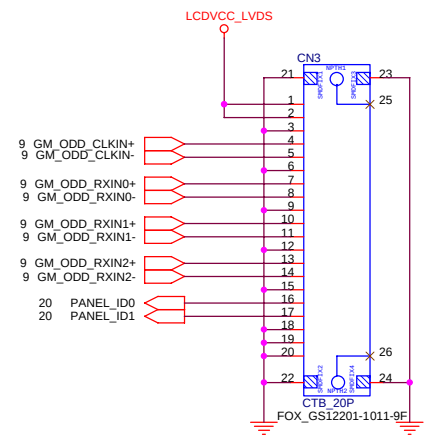
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9V_S3_SUS



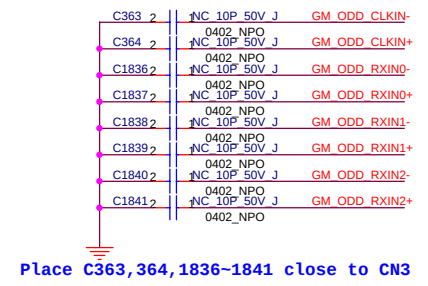
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9V_S3_SUS



LVDS CONNECTOR

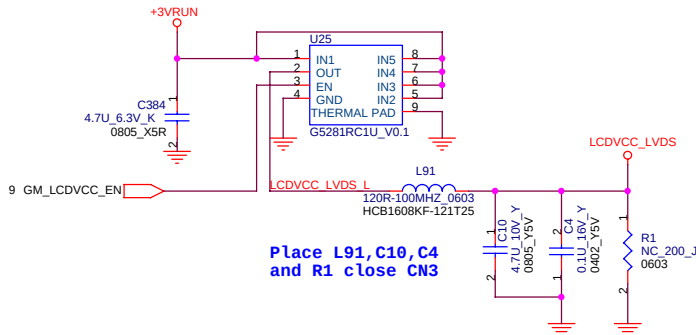


For EMI



Place C363,364,1836~1841 close to CN3

LCD POWER

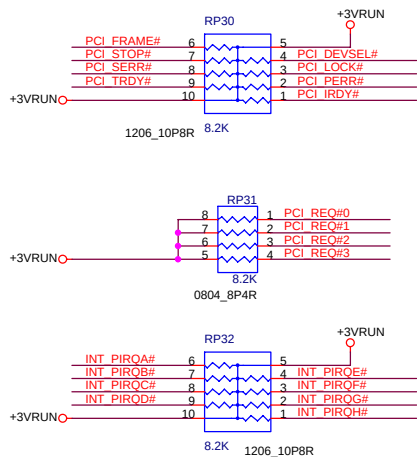


Place L91,C10,C4 and R1 close CN3

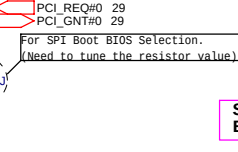
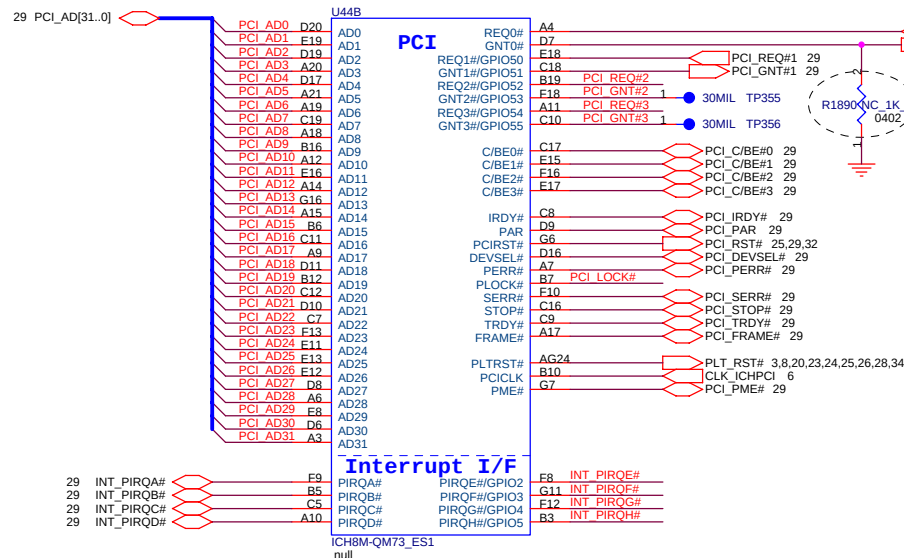
DISCHARGE
DISCHARGE

The R1 will consume about 0.054 Watt (3.3x3.3/200 = 0.054W). We changed resistor to 0603 size (1/8 watt)

Cable ID(1:0)0	0	0	1	1	0	1	1
Vendor	CPT						
Type							
Model Name	CLAA154WA05AN						
Size	15.4"	15.4"	15.4"	15.4"			

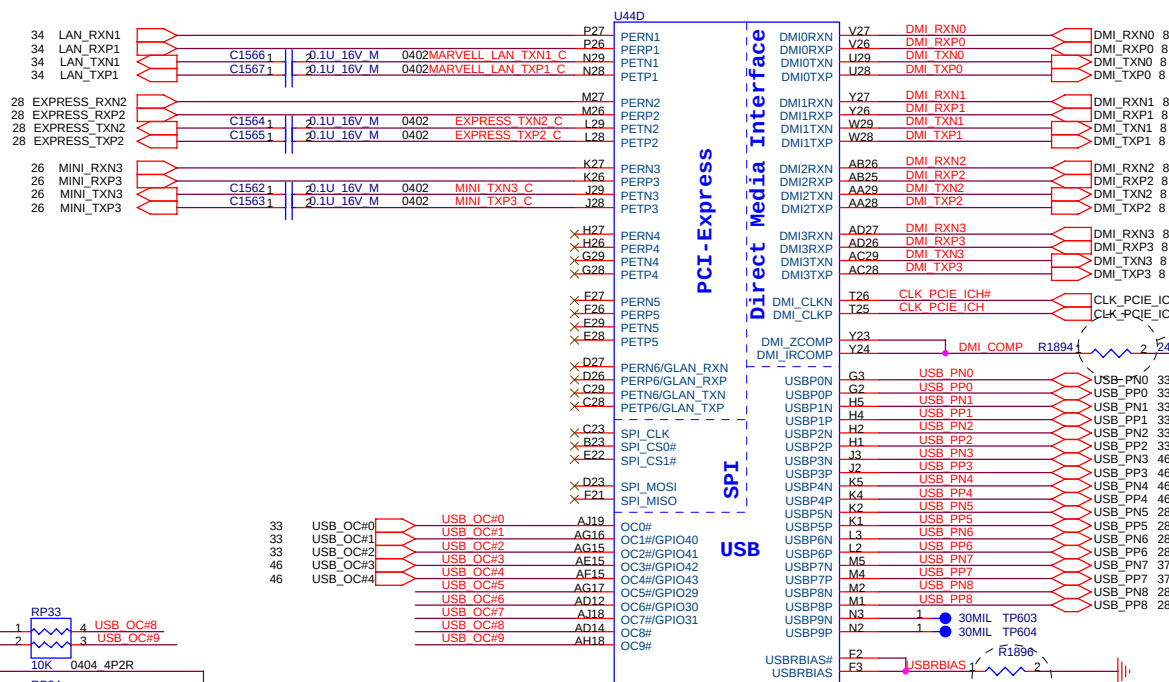


PCI Pullups



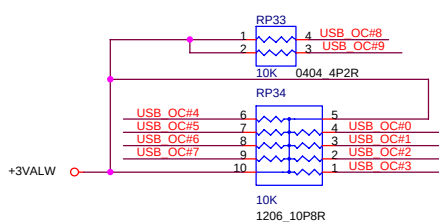
Strap for Boot-BIOS

	GNT0#	SPI_CS1#
IPC(Default)	H1	H1
PCI	H1	LOW
SPI	LOW	H1

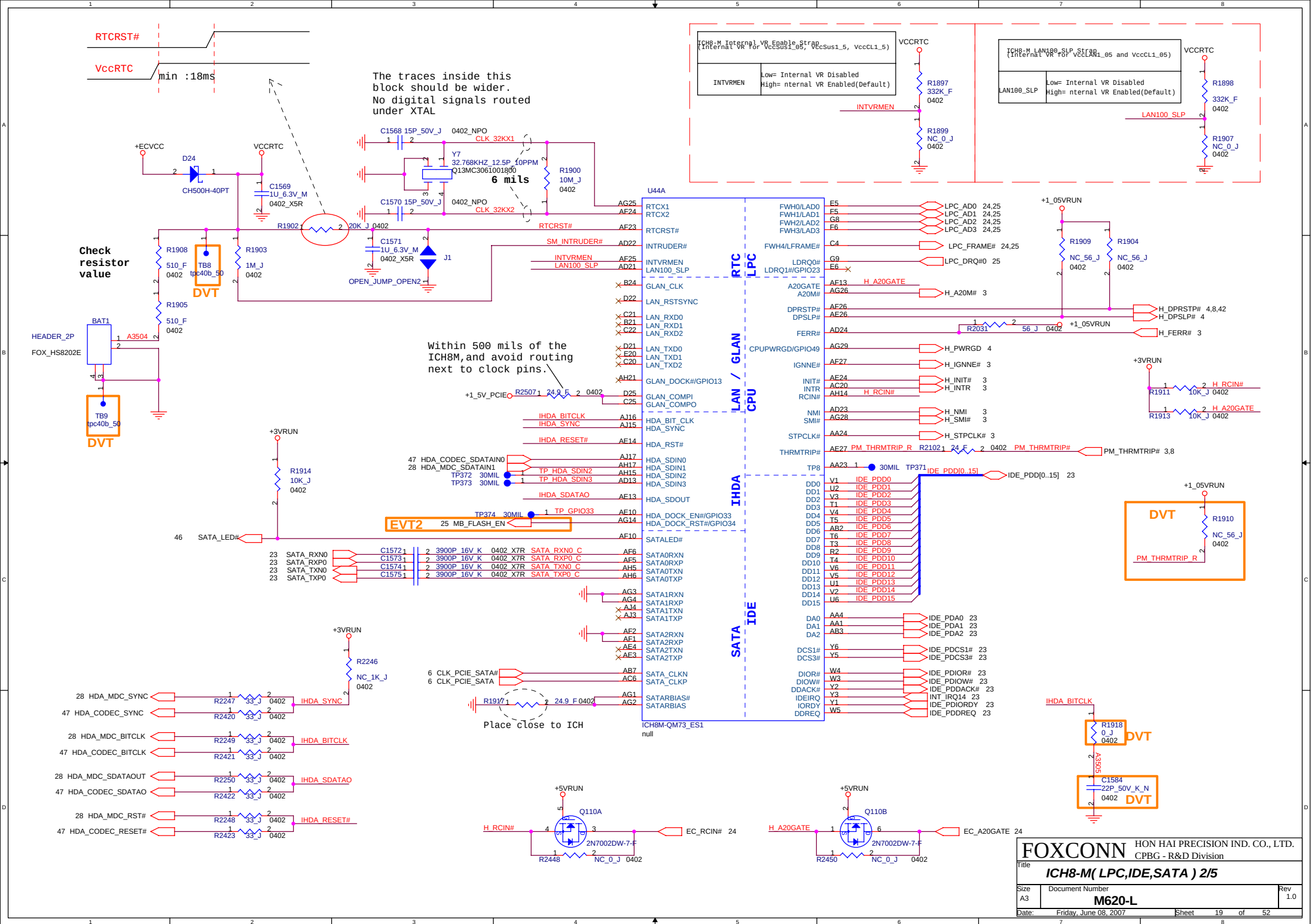


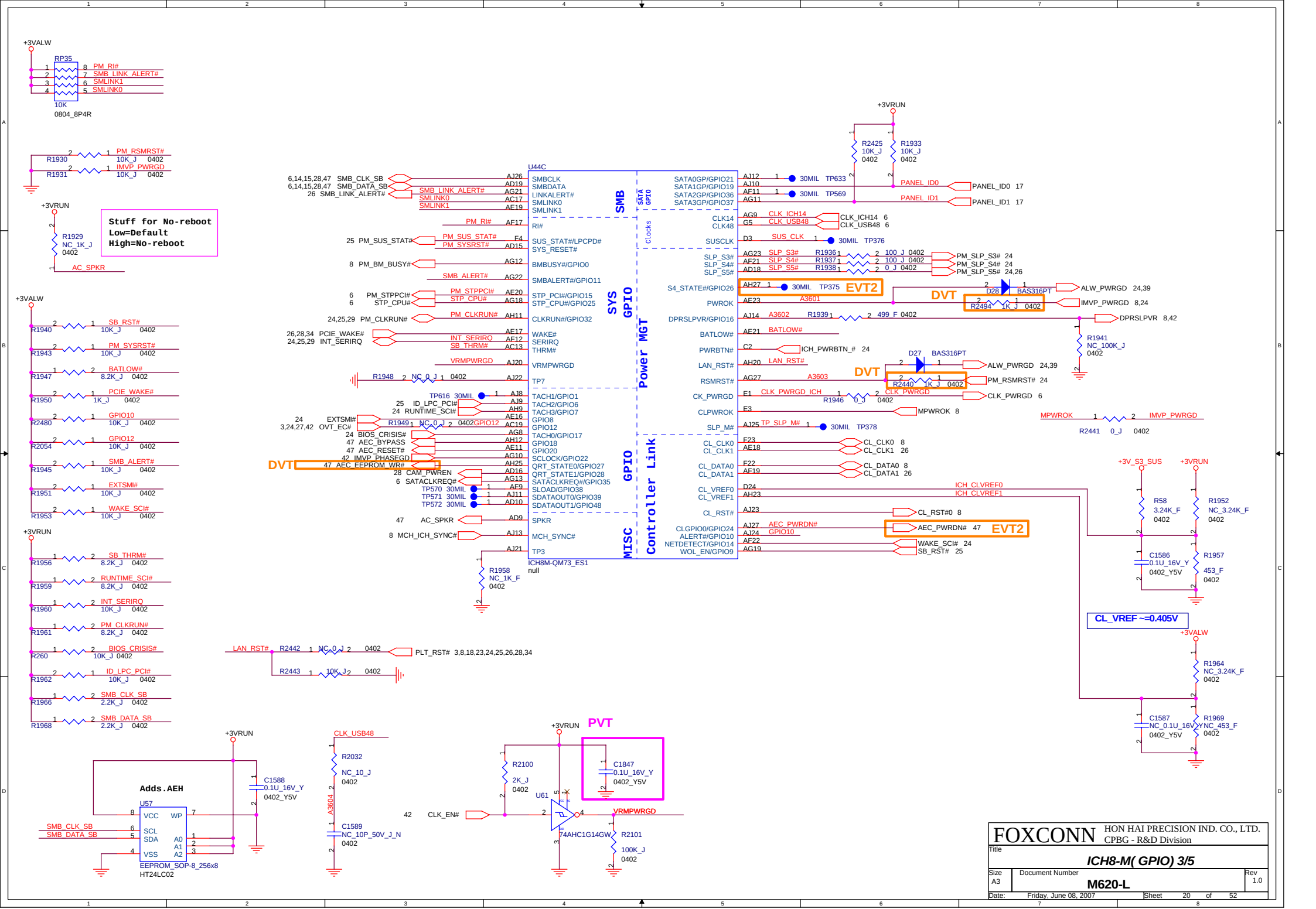
Place within 500 mils of ICH

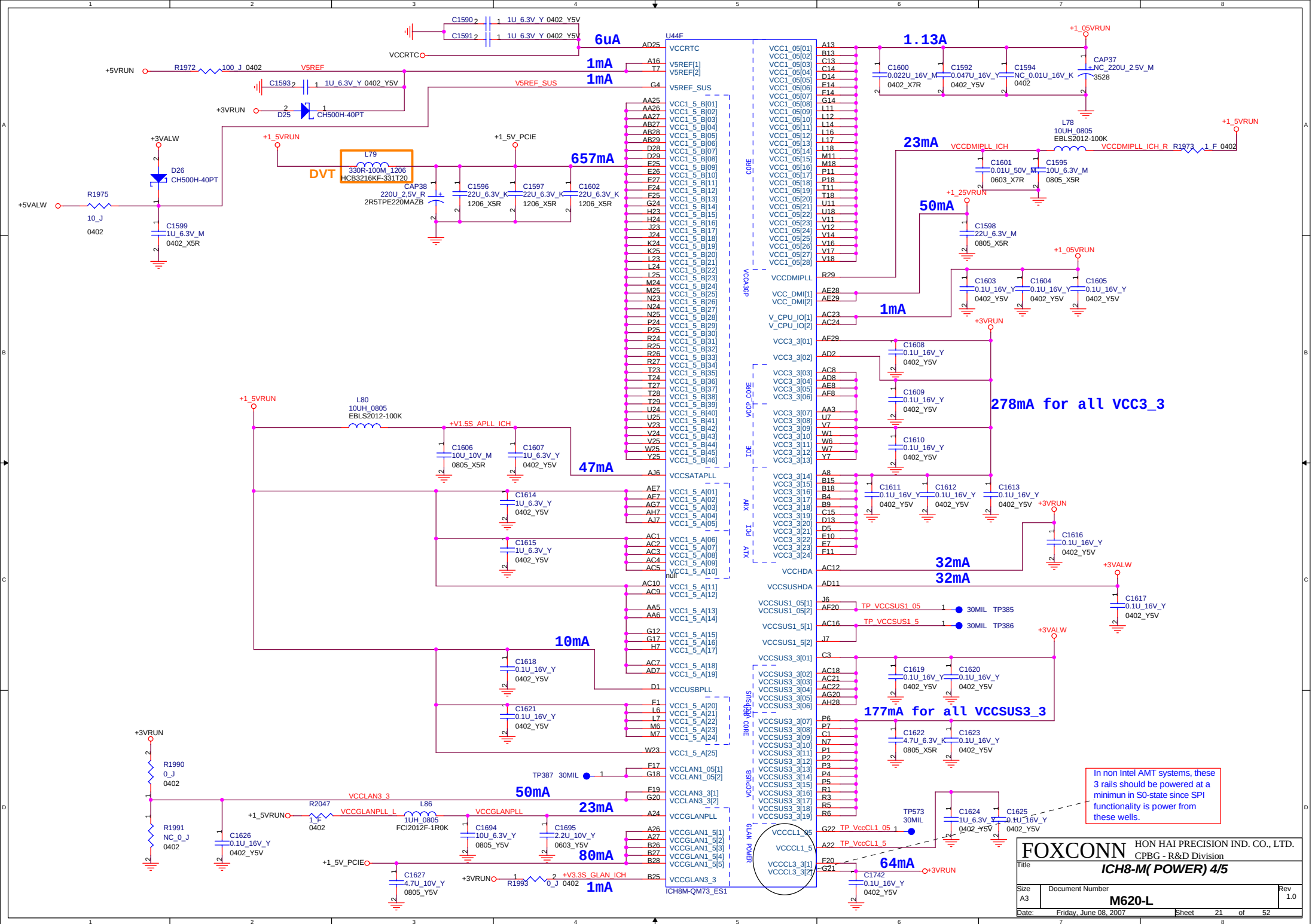
USB PORT	Function
PORT-0	REAR-1
PORT-1	REAR-2
PORT-2	REAR-3
PORT-3	SIDE-1
PORT-4	SIDE-2
PORT-5	EXPRESS CARD
PORT-6	CAMERA
PORT-7	CIR
PORT-8	OIDE
PORT-9	NC

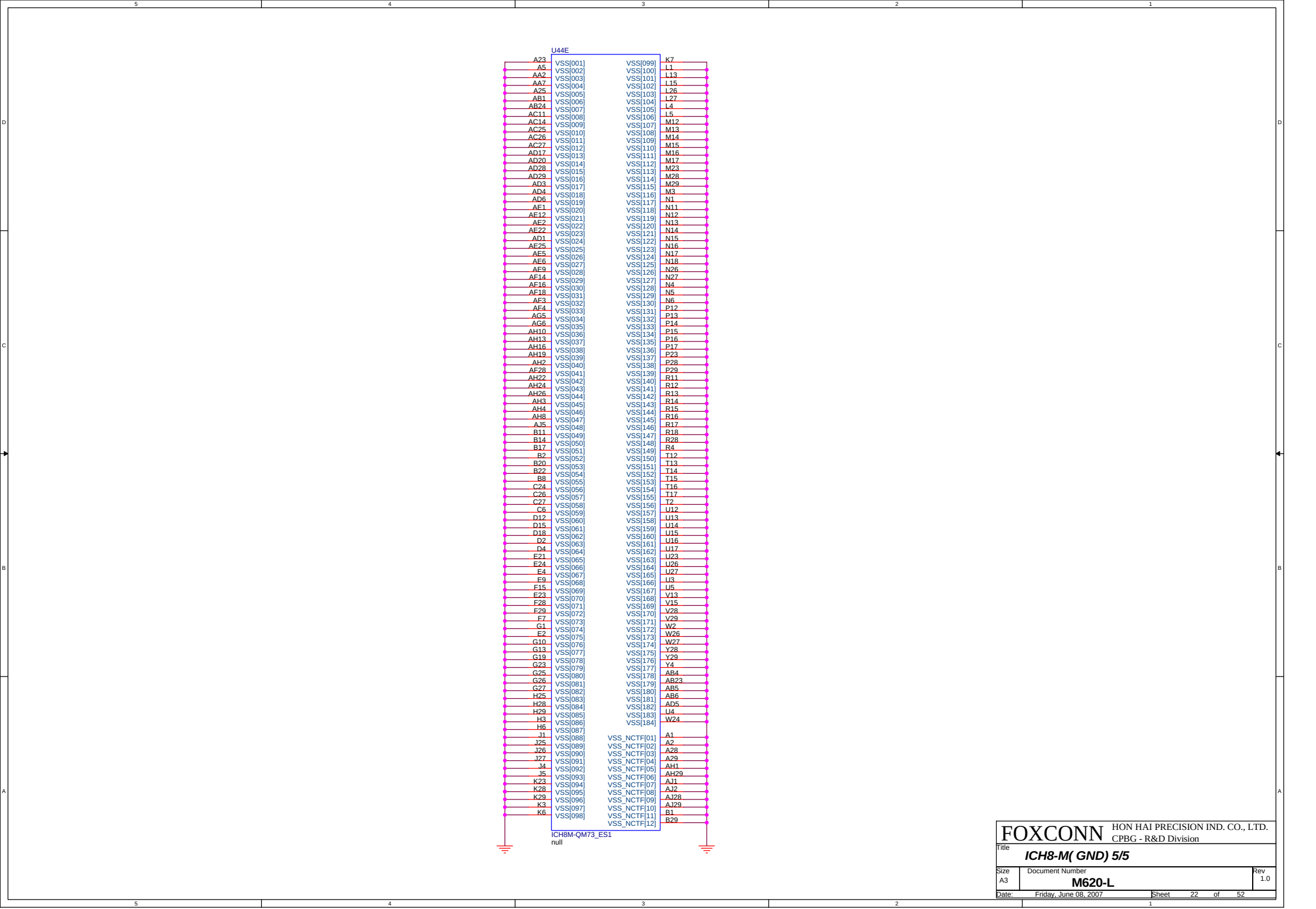


Place within 500 mils of ICH and don't routing next to high speed signals

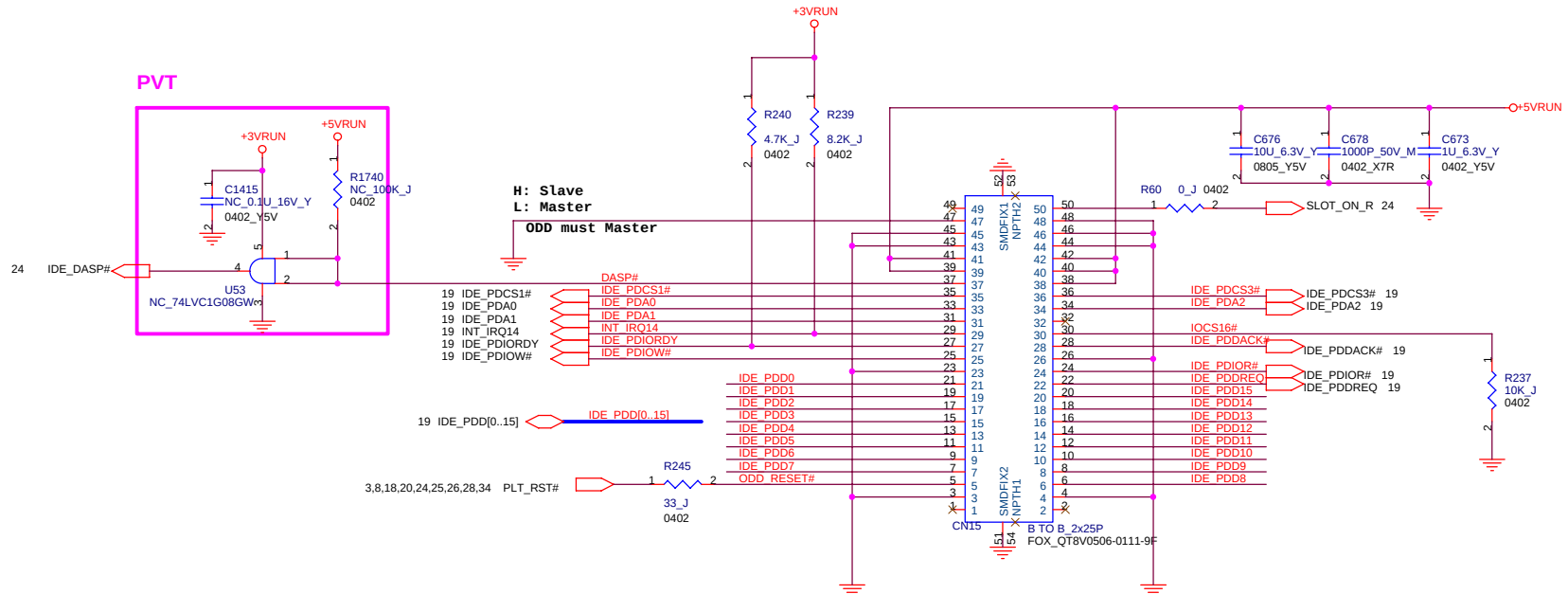
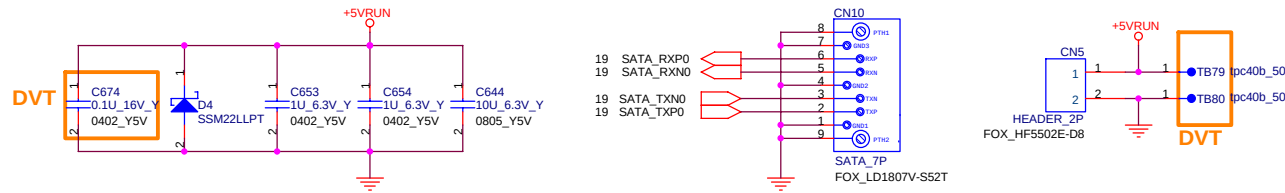




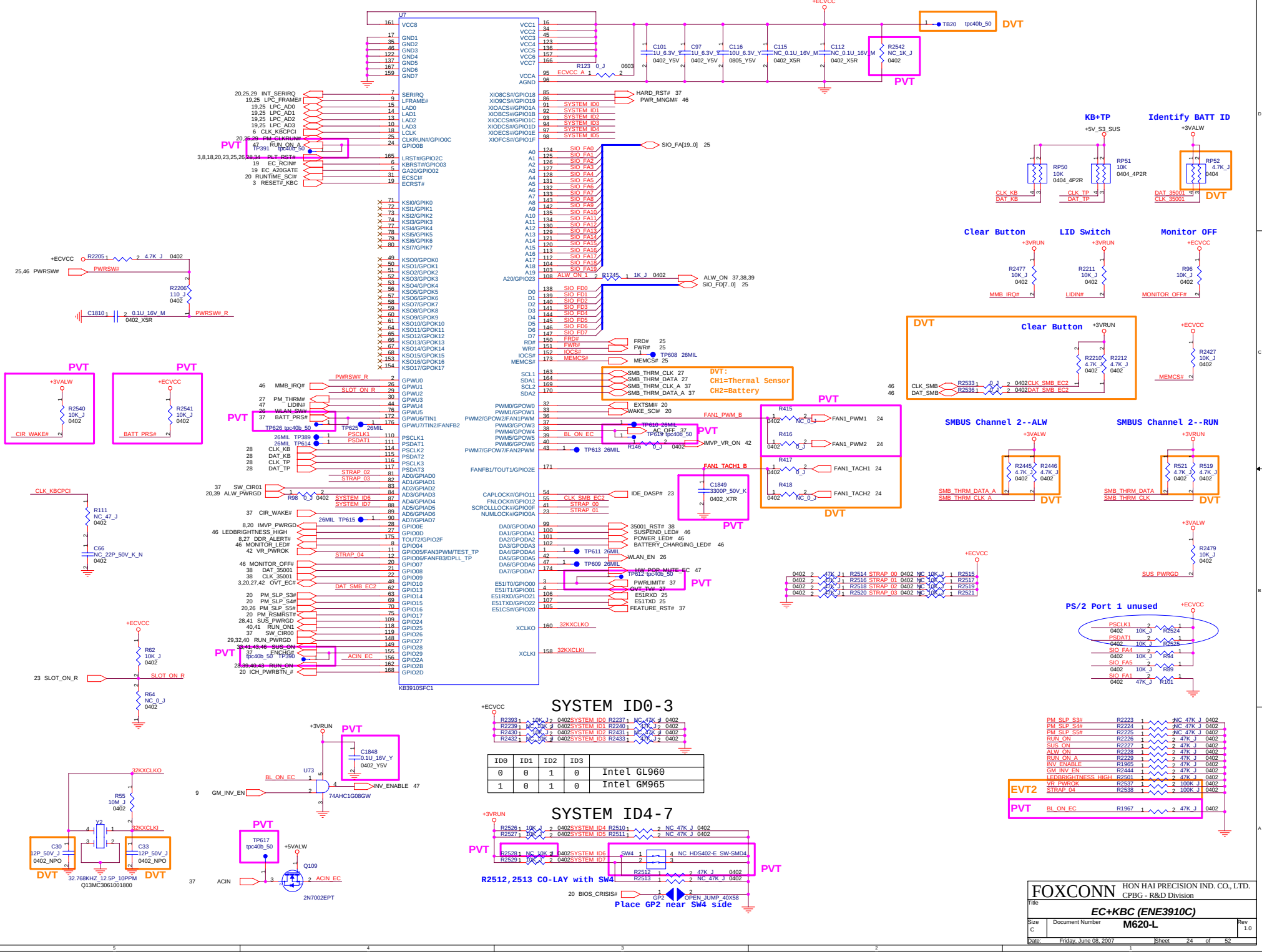




SATA HDD CONN



CD-ROM CONN



SYSTEM ID0-3

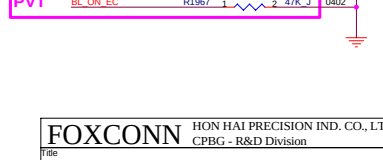
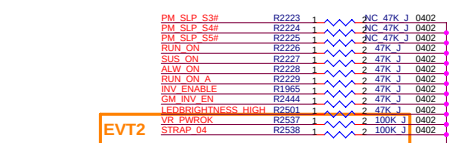
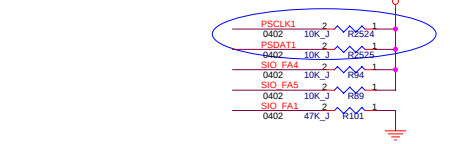
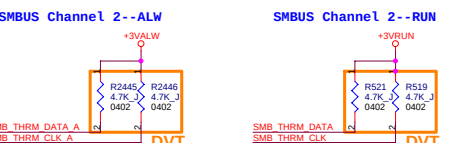
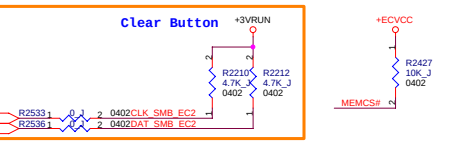
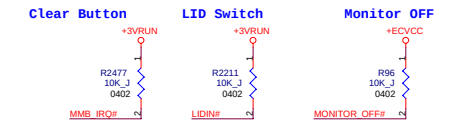
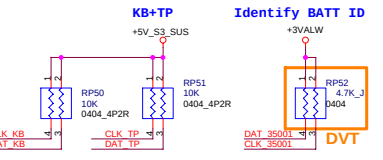
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1	0	1	0

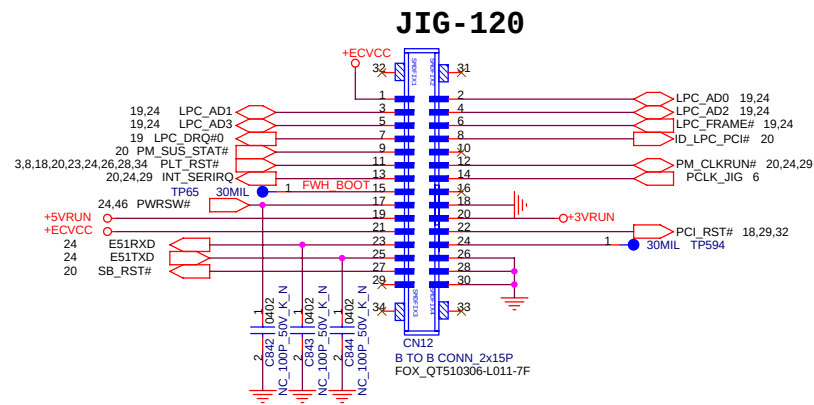
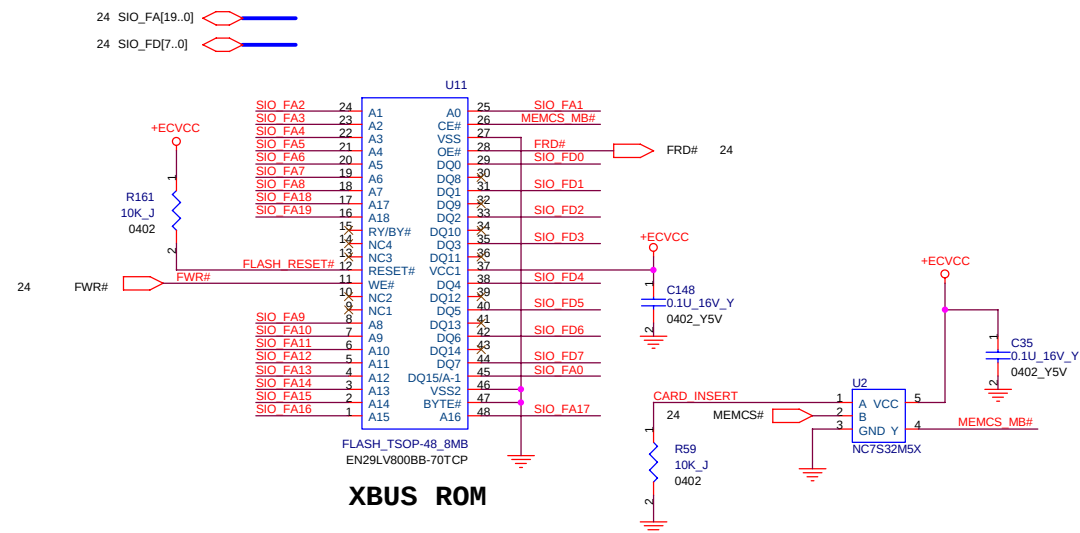
Intel GL960
Intel GM965

SYSTEM ID4-7

ID4	ID5	ID6	ID7
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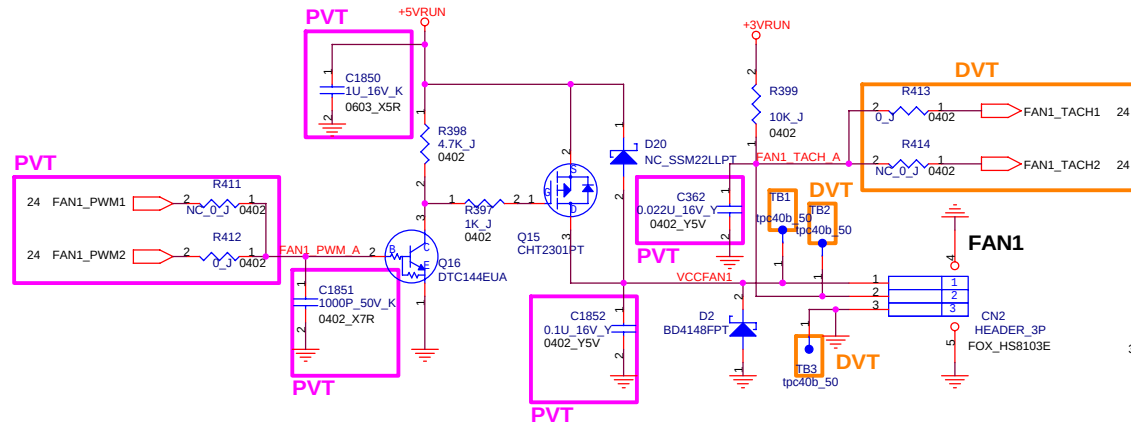
Intel GL960
Intel GM965



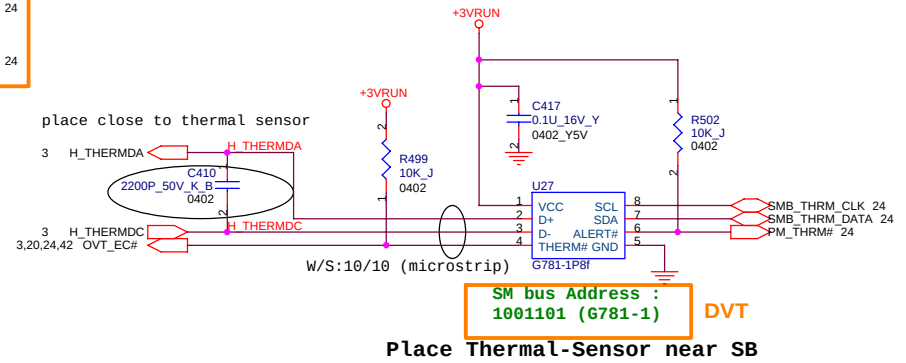


EXTERNAL XBUS ROM INTERFACE

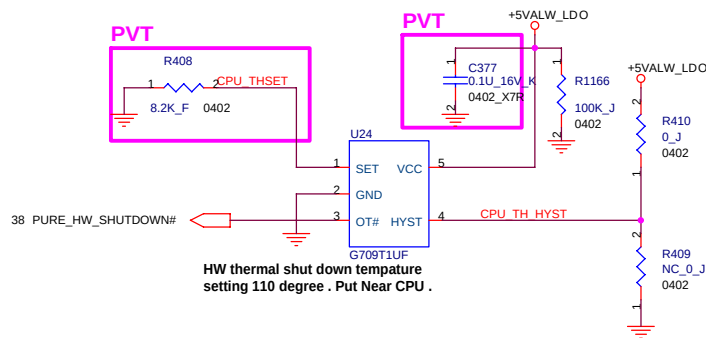
FAN



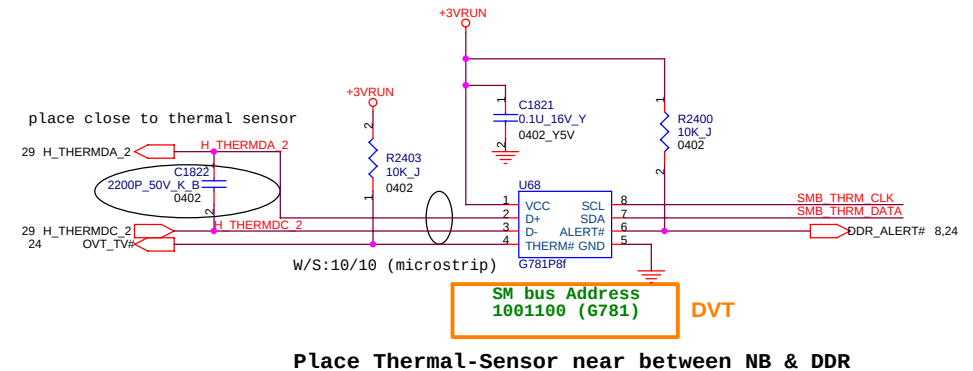
CPU/AUDIO SENSOR G781-1

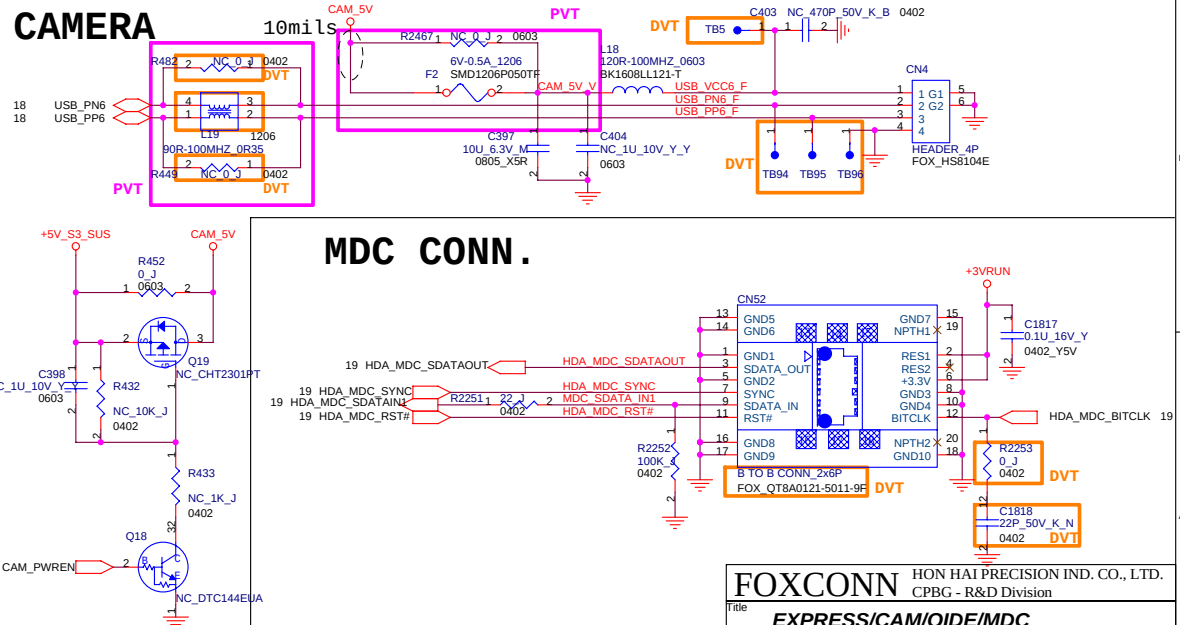
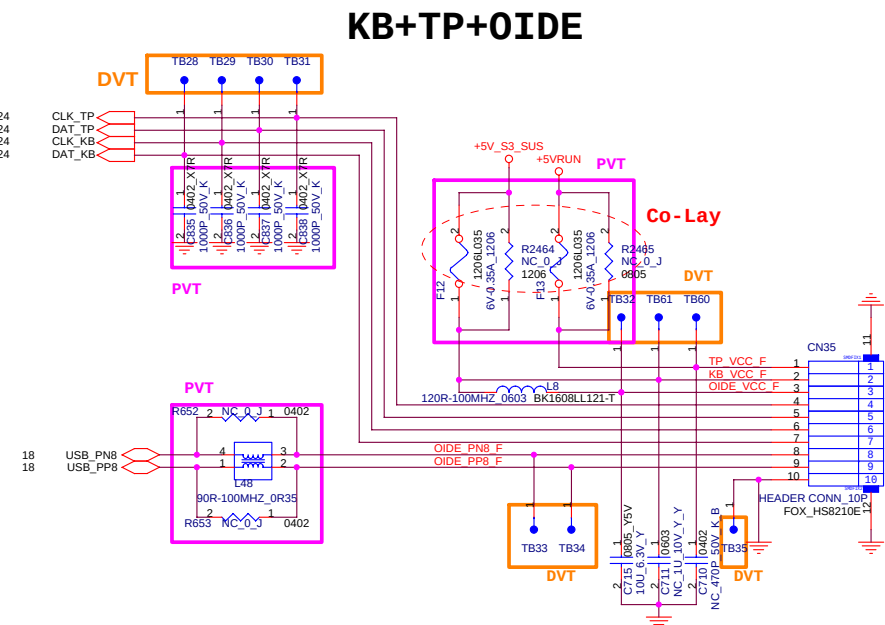
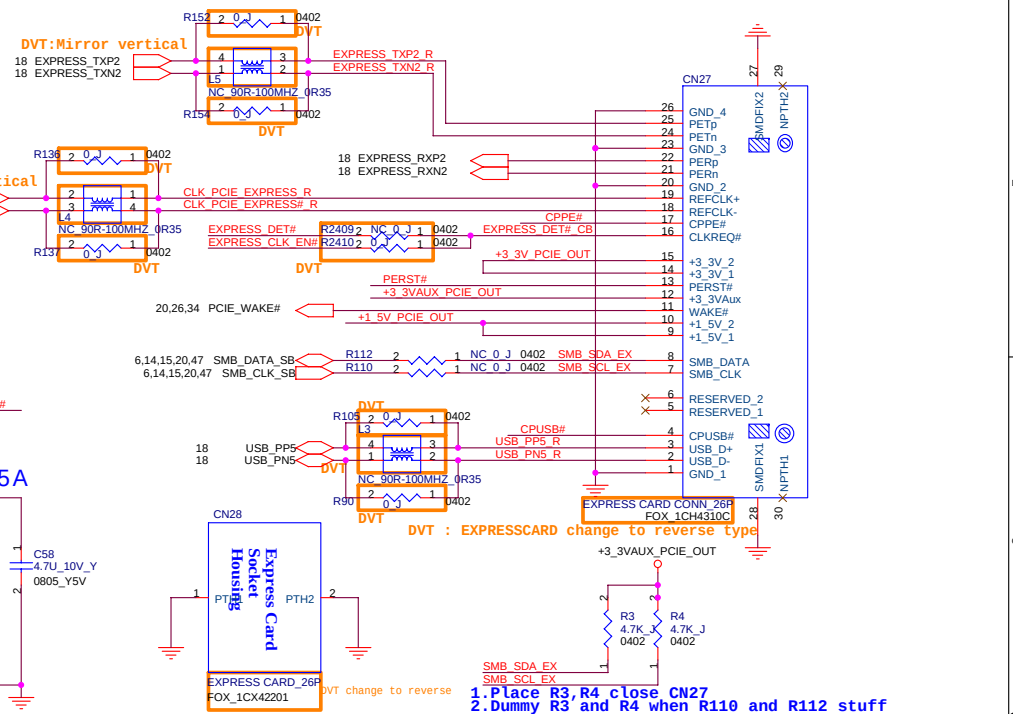
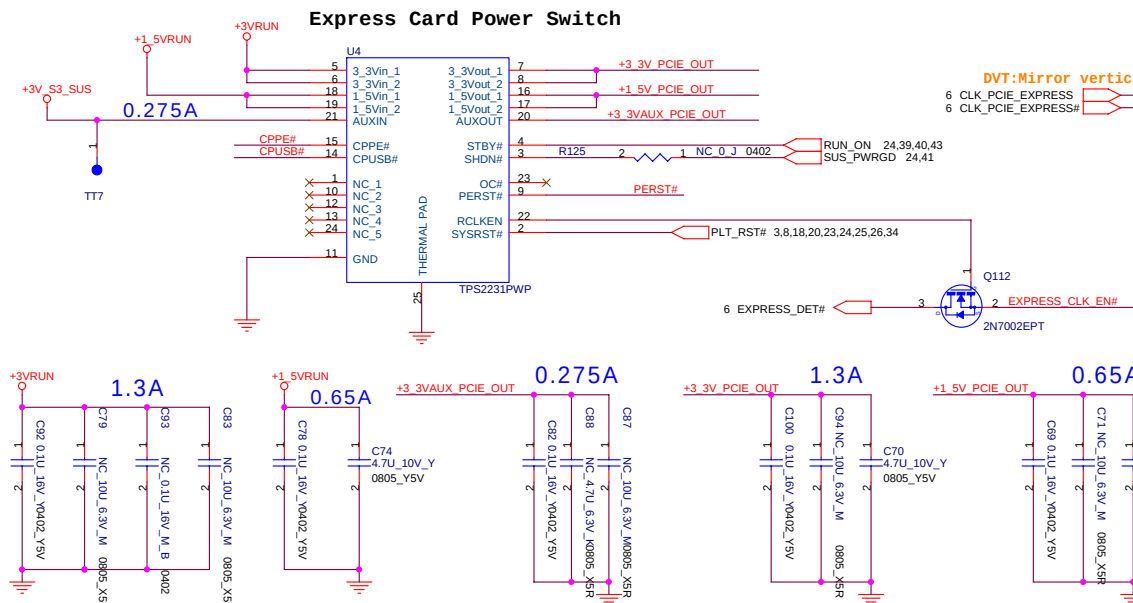


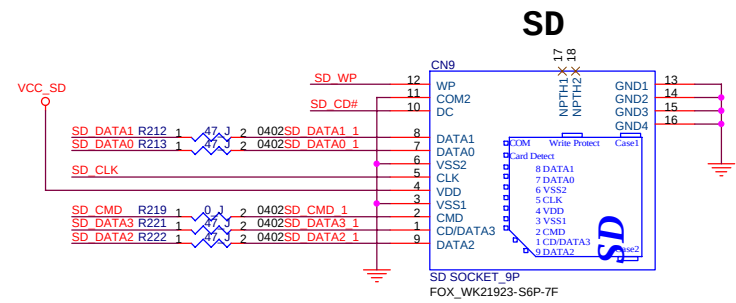
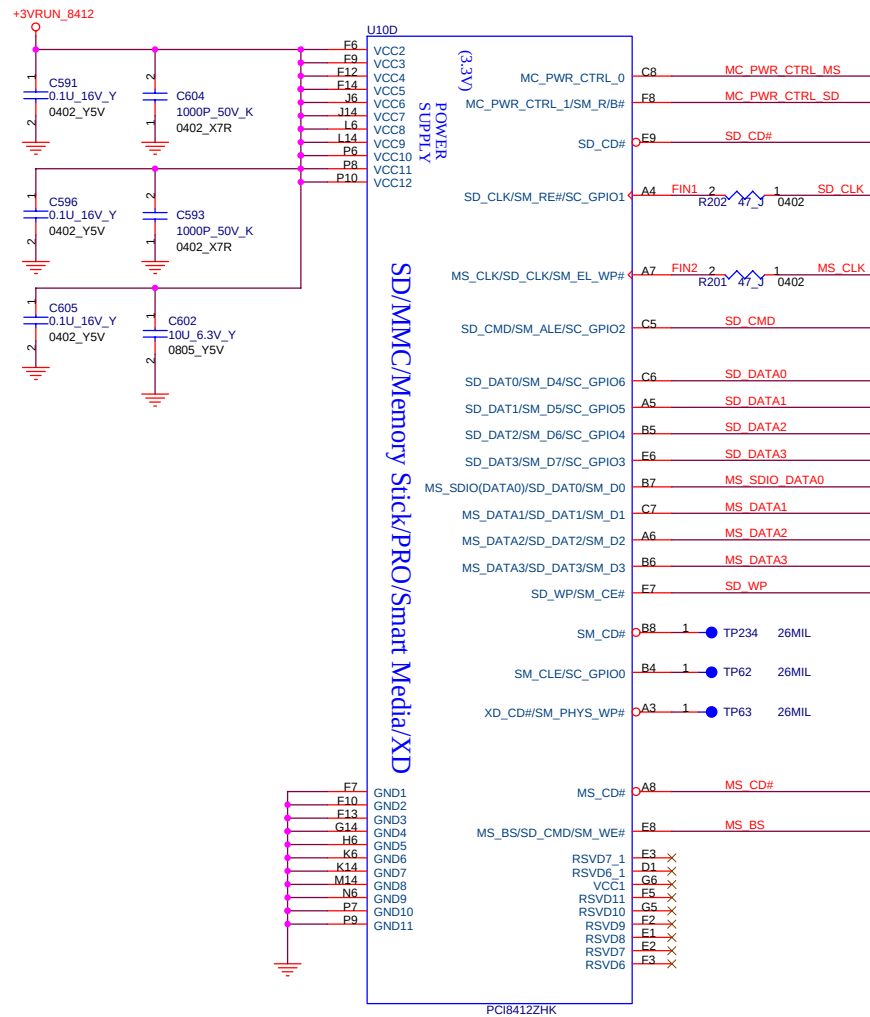
HW THERMAL PROTECTION



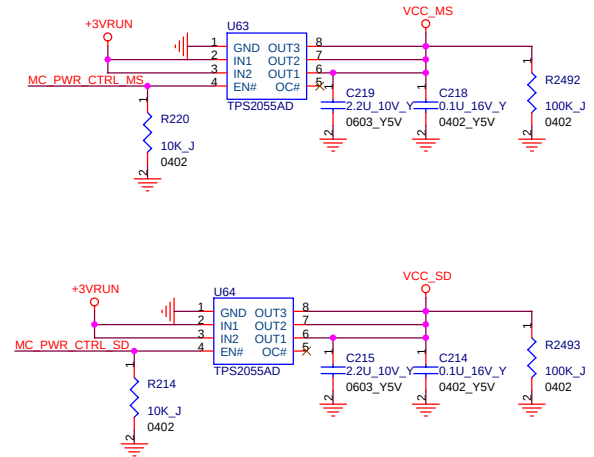
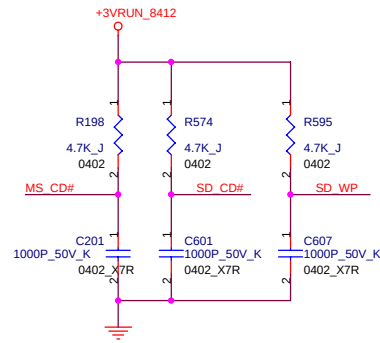
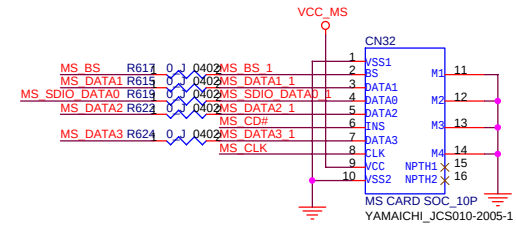
GMCH/DDR/TV SENSOR G781

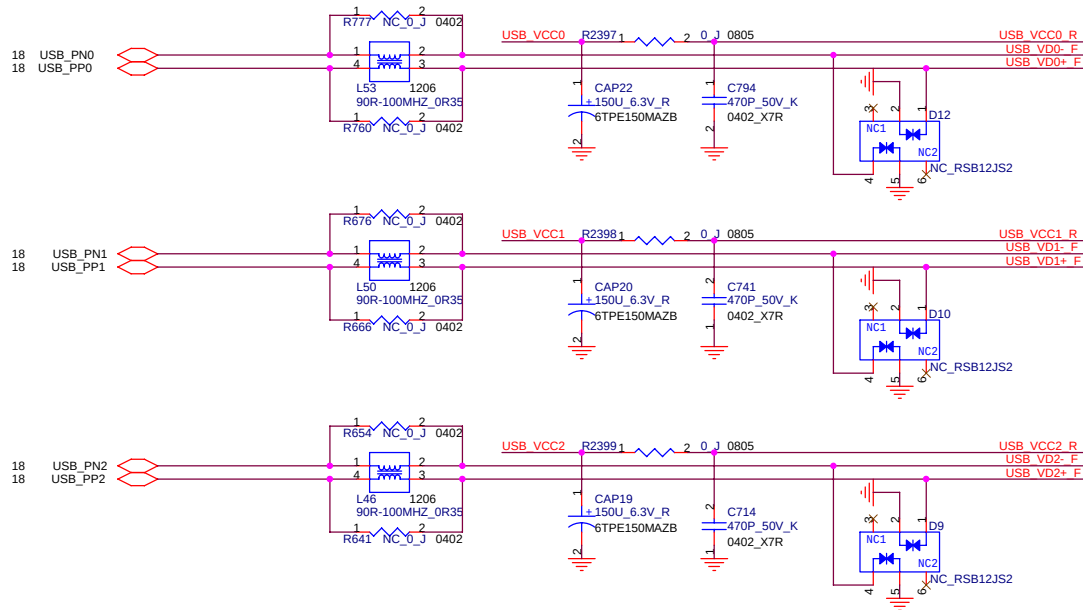
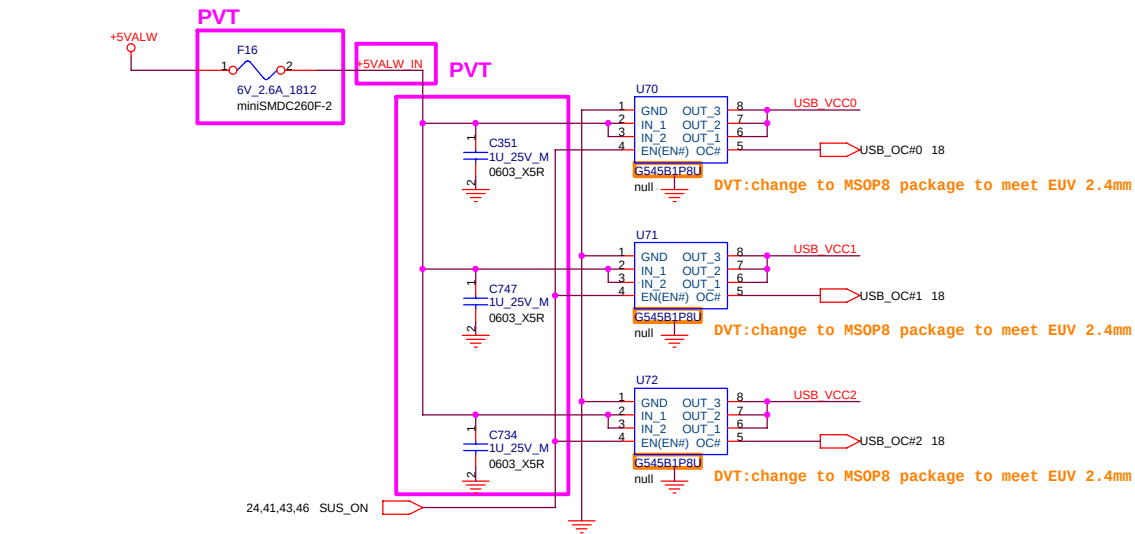




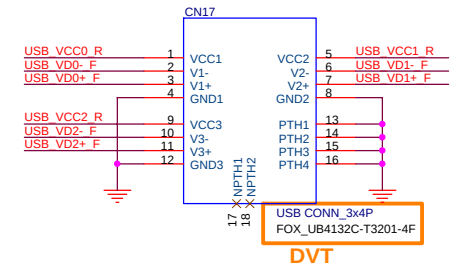


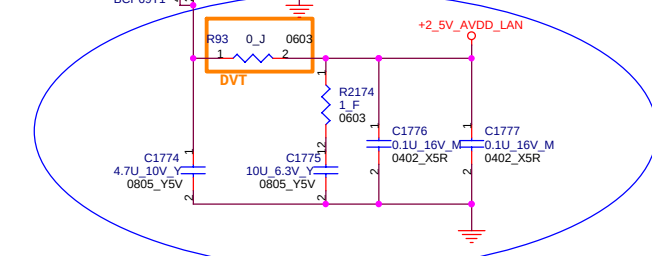
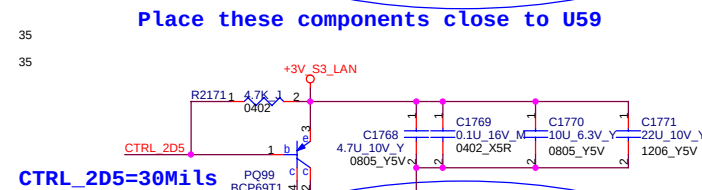
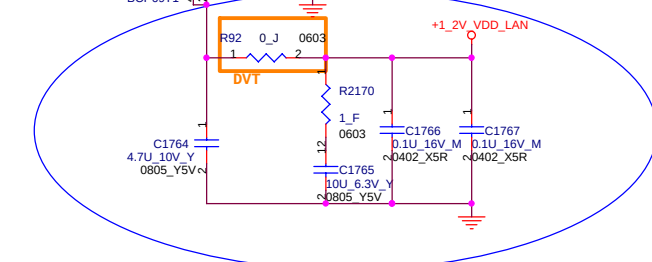
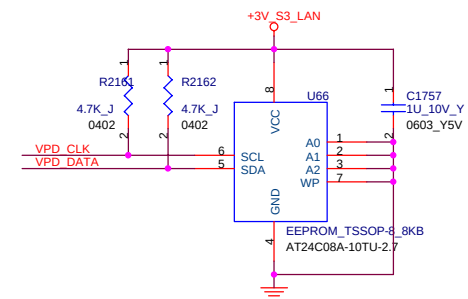
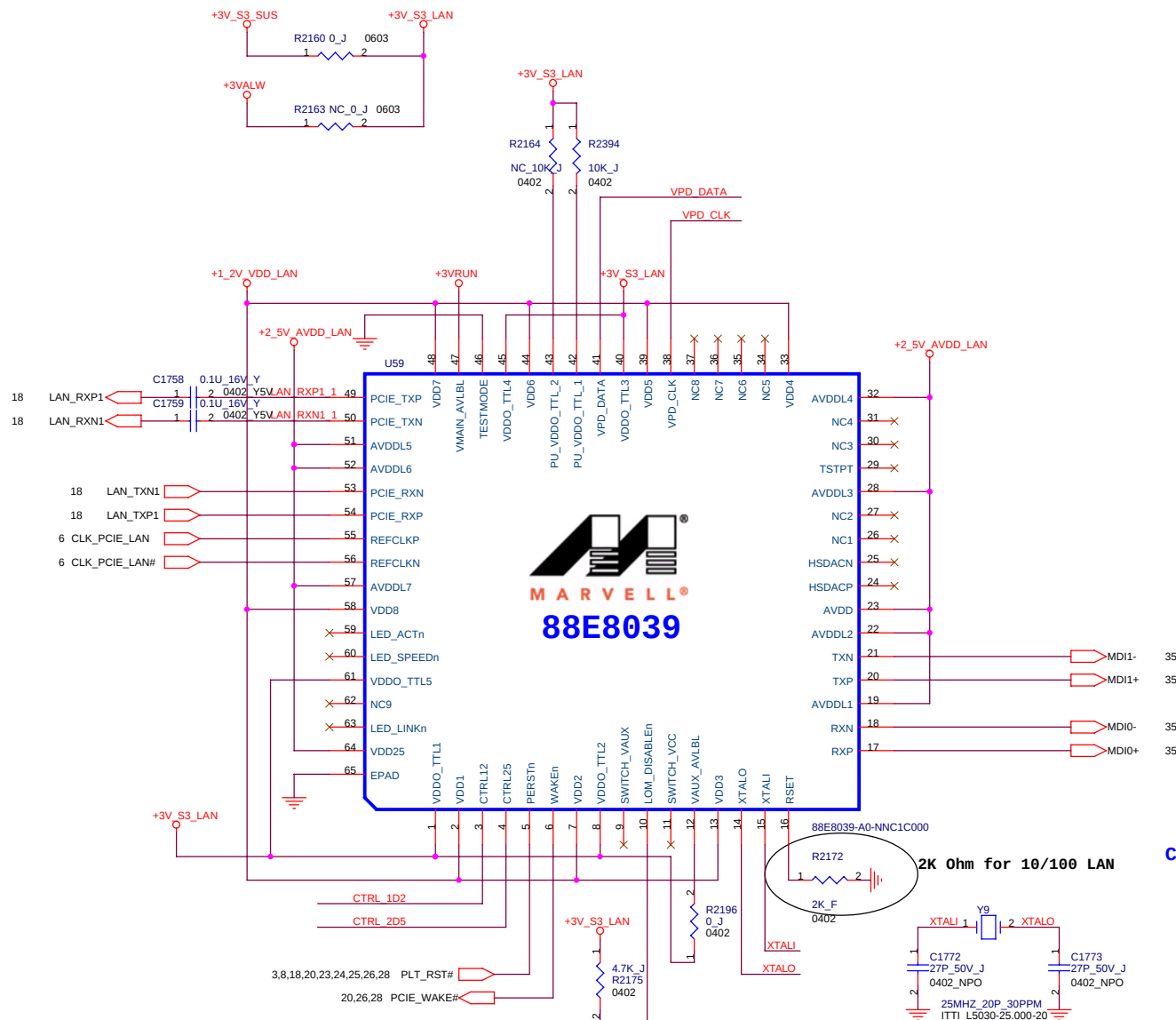
MS Duo

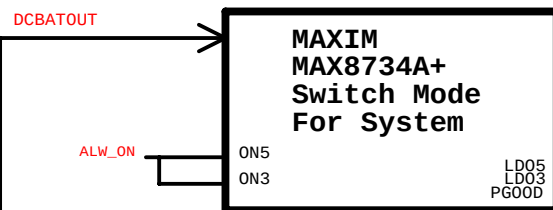
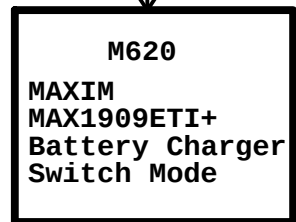
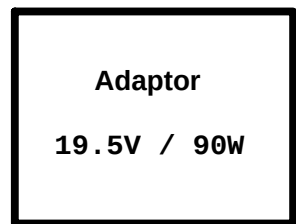




REAR USB CONN X 3







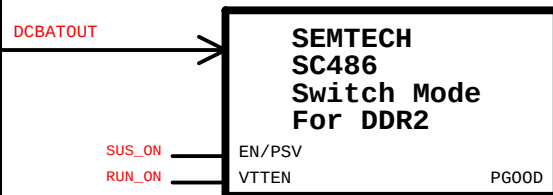
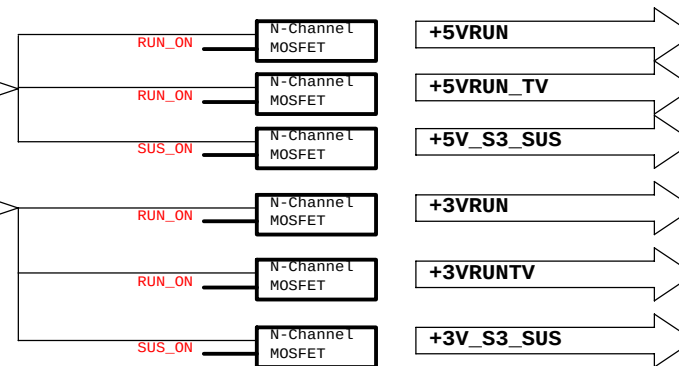
System

+5VALW 7A

System

+3VALW/7A

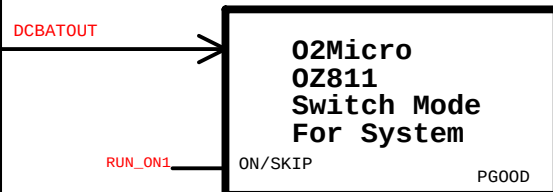
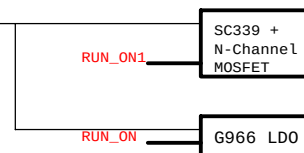
+5VALW_LDO
+ECVCC
ALW_PWRGD



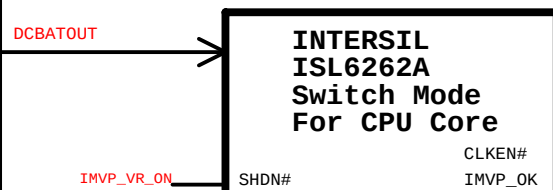
+1_8V_S3_SUS/10A

+0_9V_S3_SUS/3.0A

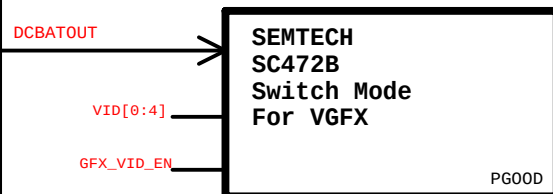
DDRDIMM_VREF



+1_05VRUN/ 7.5A / 15A



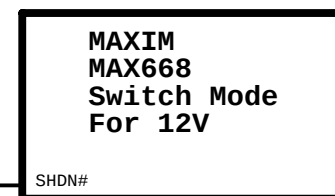
VHOCORE/44A



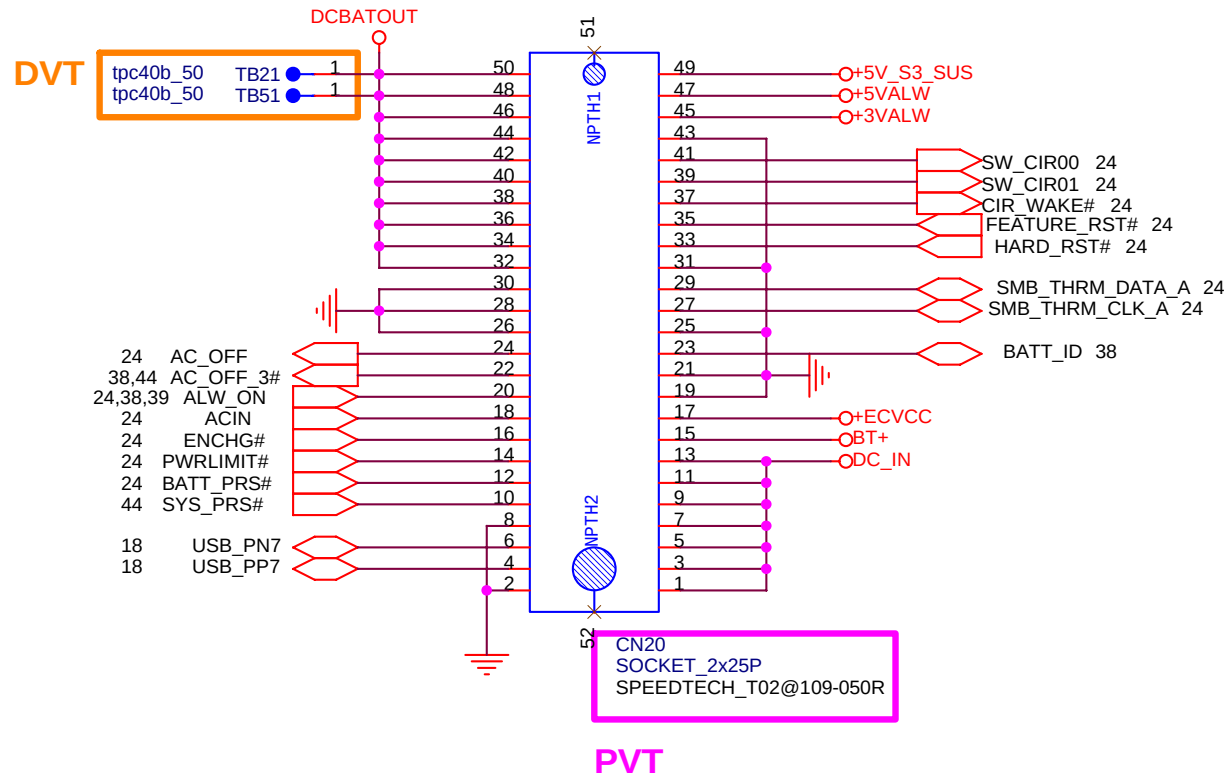
VGFX(1.05V)/7.5A

+5VALW

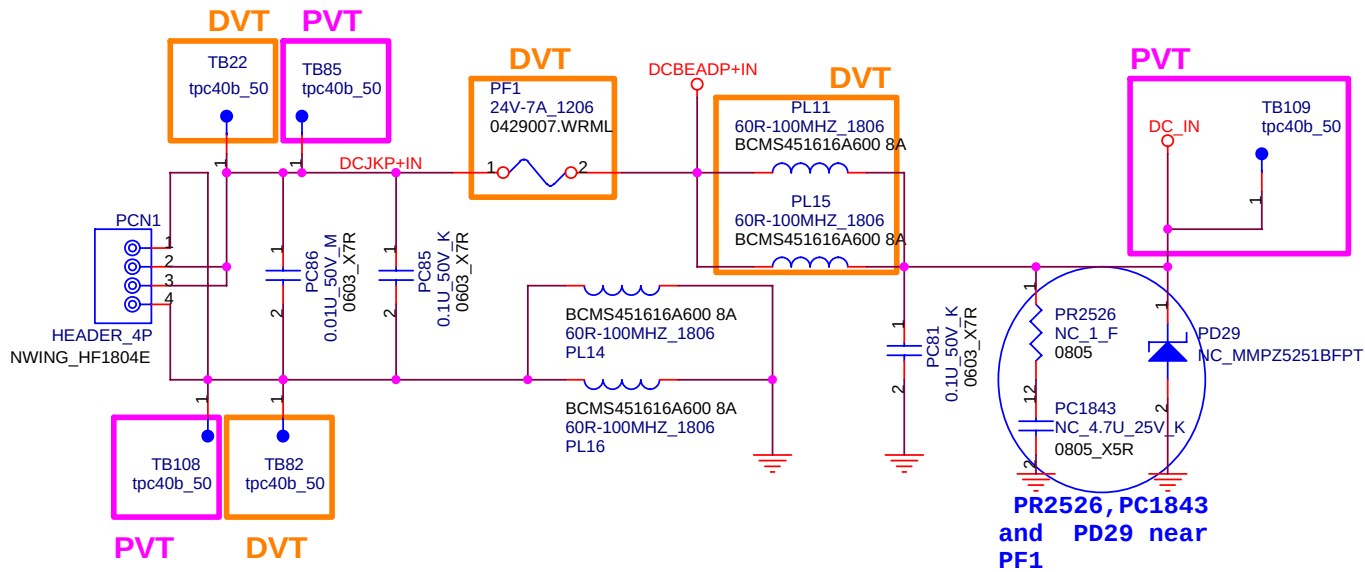
RUN_ON_A



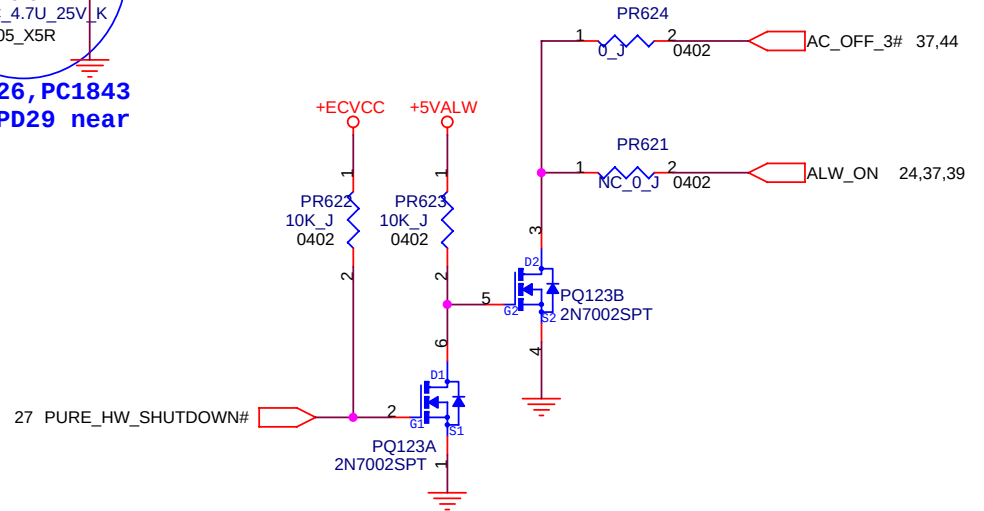
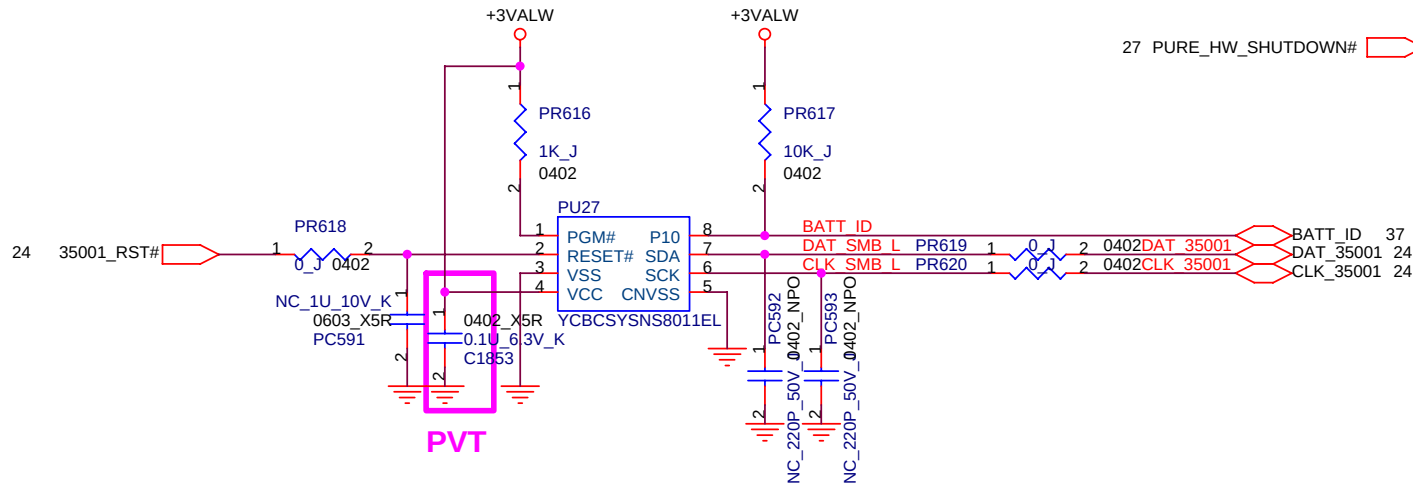
+12VRUN/1.2A

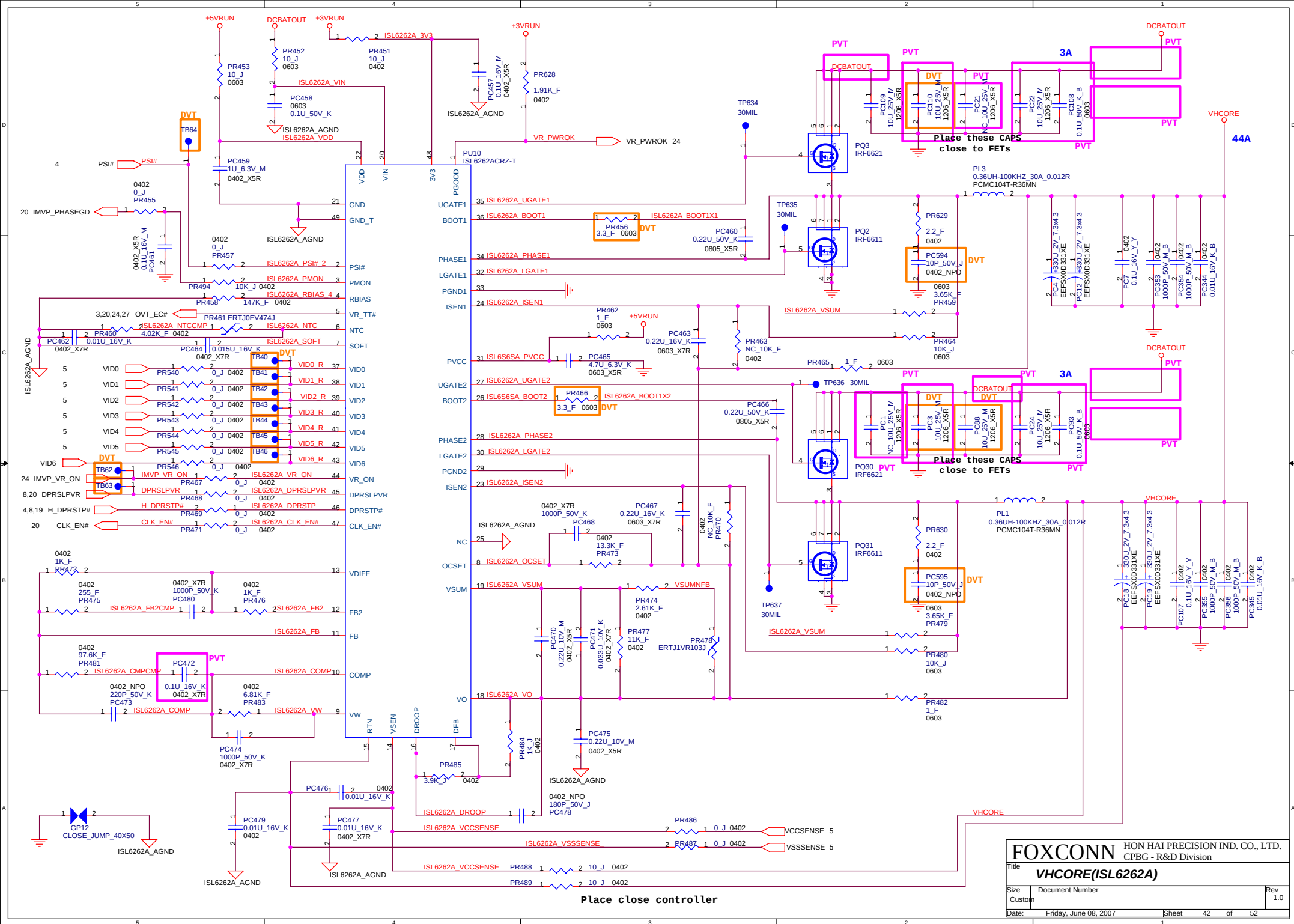


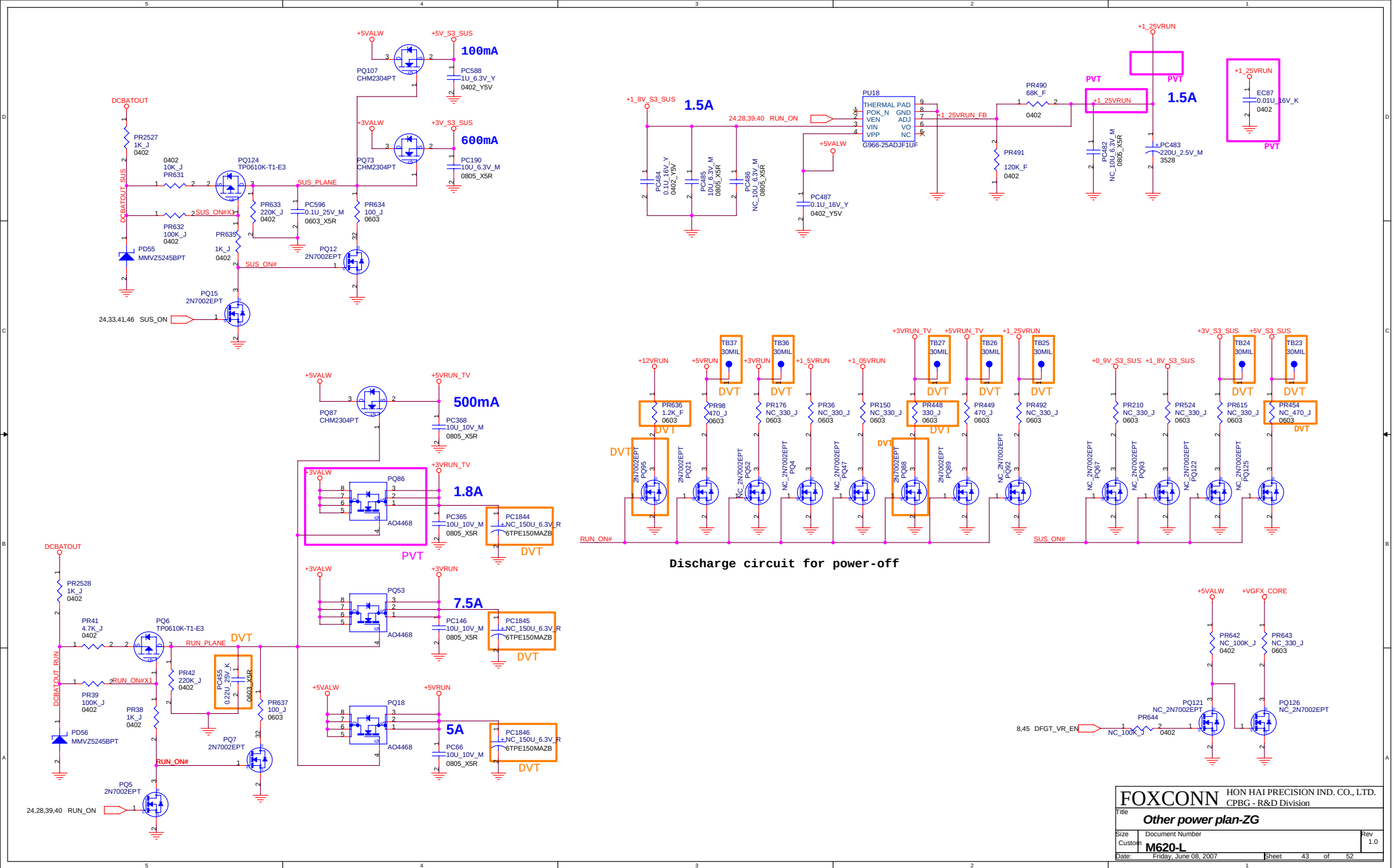
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Title			
Battery DB Connector			
Size A	Document Number M620-L		Rev 1.0
Date:	Friday, June 08, 2007	Sheet	37 of 52

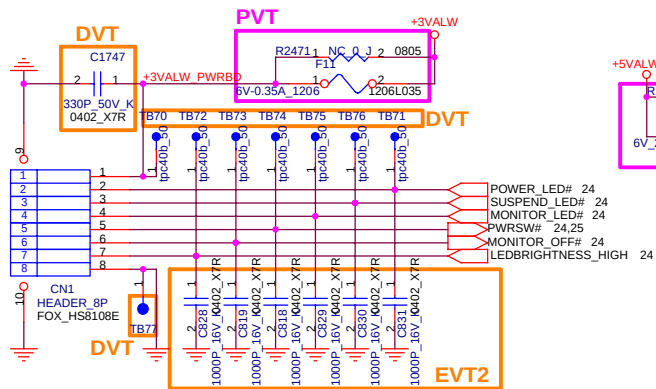


Identify Battery

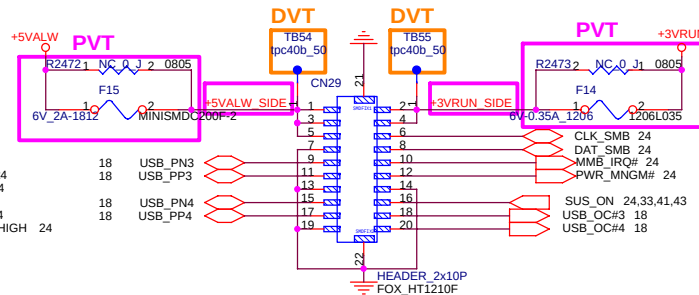




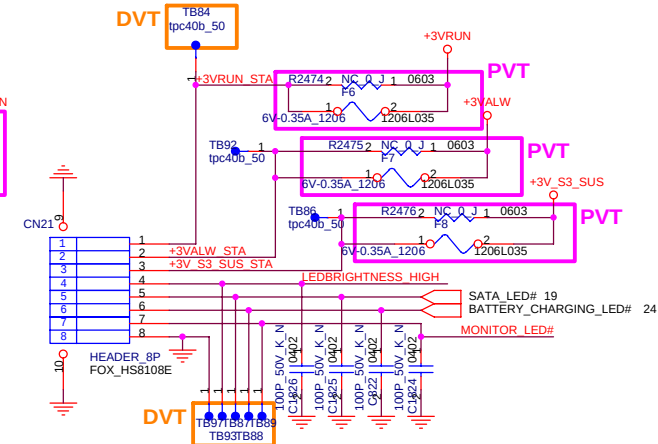




Power LED/Power BTN

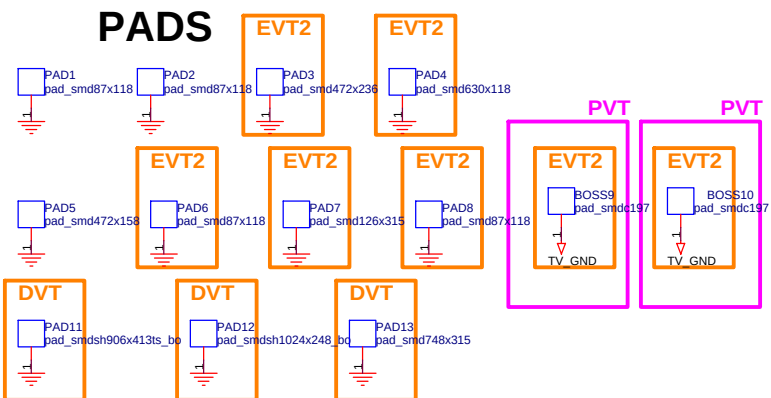


SIDE USB CONN

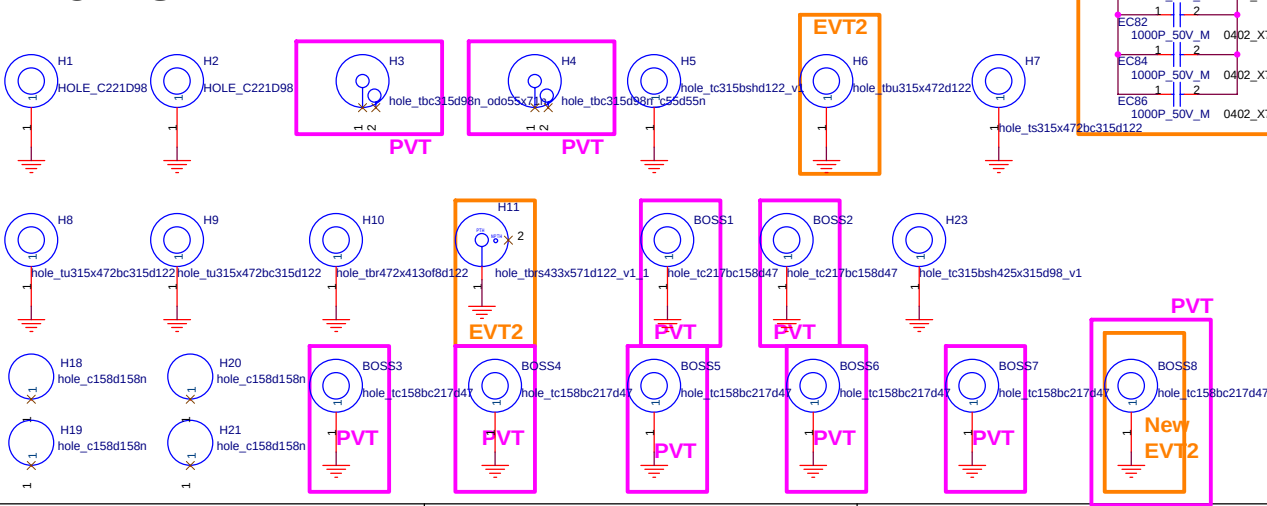


STATUS LED CONN

PADS

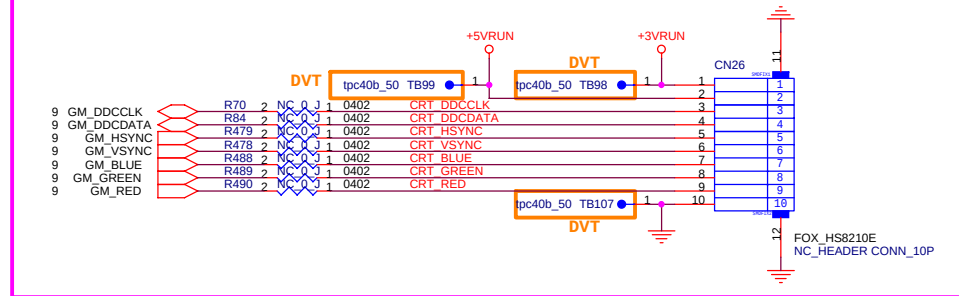


HOLES

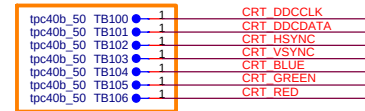


FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
Title			
HOLE			
Size	Document Number	Rev	
A3	M620-L	1.0	
Date:	Friday, June 08, 2007	Sheet	46 of 52

PVT



DVT



2006/12/15
P.6:Change C1631,1633,1637,1639,1644,1646 from 25V to 6.3V range
P.9:Add R1839 10K Ohm pull-down
P.9:Add R1841 100K Ohm pull-down
P.17:Add C1836-1841 dummy 10pF caps for EMI used
P.17:Modify LVDS power from G5841 to G5281 and delete L91
P.24:Exchange SPI ROM trace resistor R2411 for SDI and SDO
P.25:Exchange SPI ROM SDI and SDO trace
P.25:Dummy this page
P.26:Dummy ISA ROM and ISA Debug port
P.27:Add Power plane select function R632,636,637,2482 for customer request
P.29:Change CN28 symbol
P.30:Change R2491 from 1206 to 0603 size (sync to M630/640)
P.34:Change back USB Power from SUS power to ALW power
P.34:Update USB Vertical conn P/N
P.35:Add +3VALW power R2163 0R Ohm for customer request
P.35:Change back 1.8V to 2.5V power (follow vendor suggestion)
P.36:Change CN45 from HS8104E to HS8108E
P.36:Add R2504,2505 75R to GND for LAN Design rule
P.47:Update all HOLES and PADS
P.47:Change back Side-USB Power from SUS power to ALW power
P.48:Delete U74 and net:CSPDIF for customer request
P.48:Change CN46,48 connector type=normal open and delete R2197,R2200

2006/12/16
P.6:Delete R1994,L83-85,C1635,1641,1649 (By ICS FAE suggest)
P.9:Change R1471 and R1475 from 39R to 30R(follow Schematic check list V1.5)
P.20:Exchange GPIO24 and GPIO28 by S/W require
P.24:Move R1930 to P.20 and change 47K to 10K(follow Schematic check list V1.5)
P.24:Change GPIO pin by S/W require
P.31:Update CN14 P/N
P.32:Update CN32 P/N
P.41:Delete PR602 and Add GP1
P.41:Change PR601 package from 0603 to 0402
P.43:Change PR468 from 499R to 0R(Double same serial resistor with R1939)
P.47:Delete H16,17,22 and change H18-21 shape
P.48:Update CN50 symbol

2006/12/19
P.6:Delete PC29 (By Power require)
P.27:Add Q118,Q119,R2508,R2509 and Change +3VALW power to +3V_EMINI_AUX power (Follow customer require)
P.27:Delete Q117,R2499 and change R2498 from 470R to 68R (Follow Software Spec P.8)

2006/12/20
P.20:Change SW4 from HDS406E to HDS404E
P.20:Delete R2428,2429
P.24:Add SW3
P.24:Delete R2232
P.24:Delete R2237,2240,2431,2433 and Change Model ID to System ID
P.24:Change R2393,2239,2430,2432 from NC to 100K
P.25:Add RP54 for SYSTEM ID4-7
P.25:Delete R2481
P.26:Delete CN12 PIN29 (JIG_SMI#)
P.33:Update CN43 P/N
P.40:Update PQ55,56,57,58 Symbol
P.44:Update PQ18,53 Symbol
P.48:Change CN19 from SMD to DIP Type
P.48:Update CN50 part description
P.48:Add R2522,2523 and change CN50 AGND to GND (for customer require)

2006/12/21
P.24:Change GPIO signal: R2507 is connect from WLAN_EN# to HARD_RST#
P.24:Delete R2478 (Double Pull High)
P.24:Add R2481 for EC strap
P.24:Delete R1932 Pull-down resistor (HW_POP_MUTE_EC)
P.24:Change RP51 to R2526-2529 resistors
P.27:Change Q32 type with ESD protection
P.27:Change Q118 type (Change to meet SPEC)
P.27:Change NET:MINI_PCIE_+1_5V to MINI_PCIE_+1_5VRUN
P.27:Change MINI_PCIE_+3_3V to MINI_PCIE_+3_3VSUS
P.27:Add C1842 (Follow customer require)
P.39:Change PR622 connect Power from +5VALW to +ECVCC
P.39:Move B_PR2,B_PC5 and B_PD2 from ChargerBoard to MainBoard and rename to PR2526,PC1843 and PD29 (Follow customer require)
P.42:Change PR193 from 6.8K to 5.49K (For OCP setting)
P.42:Fix PU7 PGD signal=SUS_PWRGD (Orignal is missing trace)
P.43:Change PC464 P/N from 1C-2B20153-M000 to 1C-2B20153-K000 (BOM)
P.47:Fix error CN21 Pin-7 from MONITOR_OFF# to MONITOR_LED#
P.48:Change C1797,C1798 P/N from 1C-2B20153-M000 to 1C-2B20153-K000 (BOM)

2006/12/22
P.17:Add L91 for EMI require
P.20:Change SW4 from 4-DIP to 2-DIP SMD Switch
P.24:Delete SW5
P.33:Change CAP41 package (Power team require)
P.35:Add L92,93 for EMI require
P.36:Delete CN45 Pin9,10 net from GND_TR to NC
P.48:Add R2531 and R2532 for EMI require
P.48:Add EC49 and EC50 for EMI require
P.48:Add EC51 and EC52 for EMI require
P.48:Move P.47 EC35,EC48 to this page and connect to LINE_IN_L and LINE_IN_R
P.48:Move P.47 EC45,EC46 to this page and connect to EXTMIC_R_IN and EXTMIC_L_IN

2006/12/23
P.44:Add PR2527,PD55 in SUS_ON circuit (For power spec)
P.44:Add PR2528,PD56 in RUN_ON circuit (For power spec)

2006/12/25
P.20:Add net name:ICH_CLVREF0 and ICH_CLVREF1 for layout
P.29:L3 SWAP 1,4 and 2,3 (Layout issue)
P.38:Fix CN20 NPTH connect to GND issue
P.47:Update H10,H11 Hole symbol (ME modify)
P.48:Change EC35,45,46 and EC48 from 0.01uF to 0.001uF (Customer require)
P.48:C1834,C1835,R2483,2484,2485 and R2486 Dummy (Customer require same parts on the Audio board)

2006/12/26
P.25:Change DAT_35001,CLK_35001 net name to DAT_35001_R1,CLK_35001_R1
P.25:Delete TP612,TP620
P.25:Add R2533 and R2536 for 2nd clear button GPIO use and Add net DAT_35001_R2,CLK_35001_R2
P.46:Change PR496,PR498,PR500,PR501,PR506,PR35,PR532 to NC
P.46:Change PR526,PR529,PR530,PR531,PR533 from NC to mount
P.46:Change PR530,PR531,PR533,PR534 from 0R to 10K
P.47:Update H1,H2 footprint size (HOLE impact LVDS Connector issue)

2006/12/27
P.11:Replace R1848,R205 (missing)
P.19:Replace R2507 to +1.05V_PCIE (Missing)
P.19:Delete R1919,C1585 and net:HDA_CODEC_BITCLK (Double components)
P.20:Delete R1934,R1954,R1955,R2424 and exchange net to TP569,TP570,TP571,TP572 (EC change)
P.24:Delete this Page (For customer require)
P.25:Swap RP52 Pin3,4 net
P.25:Move SW4 and GP2 to EC side,And change pull-up power from +ECVCC to +3VRUN
P.25:Add R2506,R2507 for SYSTEM_ID
P.26:Delete SPI ROM and SPI Debug port circuit (For customer require)
P.48:Change CN51 Pin33 from GND to DCBATOUT (For customer new panel spec infomation)

2006/12/28
P.3:Change R1757 from 4.7K to 47K (EC change)
P.25:Change R2210,R2212 Pin-1 net from CLK/DAT_SMB to CLK/DAT_SMB_EC2
P.25:Change Q109 from +ECVCC to +5VALW
P.39:Change PD29,PR2526 and PC1843 to dummy
P.48:Swap CN51 Pin36,38 net (For layout)

2006/12/29
P.8:Delete TP584 (Layout issue)
P.25:R2103,R2104,R2534,R2535 Dummy and R2210,R2212,R2533,R2536 Mount (For Clear Button Interface)
P.47:Delete EC26

2007/02/03
Del P.24 (Winbond EC) page and add History for EVT2
P.19:Change net name TP_GPI034 to MB_FLASH_EN
P.20:Change net name MB_FLASH_EN to TP375
P.20 and P.48:Rename GPIO20 from AEC_PWRDN# to AEC_RESET#
P.20:Del TP596 and rename GPIO24 to AEC_PWRDN#
P.25:Add R2537,R2538 pull-down for EC strap
P.25:Del TP621
P.26:Change LED 2 type (Customer require)
P.39:Add PL17 and PL18 (Power issue)
P.39:Add PC1847,PC1848 and PC1849 (Power issue)
P.40:Change PR627 from 0R to 3.3R (Power issue)
P.40:Change PR601 from 604K to 300K (Power issue)
P.42:Change PR485 from 3.3K to 3.9K (Power issue)
P.43:Add PC1844,PC1845 and PC1846 (Power issue)
P.43:Change PR615.1(+5V_S3_SUS) to (+3V_S3_SUS)
P.45:Change PR526,PR611,PR499 and PR34 to NC
P.47:Del GP24 and add C1843,C1844 (For EMI issue)
P.47:Del GP25 and add C1845,C1846 (For EMI issue)
P.48:Rename RUN_PWRGD to AEC_PWRDN#

2007/02/07
P.42:Add TP634~TP637 for Power test use
P.47:Add EC53~EC68 for EMI require
P.47:Change EC17 and EC19 from DCBEADP+IN to DCBATOUT

2007/02/08
P:47:Change CN49 Pin7,8 from A_GND to GND (Customer require)

2007/02/09
P.28:Change CN4 type from HS8204E to HS8104E
P.29:Add PJ37-42 open jumper for EMI require
P.46:Change CN21 type from HS8208E to HS8108E
P.46:Change PAD3,4 type and add PAD6,7,9,10 for ME require
P.46:Change H3,H4,H6,H11 type and add H29 for ME require

2007/02/26
P.39:Change PC139,PC159,PC160,PC341,PC346,PC347 from NC to mount
P.39:Change PC147 from 330uF to 150uF
P.40:Change PR627 from 0R to 3.3R
P.40:Change PR601 from 604K to 300K
P.41:Change PC343,PC351,PC352 from NC to mount
P.42:Change PR485 from 3.3K to 3.9K
P.42:Change PC7,PC107,PC344,PC345,PC353,PC354,PC355,PC356 from NC to mount

2007/02/28
P.5:Change CAP25 P/N (substitute materiel)
P.11:Change D22,L58,L66,L75,L76,CAP26,CAP28,CAP31 P/N (substitute materiel)
P.12:Change CAP34,CAP36 P/N (substitute materiel)
P.19:Change D24 P/N (substitute materiel)
P.20:Change R2443 from 0R to 10K (Intel spec)
P.21:Change D25,D26,CAP38 P/N (substitute materiel)
P.29:Change L55,L56 P/N (substitute materiel)
P.33:Change CAP19,CAP20,CAP22 P/N (substitute materiel)
P.35:Change U67 P/N (substitute materiel)
P.38:Change PL11,PL14,PL15,PL16 P/N (substitute materiel)
P.39:Change PL17,PL18 P/N (substitute materiel)
P.40:Change PC23,PC589,PC574,PC576,PC577 P/N (substitute materiel)
P.41:Change PC144,PC148 P/N (substitute materiel)
P.43:Change PC1844,PC1845,PC1846 P/N (substitute materiel)
P.45:Change PC523,PC524 P/N (substitute materiel)
P.47:Change U75,L87,L88 P/N (substitute materiel)

2007/03/08
P.3:Change Q3 P/N (Buyer require)
P.6:Update U33 symbol from ICS9LPR358YGLFT to ICS9LPR358AGLFT
P.17:Change CN3 type for cost down
P.24:Change R2538 from 47K to 100K
P.27:Swap U27(G781),U68(G781-1) for S/W require
P.28:Change CN27,CN28 form normal type to reverse type (Customer require)
P.28:Change R2409 to NC and change R2410 to mount (Follow M6340)
P.28:Add TB94,TB95,TB96 (For BFT)
P.28:Mirror vertical L4,L5 (For layout require)
P.29:Change Q47 P/N (Buyer require)
P.32:Change CN43,CN44 form normal type to reverse type (Customer require)
P.33:Change U70,U71,U72 package (EUV spec require)
P.39:Dummy PL17,PL18 (Cost down)
P.43:Dummy PR454,PQ88

2007/03/13
P.6:Modify R2022.1 connection from AEC_CLK14 to R_CLK_ICH14
Page:All:Add Test point for BFT

2007/03/16
P.24:Change RP52 from 10K to 4.7K (To meet S/W spec)
P.24:Swap SMB-1 and SMB-2 signals
P.28:Change R152,R154,R136,R137,R482,R449,R105,R90 from NC to mount
P.28:Change L3,L4,L5,L9 from mount to NC
P.32:Change back CN44 symbol (ME turn 180drgee)
P.34:Del L92,L93 and change to R92,R93

2007/03/20
P.2:Update Block Diagram
P.24:Change R519,R521,R2445,R2446 from 10K to 4.7K (To meet S/W spec)

2007/03/22
P.39:Change PR192,PR198 from 0R to 3.3R (For EMI issue)
P.41:Change PR195 from 0R to 3.3R (For EMI issue)
P.42:Change PR456,PR466 from 0R to 3.3R (For EMI issue)
P.42:Add TB62.TB63 (Power request)
P.42:Change TT20,TT21,TT22,TT23,TT24,TT25,TT26 to TB40,TB41,TB42,TB43,TB44,TB45,TB46 (Power request)
P.43:Add TB23,TB24,TB25,TB26,TB27,TB36,TB37 (Power request)
P.44:Change TP:TT45,TT46,TT57,TT16,TT17,TT18,TT19,TT44,TT43,TT42,TT32,TT41 to TB38,TB39,TB65,TB66,TB67,TB68,TB69,TB81,TB83,TB47,TB49,TB50,TB48 (For BFT test)
P.46:Add EC43,EC69-74,EC78-82,EC84-86 for decrease noise
P.47:Change R2531,R2532,R2198,R2199 from 0R resistor to 120R-100MHz bead (EMI Request)
P.47:Change EC49,EC50,EC51,EC52 from NC to Mount(EMI Request)

2007/03/23
P.17:Change back CN3 connector type to EVT used
P.23:Add C674 (EMI Request)
P.41:Change PC166,PC170 from NC to mount (EMI Request)
P.42:Add bead PL19,PL20 (EMI Request)
P.46:Add cap C1747 (EMI Request)
P.46:Add cap EC6,EC7 (EMI Request)

2007/03/26
P.8:Add C1453 (For power test fail)
P.19:Change R1918 from NC.47R to 0R (EMI Request)
P.19:Change C1584 from NC to mount (EMI Request)
P.24:Correct SMBUS Defination
P.28:Change R2253 from NC.47R to 0R (EMI Request)
P.28:Change C1818 from NC to mount (EMI Request)
P.32:Change CN43 type (ME new tooling)
P.38:Move PF1 from right side to left side of PL11 and PL15
P.43:Change PR448,PR636,PQ88,PQ95 from NC to mount (For discharge too slow)
P.46:Add PAD11,PAD12,PAD13 (RF Request)
P.46:Change all TestPoint from 30mils to 40mils (For BFT test)
P.47:Change CN50 type (ME new tooling)

2007/03/27
P.11:Del L66,L67,L70,L73,C1517,C1518,C1520,C1527,R2419 (Intel Layout Guide V2.0)
P.11:Modify VCCA_TVA/B/C_DAC1/2 circuit (Intel Layout Guide V2.0)
P.19:Change BAT1 TestPoint type to 40mils
P.23:Change CN5 TestPoint type to 40mils
P.26:Change WOL function form S5 to S3 status
P.27:Change CN2 TestPoint type to 40mils
P.28:Change CN35 TestPoint type to 40mils
P.28:Change CN4 TestPoint type to 40mils
P.28:Update CN52 connector
P.28:Stuff R2253,C1818 (For EMI request)
P.35:Change CN45 TestPoint type to 40mils
P.38:Change PCN1 TestPoint type to 40mils
P.40:Add RUN_ON net and PR580 for power sequency
P.40:Change PR579 from stuff to NC (For can't boot from ext debug board issue)
P.47:Change CN18,CN19 TestPoint type to 40mils
P.48:Change CN26 TestPoint type to 40mils

2007/03/29
P.20:Change R2494 from 4.7K to 1K (Follow M6340)
P.20:Change R2440 from 4.7K to 1K (Follow M6340)
P.24:Add TestPoint for BFT test
P.24:Change C30,C33 from 10pF to 12pF (Vendor suggest)
P.37:Add TestPoint for BFT test

2007/03/30
P.21:Change L79 from 10uH choke to 330R bead (Follow intel schematic)

2007/03/31
P.40 Add PC600 for power leakage issue (Default is NC)
P.40 Add PD26 for power leakage issue (Default is NC)

2007/04/02
P.08:Add R1803 to isolate PM_THRMTRIP#_R side (Intel sighting report #30678)
P.19:Add R1910 for reserve disable ThermalTrip function
P.24:Add R415,R416,R417,R418 for FAN PWM layout path select
P.27:Add R411,R412,R413,R414 for FAN TACH layout path select
P.41:NC PC154 (Power reserved)

2007/04/03
P.42:Change PC472 type for cost and common parts
P.47:Add R2530,R2534 for ground path select (Customer request and default is connect to A_GND)

2007/04/04
P.8:Change R1803 from NC to stuff
P.42:Change PC594,PC595 P/N from +/-10% to +/-5%

2007/04/18
P.26:Change LED2 color from Green to Yellow Green
P.39:Change PR78,PR82 from 68K to 82K (3/5V power limit up)
P.42:Dummy PC110,PC3 and mount PC21,PC88 (Power request)
P.43:Change PC1844,PC1845.PC1846 from 220uF/2.5V to 150uF/6.3V (Spec error)
P.47:Change CN50 type from high-speed to low-speed (Customer request)

2007/05/04
P.11:

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
File		CPBG - R&D Division	
Size		History (PVT)	
C	Document Number	M620-L	Rev 1.0
Date	Monday, June 25, 2007	Sheet 52 of 52	