PEGATRON CONFIDENTIAL

MODEL NAME :

PCB NO :

69- P/N :

AIC70 Schematic

Intel Arrandale rPGA-989
PCH BGA 1071

2011-05-04

REV : R2.0

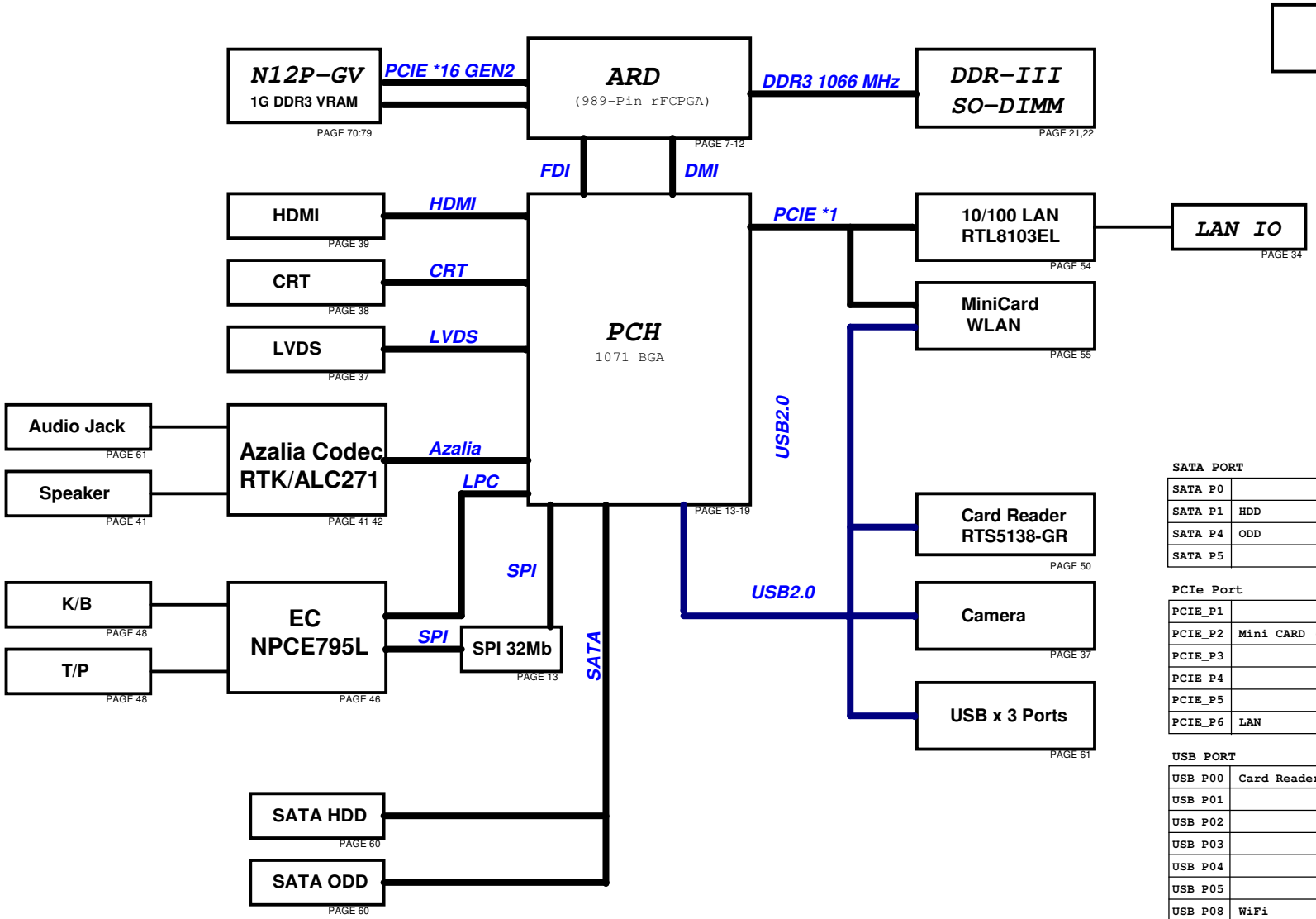
PEGATRON Title : Cover Page

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 1 of 77

AIC70 BLOCK DIAGRAM



POWER

CPU VCORE PAGE 80
SYSTEM, +3V, +5V PAGE 81
+VCCP PAGE 82
DDR & VTT PAGE 83
+VGFX_CORE PAGE 86
+VGA_CORE PAGE 87
SMART CHARGER PAGE 88
POWER DETECT PAGE 90
LOAD SWITCH PAGE 91
POWER PROTECT PAGE 92

SATA PORT

SATA P0	
SATA P1	HDD
SATA P4	ODD
SATA P5	

PCIe Port

PCIE_P1	
PCIE_P2	Mini CARD (WLAN)
PCIE_P3	
PCIE_P4	
PCIE_P5	
PCIE_P6	LAN

USB PORT

USB P00	Card Reader
USB P01	
USB P02	
USB P03	
USB P04	
USB P05	
USB P08	WiFi
USB P09	
USB P10	Camera
USB P11	External
USB P12	External
USB P13	External

Power Rails

Sleep State	RTC	VA	VSUS	V	VS
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4	ON	ON	ON	OFF	OFF
S5/ AC	ON	ON	ON	OFF	OFF
S5/ DC	ON	ON	OFF	OFF	OFF

PEGATRON Title : BLOCK DIAGRAM

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 2 of 77

SCHEMATIC INDEX V1.2

PAGE#	Description	NOTE
01	Cover Page	
02	Block Diagram	
03	PAGE INDEX	
07-12	CPU	
13-19	PCH	
21-22	DDR3 SO-DIMM	
24	Clock Generator	
33-34	LAN	
37	LVDS CON	
38	RGB CON	
39	HDMI (Level shift for UMA)	
41-42	AUDIO CODEC & De-POP	
46-48	EC NPCE795L / KB / TP	
49	THERMAL / FAN	
50	CARD READER	
55	MINI CARD -WiFi & BT3.0	
60	SATA(HDD & ODD)	
61	USB & AUDIO CONN	
63	DC-IN / BATTERY CONN / Discharge	
65	PWR CONN & Debug CONN	
66	Led & Nut & ME Pad	
70-79	dGPU Schematics	
80-94	Power Schematics	
95	EE History	
96	ODD Board	
97	PWR Board	
98	TP SW Board & LID Switch	
99	AUDIO Board	

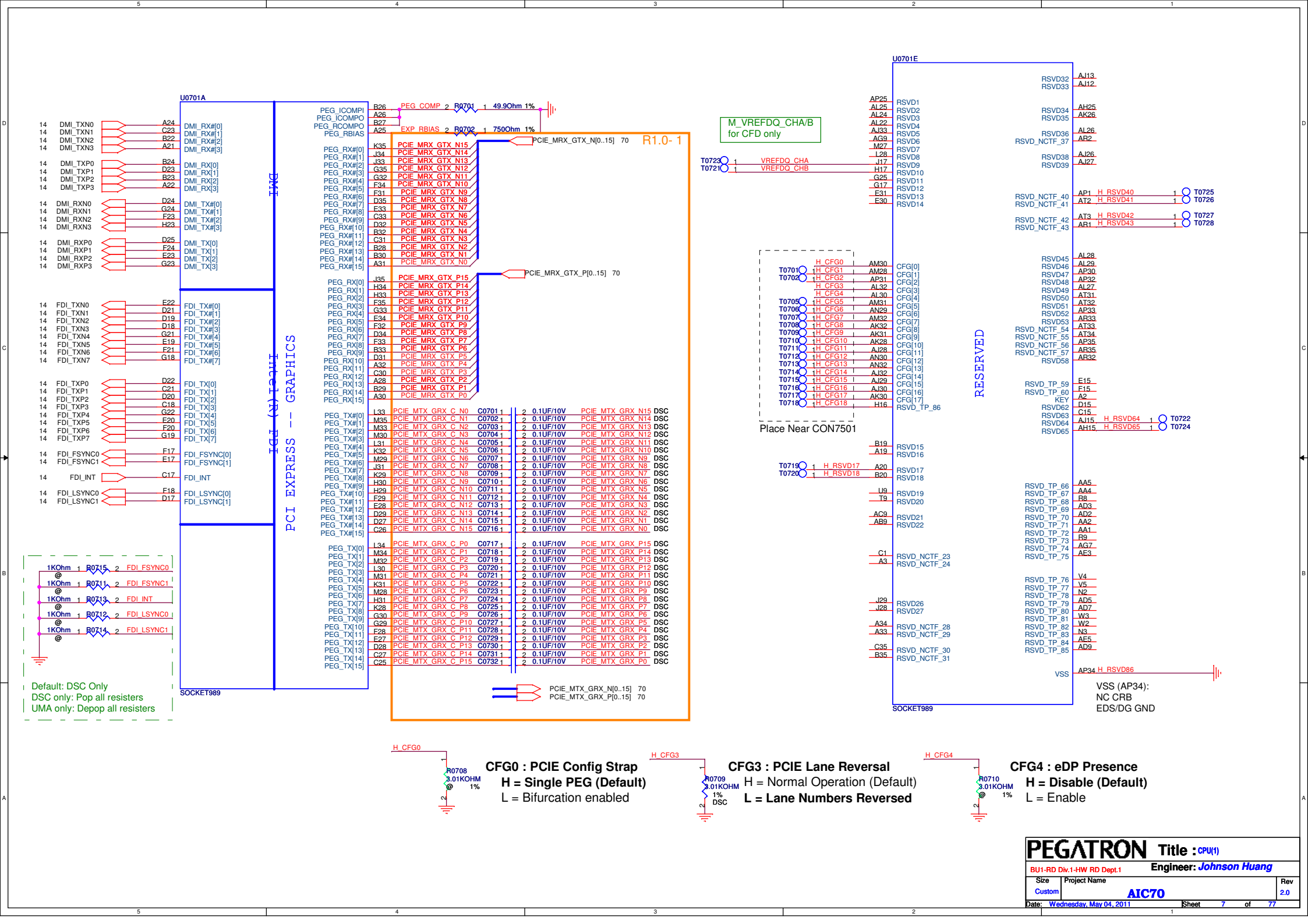
PAGE#	Description	NOTE

PEGATRON Title : PAGE INDEX

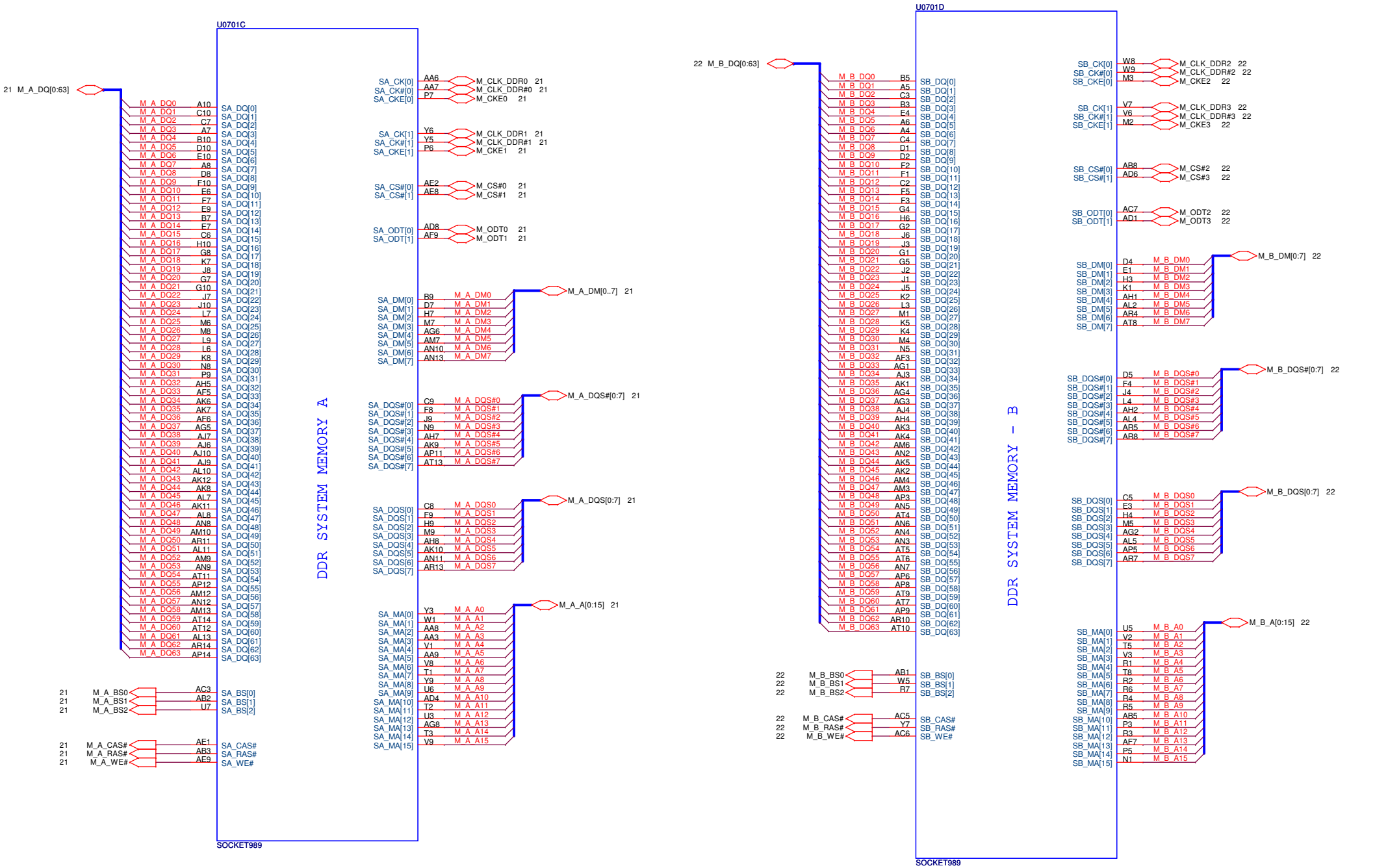
BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 3 of 77



PEGATRON	Title : CPU(1)		
BU1-RD Div.1-HW RD Dept.1	Engineer: Johnson Huang		
Size: Custom	Project Name: AIC70		Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 7 of 77		

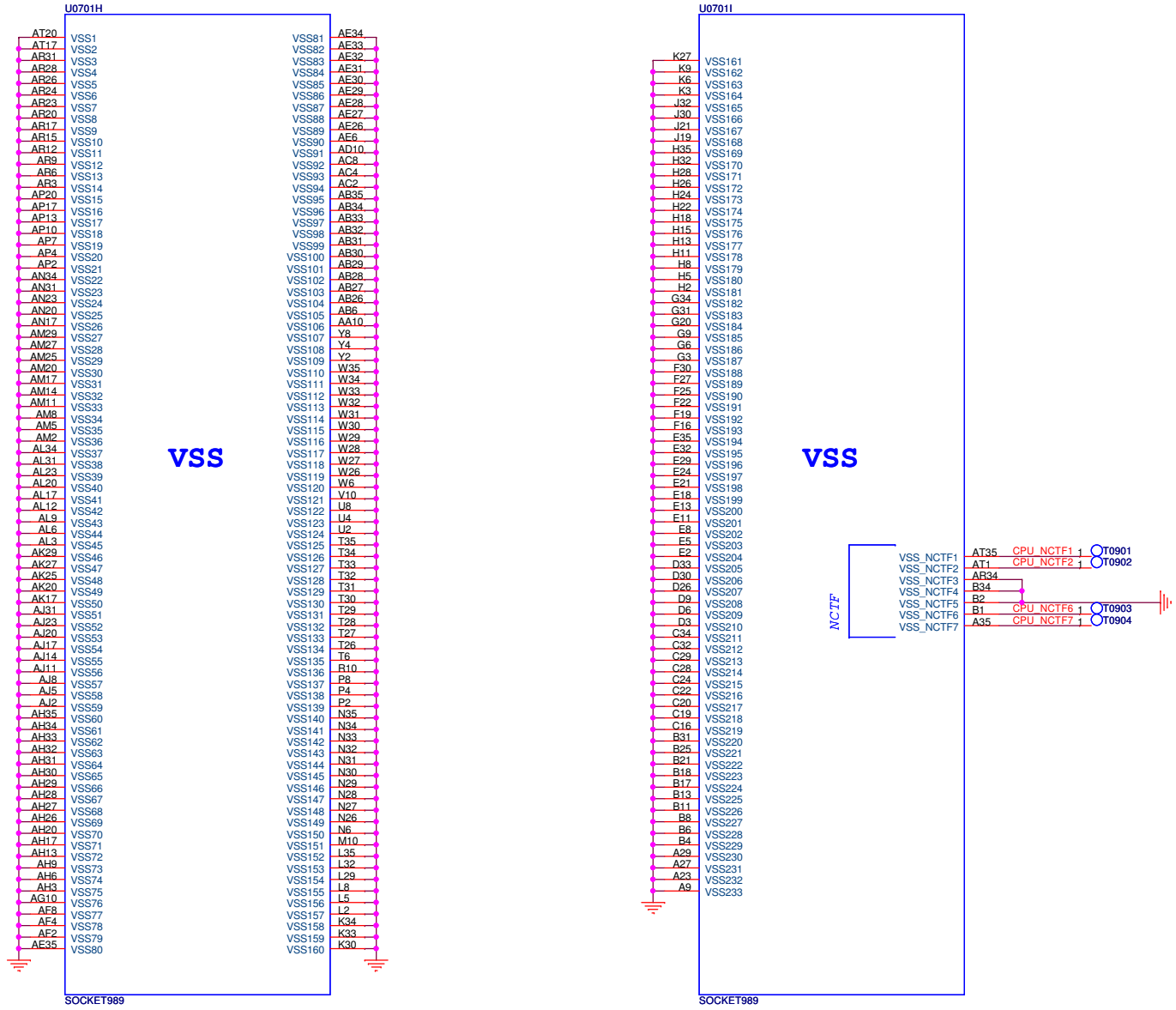


PEGATRON Title : CPU CLK/MISC/JTAG

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 8 of 77

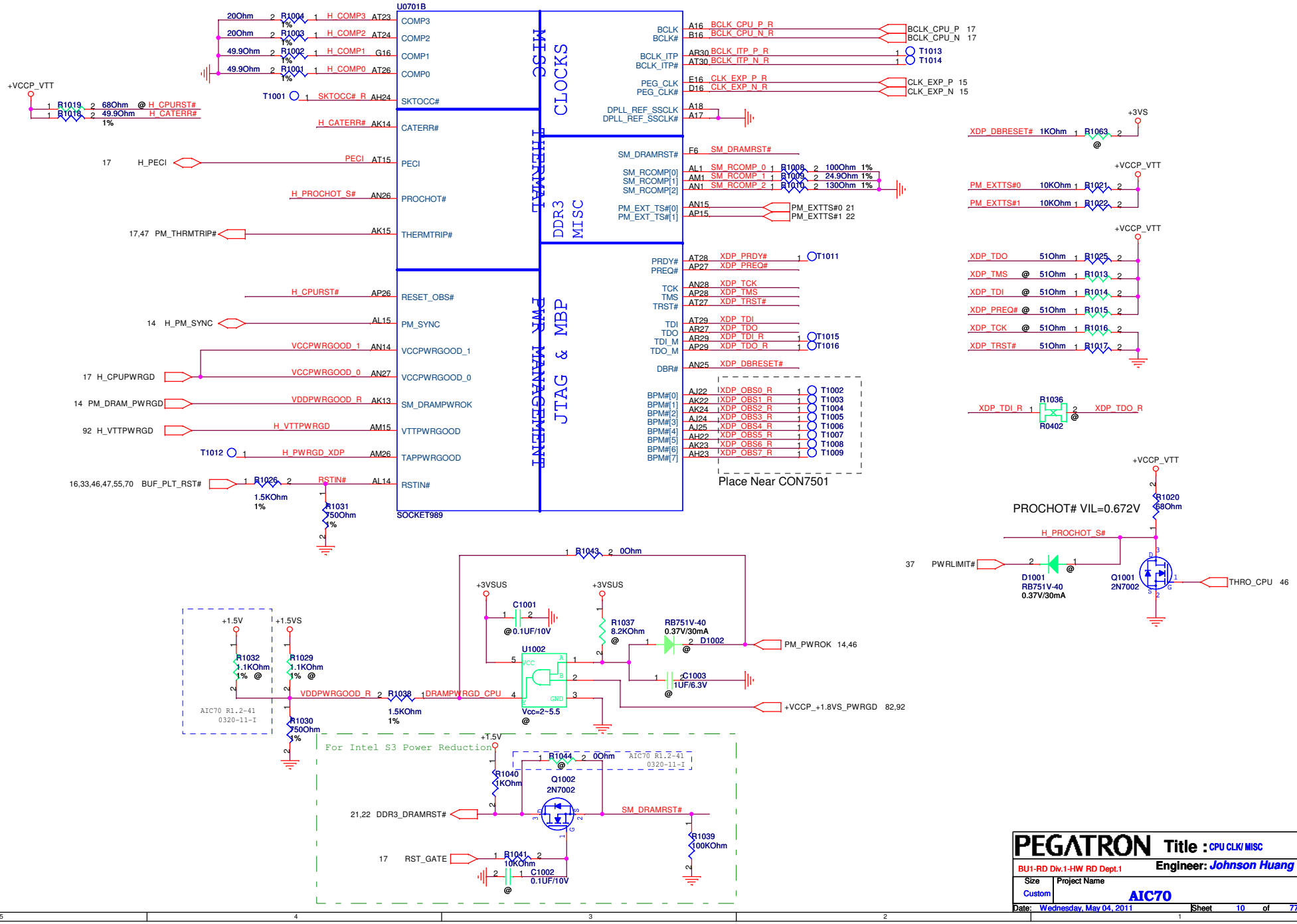


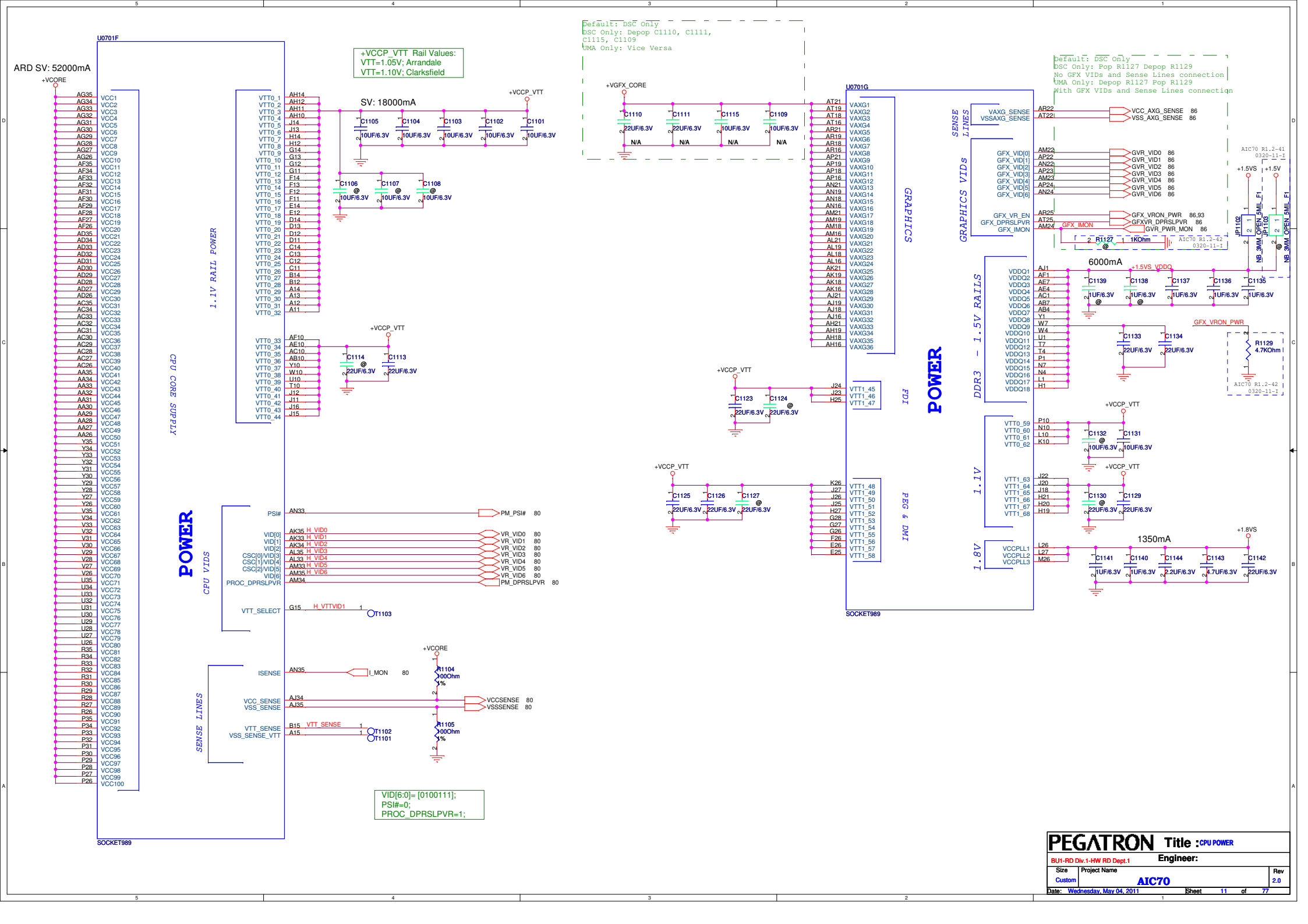
PEGATRON Title : CPU GND

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

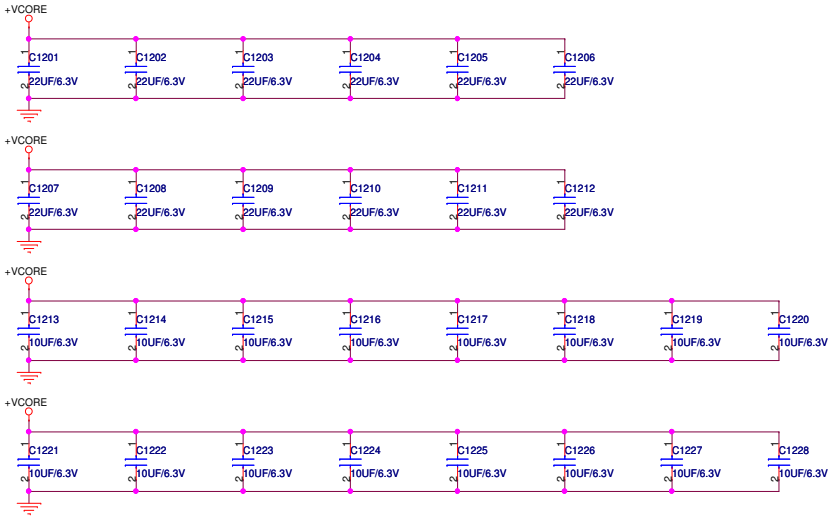
Date: Wednesday, May 04, 2011 Sheet 9 of 77


U0701B
SOCKET989
MISC CLOCKS
THERMAL DDR3 MISC
PWR MANAGEMENT JTAG & MBP
COMP3
COMP2
COMP1
COMP0
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
RESET_OBS#
PM_SYNC
VCCPWRGOOD_1
VCCPWRGOOD_0
SM_DRAMPWROK
VTTPWRGOOD
TAPPWRGOOD
RSTIN#
BCLK
BCLK#
BCLK_ITP
BCLK_ITP#
PEG_CLK
PEG_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
PM_EXT_TS#[0]
PM_EXT_TS#[1]
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
TDI_M
TDO_M
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]
Place Near CON7501
PROCHOT# VIL=0.672V
For Intel S3 Power Reduction
PEGATRON
Title : CPU CLK/ MISC
Engineer: Johnson Huang
BU1-RD Div.1-HW RD Dept.1
Size: Custom
Project Name: AIC70
Rev: 2.0
Date: Wednesday, May 04, 2011
Sheet 10 of 77


U0701F
ARD SV: 52000mA
+VCORE
+VCCP_VTT Rail Values:
VTT=1.05V; Arrandale
VTT=1.10V; Clarksfield
SV: 18000mA
1.1V RAIL POWER
CPU CORE SPLIT
POWER
CPU VIDS
SENSE LINES
PSI#
VID[0]
VID[1]
VID[2]
CSC[0]VID[3]
CSC[1]VID[4]
CSC[2]VID[5]
VID[6]
PROC_DPRSLPVR
VTT_SELECT
ISENSE
VCC_SENSE
VSS_SENSE
VTT_SENSE
VSS_SENSE_VTT
VID[6:0]= [0100111];
PSI#=0;
PROC_DPRSLPVR=1;
SOCKET989
Default: DSC Only
DSC Only: Depop C1110, C1111, C1115, C1109
UMA Only: Vice Versa
+VGFX_CORE
U0701G
GRAPHICS
FDI
PEG & DMI
POWER
DDR3 - 1.5V RAILS
1.1V
1.8V
SENSE LINES
GRAPHICS VIDs
Default: DSC Only
DSC Only: Pop R1127 Depop R1129
No GFX VIDs and Sense Lines connection
UMA Only: Depop R1127 Pop R1129
With GFX VIDs and Sense Lines connection
6000mA
1350mA
+1.5VS_VDDQ
GFX_VRON_PWR
PEGATRON
Title : CPU POWER
BU1-RD Div.1-HW RD Dept.1
Engineer:
Size: Custom
Project Name: AIC70
Rev: 2.0
Date: Wednesday, May 04, 2011
Sheet 11 of 77

Decoupling guide from INTEL

VCORE	10uF	x 16pcs
	22uF	x 12pcs

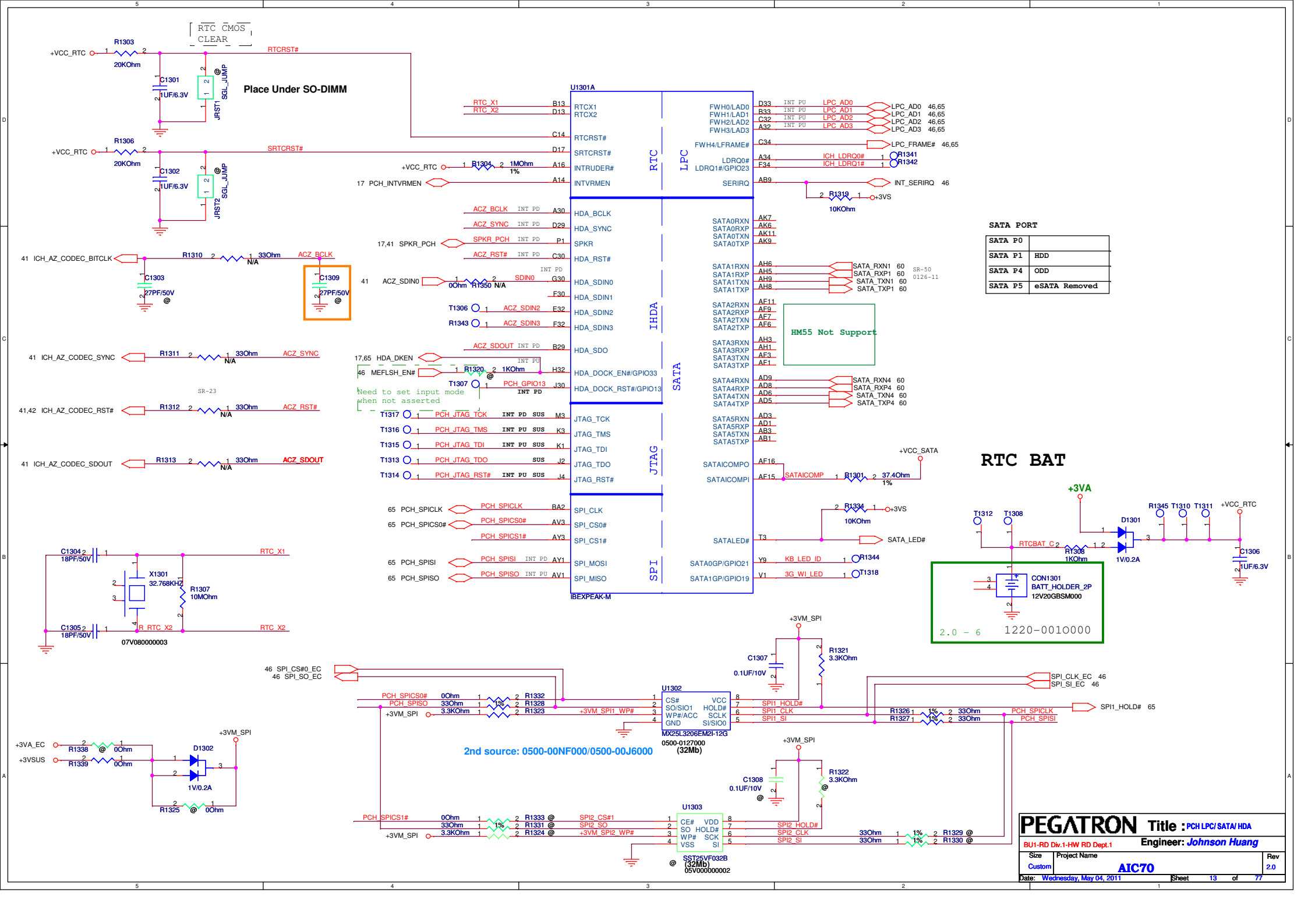


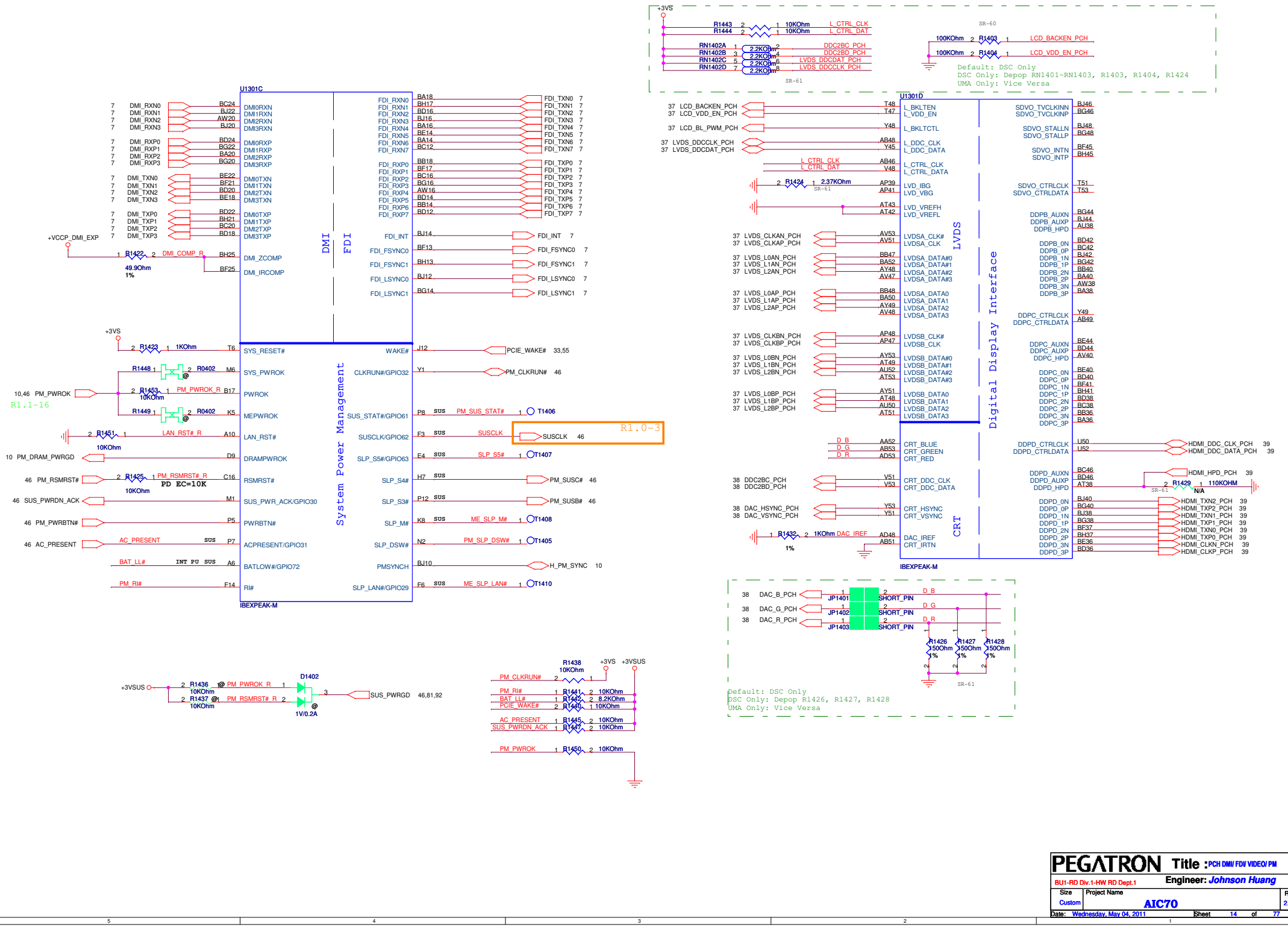
PEGATRON Title : CPU CAPS

BU1-RD Div.1-HW RD Dept.1 Engineer:

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 12 of 77


RTC CMOS CLEAR
Place Under SO-DIMM
U1301A
RTC
LPC
IHDA
SATA
JTAG
SPI
IBEXPEAK-M
HM55 Not Support
SATA PORT
SATA P0
SATA P1 HDD
SATA P4 ODD
SATA P5 eSATA Removed
RTC BAT
CON1301 BATT_HOLDER_2P 12V20GBSM000
2.0 - 6 1220-0010000
2nd source: 0500-00NF000/0500-00J6000
MX25L3206EM2I-12G
0500-0127000
(32Mb)
SST25VF032B
(32Mb)
05V000000002
PEGATRON
Title : PCH LPC/ SATA/ HDA
BU1-RD Div.1-HW RD Dept.1
Engineer: Johnson Huang
Size Custom
Project Name AIC70
Rev 2.0
Date: Wednesday, May 04, 2011
Sheet 13 of 77


U1301C
DMI
FDI
System Power Management
IBEXPEAK-M
U1301D
LVDS
Digital Display Interface
CRT
IBEXPEAK-M
SR-60
SR-61
Default: DSC Only
DSC Only: Depop RN1401~RN1403, R1403, R1404, R1424
UMA Only: Vice Versa
Default: DSC Only
DSC Only: Depop R1426, R1427, R1428
UMA Only: Vice Versa
R1.1-16
R1.0-3
PEGATRON
Title : PCH DMI/ FDI/ VIDEO/ PM
BU1-RD Div.1-HW RD Dept.1
Engineer: Johnson Huang
Size: Custom
Project Name: AIC70
Rev: 2.0
Date: Wednesday, May 04, 2011
Sheet 14 of 77

PCIE 1	
PCIE 2	Mini CARD (WLAN)
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	LAN

U1301B

IBEXPEAK-M

PCI-E* / SMBus / G-Link / PEG / CLK BUFFER / Clock Inputs from CLK / Clock Flex

HM55 Not Support

PU +3VSUS at CON5501

PU EC

Damping CPU Side

Plamrest Thermal

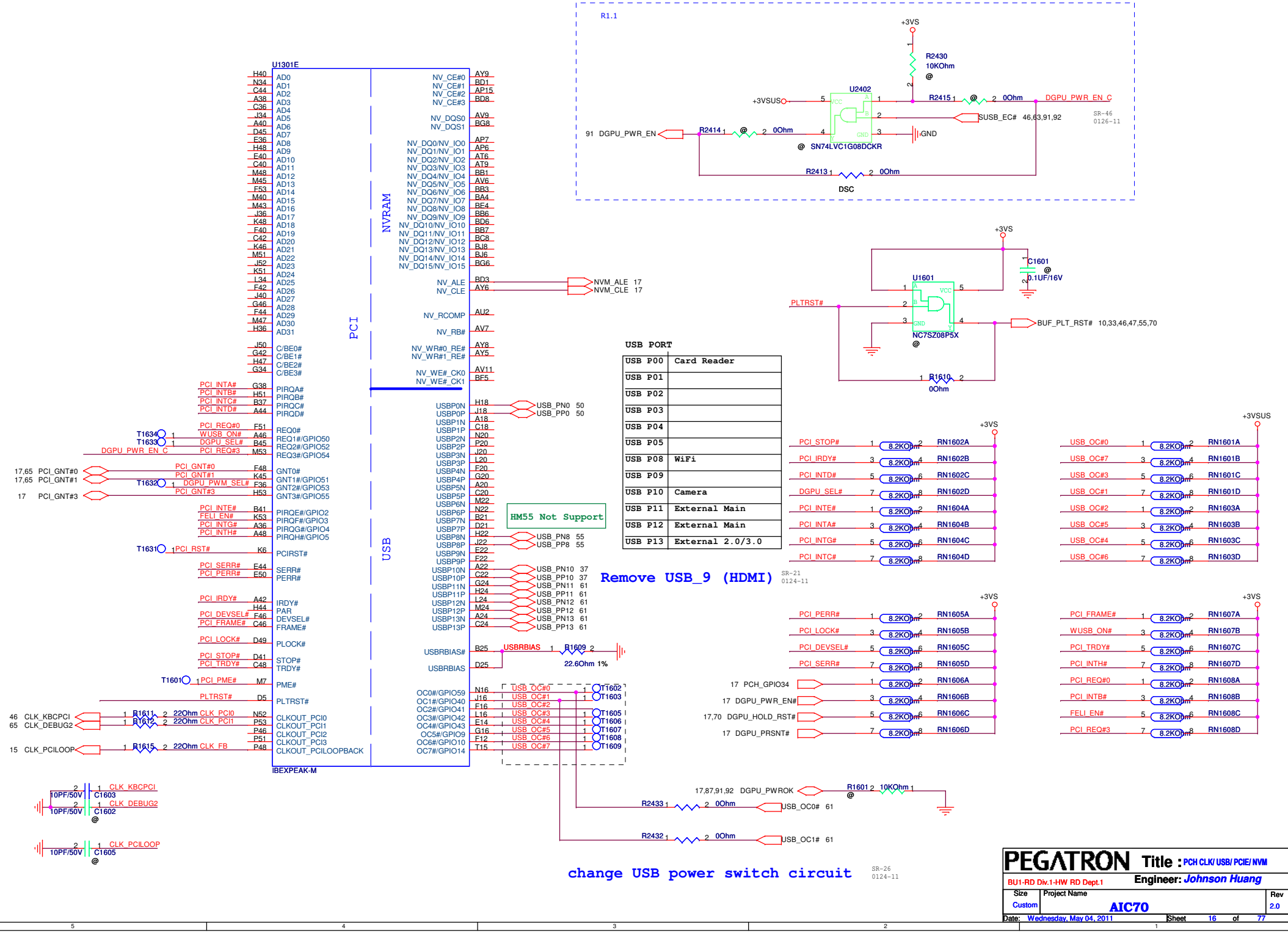
For UMA
Change to 10PF

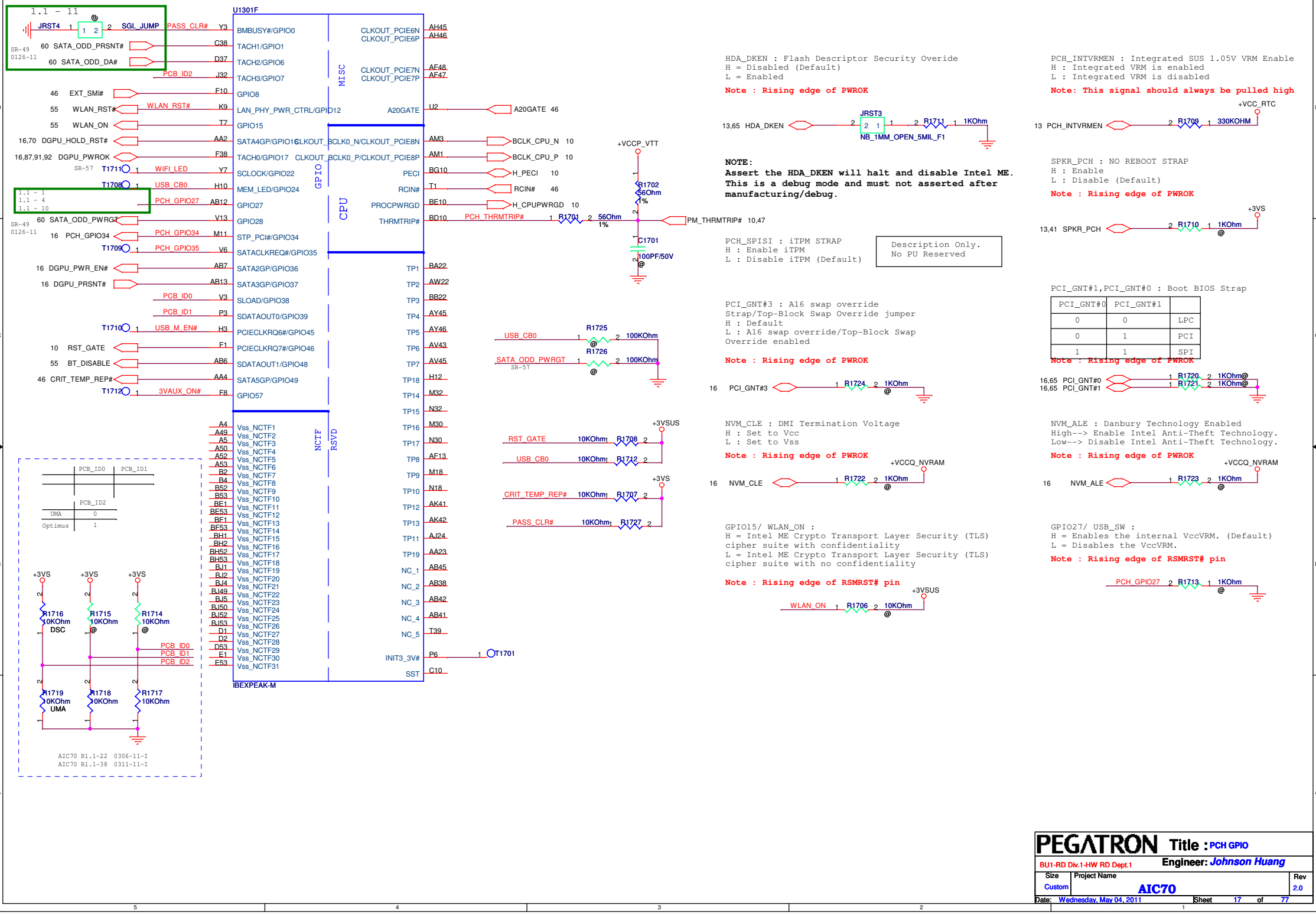
PEGATRON Title : PCH CLK/ USB/ PCIE/ NVM

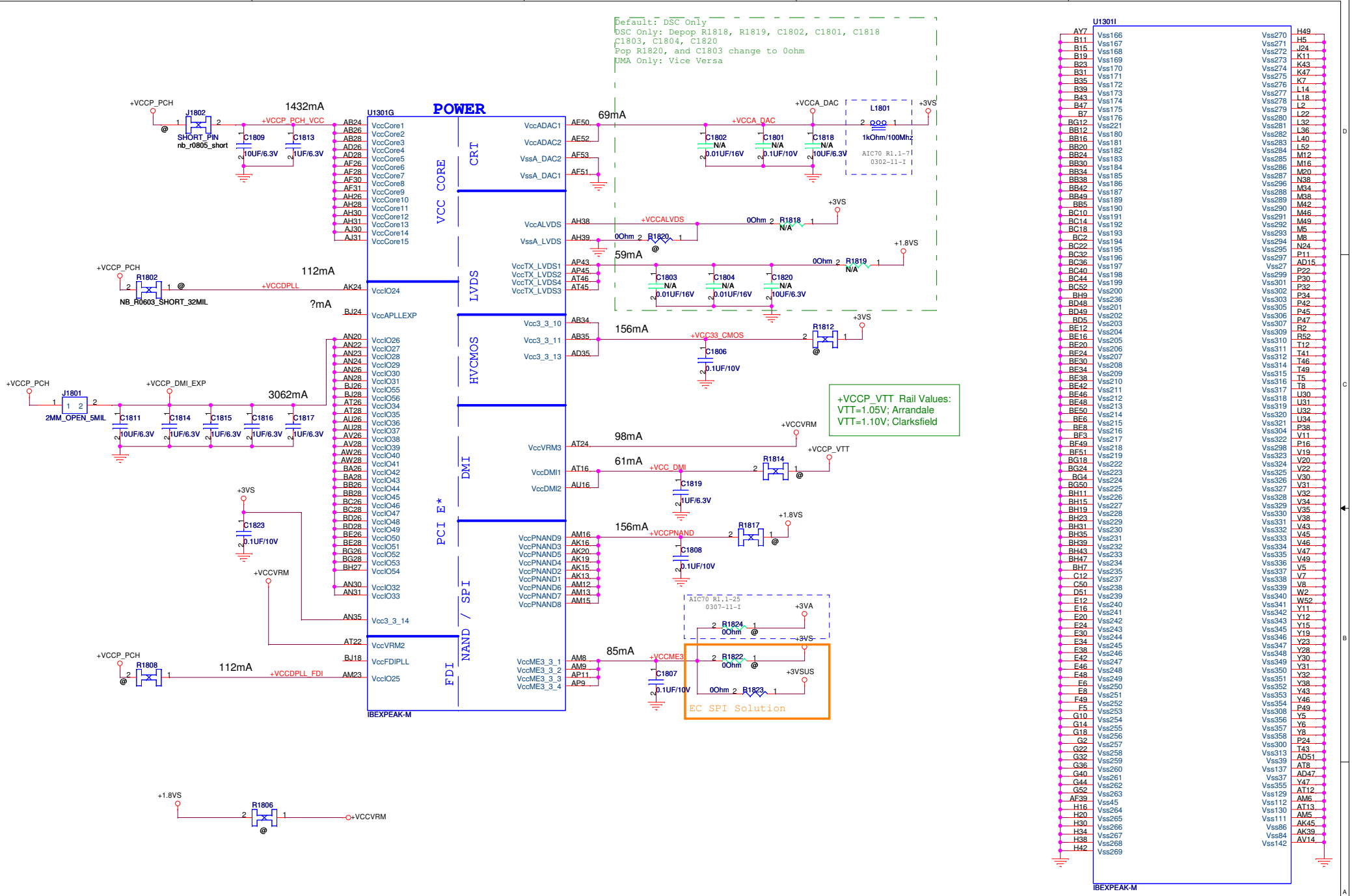
BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 15 of 77


R1.1
+3VS
R2430
10KOhm
@
U2402
+3VSUS
R2415 1 @ 2 0Ohm
DGPU_PWR_EN_C
SUSB_EC# 46,63,91,92
SR-46
0126-11
91 DGPU_PWR_EN
R2414 1 @ 2 0Ohm
GND
@ SN74LVC1G08DCKR
R2413 1 2 0Ohm
DSC
U1301E
NVRAM
PCI
USB
IBEXPEAK-M
NV_ALE 17
NVM_CLE 17
USB_PN0 50
USB_PP0 50
USB_PN8 55
USB_PP8 55
USB_PN10 37
USB_PP10 37
USB_PN11 61
USB_PP11 61
USB_PN12 61
USB_PP12 61
USB_PN13 61
USB_PP13 61
USBRBIAS
R1609 2
22.6Ohm 1%
USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
T1602
T1603
T1605
T1606
T1607
T1608
T1609
HM55 Not Support
USB PORT
USB P00 Card Reader
USB P01
USB P02
USB P03
USB P04
USB P05
USB P08 WiFi
USB P09
USB P10 Camera
USB P11 External Main
USB P12 External Main
USB P13 External 2.0/3.0
Remove USB_9 (HDMI)
SR-21
0124-11
change USB power switch circuit
SR-26
0124-11
C1601
@
0.1UF/16V
U1601
NC7SZ08P5X
PLTRST#
BUF_PLT_RST# 10,33,46,47,55,70
R1610 1 2
0Ohm
RN1602A
RN1602B
RN1602C
RN1602D
RN1604A
RN1604B
RN1604C
RN1604D
RN1601A
RN1601B
RN1601C
RN1601D
RN1603A
RN1603B
RN1603C
RN1603D
RN1605A
RN1605B
RN1605C
RN1605D
RN1606A
RN1606B
RN1606C
RN1606D
RN1607A
RN1607B
RN1607C
RN1607D
RN1608A
RN1608B
RN1608C
RN1608D
8.2KOhm
17,87,91,92 DGPU_PWROK
R1601 2 10KOhm 1
@
R2433 1 2 0Ohm
USB_OC0# 61
R2432 1 2 0Ohm
USB_OC1# 61
C1603
C1602
C1605
10PF/50V
@
PEGATRON
Title : PCH CLK/ USB/ PCIE/ NVM
BU1-RD Div.1-HW RD Dept.1
Engineer: Johnson Huang
Size Custom
Project Name AIC70
Rev 2.0
Date: Wednesday, May 04, 2011
Sheet 16 of 77


U1301F
IBEXPEAK-M
BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
MEM_LED/GPIO24
GPIO27
GPIO28
STP_PCI#/GPIO34
SATACLKREQ#/GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57
MISC
GPIO
CPU
NCTF
RSVD
CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
A20GATE
CLKOUT_BCLK0_N/CLKOUT_PCIE8N
CLKOUT_BCLK0_P/CLKOUT_PCIE8P
PECI
RCIN#
PROCPWRGD
THRMTRIP#
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP18
TP14
TP15
TP16
TP17
TP8
TP9
TP10
TP12
TP13
TP11
TP19
NC_1
NC_2
NC_3
NC_4
NC_5
INIT3_3V#
SST
Vss_NCTF1
Vss_NCTF2
Vss_NCTF3
Vss_NCTF4
Vss_NCTF5
Vss_NCTF6
Vss_NCTF7
Vss_NCTF8
Vss_NCTF9
Vss_NCTF10
Vss_NCTF11
Vss_NCTF12
Vss_NCTF13
Vss_NCTF14
Vss_NCTF15
Vss_NCTF16
Vss_NCTF17
Vss_NCTF18
Vss_NCTF19
Vss_NCTF20
Vss_NCTF21
Vss_NCTF22
Vss_NCTF23
Vss_NCTF24
Vss_NCTF25
Vss_NCTF26
Vss_NCTF27
Vss_NCTF28
Vss_NCTF29
Vss_NCTF30
Vss_NCTF31
JRST4
SGL_JUMP
PASS_CLR#
SATA_ODD_PRSNT#
SATA_ODD_DA#
PCB_ID2
EXT_SMI#
WLAN_RST#
WLAN_ON
DGPU_HOLD_RST#
DGPU_PWROK
WIFI_LED
USB_CB0
PCH_GPIO27
SATA_ODD_PWRGT
PCH_GPIO34
PCH_GPIO35
DGPU_PWR_EN#
DGPU_PRSNT#
PCB_ID0
PCB_ID1
USB_M_EN#
RST_GATE
BT_DISABLE
CRIT_TEMP_REP#
3VAUX_ON#
BCLK_CPU_N
BCLK_CPU_P
H_PECI
RCIN#
H_CPUPWRGD
PCH_THRMTRIP#
PM_THRMTRIP# 10,47
+VCCP_VTT
R1702 56Ohm 1%
C1701 100PF/50V
R1701 56Ohm 1%
R1725 100KOhm
R1726 100KOhm
R1708 10KOhm
R1712 10KOhm
R1707 10KOhm
R1727 10KOhm
+3VSUS
+3VS
PCB_ID0
PCB_ID1
PCB_ID2
UMA
Optimus
R1716 10KOhm DSC
R1715 10KOhm @
R1714 10KOhm @
R1719 10KOhm UMA
R1718 10KOhm
R1717 10KOhm
AIC70 R1.1-22 0306-11-I
AIC70 R1.1-38 0311-11-I
HDA_DKEN : Flash Descriptor Security Overide
H = Disabled (Default)
L = Enabled
Note : Rising edge of PWROK
13,65 HDA_DKEN
JRST3
R1711 1KOhm
NB_1MM_OPEN_5MIL_F1
NOTE:
Assert the HDA_DKEN will halt and disable Intel ME. This is a debug mode and must not asserted after manufacturing/debug.
PCH_SPISI : iTPM STRAP
H : Enable iTPM
L : Disable iTPM (Default)
Description Only.
No PU Reserved
PCI_GNT#3 : A16 swap override
Strap/Top-Block Swap Override jumper
H : Default
L : A16 swap override/Top-Block Swap Override enabled
Note : Rising edge of PWROK
16 PCI_GNT#3
R1724 1KOhm @
NVM_CLE : DMI Termination Voltage
H : Set to Vcc
L : Set to Vss
Note : Rising edge of PWROK
+VCCQ_NVRAM
16 NVM_CLE
R1722 1KOhm @
GPIO15/ WLAN_ON :
H = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality
L = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
Note : Rising edge of RSMRST# pin
WLAN_ON
R1706 10KOhm @
PCH_INTVRMEN : Integrated SUS 1.05V VRM Enable
H : Integrated VRM is enabled
L : Integrated VRM is disabled
Note: This signal should always be pulled high
+VCC_RTC
13 PCH_INTVRMEN
R1709 330KOHM
SPKR_PCH : NO REBOOT STRAP
H : Enable
L : Disable (Default)
Note : Rising edge of PWROK
+3VS
13,41 SPKR_PCH
R1710 1KOhm @
PCI_GNT#1,PCI_GNT#0 : Boot BIOS Strap
PCI_GNT#0 PCI_GNT#1
0 0 LPC
0 1 PCI
1 1 SPI
Note : Rising edge of PWROK
16,65 PCI_GNT#0
16,65 PCI_GNT#1
R1720 1KOhm@
R1721 1KOhm@
NVM_ALE : Danbury Technology Enabled
High--> Enable Intel Anti-Theft Technology.
Low--> Disable Intel Anti-Theft Technology.
Note : Rising edge of PWROK
+VCCQ_NVRAM
16 NVM_ALE
R1723 1KOhm @
GPIO27/ USB_SW :
H = Enables the internal VccVRM. (Default)
L = Disables the VccVRM.
Note : Rising edge of RSMRST# pin
PCH_GPIO27
R1713 1KOhm @
PEGATRON
Title : PCH GPIO
BU1-RD Div.1-HW RD Dept.1
Engineer: Johnson Huang
Size Custom
Project Name AIC70
Rev 2.0
Date: Wednesday, May 04, 2011
Sheet 17 of 77

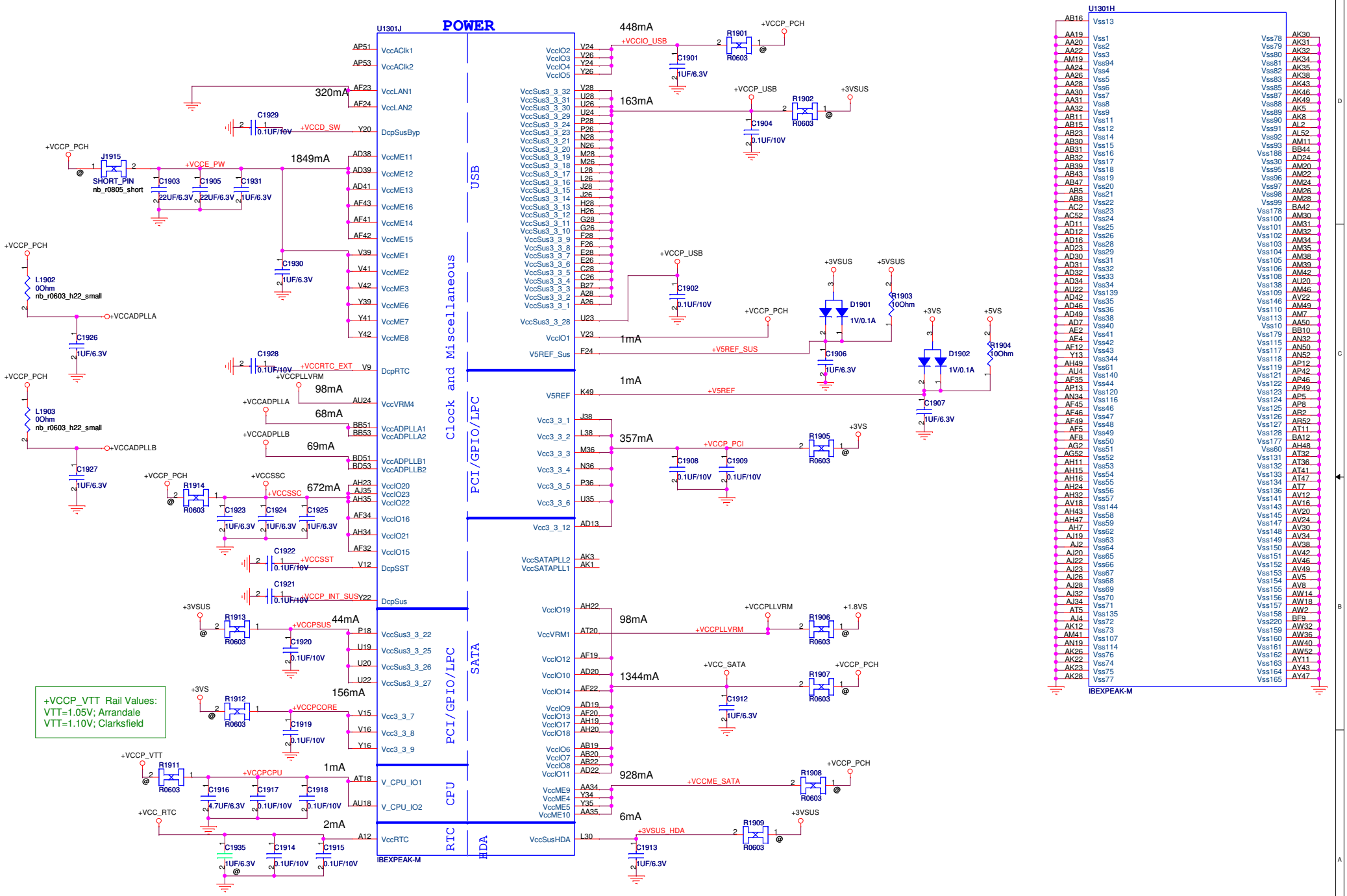


PEGATRON Title : PCH PWR(1)

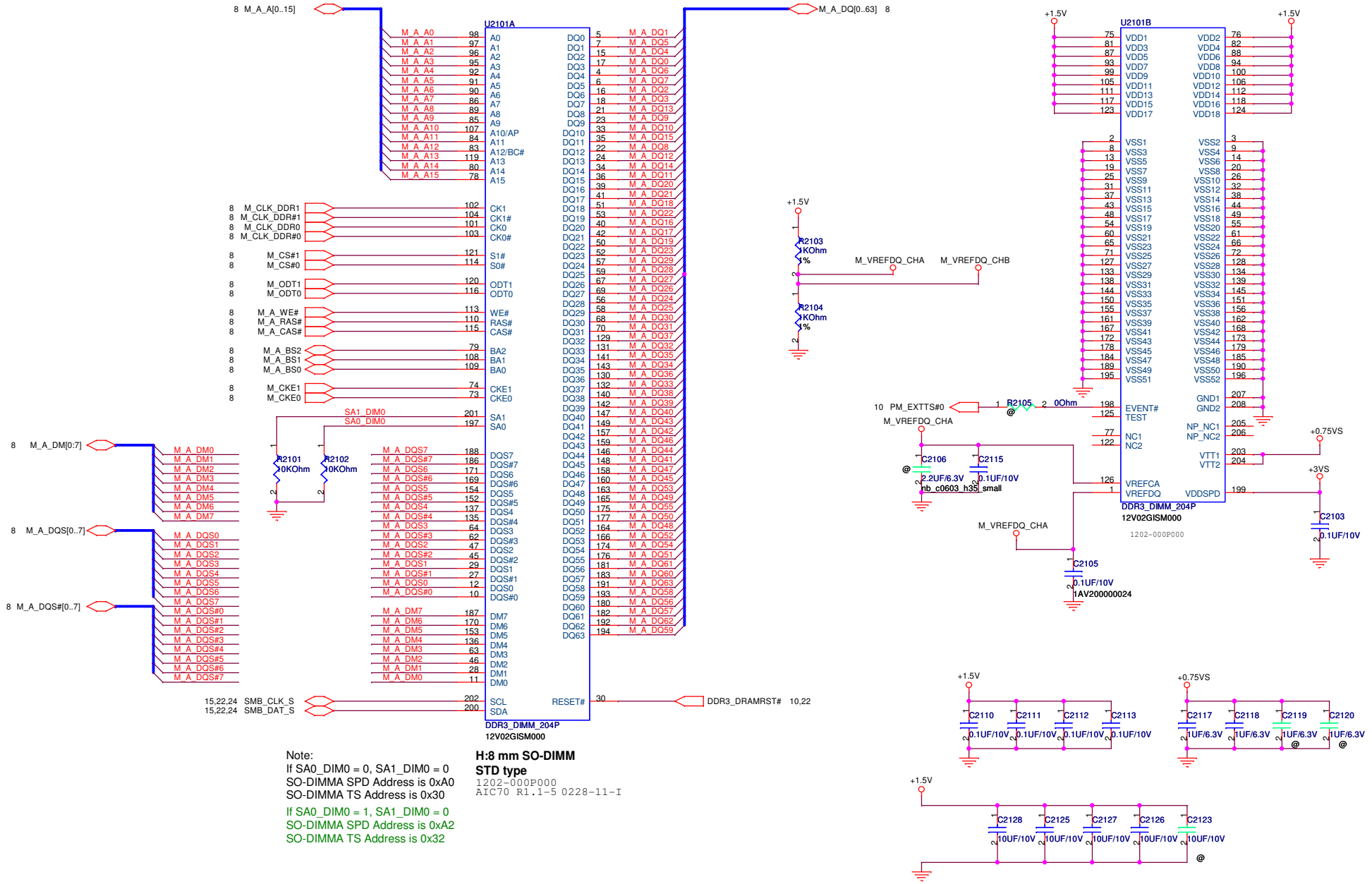
BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huangn

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 18 of 77



PEGATRON	Title : PCH PWR		
BU1-RD Div.1-HW RD Dept.1	Engineer: Johnson Huang		
Size: Custom	Project Name: AIC70		Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 19 of 77		



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

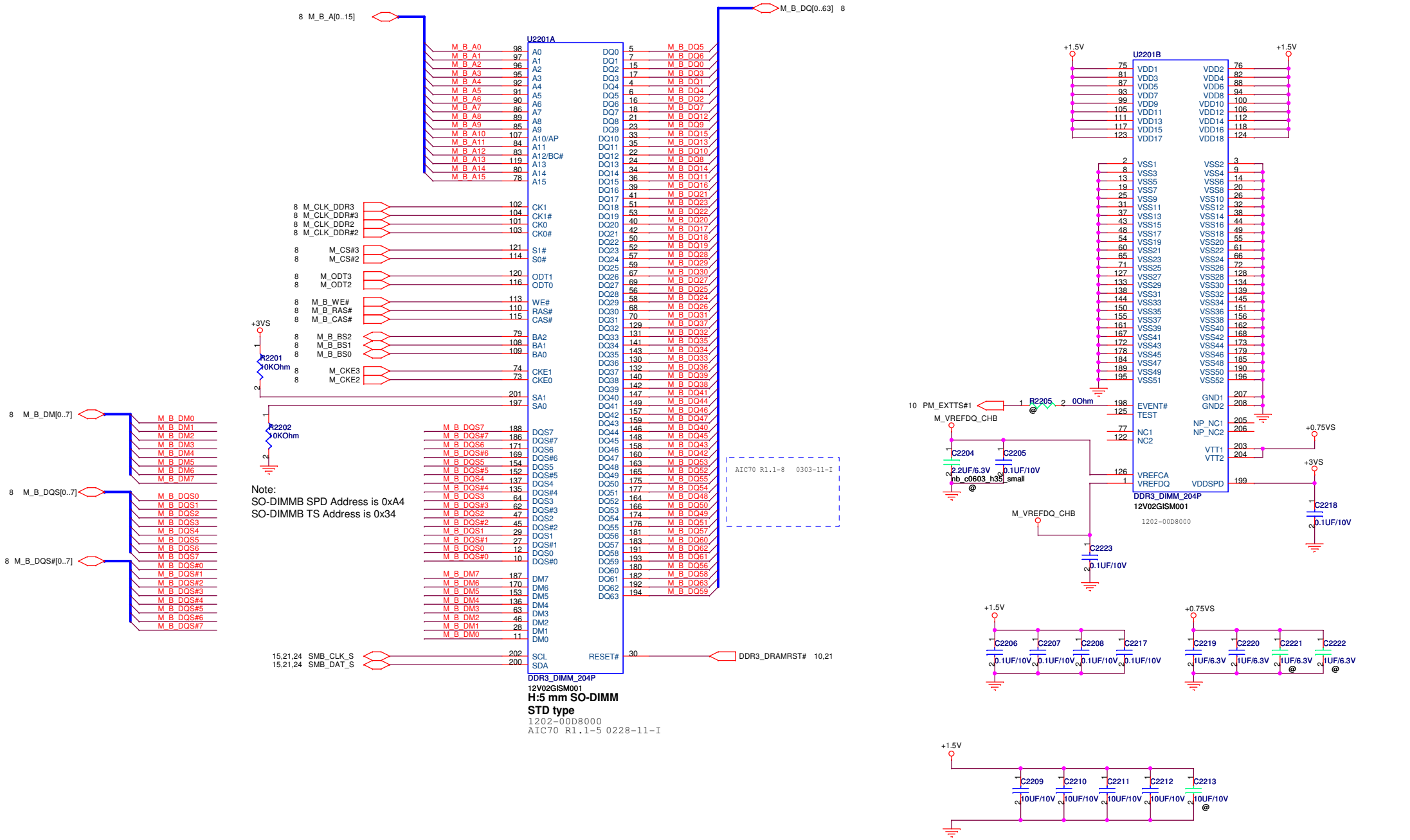
H:8 mm SO-DIMM
STD type
1202-000P000
AIC70 R1.1-5 0228-11-I

PEGATRON **Title : DDR3 SO-DIMM-Channel A**

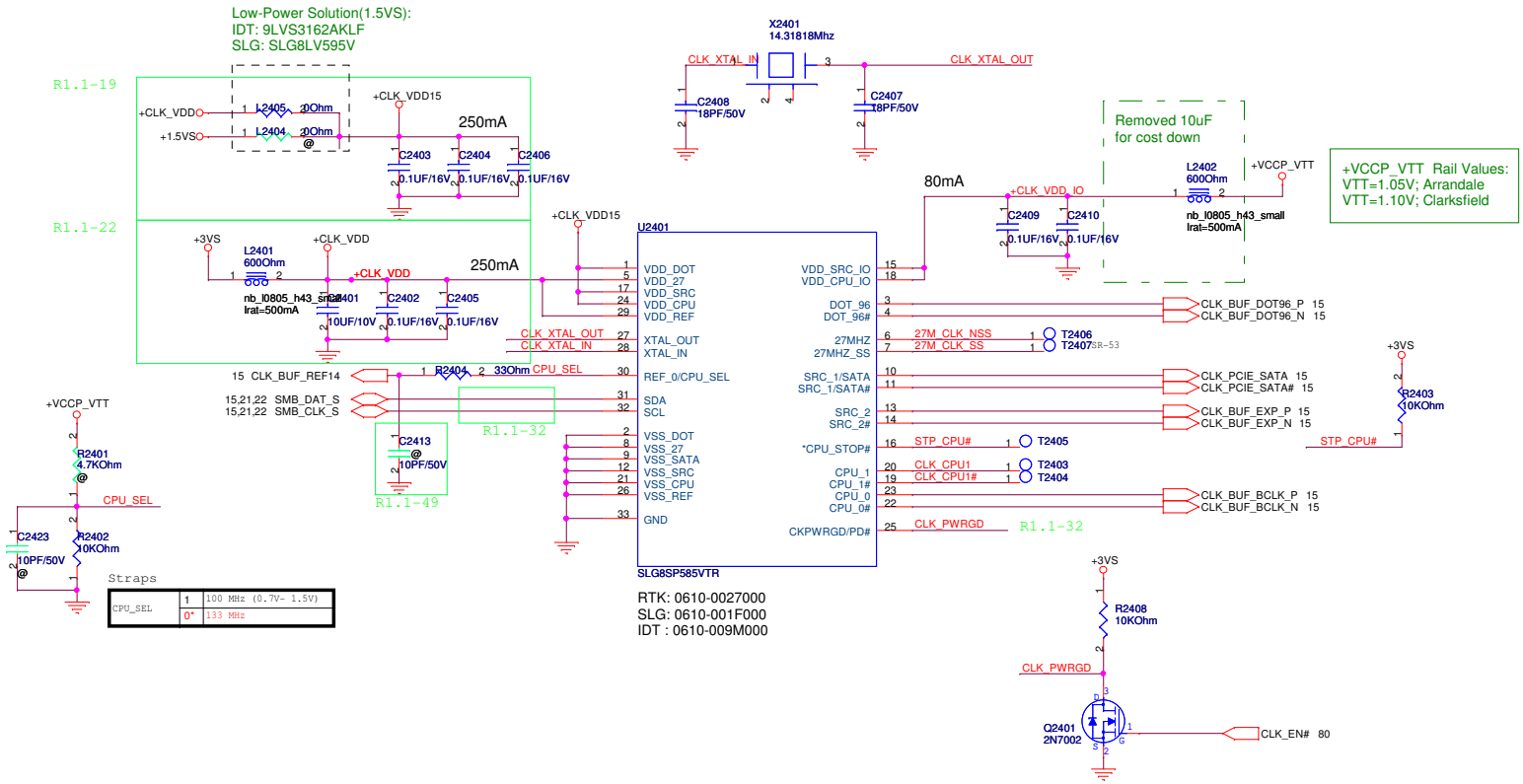
BU1-RD Div.1-HW RD Dept.1 **Engineer: *Johnson Huang***

Size	Project Name	Rev
Custom	**AIC70**	2.0

Date: Wednesday, May 04, 2011 Sheet 21 of 77



PEGATRON	Title : DDR3 SO-DIMM-Channel B		
BU1-RD Div.1-HW RD Dept.1	Engineer: Johnson Huang		
Size: Custom	Project Name: AIC70		Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 22 of 77		



PEGATRON Title : CLK GEN. SLG8SP585V

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 24 of 77

Close to LAN chip within 250mils

PCIE_RXP6_LOM C3323 0.1UF/10V PCIE_RXP6 15
PCIE_RXN6_LOM C3324 0.1UF/10V PCIE_RXN6 15
PCIE_TXP6 PCIE_TXP6 15
PCIE_TXN6 PCIE_TXN6 15
CLK_PCIE_LAN CLK_PCIE_LAN 15
CLK_PCIE_LAN# CLK_PCIE_LAN# 15

+VDD33_LOM
LED0 R3325 4.7KOhm
SR-72
+VDD33_LOM
LED1 R3331 4.7KOhm

Modify H/W strap setting SR-41 0125-11

R3313 5.1KOhm
LED1 C3332 470PF/16V
AIC70 R1.1-20 0306-11-I
R3717 10KOhm
LED0 C3333 470PF/16V
C3302 1UF/6.3V
DVDDL C3339 0.1UF/16V

Powr-on strapping
(1) LED[0]: enable overclocking
pull-high: overlocking (default)
stuff R3326, R3324; Remove R3317, R3325, R3327;
pull-low: un-overclocking
stuff R2, R3325, R3327; Remove R3326, R3324

(2) LED[1]: selection for AR8158's internal VDDCT (SWR/LDO)
pull-high: SWR mode
stuff R3330, R3332; Remove R3313, R3331, R3333;
pull-low: LDO mode
stuff R3313, R3331, R3333; Remove R3330, R3332

+VDDCT
L3301 2.2UH LX
C3311 0.1UF/10V
C3309 10UF/6.3V

+3VSUS
L3302 1.5KOhm/100Mhz Irat=1A
AIC70 R1.1-7 0302-11-I
C3313 10UF/6.3V
+VDD33_LOM
C3314 1UF/6.3V
C3315 0.1UF/16V

Close to PIN2 within 400 mil
Close to PIN2 within 200 mil

AR8158 (SWR mode)
Stuff L3301, C3311, C3309；remove C3301, R3311
AR8158 (LDO mode)
Stuff R3311, C3301, C3303；Remove L3301, C3311, C3309

+3VS
R3314 4.7KOhm
C3338 0.1UF/16V
LED1 LED0 DVDDL PCIE_TXN6 PCIE_TXP6 AVDDL CLK_PCIE_LAN CLK_PCIE_LAN#
AIC70 R1.2-45 0321-11-I

U3301A
LX VDD33 PERSTN WAKEn VDDCT_REG VDDCT AVDDL_REG XTLO
GND1 LED1[1] LED[0] DVDDL_REG RX_N RX_P AVDDL2 REFCLK_P REFCLK_N
AVDDL1 TX_P TX_N NC TESTMODE SMDATA SMCLK CLKREQn
XTLI AVDDH_REG RBIAS TRXP0 TRXN0 TRXP1 TRXN1 LED[2]
AR8158-BL1A-RL

10,16,46,47,55,70 BUF_PLT_RST#
14,55 PCIE_WAKE#
VDDCT_REG
+VDDCT
AVDDL
LX
+VDD33_LOM

R3311 0Ohm
C3301 1UF/6.3V
C3303 0.1UF/16V
AIC70 R1.1-20 0306-11-I
AIC70 R1.1-39 0311-11-I

C3310 0.1UF/10V
C3316 1UF/6.3V
C3317 0.1UF/16V
L3303 0Ohm
AIC70 R2.0-56 0406-11-I
AIC70 R2.0-65 0420-11-I

C3337 0.1UF/16V
R3316 0Ohm
T3301
T3302
AVDDL
PCIE_RXP6_LOM
PCIE_RXN6_LOM
R3315 0Ohm CLKREQn PCIE_LOM_CLKREQ# 15

Remove LAN LED circuit SR-29 0125-11

U3301B
GND2 GND3 GND4 GND5 GND9 GND8 GND7 GND6
AR8158-BL1A-RL
AIC70 R1.2-45 0321-11-I

Modify R3311 as VP SR-31 0125-11

X3301 25MHZ
XTALO XTALI
C3321 15PF/50V
C3322 15PF/50V
AIC70_R2.0-59 0411-11-I

XTALI
AVDDH
RBIAS_LOM
C3320 1UF/6.3V
C3304 0.1UF/16V
R3310 2.37KOhm

34 L_TDP
34 L_TDN
34 L_RDP
34 L_RDN

R3320 49.9Ohm
R3321 49.9Ohm
R3322 49.9Ohm
R3323 49.9Ohm
C3331 1000PF/16V
C3305 0.1UF/16V
C3306 0.1UF/16V
C3334 1000PF/16V

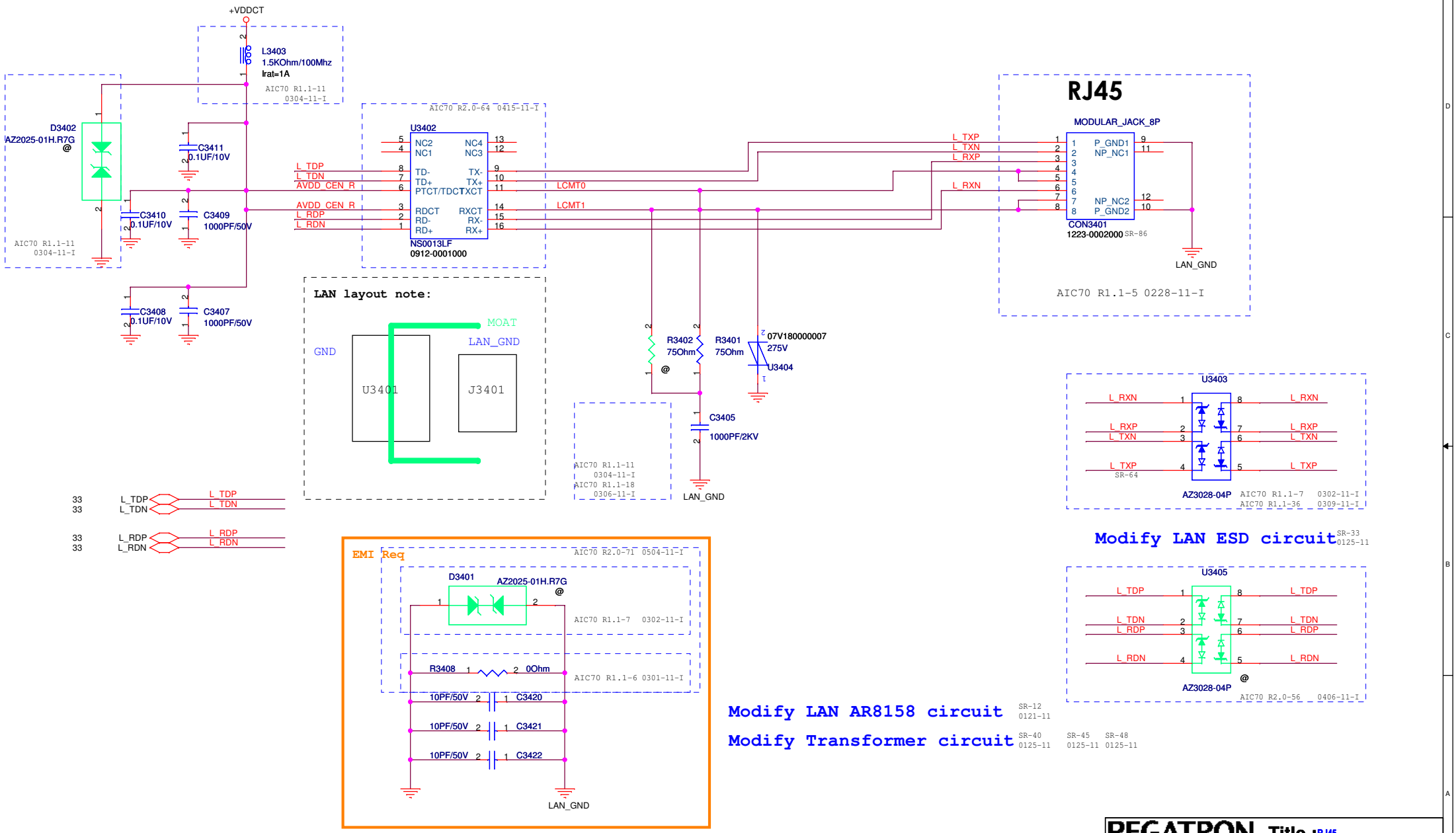
Close to LAN chip and less than 300mils

+VDD33_LOM
BUF_PLT_RST# R3328 4.7KOhm
PCIE_WAKE# R3329 4.7KOhm

Modify LAN AR8158 circuit SR-12 0121-11

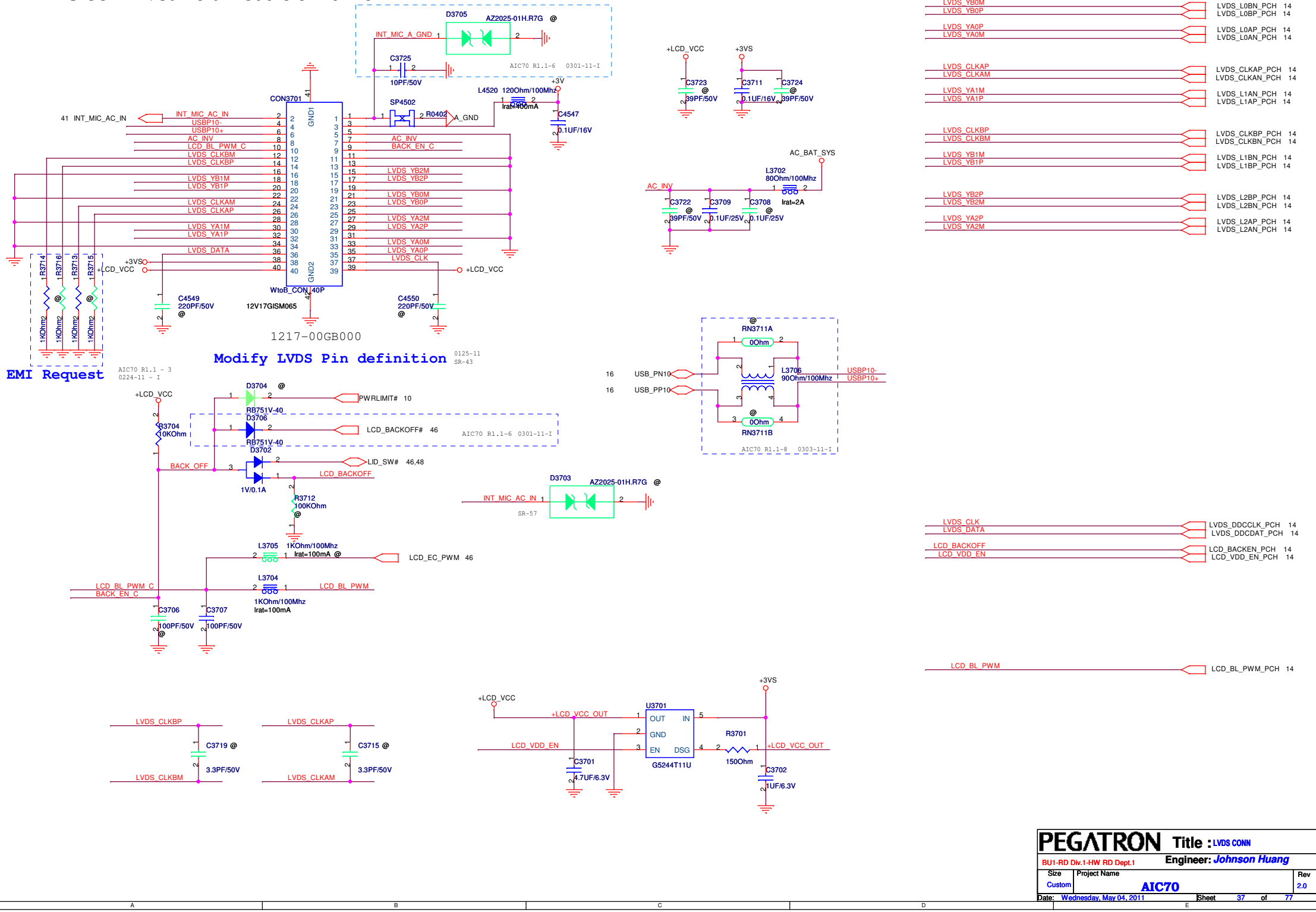
Change U3301 to AR8158 Part and remover SM BUS SR-32 0125-11

PEGATRON Title : LAN_ATHEROS_AR8158
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Johnson Huang
Size: Custom | Project Name: AIC70 | Rev: 2.0
Date: Wednesday, May 04, 2011 | Sheet 33 of 77



PEGATRON	Title : RJ45	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Johnson Huang	
Size: B	Project Name: AIC70	Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 34 of 77	

LVDS Conn w/Camera Module & Int Mic

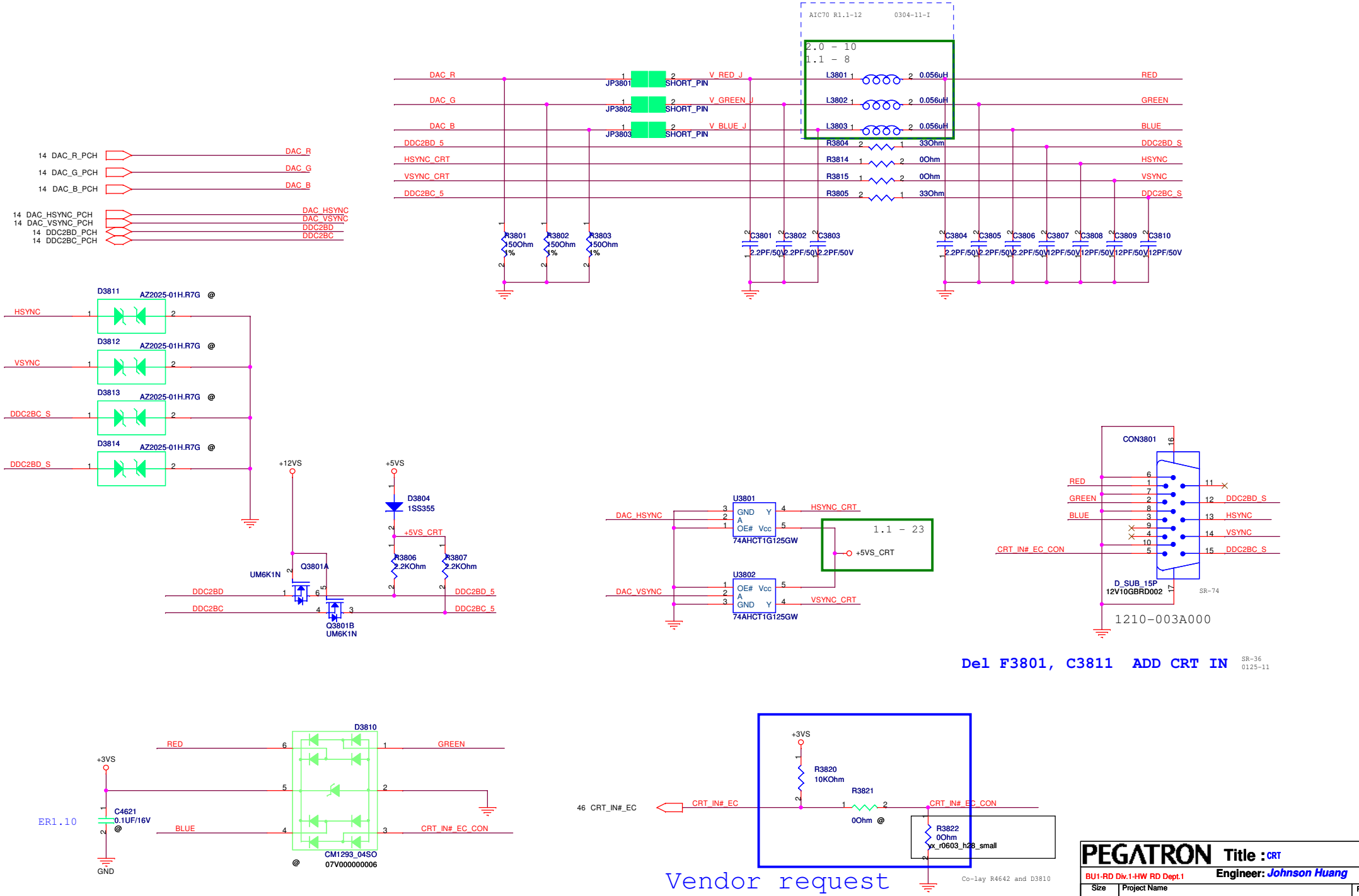


PEGATRON Title : LVDS CONN

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 37 of 77

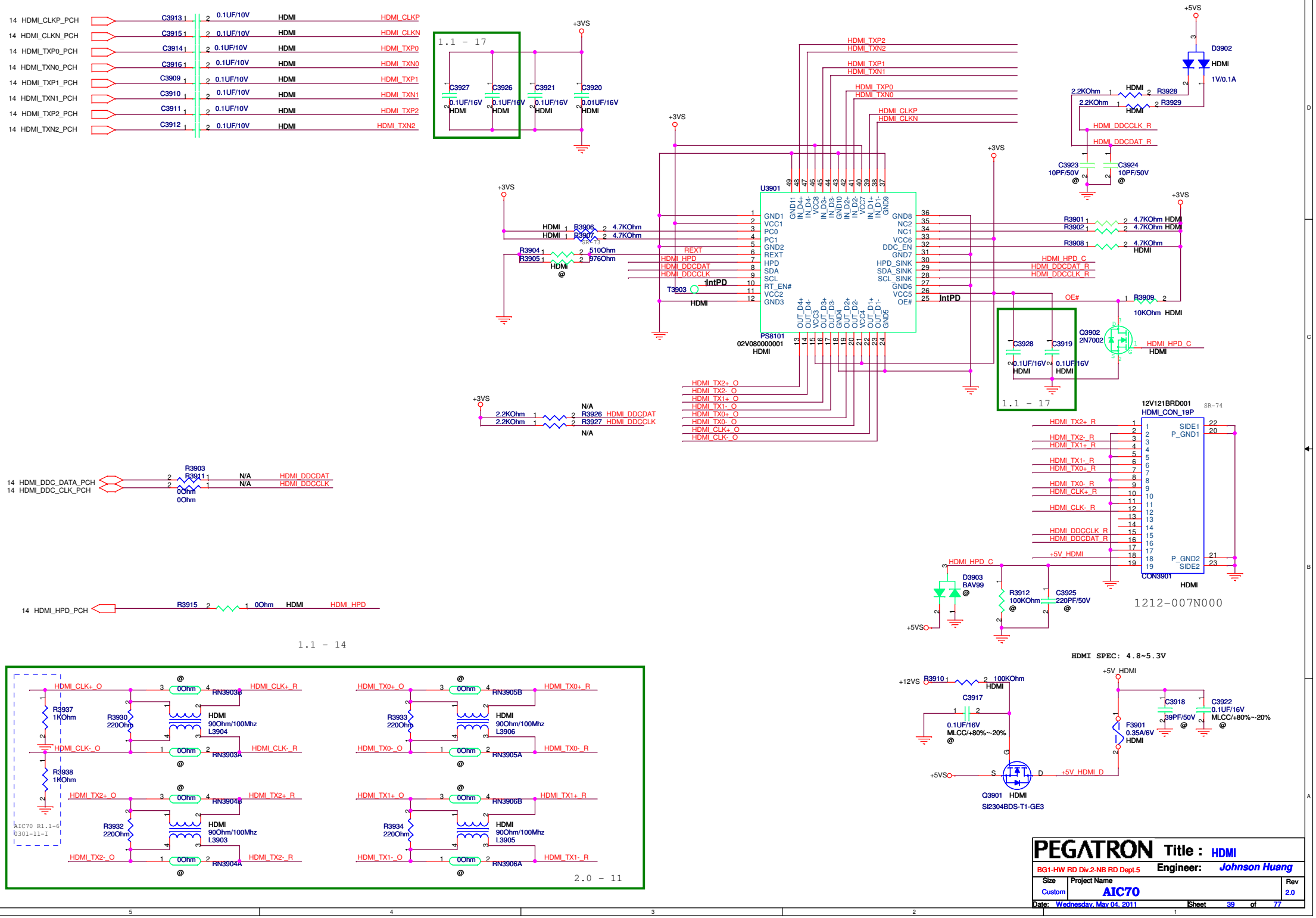


PEGATRON Title : CRT

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 38 of 77



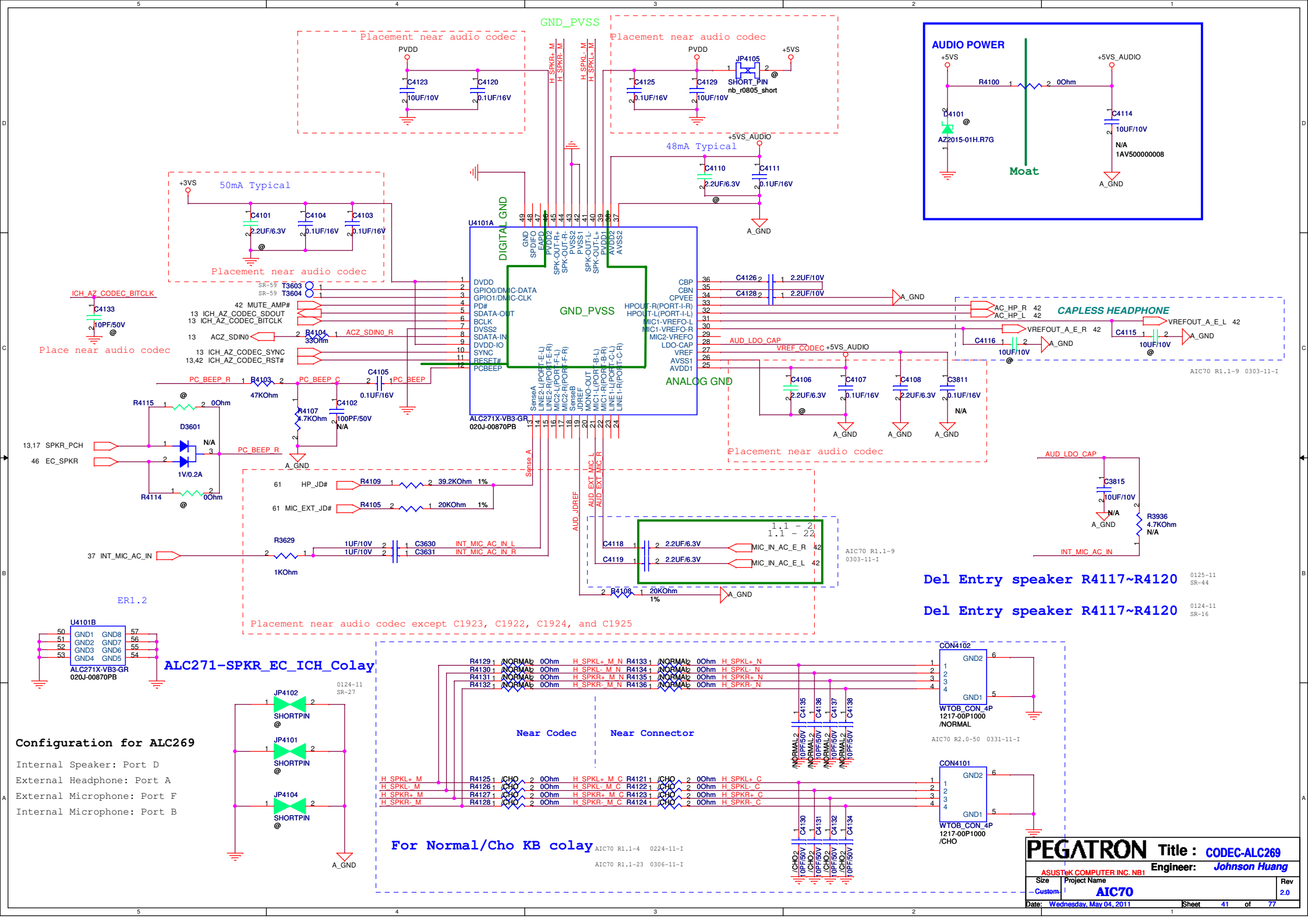
PEGATRON	Title : HDMI		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Johnson Huang		
Size: Custom	Project Name: AIC70		Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 39 of 77		

PEGATRON Title : Display Port

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

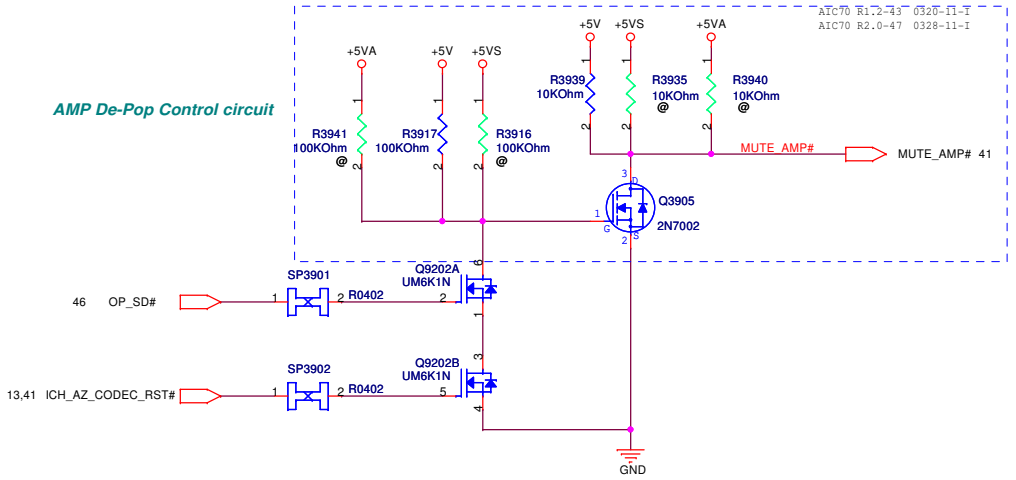
Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 40 of 77


AUDIO POWER
+5VS
+5VS_AUDIO
R4100 0Ohm
C4101
AZ2015-01H.R7G
C4114 10UF/10V
N/A
1AV500000008
Moat
A_GND
GND_PVSS
Placement near audio codec
PVDD
C4123 10UF/10V
C4120 0.1UF/16V
C4125 0.1UF/16V
C4129 10UF/10V
JP4105 SHORT_PIN nb_r0805_short
48mA Typical
C4110 2.2UF/6.3V
C4111 0.1UF/16V
50mA Typical
C4101 2.2UF/6.3V
C4104 0.1UF/16V
C4103 0.1UF/16V
U4101A
DIGITAL GND
ANALOG GND
GND_PVSS
DVDD
GPIO0/DMIC-DATA
GPIO1/DMIC-CLK
PD#
SDATA-OUT
BCLK
DVSS2
SDATA-IN
DVDD-IO
SYNC
RESET#
PCBEEP
CBP
CBN
CPVEE
HPOUT-R(PORT-I-R)
HPOUT-L(PORT-I-L)
MIC1-VREFO-L
MIC1-VREFO-R
MIC2-VREFO
LDO-CAP
VREF
AVSS1
AVDD1
ALC271X-VB3-GR
020J-00870PB
ICH_AZ_CODEC_BITCLK
C4133 10PF/50V
Place near audio codec
42 MUTE_AMP#
13 ICH_AZ_CODEC_SDOUT
13 ICH_AZ_CODEC_BITCLK
13 ACZ_SDIN0
R4104 33Ohm
ACZ_SDIN0_R
13 ICH_AZ_CODEC_SYNC
13,42 ICH_AZ_CODEC_RST#
T3603
T3604
C4126 2.2UF/10V
C4128 2.2UF/10V
AUD_LDO_CAP
VREF_CODEC
+5VS_AUDIO
C4106 2.2UF/6.3V
C4107 0.1UF/16V
C4108 2.2UF/6.3V
C3811 0.1UF/16V
N/A
CAPLESS HEADPHONE
AC_HP_R 42
AC_HP_L 42
VREFOUT_A_E_R 42
VREFOUT_A_E_L 42
C4116 10UF/10V
C4115 10UF/10V
AIC70 R1.1-9 0303-11-I
PC_BEEP_R
R4103 47KOhm
PC_BEEP_C
C4105 0.1UF/16V
PC_BEEP
R4115 0Ohm
D3601
1V/0.2A
R4114 0Ohm
R4107 4.7KOhm
C4102 100PF/50V
13,17 SPKR_PCH
46 EC_SPKR
Sense A
61 HP_JD#
R4109 39.2KOhm 1%
61 MIC_EXT_JD#
R4105 20KOhm 1%
AUD_JDREF
AUD_EXT_MIC_L
AUD_EXT_MIC_R
C4118 2.2UF/6.3V
C4119 2.2UF/6.3V
MIC_IN_AC_E_R 42
MIC_IN_AC_E_L 42
R4108 20KOhm 1%
Placement near audio codec except C1923, C1922, C1924, and C1925
37 INT_MIC_AC_IN
R3629 1KOhm
C3630 1UF/10V
C3631 1UF/10V
INT_MIC_AC_IN_L
INT_MIC_AC_IN_R
C3815 10UF/10V
R3936 4.7KOhm
Del Entry speaker R4117~R4120
0125-11 SR-44
Del Entry speaker R4117~R4120
0124-11 SR-16
ER1.2
U4101B
ALC271X-VB3-GR
020J-00870PB
ALC271-SPKR_EC_ICH_Colay
0124-11 SR-27
JP4102 SHORTPIN
JP4101 SHORTPIN
JP4104 SHORTPIN
Configuration for ALC269
Internal Speaker: Port D
External Headphone: Port A
External Microphone: Port F
Internal Microphone: Port B
Near Codec
Near Connector
CON4102
WTOB_CON_4P
1217-00P1000
/NORMAL
CON4101
WTOB_CON_4P
1217-00P1000
/CHO
AIC70 R2.0-50 0331-11-I
For Normal/Cho KB colay
AIC70 R1.1-4 0224-11-I
AIC70 R1.1-23 0306-11-I
PEGATRON
Title : CODEC-ALC269
Engineer: Johnson Huang
ASUSTeK COMPUTER INC. NB1
Size Custom
Project Name AIC70
Rev 2.0
Date: Wednesday, May 04, 2011
Sheet 41 of 77

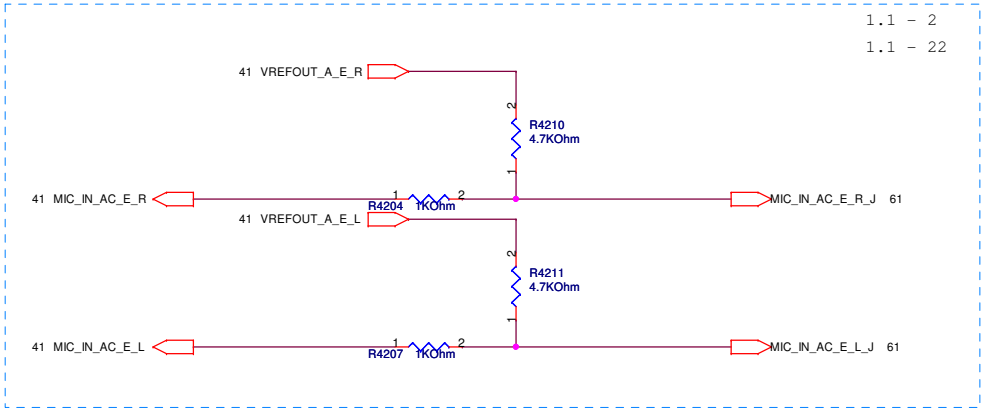
AIC70 R1.2-43 0320-11-I
AIC70 R2.0-47 0328-11-I

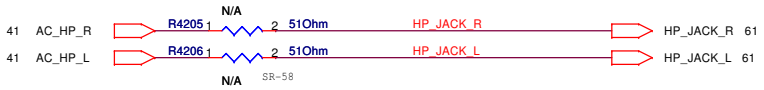
AMP De-Pop Control circuit



Modify De-Pop circuit SR-43 0125-11

1.1 - 2
1.1 - 22





PEGATRON Title : AUDIO ALC269
BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 42 of 77

PEGATRON Title : MDC CONN

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Johnson Huang

Size	Project Name	Rev
C	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 43 of 77

Del Entry audio circuit

SR-8
0121-11

PEGATRON Title : CODEC-ALC269

ASUSTeK COMPUTER INC. NB1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 44 of 77

Del Entry audio circuit

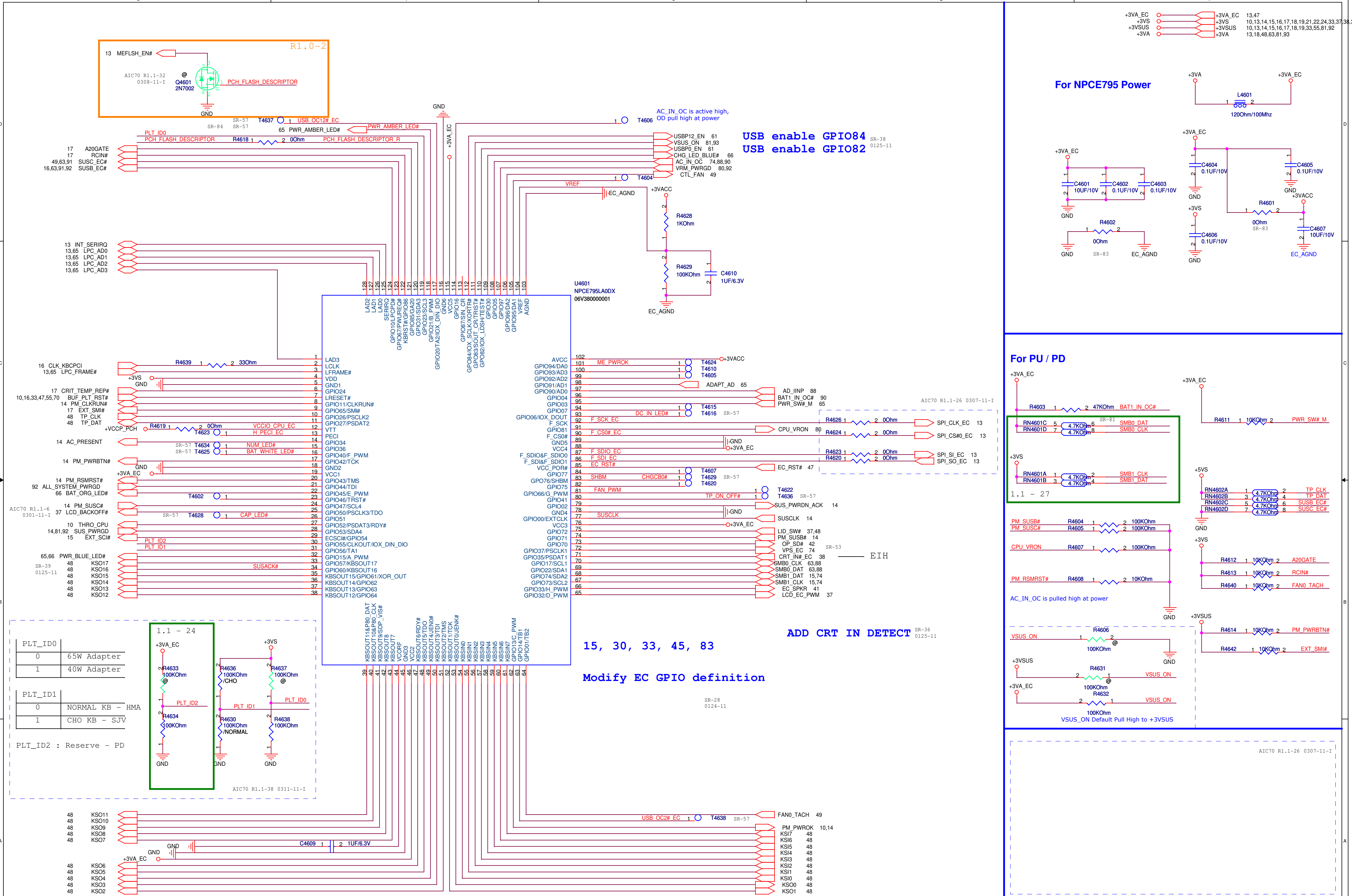
SR-8
0121-11

PEGATRON Title : AUDIO ALC269

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

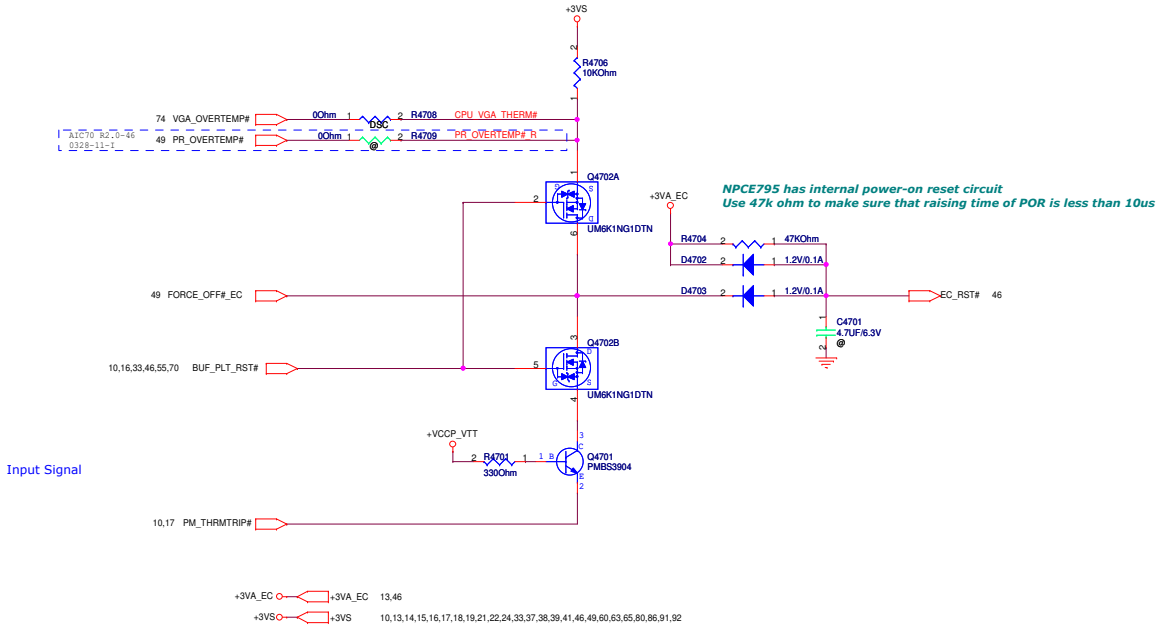
Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 45 of 77



PEGATRON	Title : NPCE795L
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Johnson Huang
Size: Custom	Project Name: AIC70 — Rev 2.0
Date: Wednesday, May 04, 2011	Sheet 46 of 77

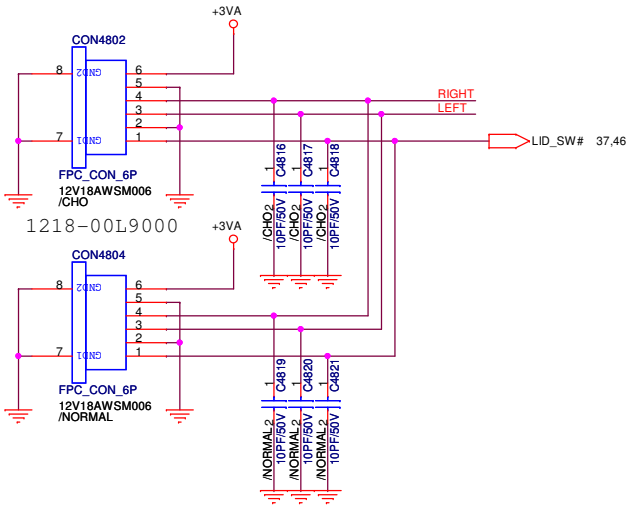
Thermal Policy



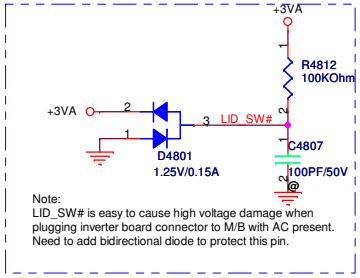
PEGATRON	Title : RST_Reset Circuit		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Johnson Huang		
Size: C	Project Name: AIC70		Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 47 of 77		

Touch Pad Button/ Hall Sensor

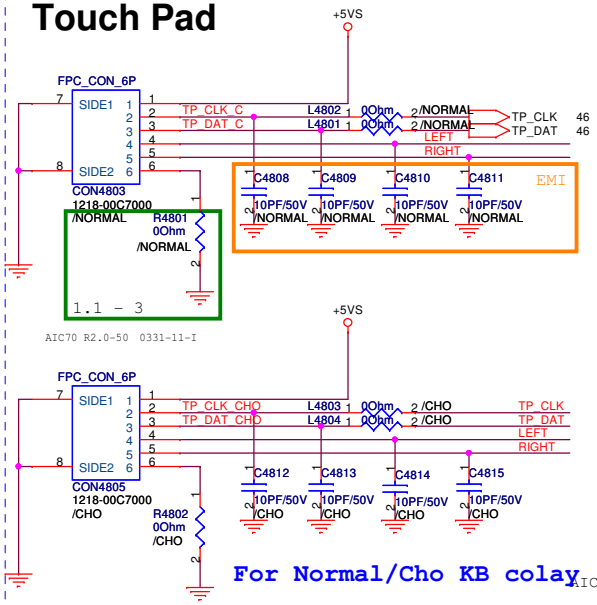
AIC70 R1.1-23 0306-11-I
AIC70 R1.1-35 0309-11-I

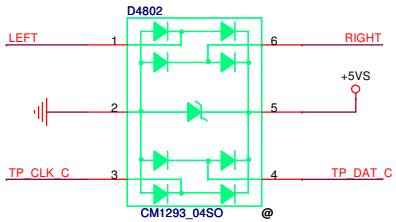


close toU4601



Touch Pad

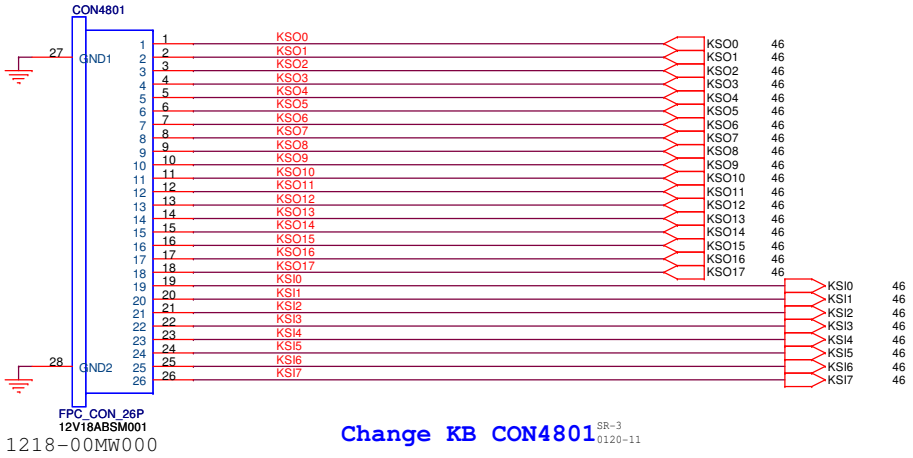




For Normal/Cho KB colay 0224-11-I
AIC70 R1.1-4

Remove TP button circuit SR-22 0124-11

Keyboard FOR 17"



Change KB CON4801 SR-3 0120-11

Change KB CON4801 PIN definition SR-25 0124-11
Reverse KB CON4801 SR-19 0124-11 SR-52 0126-11

Remove 15'' KB connector AIC70 R1.1 - 1 0224-11 - I

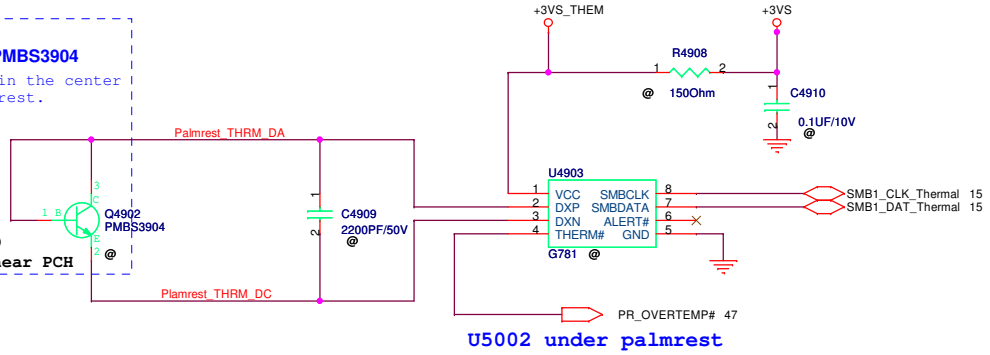
PEGATRON	Title : KB/ TP/ FLASH	
BU1-RD Div.1-HW RD Dept.1	Engineer: Johnson Huang	
Size: Custom	Project Name: AIC70	Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 48 of 77	

AIC70 R2.0-46 0328-11-I
AIC70 R2.0-49 0330-11-I

Palm Rest Thermal Sensor

PHILIP PMBS3904
Please in the center of Plamrest.

ER 1129
Place near PCH

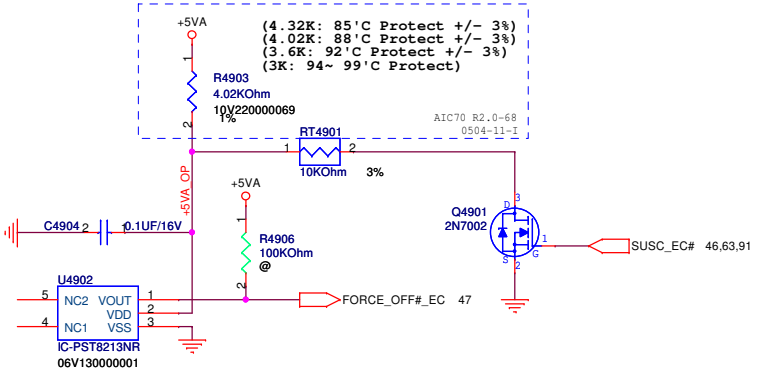


U5002 under palmrest

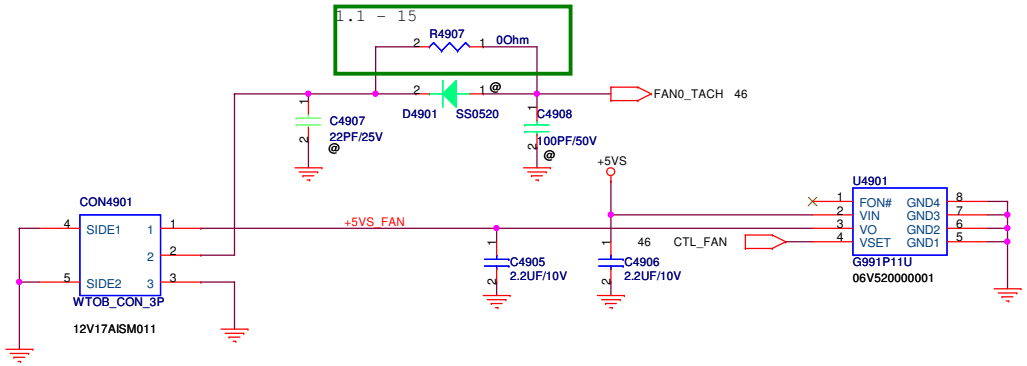
SMBUS addr=1001100x (98)

U5002: Remote(Local) thermal sensor,use remote mode.

Thermister



FAN



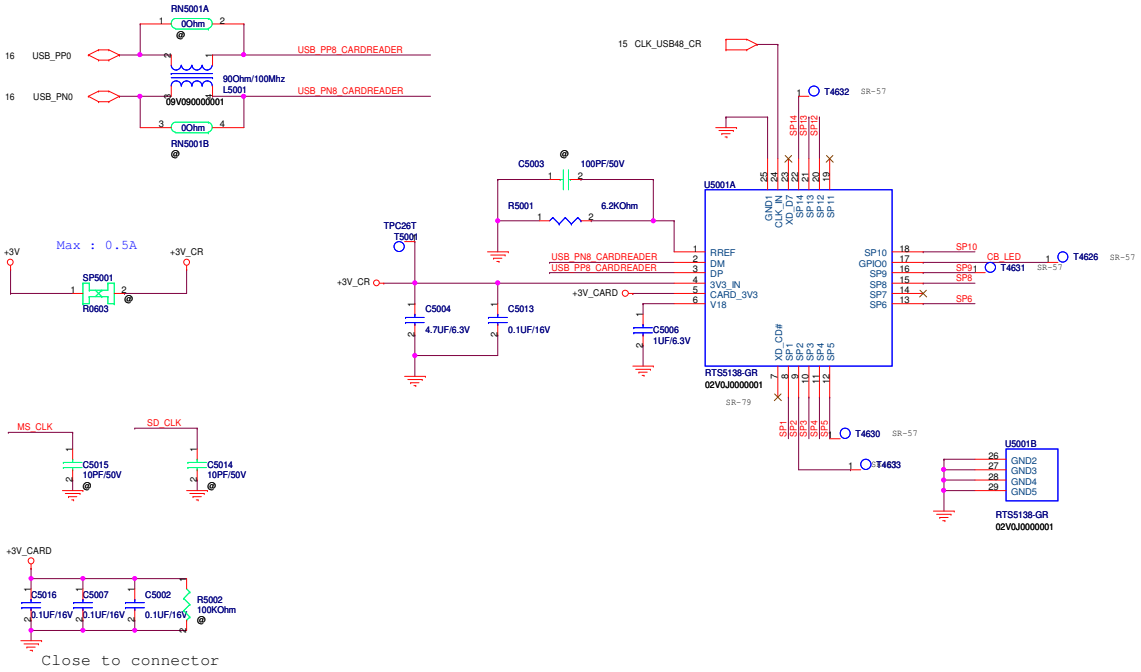
1217-00LH000

PEGATRON **Title : THERMAL/ FAN**

BU1-RD Div.1-HW RD Dept.1 **Engineer: *Johnson Huang***

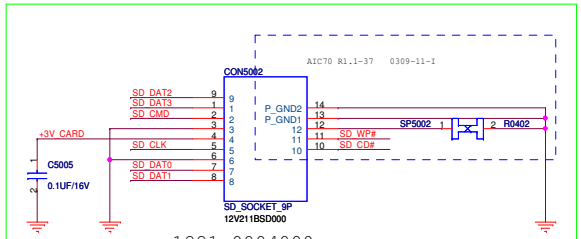
Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 49 of 77



Pin Name	Description
SP1	SDWP# / MSCLK
SP2	MS_INS#
SP3	SD_DAT1
SP4	SD_DAT0
SP5	MS_D3
SP6	SD_CD#
SP8	SD_CLK / MS_D2
SP9	MS_D0
SP10	SD_CMD
SP12	SD_DAT3 / MS_D1
SP13	SD_DAT2
SP14	MS_BS

SP1	SD_WP#	MS_CLK
SP2		MS_INS#
SP3	SD_DAT1	
SP4	SD_DAT0	
SP5		MS_D3
SP6	SD_CD#	
SP8	SD_CLK	MS_D2
SP9		MS_D0
SP10	SD_CMD	
SP12	SD_DAT3	MS_D1
SP13	SD_DAT2	
SP14		MS_BS



1221-0004000

Del Entry SD socket circuit SR-9 0121-11

Modify CON5002 SD socket circuit SR-24 0124-11

PEGATRON **Title : Realtek_RTS5138**

BG1-HW RD Div.2-NB RD Dept.5 **Engineer: Johnson Huang**

Size	Project Name	Rev
C	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 50 of 77

PEGATRON Title : USB3.0 uPD720200

BG1\HW1 Engineer: Johnson Huang

Size	Project Name	Rev
C	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 53 of 77

PEGATRON

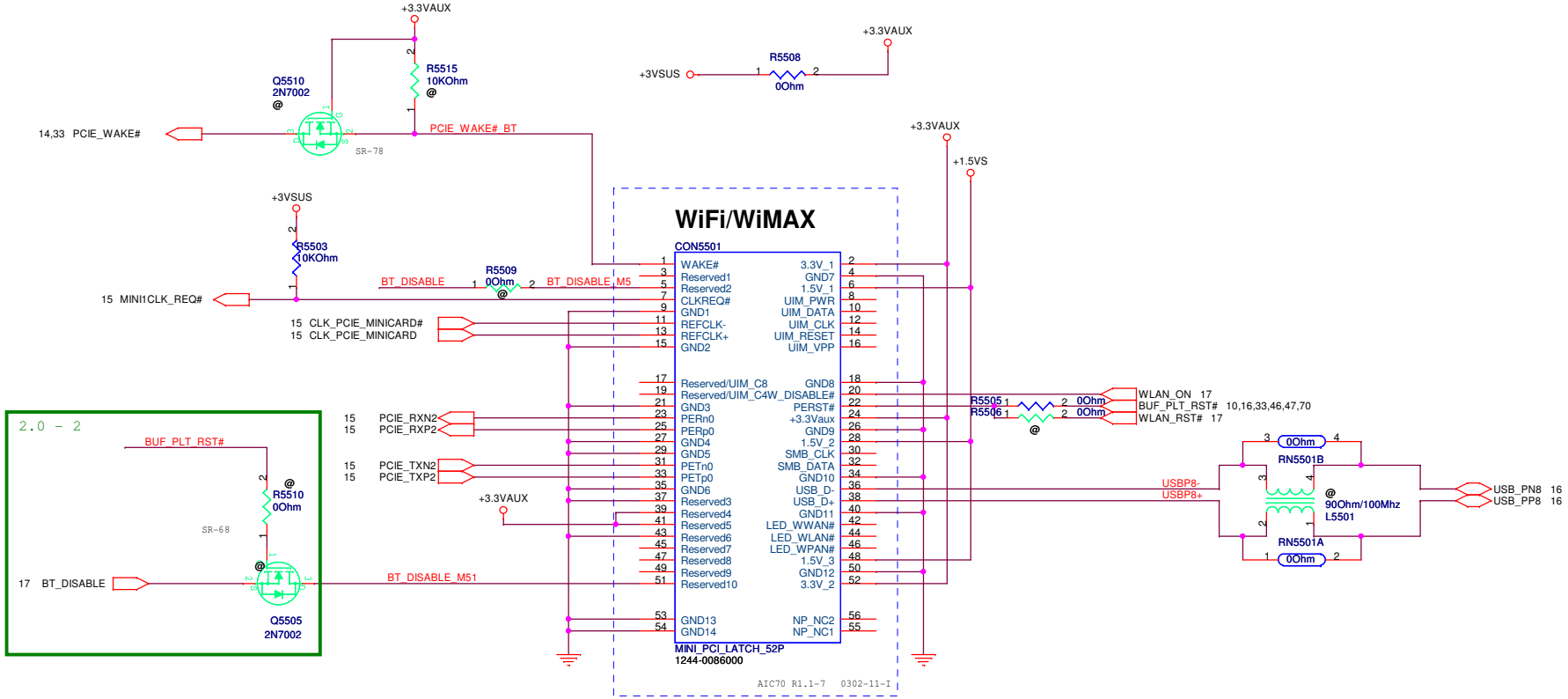
Title : PCIE NEW CARD

BU1-RD Div.1-HW RD Dept.1

Engineer: *Johnson Huang*

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 54 of 77



PEGATRON Title : WiFi/WiMAX

BU1-RD Div.1-HW RD Dept.1 Engineer:

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 55 of 77

PEGATRON

Title : MINICARD (WWAN)

BU1-RD Div.1-HW RD Dept.1

Engineer:

Size	Project Name	Rev
Custom		2.0

Date: Wednesday, May 04, 2011 Sheet 56 of 77

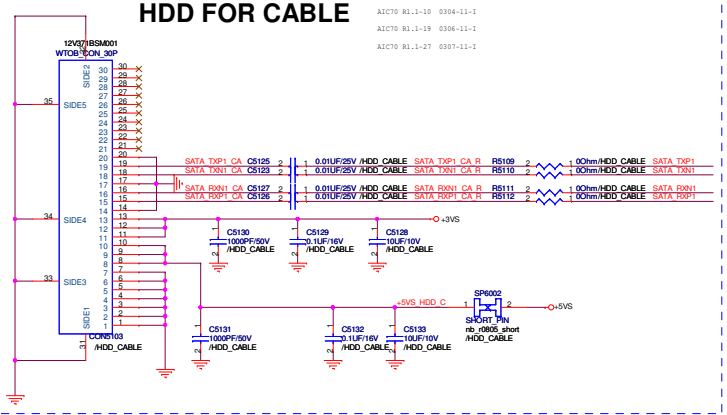
PEGATRON Title : MINICARD (WUSB /UPCONVERT)

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

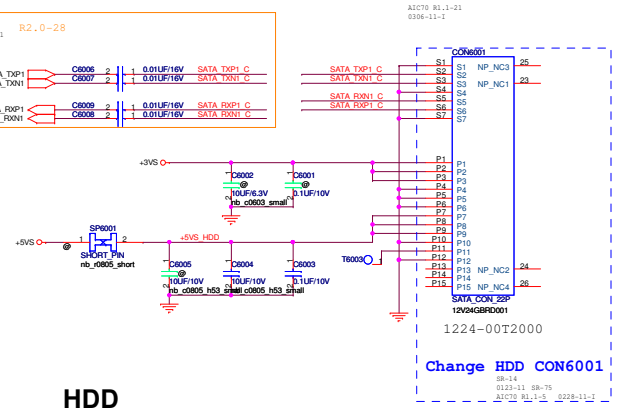
Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 57 of 77

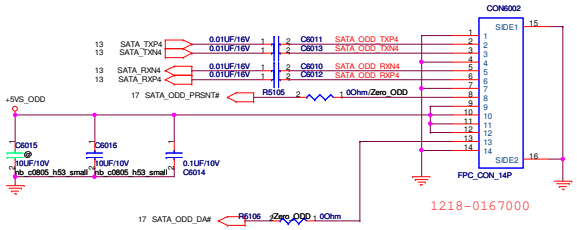
HDD FOR CABLE



HDD



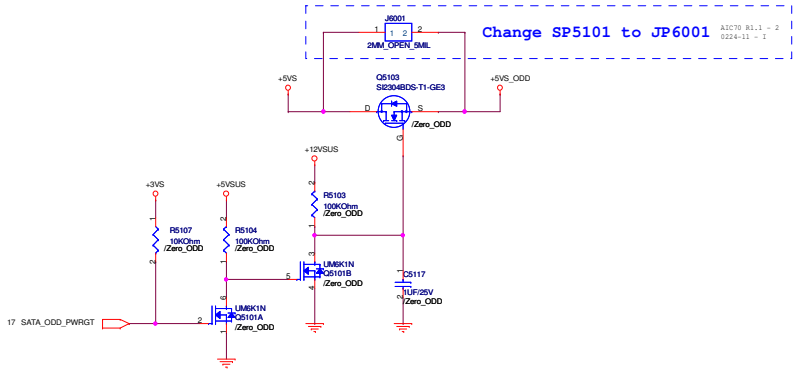
ODD FOR 17"



Remove 15'' ODD connector

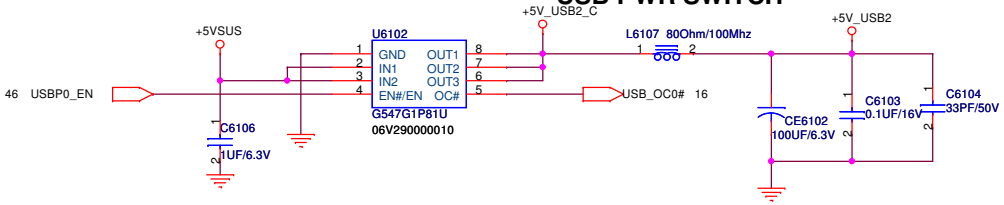
ZERO POWER ODD SUPPORT

support Hokey turn off ODD power



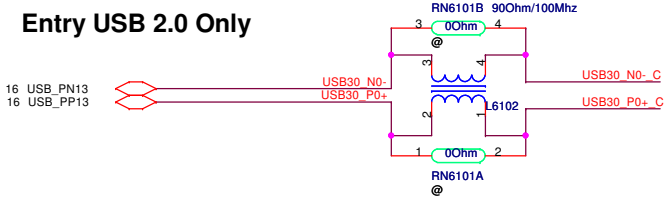
PEGATRON	Title : SATA HDD/ ODD		
BU1-RD Div.1-HW RD Dept.1	Engineer: Johnson Huang		
Size: Custom	Project Name: AIC70		Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 60 of 77		

USB PWR SWITCH



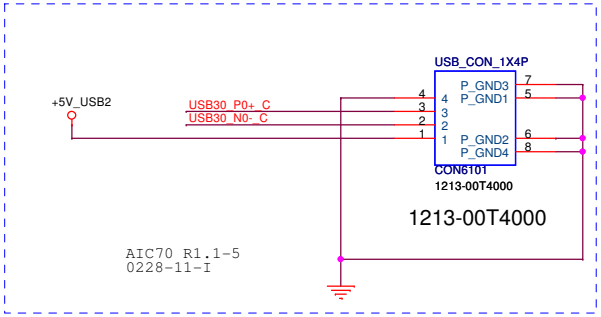
change USB power switch circuit SR-1 0120-11 SR-26 0124-11 SR-34 0125-11

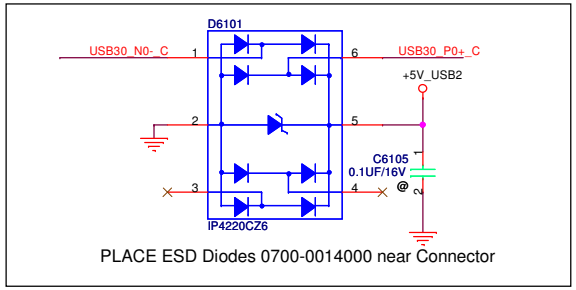
Entry USB 2.0 Only



Modify D6101, RN6101, RN6105, RN6106 SR-30 0125-11

USB 2.0



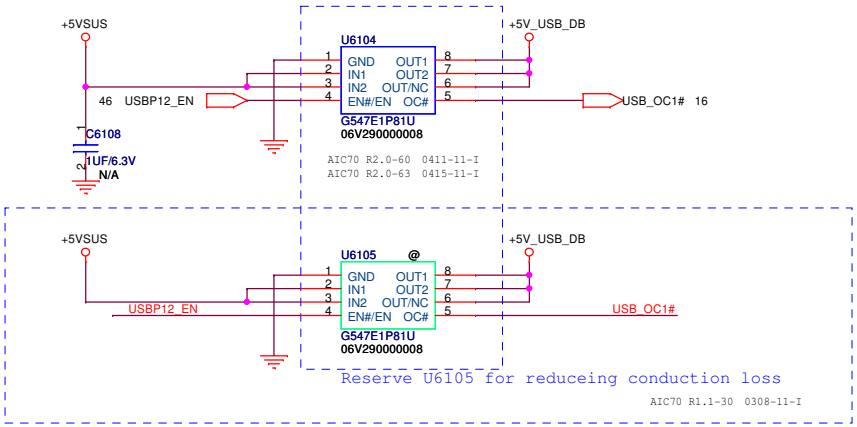


USB Conn. for Entry colay HDMI USB 2.0

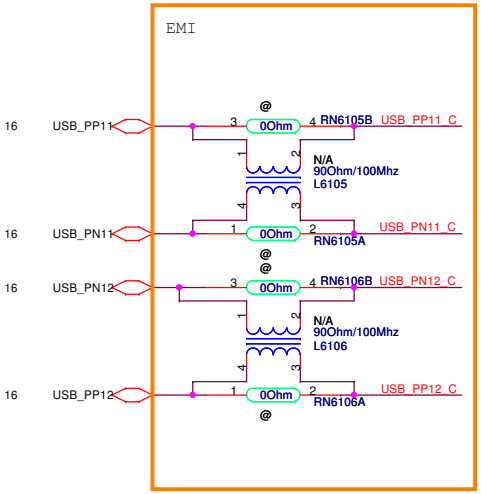
Remove USB_9 (HDMI) SR-21 0124-11

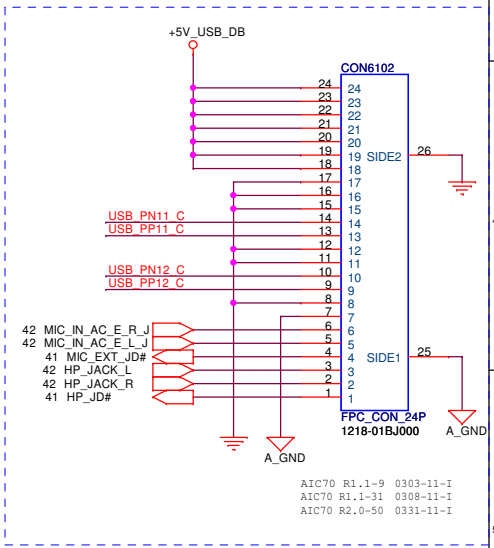
USB Power Switch for USB DB Main

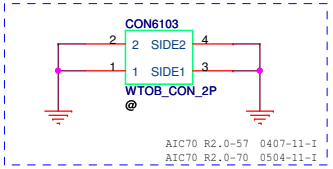
change USB power switch circuit SR-26 0124-12 SR-38 0125-13



AUDIO BOARD/w USB2.0 x2







PEGATRON Title : USB PORTS/ eSATA

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 61 of 77

TouchPanel CON

Camera Module CON

B/T MODULE

FELICA MODULE

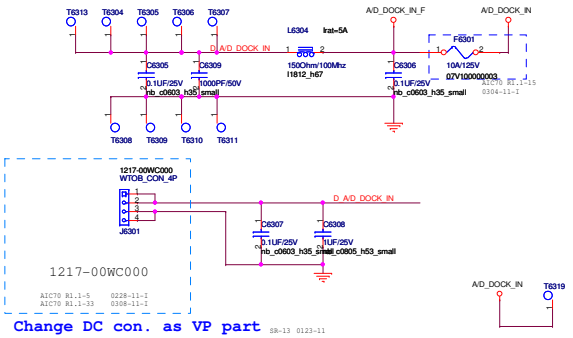
PEGATRON Title : Camera/ BT/ FL CONN

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 62 of 77

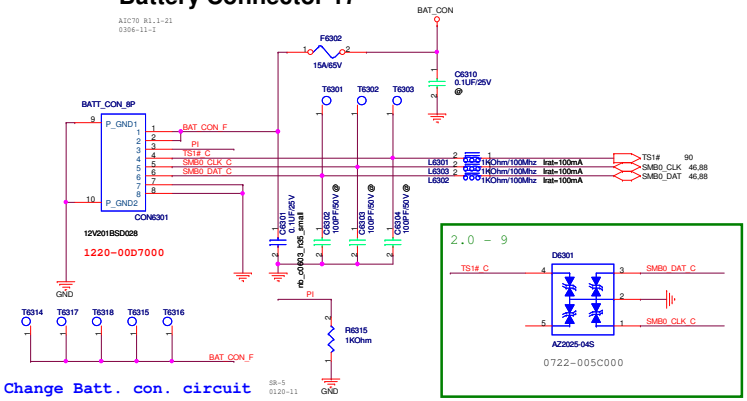
DC IN



Change DC con. as VP part
Reverse J6301

Change to 1217-00WC000

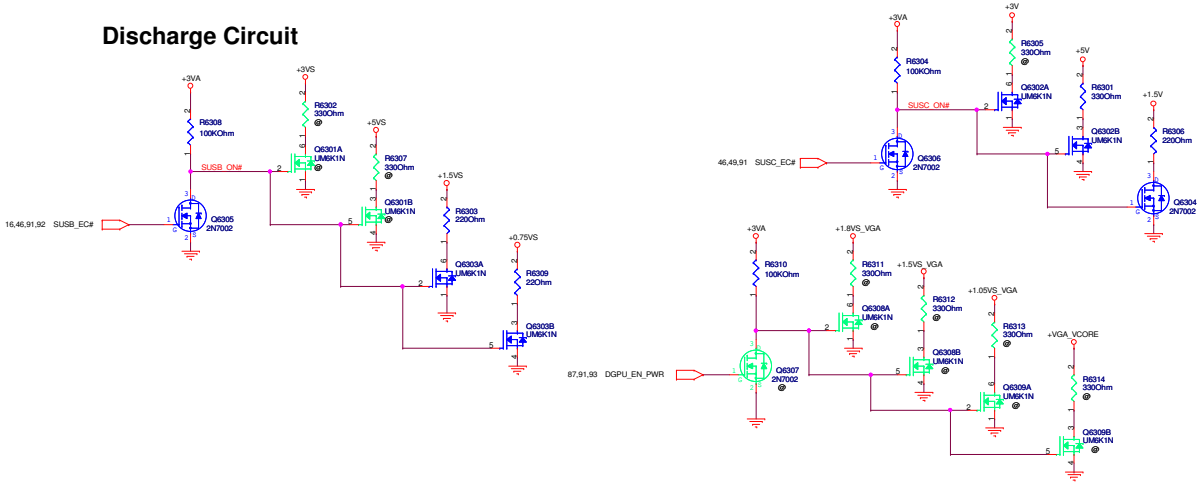
Battery Connector 17"



Change Batt. con. circuit

Remove 15'' Battery connector

Discharge Circuit



PEGATRON

Title : DC-IN/ DISCHARGE

BU1-RD Div.1-HW RD Dept.1

Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 63 of 77

Notes:
BRAIDWOOD right angled Connector (1.8V keyed)
Compatible BRAIDWOOD Modules
1.8V Mobile NVM 4GB 31.60mm x21.5mm
1.8V Mobile NVM 8GB 31.60mm x 21.5mm
1.8V Mobile NVM 16GB 31.60mm x 32.5mm

PEGATRON Title : NVM

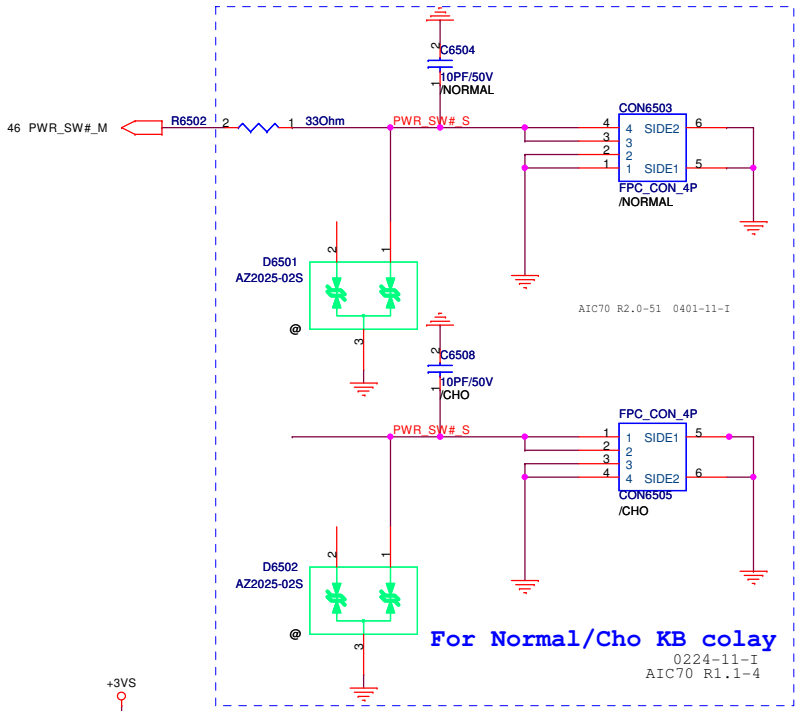
BU1-RD Div.1-HW RD Dept.1 Engineer: *Johnson Huang*

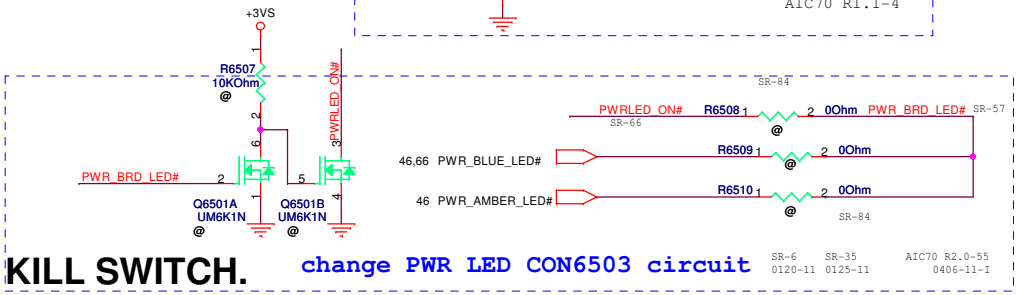
Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 64 of 77

PWR BRD/ AMBIENT/ HALL CONN.

1.1 - 12 SR-66





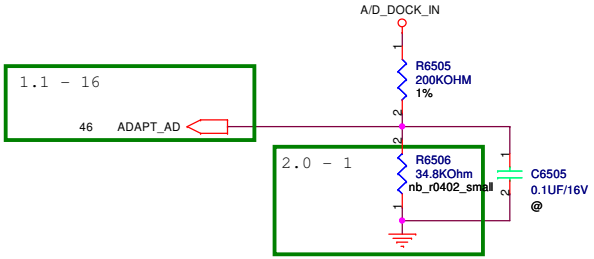
KILL SWITCH.

change PWR LED CON6503 circuit

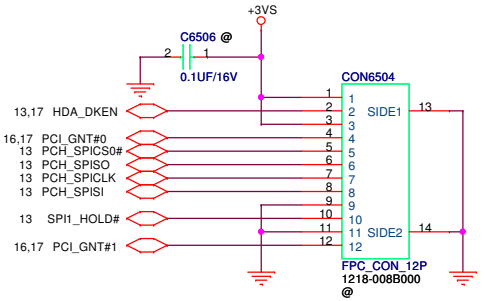
SR-6 0120-11 SR-35 0125-11 AIC70 R2.0-55 0406-11-I

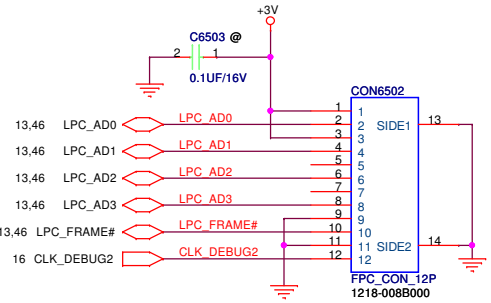
MODEM MODULE

ADAPTOR VOLTAGE DETECTOR.



DEBUG CARD CONN.





PEGATRON Title : MDC/ PWR SW/ Debug

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 65 of 77

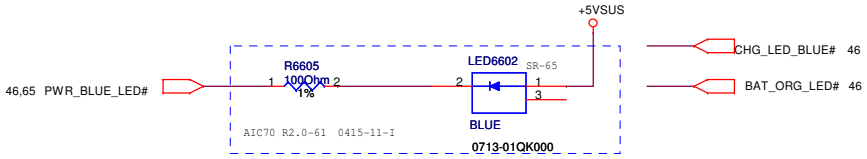
LED (Main)

Left ⟵ ⟶ Right

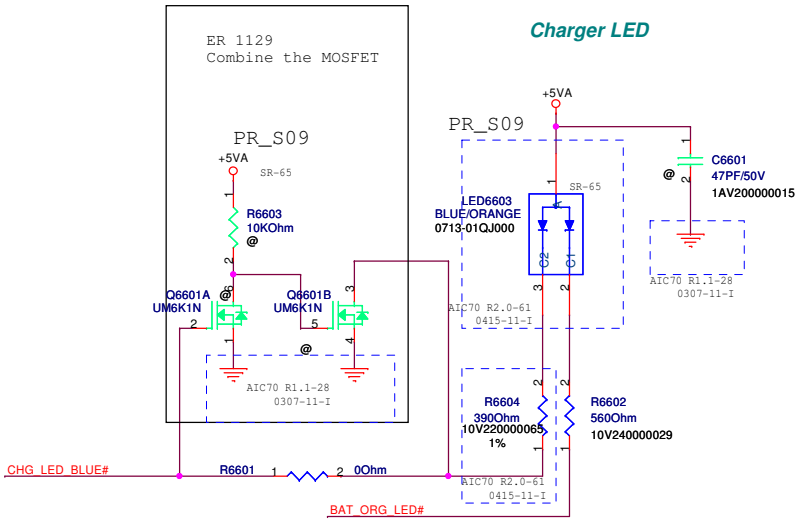
DC-IN	Power	Main Battery	HDD/ODD	Bridge Media	WiFi
White	White Amber (Blink)	White Amber (Blink)	White	White	Amber

Battery

Power LED



Charger LED

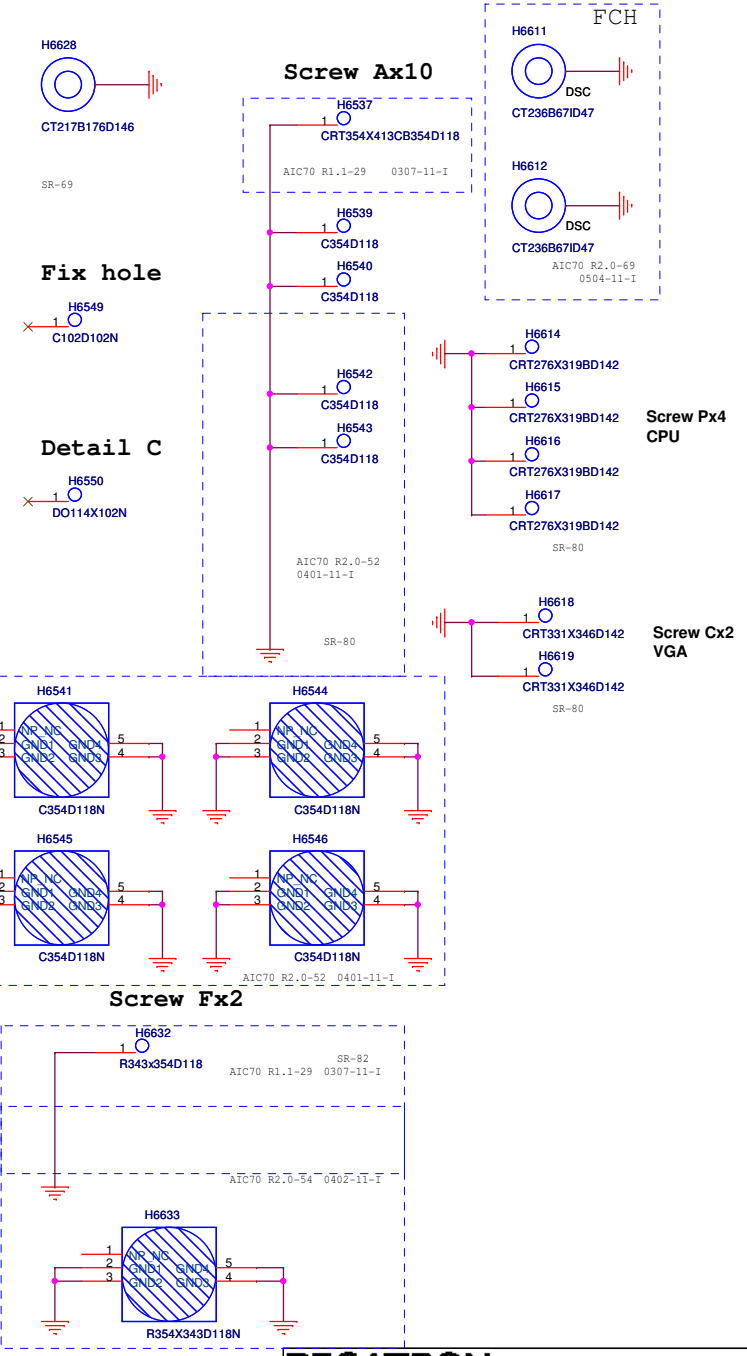


Remover LED circuit SR-18 0124-11

Modify LED circuit SR-28 0124-11 SR-39 0125-11

PCH Local Side Symbol

WLAN NUT



PEGATRON Title : LED/ CIR/ FN/ SCREW

BU1-RD Div.1-HW RD Dept.1 Engineer: Johnson Huang

Size	Project Name	Rev
Custom	AIC70	2.0

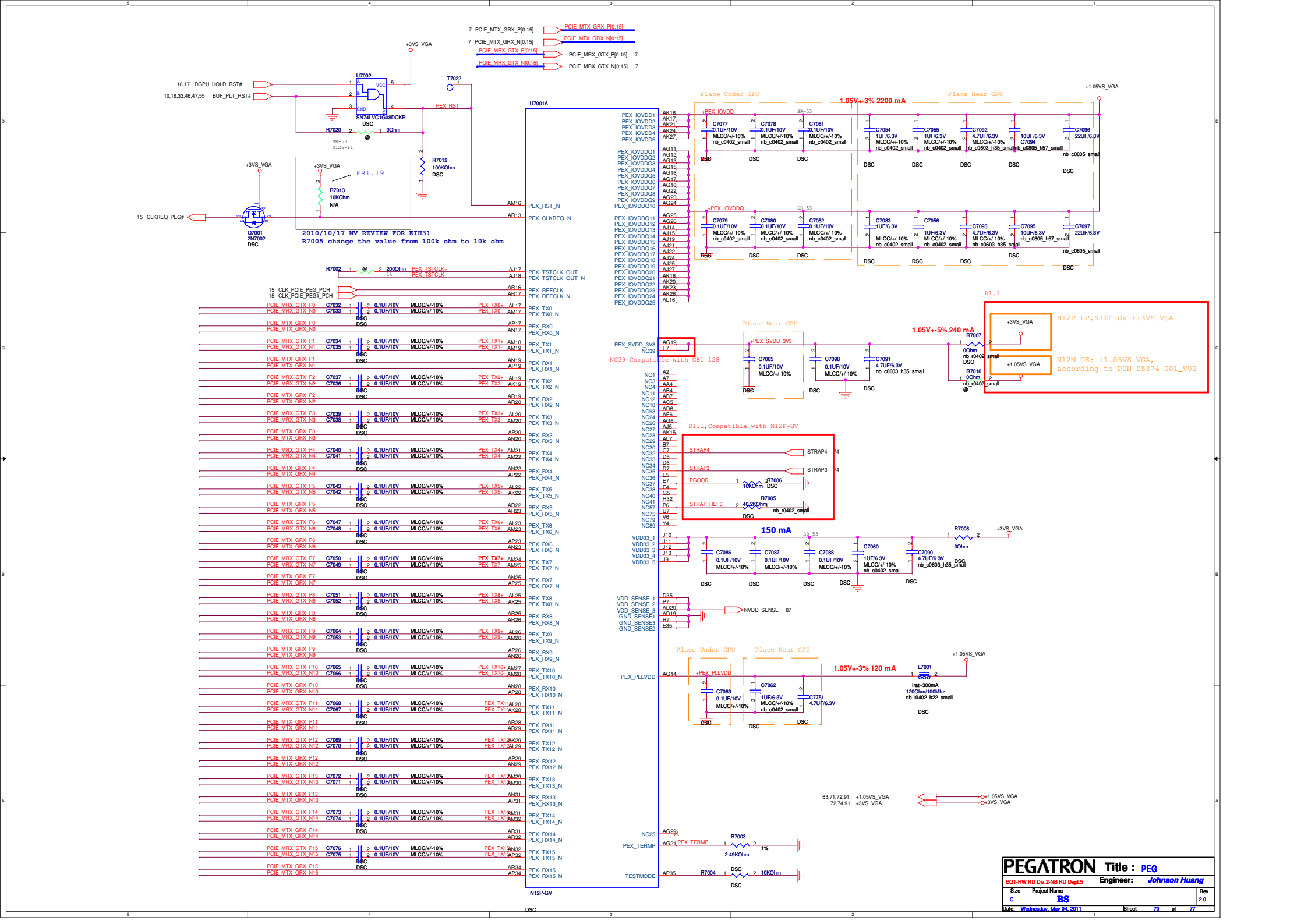
Date: Wednesday, May 04, 2011 Sheet 66 of 77

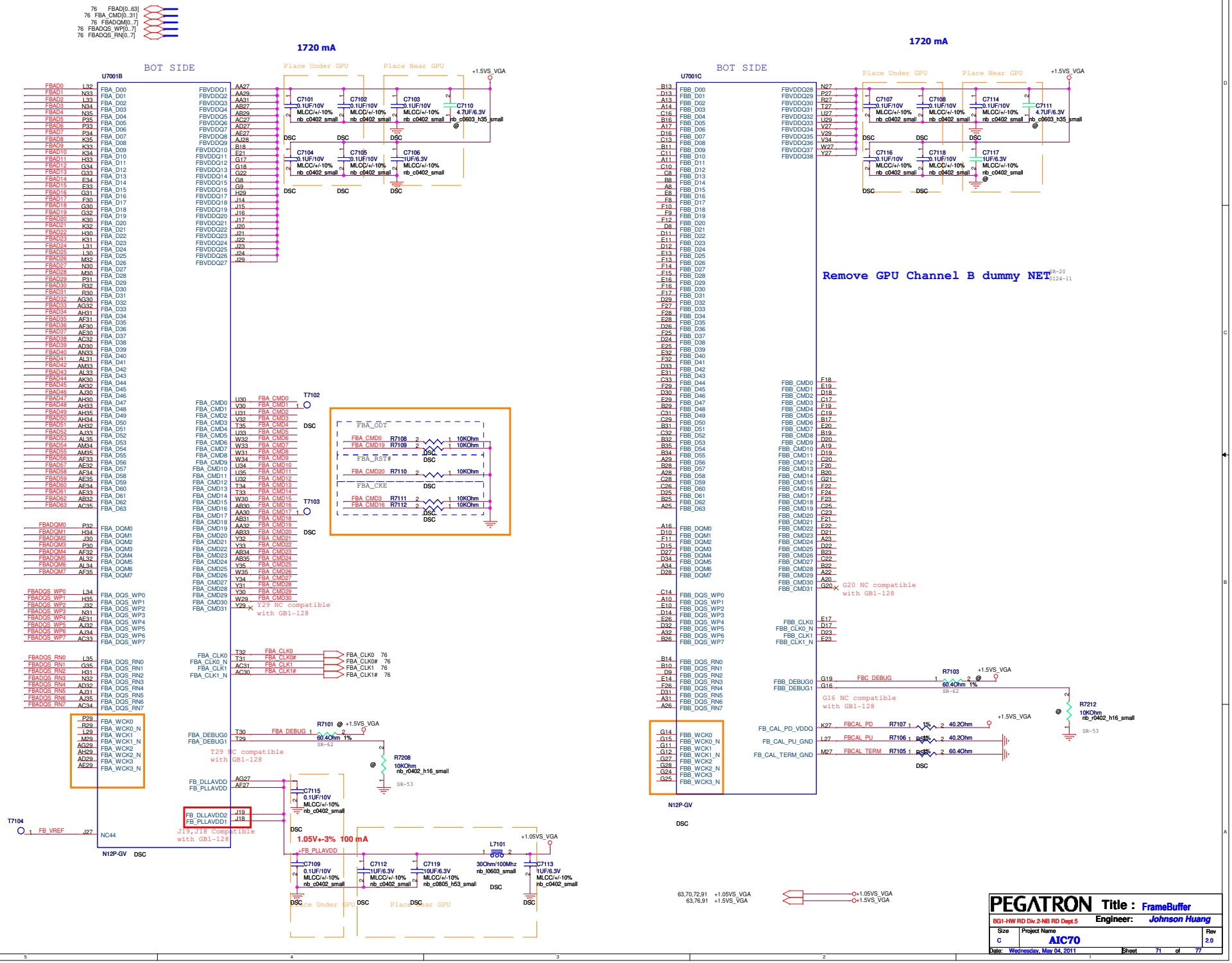
PEGATRON Title : G-Sensor TSH35TR

BU1-RD Div.1-HW RD Dept.1 Engineer: *Johnson Huang*

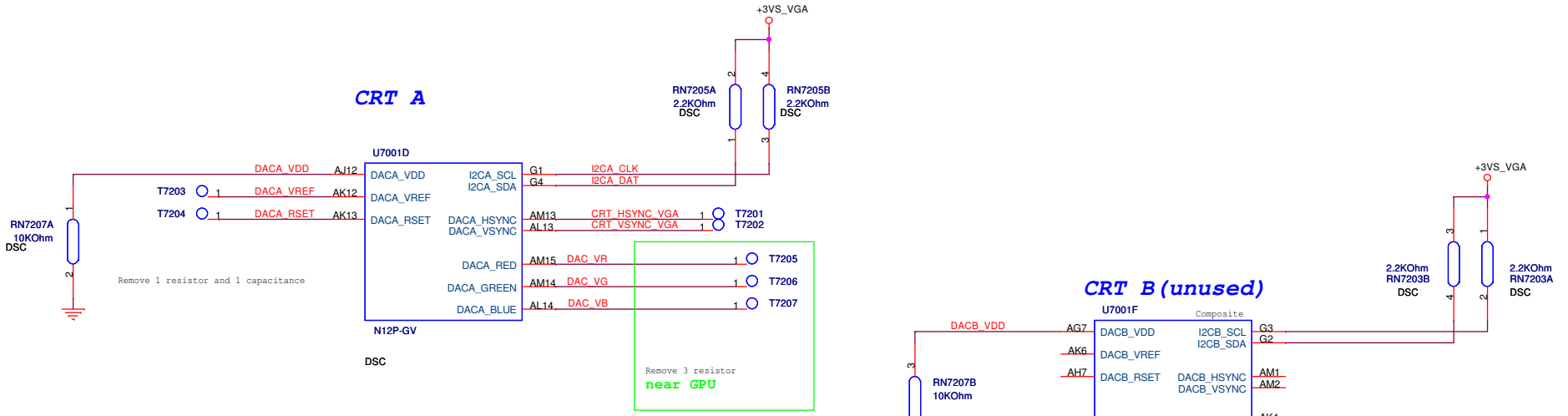
Size	Project Name	Rev
Custom		2.0

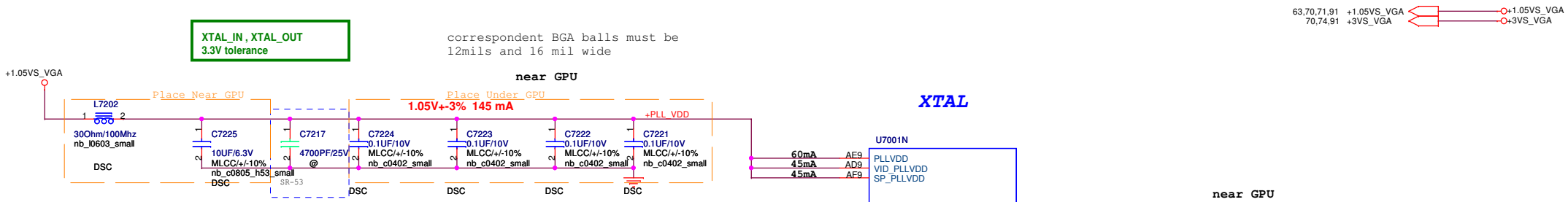
Date: Wednesday, May 04, 2011 Sheet 69 of 77


7 PCIE_MTX_GRX_P[0:15]
PCIE_MTX_GRX_P[0:15]
7 PCIE_MTX_GRX_N[0:15]
PCIE_MTX_GRX_N[0:15]
PCIE_MRX_GTX_P[0:15]
PCIE_MRX_GTX_P[0:15] 7
PCIE_MRX_GTX_N[0:15]
PCIE_MRX_GTX_N[0:15] 7
+3VS_VGA
16,17 DGPU_HOLD_RST#
10,16,33,46,47,55 BUF_PLT_RST#
U7002
SN74LVC1G08DCKR
DSC
T7022
PEX_RST
R7020 0Ohm
SR-53
0126-11
R7012
100KOhm
DSC
ER1.19
R7013
10KOhm
N/A
15 CLKREQ_PEG#
Q7001
2N7002
DSC
2010/10/17 NV REVIEW FOR EIH31
R7005 change the value from 100k ohm to 10k ohm
U7001A
PEX_RST_N
PEX_CLKREQ_N
R7002 200Ohm
PEX_TSTCLK+
PEX_TSTCLK-
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
15 CLK_PCIE_PEG_PCH
15 CLK_PCIE_PEG#_PCH
PEX_REFCLK
PEX_REFCLK_N
PCIE_MRX_GTX_P0
PCIE_MRX_GTX_N0
PCIE_MTX_GRX_P0
PCIE_MTX_GRX_N0
PEX_TX0+
PEX_TX0-
PEX_RX0
PEX_RX0_N
PCIE_MRX_GTX_P1
PCIE_MRX_GTX_N1
PCIE_MTX_GRX_P1
PCIE_MTX_GRX_N1
PEX_TX1+
PEX_TX1-
PEX_TX1
PEX_TX1_N
PEX_RX1
PEX_RX1_N
PCIE_MRX_GTX_P2
PCIE_MRX_GTX_N2
PCIE_MTX_GRX_P2
PCIE_MTX_GRX_N2
PEX_TX2+
PEX_TX2-
PEX_TX2
PEX_TX2_N
PEX_RX2
PEX_RX2_N
PCIE_MRX_GTX_P3
PCIE_MRX_GTX_N3
PCIE_MTX_GRX_P3
PCIE_MTX_GRX_N3
PEX_TX3+
PEX_TX3-
PEX_TX3
PEX_TX3_N
PEX_RX3
PEX_RX3_N
PCIE_MRX_GTX_P4
PCIE_MRX_GTX_N4
PCIE_MTX_GRX_P4
PCIE_MTX_GRX_N4
PEX_TX4+
PEX_TX4-
PEX_TX4
PEX_TX4_N
PEX_RX4
PEX_RX4_N
PCIE_MRX_GTX_P5
PCIE_MRX_GTX_N5
PCIE_MTX_GRX_P5
PCIE_MTX_GRX_N5
PEX_TX5+
PEX_TX5-
PEX_TX5
PEX_TX5_N
PEX_RX5
PEX_RX5_N
PCIE_MRX_GTX_P6
PCIE_MRX_GTX_N6
PCIE_MTX_GRX_P6
PCIE_MTX_GRX_N6
PEX_TX6+
PEX_TX6-
PEX_TX6
PEX_TX6_N
PEX_RX6
PEX_RX6_N
PCIE_MRX_GTX_P7
PCIE_MRX_GTX_N7
PCIE_MTX_GRX_P7
PCIE_MTX_GRX_N7
PEX_TX7+
PEX_TX7-
PEX_TX7
PEX_TX7_N
PEX_RX7
PEX_RX7_N
PCIE_MRX_GTX_P8
PCIE_MRX_GTX_N8
PCIE_MTX_GRX_P8
PCIE_MTX_GRX_N8
PEX_TX8+
PEX_TX8-
PEX_TX8
PEX_TX8_N
PEX_RX8
PEX_RX8_N
PCIE_MRX_GTX_P9
PCIE_MRX_GTX_N9
PCIE_MTX_GRX_P9
PCIE_MTX_GRX_N9
PEX_TX9+
PEX_TX9-
PEX_TX9
PEX_TX9_N
PEX_RX9
PEX_RX9_N
PCIE_MRX_GTX_P10
PCIE_MRX_GTX_N10
PCIE_MTX_GRX_P10
PCIE_MTX_GRX_N10
PEX_TX10+
PEX_TX10-
PEX_TX10
PEX_TX10_N
PEX_RX10
PEX_RX10_N
PCIE_MRX_GTX_P11
PCIE_MRX_GTX_N11
PCIE_MTX_GRX_P11
PCIE_MTX_GRX_N11
PEX_TX11+
PEX_TX11-
PEX_TX11
PEX_TX11_N
PEX_RX11
PEX_RX11_N
PCIE_MRX_GTX_P12
PCIE_MRX_GTX_N12
PCIE_MTX_GRX_P12
PCIE_MTX_GRX_N12
PEX_TX12+
PEX_TX12-
PEX_TX12
PEX_TX12_N
PEX_RX12
PEX_RX12_N
PCIE_MRX_GTX_P13
PCIE_MRX_GTX_N13
PCIE_MTX_GRX_P13
PCIE_MTX_GRX_N13
PEX_TX13+
PEX_TX13-
PEX_TX13
PEX_TX13_N
PEX_RX13
PEX_RX13_N
PCIE_MRX_GTX_P14
PCIE_MRX_GTX_N14
PCIE_MTX_GRX_P14
PCIE_MTX_GRX_N14
PEX_TX14+
PEX_TX14-
PEX_TX14
PEX_TX14_N
PEX_RX14
PEX_RX14_N
PCIE_MRX_GTX_P15
PCIE_MRX_GTX_N15
PCIE_MTX_GRX_P15
PCIE_MTX_GRX_N15
PEX_TX15+
PEX_TX15-
PEX_TX15
PEX_TX15_N
PEX_RX15
PEX_RX15_N
0.1UF/10V MLCC/+/-10% DSC
N12P-GV
PEX_IOVDD1
PEX_IOVDD2
PEX_IOVDD3
PEX_IOVDD4
PEX_IOVDD5
PEX_IOVDDQ1
PEX_IOVDDQ2
PEX_IOVDDQ3
PEX_IOVDDQ4
PEX_IOVDDQ5
PEX_IOVDDQ6
PEX_IOVDDQ7
PEX_IOVDDQ8
PEX_IOVDDQ9
PEX_IOVDDQ10
PEX_IOVDDQ11
PEX_IOVDDQ12
PEX_IOVDDQ13
PEX_IOVDDQ14
PEX_IOVDDQ15
PEX_IOVDDQ16
PEX_IOVDDQ17
PEX_IOVDDQ18
PEX_IOVDDQ19
PEX_IOVDDQ20
PEX_IOVDDQ21
PEX_IOVDDQ22
PEX_IOVDDQ23
PEX_IOVDDQ24
PEX_IOVDDQ25
Place Under GPU
Place Near GPU
1.05V+-3% 2200 mA
+PEX_IOVDD
C7077 0.1UF/10V MLCC/+/-10% nb_c0402_small
C7078 0.1UF/10V MLCC/+/-10% nb_c0402_small
C7081 0.1UF/10V MLCC/+/-10% nb_c0402_small
C7054 1UF/6.3V MLCC/+/-10% nb_c0402_small
C7055 1UF/6.3V MLCC/+/-10% nb_c0402_small
C7092 4.7UF/6.3V MLCC/+/-10% nb_c0603_h35_small
C7094 10UF/6.3V nb_c0805_h57_small
C7096 22UF/6.3V nb_c0805_small
+PEX_IOVDDQ
C7079 0.1UF/10V MLCC/+/-10% nb_c0402_small
C7080 0.1UF/10V MLCC/+/-10% nb_c0402_small
C7082 0.1UF/10V MLCC/+/-10% nb_c0402_small
C7083 1UF/6.3V MLCC/+/-10% nb_c0402_small
C7056 1UF/6.3V MLCC/+/-10% nb_c0402_small
C7093 4.7UF/6.3V MLCC/+/-10% nb_c0603_h35_small
C7095 10UF/6.3V nb_c0805_h57_small
C7097 22UF/6.3V nb_c0805_small
SR-53
DSC
+1.05VS_VGA
R1.1
N12P-LP,N12P-GV :+3VS_VGA
N12M-GE: +1.05VS_VGA, according to PUN-05374-001_V02
PEX_SVDD_3V3
NC39
NC39 Compatible with GB1-128
1.05V+-5% 240 mA
+PEX_SVDD_3V3
C7085 0.1UF/10V MLCC/+/-10%
C7098 0.1UF/10V MLCC/+/-10%
C7091 4.7UF/6.3V nb_c0603_h35_small
R7007 0Ohm nb_r0402_small
R7010 0Ohm nb_r0402_small
NC1
NC3
NC4
NC11
NC12
NC16
NC93
NC24
NC26
NC27
NC28
NC29
NC30
NC32
NC33
NC34
NC35
NC36
NC37
NC38
NC40
NC41
NC57
NC75
NC79
NC89
R1.1,Compatible with N12P-GV
STRAP4
STRAP3
PGOOD
R7006 10KOhm DSC
STRAP_REF3
R7005 40.2KOhm nb_r0402_small
150 mA
VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5
C7086 0.1UF/10V MLCC/+/-10%
C7087 0.1UF/10V MLCC/+/-10%
C7088 0.1UF/10V MLCC/+/-10%
C7060 1UF/6.3V MLCC/+/-10% nb_c0402_small
C7090 4.7UF/6.3V nb_c0603_h35_small
R7008 0Ohm
VDD_SENSE_1
VDD_SENSE_2
VDD_SENSE_3
GND_SENSE1
GND_SENSE3
GND_SENSE2
NVDD_SENSE 87
Place Under GPU
Place Near GPU
PEX_PLLVDD
+PEX_PLLVDD
1.05V+-3% 120 mA
C7089 0.1UF/10V MLCC/+/-10%
C7062 1UF/6.3V MLCC/+/-10% nb_c0402_small
C7751 4.7UF/6.3V
L7001 Irat=300mA 120Ohm/100Mhz nb_l0402_h22_small
63,71,72,91 +1.05VS_VGA
72,74,91 +3VS_VGA
NC25
PEX_TERMP
R7003 2.49KOhm 1%
TESTMODE
R7004 10KOhm
PEGATRON
Title : PEG
BG1-HW RD Div.2-NB RD Dept.5
Engineer: Johnson Huang
Size C
Project Name BS
Rev 2.0
Date: Wednesday, May 04, 2011
Sheet 70 of 77



PEGATRON	Title : FrameBuffer		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Johnson Huang		
Size: C	Project Name: AIC70		Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 71 of 77		





PEGATRON

Title : CRT, XTAL

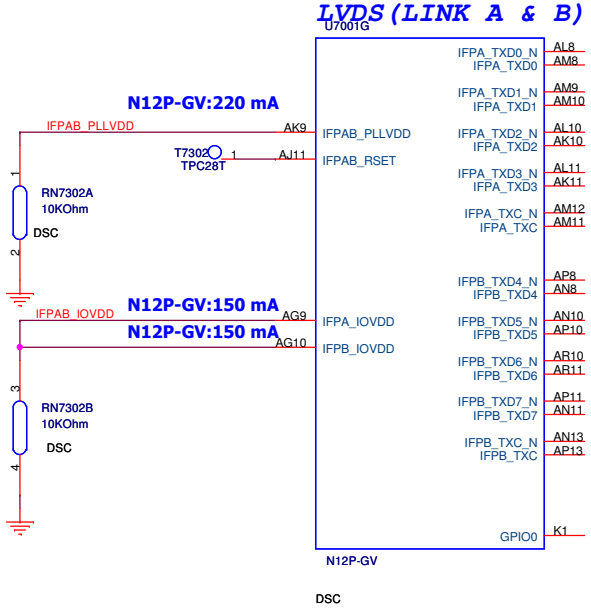
BG1-HW RD Div.2-NB RD Dept.5

Engineer: Johnson Huang

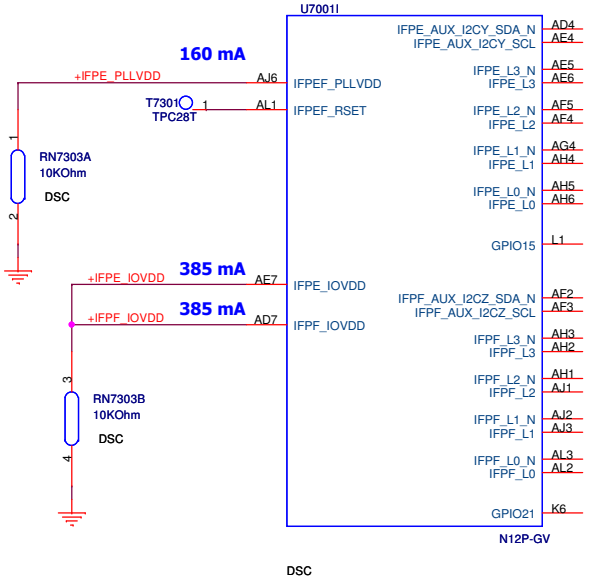
Size	Project Name	Rev
Custom	AIC70	2.0

Date: Wednesday, May 04, 2011 Sheet 72 of 77

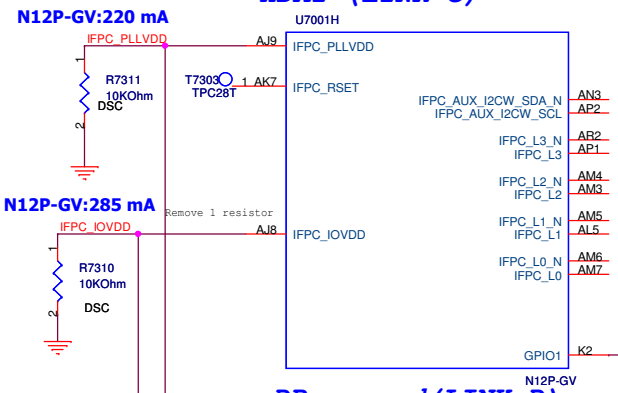
LVDS (LINK A & B)



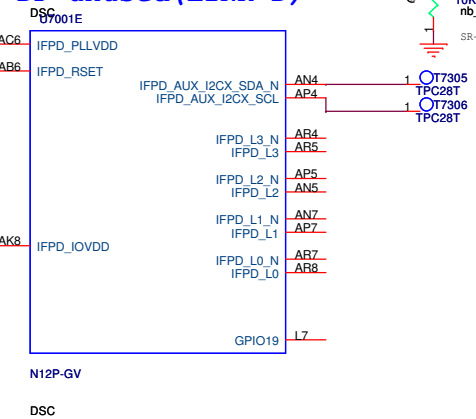
DP unused (LINK E & F)



HDMI (LINK C)



DP unused (LINK D)

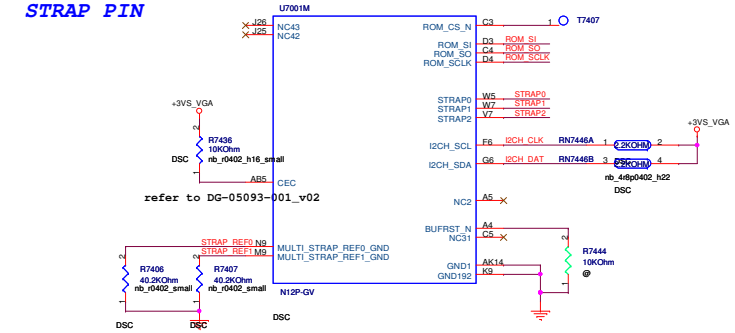


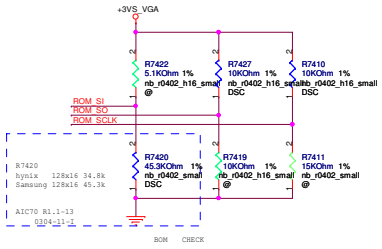
IFPx	A	B	C	D E F
TURKEY	LVDS A	LVDS B	HDMI	unused

63,70,71,72,91 +1.05VS_VGA → +1.05VS_VGA
63,91 +1.8VS_VGA → +1.8VS_VGA
70,72,74,91 +3VS_VGA → +3VS_VGA

PEGATRON Title : LVDS, HDMI
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Johnson Huang
Size: Custom | Project Name: AIC70 | Rev: 2.0
Date: Wednesday, May 04, 2011 | Sheet 73 of 77

STRAP PIN





5K	PU 1000 PD 0000
10K	PU 1001 PD 0001
15K	PU 1010 PD 0010
20K	PU 1011 PD 0011
25K	PU 1100 PD 0100
30K	PU 1101 PD 0101
35K	PU 1110 PD 0110
45K	PU 1111 PD 0111

refer to PUN-05374-001

STRAP0

USER[3:0]

3	2	1	0	PANEL	VS/HS
0	0	0	0	XGA	-/-
0	0	0	1	XGA	+/+
0	0	1	0	SXGA	+/+
0	0	1	1	SXGA+	-/-
0	1	0	0	UXGA	+/+
1	1	1	1	EDID	N/A

STRAP1

3GIO_PAD_CFG_ADR[3:0]

3	2	1	0	PANEL
0	0	0	0	RESERVED
.				
1	1	1	0	NOTEBOOK default
1	1	1	1	RESERVED

STRAP2

LOGICAL BIT

0	PCI_DEVID[0]
1	PCI_DEVID[1]
2	PCI_DEVID[2]
3	PCI_DEVID[3]

ROM_SI RAMCONFIG (MONO RAM)

```
Hynix 64Mx16    -> ram_cfg = 0x2
Samsung 64Mx16  -> ram_cfg = 0x3
Hynix 128Mx16   -> ram_cfg = 0x6
Samsung 128Mx16 -> ram_cfg = 0x7
```

ROM_SO

LOGICAL BIT

3	XCLK_417
2	FB_0_BAR_SIZE
1	SMB_ALT_ADDR
0	VGA_DEVICE

ROM_SCLK

LOGICAL BIT

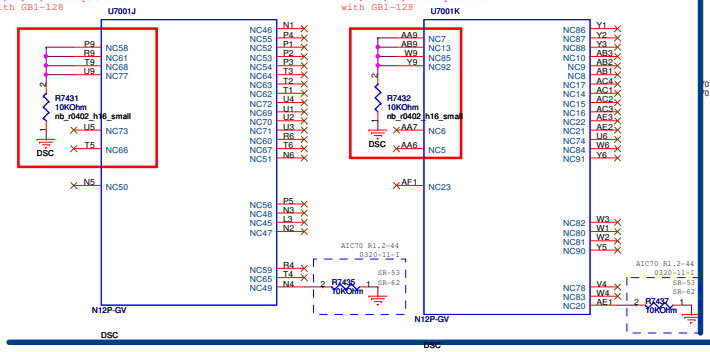
3	PCI_DEVID[4]
2	SUB_VENDER
1	SLOT_CLK_CFG
0	PEX_PLL_EN_TERM

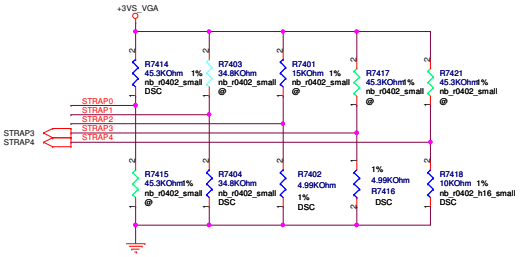
70,72,91 +3VS_VGA → +3VS_VGA

Muti I/O unused

P9,R8,W9,T9 Compatible with GB1-128

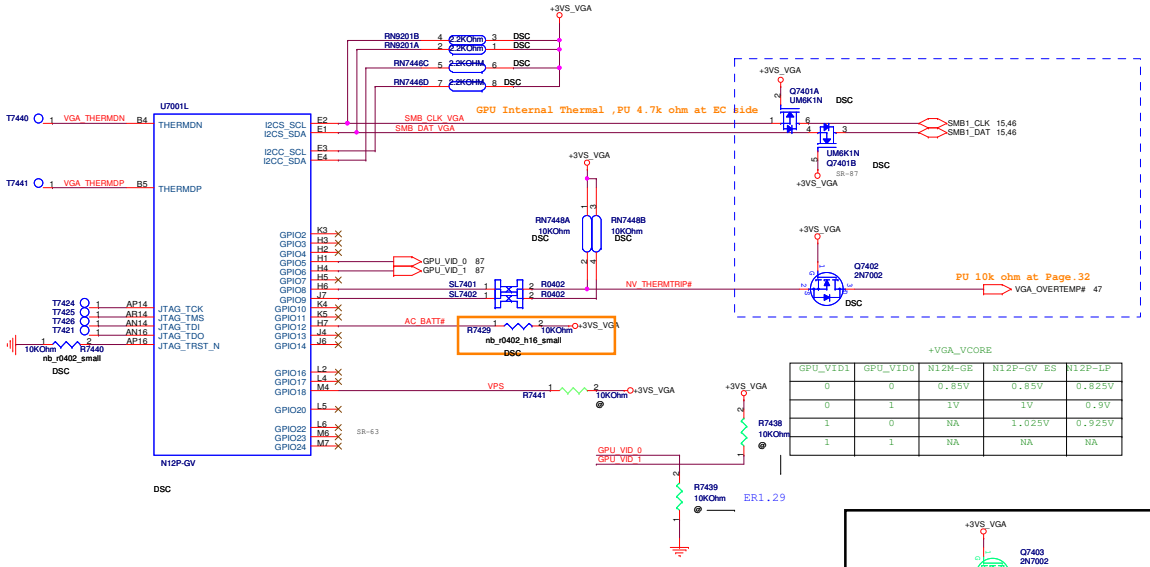
AA9,AB8,W9,Y9 Compatible with GB1-128





			N12P-LP QS		N12P-GV ES		N12M-GE QS	
			PU	PD	PU	PD	PU	PD
ROM_SO	R7427	R7419	@	10K	@	10K	@	10K
ROM_SCLK	R7410	R7411	@	15K	15K	@	15K	@
ROM_SI	R7422	R7420	@	H 64:15K S 64:20K	@	H 64:15K S 64:20K	@	H 64:15K S 64:20K
Strap2	R7401	R7402	25K	@	45K	@	15K	@
Strap1	R7403	R7404	@	35K	@	35K	@	35K
Strap0	R7414	R7415	45K	@	45K	@	45K	@
Strap3	R7417	R7416	@	@	@	20k	@	@
Strap4	R7421	R7418	@	@	@	10k	@	@

GPIO, THERM, SMBUS, JTAG, LVDS MISC, GPU_VID



+VGA_VCORE

GPU_VID1	GPU_VID0	N12M-GE	N12P-GV ES	N12P-LP
0	0	0.85V	0.85V	0.825V
0	1	1V	1V	0.9V
1	0	NA	1.025V	0.925V
1	1	NA	NA	NA

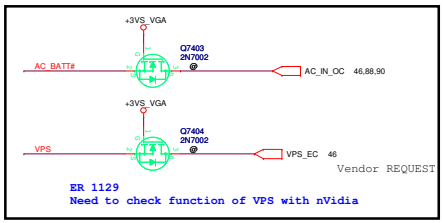


Table 12.1 GPIO Description

GPIO PIN Name	Normal Function	I/O	Functional Description
GPIO0	General Purpose		
GPIO1	HPD_C	I	Hot Plug Detect for IFPC
GPIO2	LCD0_BL_PWM	O	Panel Backlight Brightness Control (PWM capable)
GPIO3	LCD0_VCC	O	Panel Power Enable
GPIO4	LCD0_BLEN	O	Panel Backlight ON/OFF Control (PWM capable)
GPIO5	GPU_VID0	O	GPU Core VDD VID0
GPIO6	GPU_VID1	O	GPU Core VDD VID1
GPIO7	GPU_VID2	O	GPU Core VDD VID2
GPIO8	OVERT	I/O	Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	SLI_RASTER_SYNC	I/O	SLI Raster Sync
GPIO12	PWR_LEVEL	I	AC Power Detect Input
GPIO13	THERM_LOAD_STEP_DOWN	O	Power Supply Control
GPIO14	THERM_LOAD_STEP_UP	O	Power Supply Control
GPIO15	HPD_E	I	Hot Plug Detect for IFPE
GPIO16	FAN_PWM	O	Programmable Fan Control
GPIO17	Reserved		
GPIO18	Reserved		
GPIO19	HPD_D	I	Hot Plug Detect for IFPD
GPIO20	Reserved		
GPIO21	HPD_F	I	Hot Plug Detect for IFPF
GPIO22	SWAPRDY	I	SLI Swap Ready Signal
GPIO23	3DVision	O	3DVision functions
GPIO24	General Purpose		

PEGATRON Title : STRAP,THERM,ROM,MIO

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Johnson Huang

Size: Custom | Project Name: AIC70 | Rev: 2.0

Date: Wednesday, May 04, 2011 | Sheet 74 of 77

GND

U7001O

AA11	GND2	GND97	E15
AA12	GND3	GND98	E18
AA13	GND4	GND99	E24
AA14	GND5	GND100	E27
AA15	GND6	GND101	E30
AA16	GND7	GND102	E6
AA17	GND8	GND103	E9
AA18	GND9	GND104	F2
AA19	GND10	GND105	F31
AA2	GND11	GND106	F34
AA20	GND12	GND107	F5
AA21	GND13	GND108	J2
AA22	GND14	GND109	J31
AA23	GND15	GND110	J34
AA24	GND16	GND111	J5
AA25	GND17	GND112	L9
AA34	GND18	GND113	M11
AA5	GND19	GND114	M13
AB12	GND20	GND115	M15
AB14	GND21	GND116	M17
AB16	GND22	GND117	M19
AB18	GND23	GND118	M2
AB20	GND24	GND119	M21
AB22	GND25	GND120	M23
AB24	GND26	GND121	M25
AC9	GND27	GND122	M31
AD11	GND28	GND123	M34
AD13	GND29	GND124	M5
AD15	GND30	GND125	N11
AD17	GND31	GND126	N12
AD2	GND32	GND127	N13
AD21	GND33	GND128	N14
AD23	GND34	GND129	N15
AD25	GND35	GND130	N16
AD31	GND36	GND131	N17
AD34	GND37	GND132	N18
AD5	GND38	GND133	N19
AE11	GND39	GND134	N20
AE12	GND40	GND135	N21
AE13	GND41	GND136	N22
AE14	GND42	GND137	N23
AE15	GND43	GND138	N24
AE16	GND44	GND139	N25
AE17	GND45	GND140	P12
AE18	GND46	GND141	P14
AE19	GND47	GND142	P16
AE20	GND48	GND143	P18
AE21	GND49	GND144	P20
AE22	GND50	GND145	P22
AE23	GND51	GND146	P24
AE24	GND52	GND147	R2
AE25	GND53	GND148	R31
AG2	GND54	GND149	R34
AG31	GND55	GND150	R5
AG34	GND56	GND151	T11
AG5	GND57	GND152	T13
AK2	GND58	GND153	T15
AK31	GND59	GND154	T17
AK34	GND60	GND155	T19
AK5	GND61	GND156	T21
AL12	GND62	GND157	T23
AL15	GND63	GND158	T25
AL18	GND64	GND159	U11
AL21	GND65	GND160	U12
AL24	GND66	GND161	U13
AL27	GND67	GND162	U14
AL30	GND68	GND163	U15
AL6	GND69	GND164	U16
AL9	GND70	GND165	U17
AN2	GND71	GND166	U18
AN34	GND72	GND167	U19
AP12	GND73	GND168	U20
AP15	GND74	GND169	U21
AP18	GND75	GND170	U22
AP21	GND76	GND171	U23
AP24	GND77	GND172	U24
AP27	GND78	GND173	U25
AP3	GND79	GND174	V12
AP30	GND80	GND175	V14
AP33	GND81	GND176	V16
AP6	GND82	GND177	V18
AP9	GND83	GND178	V2
B12	GND84	GND179	V20
B15	GND85	GND180	V22
B21	GND86	GND181	V24
B24	GND87	GND182	V31
B27	GND88	GND183	V5
B3	GND89	GND184	V9
B30	GND90	GND185	Y11
B33	GND91	GND186	Y13
B6	GND92	GND187	Y15
B9	GND93	GND188	Y17
C2	GND94	GND189	Y19
C34	GND95	GND190	Y21
E12	GND96	GND191	Y23
		GND192	Y25

N12P-GV

DSC

VAG_VCORE

+VGA_VCORE +VGA_VCORE

U7001P

AB11	VDD1	VDD57	P21
AB13	VDD2	VDD58	P23
AB15	VDD3	VDD59	P25
AB17	VDD4	VDD60	R11
AB19	VDD5	VDD61	R12
AB21	VDD6	VDD62	R13
AB23	VDD7	VDD63	R14
AB25	VDD8	VDD64	R15
AC11	VDD9	VDD65	R16
AC12	VDD10	VDD66	R17
AC13	VDD11	VDD67	R18
AC14	VDD12	VDD68	R19
AC15	VDD13	VDD69	R20
AC16	VDD14	VDD70	R21
AC17	VDD15	VDD71	R22
AC18	VDD16	VDD72	R23
AC19	VDD17	VDD73	R24
AC20	VDD18	VDD74	R25
AC21	VDD19	VDD75	T12
AC22	VDD20	VDD76	T14
AC23	VDD21	VDD77	T16
AC24	VDD22	VDD78	T18
AC25	VDD23	VDD79	T20
AD12	VDD24	VDD80	T22
AD14	VDD25	VDD81	T24
AD16	VDD26	VDD82	V11
AD18	VDD27	VDD83	V13
AD22	VDD28	VDD84	V15
AD24	VDD29	VDD85	V17
L11	VDD30	VDD86	V19
L12	VDD31	VDD87	V21
L13	VDD32	VDD88	V23
L14	VDD112	VDD89	V25
L15	VDD34	VDD90	W11
L16	VDD35	VDD91	W12
L17	VDD36	VDD92	W13
L18	VDD37	VDD93	W14
L19	VDD38	VDD94	W15
L20	VDD39	VDD95	W16
L21	VDD40	VDD96	W17
L22	VDD41	VDD97	W18
L23	VDD42	VDD98	W19
L24	VDD43	VDD99	W20
L25	VDD44	VDD100	W21
M12	VDD45	VDD101	W22
M14	VDD46	VDD102	W23
M16	VDD47	VDD103	W24
M18	VDD48	VDD104	W25
M20	VDD49	VDD105	Y12
M22	VDD50	VDD106	Y14
M24	VDD51	VDD107	Y16
P11	VDD52	VDD108	Y18
P13	VDD53	VDD109	Y20
P15	VDD54	VDD110	Y22
P17	VDD55	VDD111	Y24
P19	VDD56		

N12P-GV

DSC

20.3 A

+VGA_VCORE

C7501 0.01UF/16V nb_c0402_small	C7502 0.01UF/16V nb_c0402_small	C7503 0.01UF/16V nb_c0402_small	C7504 0.01UF/16V nb_c0402_small	C7505 0.01UF/16V nb_c0402_small	C7506 0.01UF/16V nb_c0402_small
C7507 0.01UF/16V nb_c0402_small	C7509 0.022UF/16V nb_c0402_small	C7510 0.022UF/16V nb_c0402_small	C7511 0.022UF/16V nb_c0402_small	C7512 0.047UF/16V nb_c0402_small	C7513 0.047UF/16V nb_c0402_small
C7514 0.047UF/16V nb_c0402_small	C7515 0.1UF/10V MLCC/+/-10% nb_c0402_small	C7518 0.1UF/10V MLCC/+/-10% nb_c0402_small	C7519 0.22UF/10V nb_c0402_small	C7520 0.22UF/10V nb_c0402_small	C7521 0.22UF/10V nb_c0402_small
C7522 1UF/6.3V nb_c0402_small	C7523 4.7UF/6.3V DSC	C7524 10UF/6.3V nb_r0805_h26_small @	C7525 10UF/6.3V nb_r0805_h26_small @	C7526 10UF/6.3V nb_r0805_h26_small @	C7527 22UF/6.3V nb_c0805_h57_small

DSC

SR-53

PLACE Under GPU

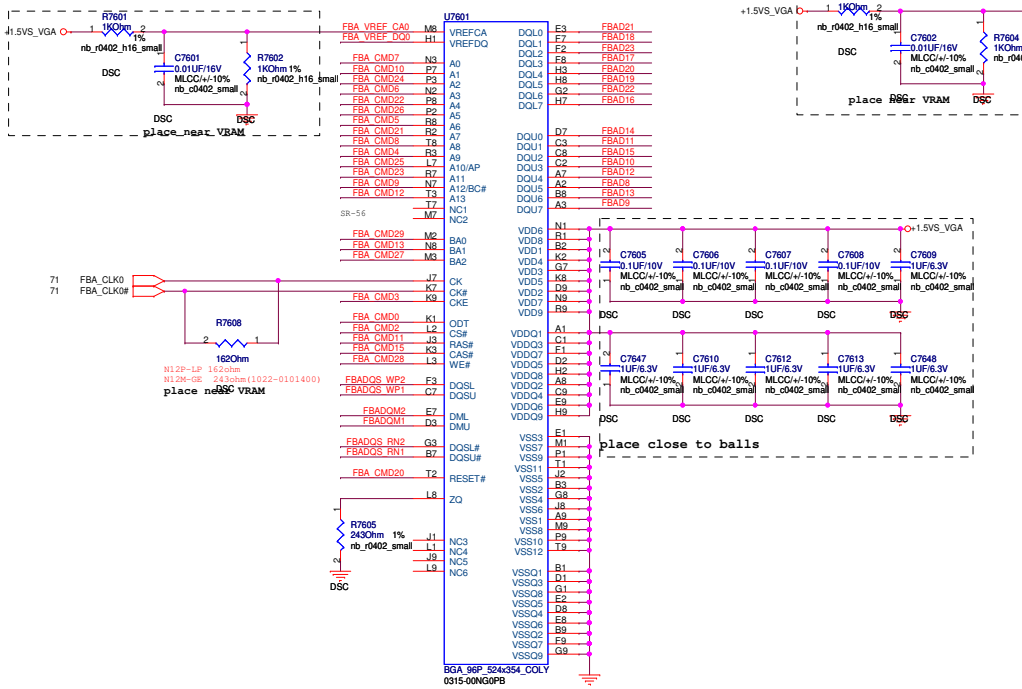
CE7528 470UF/2V PANASONIC/EEFSX0D471E4 @

63,87 +VGA_VCORE +VGA_VCORE

PEGATRON	Title : GPU PWR/GND	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Johnson Huang	
Size: Custom	Project Name: AIC70	Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 75 of 77	

VRAM CH A

TOP SIDE



BOT SIDE

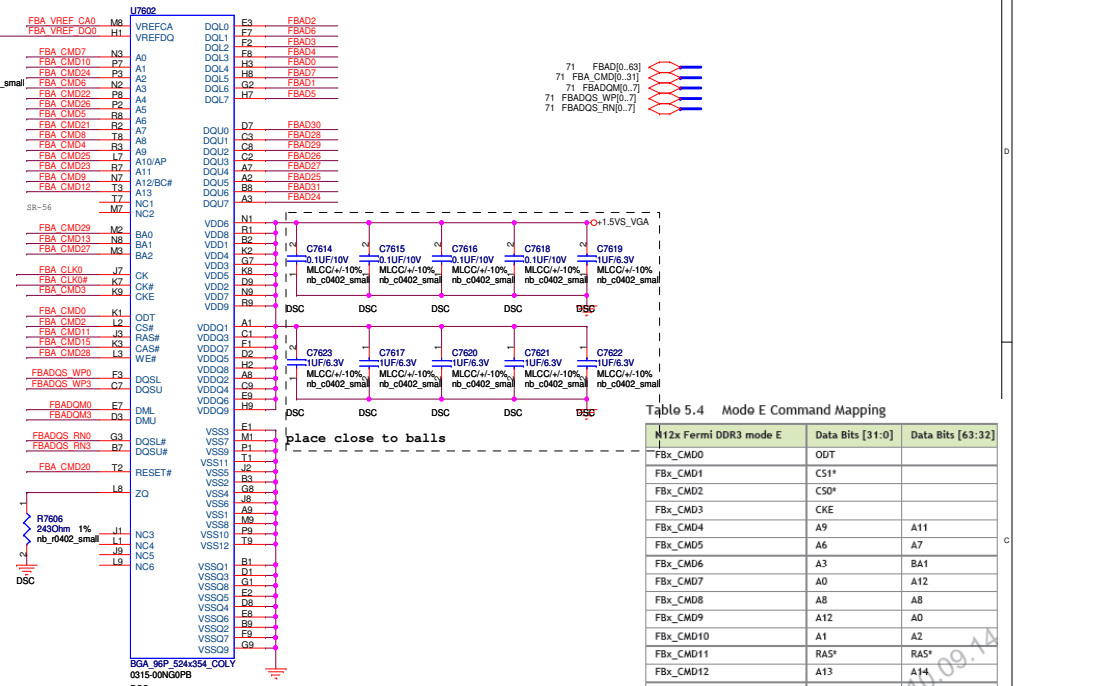
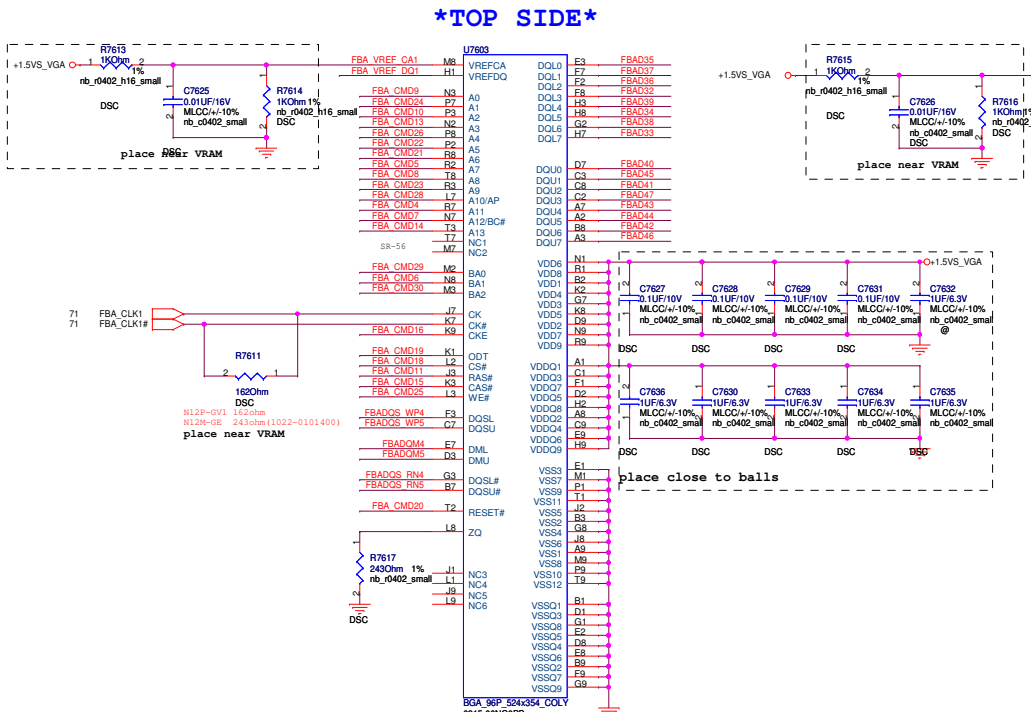


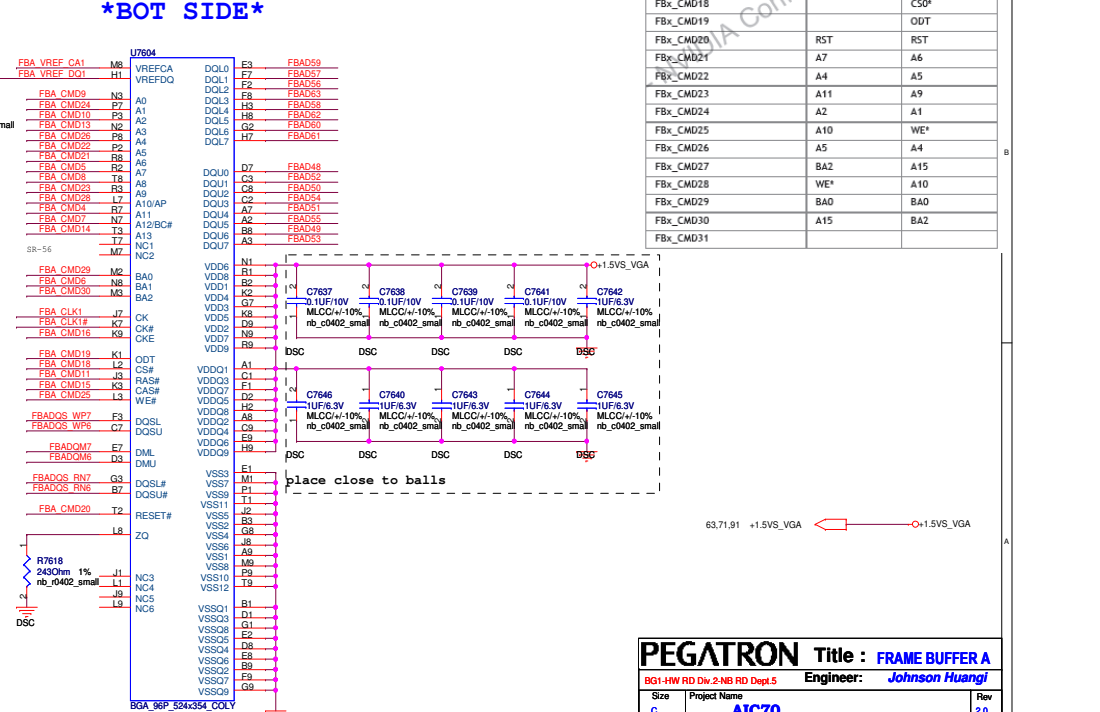
Table 5.4 Mode E Command Mapping

N12x Fermi DDR3 mode E	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	ODT	
FBx_CMD1	CS1*	
FBx_CMD2	CS0*	
FBx_CMD3	CKE	
FBx_CMD4	A9	A11
FBx_CMD5	A6	A7
FBx_CMD6	A3	BA1
FBx_CMD7	A0	A12
FBx_CMD8	A8	A8
FBx_CMD9	A12	A0
FBx_CMD10	A1	A2
FBx_CMD11	RAS*	RAS*
FBx_CMD12	A13	A14
FBx_CMD13	BA1	A3
FBx_CMD14	A14	A13
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CKE
FBx_CMD17		CS1*
FBx_CMD18		CS0*
FBx_CMD19		ODT
FBx_CMD20	RST	RST
FBx_CMD21	A7	A6
FBx_CMD22	A4	A5
FBx_CMD23	A11	A9
FBx_CMD24	A2	A1
FBx_CMD25	A10	WE*
FBx_CMD26	A5	A4
FBx_CMD27	BA2	A15
FBx_CMD28	WE*	A10
FBx_CMD29	BA0	BA0
FBx_CMD30	A15	BA2
FBx_CMD31		

TOP SIDE



BOT SIDE

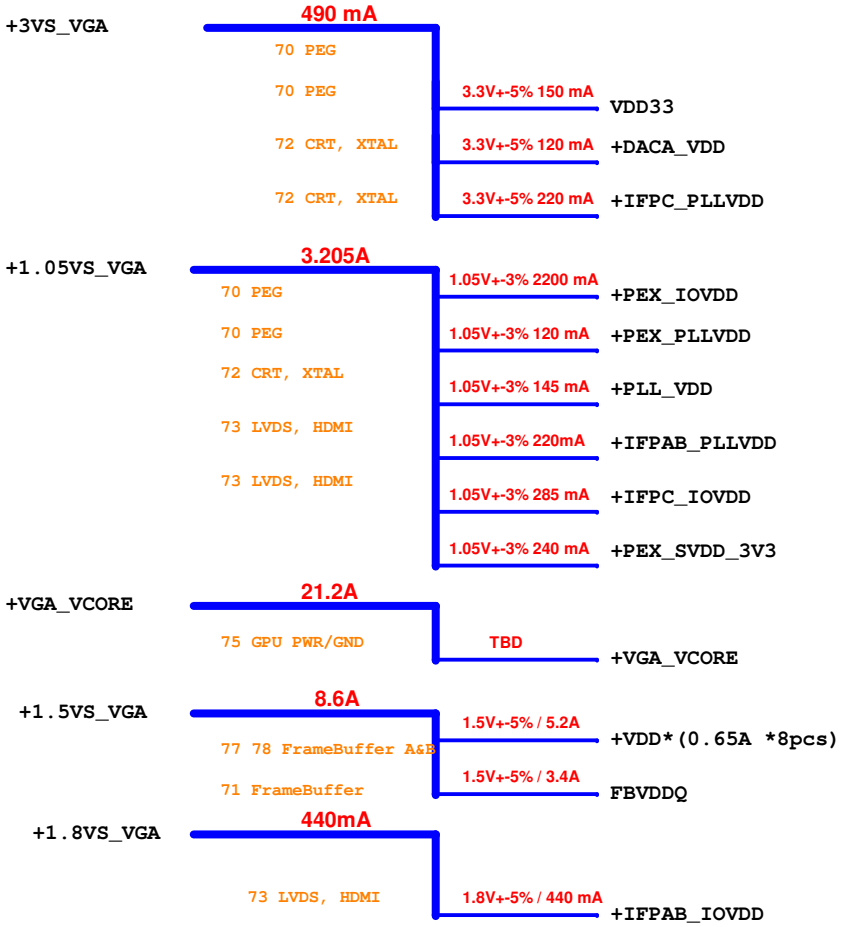


PEGATRON	Title : FRAME BUFFER A		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Johnson Huangi		
Size: C	Project Name: AIC70		Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 76 of 77		

Del B channel VRAM * 4 circuit

SR-10
0121-11

PEGATRON	Title : FRAME BUFFER C		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Johnson Huang		
Size: C	Project Name: AIC70		Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 77 of 77		



N12P-LP Total:40W (w/VRAM)

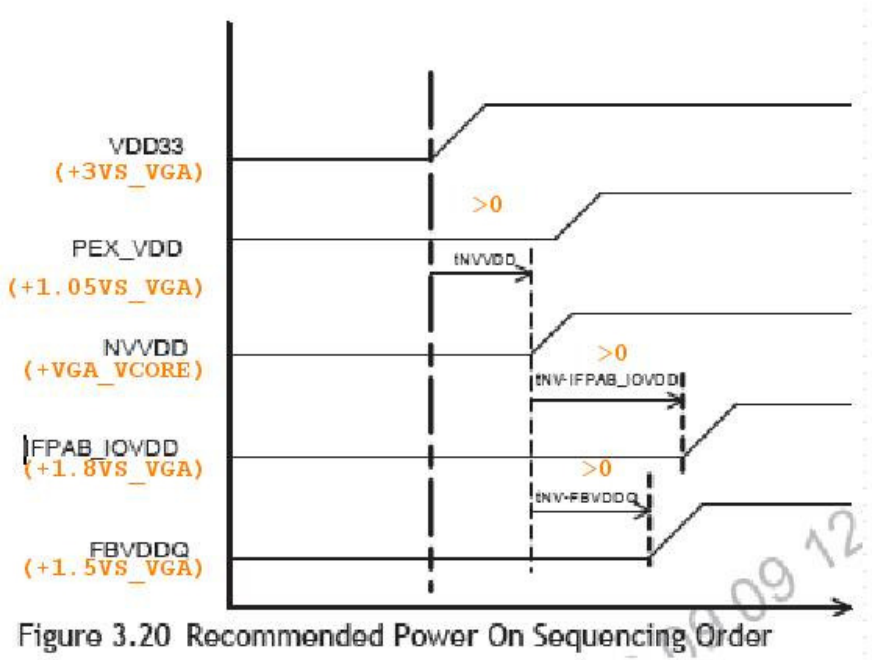


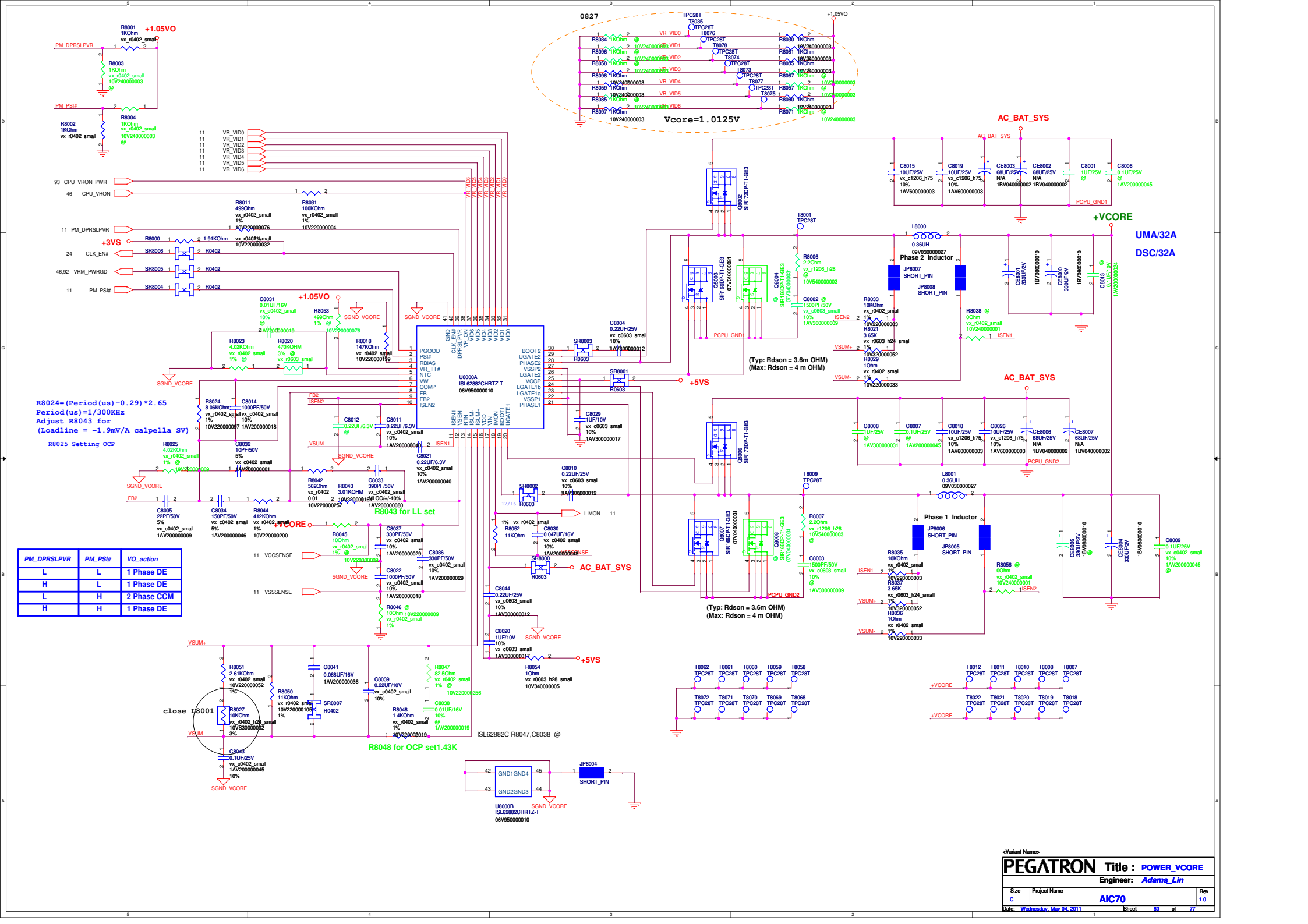
Figure 3.20 Recommended Power On Sequencing Order

Power Up Sequence :
+3VS_VGA -> +1.05VS_VGA -> +VGA_VCORE -> +1.5VS_VGA -> +1.8VS_VGA

Power Down Sequence :
+1.8VS_VGA -> +1.5VS_VGA -> +VGA_VCORE -> 1.05VS_VGA -> +3VS_VGA

according to Page 63, DG-05093-001_v02

PEGATRON	Title : POWER FOLW		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Johnson Huang		
Size: Custom	Project Name: AIC70		Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 79 of 77		



PM_DPRSLPVR	PM_PSI#	VO_action
L	L	1 Phase DE
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE

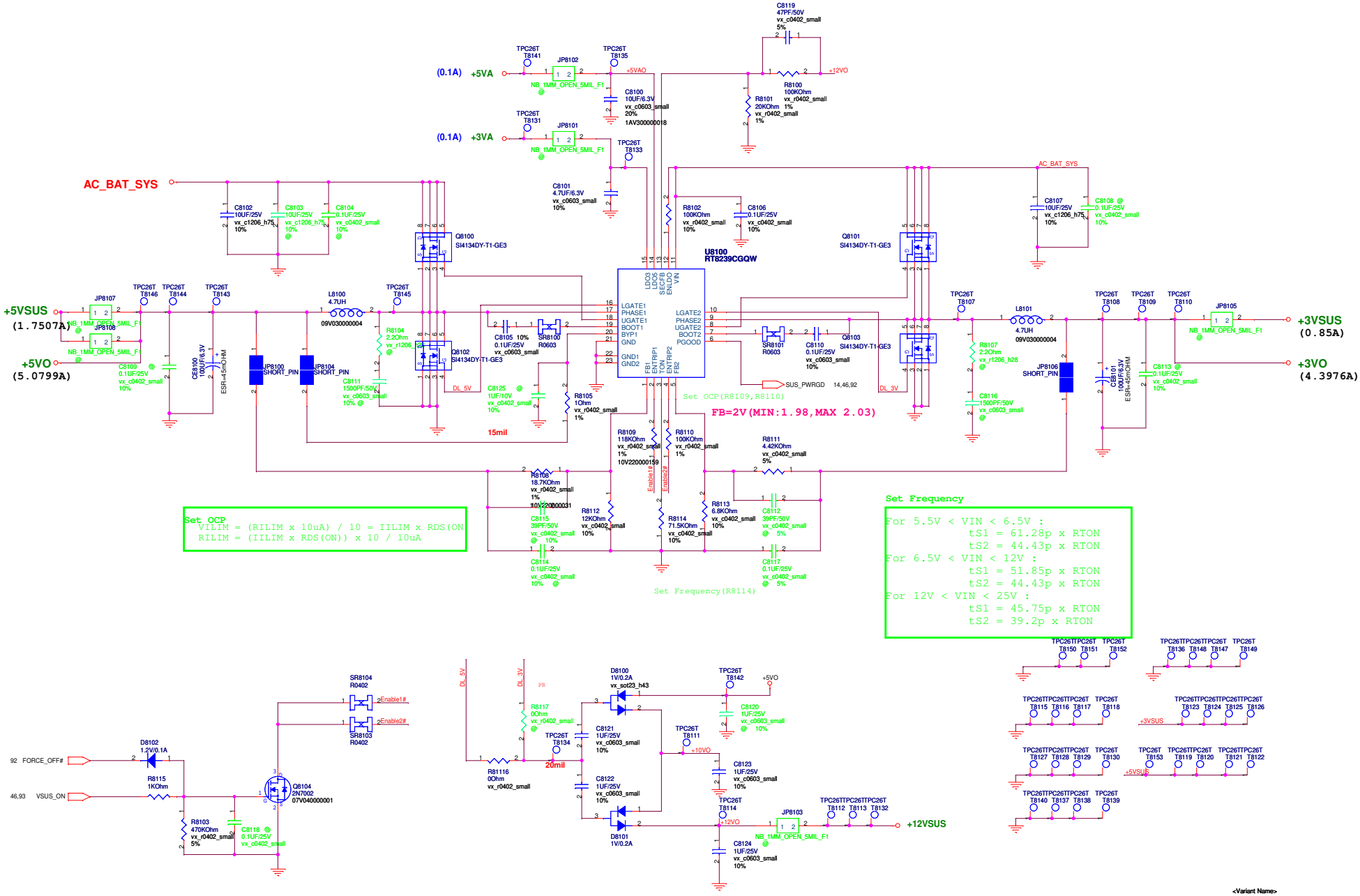
<Variant Name>

PEGATRON Title : POWER_VCORE

Engineer: Adams_Lin

Size	Project Name	Rev
C	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 80 of 77



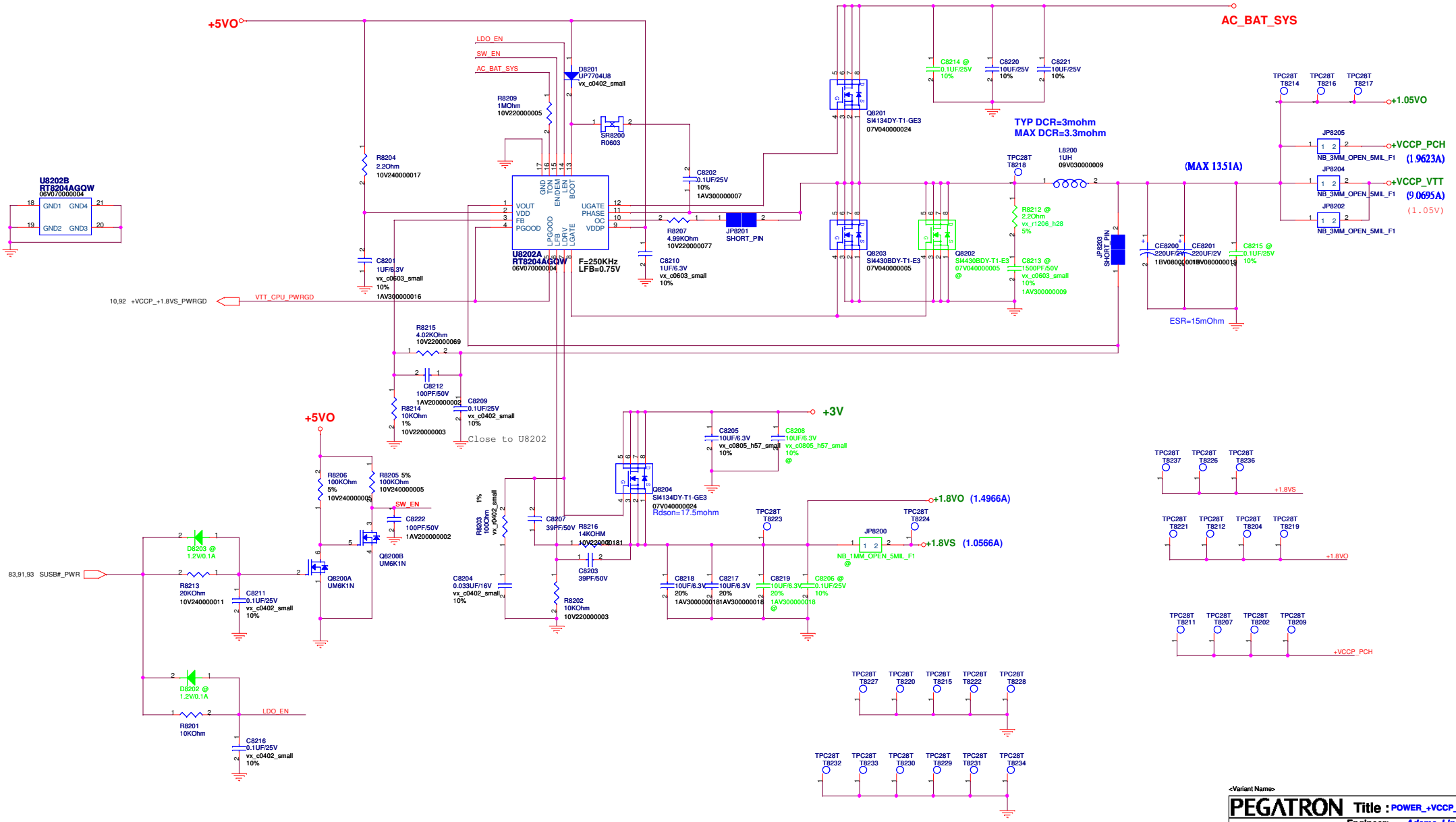
<Variant Name>

PEGATRON Title : POWER_SYSTEM

Engineer: Adams_Lin

Size	Project Name	Rev
Custom	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 81 of 77



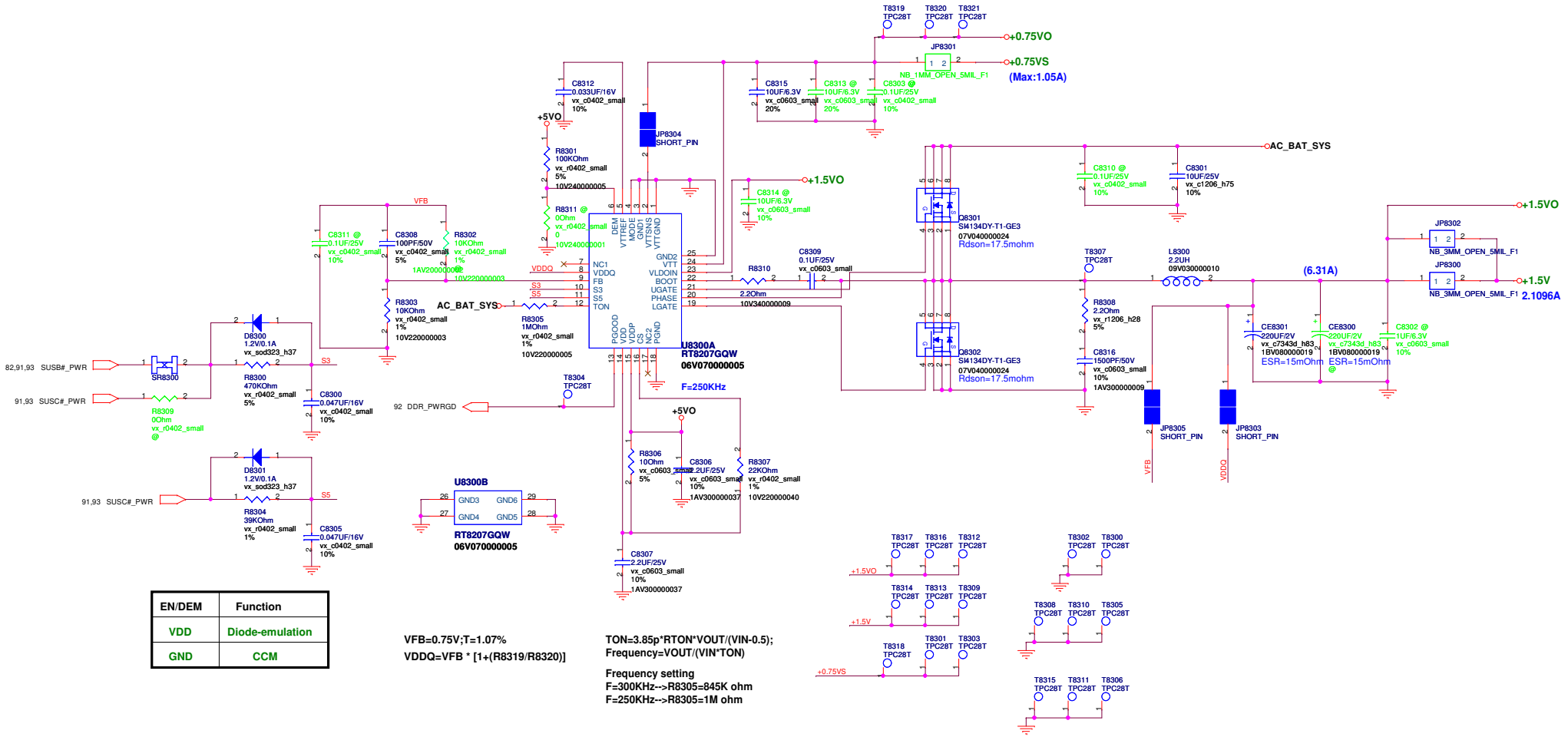
<Variant Name>

PEGATRON Title : POWER_+VCCP_+1.8VS

Engineer: Adams_Lin

Size	Project Name	Rev
Custom	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 82 of 77



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

VFB=0.75V;T=1.07%
VDDQ=VFB * [1+(R8319/R8320)]

TON=3.85p*RTON*VOUT/(VIN-0.5);
Frequency=VOUT/(VIN*TON)

Frequency setting
F=300KHz-->R8305=845K ohm
F=250KHz-->R8305=1M ohm

<Variant Name>

PEGATRON Title : POWER_DDR & VTT

Engineer: Adams_Lin

Size	Project Name	Rev
Custom	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 83 of 77

<Variant Name>

PEGATRON Title : POWER_N/A

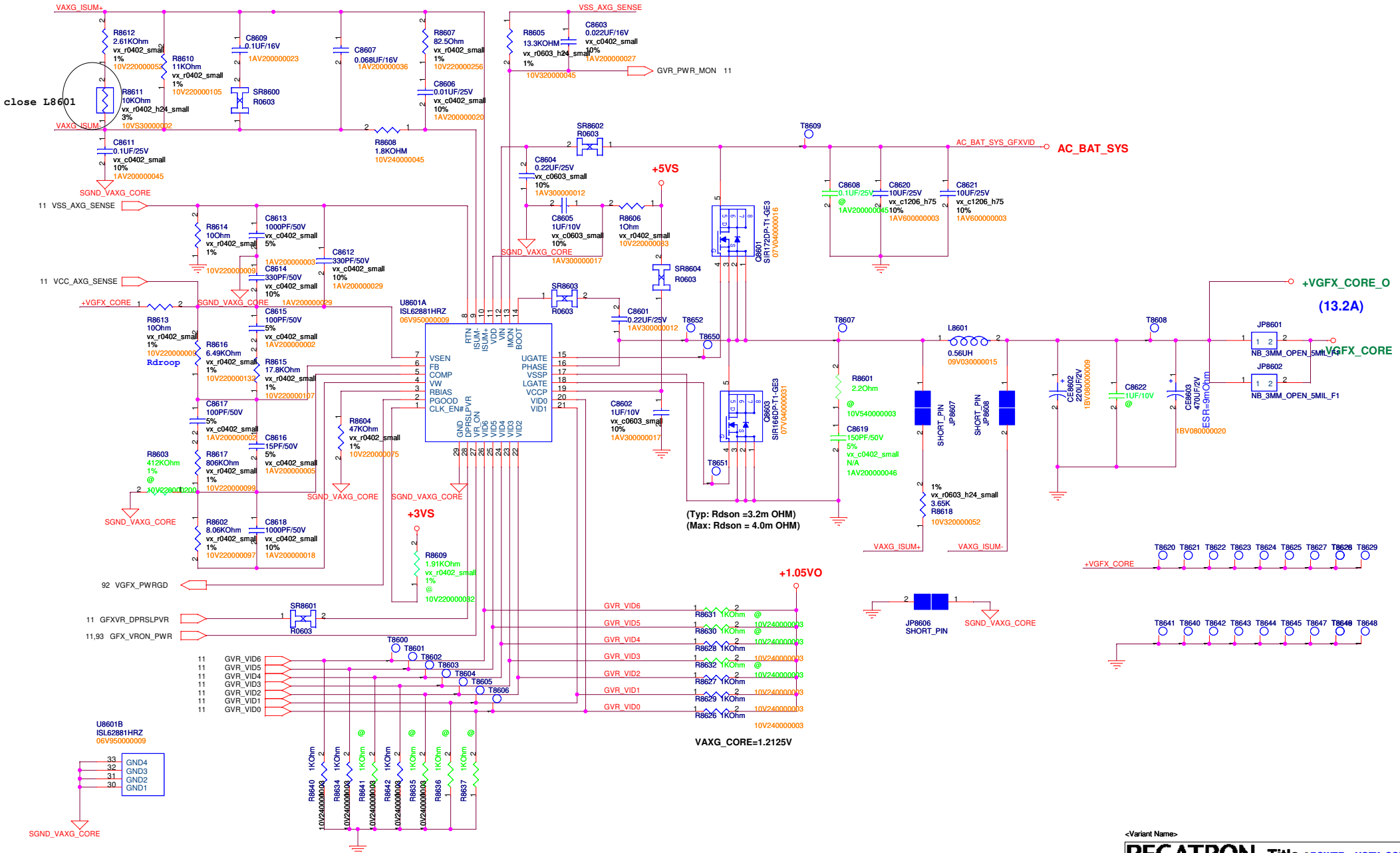
Engineer: *Adams_Lin*

Size	Project Name	Rev
Custom	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 84 of 77

<Variant Name>

PEGATRON	Title : POWER_N/A	
	Engineer: *Adams_Lin*	
Size: A	Project Name: AIC70	Rev: 1.0
Date: Wednesday, May 04, 2011	Sheet 85 of 77	



<Variant Name>

PEGATRON Title : POWER_+VGFX_CORE

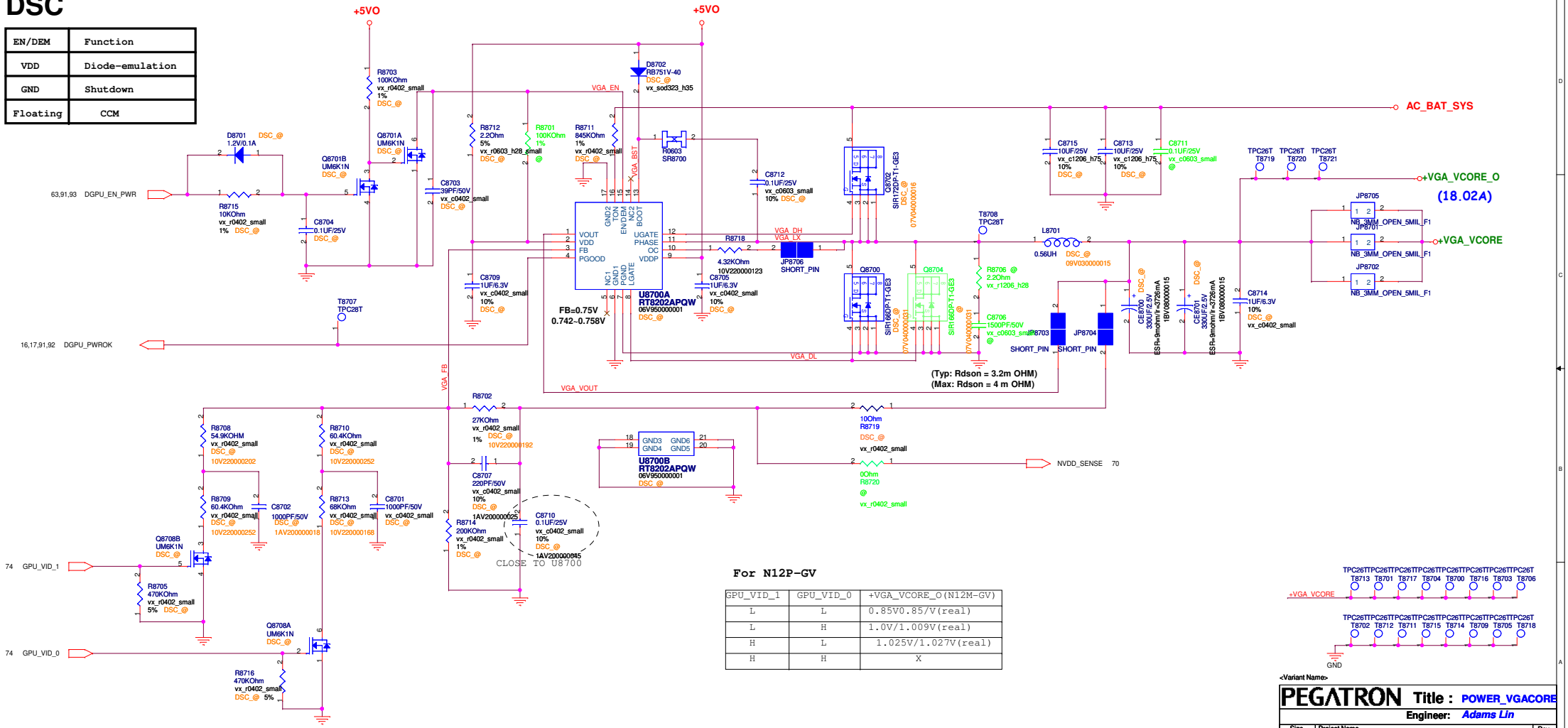
Engineer: Adams_Lin

Size	Project Name	Rev
Custom	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 86 of 77

DSC

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



GPU_VID_1	GPU_VID_0	+VGA_VCORE_O(N12M-GV)
L	L	0.85V0.85/V(real)
L	H	1.0V/1.009V(real)
H	L	1.025V/1.027V(real)
H	H	X

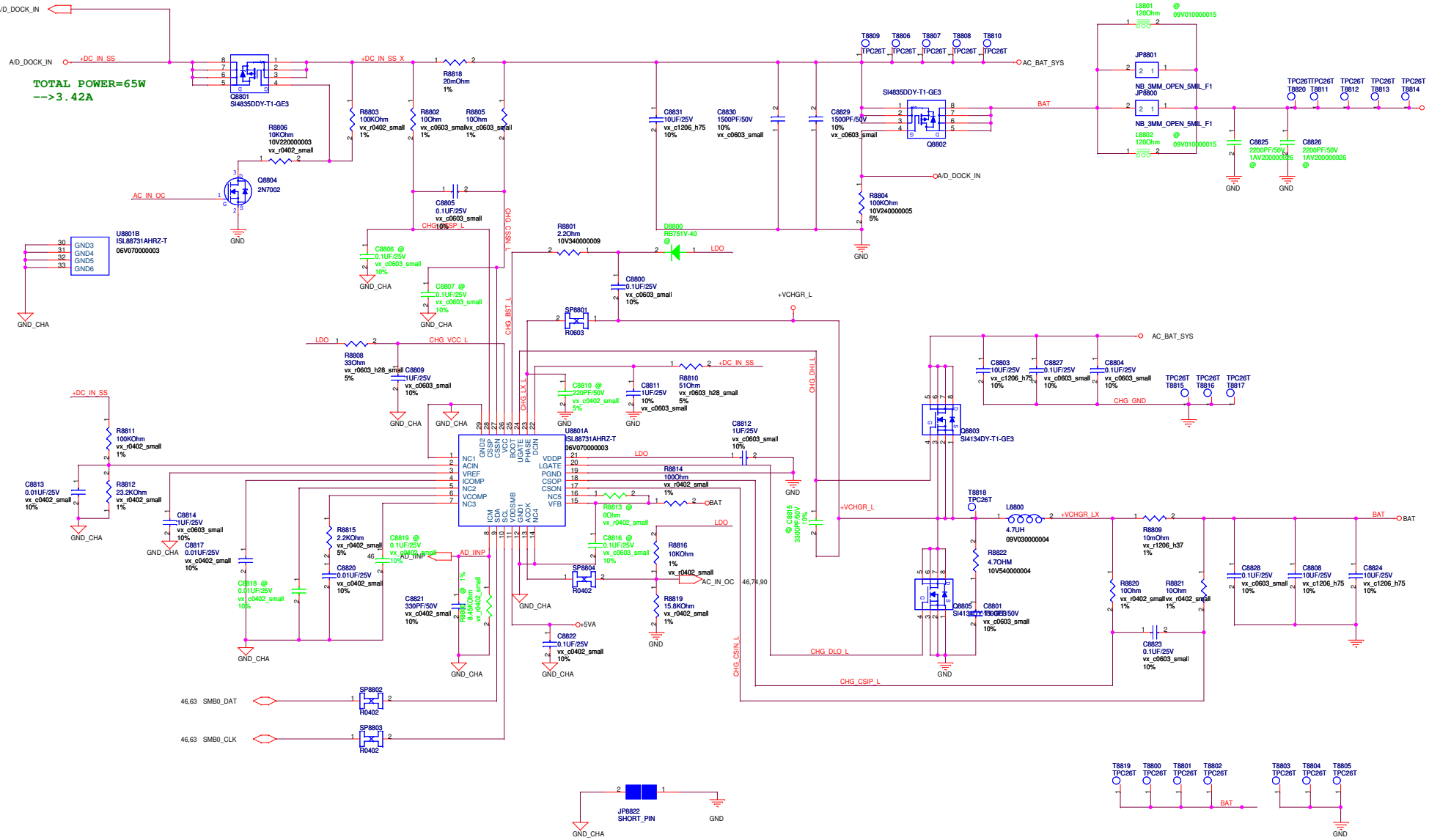
<Variant Name>

PEGATRON Title : POWER_VGACORE

Engineer: Adams Lin

Size	Project Name	Rev
Custom	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 87 of 77



<Variant Name>

PEGATRON Title : POWER CHARGER

Engineer: Adams_Lin

Size	Project Name	Rev
C	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 88 of 77

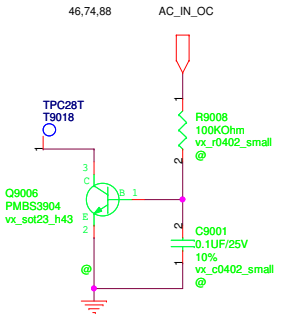
<Variant Name>

PEGATRON	Title : POWER_N/A	
	Engineer: *Adams_Lin*	
Size: A	Project Name: AIC70	Rev: 1.0
Date: Wednesday, May 04, 2011	Sheet 89 of 77	

BATTERY IN DETECT

ADAPTER IN DETECT

Use MAX17015 IC function to Cost down component



<Variant Name>

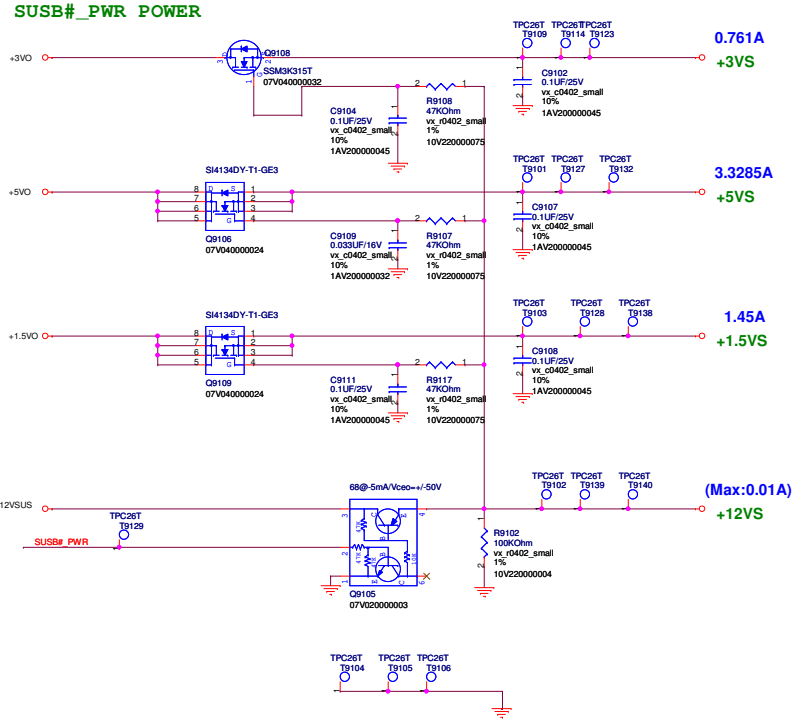
PEGATRON Title : POWER_DETECT

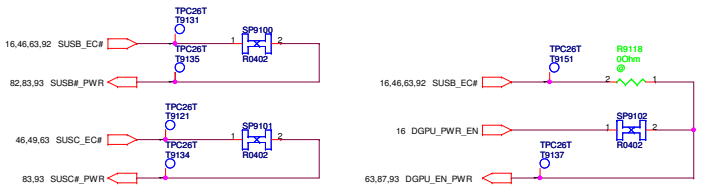
Engineer: Adams_Lin

Size	Project Name	Rev
Custom	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 90 of 77

SUSB#_PWR POWER

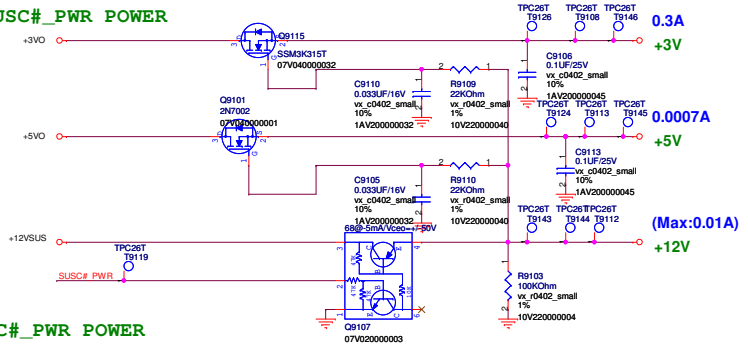




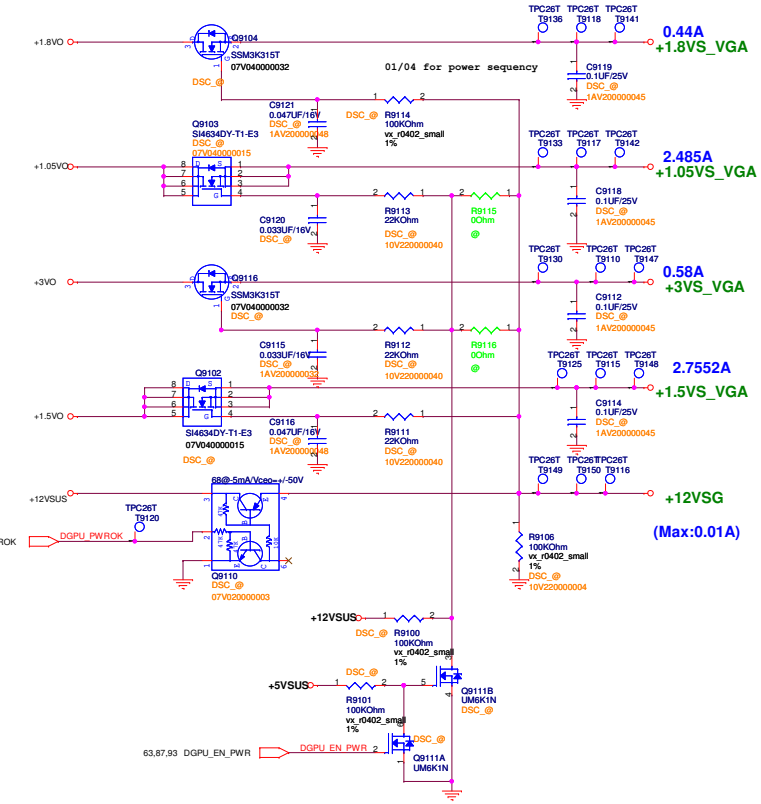
SUSC#_PWR POWER

Ron = 41.5 mΩ (max) (@VGS = 4.5 V)
Ron = 27.6 mΩ (max) (@VGS = 10 V)

NOTE:+3V=0.3A(EE)+1.4978A(+3V Provide to 1.8V PWR)=1.7978A



DSC#_PWR POWER



<Variant Name>

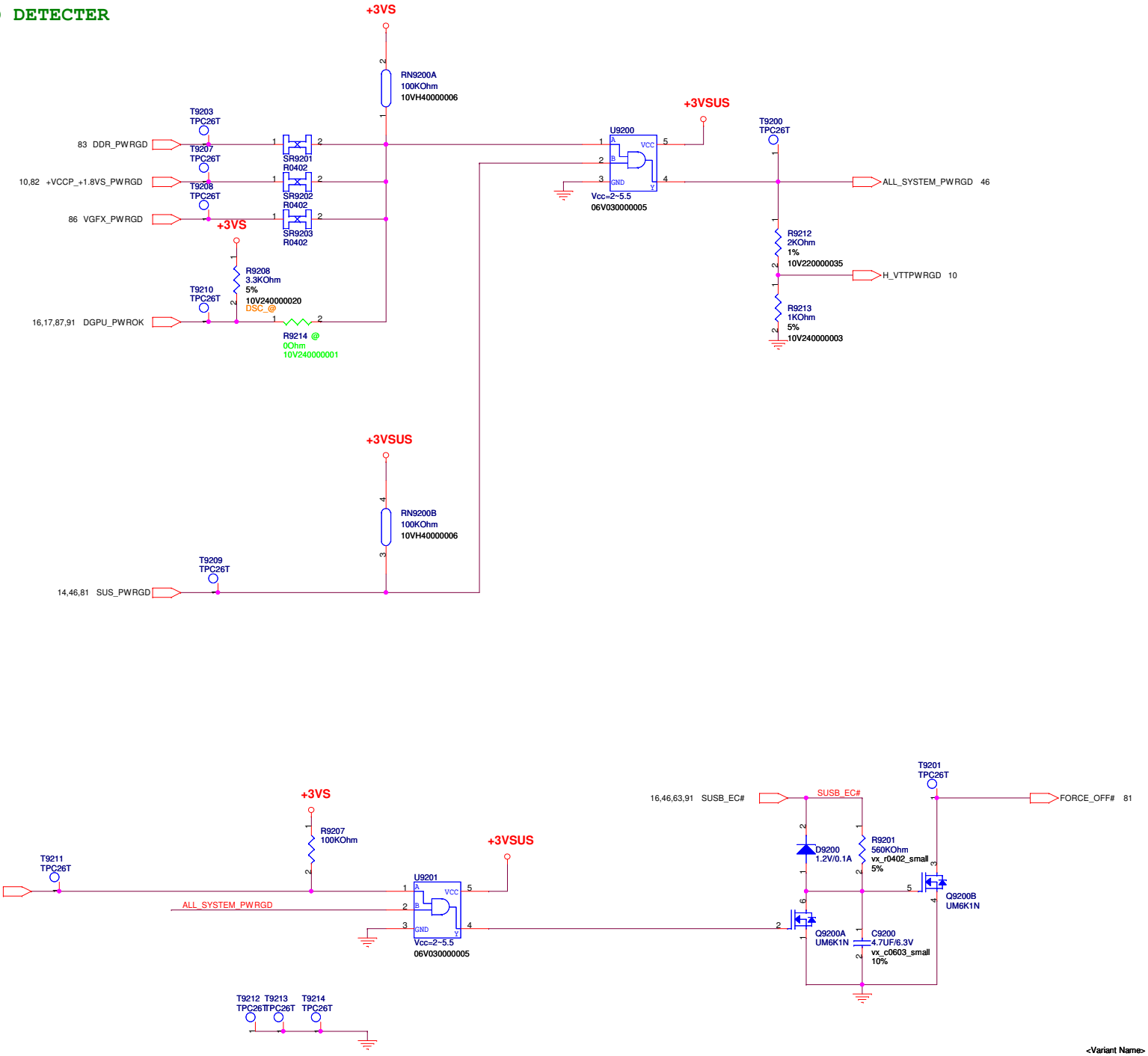
PEGATRON Title : POWER_LOAD SWITCH

Engineer: Adams_Lin

Size	Project Name	Rev
Custom	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 91 of 77

POWER GOOD DETECTER



<Variant Name>

PEGATRON Title :POWER_PROTECT

Engineer: Adams_Lin

Size	Project Name	Rev
Custom	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 92 of 77

AC_BAT_SYS → AC_BAT_SYS 37,80,81,82,83,86,87,88

BAT_CON → BAT_CON 63,88

BAT → BAT 88

+5VA → +5VA 42,49,66,81,88

+3VA → +3VA 13,18,46,48,63,81

+5VO → +5VO 81,82,83,87,91

+3VO → +3VO 81,91

+1.8VO → +1.8VO 82,91

+1.5VO → +1.5VO 83,91

+1.05VO → +1.05VO 80,82,86,91

+VGFX_CORE_O → +VGFX_CORE_O 86

+VGA_VCORE_O → +VGA_VCORE_O 87

+0.75VO → +0.75VO 83

+12VS → +12VS 38,39,91

+5VS → +5VS 15,19,38,39,41,42,46,48,49,60,63,80,86,91

+3VS → +3VS 10,13,14,15,16,17,18,19,21,22,24,33,37,38,39,41,46,47,49,60,63,65,80,86,91,92

+1.8VS → +1.8VS 11,18,19,82

+1.5VS → +1.5VS 10,11,24,55,63,91

+0.75VS → +0.75VS 21,22,63,83

+12VSUS → +12VSUS 60,81,91

+5VSUS → +5VSUS 19,60,61,66,81,91

+3VSUS → +3VSUS 10,13,14,15,16,17,18,19,33,46,55,81,92

+12V → +12V 91

+5V → +5V 42,63,91

+3V → +3V 37,50,63,65,82,91

+1.5V → +1.5V 10,11,21,22,63,83

+VGA_VCORE → +VGA_VCORE 63,75,87

+VGFX_CORE → +VGFX_CORE 11,86

+VCORE → +VCORE 11,12,80

+12VSG → +12VSG 91

+3VS_VGA → +3VS_VGA 70,72,74,91

+1.8VS_VGA → +1.8VS_VGA 63,91

+1.5VS_VGA → +1.5VS_VGA 63,71,76,91

+1.05VS_VGA → +1.05VS_VGA 63,70,71,72,91

FOR POWER TEST

+3VA

JP9300 @ SGL_JUMP (1 2) → T9300 TPC26T → CPU_VRON_PWR 80

JP9301 @ SGL_JUMP (1 2) → T9301 TPC26T → SUSB#_PWR 82,83,91

JP9302 @ SGL_JUMP (1 2) → T9302 TPC26T → SUSC#_PWR 83,91

JP9303 @ SGL_JUMP (1 2) → T9303 TPC26T → VSUS_ON 46,81

JP9304 @ SGL_JUMP (1 2) → T9304 TPC26T → DGPU_EN_PWR 63,87,91

+1.05VO

JP9305 @ SGL_JUMP (1 2) → T9305 TPC26T → GFX_VRON_PWR 11,86

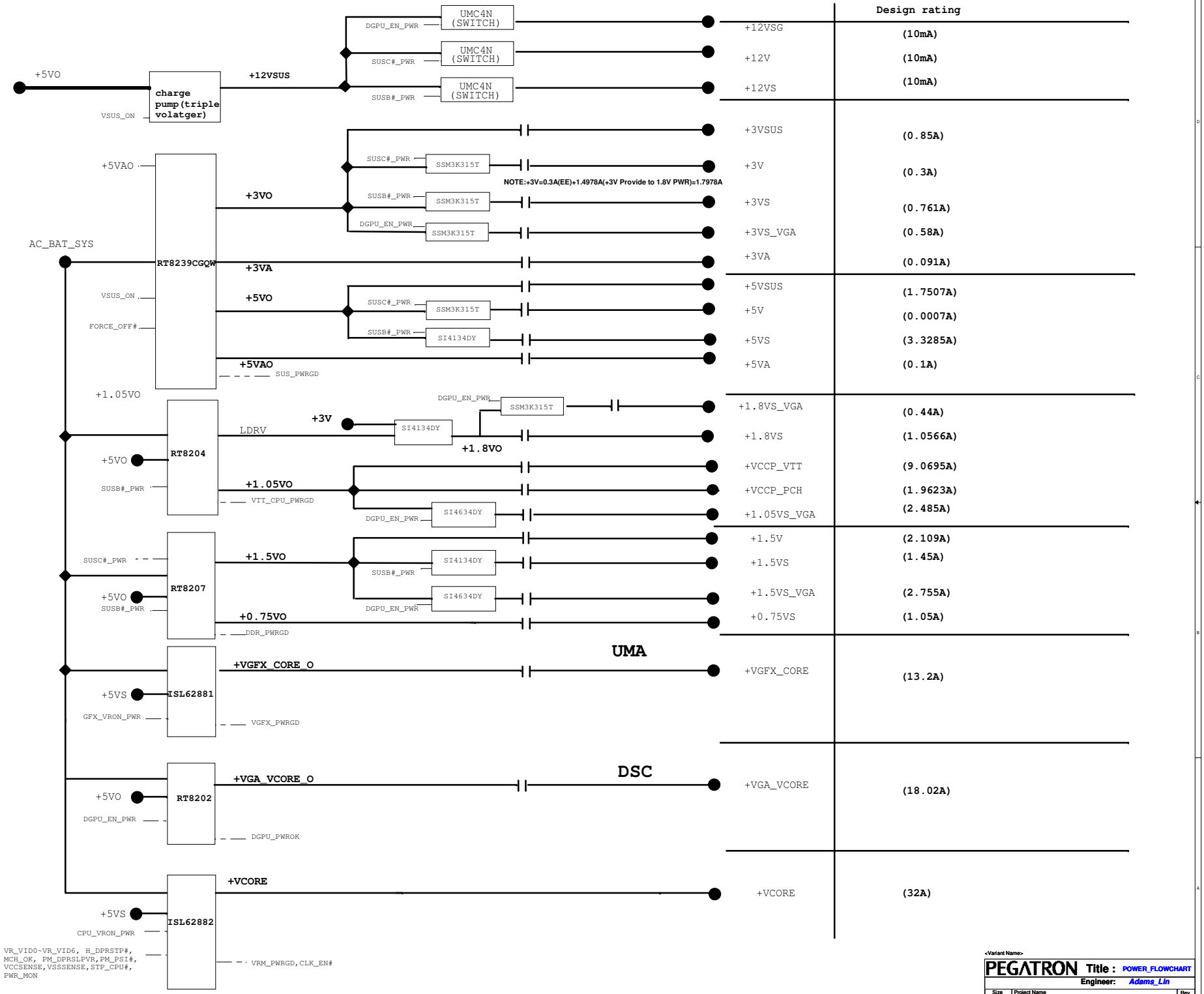
<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Adams_Lin

Size	Project Name	Rev
Custom	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 93 of 77



<Variant Name>

PEGATRON Title : POWER_FLOWCHART

Engineer: Adams_Lin

Size	Project Name	Rev
Custom	AIC70	1.0

Date: Wednesday, May 04, 2011 Sheet 94 of 77

modify notice

Item	Date	Description
SR-1	0120-11	P61, A04IO. change USB power switch circuit
SR-2	0120-11	Del P67, P68. Add P33, P34 for LAN
SR-3	0120-11	P48. change KB CON4801
SR-4	0120-11	P34. change RJ45 CON3401
SR-5	0120-11	P63. change BATT. con. circuit
SR-6	0120-11	P65, A02 change PWR LED CON6503 circuit
SR-7	0120-11	P60. change HDD CON6001
SR-8	0121-11	P44, P45 Del Entry audio circuit (Full)
SR-9	0121-11	P50. Del Entry SD socket circuit
SR-10	0121-11	P77. Del B channel VRAM * 4 circuit
SR-11	0121-11	P46. Add EC GPIO35 DGPU_PWR_EN for Power
SR-12	0121-11	P34, P35. Modify LAN AR8158 (Full)
SR-13	0123-11	P63. Change DC con. as VP part
SR-14	0123-11	P60. Change HDD CON6001
SR-15	0123-11	P7-P37 Change VP part
SR-16	0124-11	P41 Del Entry speaker R4117-R4120
SR-17	0124-11	P38-P39 Change VP part
SR-18	0124-11	P66 Remove LED circuit
SR-19	0124-11	P48. Reverse KB CON4801
SR-20	0124-11	P71. Remove GPU Channel B dummy NET
SR-21	0124-11	P16, P61. Remove USB_9(HDMI)
SR-22	0124-11	P48. Remove TP button circuit
SR-23	0124-11	P13. Remove Entry AZ R1318, R1346, R1347, R1348, R1349
SR-24	0124-11	P50. Modify CON5002 SD socket circuit
SR-25	0124-11	P48. Change KB CON4801 PIN definintion
SR-26	0124-11	P16, P61. change USB power switch circuit
SR-27	0124-11	P41, P46. ALC271-SPKR_EC_ICH_Colay
SR-28	0124-11	P46, P65. Modify LED circuit and EC GPIO definition
SR-29	0125-11	P33 Remove LAN LED circuit
SR-30	0125-11	P61 Modify D6101, RN6101, RN6105, RN6106
SR-31	0125-11	P33 Change R3311 as VP
SR-32	0125-11	P33 Change U3301 to AR8158 and delete SM BUS
SR-33	0125-11	P34 Modify LAN ESD circuit
SR-34	0125-11	P61. Modify Q6101
SR-35	0125-11	P65. Modify Q6501
SR-36	0125-11	P38, P46. Del F3801, C3811 Add CRT IN Detect
SR-37	0125-11	P63. Reverse J6301
SR-38	0125-11	P61, P46. change USB power switch and GPIO
SR-39	0125-11	P46,P66. change LED power and Net name
SR-40	0125-11	P34. Modify Transformer circuit
SR-41	0125-11	P33. Modify H/W strap setting
SR-42	0125-11	P37. Modify LVDS PIN definintion
SR-43	0125-11	P42. Modify De-Pop circuit
SR-44	0125-11	P41. Modify Audio Pin 14, 15, 27-31
SR-45	0126-11	P34. Modify Transformer circuit
SR-46	0126-11	P16. GPIO54 DGPU_PWR_EN
SR-47	0126-11	U1301, U7001 keypart no; U4602, F6302 Modify for BOM
SR-48	0126-11	P34. Modify Transformer circuit
SR-49	0126-11	P63, P60, P17, P48. Add 15" circuit BATT, ODD, Keyboard
SR-50	0126-11	P13, P60 Rename SATA 0 to SATA 1
SR-51	0126-11	P63. Reverse DC-IN J6301 PIN1 as GND
SR-52	0126-11	P48. Reverse KB CON4801
SR-53	0126-11	DGPU Sync with EH31
SR-54	0126-11	P.76. T7, M7 Setting
SR-55	0126-11	Modify as OPT display output
SR-56	0127-11	P.76. Cancel T7, M7 Setting
SR-57	0127-11	P.46, P50 Modify single net
SR-58	0127-11	P.42 Change R4205, R4206 = 51 ohm
SR-59	0127-11	P.41 DEL C4109, C4112
SR-60	0127-11	P.14 R1403, R1404 option N/A
SR-61	0127-11	P.14 R1443, R1444, RN1402, R1424, R1426, R1427, R1428 option N/A; R1429 option /HDMI_HPD_PCH
SR-62	0127-11	P71, P74. R7101, R7103, R7435, R7437 option @
SR-63	0127-11	P74. Del R7433, R7434, GPIO Test Pad
SR-64	0128-11	P34. U3403.4 RXN
SR-65	0128-11	P66. change R6603.1 (+5VA), LED6602, LED6603
SR-66	0128-11	P65. change R6508.1 (PWRLED_ON#), CON6503.6 (+5VSUS)
SR-67	0128-11	P97. Modify A04 Pwr Board
SR-68	0128-11	P55. Un-mount Q5505, R5510
SR-69	0128-11	P66. Modify Screw Hole (Sync with AAB70)
SR-70	0128-11	P63. Modify Battery CON6302, D6302 signal name

Item	Date		
SR-71	0128-11	P15. Add C1510 (22pF) for Clock fine-tune	
SR-72	0128-11	P33. change R3325, R3331 (4.7k ohm)	
SR-73	0128-11	P39. Un-mount R3907 (HDMI)	
SR-74	0128-11	Change connector by list of 0128-11	
SR-75	0129-11	Change HDD CON6001(1224-001N000)	
SR-76	0129-11	P97 (A02). Change Hotbar 6 Pad (PWR_U01)	
SR-77	0129-11	P41-P50 Change VP part	
SR-78	0129-11	P55. Add Q5510, R5515 for BT PCI-E wake up event	
SR-79	0130-11	P50. change footprint for U5001 Card reader controller	
SR-80	0130-11	P66. change CPU*4, GPU*2, System screw hole*10	
SR-81	0130-11	P46. change RN4601C (RN9202C)	
SR-82	0130-11	P66. change F screw hole *2	
SR-83	0130-11	P46. change SHORT PIN (R4601,R4602)	
SR-84	0130-11	P46, P65. change EC GPIO21 (PWR_AMBER_LED#) for PWR Brd.	
SR-85	0130-11	Modify Sub board screw hole	
SR-86	0130-11	P34. Change RJ45 CON3401 1223-00BT000	
SR-87	0131-11	P74. Change Q7401B(Q9203B)	
SR-88	0131-11	P96, P99. Del Screw hole ODD_H02, change IOH3	
SR-89	0131-11	P97. Change Power Board LED PWR_LED01	
SR-90	0131-11	P60. Change 15" ODD CON6505 as VP	
SR-91	0131-11	P96-P99. Copy from AAB70 (sub board)	
	AIC70 R1.1	Rename for AIC70_0202-11_BOM and merge AIC70_0225_PWR_B power BOM	
	AIC70 R1.1-1 0224-11-I	P48. Delete CON4804 P60. Delete CON6505,C5123,C5118,C5121,C5119,R5109,C5120,C5122,R5108 P63. Delete CON6302,F6303,C6314,C6312,C6315,C6313,C6311,R6316,D6302, L6307,L6306,L6305,T6320,T6324,T6323,T6321,T6322	
	AIC70 R1.1-2 0224-11-I	P60. Change SPS101 to JP6001 for optional ZOPODD	
	AIC70 R1.1-3 0224-11-I	P37. Add R3713,R3714,R3715,R3716 for EMI request	
	AIC70 R1.1-4 0224-11-I	P41. Delete CN4101,add C4130-C4138,R412S-R4136,CON4102 P48. Add C4816-C4821,CON4804 Change C4808-C4811 to 10pF,add C4812-C4815,CON4805,L4803,L4804,R4802 P65. Change C6504 to 10pF, add C6507,CON6505,D6502,C6508,C6509	
	AIC70 R1.1-5 0228-11-I	P61. Change CON6101 to 1213-00T4000 form 1213-00E000 P34. Change CON3401 to 1223-0002000 from 1223-00BT000 P63. Change J6301 to 1217-00WC000 from 1217-0037000 P60. Change CON6001 to 1224-00T2000(12V24GBRD001) form 1224-001N000 p98. Change TP_SW1,TP_SW2 to 1209-00YY000 from 1209-0004K000 P21. Change D1MM U2101 to 1202-000P000 from 1202-002P000 P22. Change D1MM U2201 to 1202-00D8000 from 1201-002G000	
	AIC70 R1.1-6 0301-11-I	P39. Add R3937 and R3938 for EMI request P34. Change R3408 to 0805 size for EMI request P37. Add C3725 and reserve TVS D3705 for EMI request P37. Add D3706 and net LCD_BACKOFF# P46. Add net LCD_BACKOFF# and delete T4627 P60. Add SP6001	
	AIC70 R1.1-7 0302-11-I	P55. Change Mini-PCIE connector to 1244-0086000 from 1244-000T000	
	AIC70 R1.1-8 0303-11-I	P18. Change R1821 to L1801 bead 1kOhm/100MHz P33. Change L3302 to 0901-00QR000 1.5kOHM/100MHz for EMI request P34. Add D3401 and nostuff R3408 for EMI request P97. Nostuff PWR_R2 and PWR_LED2 P99. Add IOCE2 100uF/6.3V for USB port P34. U3403 swap P37. RH3711,L3706 swap P22. M_B_DQ53 and M_B_DQ50 swap P99. delete IOCE2 100uF/6.3V for USB port	
	AIC70 R1.1-9 0303-11-I	P41. Add C4116,C4119,net VREFOUT_A_K_L,MIC_IN_AC_K_L P42. Add R4211,R4207,net MIC_IN_AC_K_J P61. Change CON6102 to 20 pin 1218-016R000 and add one +5V_USB_DB pin, one MIC_IN_AC_K_J P99. Change IOCON5 to 20 pin 1218-016R000 and add one +5VUSB_IO_C pin, one MIC_IN_AC_K_IO	
	AIC70 R1.1-10 0304-11-I	P60. Add CON5103,C5123,C5125,C5126,C5127,C5128,C5129,C5130,C5131,C5132,C5133 for HDD cable	
	AIC70 R1.1-11 0304-11-I	P34. Change L3403 to bead 1kohm/100MHz,add TVS D3402,add ESD cap C3406	
	AIC70 R1.1-12 0304-11-I	P38. Change L3801-L3803 to 0.056uH	
	AIC70 R1.1-13 0304-11-I	P74. Change R7420 to 45.3k for default samsung 128 x 16 VRAM P76. Chagne U7601-U7604 VRAM to Samsung VRAM	
	AIC70 R1.1-14 0304-11-I	P41. Change U4101 to ALC271X_VB3 020J-00870PB	
	AIC70 R1.1-15 0304-11-I	P63. Change F6301 to 07V100000003(0710-007V000)	
	AIC70 R1.1-16 0304-11-I	P80-P94. Update power circuit AIC70_0304_PWR_R11.DSN - C8207 change size	

Item	Date		
AIC70 R1.1-17	0306-11-I	P99. Add IOC7,IOD7	
AIC70 R1.1-18	0306-11-I	P34. Delete C3406	
AIC70 R1.1-19	0306-11-I	P60. Add SP6002 and use /HDD_CABLE option for HDD cable	
AIC70 R1.1-20	0306-11-I	P33. Change R3717 to 10k pull down for disable OC mode and nostuff C3303	
AIC70 R1.1-21	0306-11-I	P60. Delete /17" option P63. Delete /17" option	
AIC70 R1.1-22	0306-11-I	P17. Add PCB ID define	
AIC70 R1.1-23	0306-11-I	P48. Modify TP Button optional decription P41. Modify speaker optional decription and related net name	
AIC70 R1.1-24	0306-11-I	P1-P99. Midofy schematic optional	
AIC70 R1.1-25	0307-11-I	P18. Add R1824 for PCH SPI +3VA power	
AIC70 R1.1-26	0307-11-I	P46. delete R4627,R4625,R4621,R4622,R4615,R4616,R4617,C4608,U4602	
AIC70 R1.1-27	0307-11-I	P60. Add R5109,R5110,R5111,R5112	
AIC70 R1.1-28	0307-11-I	P66. Change GND_LEDDB to GND	
AIC70 R1.1-29	0307-11-I	P66. Delete H6538, change H6537,H6633,H6632 P98. Change TP_H1,TP_H2 P99. Change IOH6	
AIC70 R1.1-30	0308-11-I	P61. Reserve U6105 for reduceing conduction loss	
AIC70 R1.1-31	0308-11-I	P61.Change CON6102 to 24 pin (1218-00Q2000) P99. Change IOCON5 to 24 pin (1218-00Q2000)	
AIC70 R1.1-32	0308-11-I	P46. Mirror vertically Q4601	
AIC70 R1.1-33	0308-11-I	P63. Mirror vertically J6301	
AIC70 R1.1-34	0309-11-I	P80-P94. Merge power schematic AIC70_R11_201103082200.DSN	
AIC70 R1.1-35	0309-11-I	P98. Add TPC02 P48. Link C4821 Pin1 to CON4804 pin1	
AIC70 R1.1-36	0309-11-I	P34. LAN swap on U3403	
AIC70 R1.1-37	0309-11-I	P50. Add SP5002 for CON5002 pin12 connecting to GND	
AIC70 R1.1-38	0311-11-I	P46. Change PLT_ID P17. Change PCB_ID	
AIC70 R1.1-39	0311-11-I	P33. Stuff C3303	
AIC70 R1.1-40	0311-11-I	P80-P94. Update power circuit AIC70_R11_20110311_EE.DSN	
AIC70 R1.2		AIC70_R12_201103202330_I is renamed from AIC70_R11_201103111800_BOM_I.DSN	
AIC70 R1.2-41	0320-11-I	P10. Reserve R1032, R1044 for S3 CPU power P11. Reserve JP1103 for S3 CPU power	
AIC70 R1.2-42	0320-11-I	P11. R1127 nostuff and R1129 stuff for UMA and Optimus	
AIC70 R1.2-43	0320-11-I	P42. Add R3917,R3939 to +5V and nostuff R3916,R3935 for solving pop noise	
AIC70 R1.2-44	0320-11-I	P74. Stuff R7435, R7437 for NV request	
AIC70 R1.2-45	0321-11-I	P33. Change LAN footprint	
AIC70 R2.0		AIC70_R20_201103282000_I is renamed from AIC70_R12_201103211630_I.DSN	
AIC70 R2.0-46	0328-11-I	P49. Reserve Plam Rest thermal sensor, add Q4902,C4909,U4903,R4908,C4910 P47. Add R4709 P15. Add SP1501,SP1502	
AIC70 R2.0-47	0328-11-I	P42. Add R3940,R3941	
AIC70 R2.0-48	0330-11-I	P98. Colay CHO TP_SW, add TP_SW3,TP_SW4	
AIC70 R2.0-49	0330-11-I	P49. Nostuff palm rest thermal sensor	
AIC70 R2.0-50	0331-11-I	P41. Update CON4101,CON4102 P61. Update CON6102 P99. Update IOCON5 P48. Update CON4803,CON4805	
AIC70 R2.0-50	0331-11-I	P99. Rename IOCON5	
AIC70 R2.0-51	0401-11-I	P65. Change CON6503,CON6505 to 4 pin, delete C6507,C6509 P97. Change PWR_U01 to 4 pin, delete PWR_R2, PWR_LED2	
AIC70 R2.0-52	0401-11-I	P66. Change H6541,H6544,H6545,H6546 to NPTH	
AIC70 R2.0-53	0401-11-I	P80-P94. Update power circuit AIC70_R11_20110401.DSN	
AIC70 R2.0-54	0402-11-I	P66. Change H6633 to NPTH	
AIC70 R2.0-55	0406-11-I	P65. Nostuff R6507,Q6501,R6509	
AIC70 R2.0-56	0406-11-I	P33. Add L3303, U3405	
AIC70 R2.0-57	0407-11-I	P61. Add CON6103 P99. Add IOCON6	
AIC70 R2.0-58	0407-11-I	P80-P94. Update power circuit AIC70_R20_20110407_F.DSN	
AIC70 R2.0-59	0411-11-I	P33. Change C3321,C3322 to 15pF P72. Change C7208,C7209 to 15pF	
AIC70 R2.0-60	0411-11-I	P61. Change U6104, U6105 to 1.5A and stuff U6105	

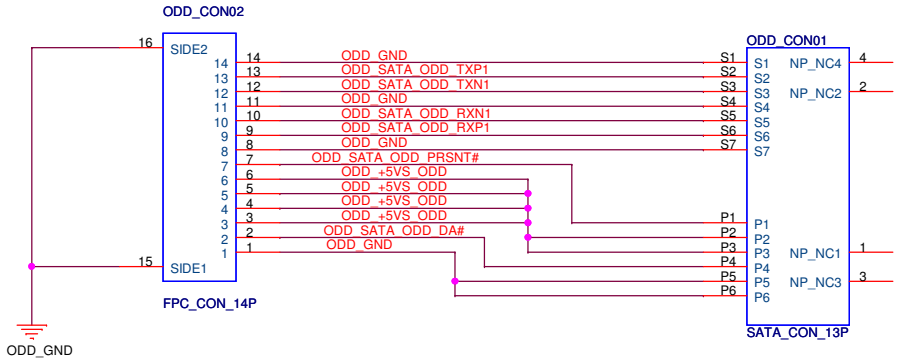
Item	Date	
AIC70 R2.0-61	0415-11-I	P66. Change LED6602 to 0713-01QK000, LED6603 to 0713-01QJ000, R6605 to 100 ohm, R6604 to 390 ohm
AIC70 R2.0-62	0415-11-I	P49. Change R4903 to 4.32k
AIC70 R2.0-63	0415-11-I	P61. Change U6104 to USB POWER SW. G547E1P81U: 06V290000008 , nostuff U6105
AIC70 R2.0-64	0415-11-I	P34. Change U3402 P/N to 0912-0001000 (only change P/N)
AIC70 R2.0-65	0420-11-I	P33. Change L3303 to 0 ohm
AIC70 R2.0-66	0421-11-I	P98. Reserve TPC02
AIC70 R2.0-67	0421-11-I	P98. Delete TP_SW3, TP_SW4
AIC70 R2.0-68	0504-11-I	P49. Change R4903 to 4.02k
AIC70 R2.0-69	0504-11-I	P66. Change H6611, H6612 to DSC optional
AIC70 R2.0-70	0504-11-I	P61. Nostuff CON6103 P99. Nostuff IOCON6
AIC70 R2.0-71	0504-11-I	P34. Nostuff D3401, stuff R3408

PEGATRON Title : Power History

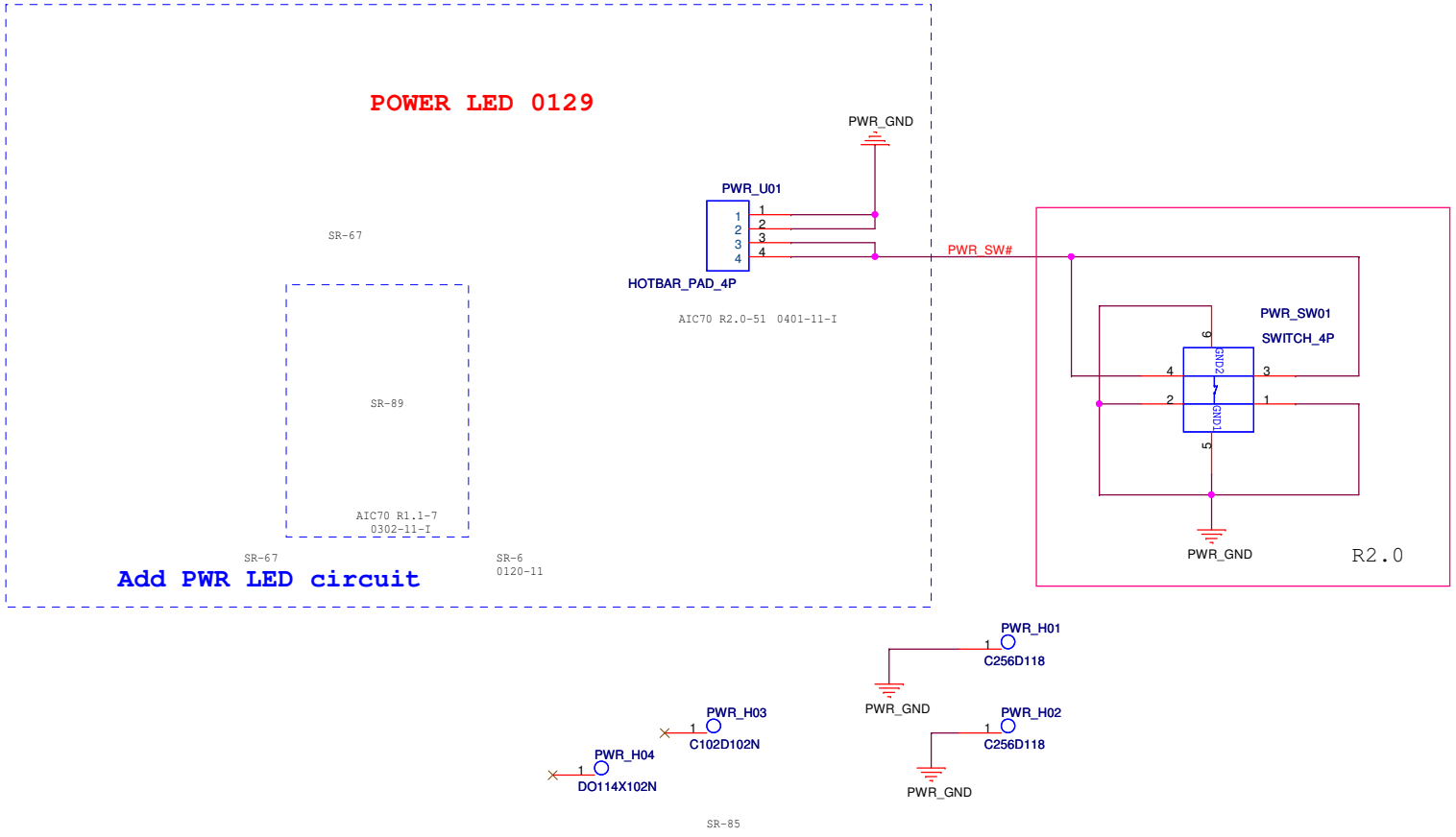
Engineer:

Size	Project Name	Rev
Custom		xx

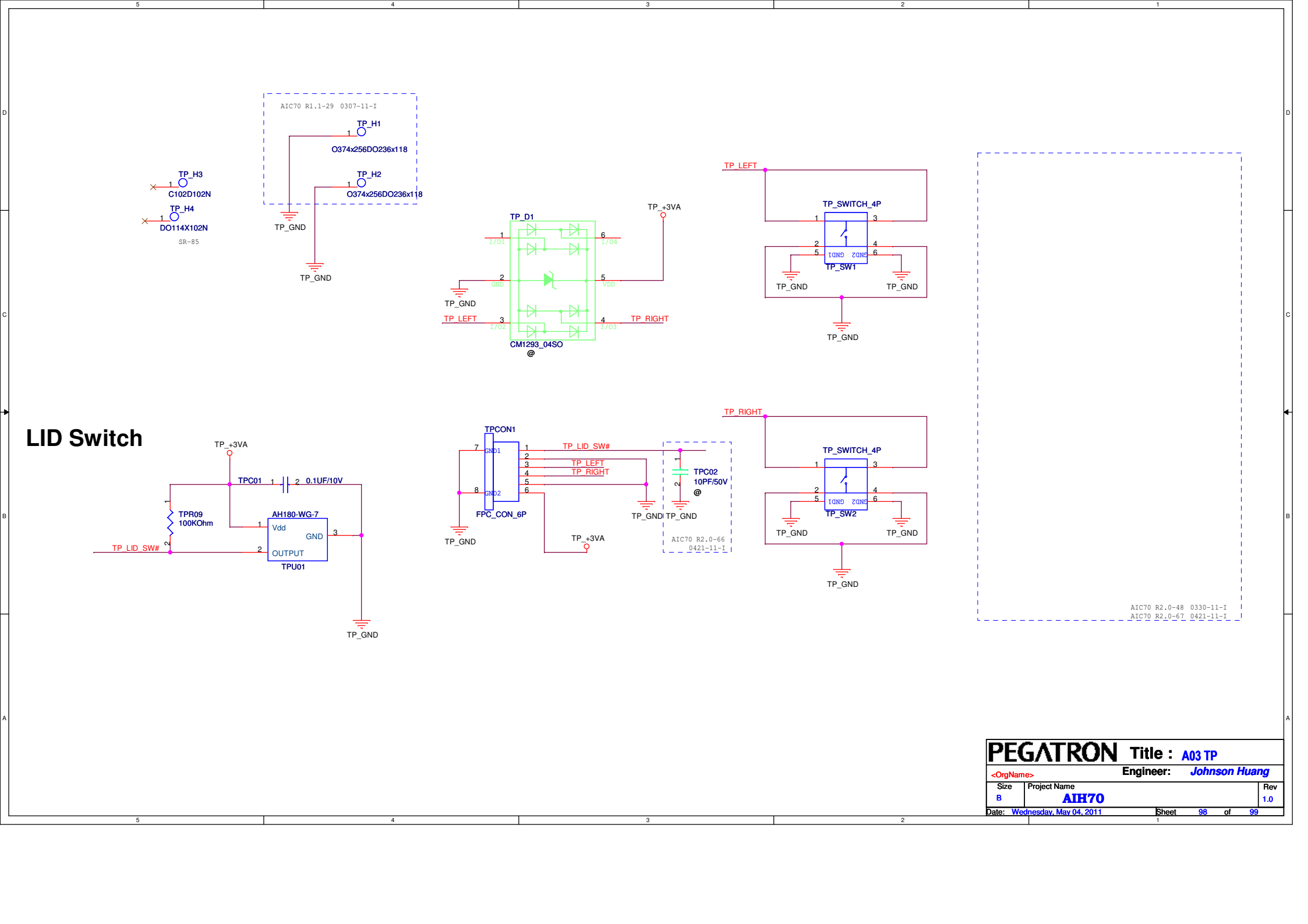
Date: Wednesday, May 04, 2011 Sheet 36 of 77



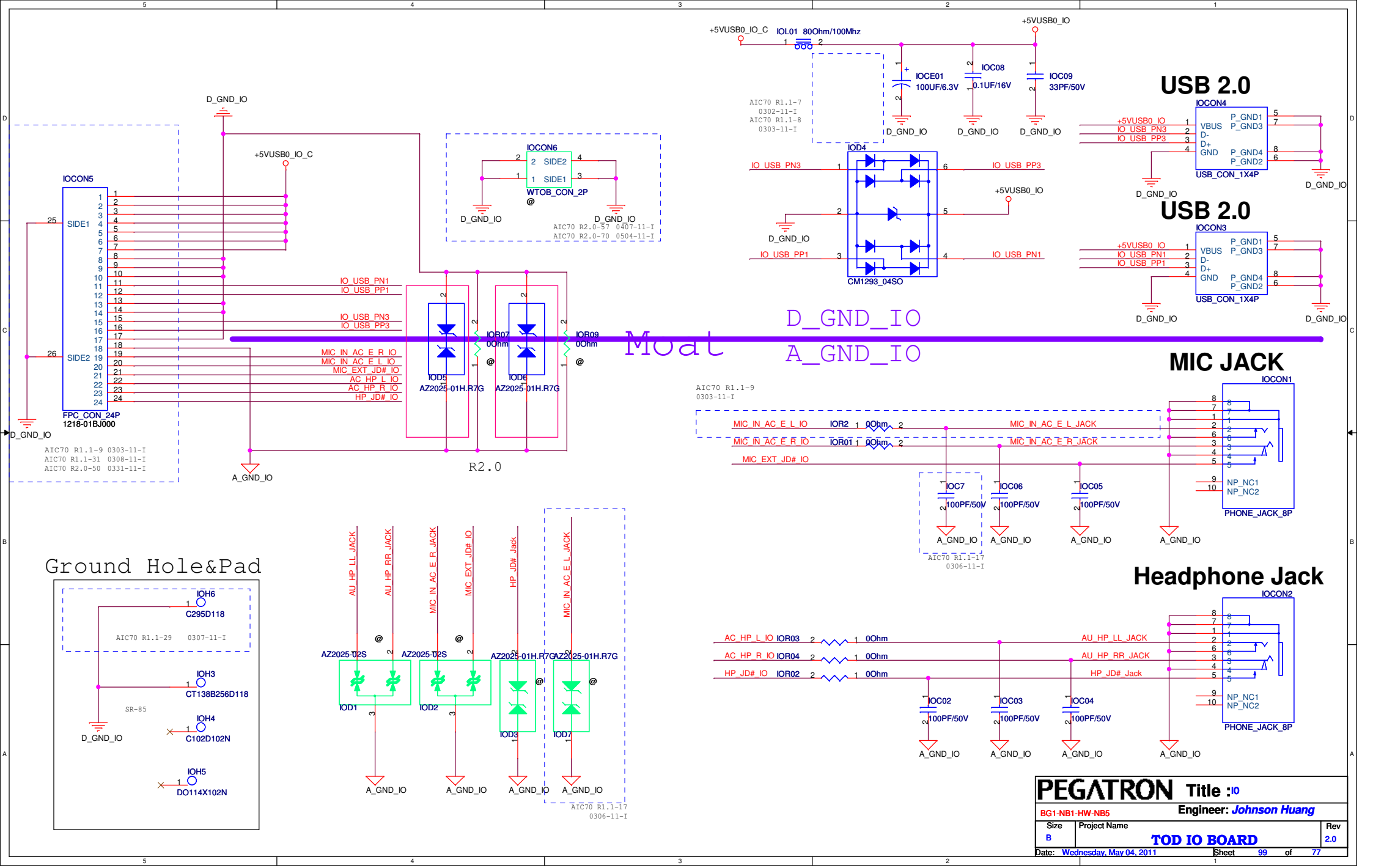
PEGATRON	Title : ODD	
BU1-RD Div.1-HW RD Dept.1	Engineer: Johnson Huang	
Size: B	Project Name: TOD ODD BOARD	Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 96 of 77	



PEGATRON	Title : PWR BTN	
BU1-RD Div.1-HW RD Dept.1	Engineer: Johnson Huang	
Size: B	Project Name: TOD POWER SW	Rev: 2.0
Date: Wednesday, May 04, 2011	Sheet 97 of 77	



PEGATRON	Title : A03 TP	
<OrgName>	Engineer: Johnson Huang	
Size: B	Project Name: AIH70	Rev: 1.0
Date: Wednesday, May 04, 2011	Sheet 98 of 99	


+5VUSB0_IO_C
IOL01 80Ohm/100Mhz
+5VUSB0_IO
IOCE01 100UF/6.3V
IOC08 0.1UF/16V
IOC09 33PF/50V
AIC70 R1.1-7 0302-11-I
AIC70 R1.1-8 0303-11-I
D_GND_IO
USB 2.0
IOCON4
+5VUSB0_IO
IO_USB_PN3
IO_USB_PP3
VBUS
D-
D+
GND
P_GND1
P_GND3
P_GND4
P_GND2
USB_CON_1X4P
IOD4
IO_USB_PN3
IO_USB_PP3
IO_USB_PP1
IO_USB_PN1
CM1293_04SO
USB 2.0
IOCON3
IO_USB_PN1
IO_USB_PP1
IOCON5
SIDE1
SIDE2
FPC_CON_24P
1218-01BJ000
IOCON6
SIDE2
SIDE1
WTOB_CON_2P
AIC70 R2.0-57 0407-11-I
AIC70 R2.0-70 0504-11-I
AIC70 R1.1-9 0303-11-I
AIC70 R1.1-31 0308-11-I
AIC70 R2.0-50 0331-11-I
IO_USB_PN1
IO_USB_PP1
IO_USB_PN3
IO_USB_PP3
MIC_IN_AC_E_R_IO
MIC_IN_AC_E_L_IO
MIC_EXT_JD#_IO
AC_HP_L_IO
AC_HP_R_IO
HP_JD#_IO
IOR07 0Ohm
IOR09 0Ohm
IOD5 AZ2025-01H.R7G
IOD6 AZ2025-01H.R7G
A_GND_IO
D_GND_IO
Moat
R2.0
MIC JACK
IOCON1
AIC70 R1.1-9 0303-11-I
MIC_IN_AC_E_L_IO
MIC_IN_AC_E_R_IO
MIC_EXT_JD#_IO
IOR2 0Ohm
IOR01 0Ohm
MIC_IN_AC_E_L_JACK
MIC_IN_AC_E_R_JACK
IOC7 100PF/50V
IOC06 100PF/50V
IOC05 100PF/50V
NP_NC1
NP_NC2
PHONE_JACK_8P
AIC70 R1.1-17 0306-11-I
Ground Hole&Pad
IOH6
C295D118
AIC70 R1.1-29 0307-11-I
IOH3
CT138B256D118
SR-85
IOH4
C102D102N
IOH5
DO114X102N
AU_HP_LL_JACK
AU_HP_RR_JACK
MIC_IN_AC_E_R_JACK
MIC_EXT_JD#_IO
HP_JD#_Jack
MIC_IN_AC_E_L_JACK
AZ2025-02S
AZ2025-01H.R7G
IOD1
IOD2
IOD3
IOD7
AIC70 R1.1-17 0306-11-I
Headphone Jack
IOCON2
AC_HP_L_IO IOR03 0Ohm
AC_HP_R_IO IOR04 0Ohm
HP_JD#_IO IOR02 0Ohm
AU_HP_LL_JACK
AU_HP_RR_JACK
HP_JD#_Jack
IOC02 100PF/50V
IOC03 100PF/50V
IOC04 100PF/50V
NP_NC1
NP_NC2
PHONE_JACK_8P
PEGATRON
Title : IO
BG1-NB1-HW-NB5
Engineer: Johnson Huang
Size B
Project Name TOD IO BOARD
Rev 2.0
Date: Wednesday, May 04, 2011
Sheet 99 of 77