Berry DG15 Discrete/UMA Schematics Document

Arrandale

Intel PCH

2010-02-03

REV : A00

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
M96:DIS M96 platform installed
*VRAM_1G:VRAM 128M*16 installed*
Colay :Manual modify BOM

<Core Design>

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Title: *Cover Page*

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A3	*Berry*	*A00*

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Berry Block Diagram (Discrete/UMA co-lay)

Project code : 91.4HH01.001
PCB P/N : 48.4HH01.0SA
Revision : 09909-1

##OnMainBoard

1.Park-XT;512MB
(64Mx16b*4)
Dell P/N:9TGTN$AA HYNIX
Dell P/N:C995R$AA SAMSUNG
2.Park-XT;1GB (128Mx16b*4)
Dell P/N:PXFYJ$AA HYNIX
Dell P/N:C09DT$AA SAMSUNG
(1 and 2 co-lay)

VRAM 1GB/512MB 85,86,87,88
DDR3 800MHz
Clock Generator SLG8SP585 7
AMD Graphic Park-XT (Discrete only) 80,81,82,83,84
PCIe x 16 (Discrete only)
Intel CPU Arrandale 8,9,10,11,12,13,14
DDRIII 800/1066 Channel A
DDRIII 800/1066 Channel B
DDRIII 800/1066 Slot 0 18
DDRIII 800/1066 Slot 1 19
FDIx4x2 (UMA only)
DMIx4
Discreet/UMA Co-lay
HDMI 57
LCD 54
HDMI
Level shifter 57
LVDS(Dual Channel)
RGB CRT
Intel PCH HM57
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24,25,26,27,28
CRT
Left Side: USB x 2
CRT Board 77
Bluetooth 73
CAMERA 54
USB2.0 x 4
AZALIA
Internal Analog MIC
HP1
MIC IN
2CH SPEAKER
Azalia CODEC IDT 92HD79B1 30
SPI
Flash ROM 4MB 62
LPC Bus
LPC debug port 70
KBC NUVOTON NPCE781BA0DX 37
SPI
SMBus
Flash ROM 256kB 62
Touch PAD 68
Int. KB 68
Thermal Main:G7922 Sec.EMC2102 39
Fan 58
PCIE x 3
SATA x 1
USB 2.0 x 4
USB 2.0 x 1
SATA x 2
I/O Board Connector 76
PCIE x 1
USB x 1
PCIE x 1
Mini-Card 802.11a/b/g
10/100 NIC Realtek RTL8103T-VB
RJ45 CONN
SATAx1 / USB2.0x1
ESATA/USB Combo
PCIE x 1,USB x 1
Mini-Card WWAN
SIM
USB 2.0 x 1
Right Side: USB x 1
CardReader Realtek RTS5159 78
SD/MMC+/MS/ MS Pro/xD
HDD 59
ODD 59

CPU DC/DC ISL62883 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC RT8205B 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW

SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE

VGA RT8208B 89	
INPUTS	OUTPUTS
+PWR_SRC	+VGA_CORE

TI CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_RUN_VGA

SYSTEM DC/DC APL5930 90	
INPUTS	OUTPUTS
+1.5V_SUS	+1.0V_RUN_VGA

Switches	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Bottom

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Title: Block Diagram
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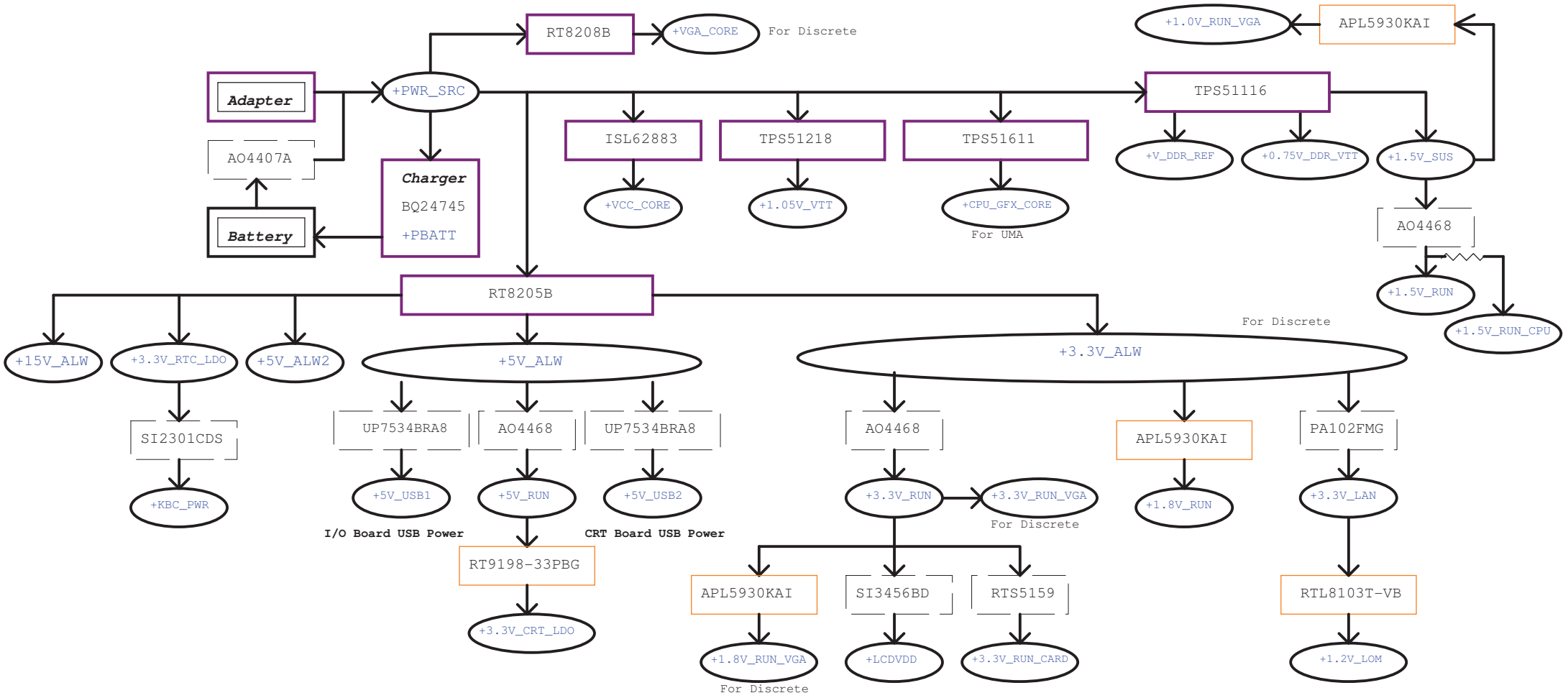

Power Shape

Regulator | **LDO** | **Switch**

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Title: ***Power Block Diagram***

Size	Document Number	Rev
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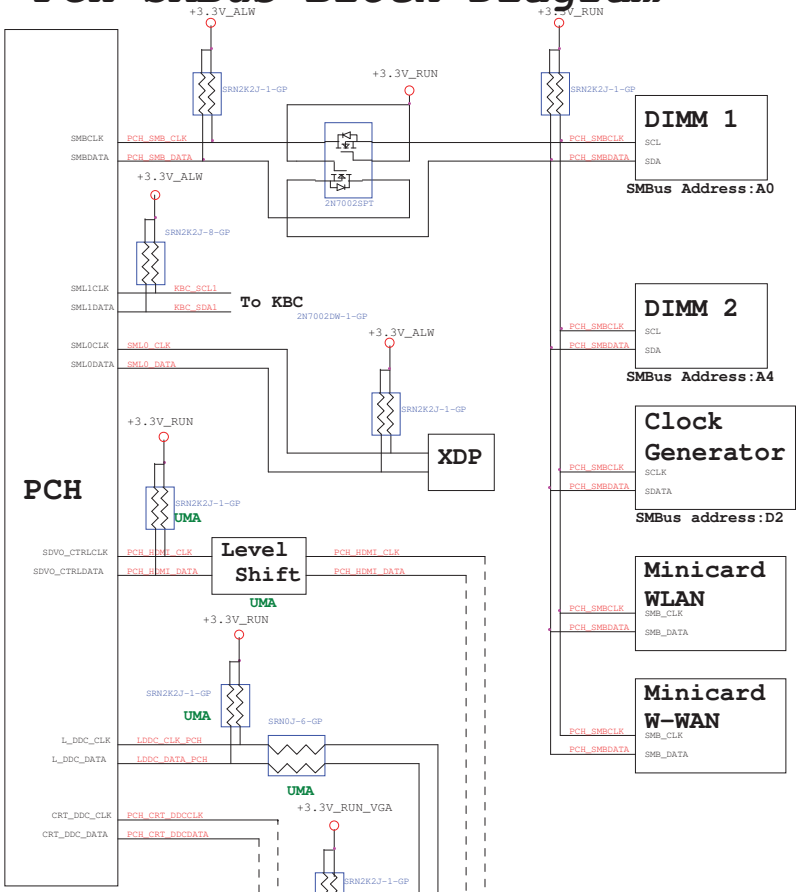
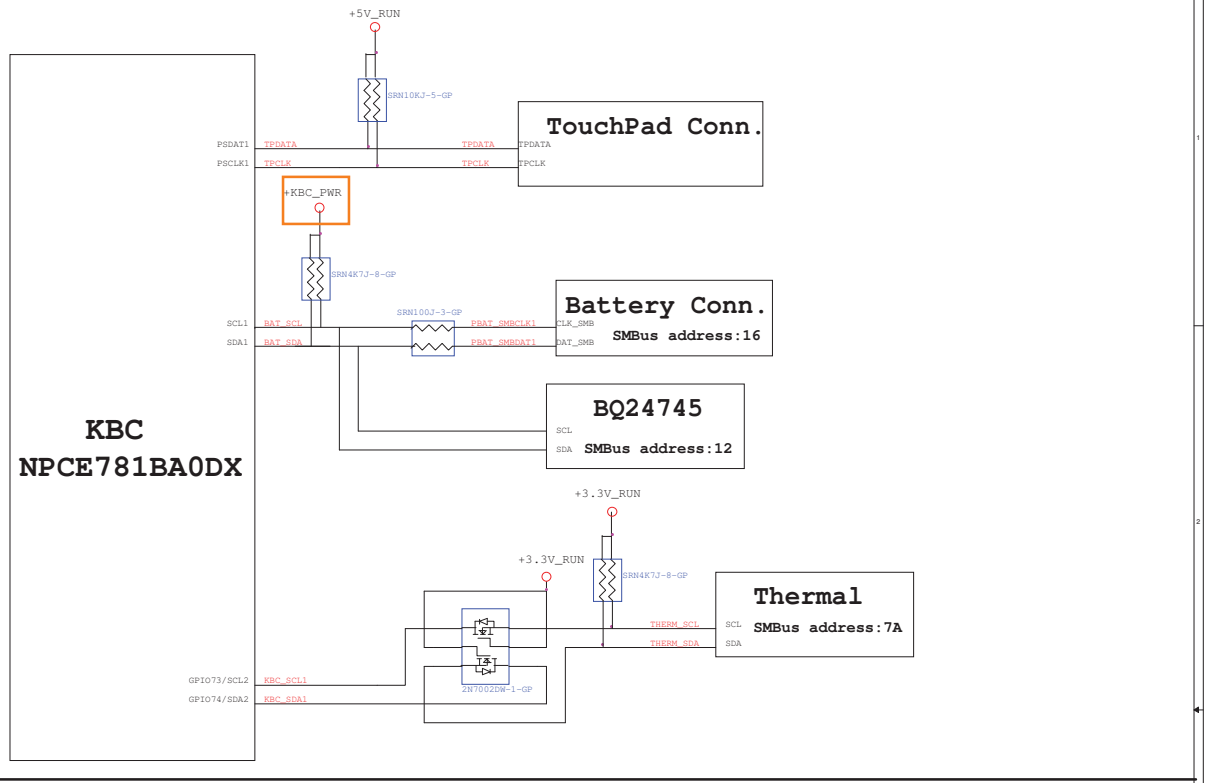
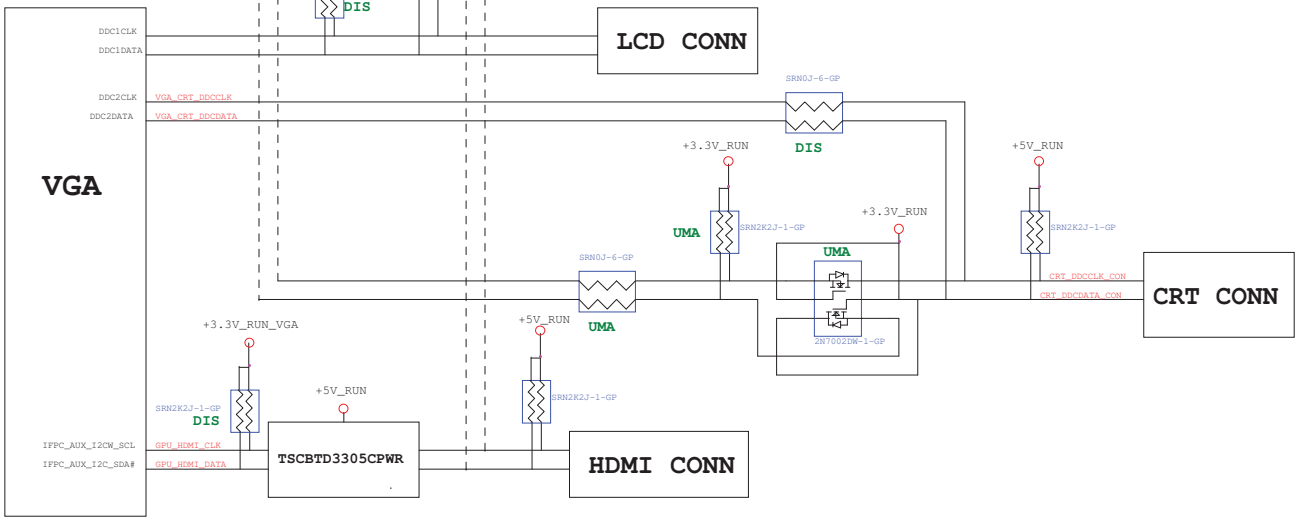
PCH SMBus Block Diagram



KBC SMBus Block Diagram





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Title: SMBUS Block Diagram

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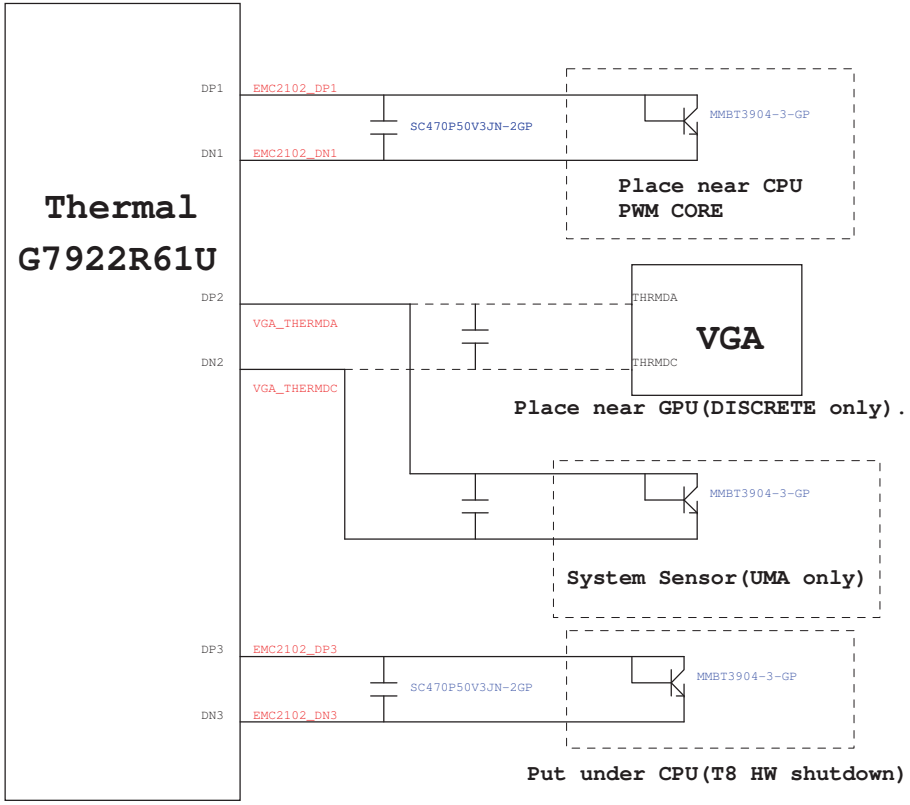
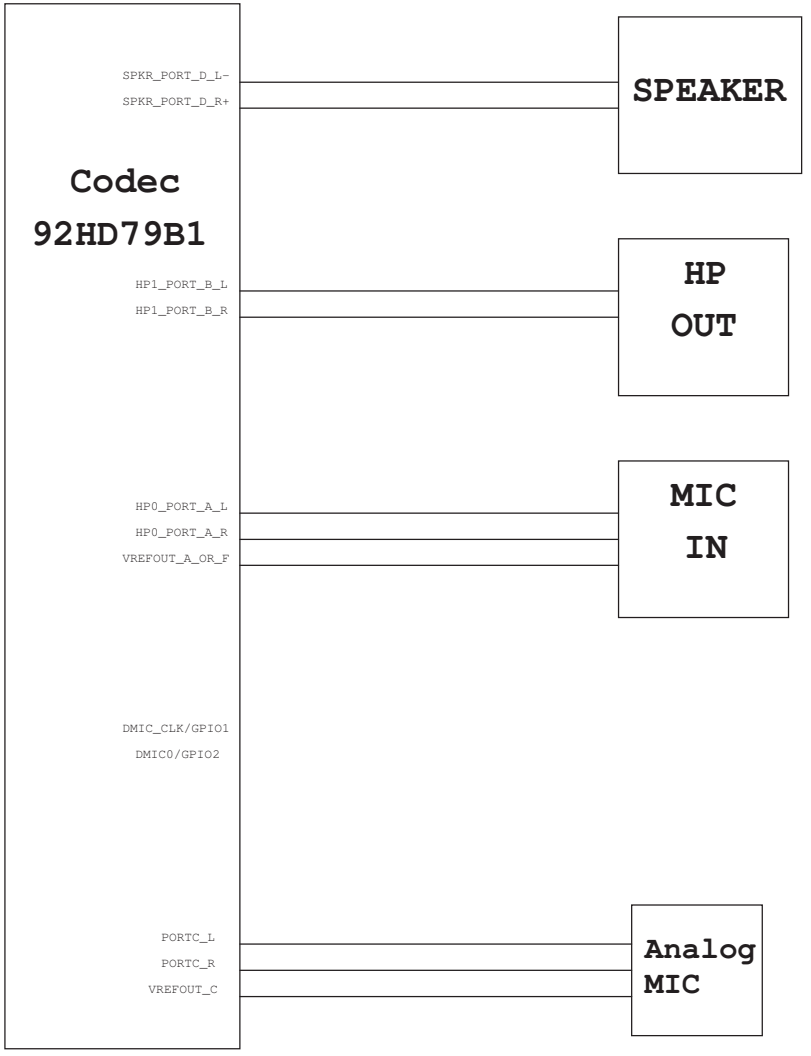
Thermal Block Diagram



Audio Block Diagram



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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#/GPIO51	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCIE Routing

LANE1	RESERVED
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	W-WAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	H55/HM55 no support
LANE8	H55/HM55 no support

USB Table

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	RESERVED
4	CARD READER
5	BLUETOOTH
6	HM55 no support
7	HM55 no support
8	USB1 (I/O Board)
9	USB0 (I/O Board ESATA)
10	RESERVED
11	W-WAN (I/O Board)
12	RESERVED
13	CAMERA

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	HM55 no support
3	HM55 no support
4	ESATA
5	RESERVED

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Title: Table of Content

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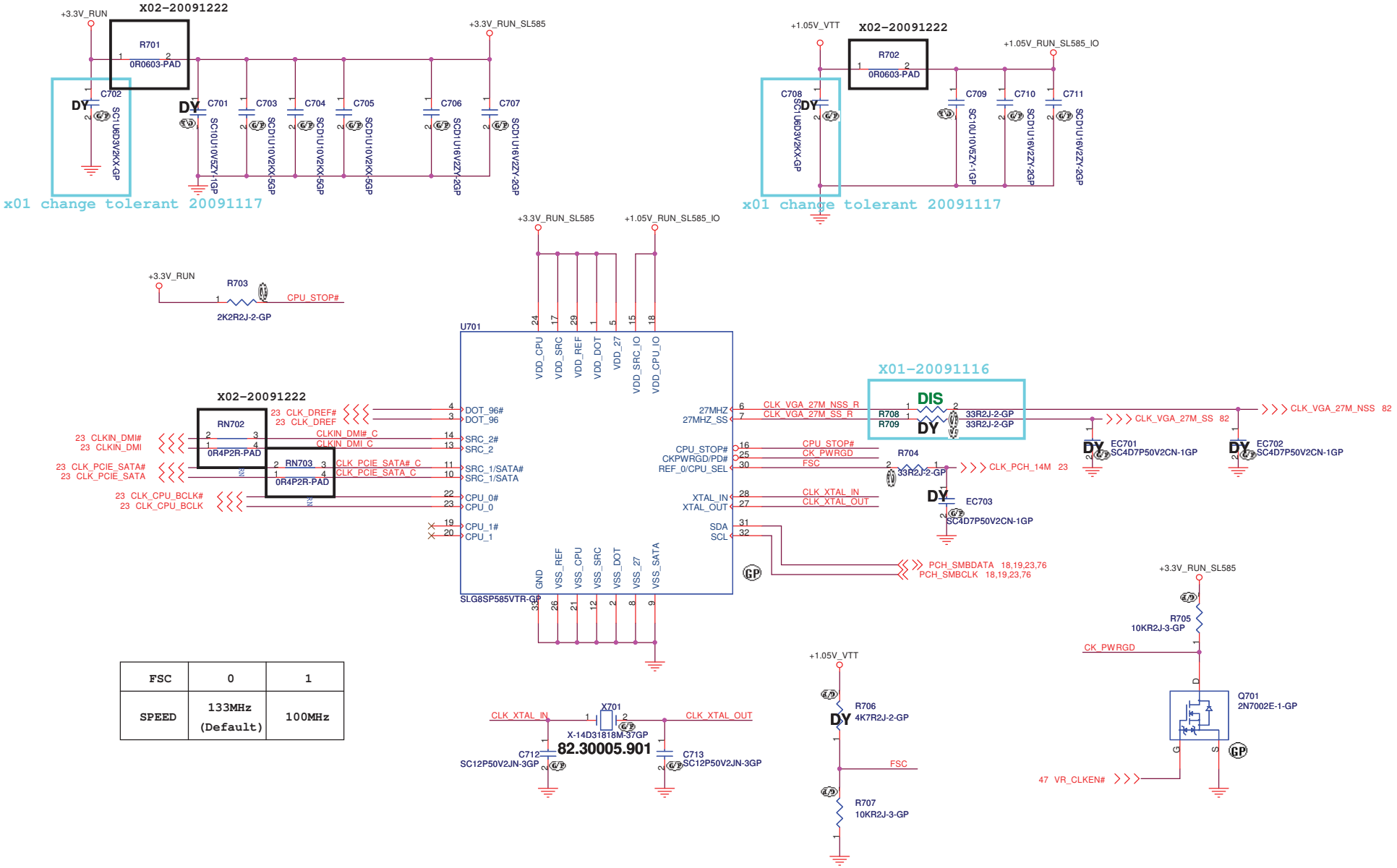
SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator SLG8SP585

Size	Document Number	Rev
	Berry	A00

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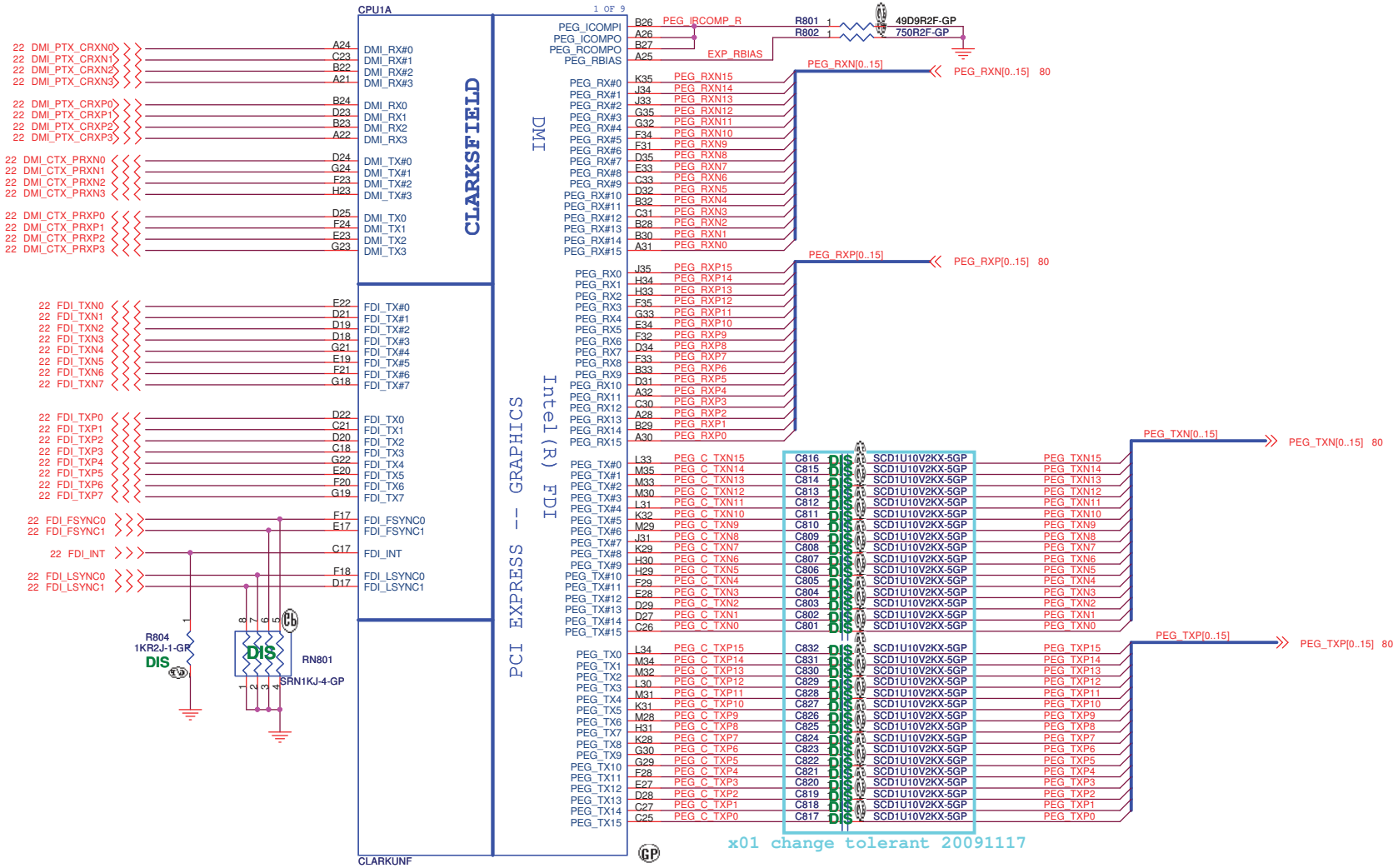
SSID = CPU



62.10055.341

SEC. 62.10053.561

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Title		
CPU (PCIE/DMI/FDI)		
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SSID = CPU

Processor Pullups

Processor Compensation Signals

CLARKSFIELD

CLARKUNF

X02-20091222

X01 20091121
VTTPWRGOOD signal must be clean and close to CPU

For EMI

x01 change tolerant 20091117

X01 20091112

A00-20100226

A00-20100208

X01 20091117

X03-20100118

X01 20091111

DDR3 Compensation Signals

X02-20091224

JTAG MAPPING	
Scan Chain (Default)	Stuff --> R928, R931, R934 No Stuff --> R929, R933
CPU Only	Stuff --> R928, R929 No Stuff --> R931, R934, R933
GMCH Only	Stuff --> R933, R934 No Stuff --> R928, R929, R931

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Title: CPU (THERMAL/CLOCK/PM)

Size | Document Number: Berry | Rev: A00

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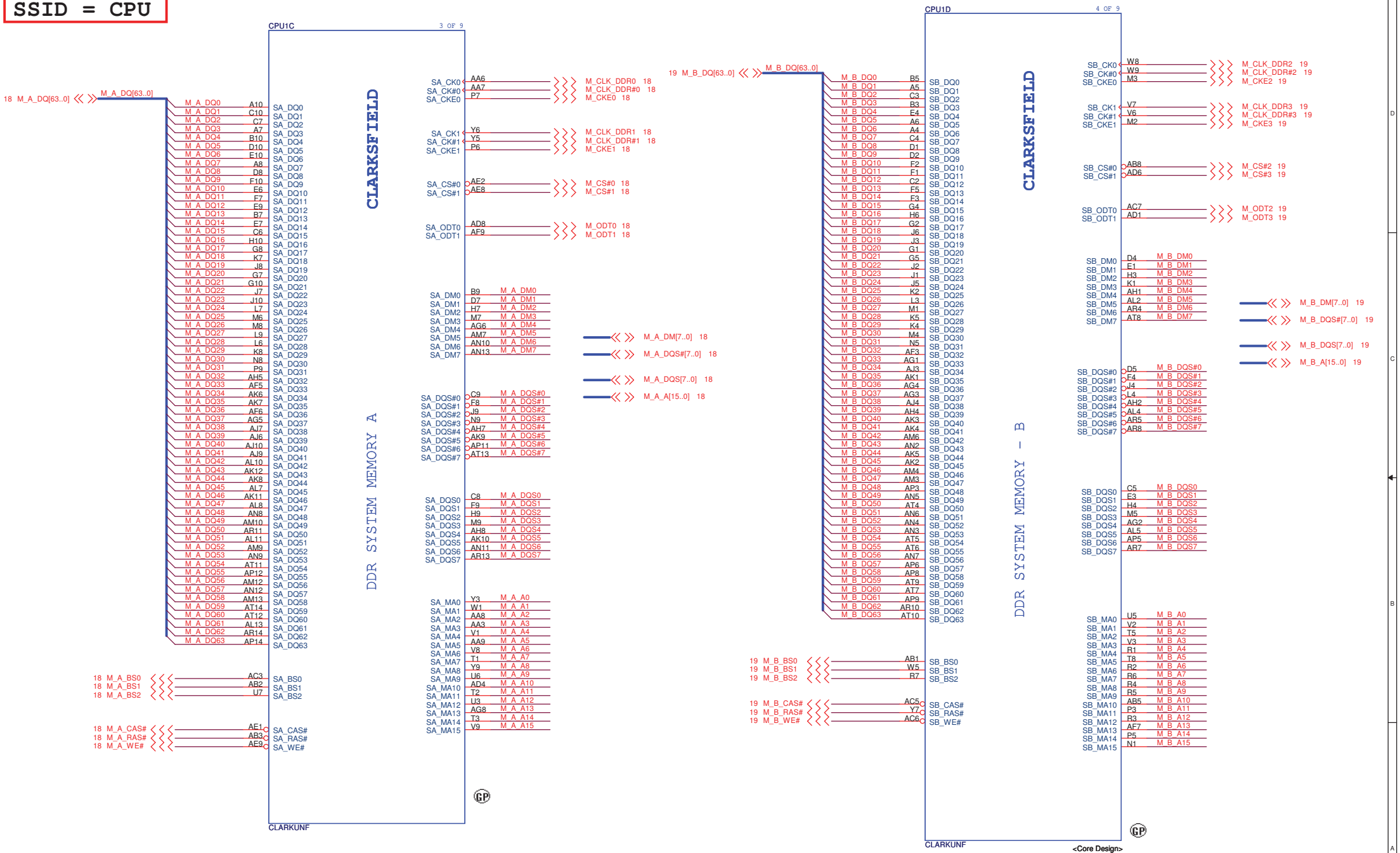
SSID = CPU



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Title	CPU (DDR)	
Size	Document Number: Berry	Rev: A00
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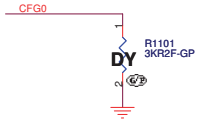
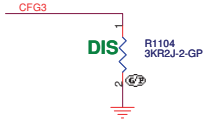
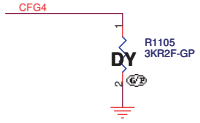
SSID = CPU



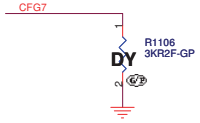
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



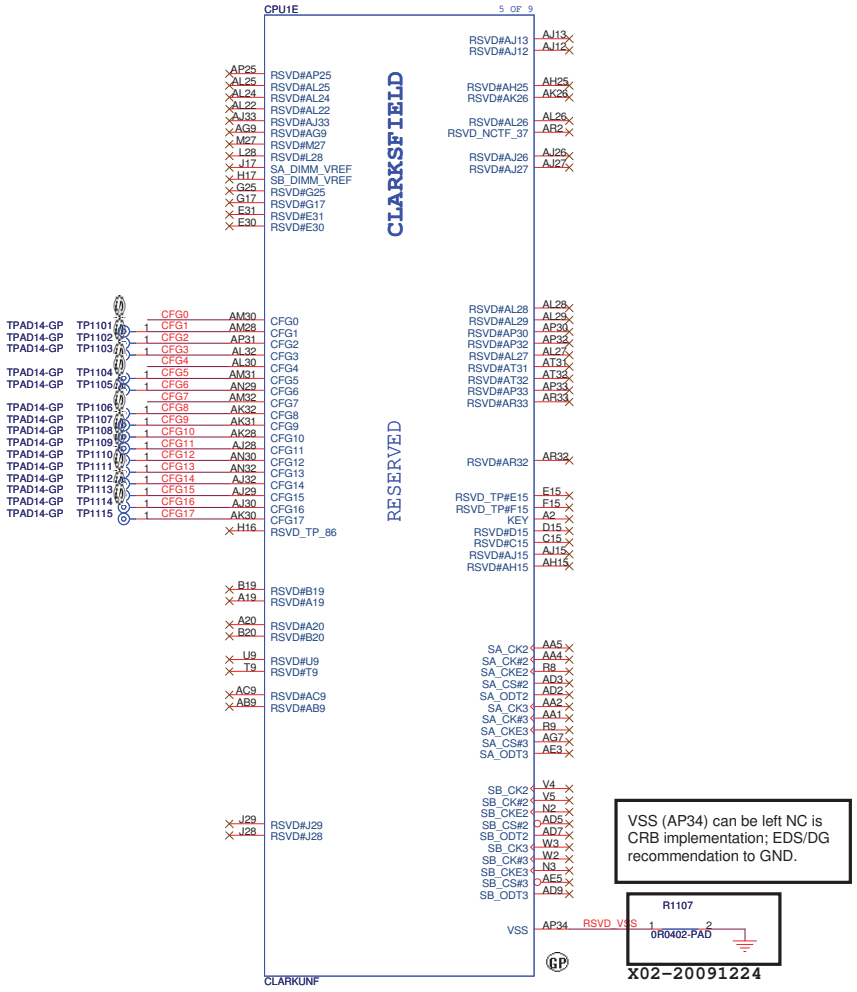
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

X02-20091224

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Title		
CPU (RESERVED)		
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SSID = CPU

PROCESSOR CORE POWER

48A

+VCC_CORE

CPU1F

6 OF 9

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

CLARKUNF

x01 change tolerant 20091117

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

POWER

CPU VIDS

PSI# AN33 → PSI# 47

VID AK35 H_VID0, AK33 H_VID1, AK34 H_VID2, AL35 H_VID3, AL33 H_VID4, AM33 H_VID5, AM35 H_VID6 → H_VID[6..0] 47

PROC_DPRSLPVR AM34 → PM_DPRSLPVR 47

VTT_SELECT G15 H_VTTVID1 → TP1201 TPAD14-GP

H_VTTVID1 = Low, 1.1V

H_VTTVID1 = High, 1.05V

SENSE LINES

ISENSE AN35 → IMVP_IMON 47

VCC_SENSE AJ34, VSS_SENSE AJ35 → VCC_SENSE 47, VSS_SENSE 47

VTT_SENSE B15, VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT → VTT_SENSE 49, TP1202 TPAD14-GP

R1201 100R2F-L1-GP-U

R1202 100R2F-L1-GP-U

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Title: CPU (VCC_CORE)

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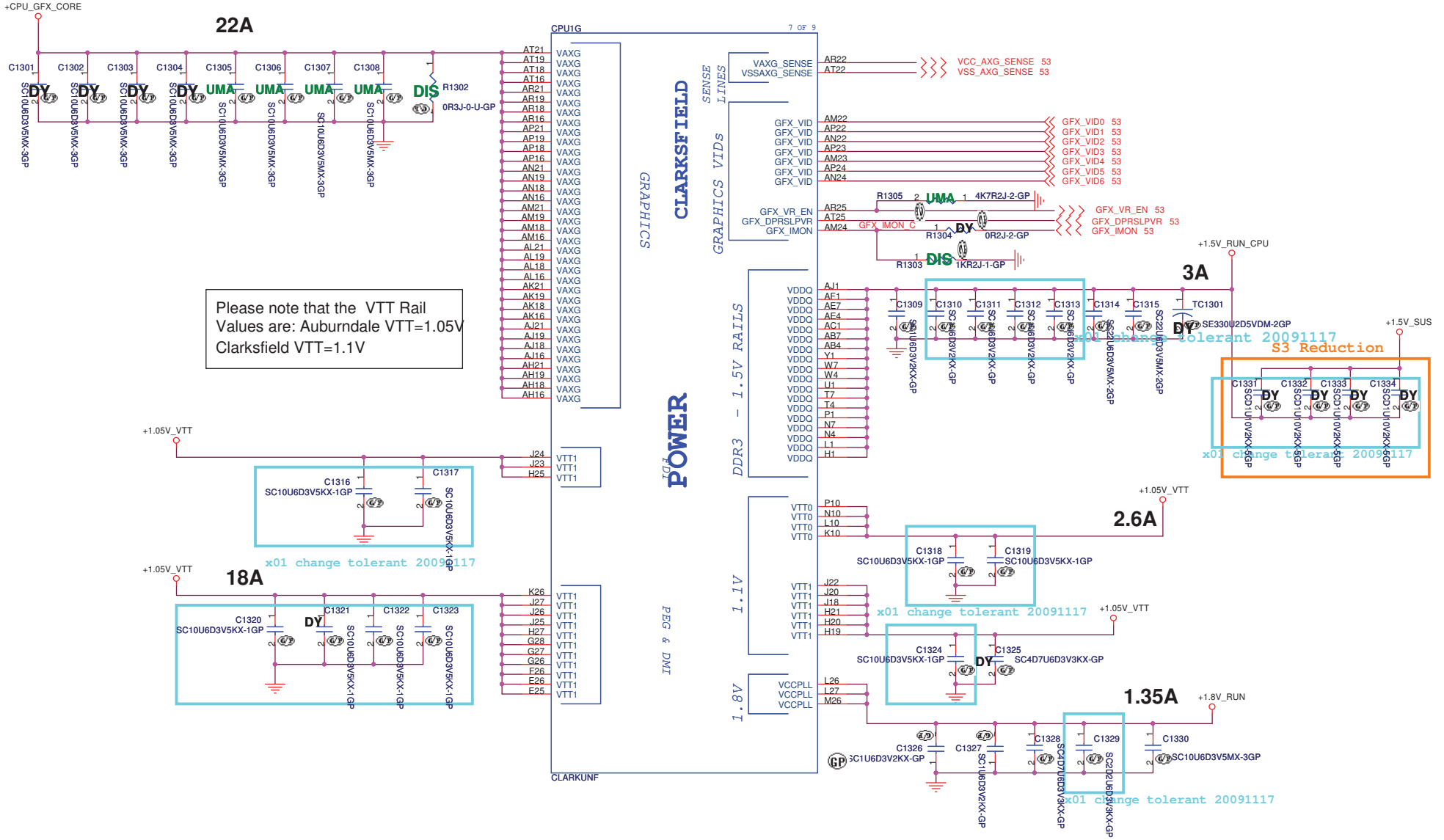
SSID = CPU



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Title: CPU (VCC_GFXCORE)

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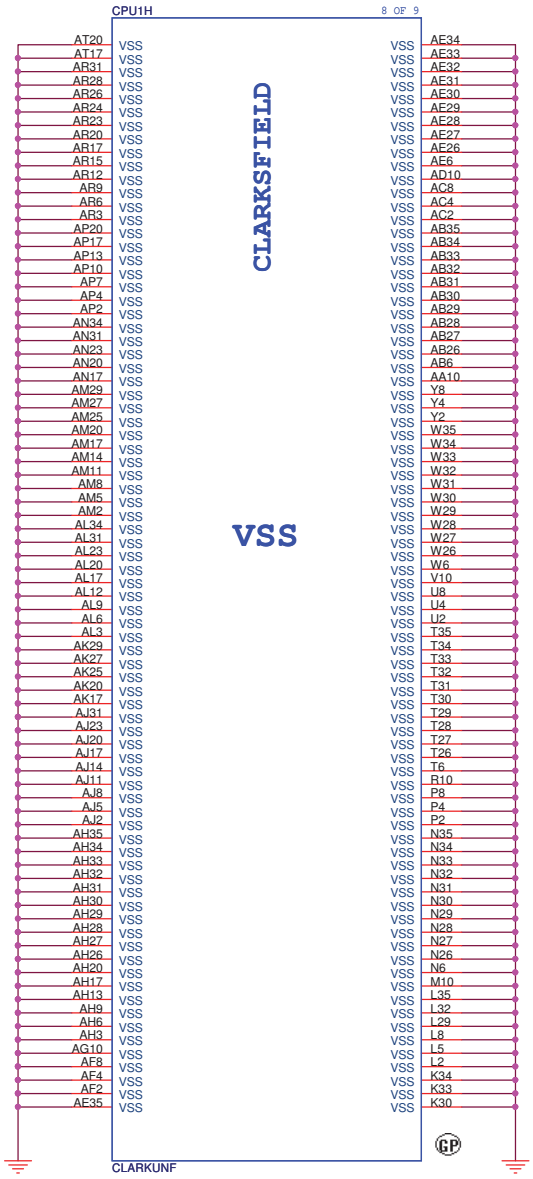
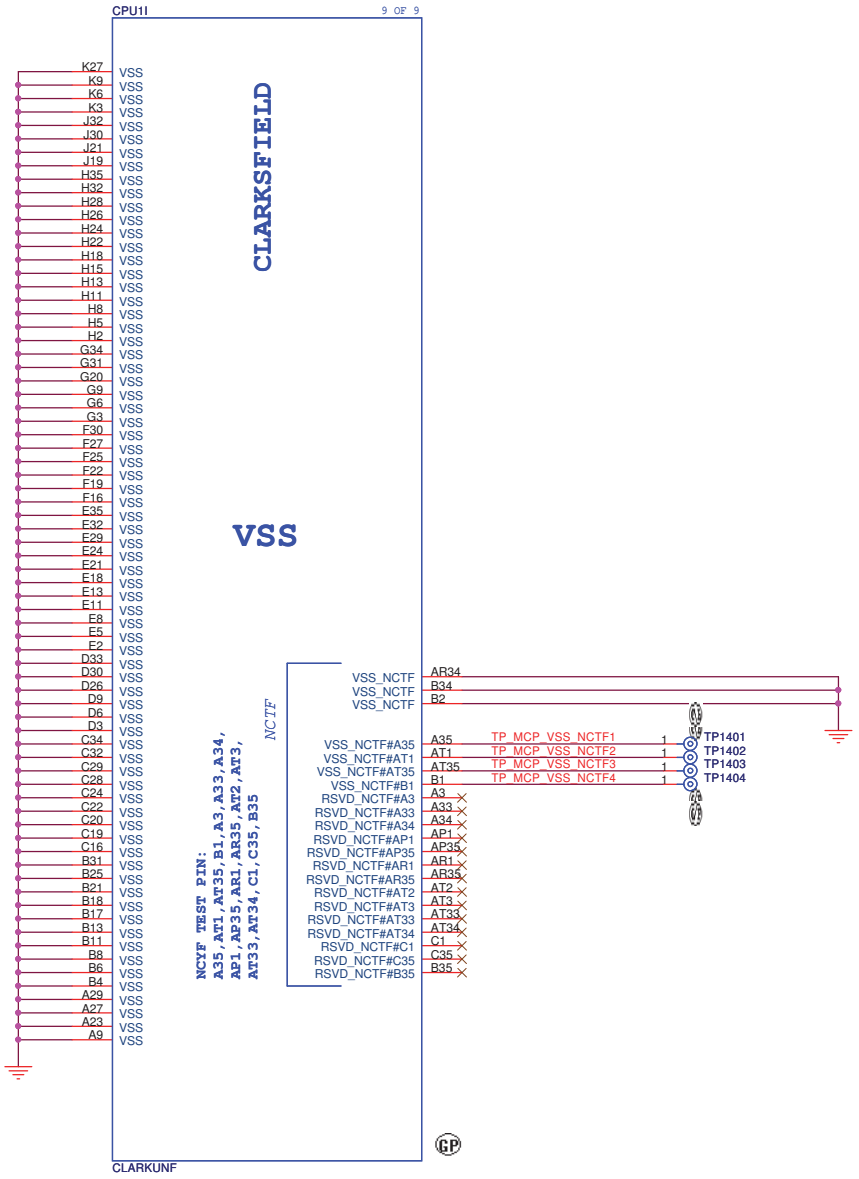
SSID = CPU





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Title	CPU (VSS)	
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Title: *Reserved*

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Size: A3 | Document Number: *Berry* | Rev: *A00*

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Title: *Reserved*

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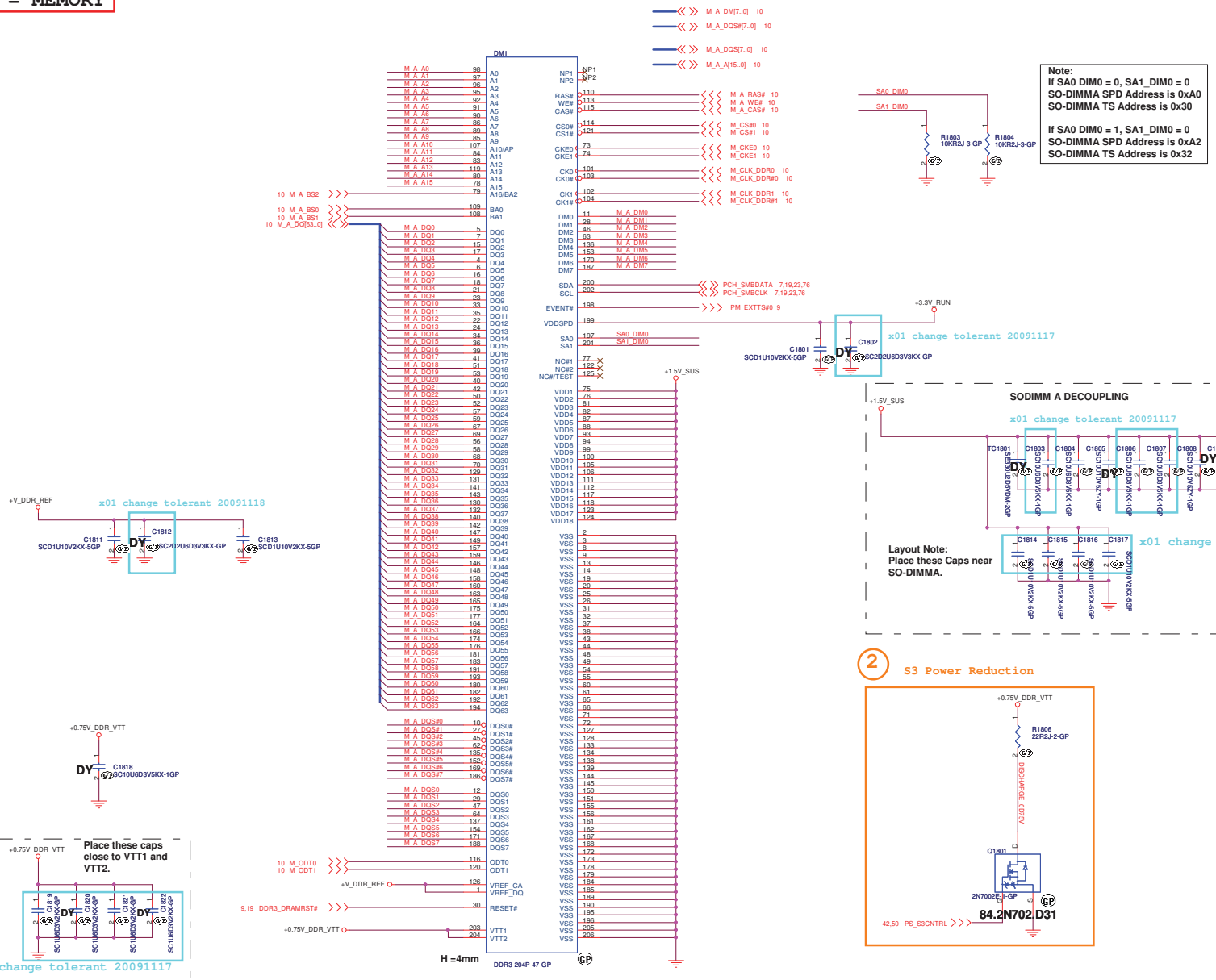
SSID = MEMORY



62.10017.P31

SEC. 62.10017.P11

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Title: DDR3-SODIMM1

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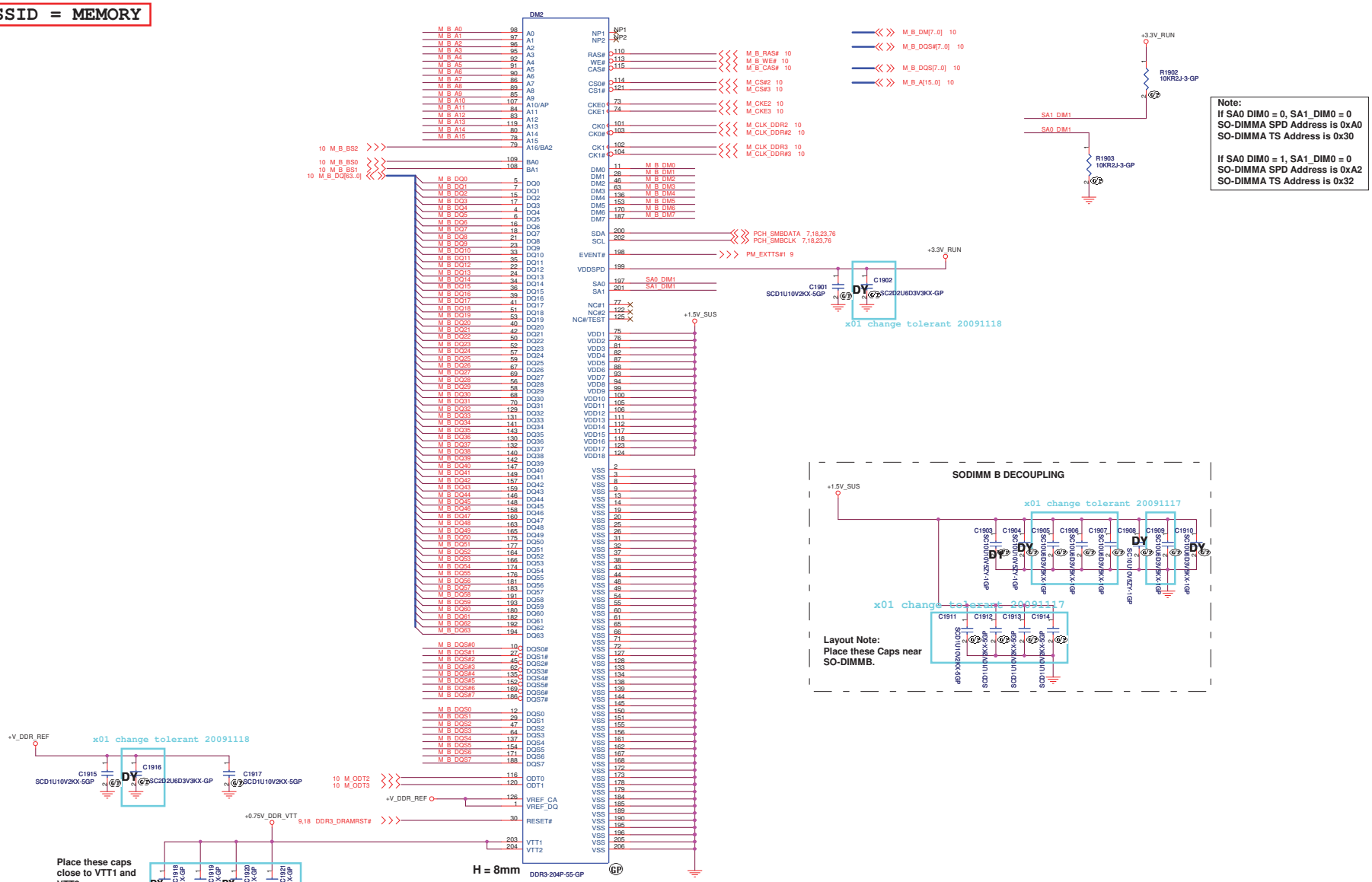
SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM B DECOUPLING

Layout Note:
Place these Caps near SO-DIMMB.

Place these caps close to VTT1 and VTT2.

62.10017.Q31

SEC. 62.10017.N71

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

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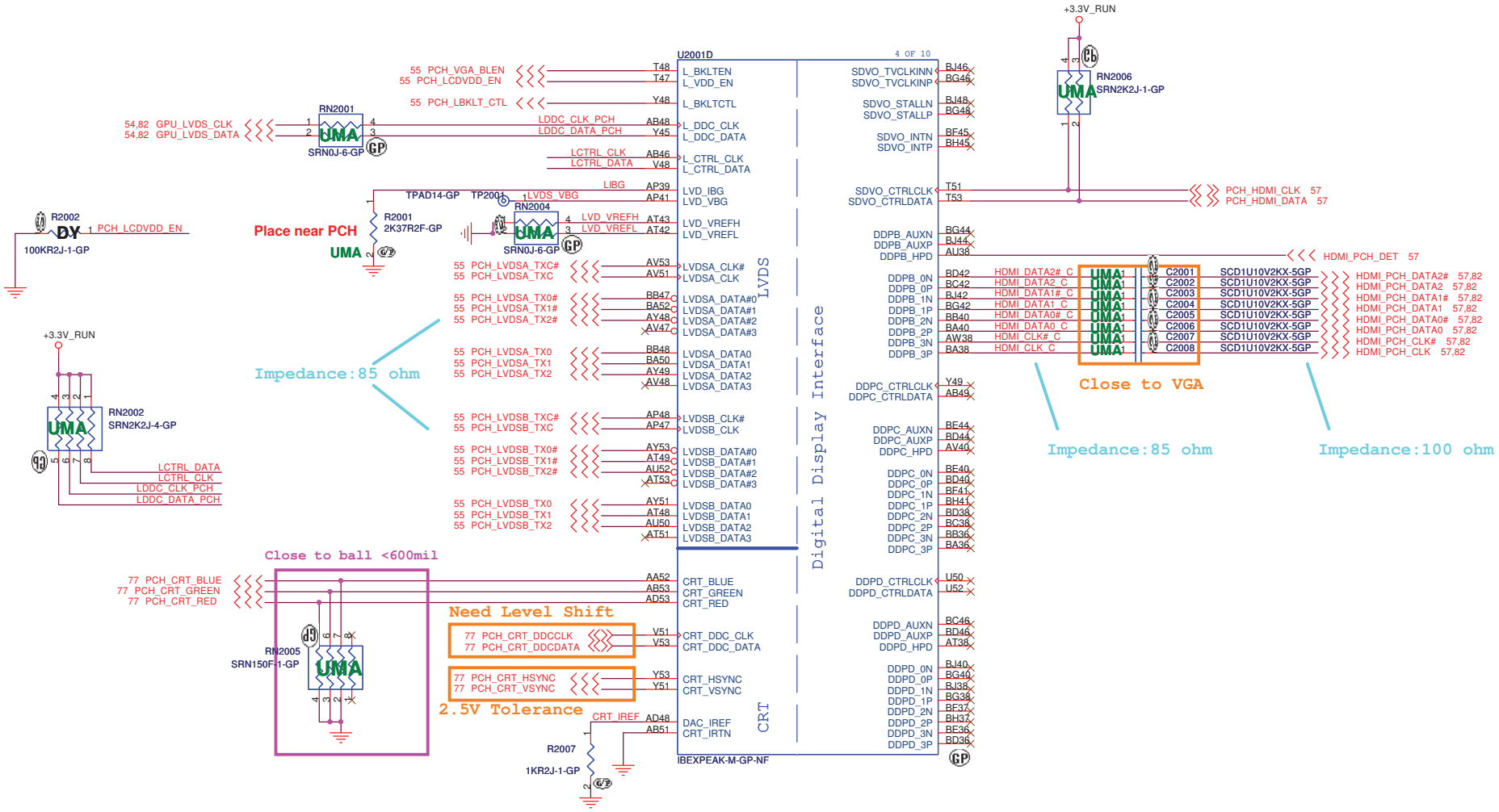
Title: DDR3-SODIMM2

Size | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 19 of 92



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (LVDS/CRT/DDI)	
Size	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet 20 of 92	

SSID = PCH

RN2101 SRN8K2J-2-GP-U
RN2103 SRN8K2J-2-GP-U
RN2102 SRN8K2J-4-GP
RN2104 SRN8K2J-2-GP-U

U2001E — IBEXPEAK-M-GP-NF — 5 OF 10

BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:
Disabled when Low.
Enable when High.

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	X
4	CARD READER
5	BLUETOOTH
6	X
7	X
8	USB1 (I/O Board)
9	ESATA (I/O Board COMBO)
10	X
11	W-WAN (I/O Board)
12	X
13	CAMERA

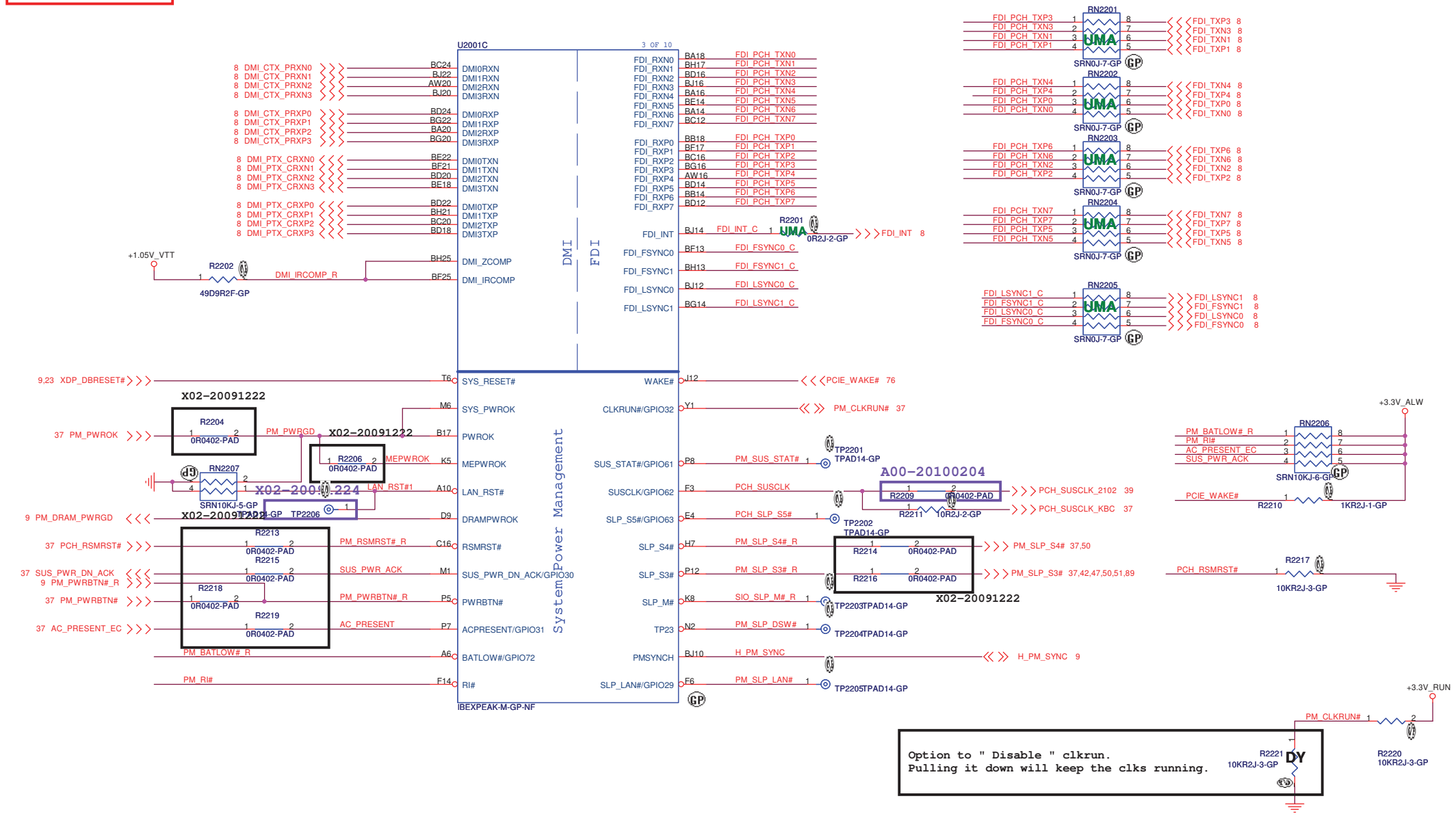
KBC CLK EMI

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: Document Number: Berry
Rev: A00
Date: Monday, March 29, 2010 Sheet 21 of 92

SSID = PCH



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (DM I/FDI/PM)	
Size	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet 22 of 92	

SSID = PCH

U2001B

2 OF 10

IBEXPEAK-M-GP-NF

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

x01 change tolerant 20091117

X01 20091118

DIS uses 0ohm 63.R0034.1DL
UMA uses 12pF 78.12034.1FL

X01 2009/11/06

X01 2009/11/05

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 23 of 92

SSID = PCH

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

X01 20091118 layout swap

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

For EMI

x01 Change tolerant 20091117

x01 Change tolerant 20091117

HDD

ODD

ESATA

IBEXPEAK-M-GP-NF

<Core Design>

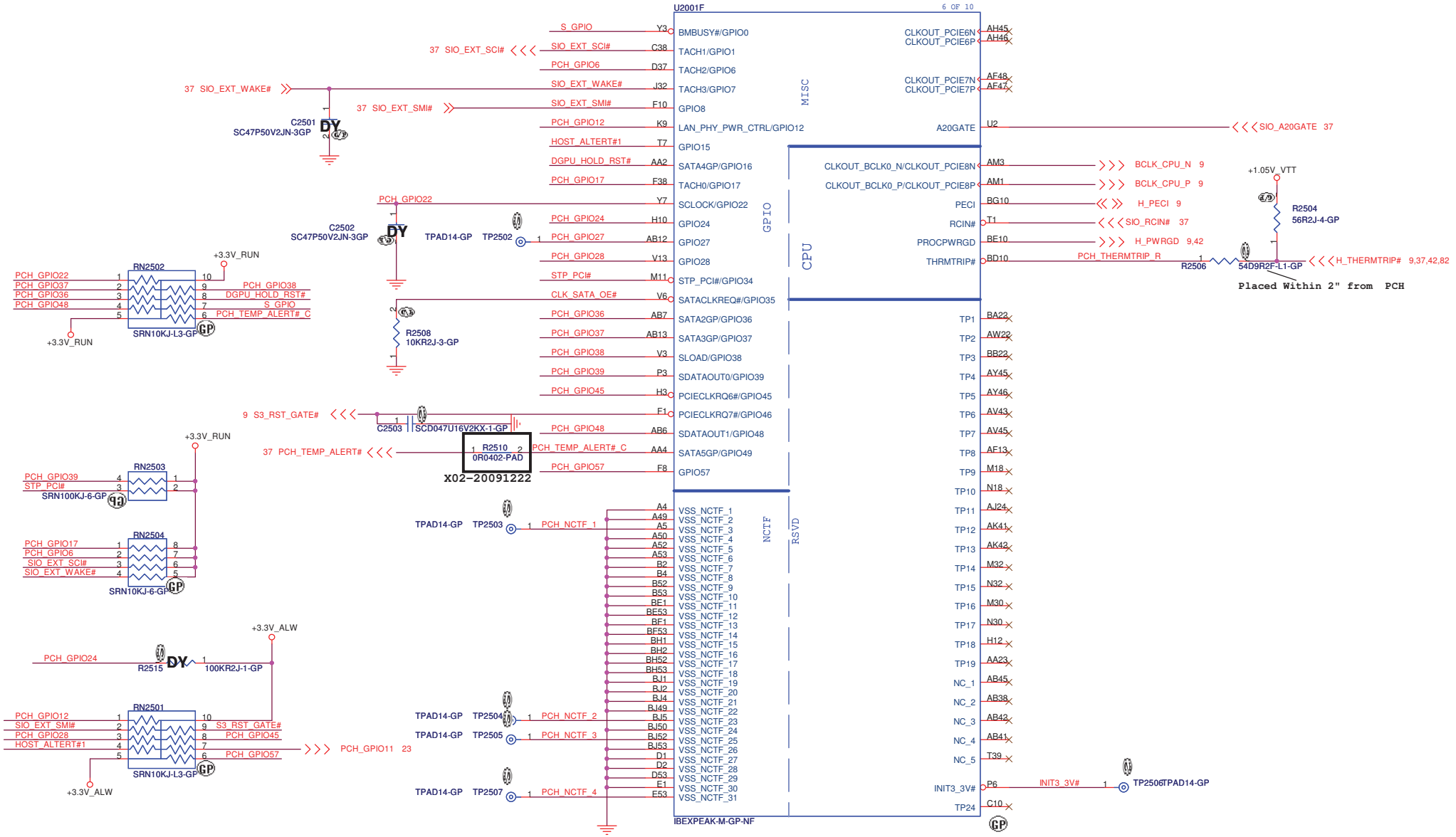
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
	Berry	A00

Date: Monday, March 29, 2010 Sheet 24 of 92

SSID = PCH

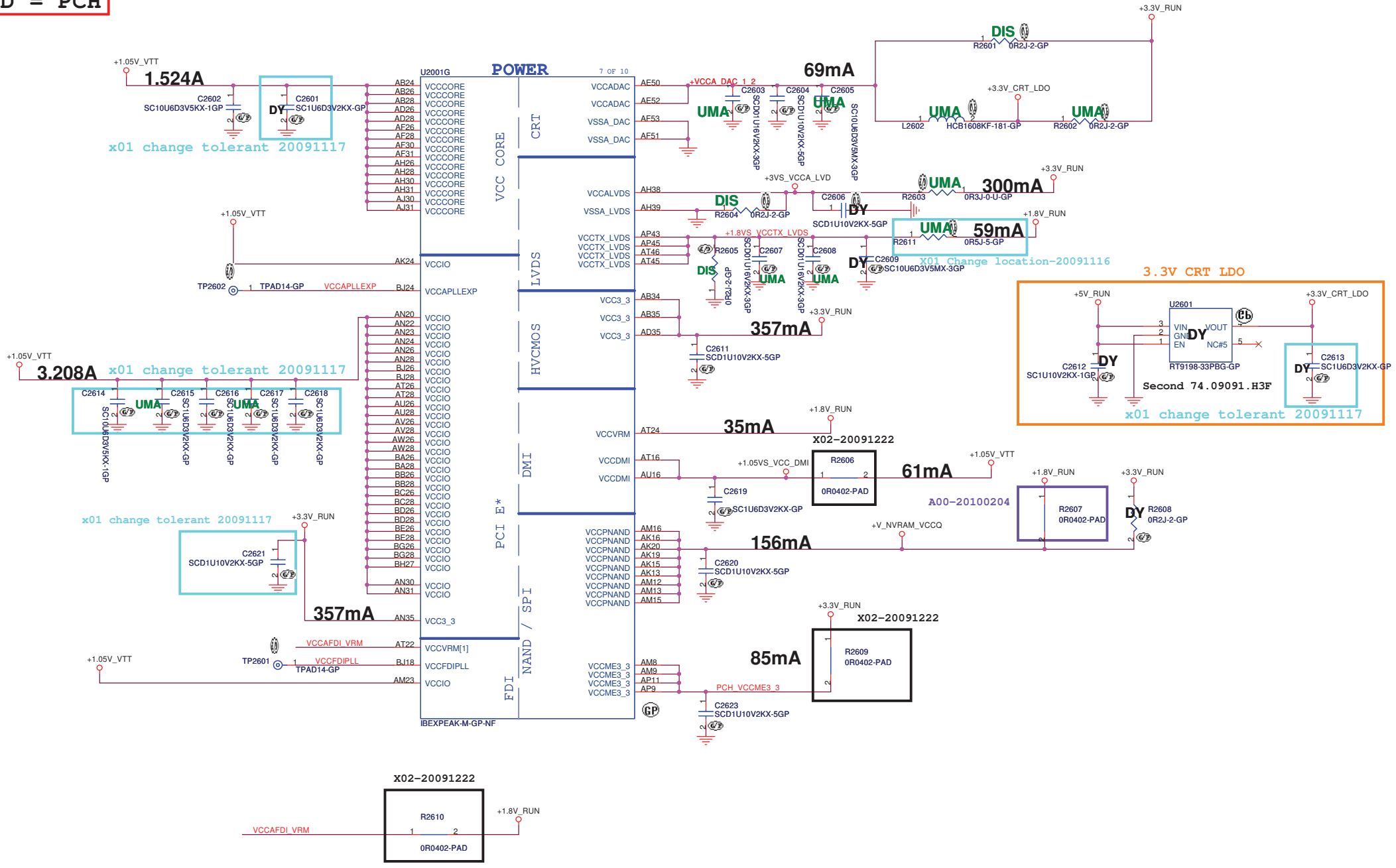


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (GPIO/CPU)	
Size	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet 25 of 92	

SSID = PCH


POWER
U2001G
7 OF 10
IBEXPEAK-M-GP-NF
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.524A
3.208A
69mA
300mA
59mA
357mA
35mA
61mA
156mA
85mA
x01 change tolerant 20091117
x01 Change location-20091116
3.3V CRT LDO
Second 74.09091.H3F
A00-20100204
X02-20091222
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (POWER1)
Berry
A00
Wednesday, February 10, 2010
Sheet 26 of 92

SSID = PCH

U2001J POWER 10 OF 10

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | CPU | RTC | HDA

TP2701 VCCACLK TPAD14-GP

AP51 VCCACLK
AP53 VCCACLK
AF23 VCCLAN
AF24 VCCLAN
Y20 DCPSUSBYP
AD38 VCCME
AD39 VCCME
AD41 VCCME
AF43 VCCME
AF41 VCCME
AF42 VCCME
V39 VCCME
V41 VCCME
V42 VCCME
Y39 VCCME
Y41 VCCME
Y42 VCCME
V9 DCPRTC
AU24 VCCVRM
BB51 VCCADPLLA
BB53 VCCADPLLA
BD51 VCCADPLLB
BD53 VCCADPLLB
AH23 VCCIO
AJ35 VCCIO
AH35 VCCIO
AF34 VCCIO
AH34 VCCIO
AF32 VCCIO
V12 DCPSST
Y22 DCPSUS
P18 VCCSUS3_3
U19 VCCSUS3_3
U20 VCCSUS3_3
U22 VCCSUS3_3
V15 VCC3_3
V16 VCC3_3
Y16 VCC3_3
AT18 V_CPU_IO
AU18 V_CPU_IO
A12 VCCRTC
IBEXPEAK-M-GP-NF

V24 VCCIO
V26 VCCIO
Y24 VCCIO
Y26 VCCIO
V28 VCCSUS3_3
U28 VCCSUS3_3
U26 VCCSUS3_3
U24 VCCSUS3_3
P28 VCCSUS3_3
P26 VCCSUS3_3
N28 VCCSUS3_3
N26 VCCSUS3_3
M28 VCCSUS3_3
M26 VCCSUS3_3
L28 VCCSUS3_3
L26 VCCSUS3_3
J28 VCCSUS3_3
J26 VCCSUS3_3
H28 VCCSUS3_3
H26 VCCSUS3_3
G28 VCCSUS3_3
G26 VCCSUS3_3
F28 VCCSUS3_3
F26 VCCSUS3_3
E28 VCCSUS3_3
E26 VCCSUS3_3
C28 VCCSUS3_3
C26 VCCSUS3_3
B27 VCCSUS3_3
A28 VCCSUS3_3
A26 VCCSUS3_3
U23 VCCSUS3_3
V23 VCCIO
F24 V5REF_SUS
K49 V5REF
J38 VCC3_3
L38 VCC3_3
M36 VCC3_3
N36 VCC3_3
P36 VCC3_3
U35 VCC3_3
AD13 VCC3_3
AK3 VCCSATAPLL
AK1 VCCSATAPLL
AH22 VCCIO
AT20 VCCVRM
AH19 VCCIO
AD20 VCCIO
AF22 VCCIO
AD19 VCCIO
AF20 VCCIO
AF19 VCCIO
AH20 VCCIO
AB19 VCCIO
AB20 VCCIO
AB22 VCCIO
AD22 VCCIO
AA34 VCCME
Y34 VCCME
Y35 VCCME
AA35 VCCME
L30 VCCSUSHDA

C2705 SC1U6D3V2KX-GP DY
C2706 SCD1U10V2KX-5GP
C2709 SCD1U10V2KX-5GP
C2718 SCD1U10V2KX-5GP
C2719 SCD1U10V2KX-5GP
C2727 SC1U6D3V2KX-GP
C2733 SC1U6D3V2KX-GP
C2703 SCD1U10V2KX-5GP
C2704 SC10U6D3V5MX-GP DY
C2707 SC10U6D3V5KX-1GP
C2708 SC1U6D3V2KX-GP
C2710 SC1U6D3V2KX-GP DY
C2711 SC10U6D3V5MX-3GP DY
C2712 SC1U6D3V2KX-GP
C2713 SC1U10V2KX-1GP
C2714 SCD1U10V2KX-5GP
C2715 SC1U10V2KX-1GP
C2716 SC10U6D3V5MX-3GP DY
C2717 SC1U6D3V2KX-GP
C2720 SC1U6D3V2KX-GP
C2721 SC1U6D3V2KX-GP
C2722 SC1U6D3V2KX-GP
C2725 SCD1U10V2KX-5GP
C2726 SCD1U10V2KX-5GP
C2728 SCD1U10V2KX-5GP
C2729 SCD1U10V2KX-5GP
C2730 SC10U6D3V5KX-1GP
C2731 SCD1U10V2KX-5GP
C2732 SCD1U10V2KX-5GP
C2734 SCD1U10V2KX-5GP
C2735 SCD1U10V2KX-5GP

L2702 IND-10UH-218-GP
L2703 IND-10UH-218-GP
D2701 CH751H-40PT-GP
D2702 CH751H-40PT-GP
R2702 10R2J-2-GP
R2701 10R2J-2-GP
R2703 0R0402-PAD
TP2702 VCCSATAPLL TPAD14-GP

+1.05V_VTT
+3.3V_ALW
+3.3V_RUN
+5V_ALW
+5V_RUN
+1.8V_RUN
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+VCCRTCEXT
+VCCSST
+1.05VALW_INT_VCCSUS
+5VALW_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+VCCSUSHDA
DCPSUSBYP

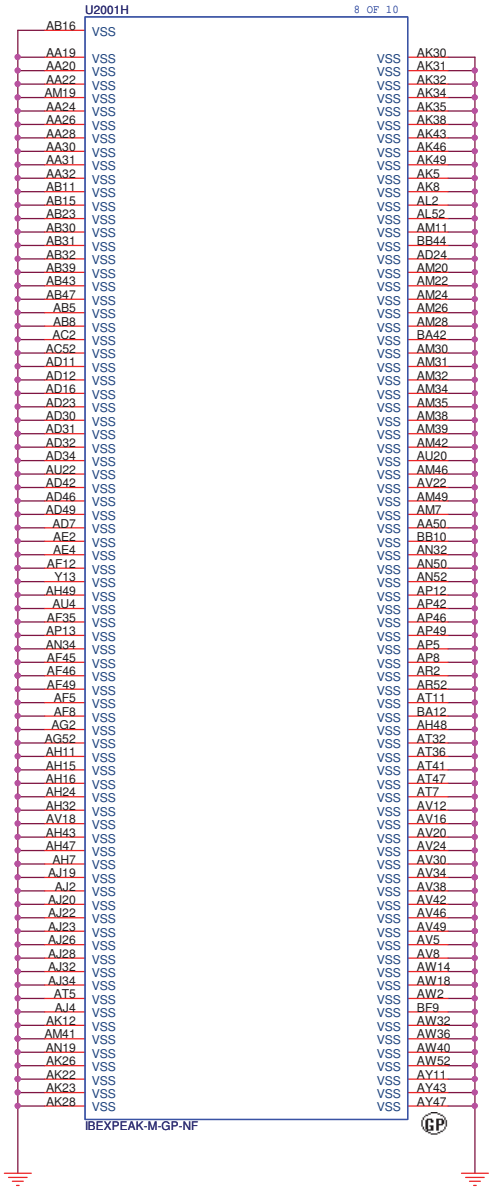
x01 change tolerant 20091117
x01 20091121
x01 change tolerant 20091118
1.998A
72mA
73mA
163mA
1mA
2mA
6mA
x02-20091222

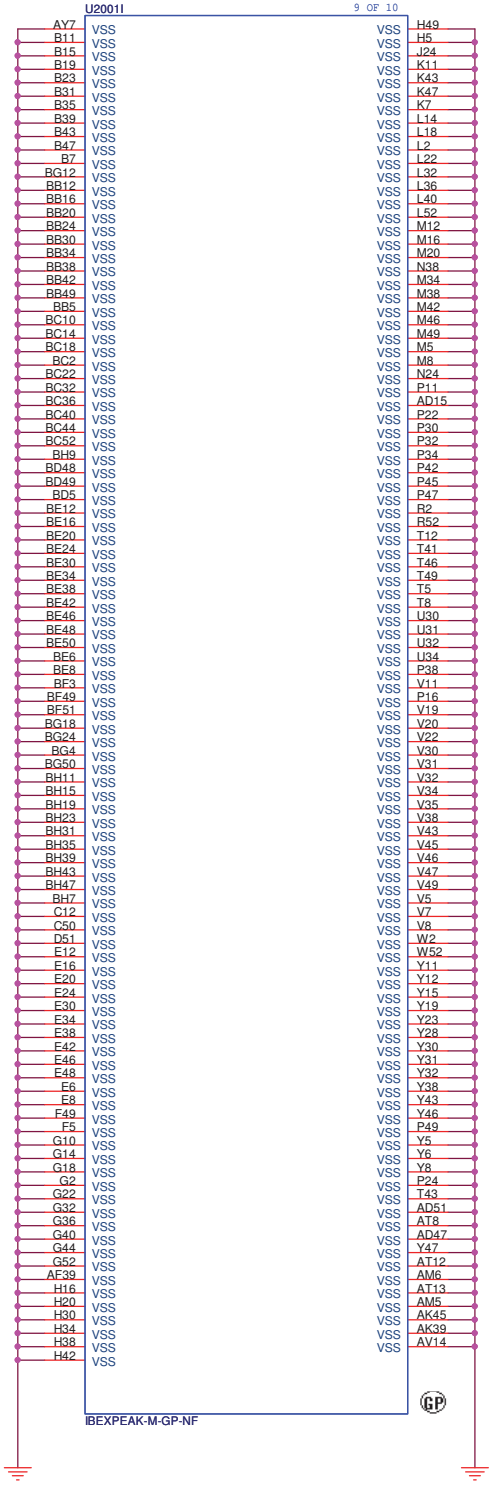
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER2)
Size:
Document Number: Berry
Rev: A00
Date: Wednesday, February 10, 2010 Sheet 27 of 92

SSID = PCH





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size	Document Number	Rev
	Berry	A00

Date: Wednesday, February 10, 2010 Sheet 28 of 92

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<Core Design>

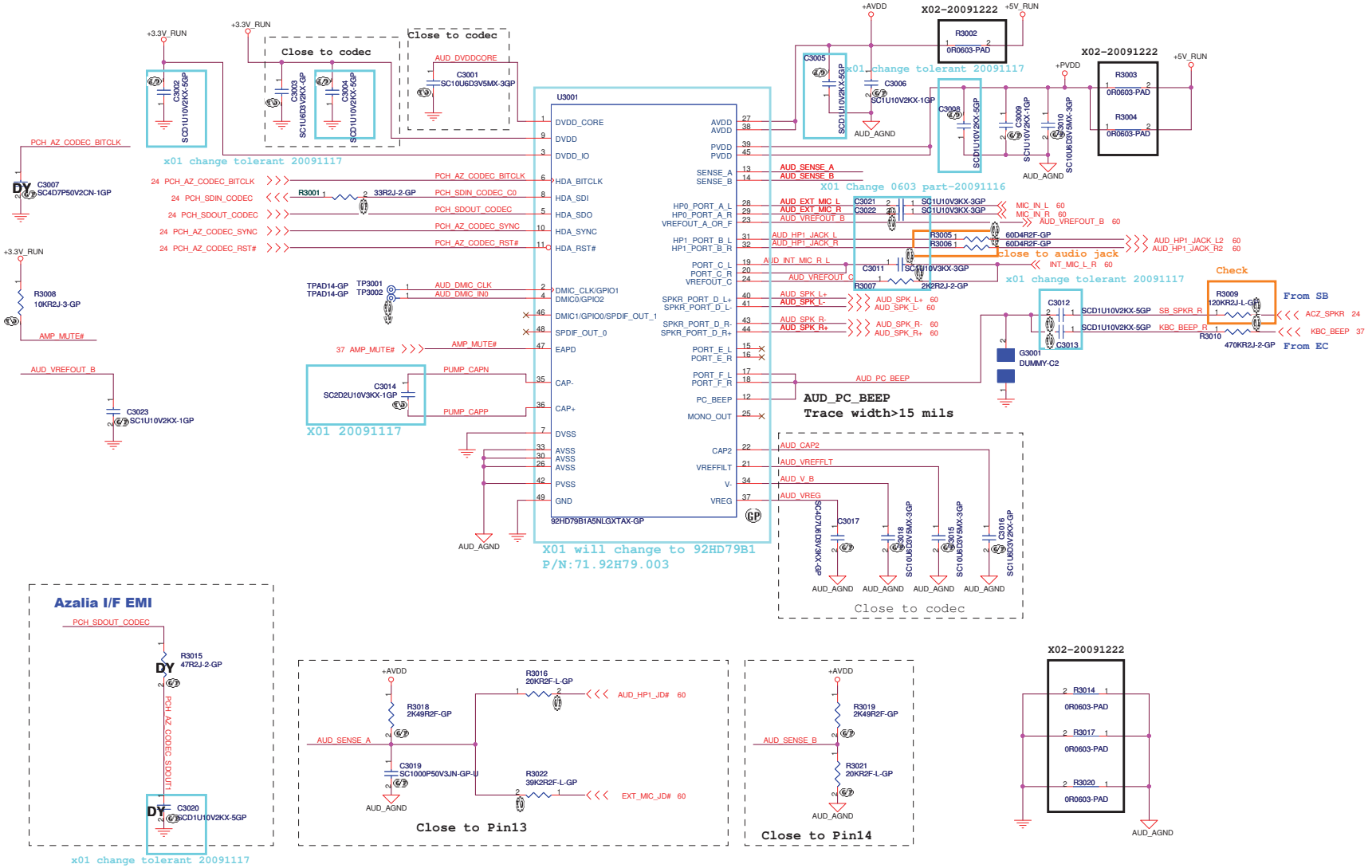
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 29 of 92

SSID = AUDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD81B1

Size	Document Number	Rev
Custom	Berry	A00

Date: Monday, March 29, 2010 Sheet 30 of 92

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 31 of 92

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
Custom	Berry	A00

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 33 of 92

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 34 of 92

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 35 of 92

(Blanking)

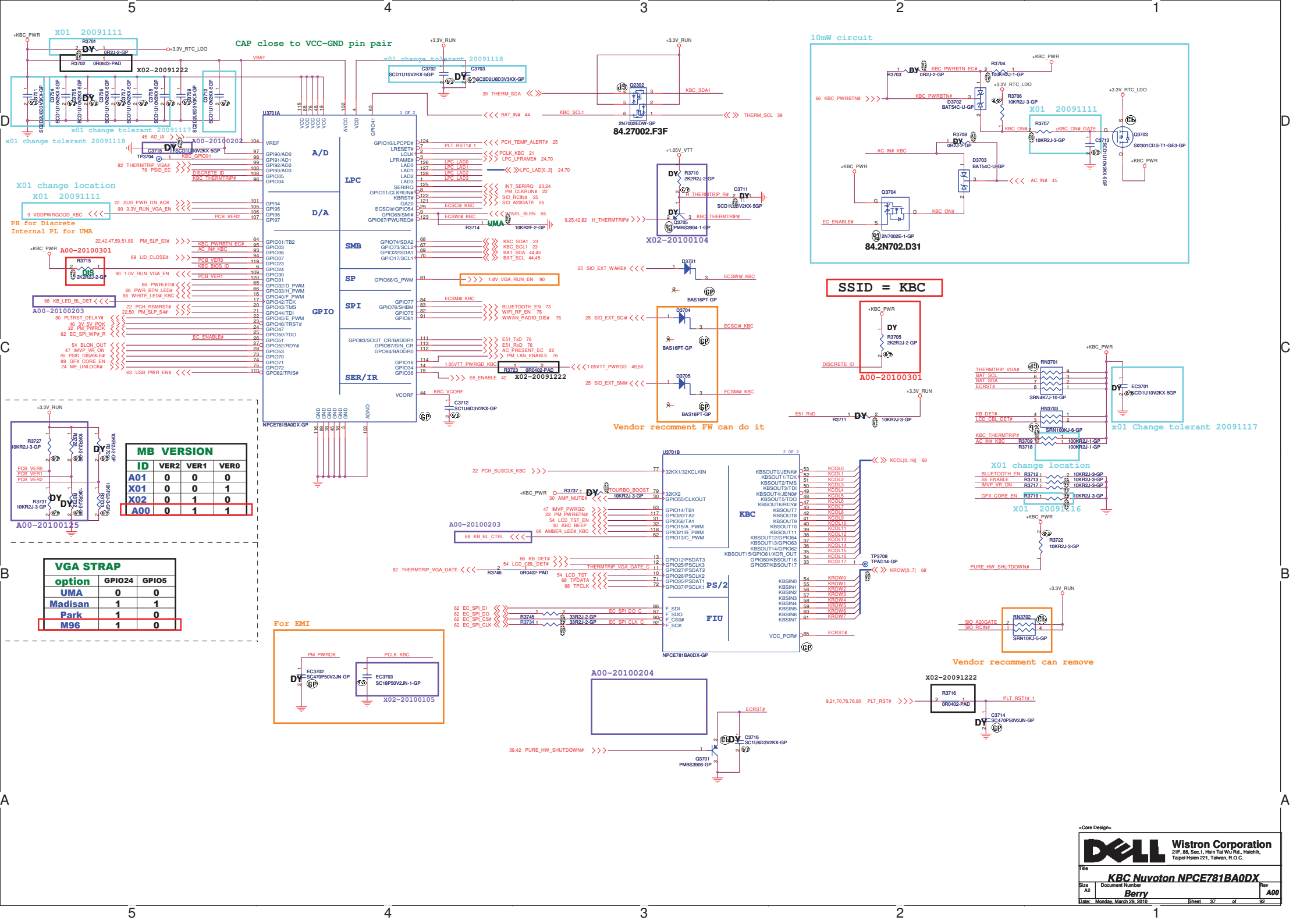
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 36 of 92


CAP close to VCC-GND pin pair
10mW circuit
SSID = KBC
MB VERSION
ID VER2 VER1 VER0
A01 0 0 0
X01 0 0 1
X02 0 1 0
A00 0 1 1
VGA STRAP
option GPIO24 GPIO5
UMA 0 0
Madisan 1 1
Park 1 0
M96 1 0
U3701A
NPCE781BA0DX-GP
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
U3701B
KBC
PS/2
FIU
Vendor recommend FW can do it
Vendor recommend can remove
For EMI
84.27002.F3F
84.2N702.D31
X01 20091111
X02-20091222
A00-20100202
A00-20100301
A00-20100203
A00-20100125
X02-20100104
A00-20100204
X02-20100105
x01 change tolerant 20091118
x01 change tolerant 20091117
X01 change location
PH for Discrete
Internal PL for UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC Nuvoton NPCE781BA0DX
Berry
A00
Monday, March 29, 2010
Sheet 37 of 92

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	***Berry***	***A00***

Date: Wednesday, February 10, 2010 Sheet 38 of 92

SSID = Thermal

1. Place near CPU PWM CORE and PCH.

Layout notice :
Both DN1 and DP1 routing 10 mil
trace width and 10 mil spacing.

C3905 must be near Q3901

Q3901 PMBS3904-1-GP

C3904 SC470P50V2JN-GP

C3905 SC470P50V2JN-GP

near EMC2102

2. System Sensor(UMA Only)

Layout notice :
Both DN2 and DP2 routing 10 mil
trace width and 10 mil spacing.

Q3902 PMBS3904-1-GP

C3906 SC470P50V2JN-GP

EMC2102_DN2_UMA

EMC2102_DP2_UMA

R3903 0R2J-2-GP

R3904 0R2J-2-GP

Reserved DISCRETE

82 VGA_THERMDC

R3906 0R2J-2-GP

82 VGA_THERMDA

R3907 0R2J-2-GP

C3907 SC470P50V2JN-GP

3.VGA Sensor(DISCRETE Only)

Layout notice :
Both VGA_THERMDA and VGA_THERMDC routing
10 mil trace width and 10 mil spacing.

C3907 must be near Q3902

Q3903 PMBS3904-1-GP

C3908 SC470P50V2JN-GP

C3909 SC470P50V2JN-GP

C3 must be near EMC2102

4.HW T8 sensor

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

+5V_RUN

x01 change tolerant 20091117

C3902 SC10U6D3V5MX-3GP

C3901 SCD1U10V2KX-5GP

+3.3V_RUN

R3902 49D9R2F-GP

EMC2102_VDD_3D3

C3903 SCD1U10V2KX-5GP

R3901 10KR2J-3-GP

EMC2102_FAN_TACH

EMC2102_FAN_TACH 58

EMC2102_FAN_DRIVE

EMC2102_FAN_DRIVE 58

THERM_SCL 37

THERM_SDA 37

U3901

EMC2102

GND
TACH
VDD_5Va
FANa
FANb
VDD_5Vb
SMCLK
SMDATA

VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3

NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15

NC#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#

EMC2102-DZK-GP

EMC2102_DN1
EMC2102_DP1
EMC2102_DN2
EMC2102_DP2
EMC2102_DN3
EMC2102_DP3

CLK_32K

EMC2102_CLK_SEL

EMC2102_RESET#

TP3901

X02-20091222

R3905 0R0402-PAD

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

RN3901 SRN4K7J-8-GP

THERM_SCL
THERM_SDA

RN3902 SRN10KJ-5-GP

THERM_POWER_OK#
THERMTRIP#

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

R3908 10KR2J-3-GP

EMC2102_SHDN

THERM_POWER_OK#
THERMTRIP#

R3909 10KR2J-3-GP

EMC2102_FAN_mode

A00-20100204

R3911 0R0402-PAD

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

THERM_SYS_SHDN#

Q3904 2N7002E-1-GP

84.2N702.D31

PURE_HW_SHUTDOWN# 37,42

V_DEGREE

Main G7922R61U for GMT P/N:74.07922.0B3
SEC. EMC2102 for SMSC P/N:74.02102.A73

C3910 SCD1U10V2KX-5GP

R3913 10KR2F-2-GP

C3911 SCD1U10V2KX-5GP

R3914 2K37R2F-GP

TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)

x01 change tolerant 20091117

T8 shutdown is set 88 deg-C.

22 PCH_SUSCLK_2102

32K suspend clock output

Q3905 2N7002E-1-GP

84.2N702.D31

42 RUN_ENABLE

CLK_32K_R

R3915 10R2J-2-GP

CLK_32K

C3913 SC4D7P50V2CN-1GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: Berry | Rev: A00

Date: Tuesday, April 06, 2010 | Sheet 39 of 92

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 40 of 92

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<Core Design>

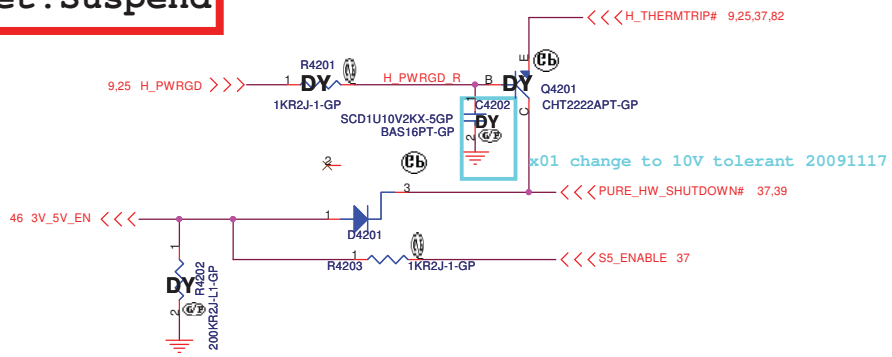
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

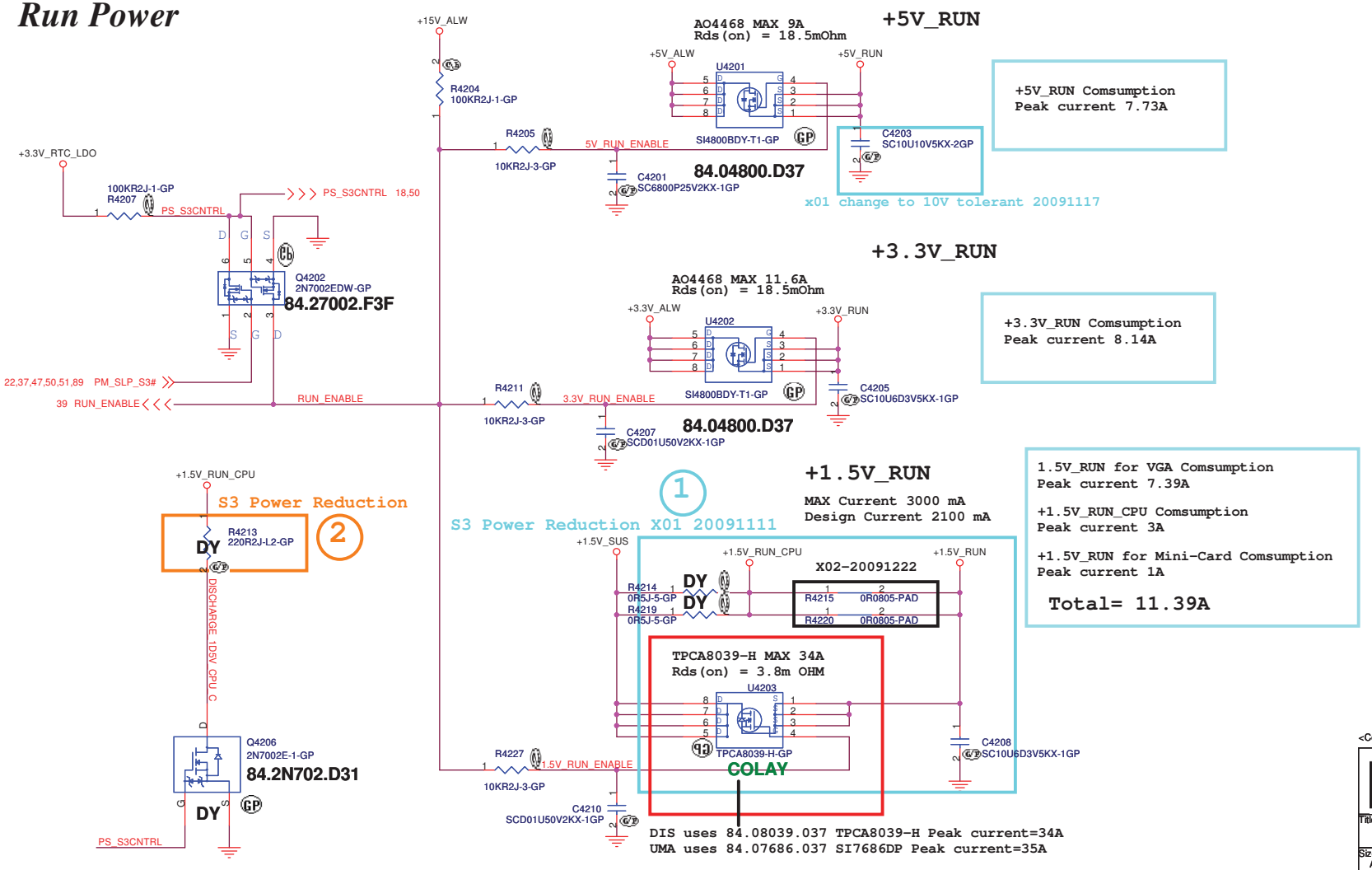
Size	Document Number	Rev
A3	*Berry*	*A00*

Date: Wednesday, February 10, 2010 Sheet 41 of 92

SSID = Reset.Suspend



Run Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	Berry	A00

Date: Monday, March 29, 2010 Sheet 42 of 92

(Blanking)

<Core Design>

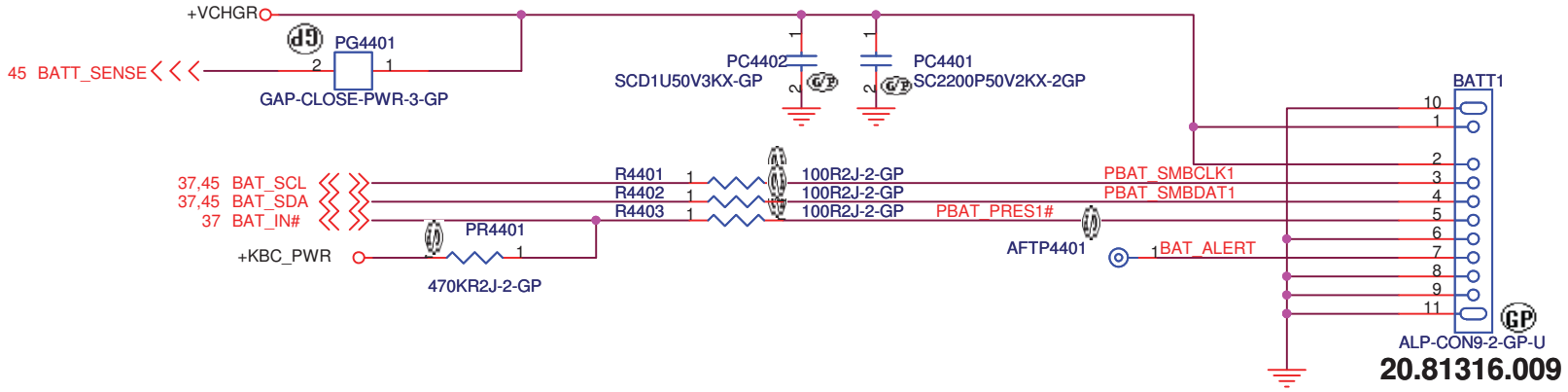
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

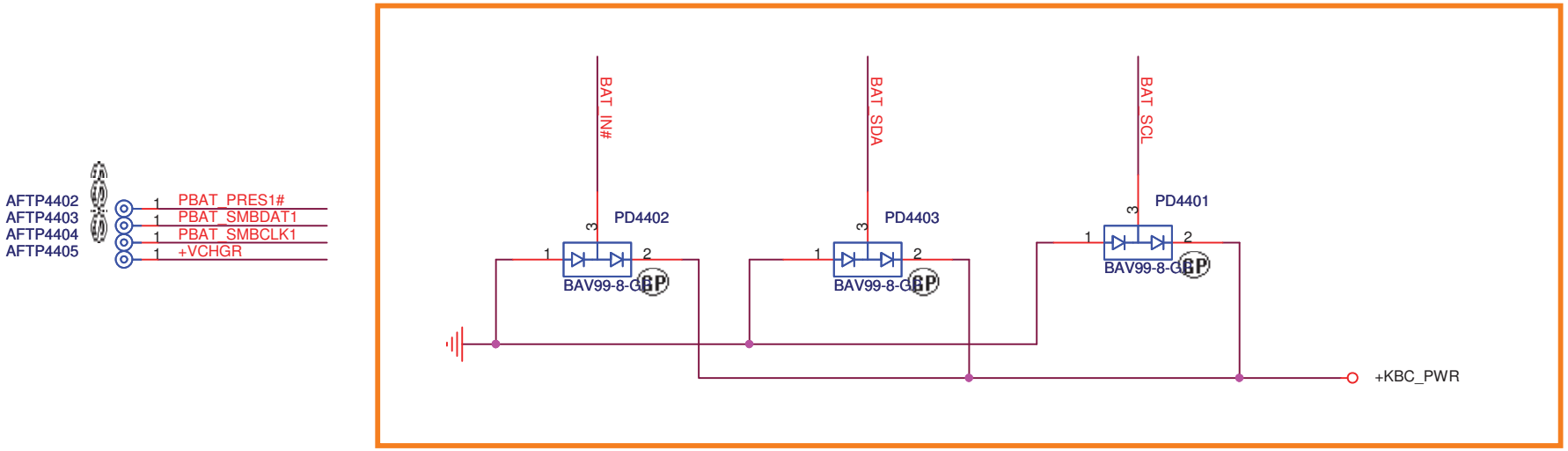
Date: Wednesday, February 10, 2010 | Sheet 43 of 92

Batt Connecter



For actual location, need to be swap all pin

Close to Batt Connector



<Core Design>

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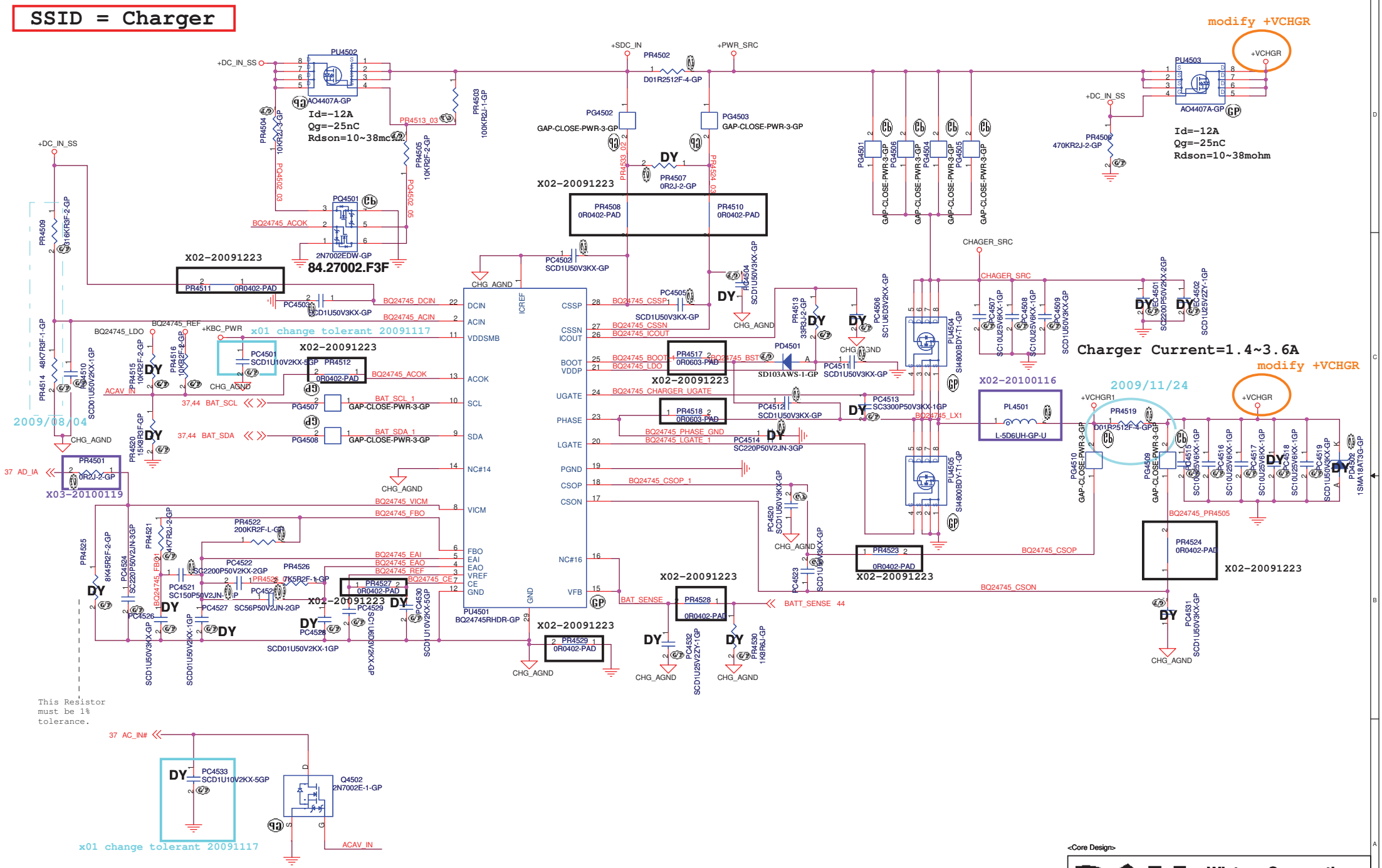
Title: **BATT CONN**

Size	Document Number	Rev
A4	Berry	A00

Date: Monday, March 29, 2010 Sheet 44 of 92

SSID = Charger



<Core Design>

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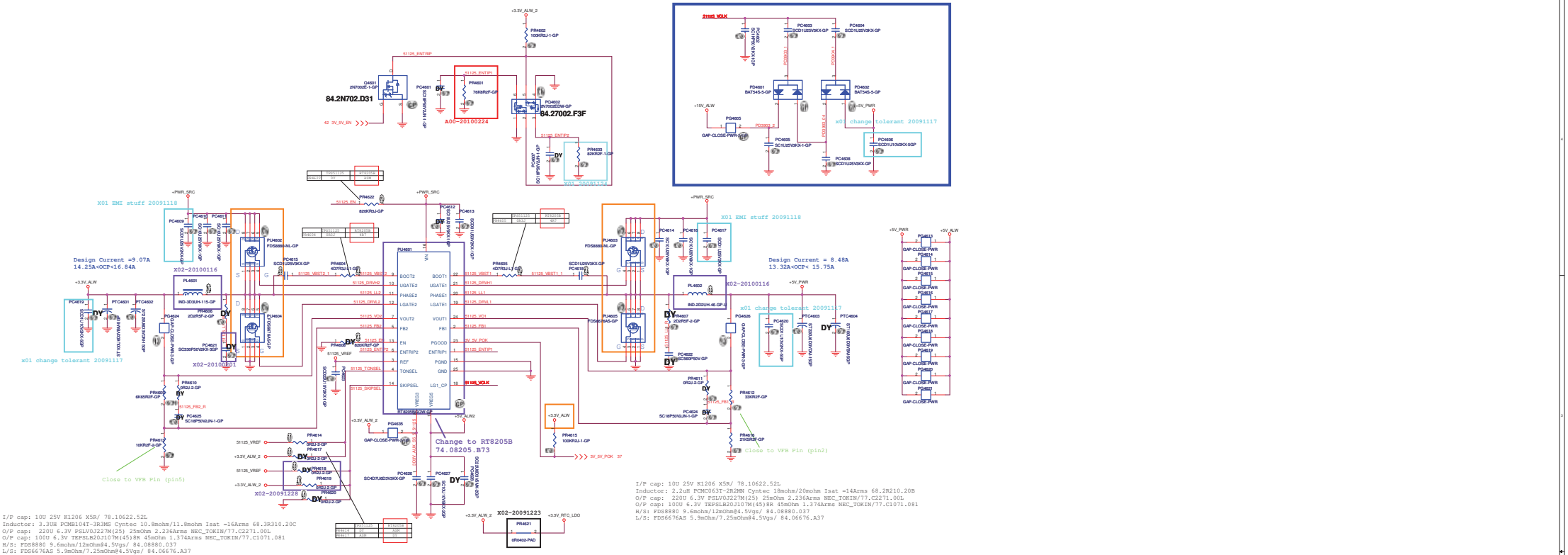
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size	Document Number	Rev
Custom	Berry	A00

Date: Monday, March 29, 2010 Sheet 45 of 92



TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

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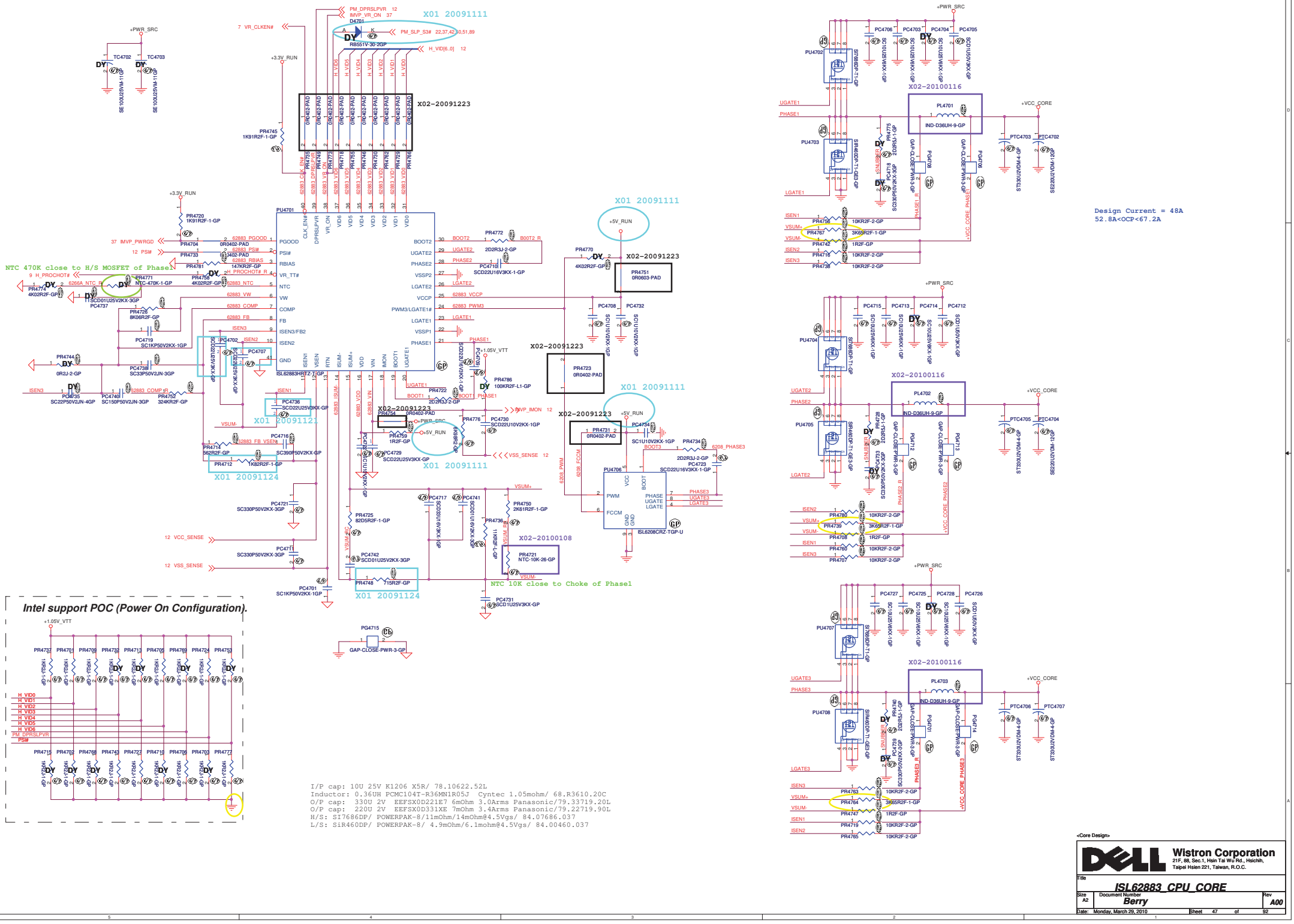
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205B_5V/3D3V

Size	Document Number	Rev
A1	Berry	A00

Date: Monday, March 08, 2010 Sheet 46 of 50


ISL62883_CPU_CORE
Design Current = 48A
52.8A<OCP<67.2A
NTC 470K close to H/S MOSFET of Phase1
NTC 10K close to Choke of Phase1
Intel support POC (Power On Configuration).
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J Cyntec 1.05mohm/ 68.R3610.20C
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
H/S: SiZ786DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62883_CPU_CORE
Size A2
Document Number Berry
Rev A00
Date: Monday, March 29, 2010
Sheet 47 of 92

(Blanking)

<Core Design>

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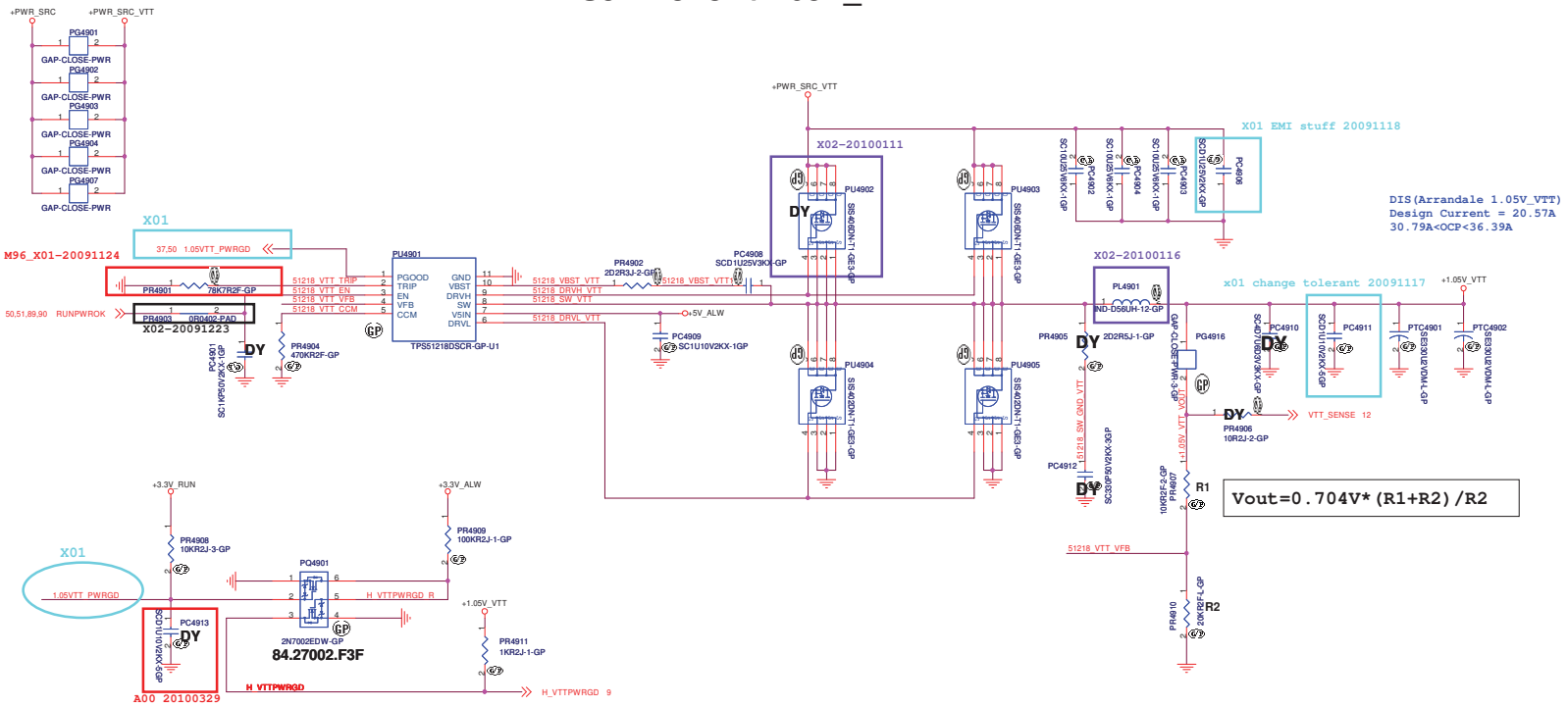
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 48 of 92

TPS51218 for +1.05V_VTT



Frequency setting
470K --->290KHz
200K --->340KHz
100K --->380KHz
39K --->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218 +1.05V VTT

Size: A2 | Document Number: Berry | Rev: A00

Date: Tuesday, April 06, 2010 | Sheet 49 of 92

SSID = PWR.Plane.Regulator_1p5v0p75v

Modified net name

+PWR_SRC_1D5V

x01-20091124

PR5001 5D1R3J-GP

PR5002 14K7R2F-L-GP

PC5002 SC1KP50V2KX-1GP

PC5003 SC1U10V2KX-1GP

PC5001 SC1U10V2KX-1GP

PR5004 20KR2F-L-GP

PR5006 620KR2F-GP

PR5005 0R3J-0-U-GP

PD5001 RB551V-30-2GP

PU5001 TPS51116RGER-GP-U

PR5008 1M1R2J-GP

PR5009 0R0402-PAD

PC5007 SC1KP50V2KX-1GP

PC5005 SC1U6D3V2KX-GP

PR5010 0R2J-2-GP

PC5008 SC1U10V2KX-1GP

PR5011 0R0603-PAD

PC5010 SCD033U16V3KX-GP

x01 change tolerant 20091117

RT: ASM
TI: Non_ASM

5 S3 Power Reduction X01 20091111

PQ5003 2N7002E-1-GP 84.2N702.D31

PR5016 100KR2J-1-GP

PQ5002 2N7002E-1-GP 84.2N702.D31

PQ5001 PMBS3904-1-GP

PR5017 4K7R2J-2-GP

PC5024 SCD1U10V2KX-5GP

PR5018 10KR2J-3-GP

PR5015 0R2J-2-GP

X02-20091224

PR5019 0R0402-PAD

PR5003 0R2J-2-GP

PC5004 SCD1U10V2KX-5GP

x01 change tolerant 20091118

X02-20091223

PR5007 0R0402-PAD

PC5006 SCD1U10V2KX-5GP

PG5002 PG5003 PG5004 PG5006 GAP-CLOSE-PWR

Design Current = 14.45A
22.71A<OCP< 26.84A

PU5002 SI7686DP-T1-GP

PU5003 SIR460DP-T1-GE3-GP

PU5004 SIR460DP-T1-GE3-GP

PC5009 SC10U25V6KX-1GP

PC5011 SC10U25V6KX-1GP

PC5012 SC10U25V6KX-1GP

PC5013 SCD1U25V2KX-GP

PC5014 SC4D7U25V6KX-GP

X02-20100116

PL5001 IND-1D5UH-34-GP

PR5012 2D2R5F-2-GP

PC5022 SC330P50V2KX-3GP

X02-20100201

PC5019 SCD1U25V3KX-GP

PC5020 SC4D7U6D3V3KX-GP

PC5021 SCD1U10V2KX-5GP

PTC5002 PTC5001 SE330U2VDM-1-GP

PG5017 GAP-CLOSE-PWR3-GP

PR5013 30KR2F-GP

PR5014 30KR2F-GP

PC5023 SC18P50V2JN-1-GP

Close to VFB Pin (pin5)

x01 change to 330uF 20091124

x01 change tolerant 20091117

PC5015 PC5016 PC5017 PC5018 SC10U6D3V5MX-3GP

PG5001 PG5016 GAP-CLOSE-PWR

Design Current = 0.7A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

<Core Design>

Wistron Corporation
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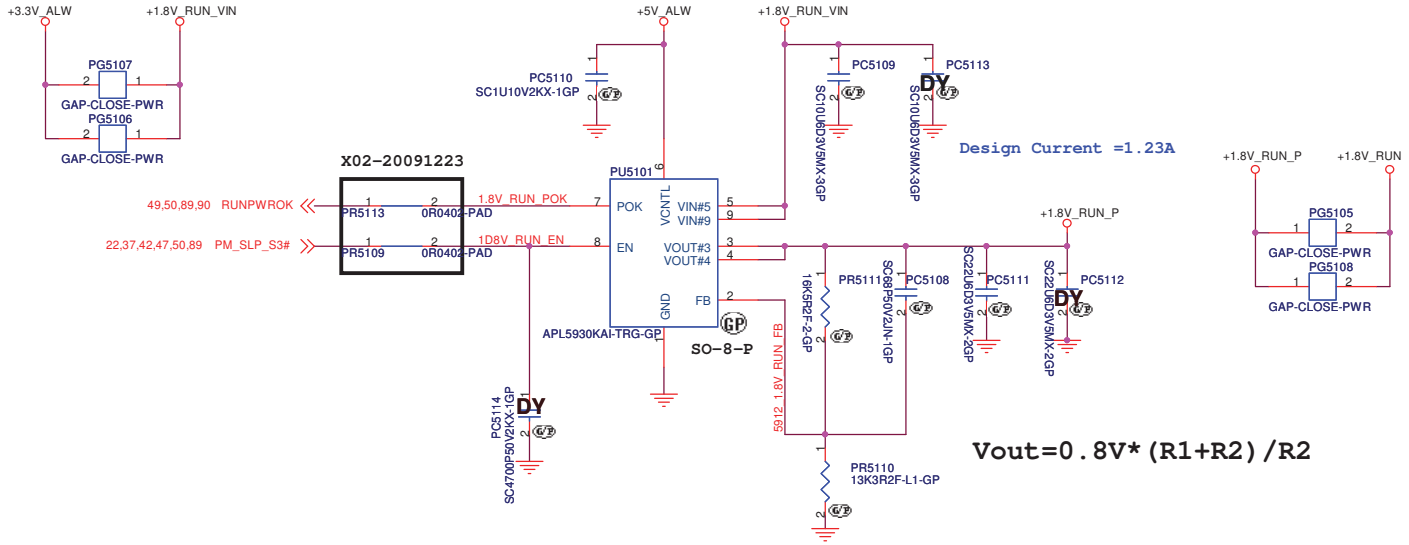
Title: TPS51116_+1.5V_SUS

Size: Custom | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 50 of 92

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	APL5930_+1.8V_RUN	
Size A3	Document Number Berry	Rev A00
Date: Monday, March 29, 2010	Sheet 51 of 92	

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<Core Design>

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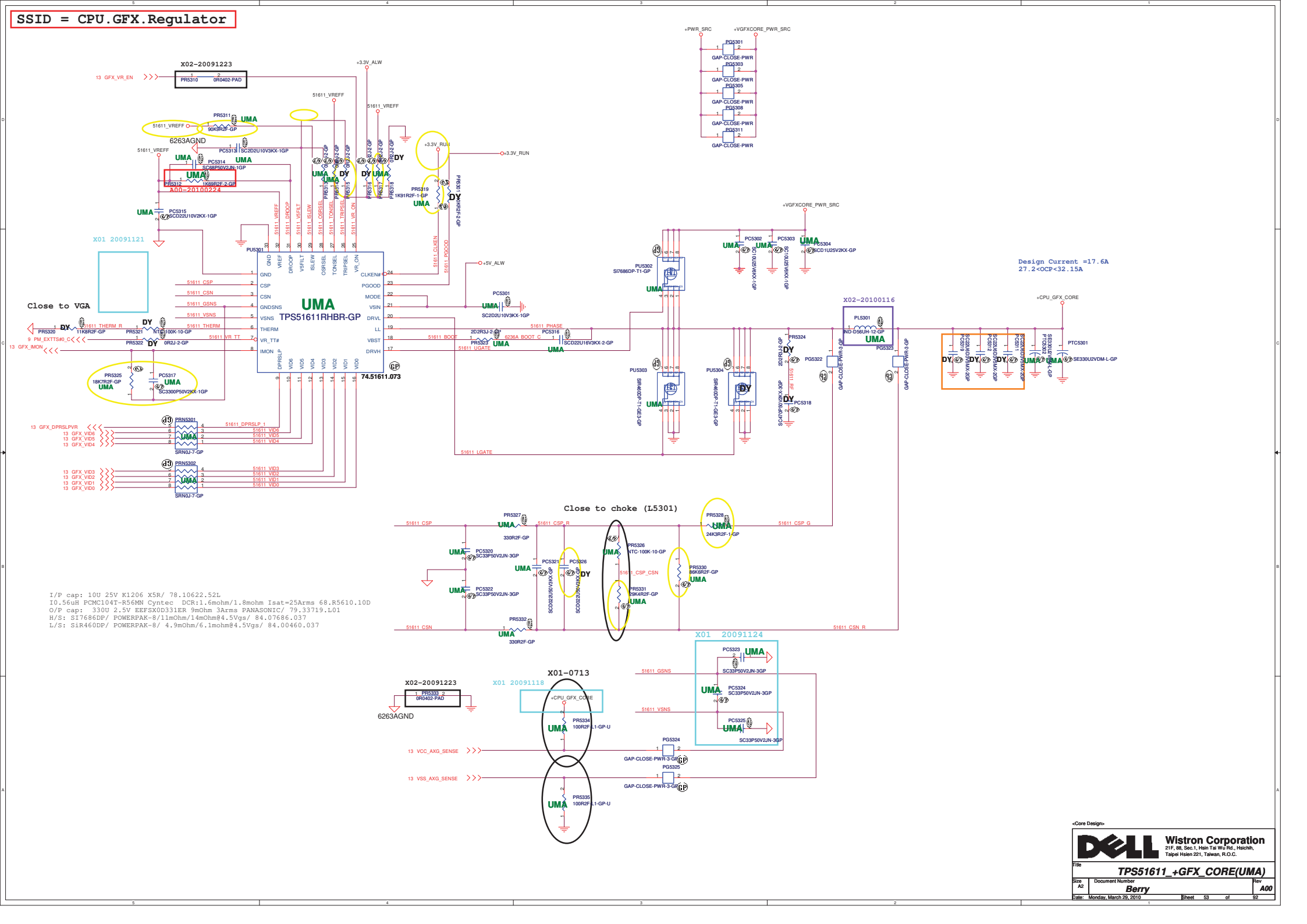
Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

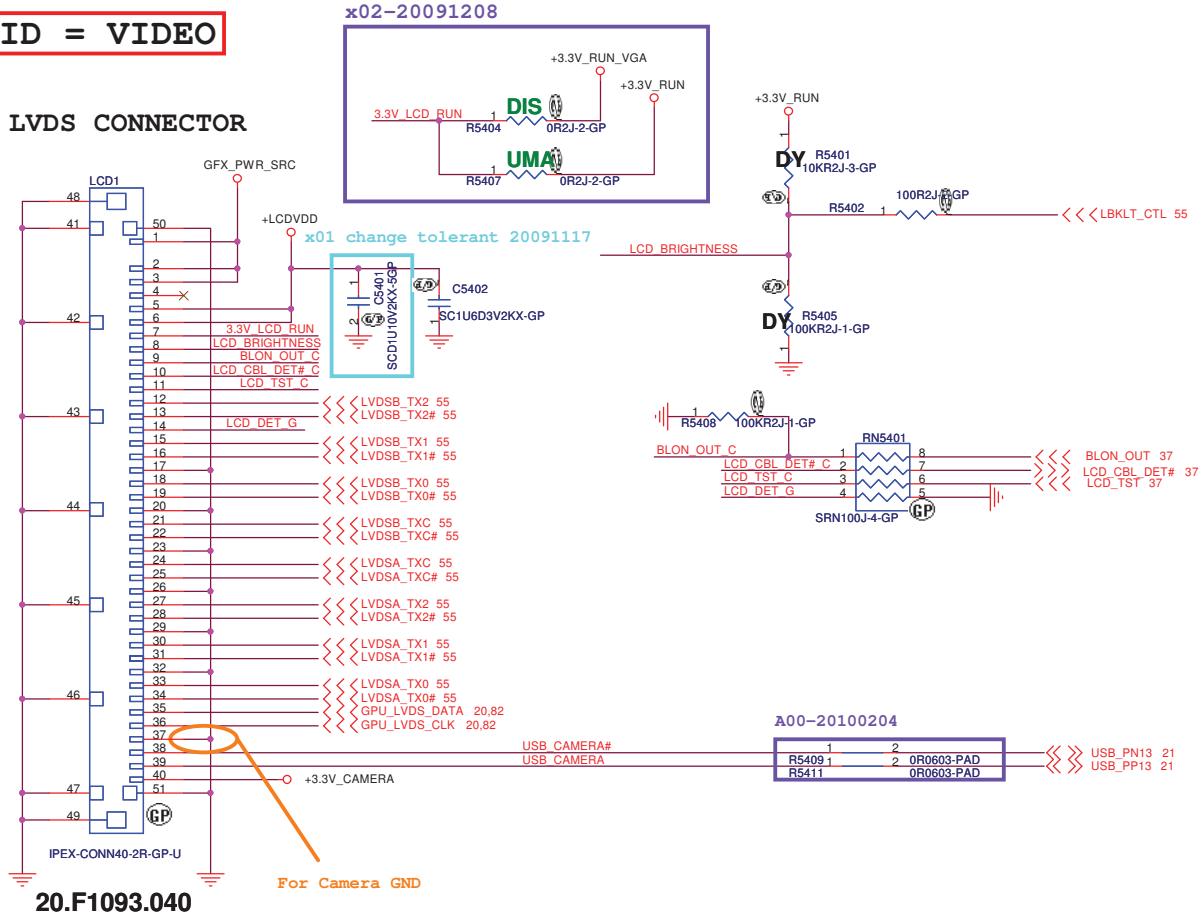
Date: Wednesday, February 10, 2010 | Sheet 52 of 92

SSID = CPU.GFX.Regulator



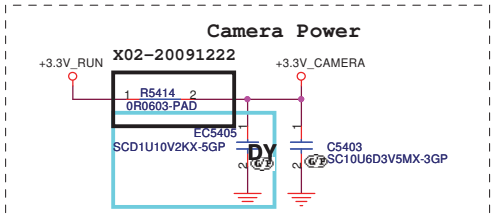
SSID = VIDEO

LVDS CONNECTOR



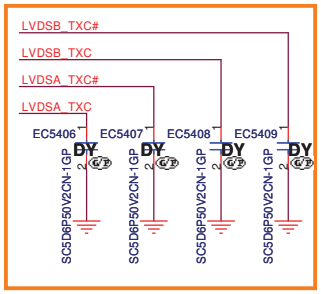
20.F1093.040

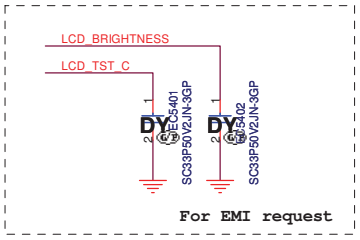
Camera Power



x01 change tolerant 20091117

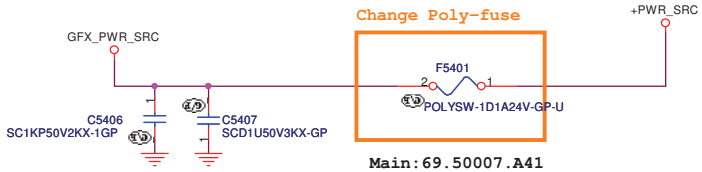
Close to LVDS connector





SSID = Inverter

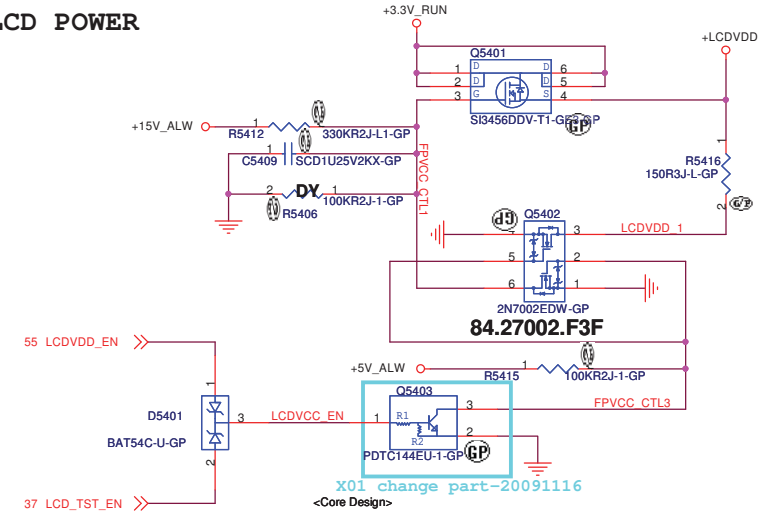
INVERTER POWER



Main:69.50007.A41
Second:69.50007.A31

SSID = VIDEO

LCD POWER



<Core Design>

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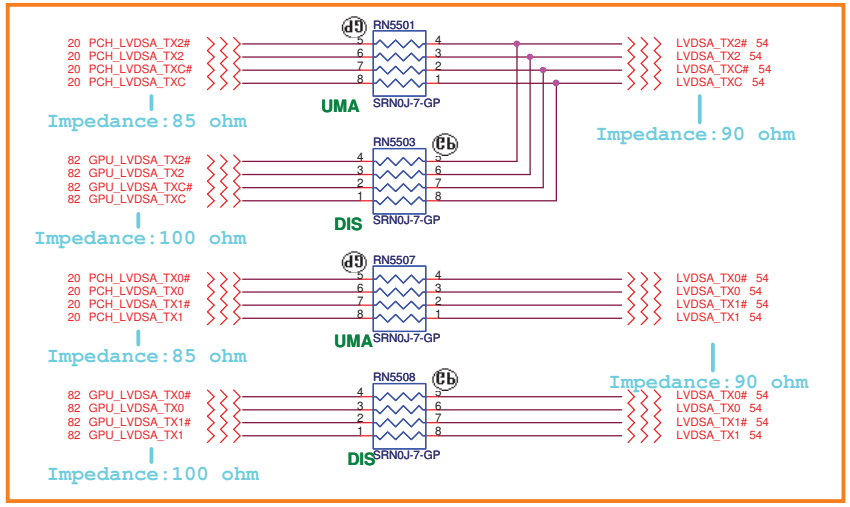
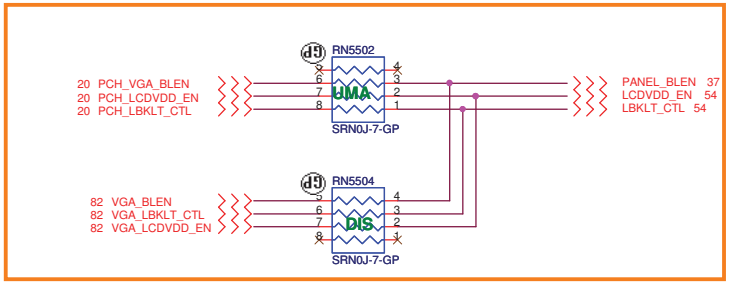
Title	LCD/Inverter Connector	
Size A3	Document Number Berry	Rev A00
Date: Monday, March 29, 2010	Sheet 54 of 92	

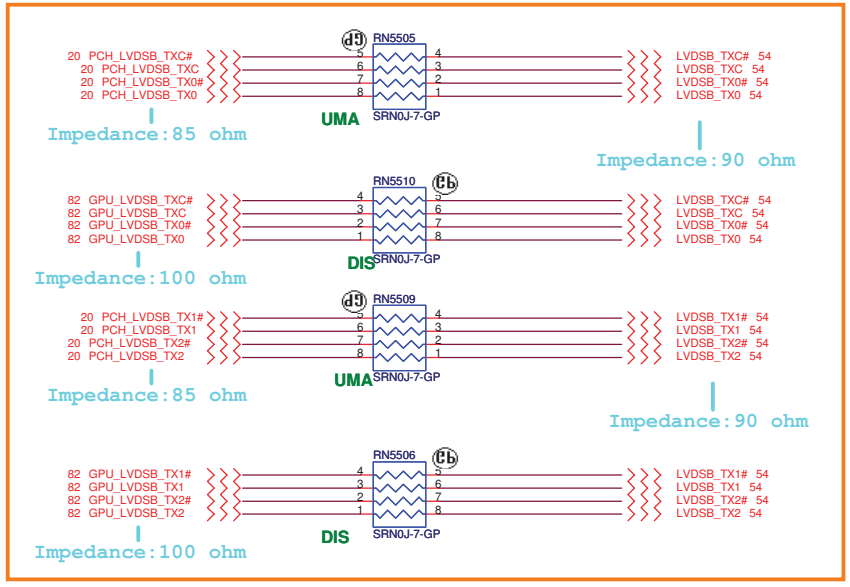
LVDS Channel A



Panel BL brightness/Power En/BL En



LVDS Channel B



<Core Design>

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Title	LVDS_Switch	
Size	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet 55 of 92	

(Blanking)

<Core Design>

Wistron Corporation
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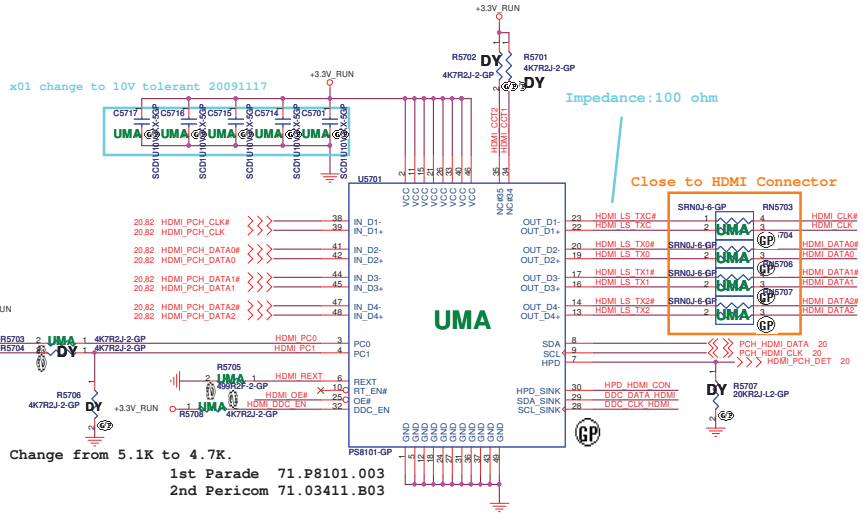
Taipei Hsien 221, Taiwan, R.O.C.

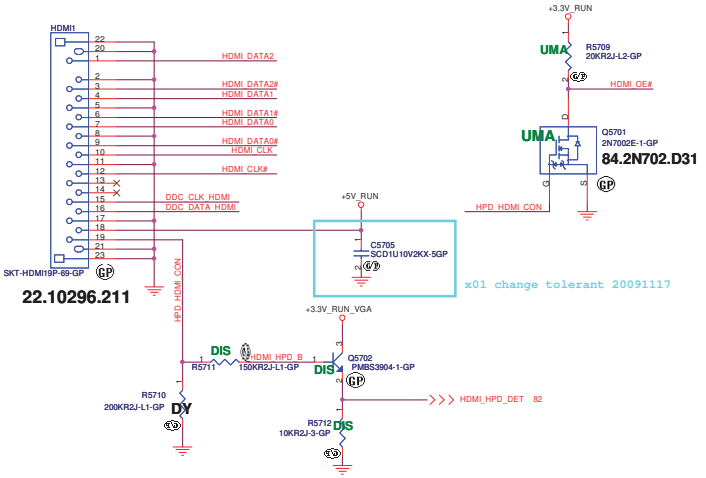
Title	LVDS_Switch	
Size: A3	Document Number: Berry	Rev: A00
Date: Wednesday, February 10, 2010	Sheet 56 of 92	

SSID = VIDEO

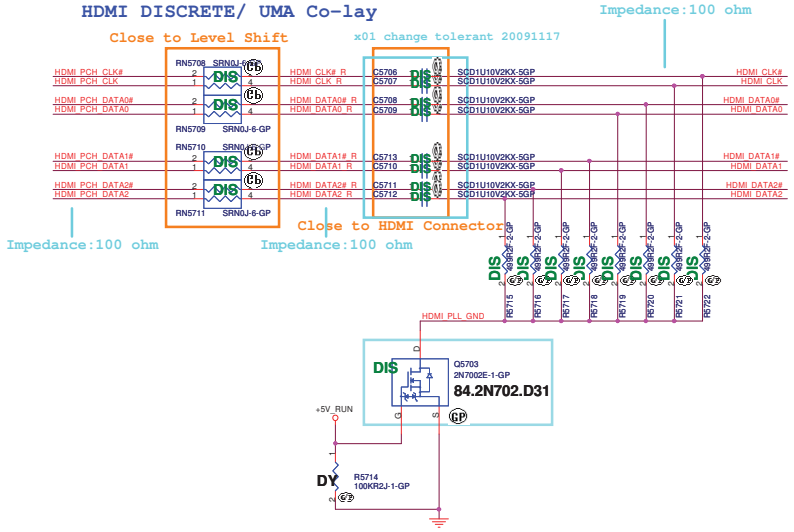
HDMI Level Shifter & CONNECTOR

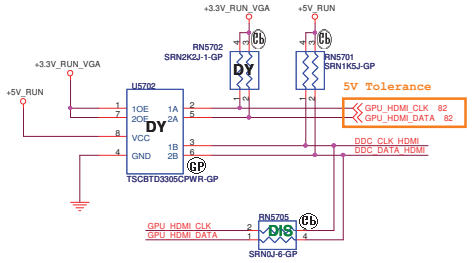


HDMI CONN



HDMI DISCRETE/ UMA Co-lay





<Core Design>
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

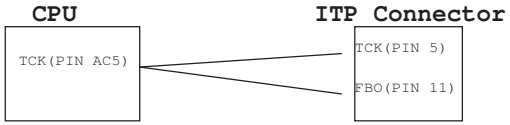
Size: A2 | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 57 of 92

SSID = User.Interface

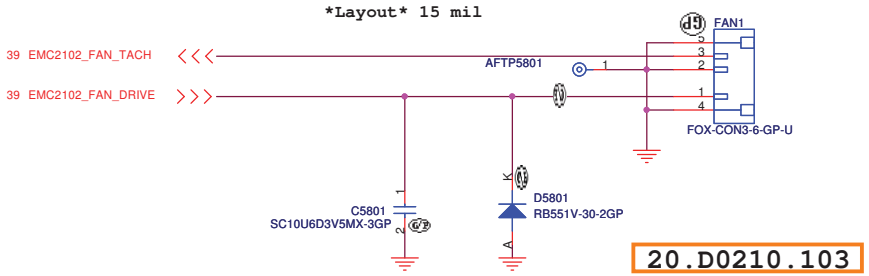
ITP Connector

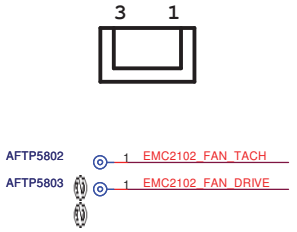
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



SSID = Thermal

Fan Connector





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

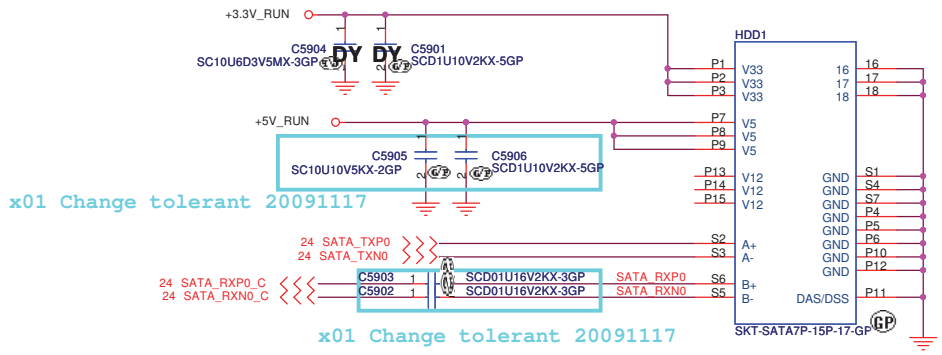
Title: ITP/Fan Connector

Size	Document Number	Rev
A3	Berry	A00

Date: Monday, March 29, 2010 Sheet 58 of 92

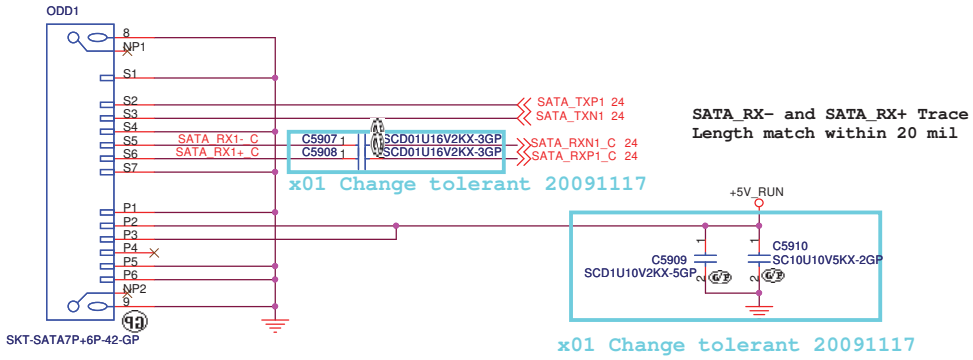
SSID = SATA

SATA HDD Connector



62.10065.C71

ODD Connector



SATA_RX- and SATA_RX+ Trace Length match within 20 mil

62.10065.581

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

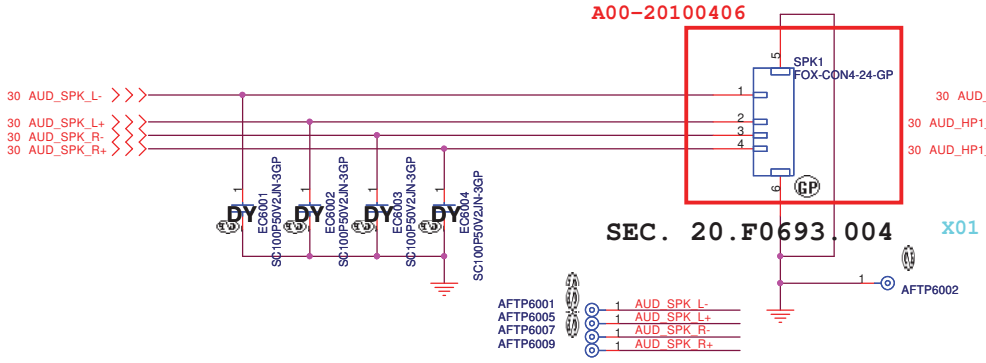
Title: HDD/ODD

Size	Document Number	Rev
A3	Berry	A00

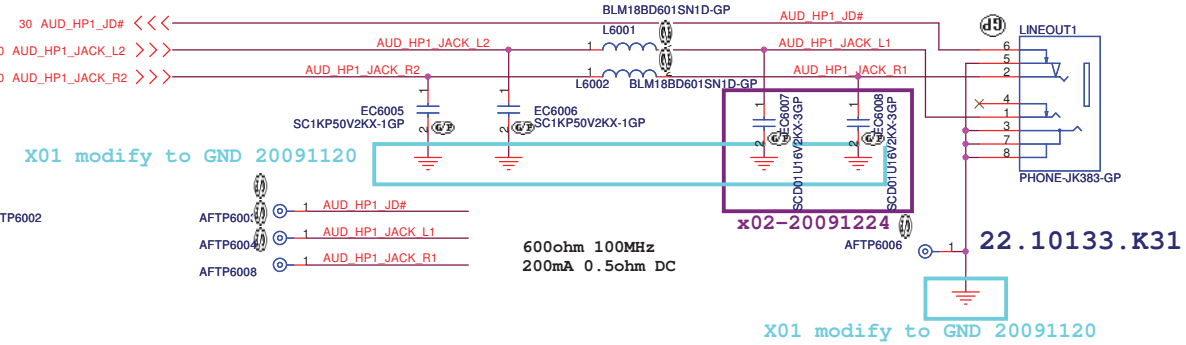
Date: Monday, March 29, 2010 Sheet 59 of 92

SSID = AUDIO

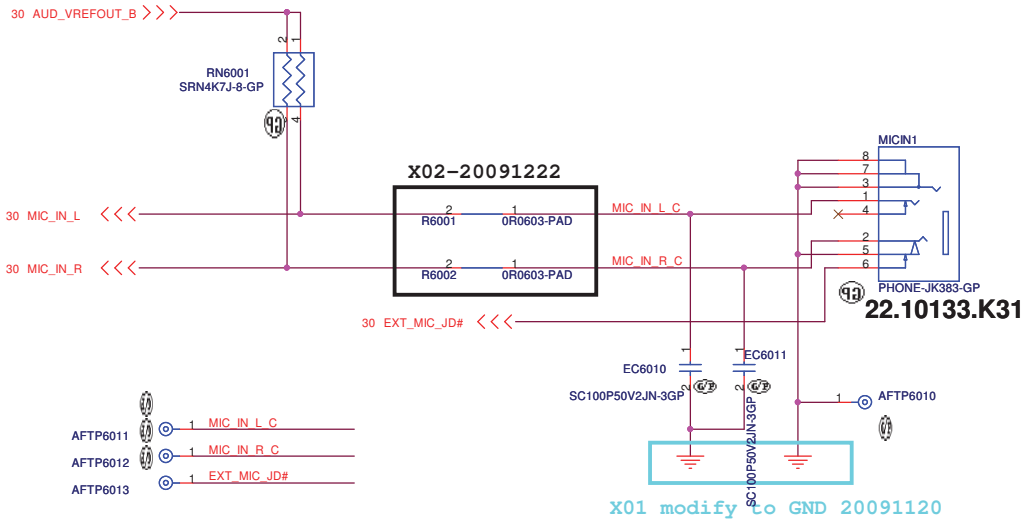
Speaker Connector



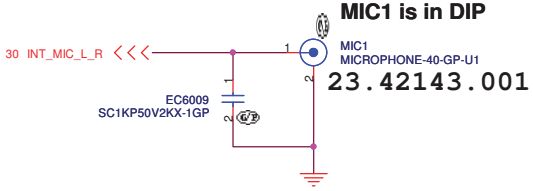
LINE1 OUT

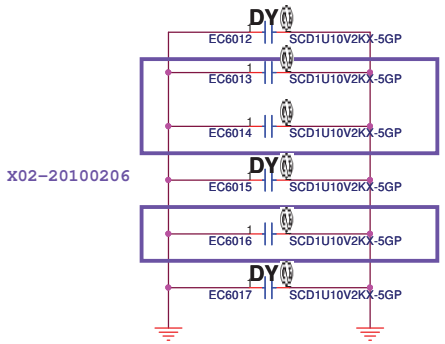


MIC IN



Internal Microphone





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size	Document Number	Rev
A3	Berry	A00

Date: Monday, April 26, 2010 Sheet 60 of 92

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

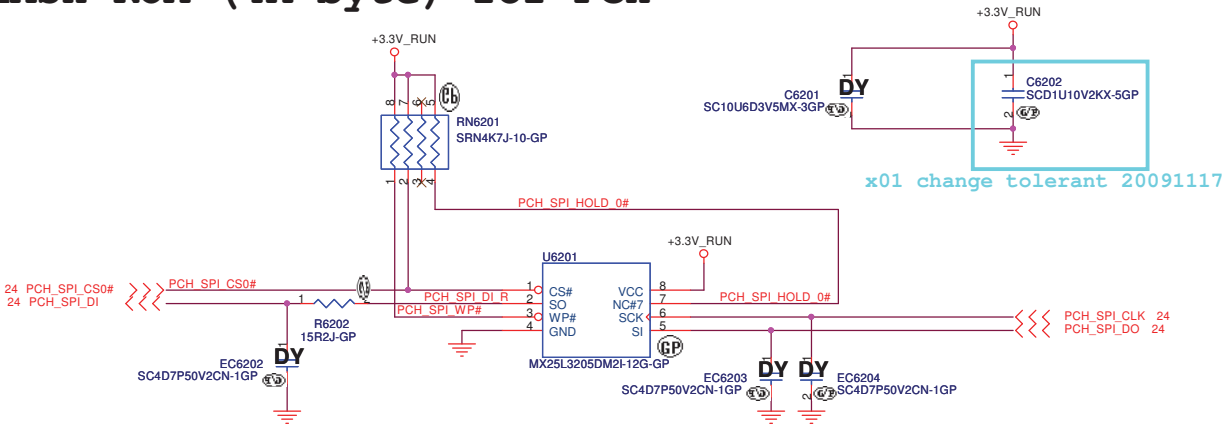
Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

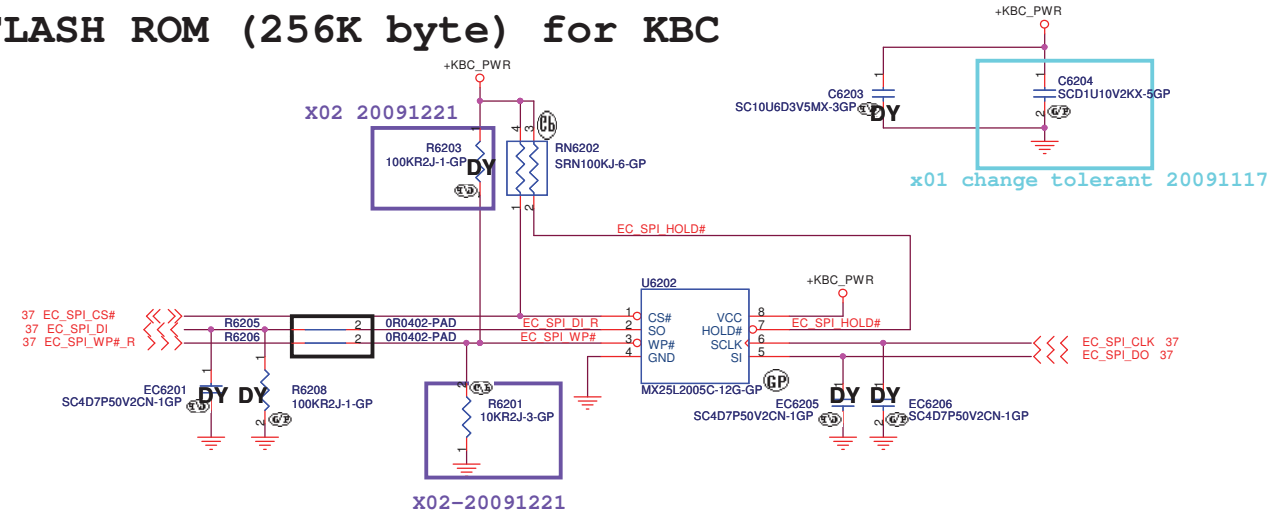
Date: Wednesday, February 10, 2010 | Sheet 61 of 92

SSID = Flash.ROM

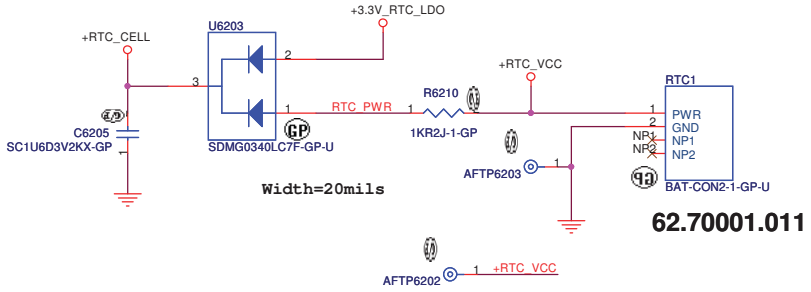
SPI FLASH ROM (4M byte) for PCH



SPI FLASH ROM (256K byte) for KBC



SSID = RBATT



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

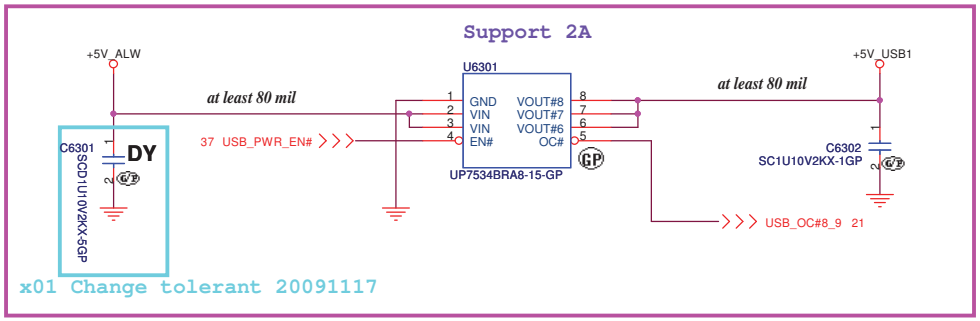
Size	Document Number	Rev
A3	Berry	A00

Date: Monday, March 29, 2010 Sheet 62 of 92

SSID = USB

IO Board USB Power

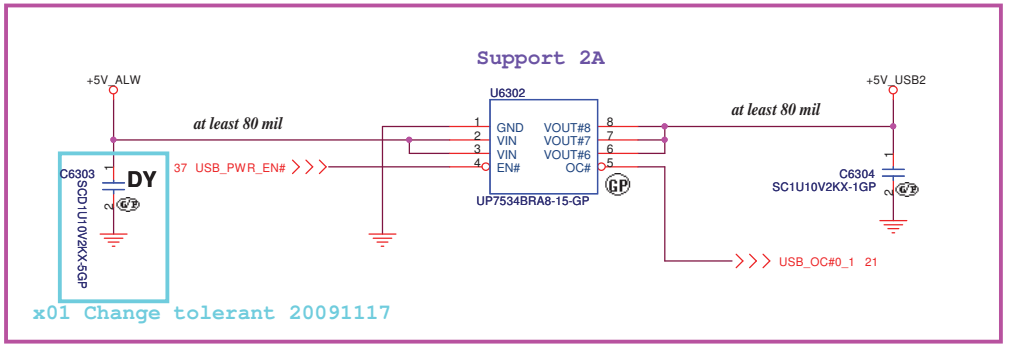
Close to I/O connector



USB POWER SW
Main UP7534BRA8-15 P/N:74.07534.079
SEC AP2101MPG-13 P/N: 74.02101.079

CRT Board USB Power

Close to CRT Board connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB Power SW	
Size	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet 63 of 92	

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

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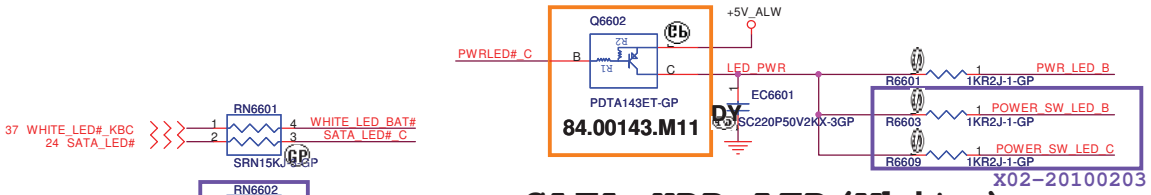
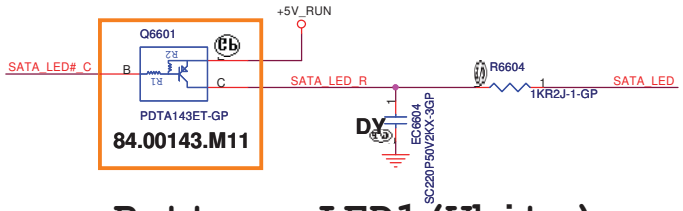
SSID = User.Interface

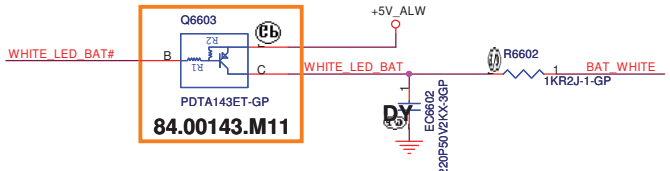
Power LED(White)

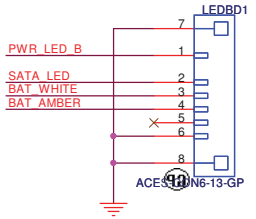


SATA HDD LED(White)

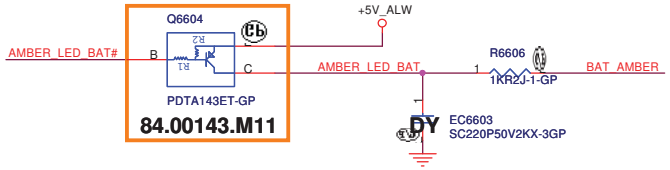


Battery LED1(White)

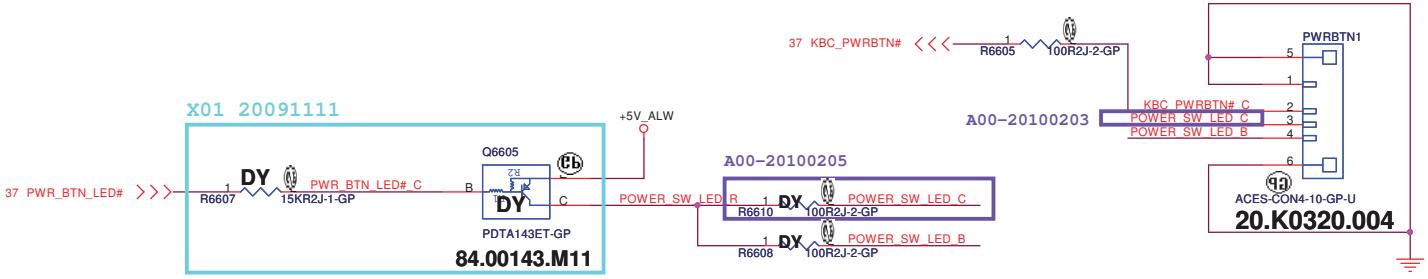




Battery LED2(Amber)



Power button LED(White)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED Bard/Power Button	
Size A3	Document Number Berry	Rev A00
Date: Monday, March 29, 2010	Sheet 66 of 92	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

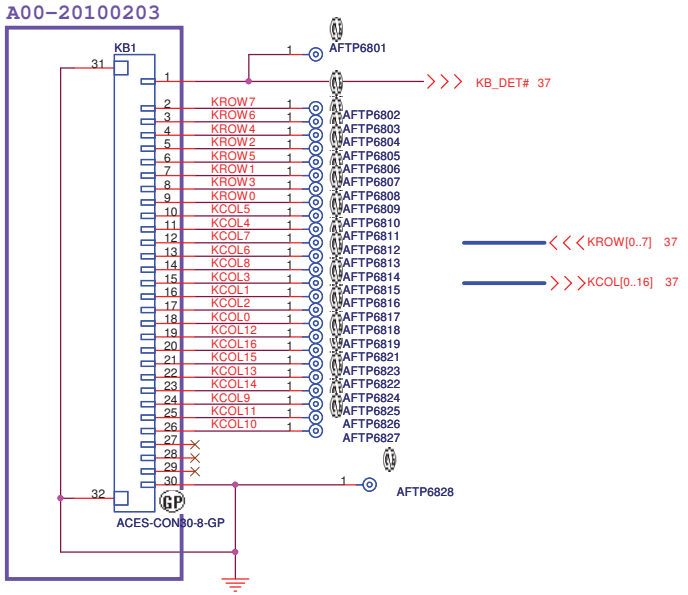
Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 67 of 92

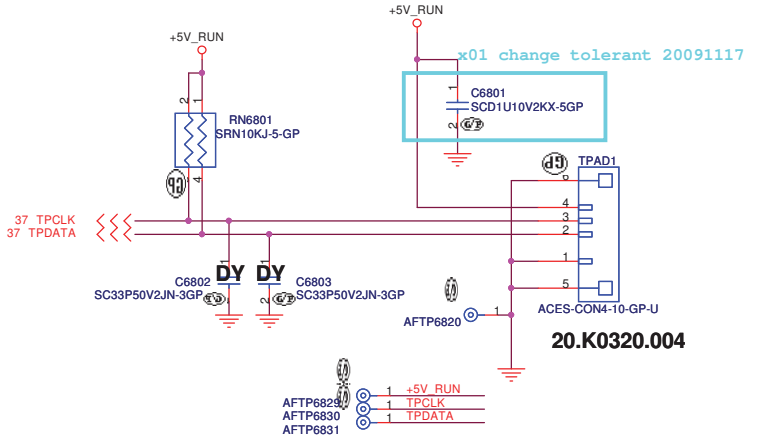
SSID = KBC

Internal KeyBoard Connector

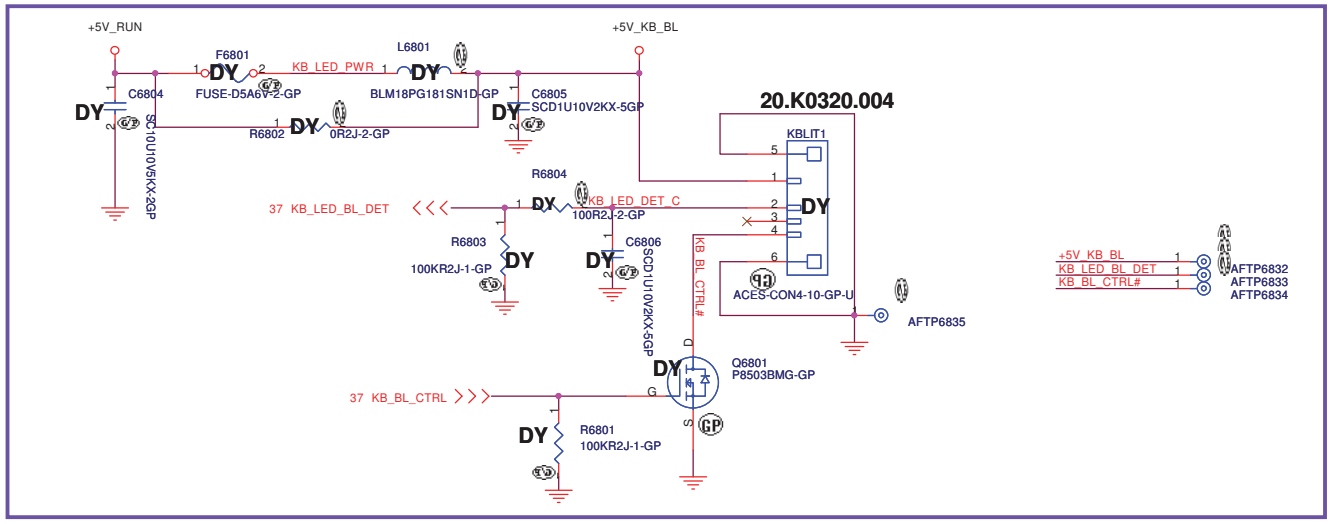


SSID = Touch.Pad

TouchPad Connector



KB Backlight Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size: A3 | Document Number: Berry | Rev: A00

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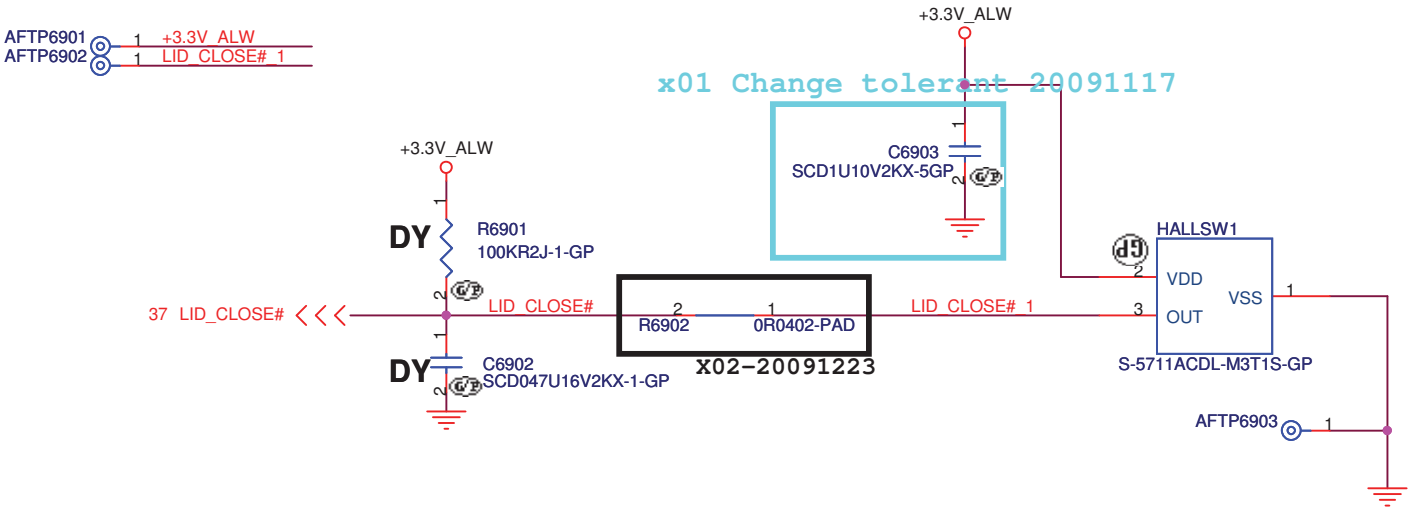

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	***Berry***	***A00***

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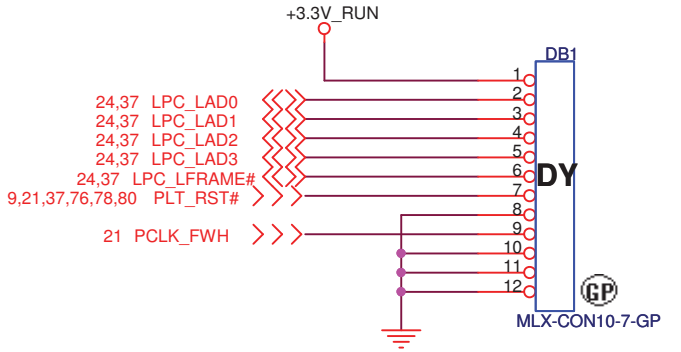

20.D0183.110

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	***Berry***	***A00***

Date: Monday, March 29, 2010 Sheet 70 of 92

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

RESERVED

Size	Document Number	Rev
A4	***Berry***	***A00***

Date: Wednesday, February 10, 2010 Sheet 71 of 92

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<Core Design>

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Title

RESERVED

Size	Document Number	Rev
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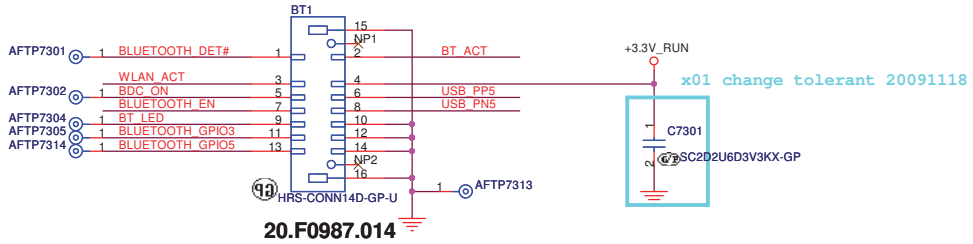
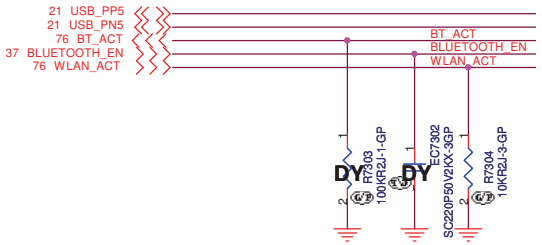
Date: Wednesday, February 10, 2010 Sheet 72 of 92

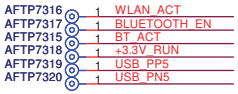
SSID = User.Interface

Bluetooth Module conn.



20.F0987.014





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth		
Size: A3	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet 73 of 92	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 74 of 92

(Blanking)

<Core Design>

Wistron Corporation
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Title

Reserved

Size	Document Number	Rev
A4	***Berry***	***A00***

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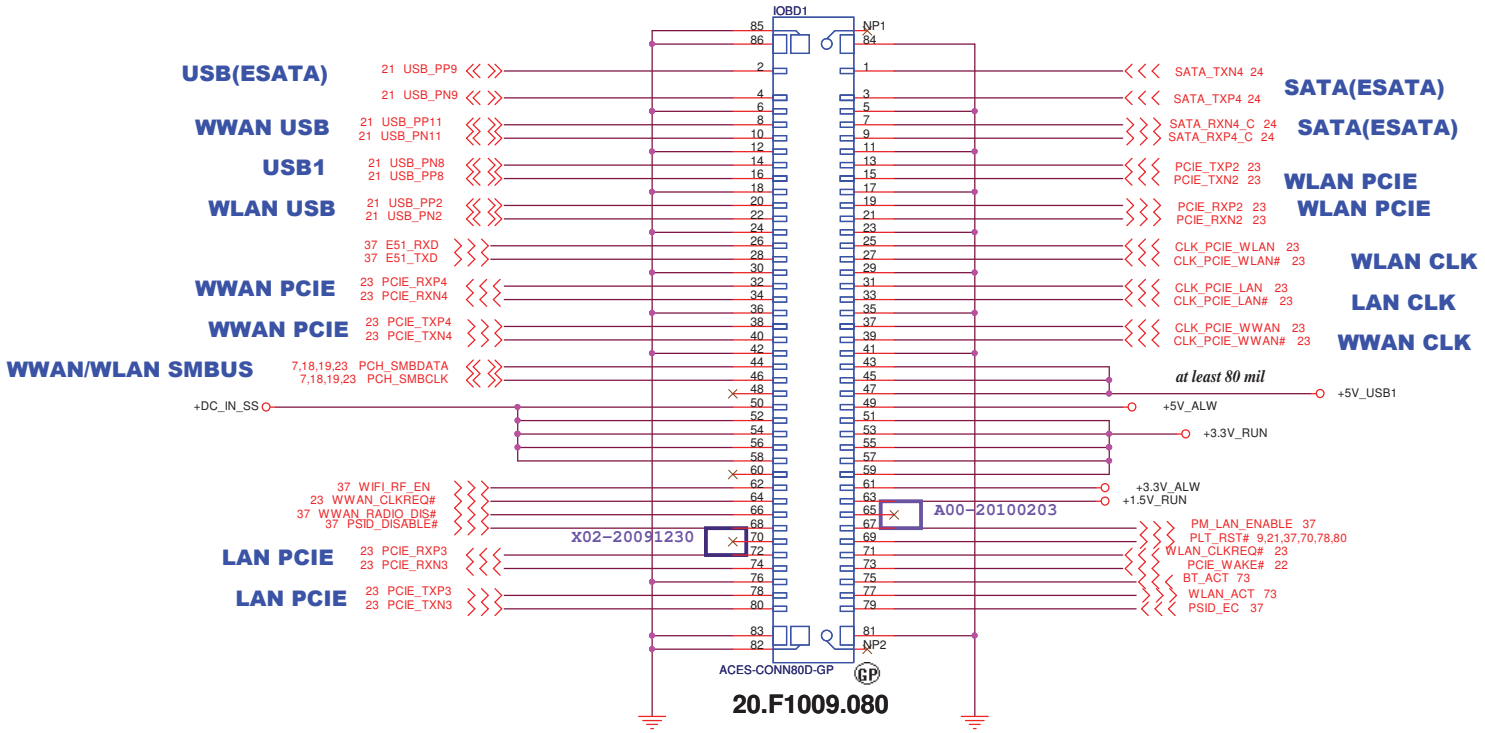
IO Board CONN 80 pin



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	IO Board Connector	
Size: A3	Document Number: Berry	Rev: A00
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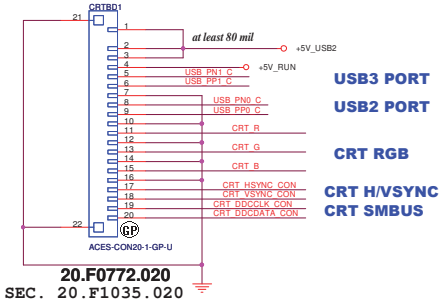
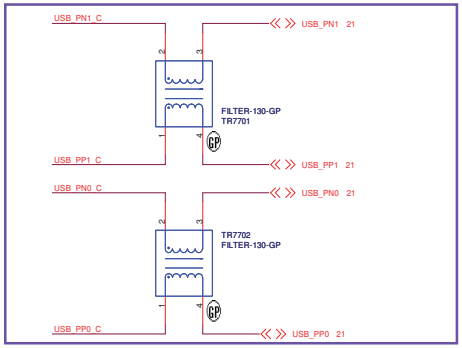
CRT Board Connector



20.F0772.020

SEC. 20.F1035.020

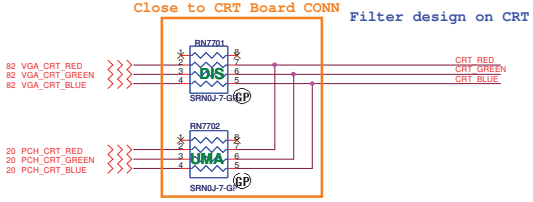
A00-20100120



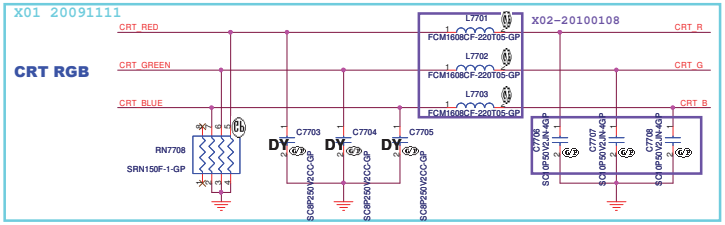
CRT RGB

Close to CRT Board CONN

Filter design on CRT Board

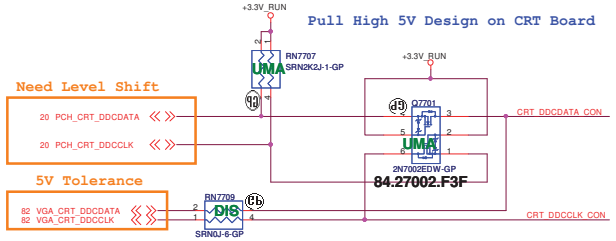


X01 20091111



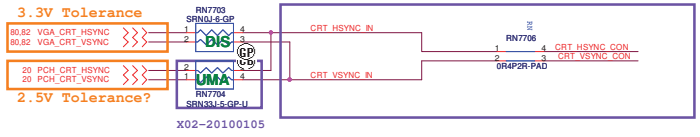
CRT DDCDATA & DDCCLK level shift

Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift

Close to CRT Board CONN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Board Connector

Size: A2 | Document Number: Berry | Rev: A00

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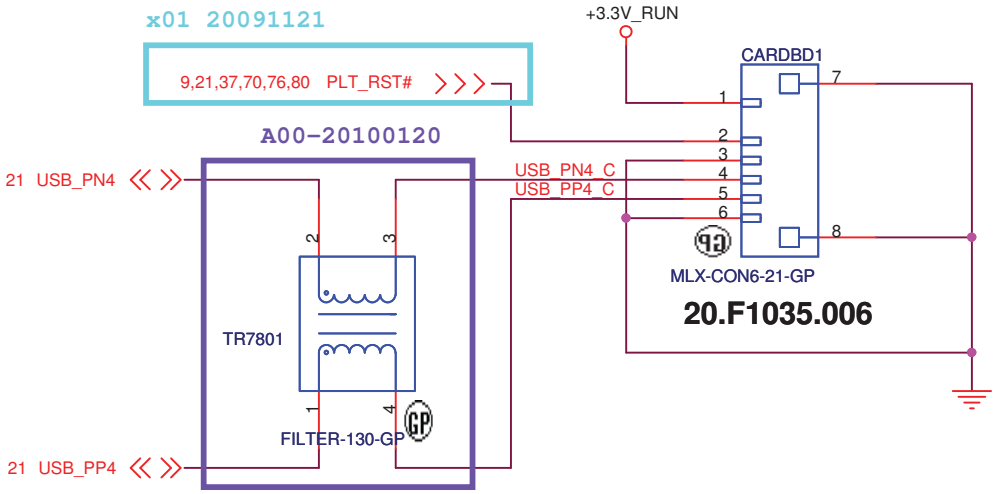
SSID = SDIO

Card Reader connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN		
Size: A4	Document Number: Berry	Rev: A00
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H1
HTE95BE95R29-R-5-GP

H2
HTE95BE95R29-R-5-GP

H3
HTE95BE95R29-R-5-GP

H4
HTE95BE95R29-R-5-GP

H5
HOLE256R111-GP

H6
HTE95BE95R29-R-5-GP

H7
HTE95BE95R29-R-5-GP

H8
HTE95BE95R29-R-5-GP

H9
HTE95BE95R29-R-5-GP

H10
HOLE335R115-GP

H11
HOLE256R111-GP

CPU Thermal module hole

HTML1
HOLE197R166-GP
DY

HTML2
HOLE197R166-GP
DY

HTML3
HOLE197R166-GP
DY

GPU Thermal module hole

HGPU1
STF237R117H83-1-GP

stand off

HBT1
STF237R117H123-GP

EMI Reserve

+PWR_SRC

X01 stuff 20091119

EC7901 SCD1U25V2KX-GP
EC7902 SCD1U25V2KX-GP
EC7904 SCD1U25V2KX-GP
EC7903 SCD1U25V2KX-GP
EC7905 SCD1U25V2KX-GP
EC7907 SCD1U25V2KX-GP
EC7909 SCD1U25V2KX-GP

DY EC7942 SCD1U25V2KX-GP
DY EC7940 SCD1U25V2KX-GP
DY EC7941 SCD1U25V2KX-GP
DY EC7939 SCD1U25V2KX-GP
DY EC7943 SCD1U25V2KX-GP
DY EC7938 SCD1U25V2KX-GP

+VGFXCORE_PWR_SRC

DY EC7906 SCD1U25V2KX-GP

+PWR_SRC_VTT

EC7911 SCD1U25V2KX-GP

X01 stuff 20091118

+PWR_SRC_1D5V

DY EC7916 SCD1U25V2KX-GP

EMI Reserve

SPR1
SPRING-58-GP
DY

X01 RF Reserved-20091118

+PWR_SRC_1D5V
56pF*1
EC7908 SC56P50V2JN-2GP

+PWR_SRC
56pF*7
EC7912 SC56P50V2JN-2GP
EC7913 SC56P50V2JN-2GP
EC7917 SC56P50V2JN-2GP
EC7919 SC56P50V2JN-2GP
EC7920 SC56P50V2JN-2GP
EC7922 SC56P50V2JN-2GP
EC7925 SC56P50V2JN-2GP

+PWR_SRC
+1.5V_SUS
0.1uF*2
EC7921 SCD1U25V2KX-GP
EC7933 SCD1U25V2KX-GP

X02-20100208

+1.05V_VTT
DY EC7923 SCD1U25V2KX-GP
UMA EC7924 SCD1U25V2KX-GP
UMA EC7926 SCD1U25V2KX-GP
UMA EC7927 SCD1U25V2KX-GP

+1.5V_SUS
DY EC7945 SCD1U25V2KX-GP
DY EC7929 SCD1U25V2KX-GP
DY EC7936 SCD1U25V2KX-GP
DY EC7944 SCD1U25V2KX-GP

A00-20100204

+CPU_GFX_CORE
0.1uF*2
DY EC7946 SCD1U25V2KX-GP
DY EC7947 SCD1U25V2KX-GP

+VGA_CORE
56pF*1
DY EC7928 SC56P50V2JN-2GP

+1.5V_SUS
56pF*3
DY EC7930 SC56P50V2JN-2GP
DY EC7931 SC56P50V2JN-2GP
DY EC7932 SC56P50V2JN-2GP

+VCC_CORE
56pF*2
UMA EC7934 SC56P50V2JN-2GP
DY EC7935 SC56P50V2JN-2GP

X02-20100209

+5V_RUN
56pF
DY EC7937 SC56P50V2JN-2GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	Berry	A00

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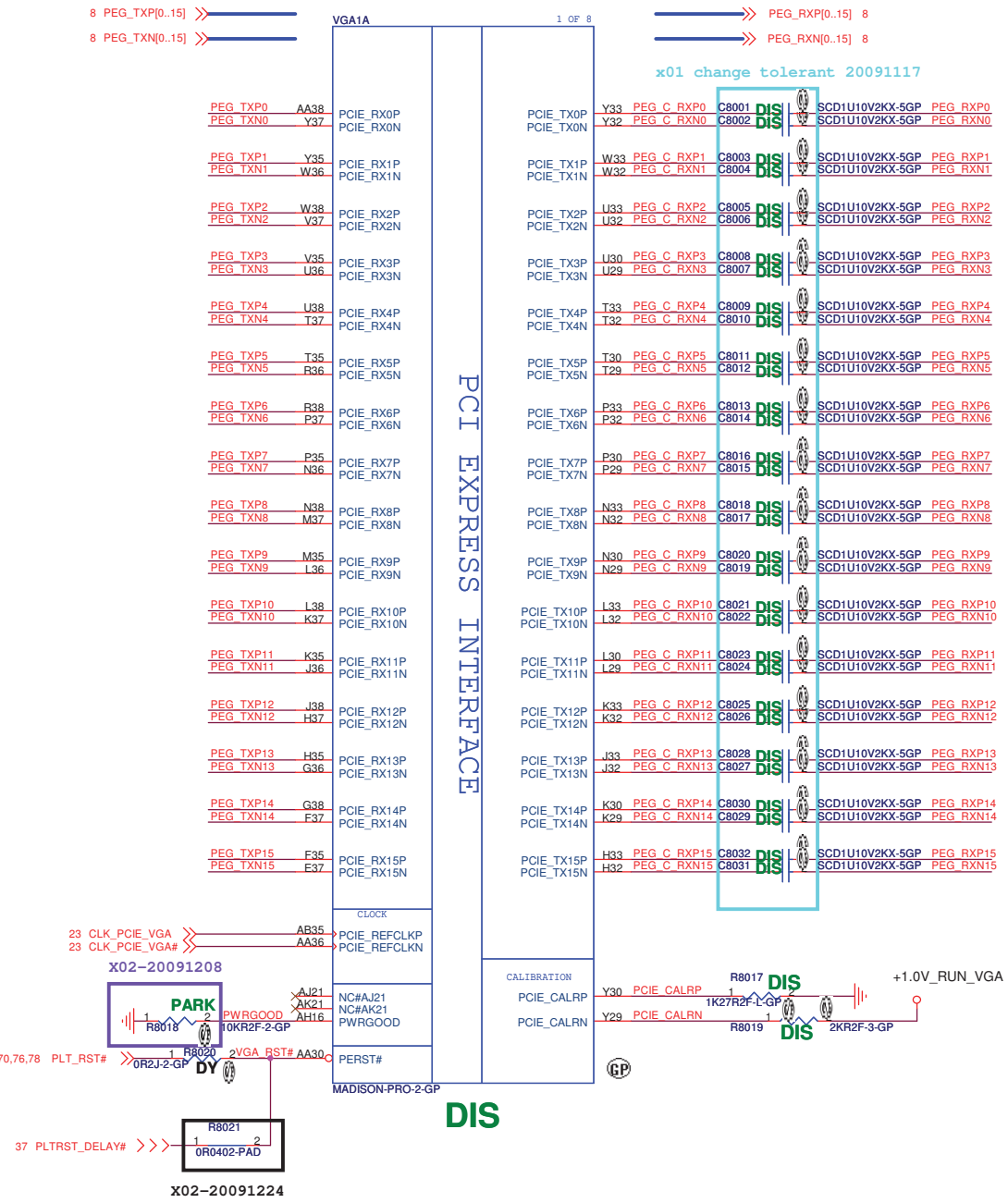


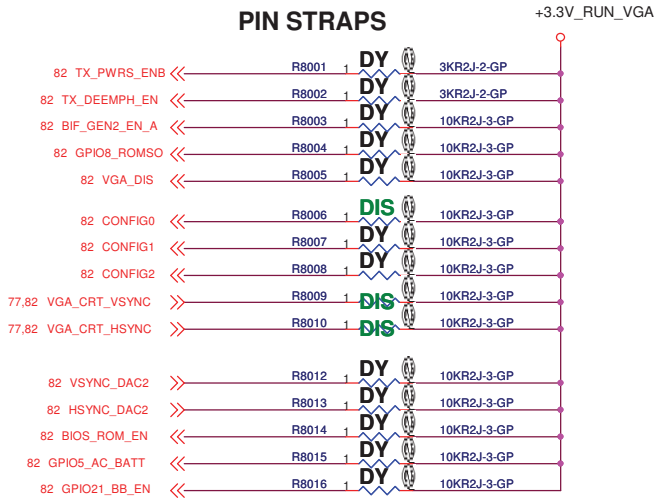
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU PCIE/STRAPPING(1/5)

Size: A3 | Document Number: Berry | Rev: A00

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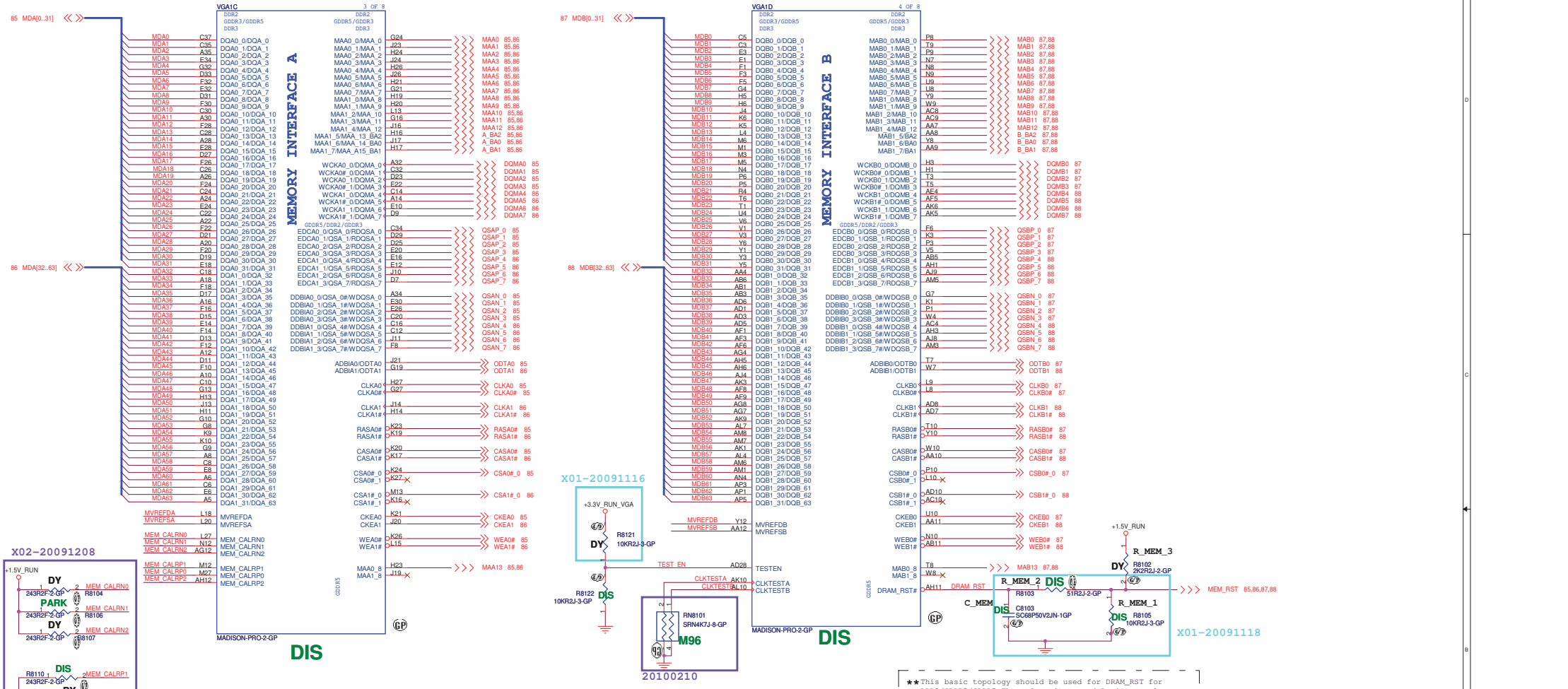


DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

DDR3/GDDR3 Memory Stuff Option(M92/M96)

	GDDR3	DDR3
MVDDQ	1.8V/1.5V	1.5V
Ra	40.2R	100R
Rb	100R	100R

Designator	For Mannhatton	For M96-M2/M92-M2
R_MEM_1	10K	2.2nF
R_MEM_2	51R	0R/Short
R_MEM_3	DNI	DNI
C_MEM	68pF	10K

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size	Document Number	Rev
C	Berry	A00

Date: Monday, March 29, 2010 Sheet 81 of 92

MEMORY ID Table

DVPDATA[0:3]	Description
0001	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz) 64M*16
0011	DDR3 Hynix-H5TQ2G63BFR-12C (800MHz) 128M*16
0010	DDR3 SAMSUNG K4W2G1646B-HC12 (800MHz) 128M*16
0000	DDR3 SAMSUNG-K4W1G1646E-HC12 (800MHz) 64M*16

DVPDATA[0:3] Default:Pull down

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

For new version no 27M

LVDS Interface

MEM_ID Control
X02-20091222

Straps

I2C Bus for LVDS

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

X02-20100104

X02-20100104

X02-20091222

X02-20091210
Voltage Swing:1.8V

X02 20091208

DDC1 channel for CRT

DDC2 channel for HDMI

DDC1/DDC2/DDC6 have 5V-tolerant

x01 Change tolerant 20091117

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

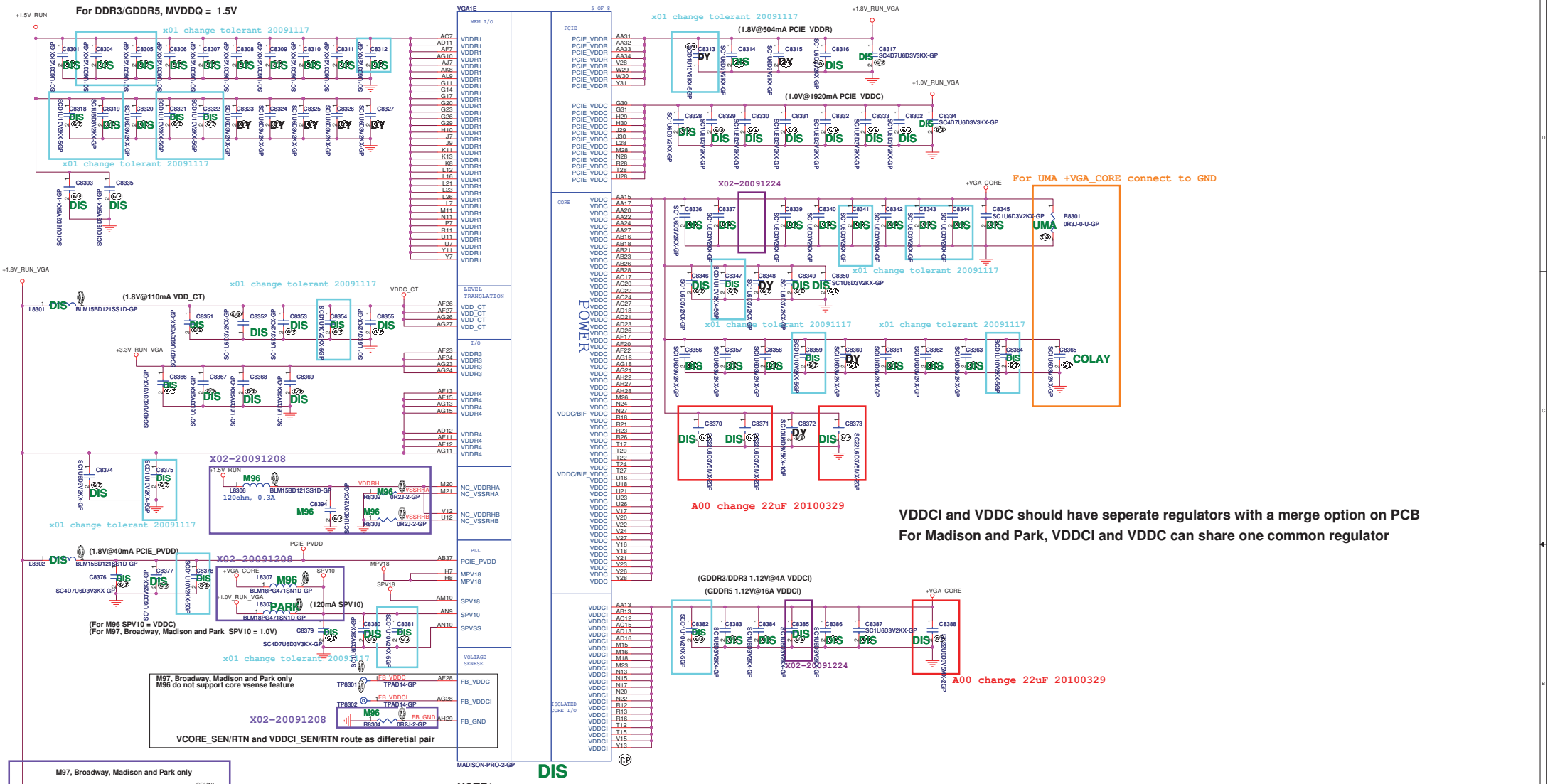
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 82 of 92



NOTE1:
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134

NOTE2:
FB_VDDC, FB_VDDCI and FB_GND are not support on M96

NOTE3:
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.

NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax

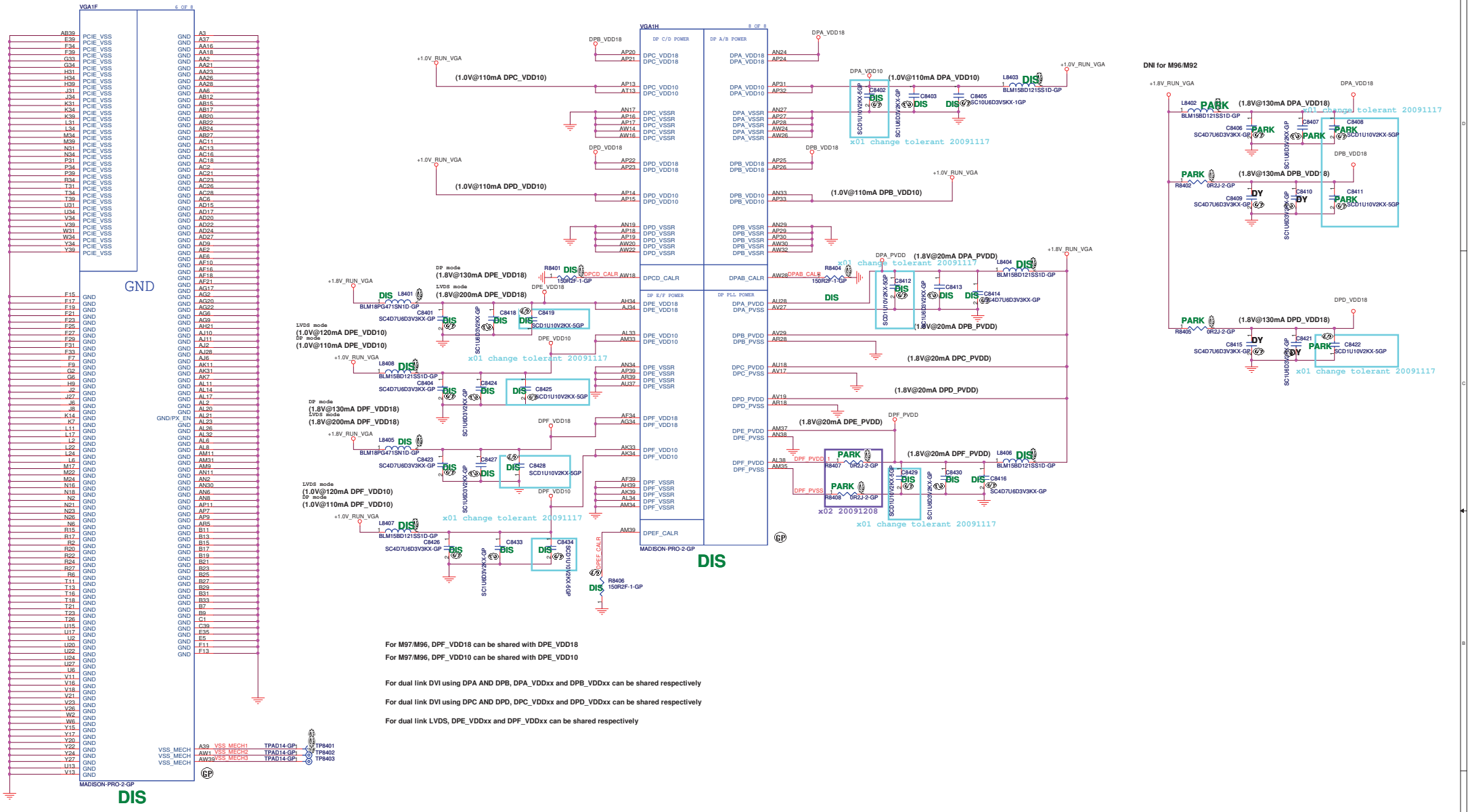
<Core Design>

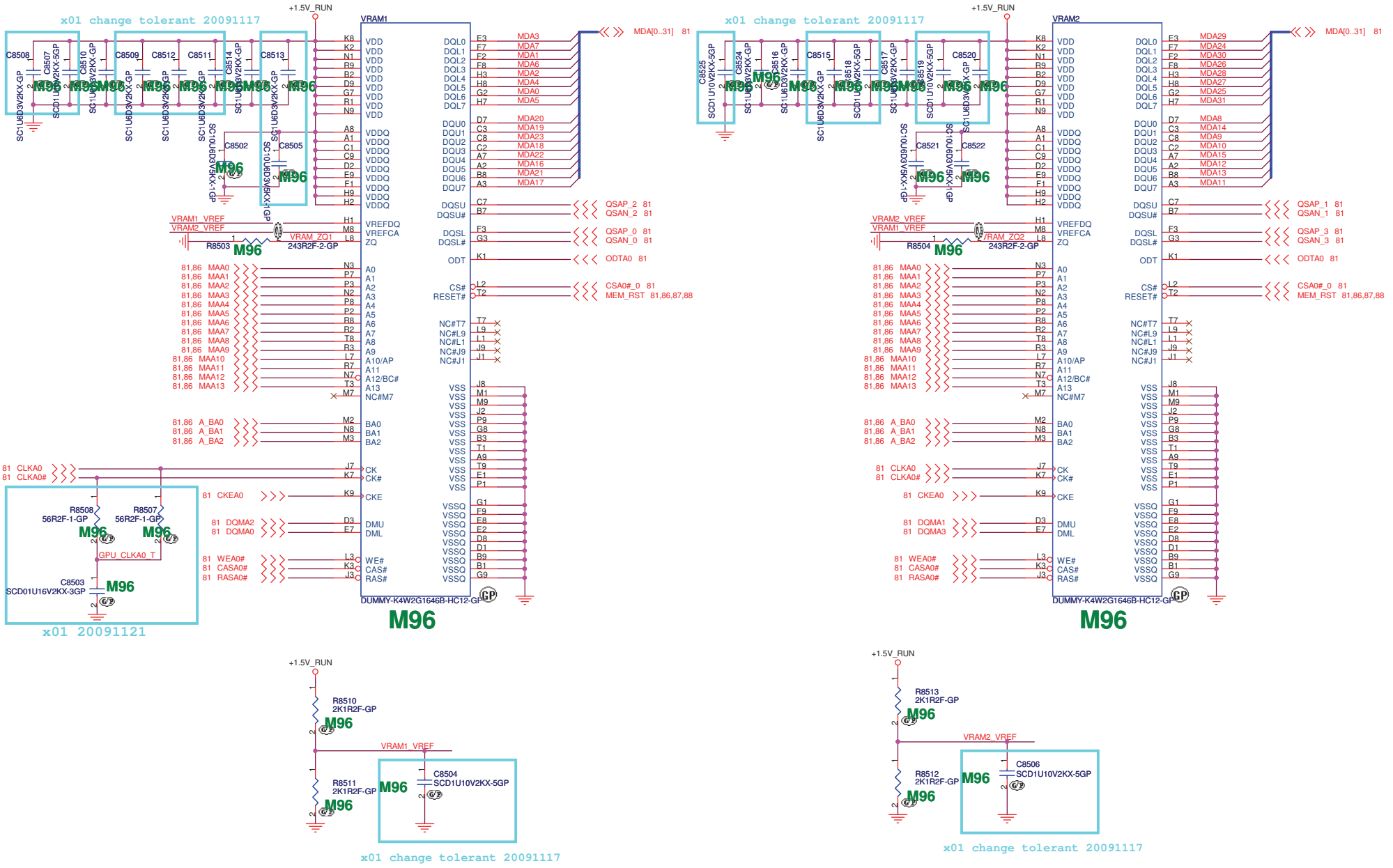
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size	Document Number	Rev
A2	Berry	A00

Date: Wednesday, March 31, 2010 Sheet 83 of 92


VGA1F
6 OF 8
GND
DIS
MADISON-PRO-2-GP
VGA1H
8 OF 8
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
(1.0V@110mA DPC_VDD10)
(1.0V@110mA DPD_VDD10)
(1.0V@110mA DPA_VDD10)
(1.0V@110mA DPB_VDD10)
(1.8V@20mA DPA_PVDD)
(1.8V@20mA DPB_PVDD)
(1.8V@20mA DPC_PVDD)
(1.8V@20mA DPD_PVDD)
(1.8V@20mA DPE_PVDD)
(1.8V@20mA DPF_PVDD)
x01 change tolerant 20091117
x02 20091208
DNI for M96/M92
(1.8V@130mA DPA_VDD18)
(1.8V@130mA DPB_VDD18)
(1.8V@130mA DPD_VDD18)
For M97/M96, DPF_VDD18 can be shared with DPE_VDD18
For M97/M96, DPF_VDD10 can be shared with DPE_VDD10
For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively
For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively
For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU_DPPWR/GND(5/5)
Size
A2
Document Number
Berry
Rev
A00
Date: Monday, February 22, 2010
Sheet 84 of 92



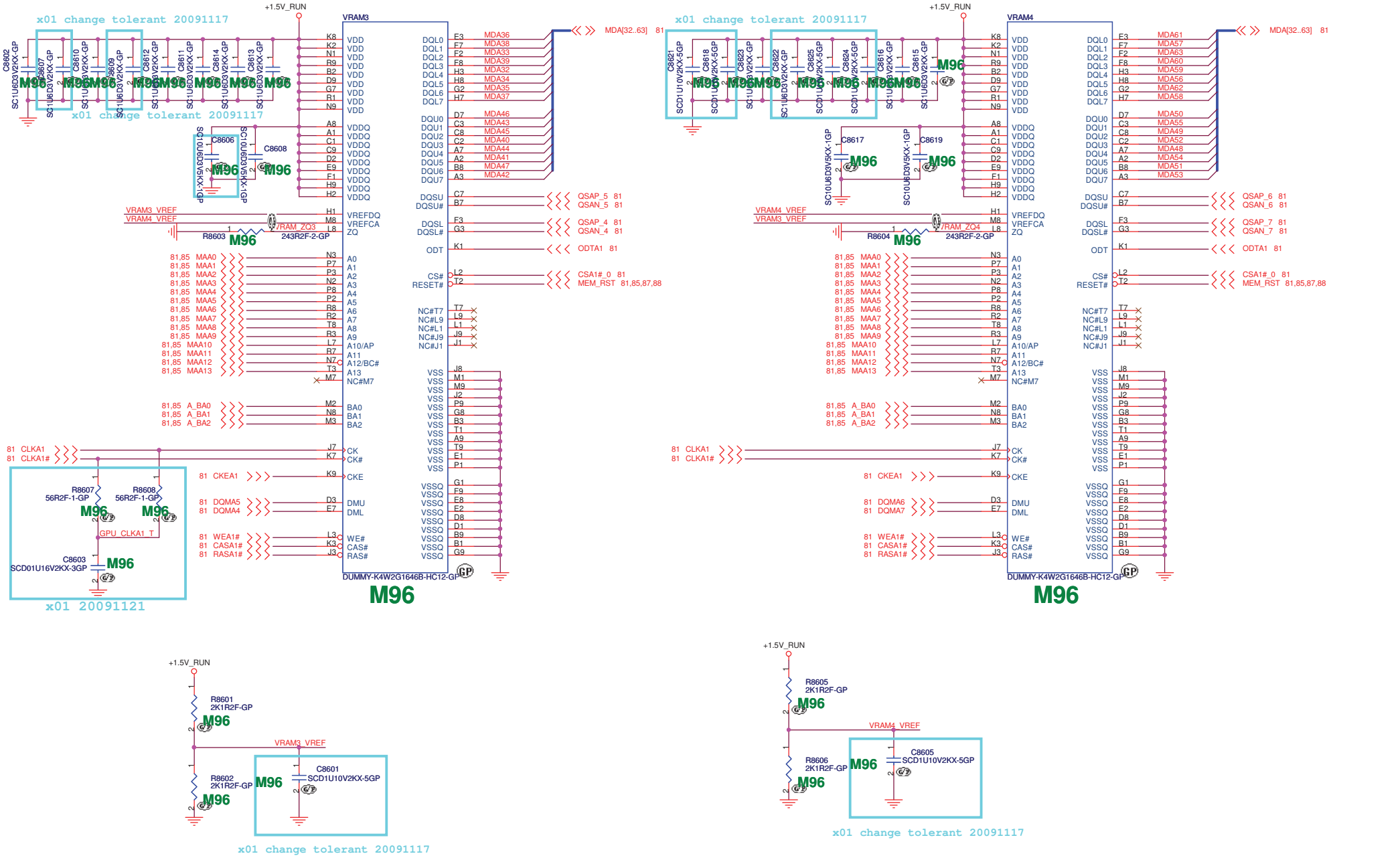
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
Custom	Berry	A00

Date: Monday, March 29, 2010 Sheet 85 of 92



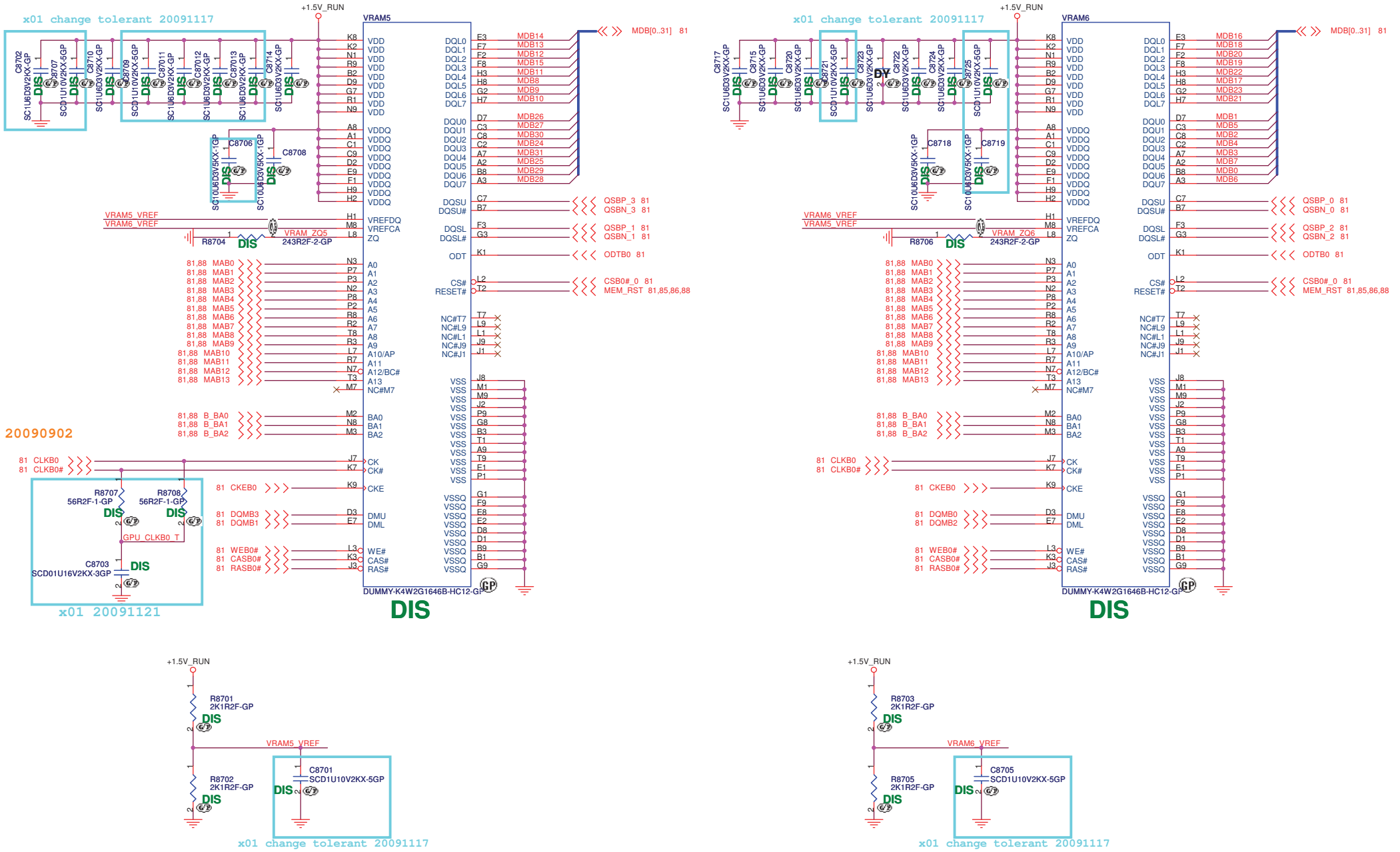
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 86 of 92



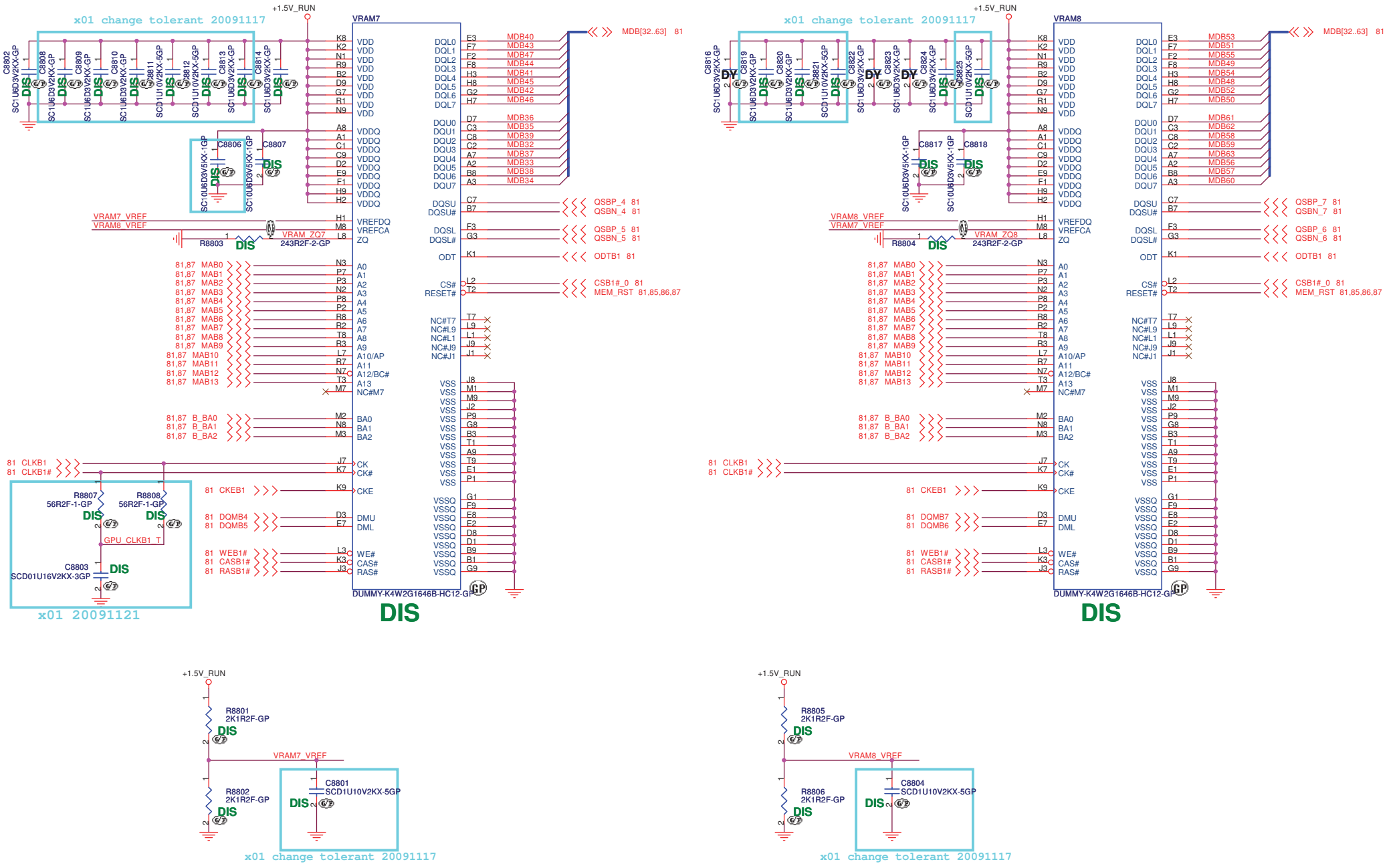
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

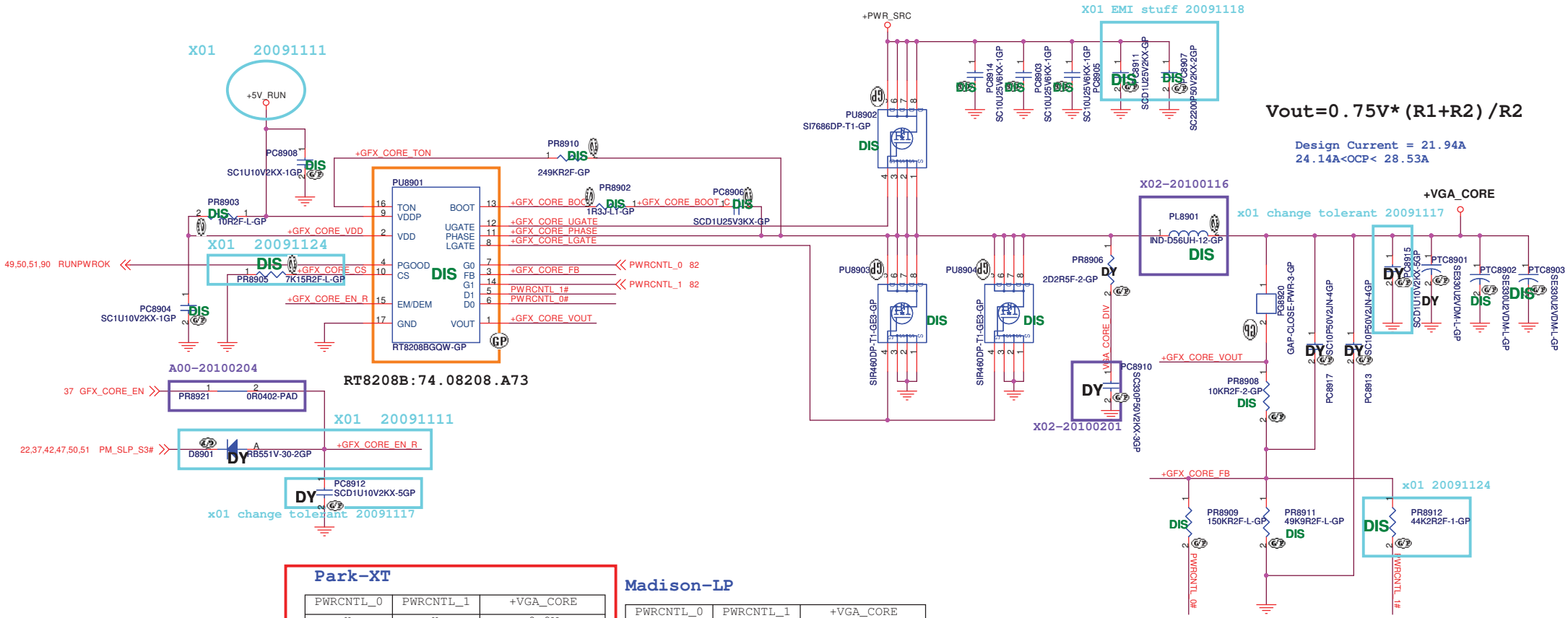
Size: A3 | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 87 of 92


x01 change tolerant 20091117
+1.5V_RUN
VRAM7
VRAM8
MDB[32..63] 81
QSBP_4 81
QSBN_4 81
QSBP_5 81
QSBN_5 81
QSBP_7 81
QSBN_7 81
QSBP_6 81
QSBN_6 81
ODTB1 81
CSB1#_0 81
MEM_RST 81,85,86,87
VRAM7_VREF
VRAM8_VREF
R8803
R8804
VRAM_ZQ7
VRAM_ZQ8
243R2F-2-GP
DUMMY-K4W2G1646B-HC12-GP
DIS
x01 20091121
GPU_CLKB1_T
R8807
R8808
56R2F-1-GP
C8803
SCD01U16V2KX-3GP
R8801
R8802
2K1R2F-GP
C8801
SCD1U10V2KX-5GP
R8805
R8806
C8804
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GPU-VRAM7,8 (4/4)
Size
A3
Document Number
Berry
Rev
A00
Date: Monday, March 29, 2010
Sheet 88 of 92

SSID = Video.PWR.Regulator

RT8208BGQW for +VGA_CORE



Vout=0.75V*(R1+R2)/R2

Design Current = 21.94A
24.14A<OCP< 28.53A

Park-XT

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.12V

Madison-LP

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
L	L	1.12V

M96-LP

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
L	L	1.0V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

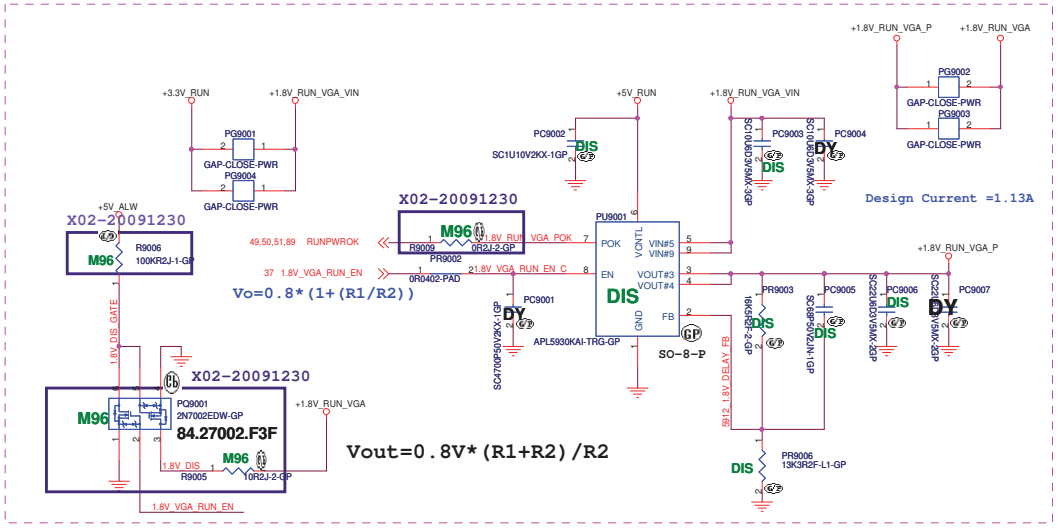
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_+VGA_CORE

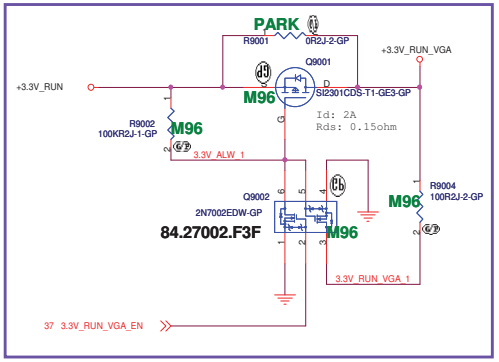
Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: A00

Date: Wednesday, March 31, 2010 | Sheet 89 of 92

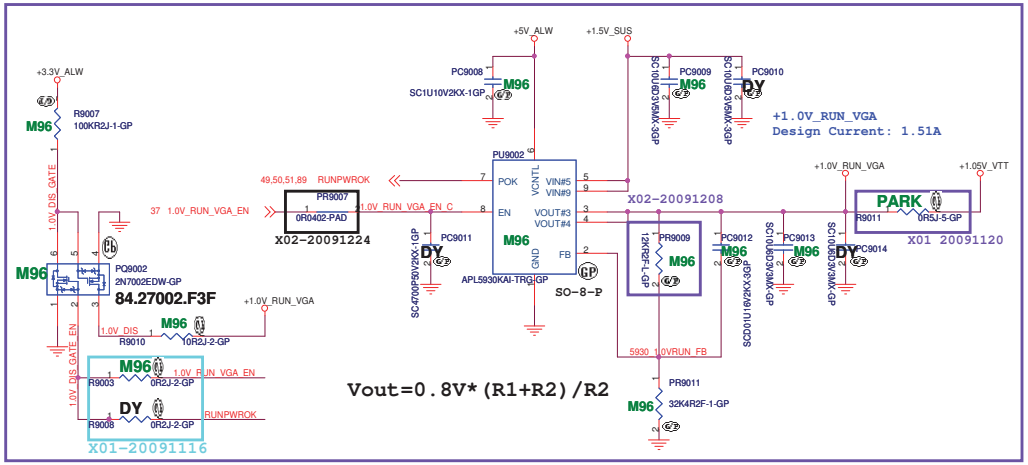
APL5930 for +1.8V_RUN_VGA



+3.3V_RUN_VGA



APL5930KAI for +1.0V_RUN_VGA



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size	Document Number	Rev
C	Berry	A00

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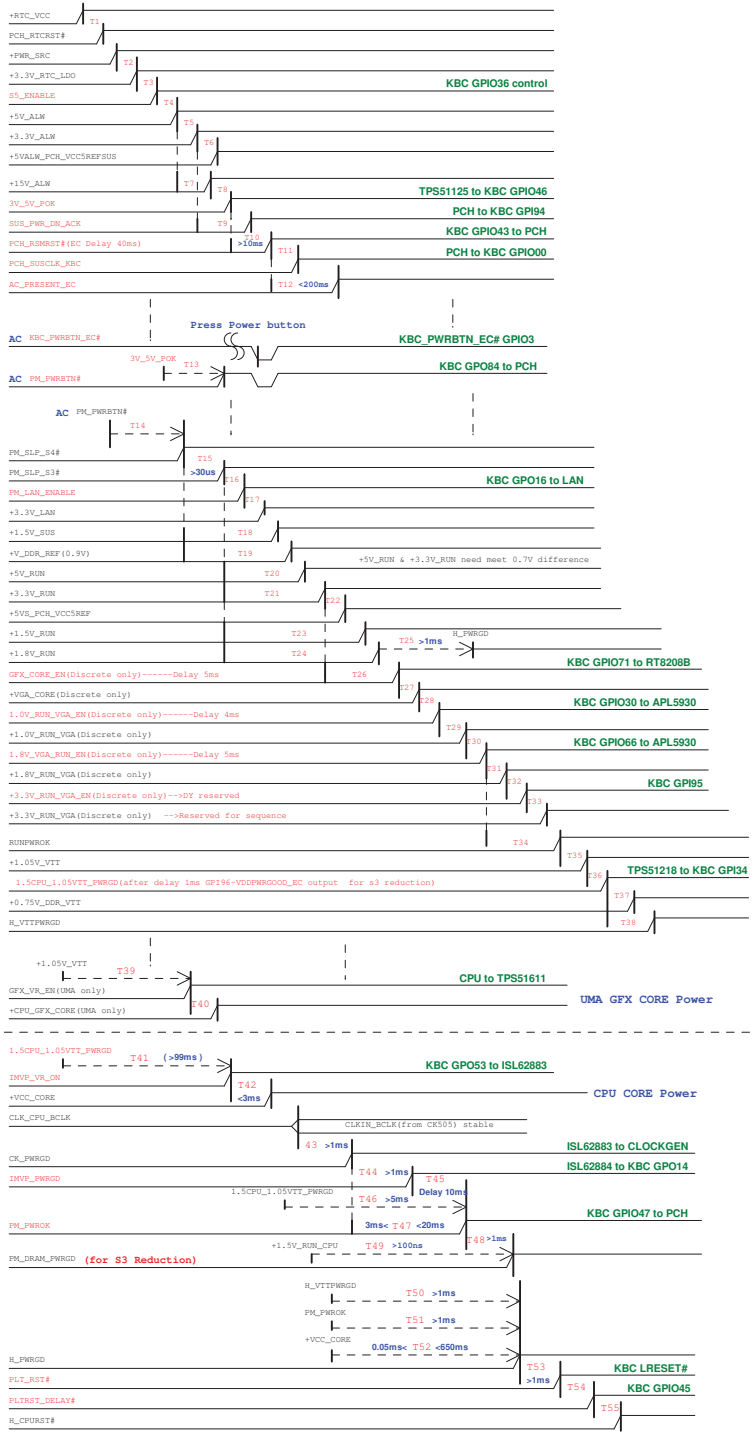
D15 Intel-Power Up Sequence

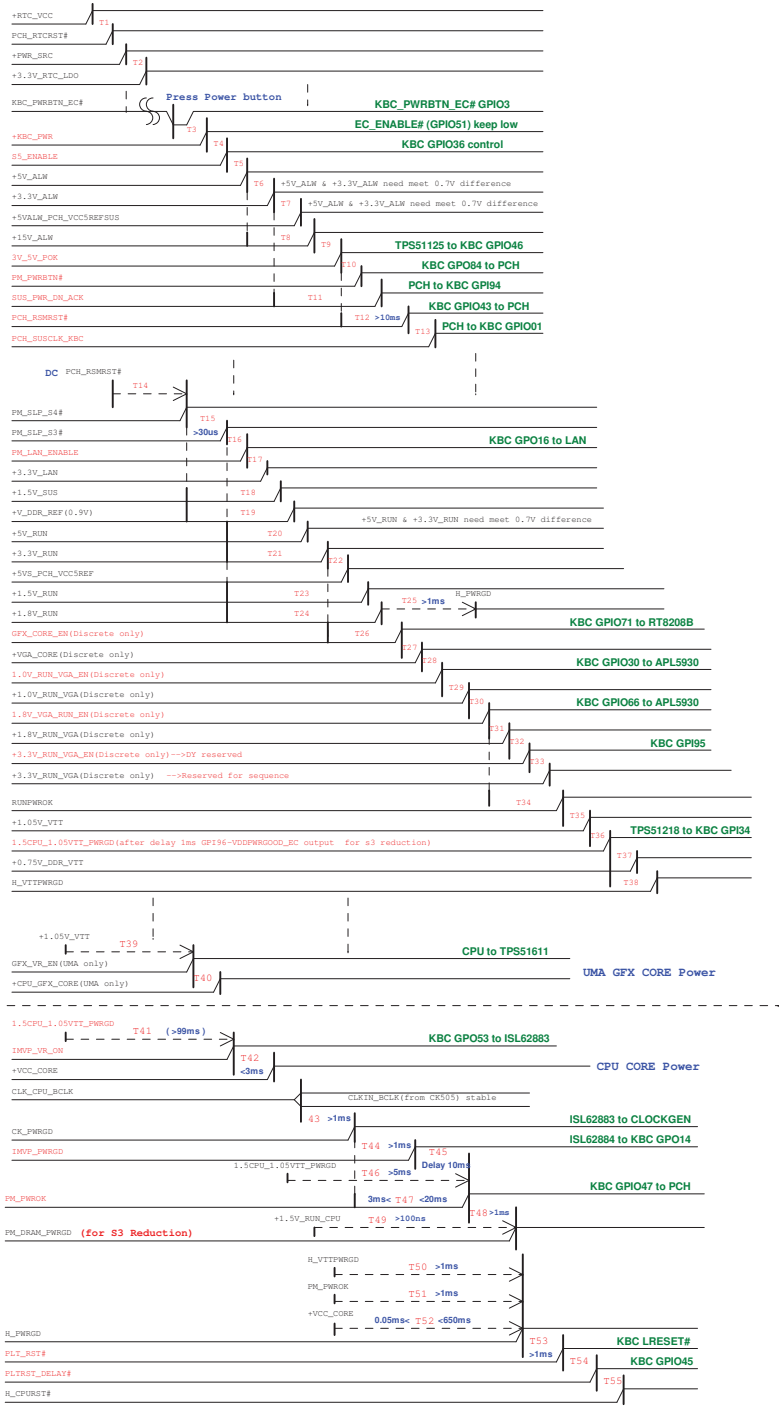
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size	Document Number	Rev
A1	Berry	A00

Date: Tuesday, March 09, 2010 Sheet 91 of 96

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 92 of 92