Compal Confidential

HBL50 Schematics Document

Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M

(With nVIDIA G73M/72MV)

2005-11-08

REV: 0.3

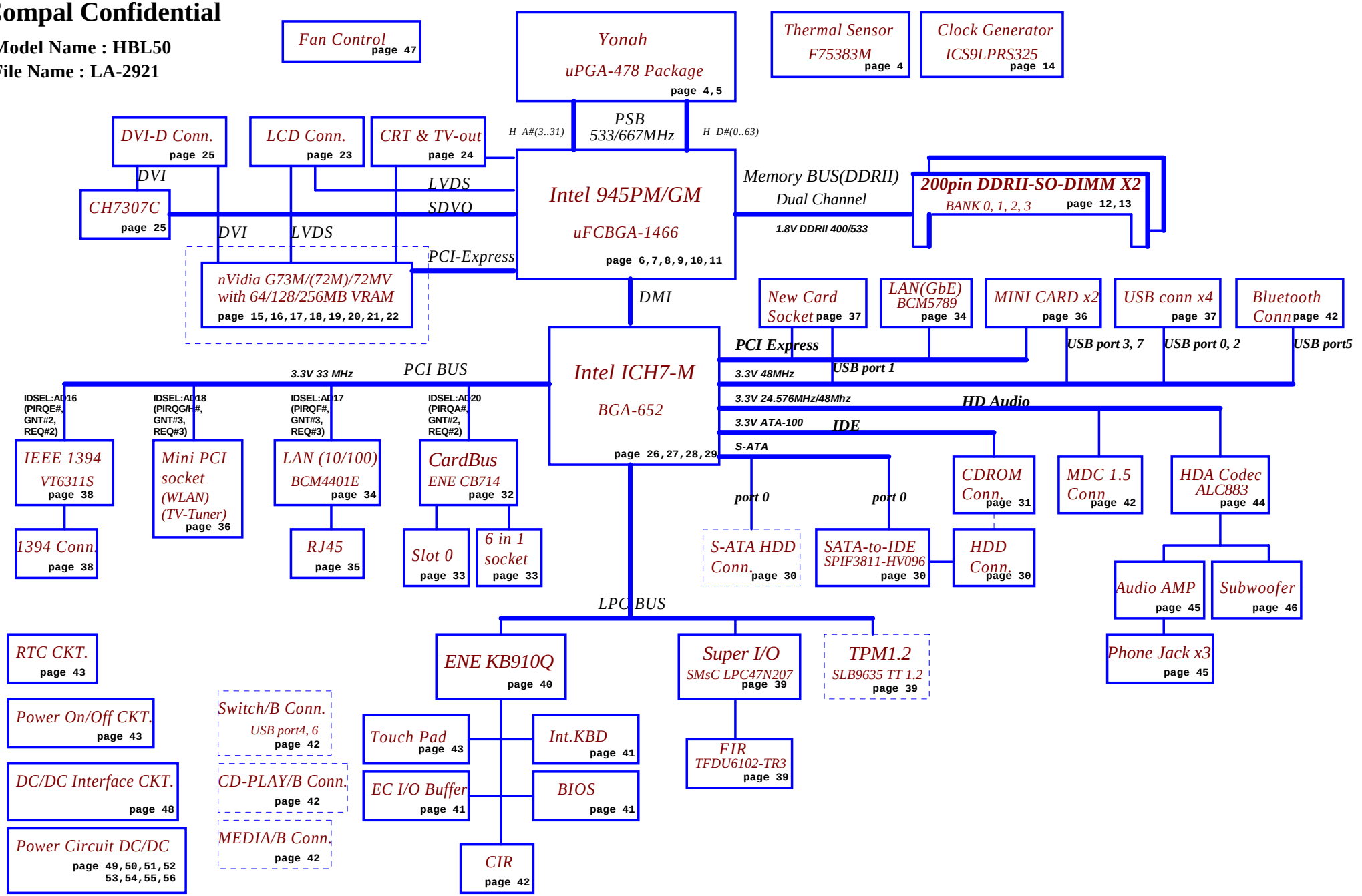
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title	Cover Page	
Size: B	Document Number: HBL50 LA-2921P	Rev: 0.3
Date: Friday, November 11, 2005	Sheet 1 of 59	

Compal Confidential

Model Name : HBL50
File Name : LA-2921



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: Block Diagrams

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 2 of 59

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
Fintek F75383M	1001 100X b

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VGA	PM@ + VGA@
UMA	GM@
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI CARD1	MINI1@
MINI CARD2	MINI2@
SATA-to-IDE	3811@
PATA	PATA@
GRAPEVINE	GRA@
G72MV Only	G72@
G73 Only	G73@
VRAM	X76@
VRAM 64M	64@
VRAM 128M	64@+128@
VRAM 256M	64@+128@+256@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
LCM	LCM@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@
VP1020	VP1020@
INTERNAL MIC	INTMIC@
1394	1394@
SATA HDD	SATA@

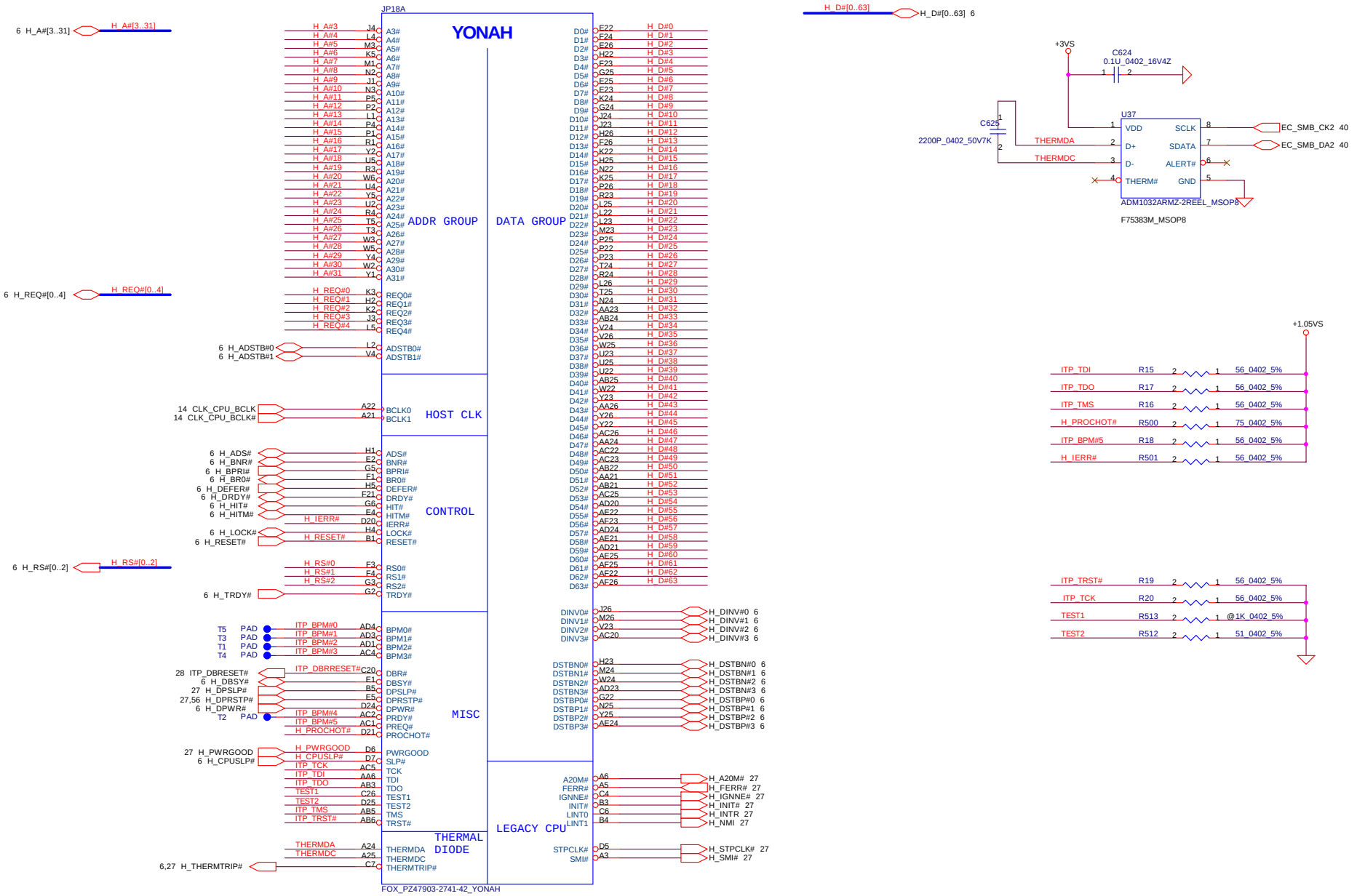
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: Notes List

Size: B | Document Number: HBL50 LA-2921P | Rev: 0.3

Date: Friday, November 11, 2005 | Sheet 3 of 59



Layout Note:
THERMDA & THERMDC Trace / Space = 10 / 10 mil

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

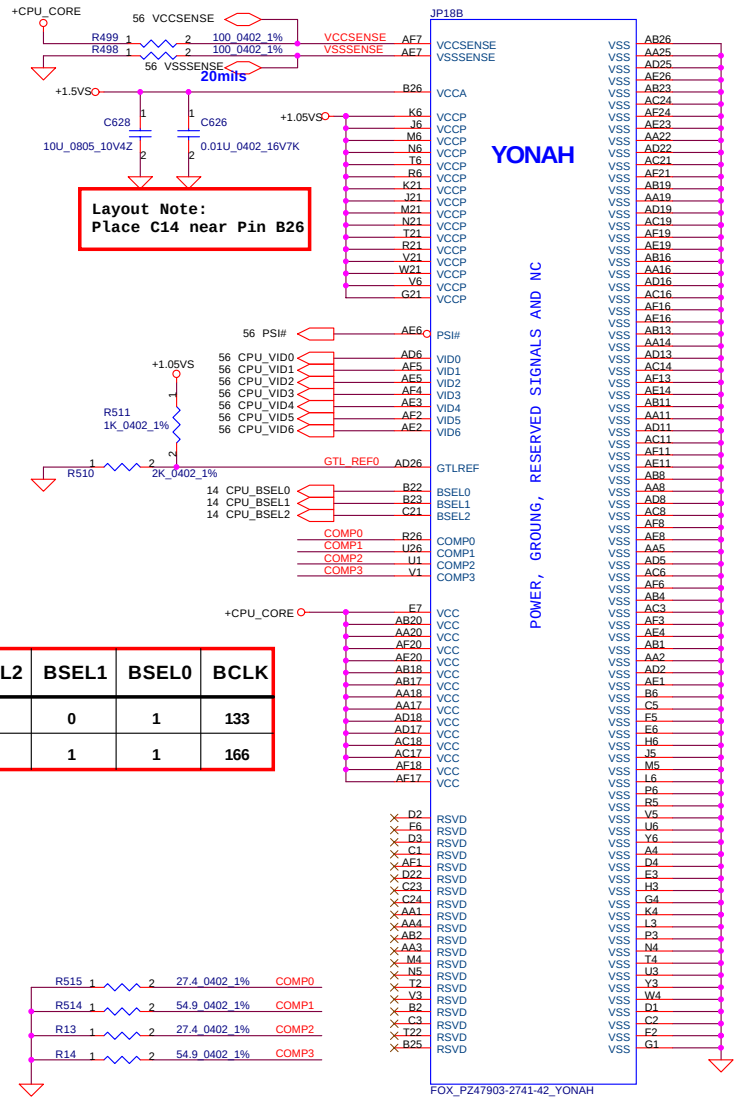
Compal Electronics, Inc.

Title: Yonah (1/2)

Size: Custom | Document Number: HBL50 LA-2921P | Rev: 0.3

Date: Friday, November 11, 2005 | Sheet 4 of 59

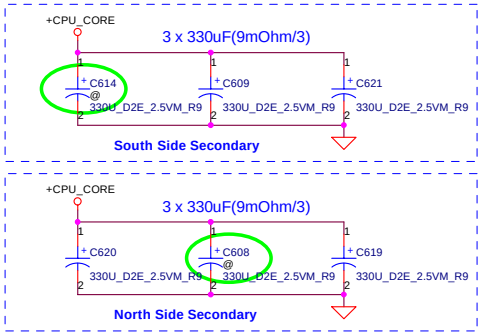
Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4Ohms with 50 mil spacing.
Place PU and PD wihin 1 inch of CPU.

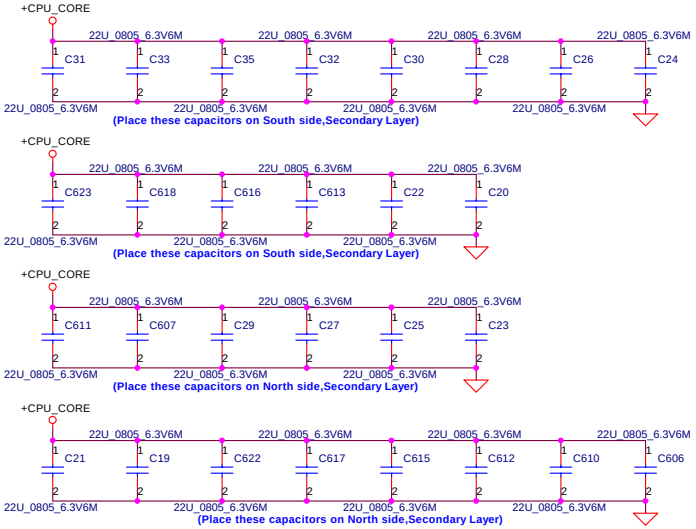


BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133
0	1	1	166

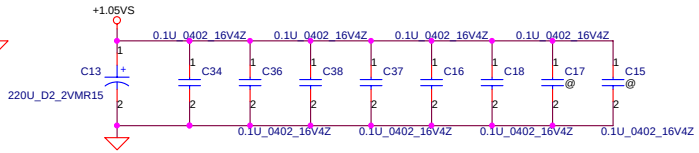
TRACE CLOSELY CPU < 0.5'

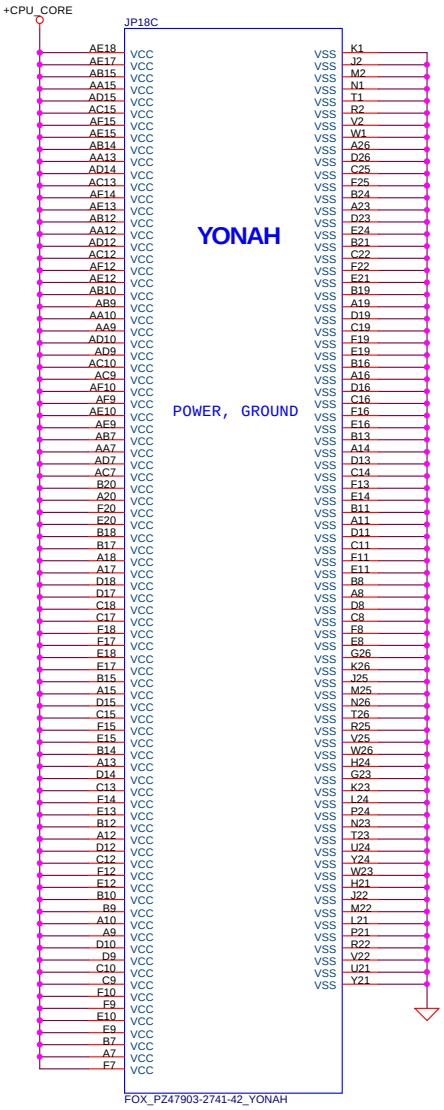
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Space 25mils (55Ohms)





+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32





Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

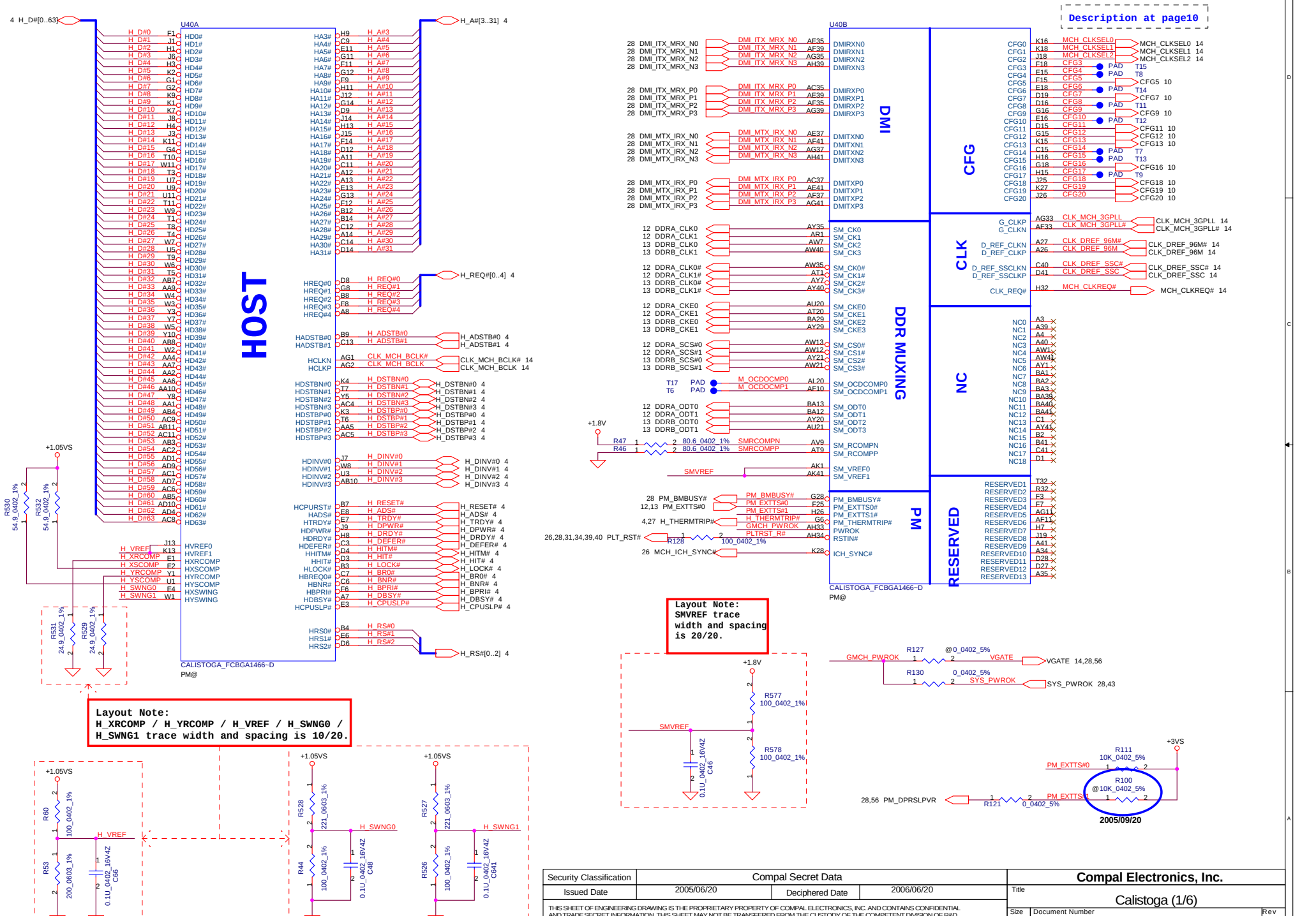
Compal Electronics, Inc.

Title: Yonah (2/2)

Size: B | Document Number: HBL50 LA-2921P | Rev: 0.3

Date: Friday, November 11, 2005 | Sheet 5 of 59

945GM(A-3)(QK56)[QS]: SA0000059D0(ABO!)
945PM(A-3)(QK58)[QS]: SA00000KD70(ABO!)



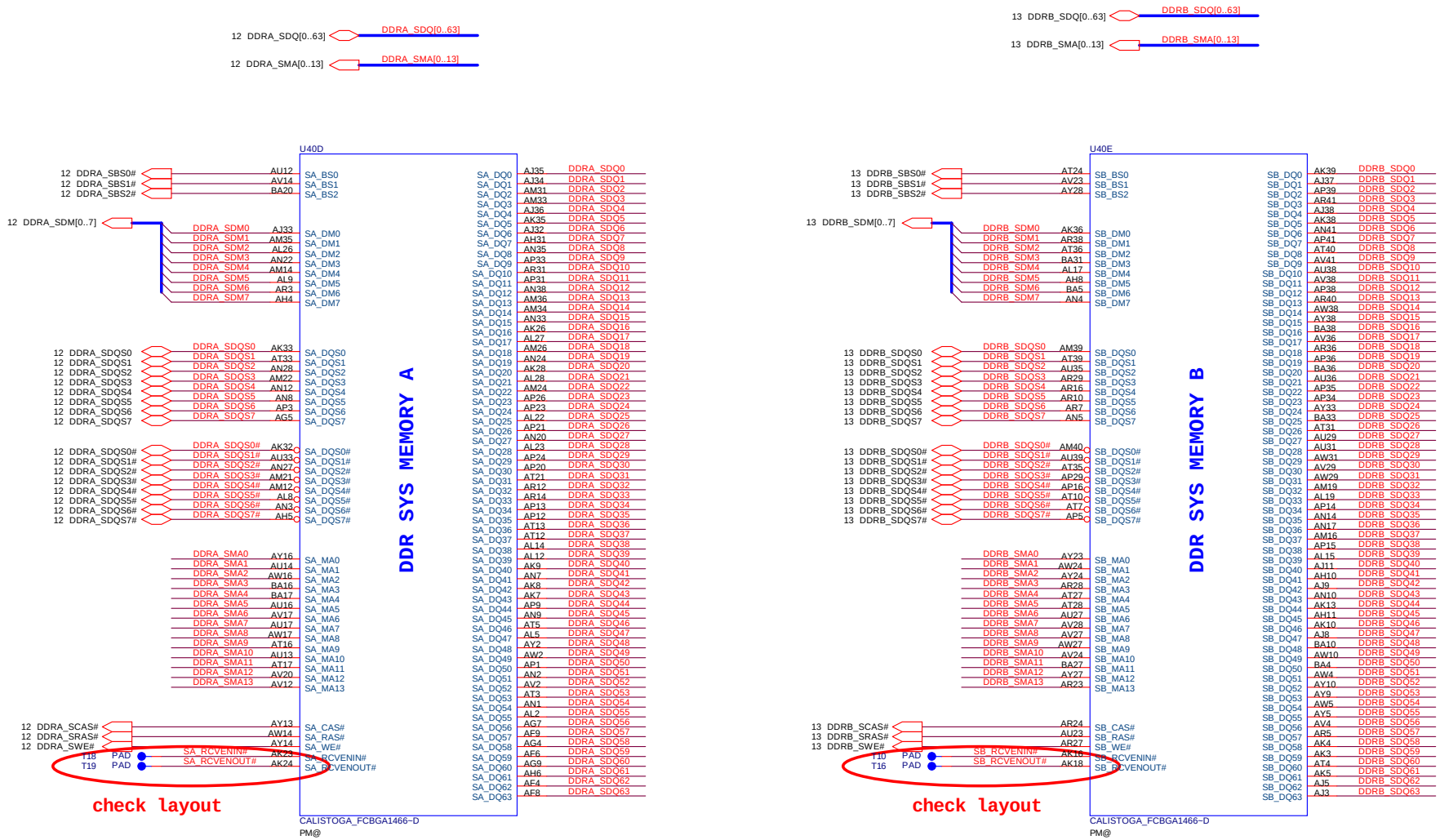
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: Calistoga (1/6)

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

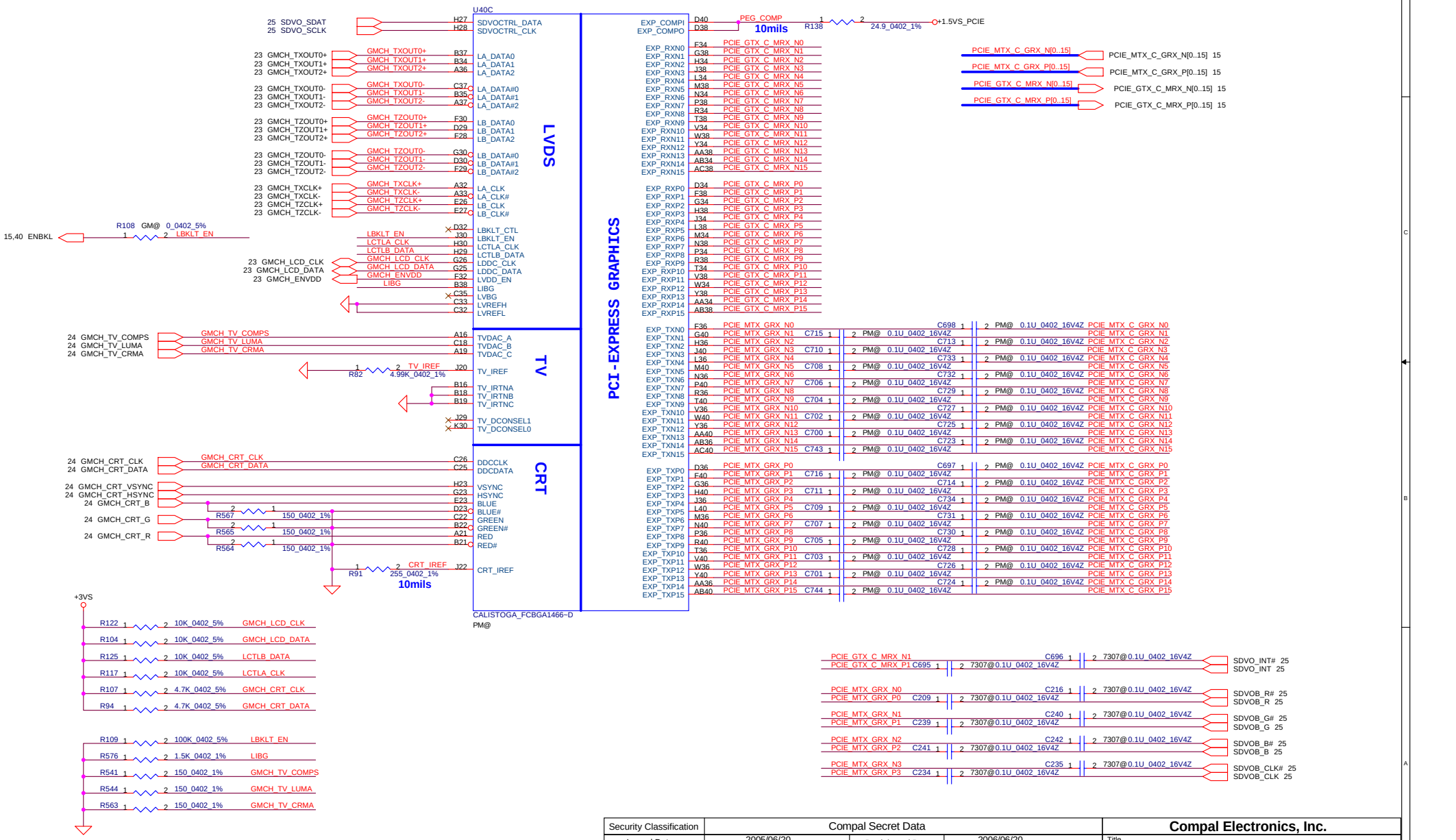
Date: Friday, November 11, 2005 Sheet 6 of 59



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title	Calistoga (2/6)	
Size B	Document Number HBL50 LA-2921P	Rev 0.3
Date: Friday, November 11, 2005	Sheet 7 of 59	



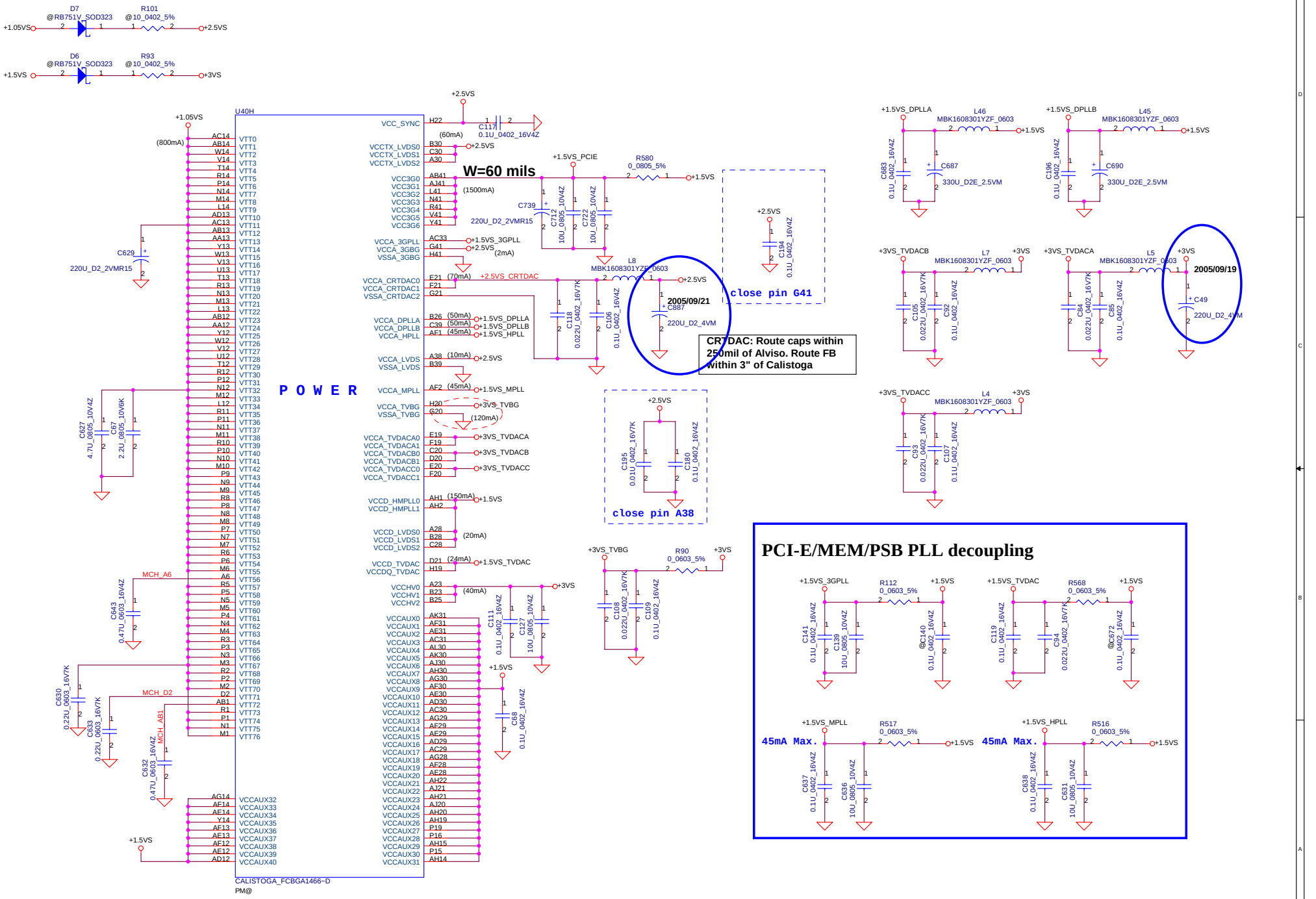
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: Calistoga (3/6)

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 8 of 59



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: Calistoga (4/6)

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 | Sheet 9 of 59

Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation*(Default)
CFG11 PSB 4X CLK Enable	0 = Reserved 1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

2005/09/20

Place near pin AT41 & AM41

Place near pin BA23

Place near pin BA15

Place near pin AV1 & AJ1

CALISTOGA_FCBGA1466-D

PM@

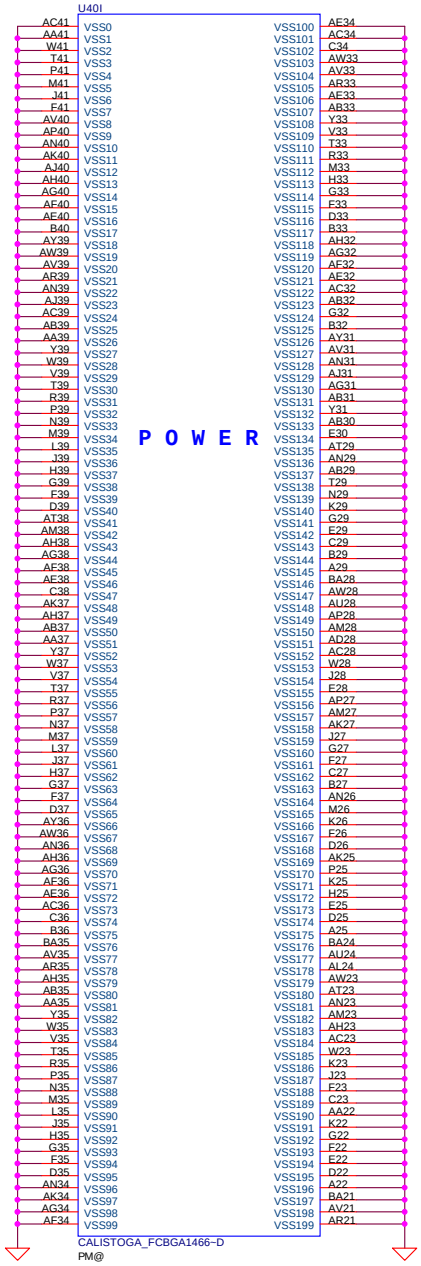
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

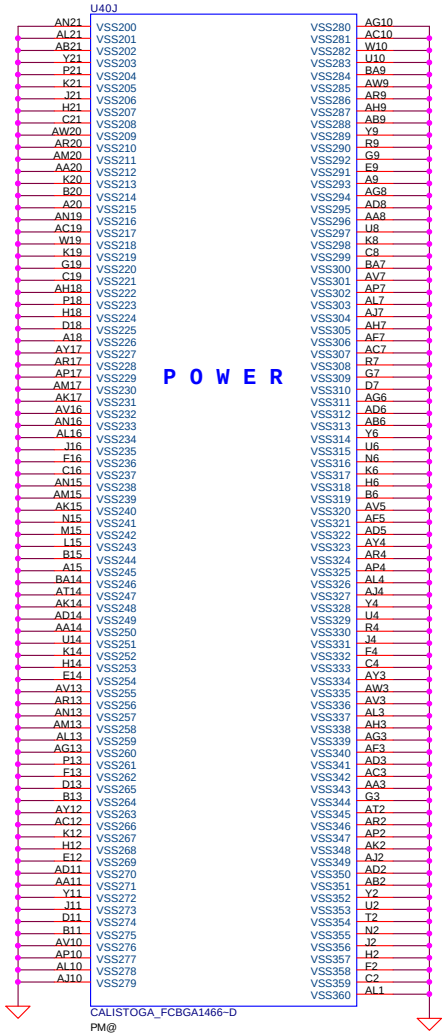
Compal Electronics, Inc.

Title: Calistoga (5/6)

Size: B | Document Number: HBL50 LA-2921P | Rev: 0.3

Date: Friday, November 11, 2005 | Sheet 10 of 59





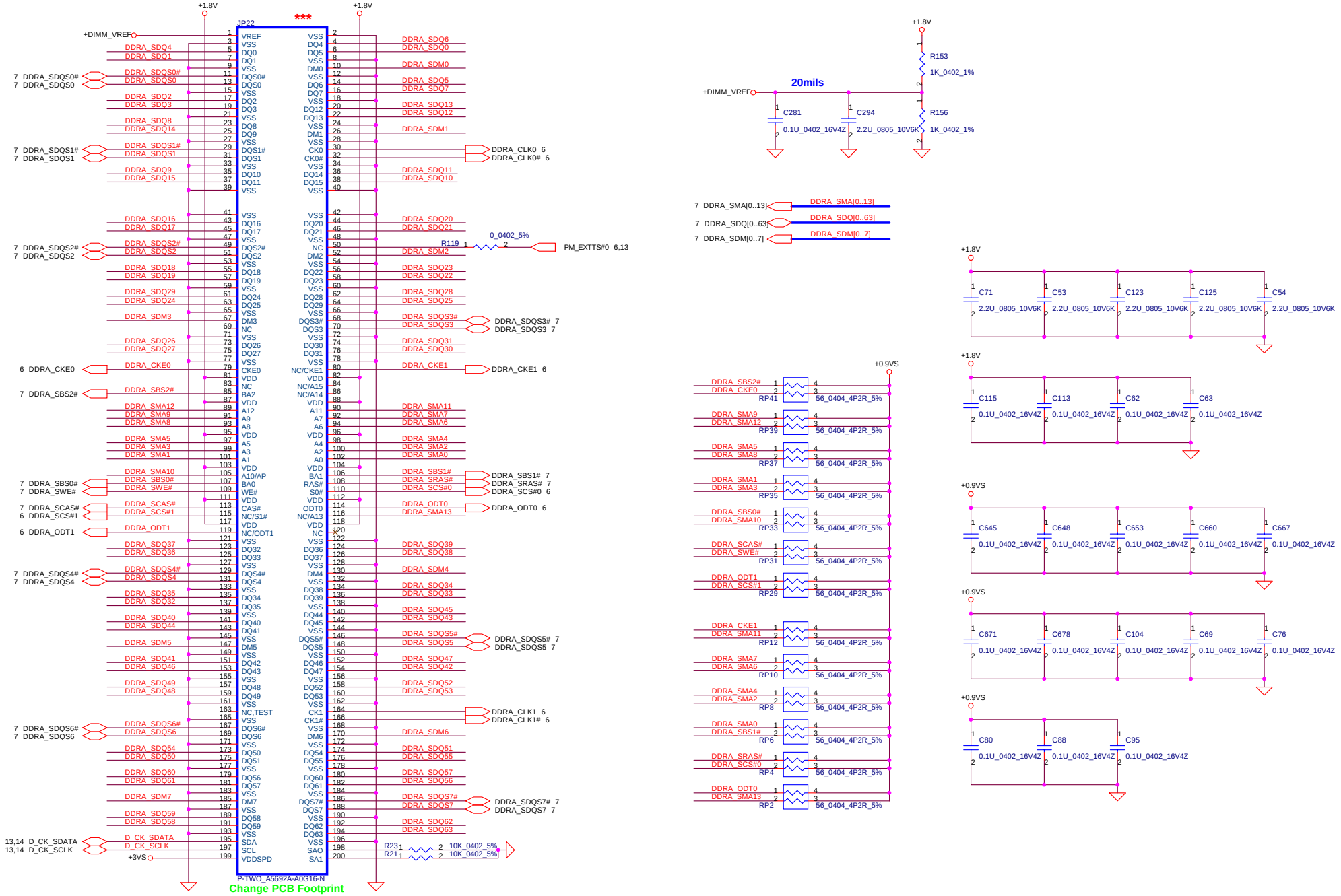
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: Calistoga (6/6)

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 11 of 59



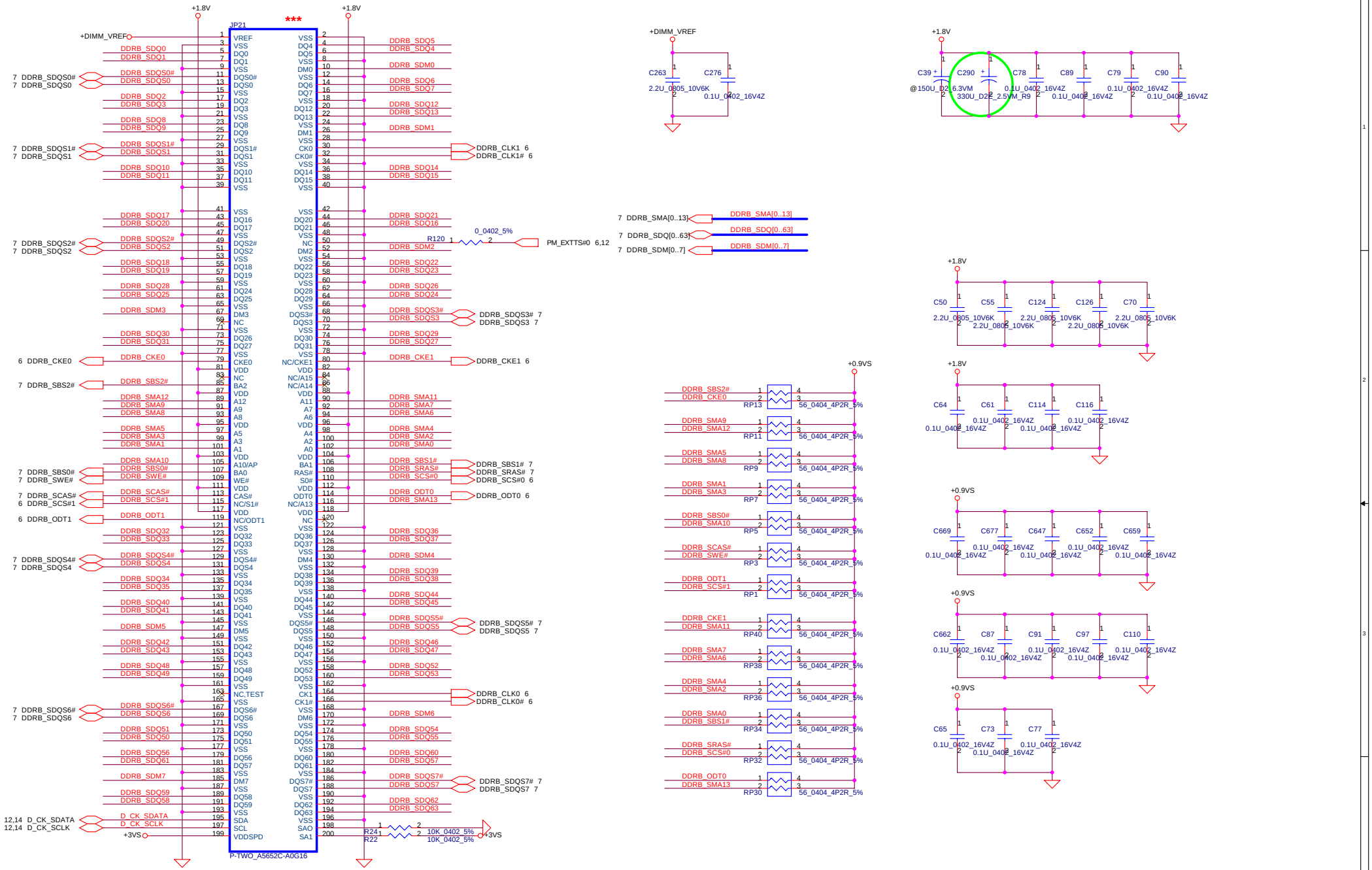
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: DDRII-SODIMM0

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 12 of 59



DIMM1 STD H:5.2mm (BOT)

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title	DDRII-SODIMM1
Size	B
Document Number	HBL50 LA-2921P
Rev	0.3
Date:	Friday, November 11, 2005
Sheet	13 of 59

Clock Generator

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR325

	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz_1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

**SEL_24M/PCICLK2=0=TESTMODE
**SEL_PCI6/PCICLK1=0=CLKREQ5#

**SEL_PCI5=1=PCICLK5

ITP_EN/PCICLK_F0=0=SRC pair

2005/08/31

2005/10/18

2005/08/31

2005/10/18

G72@
G73M: ICS9LPR325CKLFT_MLF72: SA00000RE20
G72M:SLG8LP465VTR: SA00000TS00

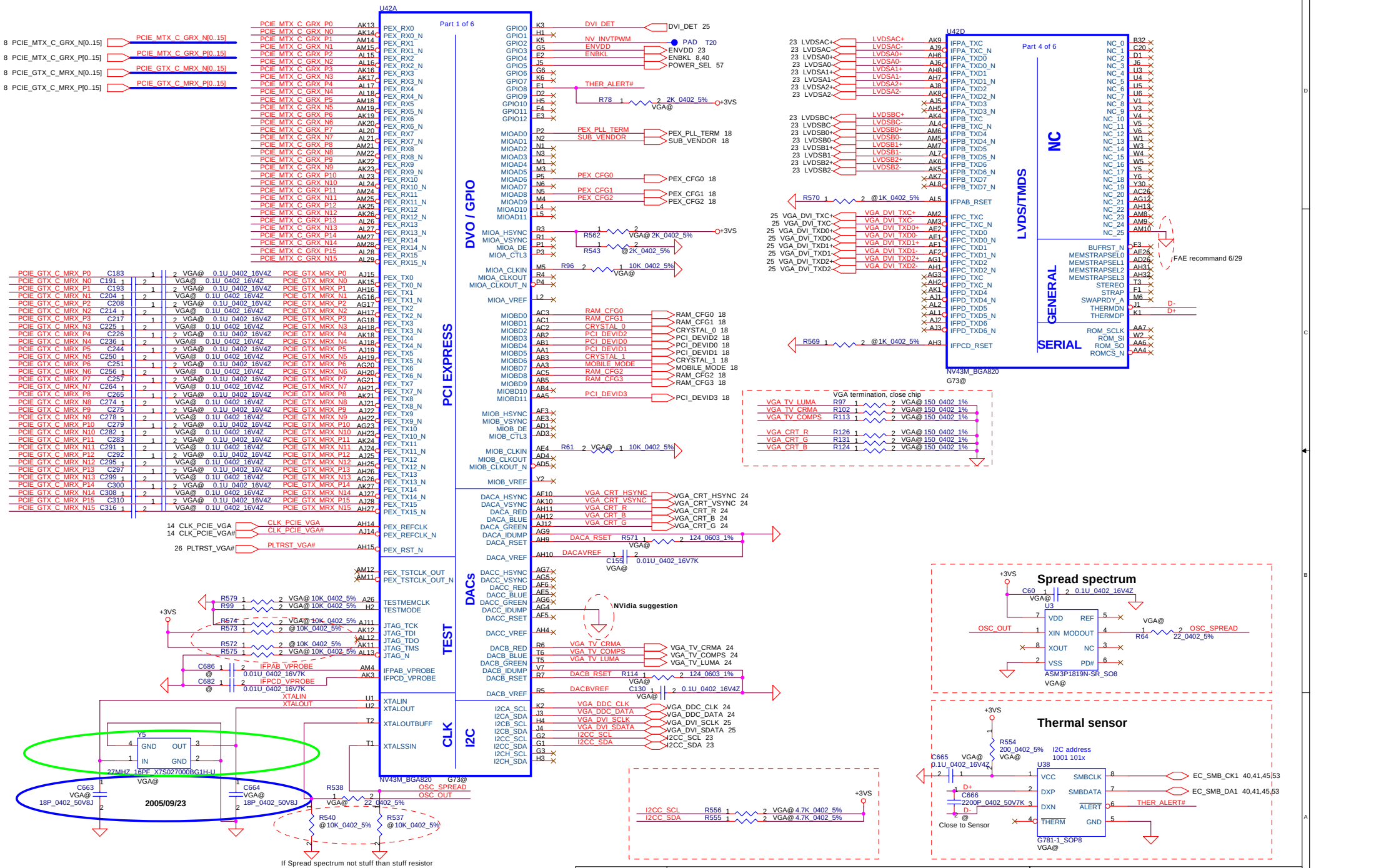
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: Clock Generator

Size: B | Document Number: HBL50 LA-2921P | Rev: 0.3

Date: Friday, November 11, 2005 | Sheet 14 of 59



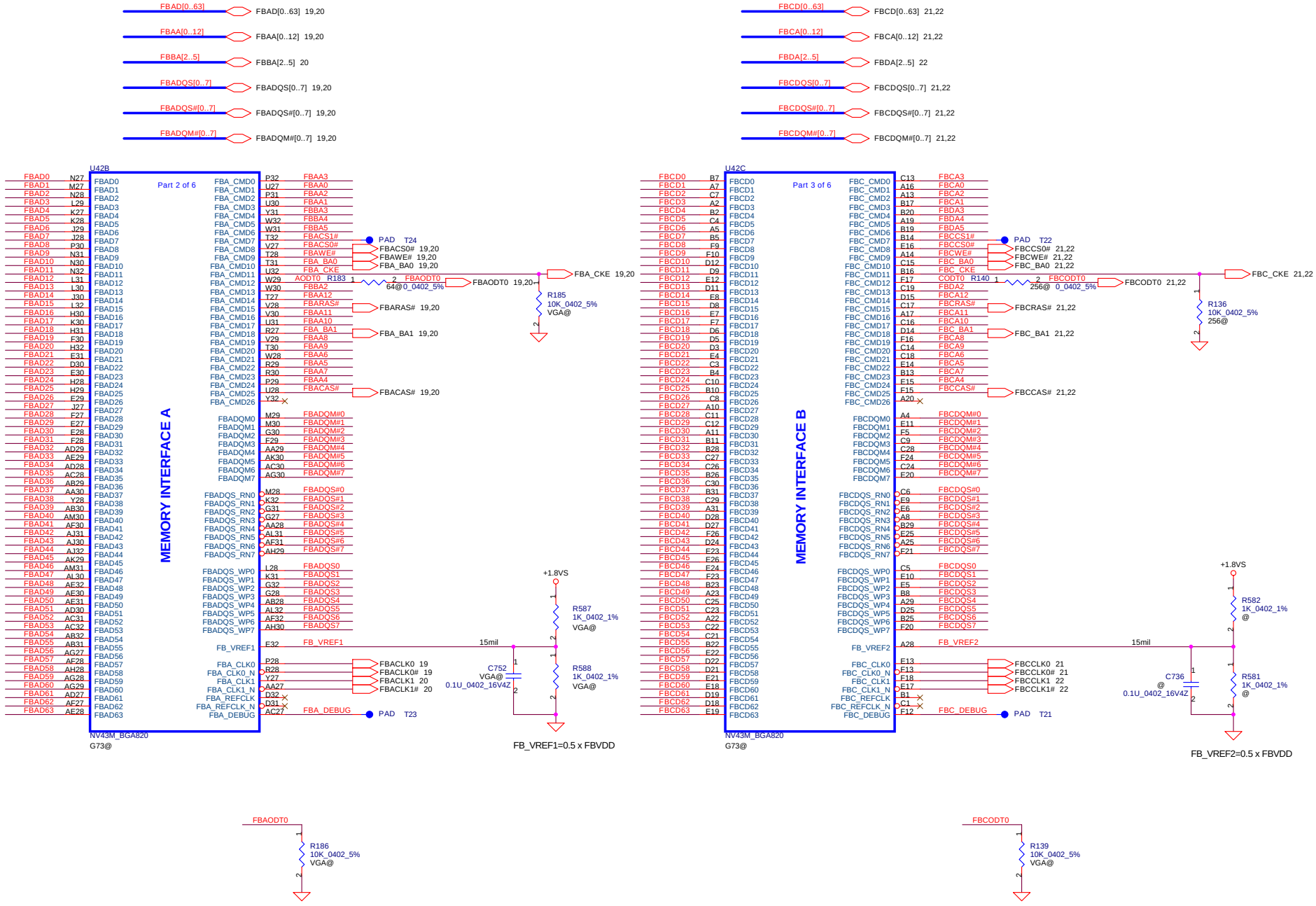
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: G72/G73 Main

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 15 of 59



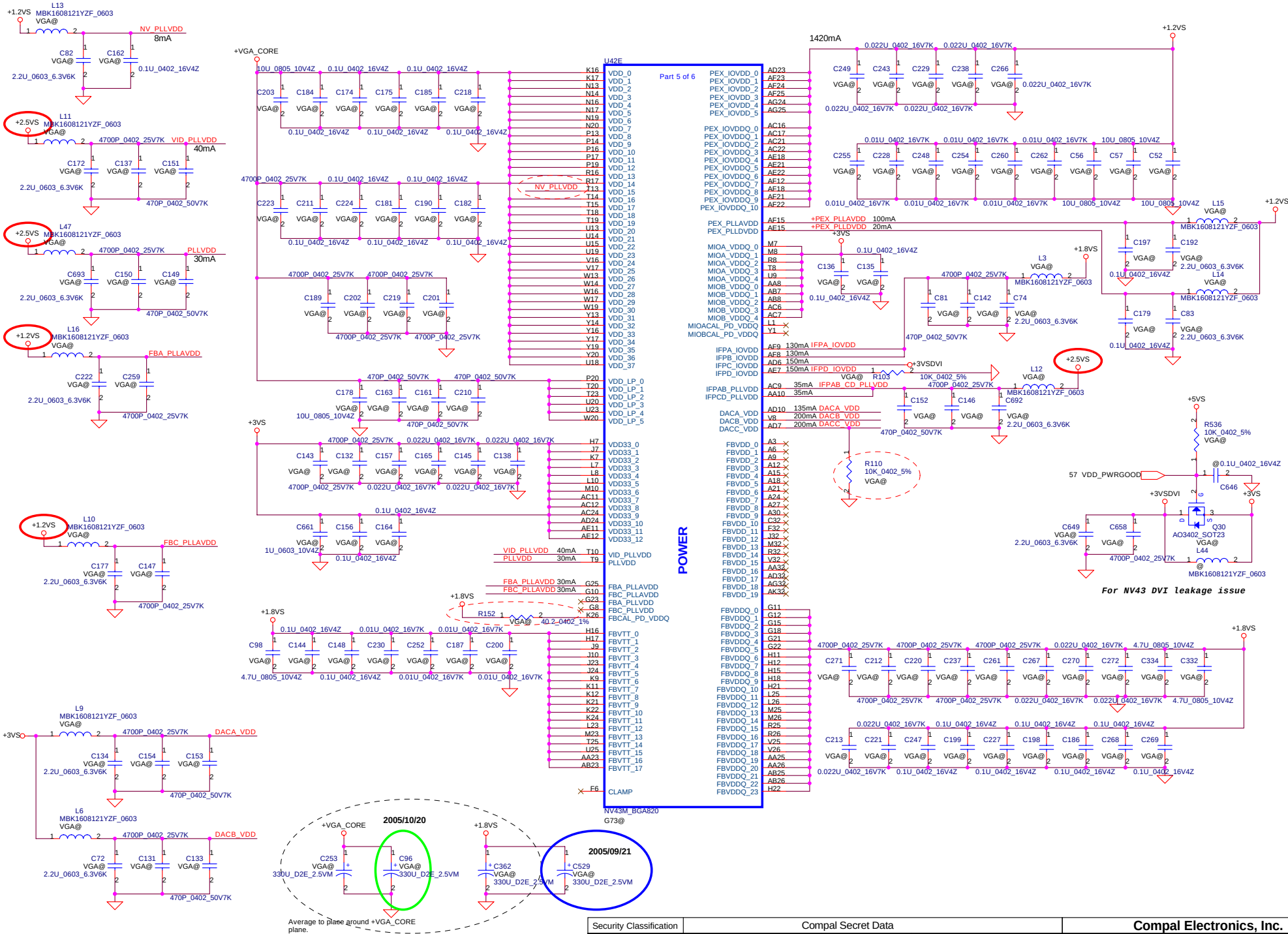
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: G72/G73 Memory

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 16 of 59



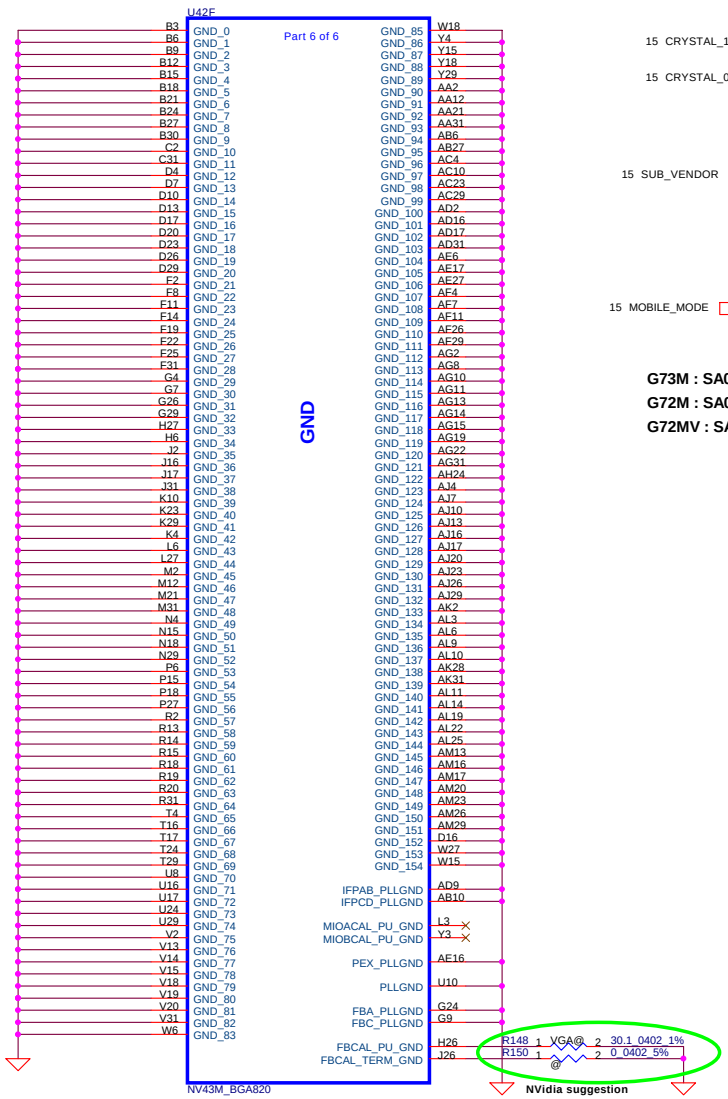
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

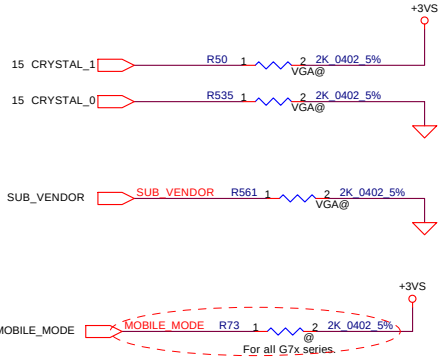
Compal Electronics, Inc.

Title: G72/G73 Power

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 17 of 59





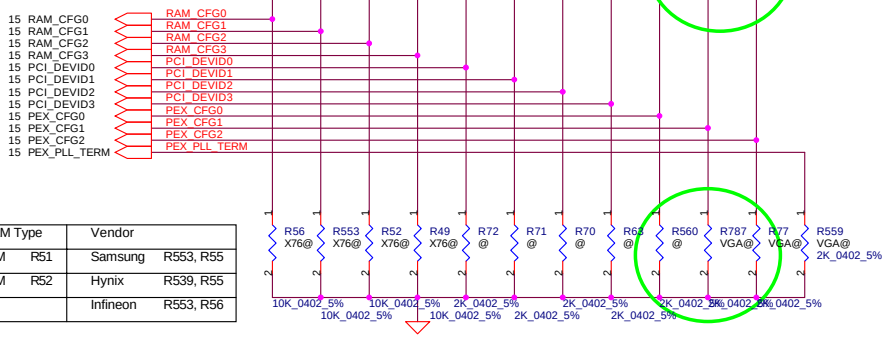
G73M : SA00000QZ00
G72M : SA00000QY00
G72MV : SA00000QY20

STRAPS	PIN	DESCRIPTION	Value	Value
CRYSTAL[1:0]	MIOBD[6,2]	27MHz=10, 14.318MHz=01, 13.5MHz=00	10	
ROM_TYPE[1:0]	MIOBD [11:10]	Parallel=00, SERIAL M25P10=01, Serial SST45VF=10	01	
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
PEX_CFG[2:0]	MIOAD [9,8,6]	Recommended for G7x	010	
RAM_CFG[3:0]	MIOAD[5:2]	16Mx16x4 1.8V (128bit G73M)	0001	Samsung
		16Mx16x4 1.8V (128bit G73M)	0011	Hynix
		16Mx16x4 1.8V (64bit G73M)	1001	Samsung
		16Mx16x4 1.8V (64bit G73M)	1011	Hynix
		16Mx16x4 1.8V (64bit G72MV)	0001	Samsung
		16Mx16x4 1.8V (64bit G72MV)	0011	Hynix
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxx8 G72M-0x01D8	1000	
		G72MV-0x01D7 TBD/TBD	0111	
MOBILE_MODE	MIOBD7	For NV44M/G7x		0

RAM_CFG[1:0]
(Manufacture)
(01=Sam, 10=Inf, 11=Hyn)

RAM_CFG[2] (0=16M or 1=32M)

RAM_CFG[3] (Bandwidth 0=Full, 1=Half)



Bandwidth		RAM Type		Vendor	
FULL	R49	32M	R51	Samsung	R553, R55
HALF	R48	16M	R52	Hynix	R539, R55
				Infineon	R553, R56

Package		
(10*12.5)	Infineon GDDR2(400): SA00000S800 (HYB18T256161AFL-25)	Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)
(11*13)	Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)	Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)
(8*13)	Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)	Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)

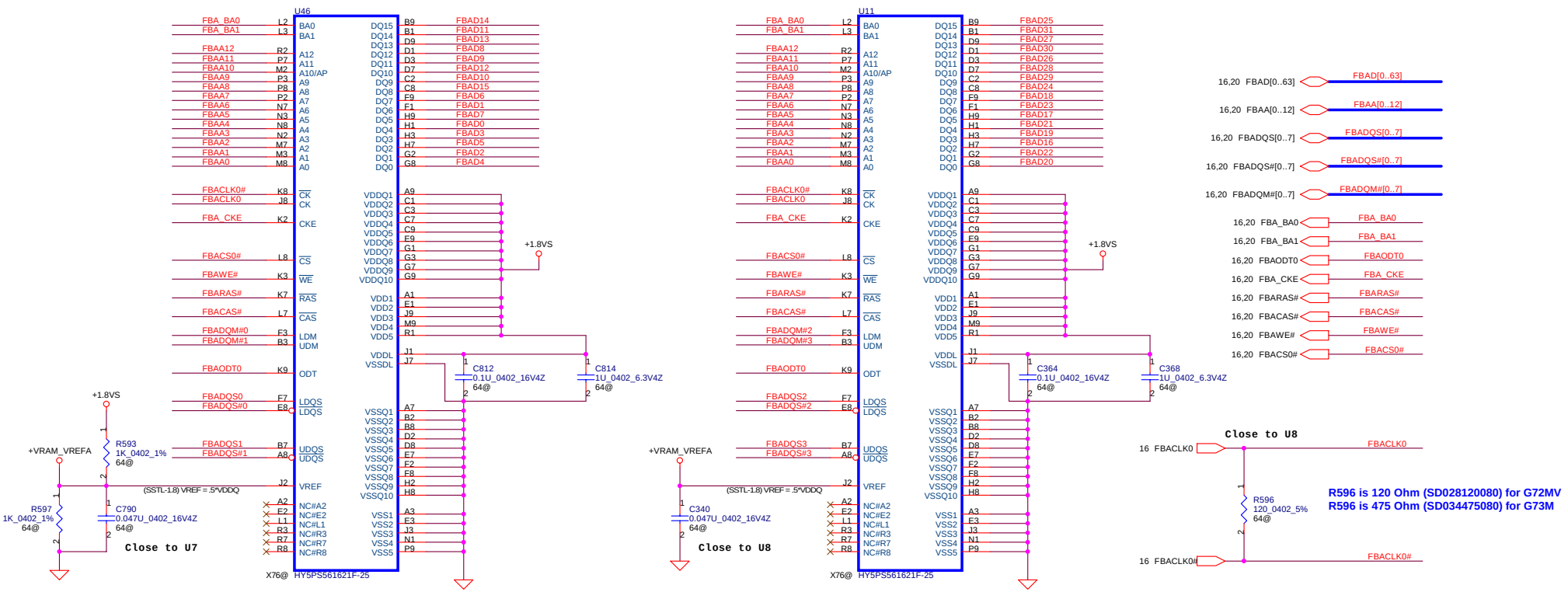
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: G72/G73 GND & STRAP

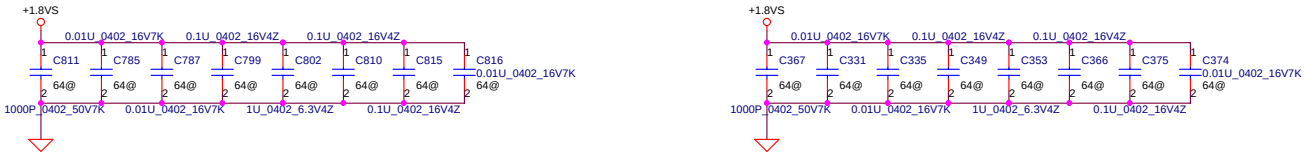
Size: B | Document Number: HBL50 LA-2921P | Rev: 0.3

Date: Friday, November 11, 2005 | Sheet 18 of 59



DDR2 BGA MEMORY

DDR2 BGA MEMORY



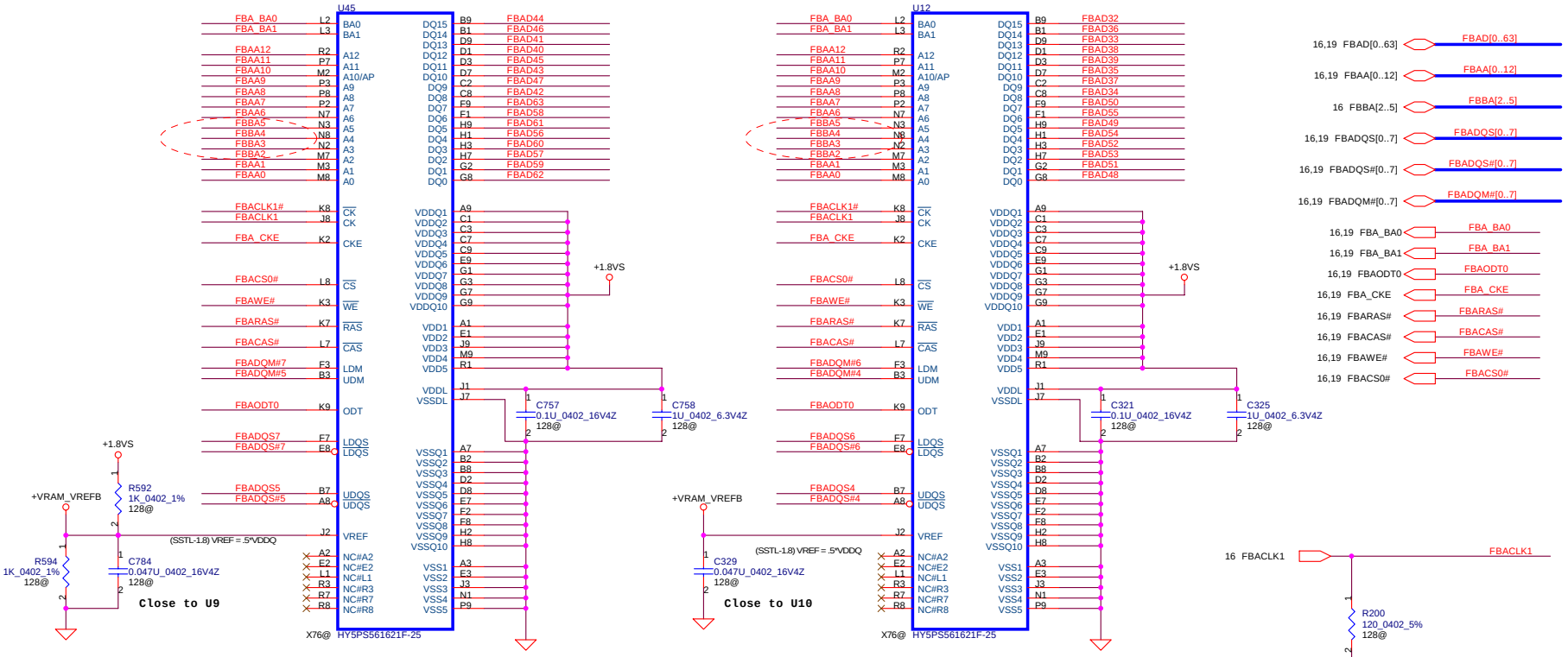
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: VRAM DDRA

Size	Document Number	Rev
Custom	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 19 of 59



DDR2 BGA MEMORY

DDR2 BGA MEMORY

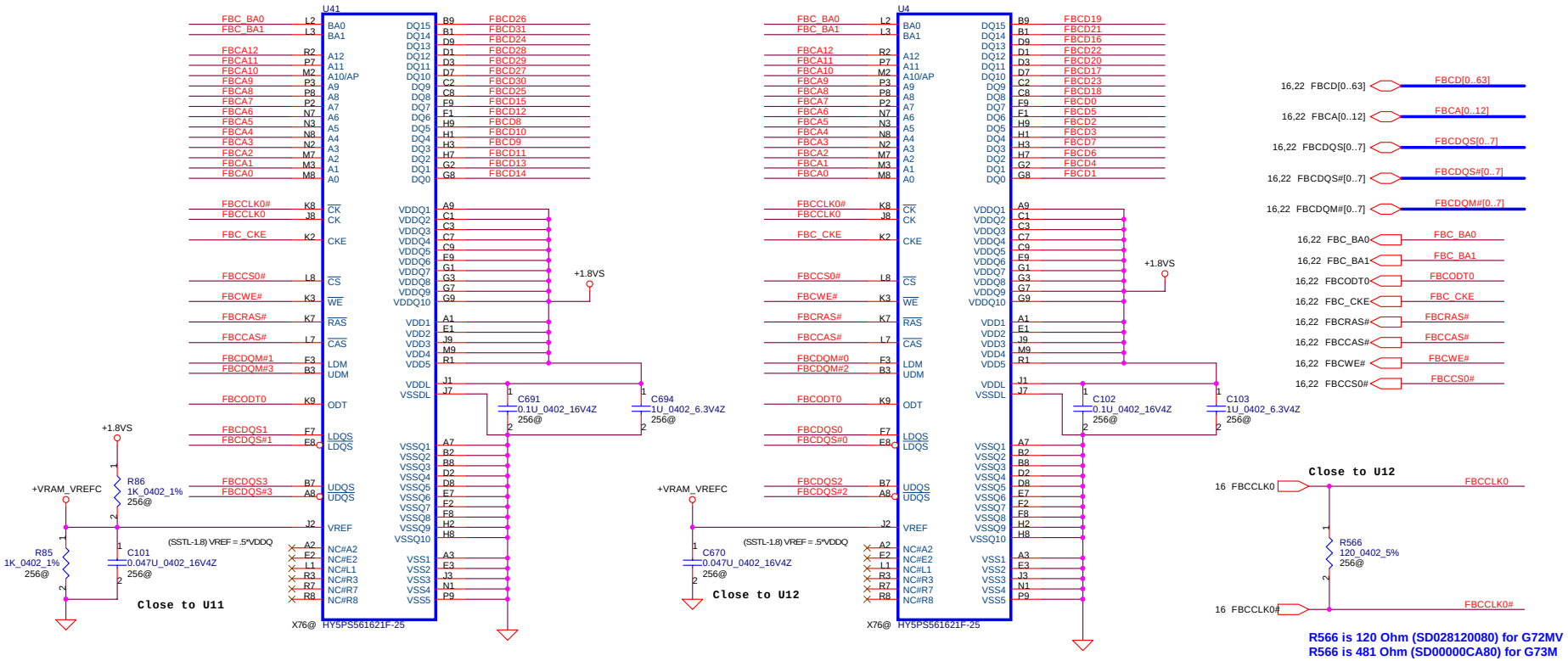
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: VRAM DDRB

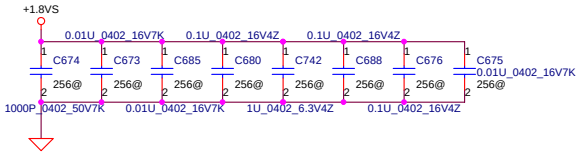
Size	Document Number	Rev
Custom	HBL50 LA-2921P	0.3

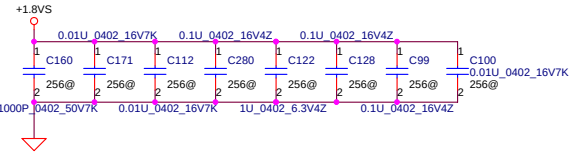
Date: Friday, November 11, 2005 Sheet 20 of 59



DDR2 BGA MEMORY

DDR2 BGA MEMORY





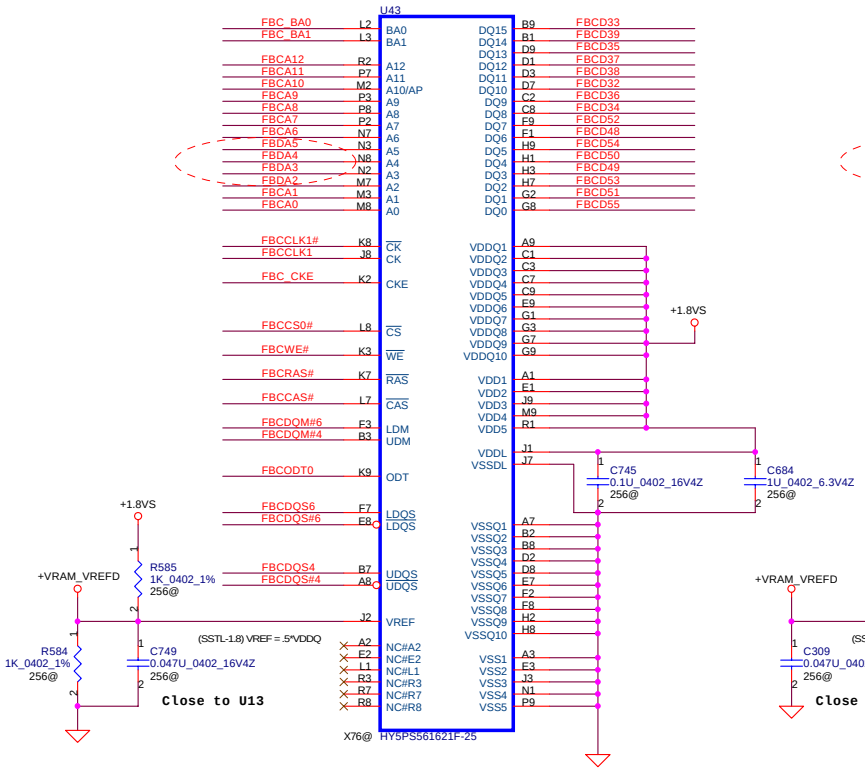
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

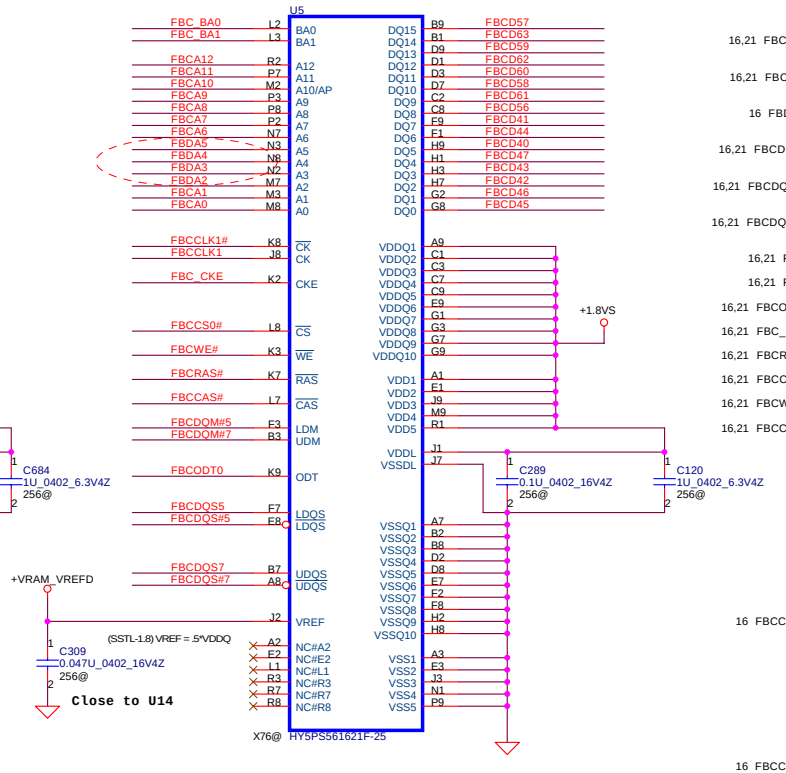
Title: VRAM DDRC

Size	Document Number	Rev
Custom	HBL50 LA-2921P	0.3

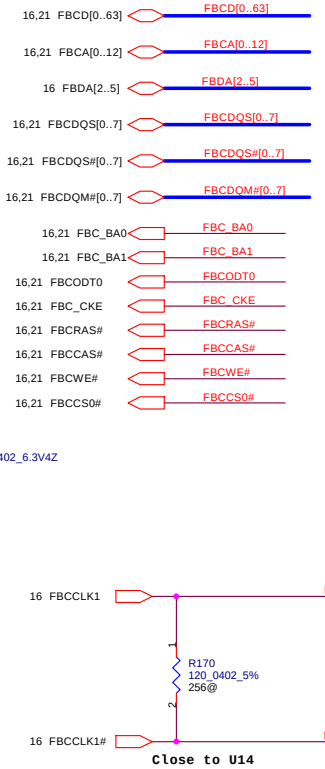
Date: Friday, November 11, 2005 Sheet 21 of 59



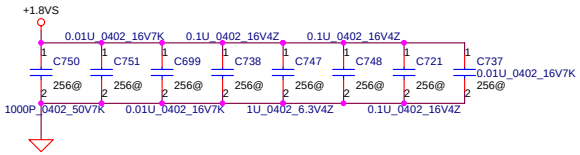
DDR2 BGA MEMORY

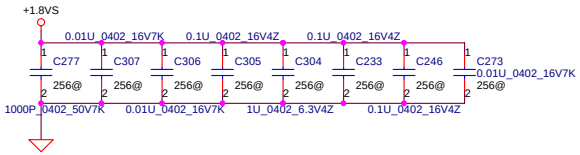


DDR2 BGA MEMORY



R170 is 120 Ohm (SD028120080) for G72MV
R170 is 481 Ohm (SD00000CA80) for G73M





Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

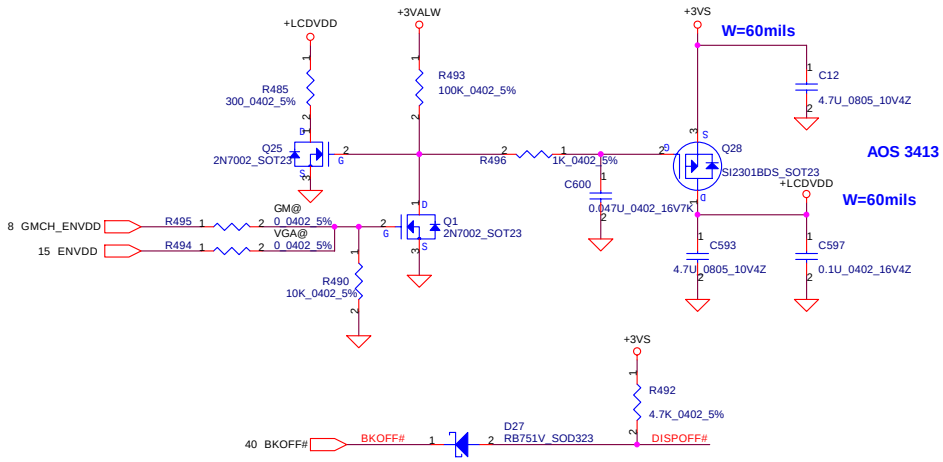
Compal Electronics, Inc.

Title: VRAM DDRD

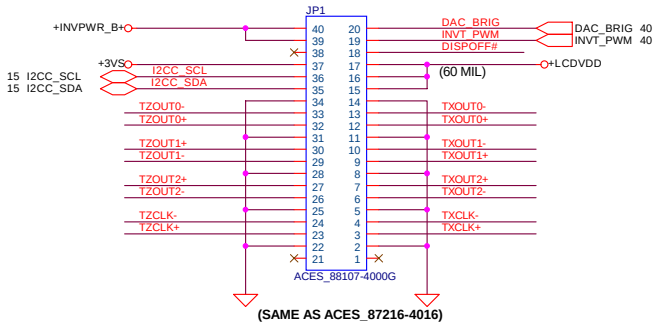
Size	Document Number	Rev
Custom	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 | Sheet 22 of 59

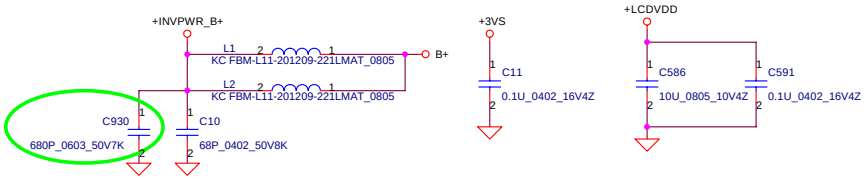
LCD POWER CIRCUIT

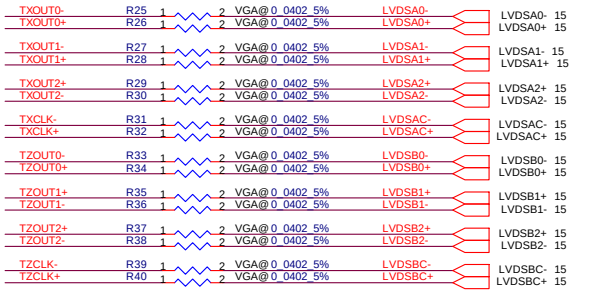


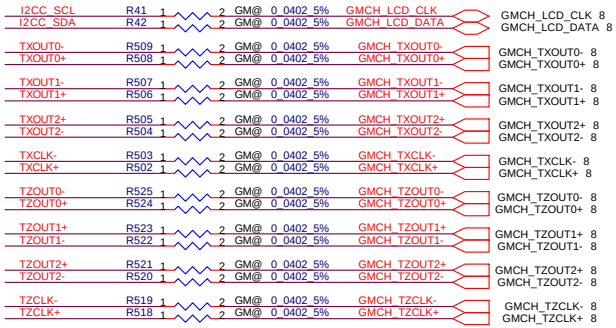
LCD/PANEL BD. Conn.



(SAME AS ACES_87216-4016)







Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

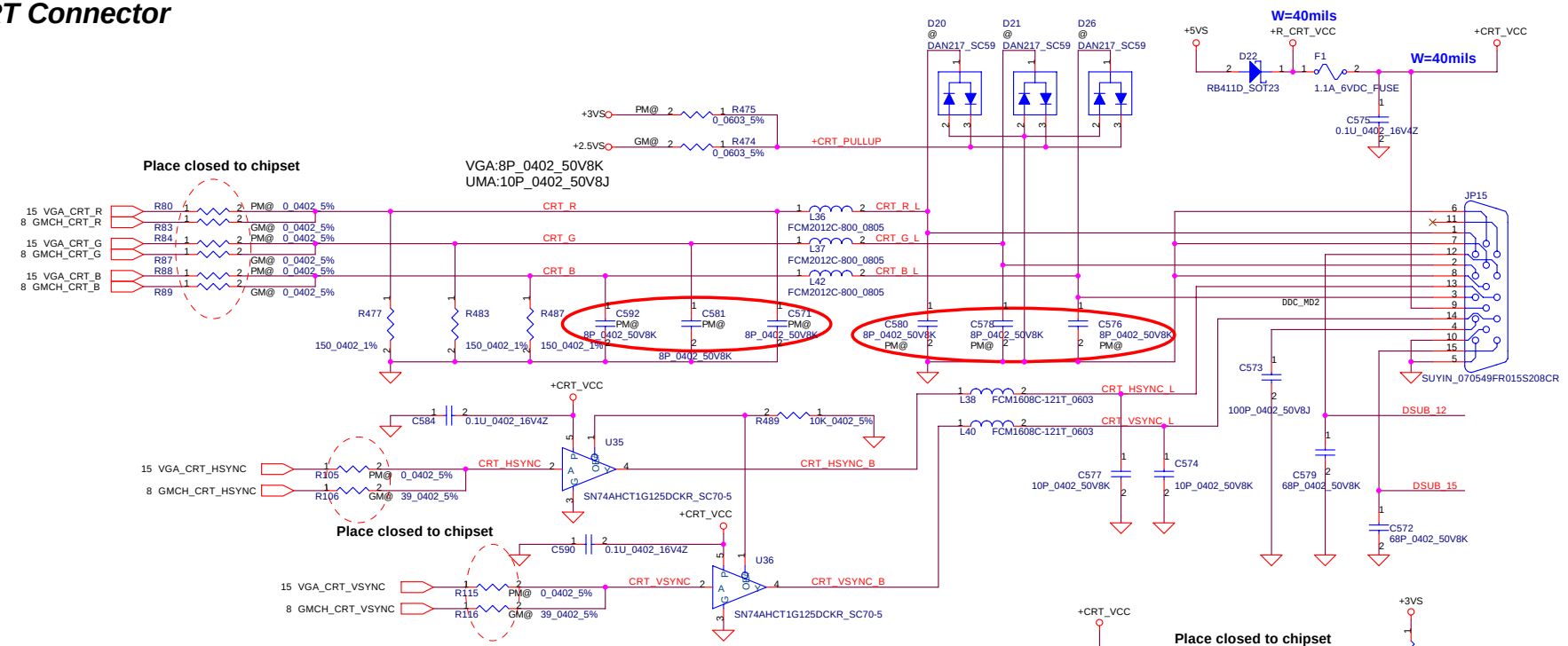
Compal Electronics, Inc.

Title: LCD Connector

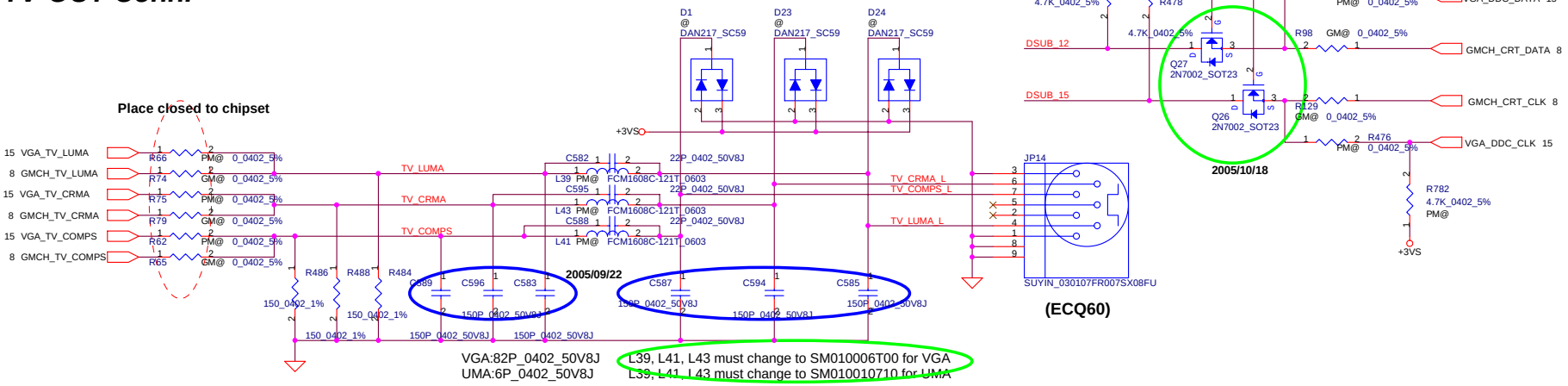
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 23 of 59

CRT Connector



TV-OUT Conn.



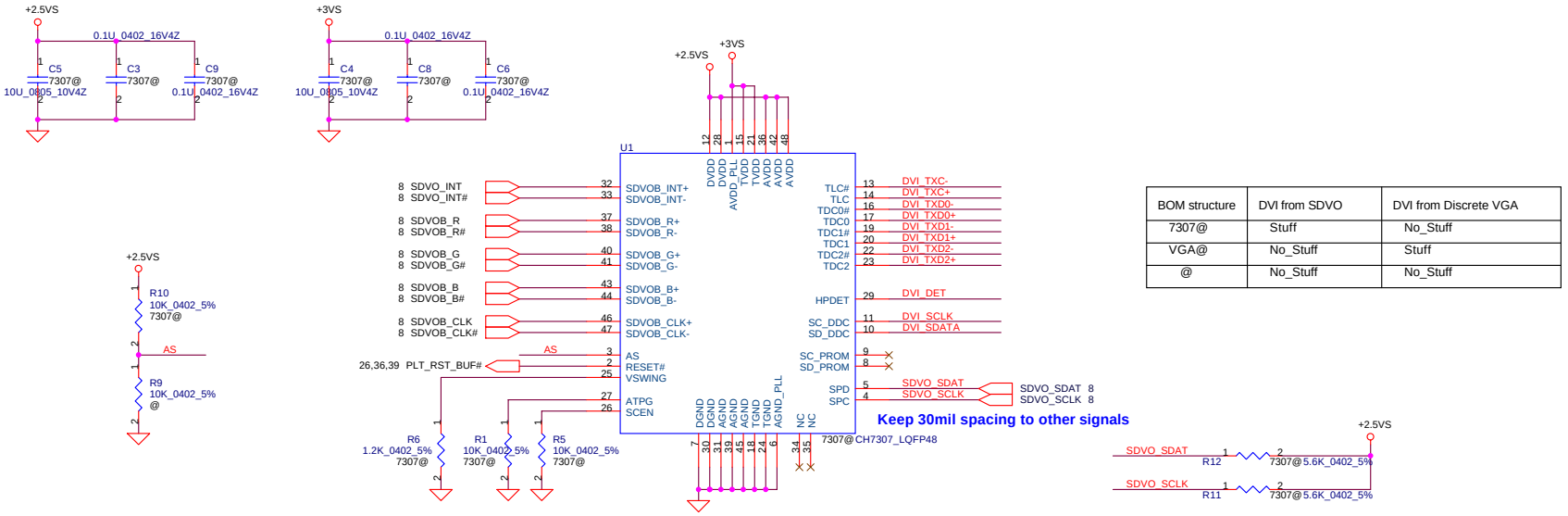
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

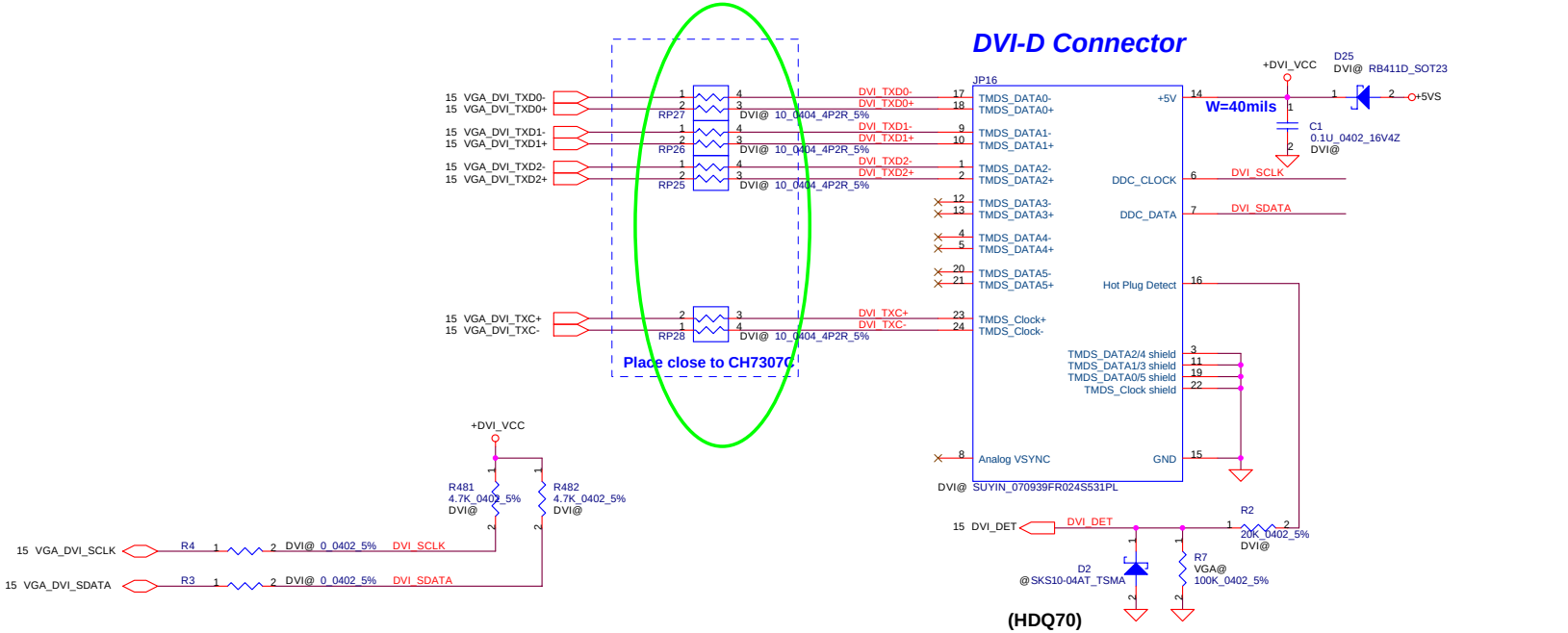
Title: CRT & TV-OUT Connector

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 24 of 59



BOM structure	DVI from SDVO	DVI from Discrete VGA
7307@	Stuff	No_Stuff
VGA@	No_Stuff	Stuff
@	No_Stuff	No_Stuff



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

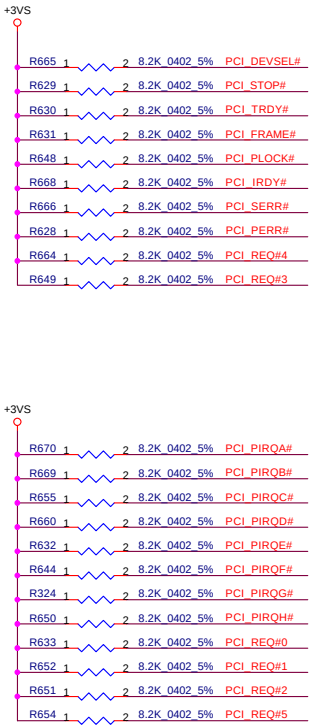
Compal Electronics, Inc.

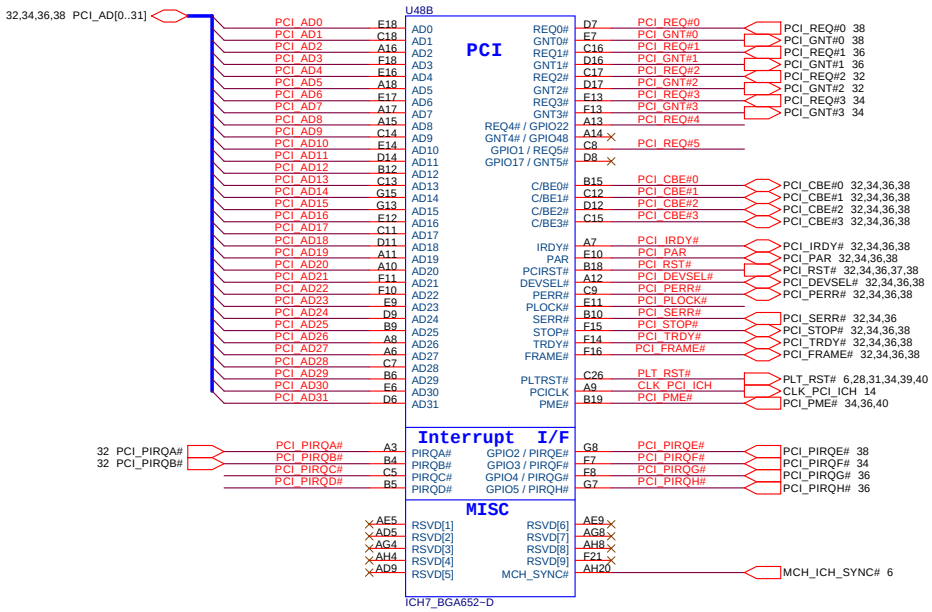
Title: CH7307 & DVI-D Connector

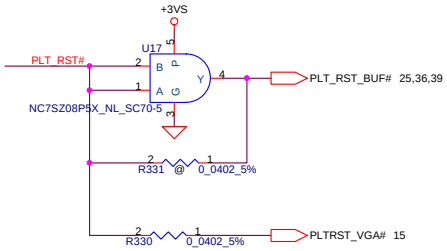
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

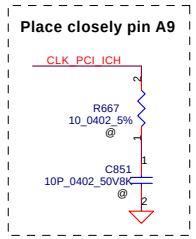
Date: Friday, November 11, 2005 Sheet 25 of 59

ICH7M(B-0)(QK65)[QS]:SA00000V160
ICH7M-DH(B-0)(QK17)[QS]:SA00000JK60









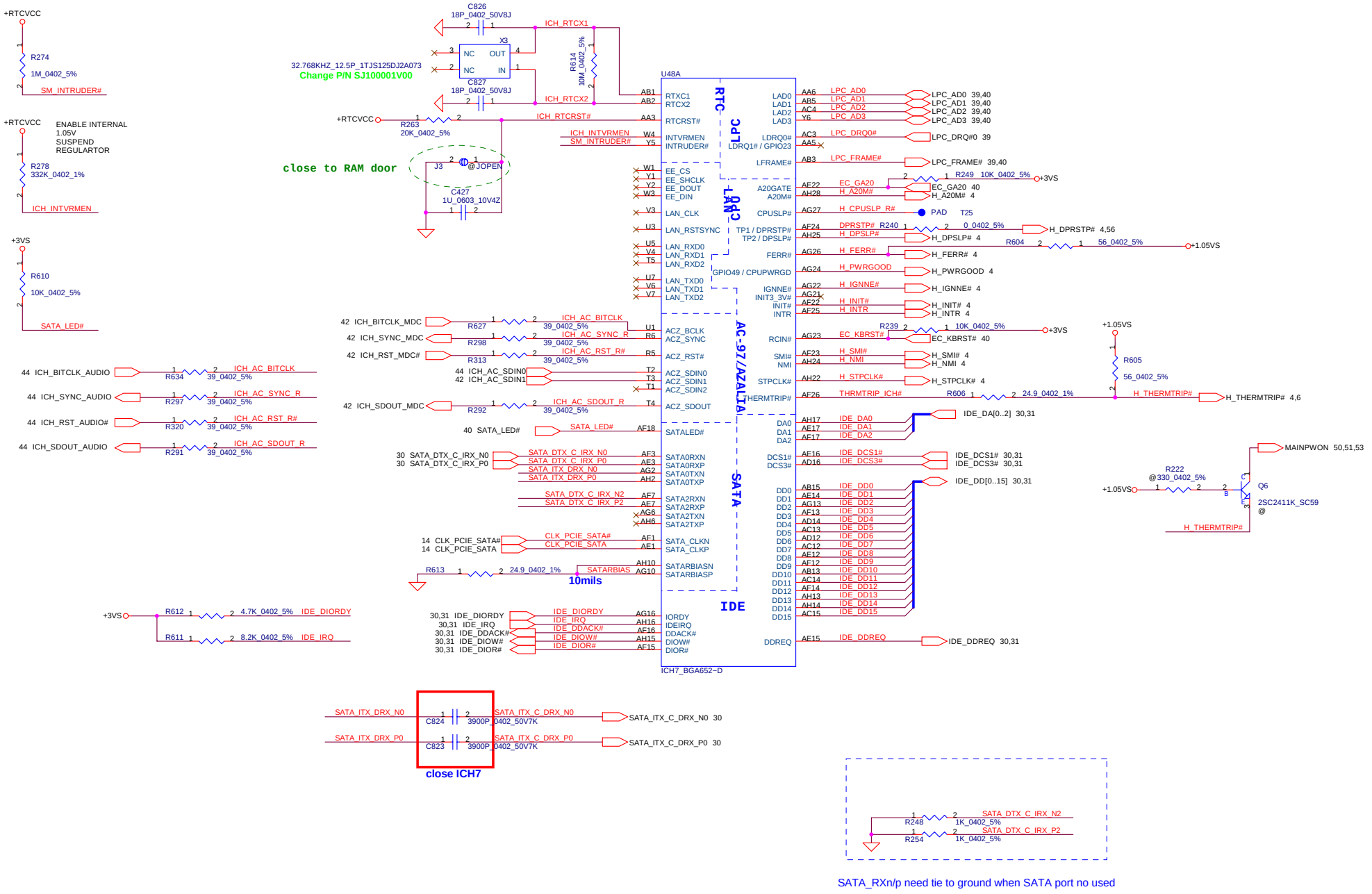
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: ICH7-M(1/4)

Size | Document Number: HBL50 LA-2921P | Rev: 0.3

Date: Friday, November 11, 2005 | Sheet 26 of 59



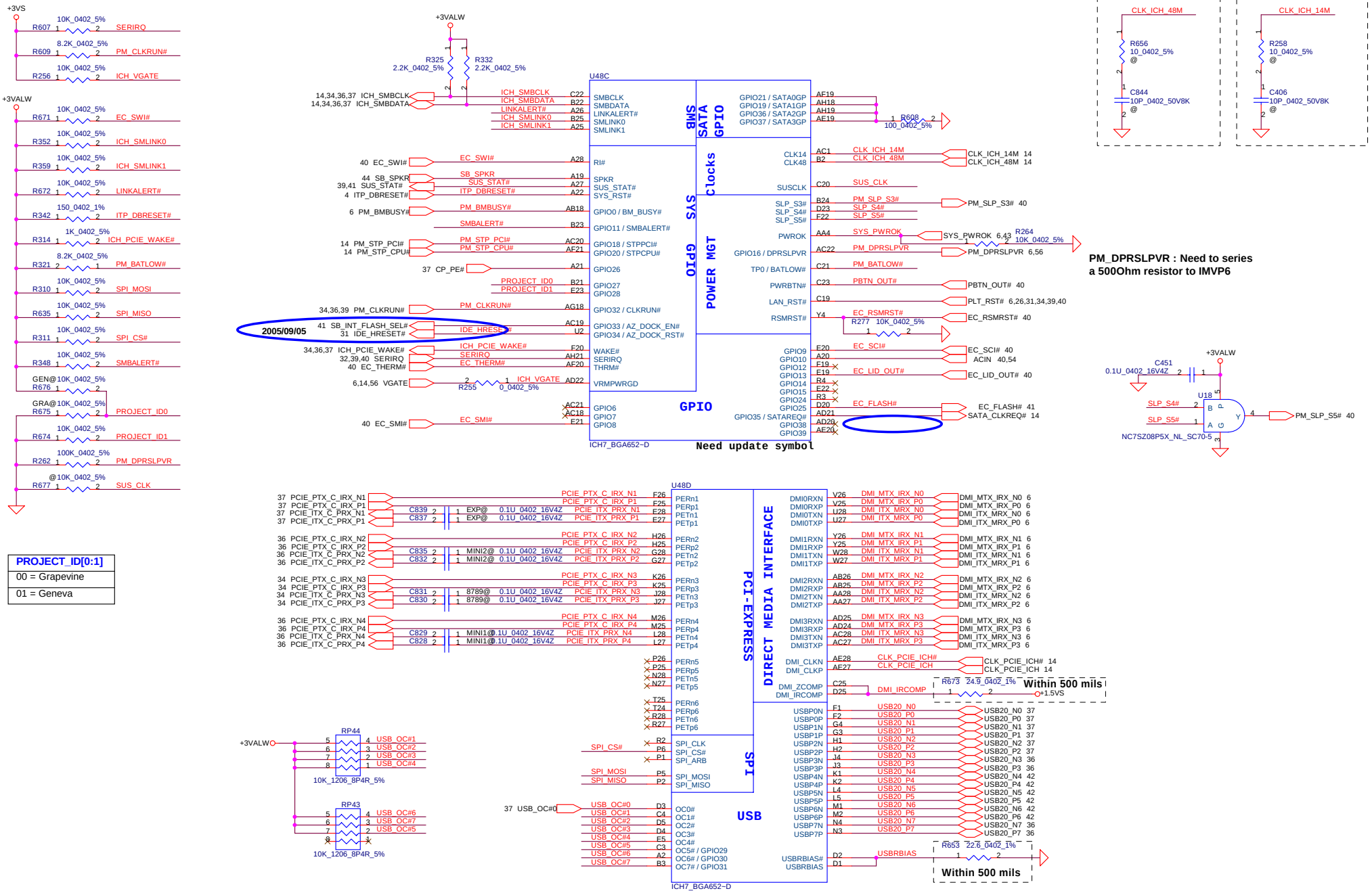
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: **ICH7-M(2/4)**

Size	Document Number	Rev
Custom	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 27 of 59



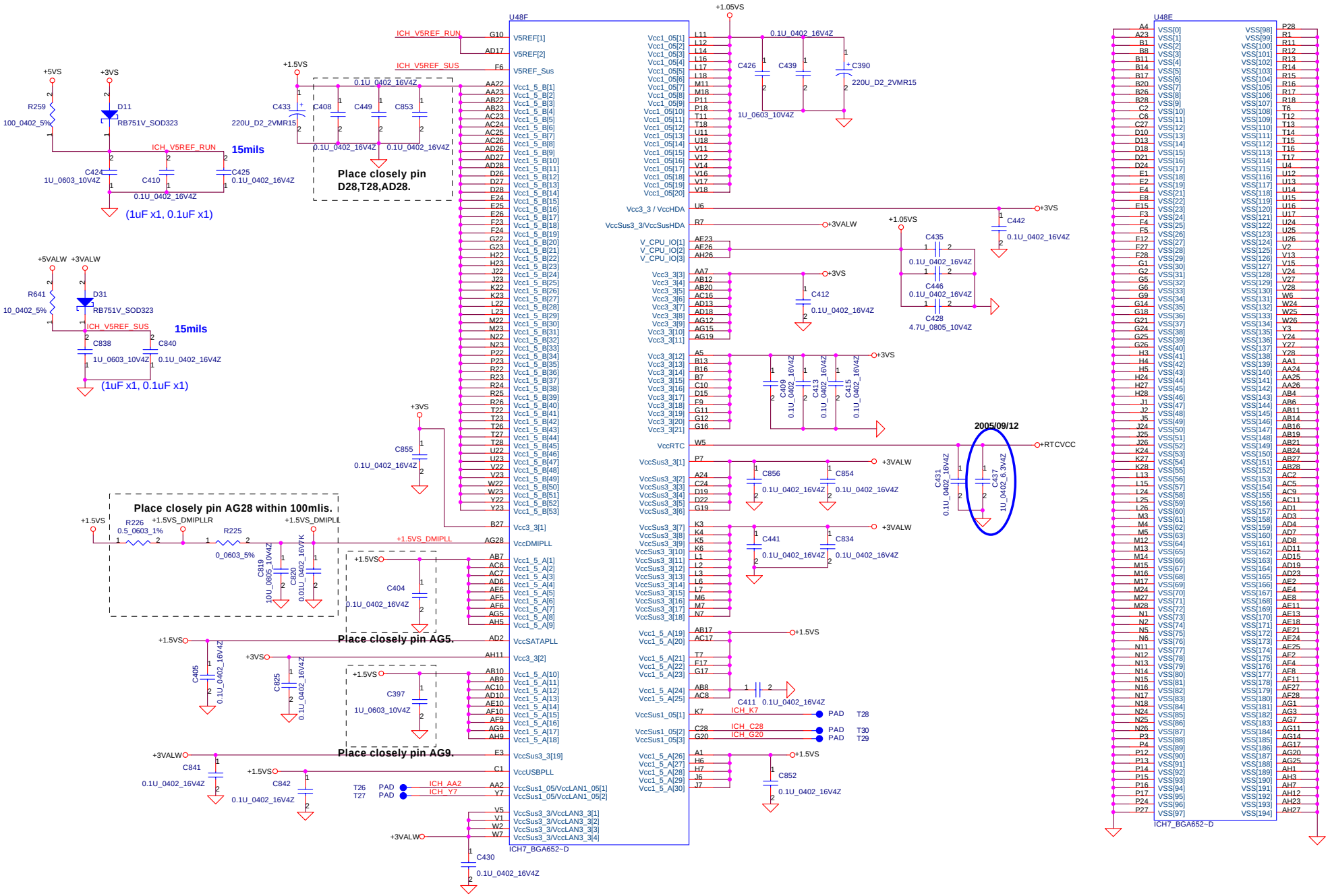
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: ICH7-M(3/4)

Size	Document Number	Rev
Custom	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 28 of 59



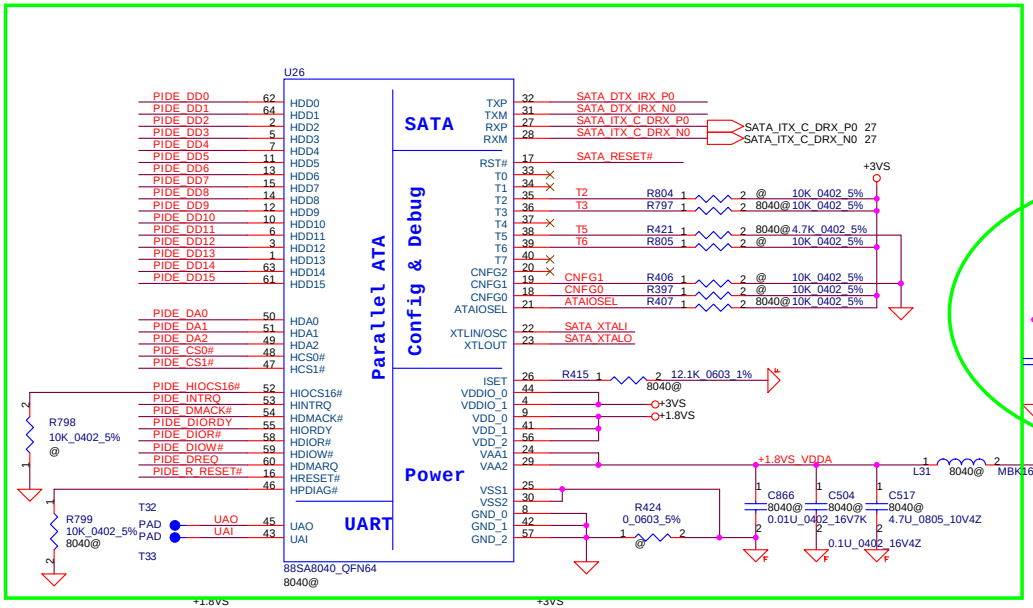
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

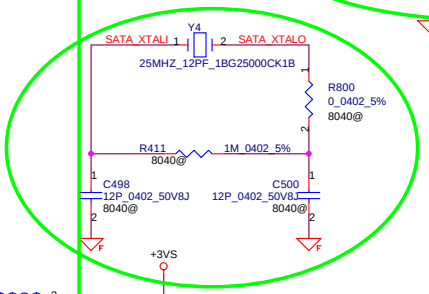
Compal Electronics, Inc.

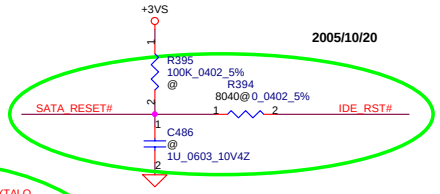
Title: **ICH7-M(4/4)**

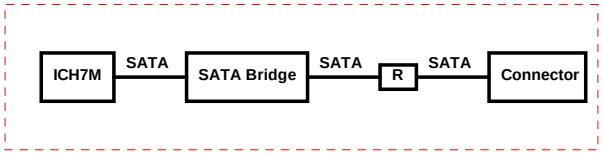
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

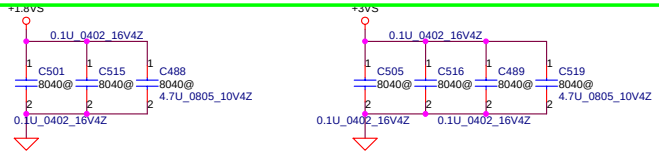
Date: Friday, November 11, 2005 | Sheet 29 of 59

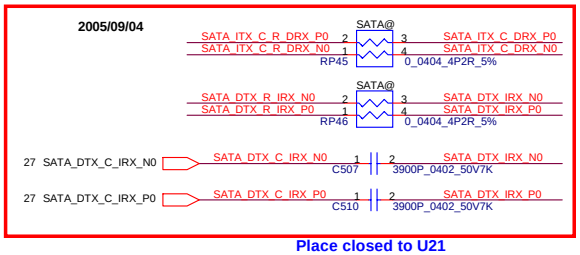


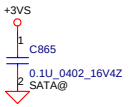




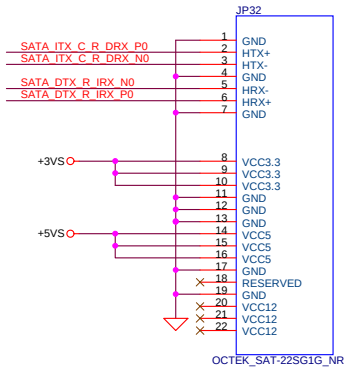






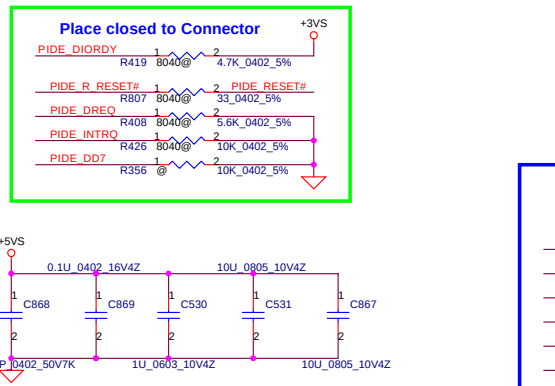


SATA HDD Conn.

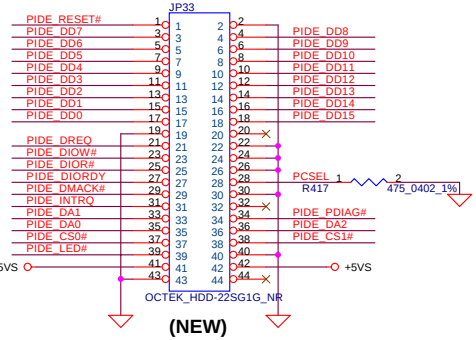


(NEW)

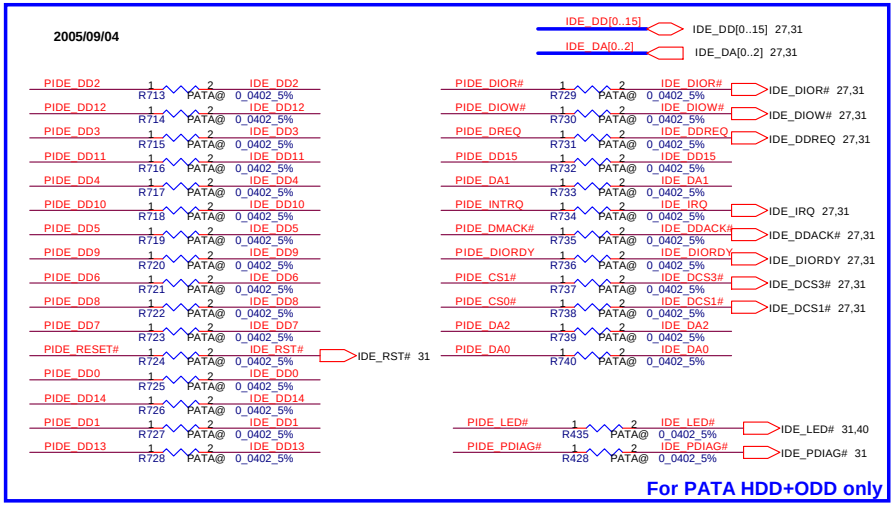
Change Library



PATA HDD Conn.



(NEW)



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

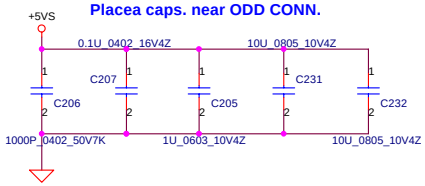
Compal Electronics, Inc.

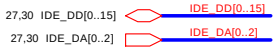
Title: SATA Bridge

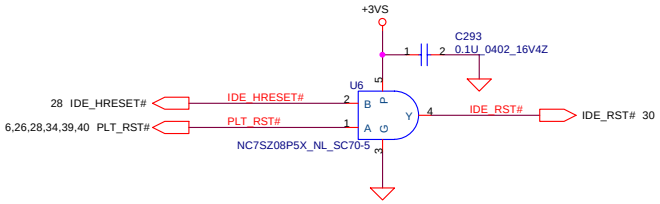
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

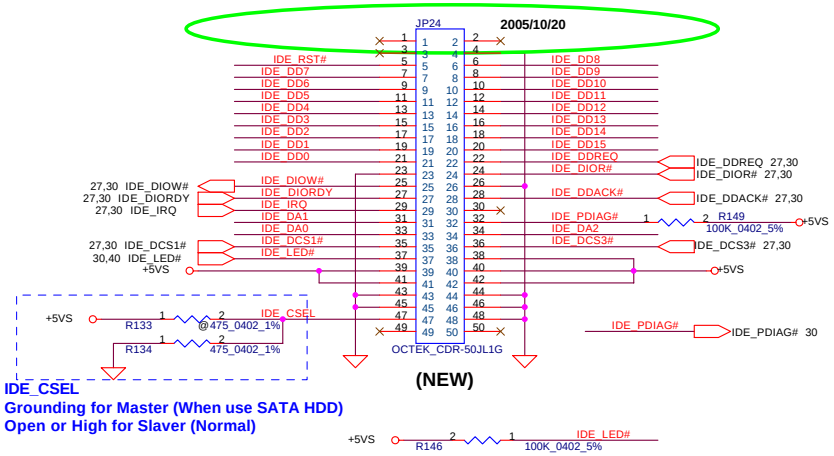
Date: Friday, November 11, 2005 Sheet 30 of 59

Placea caps. near ODD CONN.









(NEW)

IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

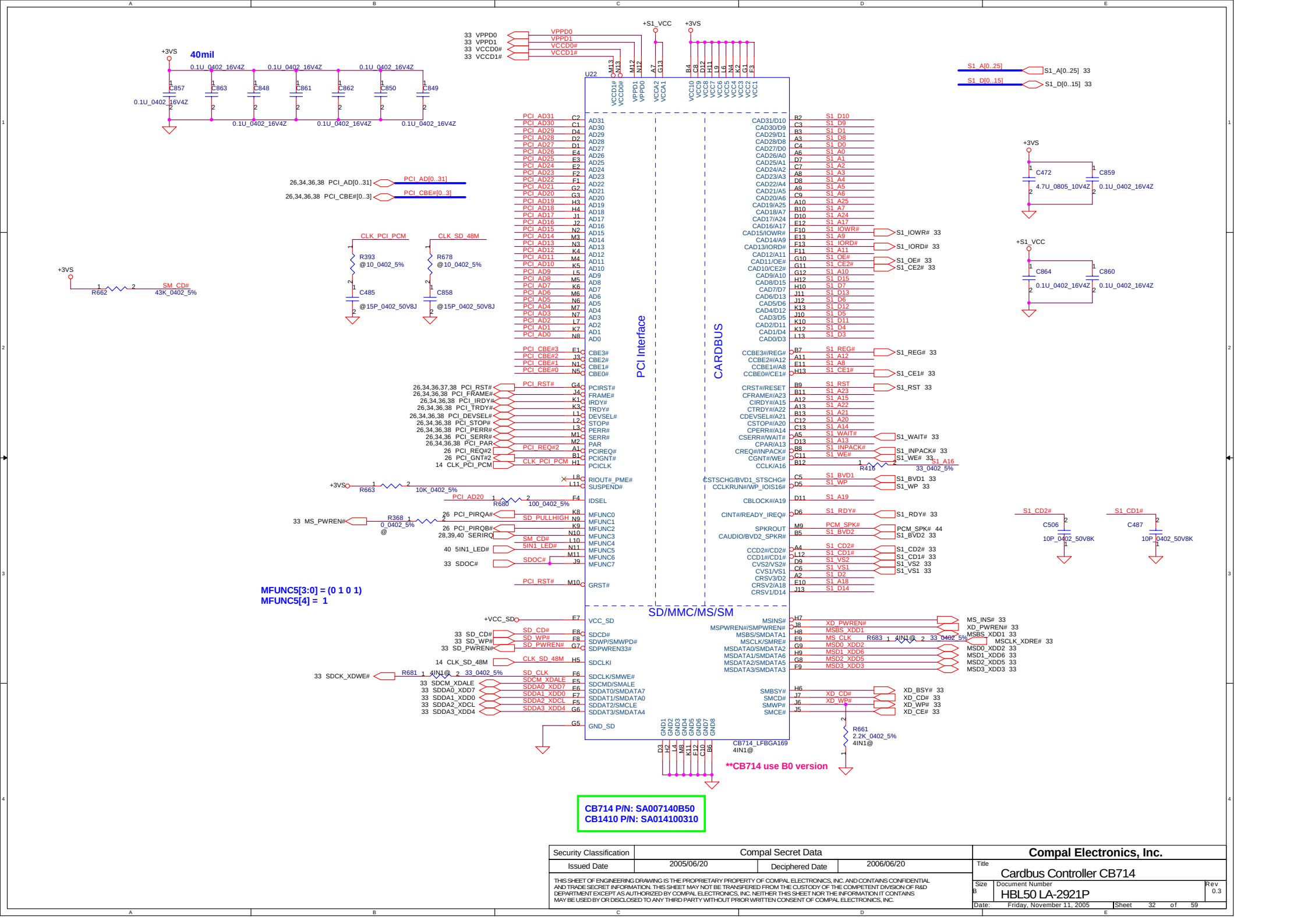
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: ODD & SATA HDD Connector

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 | Sheet 31 of 59



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

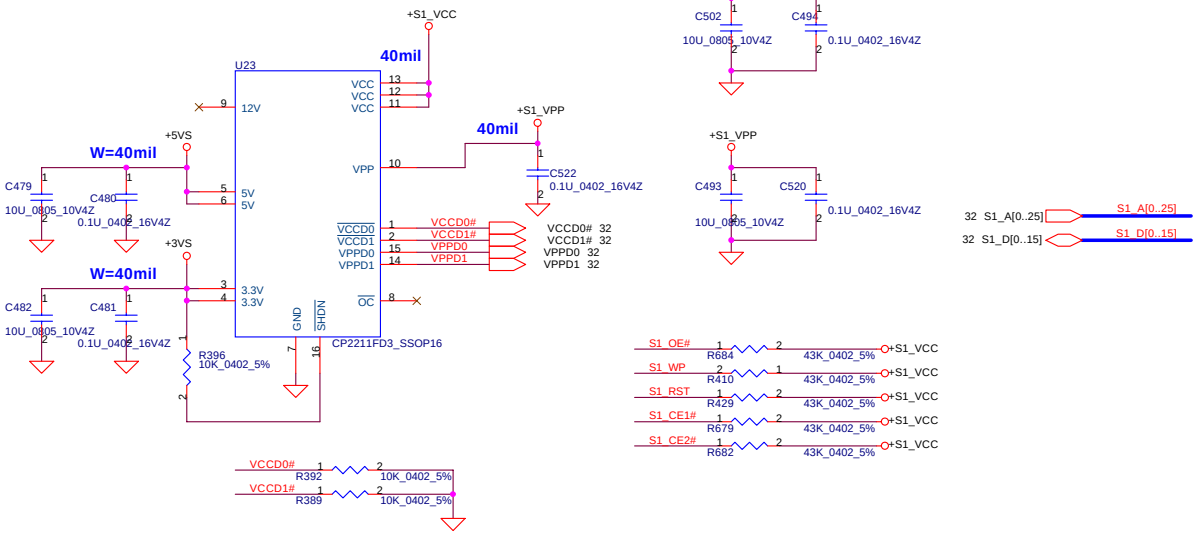
Compal Electronics, Inc.

Title: Cardbus Controller CB714

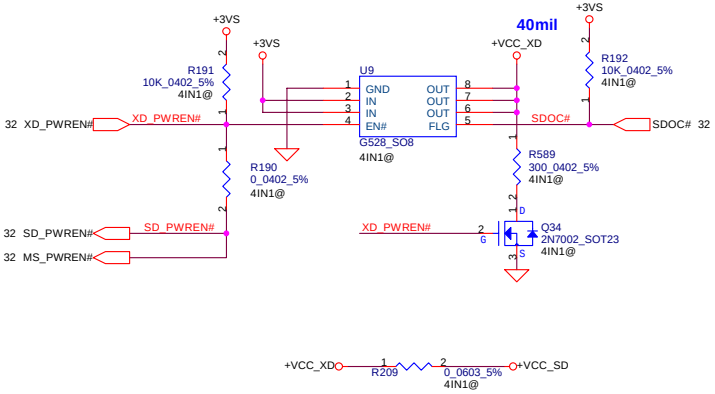
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

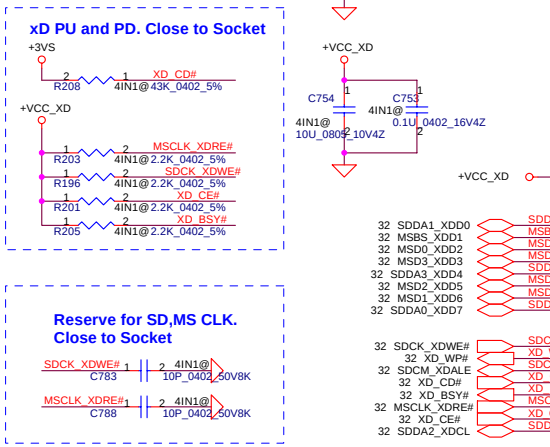
Date: Friday, November 11, 2005 Sheet 32 of 59

PCMCIA Power Control

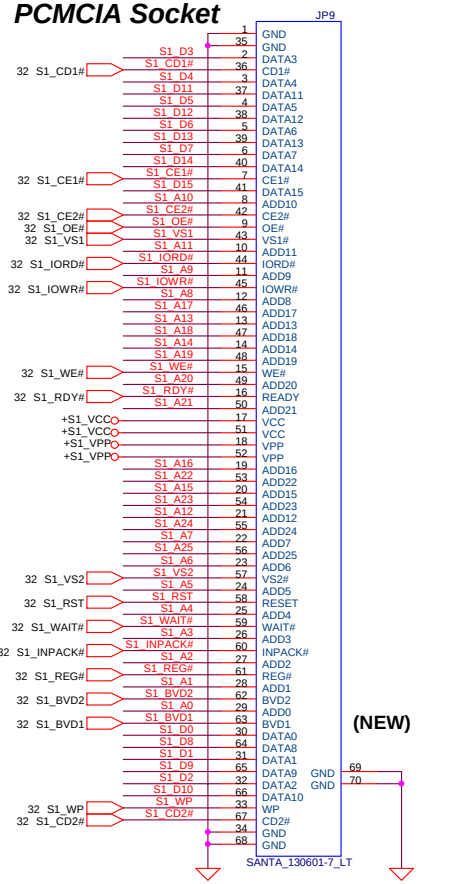


SD/MS Power Control
XD Power Control

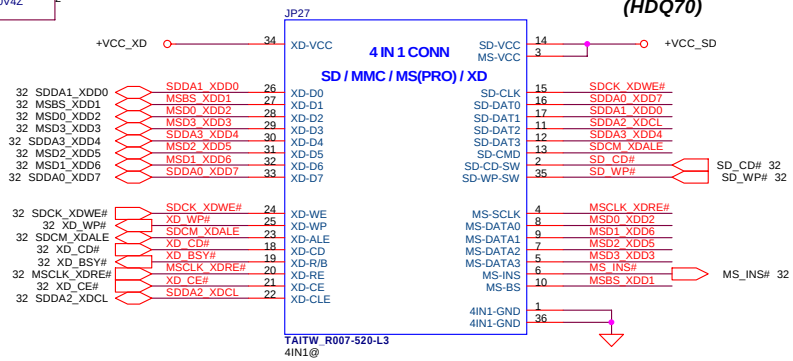




PCMCIA Socket



4 IN 1 Socket
(HDQ70)



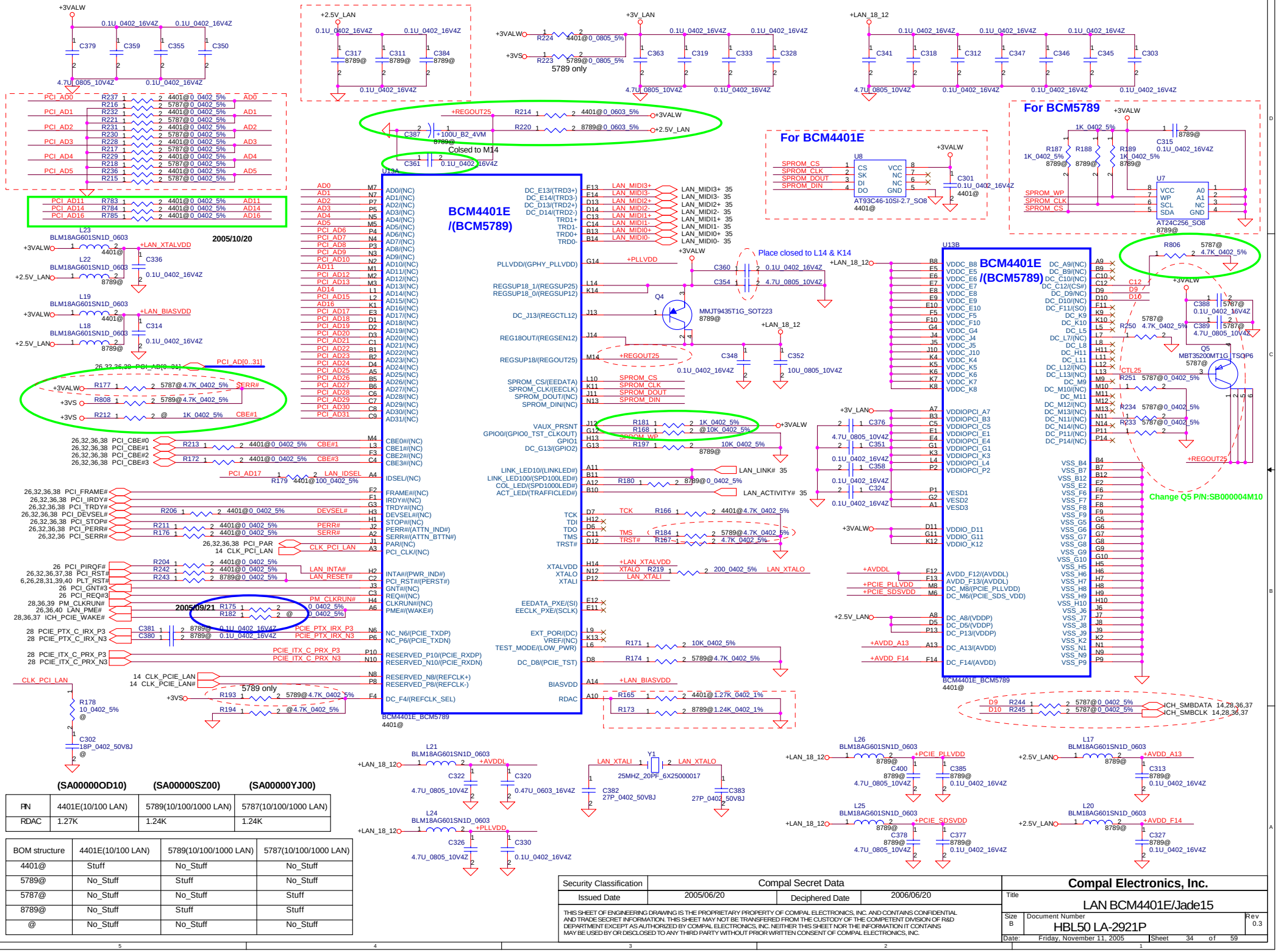
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: PCMCIA Socket

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 33 of 59



	(SA00000OD10)	(SA00000SZ00)	(SA00000YJ00)
PN	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
RDAC	1.27K	1.24K	1.24K

BOM structure	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
4401@	Stuff	No_Stuff	No_Stuff
5789@	No_Stuff	Stuff	No_Stuff
5787@	No_Stuff	No_Stuff	Stuff
8789@	No_Stuff	Stuff	Stuff
@	No_Stuff	No_Stuff	No_Stuff

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

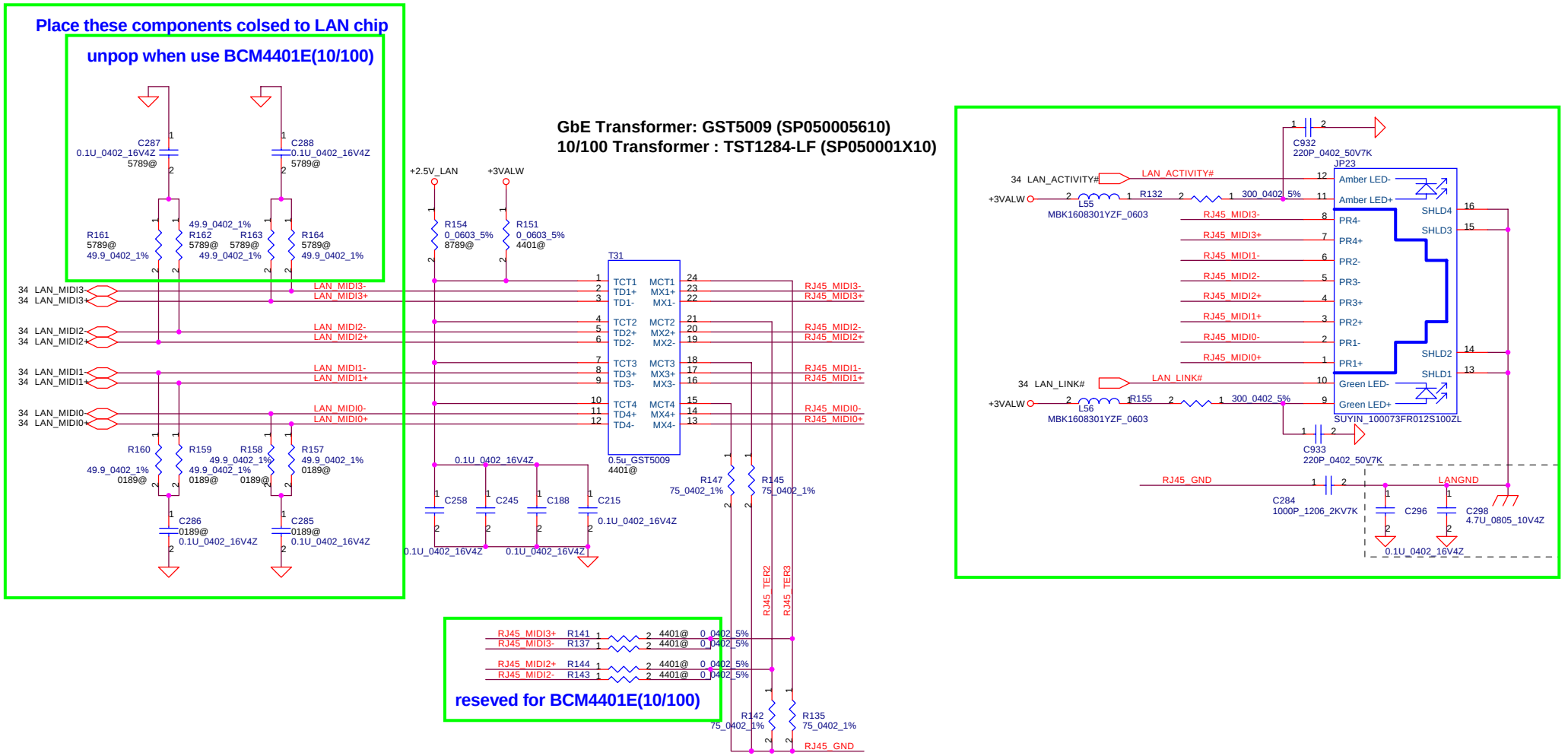
Compal Electronics, Inc.

Title: LAN BCM4401E/Jade15

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 34 of 59

LAN BCM4401E/ BCM5789



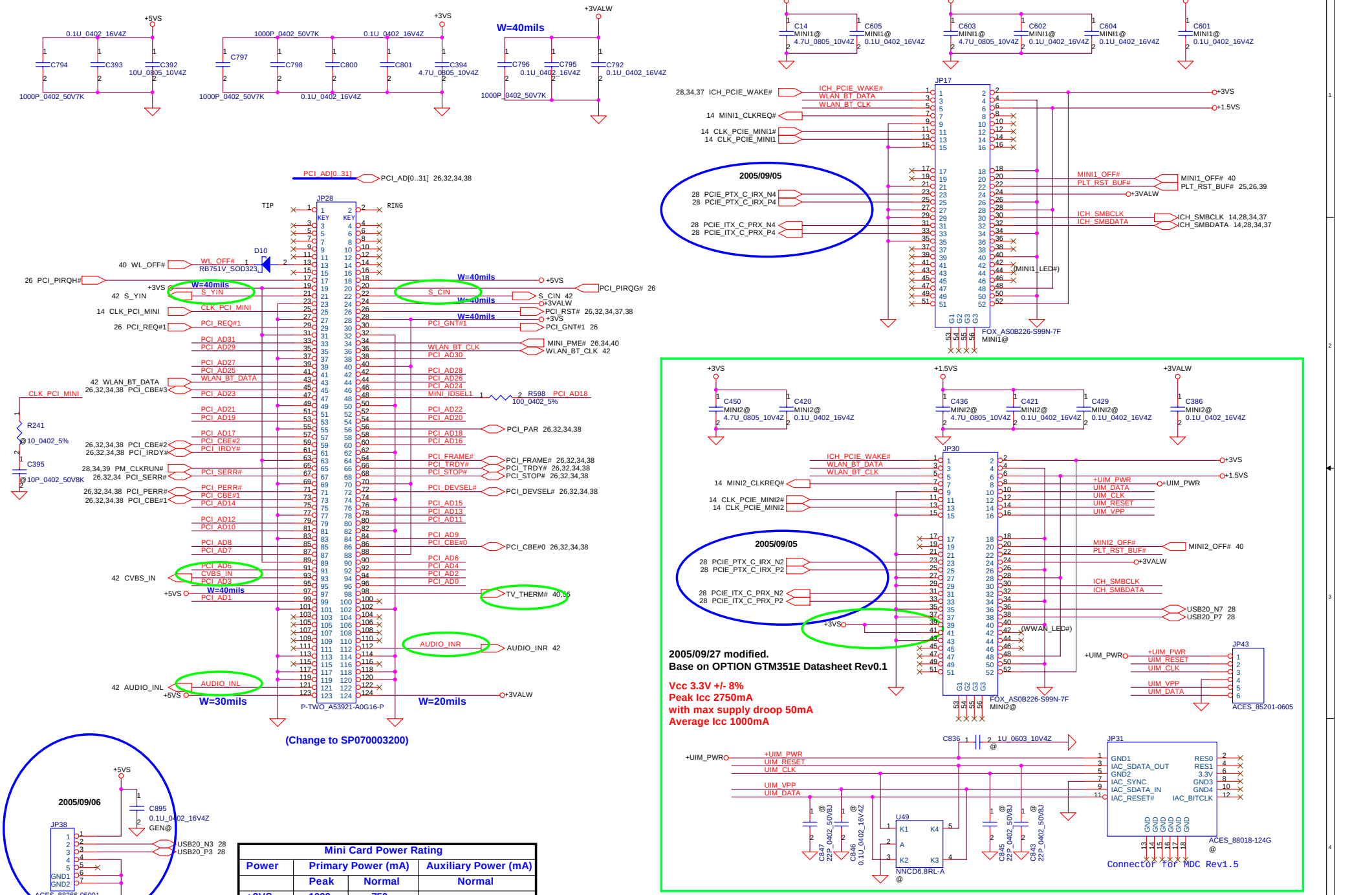
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45/RJ11

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 35 of 59



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

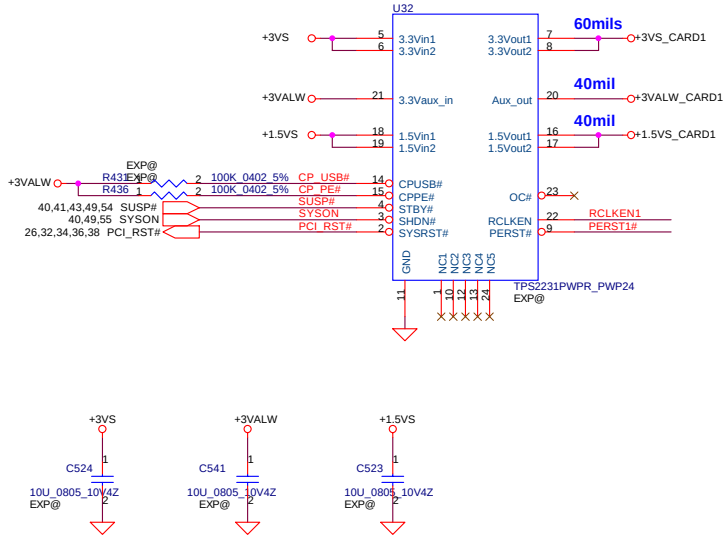
Compal Electronics, Inc.

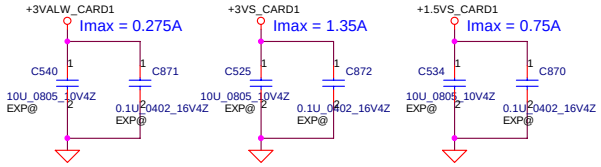
Title: MINI-PCI Slot (WLAN)

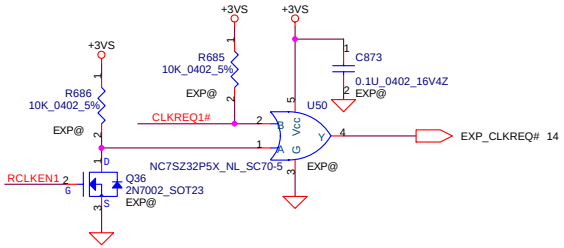
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 36 of 59

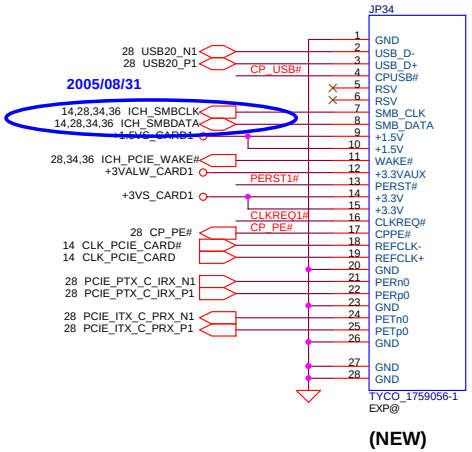
New Card Power Switch





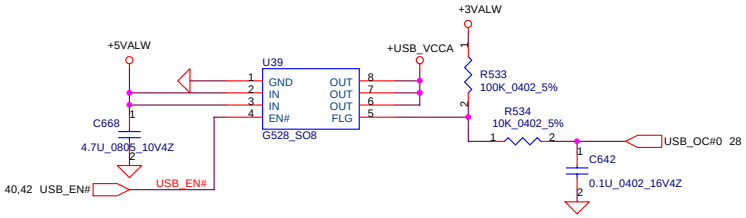


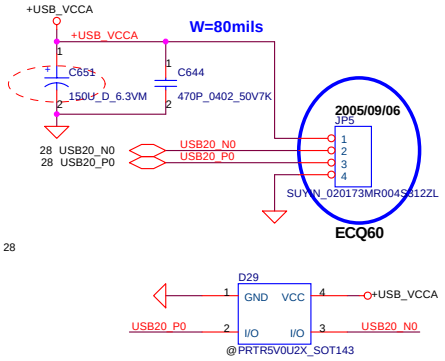
New Card Socket (Left)



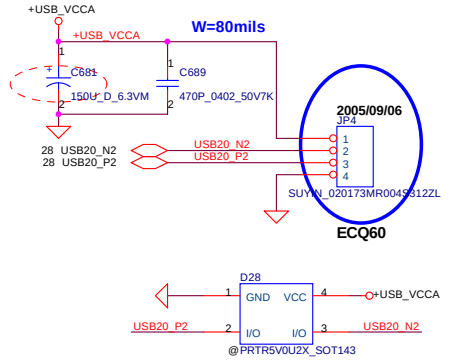
(NEW)

USB CONN. 1 & 2





SUYIN_020173MR004G533ZR_4P



SUYIN_020173MR004G533ZR_4P

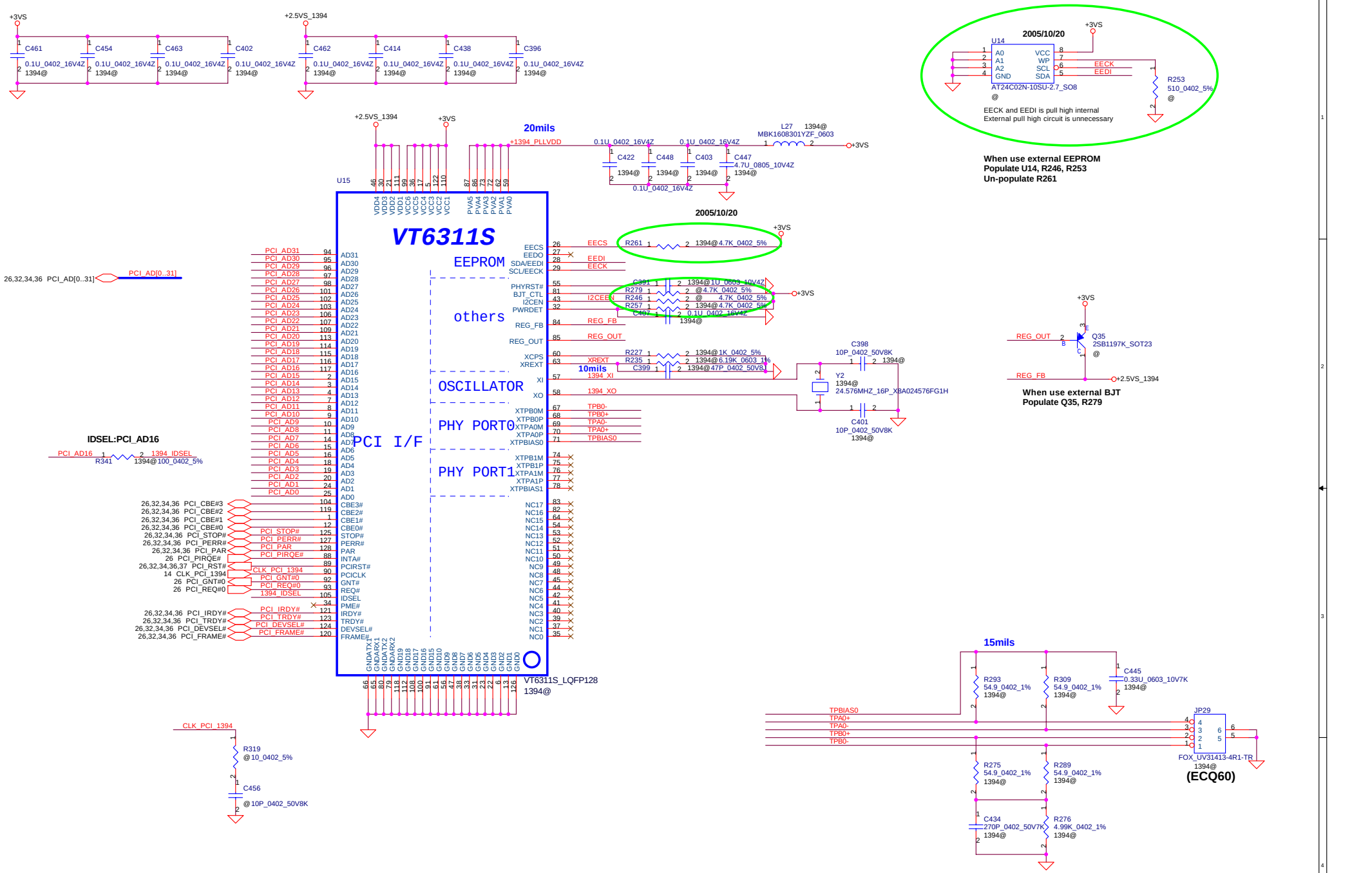
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: NEW CARD SOCKET

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 | Sheet 37 of 59



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

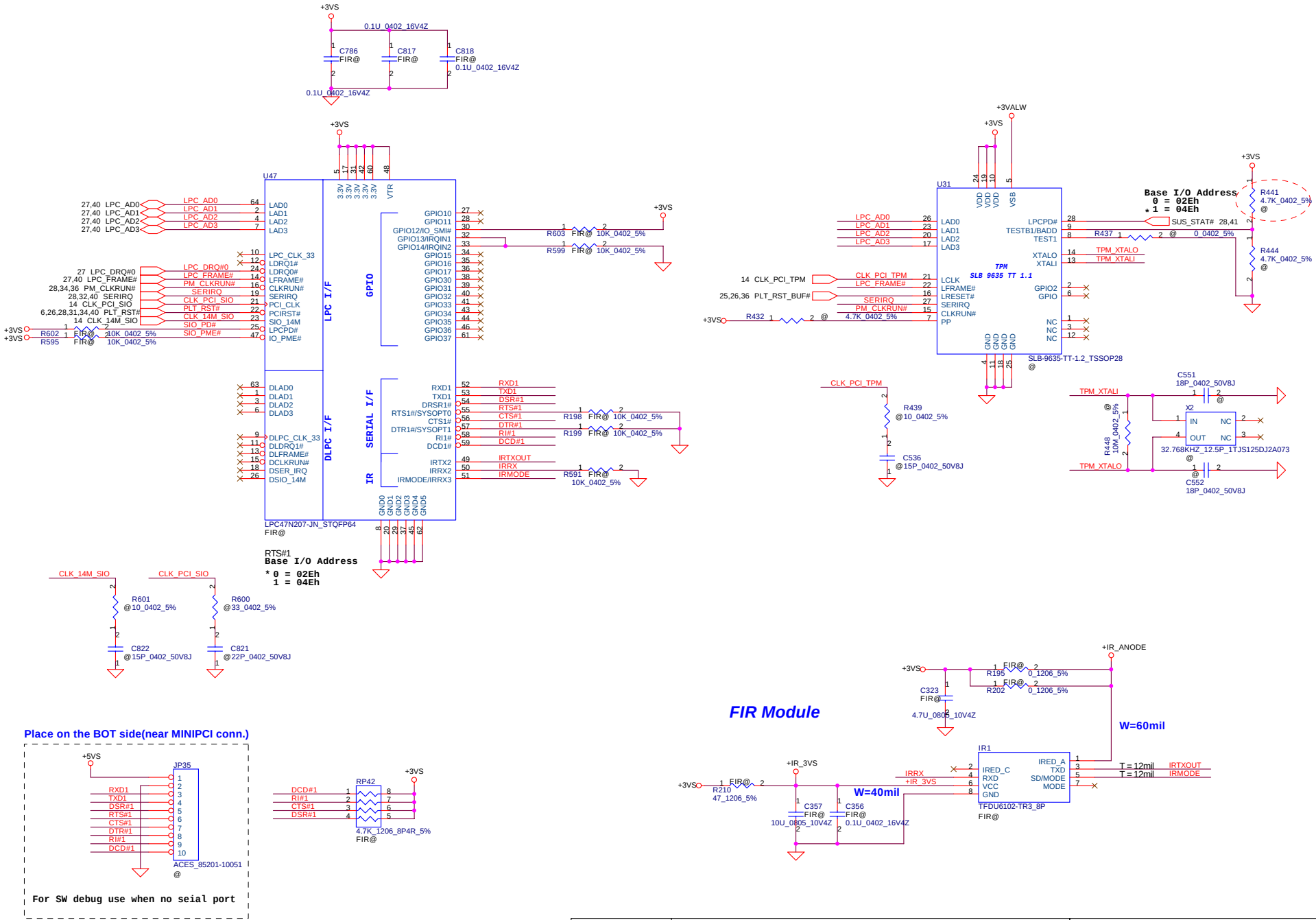
Compal Electronics, Inc.

Title: IEEE1394 VIA VT6311S

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 38 of 59

SUPER I/O SMsC LPC47N207



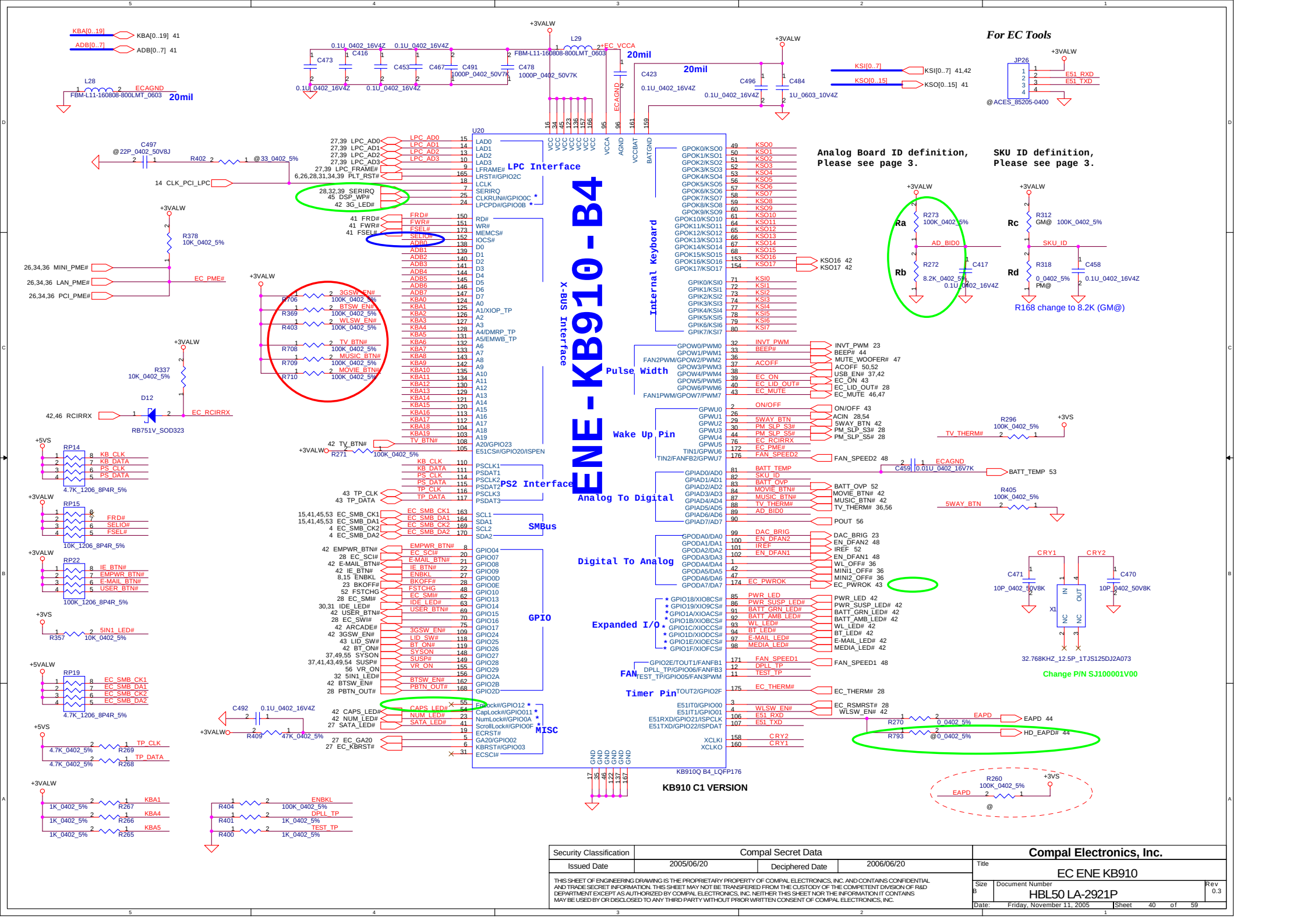
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

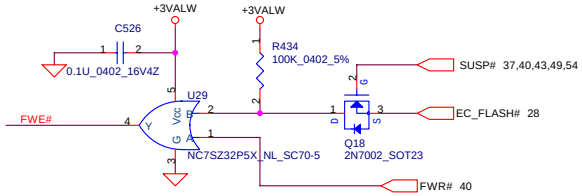
Compal Electronics, Inc.

Title: SIO1036 & FIR

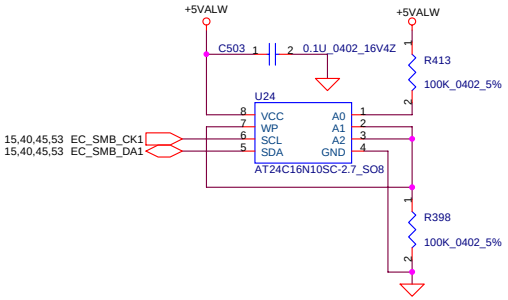
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 39 of 59

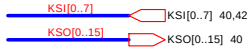

ENE-KB910-B4
KB910 C1 VERSION
KB910Q B4_LQFP176
LPC Interface
PS2 Interface
SMBus
GPIO
MISC
X-BUS Interface
Internal Keyboard
Pulse Width
Wake Up Pin
Analog To Digital
Digital To Analog
Expanded I/O
FAN
Timer Pin
For EC Tools
Analog Board ID definition, Please see page 3.
SKU ID definition, Please see page 3.
R168 change to 8.2K (GM@)
Change P/N SJ100001V00
32.768KHZ_12.5P_1TJS125DJ2A073
RB751V_SOD323
20mil
Security Classification
Compal Secret Data
Issued Date
2005/06/20
Deciphered Date
2006/06/20
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
EC ENE KB910
Size
B
Document Number
HBL50 LA-2921P
Rev
0.3
Date:
Friday, November 11, 2005
Sheet
40
of
59

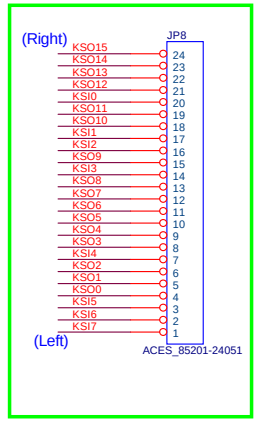


Check PCB Footprint

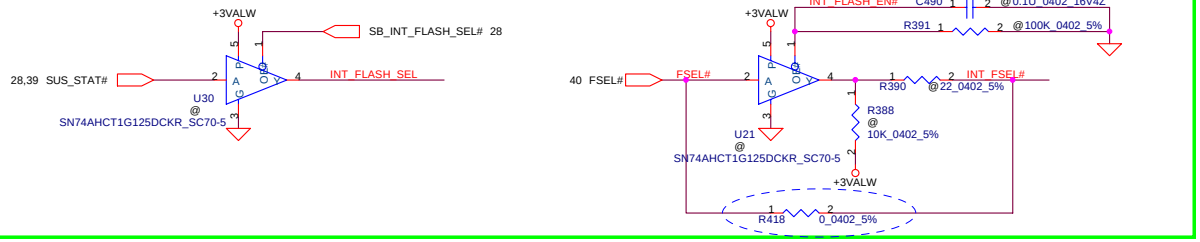


INT_KBD Conn.

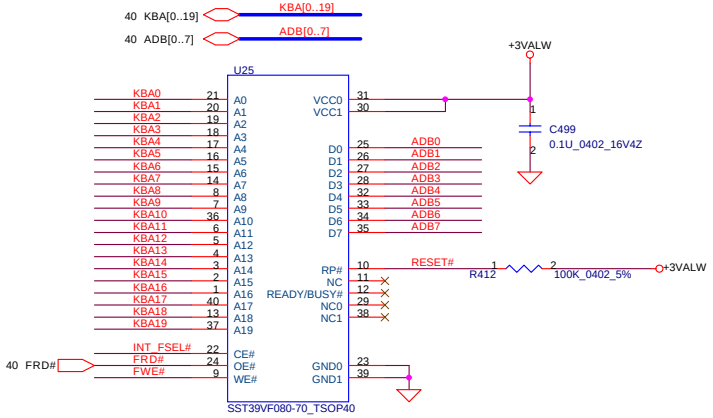




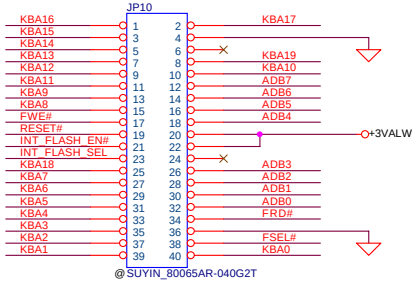
FOR DEBUG ONLY

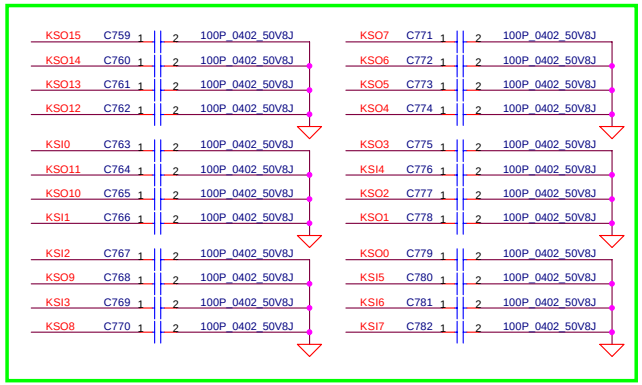


1MB Flash ROM



1MB ROM Socket





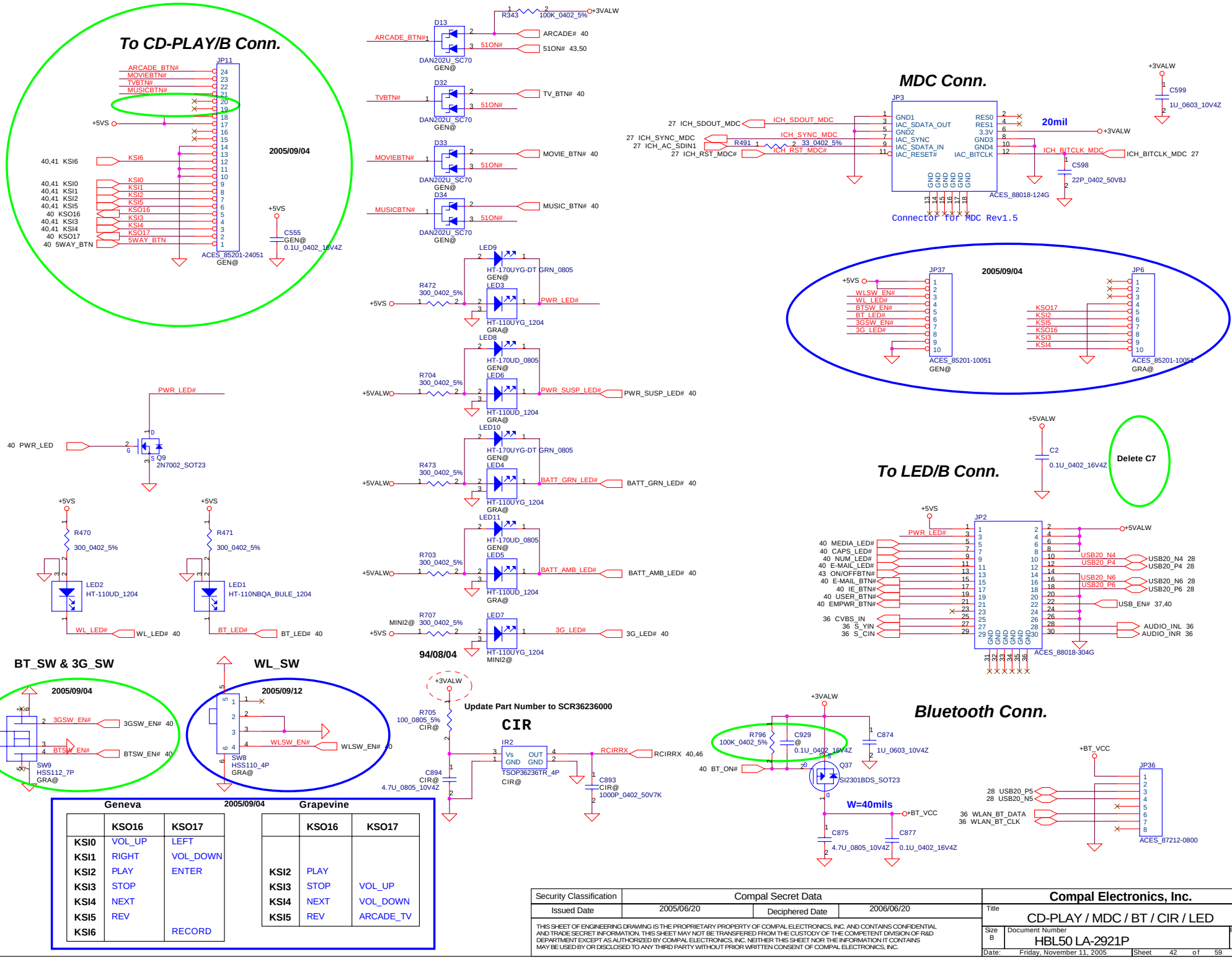
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 41 of 59



Security Classification	Compal Secret Data
Issued Date	2005/06/20
Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: CD-PLAY / MDC / BT / CIR / LED

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 42 of 59

Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

ON/OFF switch

TOP Side

J2 @JOPEN
J1 @JOPEN

Bottom Side

Power Button

+3VALW
R399 100K_0402_5%
42 ON/OFFBTN# → ON/OFFBTN# → D14 DAN202U_SC70
ON/OFF 40
51ON# 42,50
C495 1000P_0402_50V7K
D15 RLZ20A_LL34
40 EC_ON → EC_ON → Q16 2N7002_SOT23
R414 10K_0402_5%

Lid Switch

Change P/N : SN111000207
SW1 MPU-101-81_4P
2005/09/04
+3VALW
R8 100K_0402_5%
LID_SW# 40
D3 @ PSOT24C_SOT23

RTC Battery

BATT1 45@RTCBATT
+RTCBATT
D30 BAS40-04_SOT23
+RTCVCC
CHGRTC
C833 0.1U_0402_16V4Z

Scroll Up

SW2 EVQPLHA15_4P
SCRL_U

Scroll Left

SW5 EVQPLHA15_4P
SCRL_L

Scroll Right

SW6 EVQPLHA15_4P
SCRL_R

Scroll Down

SW7 EVQPLHA15_4P
SCRL_D

Left

SW3 EVQPLHA15_4P
BTN_L

Right

SW4 EVQPLHA15_4P
BTN_R

D17 @ PSOT24C_SOT23 (SCRL_R, BTN_R)
D19 @ PSOT24C_SOT23 (SCRL_L, SCRL_U)
D18 @ PSOT24C_SOT23 (SCRL_D, BTN_L)

Power ON Circuit

Change P/N : SA00000LR00

2005/10/20
+3VS
R420 180K_0402_5%
49,53,54 SUSP → Q41 2N7002_SOT23
C512 1U_0805_25V4Z

+3VALW
U28A SN74LVC14APWLE_TSSOP14 (+3VALW POWER)
U28B SN74LVC14APWLE_TSSOP14 (+3VALW POWER)
R789 @0_0402_5%
SYS_PWROK 6,28
For South Bridge
40 EC_PWROK
R790 0_0402_5%

2005/10/20
+3VS
D36 RB751V_SOD323
R425 62K_0402_1%
C521 0.1U_0402_16V4Z

+3VALW
U28C SN74LVC14APWLE_TSSOP14
U28D SN74LVC14APWLE_TSSOP14
VS_ON 55
For +VCCP/+1.05VS

2005/10/20
37,40,41,49,54 SUSP#
R422 PM@ 62K_0402_1%
+3VS
D37 RB751V_SOD323 PM@
C513 PM@ 0.1U_0402_16V4Z

+3VALW
C511 0.1U_0402_16V4Z
U28E SN74LVC14APWLE_TSSOP14
U28F SN74LVC14APWLE_TSSOP14
VGA_ON 57

To TP/B Conn.

+5VS
40 TP_DATA
40 TP_CLK
C176 0.1U_0402_16V4Z
JP7 ACES_87151-1207
TP_DATA
TP_CLK
BTN_R
SCRL_R
SCRL_U
SCRL_L
SCRL_D
BTN_L

BTN_R	C168	2	@100P_0402_50V8J
SCRL_R	C169	2	@100P_0402_50V8J
SCRL_U	C170	2	@100P_0402_50V8J
SCRL_L	C158	2	@100P_0402_50V8J
SCRL_D	C166	2	@100P_0402_50V8J
BTN_L	C173	2	@100P_0402_50V8J
TP_DATA	C167	2	@100P_0402_50V8J
TP_CLK	C159	2	@100P_0402_50V8J

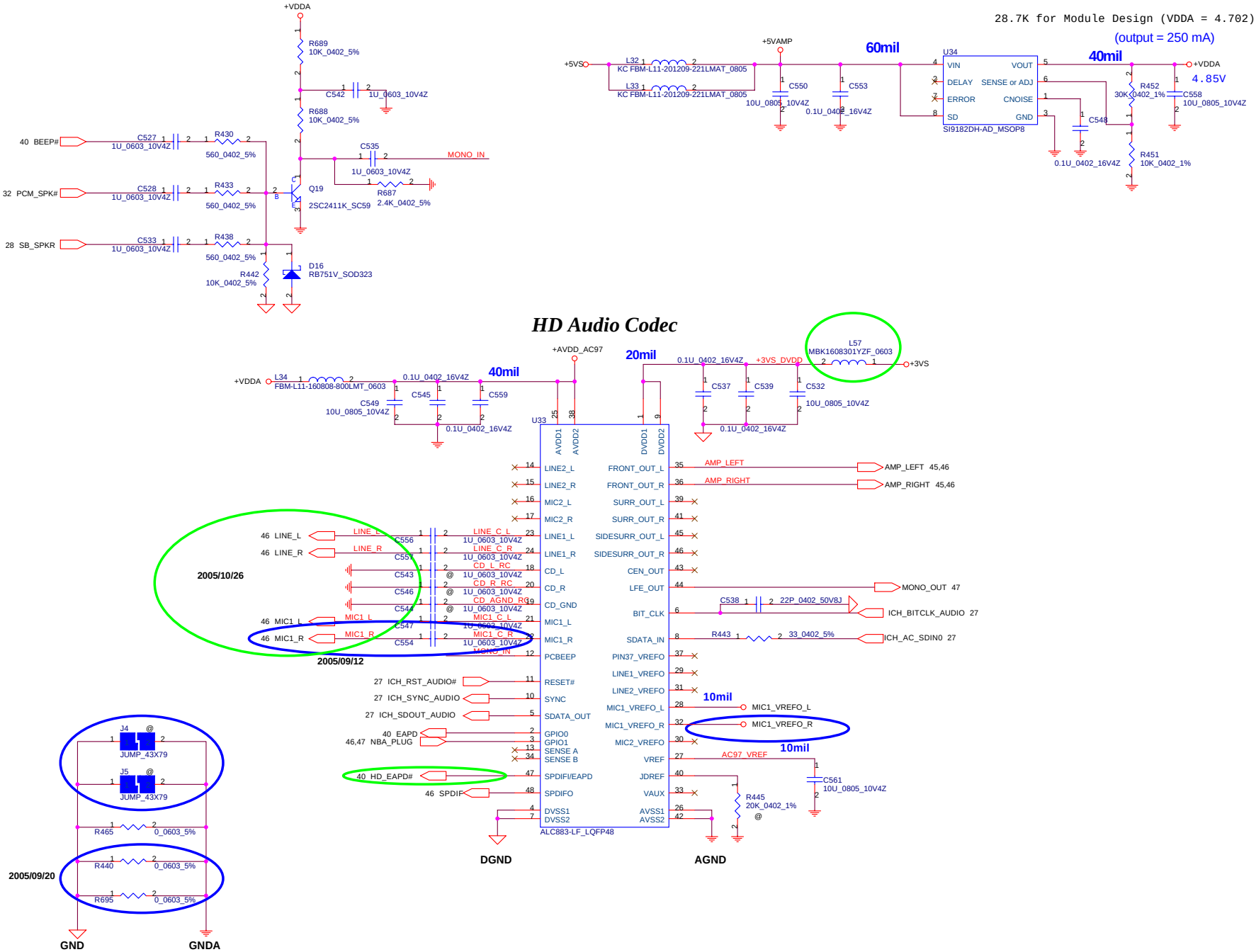
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: Power OK, Reset and RTC Circuit, TP

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 43 of 59



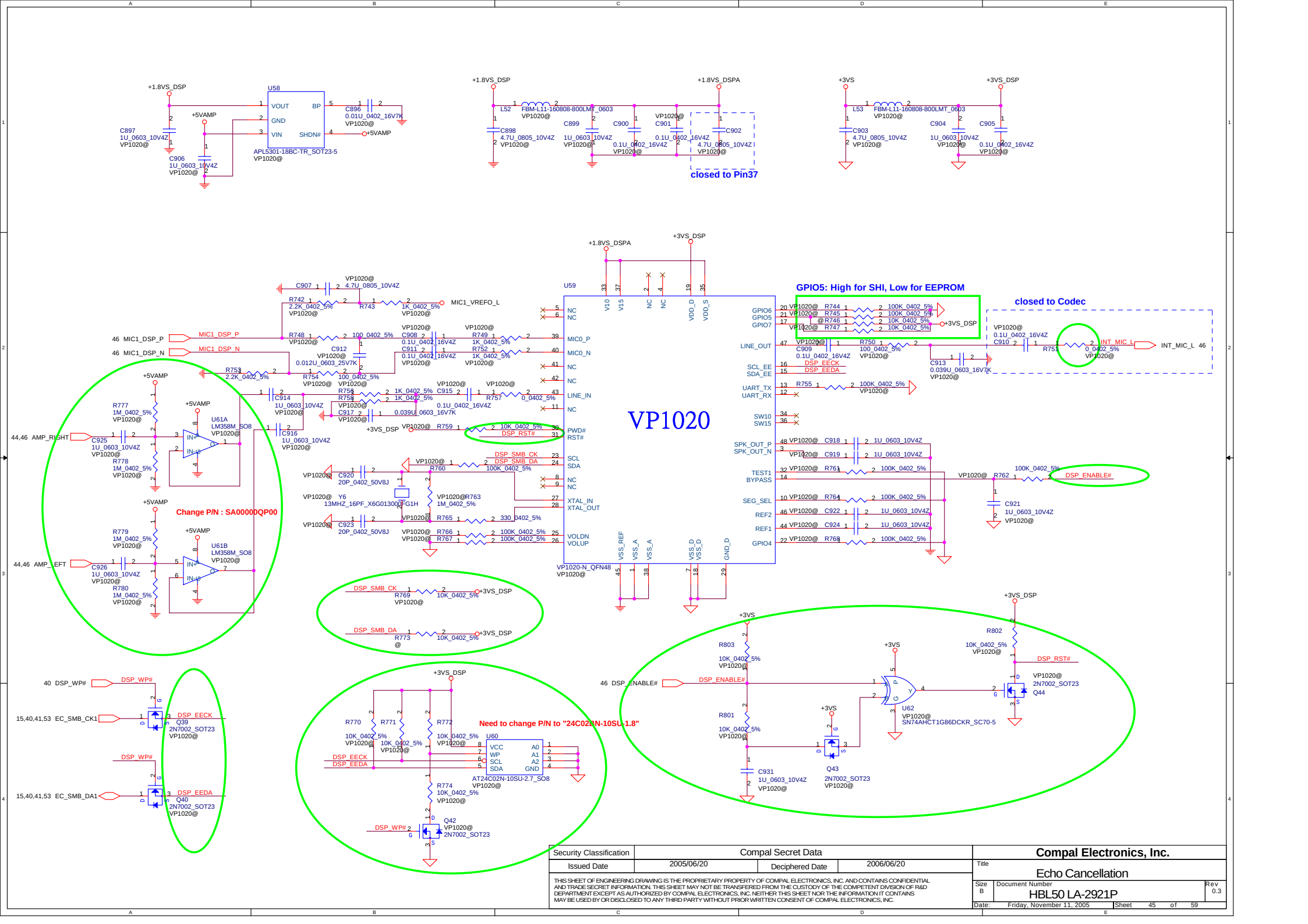
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: HD Audio Codec ALC883

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 | Sheet 44 of 59



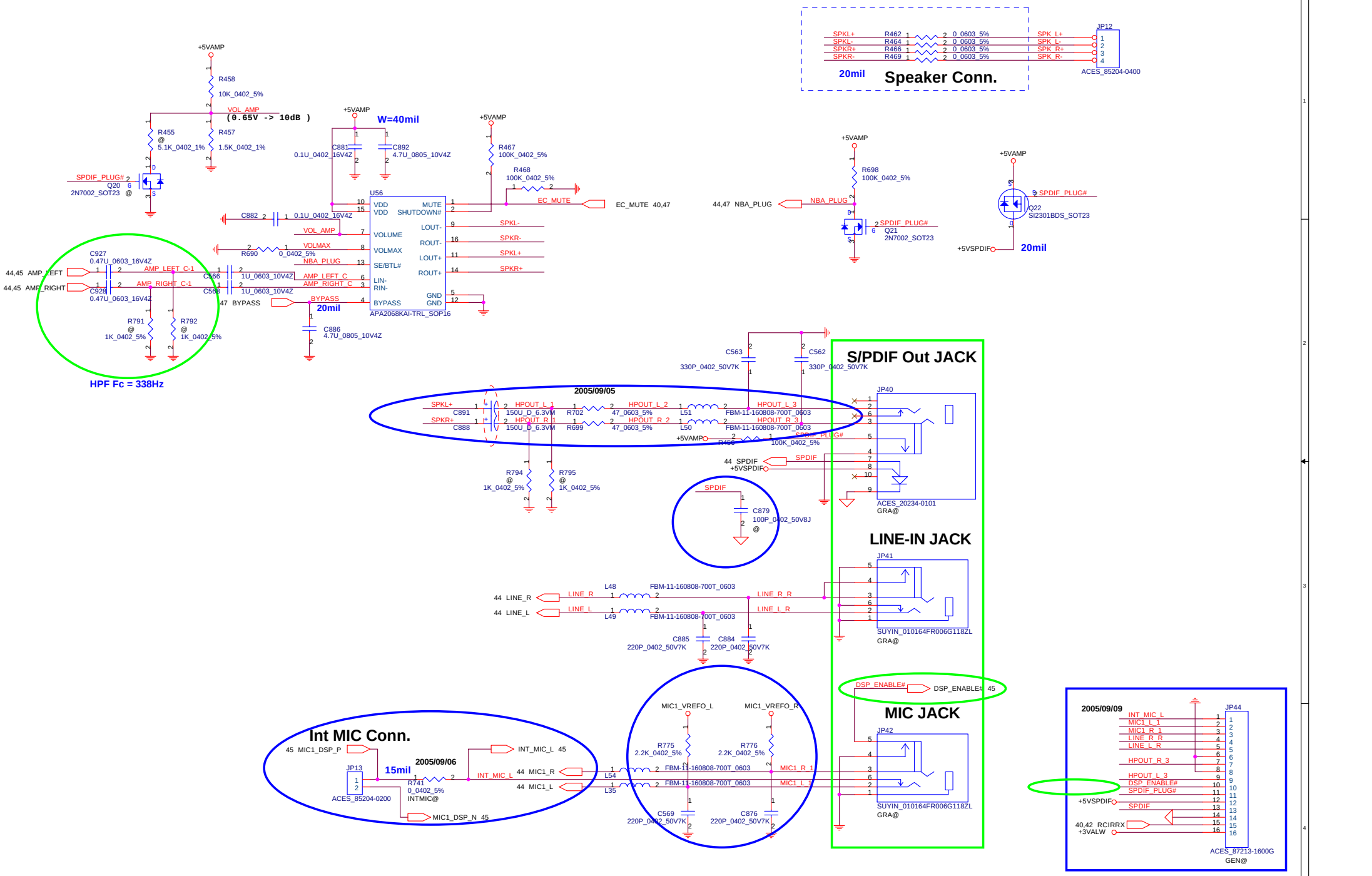
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: Echo Cancellation

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 45 of 59



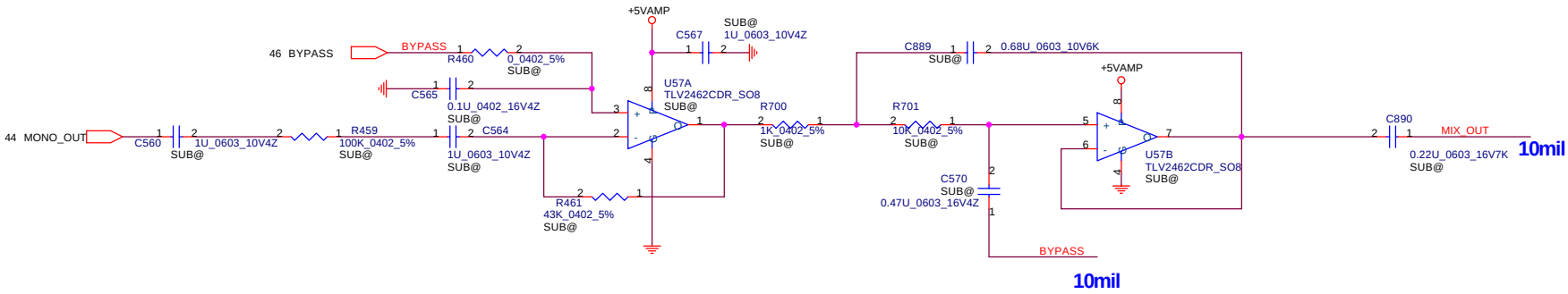
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: Amplifier & Audio Jack

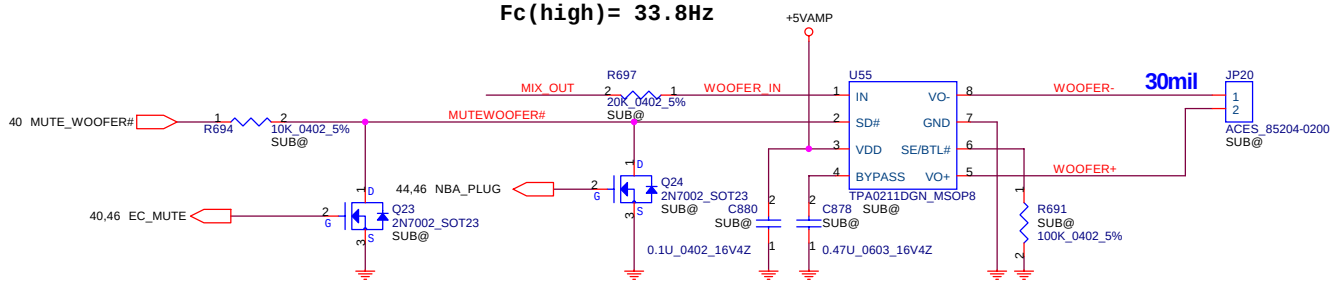
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 | Sheet 46 of 59



fo= 725 Hz

Fc(high)= 33.8Hz



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

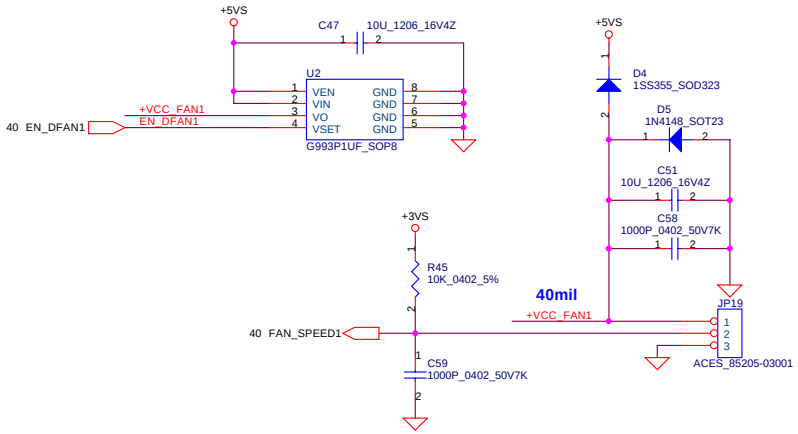
Compal Electronics, Inc.

Title: Subwoofer

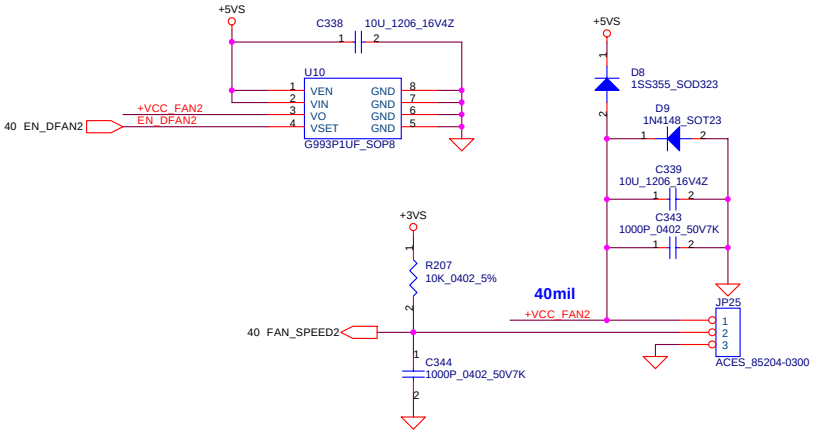
Size: B | Document Number: HBL50 LA-2921P | Rev: 0.3

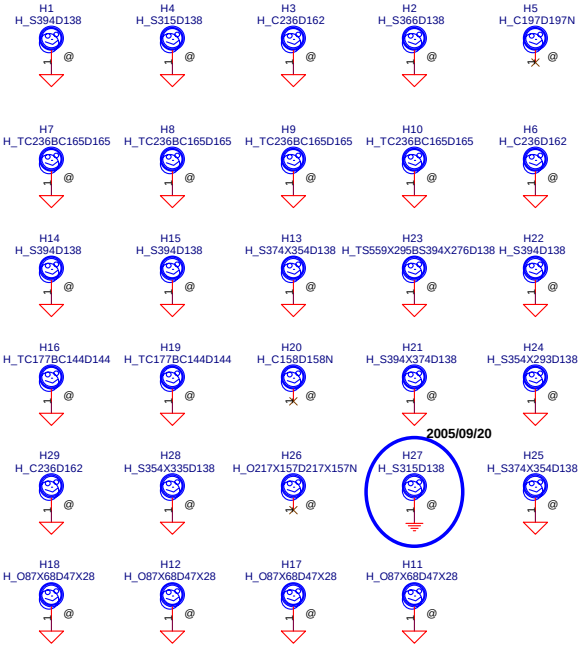
Date: Friday, November 11, 2005 | Sheet 47 of 59

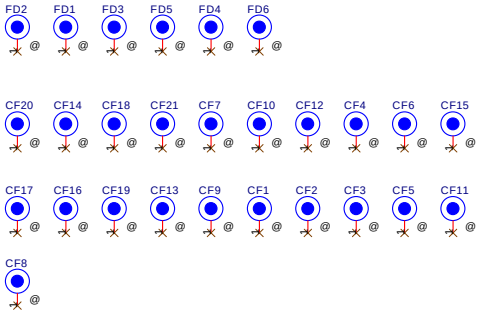
FAN1 Conn



FAN2 Conn







Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

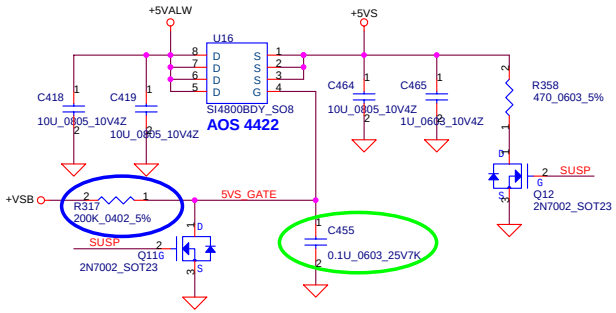
Compal Electronics, Inc.

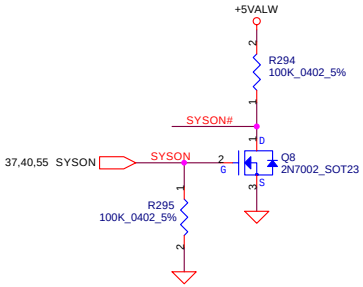
Title: FAN & Screw Hole

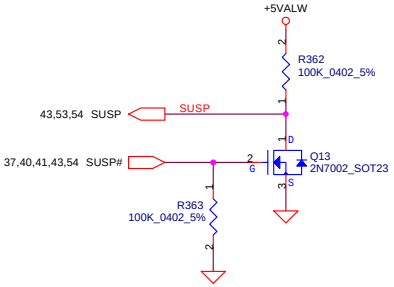
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 | Sheet 48 of 59

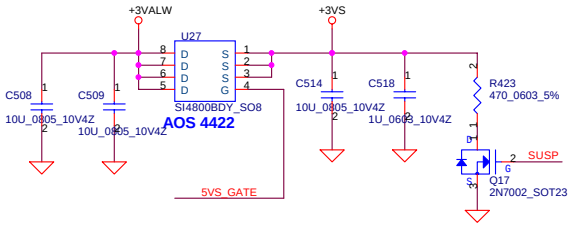
+5VALW TO +5VS



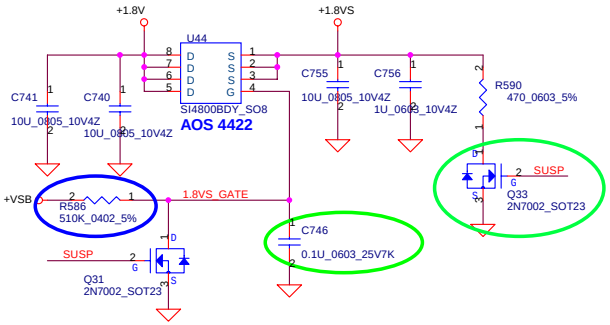


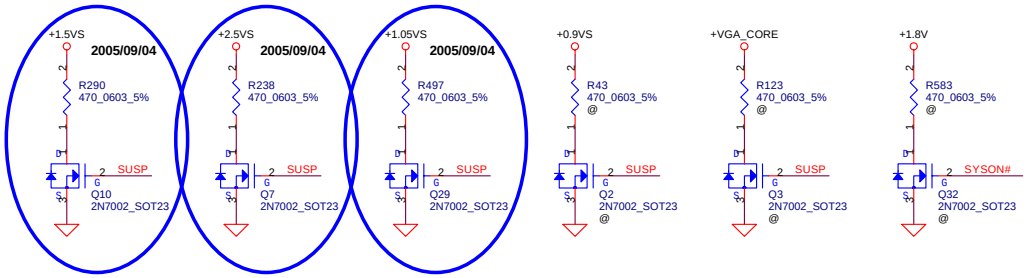


+3VALW TO +3VS



+1.8V to +1.8VS





SUSP

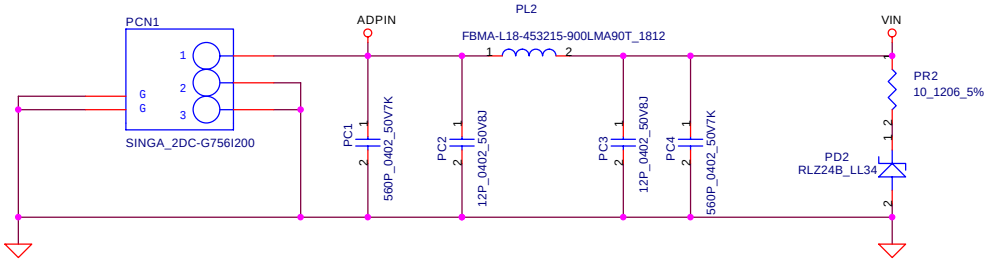
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

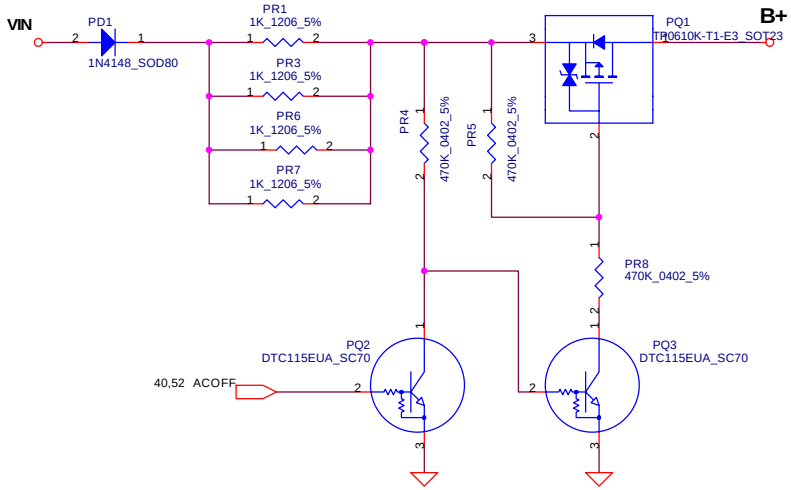
Compal Electronics, Inc.

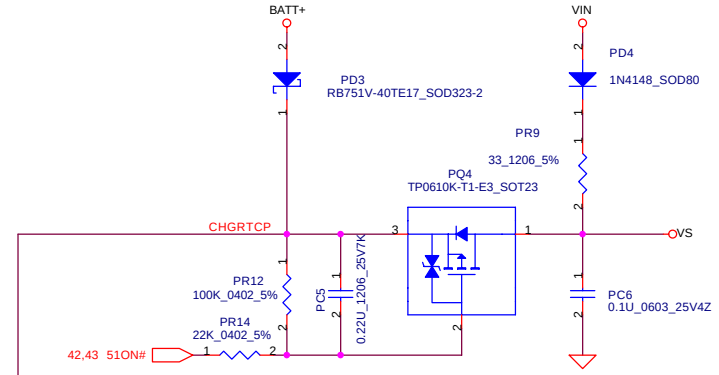
Title: DC Interface

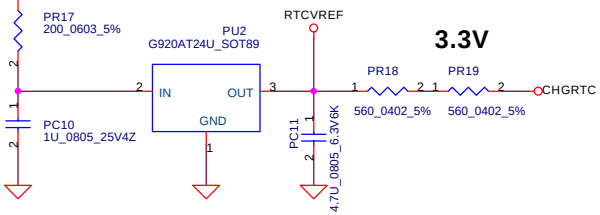
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

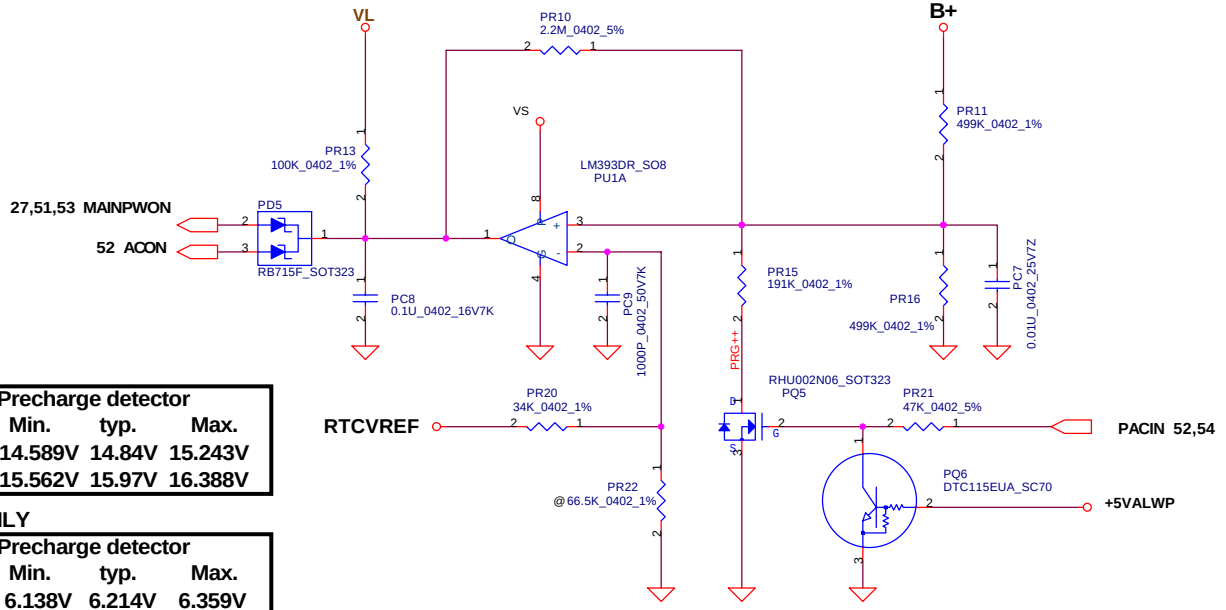
Date: Friday, November 11, 2005 | Sheet 49 of 59











ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

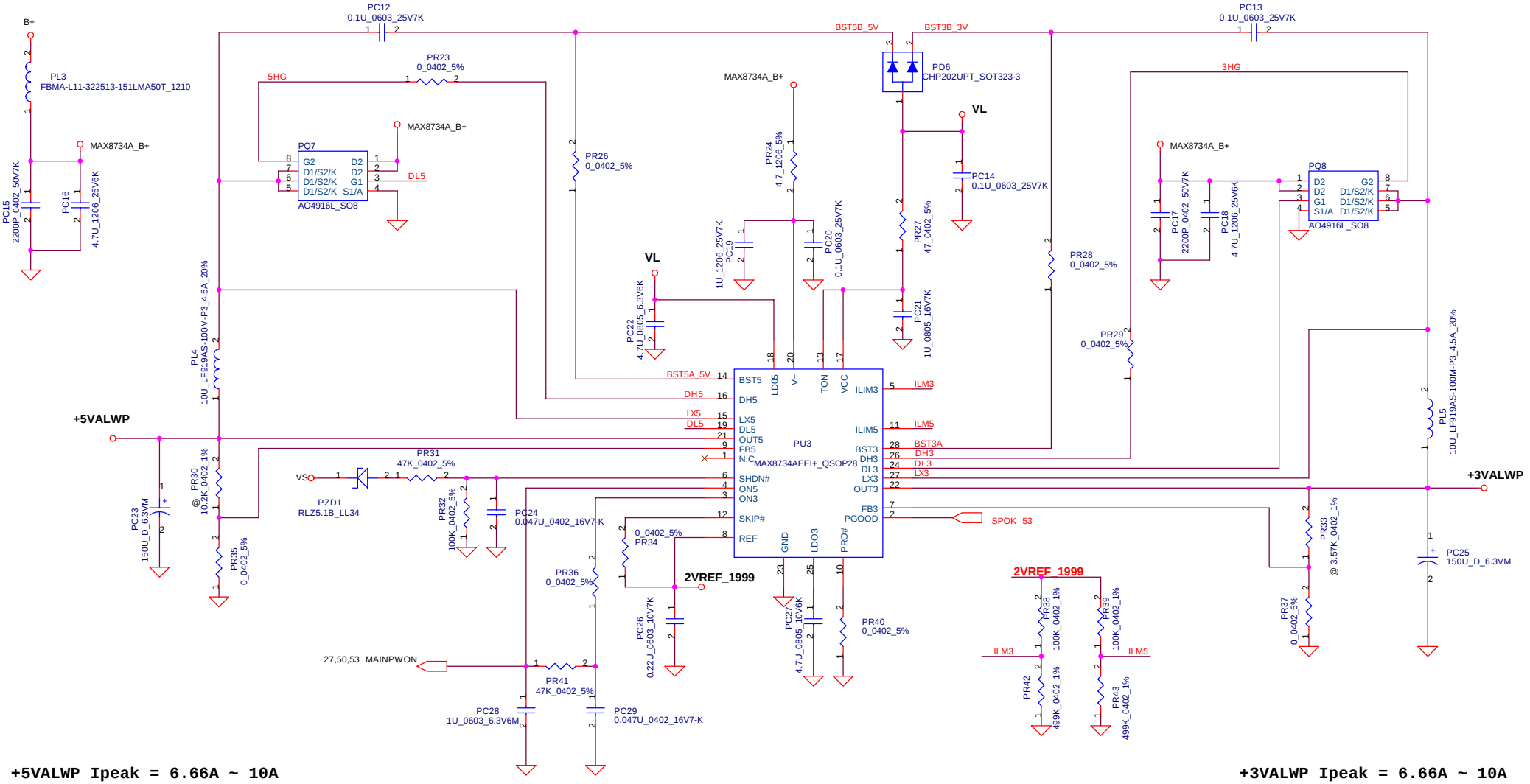
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: **DCIN/DECTOR/RTC**

Size	Document Number	Rev
B	HBL50 LA-2921P	0.2

Date: Friday, November 11, 2005 | Sheet 50 of 59



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

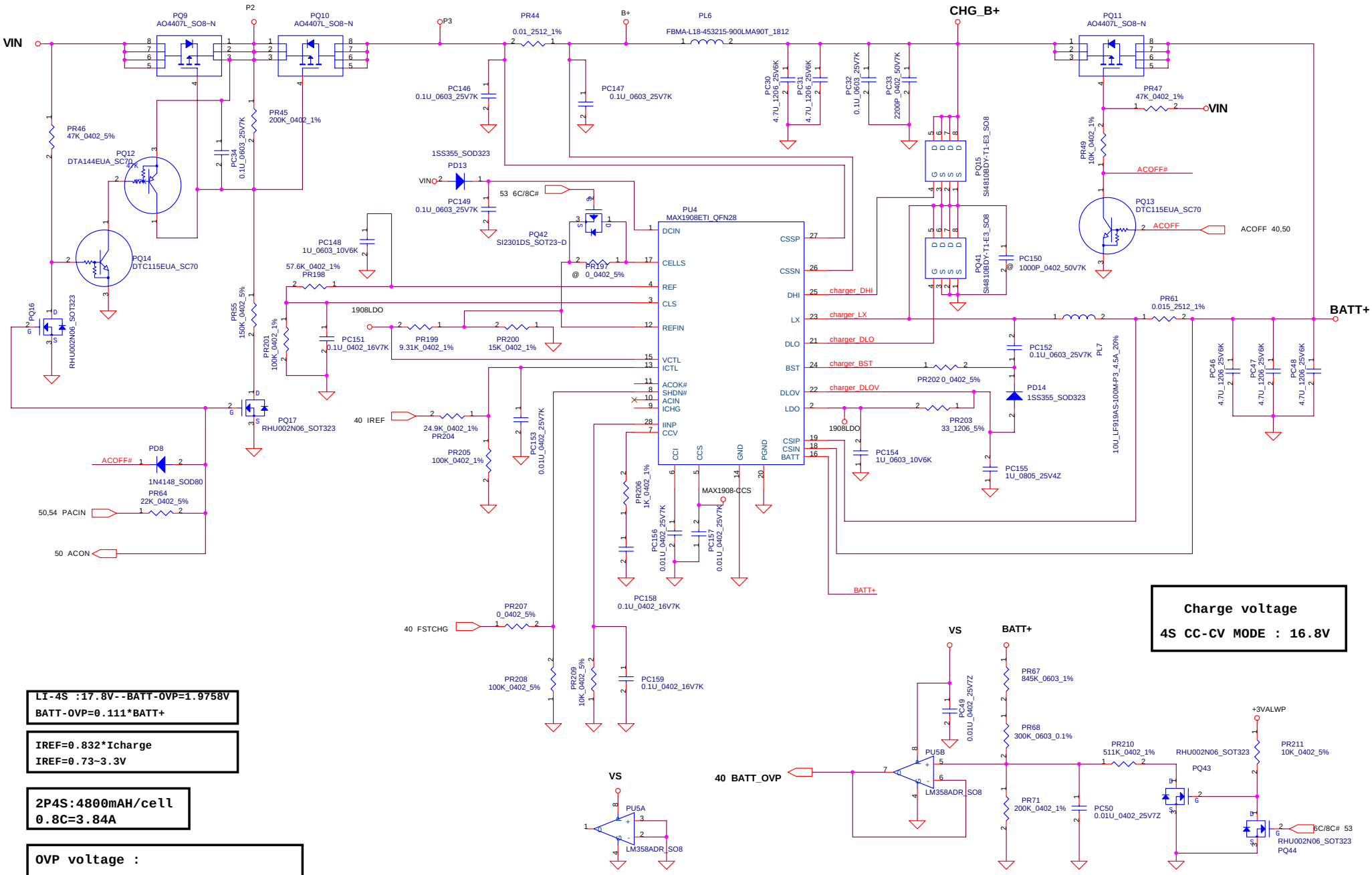
Title: **+5VALWP/+3VALWP**

Size	Document Number	Rev
Custom	**HBL50 LA-2921P**	0.2

Date: Friday, November 11, 2005 | Sheet 51 of 59

Charger

Iadp=0~4.74A(90W)



Charge voltage

4S CC-CV MODE : 16.8V

LI-4S :17.8V--BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

IREF=0.832*Icharge
IREF=0.73~3.3V

2P4S:4800mAH/cell
0.8C=3.84A

OVP voltage :

LI-3S :17.8V----BATT-OVP=1.9758V

BATT-OVP=0.111*BATT+

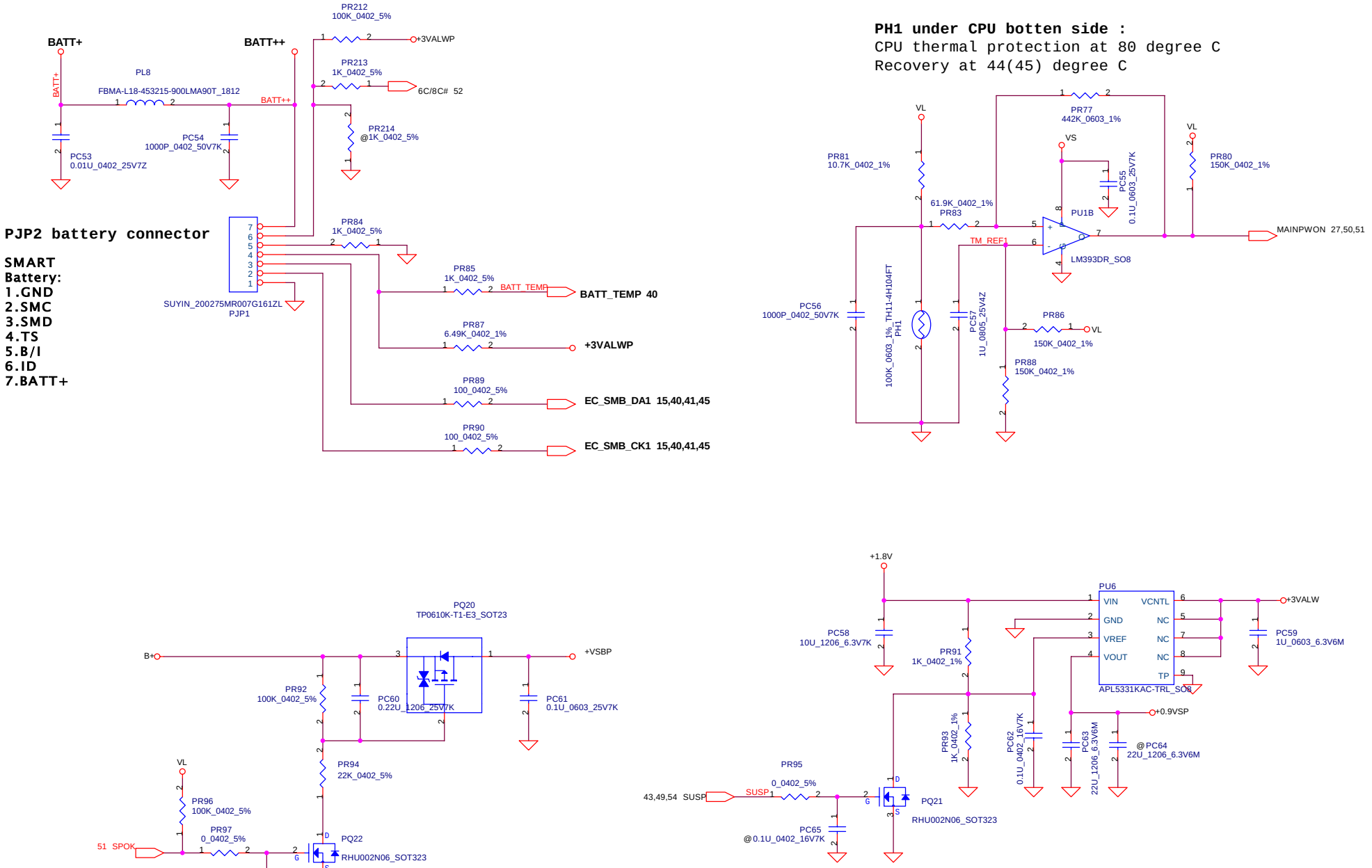
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: **Charger**

Size	Document Number	Rev
B	HBL50 LA-2921P	0.2

Date: Friday, November 11, 2005 Sheet 52 of 59



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: **BATTERY CONN. / OTP/+0.9VSP**

Size	Document Number	Rev
B	HBL50 LA-2921P	0.2

Date: Friday, November 11, 2005 Sheet 53 of 59

AC Adapter Detector

+1.5VSP — PJ1 (PAD-OPEN 3x3m) — +1.5VS
(2.5A,100mils ,Via NO.=5)

+1.8VP — PJ2 (PAD-OPEN 3x3m) — +1.8V
(6A,240mils ,Via NO.= 12)

+5VALWP — PJ3 (PAD-OPEN 3x3m) — +5VALW
(5A,200mils ,Via NO.= 10)

+0.9VSP — PJ4 (PAD-OPEN 3x3m) — +0.9VS
(0.3A,40mils ,Via NO.= 2)

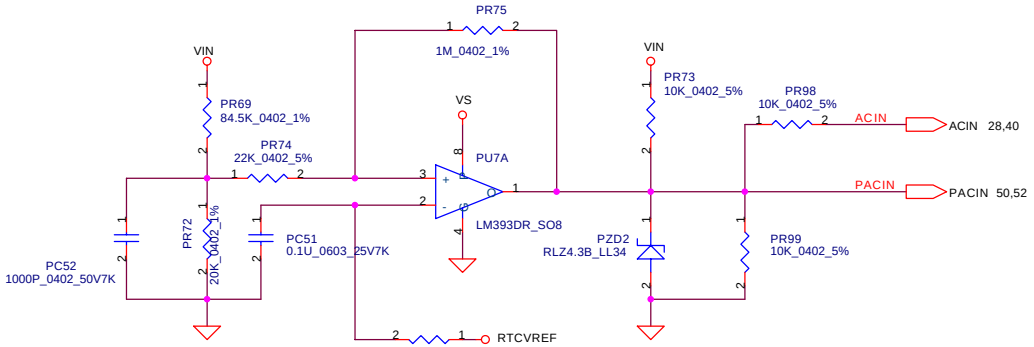
+3VALWP — PJ5 (PAD-OPEN 3x3m) — +3VALW
(4.5A,180mils ,Via NO.= 9)

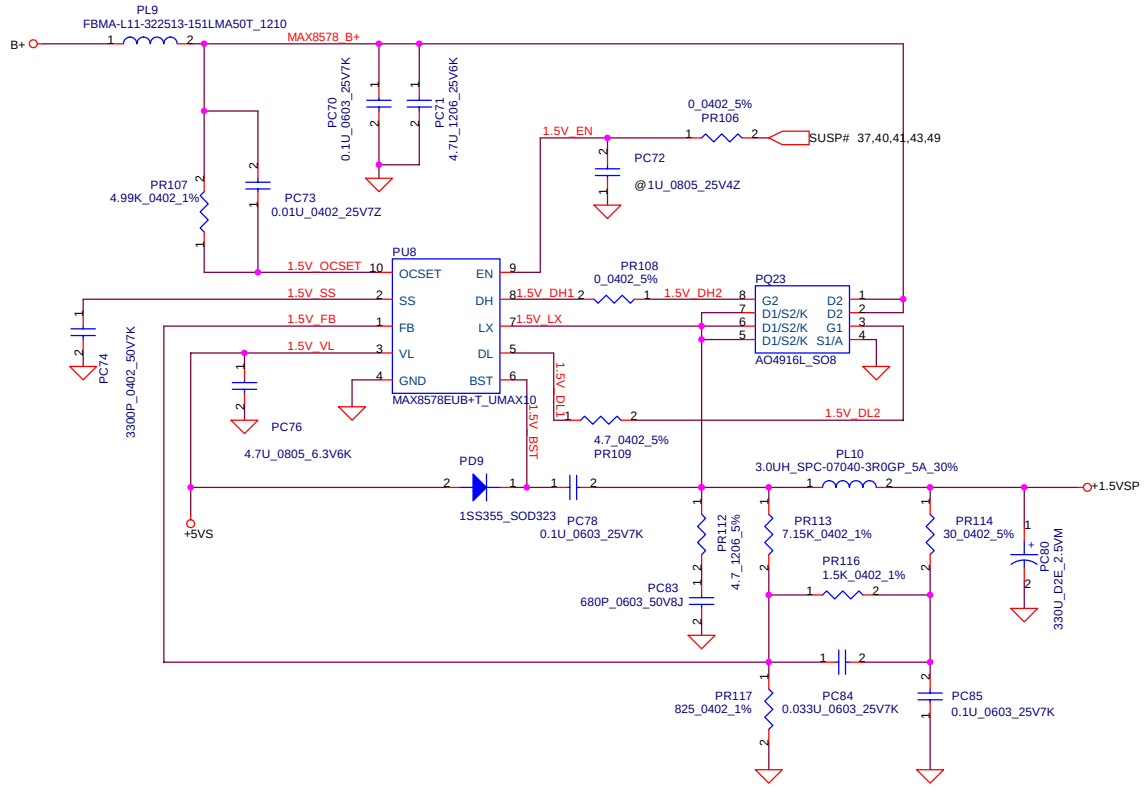
+2.5VSP — PJ6 (PAD-OPEN 3x3m) — +2.5VS
(0.3A,40mils ,Via NO.= 2)

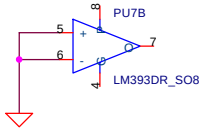
+1.05VSP — PJ7 (PAD-OPEN 3x3m) — +1.05VS
(2A,80mils ,Via NO.= 4)

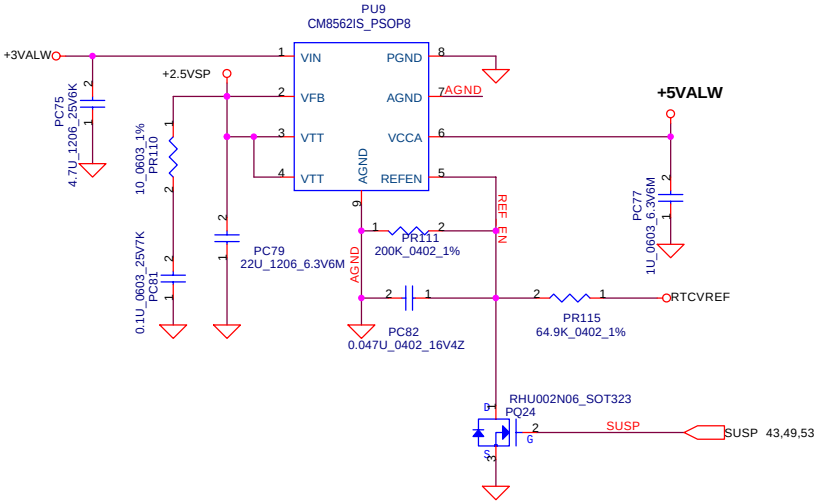
+VSBP — PJ8 (JUMP_43X79) — +VSB

Vin Detector
17.90V/17.24V









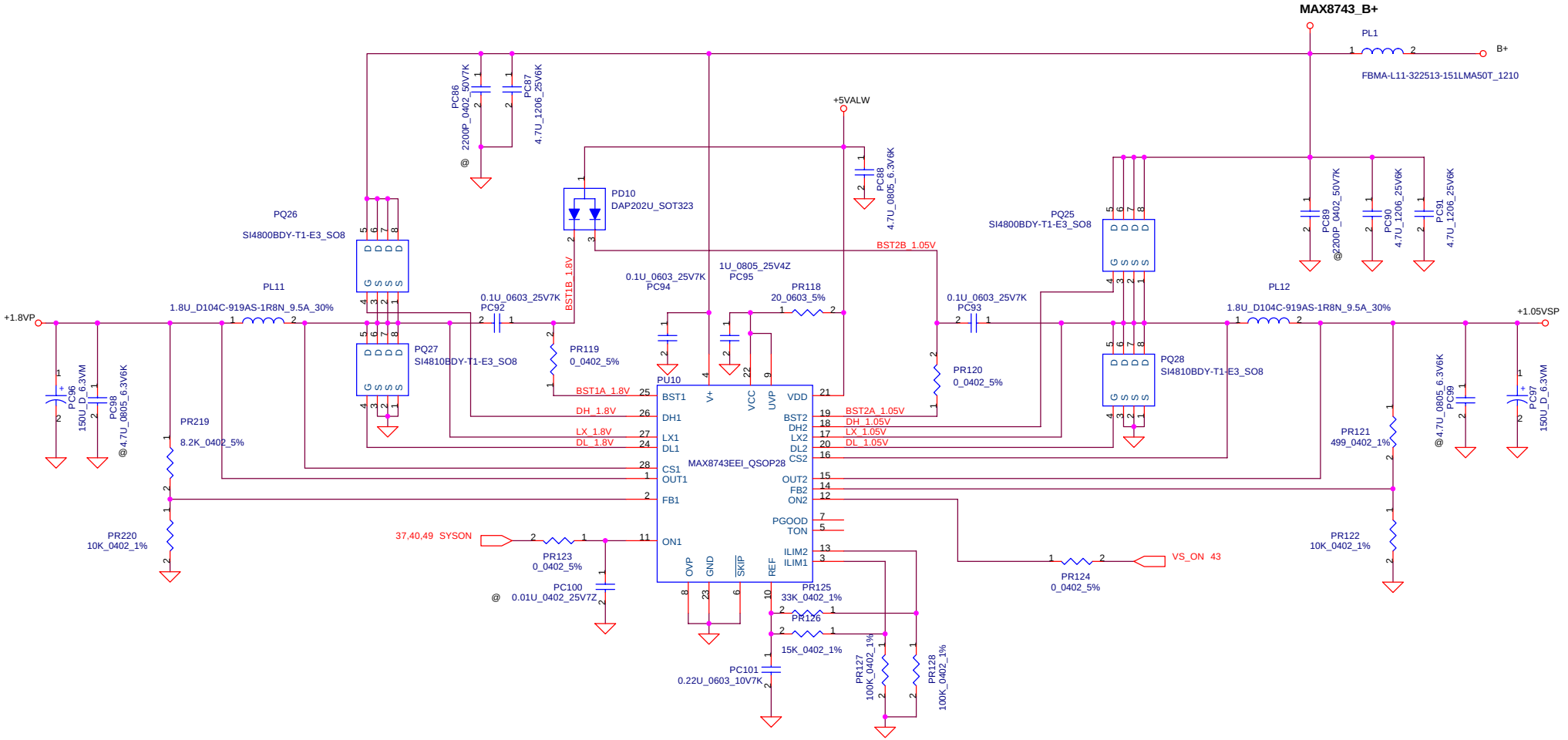
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: **+1.5VSP/RTCVREF**

Size	Document Number	Rev
B	**HBL50 LA-2921P**	0.2

Date: Friday, November 11, 2005 Sheet 54 of 59



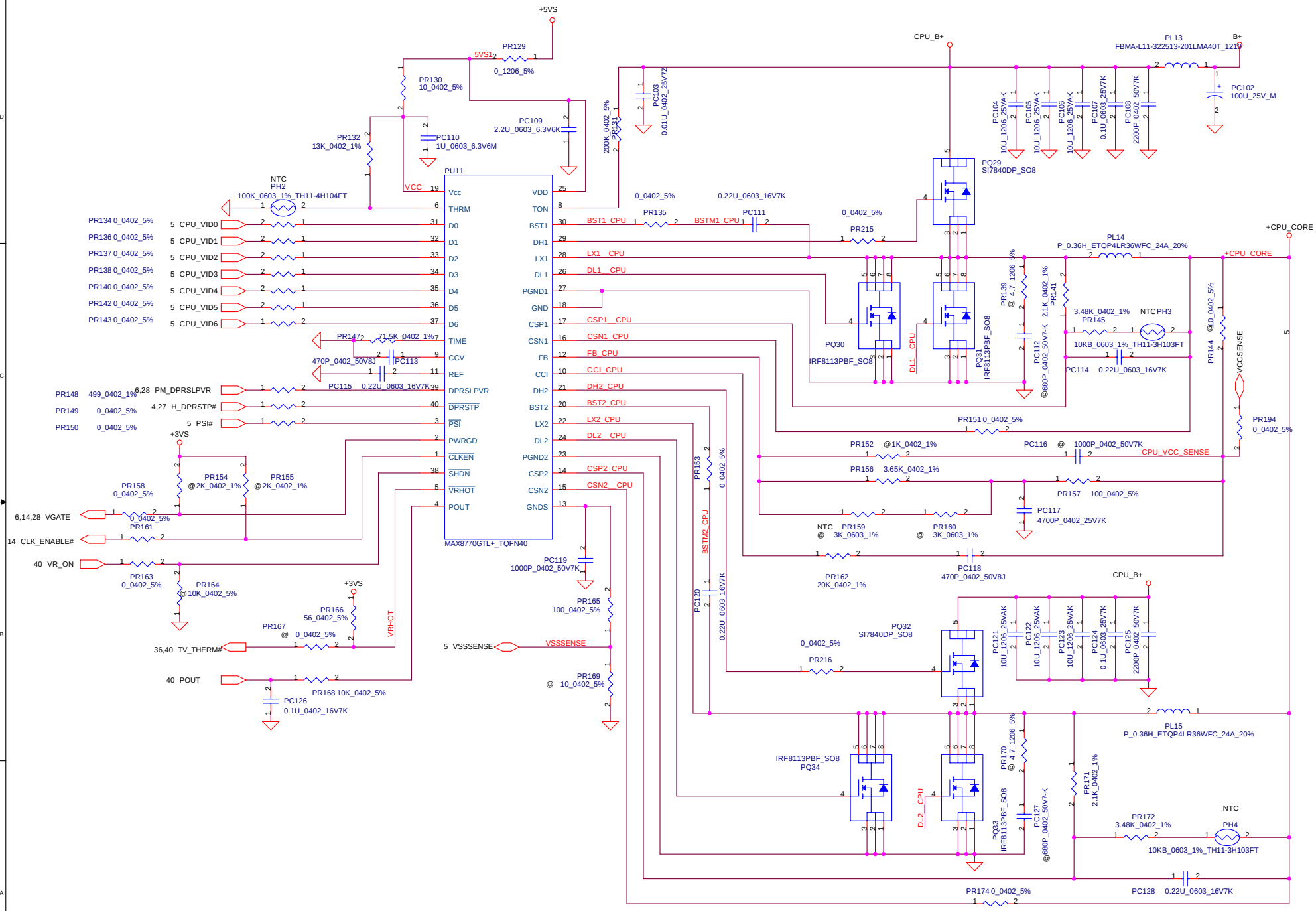
Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: **+1.05VSP/+1.8VP**

Size	Document Number	Rev
B	**HBL50 LA-2921P**	0.2

Date: Friday, November 11, 2005 | Sheet 55 of 59



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: **+CPU_CORE**

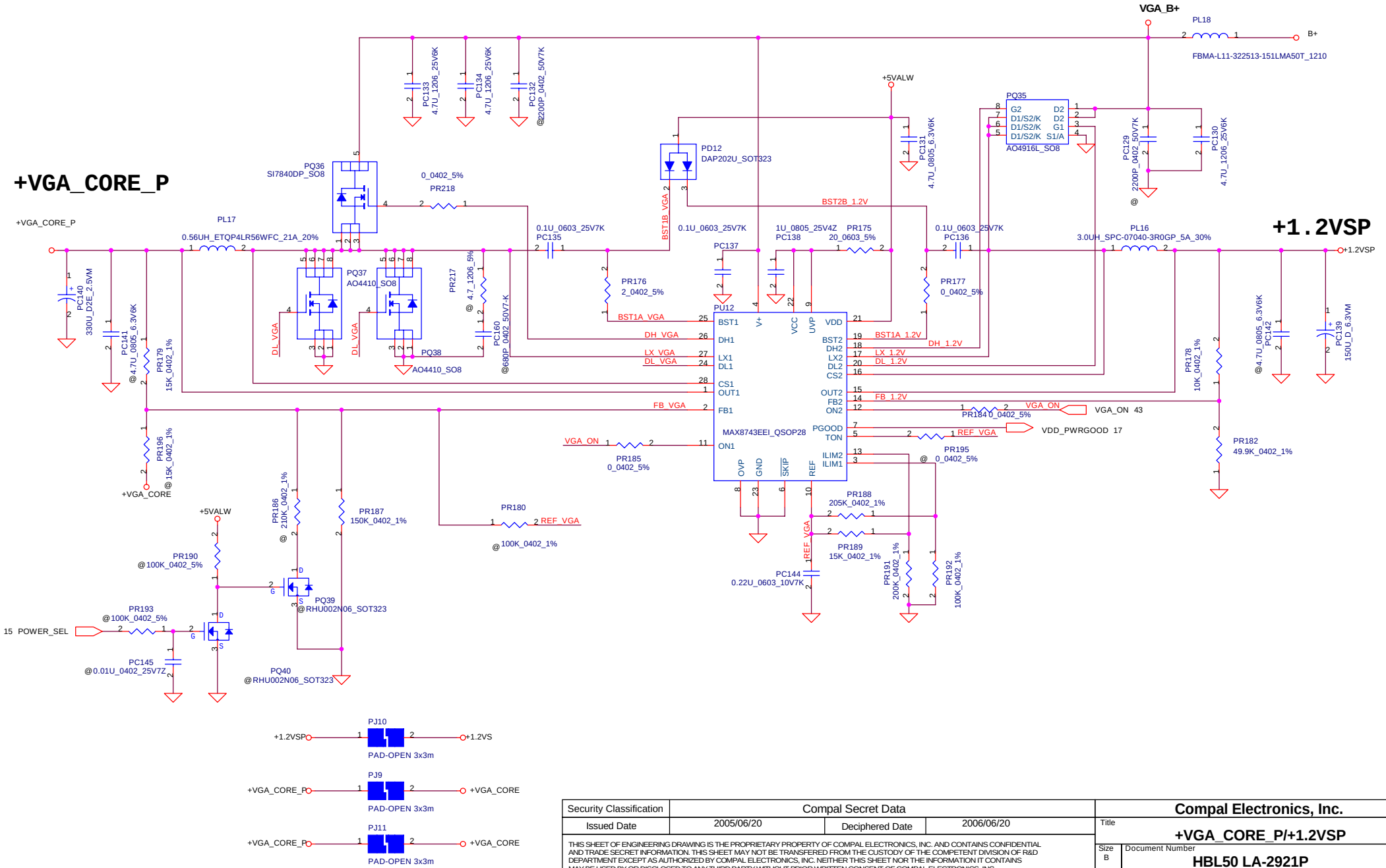
Size	Document Number	Rev
Custom	HBL50 LA-2921P	0.2

Date: Friday, November 11, 2005 | Sheet 56 of 59

POWER_SEL	H	L
+VGA_CORE FOR G73.	+0.95V(VGA@+G72@)	+1.025V
+VGA_CORE FOR G72.	+1.1V(VGA@)	

+VGA_CORE_P

+1.2VSP



Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: +VGA_CORE_P/+1.2VSP

Size	Document Number	Rev
B	HBL50 LA-2921P	0.2

Date: Friday, November 11, 2005 Sheet 57 of 59

A --> B Change List

1. Page06 : No stuff R100 10K_0402_5%
2. Page09 : Add C49 & C887 220U_D2_4VM
3. Page10 : No stuff R57 2.2K_0402_5%
4. Page14 : Add R711 10K_0402_5% to set 96MHz output
   Change Q14 & Q15 pin1 net name to connect to ICH7M
   Change U19 ICS9LPRS325CKLFT part number to SA00000RE20
5. Page15 : Change C663, C664 from 22P_0402_50V8J to 18P_0402_50V8J.
6. Page18 : Modify VGA Device ID for G72MV & G73.
7. Page24 : Change VGA_DDC_CLK & VGA_DDC_DATA to Q26 & Q27 Level shift.
   Add R781 & R782 4.7K_0402_5%
   Change C589, C596, C583, C587, C594, C585 to 150P_0402_50V8J
8. Page28 : Change SB_INT_FLASH_SEL# from ICH7M GPIO38 to GPIO33.
9. Page29 : Change C437 from 0.1U_0402_16V4Z to 1U_0402_6.3V4Z
10. Page30 : Change PATA HDD+ODD select resistor form RP to R_0402 (0_0402_5%)
11. Page34 : Stuff R175 & no stuff R182(0_0402_5%) for BCM4401E/BCM5789M/BCM5787M
12. Page35 : Modify LAN_ACTIVITY# & LAN_LINK# LED color
13. Page 36 : Add JP38 & C895 for CAMERA.
    Swap JP17 PCIE TX & RX Signal.
    Swap JP30 PCIE TX & RX Signal.
14. Page37 : Connect JP34 SMBus interface to ICH7M
    Change JP4 & JP5 USB connector to BOTTOM.
15. Page38 : Add 1394@ BOM Structure.
16. Page41 : Delete LCM interface Extension I/O.
    No stuff R390 & Stuff R418 for Flash ROM interface.
17. Page42 : Change JP11 from 34 pin to 24 pin.
    Change SW8 & SW9.
    Add JP37.
18. Page43 : Change U28 Part Number.
    Change SW1 Part Number.
    Change R425 from 10K_0402_5% to 62K_0402_1%
    Change R422 from 10K_0402_5% to 62K_0402_1% & add C513 0.1U_0402_16V4Z
19. Page44 : Add C554 for MIC_R
    Add R440, R695 (0_0603_5%) & J4, J5 for EMI request.
20. Page45 : Add Echo Cancellation function.
21. Page46 : Correct Headphone L & R signal.
    Reserved C879 for EMI request
    Modify MIC Jack circuit. add R741, R775, R776, L54, C876
    Change JP44 from 14 pin to 16 pin
22. Page48 : H27 connect to GNDA.
23. Page49 : Add R290, R238, R497, Q10, Q7, Q29
    Change R317 to 200K_0402_5%
    Change R586 to 510K_0402_5%

B --> C Change List

1. Page05 : No stuff C608, C614
2. Page12 : Change JP22 Footprint
3. Page14 : Change R620 from 2K_0402_5% to 10K_0402_5% & add Q38
4. Page15 : Delete DVI pull high resistor
5. Page17 : AddC96 330U for +VGA_CORE
6. Page18 : Modify PEX_CFG[0..2] setting from 02 to 01.
7. Page30 : Delete R395 & C486, add R394 for SATA bridge reset timing
   Modify SATA HDD connector library
8. Page31 : Delete IDE_CD_L, IDE_CD_R & CD_GNDA
9. Page34 : Add R783, R784, R785 for BCM5787M, stuff R214 when use BCM4401E,
   Del R168, change Q5 P/N
10. Page36 : Add +3VS, GND at JP30 for 3G device
11. Page38 : No stuff U14, R253, R246 & stuff R261
12. Page40 : Reserved R793 for ALC883 pin47 EAPD, & define KB910 Pin174 as EC_PWROK
13. Page41 : No stuff U21, U30, C490, R391, R390, R388 & stuff R418
14. Page42 : Modify SW9 Pin1, Pin5 as NC, no stuff C7
15. Page43 : Modify Power OK circuit. add R790 for EC_PWROK, reserved Q41, R420, C512
    add D35, D37, Change BATT1 P/N to SP093PA0200
16. Page44 : Delete ALC883 CD input circuit, add HD_EAPD# signal
17. Page46 : Add C927, C928, reserved R791, R792
18. Page49 : Stuff Q33

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: HW PIR

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 Sheet 58 of 59

Security Classification	Compal Secret Data		
Issued Date	2005/06/20	Deciphered Date	2006/06/20

Compal Electronics, Inc.

Title: PWR PIR

Size	Document Number	Rev
B	HBL50 LA-2921P	0.3

Date: Friday, November 11, 2005 | Sheet 59 of 59