

Compal Confidential

KAL90 M/B Schematics Document

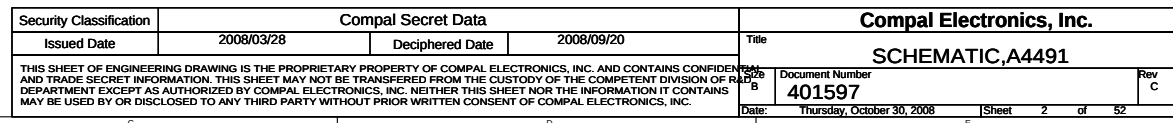
Intel Penryn Processor with Cantiga + DDRII + ICH9M

2008-10-30

REV:1.0

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Issued Date	2008/03/28	Deciphered Date	2008/09/20	Title	SCHEMATIC,A4491
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Date: Thursday, October 30, 2008				Document Number	401597
Sheet 1 of 52					

Model Name : KAL90
File Name : LA-4491P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
MEDIA CONSOLE	1010 000X b	NB9M THERMAL SENSOR	

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

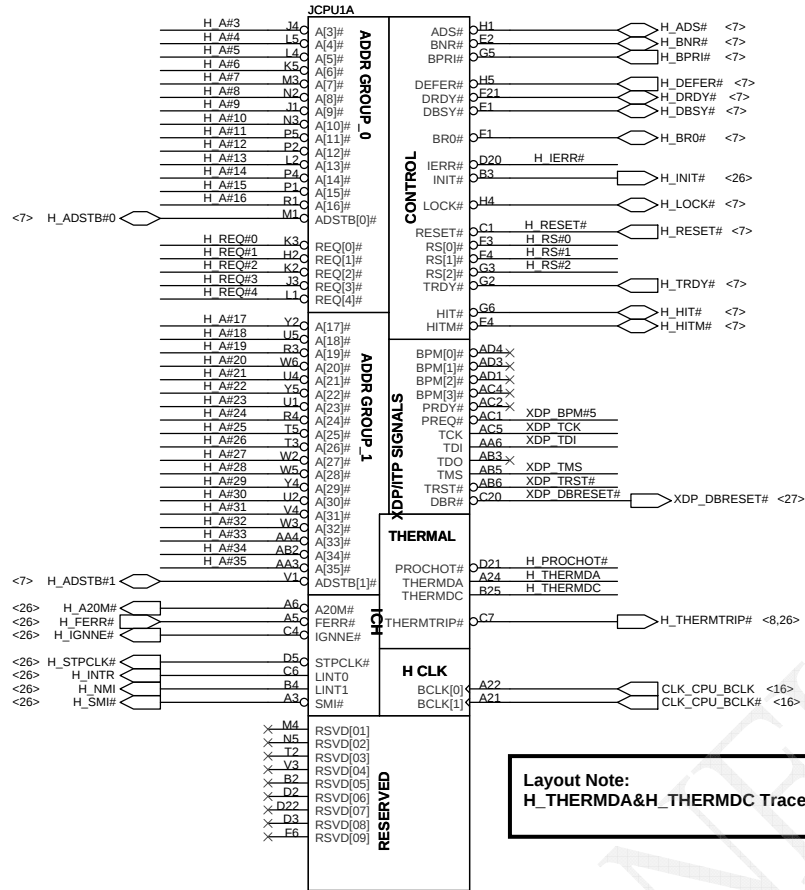
BTO Option Table

BTO Item	BOM Structure
JAL90	JAL90@
JAW50	JAW50@
UMA	GM@
JAL90-UMA	JAL90GM@
JAW50	GLPM@
Discrete	
Discrete	PM@
ALC888VC	888VC@
ALC888VB	888VB@
AR8121	8121@
AR8112	8112@
ALC268	268@

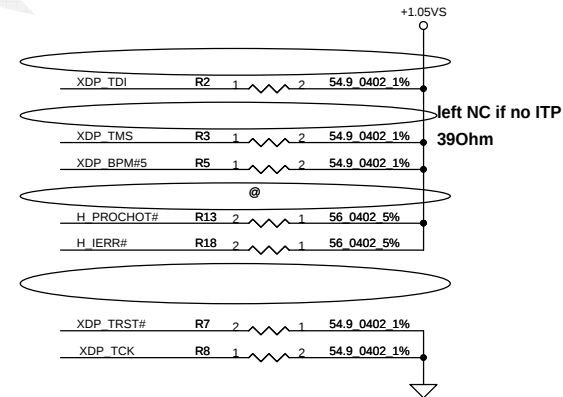
BOM Configuration Table

Project	BOM Configuration
KAL90-UMA	XXXXXXXXXX: JAL90GM@/JAL90@/GM@/888VC@/8121@/ESATA@
KAL90-Dis	XXXXXXXXXX: PM@/JAL90@/GLPM@/888VC@/8121@/ESATA@

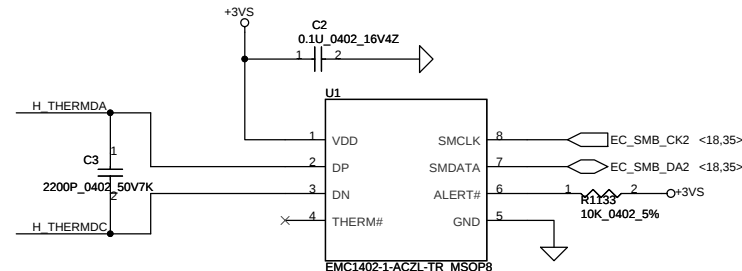
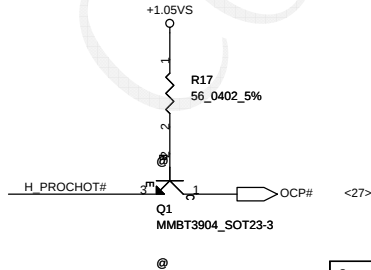
<7> H_A# [3..35] H_A# [3..35]
 <7> H_REQ# [0..4] H_REQ# [0..4]
 <7> H_RS# [0..2] H_RS# [0..2]

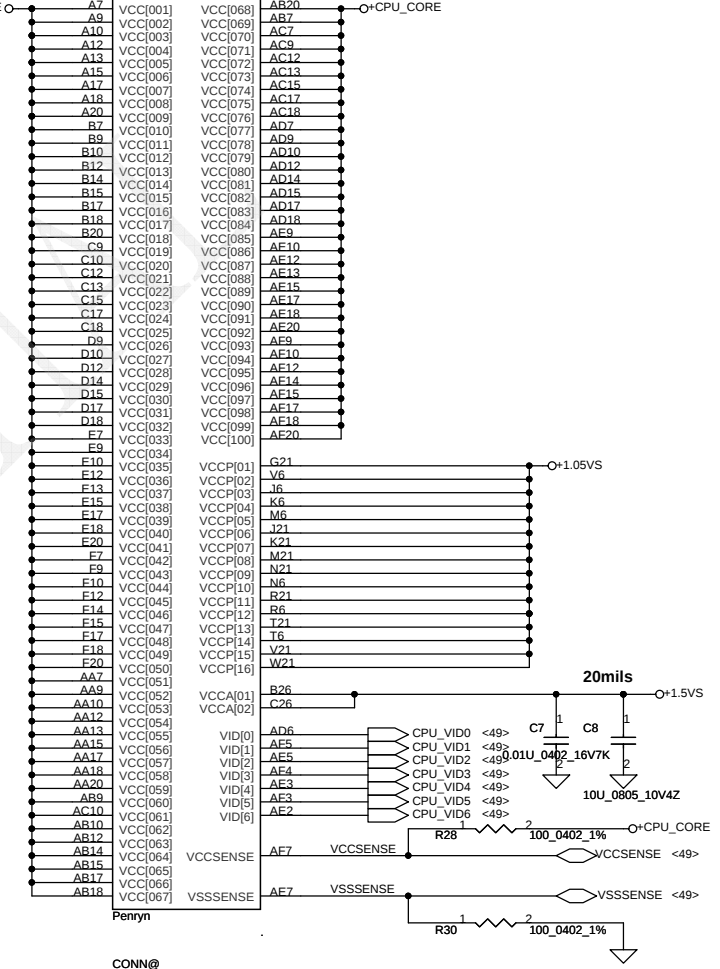
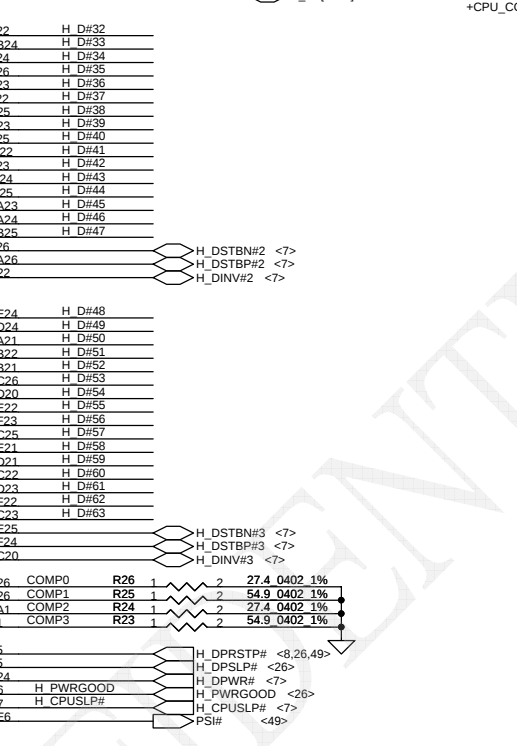
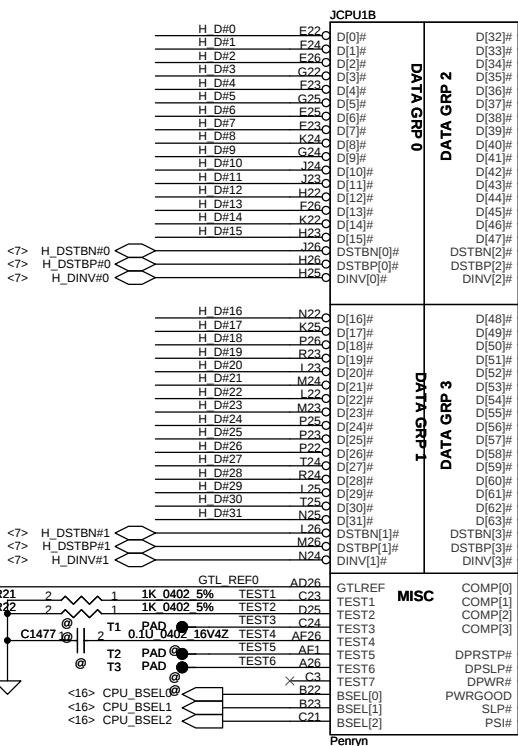


Layout Note:
 H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil



BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166



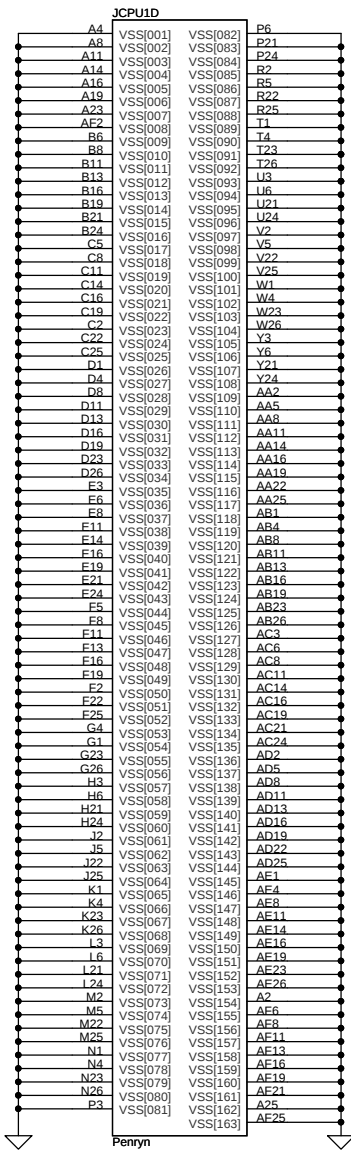


TRACE CLOSELY CPU < 0.5"

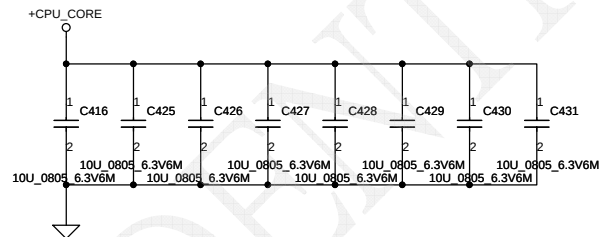
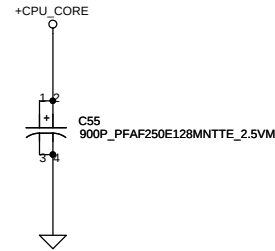
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)

COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

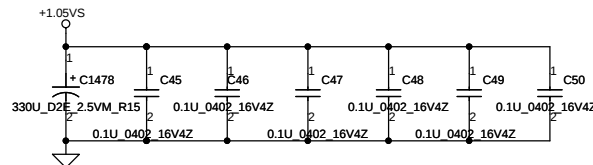
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		Size B		Document Number				Rev C	
		401597							
		Date:		Thursday, October 30, 2008		Sheet		5 of 52	



CONN@

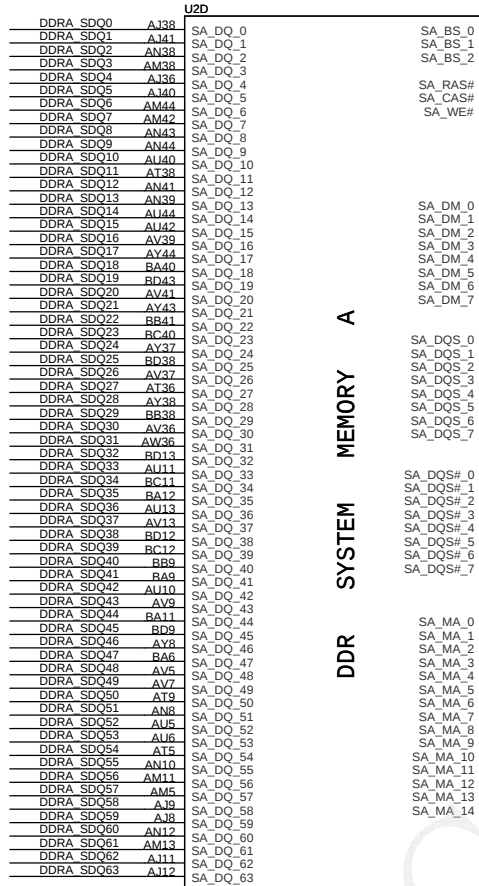


+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32

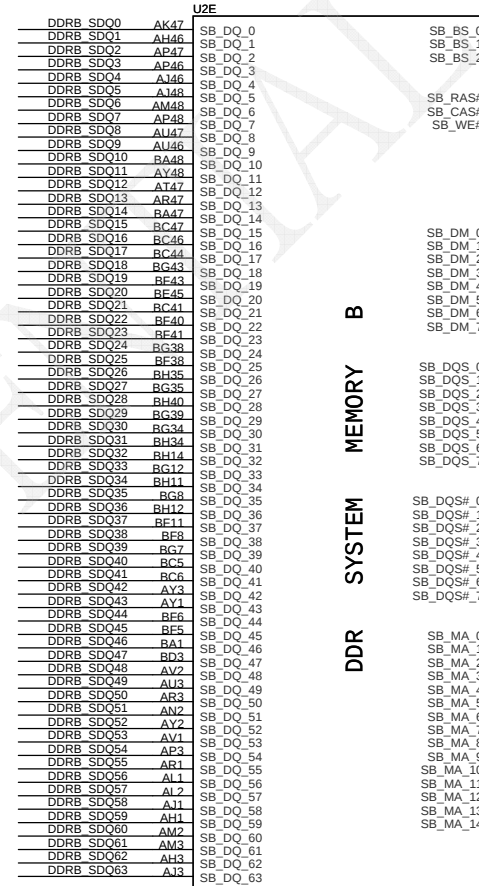


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<15> DDRB_SDQ[0..63] <15> DDRB_SDM[0..7] <15> DDRB_SMA[0..14]

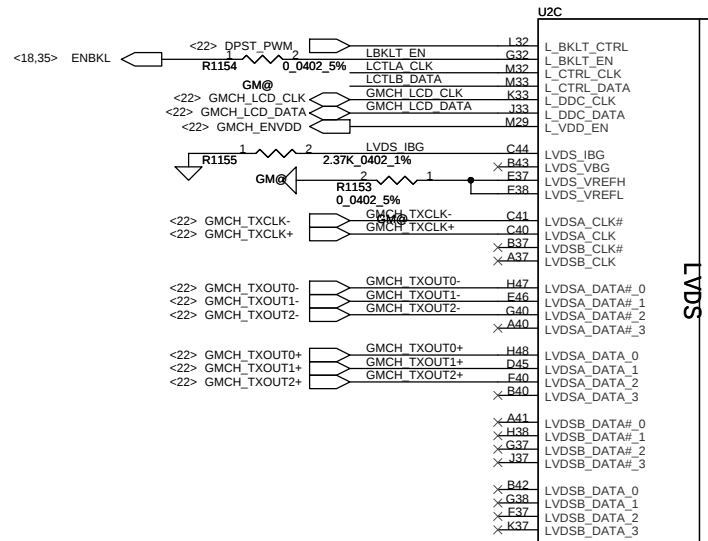


CANTIGA ES_FCBGA1329
GM@

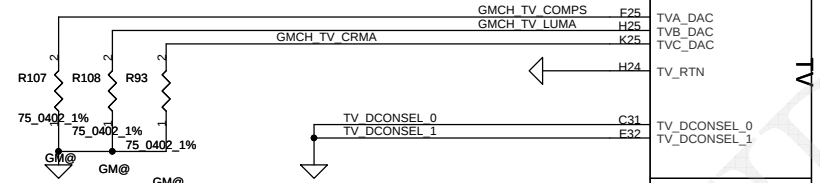


CANTIGA ES_FCBGA1329
GM@

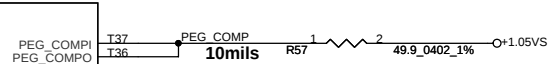
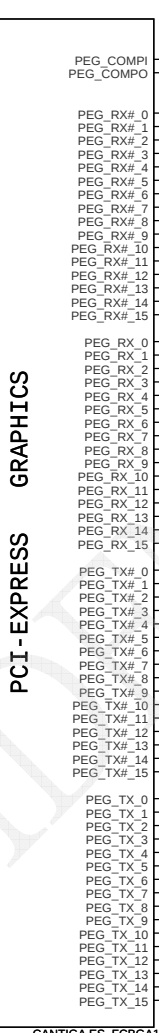
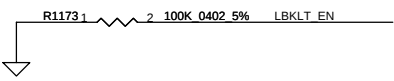
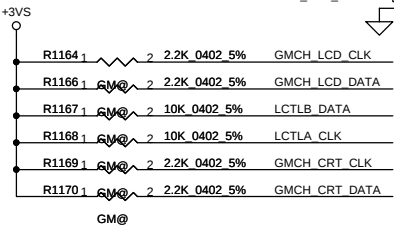
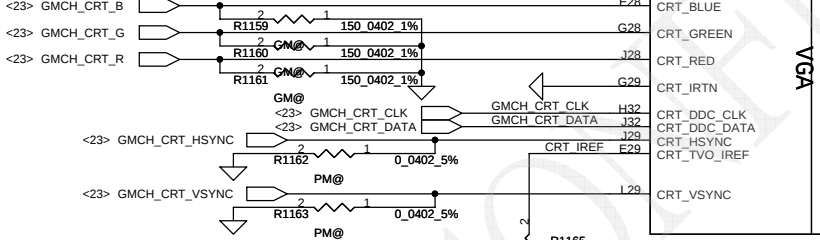
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Size	B	Document Number	401597	Rev	C
Date:	Thursday, October 30, 2008	Sheet	9	of	52



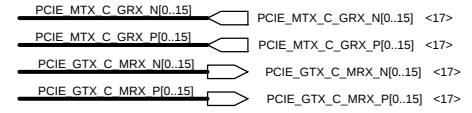
Change to 00hm when use PM chip



Change to 00hm when use PM chip

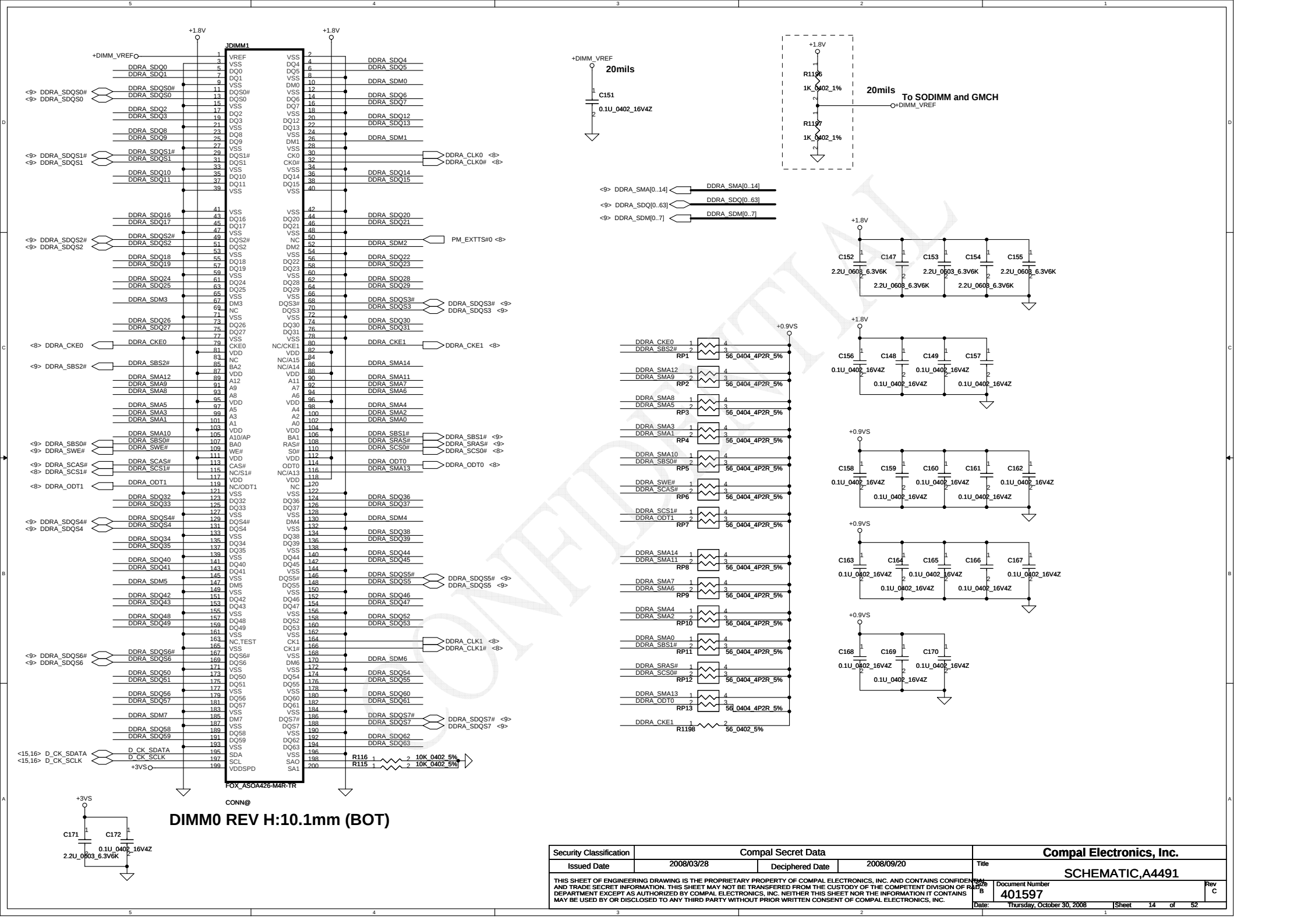


PEG_RX#_0	H44	PCIE GTX C MRX N0
PEG_RX#_1	J46	PCIE GTX C MRX N1
PEG_RX#_2	L44	PCIE GTX C MRX N2
PEG_RX#_3	L40	PCIE GTX C MRX N3
PEG_RX#_4	N41	PCIE GTX C MRX N4
PEG_RX#_5	P48	PCIE GTX C MRX N5
PEG_RX#_6	N44	PCIE GTX C MRX N6
PEG_RX#_7	T43	PCIE GTX C MRX N7
PEG_RX#_8	U43	PCIE GTX C MRX N8
PEG_RX#_9	Y43	PCIE GTX C MRX N9
PEG_RX#_10	Y48	PCIE GTX C MRX N10
PEG_RX#_11	Y36	PCIE GTX C MRX N11
PEG_RX#_12	AA43	PCIE GTX C MRX N12
PEG_RX#_13	AD37	PCIE GTX C MRX N13
PEG_RX#_14	AC47	PCIE GTX C MRX N14
PEG_RX#_15	AD39	PCIE GTX C MRX N15
PEG_RX_0	H43	PCIE GTX C MRX P0
PEG_RX_1	J44	PCIE GTX C MRX P1
PEG_RX_2	L43	PCIE GTX C MRX P2
PEG_RX_3	L41	PCIE GTX C MRX P3
PEG_RX_4	N40	PCIE GTX C MRX P4
PEG_RX_5	P47	PCIE GTX C MRX P5
PEG_RX_6	N43	PCIE GTX C MRX P6
PEG_RX_7	T42	PCIE GTX C MRX P7
PEG_RX_8	U42	PCIE GTX C MRX P8
PEG_RX_9	Y42	PCIE GTX C MRX P9
PEG_RX_10	Y47	PCIE GTX C MRX P10
PEG_RX_11	Y27	PCIE GTX C MRX P11
PEG_RX_12	AA42	PCIE GTX C MRX P12
PEG_RX_13	AD36	PCIE GTX C MRX P13
PEG_RX_14	AC48	PCIE GTX C MRX P14
PEG_RX_15	AD40	PCIE GTX C MRX P15



PEG_TX#_0	J41	PCIE MTX GRX N0
PEG_TX#_1	M46	PCIE MTX GRX N1
PEG_TX#_2	M47	PCIE MTX GRX N2
PEG_TX#_3	M40	PCIE MTX GRX N3
PEG_TX#_4	M42	PCIE MTX GRX N4
PEG_TX#_5	R48	PCIE MTX GRX N5
PEG_TX#_6	N38	PCIE MTX GRX N6
PEG_TX#_7	T40	PCIE MTX GRX N7
PEG_TX#_8	U37	PCIE MTX GRX N8
PEG_TX#_9	U40	PCIE MTX GRX N9
PEG_TX#_10	Y40	PCIE MTX GRX N10
PEG_TX#_11	AA46	PCIE MTX GRX N11
PEG_TX#_12	AA37	PCIE MTX GRX N12
PEG_TX#_13	AA40	PCIE MTX GRX N13
PEG_TX#_14	AD43	PCIE MTX GRX N14
PEG_TX#_15	AC46	PCIE MTX GRX N15
PEG_TX_0	J42	PCIE MTX GRX P0
PEG_TX_1	L46	PCIE MTX GRX P1
PEG_TX_2	M48	PCIE MTX GRX P2
PEG_TX_3	M39	PCIE MTX GRX P3
PEG_TX_4	M43	PCIE MTX GRX P4
PEG_TX_5	R47	PCIE MTX GRX P5
PEG_TX_6	N37	PCIE MTX GRX P6
PEG_TX_7	T39	PCIE MTX GRX P7
PEG_TX_8	U36	PCIE MTX GRX P8
PEG_TX_9	Y39	PCIE MTX GRX P9
PEG_TX_10	Y46	PCIE MTX GRX P10
PEG_TX_11	AA36	PCIE MTX GRX P11
PEG_TX_12	AA39	PCIE MTX GRX P12
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PEG_TX_15	AD46	PCIE MTX GRX P15

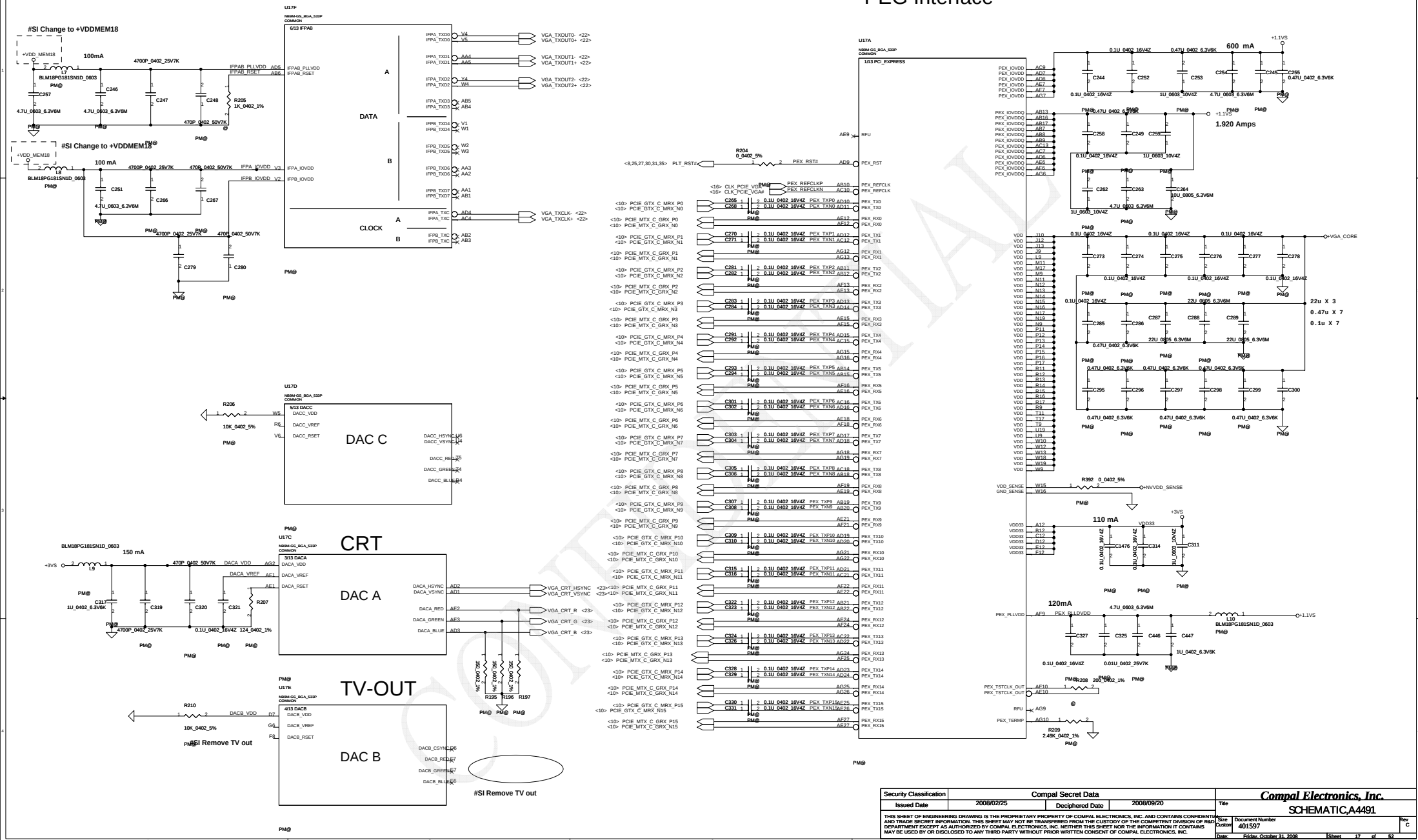
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				Date	Thursday, October 30, 2008
				Sheet	10 of 52



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				401597	C
				Date: Thursday, October 30, 2008	Sheet 14 of 52

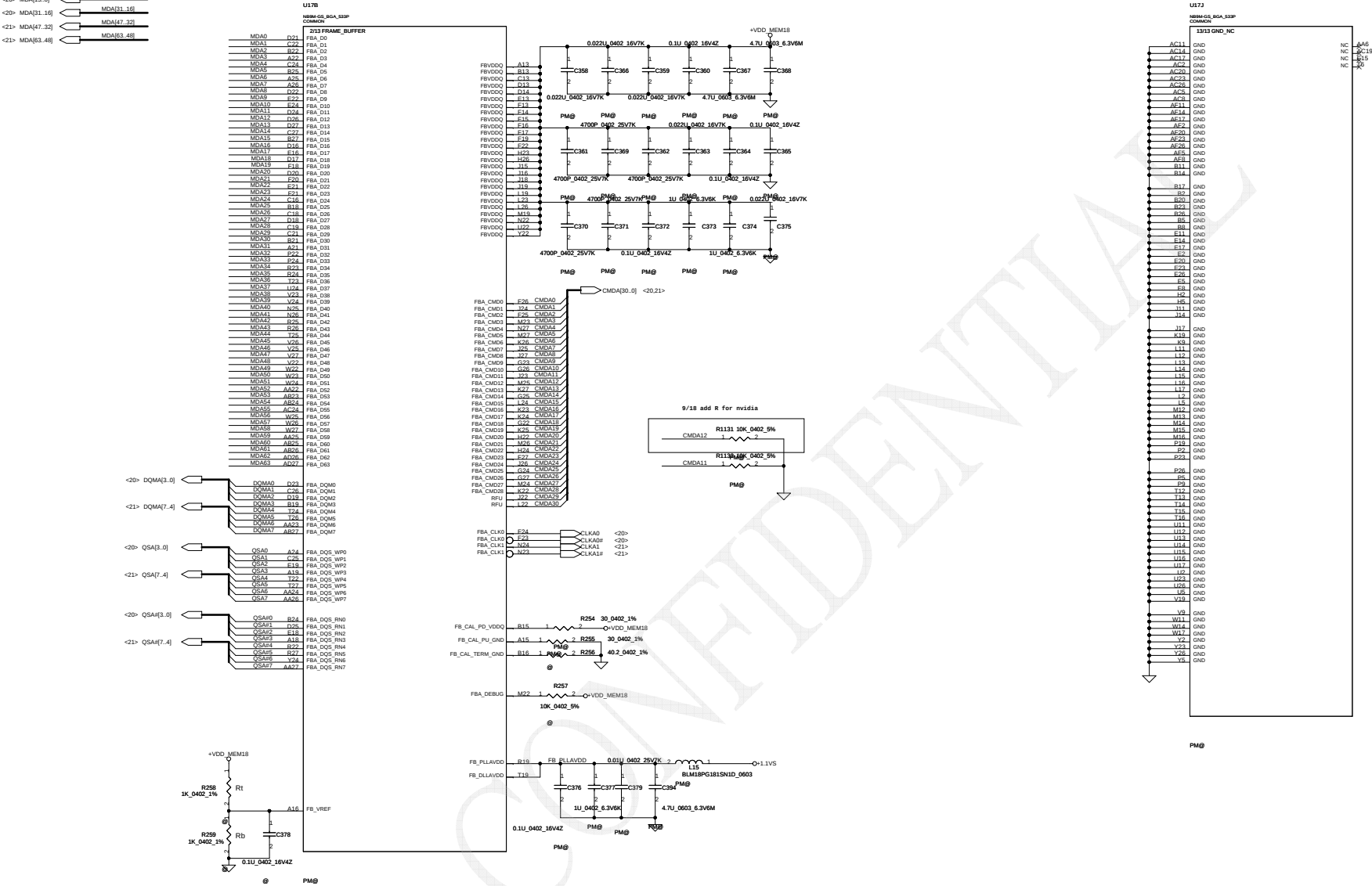
LVDS & DAC Interface

PEG Interface



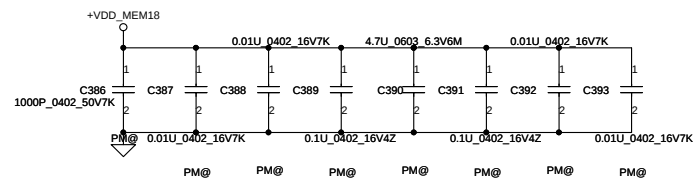
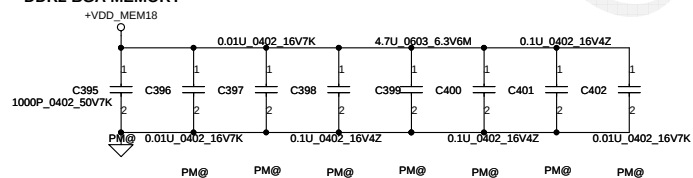
VRAM Interface

- <20> MDA[15..0]
- <20> MDA[31..16]
- <21> MDA[47..32]
- <21> MDA[63..48]



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Size	Custom	Document Number	401597	Rev	C
Date	Friday, October 31, 2008	Sheet	19	of	62

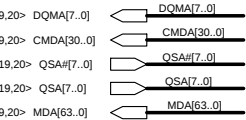
64Mx16 DDR2 400MHz*4==>512MB



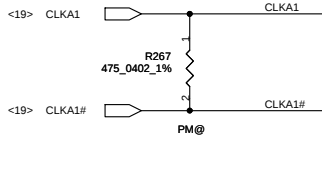
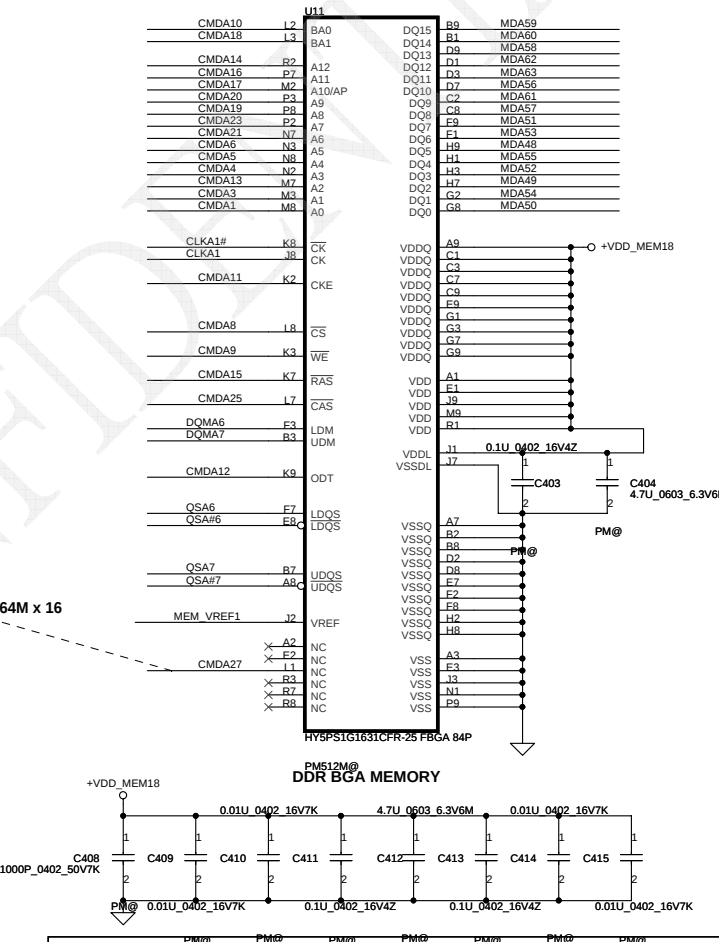
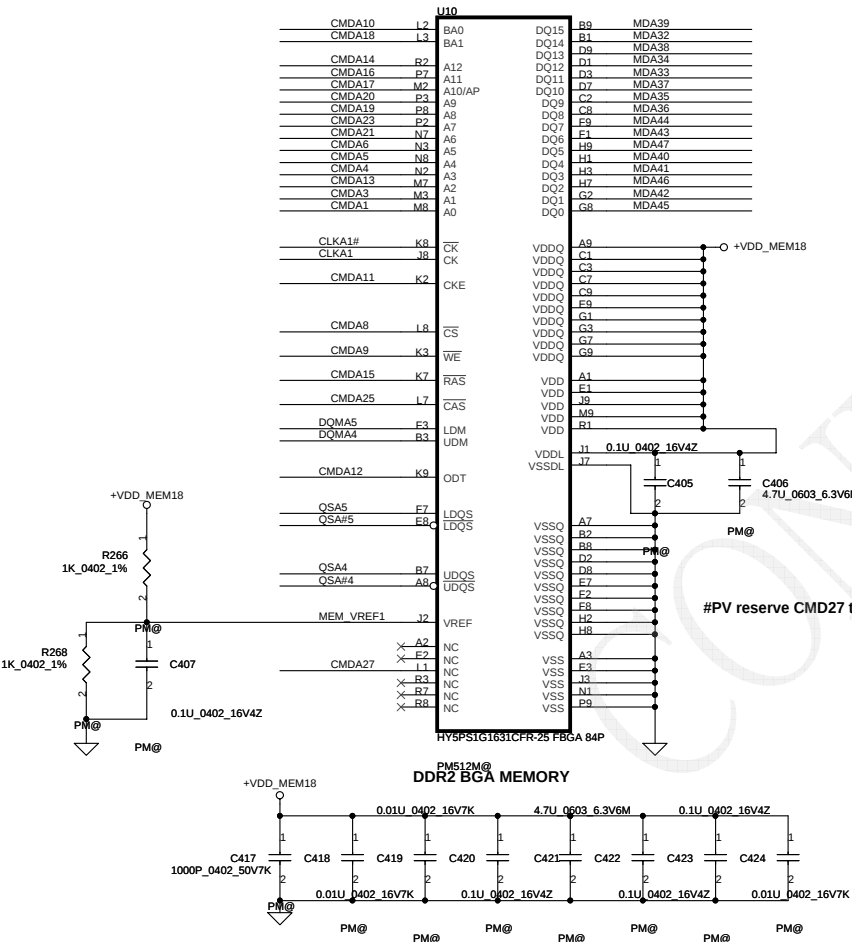
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

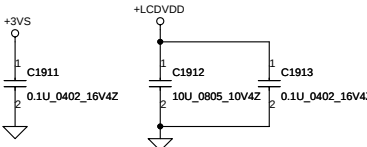
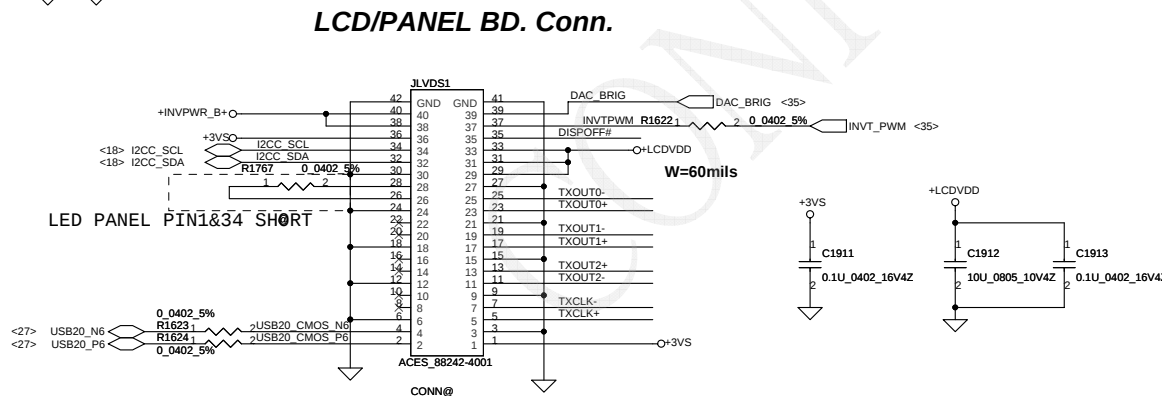
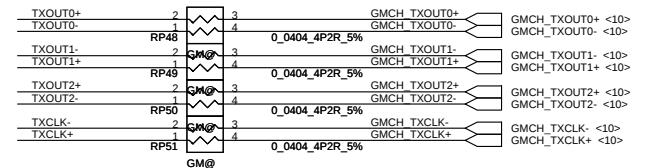
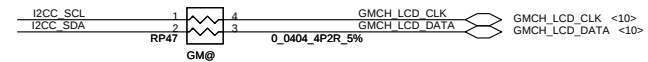
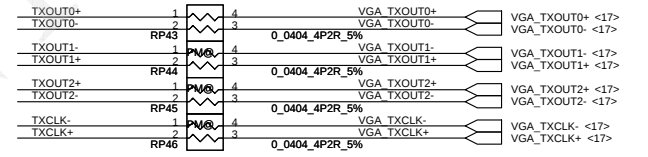
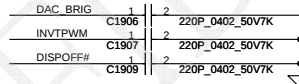
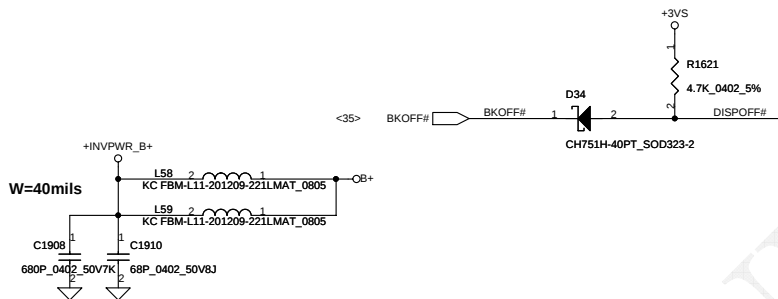
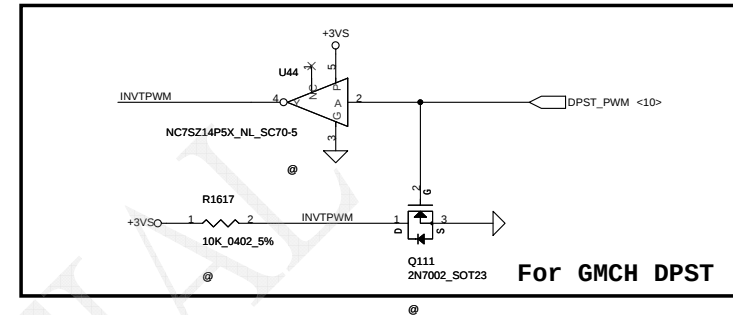
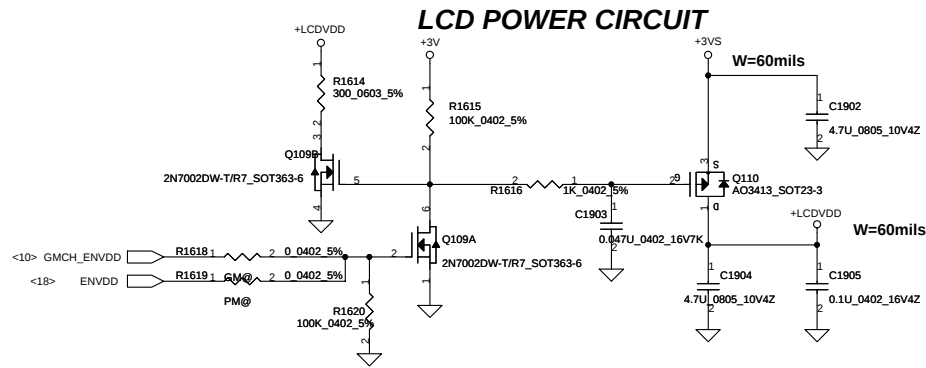
64Mx16 DDR2 400MHz*4==>512MB



DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

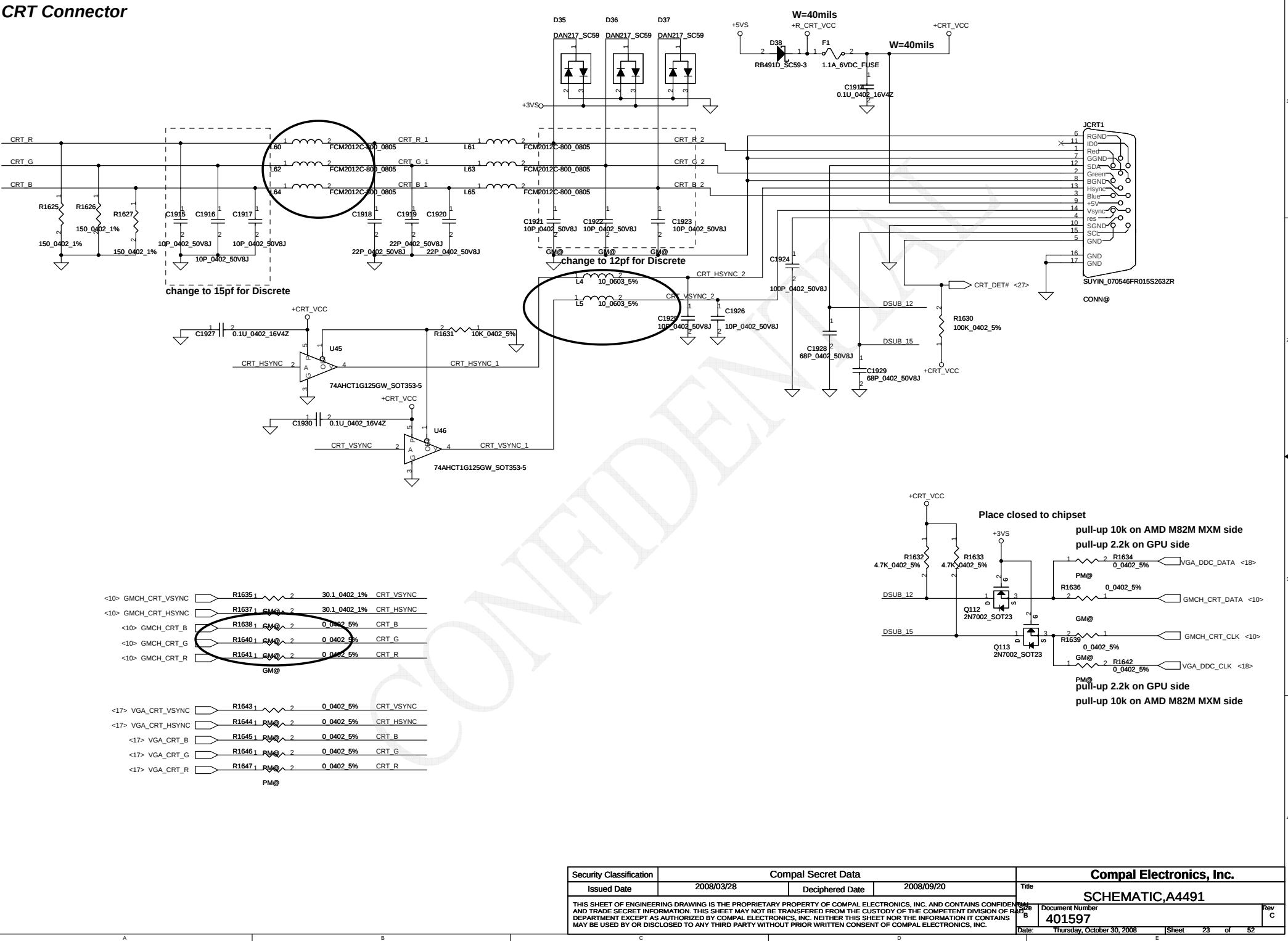


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Date								Document Number	Rev
Friday, October 31, 2008								401597	C
Sheet								21	of 52

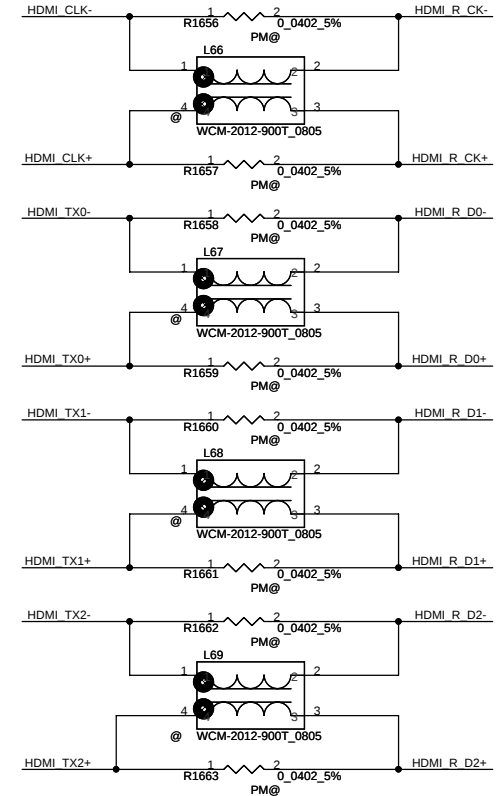
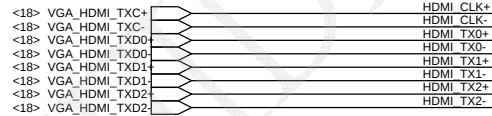
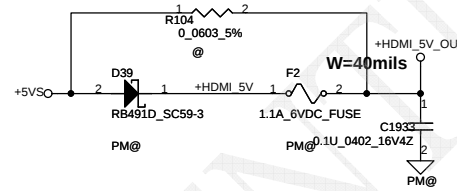
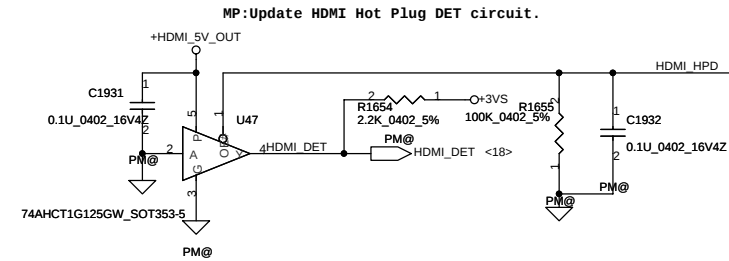
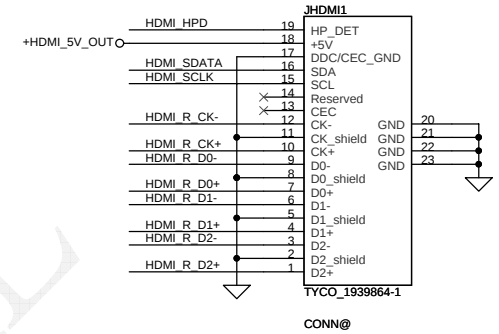
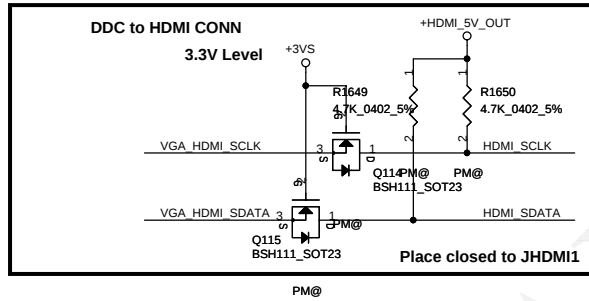
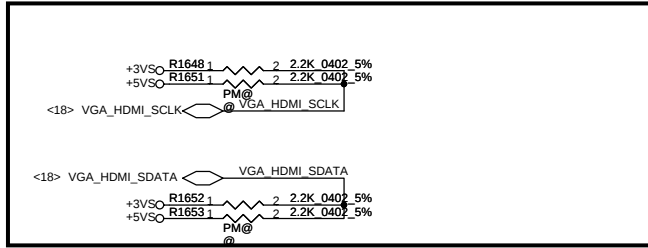


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				Document Number				401597			
				Rev				C			
				Date:				Thursday, October 30, 2008			
				Sheet				22 of 52			

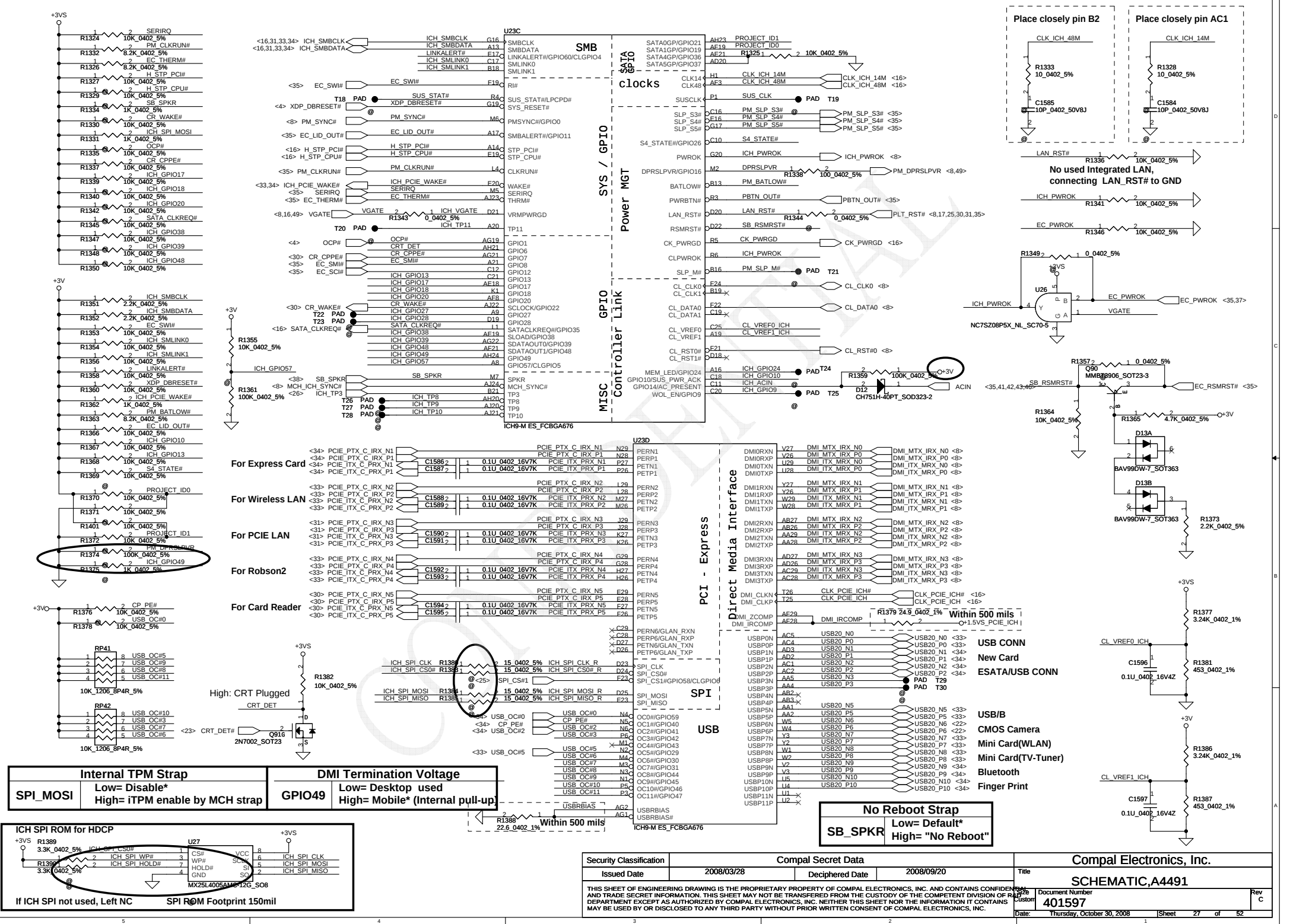
CRT Connector



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				SCHEMATIC,A4491			
				Document Number		Rev	
				401597		C	
				Date:		Thursday, October 30, 2008	
				Sheet		23 of 52	



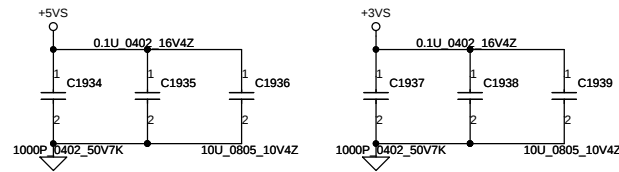
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				Date	Thursday, October 30, 2008
				Sheet	24 of 52



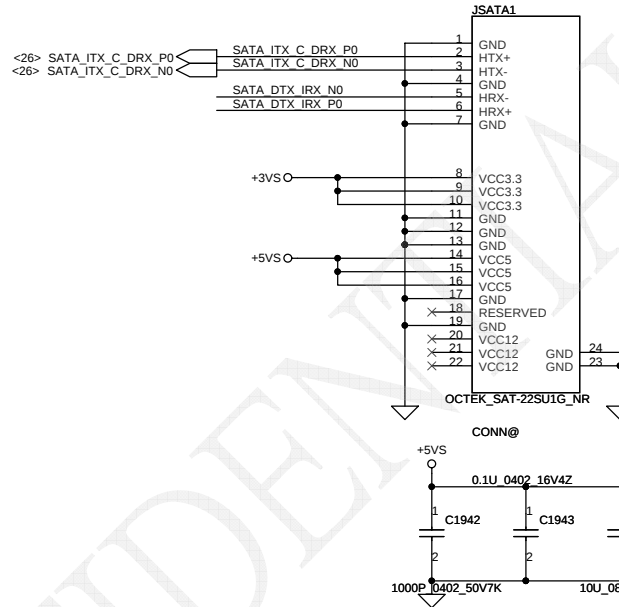
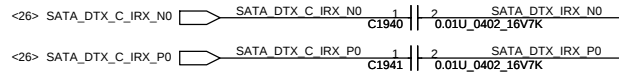
Internal TPM Strap		DMI Termination Voltage	
SPI_MOSI	Low= Disable* High= iTPM enable by MCH strap	GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

No Reboot Strap
SB_SPKR Low= Default*
High= "No Reboot"

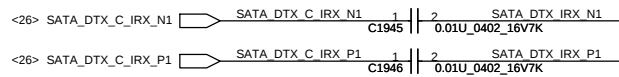
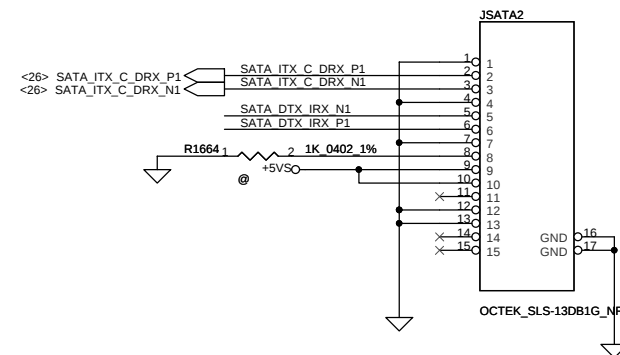
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Customer		401597	
Date		Thursday, October 30, 2008	
Sheet		27 of 52	



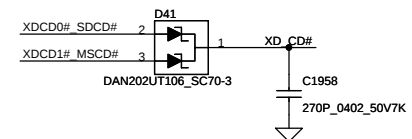
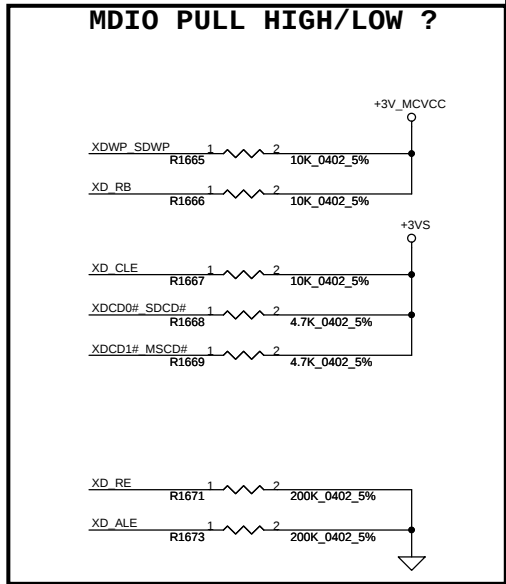
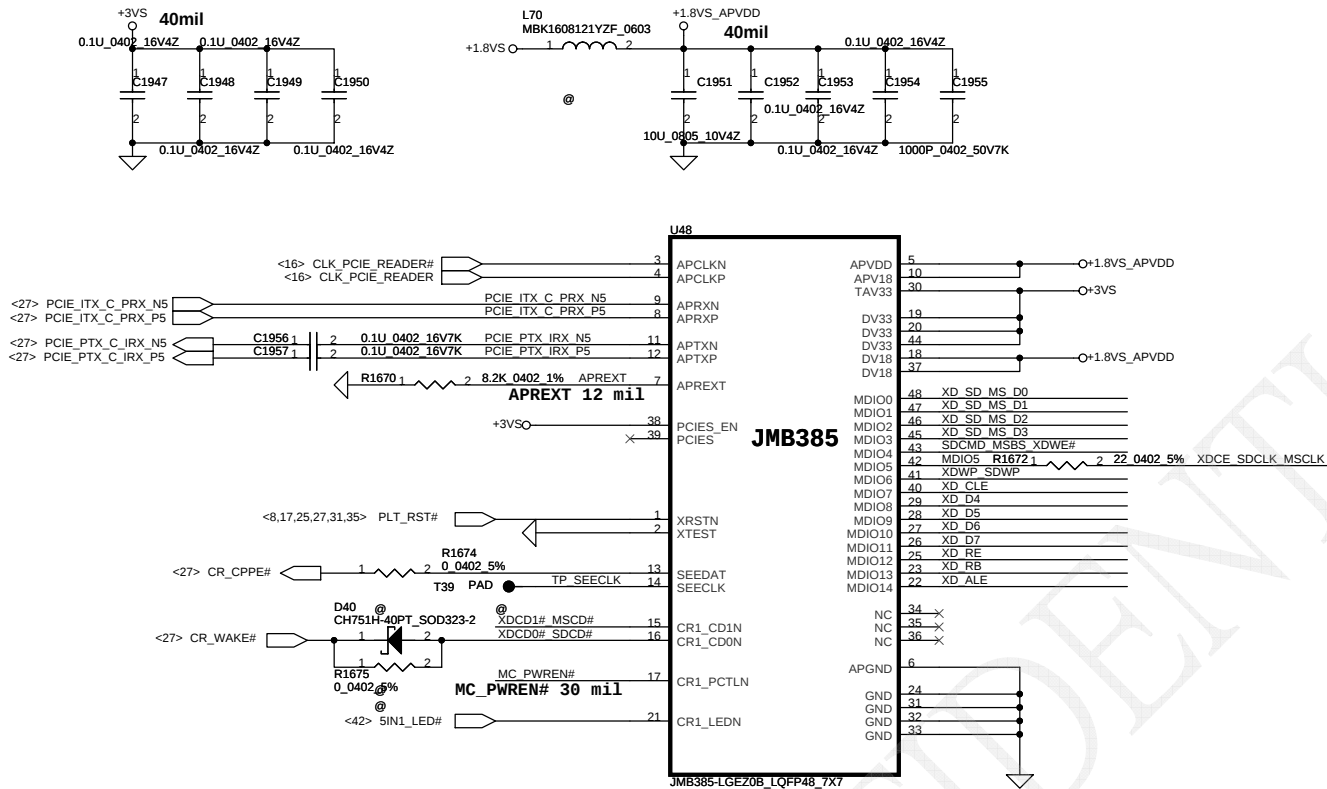
SATA HDD Conn.



SATA ODD Conn.

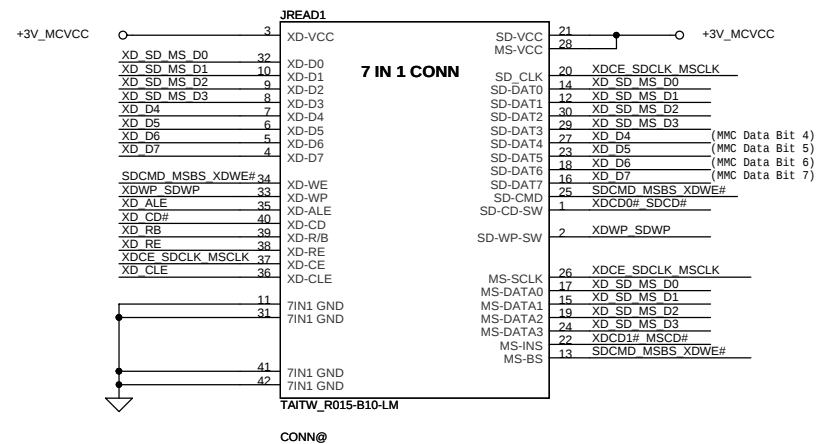
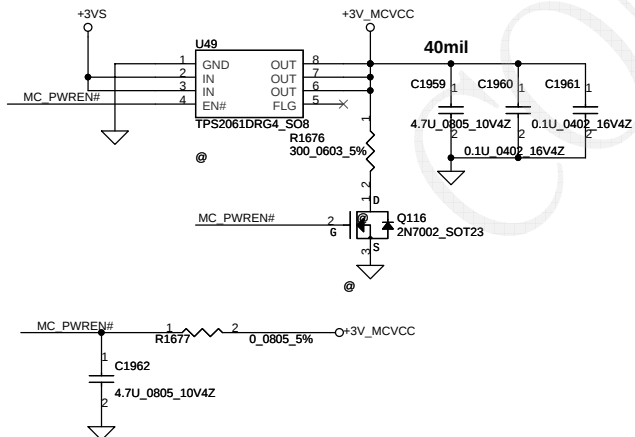


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				Date	Thursday, October 30, 2008
				Sheet	29 of 52
				Rev	C



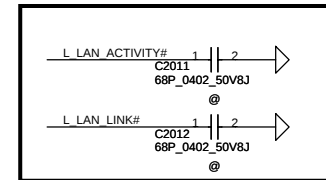
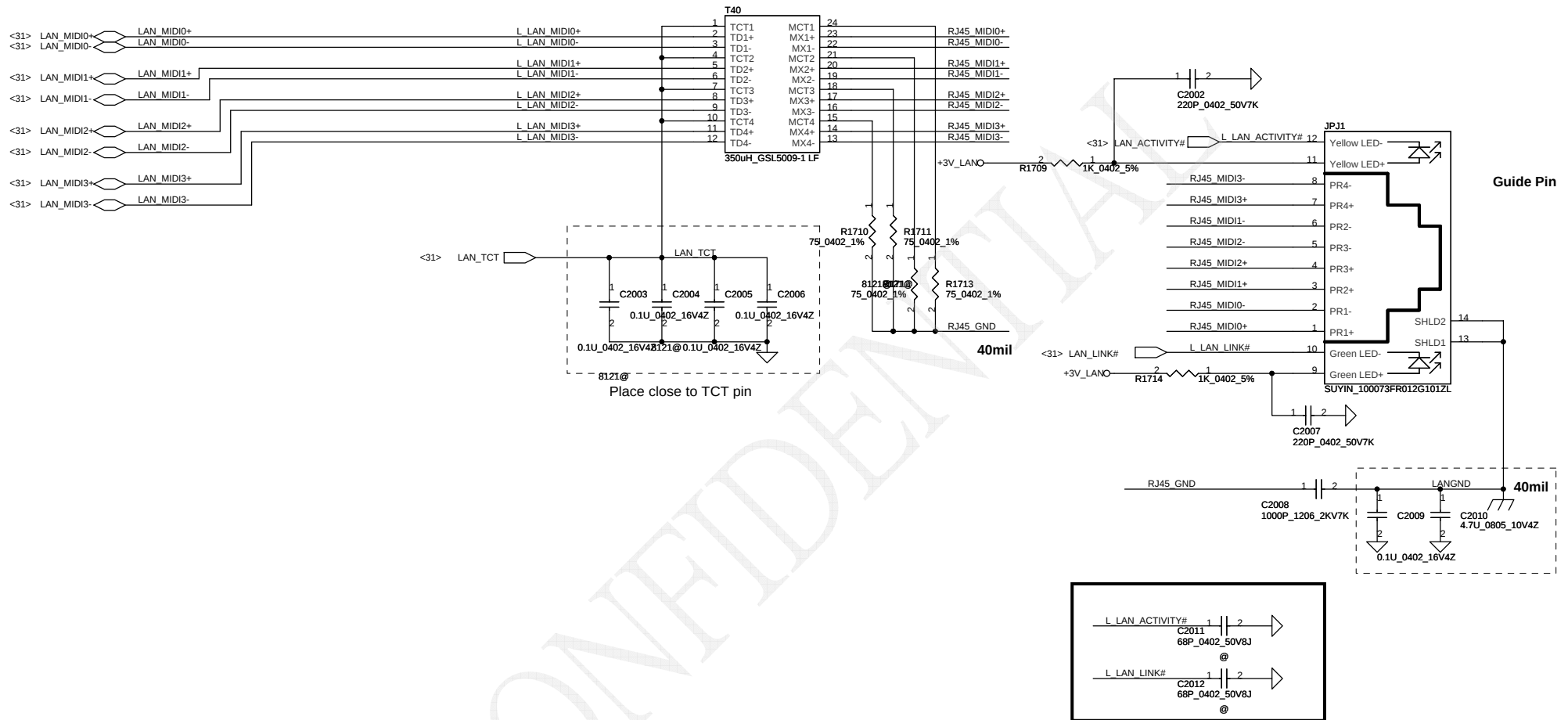
4 IN 1 Socket Push Type(New)

Memory Card Power Switch



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Date:	Thursday, October 30, 2008	Sheet	30	of	52

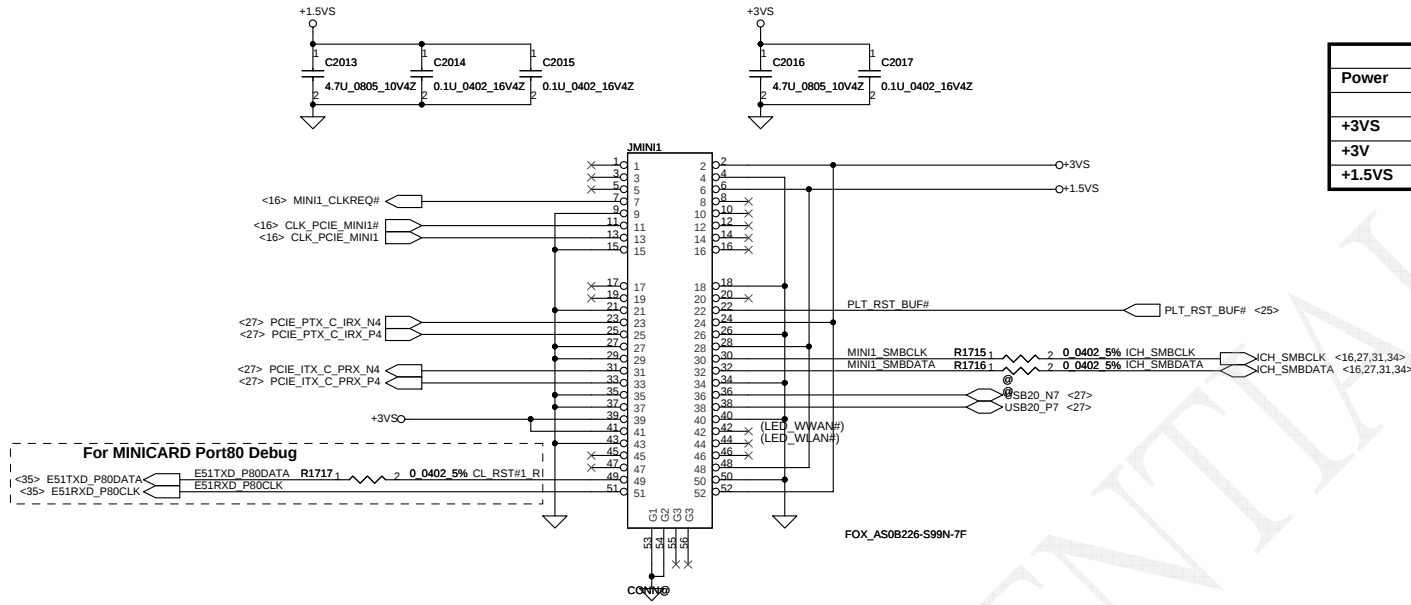
LAN AR8121/8112



For EMI

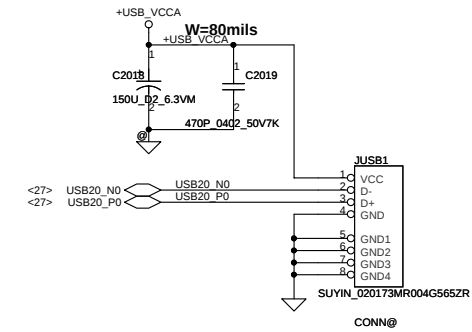
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				Date	Thursday, October 30, 2008
				Sheet	32 of 52

For Robson2

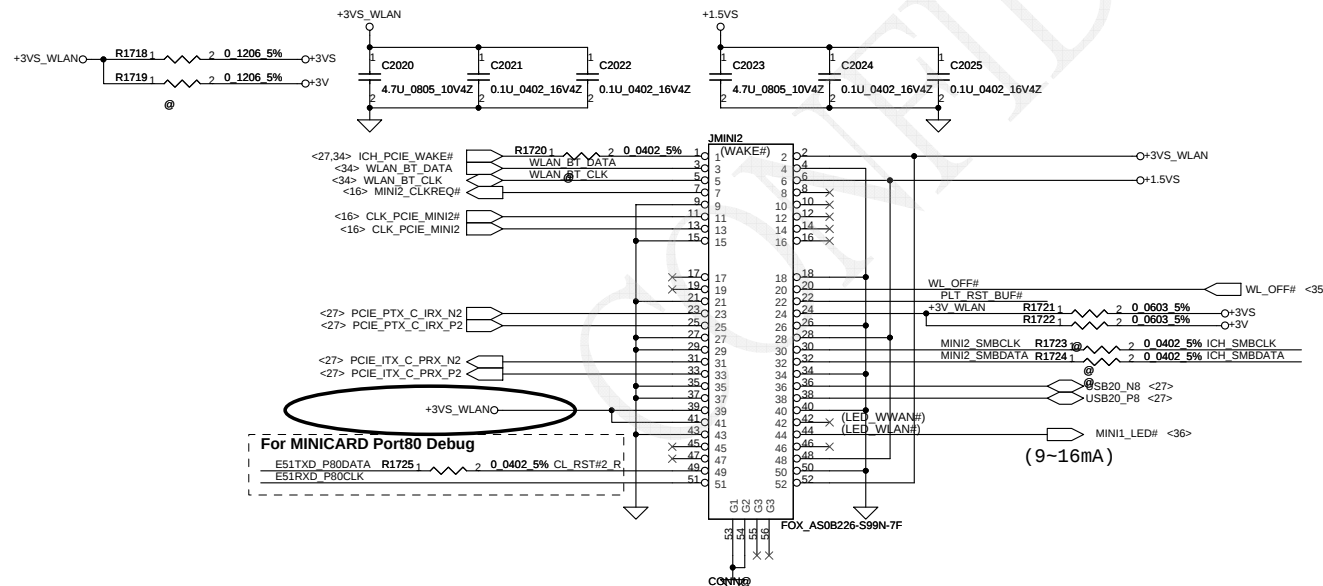


Power	Mini Card Power Rating		Auxiliary Power (mA)
	Peak	Normal	
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

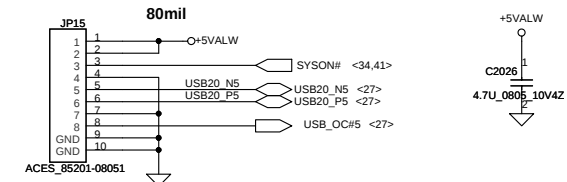
USB CONN.



For Wireless LAN



To USB/B Connector



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				Document Number	401597
				Date	Thursday, October 30, 2008
				Sheet	33 of 52

U52

40mil

60mils

40mil

<25> PCI_RST#

<35,41,47> SYSON

<35,37,41,50> SUSP#

CP PE#

CP USB#

(Internal Pull High to AUXIN)

RCLKEN1

1.5Vin

1.5Vout

3.3Vin

3.3Vout

AUX_IN

SYSRST#

SHDN#

STBY#

CPPE#

CPUSB#

RCLKEN

11

13

3

5

15

19

8

16

7

21

+1.5VS_CARD

+3VS_CARD

+3VALW_CARD

PERST1#

NC

GND

Thermal_Pad

G577NSR91U_TQFN20_4x4

+3VS

C2034

10U_0805_10V4Z

+3V

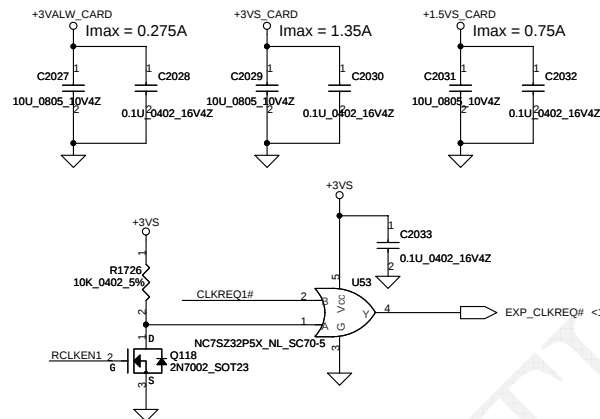
C2035

10U_0805_10V4Z

+1.5VS

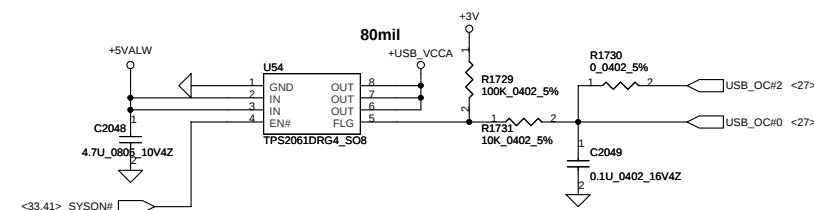
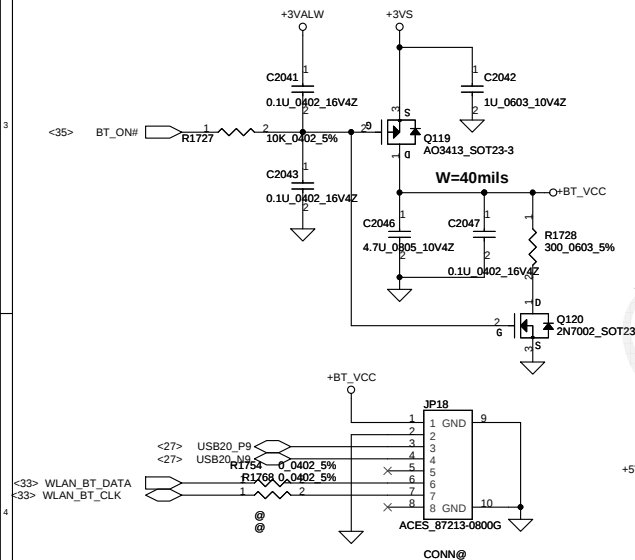
C2036

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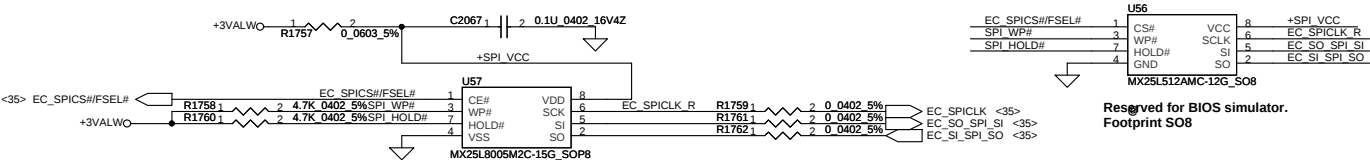
[illegible]

The diagrams illustrate the electrical connections for three components, D59, D60, and D61, which are identified as PRTR5V0U2X_SOT143-4.

- Component D59:**
 - PIN (Pin 4) is connected to +USB_VCCA.
 - IO1 (Pin 2) is connected to USB20_P2.
 - IO2 (Pin 3) is connected to USB20_N2.
 - GND (Pin 1) is connected to ground.
- Component D60:**
 - PIN (Pin 4) is connected to +5VALW.
 - IO1 (Pin 2) is connected to SATA_ITX_C_DRX_P5.
 - IO2 (Pin 3) is connected to SATA_ITX_C_DRX_N5.
 - GND (Pin 1) is connected to ground.
- Component D61:**
 - PIN (Pin 4) is connected to +5VALW.
 - IO1 (Pin 2) is connected to SATA_IRX_DTX_N5.
 - IO2 (Pin 3) is connected to SATA_IRX_DTX_P5.
 - GND (Pin 1) is connected to ground.

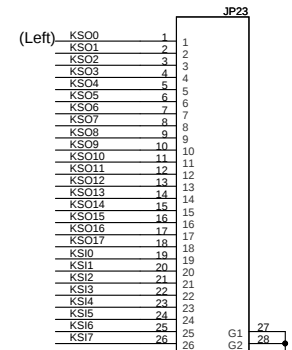
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				401597	
Date	Thursday, October 30, 2008	Sheet	34	of	52



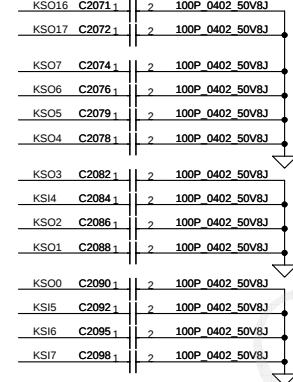
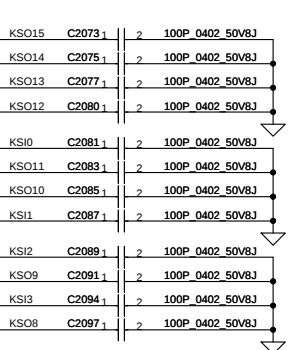
ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

INT_KBD Conn.

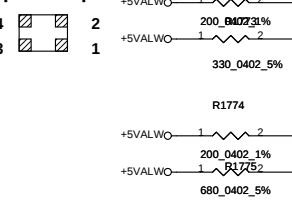


(Left)

(Right)

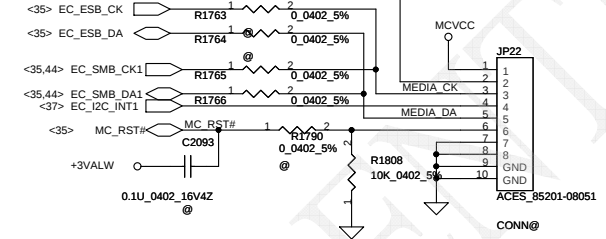


Compal Footprint



footprint not right

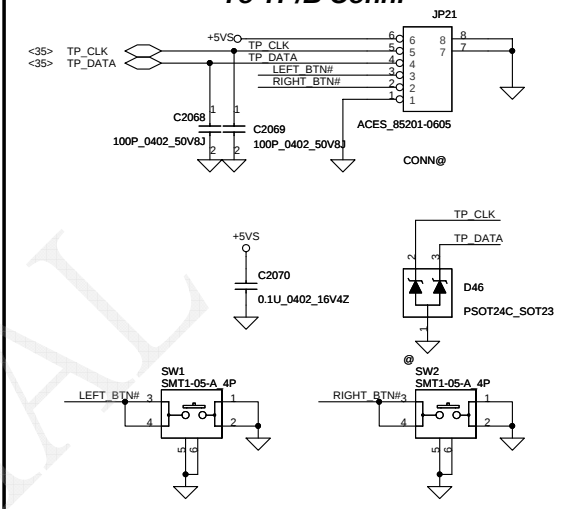
To Media/B Conn.



To BTN/B Conn.

	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#

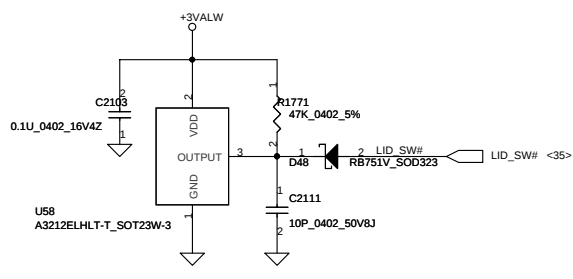
To TP/B Conn.



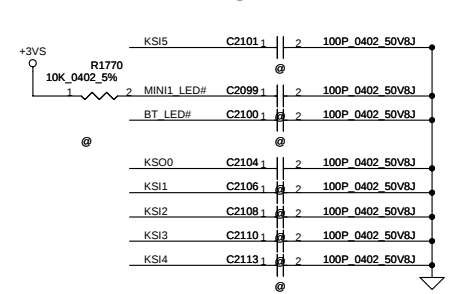
e-key/B



Lid Switch (Hall Effect Switch)

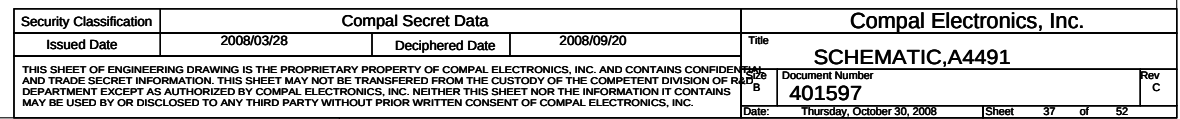


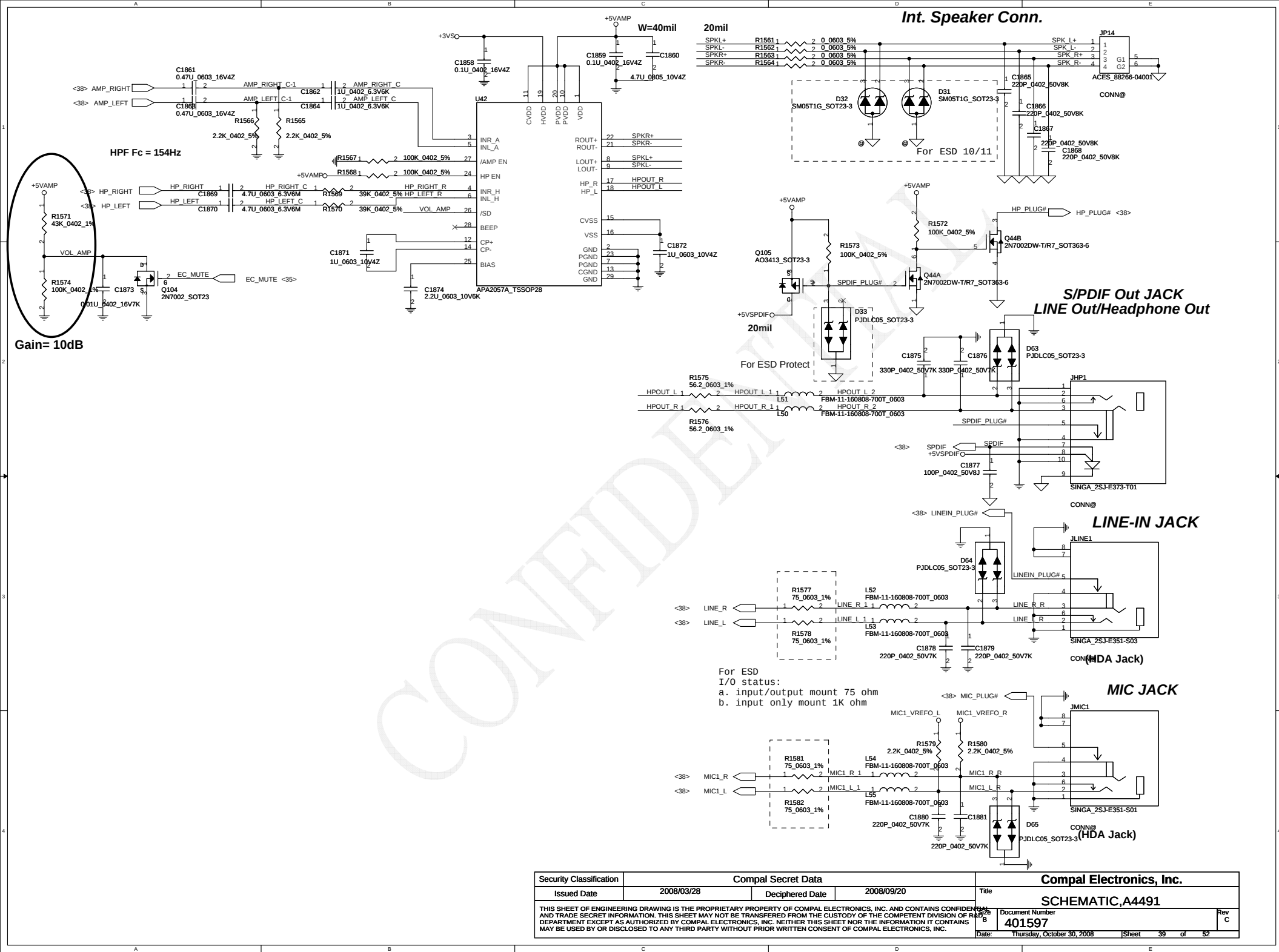
FOR EMI



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				Rev C
				Date: Thursday, October 30, 2008 Sheet 36 of 52

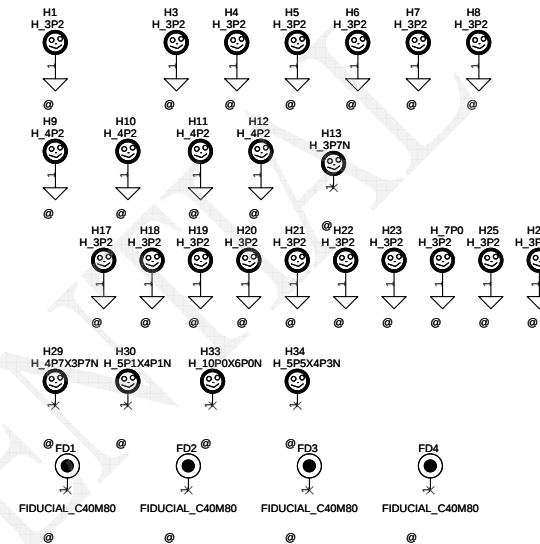
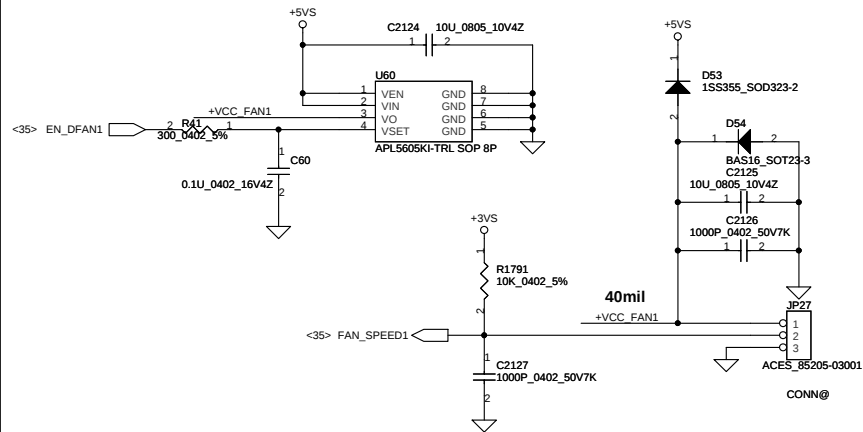
ON/OFF switch



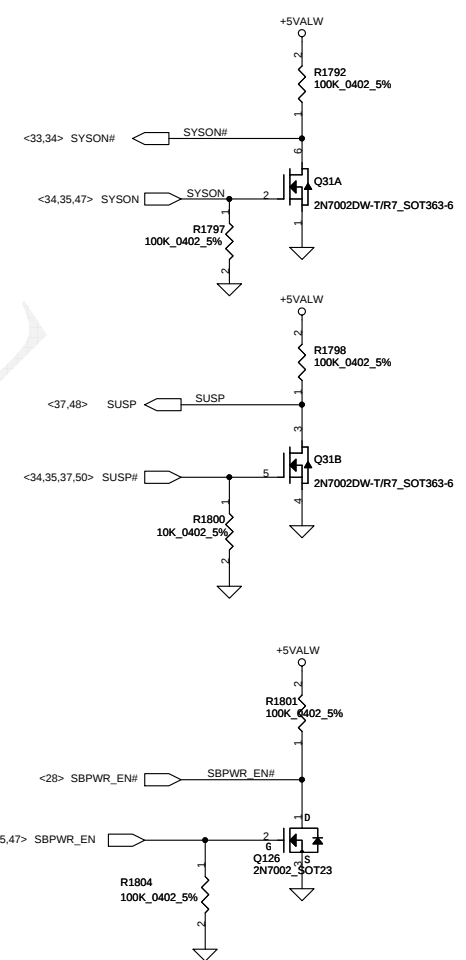
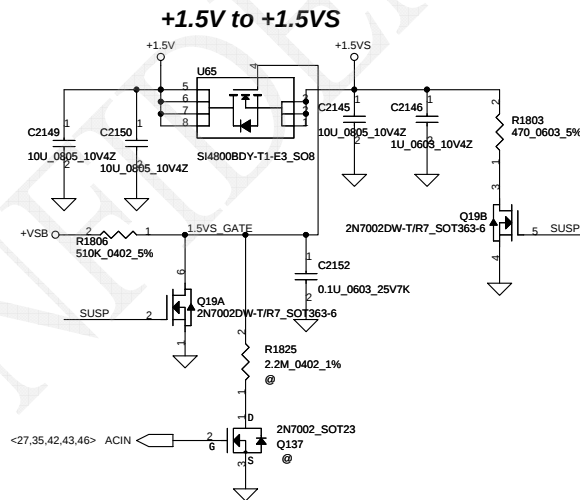
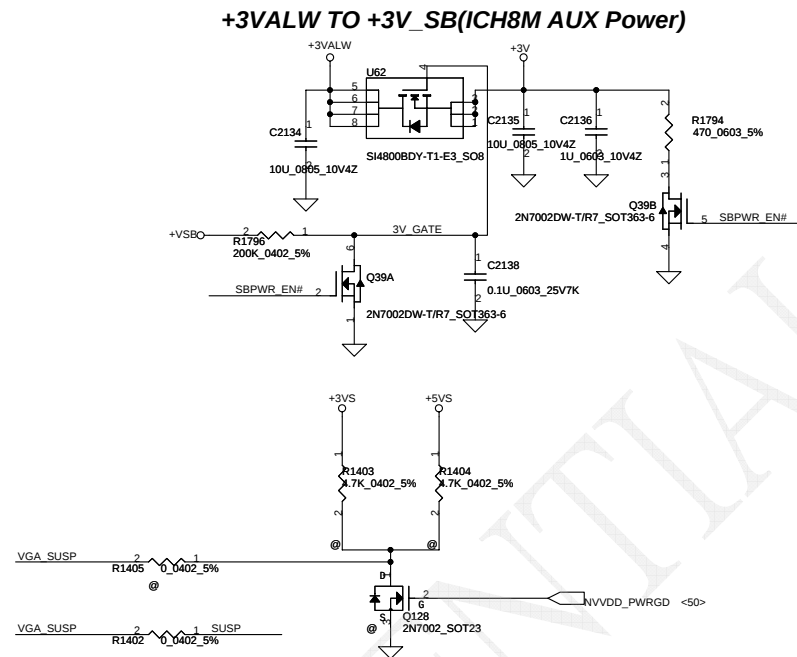
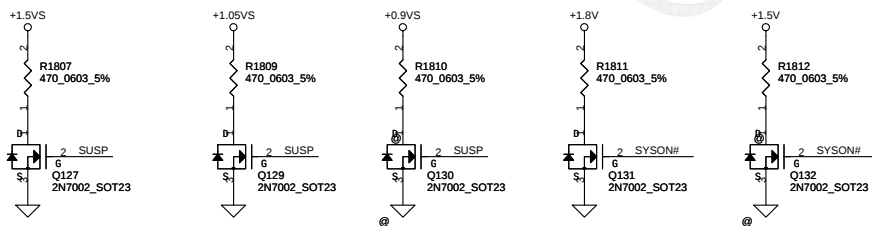


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				Date:	Thursday, October 30, 2008
				Sheet	39 of 52
				Rev	C

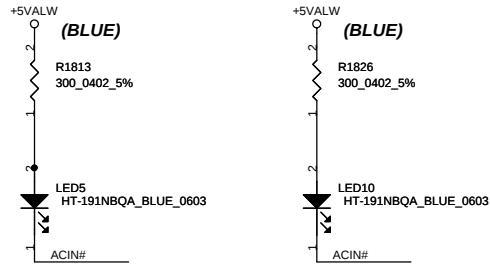
FAN1 Conn



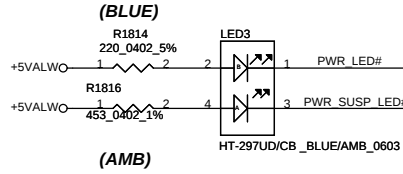
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				Date:	Thursday, October 30, 2008
				Sheet	40 of 52



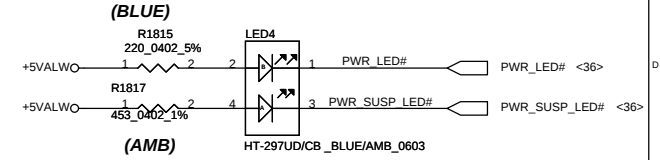
Enlightener LED



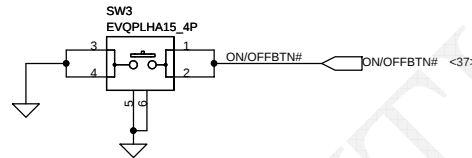
ON/OFF LED LEFT



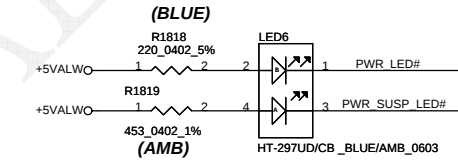
ON/OFF LED RIGHT



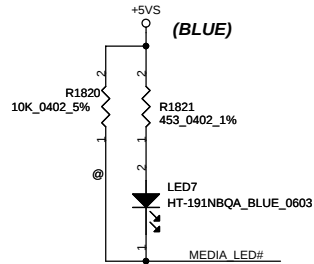
ON/OFF Button



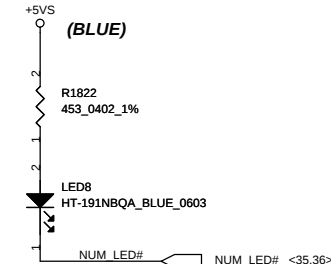
ON/OFF LED DOWN



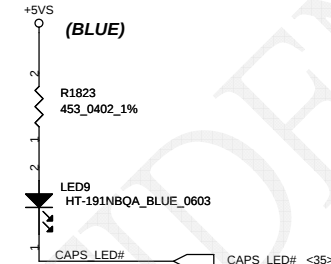
MEDIA_LED



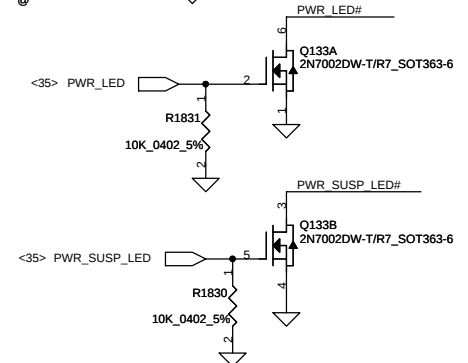
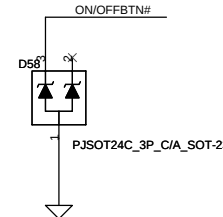
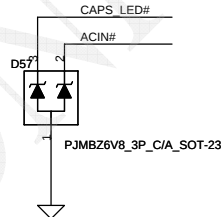
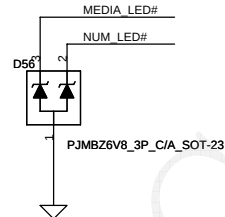
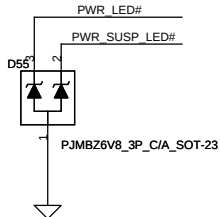
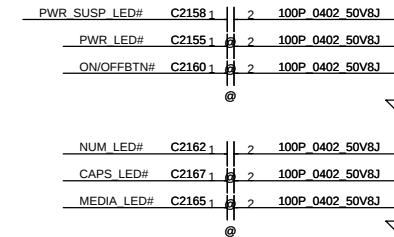
NUM_LED



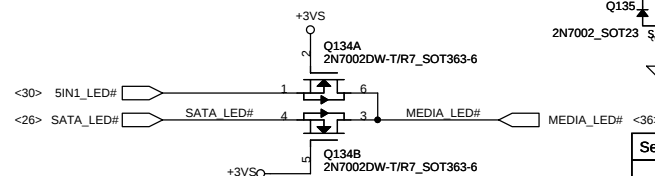
CAPS_LED



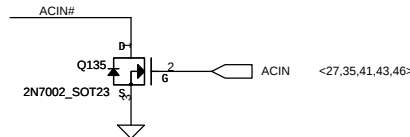
FOR EMI



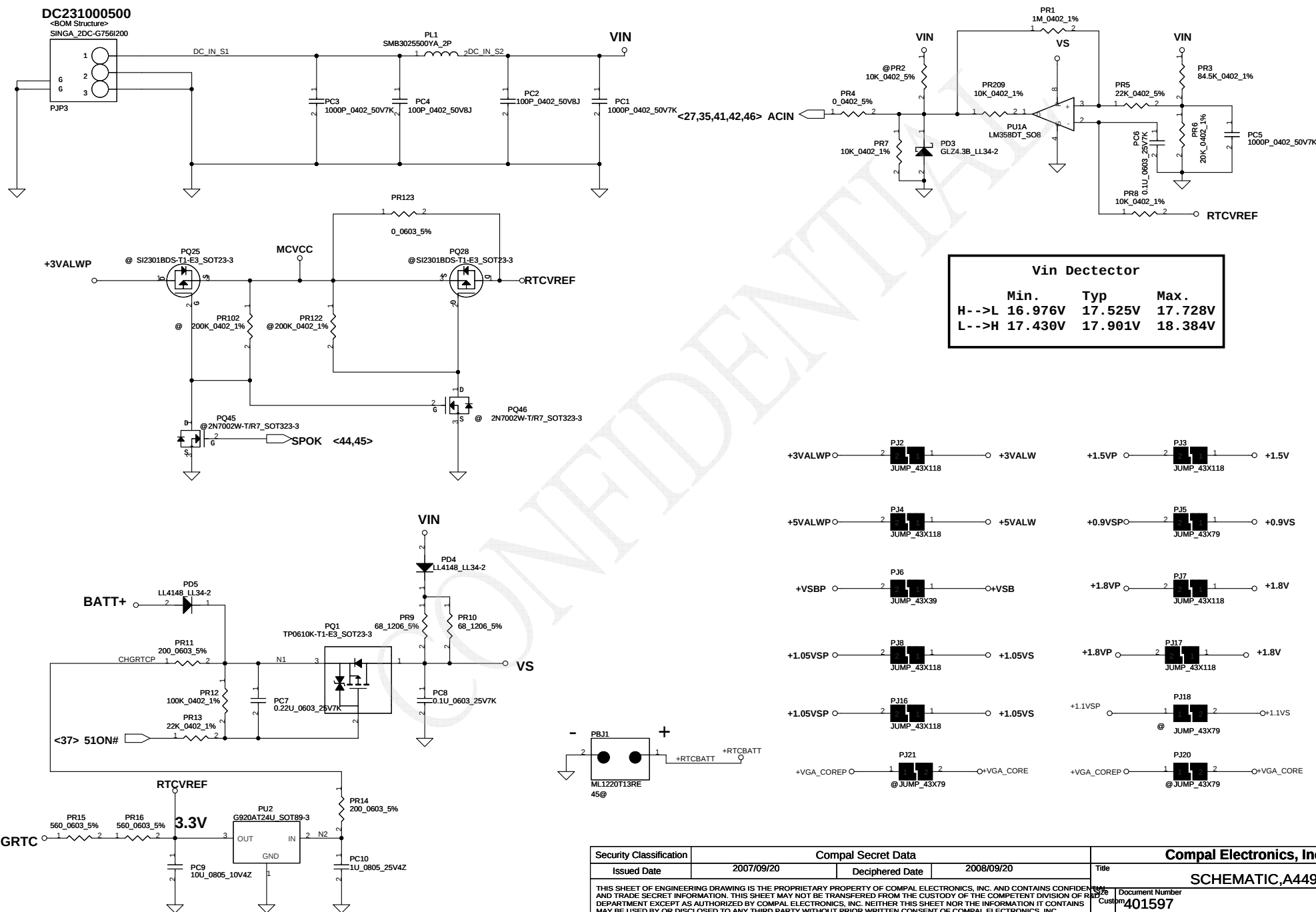
**D1 D2 D3 USE PANJIT PJMBZ6V8
SCA00000I00
6.8V**

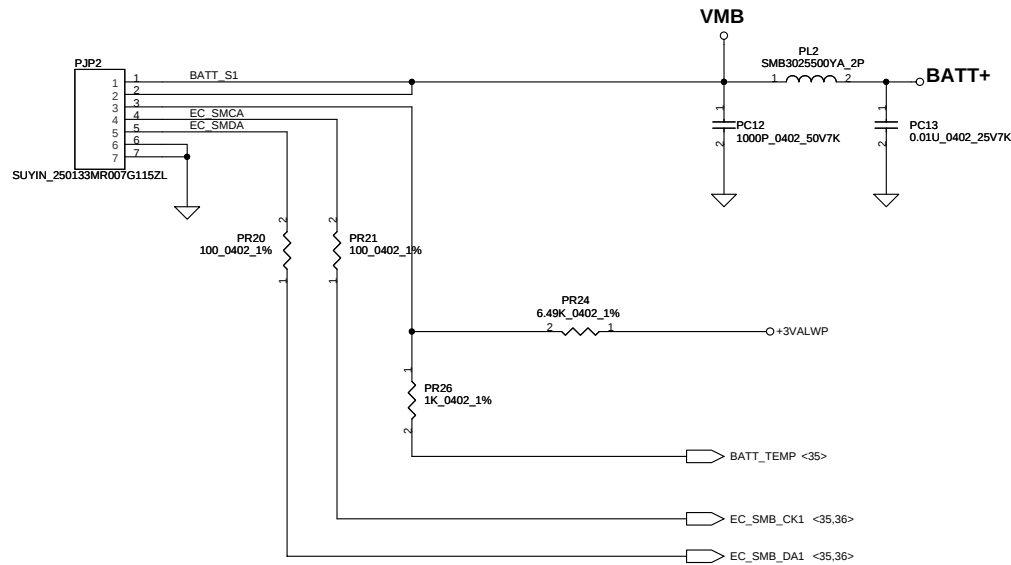


**D4 USE
PJSOT24C 3P C/A SOT-23
SCA00000E00
24V**

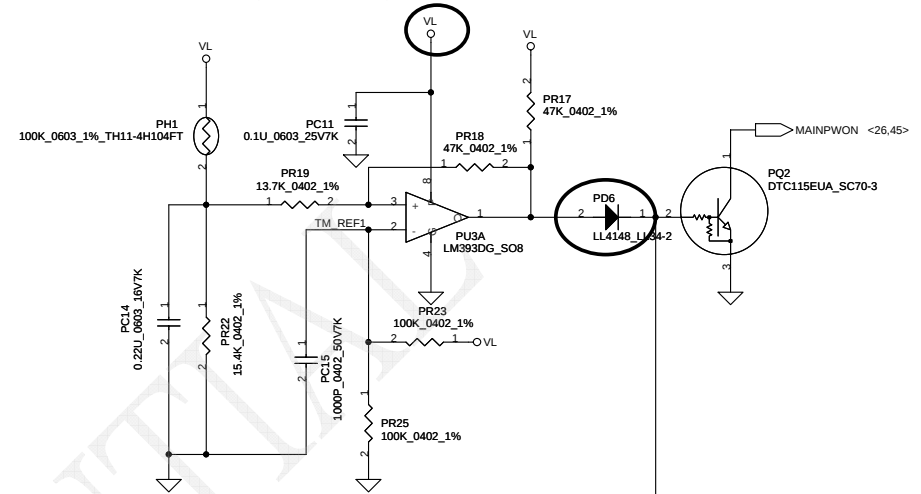


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Date:				Thursday, October 30, 2008				Sheet 42 of 52			

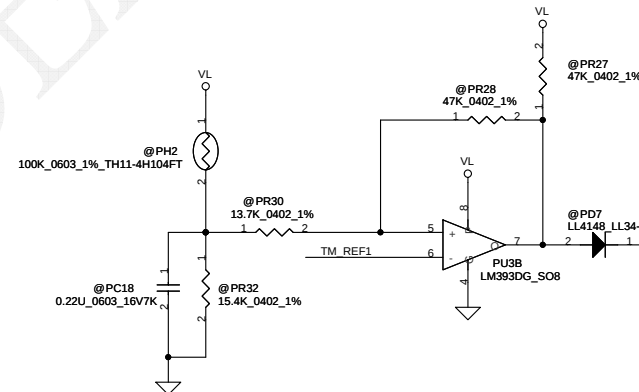
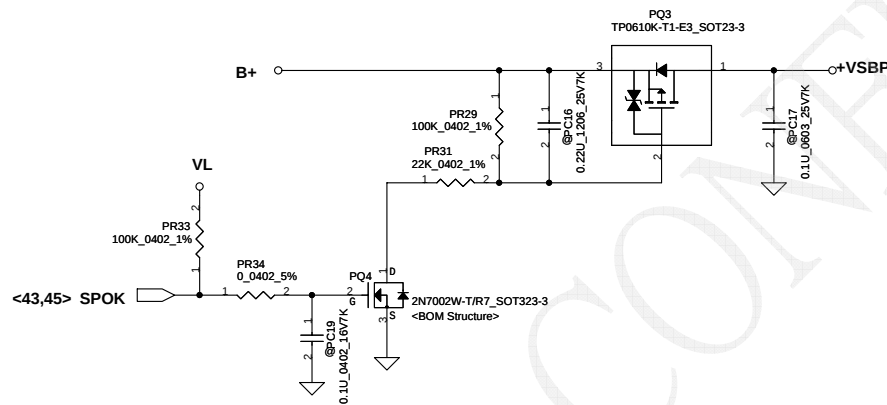




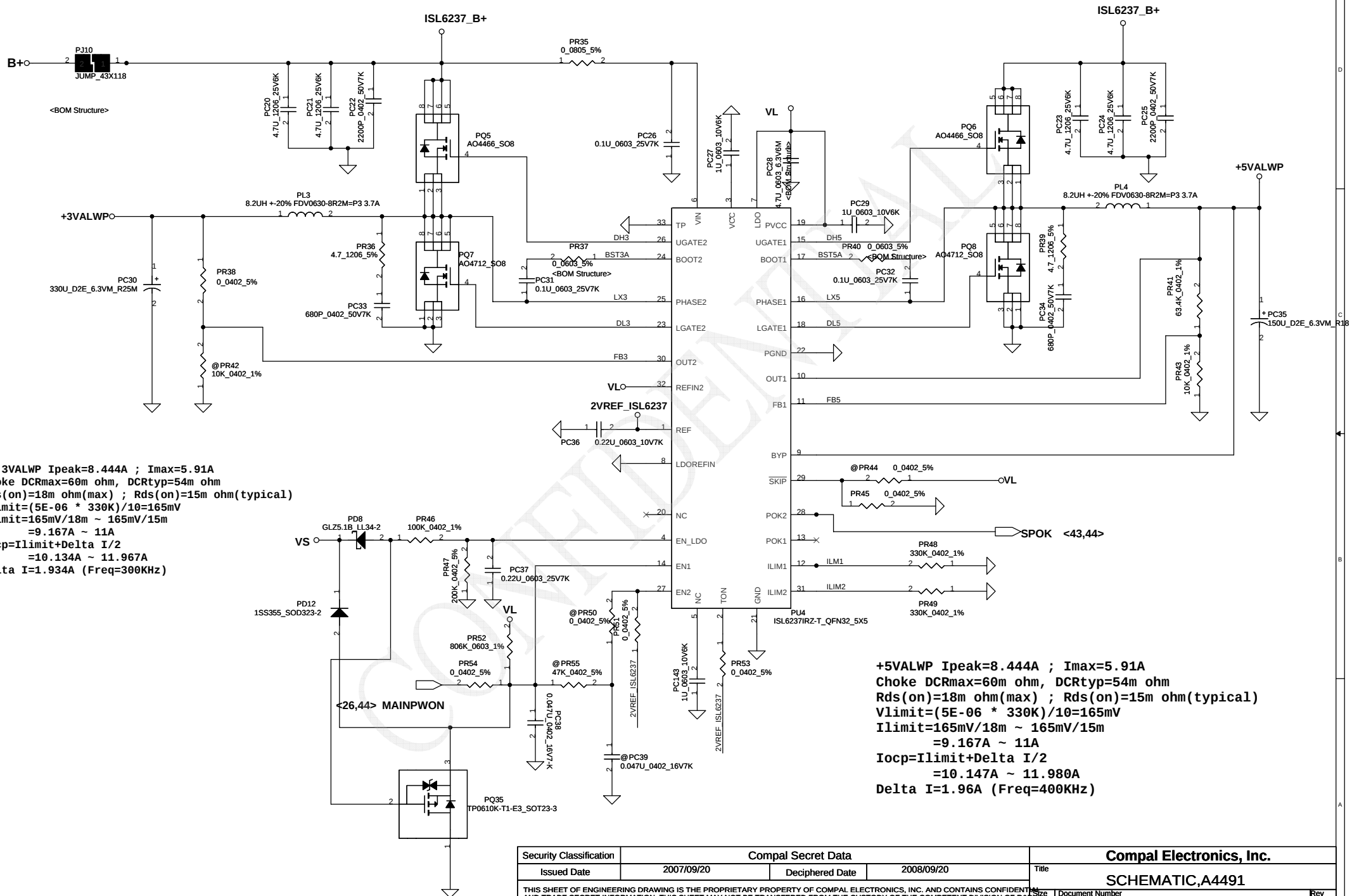
PH1 under CPU botten side :
 CPU thermal protection at 96 degree C
 Recovery at 60 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 47 degree C



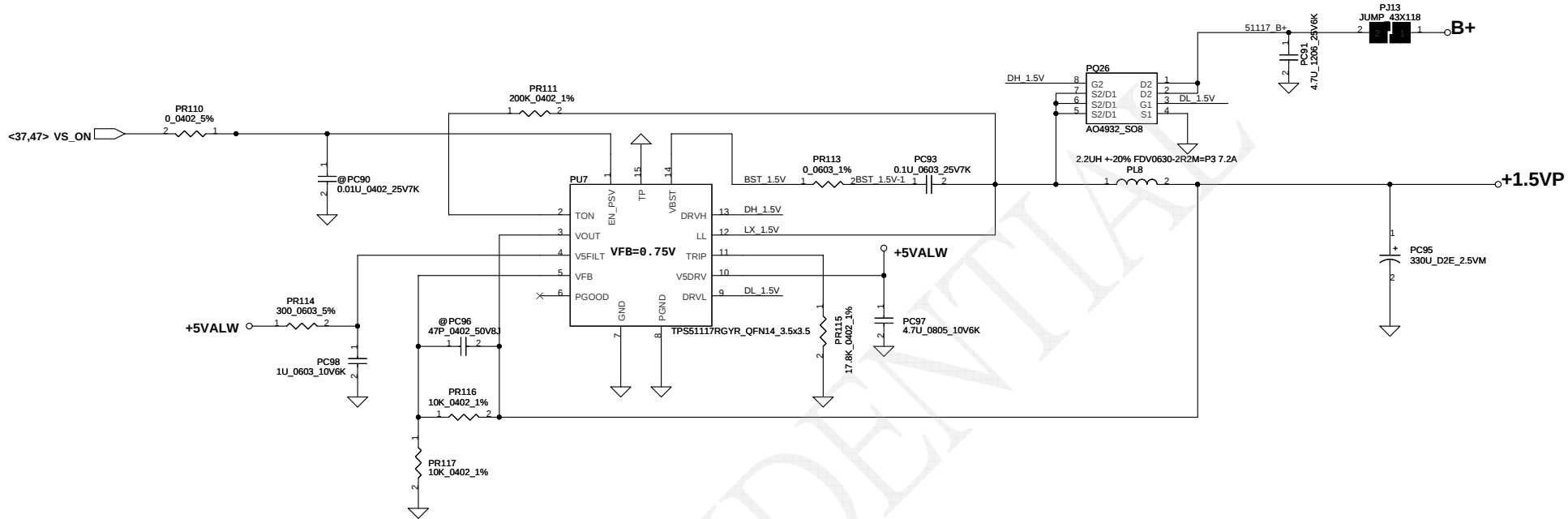
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				Rev	C
				Date:	Thursday, October 30, 2008
				Sheet	44 of 52



+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

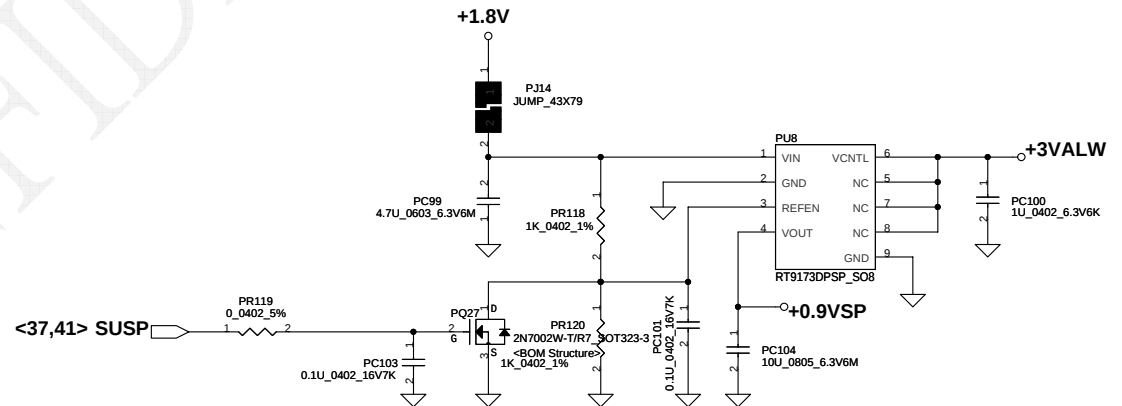
+5VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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				401597	C
Date: Thursday, October 30, 2008				Sheet	52
				45	of



VFB=0.75V
 $V_o = VFB * (1 + PR87 / PR88) = 0.75 * (1 + 4.02K / 10K) = 1.05V$
 $Ton = 200K$
 $Fsw = 400KHz$

Cout ESR=15m ohm
 $I_{peak} = 14.02A$, $I_{max} = 9.81A$
 $\Delta I = ((19 - 1.05) * (1.05 / 19)) / (L * Fsw) = 2.4872A$
 $\Rightarrow 1/2 \Delta I = 1.243A$
 $V_{trip} = R_{trip} * I_{0uA} = 17.8K * 10uA = 0.178V$
 $I_{ocpmin} = V_{trip} / R_{dsonmax} * 1.2 + 1.243A = 0.178 / (0.0115 * 1.2) + 1.243 = 12.898A + 1.243A = 14.141A$
 $I_{ocpmax} = (0.178 / (0.009 * 1.1)) + 1.243A = 17.98A + 1.243A = 19.22A$
 $I_{ocp} = 14.141A - 19.22A$



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				401597
				Rev C
				Date: Thursday, October 30, 2008
				Sheet 48 of 52

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	cpu load line fail	Measure cpu load line can't fit spec	0.2	49	change the resistance value of pr173.from 4.42k to 3.83k	2008/08/08	DVT
2	Change resistance size	EMI request	0.2	49	Change pc116 and pc117 size from 0402 to 0603	2008/08/08	DVT
3	Change p-mos part number	Vender change EOL	0.2	46	PQ12 part number from 4835bdy to 483500y	2008/08/08	DVT
4	Change device size	device too large can't fit layout space	0.2	44-50	PQ4, PQ14, PQ16, PQ18, PQ19, PQ20, PQ27, PQ36, PQ37, PQ41, PQ42 change to sot323-3	2008/08/12	DVT
5	Change resistance value	1.05V tranient fail	0.2	47	PR94 from 60.4k to 59k	2008/08/12	DVT
6	change resistance	for hdmi	0.2	45	pr41 change from 61.3k to 63.4k	2008/08/14	DVT

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A --> B Change List

7/16 -----
Page 41 Update U61,U62,U63,U65 Change SI4800BDY
Page 41 Change 910K

Page 41 Update R1405,R1403,R1404 with BOM Structure @
7/23 -----
Page 23 Change C1918,C1919,C120 10P
Page 23 DEL C1915, C1916,C1917 with BOM Structure PM@
Page 6, Add C416,C425,C426,C427,C428,C429,C430,C431 10U_0805
Page 12,Change C1501 22U to 220U
7/30 -----
Page 36 Add C2071,C2072,C2073,C2074,C2075,C2076,
C2077,C2078,C2079,C2081,C2082,C2083
,C2084,C2085,C2086,C2087,C2088,C2089,
C2090,C2091,C2092,C2093,C2094,C2095,
C2096,C2097,C2098
7/30 -----
Page 28 DEL R1395,R1397
Page 28 Change R1394,R1396 with BOM Structure
8/7 -----
Page 38 DEL L48
Page 38 Update R1534 with BOM Structure
Page 39 Add D63,D64,D65
Page 39 Update JHP1 PIN6 AND PIN10 to GND
Page 39 Update JLINE1 PIN6 to GND
Page 39 Update JM1C1 PIN6 to GND
8/13 -----
Page 31 DEL U50
Page 33 Change JP15 PIN5 (USB20_P5) to PIN6
Page 33 Change JP15 PIN6 (USB20_N5) to PIN5
8/14 -----
Page 37 Add R1776
Page 37 DEL R1778
Page 40 DEL H16
Page 40 Add H34

B--> C Change List

0920-----
Page 6, Change R1678,R1679,R1682,R1683,R1684,R1687,R1689,R1691 to SD034499A80

1009-----
Page 37,Add
R1838,R1837 to 10K
R1836 to 510k
Q124,Q138 to 2N7002
D47 to 1SS355

1015-----
Page 36, Change
R1772,R1774 to 220R
R1773 to 330R
R1775 to 680R

Page 42, Change
R1814,R1815,R1818 to 220R

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				Rev C	
Date: Thursday, October 30, 2008				Sheet 52 of 52	