

Compal Confidential

ICL50/51, ICK70/71 Schematics Document

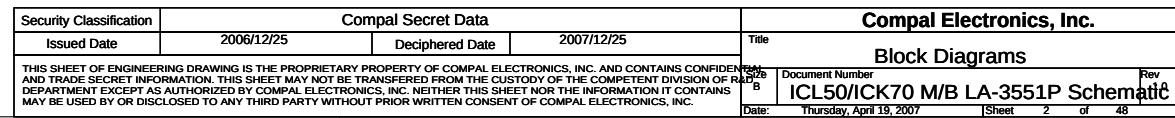
Intel Merom Processor with Crestline(PM965/GM965) + DDRII + ICH8M
(With ATI MXM/B)

2007-4-20

REV: 1A

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/04/04	Deciphered Date	2008/04/04	Title	Cover Page
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				ICL50/ICK70 M/B LA-3551P Schematic	
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Model Name : ICL50/51, ICK70/ICK71
File Name : LA-3551P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394/Card Reader	AD16	0	PIRQE PIRQG

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

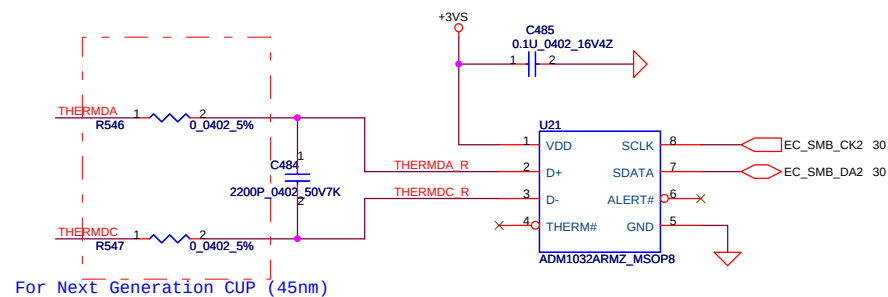
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

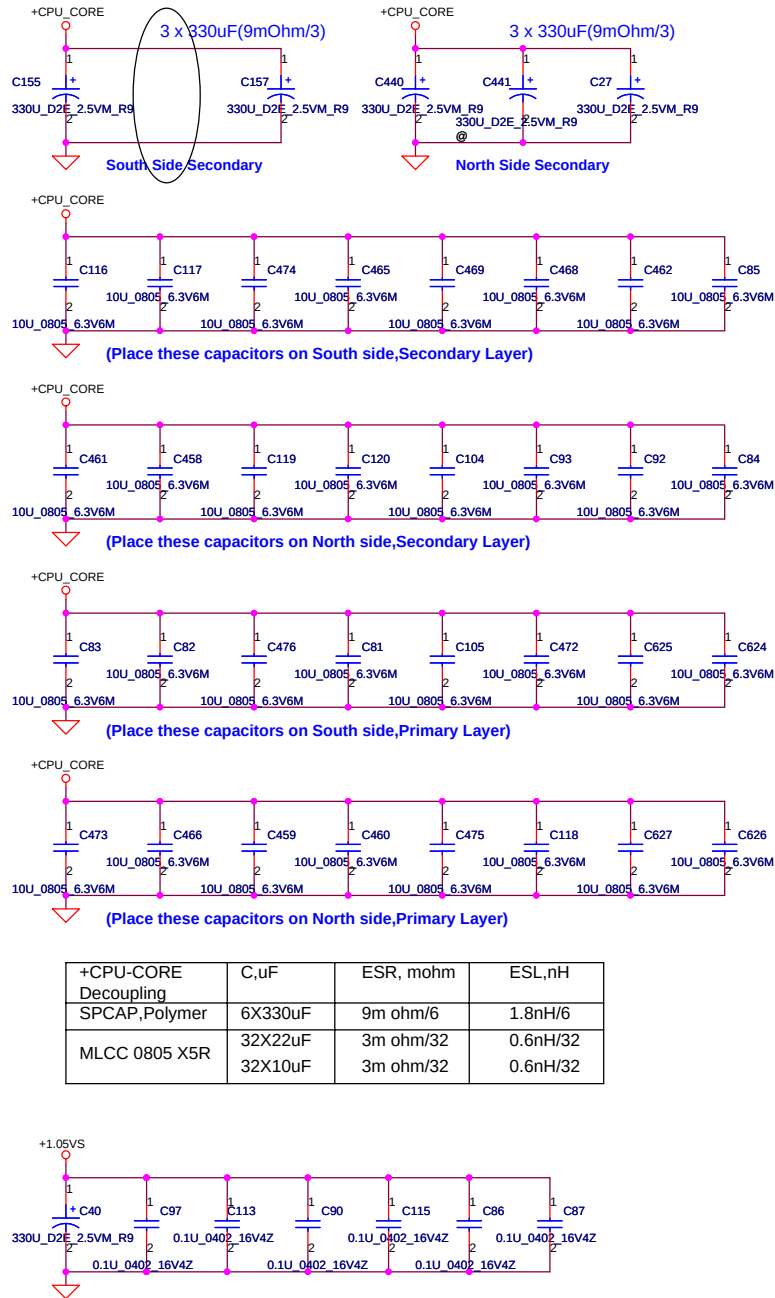
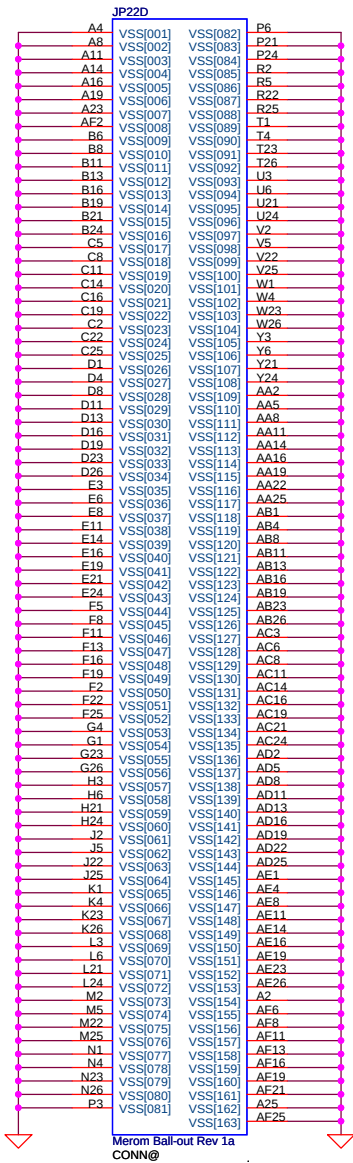
BTO Option Table

BTO Item	BOM Structure
Discrete	PM@
UMA	GM@

EC SM Bus2 address

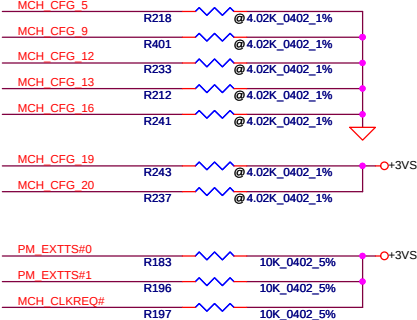


Layout Note:
THERMDA&THERMDC Trace / Space = 10 / 10 mil
THERMDA_R&THERMDC_R Trace / Space = 10 / 10 mil



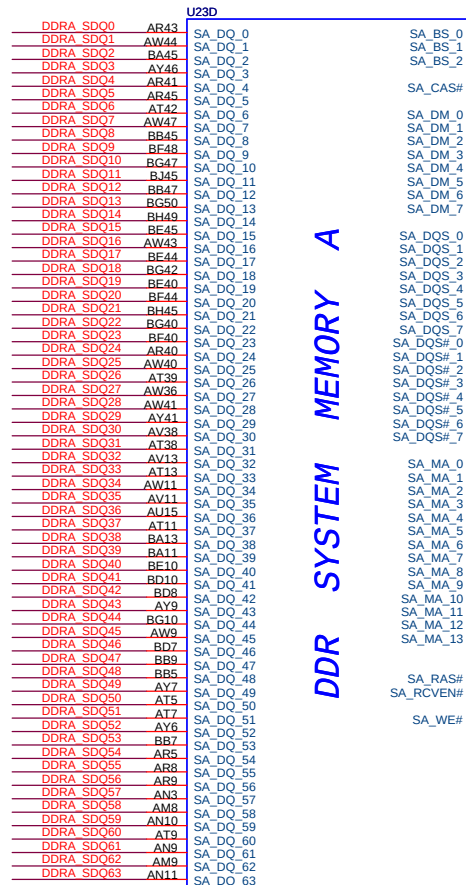


CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present

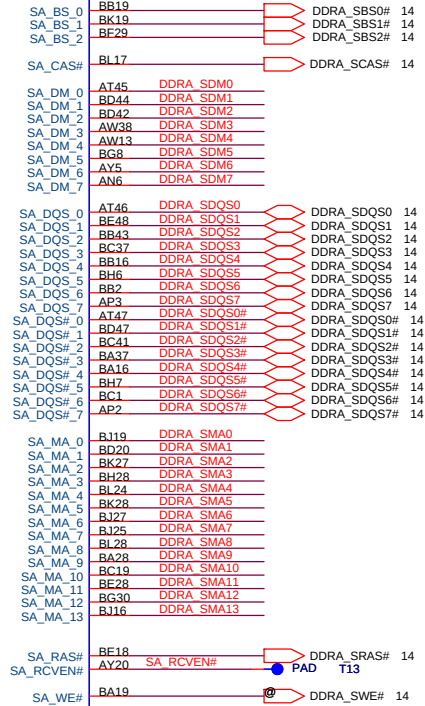


14 DDRA_SDQ[0..63] < DDRA_SDQ[0..63]
14 DDRA_SDM[0..7] < DDRA_SDM[0..7]
14 DDRA_SMA[0..13] < DDRA_SMA[0..13]

15 DDRB_SDQ[0..63] < DDRB_SDQ[0..63]
15 DDRB_SDM[0..7] < DDRB_SDM[0..7]
15 DDRB_SMA[0..13] < DDRB_SMA[0..13]

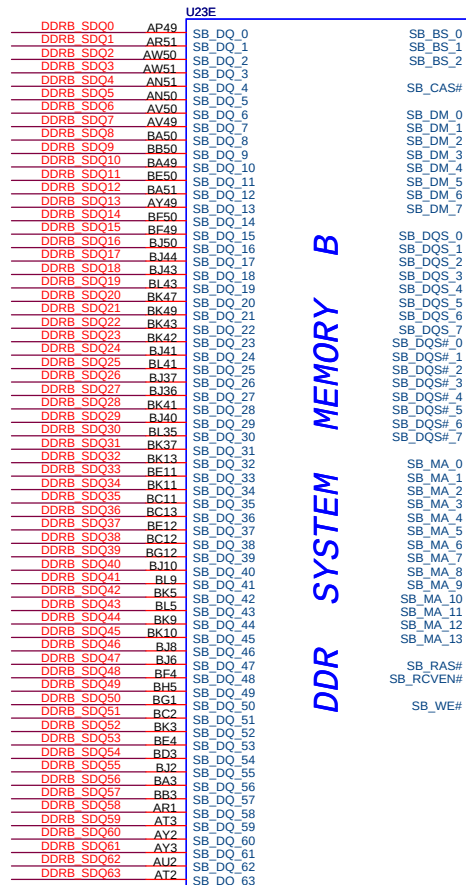


DDR SYSTEM MEMORY A



CRESTLINE_1p0

PM@

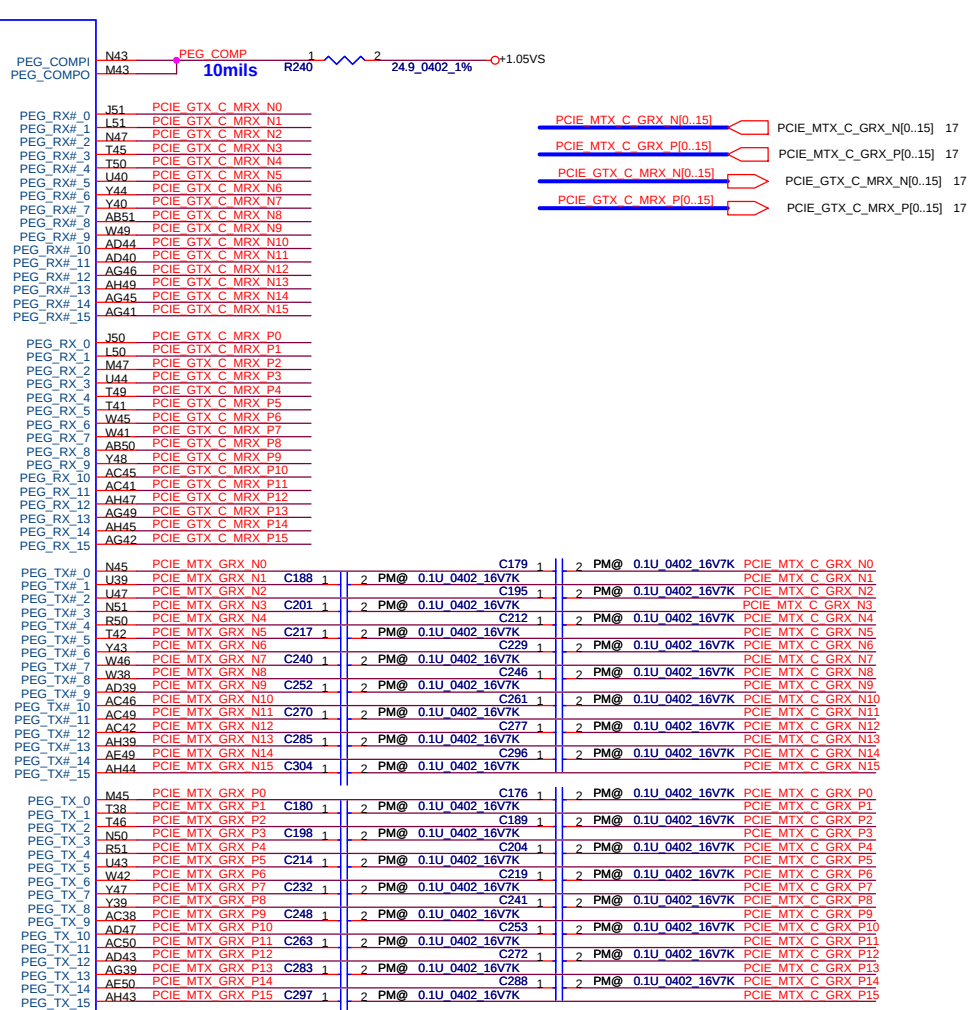
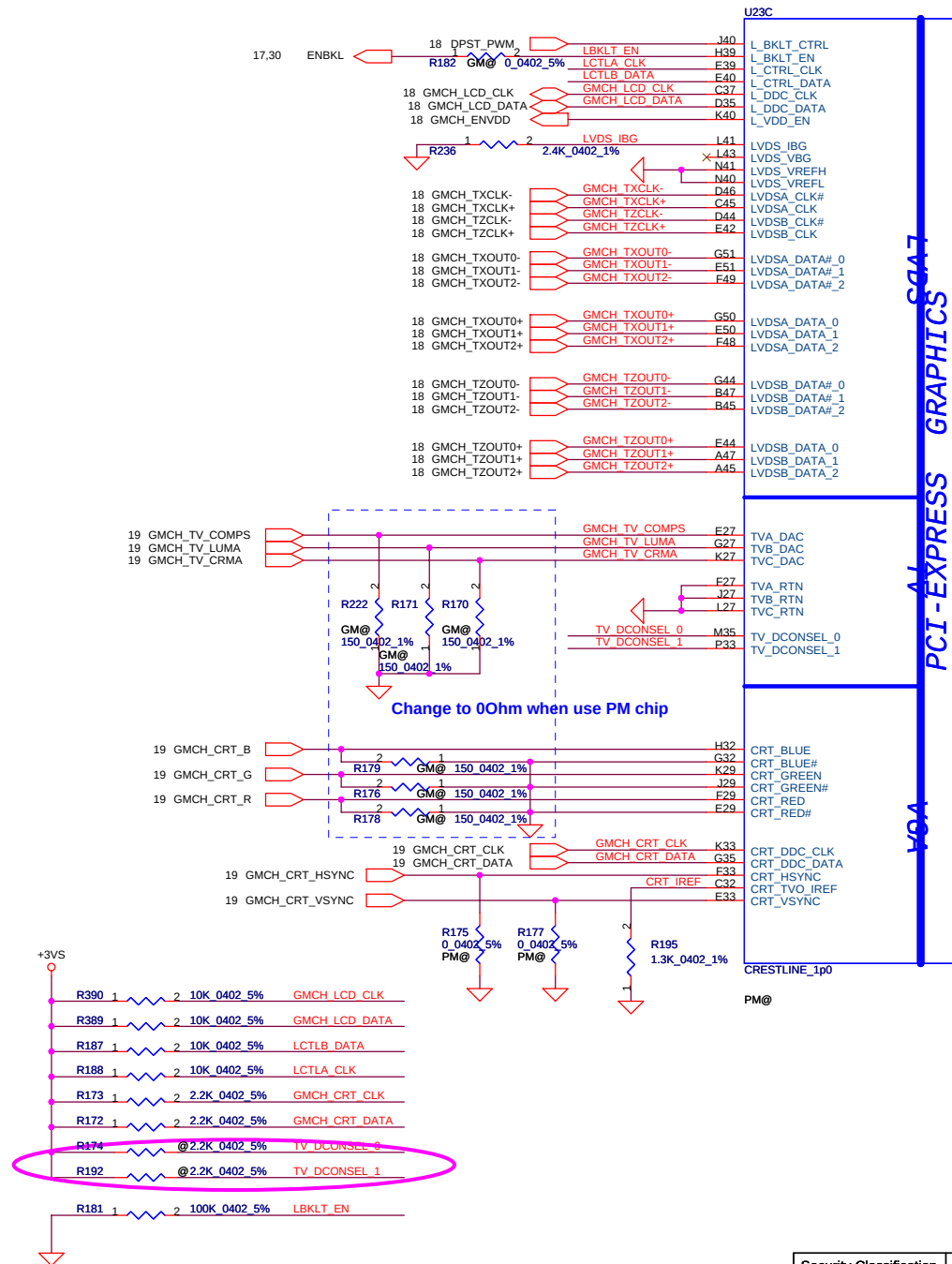


DDR SYSTEM MEMORY B

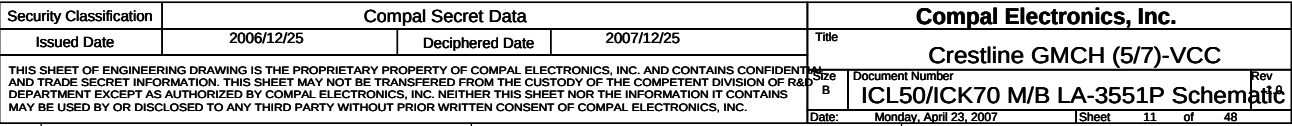
CRESTLINE_1p0

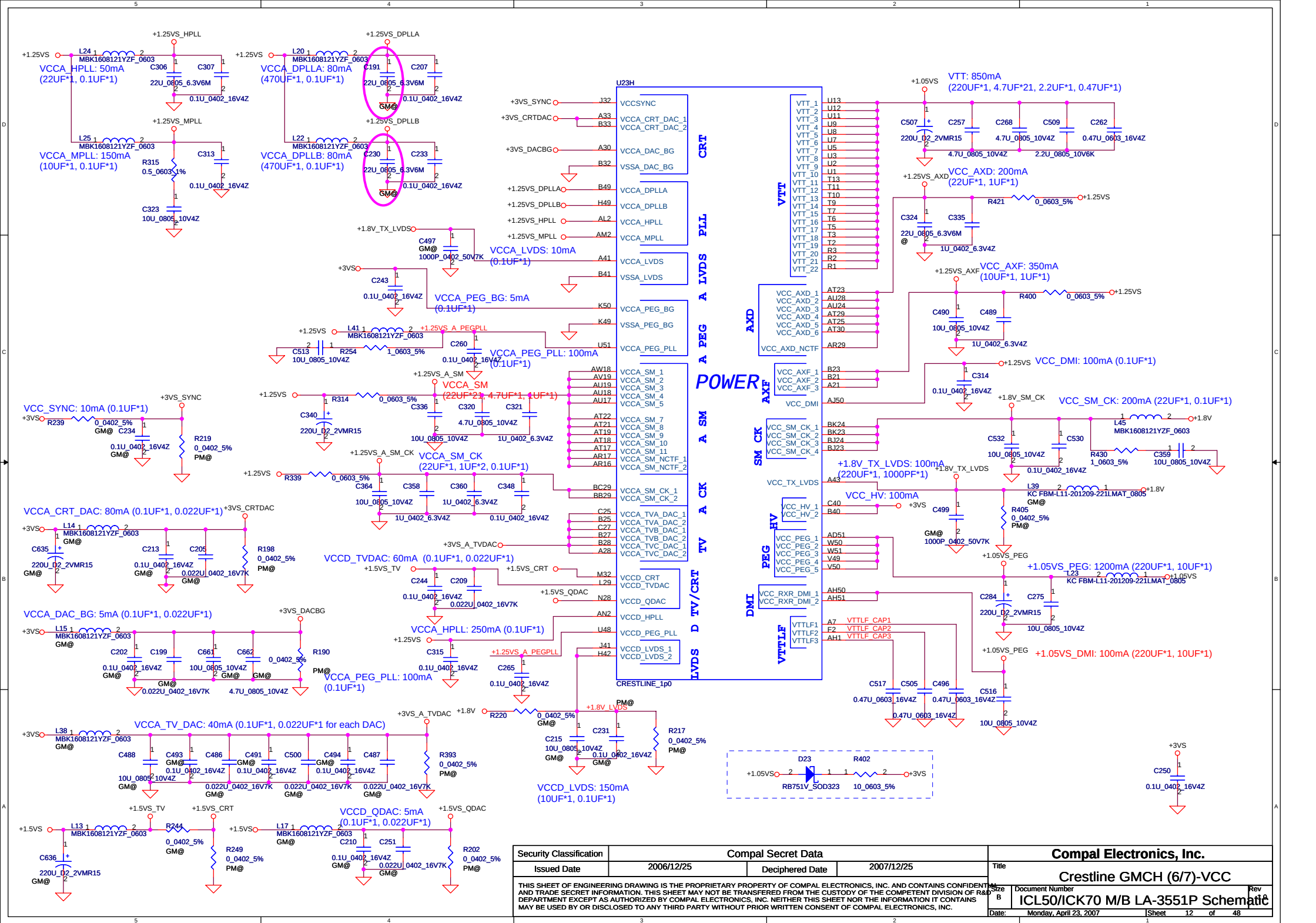
PM@

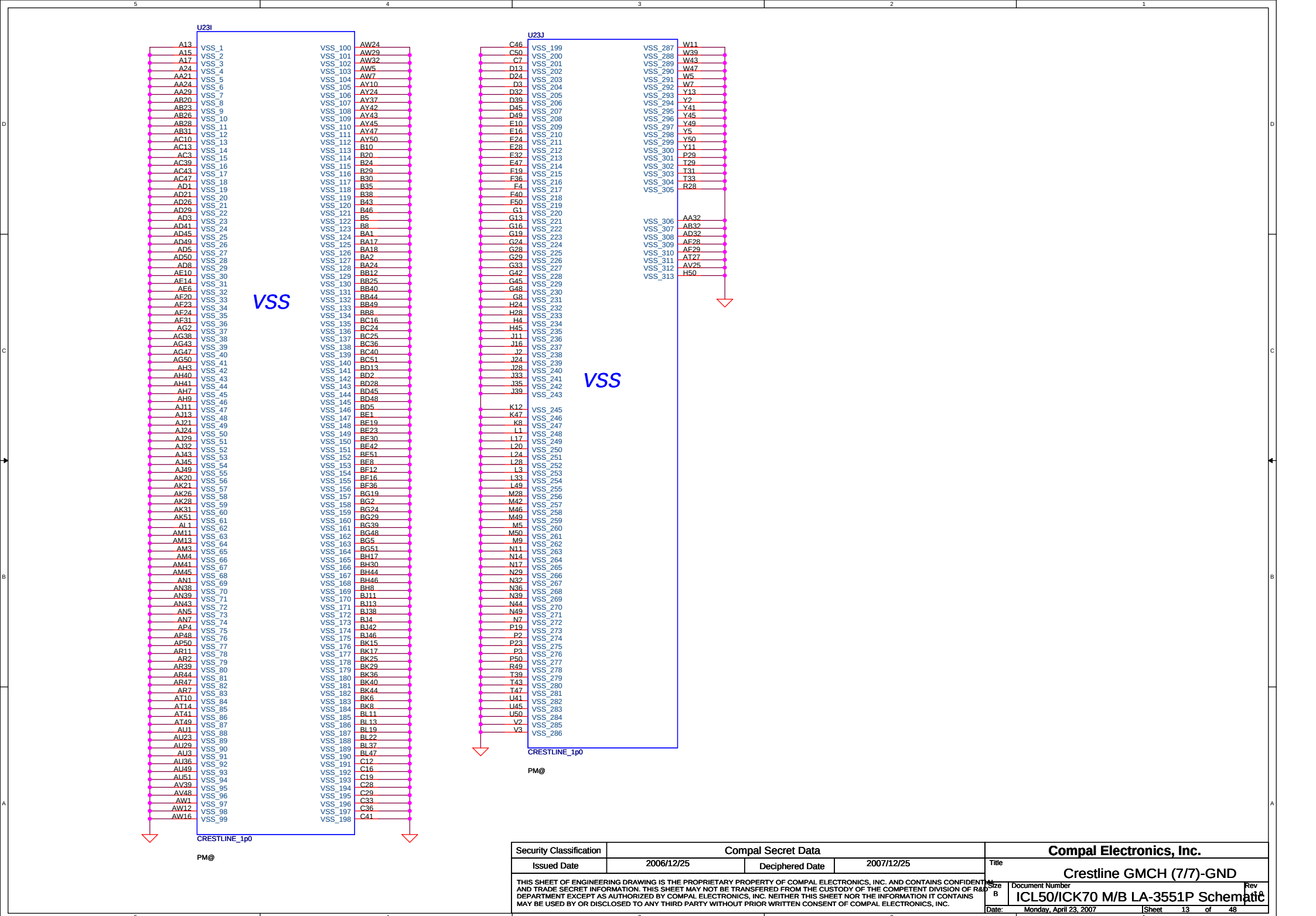
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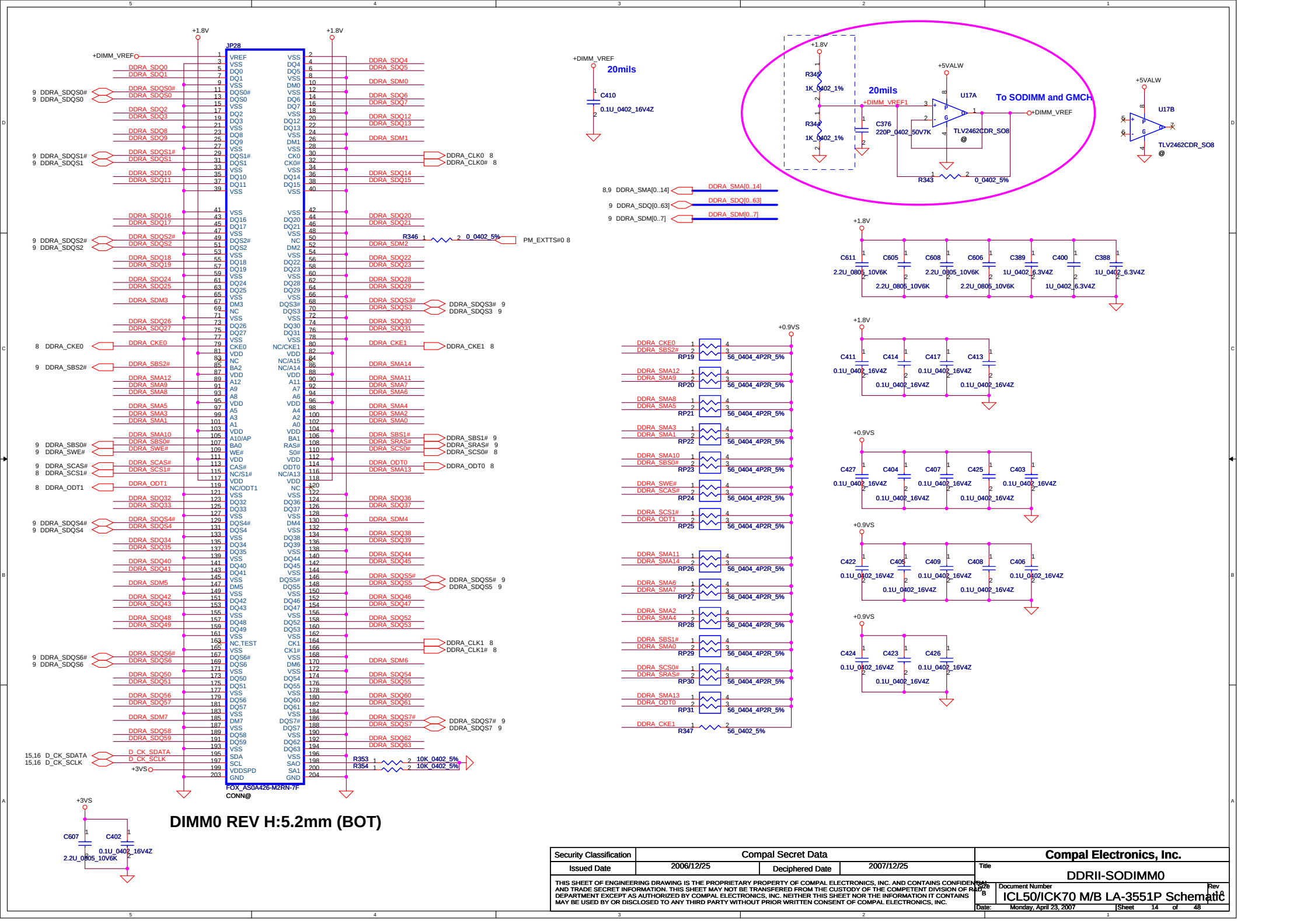
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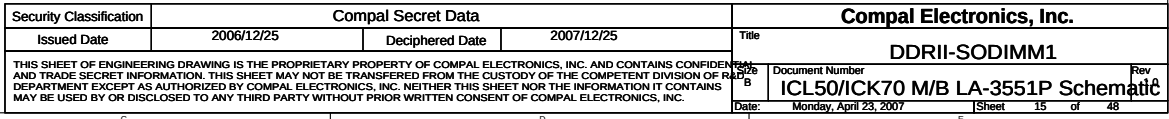






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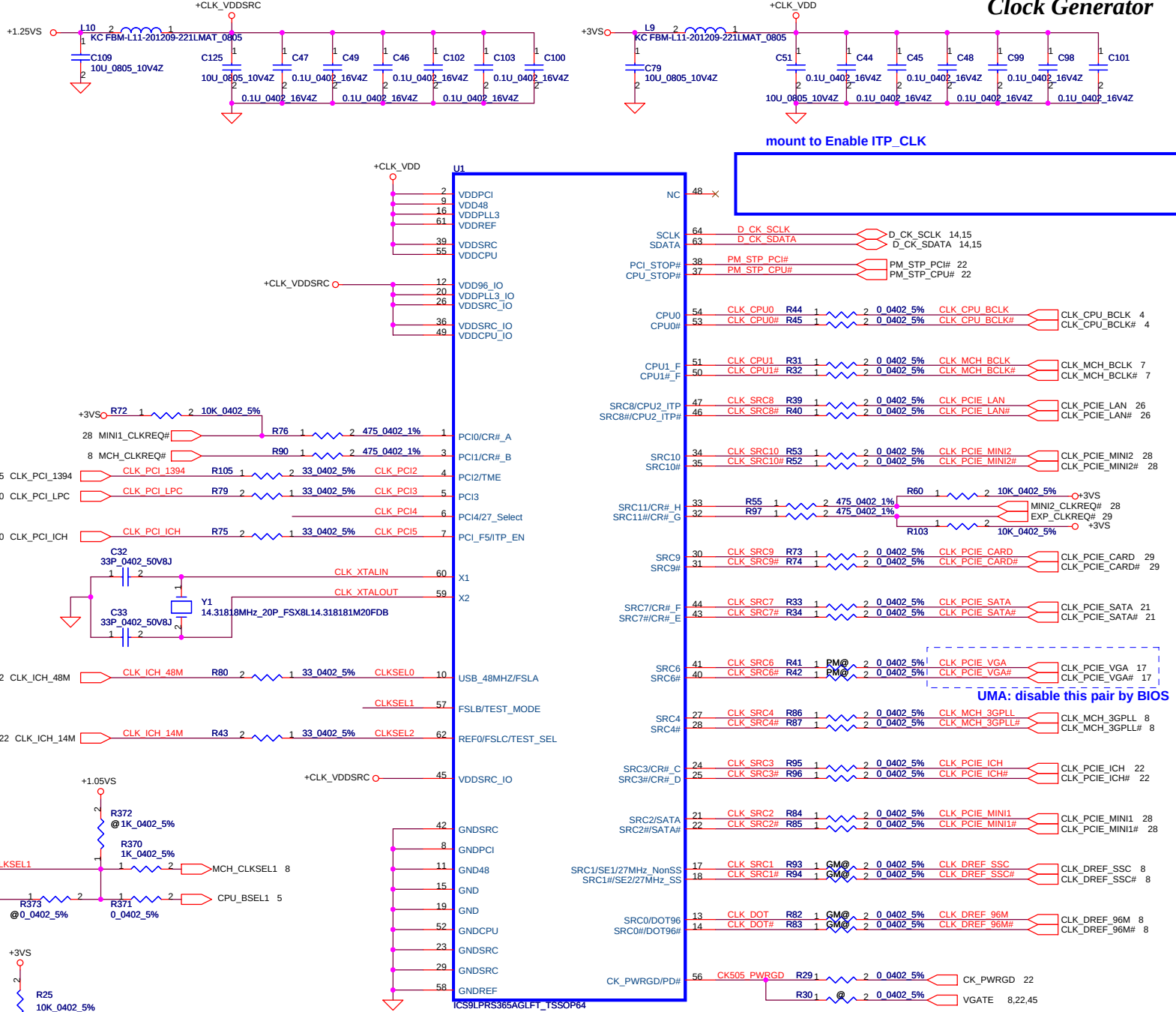
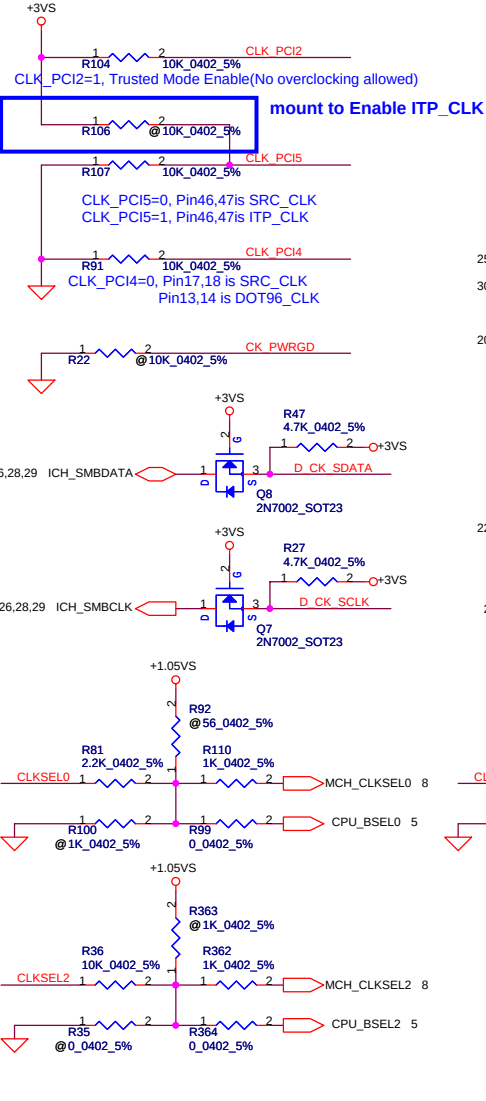


FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR365

CLK_REQ#	Control	Free-Run
CR#_A(WLAN)	PCIEX2	PCIEX0
CR#_B(MCH)	PCIEX4	PCIEX1
CR#_G(NEW CARD)	PCIEX9	
CR#_H(MINI CARDII)	PCIEX10	

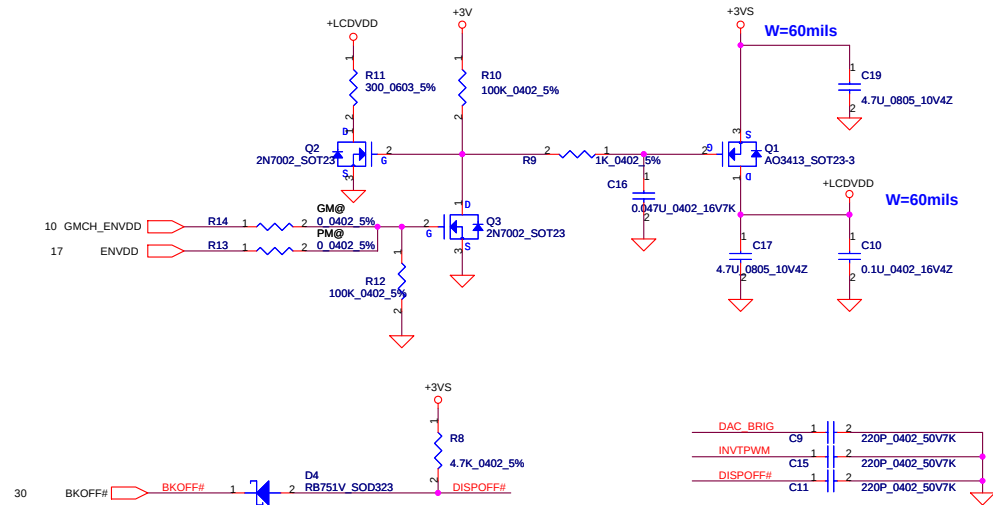
SRC6(VGA_CLK): Discrete VGA[Enable] UMA[Disable]



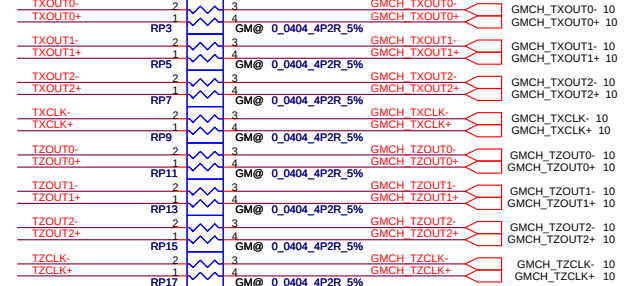
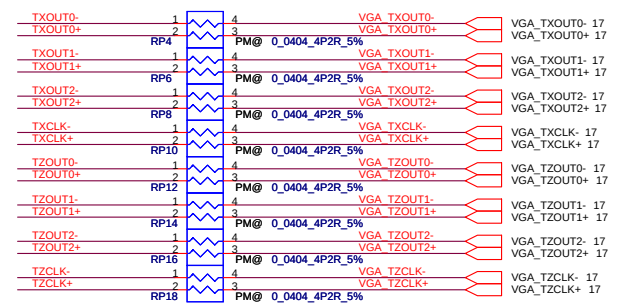
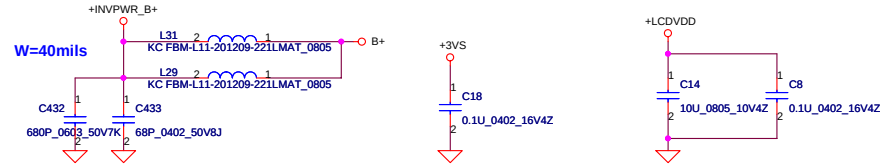
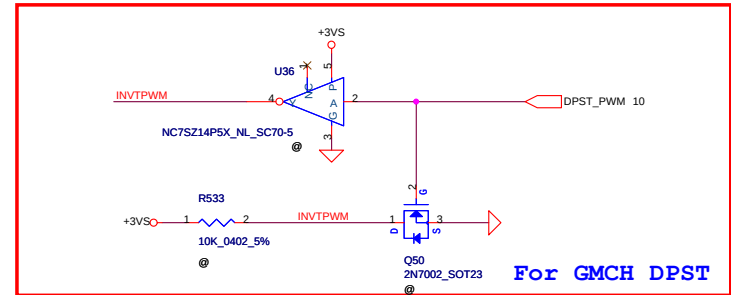
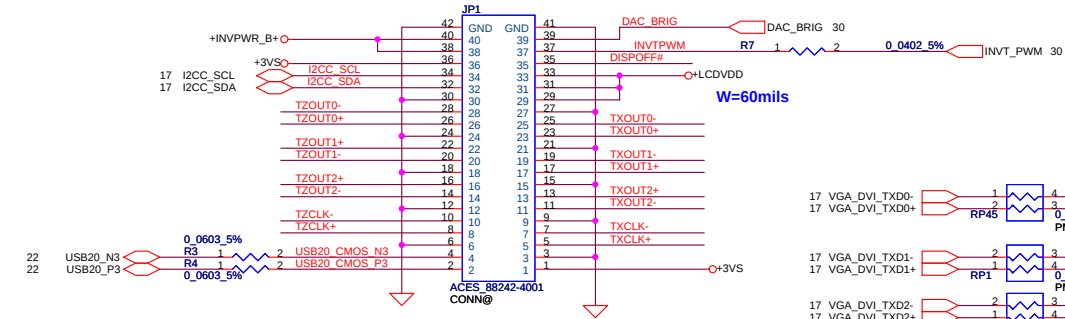
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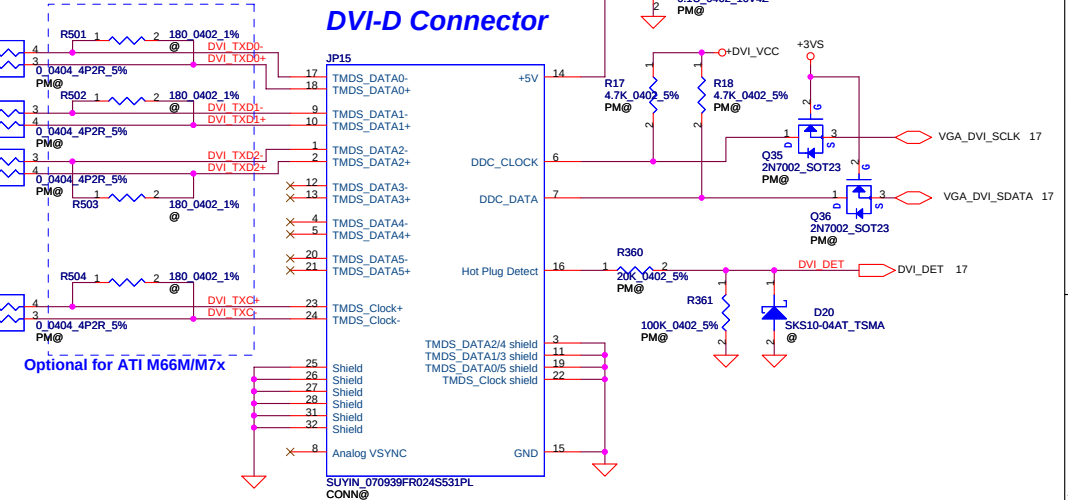
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

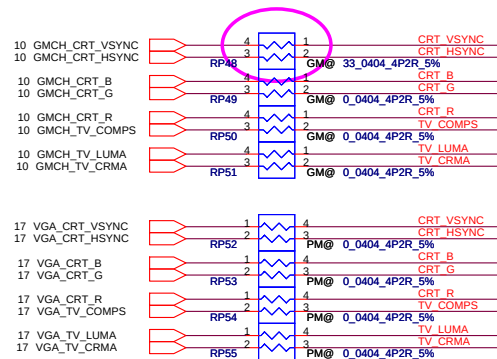


DVI-D Connector



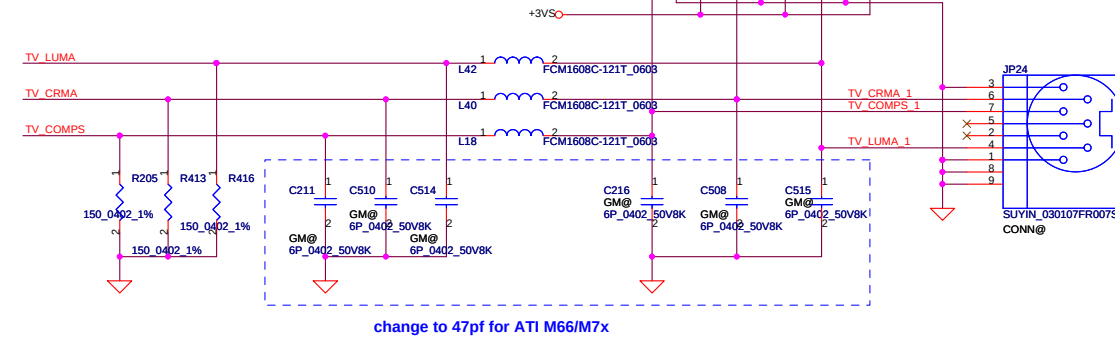
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Deciphered Date				2007/12/25				LVDS & DVI Connector			
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CRT Connector

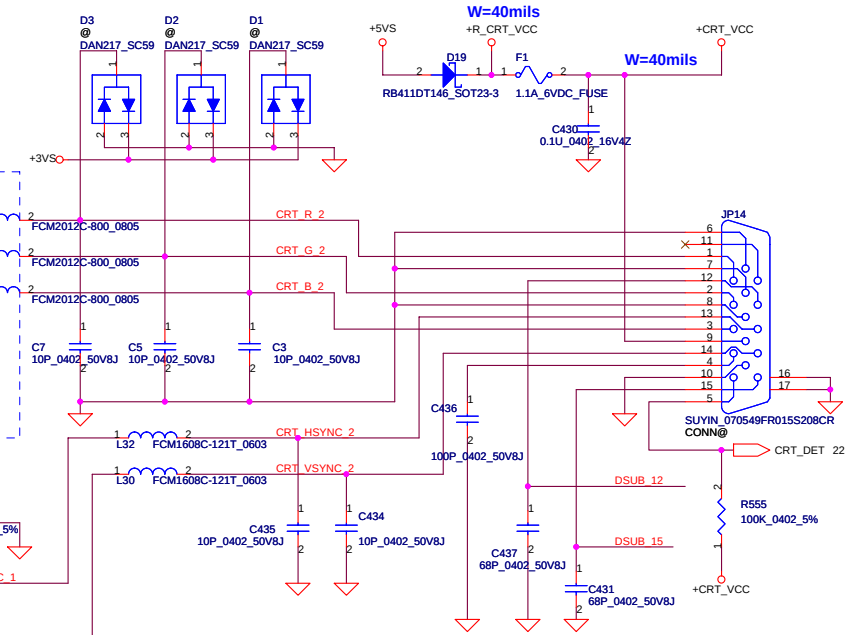
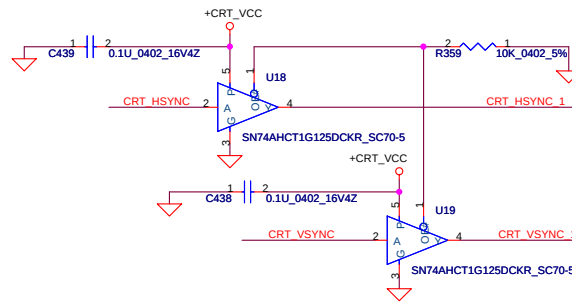


Place closed to chipset

TV-OUT Conn.

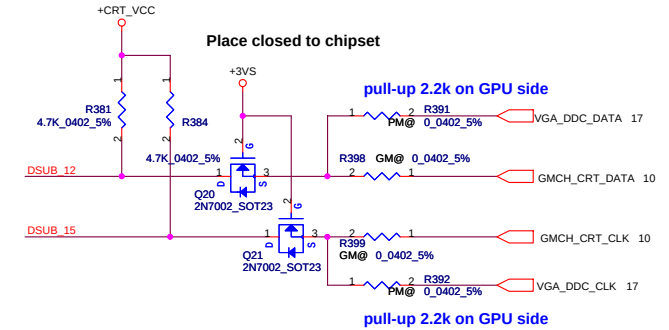


change to 47pf for ATI M66/M7x



change to 47pf for ATI M66/M7x

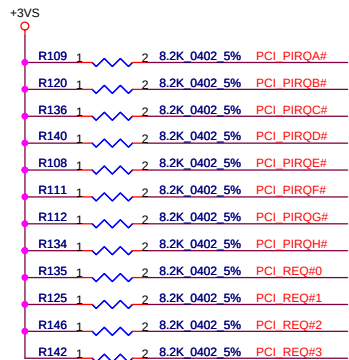
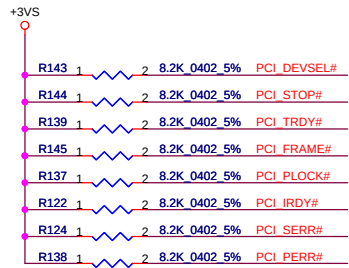
Place closed to chipset



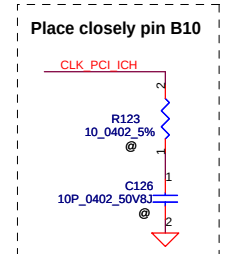
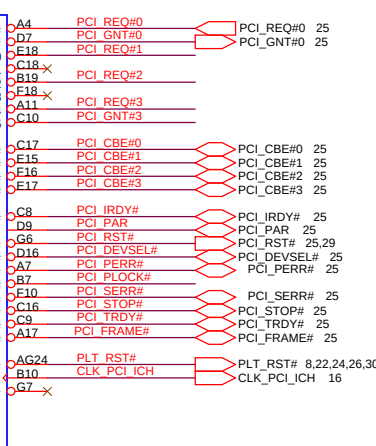
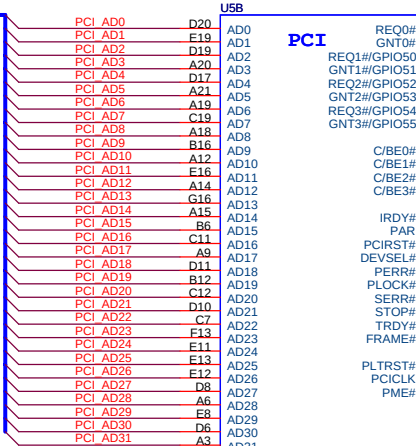
pull-up 2.2k on GPU side

pull-up 2.2k on GPU side

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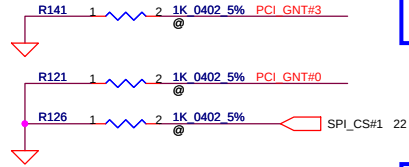
25 PCI_AD[0..31]



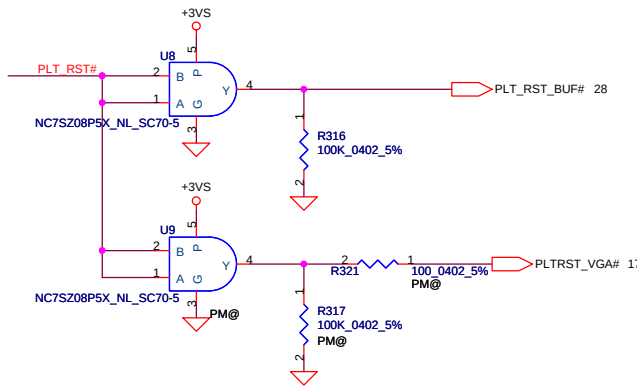
Interrupt I/F

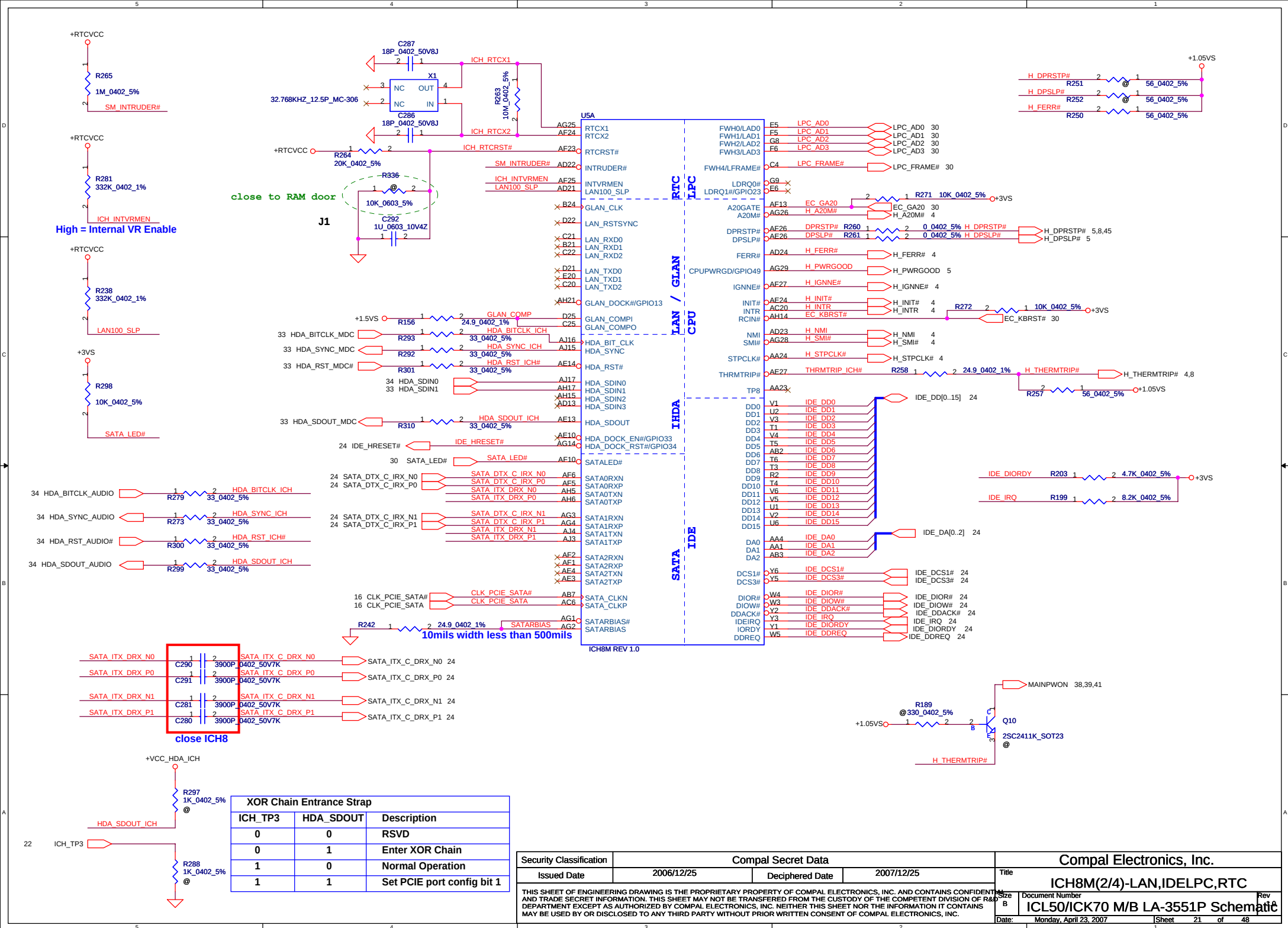


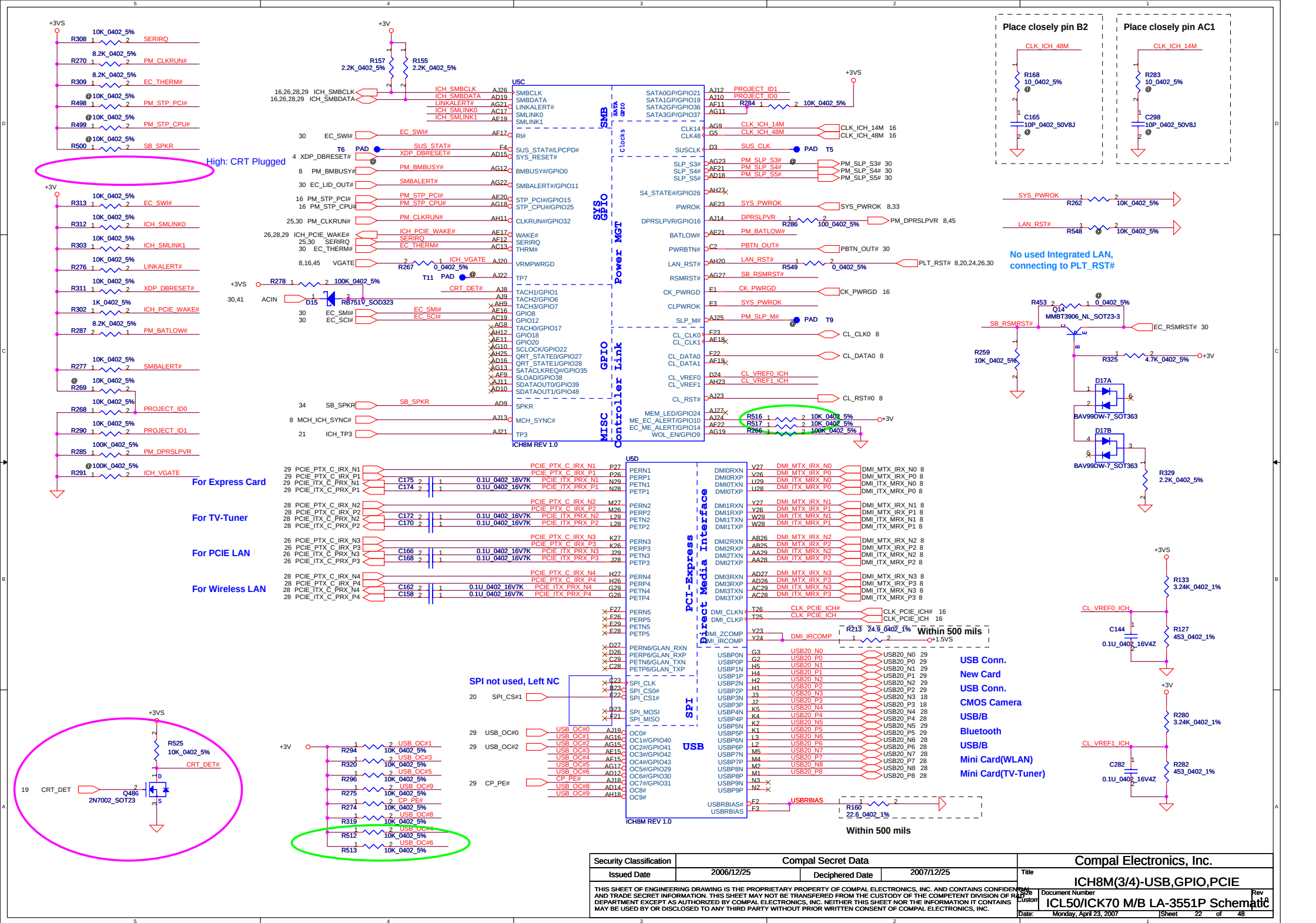
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

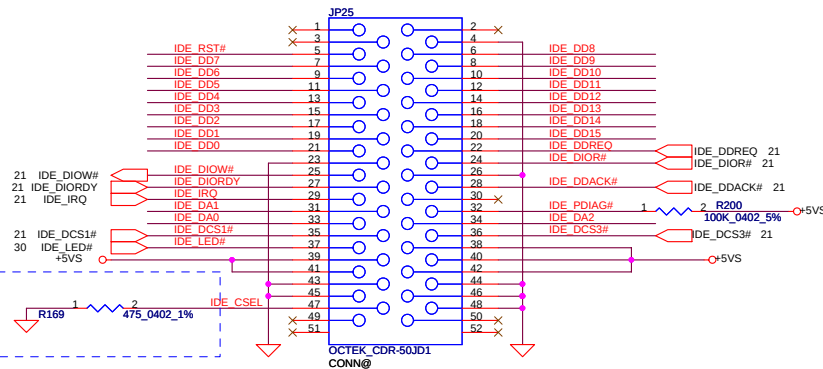


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

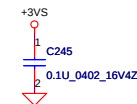
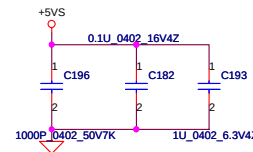








+5VS  IDE_LED#



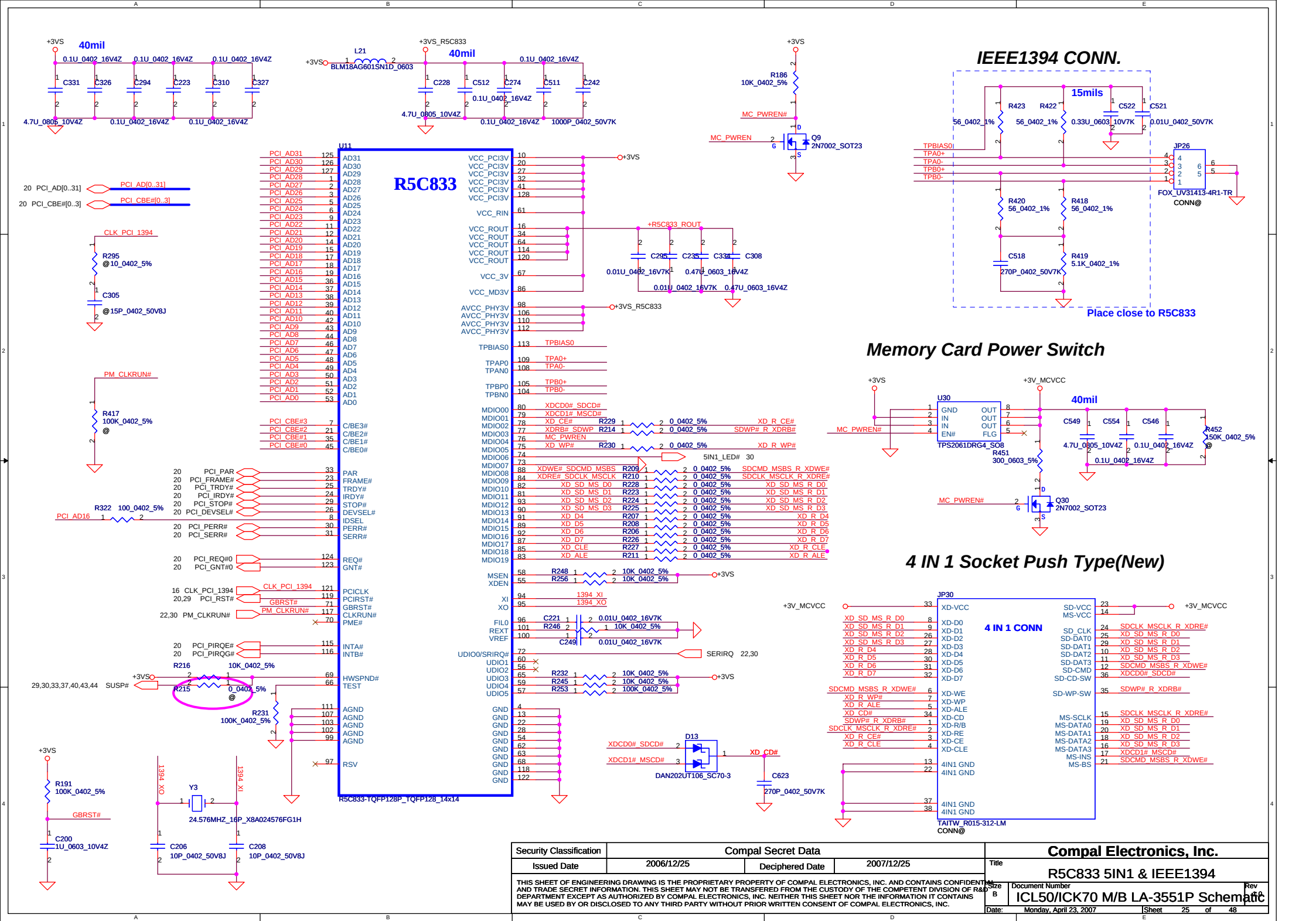
JP27

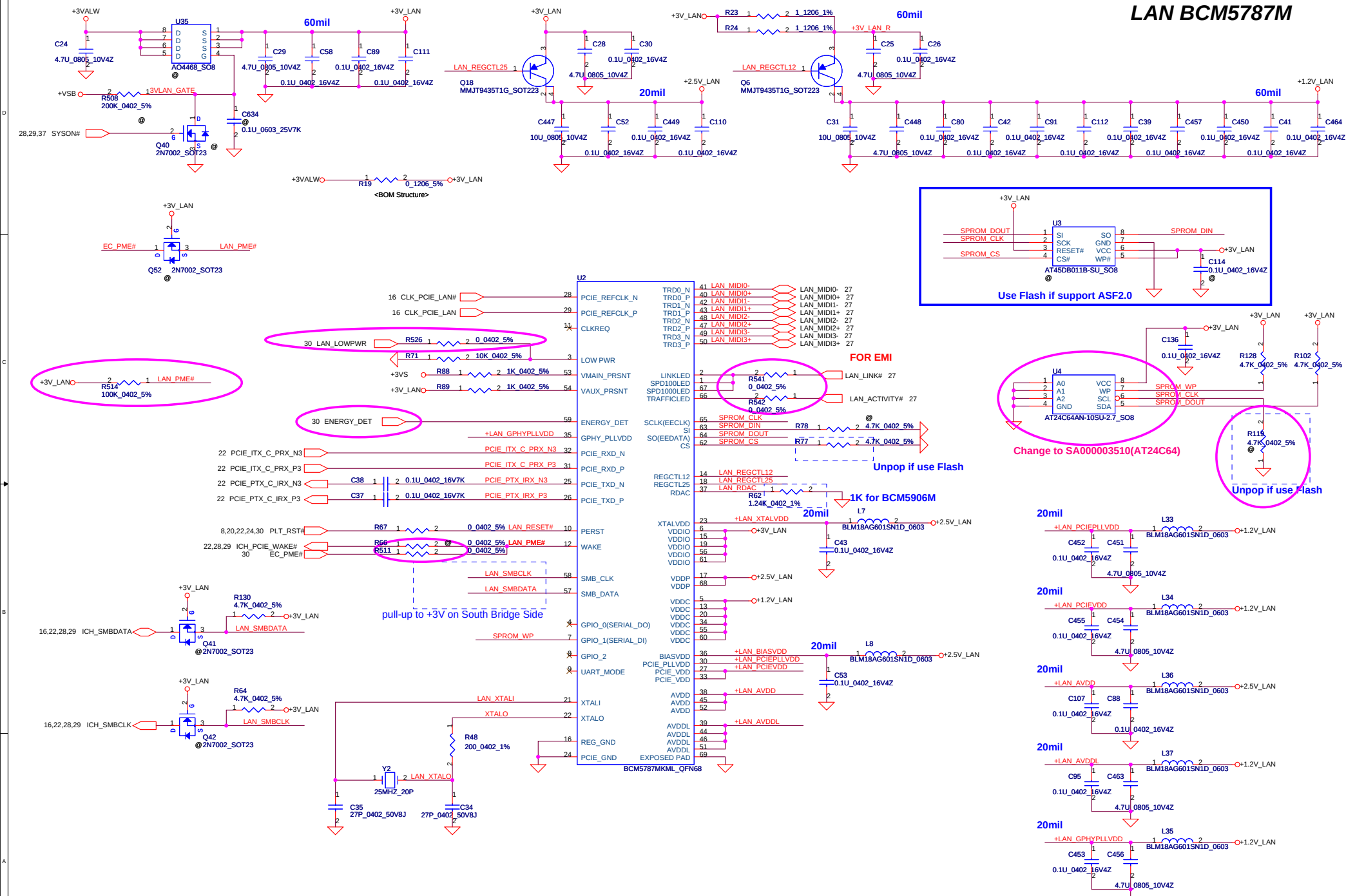
Pin	Signal
1	GND
2	HTX1+
3	HTX1+
4	GND
5	HRX1+
6	HRX1+
7	GND
8	VCC3.3
9	VCC3.3
10	VCC3.3
11	GND
12	GND
13	GND
14	VCC5
15	VCC5
16	VCC5
17	GND
18	RESERVED
19	GND
20	VCC12
21	VCC12
22	VCC12
23	GND
24	HTX1+
25	GND
26	HRX1+
27	HRX1+
28	GND
29	GND
30	GND1
31	GND2

OTESK SAS-22CA1
CONN@

2nd HDD for 17"

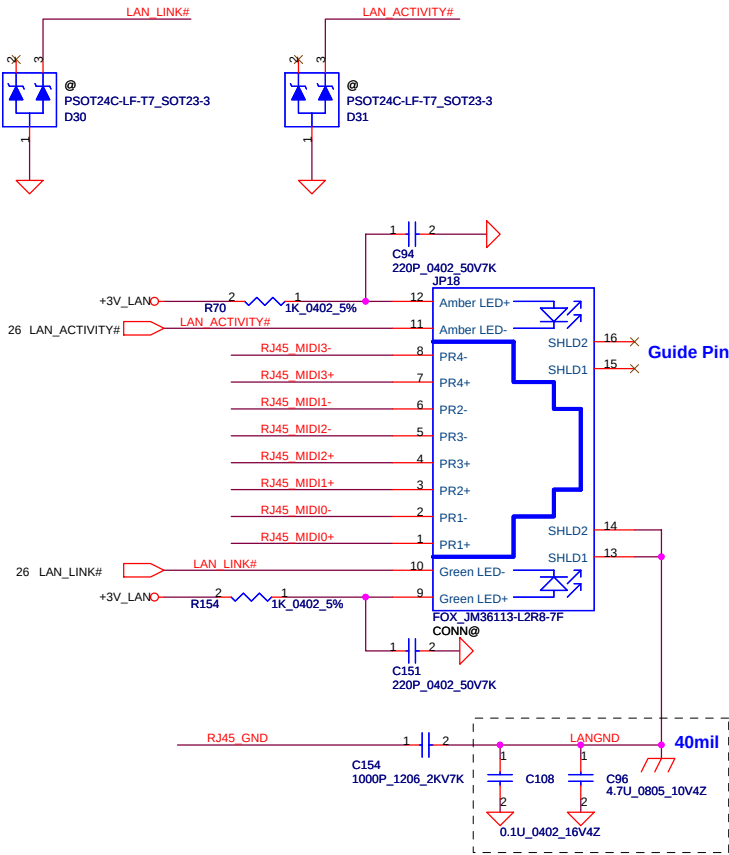
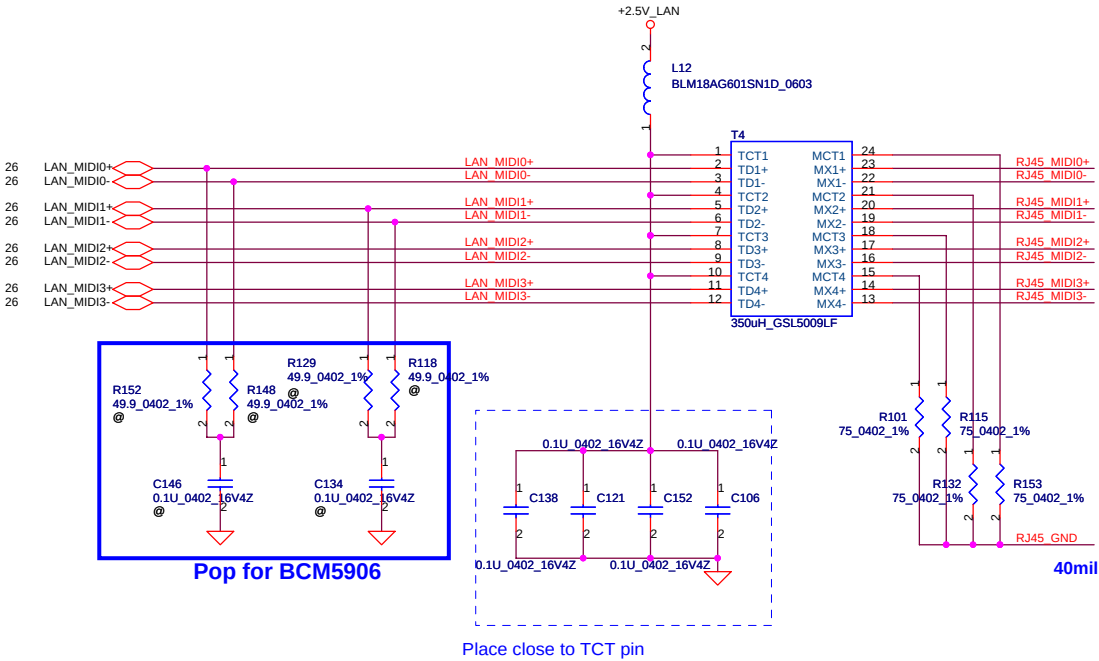
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				ICL50/ICK70 M/B LA-3551P Schematic	1
Date	Monday, April 23, 2007		Sheet	24 of 48	



LAN BCM5787M

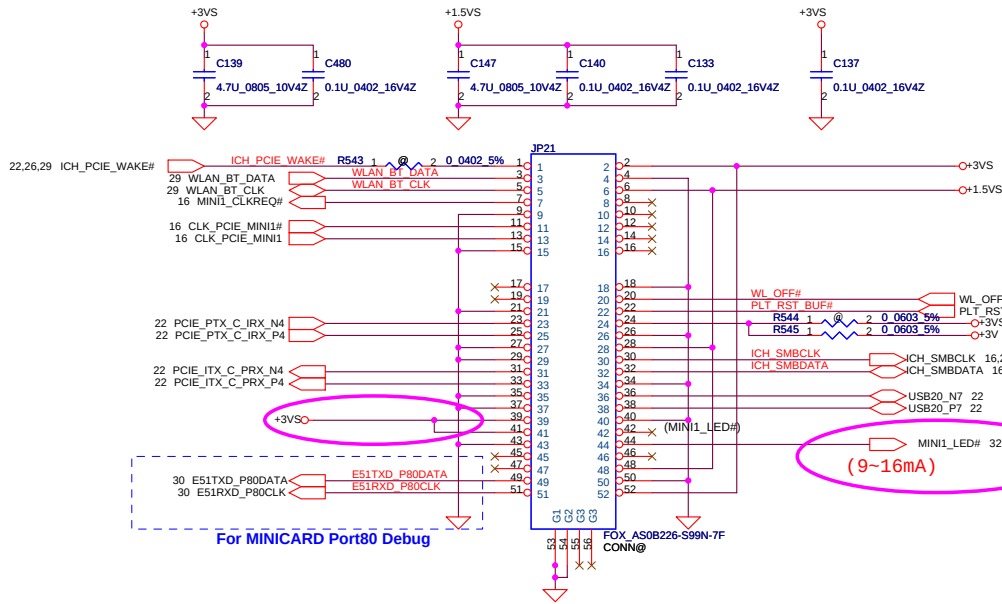
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/12/25	Deciphered Date	2007/12/25	Title	LAN BCM5787M
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				ICL50/ICK70 M/B LA-3551P Schematics	
Date:		Monday, April 23, 2007		ISheet	26 of 48

LAN BCM5787M



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2007/12/25		2007/12/25		Title	
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Date		Monday, April 23, 2007		Sheet 27 of 48	

For Wireless LAN

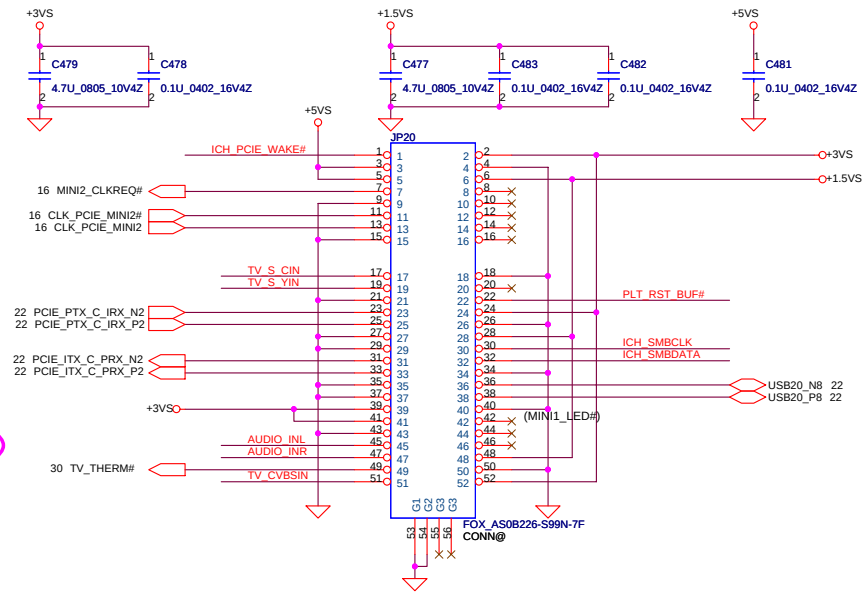


For MINICARD Port80 Debug

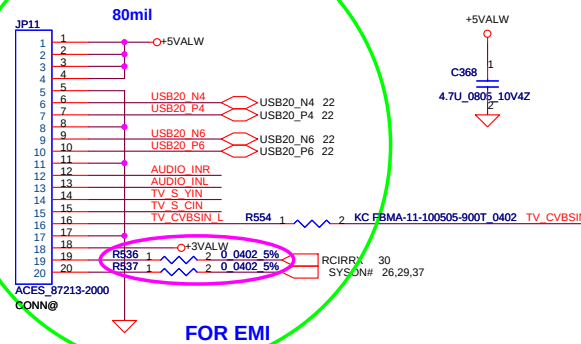
Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

For TV-Tuner/HW MPEG



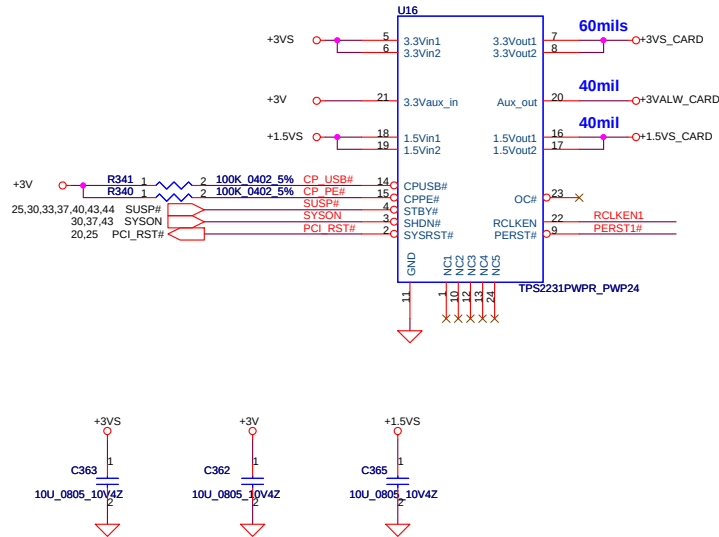
To USB/B Connector



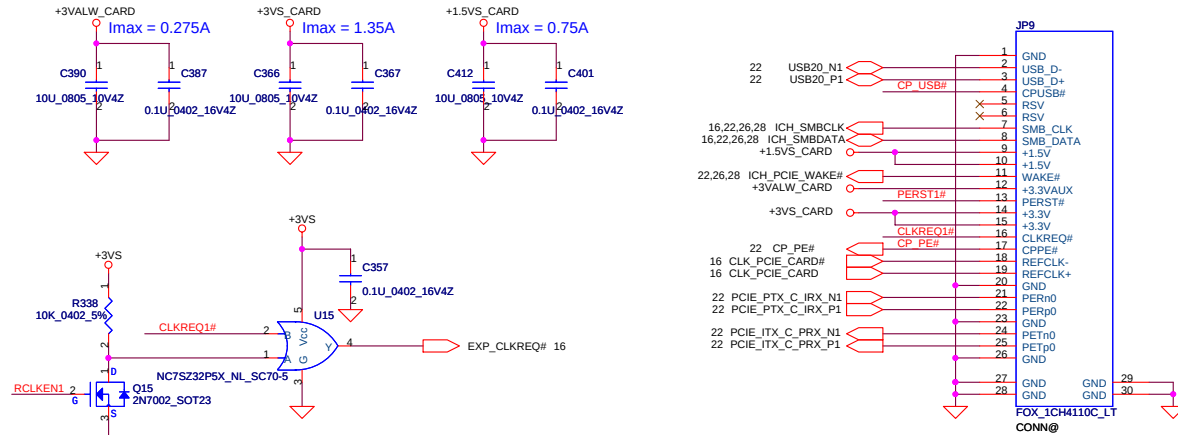
AV-IN Connector
CIR

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				Date	Monday, April 23, 2007
				Sheet	28 of 48

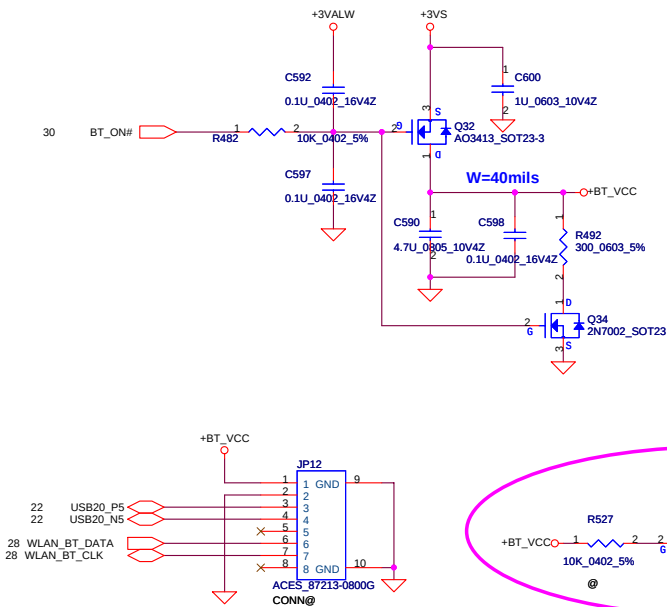
New Card Power Switch



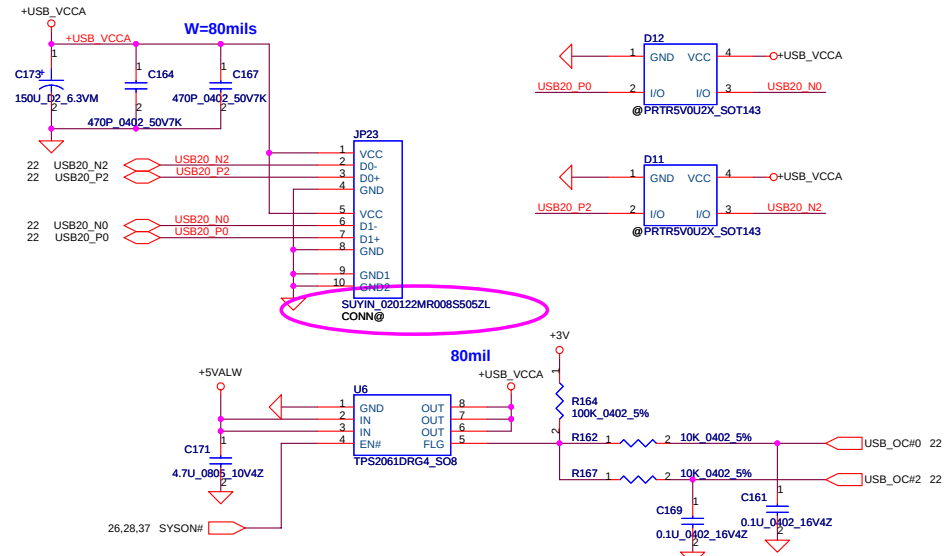
New Card Socket (Left/TOP)



Bluetooth Conn.



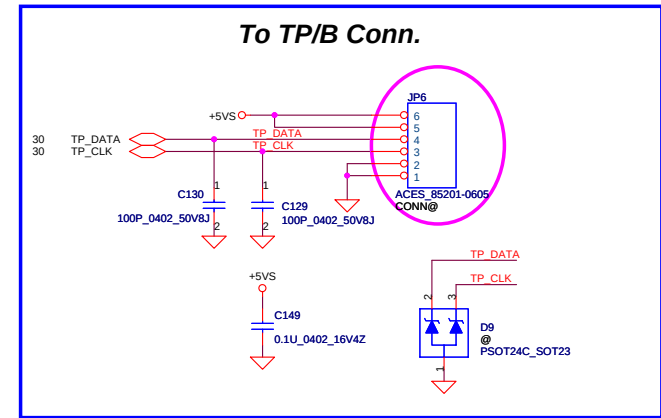
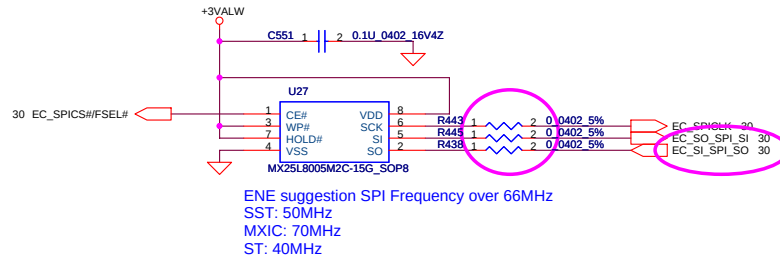
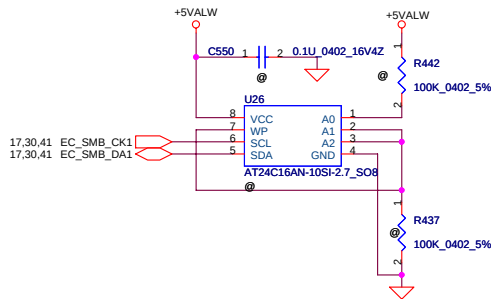
USB CONN. (Stack-up Type)



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				Rev 1.8	Document Number
				ICL50/ICK70 M/B LA-3551P Schematic	
				Date: Monday, April 23, 2007	Rev
				Sheet 29 of 48	

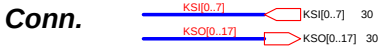


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Issued Date	2006/12/25	Deciphered Date	2007/12/25	Title	EC ENE KB925(Reserved)
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				B	ICL50/ICK70 M/B LA-3551P Schematic
				Date	Thursday, April 19, 2007
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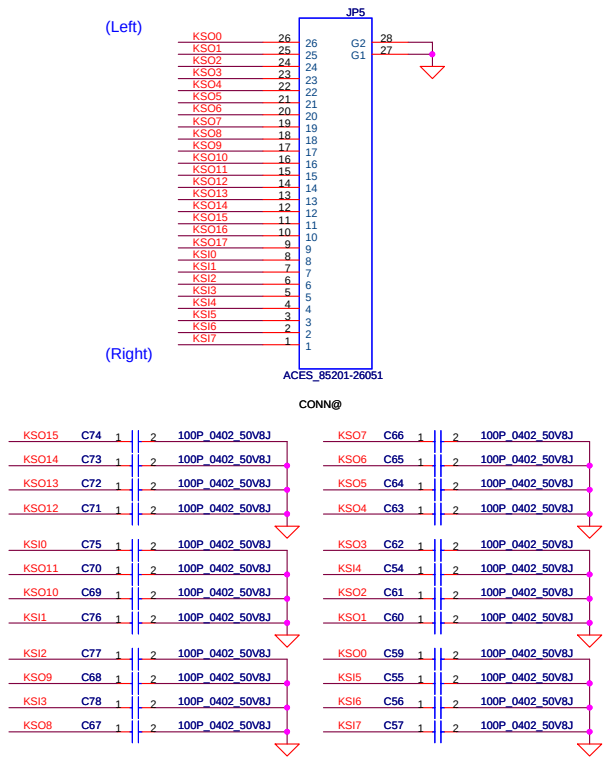


INT_KBD Conn.

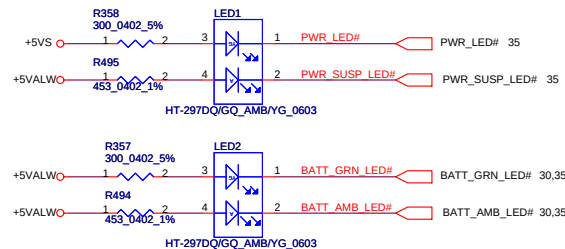
(Left)



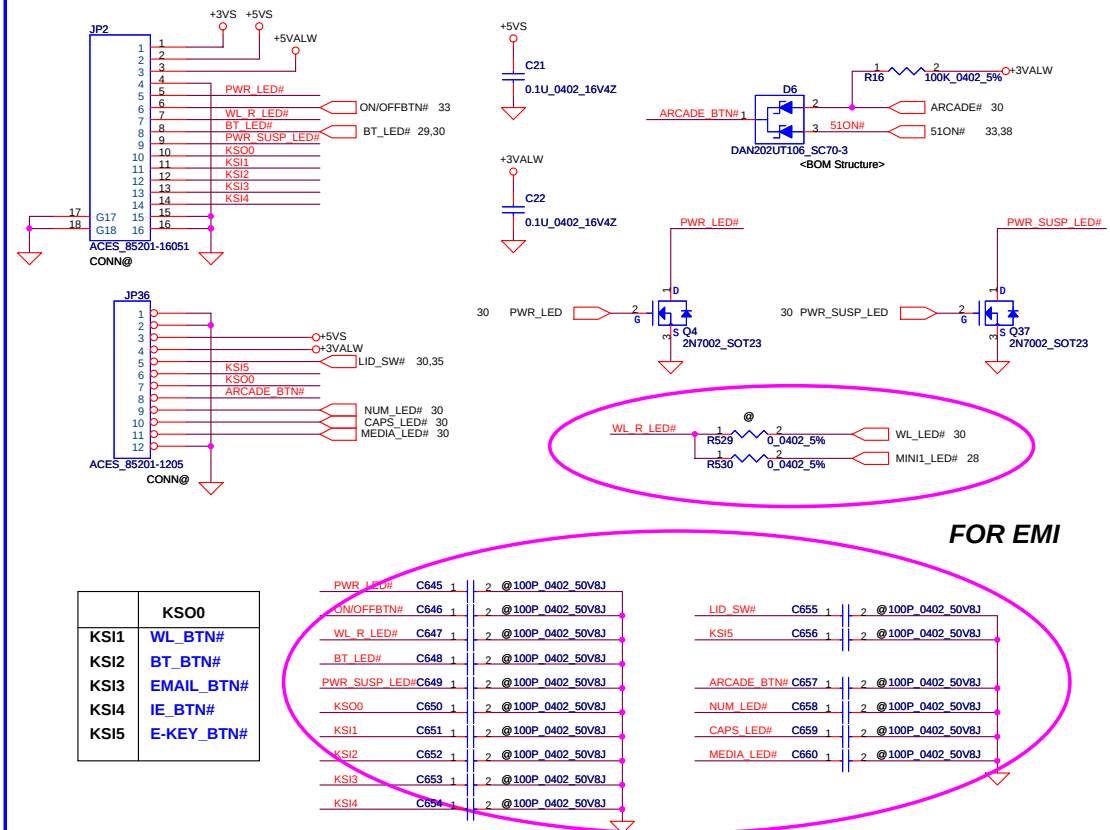
(Right)



Compal Footprint



To BTN/B Conn.



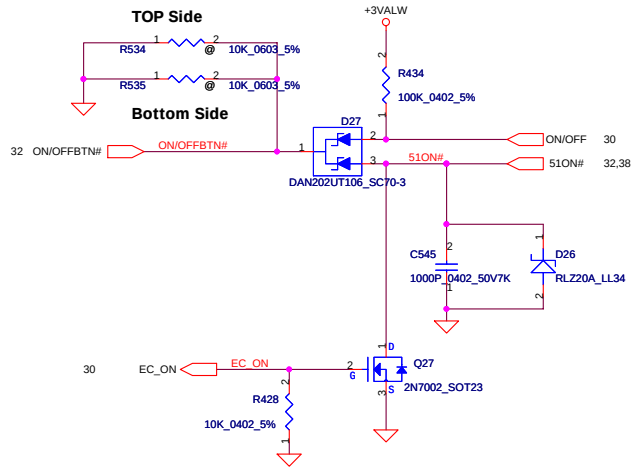
FOR EMI

KSO0		KSI5	
PWR_LED#	C645	LID_SW#	C655
ON/OFFBTN#	C646	KSI5	C656
WL_R_BTN#	C647	ARCADE_BTN#	C657
BT_BTN#	C648	NUM_LED#	C658
PWR_SUSP_LED#	C649	CAPS_LED#	C659
KSO0	C650	MEDIA_LED#	C660
KSI1	C651		
KSI2	C652		
KSI3	C653		
KSI4	C654		

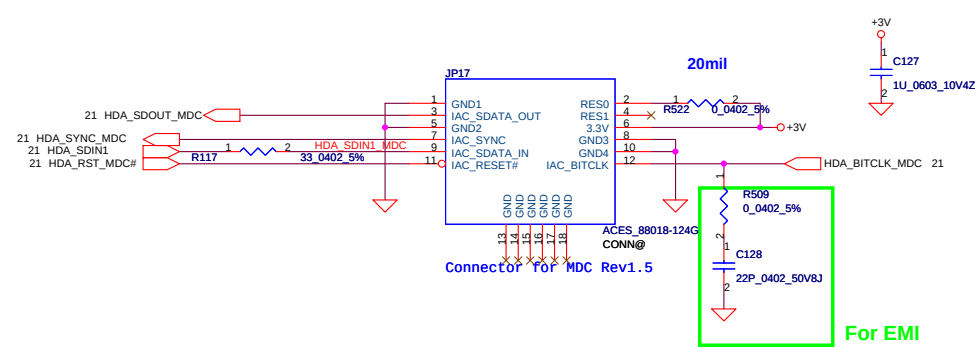
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				ICL50/ICK70 M/B LA-3551P Schematic	
				Date: Monday, April 23, 2007	Sheet 32 of 48

Power Button

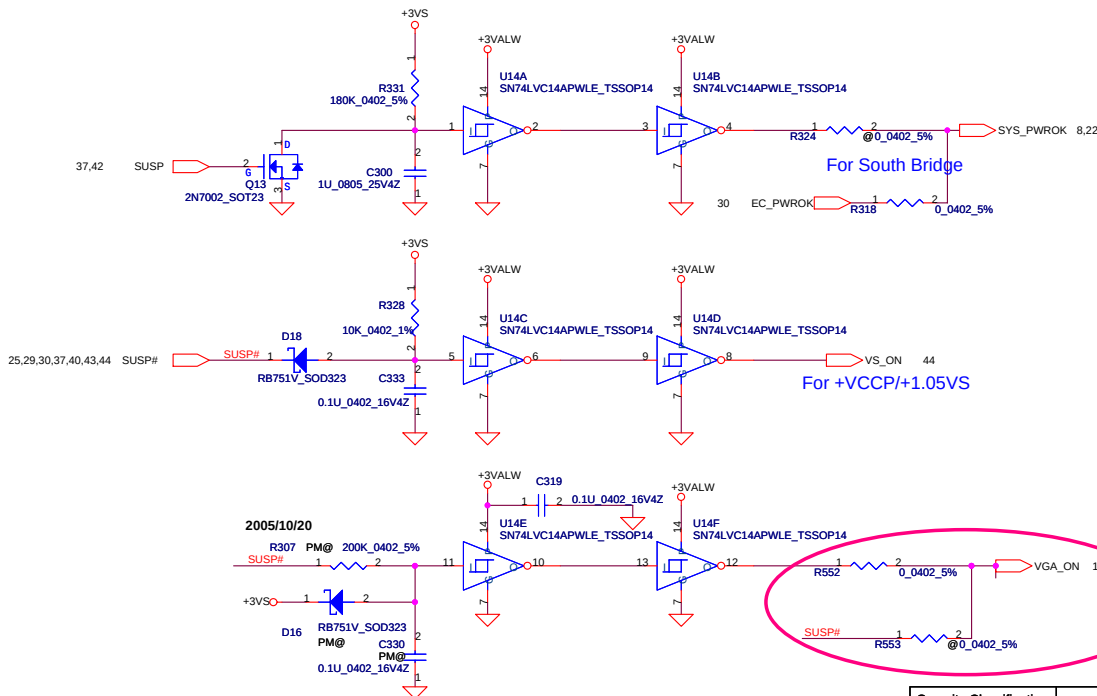
ON/OFF switch



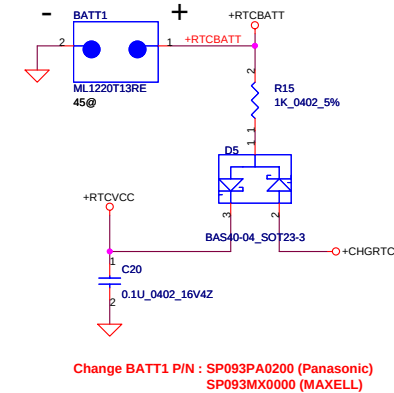
HDA MDC Conn.



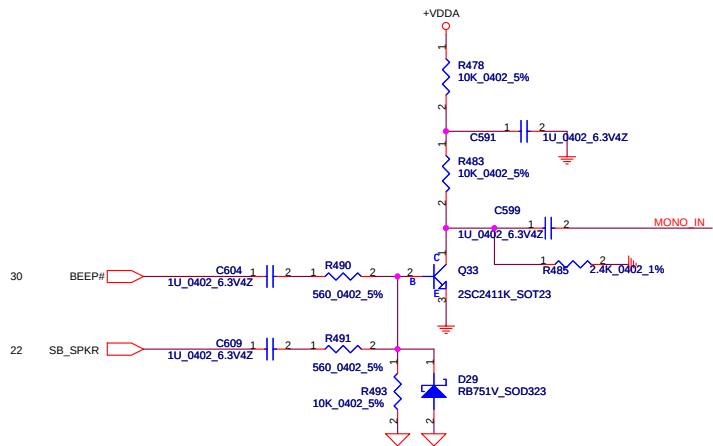
Power ON Circuit



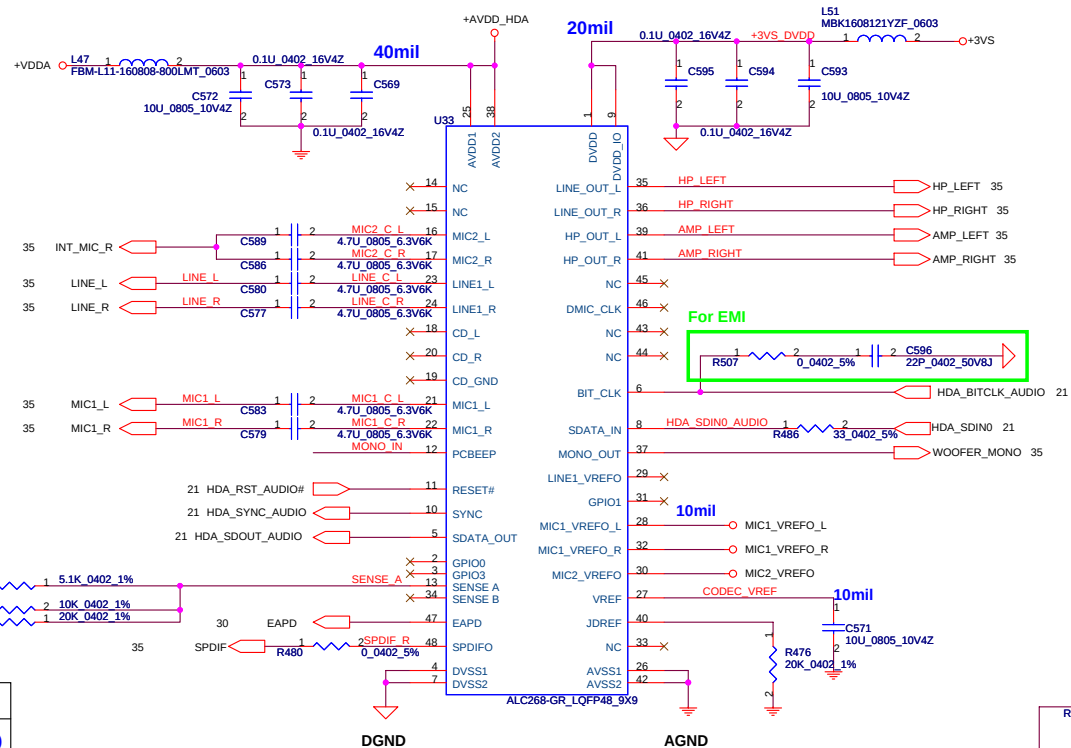
RTC Battery



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2006/12/25				2007/12/25				Title			
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								ICL50/ICK70 M/B LA-3551P Schematic			
								Date: Monday, April 23, 2007			
								Sheet 33 of 48			



HD Audio Codec

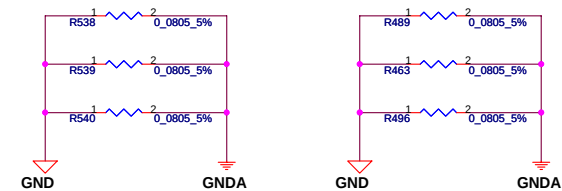


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

28.7K for Module Design (VDDA = 4.702)

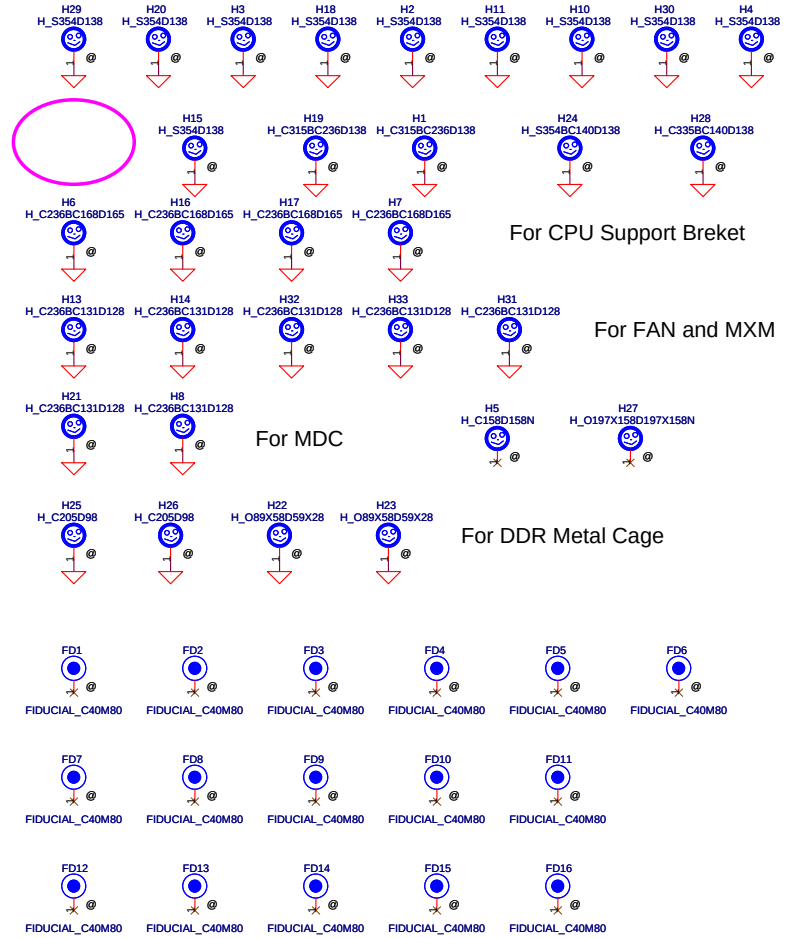
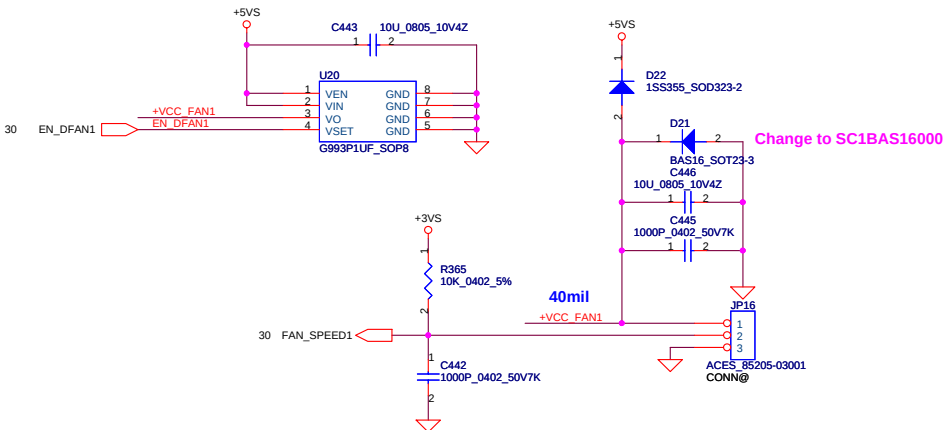
(output = 250 mA)

4.85V

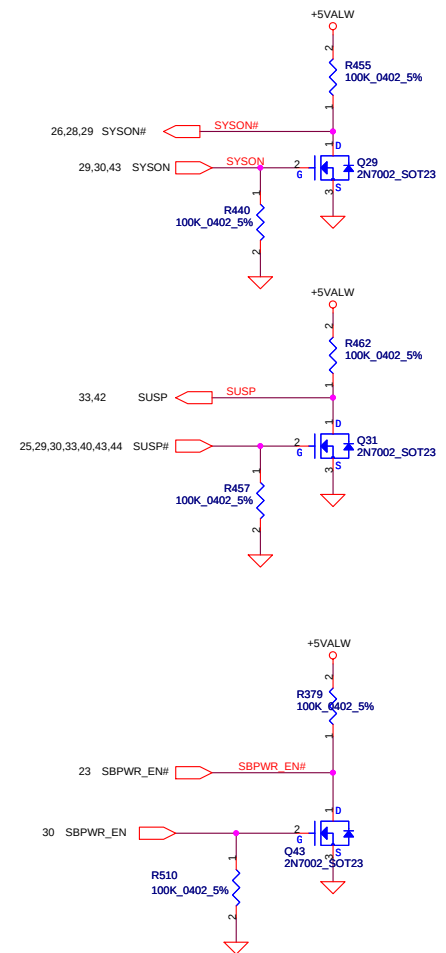
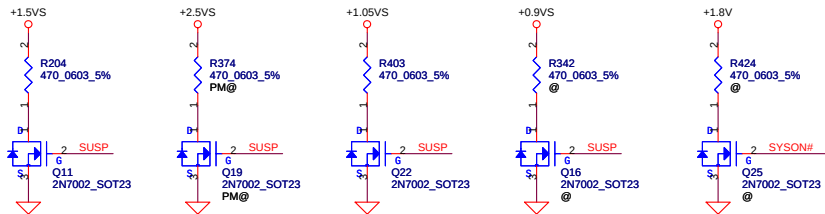
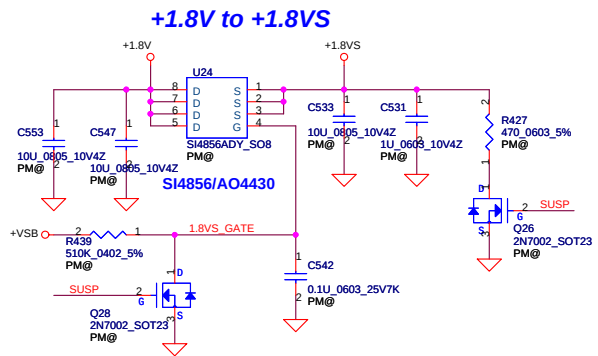
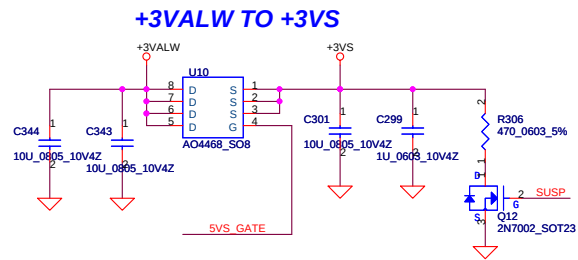
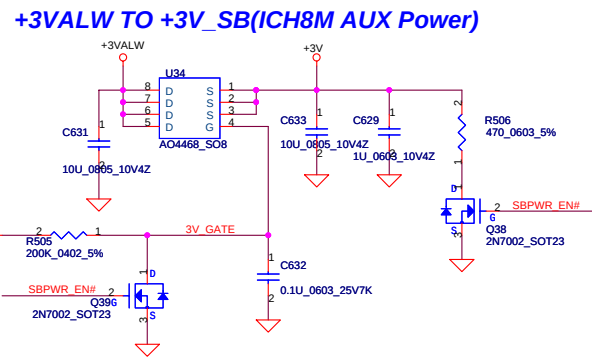
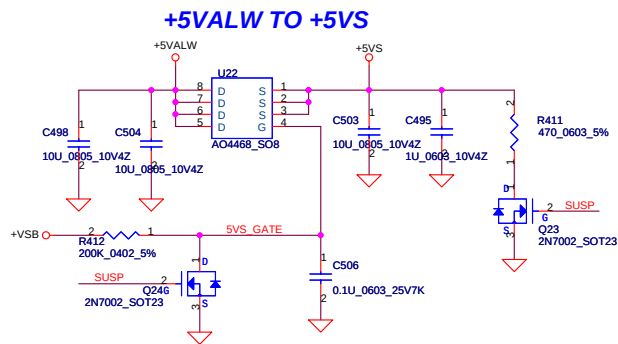


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						Document Number		Rev	
						ICL50/ICK70 M/B LA-3551P Schematic			
Date:		Monday, April 23, 2007		Sheet		34		of 48	

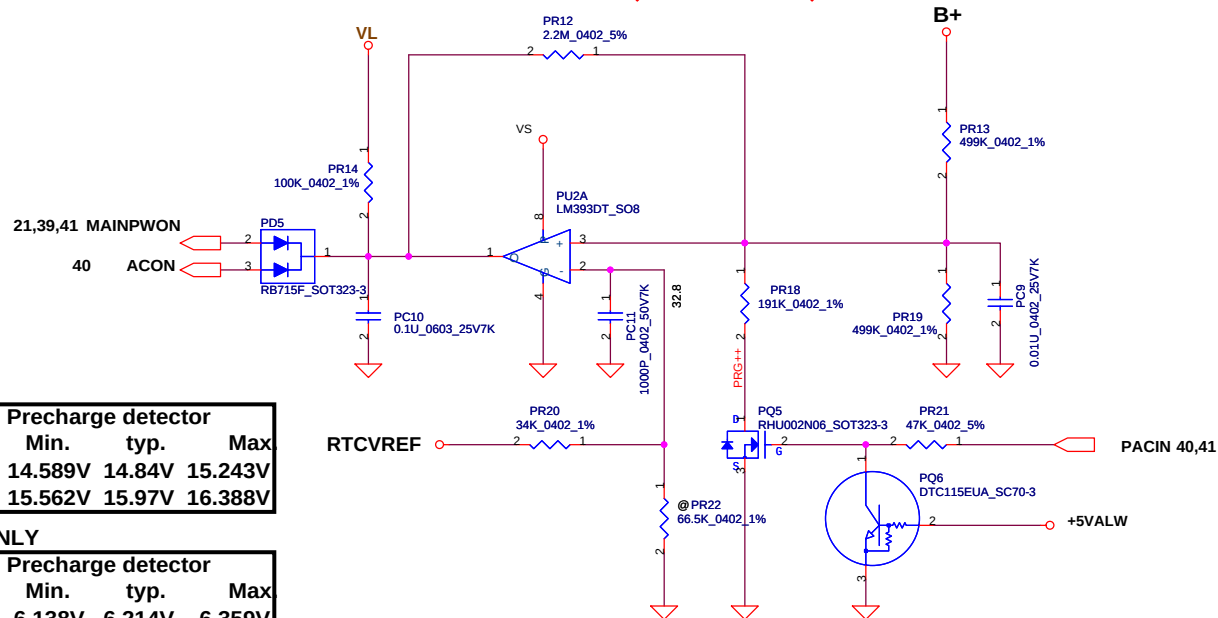
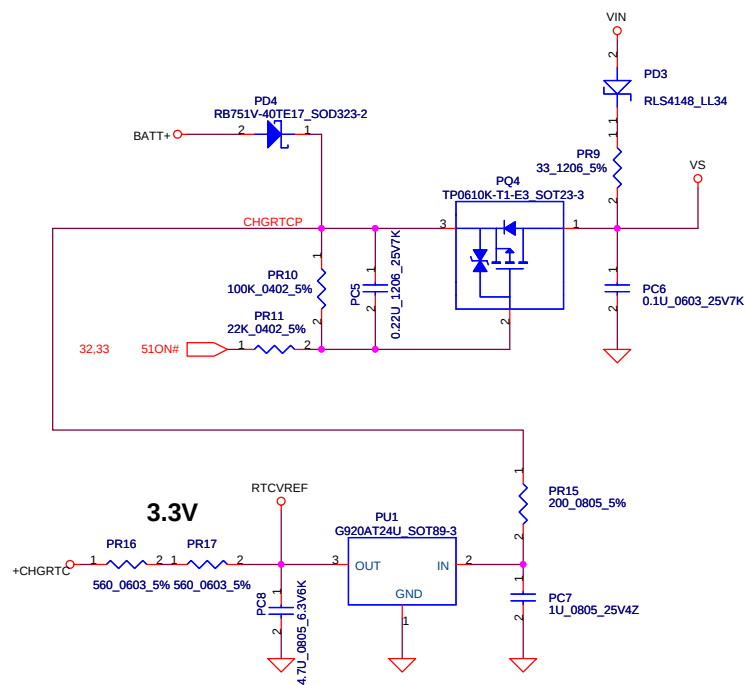
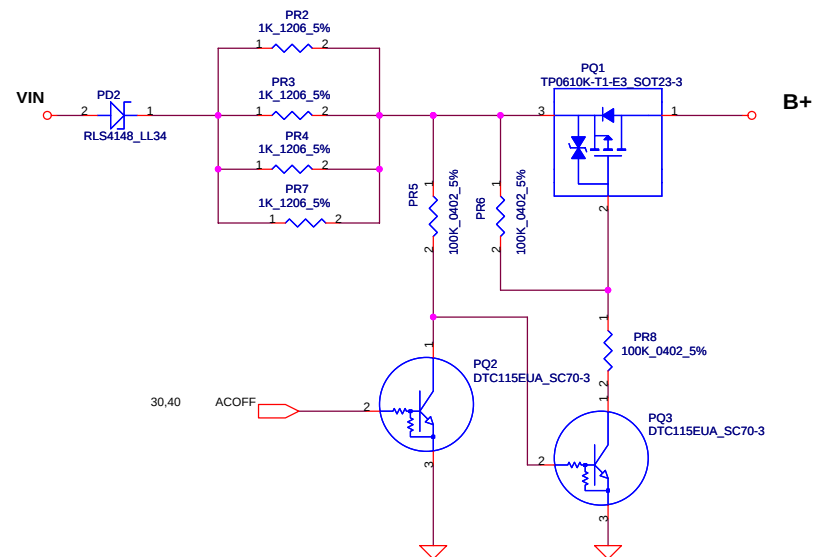
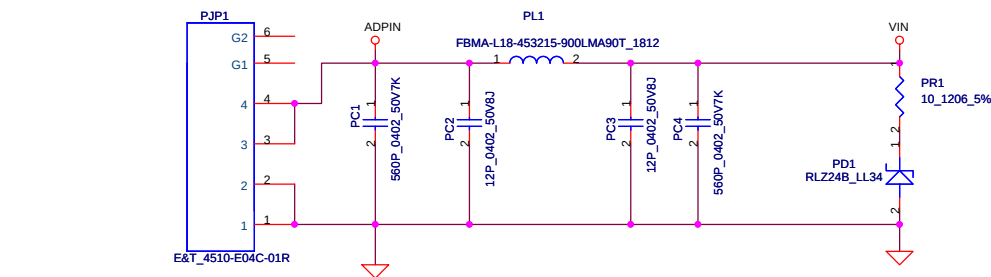
FAN1 Conn



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				ICL50/ICK70 M/B LA-3551P Schematic	1
				Date	Monday, April 23, 2007
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				Document Number	Rev
				ICL50/ICK70 M/B LA-3551P Schematic	
				Date: Monday, April 23, 2007	Sheet 37 of 48

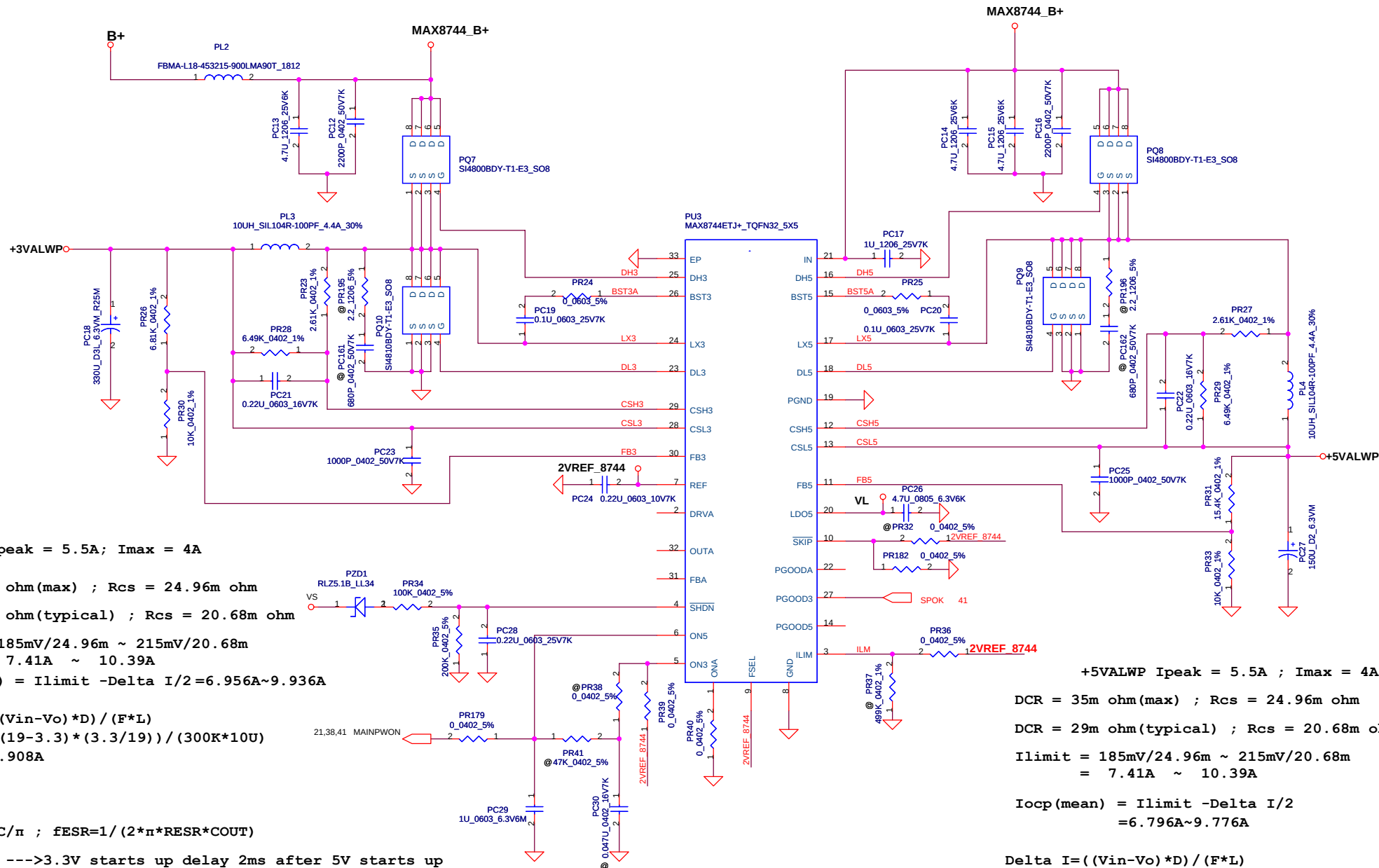


ACIN

	Precharge detector		
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

	Precharge detector		
	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

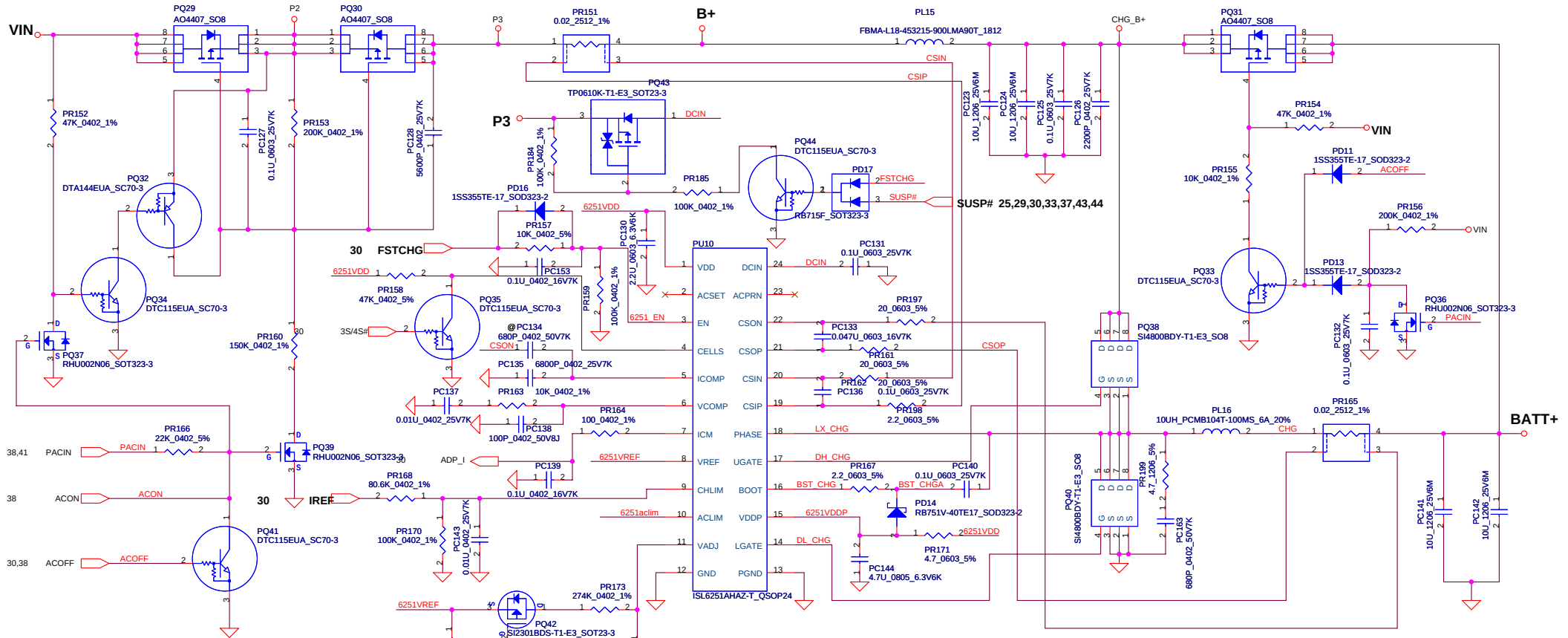


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				ICL50/ICK70	1.0
				Date: Thursday, April 19, 2007	Sheet 39 of 48

Iada=0~4.74A (90W)

ADP_I = 19.9*Iadapter*Rsense

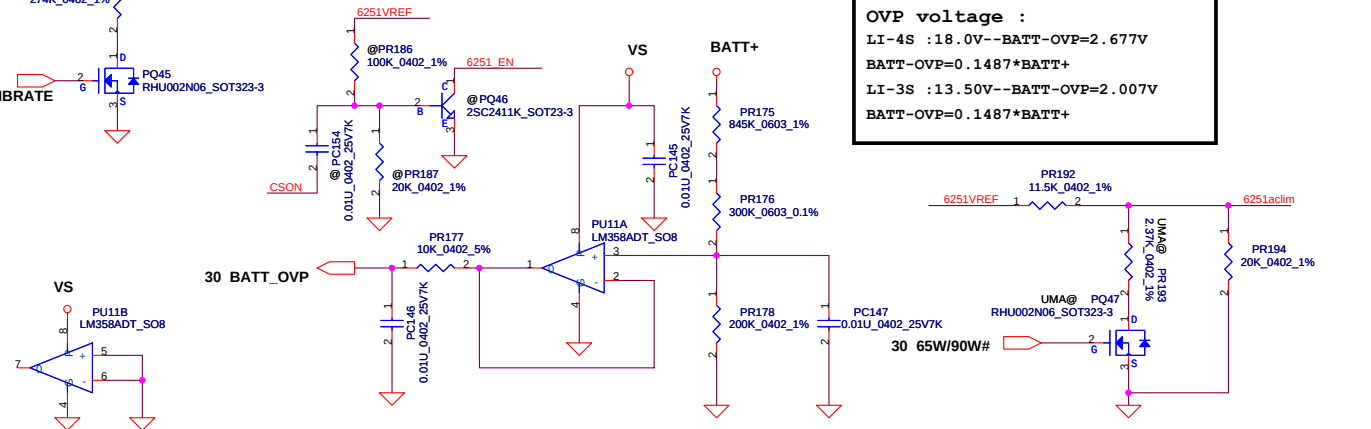
CP = 85%*Iada ; CP = 4.07A



CP mode
 $I_{input} = (1/0.02) * ((0.05 * V_{acli}) / (2.39 + 0.05))$
 where $V_{acli} = 1.502V$, $I_{input} = 4.07A$
 $V_{acli} = 2.39 * ((10K // 152K) / ((5.76K // 152K) + (10K // 152K)))$
 $= 1.502V$

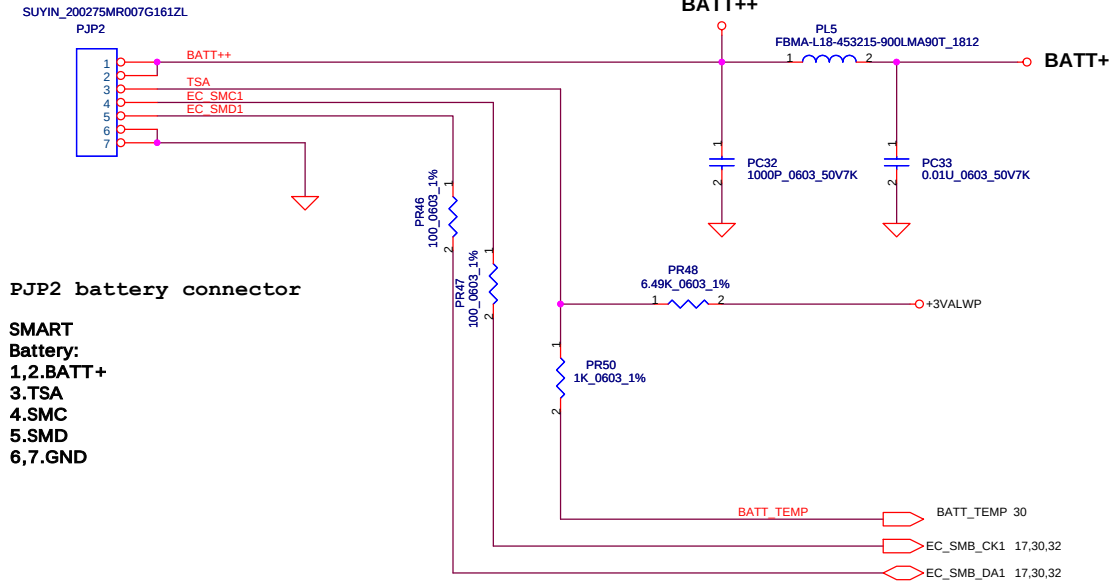
CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V



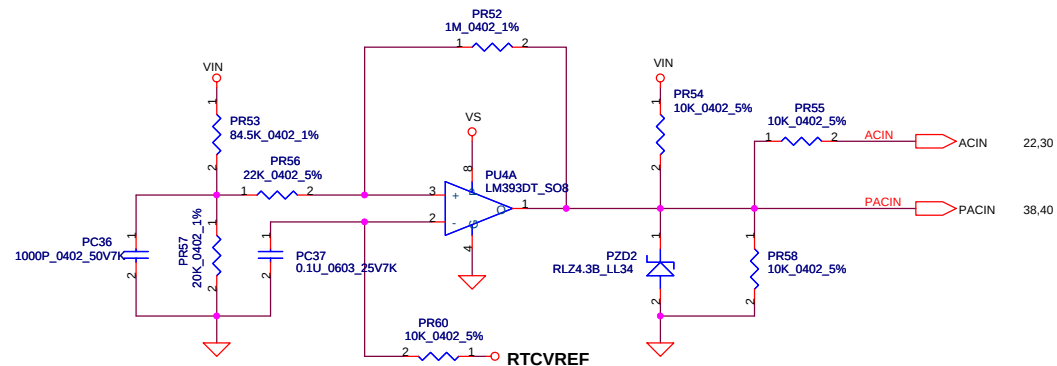
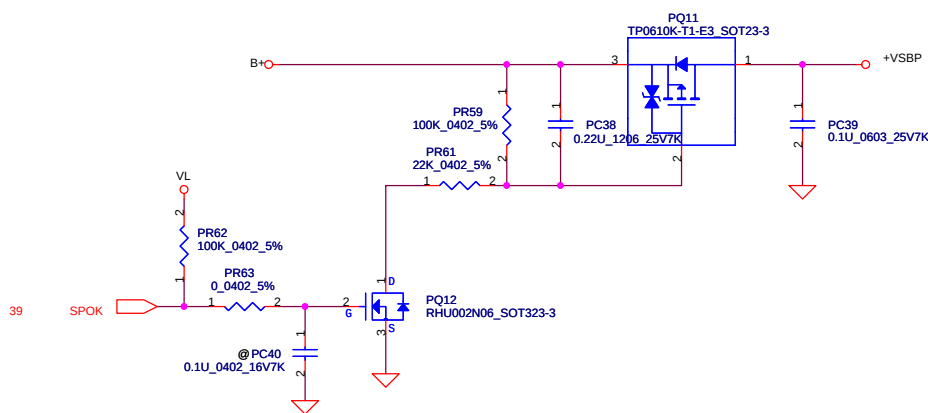
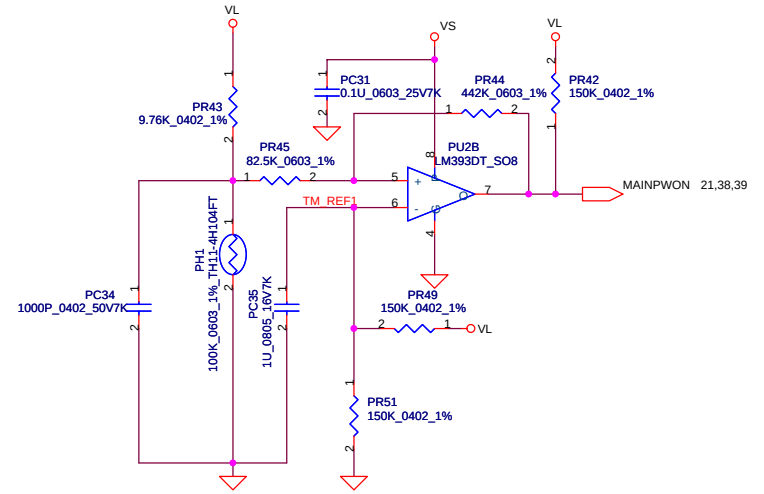
OVP voltage :
 LI-4S : 18.0V -- BATT-OVP = 2.677V
 BATT-OVP = 0.1487 * BATT+
 LI-3S : 13.50V -- BATT-OVP = 2.007V
 BATT-OVP = 0.1487 * BATT+

PH1 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C



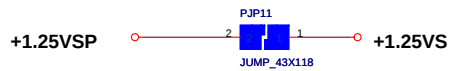
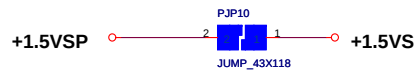
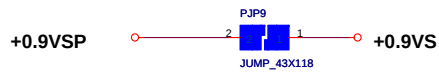
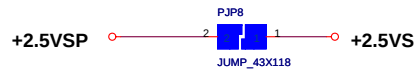
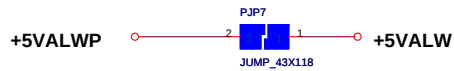
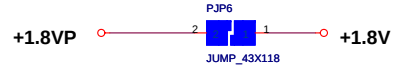
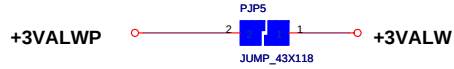
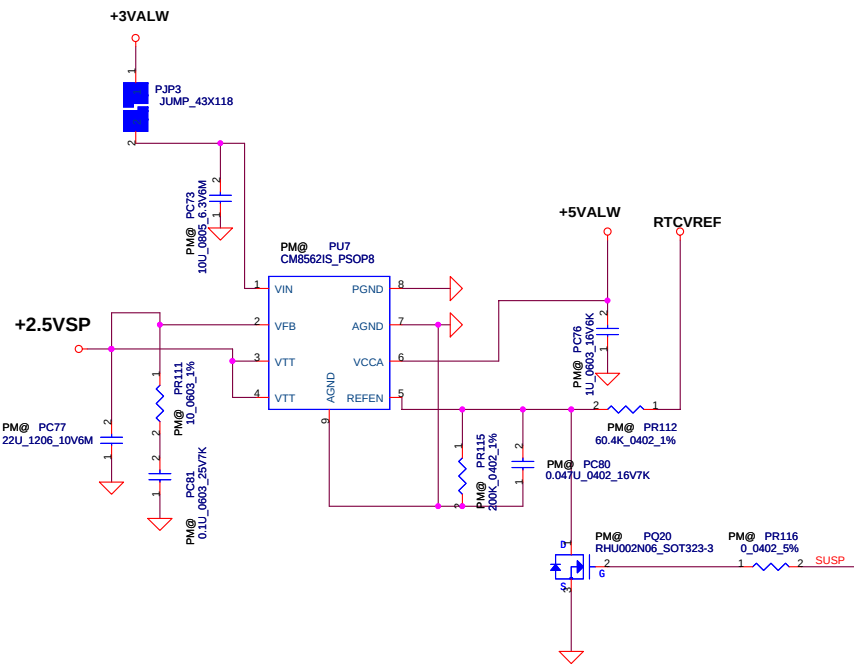
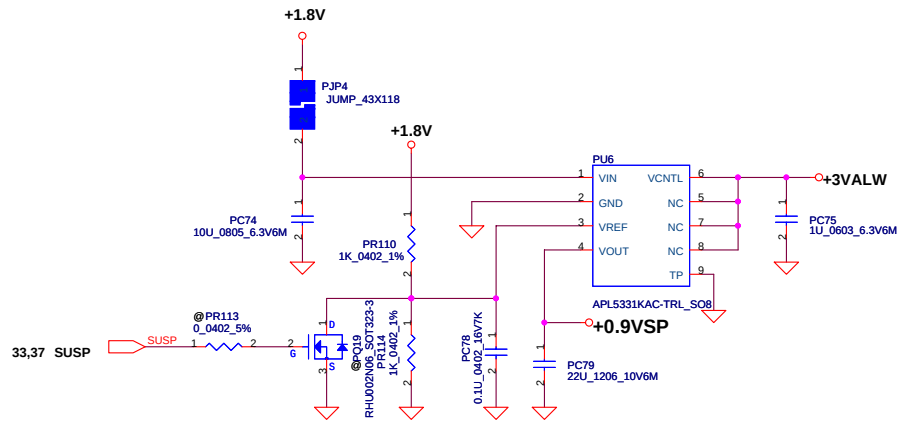
PJP2 battery connector

SMART
Battery:
1,2.BATT+
3.TSA
4.SMC
5.SMD
6,7.GND

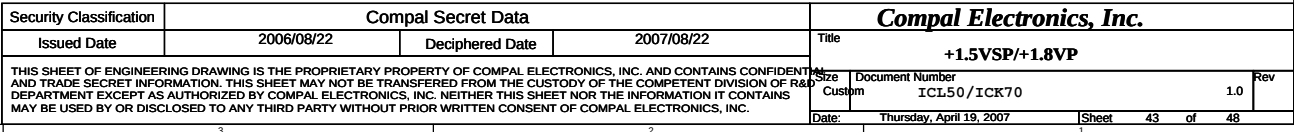


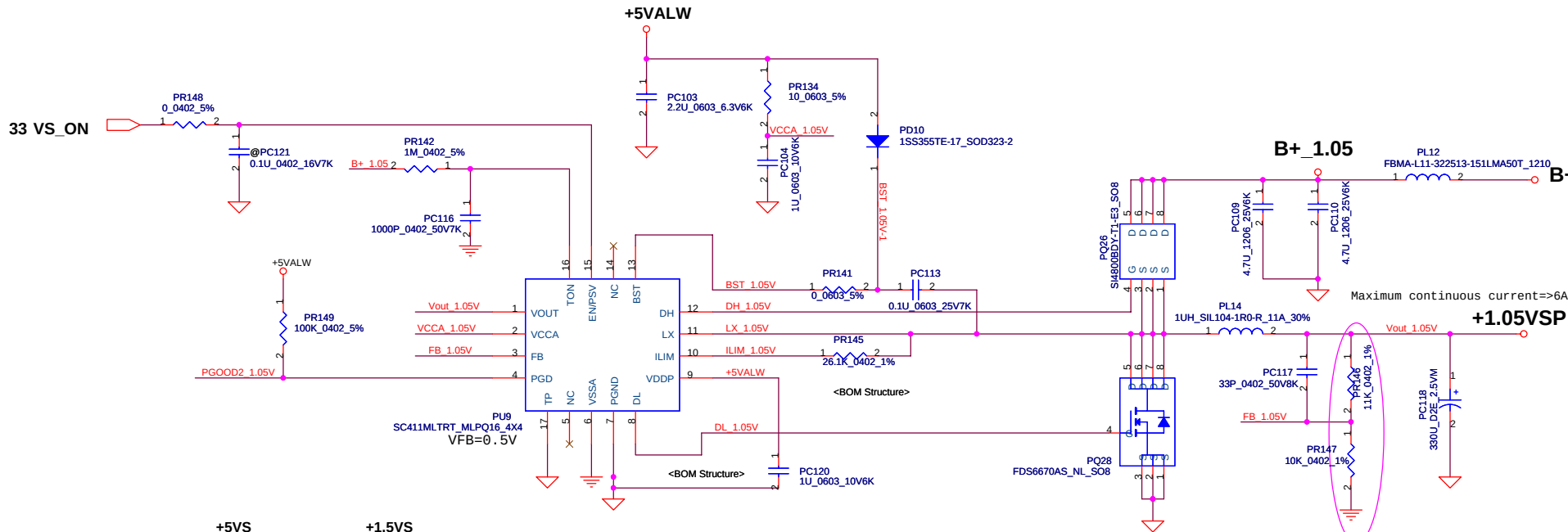
Vin Detector		
Min.	typ.	Max.
H-->L 16.976V	17.257V	17.728V
L-->H 17.430V	17.901V	18.384V

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Issued Date		2006/08/22	Deciphered Date		2007/08/22		Title	+0.9VSP/+2.5VSP	
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Close to IC Side
Differential routing of feedback to VSSA2 and VOUT2 PIN

VFB=0.5V, Ipeak=14.02A, Imax=9.814A

The current rating of +1.05VSP include +VCC_GFX current.

$$V_o = VFB * (1 + PR146 / PR147) = 1.05V$$

$$T_{on} = (3.3E-12 * (PR142 + 37K) * (V_{out} / V_{Bat})) + 50ns = 0.2391\mu s$$

SI4810BDY: Rds(on) => Typ: 9mOhm
Max: 11.5 mOhm

$$I_{valleymin} = 9 * 10E-6 * (PR145 / R_{ds}(ON))_{max} * 1.5$$

$$= 9 * 10E-6 * (26.1K / (0.0115 * 1.5)) = 13.617A$$

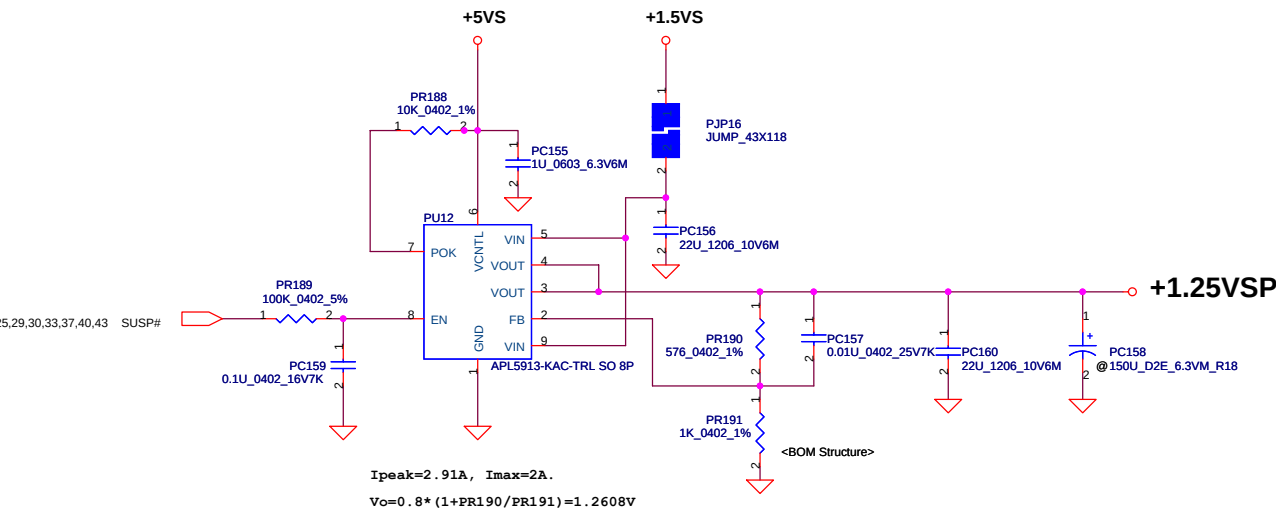
$$I_{valleymax} = 11 * 10E-6 * (PR145 / R_{ds}(ON))_{min} * 1.2$$

$$= 11 * 10E-6 * (26.1K / (0.009 * 1.3)) = 20.076A$$

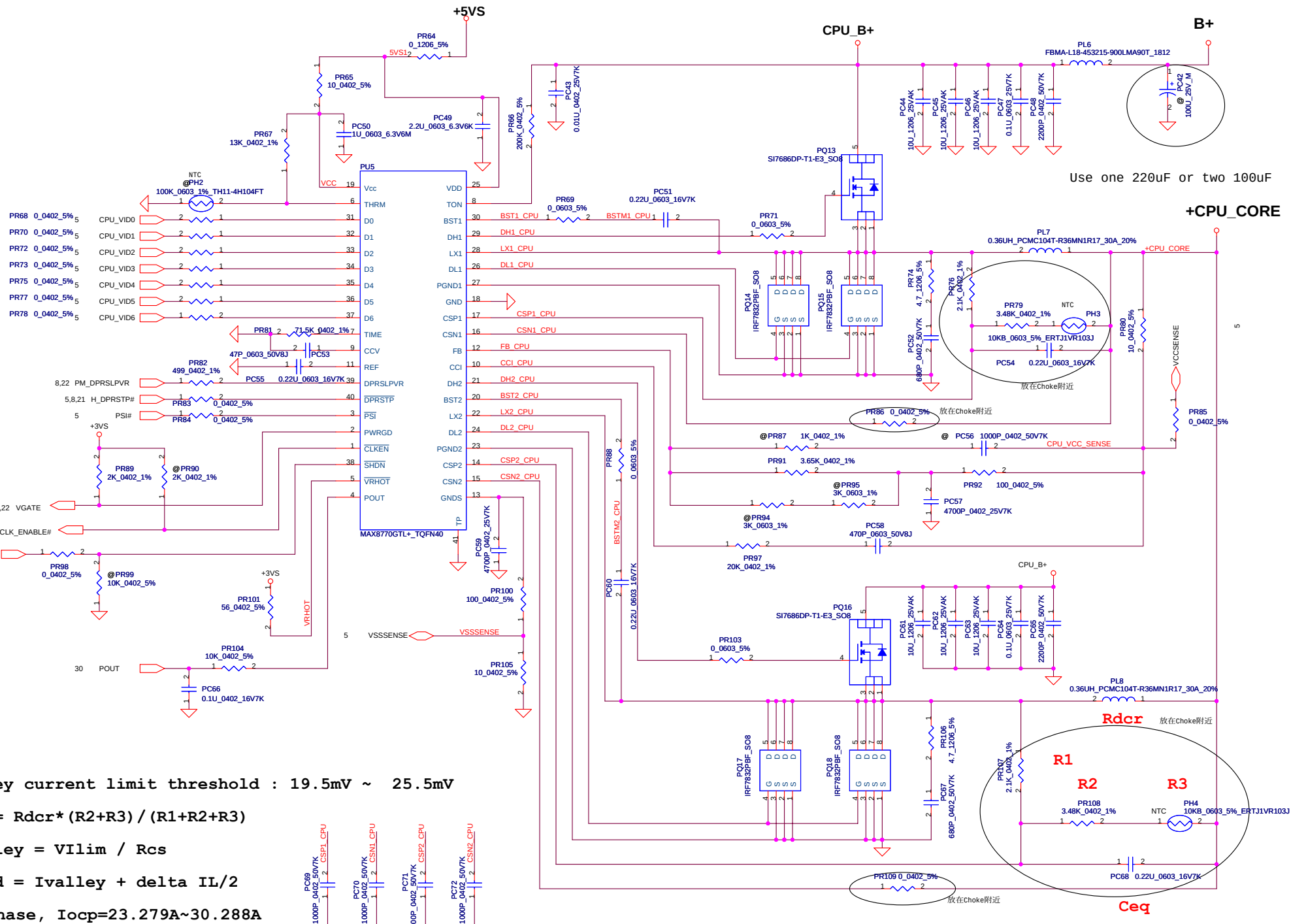
$$I_{ripple} = (v_{in} - v_{out}) * (T_{on} / L) = 4.292A, 1/2 I_{ripple} = 2.146A$$

$$I_{ocp} = I_{valley} + I_{ripple} / 2$$

OCP=>15.763A~22.222A



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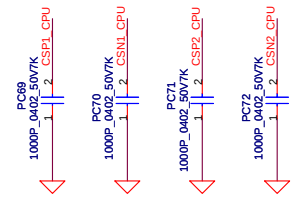
Valley current limit threshold : 19.5mV ~ 25.5mV

$$R_{cs} = R_{dcr} * (R2 + R3) / (R1 + R2 + R3)$$

$$I_{valley} = V_{lim} / R_{cs}$$

$$I_{load} = I_{valley} + \Delta IL / 2$$

Per phase, $I_{ocp} = 23.279A \sim 30.288A$



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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	CPU_CORE high side MOS desine change	In order to prevent EOL of SI7840, change to SI7686.	0.1	45	Change PQ13 and PQ16 form SB578400080(S TR SI7840DP-T1-E3 1N SO8) to SB000008L80(S TR SI7686DP-T1-E3 1N SO8).	10/30/06	EVT
2	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ43 SB906100210(S TR TP0610K)	12/21/06	DVT
3	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ44 SB301150000(S TR DTC115EUA)	12/21/06	DVT
4	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PD16 SC1SS355010(S DIO 1SS355) Delete PD12 SC1SS355010(S DIO 1SS355)	12/21/06	DVT
5	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PD17 SCSB715F000(S DIO RB715F)	12/21/06	DVT
6	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR184,PR185 SD034100380(S RES 1/16W 100K 0402 1%)	12/21/06	DVT
7	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PC153 SE076104K80(S CER CAP 0.1U 0402 16V K X7R)	12/21/06	DVT
8	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ45 SB502060000(S TR RHU002N06)	12/21/06	DVT
9	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ46 SB324110010(S TR 2SC411K)	12/21/06	DVT
10	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR183 SD034274380(S RES 1/16W 274K 0402 1%)	12/21/06	DVT
11	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR186 SD034100380(S RES 1/16W 100K 0402 1%)	12/21/06	DVT
12	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR187 SD034200280(S RES 1/16W 20K 0402 1%)	12/21/06	DVT
13	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PC154 and PC146 SE075103K80(S CER CAP 0.01U K 25V X7R 0402)	12/21/06	DVT
14	Noise issue in S3 mode and idle mode.	In order to prevent noise issue in S3 mode and idle mode.	0.2	40	Add PC42 SF22004M210(S CAP 220U 25V_M)	12/21/06	DVT
15	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Change PR157 from SD028000080(s res 1/16w 0 0402 5%) TO SD0281000280(S RES 1/16W 10K 0402 5%)	12/21/06	DVT
16	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PR34 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100380(S RES 1/16W 100K 0402 5%)	12/21/06	DVT
17	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PR35 SD028100380(S RES 1/16W 100K 0402 5%) to SD028200380(S RES 1/16W 200K 0402 5%)	12/21/06	DVT
18	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PC28 from SE042104K80(S CER CAP 0.1U 25V K X7R 0603) to SE000005ZM8(S CER CAP 0.22U 25V K X7R 0603)	12/21/06	DVT
19	CPU MOSFET switching has interference.	Improve CPU switching interference.	0.2	45	Change PC69,PC70,PC71,PC72 from SE082221J80 to SE068102J80 (S CER CAP 1000P 25V J NPO 0402)	12/21/06	DVT
20	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PU7 SA085620080 from X63470BOL01.	12/21/06	DVT
21	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PQ20 SB502060000 from X63470BOL01.	12/21/06	DVT
22	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR111 SD014100A80 from X63470BOL01.	12/21/06	DVT
23	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR112 SD034604280 from X63470BOL01.	12/21/06	DVT

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1	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR115 SD034200380 from X63470BOL01.	10/30/06	EVT
2	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR116 SD028000080 from X63470BOL01.	12/21/06	DVT
3	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC73 SE142475K80 from X63470BOL01.	12/21/06	DVT
4	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC76 SE135105K80 from X63470BOL01.	12/21/06	DVT
5	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC77 SE116226M80 from X63470BOL01.	12/21/06	DVT
6	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC80 SE076473K80 from X63470BOL01.	12/21/06	DVT
7	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC81 SE042104K80 from X63470BOL01.	12/21/06	DVT
8	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PQ25 SB548000310(S TR SI4800BDY).	12/27/06	DVT
9	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PQ27 SB548100020(S TR 4810BDY)	12/27/06	DVT
10	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Change PD10 from SC1P202U010 to SC1SS355010.	12/27/06	DVT
11	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR135 SD034100380.	12/27/06	DVT
12	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR140,SD013000080, PR150 SD028000080.	12/27/06	DVT
13	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR181 SD013100A80.	12/27/06	DVT
14	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR139 SD034150280.	12/27/06	DVT
15	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR144 SD034100280	12/27/06	DVT
16	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR137 SD034105280.	12/27/06	DVT
17	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR138 SD028100480.	12/27/06	DVT
18	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC105,PC106 SE142475K80.	12/27/06	DVT
19	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC107,PC151 SE080105K80.	12/27/06	DVT
20	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC108 SE074102K80.	12/27/06	DVT
21	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC111 SE042104K80.	12/27/06	DVT
22	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC112 SE068330K80	12/27/06	DVT
24	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PL13 SH000008Y80.	12/27/06	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC114 SGA20221D30	12/27/06	DVT
2	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Change PU9 from SA00001FD80 to SA00001FB80	12/27/06	DVT
3	For SMT BOM convenient.	For SMT BOM convenient.	0.3	40	Change PD14 from SC1H751H010 to SC1B751V010.	12/27/06	DVT
4	Increase _1.5VSP OCP point	Increase _1.5VSP OCP point for +1.25VSP new solution.'	0.3	43	Change PR128 from SD034154280 to SD034374380.	12/27/06	DVT
5	Decrease +1.05VSP OCP point.	Decrease +1.05VSP OCP point.	0.3	44	Change PR145 from SD034324280 to SD034261280		DVT
6	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PU12 SA000015410.	12/27/06	DVT
7	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR188 SD034100280.	12/27/06	DVT
8	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR189 SD034100380.	12/27/06	DVT
9	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR191 SD034100180.	12/27/06	DVT
10	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR190 SD034576080.	12/27/06	DVT
11	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC155 SE107105M80.	12/27/06	DVT
12	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC156, PC160 SE116226M80	12/27/06	DVT
13	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC157 SE075103K80.	12/27/06	DVT
14	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC159 SE076104K80.	12/27/06	DVT
15	Increase +1.5VSP output capacitor.	Increase +1.5VSP output capacitor.	0.3	43	Change PC98 from SGA20221D30 to SGA19331D00	12/27/06	DVT
16	Cost issue.	Cost issue.	0.3	44	Change PC118 from SGA20471D00 to SGA19331D00.	12/30/06	DVT
17	BOM issue.	BOM issue.	0.3	45	Change PH3, PH4 from SL210021F20 to SL200000200	12/30/06	DVT
18	Assembly issue.	Due to assembly hard, delete PC42.	0.3	45	Delete PC42 SM22004M210.	12/30/06	DVT
19	Cost issue.	Cost issue.	0.4	42	Change PC73 from SE142475K80 to SE093106M80	01/04/06	DVT
20	Cost issue.	Cost issue.	0.4	42	Change PC73 from SE153106K80 to SE093106M80	01/04/06	DVT
21	Add pull high resister for VAGTE.	Add pull high resister for VAGTE.	0.4	45	Add PR89 SD034200180(S RES 1/16W 2K 0402 1%)	01/04/06	DVT
22	Delete PQ46	PQ46 has potential risk to cause system battery OVP.	0.4	40	Delete PQ46 SB324110010(S TR 2SC411K)	01/04/06	DVT
23	Material shipping issue.	Material shipping issue.	0.4	45	Change PC69, PC70, PC71, PC72 from SE068102J80 to SE074102K80	01/04/06	DVT

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1	Cost down	Cost down	0.5	40	Change PQ38 from SB548100020 to SB548000310.	03/09/07	PVT
2	Cost down	Cost down	0.5	40	Change PQ40 from SB548100020 to SB548000310.	03/09/07	PVT
3	For EMI board band issue.	For EMI board band issue.	0.6	40	Add PR199 SD001470B80(S RES 1/4W 4.7 1206 +-5%)	04/01/07	Pre-MP
4	For EMI board band issue.	For EMI board band issue.	0.6	40	Add PC163 SE074681K80(S CER CAP 680P 50V K X7R)	04/01/07	Pre-MP
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