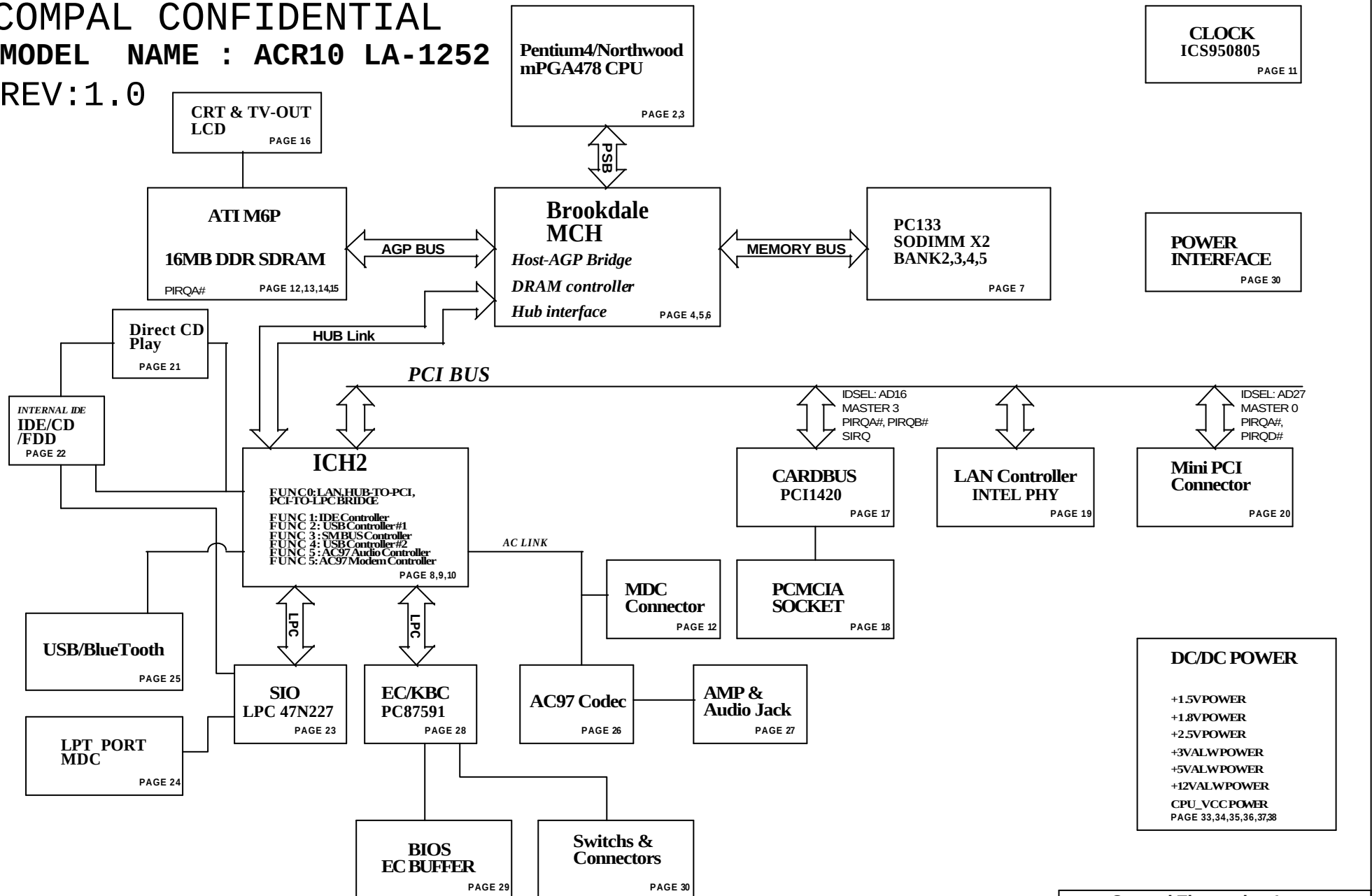


COMPAL CONFIDENTIAL

MODEL NAME : ACR10 LA-1252
REV:1.0



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Date

2002.04.04

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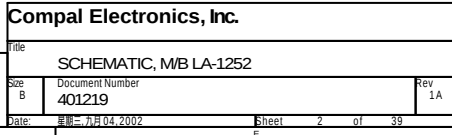
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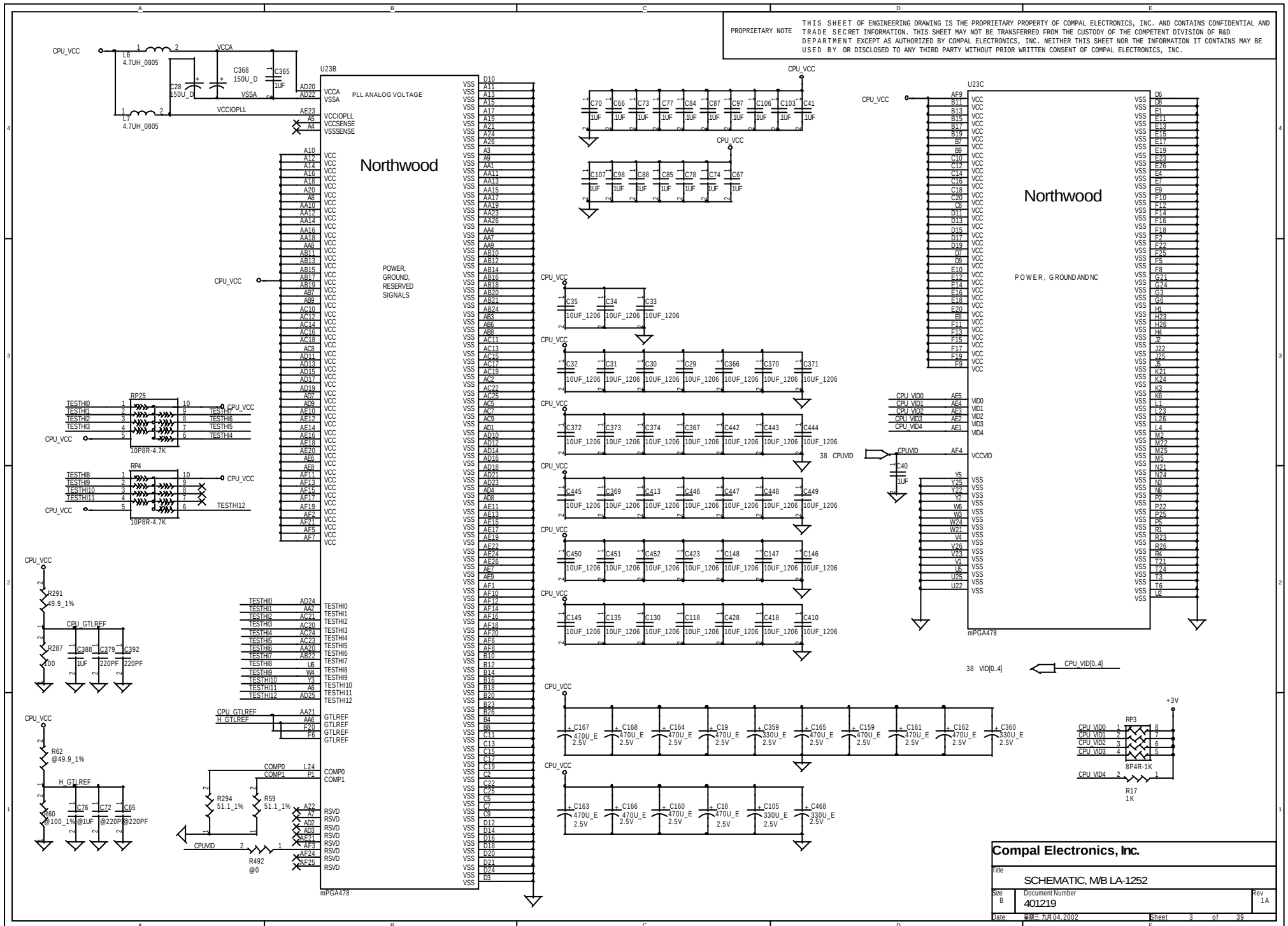
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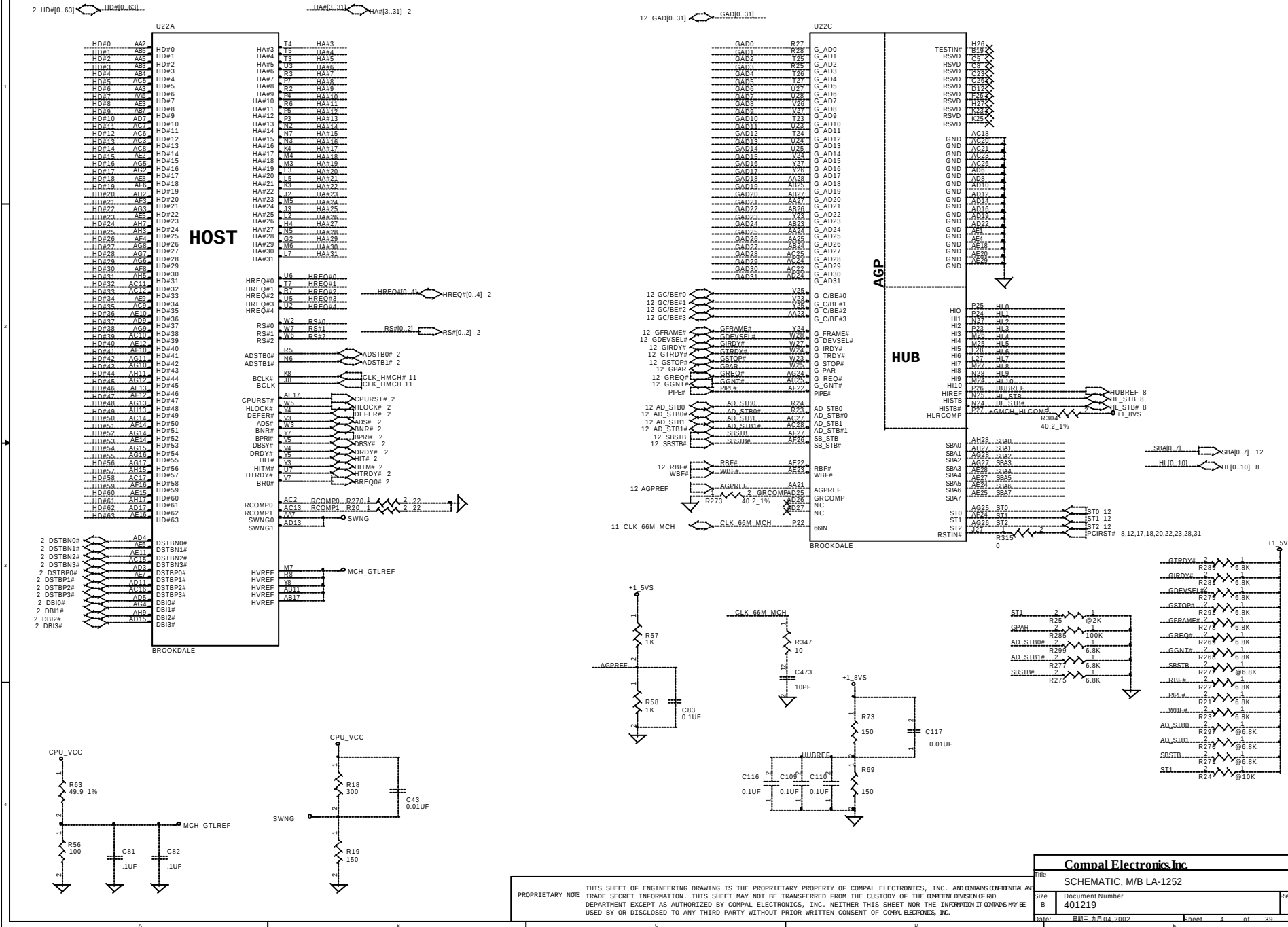
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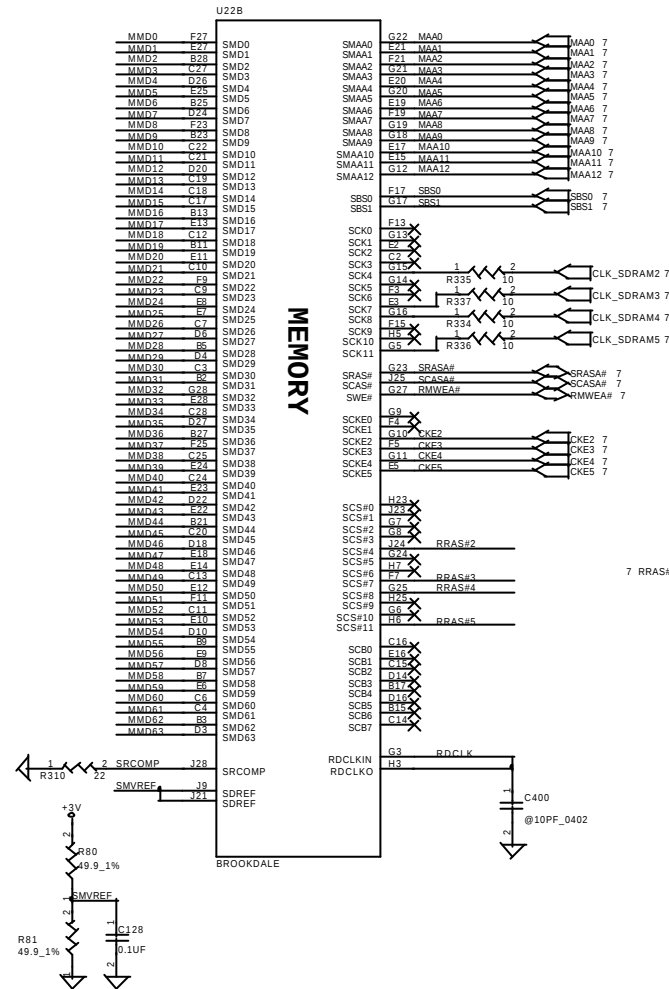
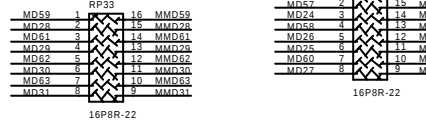
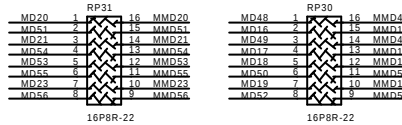
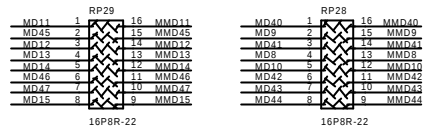
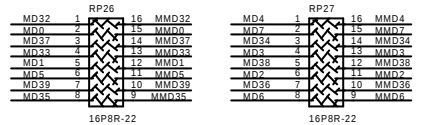


MC-1/3(GTL+,AGP,HUB)



MCH-2/3(SDRAM)

7 MD[0..63] MD[0..63]

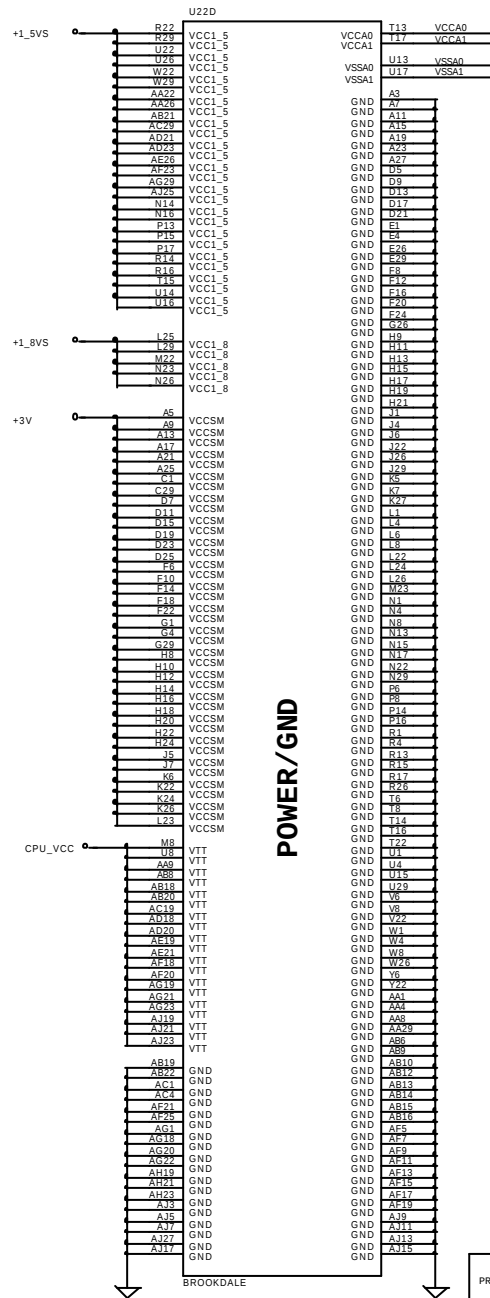


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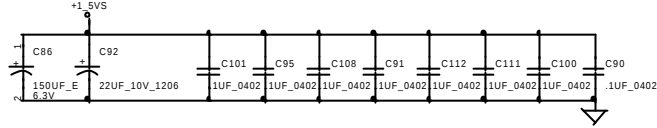
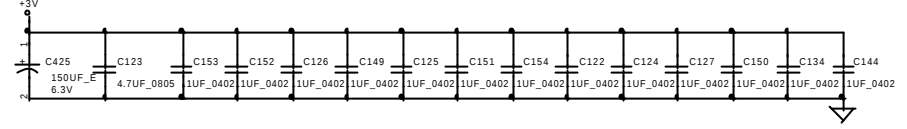
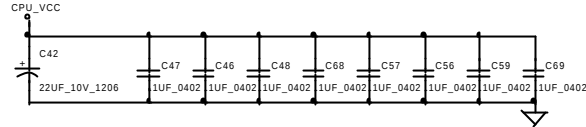
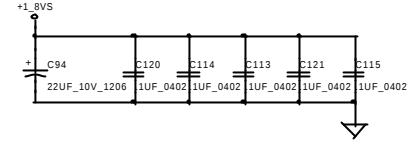
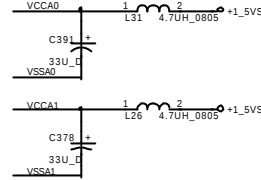
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MCH-3/3(Power)



POWER/GND

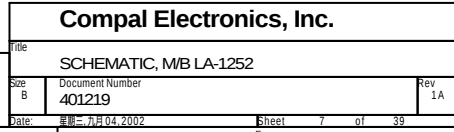


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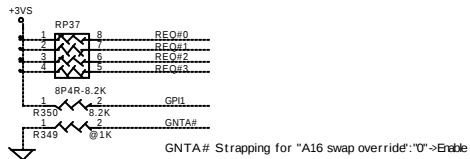
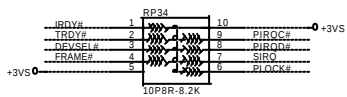
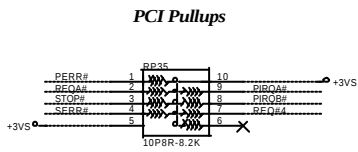
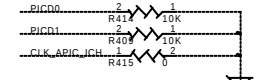
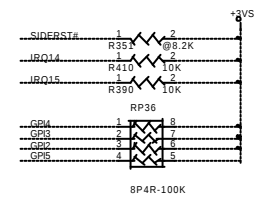
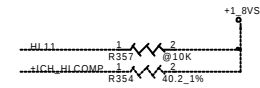
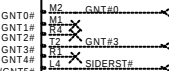
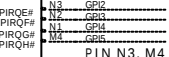
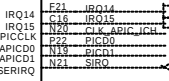
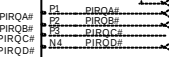
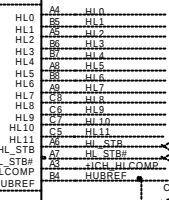
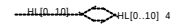
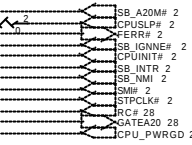
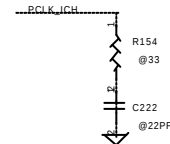
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(FW82801BA)



PCI REQ ASSIGNMENT	
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REQ#1	NC
REQ#2	NC
REQ#3	PCMCIA CONTROLLER
REQ#4	NC

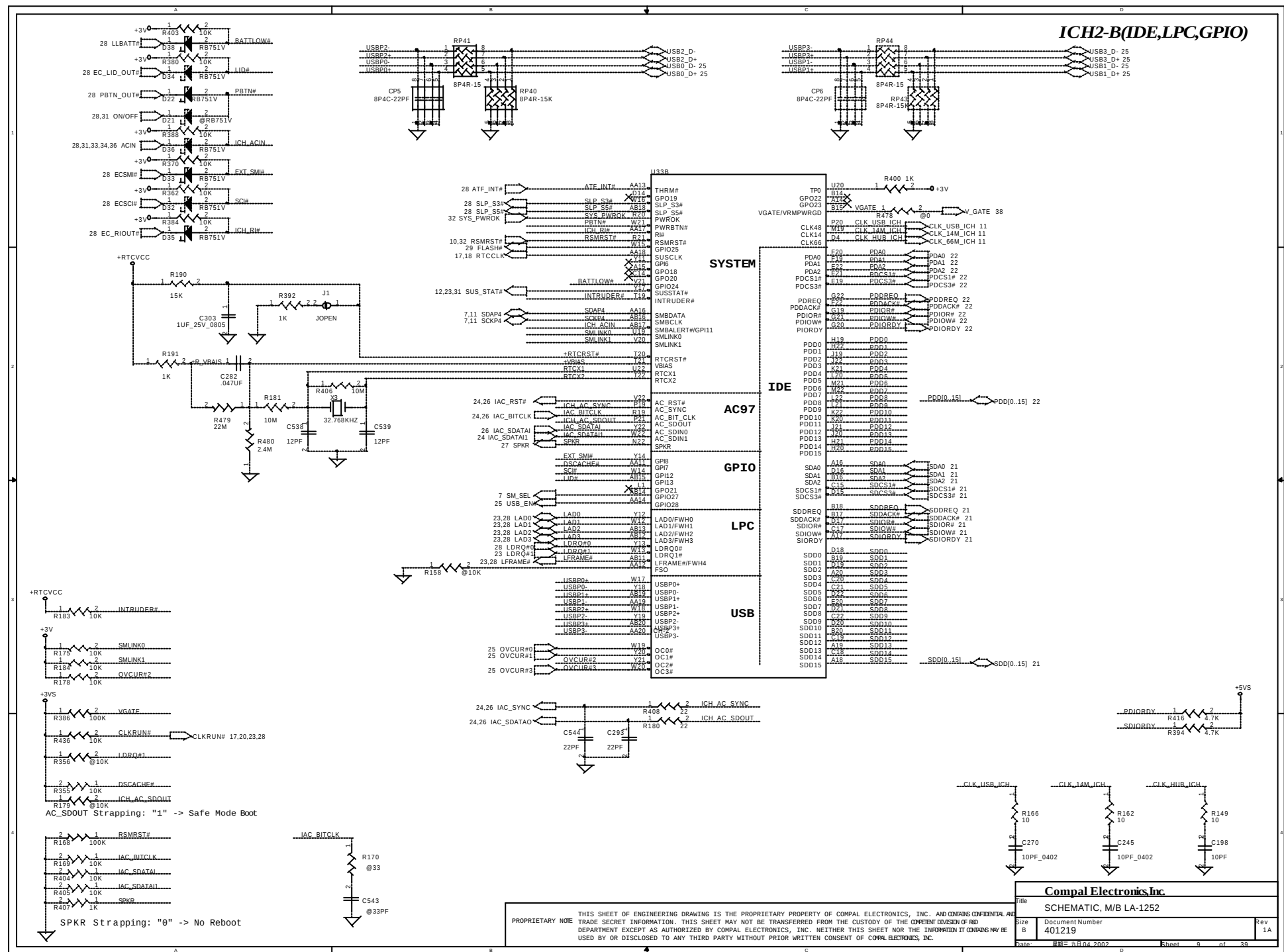


PCI Pullups

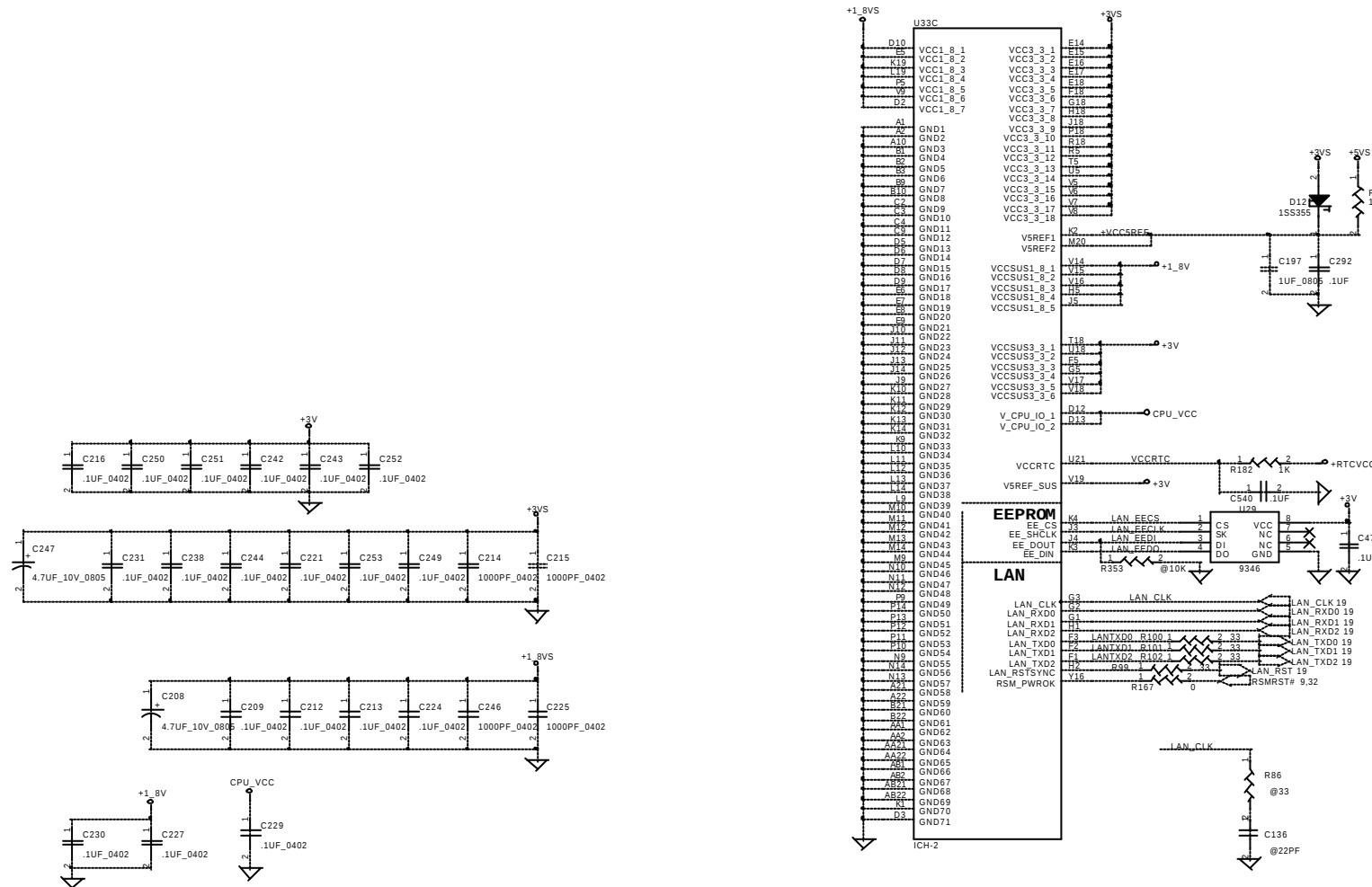
GNTA# Strapping for "A16 swap override": "0" -> Enable

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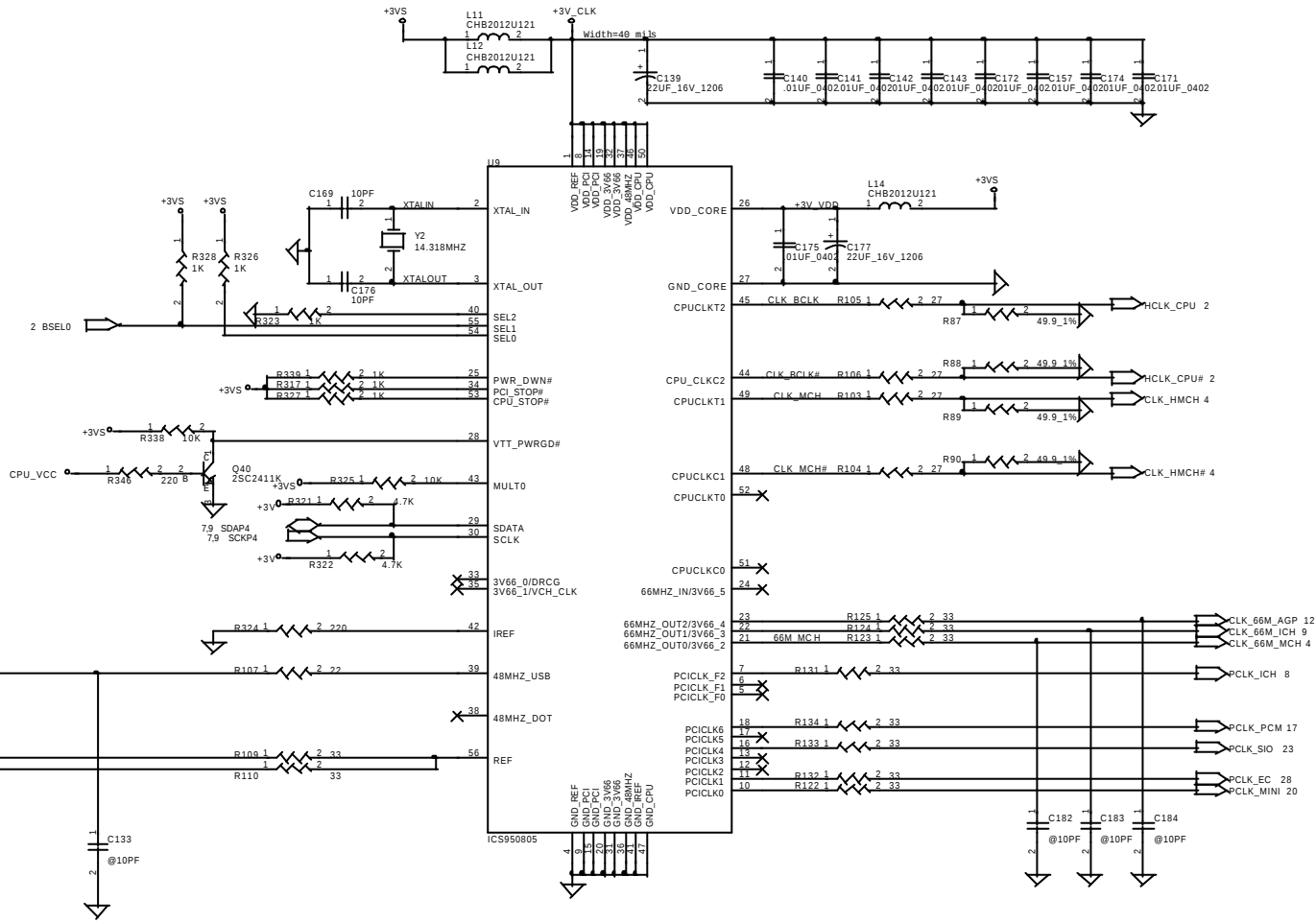
ICH2-C(LAN,Power)



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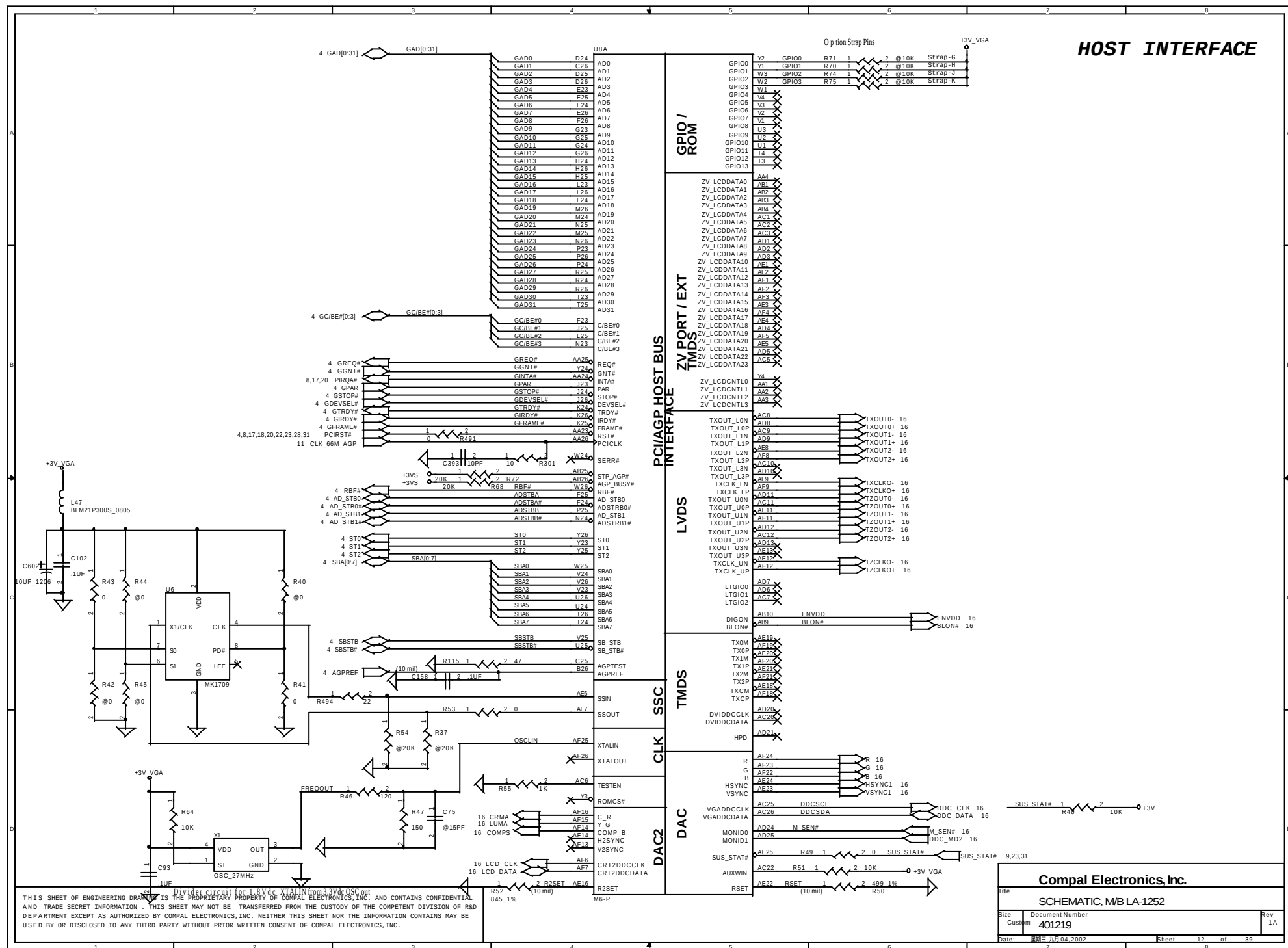
Clock Generator



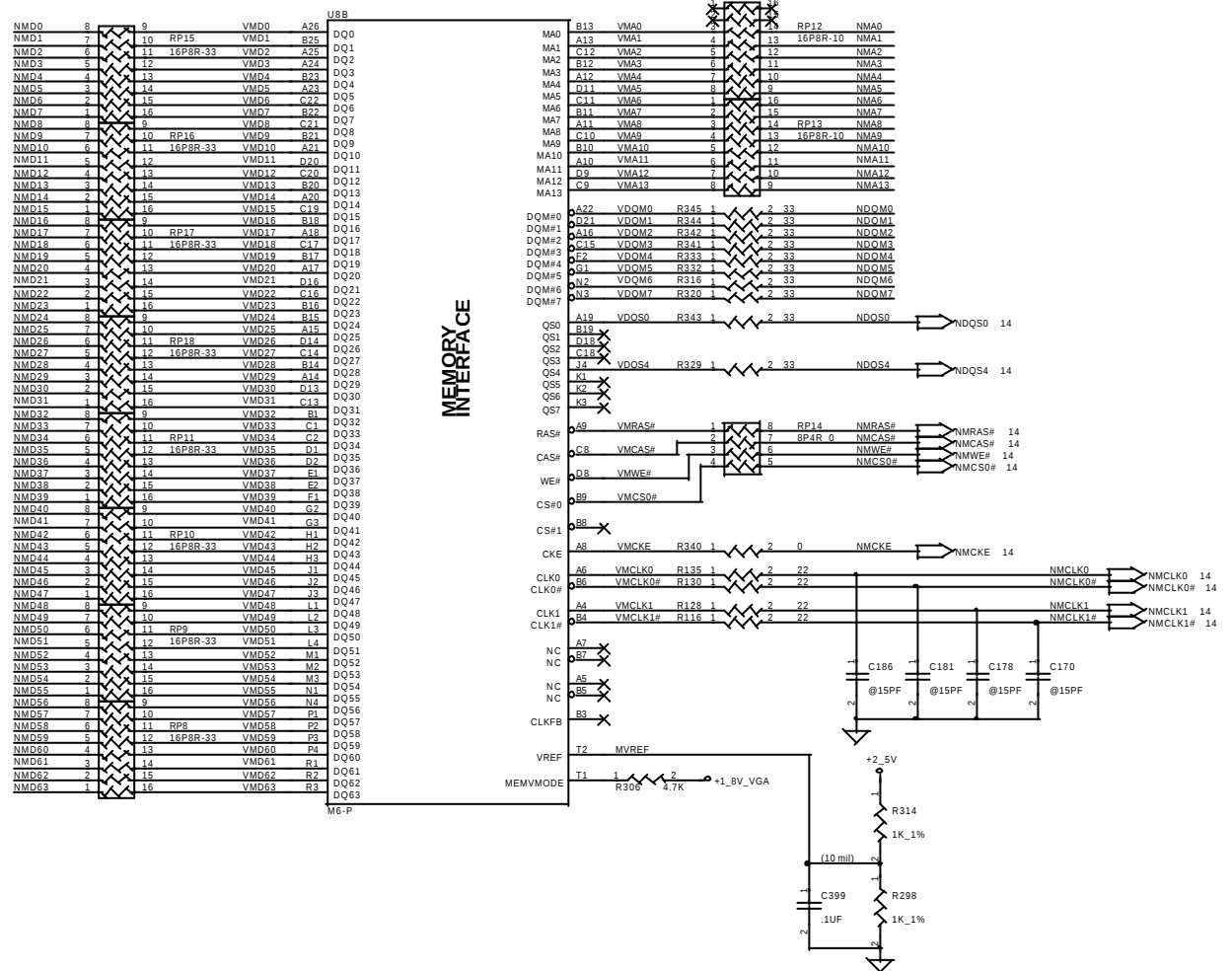
SEL2	SEL1	SEL0	CPUCLK0 (0..21)	CPUCLK1 (0..21)
0	0	0	66.67	66.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

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MEMORY INTERFACE



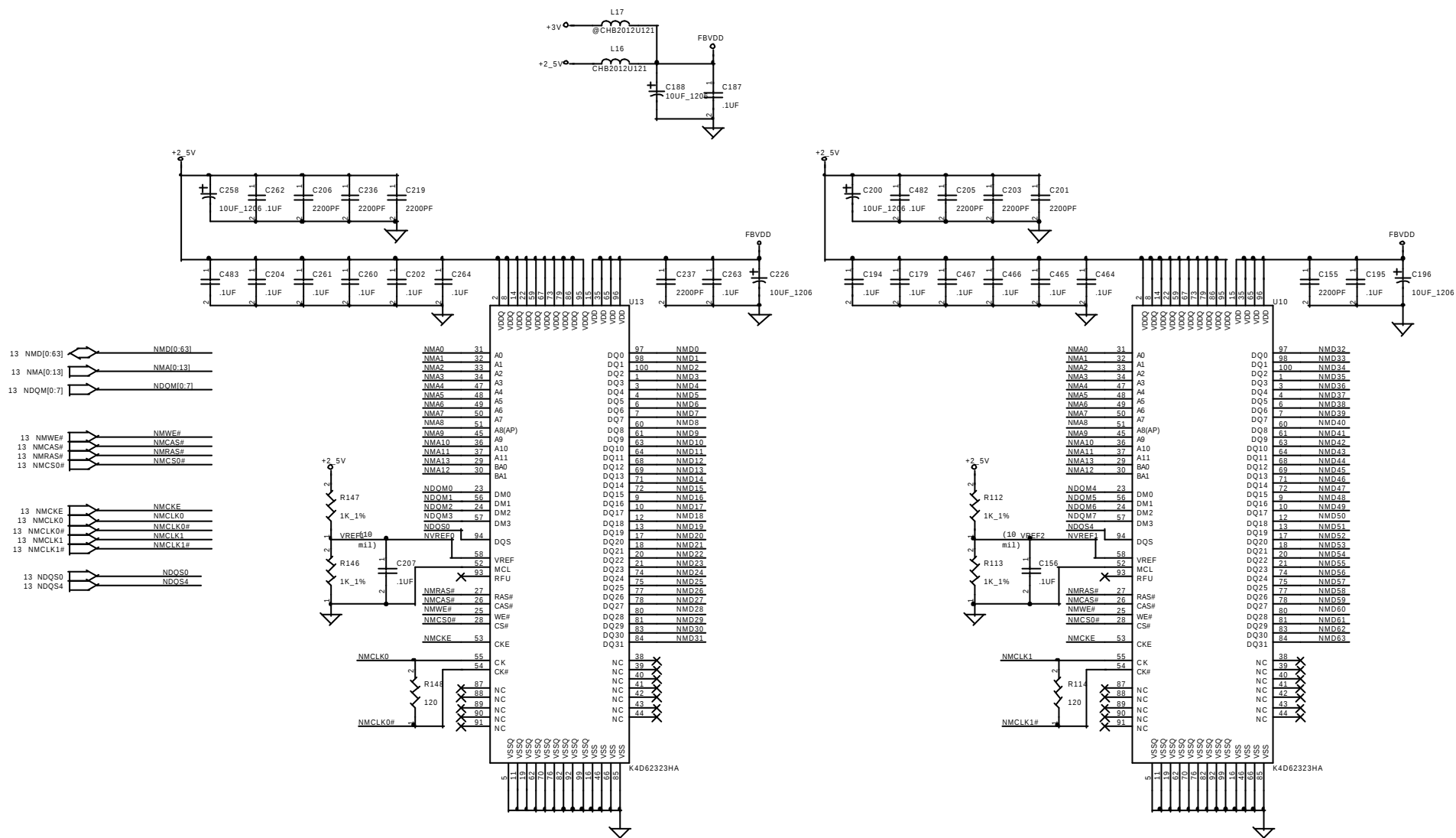
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DDR SDRAM



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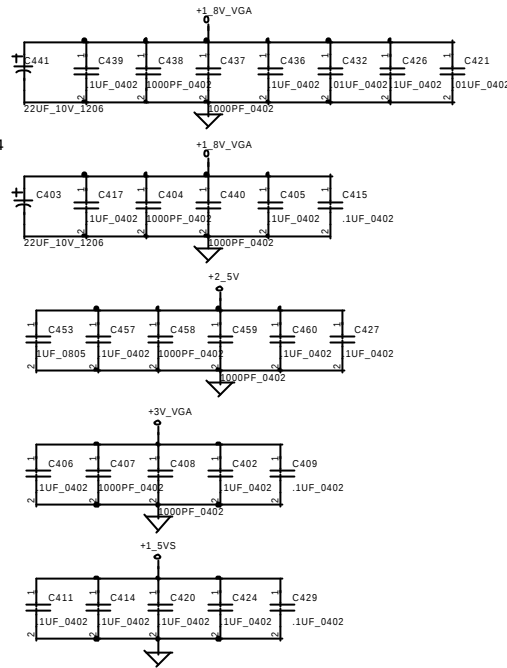
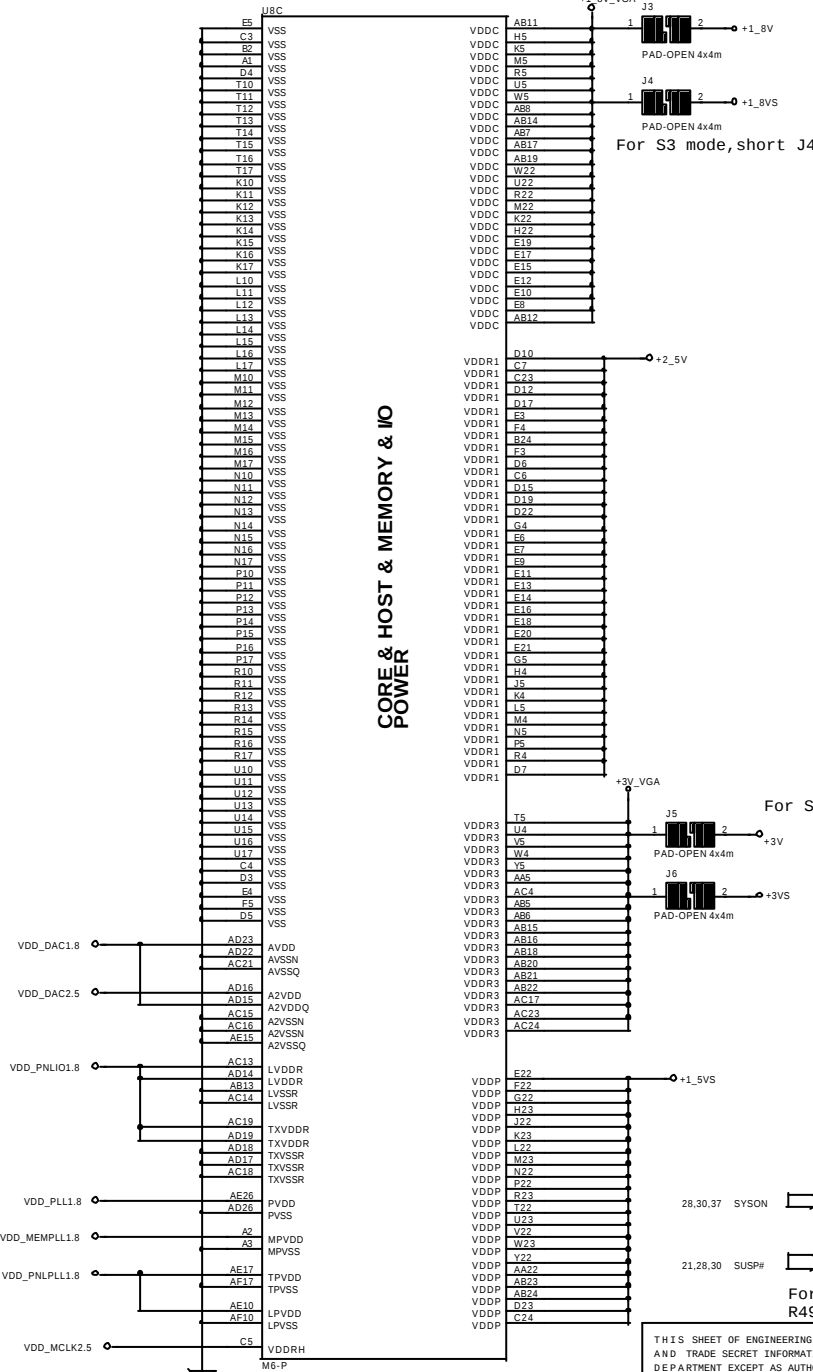
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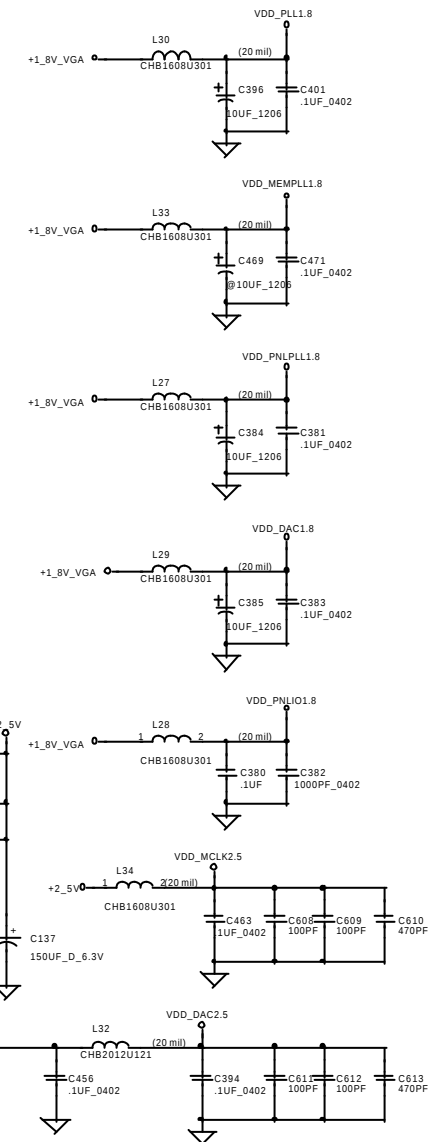
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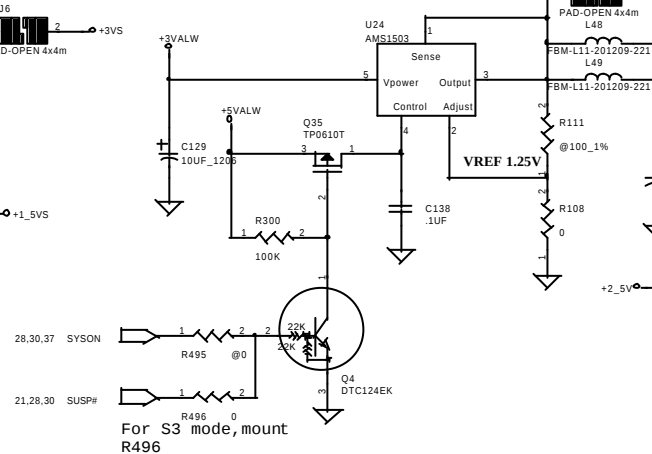
CORE & HOST & MEMORY & IO POWER



POWER INTERFACE

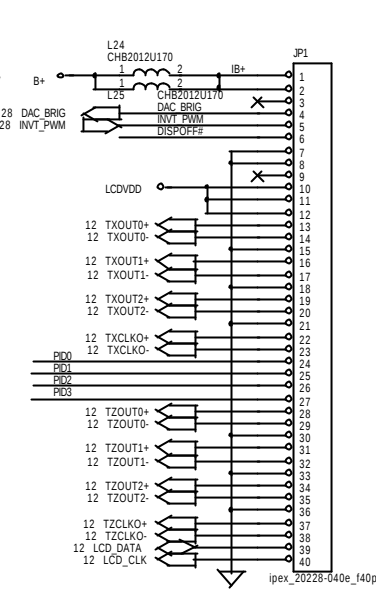
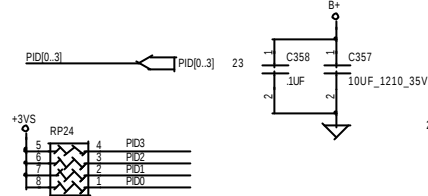
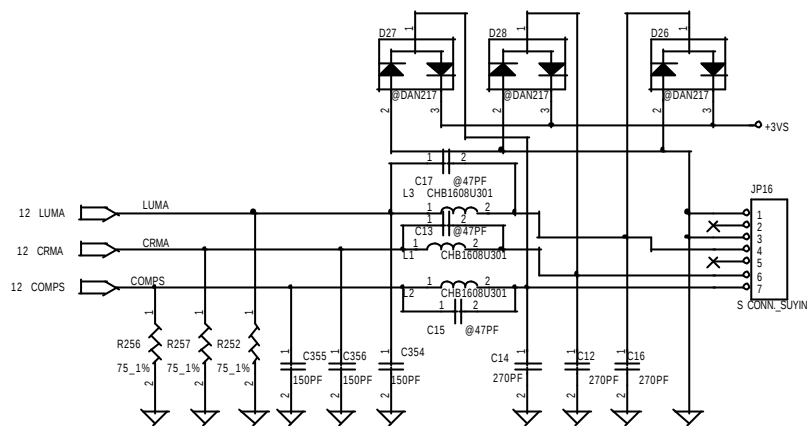


+2.5Vdc Regulator

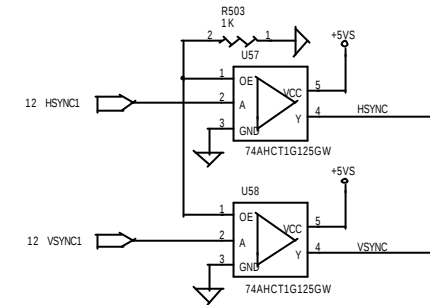
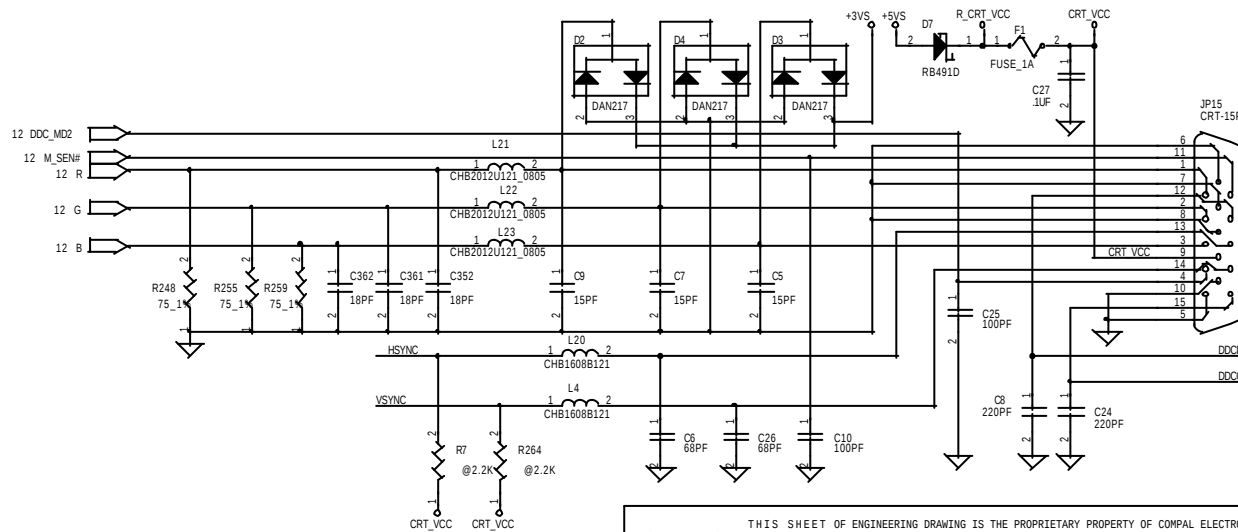


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CRT Connector



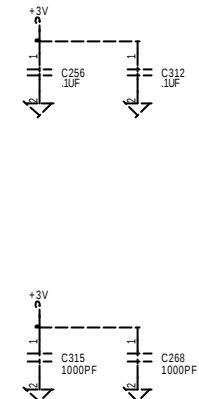
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CARDBUS PCI1420



Power

PCI Interface

Slot B

Slot A

IRQ/DMA

GND

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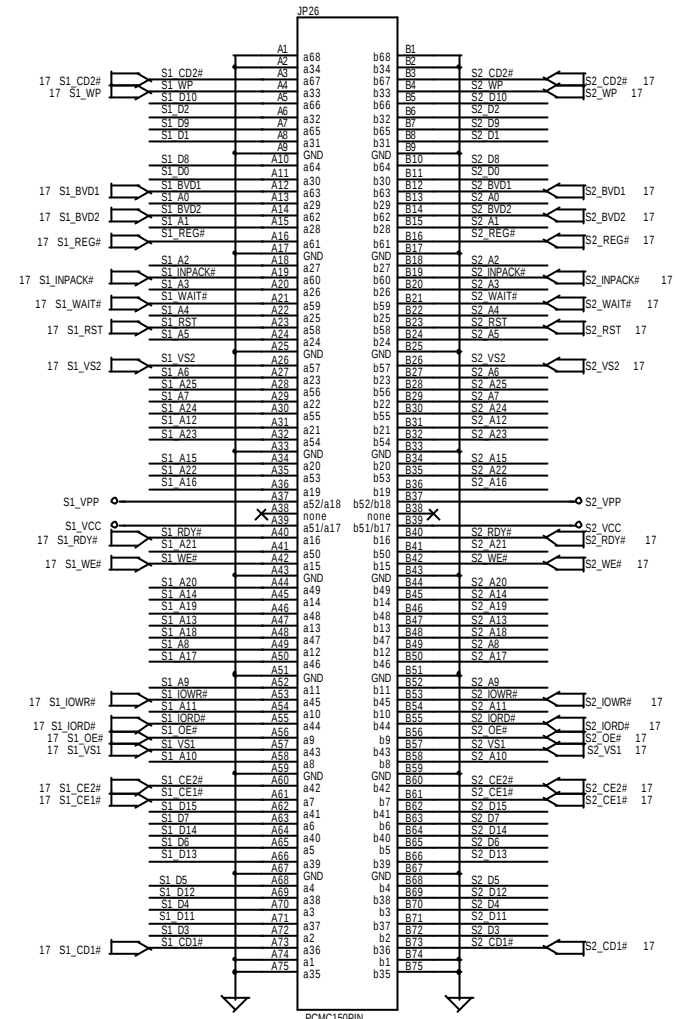
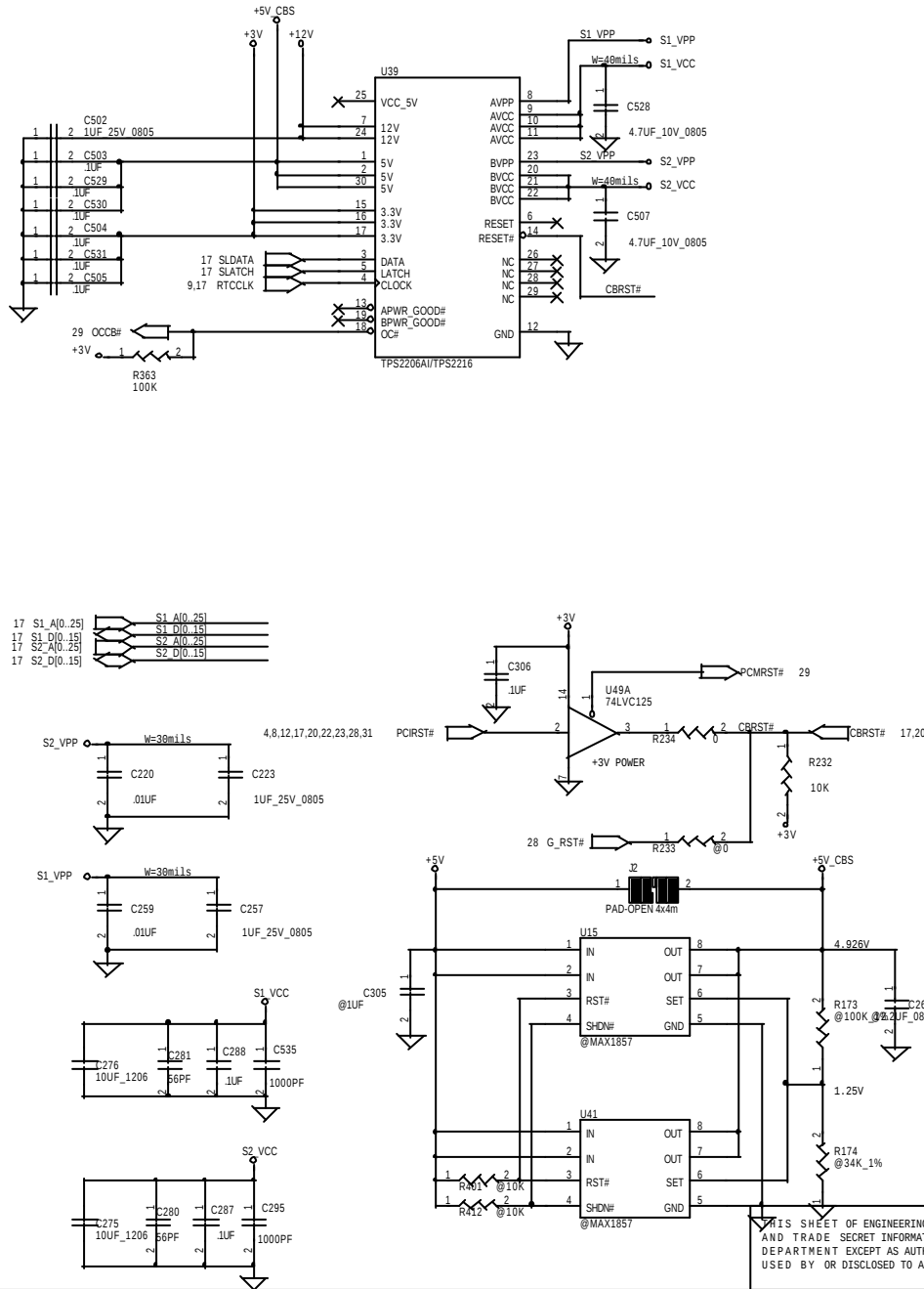
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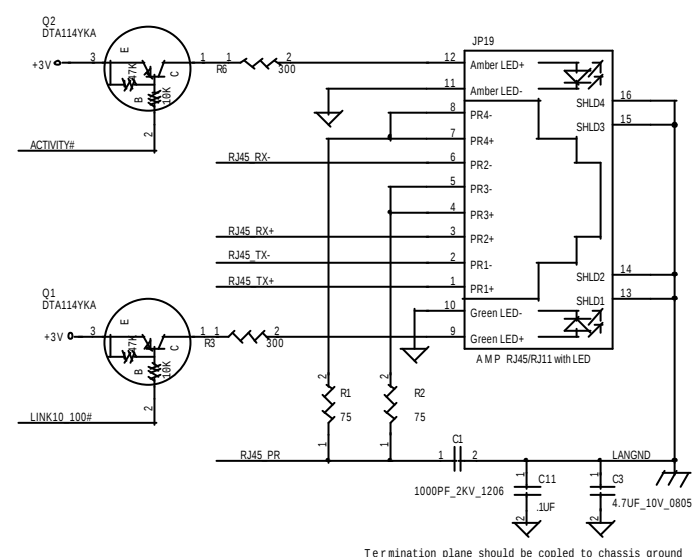
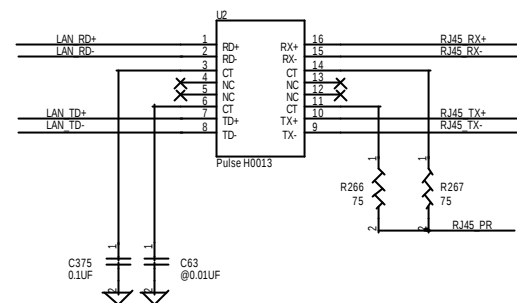
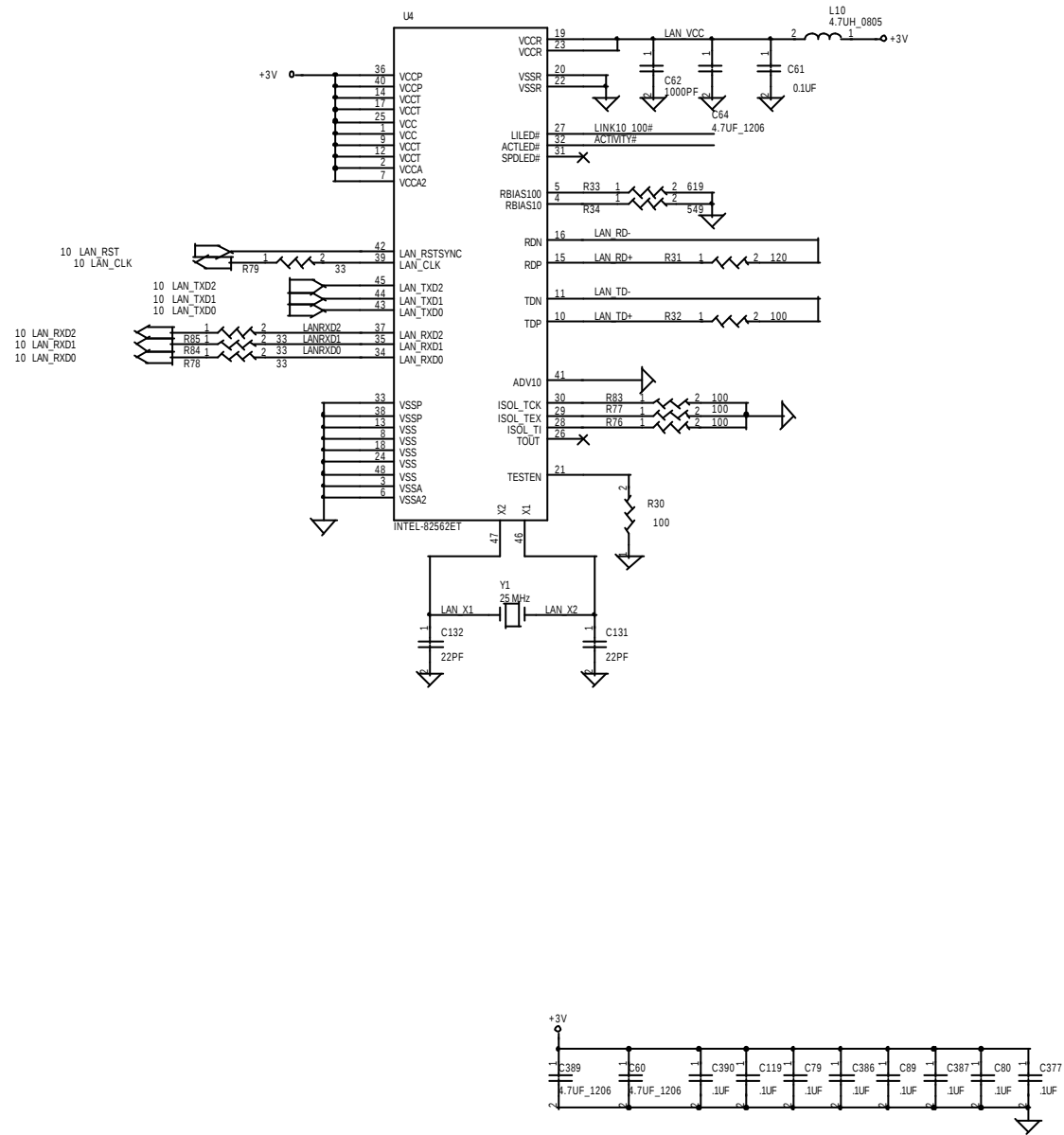
PCMCIA POWER CTRL.

CARDBUS SOCKET



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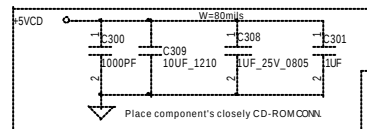
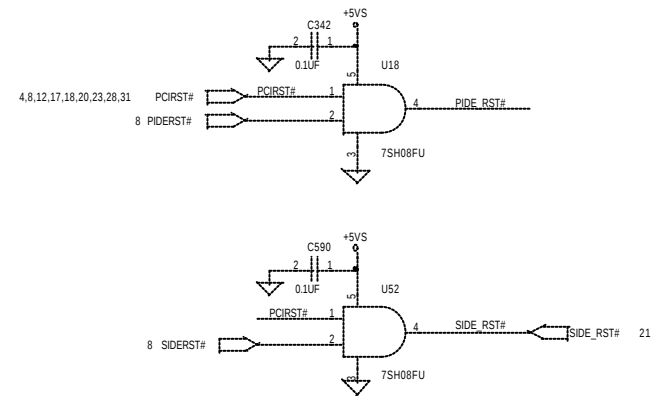
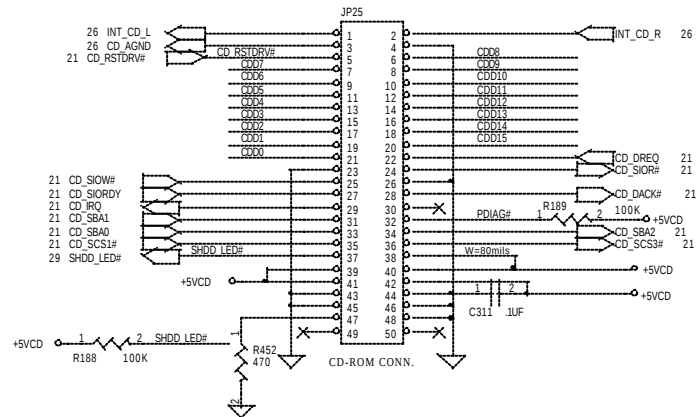
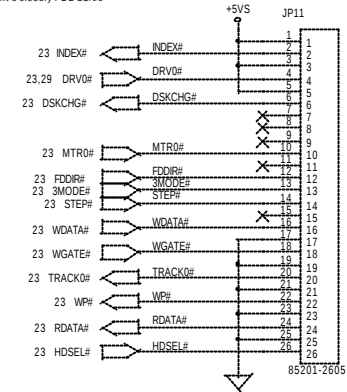
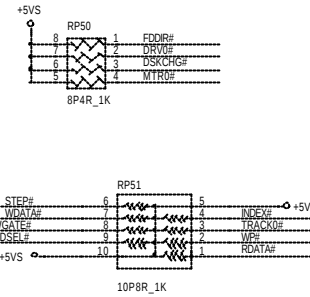
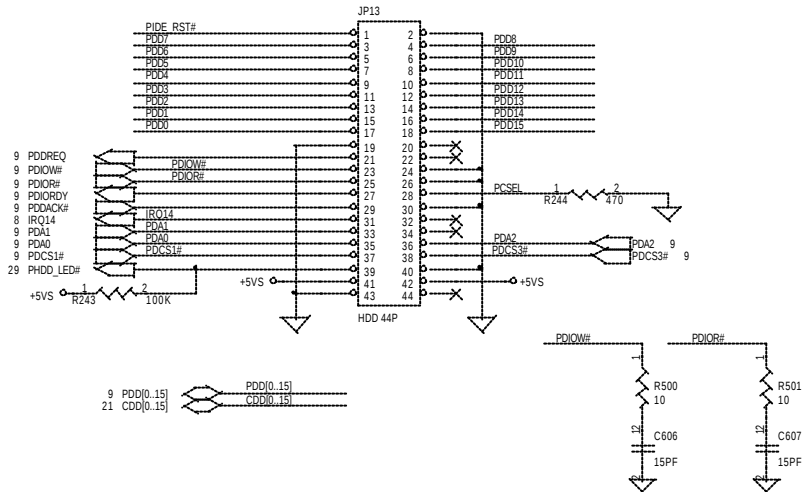
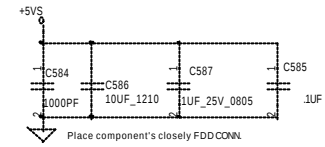
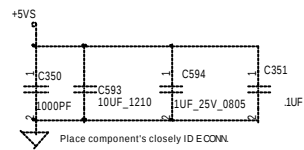
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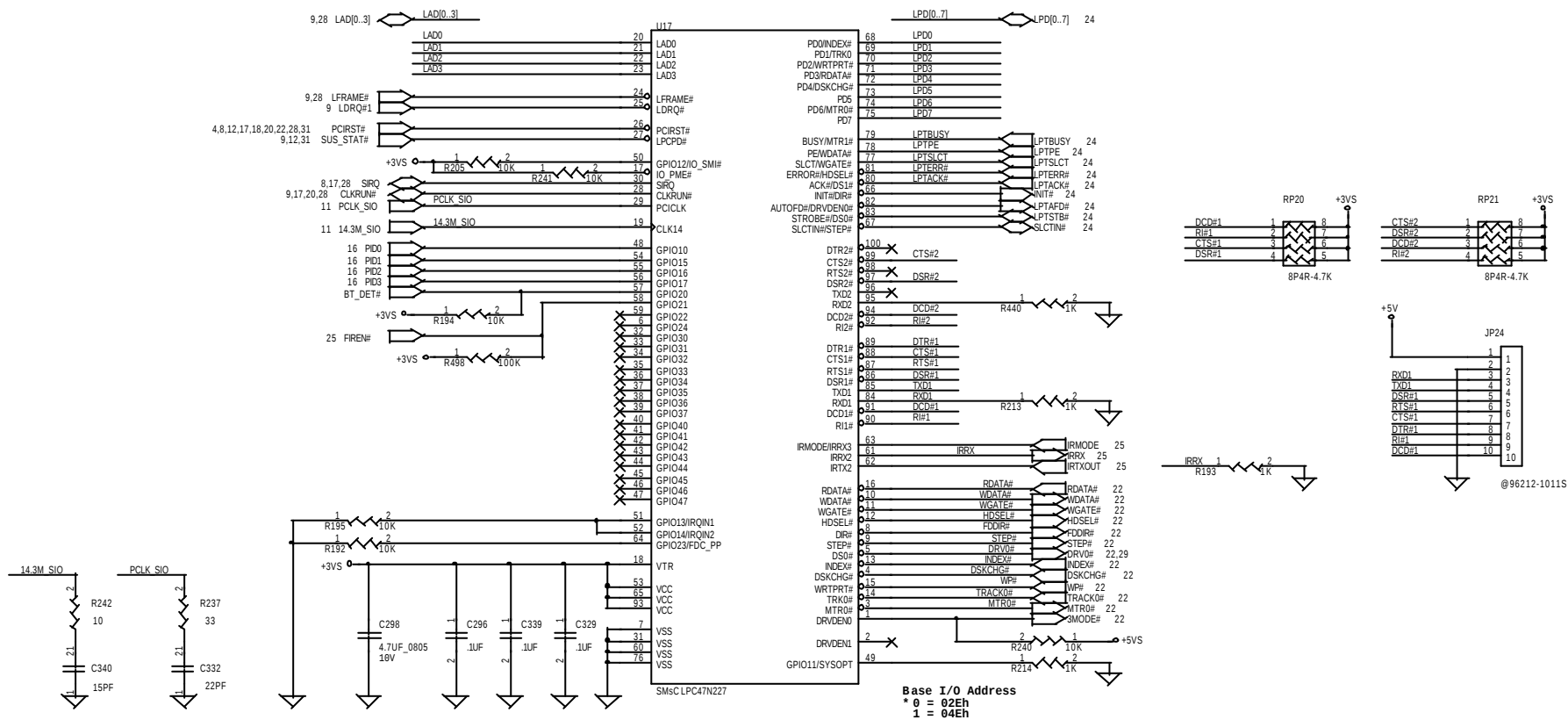
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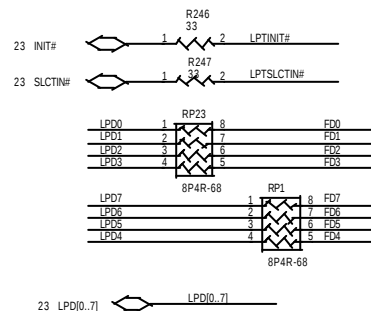
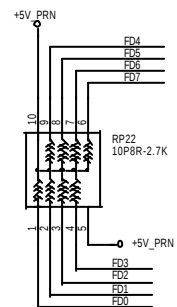
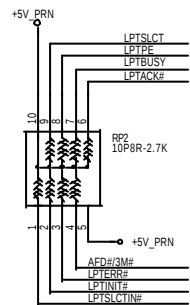
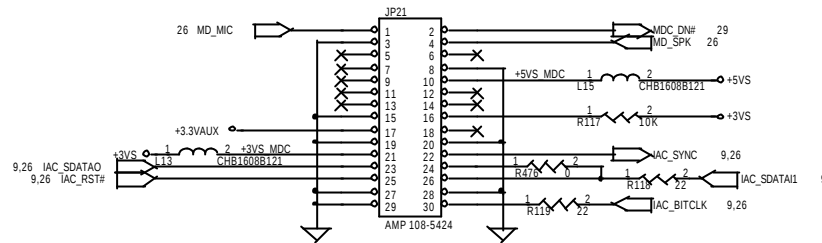
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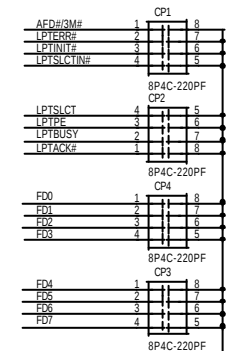
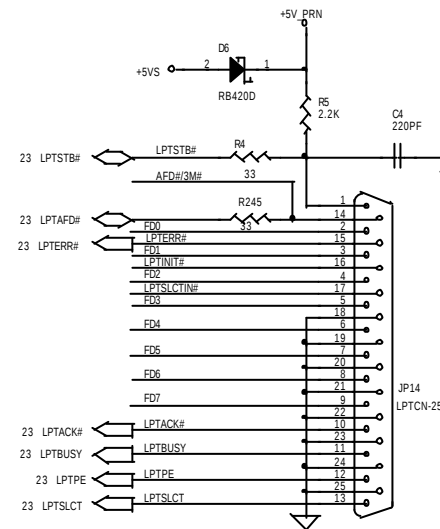
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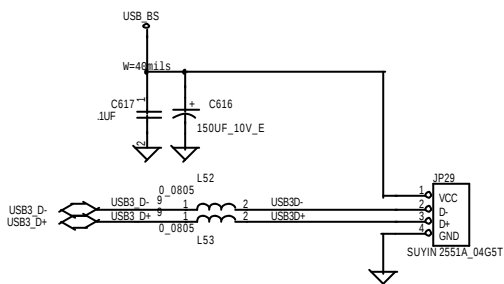
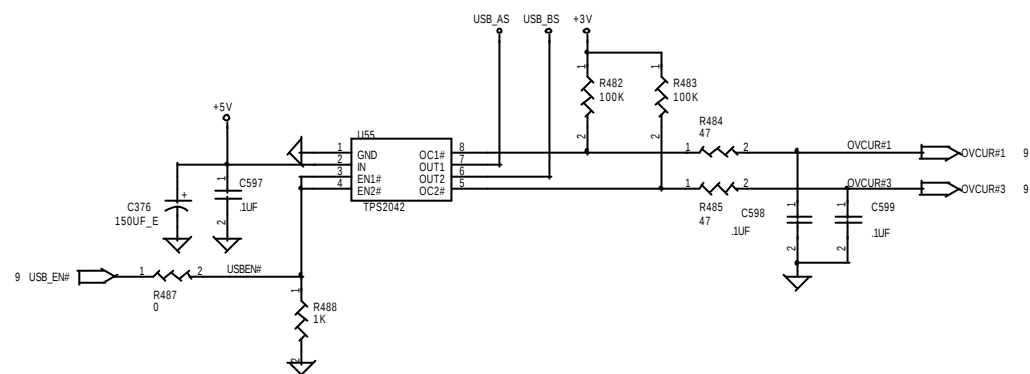
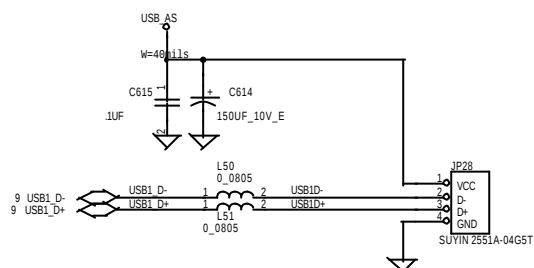
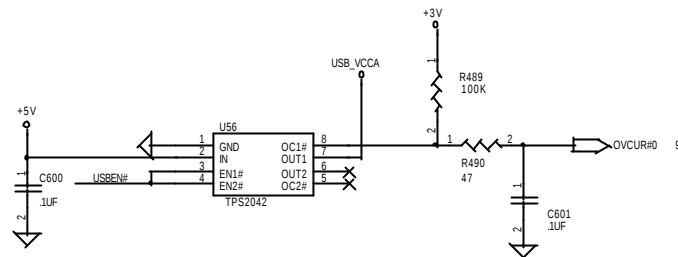
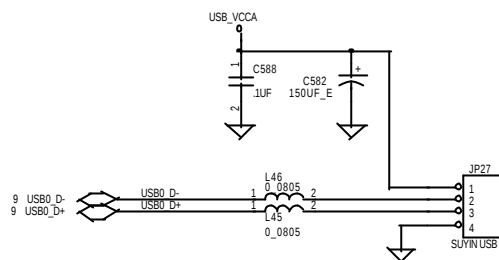
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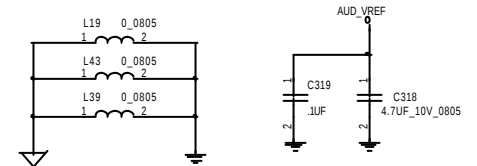
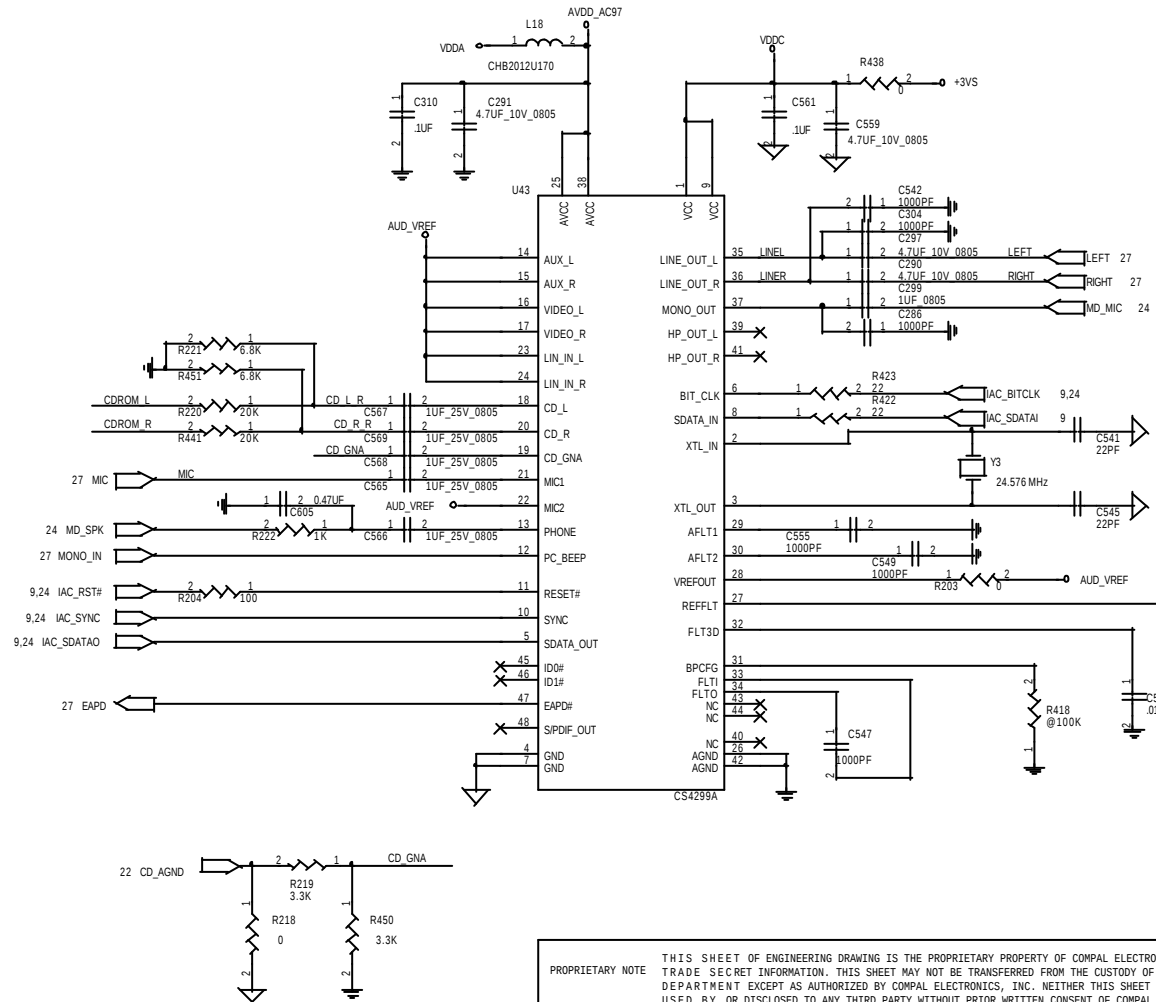
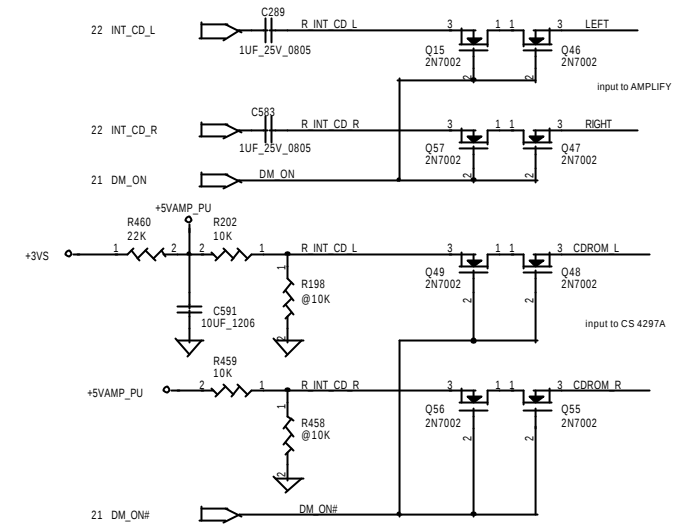
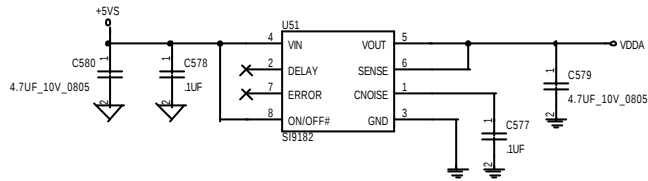


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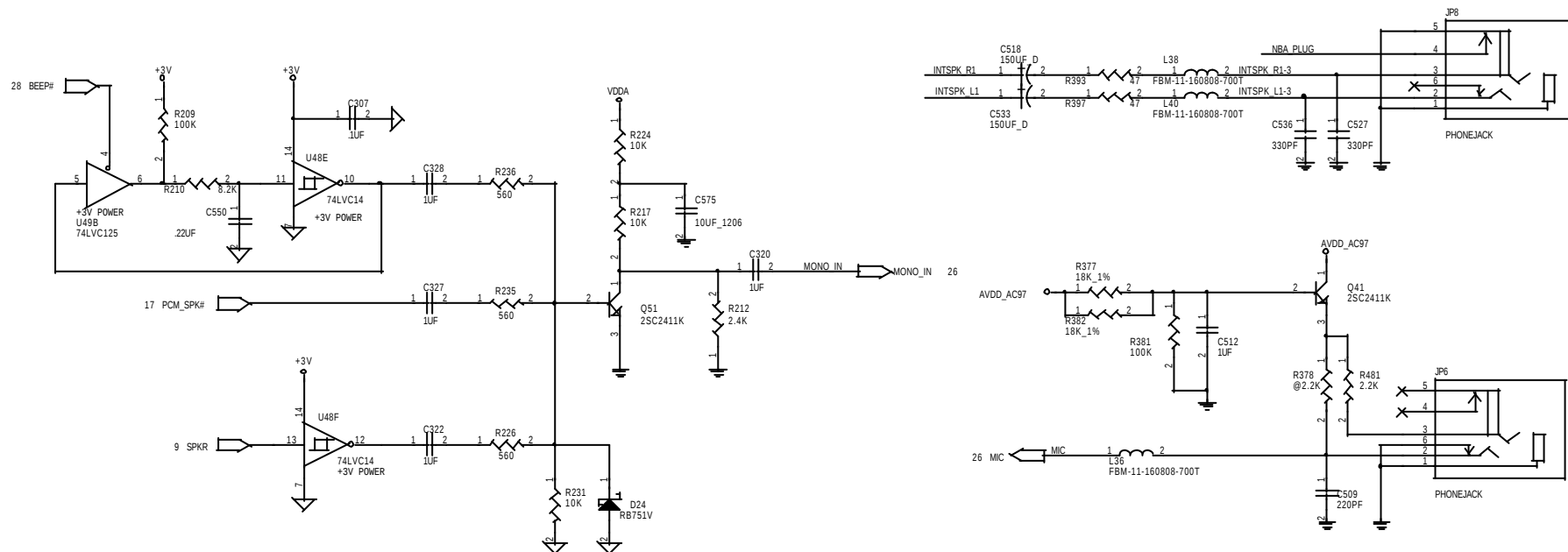
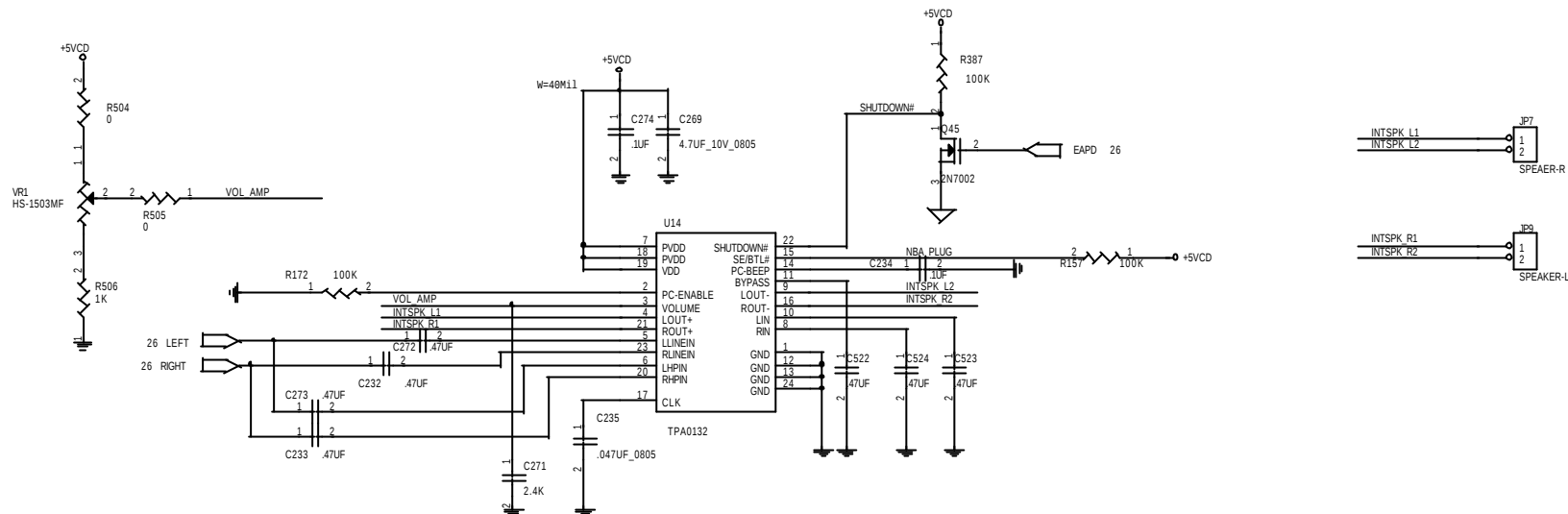
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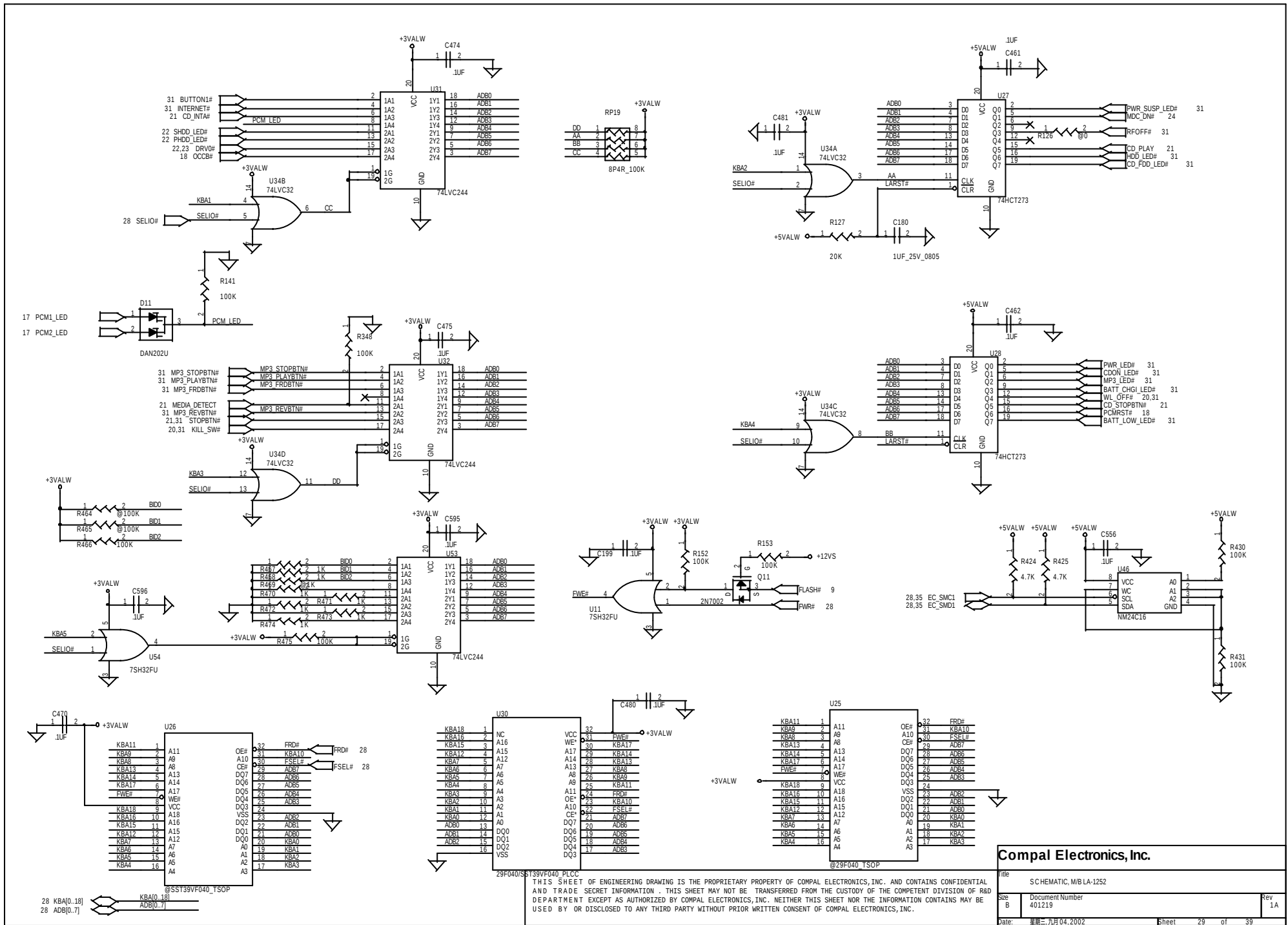
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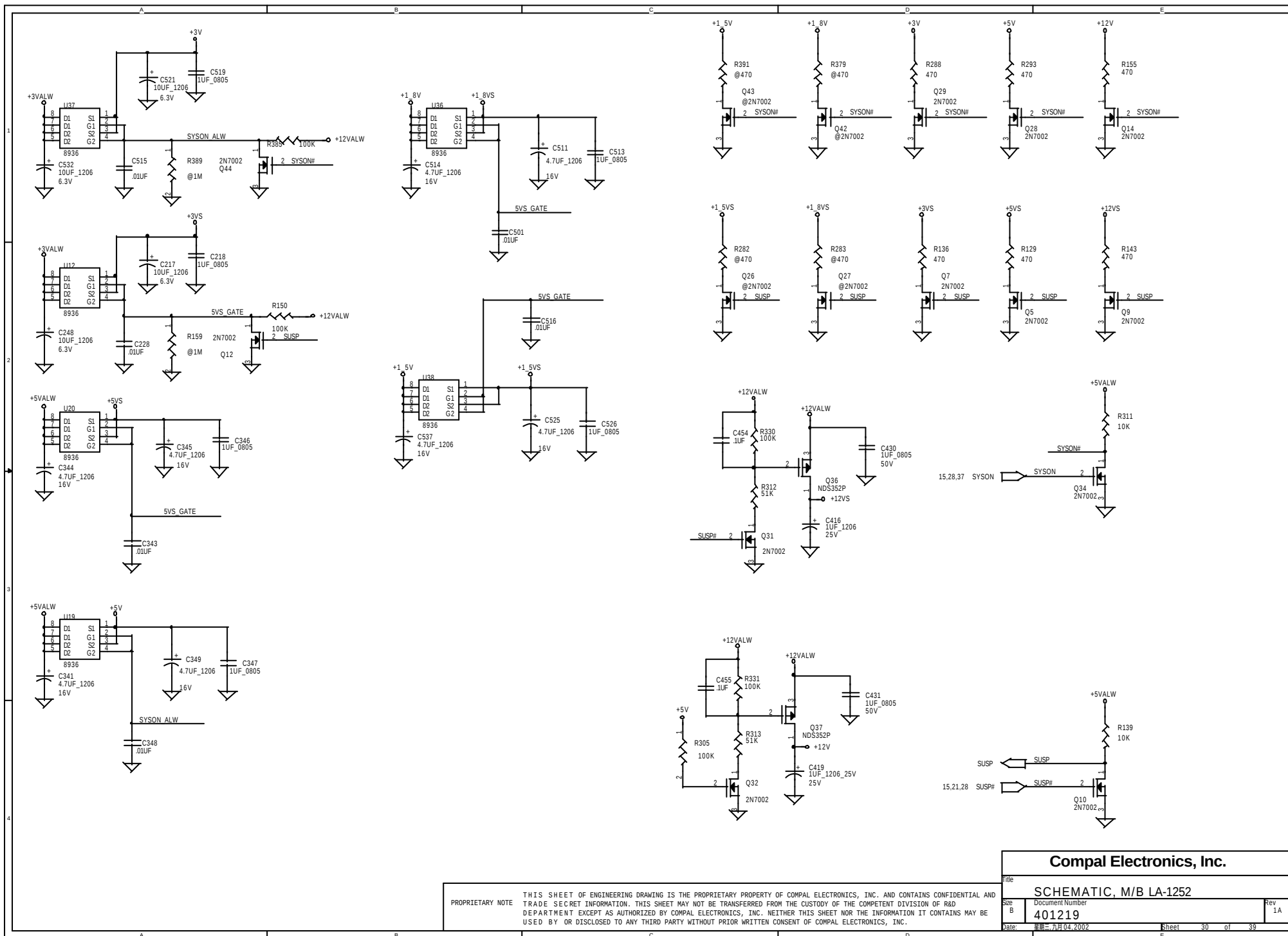
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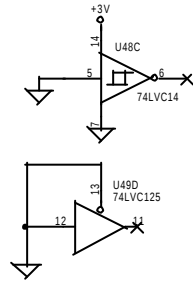
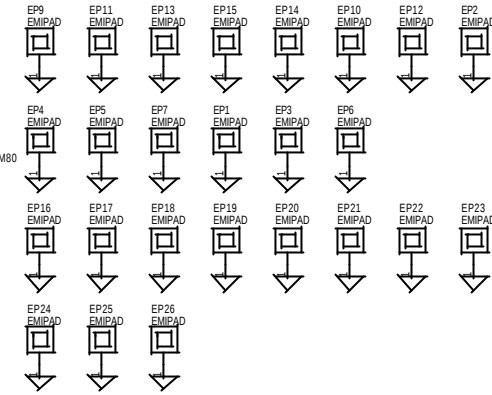
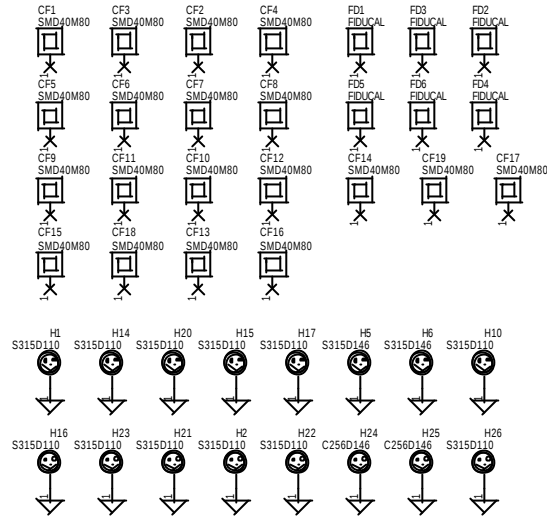
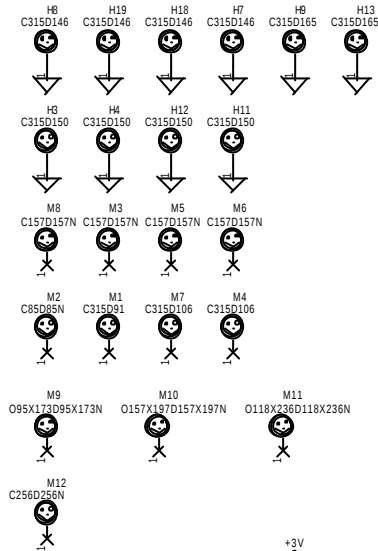
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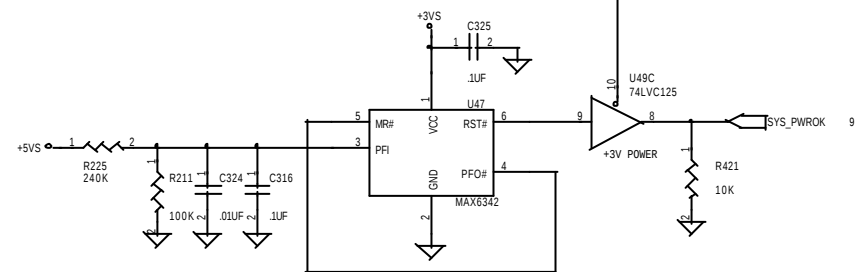
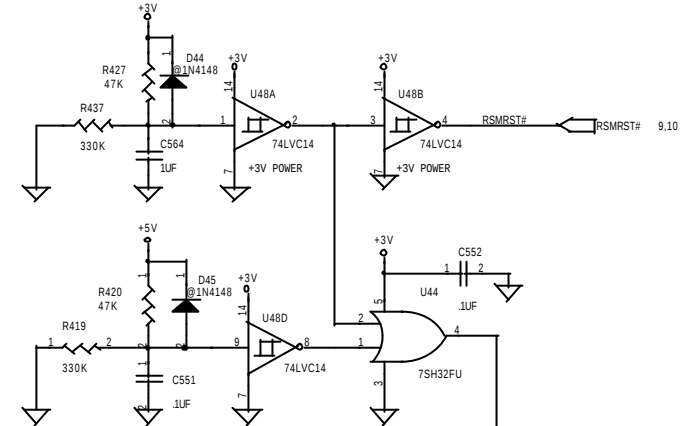
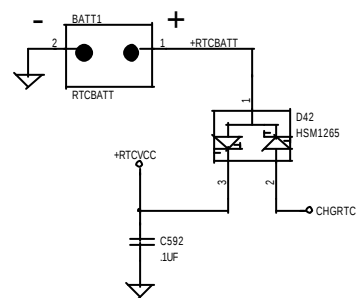
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RTC BATT



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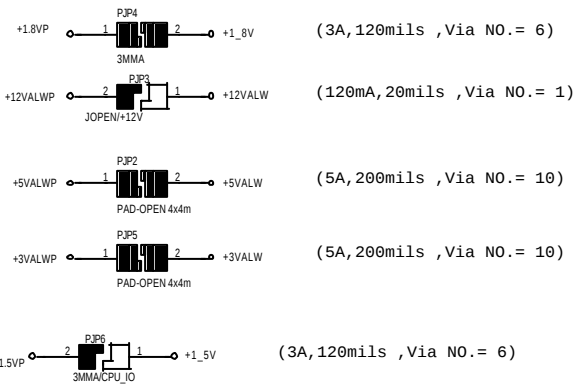
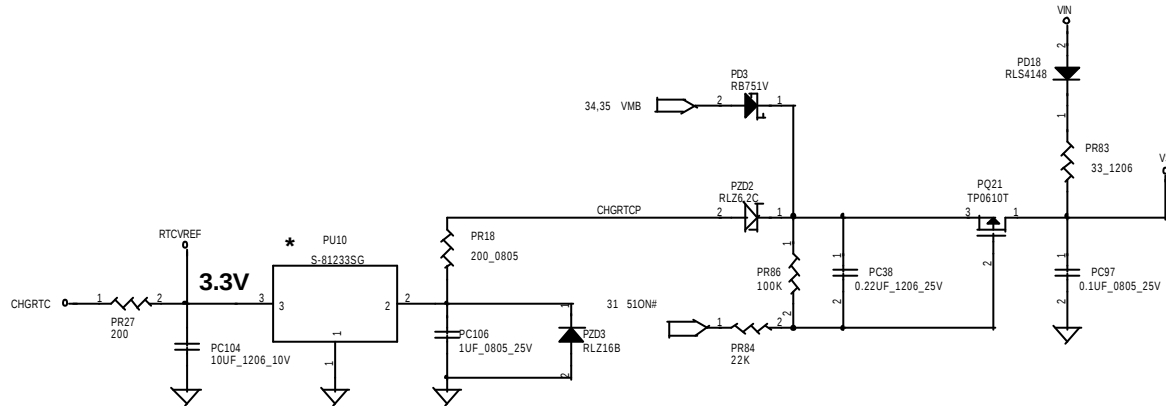
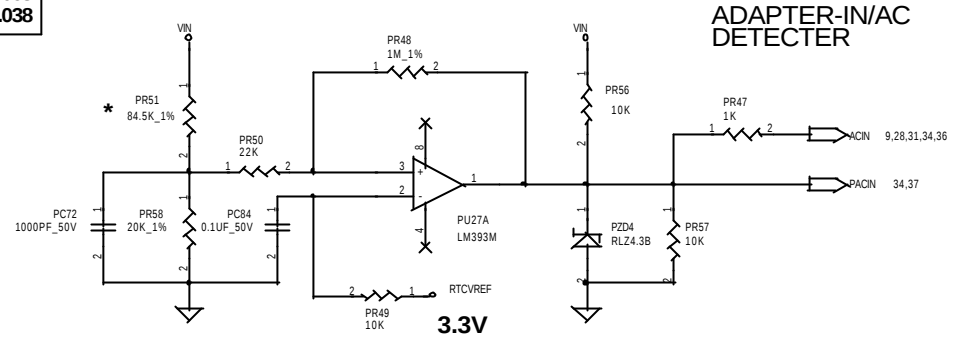
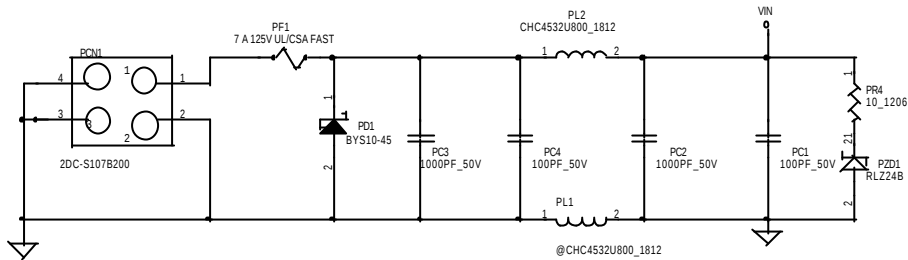
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Vin Detector

High 18.764 17.901 17.063
Low 17.745 16.903 16.038

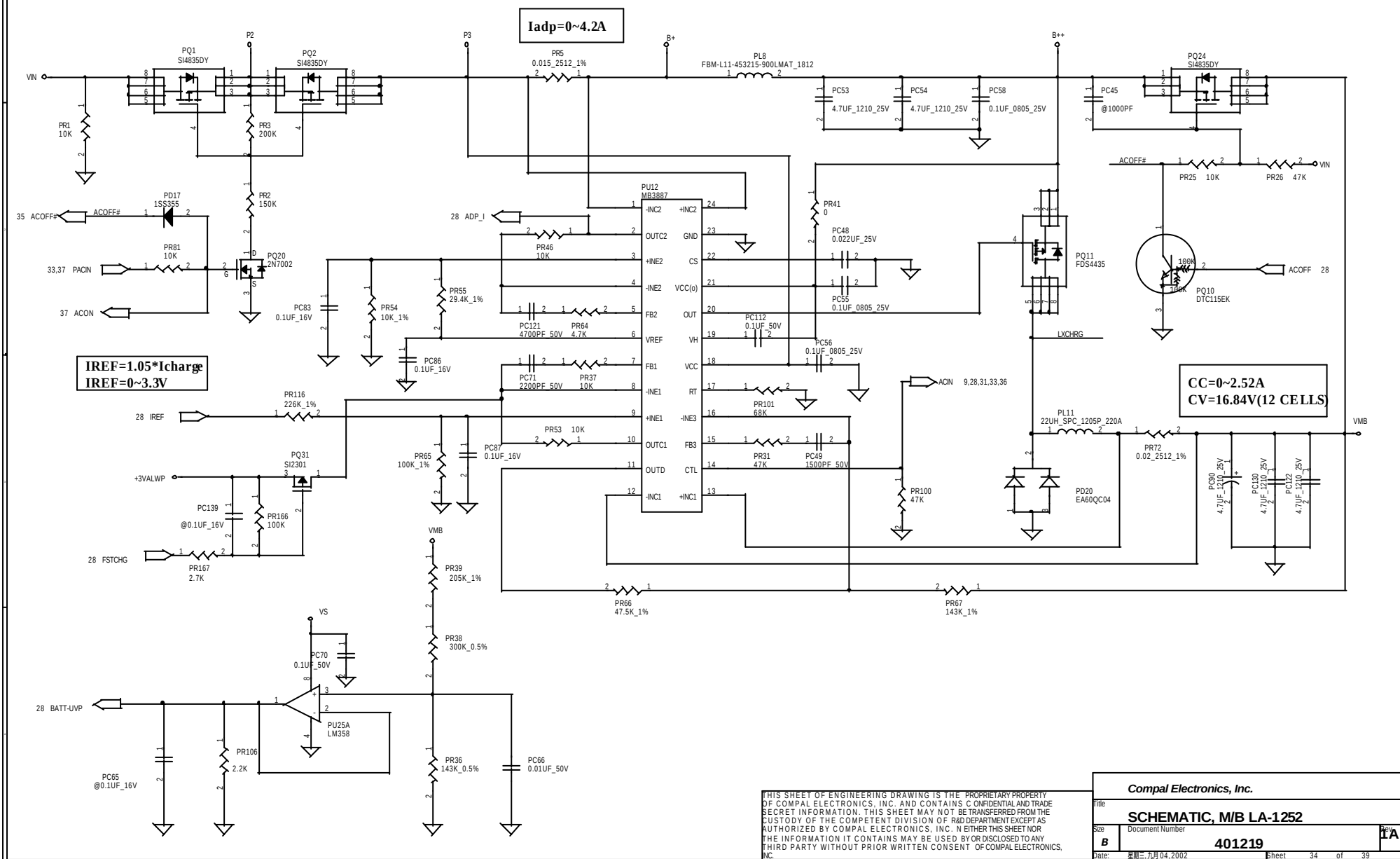


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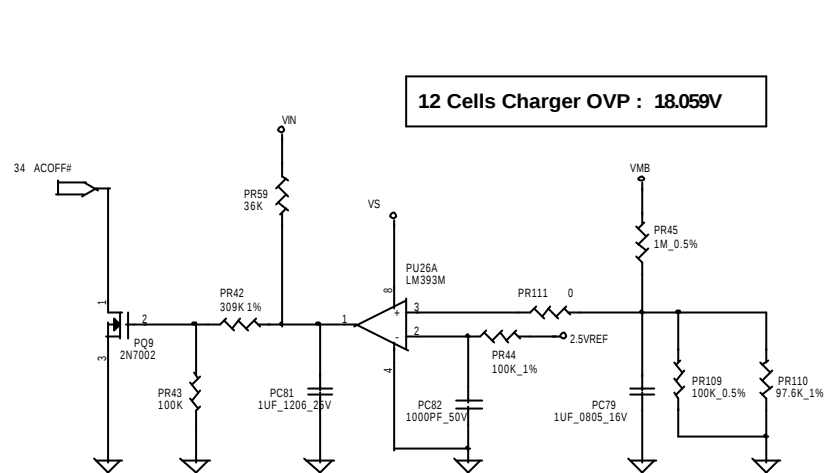
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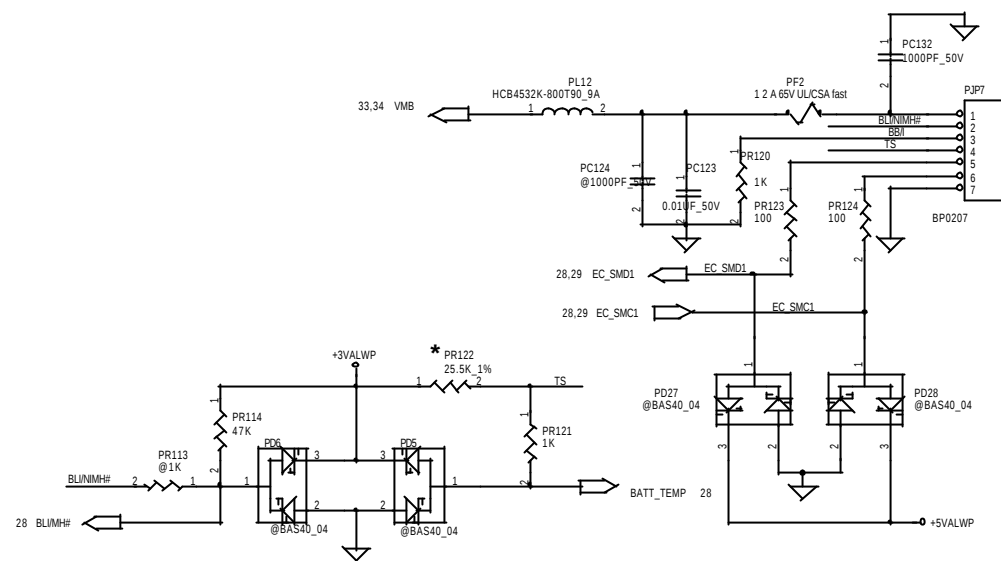
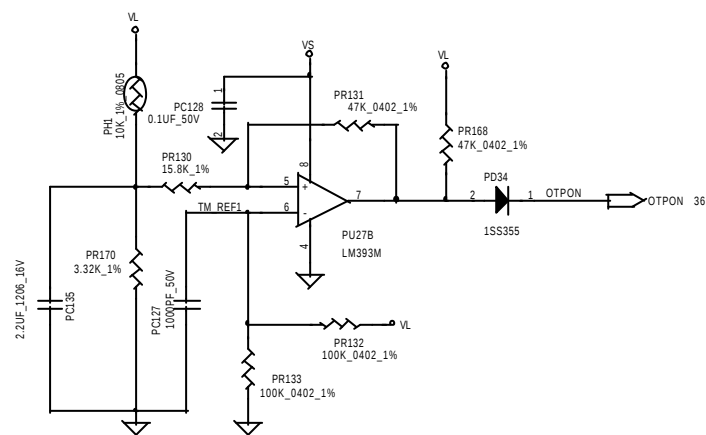
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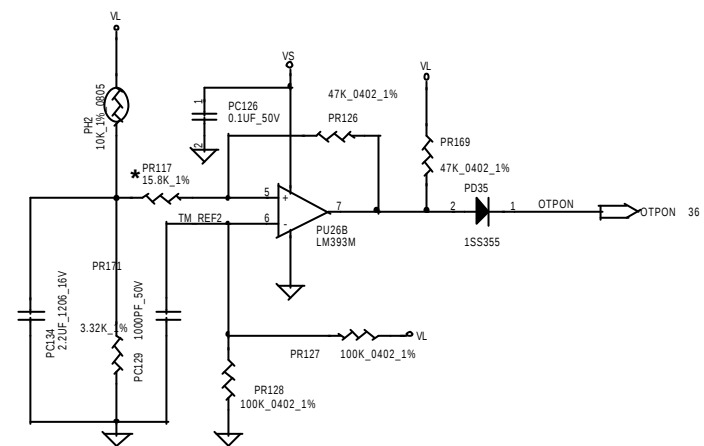
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PH1 under CPU bottom side :
CPU thermal protection at 82 degree C
Recovery at 50 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 82 degree C
Recovery at 50 degree C



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+3.3V/+5V/+12V

+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

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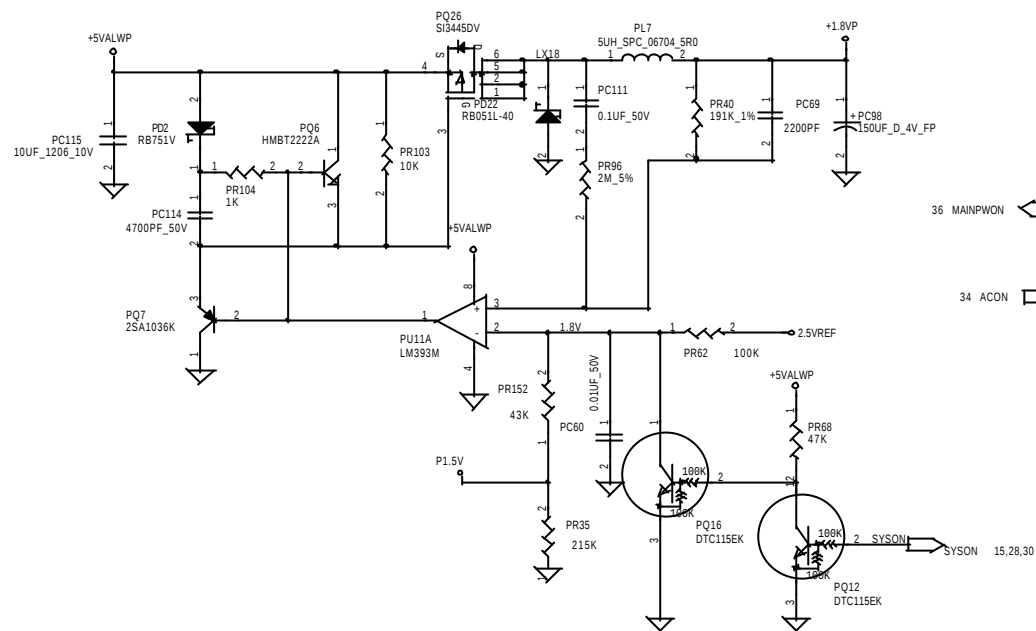
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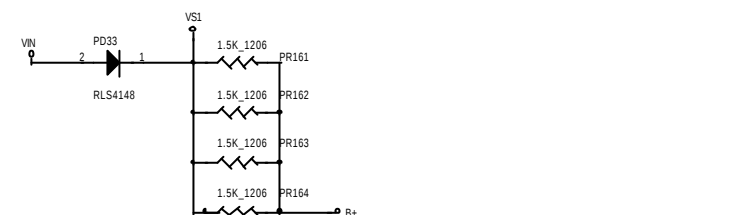
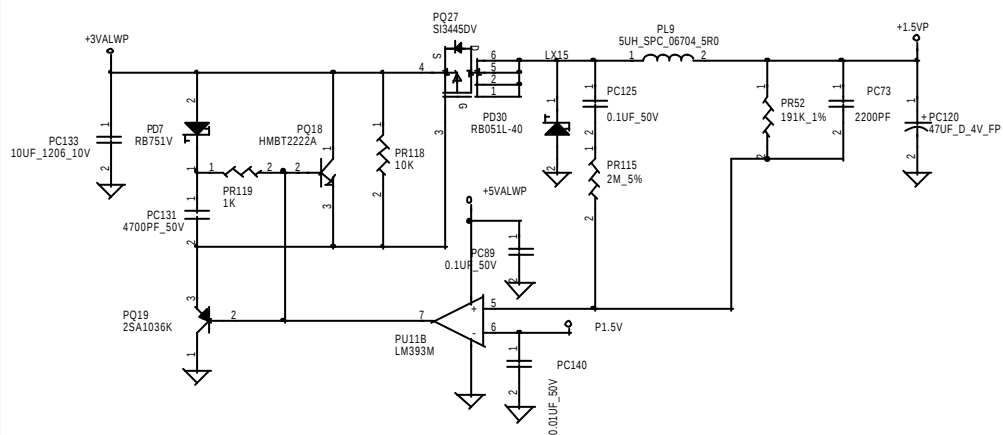
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1.8V/1.5V

+1.8VP+-5%



+1.5VP+-5%



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ACR10 PIR LIST

HW PIR LIST

PWR PIR LIST

ATEST 9/6~

1	+2.5V LEVEL ERROR	Remove R111 100ohm Change R108 from 100 to 0 ohm	P15
2	SDRAM BANK select error	Change CLK_SDRAM3 from U22.F3 to U22.E3 Change CLK_SDRAM5 from U22.H5 to U22.G5 Change RRAS#3 from U22.H7 to U22.F7 Change RRAS#5 from U22.G6 to U22.H6	P5
3	Add CPU VCCVID pin	Add R492 connect to U23.AF3	P3
4	TV OUT output error	Change CRMA from U8.AF15 to U8.AF16 Change LUMA from U8.AF16 to U8.AF15	P12
5	Add MK1787 output terminate	Add R494 22 ohm	P12
6	Add low pass filter for MK1787 power pin	Add L47	P12
7	Change VGA option resistor to jumper	Change R284 to J3 Change R286 to J4 Change R295 to J5 Change R296 to J6	P15
8	Reserve +2.5V option control	Add R495 for SYSON control Add R496 for SUSP control	P15
9	Change LCD connector type	Change JP1	P16
10	Add TI TPS2042 for USB protect circuit	Add U56(TPS2042)	P25

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