

Compal Confidential

HCW50 Schematics Document

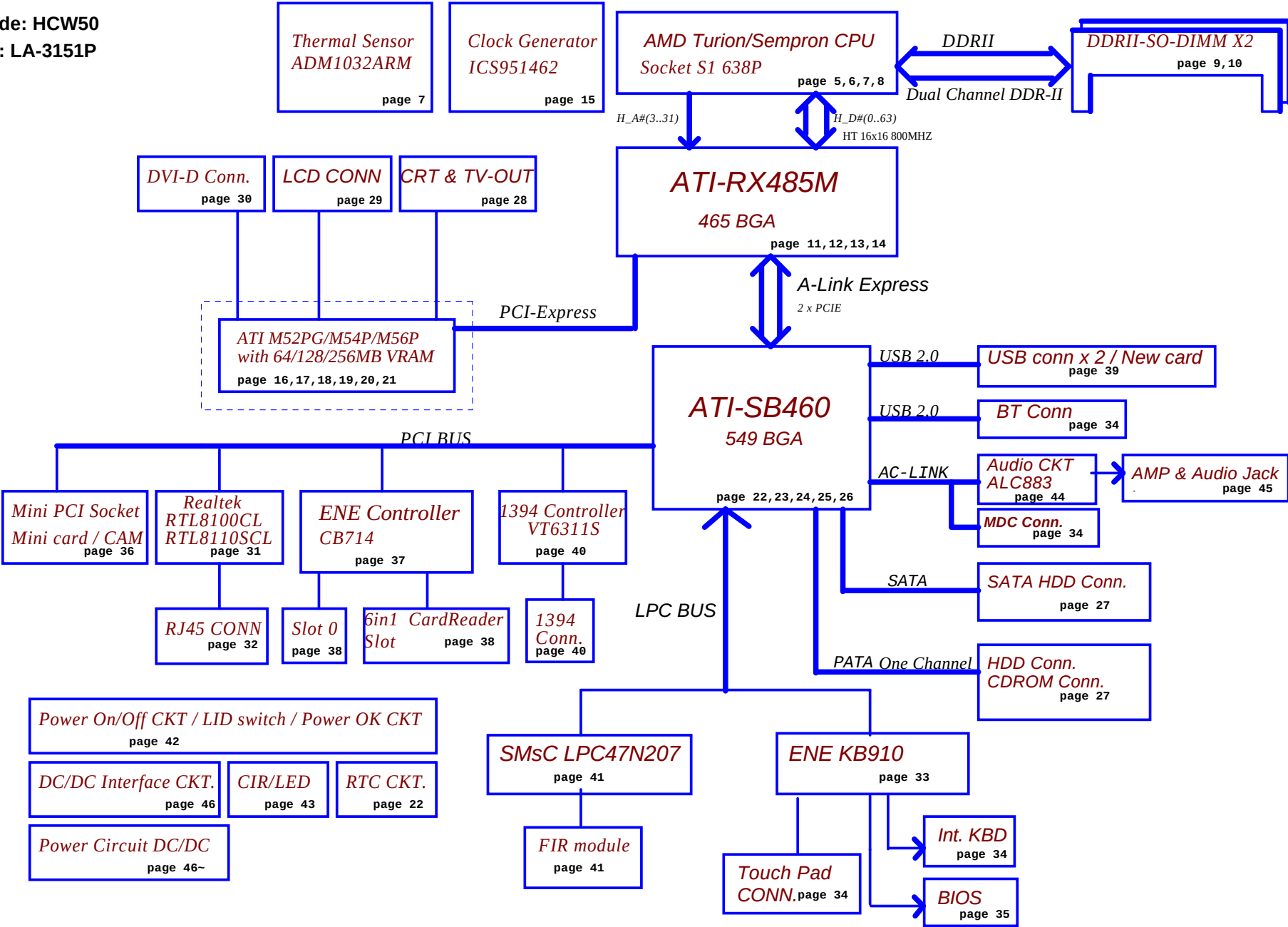
AMD/Sempron/ATI RX485/SB460 W/s M52/54/56P

2006 / 02 / 28 Rev:0.3 (For PVT)

Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		SCHEMATIC, M/B LA-3151P	
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Project Code: HCW50
File Name : LA-3151P



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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDRII terminator	ON	ON	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON*
+1.2VS	1.2V switched power rail for PCIE	ON	OFF	OFF
+0.9VS	0.9V switched power rail for VRAM terminator	ON	OFF	OFF
+1.8VALW	1.8V switched power rail	ON	ON	ON*
+VDD_CORE	1.0~1.2V switched power rail for VGA	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

SB460 SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL				SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON				
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW				
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF				
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF				
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

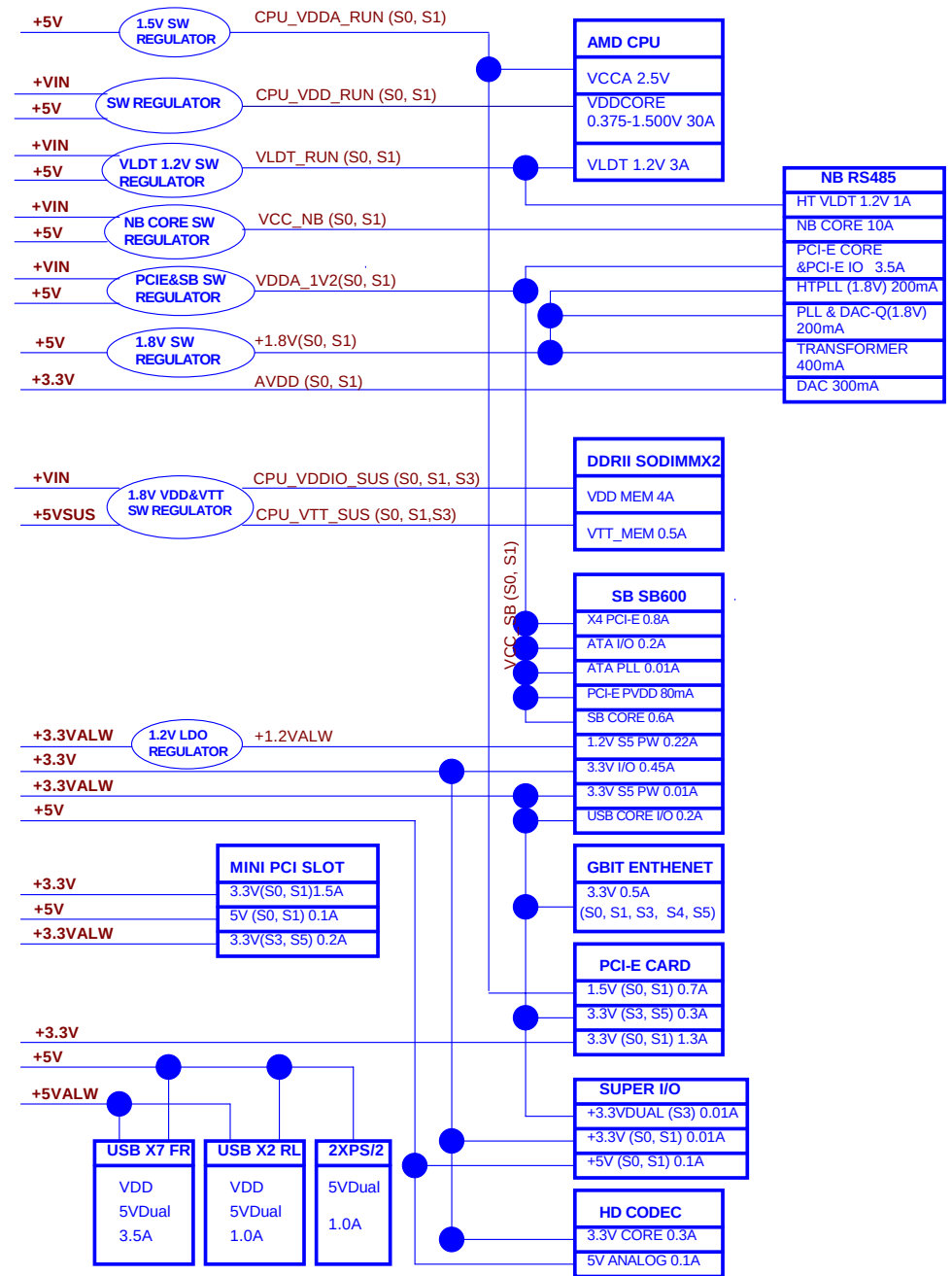
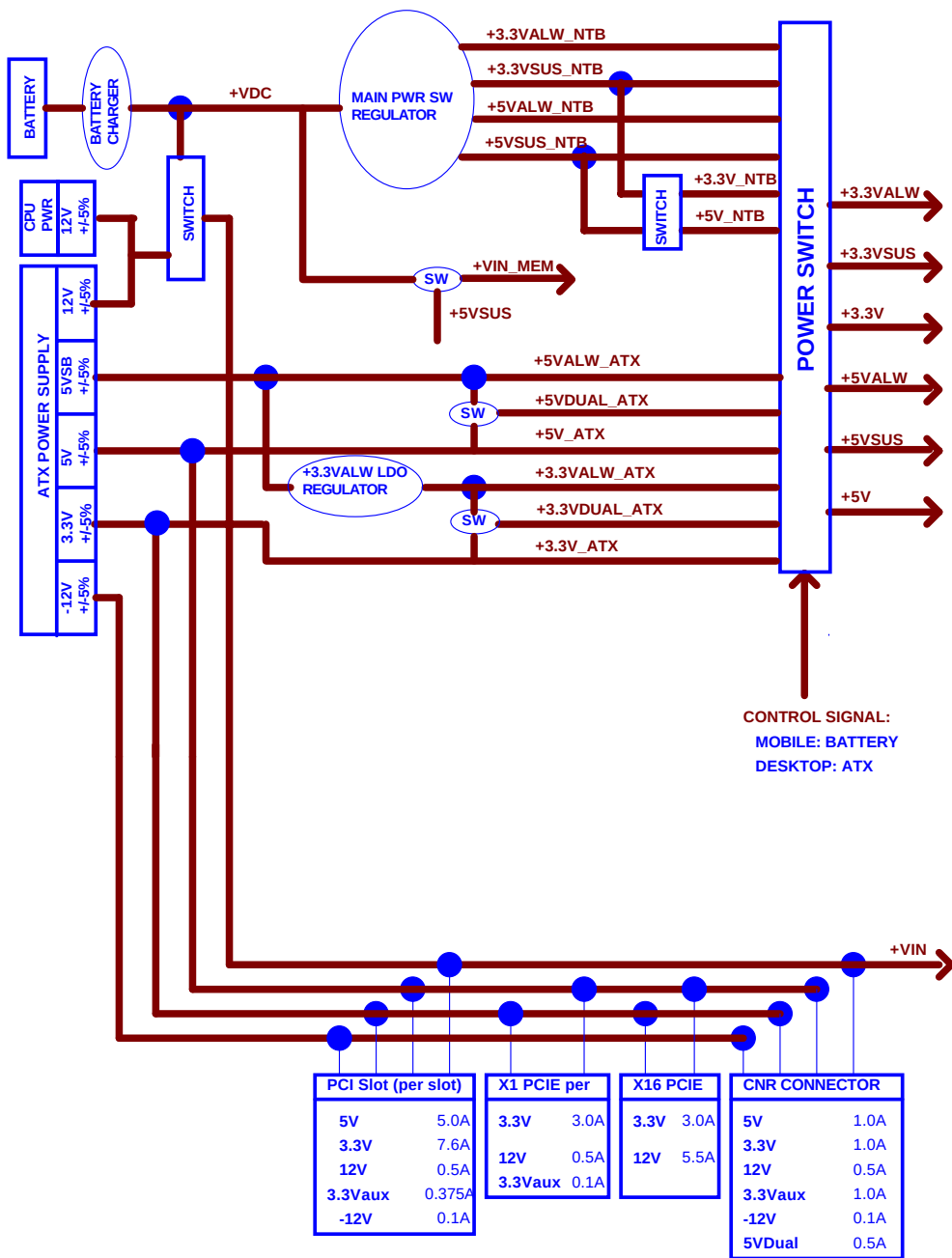
SKU ID Table

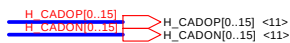
SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
VGA	
UMA	
UMA's DVI	
LAN(10/100)	
LAN(GIGA)	
MINI CARD1	
MINI CARD2	
SATA-to-IDE	
PATA	
GRAPEVINE	
G72MV Only	
G73 Only	
VRAM	
VRAM 64M	
VRAM 128M	
VRAM 256M	
MEDIA/B	
CIR	
FIR	
GENEVA	
LCM	
Sub-woofer	

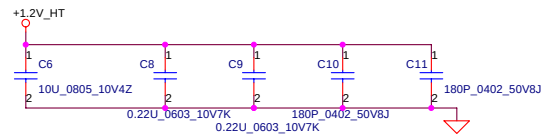
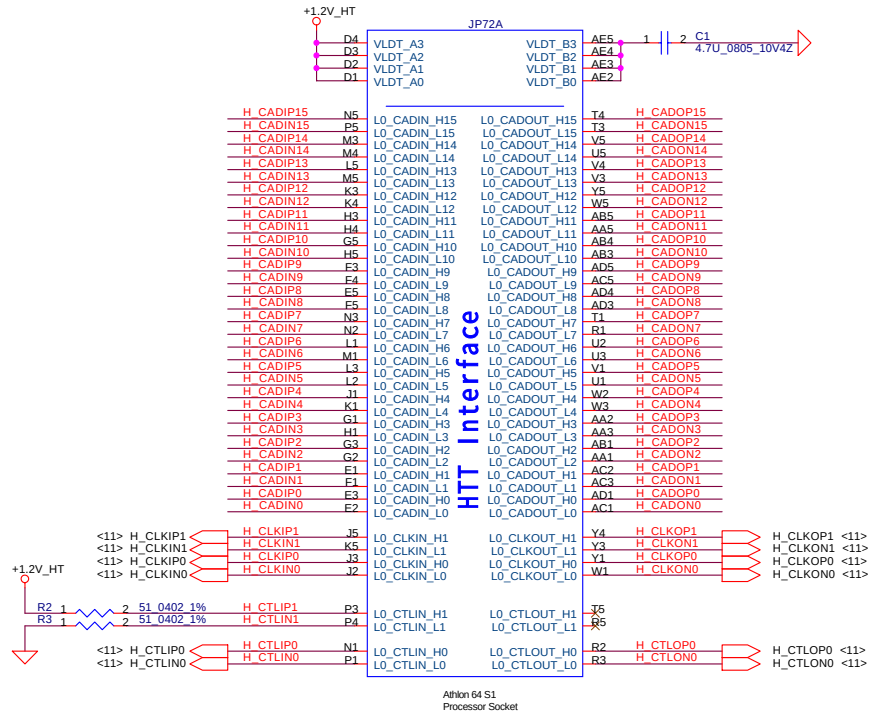
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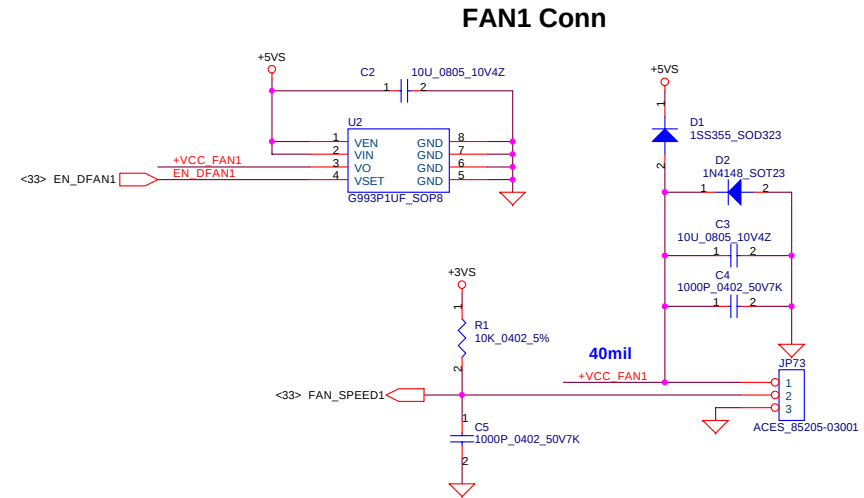
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



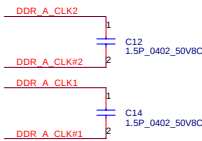
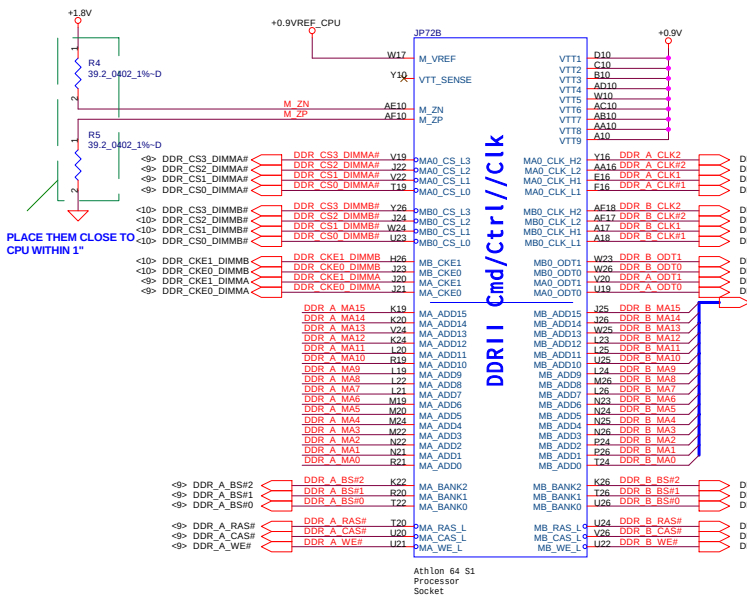
LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY
TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY
TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

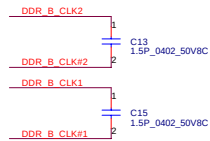


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VDD VTT SUS_CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

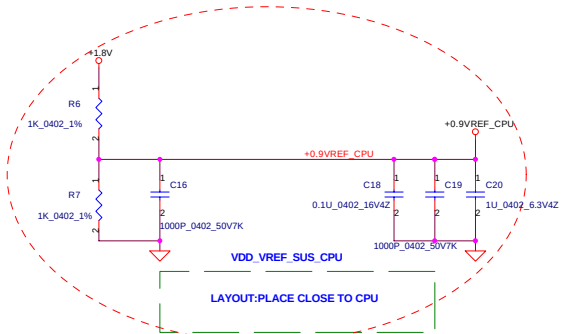


PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

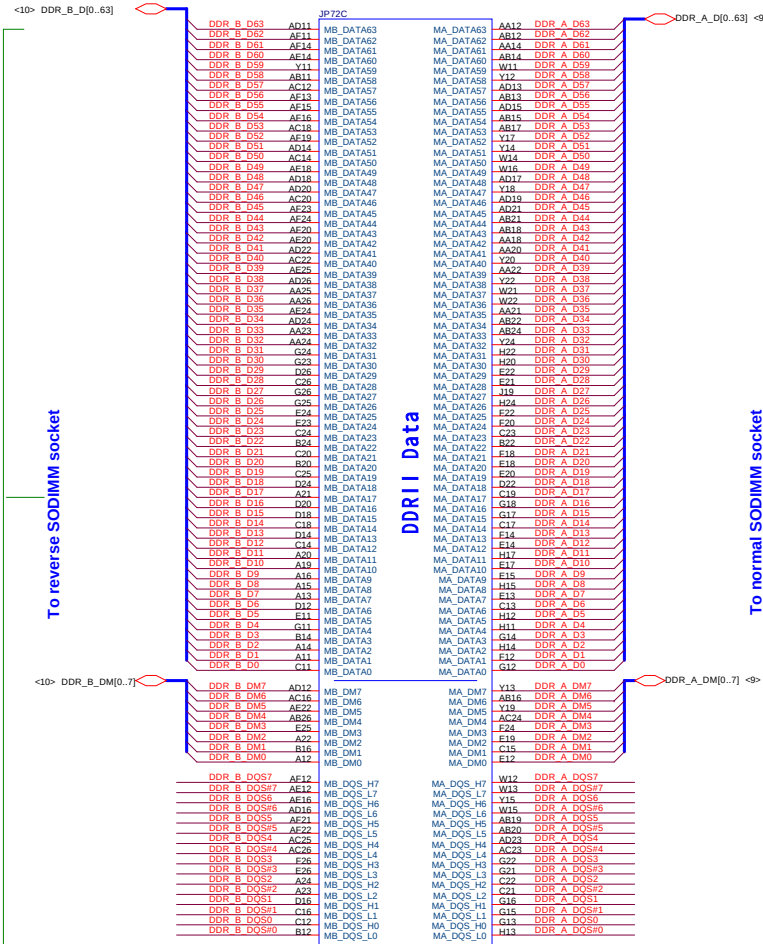


PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

ATI check , Use +0.9V PWR , can delete or not



Processor DDR2 Memory Interface



DDR: DATA
Athlon 64 S1
Processor Socket



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ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX.
50 mils WIDE (USE 2x25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

SB460 ONLY

place them to CPU within 1"

Modify 11/22

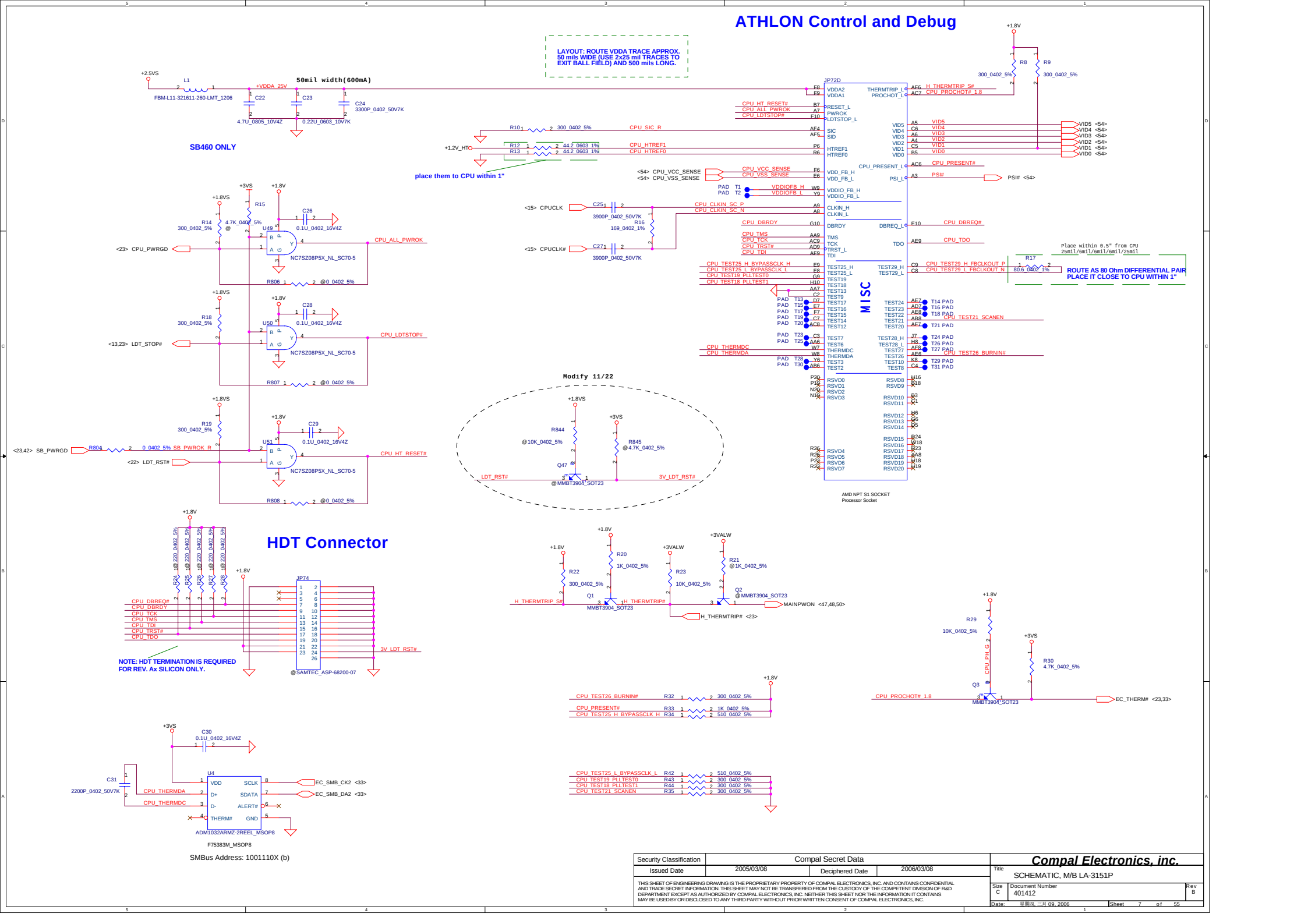
AMD NPT S1 SOCKET
Processor Socket

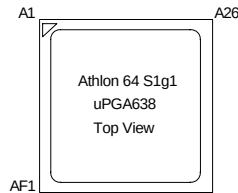
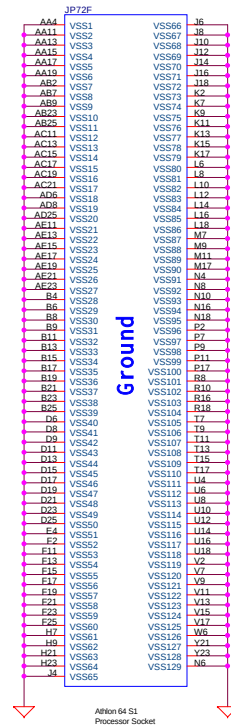
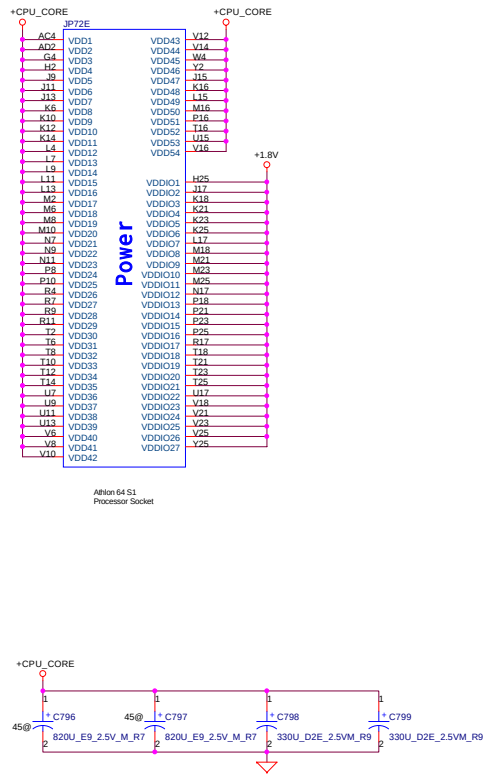
Place within 0.5" from CPU
25mil/6mil/6mil/6mil/25mil
ROUTE AS 80 Ohm DIFFERENTIAL PAIR
PLACE IT CLOSE TO CPU WITHIN 1"

HDT Connector

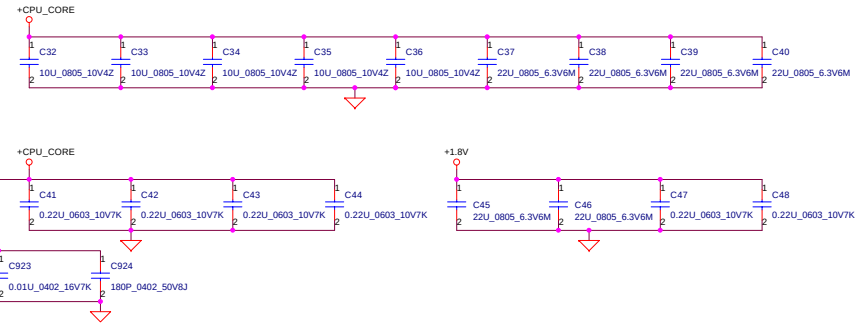
NOTE: HDT TERMINATION IS REQUIRED
FOR REV. Ax SILICON ONLY.

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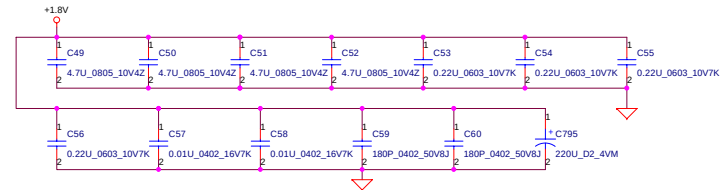




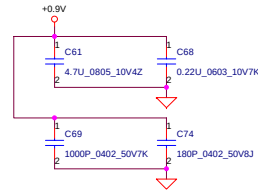
BOTTOMSIDE DECOUPLING



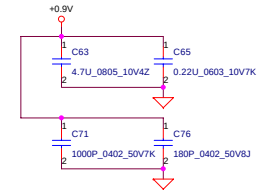
DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE



CPU left-hand side

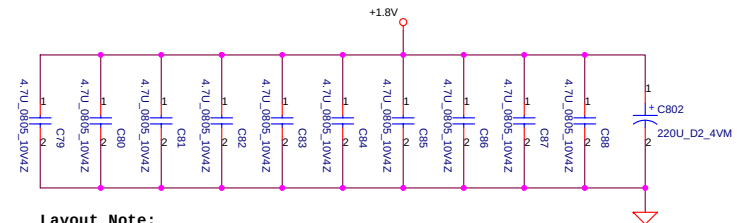
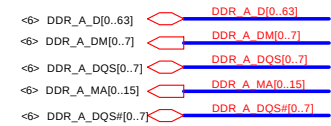
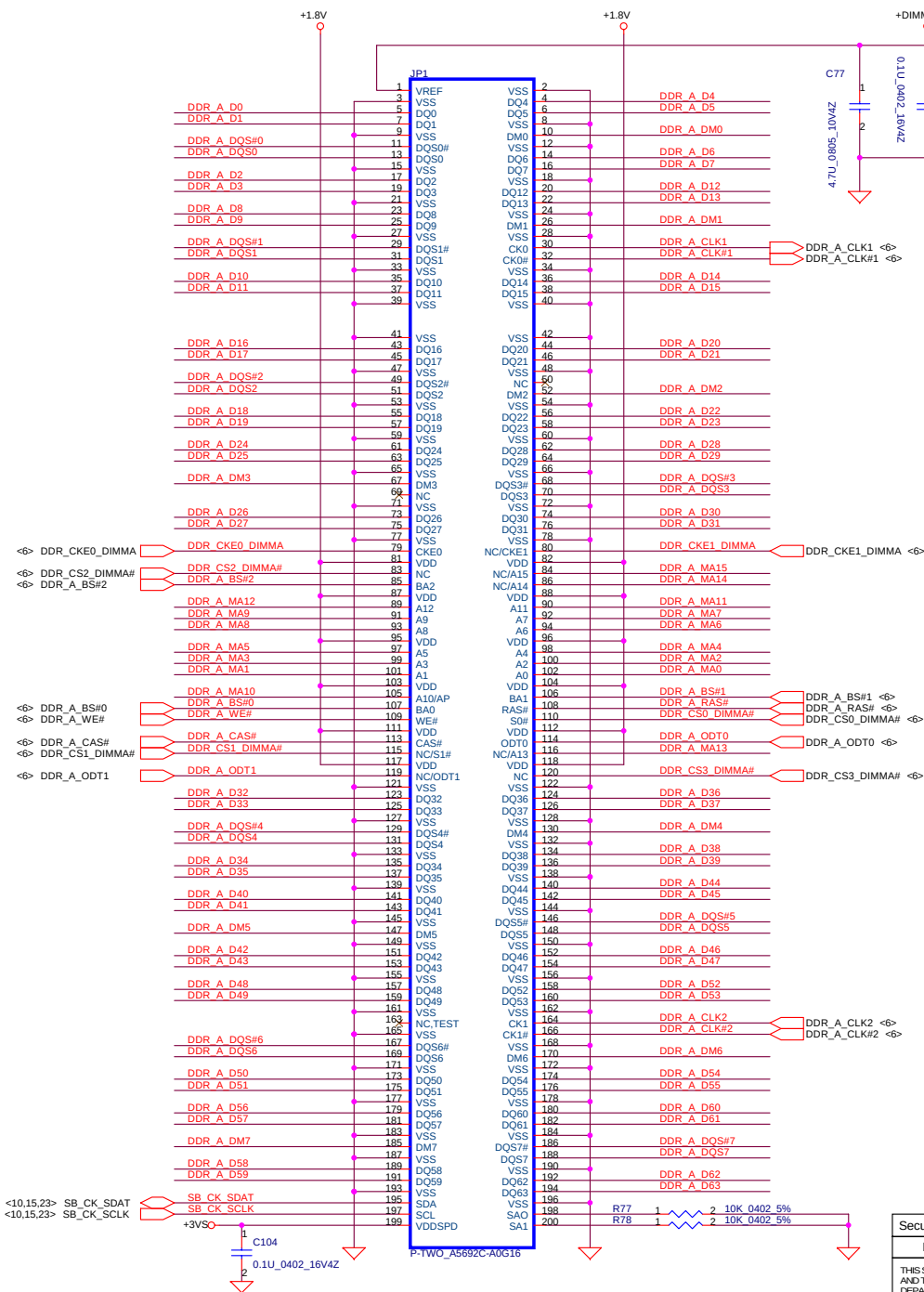


CPU right-hand side

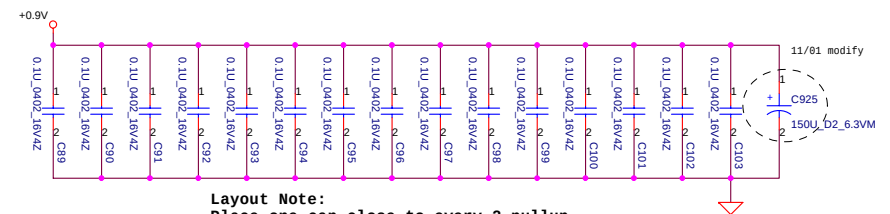


PROCESSOR POWER AND GROUND

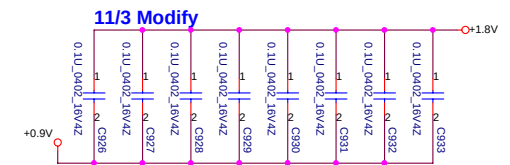
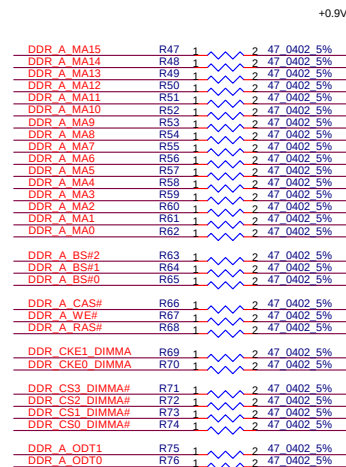
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Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

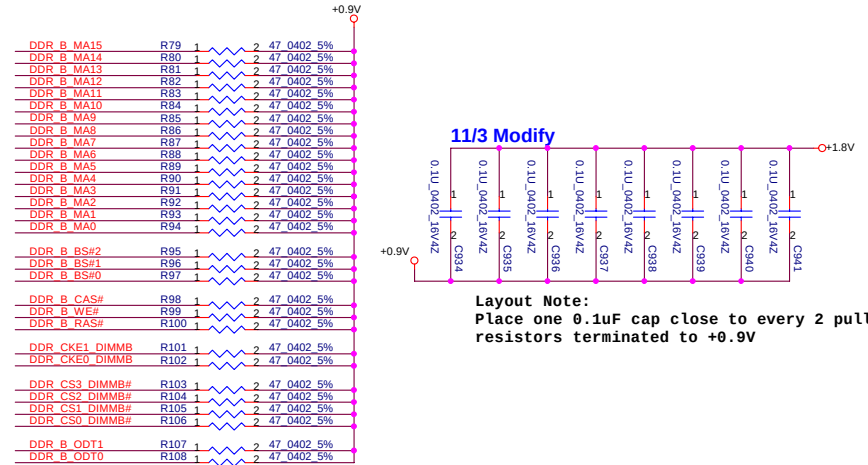
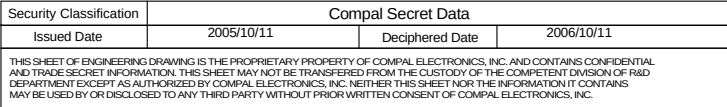


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

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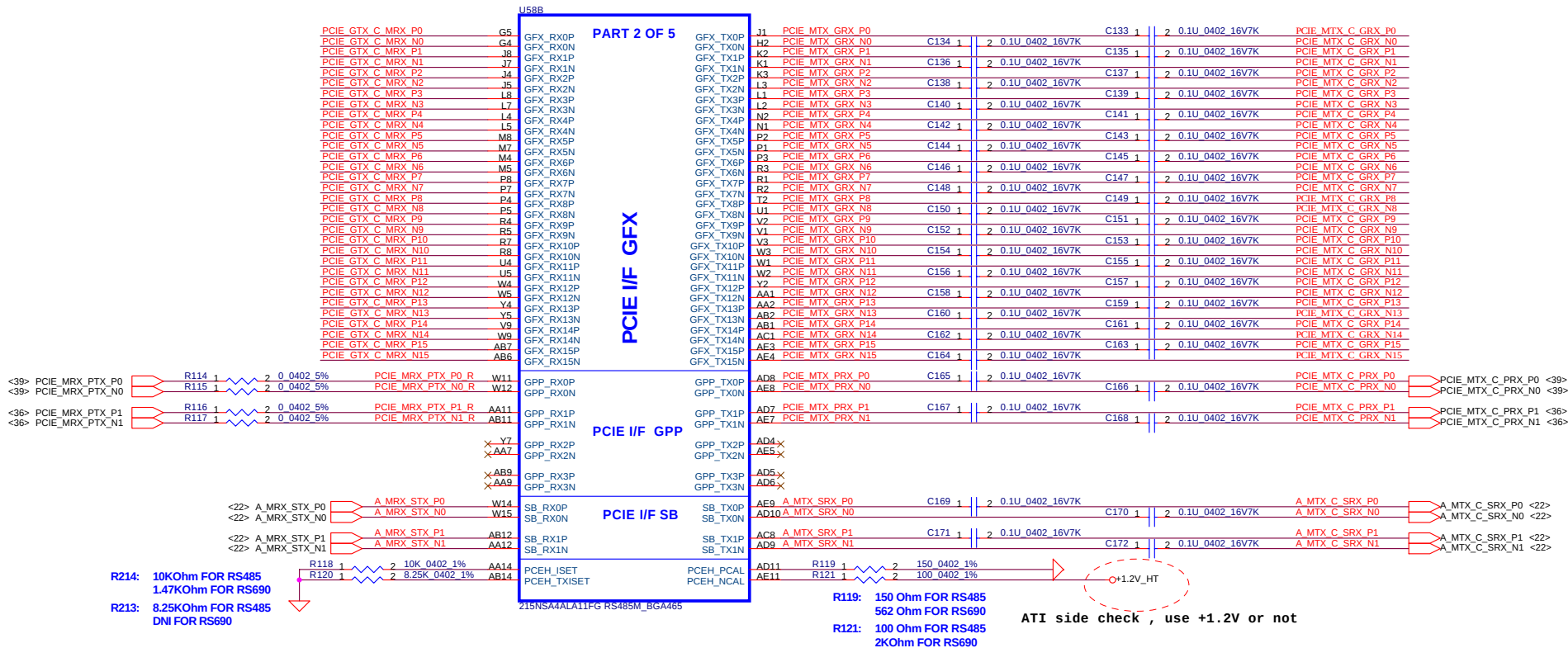




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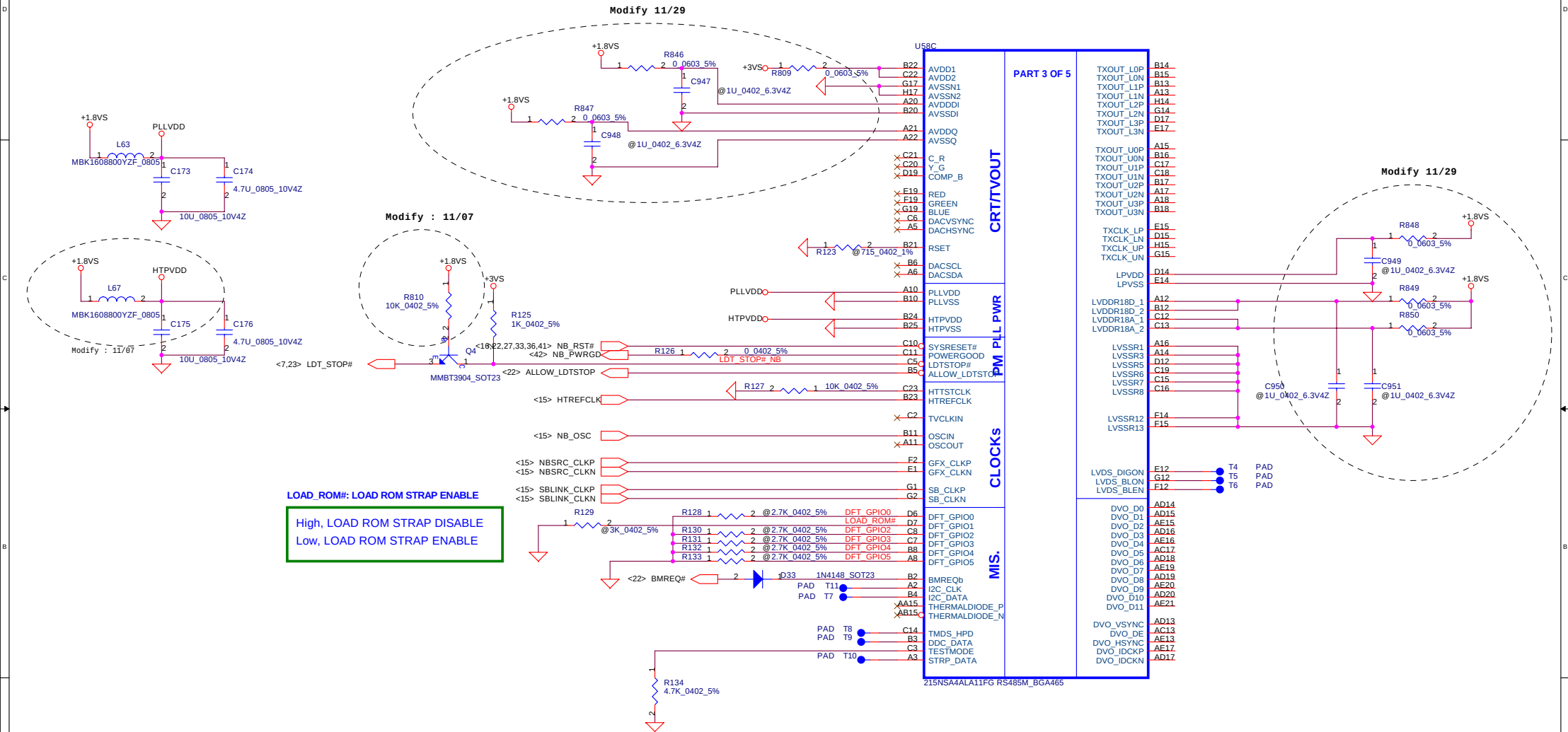
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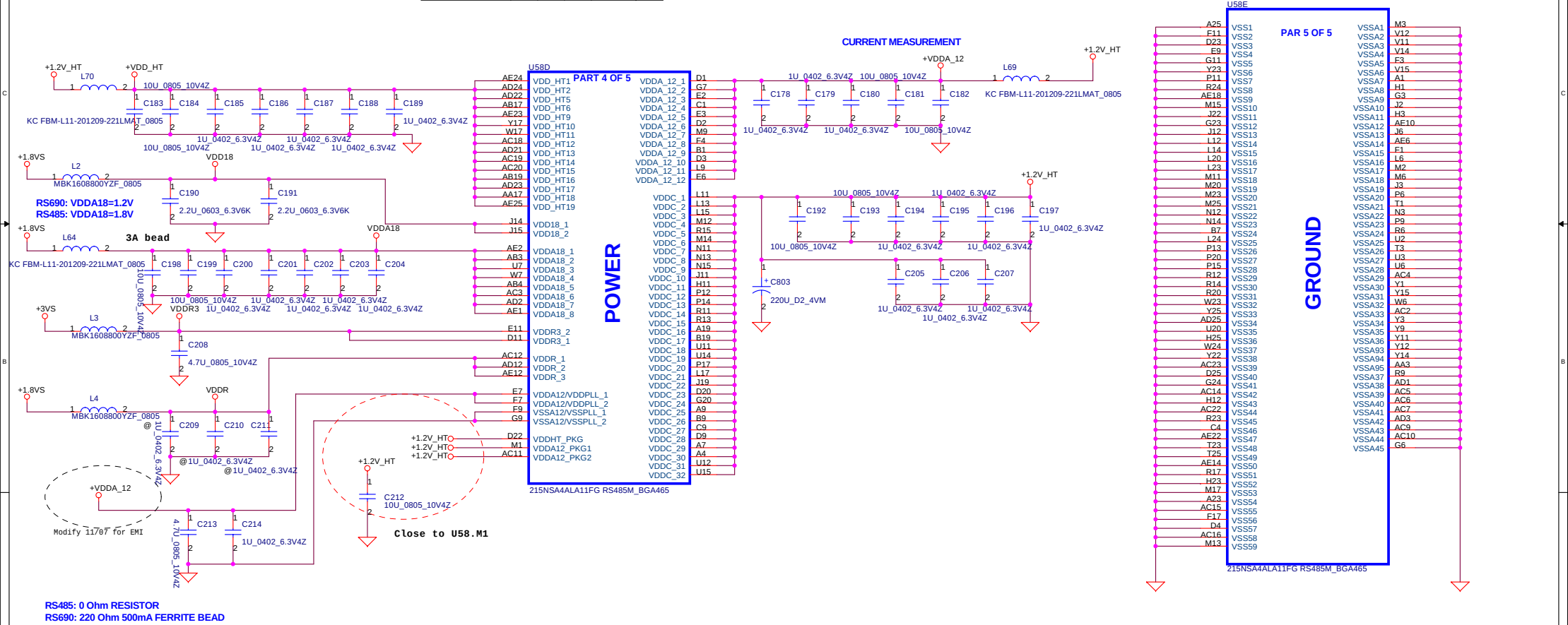
ATI check , CRT / TV/ LVDS can delete or not when I use RX485



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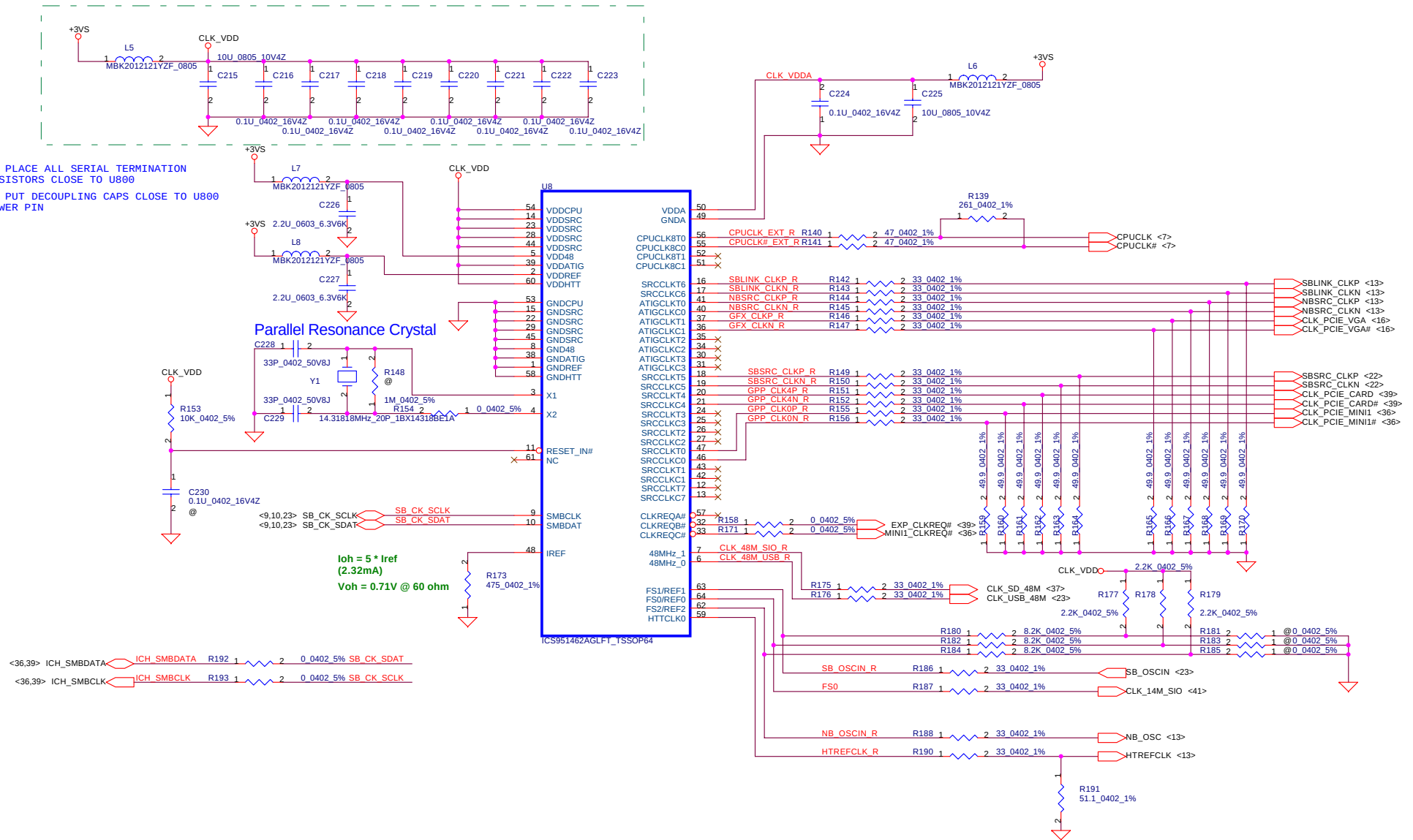
NB RS485 POWER STATES

Power	Signal	S0	S1	S3	S4/S5	G3
VDDHT		ON	ON	OFF	OFF	OFF
VDDR		ON	ON	OFF	OFF	OFF
VDD18		ON	ON	OFF	OFF	OFF
VDDC		ON	ON	OFF	OFF	OFF
VDDA18		ON	ON	OFF	OFF	OFF
VDDA12		ON	ON	OFF	OFF	OFF
AVDD		ON	ON	OFF	OFF	OFF
AVDDDI		ON	ON	OFF	OFF	OFF
PLLVD		ON	ON	OFF	OFF	OFF
HTPVDD		ON	ON	OFF	OFF	OFF
VDDR3		ON	ON	OFF	OFF	OFF
LPVDD		ON	ON	OFF	OFF	OFF
LVDDR18D		ON	ON	OFF	OFF	OFF
LVDDR18A		ON	ON	OFF	OFF	OFF





- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

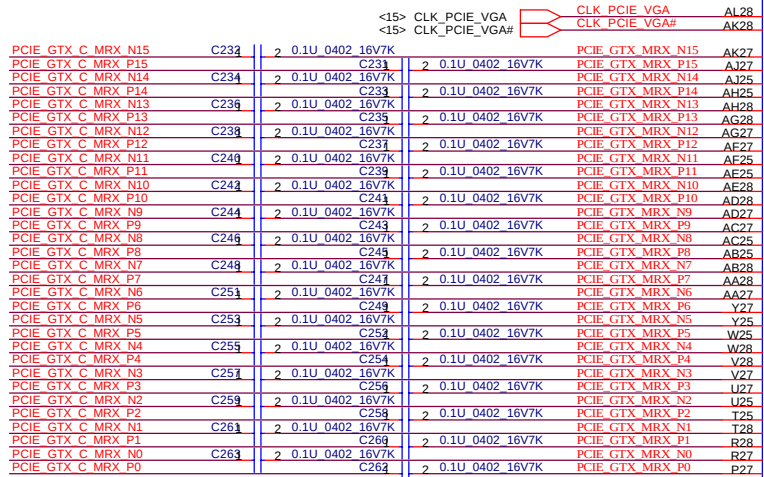


EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HIT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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PCIE Lane Reversal



U9A

GPIO

GPIO_0

GPIO_1

GPIO_2

GPIO_3

GPIO_4

GPIO_5

GPIO_6

GPIO_7

GPIO_8

GPIO_9

GPIO_10

GPIO_11

GPIO_12

GPIO_13

GPIO_14

GPIO_15

GPIO_16

GPIO_17

GPIO_18

GPIO_19

GPIO_20

GPIO_21

GPIO_22

GPIO_23

GPIO_24

GPIO_25

GPIO_26

GPIO_27

GPIO_28

GPIO_29

GPIO_30

GPIO_31

GPIO_32

GPIO_33

GPIO_34

GPIO_35

GPIO_36

GPIO_37

GPIO_38

GPIO_39

GPIO_40

GPIO_41

GPIO_42

GPIO_43

GPIO_44

GPIO_0

GPIO_1

GPIO_2

GPIO_3

GPIO_4

GPIO_5

GPIO_6

GPIO_7

GPIO_8

GPIO_9

GPIO_10

GPIO_11

GPIO_12

GPIO_13

GPIO_14

GPIO_15

GPIO_16

GPIO_17

GPIO_18

GPIO_19

GPIO_20

GPIO_21

GPIO_22

GPIO_23

GPIO_24

GPIO_25

GPIO_26

GPIO_27

GPIO_28

GPIO_29

GPIO_30

GPIO_31

GPIO_32

GPIO_33

GPIO_34

GPIO_35

GPIO_36

GPIO_37

GPIO_38

GPIO_39

GPIO_40

GPIO_41

GPIO_42

GPIO_43

GPIO_44

PCIEXPRESS

CRT

TV

THERMAL

XTAL

Straps: (Internal pull down)

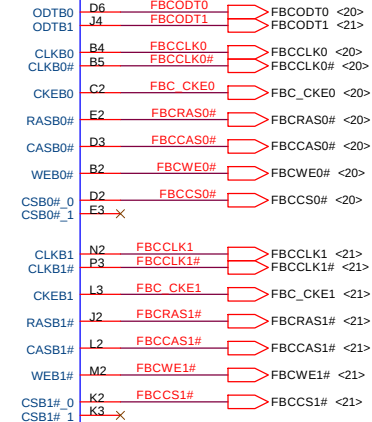
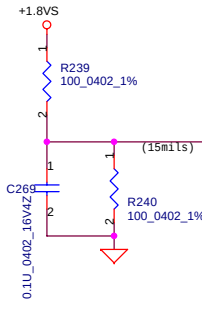
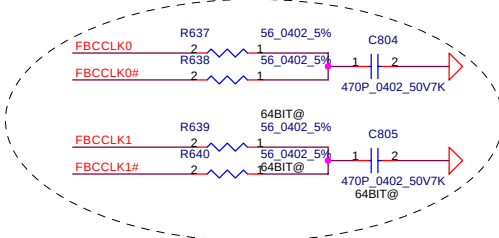
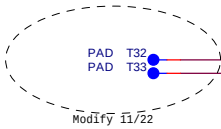
Transmitter power saving enable	GPIO[0]	0: 50% TX output swing 1: Full TX output swing
Transmitter de-emphasis enable	GPIO[1]	0: TX de-emphasis disable 1: TX de-emphasis enable
Debug Access	GPIO[4]	0: OFF Pad must be available 1: ON
PLL_IBIAS_RD	GPIO[6,5]	Default : 01
ROM ID Config	GPIO[9, 13:11]	000X: No ROM, AP_SIZE=00 128M share 001X: No ROMMemory AP_SIZE=01 256M share 010X: No ROMMemory AP_SIZE=10 64M share 011X: No ROMMemory AP_SIZE=11 Reserved

Vedio Memory Config. (VGA Internal PD)

MEMID[2:0]	Size	Size	Vender	Chips	VGA	Frequence
0 0 0	64MB	16M16	Hynix	2		
0 0 1	64MB	16M16	Samsung	2		
0 1 0	128MB	16M16	Hynix	4		A-test
0 1 1	128MB	16M16	Samsung	4		A-test
1 0 0	256MB	32M16	Hynix	4		A-test
1 0 1	256MB	32M16	Samsung	4		A-test
1 1 0			Resreved			
1 1 1			Resreved			

TBD

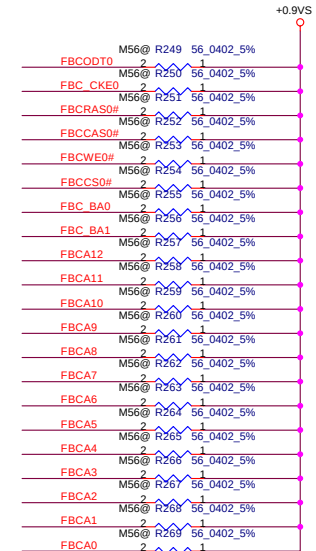
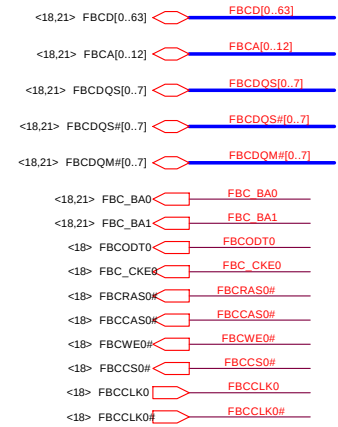
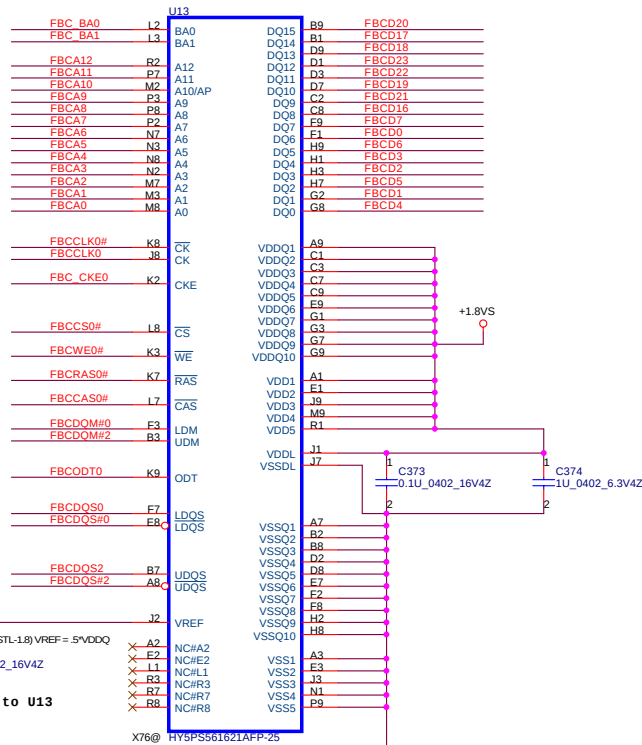
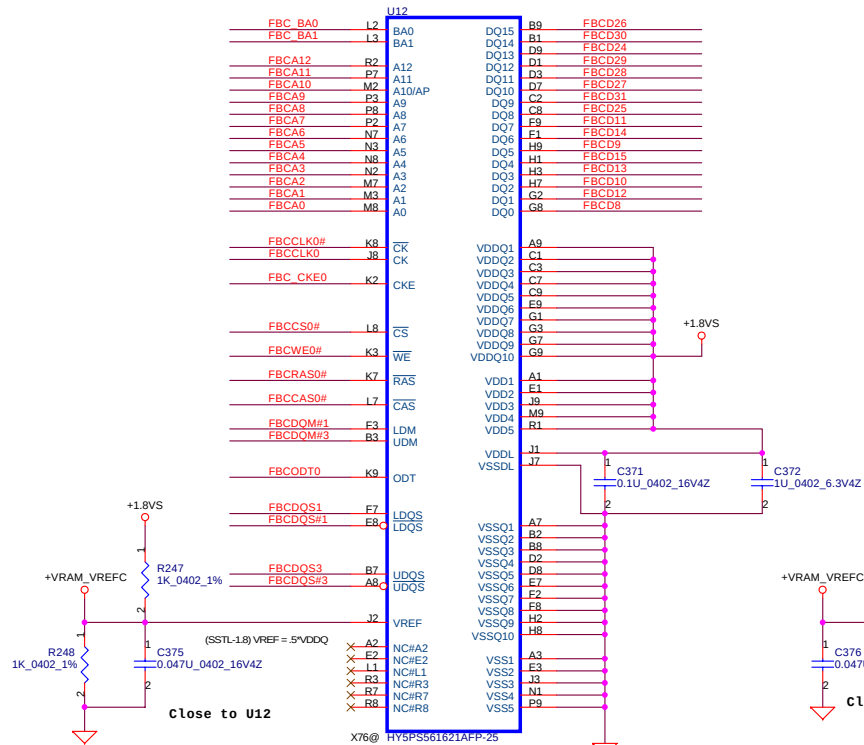
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11/03/05' SWAP NET
11/04/05' SWAP NET
11/08/05' SWAP NET

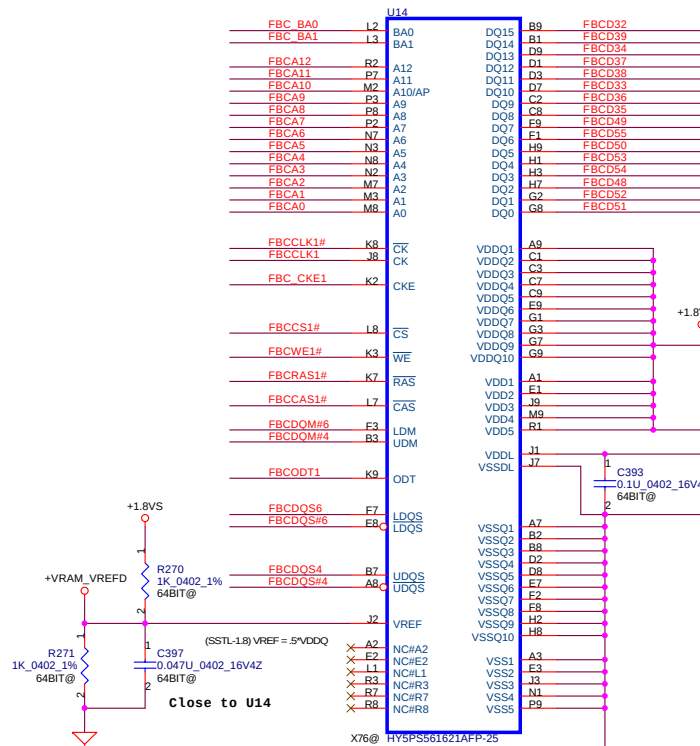
11/03/05' SWAP NET



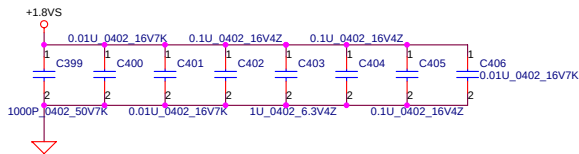
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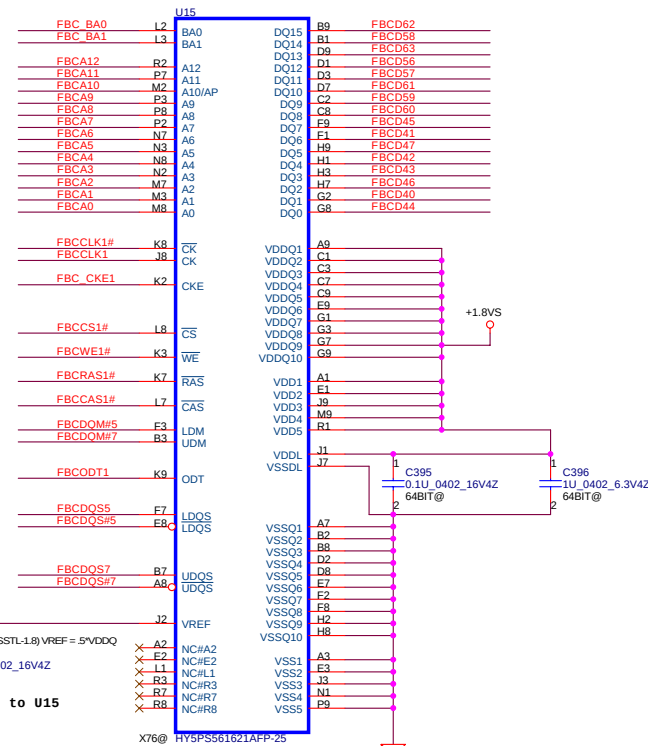
11/03/05' SWAP NET



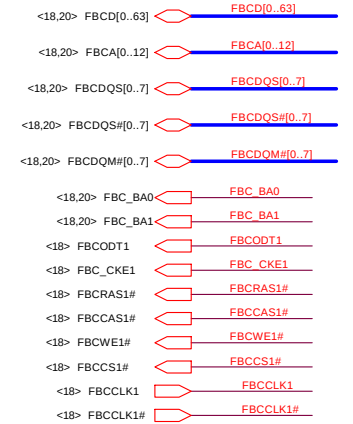
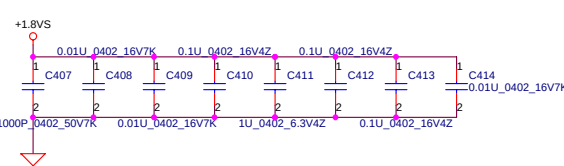
DDR2 BGA MEMORY



11/03/05' SWAP NET

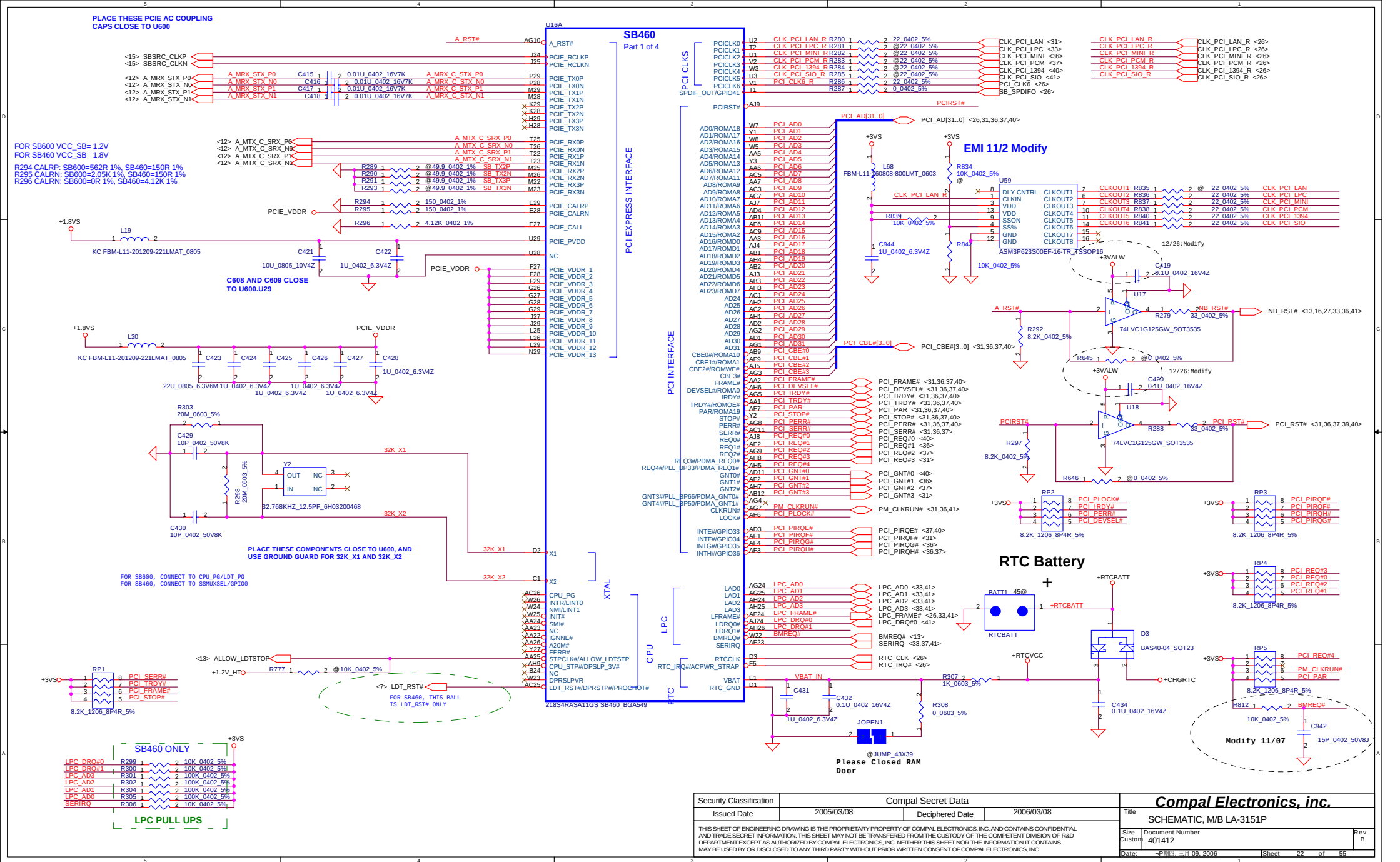


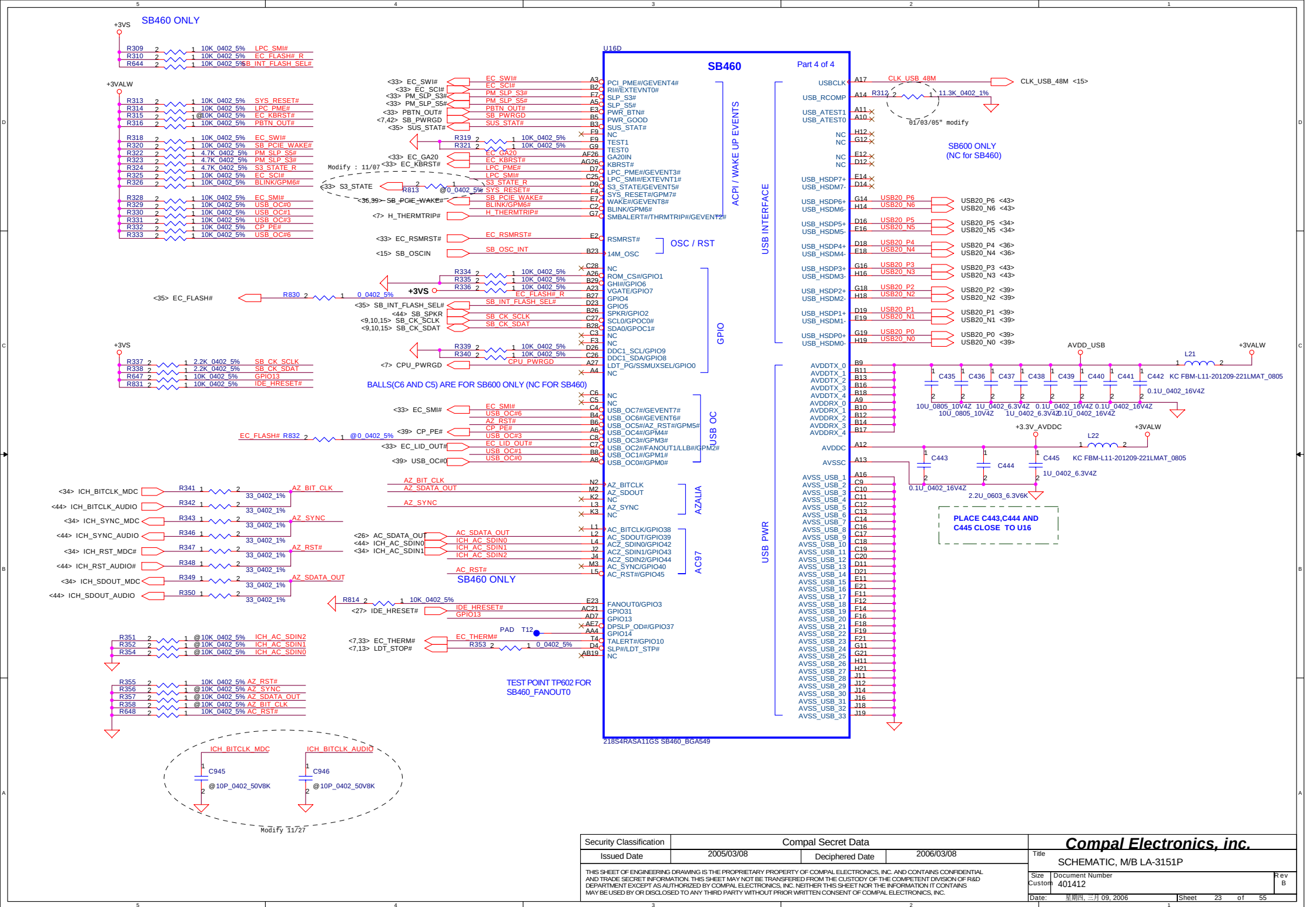
DDR2 BGA MEMORY

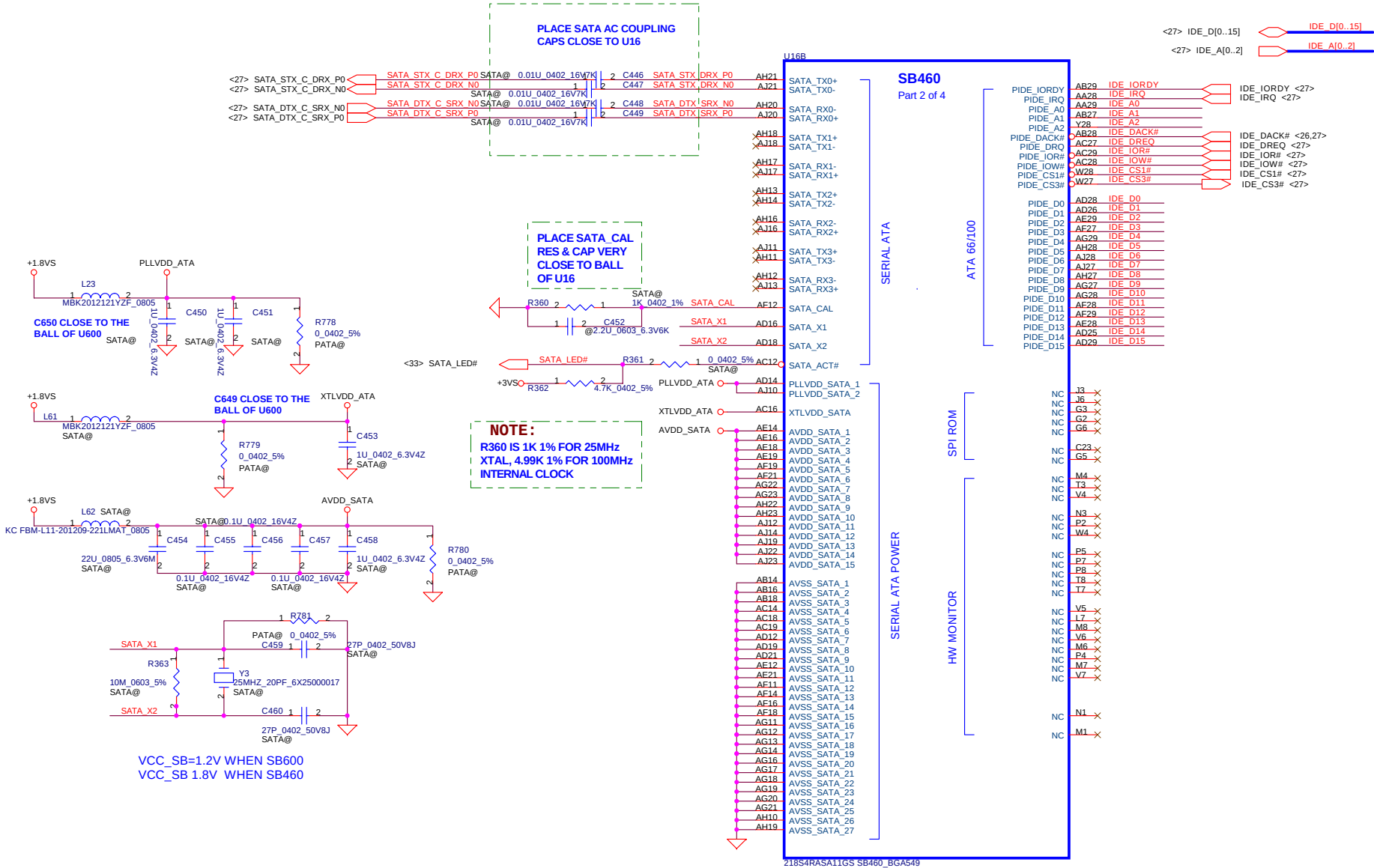


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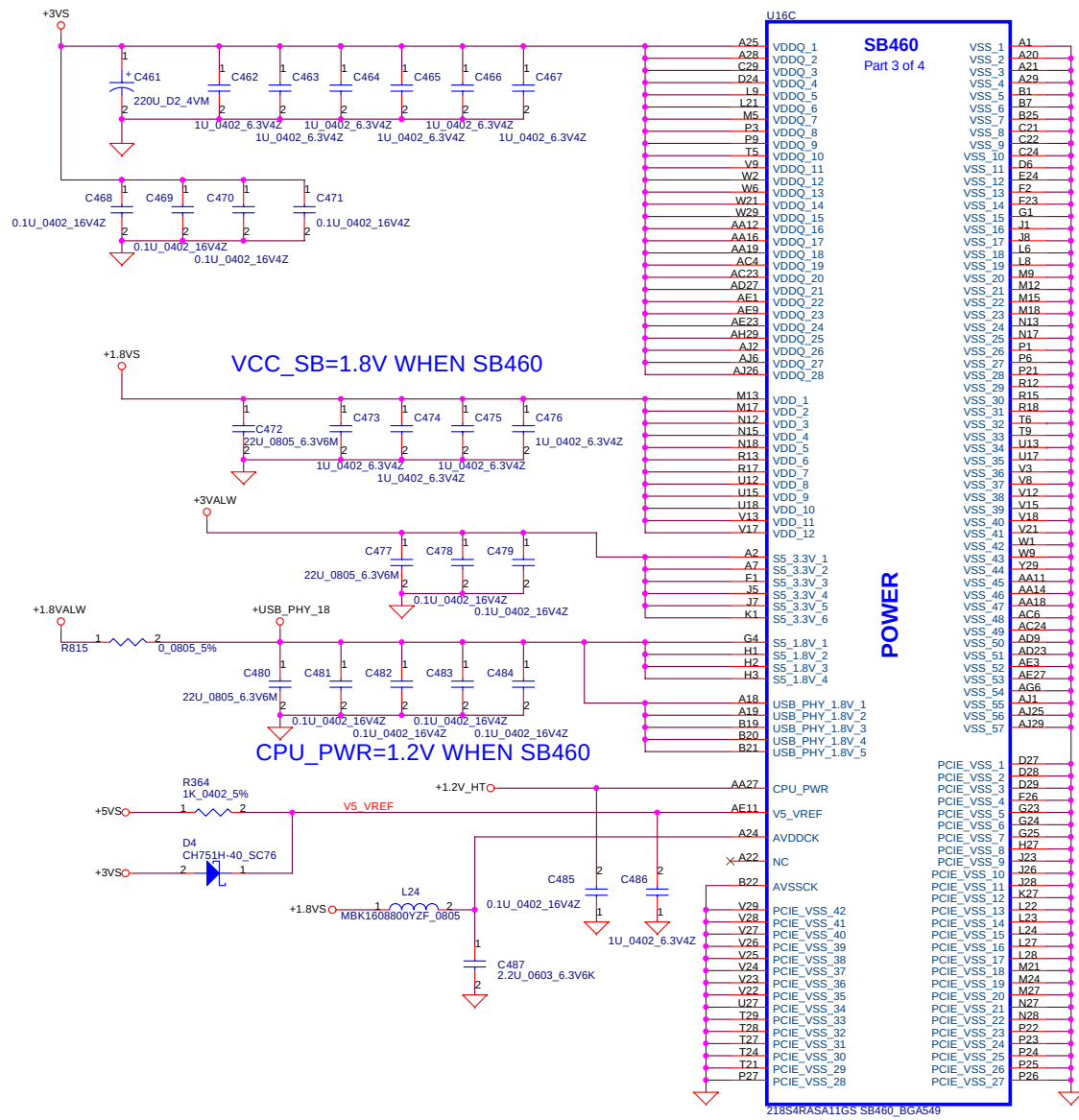
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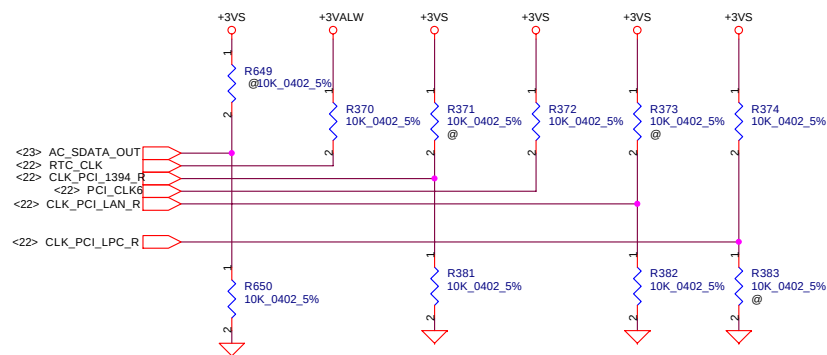
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REQUIRED STRAPS

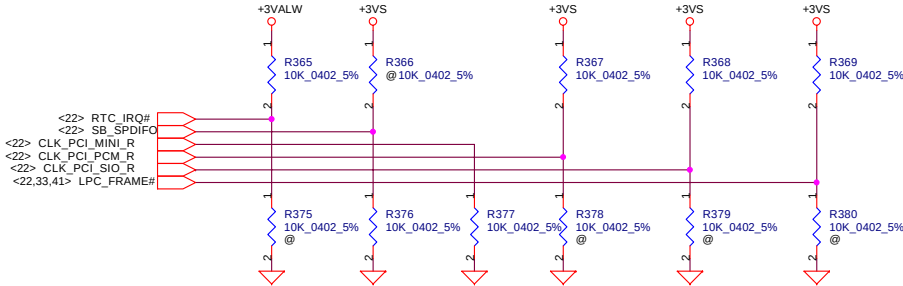
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED



PULL	SB600				SB460			
	AC_SDATA_OUT	RTC_CLK	PCI_CLK4 CLK_PCI_1394	PCI_CLK6	PCI_CLK0 CLK_PCI_LAN	PCI_CLK1 CLK_PCI_LPC	PCI_CLK0 CLK_PCI_LAN	PCI_CLK1 CLK_PCI_LPC
	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM	DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM	DEFAULT
	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	L, L = FWH ROM		L, L = FWH ROM	
HIGH	DEFAULT	DEFAULT	DEFAULT	DEFAULT				
LOW	DEFAULT	DEFAULT	DEFAULT	DEFAULT				

NOTE: R365 PU RESISTOR FOR
RTC_IRQ# IS REQUIRED FOR SB460
TO KEEP THE INPUT FROM FLOATING.

SB460 ONLY



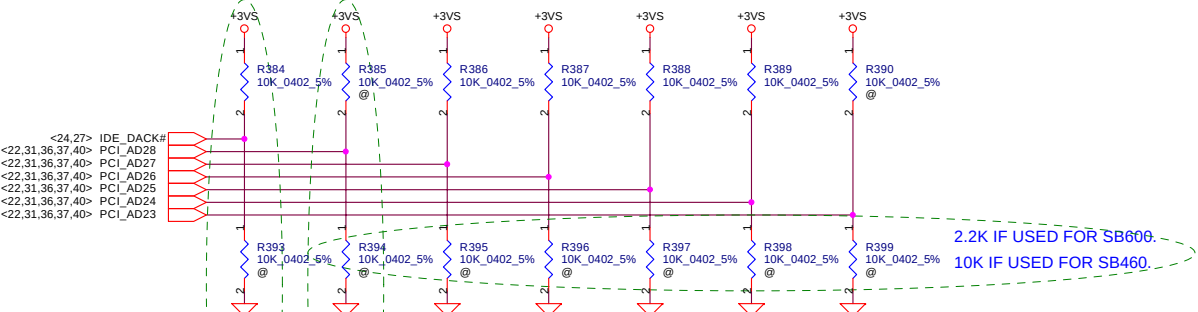
PULL	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
	RTC_IRQ#	SB_SPDIFO	CLK_PCI_MINI	CLK_PCI_PCM	CLK_PCI_SIO	LPC_FRAME#
	MANUAL PWR ON	SIO 24MHZ	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE	PCIE_CM_SET LOW	ENABLE THERMTRIP#
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
HIGH						
LOW						



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
HIGH	USE LONG RESET	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB460 ONLY

SB600 ONLY

SB600 ONLY

NOTE: FOR
SB460,
PCI_AD23 IS
RESERVED

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<24> IDE_D[0..15] IDE_D[0..15]
<24> IDE_A[0..2] IDE_A[0..2]

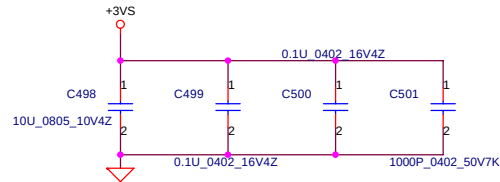
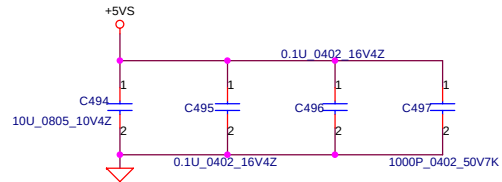
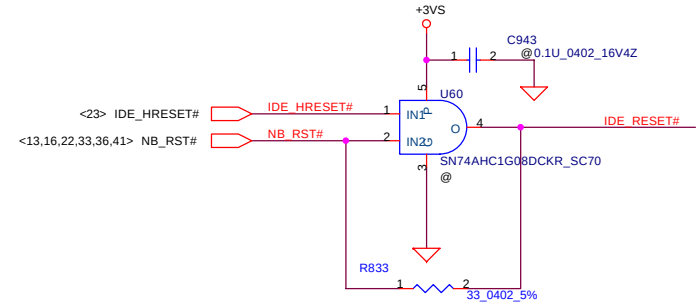


Diagram illustrating the SATA connector pinout for the OTEK SAT-22SG1G_NR. The connector is a 22-pin SATA connector, with pins 1 through 22 labeled on the right side. The pins are connected to various signals and power planes as follows:

- Pins 1-7 (Left side):
 - Pin 1: SATA_STX_C_DRX_P0
 - Pin 2: SATA_STX_C_DRX_N0
 - Pin 3: HTX+
 - Pin 4: HTX-
 - Pin 5: SATA_DTX_C_SRX_N0
 - Pin 6: SATA_DTX_C_SRX_P0
 - Pin 7: HRX+
- Pins 8-22 (Right side):
 - Pins 8, 9, 10: VCC3.3
 - Pins 11, 12, 13: GND
 - Pins 14, 15, 16: VCC5
 - Pins 17, 18: RESERVED
 - Pins 19, 20, 21, 22: VCC12

A dashed oval encloses the pins 1-7 and 8-17, with a note "Modify 11/07 for EMI".

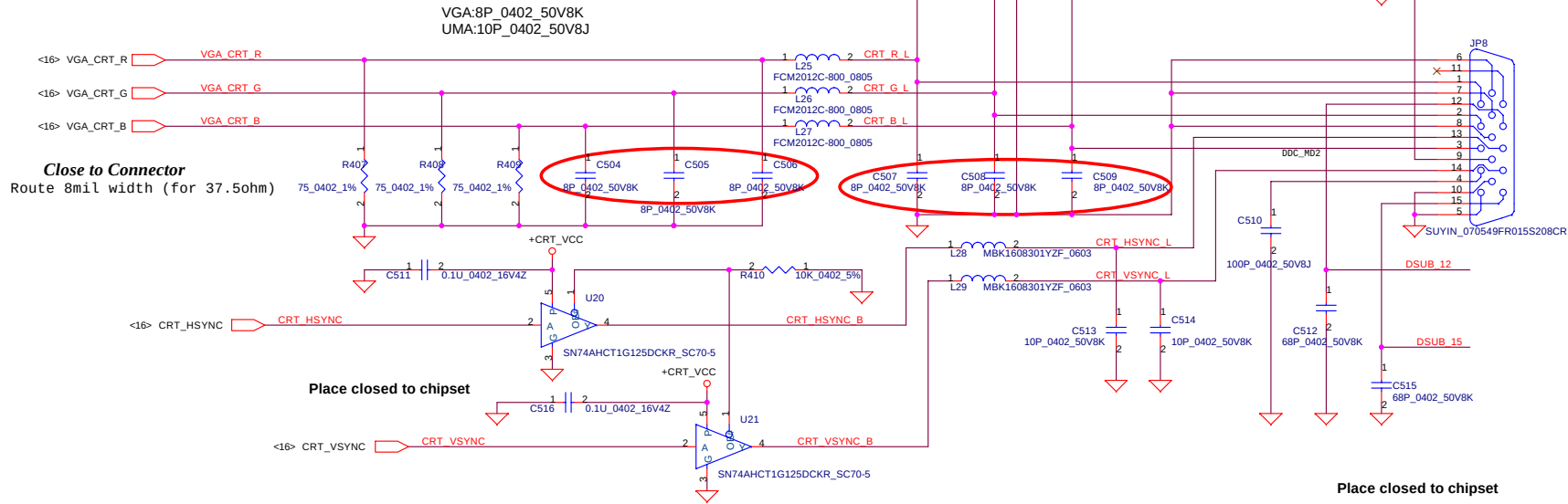
SATA@ OTEK SAT-22SG1G_NR
(NEW)

[illegible]

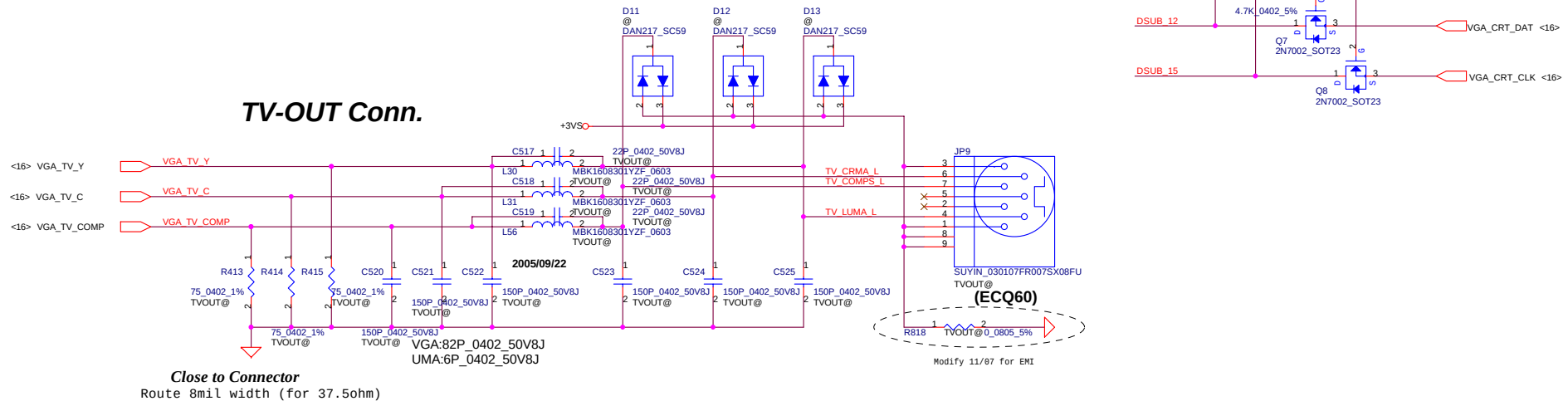
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CRT Connector

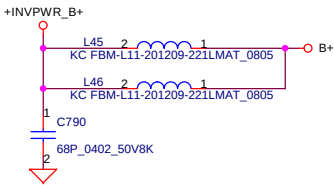
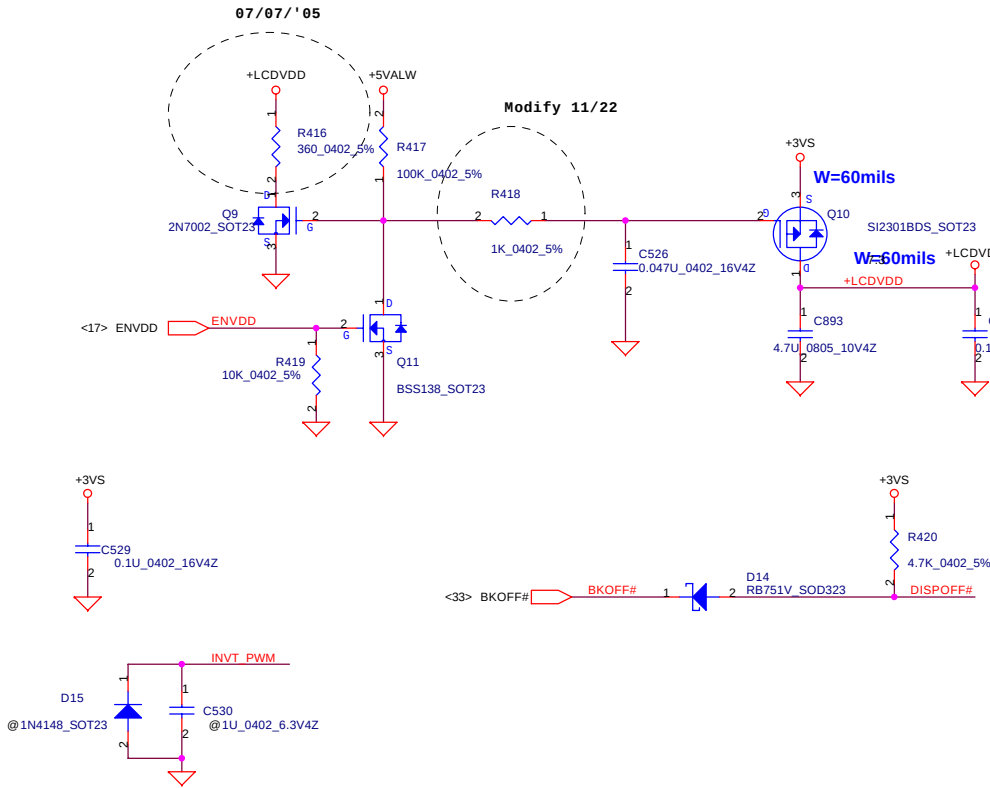


TV-OUT Conn.

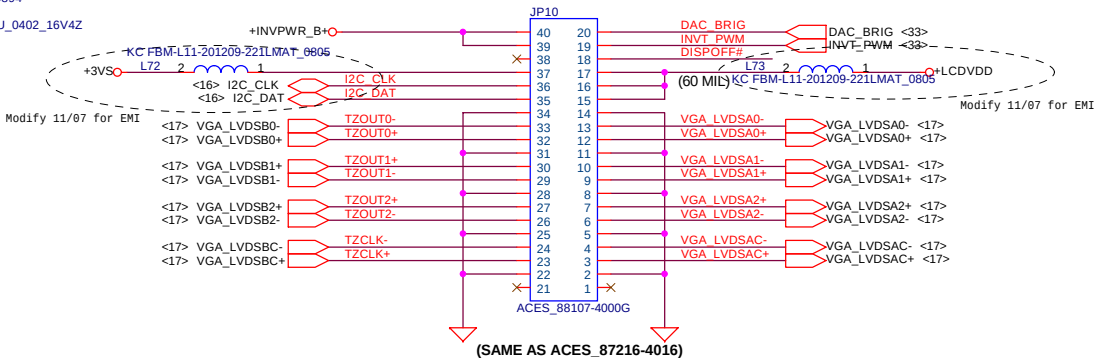


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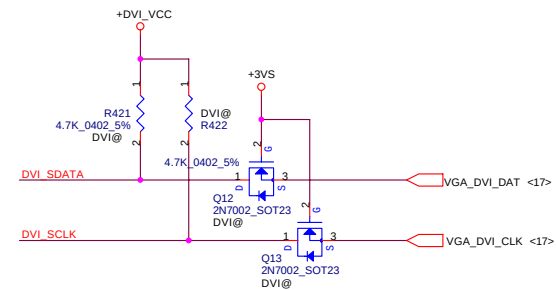
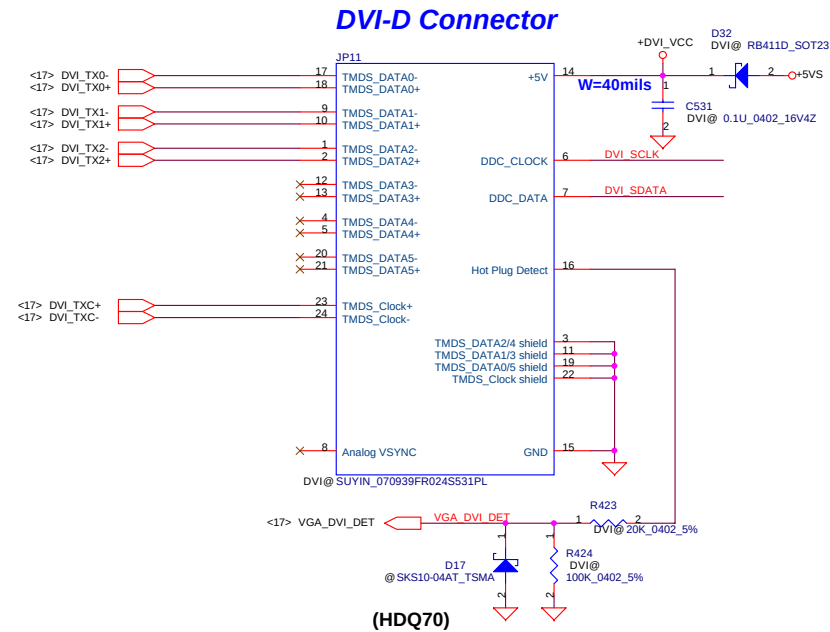
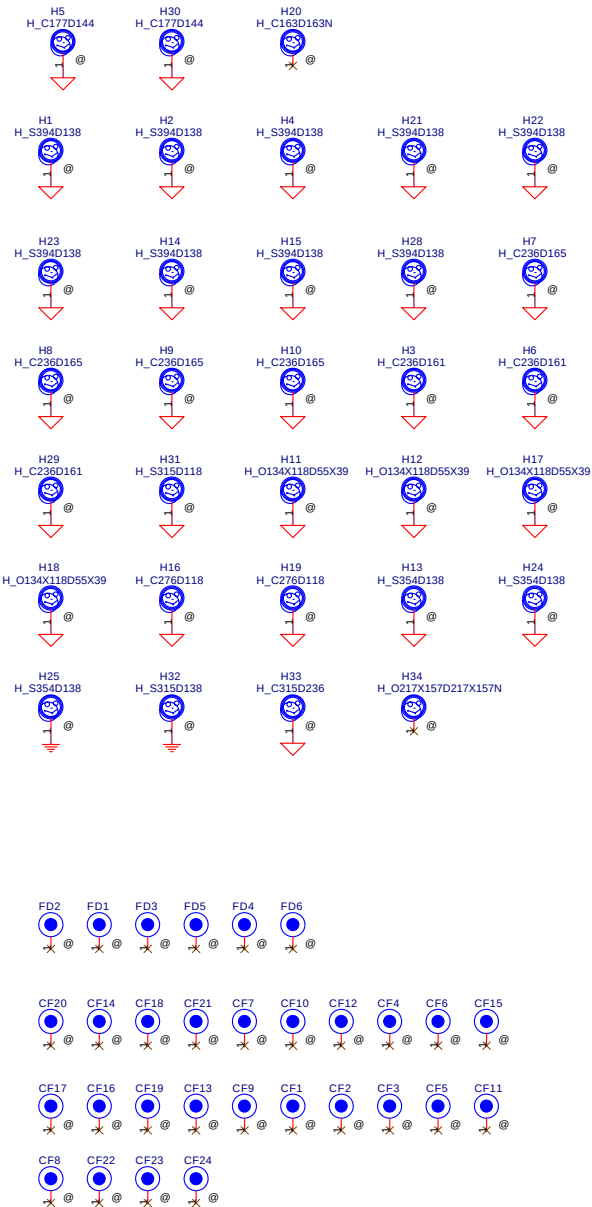
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

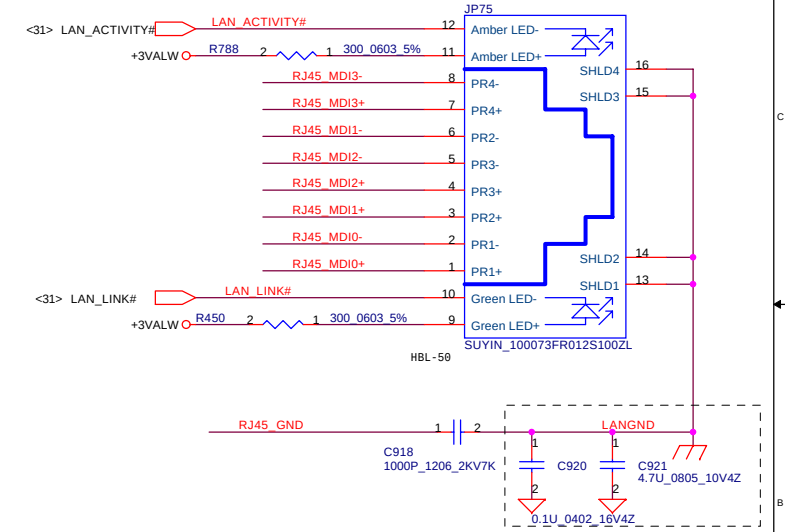
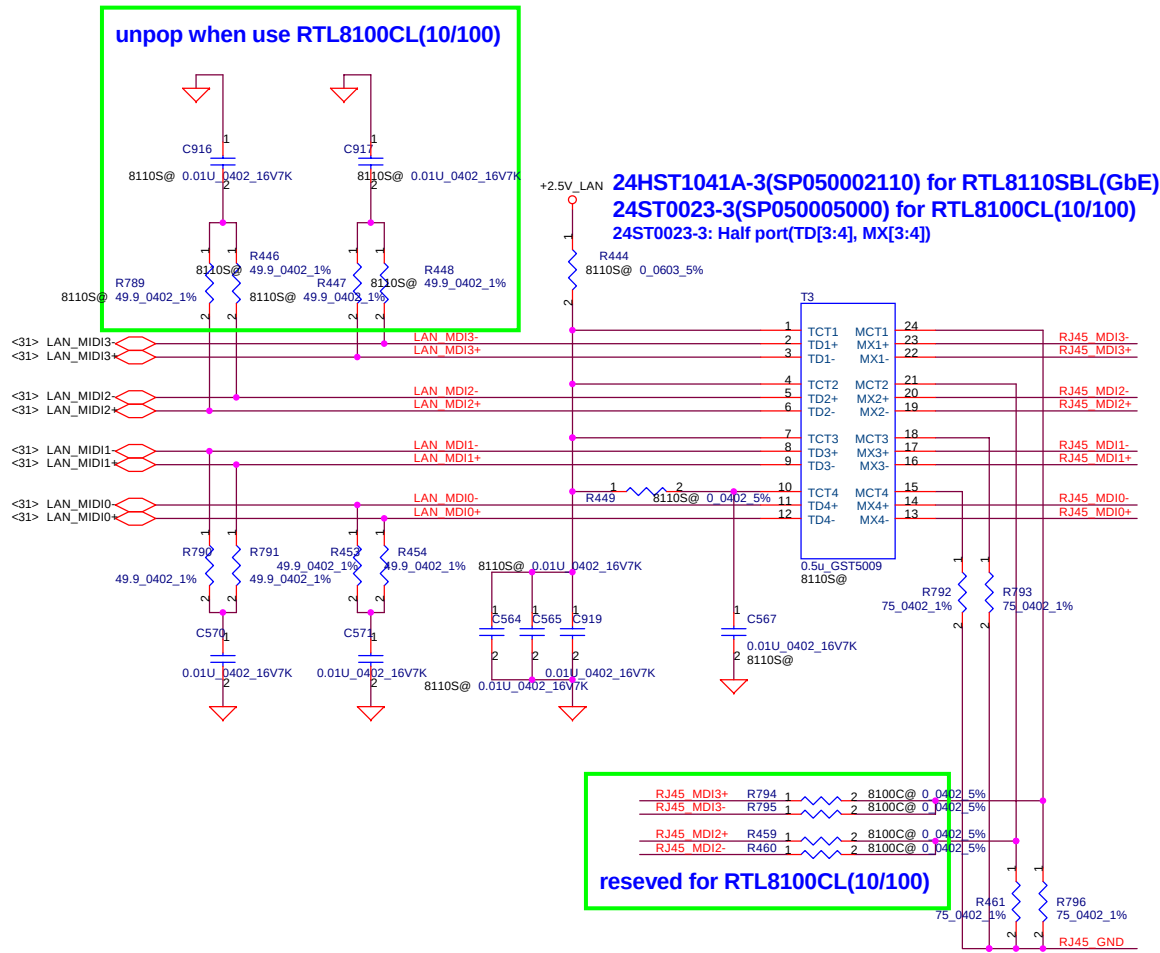


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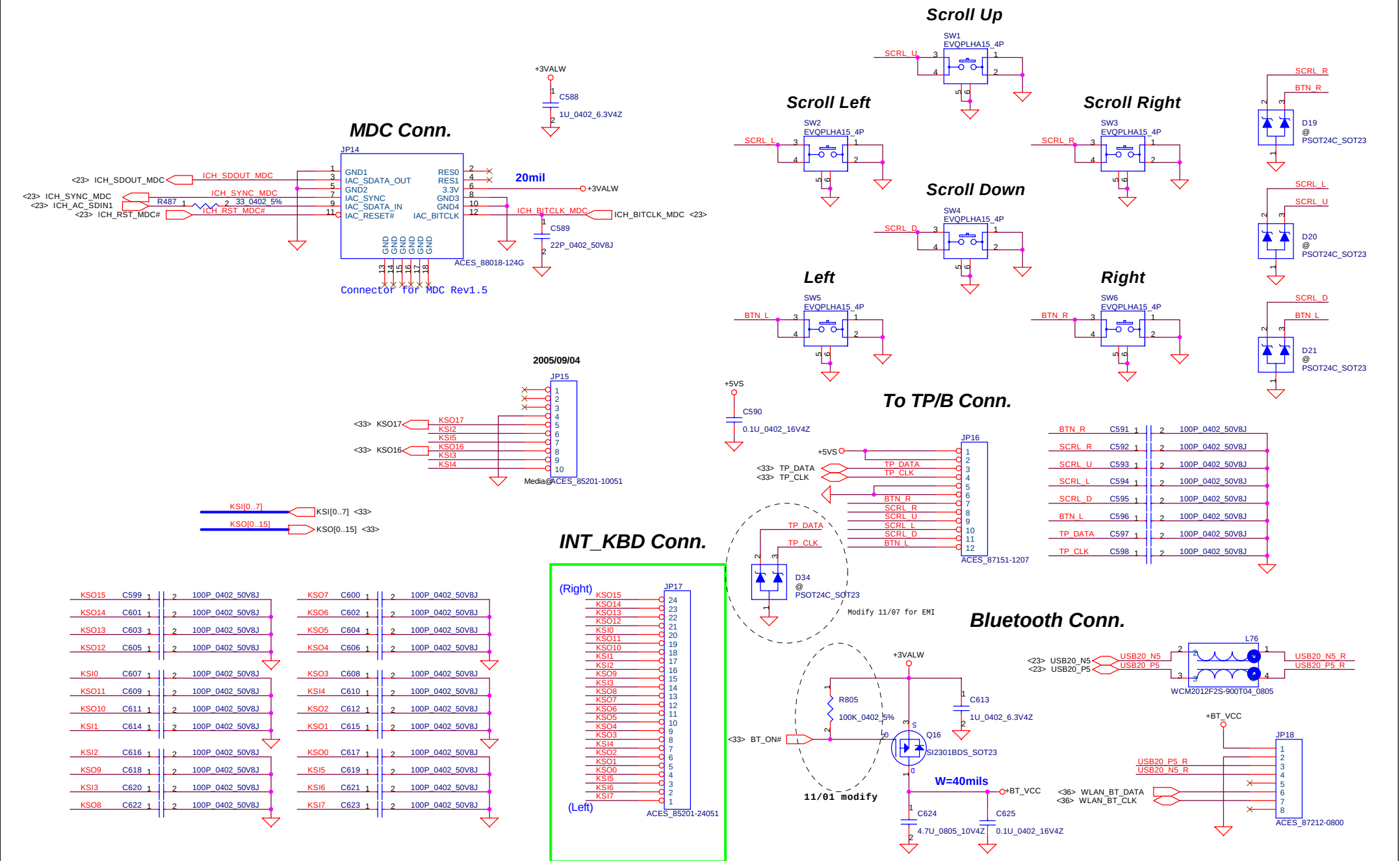


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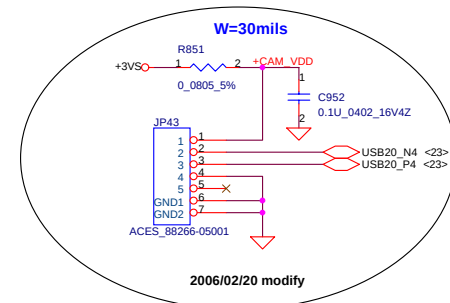
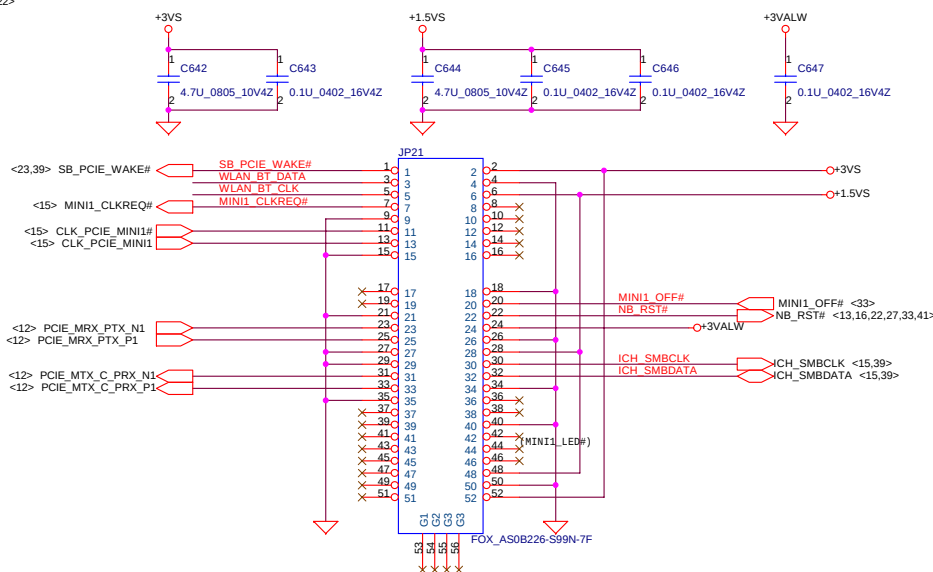
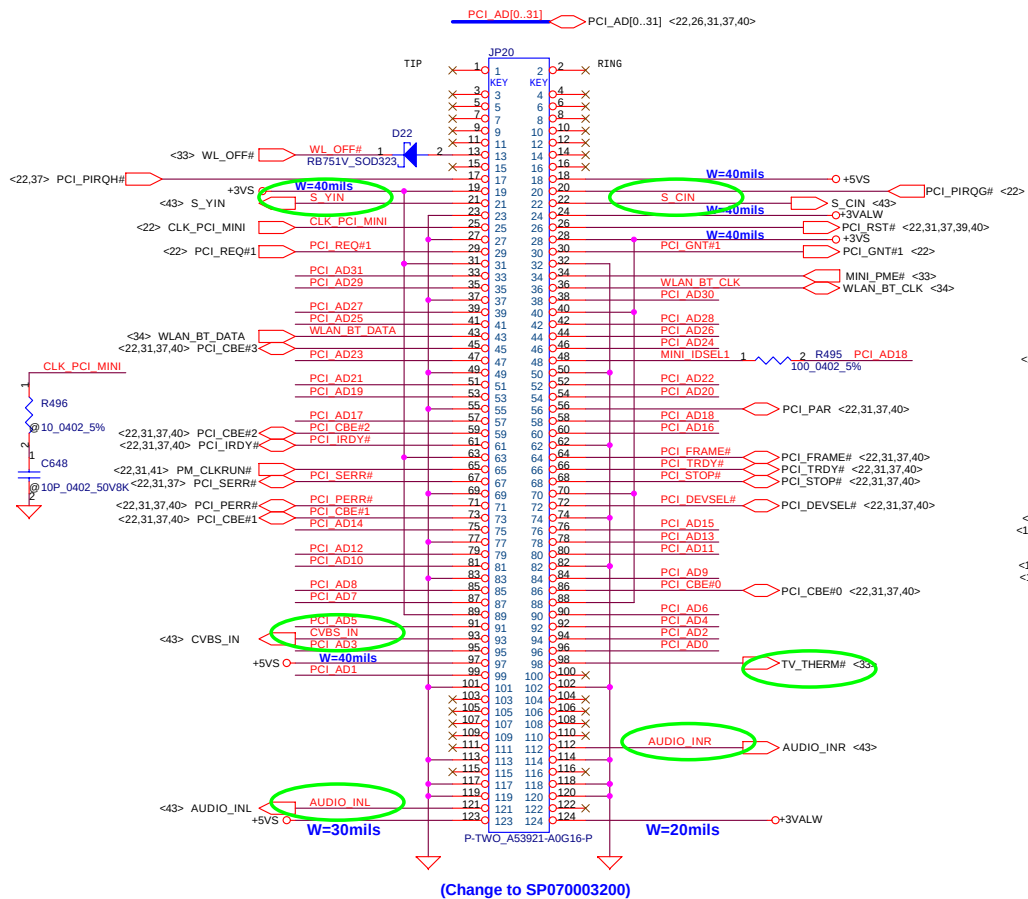
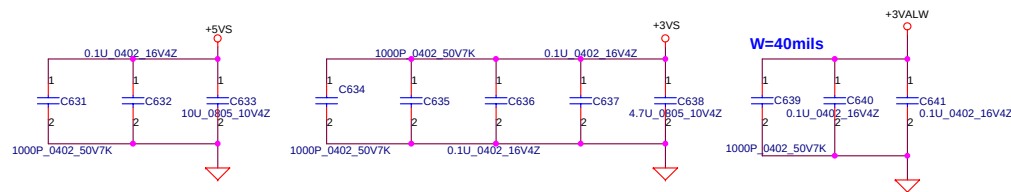
LAN RTL8110SBL/RTL8100CL



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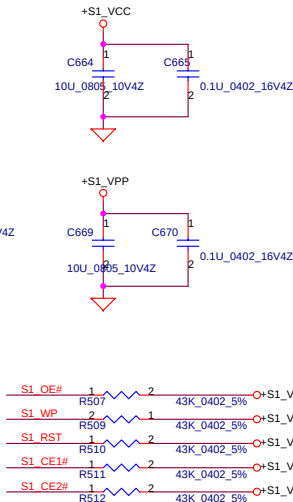
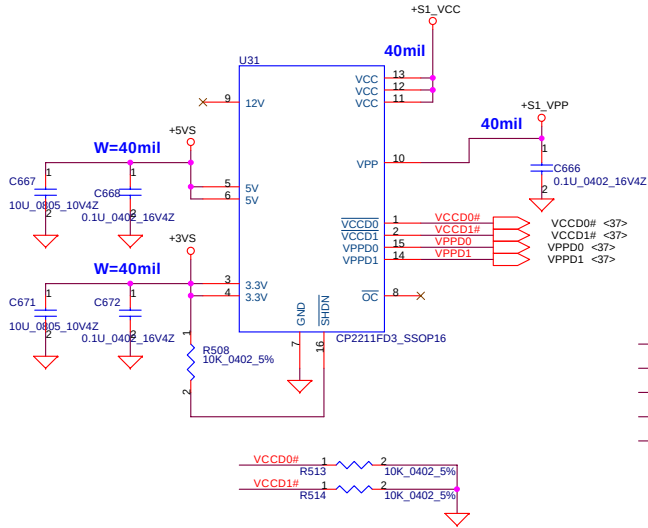
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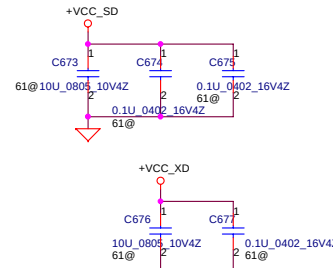
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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								Size B	Document Number						Rev B
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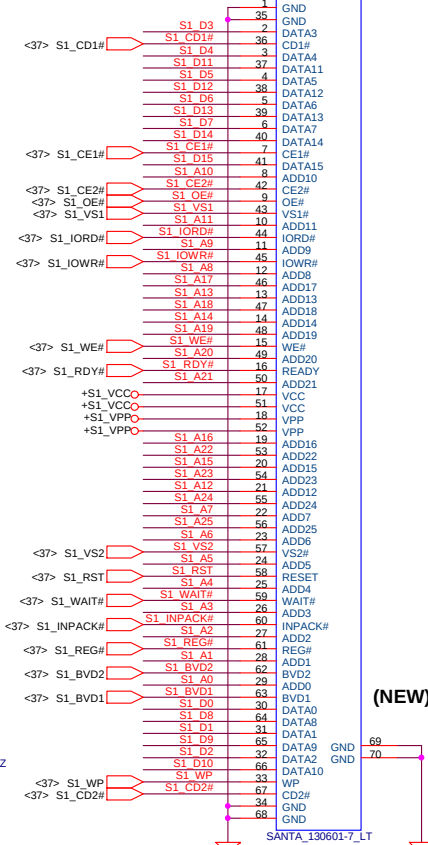
PCMCIA Power Control



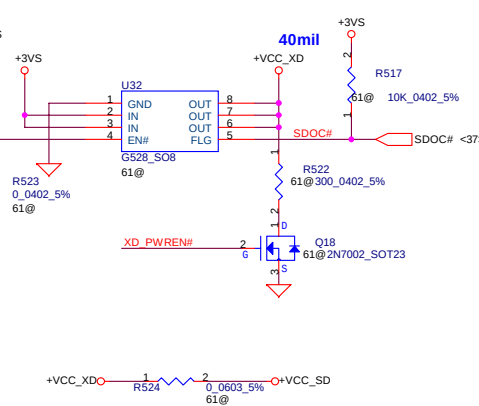
<37> S1_A[0..25] S1_A[0..25]
<37> S1_D[0..15] S1_D[0..15]



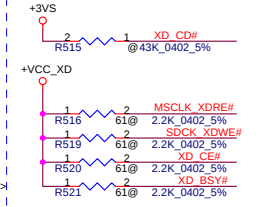
PCMCIA Socket



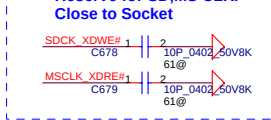
SD/MS Power Control



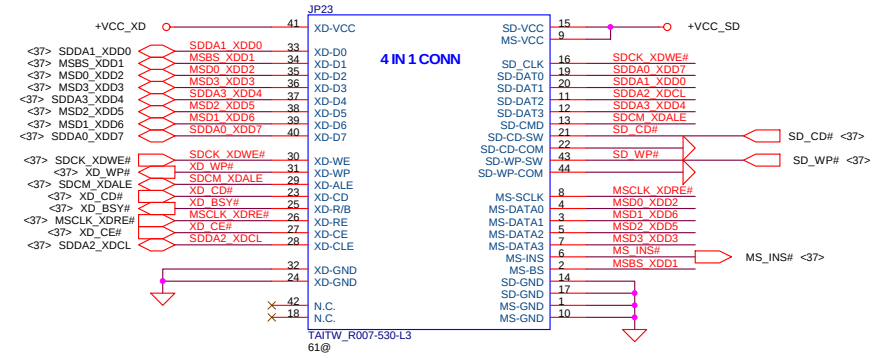
xD PU and PD. Close to Socket



Reserve for SD,MS CLK. Close to Socket



4 IN 1 Socket (HDQ70)

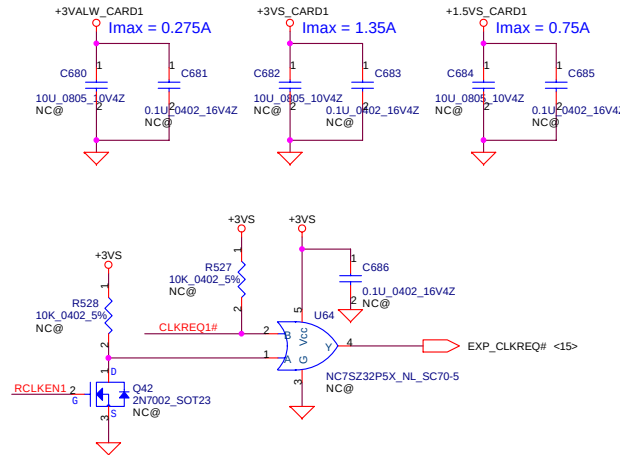
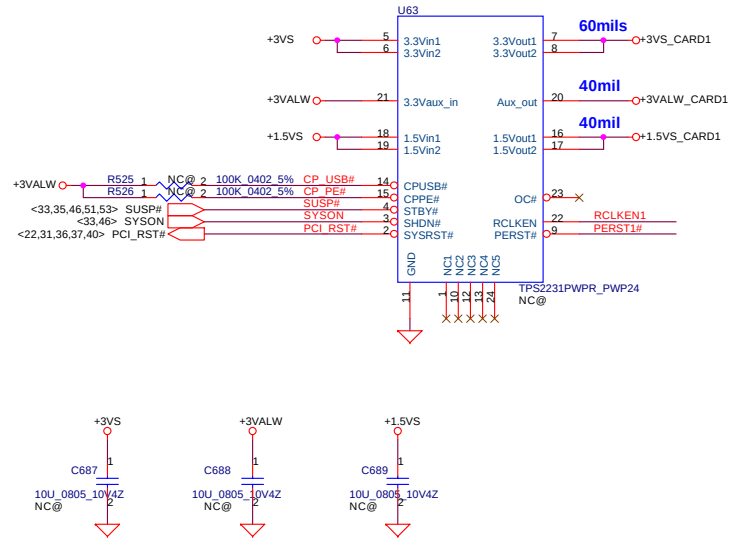


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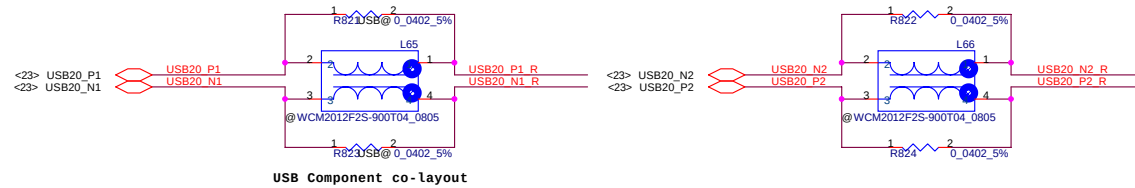
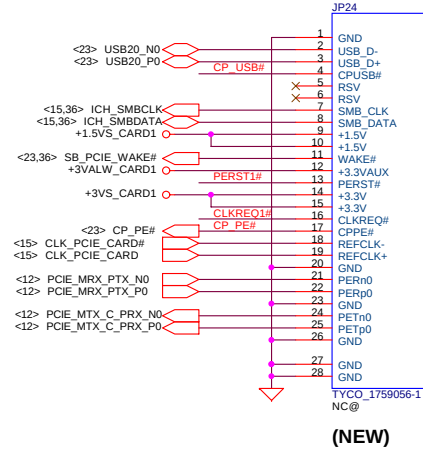
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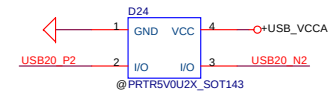
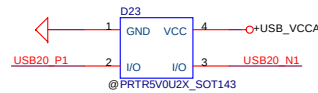
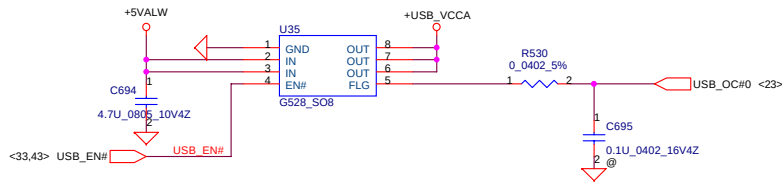
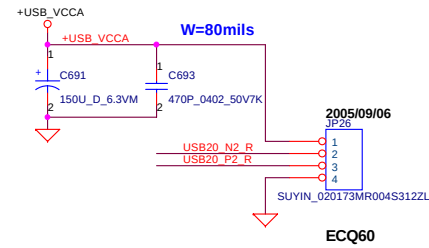
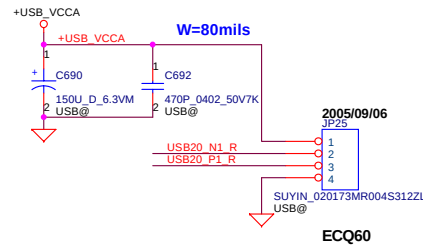
New Card Power Switch



New Card Socket (Left)



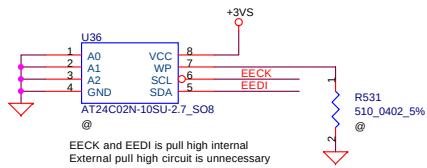
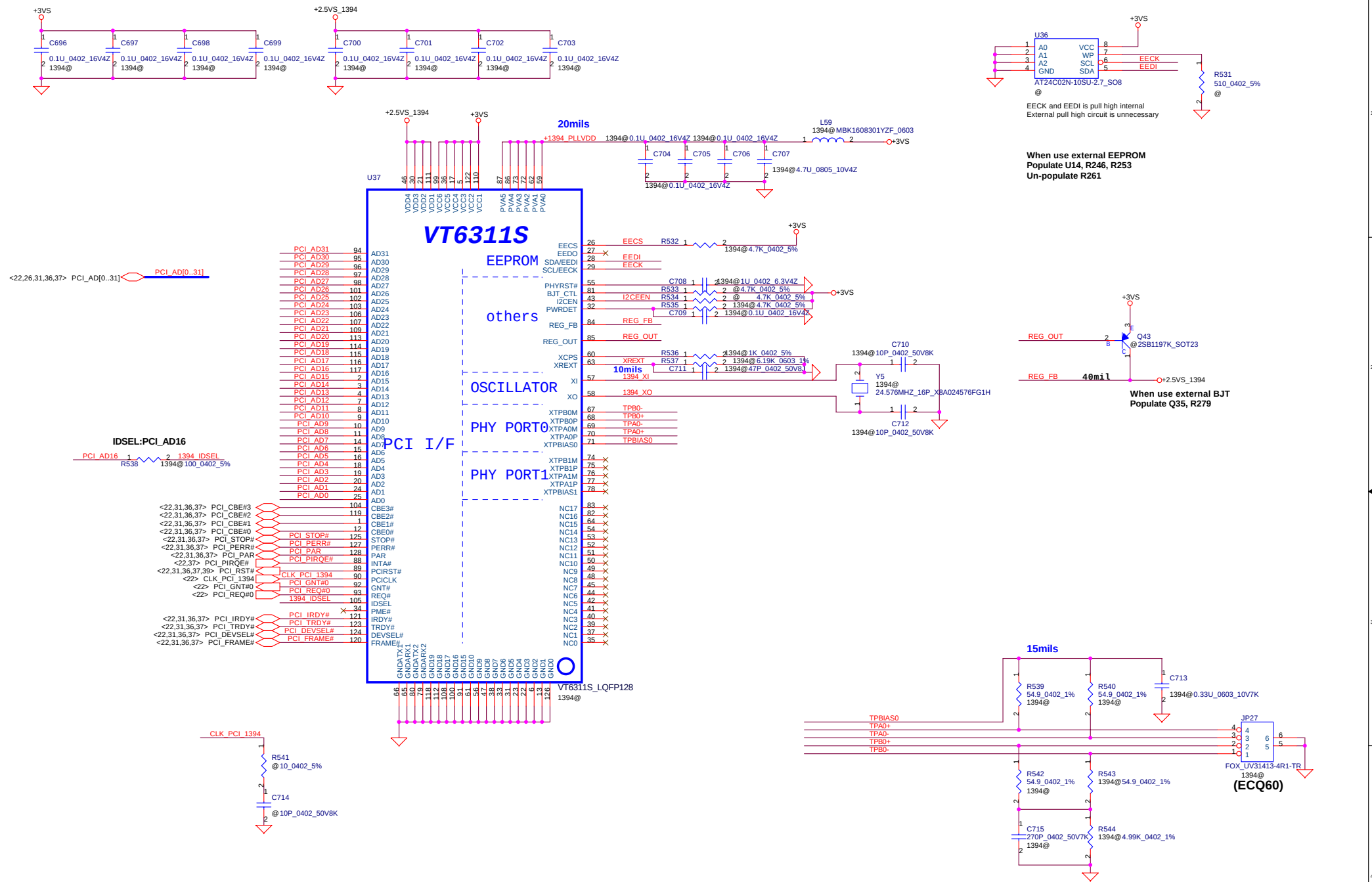
USB CONN. 1 & 2



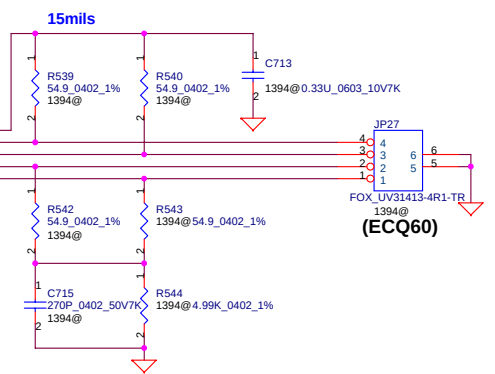
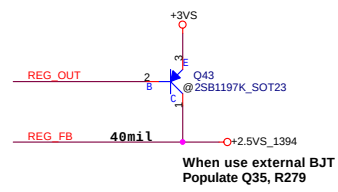
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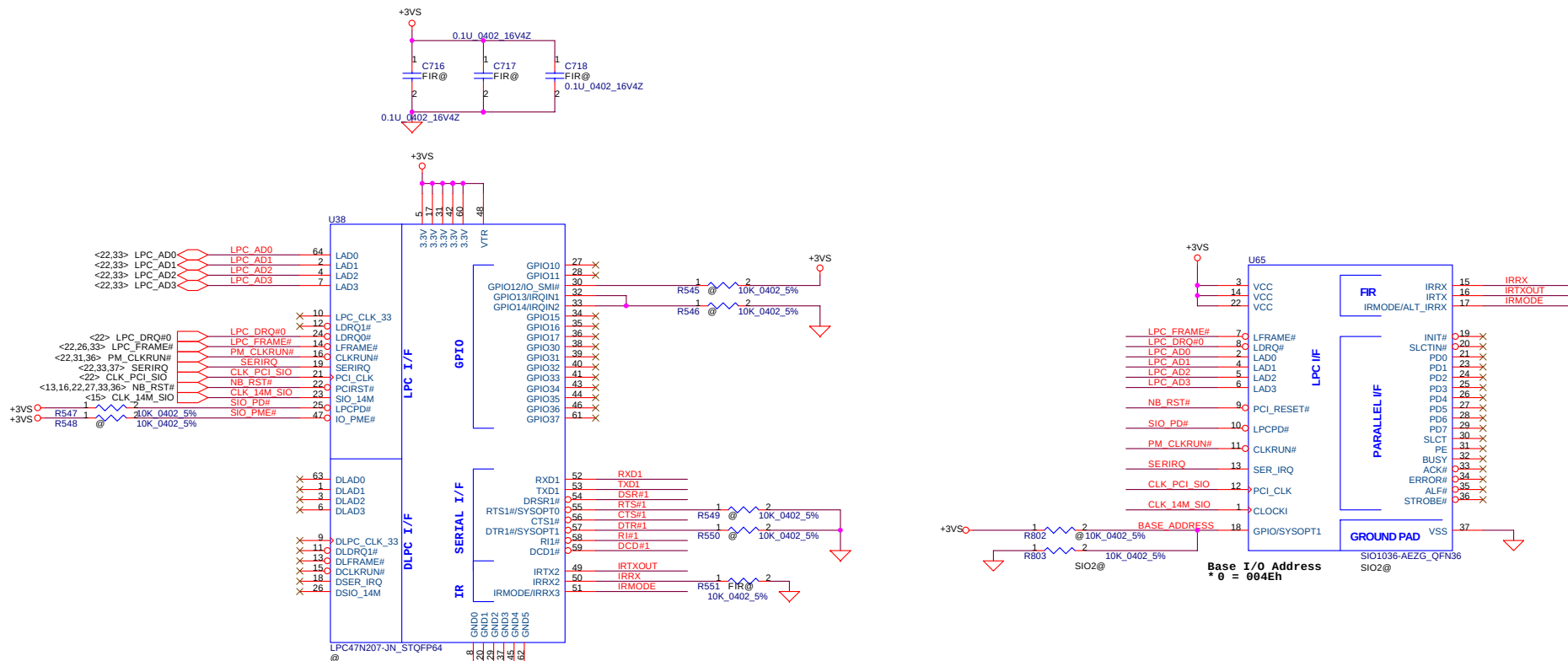


When use external EEPROM
Populate U14, R246, R253
Un-populate R261



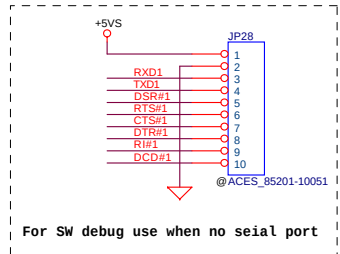
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SUPER I/O SMSc LPC47N207



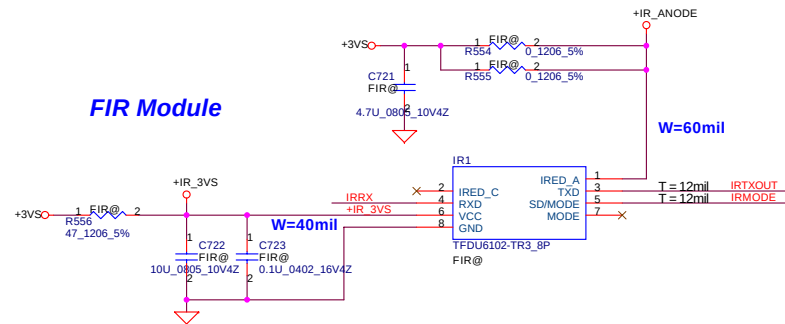
RTS#1
Base I/O Address
* 0 = 02Eh
1 = 04Eh

Place on the BOT side (near MINIPCI conn.)



For SW debug use when no serial port

FIR Module



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The diagram shows the timing of several signals during a suspend-to-standby transition. The signals are:

- VLDT_EN**: Active high signal.
- NB_PWRGD**: Active low signal.
- SB_PWRGD**: Active low signal.
- SUSP#**: Active low signal.
- +1.8VS**: Supply voltage.

Key timing points are marked:

- T1**: Start of the suspend-to-standby transition.
- T2**: Start of the suspend-to-deep-sleep transition.

The schematic diagram illustrates the Power Button circuit, divided into the TOP Side and Bottom Side.

TOP Side:

- The circuit is powered by a +3VALW supply.
- A resistor R562 (100K_0402_5%) is connected between the +3VALW supply and the gate of the MOSFET Q44 (2N7002_SOT23).
- The gate of Q44 is also connected to the ON/OFF button (<33> ON/OFFBTN#) and the 51ON# signal (<47> 51ON#).
- The drain of Q44 is connected to the gate of the MOSFET D25 (DAN202U_SC70).
- The source of Q44 is connected to ground.
- The source of D25 is connected to ground.
- The drain of D25 is connected to the 51ON# signal (<47> 51ON#).
- A capacitor C727 (1000P_0402_50V7K) is connected between the 51ON# signal and ground.
- A diode D27 (RLZ220A_LL34) is connected between the 51ON# signal and ground.

Bottom Side:

- The circuit is powered by a +3VALW supply.
- A resistor R564 (10K_0402_5%) is connected between the +3VALW supply and the gate of the MOSFET Q44 (2N7002_SOT23).
- The gate of Q44 is also connected to the ON/OFF button (<33> ON/OFFBTN#) and the 51ON# signal (<47> 51ON#).
- The drain of Q44 is connected to the gate of the MOSFET D25 (DAN202U_SC70).
- The source of Q44 is connected to ground.
- The source of D25 is connected to ground.
- The drain of D25 is connected to the 51ON# signal (<47> 51ON#).
- A capacitor C727 (1000P_0402_50V7K) is connected between the 51ON# signal and ground.
- A diode D27 (RLZ220A_LL34) is connected between the 51ON# signal and ground.

Lid Switch

Change P/N : SN111000207

SW7

MPU-101-81_4P

2005/09/04

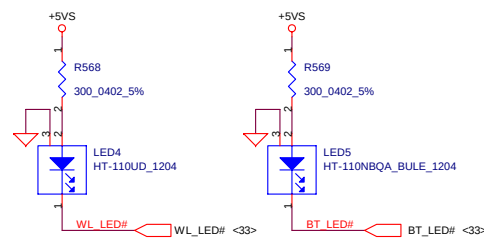
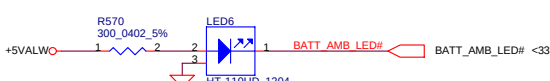
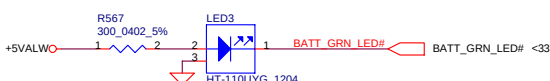
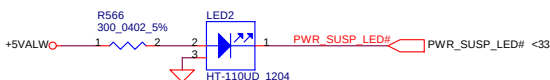
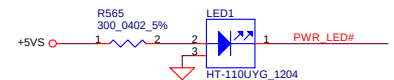
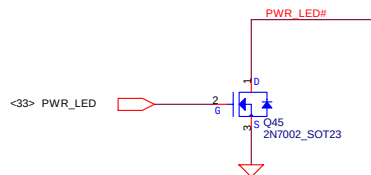
+3V3VW

R563
100K_0402_5%

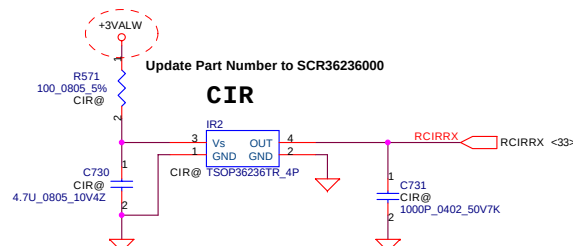
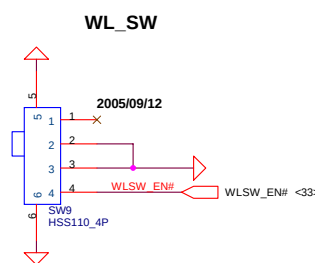
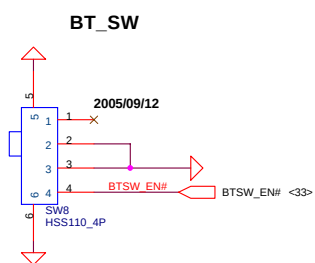
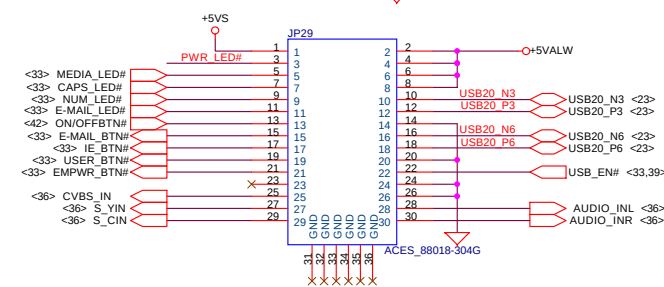
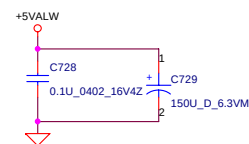
LID_SW# <3>

D26
@
PSOT24C_SOT23

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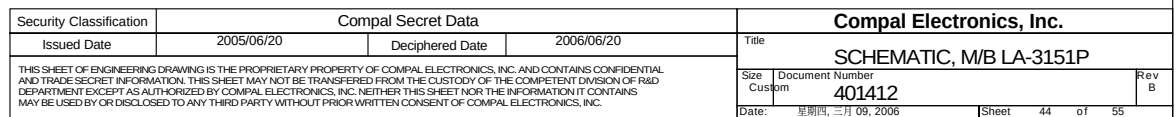


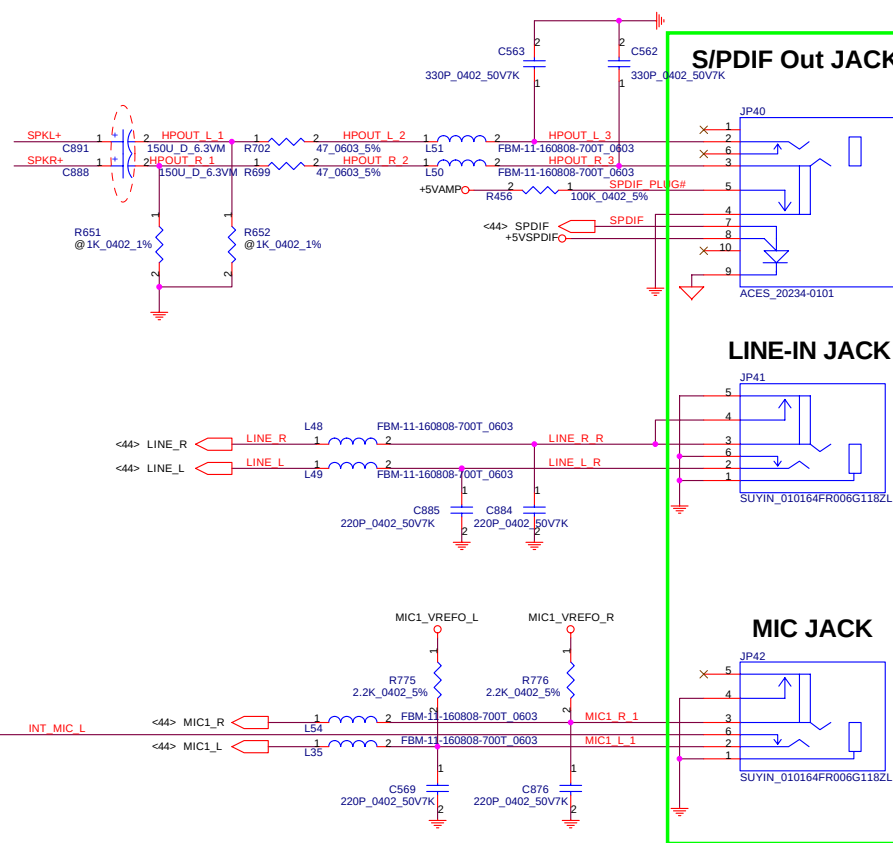
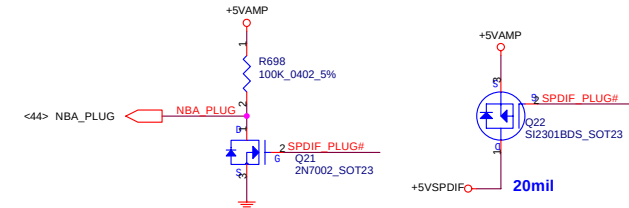
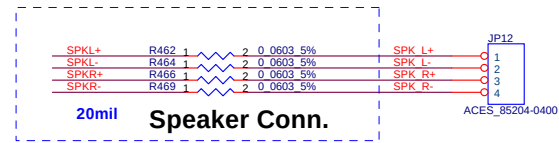
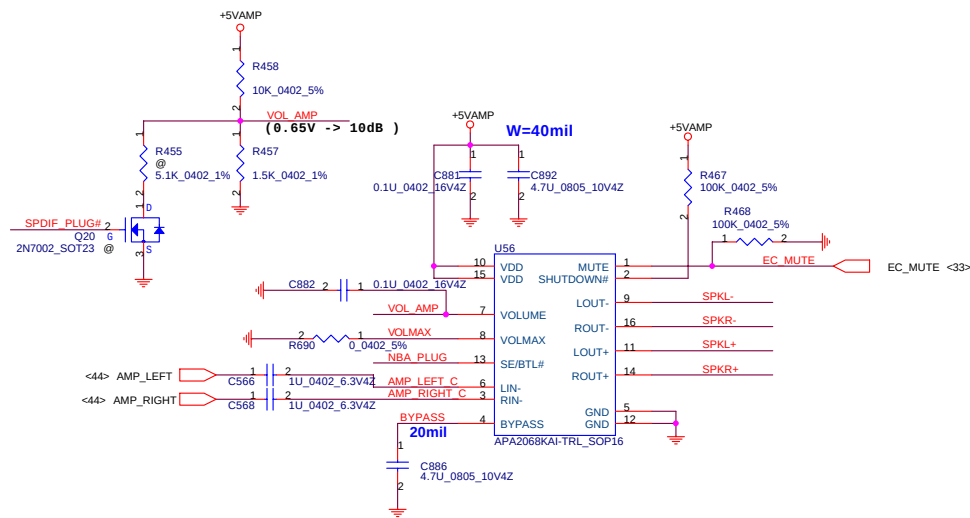
To LED/B Conn.



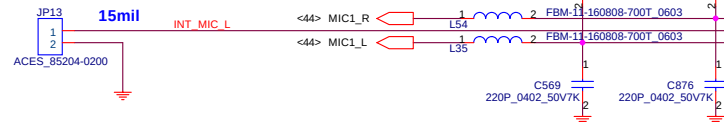
Geneva		Grapevine	
	KSO16	KSO17	
KSI0	VOL_UP	LEFT	
KSI1	RIGHT	VOL_DOWN	
KSI2	PLAY	ENTER	
KSI3	STOP		
KSI4	NEXT		
KSI5	REV		
KSI6		RECORD	

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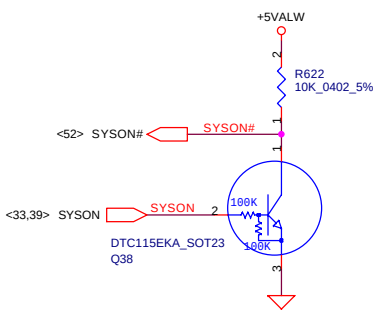
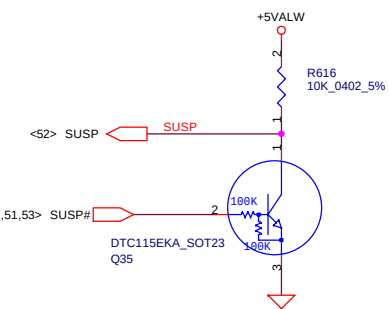
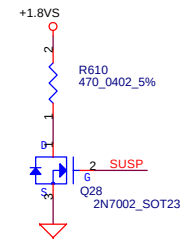
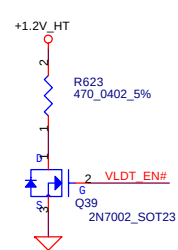
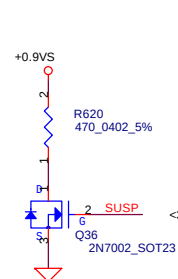
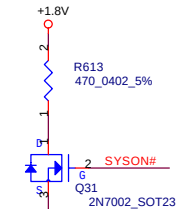
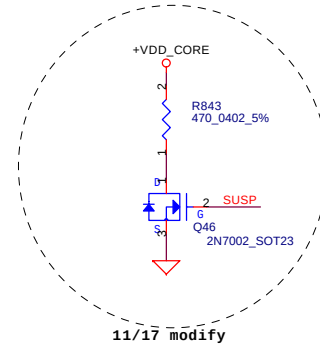
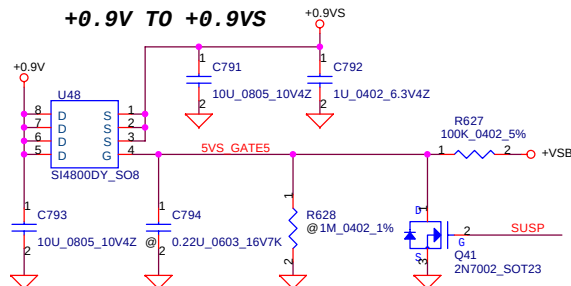
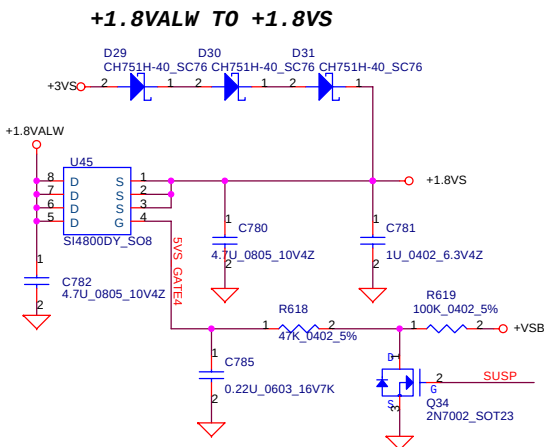
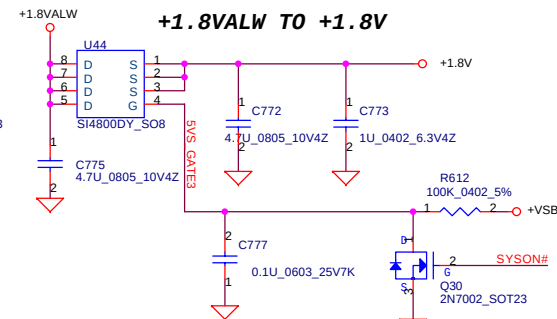
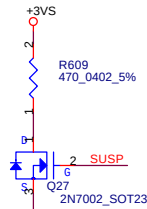
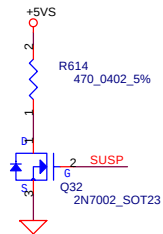
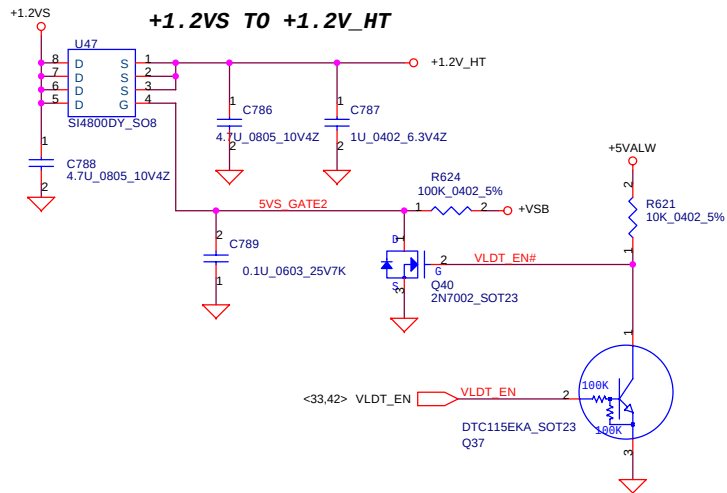
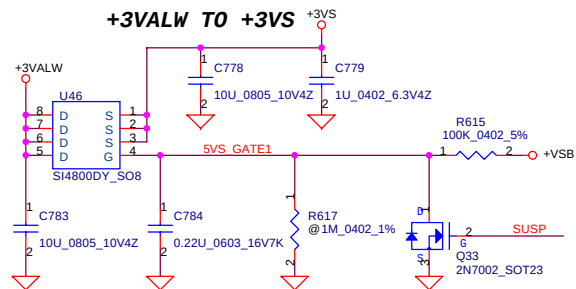
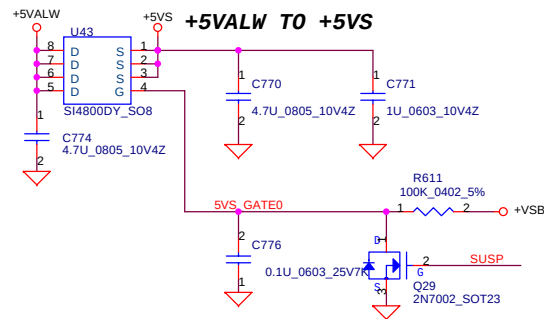




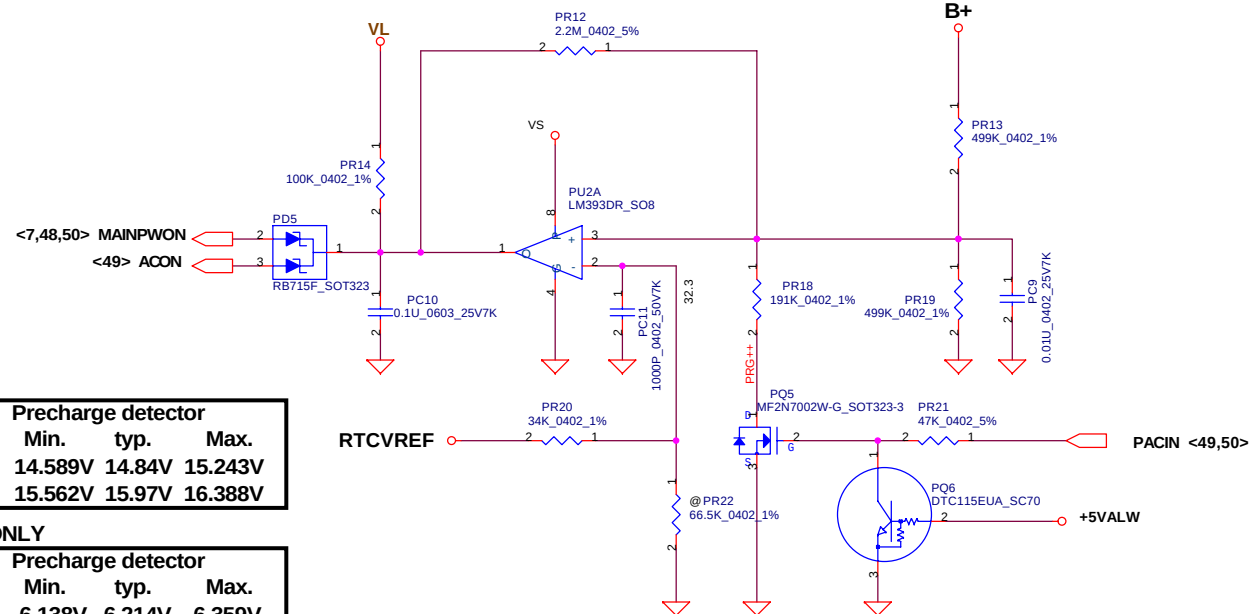
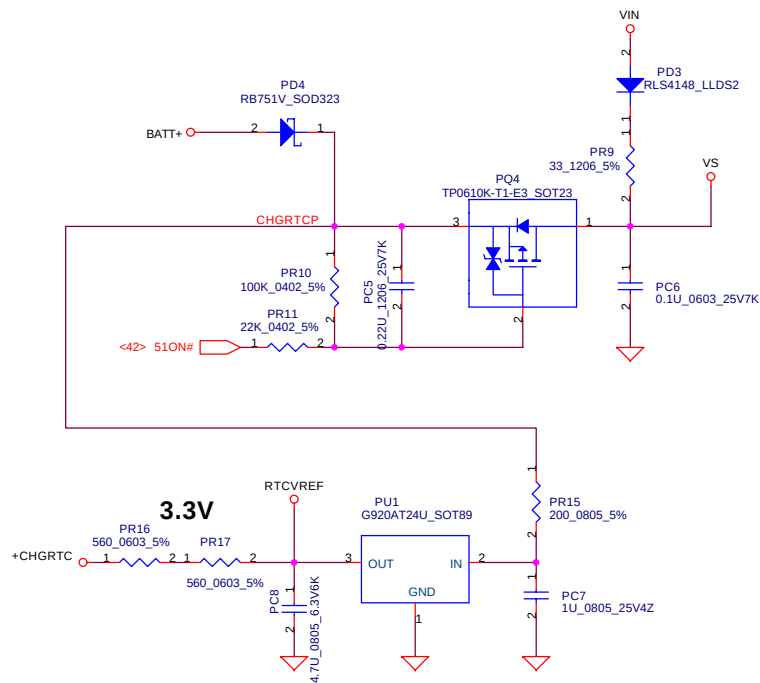
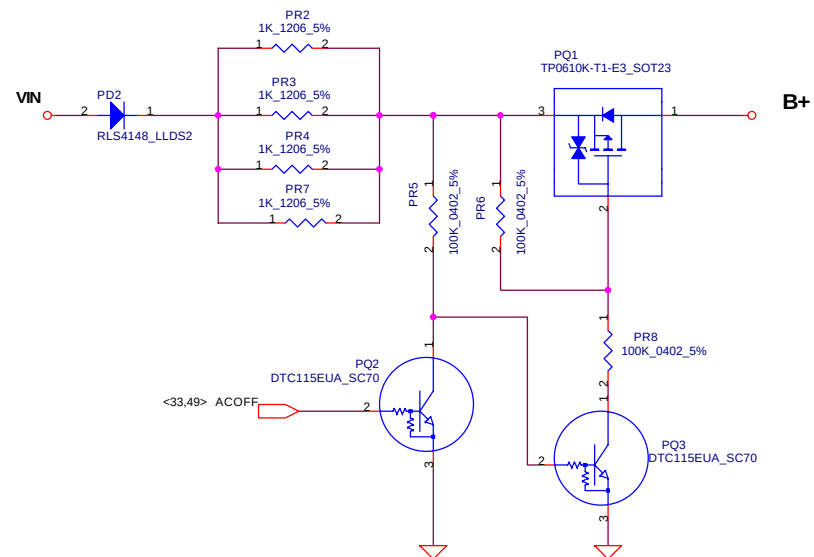
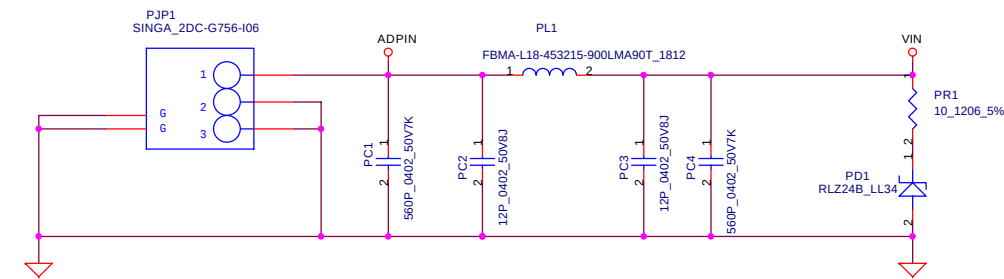
Int MIC Conn.



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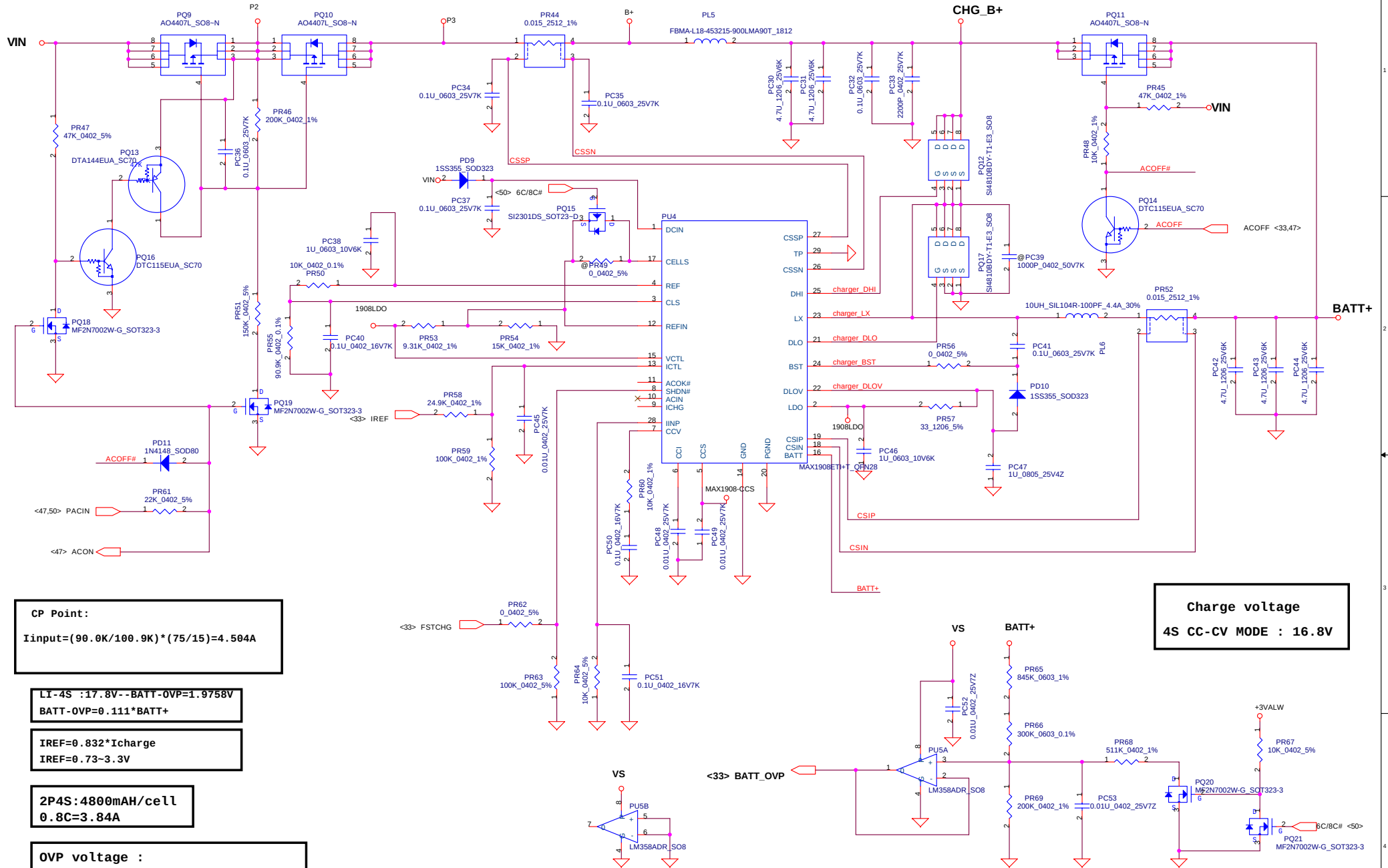
ACIN

	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

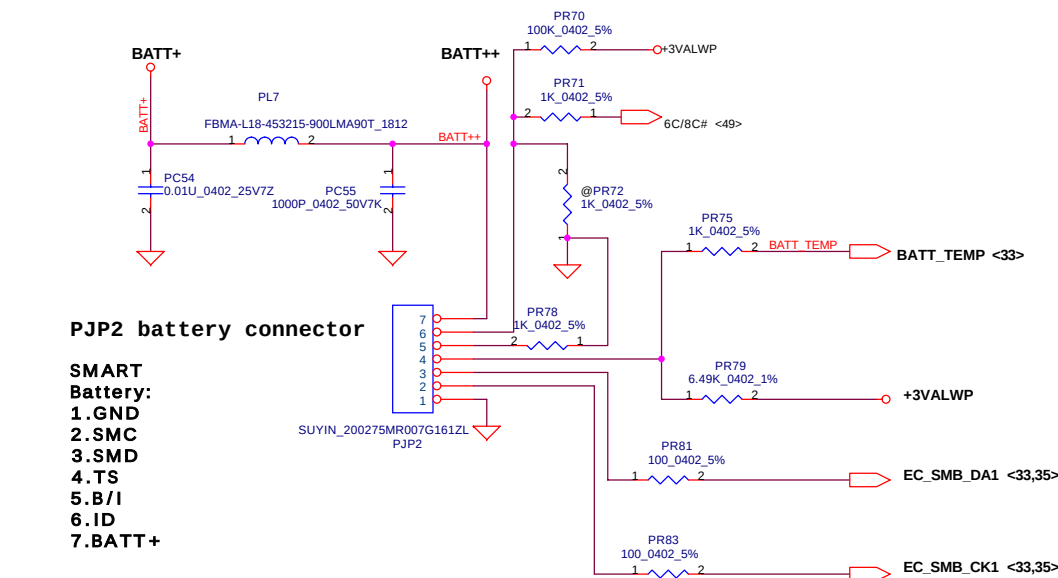
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I_{adp}=0~4.5A (90W)

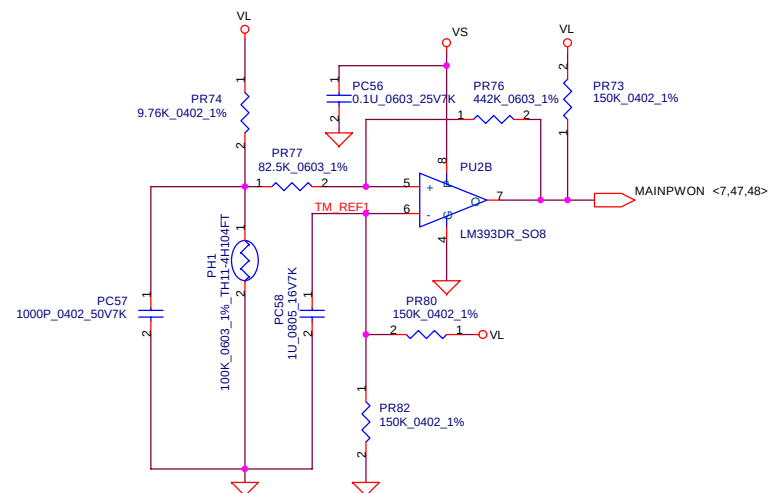
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PJP2 battery connector

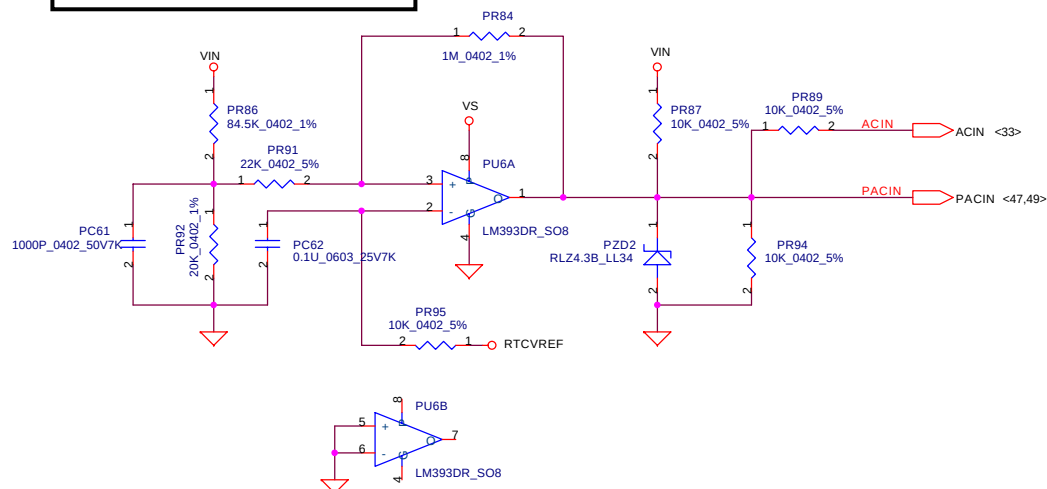
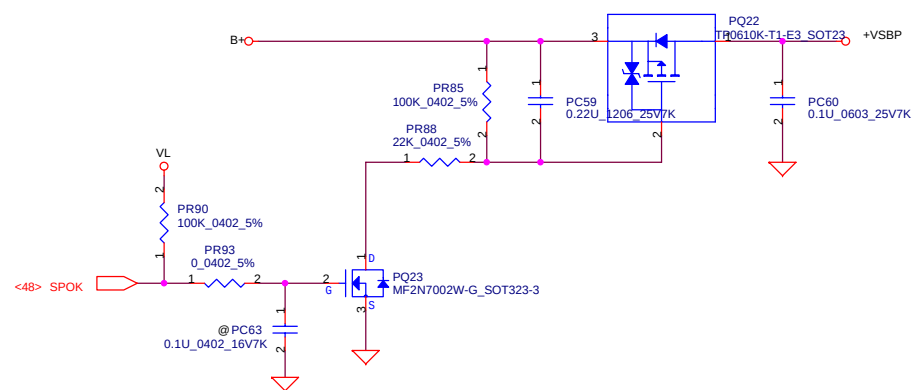
SMART Battery:
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+



PH1 under CPU bottom side :
 CPU thermal protection at 90 degree C
 Recovery at 70 degree C

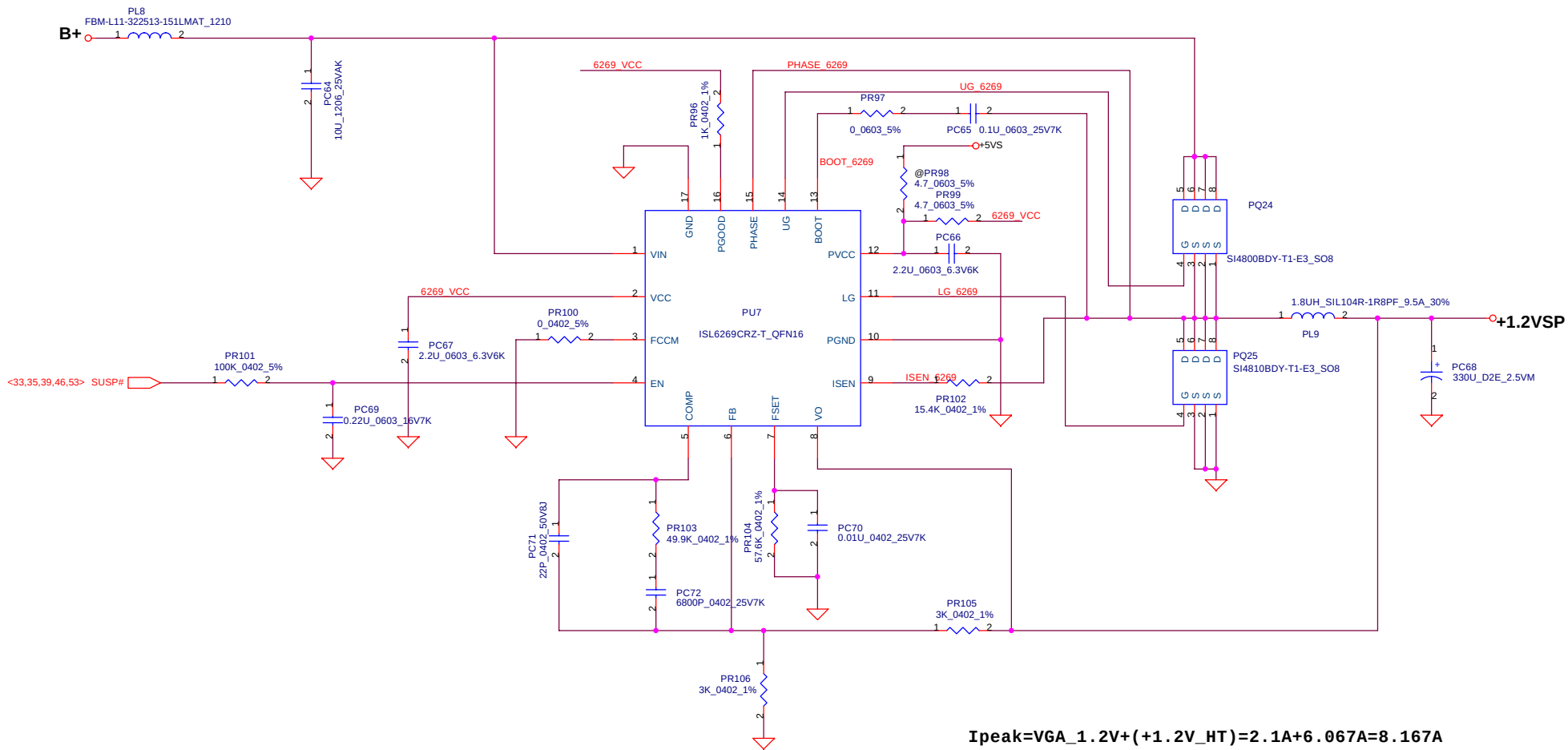


Vin Detector			
Min.	typ.	Max.	
H-->L	16.976V	17.257V	17.728V
L-->H	17.430V	17.901V	18.384V



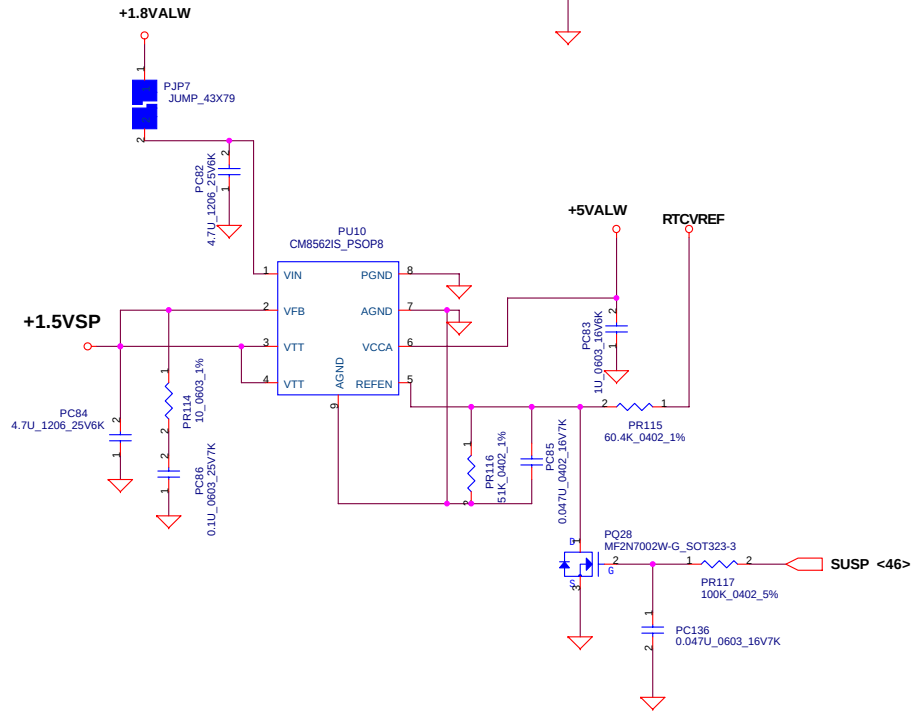
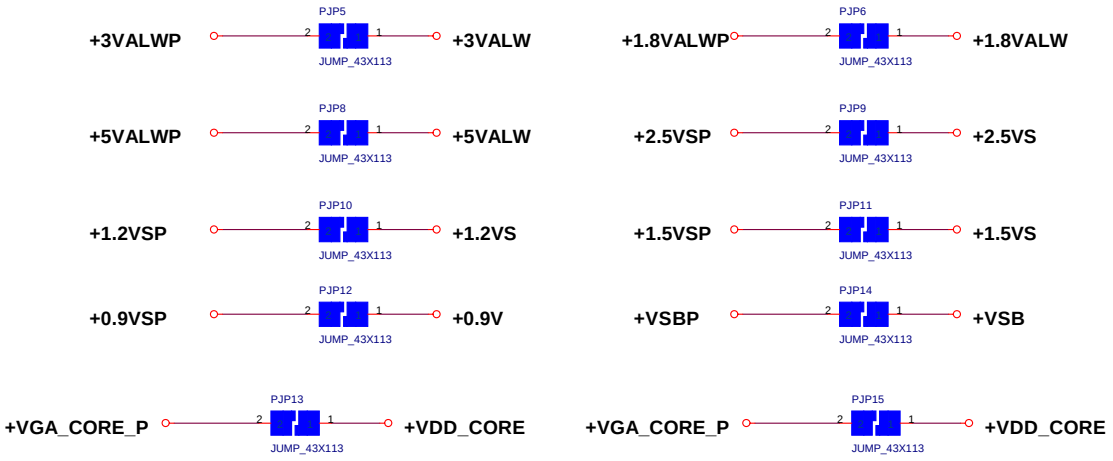
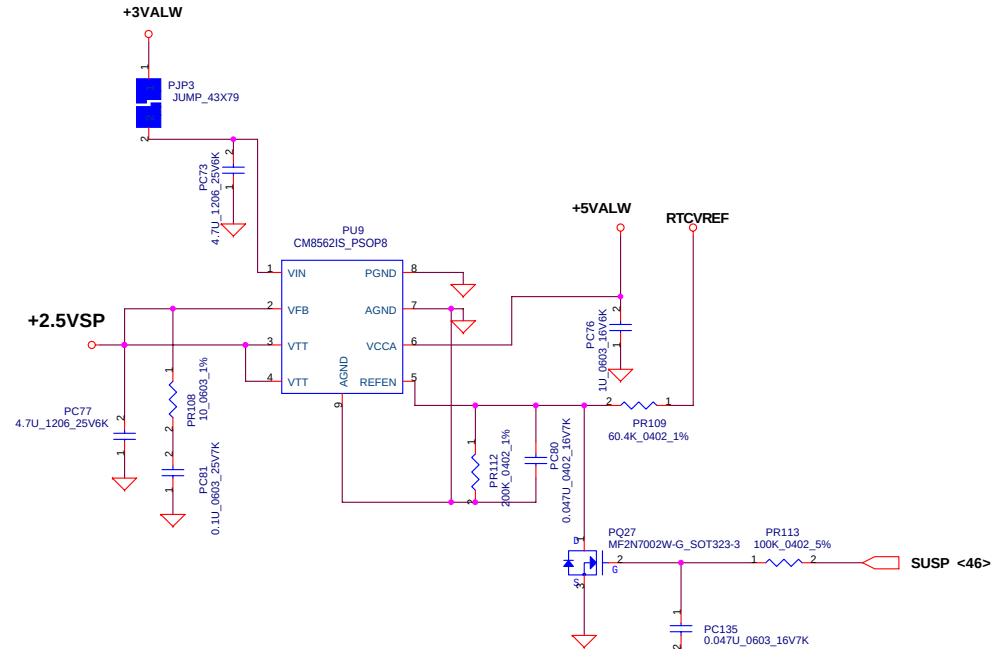
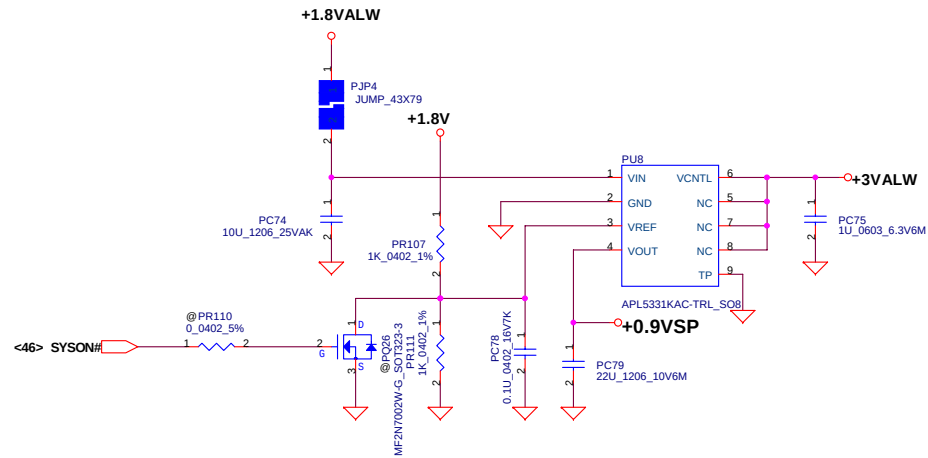
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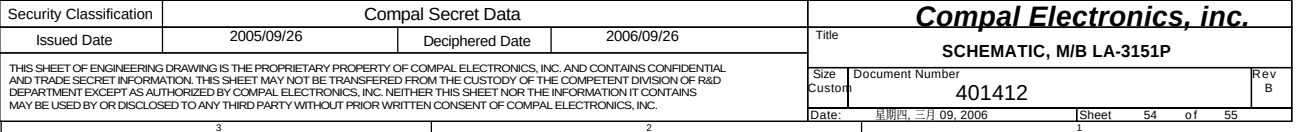


$I_{peak} = V_{GA_1.2V} + (+1.2V_{HT}) = 2.1A + 6.067A = 8.167A$
 $I_{max} = 5.7A$
 $I_{ocmin} = 9.23A$
 $I_{ocmax} = 19.23A$

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	VER	Phase
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2							
3							
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