

Compal Confidential

KALG1 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-03-02

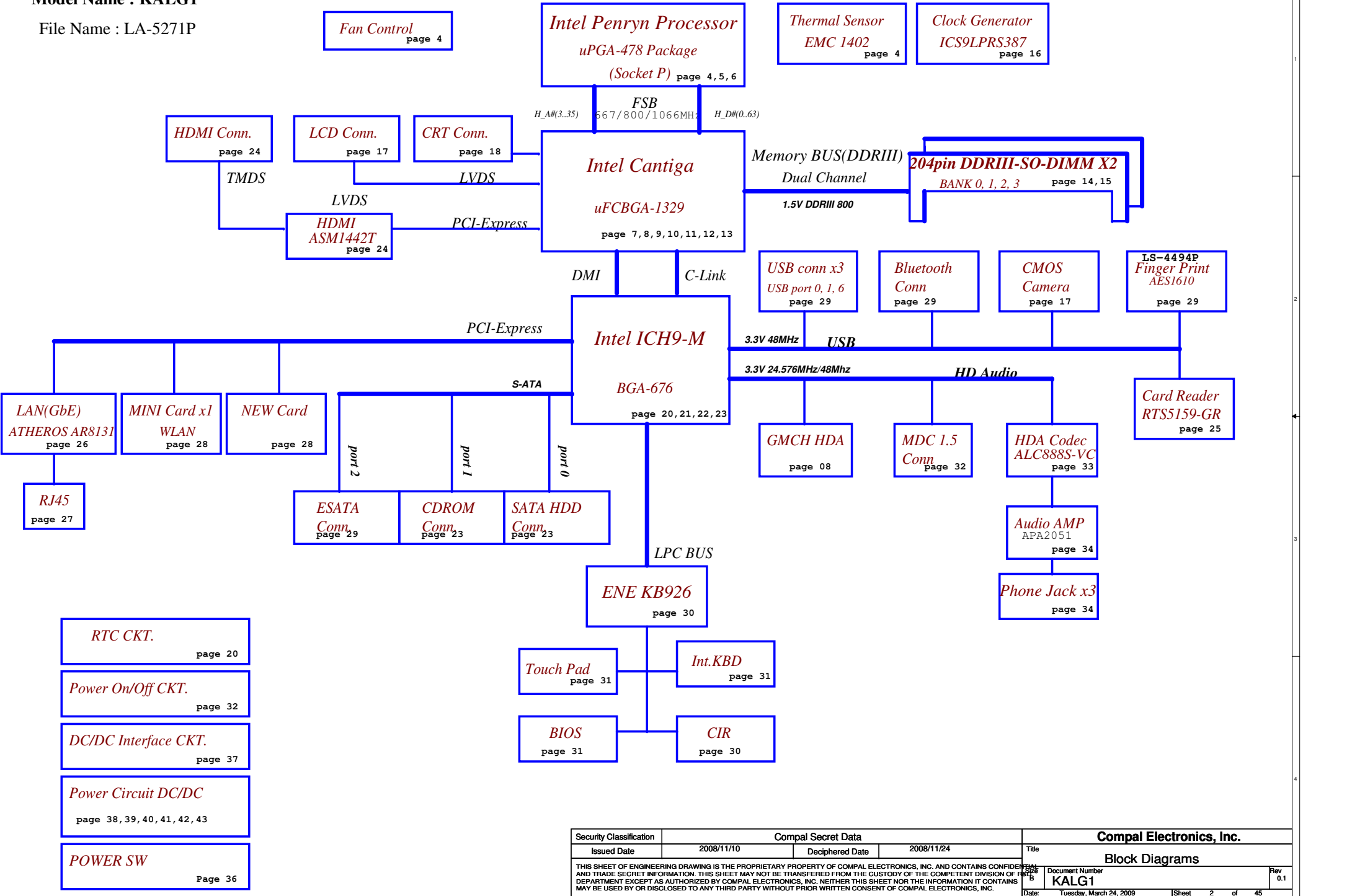
REV 02

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Model Name : KALG1

File Name : LA-5271P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75VS power rail for DDR3 terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for NB(LVDS)	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3V	3.3V power rail for SB	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail for SB	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 100X b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR3 DIMMA	1001 000Xb
DDR3 DIMMB	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1				
2				
3				
4				
5				
6				
7				

BOARD ID Table

Board ID	PCB Revision
0	PCB 08Y LA-5271P REV0 M/B
1	
2	
3	
4	
5	
6	
7	

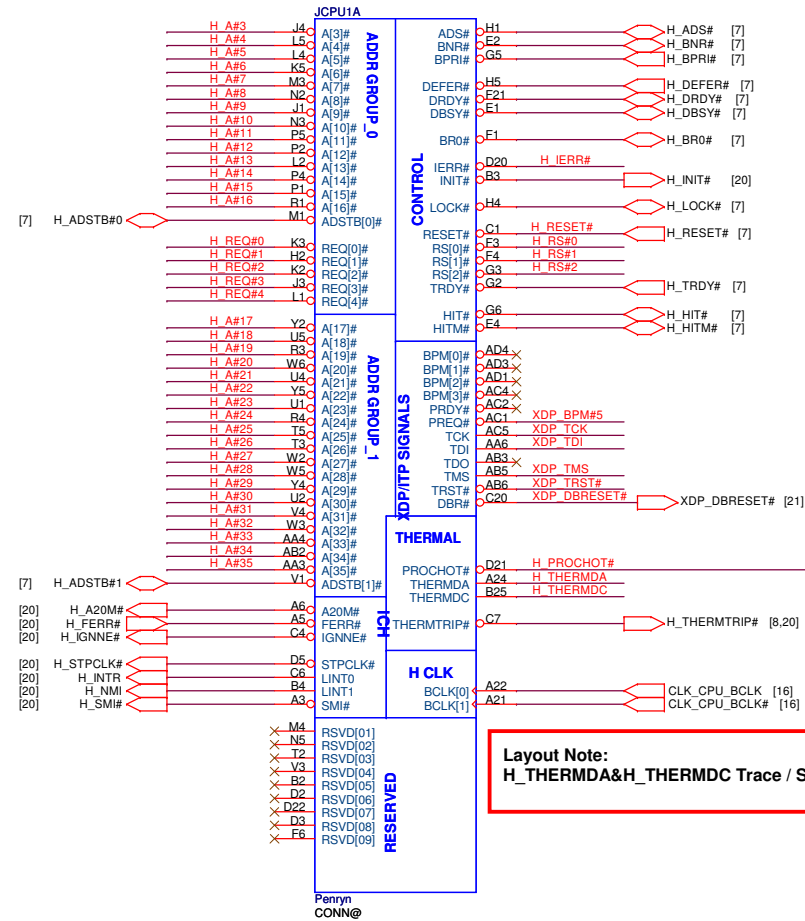
BTO Option Table

BTO Item	BOM Structure
GL40	GL40@
GM45	GM45@

BOM Configuration Table

Project	BOM Configuration
KALG1-GM45	GM45@/KALG1@/KAL90_G0_90+@
KALG1-GL40	GL40@/KALG1@/KAL90_G0_90+@

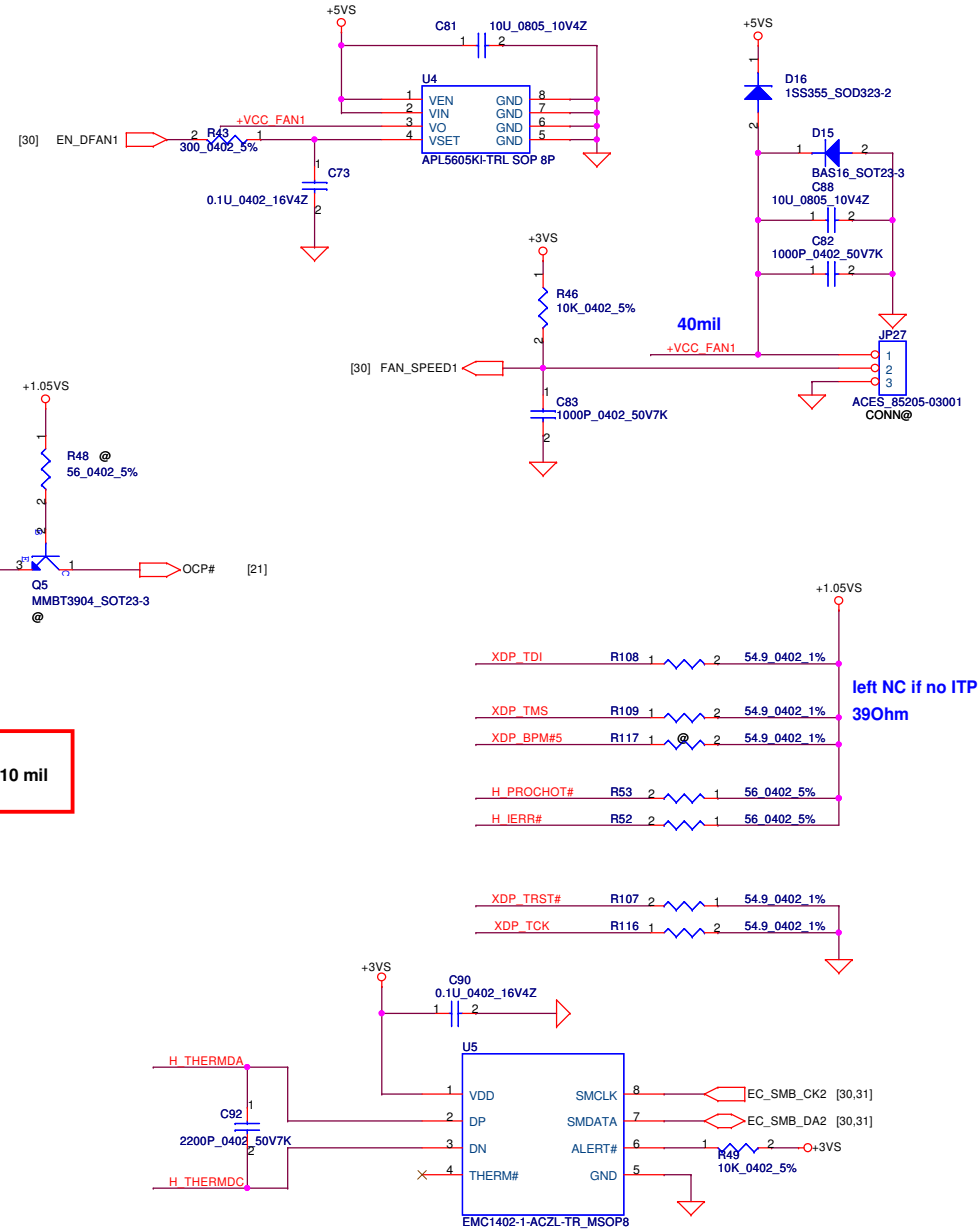
[7] H_A# [3..35]  H_A# [3..35]
 [7] H_REQ# [0..4]  H_REQ# [0..4]
 [7] H_RS# [0..2]  H_RS# [0..2]



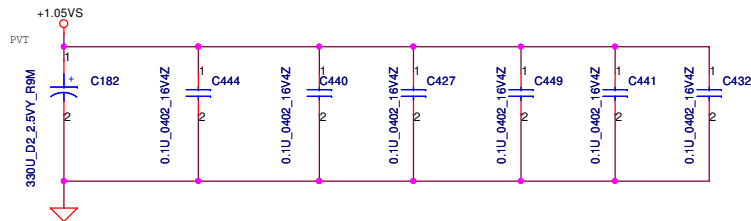
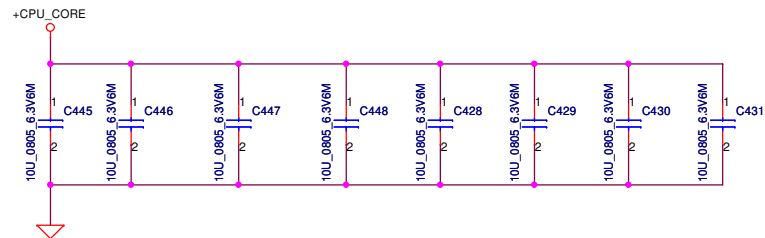
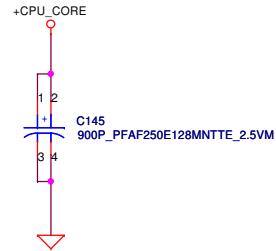
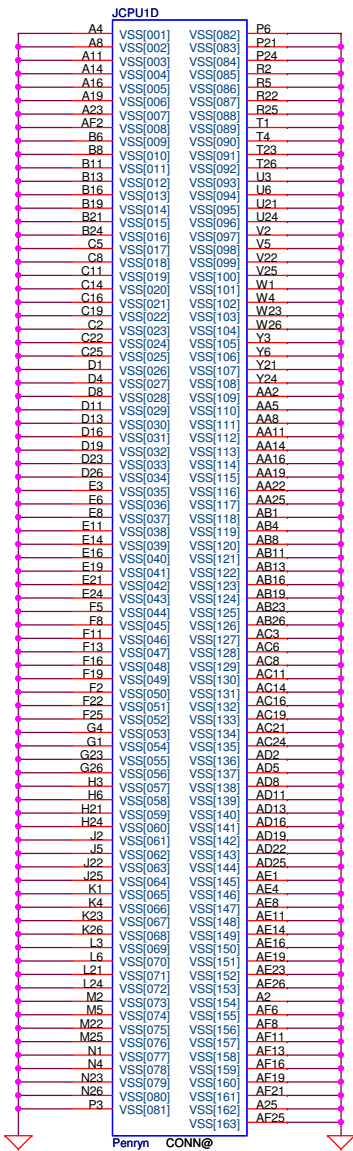
Layout Note:
 H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil

BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

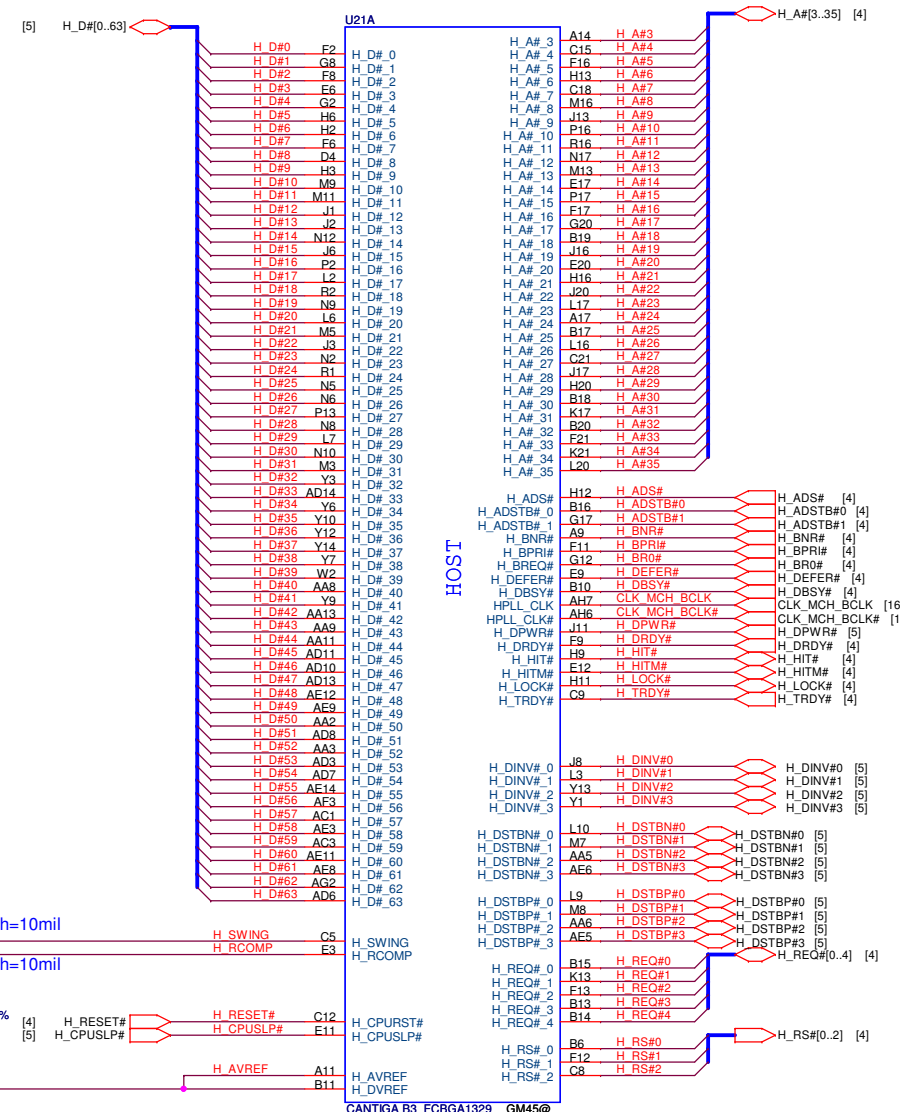
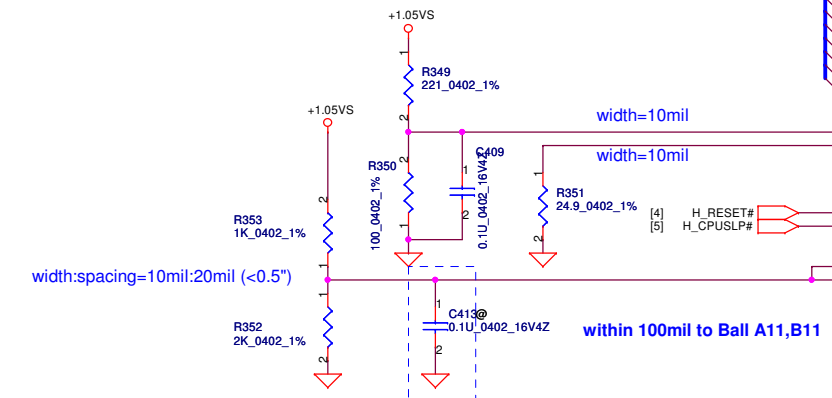
FAN1 Conn



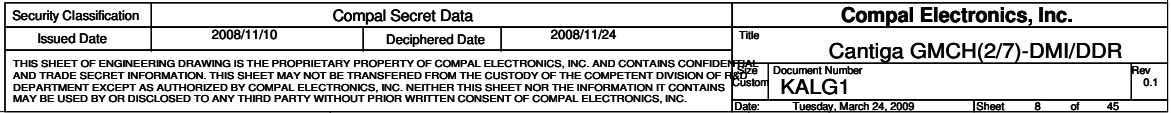
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[14] DDR_A_D[0..63]

U21D
DDR A D0 AJ38 SA_DQ_0
DDR A D1 AJ41 SA_DQ_1
DDR A D2 AJ43 SA_DQ_2
DDR A D3 AM58 SA_DQ_3
DDR A D4 AJ36 SA_DQ_4
DDR A D5 AJ40 SA_DQ_5
DDR A D6 AM44 SA_DQ_6
DDR A D7 AM42 SA_DQ_7
DDR A D8 AN53 SA_DQ_8
DDR A D9 AN44 SA_DQ_9
DDR A D10 AU40 SA_DQ_10
DDR A D11 AT38 SA_DQ_11
DDR A D12 AN41 SA_DQ_12
DDR A D13 AN39 SA_DQ_13
DDR A D14 AU44 SA_DQ_14
DDR A D15 AU42 SA_DQ_15
DDR A D16 AV39 SA_DQ_16
DDR A D17 AY44 SA_DQ_17
DDR A D18 BA40 SA_DQ_18
DDR A D19 BD43 SA_DQ_19
DDR A D20 AV41 SA_DQ_20
DDR A D21 AY43 SA_DQ_21
DDR A D22 BE41 SA_DQ_22
DDR A D23 BC40 SA_DQ_23
DDR A D24 AY37 SA_DQ_24
DDR A D25 BC38 SA_DQ_25
DDR A D26 AV37 SA_DQ_26
DDR A D27 AT36 SA_DQ_27
DDR A D28 AY38 SA_DQ_28
DDR A D29 BE38 SA_DQ_29
DDR A D30 AV36 SA_DQ_30
DDR A D31 AW38 SA_DQ_31
DDR A D32 BD13 SA_DQ_32
DDR A D33 AU11 SA_DQ_33
DDR A D34 BC11 SA_DQ_34
DDR A D35 BA12 SA_DQ_35
DDR A D36 AU13 SA_DQ_36
DDR A D37 AV13 SA_DQ_37
DDR A D38 BD12 SA_DQ_38
DDR A D39 BC12 SA_DQ_39
DDR A D40 BB9 SA_DQ_40
DDR A D41 BA9 SA_DQ_41
DDR A D42 AU10 SA_DQ_42
DDR A D43 AV9 SA_DQ_43
DDR A D44 BA11 SA_DQ_44
DDR A D45 BD9 SA_DQ_45
DDR A D46 AV8 SA_DQ_46
DDR A D47 BA6 SA_DQ_47
DDR A D48 AV5 SA_DQ_48
DDR A D49 AT9 SA_DQ_49
DDR A D50 AT9 SA_DQ_50
DDR A D51 AN8 SA_DQ_51
DDR A D52 AU6 SA_DQ_52
DDR A D53 AU6 SA_DQ_53
DDR A D54 AT5 SA_DQ_54
DDR A D55 AN10 SA_DQ_55
DDR A D56 AM11 SA_DQ_56
DDR A D57 AM5 SA_DQ_57
DDR A D58 AJ9 SA_DQ_58
DDR A D59 AJ8 SA_DQ_59
DDR A D60 AN12 SA_DQ_60
DDR A D61 AM13 SA_DQ_61
DDR A D62 AU11 SA_DQ_62
DDR A D63 AT12 SA_DQ_63

DDR SYSTEM MEMORY A

SA_RS_0
SA_RS_1
SA_RS_2
SA_RAS#
SA_CAS#
SA_WE#

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7

SA_DQS#_0
SA_DQS#_1
SA_DQS#_2
SA_DQS#_3
SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BD21 DDR A BS0
BG18 DDR A BS1
AT25 DDR A BS2

AM37 DDR A DM0
AT41 DDR A DM1
AY41 DDR A DM2
AU39 DDR A DM3
BB12 DDR A DM4
AY6 DDR A DM5
AT7 DDR A DM6
AJ5 DDR A DM7

AJ44 DDR A DQS0
AT44 DDR A DQS1
BA43 DDR A DQS2
BC37 DDR A DQS3
AW12 DDR A DQS4
BC4 DDR A DQS5
AU8 DDR A DQS6
AM7 DDR A DQS7

AJ43 DDR A DQS#0
AT43 DDR A DQS#1
BA44 DDR A DQS#2
BC37 DDR A DQS#3
AY12 DDR A DQS#4
BD8 DDR A DQS#5
AJ9 DDR A DQS#6
AN8 DDR A DQS#7

BA21 DDR A MA0
BC24 DDR A MA1
BD24 DDR A MA2
BH24 DDR A MA3
BC25 DDR A MA4
BA24 DDR A MA5
BD24 DDR A MA6
BC27 DDR A MA7
BF26 DDR A MA8
AW24 DDR A MA9
BC21 DDR A MA10
BC26 DDR A MA11
BH26 DDR A MA12
BH17 DDR A MA13
AY25 DDR A MA14

DDR_A_DM[0..7] [14]
DDR_A_DQS[0..7] [14]
DDR_A_DQS#[0..7] [14]
DDR_A_MA[0..14] [14]

[15] DDR_B_D[0..63]

U21E
DDR B D0 AK7 SB_DQ_0
DDR B D1 AH6 SB_DQ_1
DDR B D2 AP47 SB_DQ_2
DDR B D3 AP46 SB_DQ_3
DDR B D4 AJ46 SB_DQ_4
DDR B D5 AJ48 SB_DQ_5
DDR B D6 AM8 SB_DQ_6
DDR B D7 AP48 SB_DQ_7
DDR B D8 AU47 SB_DQ_8
DDR B D9 AU46 SB_DQ_9
DDR B D10 BA48 SB_DQ_10
DDR B D11 AY48 SB_DQ_11
DDR B D12 AT47 SB_DQ_12
DDR B D13 AB47 SB_DQ_13
DDR B D14 BA47 SB_DQ_14
DDR B D15 BC47 SB_DQ_15
DDR B D16 BC46 SB_DQ_16
DDR B D17 BC44 SB_DQ_17
DDR B D18 BC43 SB_DQ_18
DDR B D19 BE43 SB_DQ_19
DDR B D20 BE45 SB_DQ_20
DDR B D21 BC41 SB_DQ_21
DDR B D22 BE40 SB_DQ_22
DDR B D23 BE41 SB_DQ_23
DDR B D24 BC38 SB_DQ_24
DDR B D25 BF38 SB_DQ_25
DDR B D26 BH35 SB_DQ_26
DDR B D27 BC35 SB_DQ_27
DDR B D28 BH40 SB_DQ_28
DDR B D29 BC39 SB_DQ_29
DDR B D30 BC34 SB_DQ_30
DDR B D31 BH34 SB_DQ_31
DDR B D32 BH14 SB_DQ_32
DDR B D33 BC12 SB_DQ_33
DDR B D34 BH11 SB_DQ_34
DDR B D35 BC8 SB_DQ_35
DDR B D36 BH12 SB_DQ_36
DDR B D37 BE11 SB_DQ_37
DDR B D38 BF8 SB_DQ_38
DDR B D39 BG7 SB_DQ_39
DDR B D40 BC5 SB_DQ_40
DDR B D41 BC6 SB_DQ_41
DDR B D42 AY3 SB_DQ_42
DDR B D43 AY1 SB_DQ_43
DDR B D44 BF5 SB_DQ_44
DDR B D45 BF5 SB_DQ_45
DDR B D46 BA1 SB_DQ_46
DDR B D47 BC3 SB_DQ_47
DDR B D48 AV2 SB_DQ_48
DDR B D49 AU3 SB_DQ_49
DDR B D50 AF3 SB_DQ_50
DDR B D51 AN2 SB_DQ_51
DDR B D52 AV2 SB_DQ_52
DDR B D53 AN1 SB_DQ_53
DDR B D54 AF3 SB_DQ_54
DDR B D55 AN1 SB_DQ_55
DDR B D56 AL1 SB_DQ_56
DDR B D57 AL2 SB_DQ_57
DDR B D58 AH1 SB_DQ_58
DDR B D59 AH1 SB_DQ_59
DDR B D60 AM2 SB_DQ_60
DDR B D61 AM3 SB_DQ_61
DDR B D62 AH3 SB_DQ_62
DDR B D63 AJ3 SB_DQ_63

DDR SYSTEM MEMORY B

SB_RS_0
SB_RS_1
SB_RS_2
SB_RAS#
SB_CAS#
SB_WE#

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
SB_DQS_5
SB_DQS_6
SB_DQS_7

SB_DQS#_0
SB_DQS#_1
SB_DQS#_2
SB_DQS#_3
SB_DQS#_4
SB_DQS#_5
SB_DQS#_6
SB_DQS#_7

SB_MA_0
SB_MA_1
SB_MA_2
SB_MA_3
SB_MA_4
SB_MA_5
SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

BC16 DDR B BS0
BB17 DDR B BS1
BB33 DDR B BS2

AU17 DDR B RAS#
BG16 DDR B CAS#
BF14 DDR B WE#

AJ47 DDR B DQS0
AY46 DDR B DQS1
BC41 DDR B DQS2
BC37 DDR B DQS3
BA49 DDR B DQS4
BB2 DDR B DQS5
AU1 DDR B DQS6
AN6 DDR B DQS7

AJ46 DDR B DQS#0
AY47 DDR B DQS#1
BH41 DDR B DQS#2
BH47 DDR B DQS#3
BG9 DDR B DQS#4
BC2 DDR B DQS#5
AT2 DDR B DQS#6
AN5 DDR B DQS#7

AV17 DDR B MA0
BA25 DDR B MA1
BC25 DDR B MA2
AU25 DDR B MA3
BB26 DDR B MA4
AU28 DDR B MA5
AW28 DDR B MA6
AT33 DDR B MA7
BD33 DDR B MA8
BB16 DDR B MA9
AW33 DDR B MA10
AY33 DDR B MA11
BH15 DDR B MA12
AU33 DDR B MA13
AU33 DDR B MA14

DDR_B_DM[0..7] [15]
DDR_B_DQS[0..7] [15]
DDR_B_DQS#[0..7] [15]
DDR_B_MA[0..14] [15]

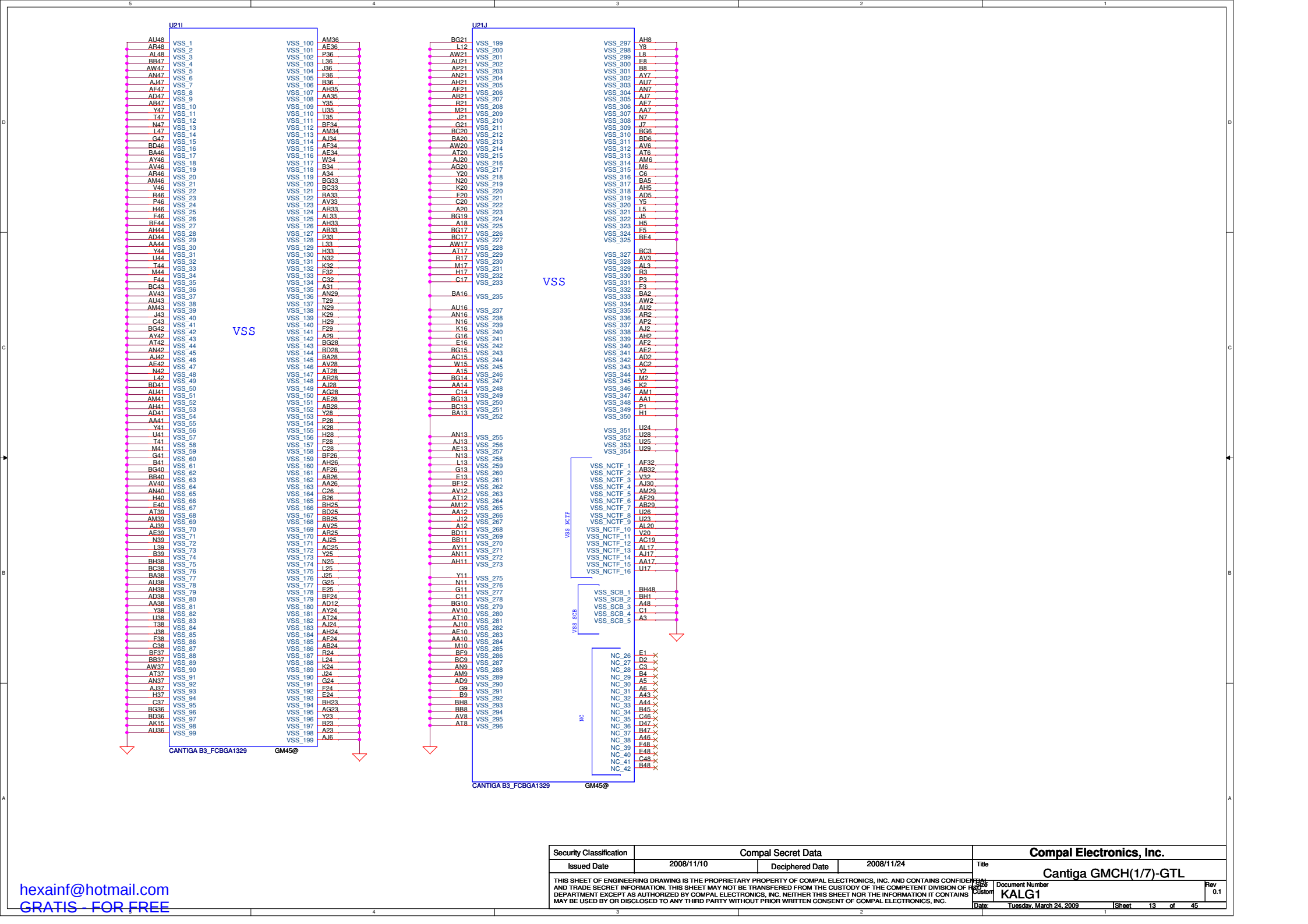
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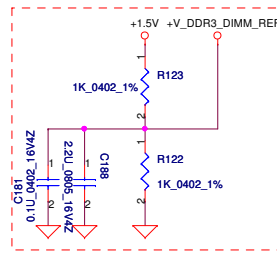
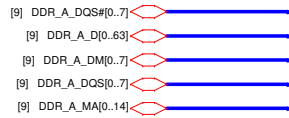
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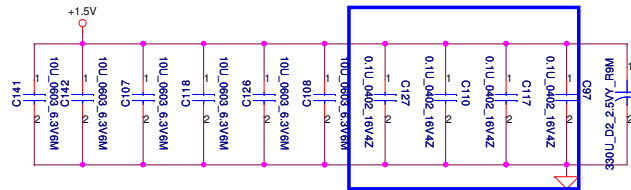
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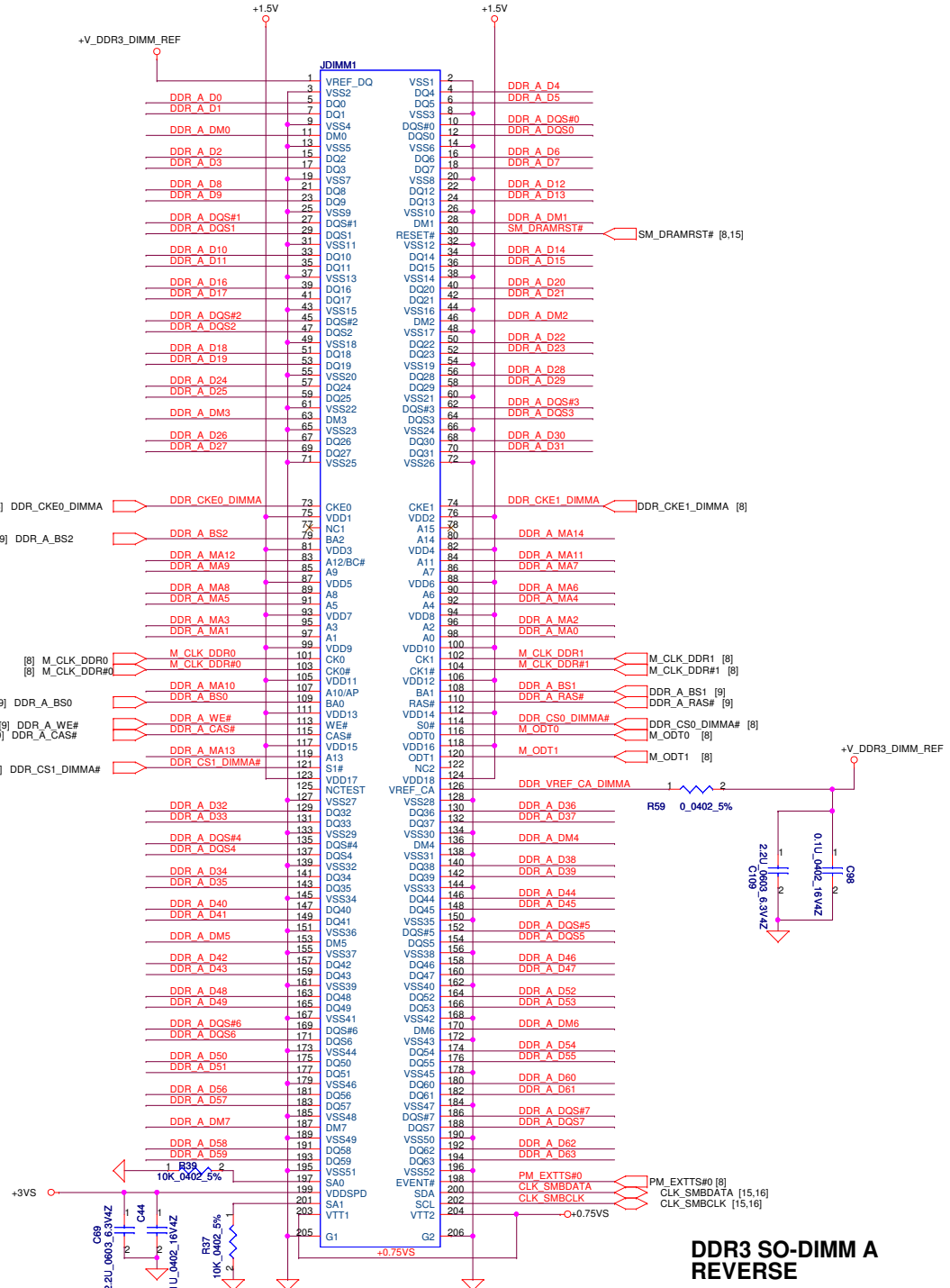
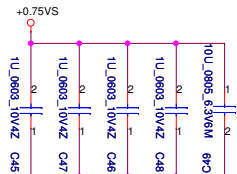


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command
and Control signals of DIMM

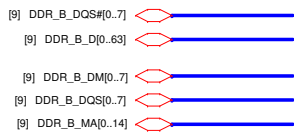


Layout Note:
Place near JP4.203 & JP4.204



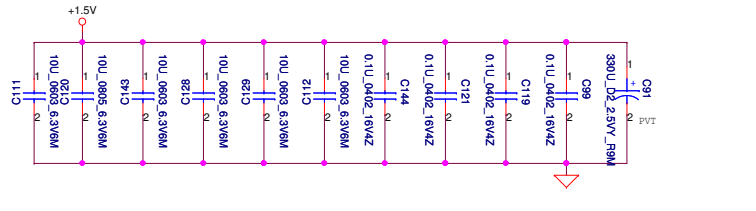
DDR3 SO-DIMM A REVERSE

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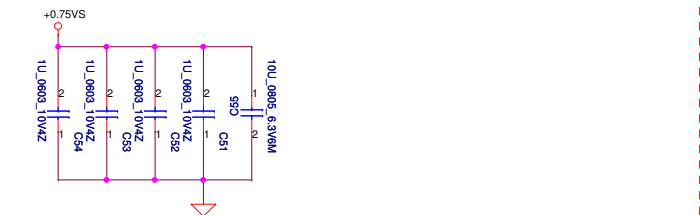


Layout Note:
Place near JP5

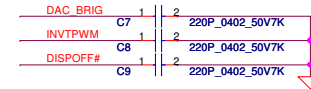
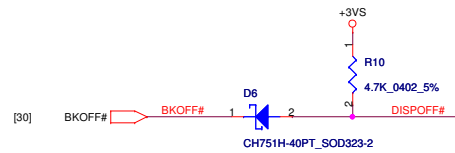
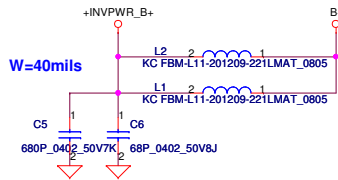
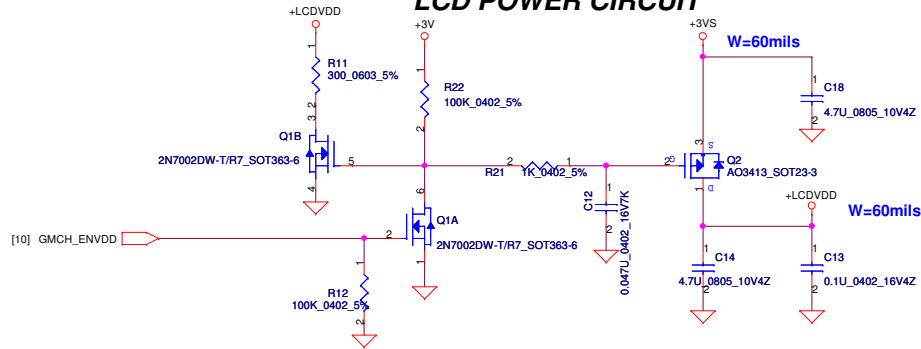
Layout Note: Place these 4 Caps near Command
and Control signals of DIMMB



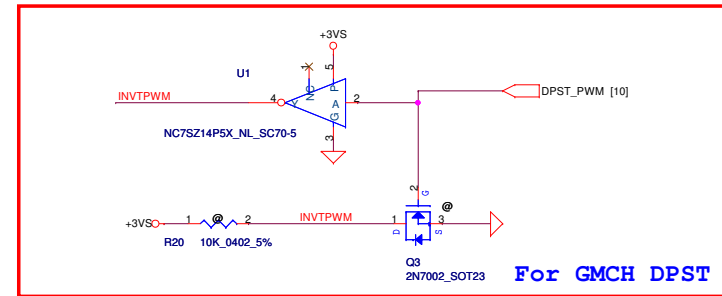
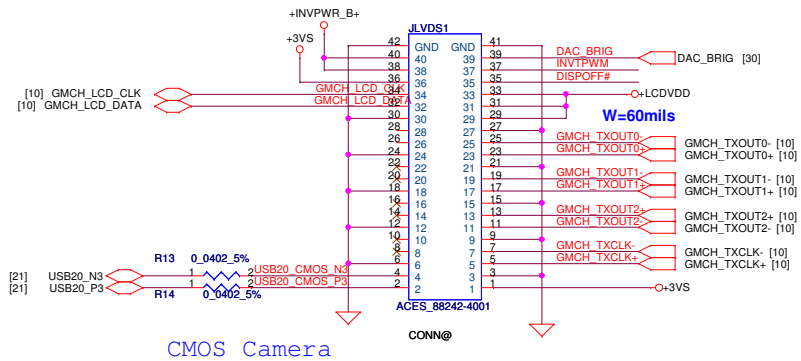
Layout Note:
Place near JP5.203 & JP5.204



LCD POWER CIRCUIT

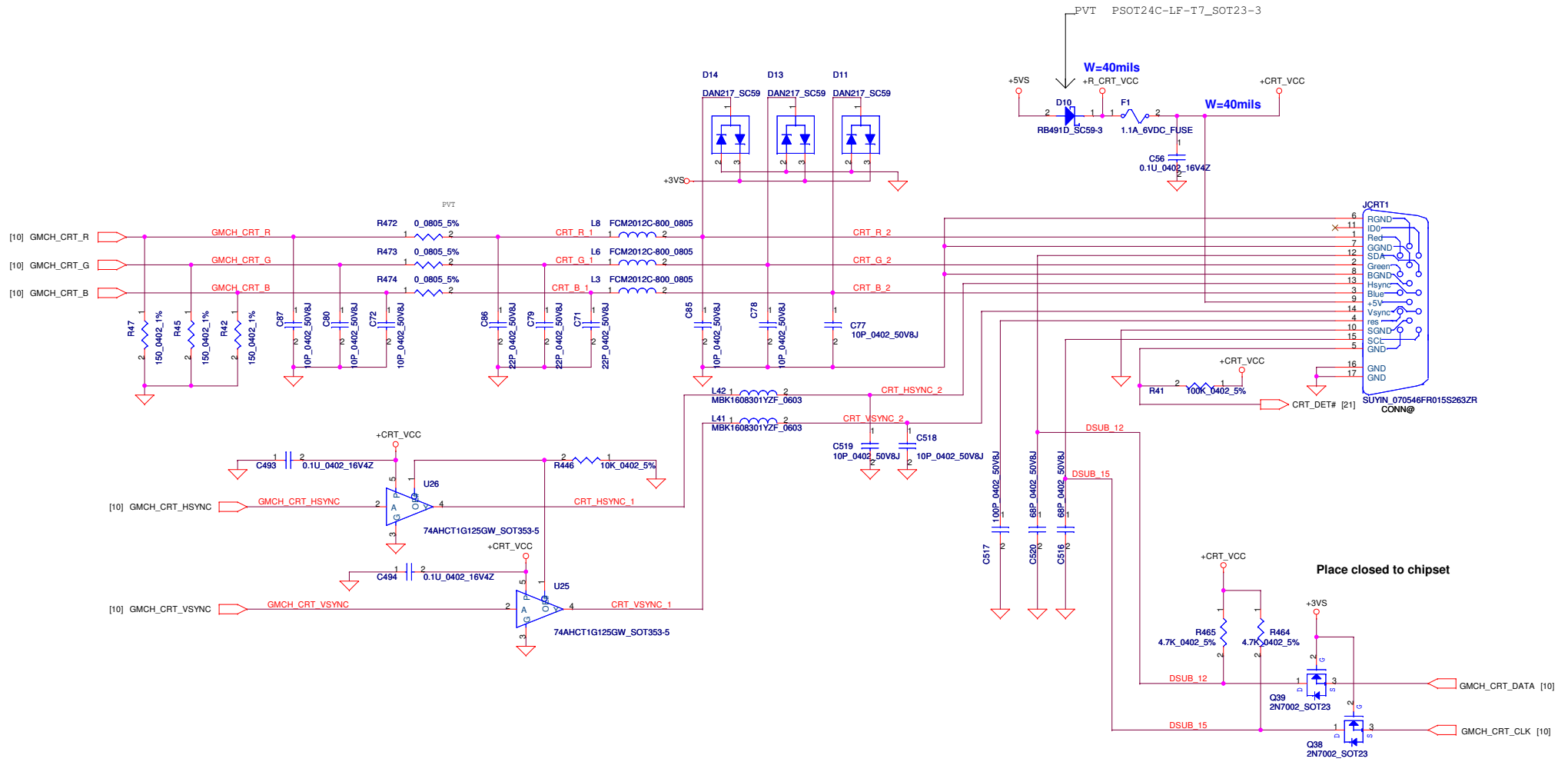


LCD/PANEL BD. Conn.

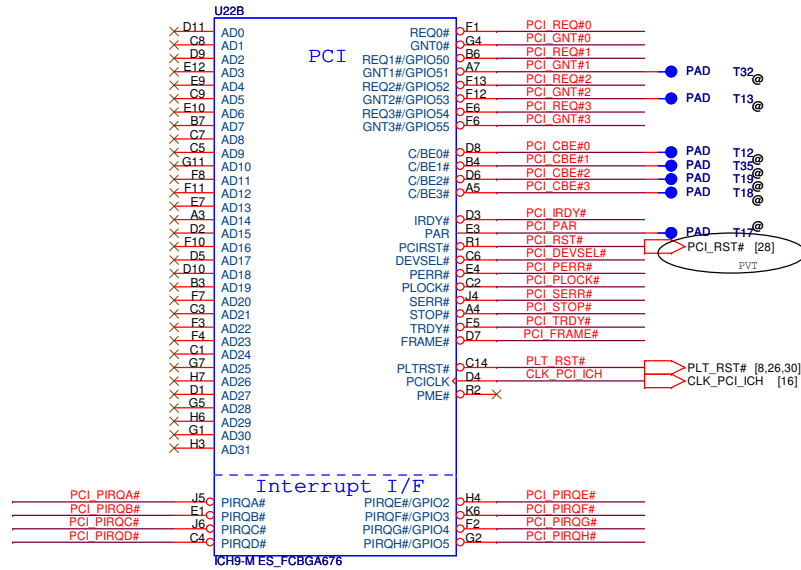
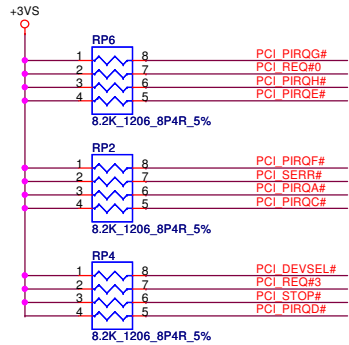
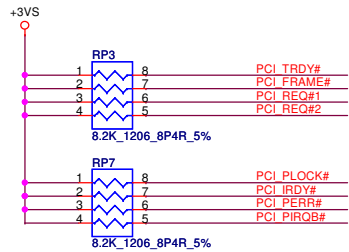


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CRT Connector

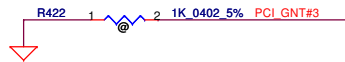


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								KALG1		0.1	

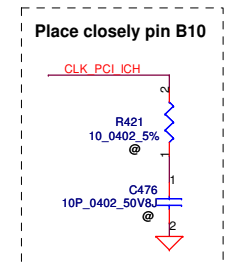
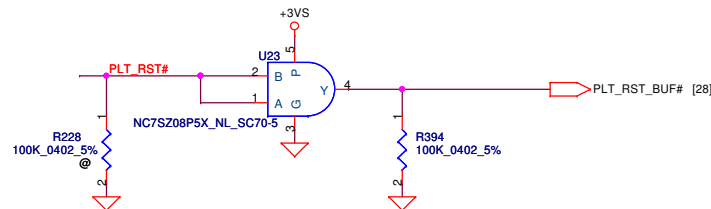
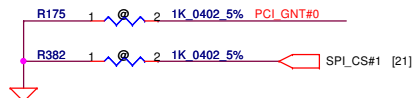


DMI for ESI-compatible operation
PCI_GNT#1 Low= DMI for ESI-compatible operation
 High= Default* (Internal pull-up)

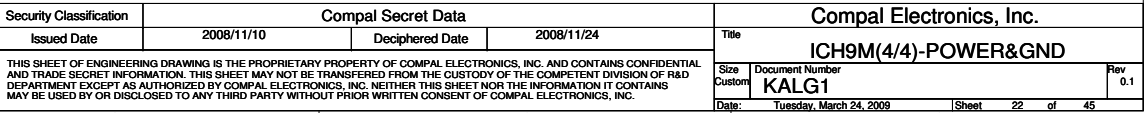
A16 Swap Override Strap
PCI_GNT#3 Low= A16 swap override Enable
 High= Default*



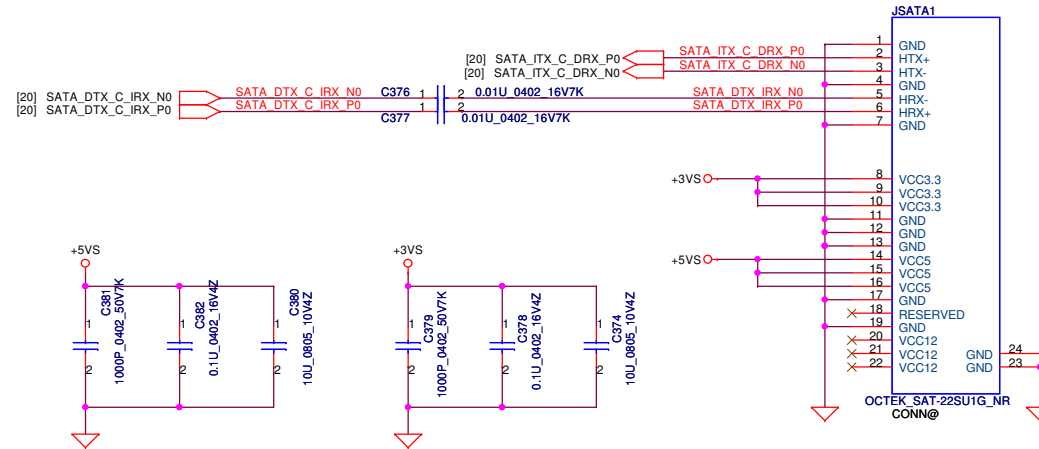
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



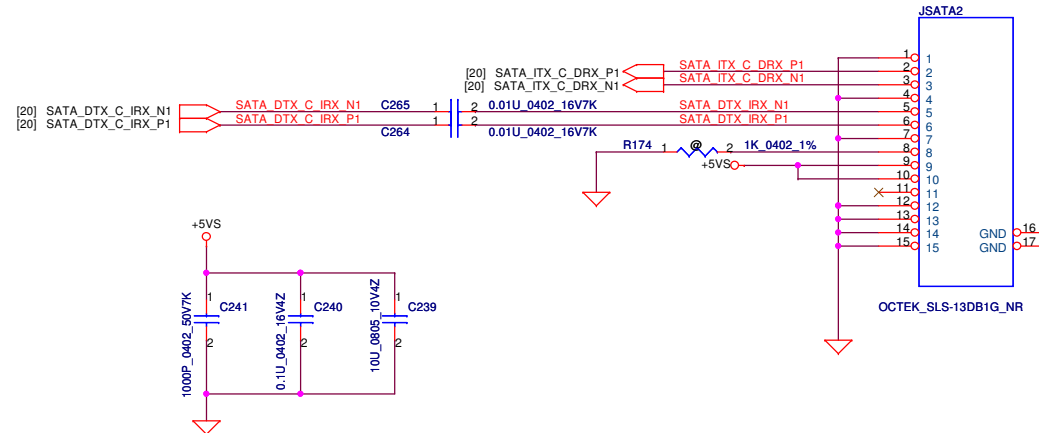
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Size		Document Number		Rev	
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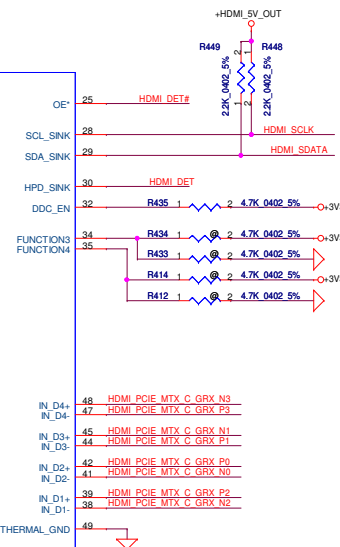
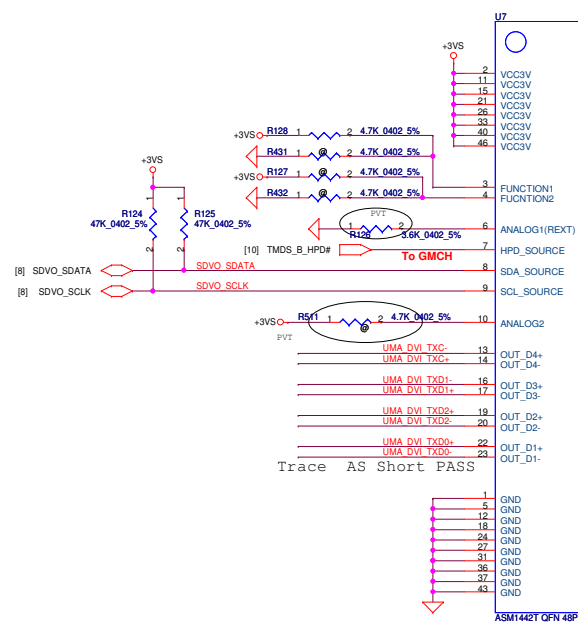
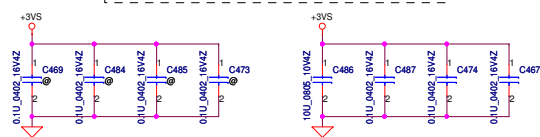
SATA HDD Conn.



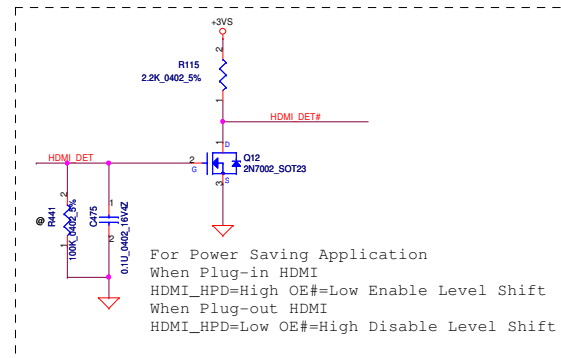
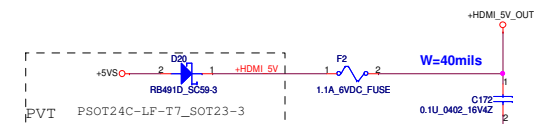
SATA ODD Conn.



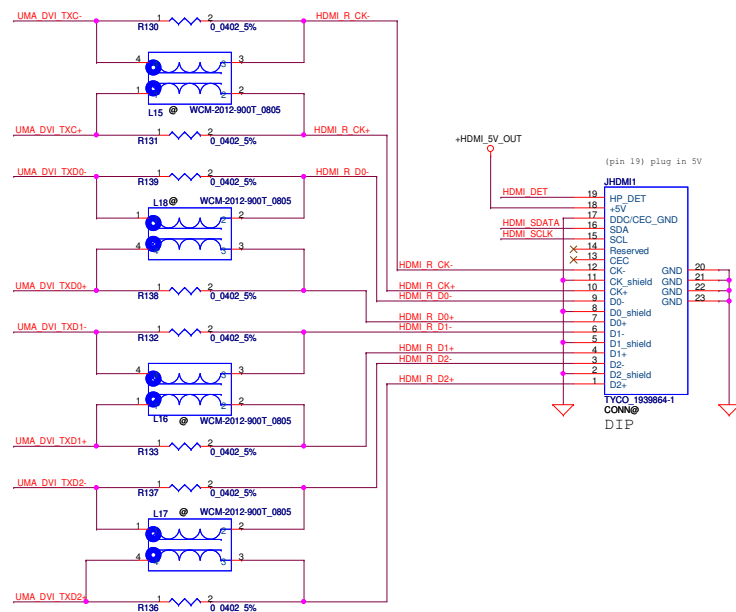
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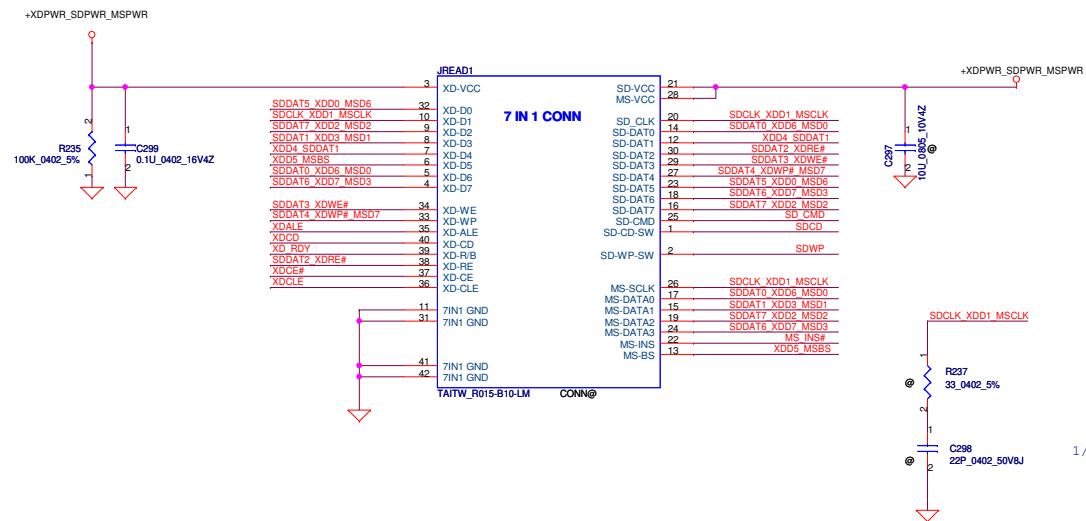
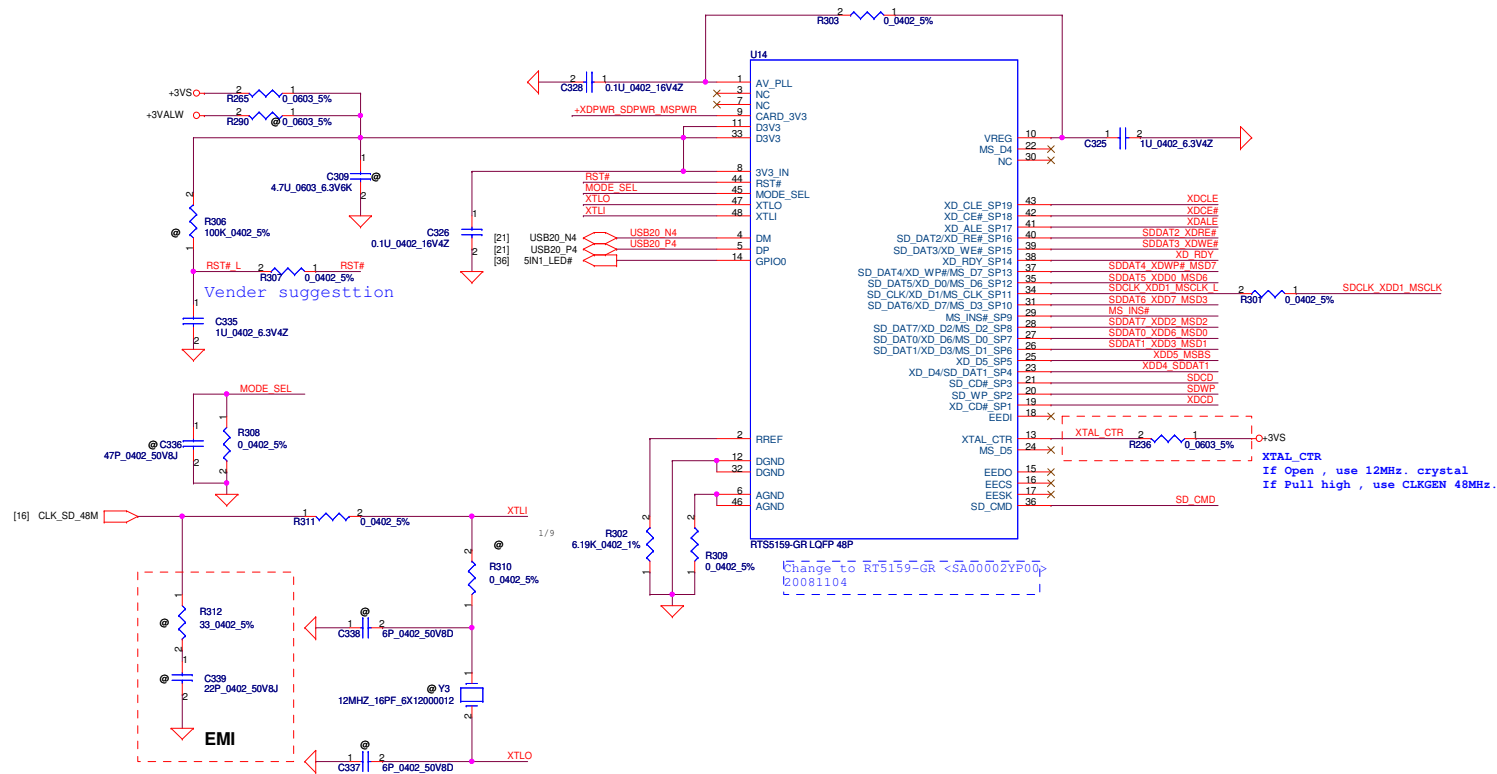
20071031:
Add U1. 49 (THERMAL_GND) to GND Plane



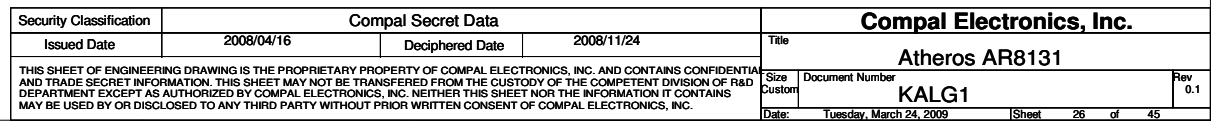
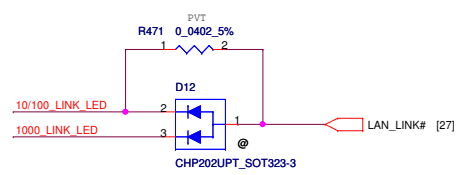
HDMI_PCIE_MTX_C_GRX_N[0..3]	HDMI_PCIE_MTX_C_GRX_N[0..3]	[10]
HDMI_PCIE_MTX_C_GRX_P[0..3]	HDMI_PCIE_MTX_C_GRX_P[0..3]	[10]

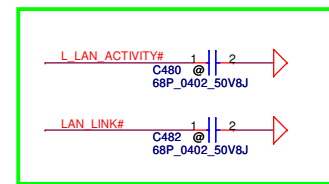
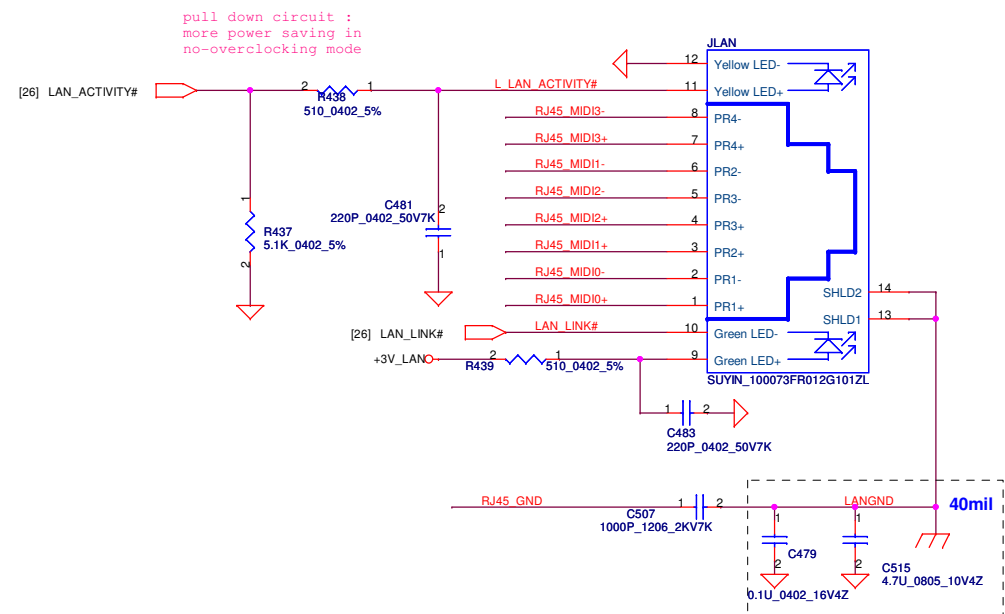
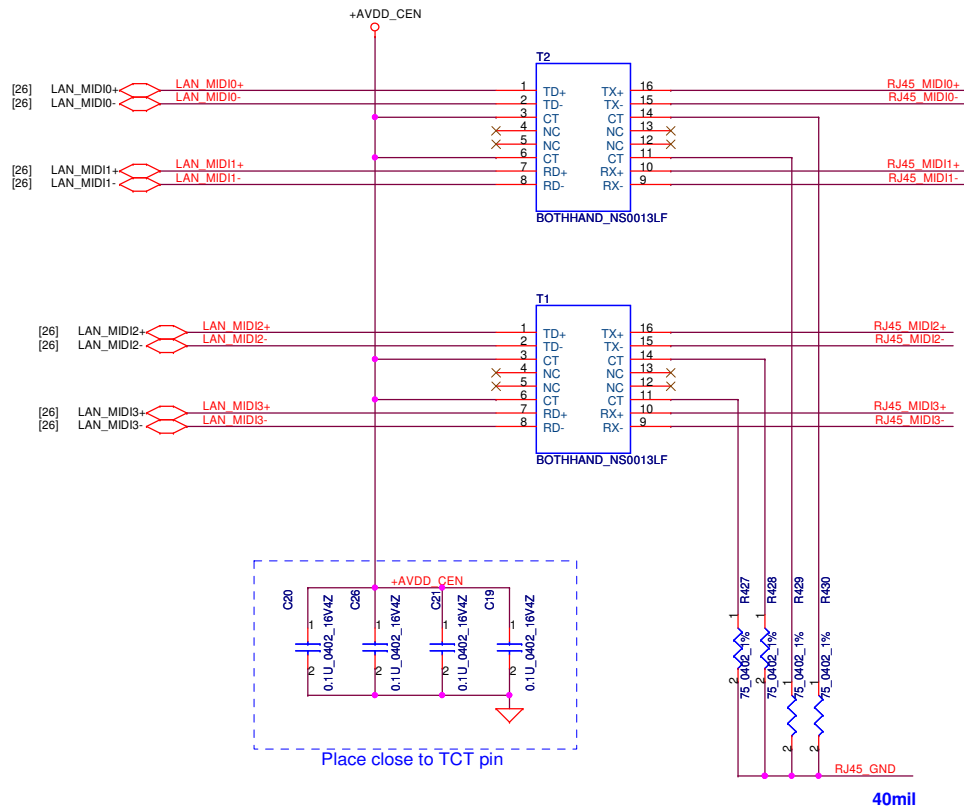


Intel Cantiga TMDs Pin Definition	
TMDs_B_CLK	PEG_TXP_3
TMDs_B_CLK#	PEG_TXN_3
TMDs_B_DATA0	PEG_TXP_2
TMDs_B_DATA0#	PEG_TXN_2
TMDs_B_DATA1	PEG_TXP_1
TMDs_B_DATA1#	PEG_TXN_1
TMDs_B_DATA2	PEG_TXP_0
TMDs_B_DATA2#	PEG_TXN_0
TMDs_B_HPD#	PEG_RXP_3



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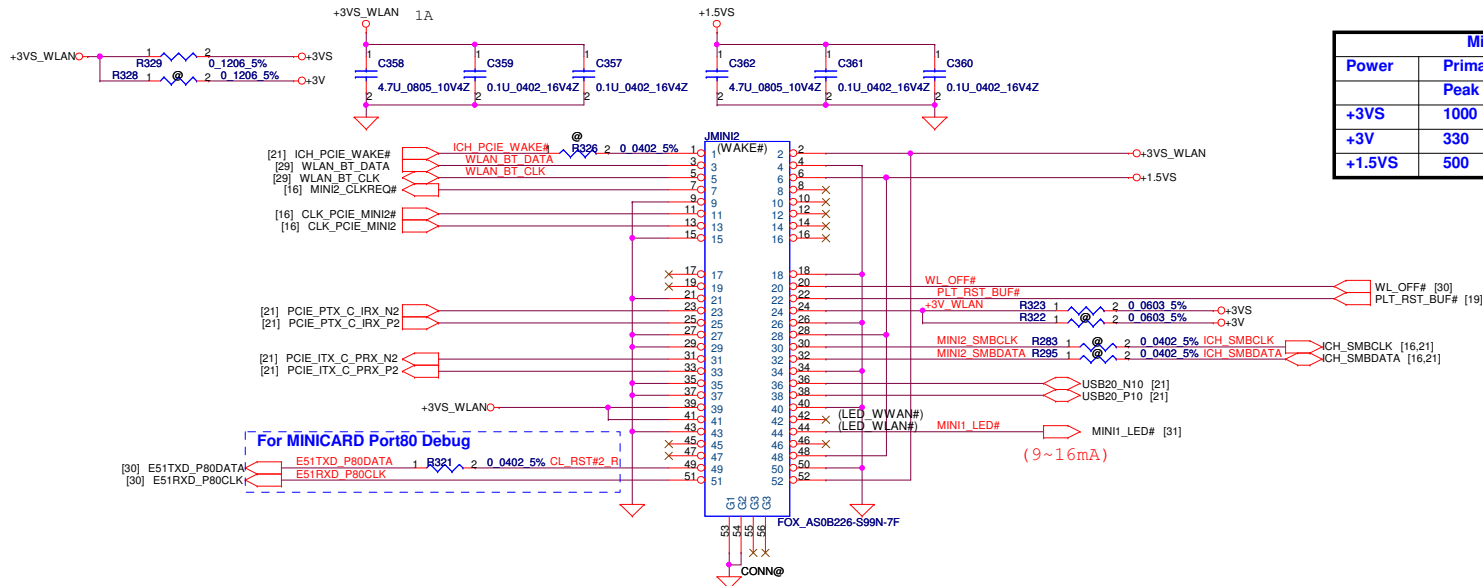




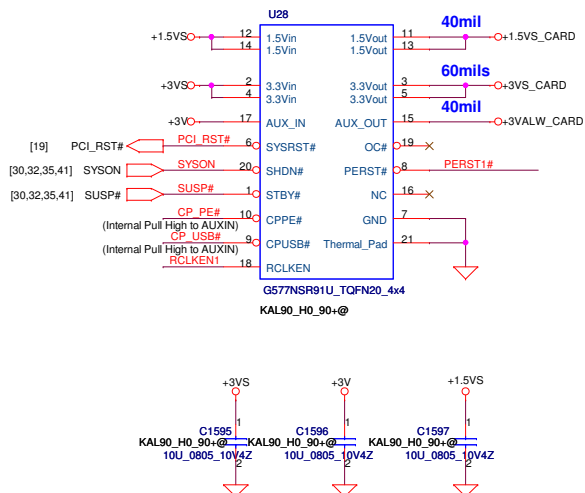
For EMI

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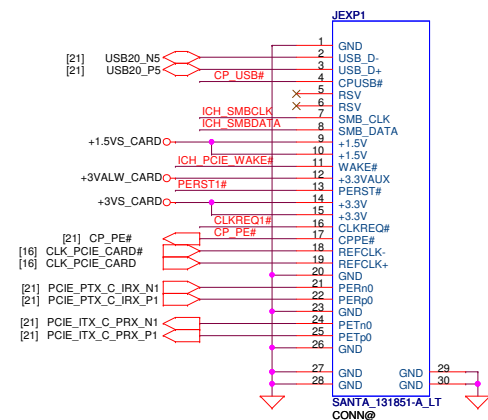
For Wireless LAN



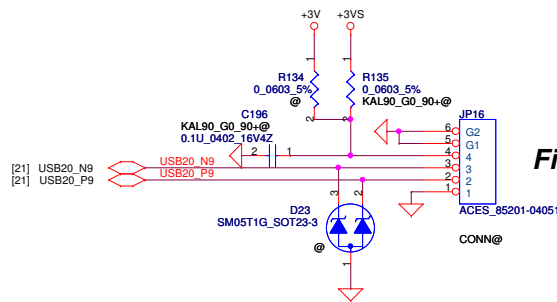
New Card Power Switch



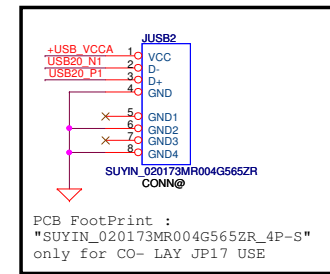
New Card Socket (Left/TOP)



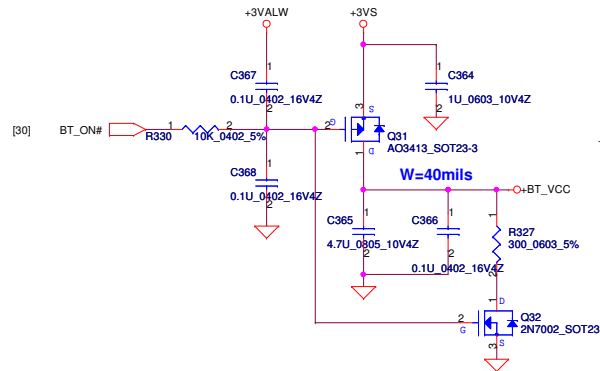
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2008/11/10				2008/11/24				NEW CARD & MINI CARD-WLAN			
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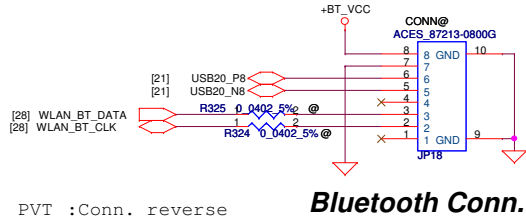
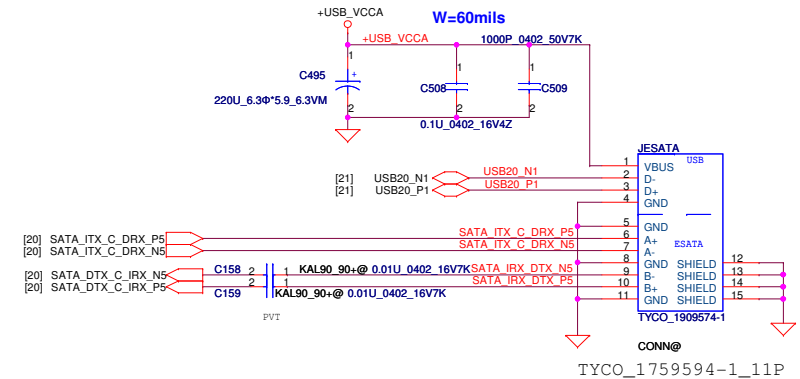
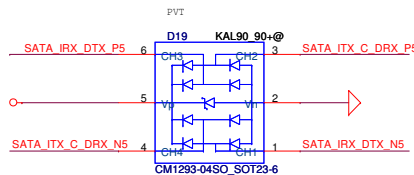
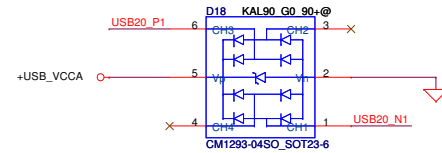
Finger Print Conn.



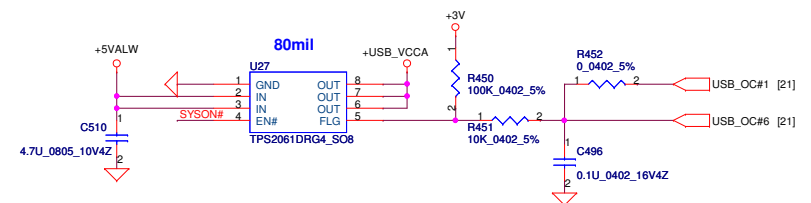
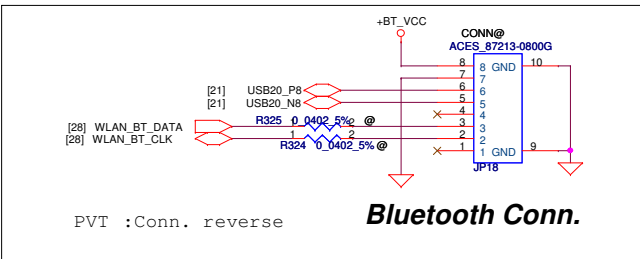
ESATA CONN



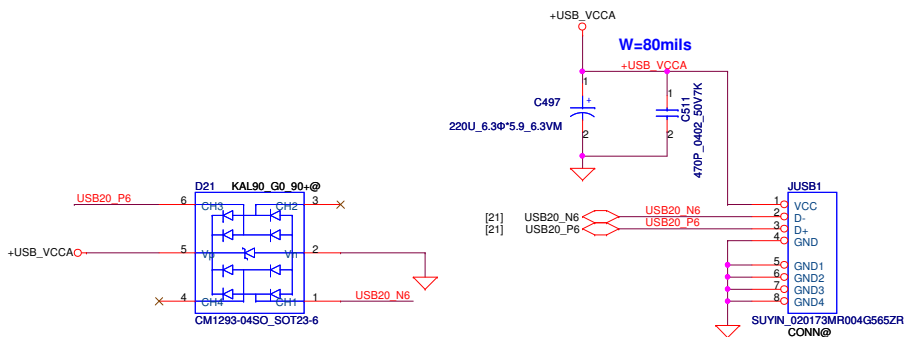
Bluetooth Conn.



PVT :Conn. reverse

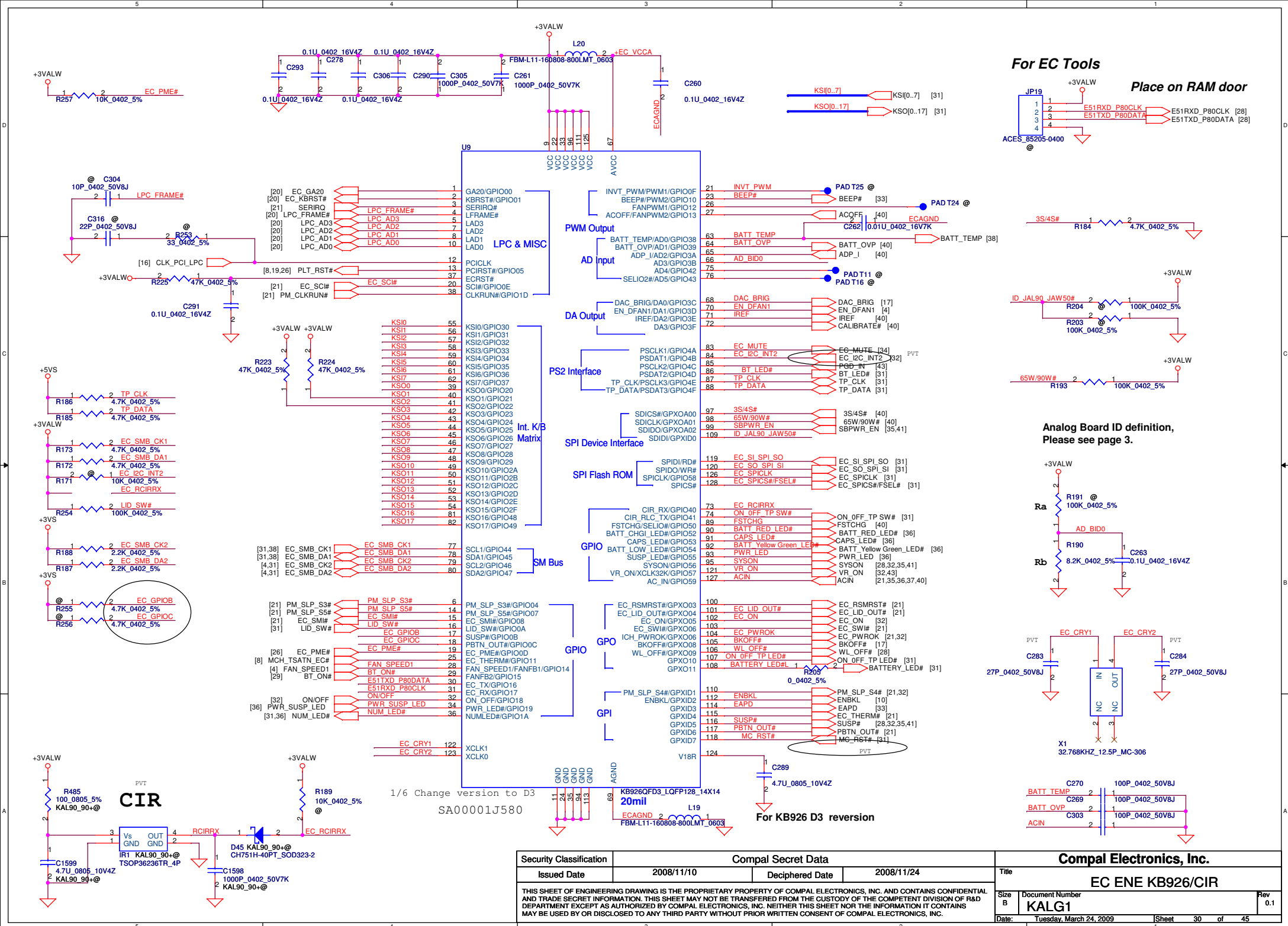


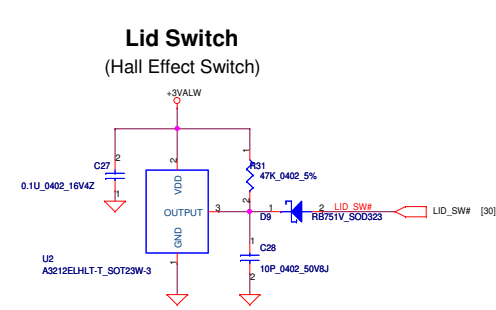
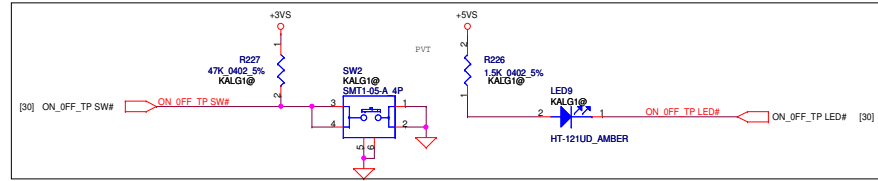
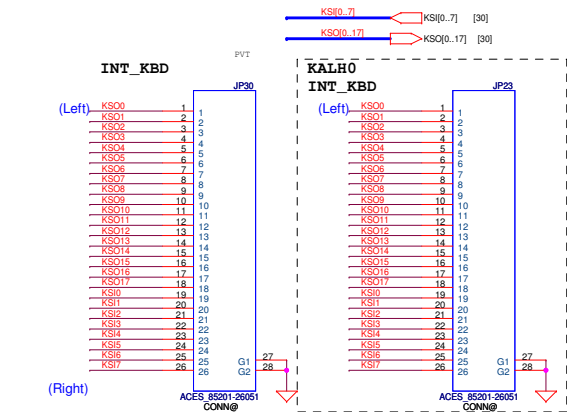
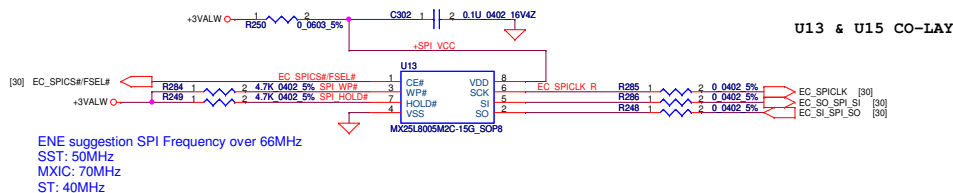
To USB/B Connector



USB CONN.

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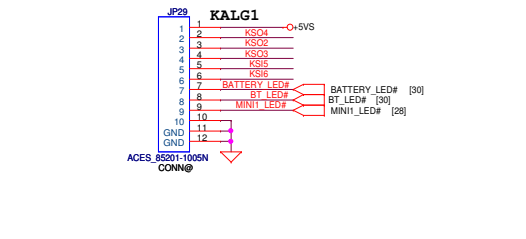
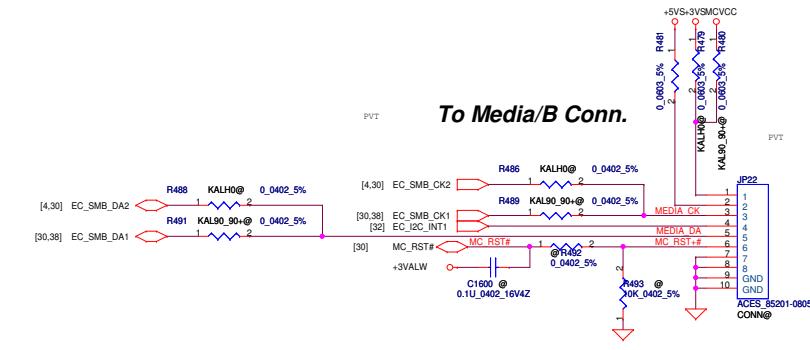
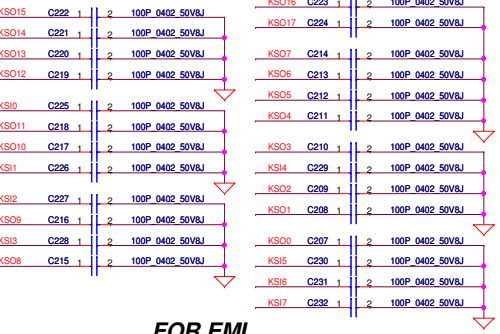
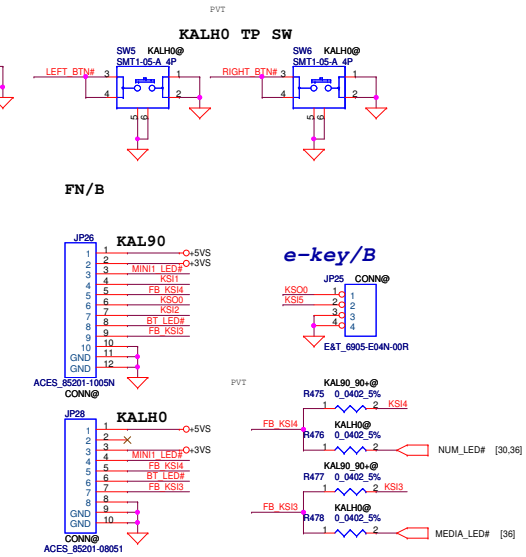
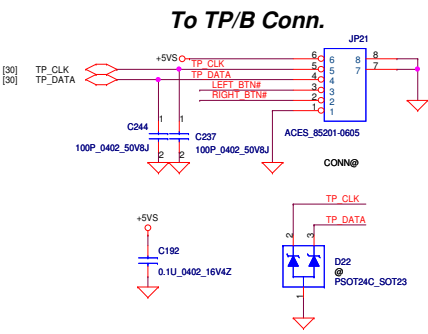




To BTN/B Conn.

	KSO0
KS11	WL_BTN#
KS12	BT_BTN#
KS13	EMAIL_BTN#
KS14	IE_BTN#
KS15	E-KEY_BTN#

	KSO4	KSO2	KSO3
KS15	WL_BTN#	Volume Down	Back Up
KS16	BT_BTN#	Volume Up	Program (KBLG0)
			Battery (KALG0)



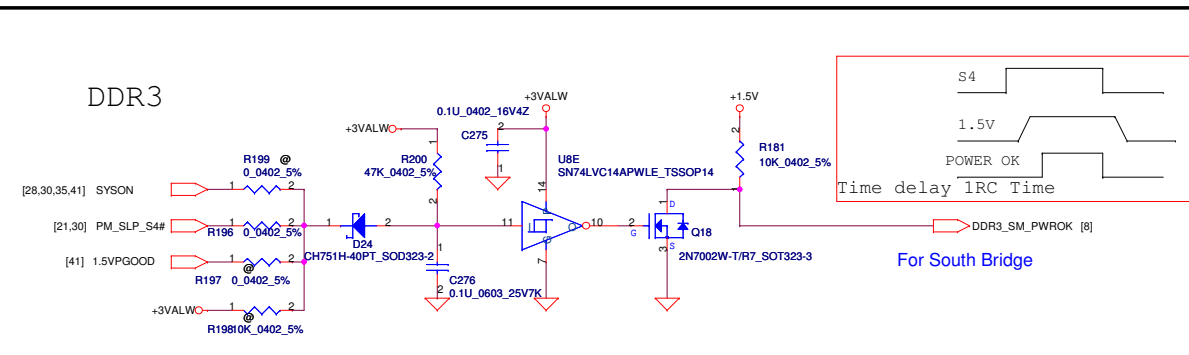
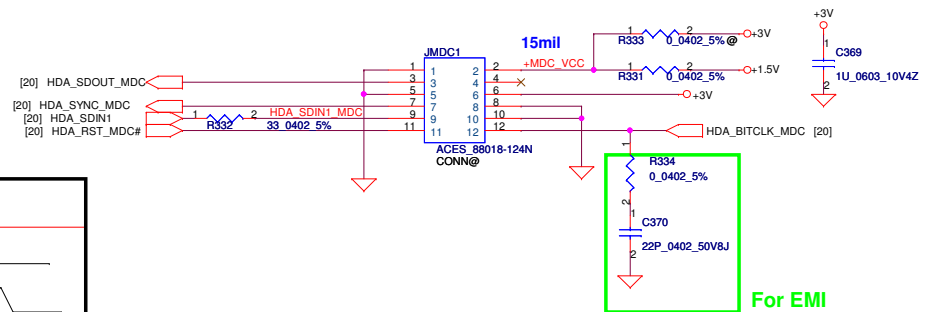
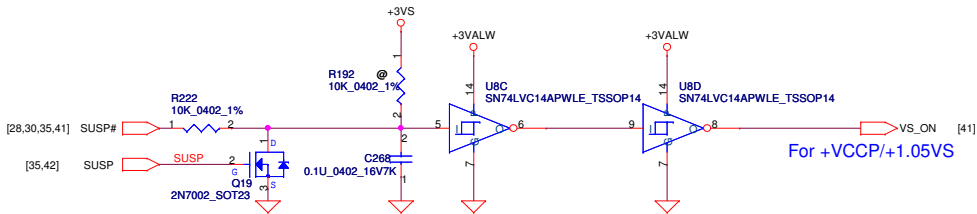
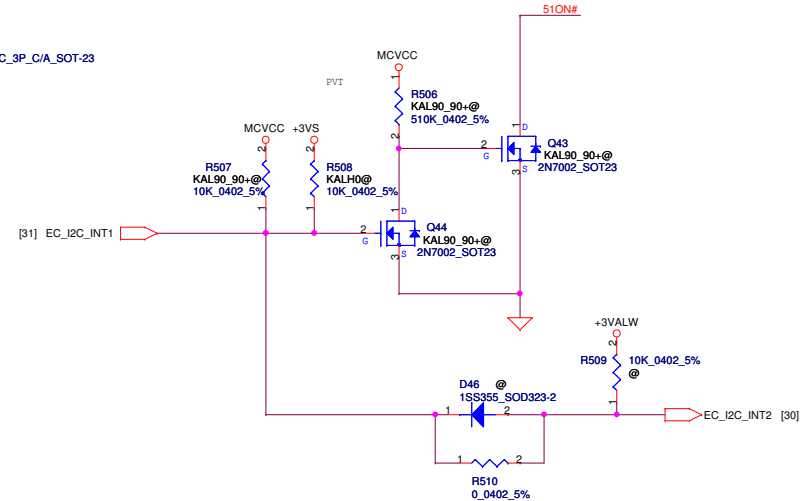
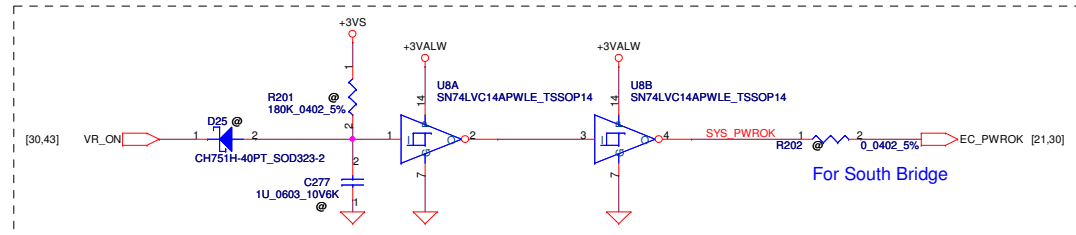
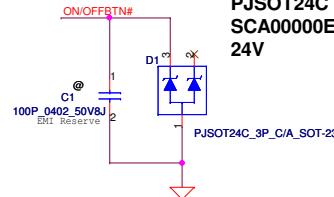
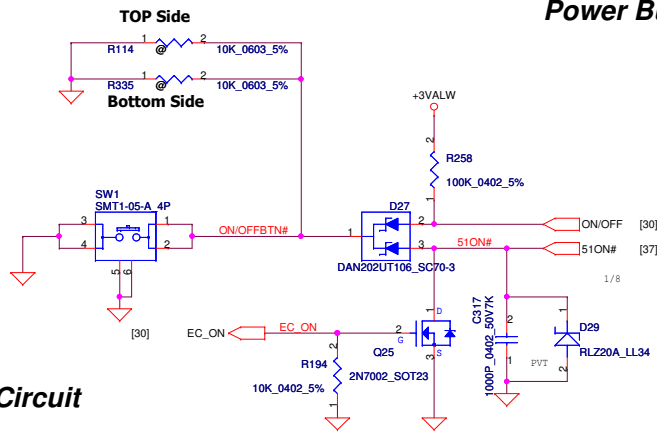
Power Button

D58 USE
PJSOT24C 3P C/A SOT-23
SCA00000E00
24V

Power ON Circuit

HDA MDC Conn.

DDR3



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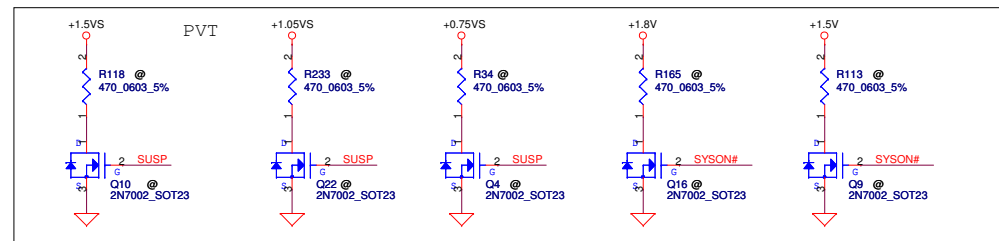
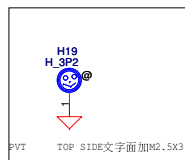
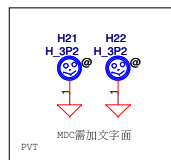
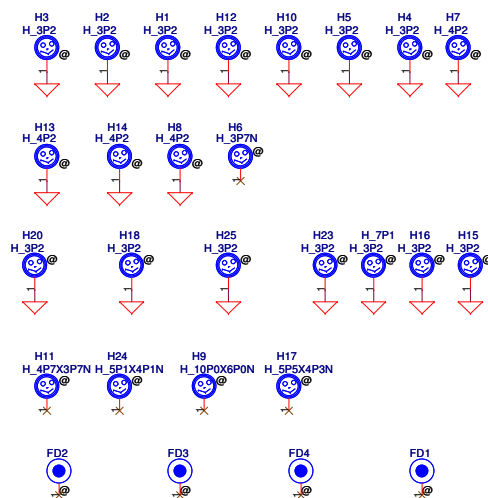
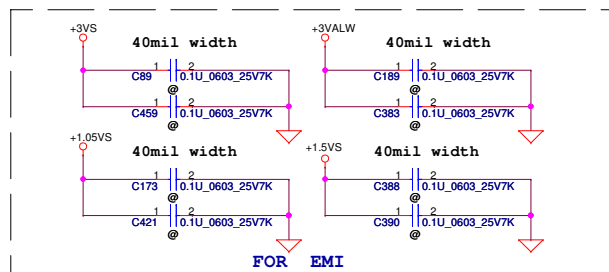
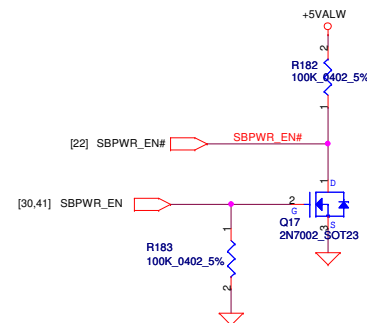
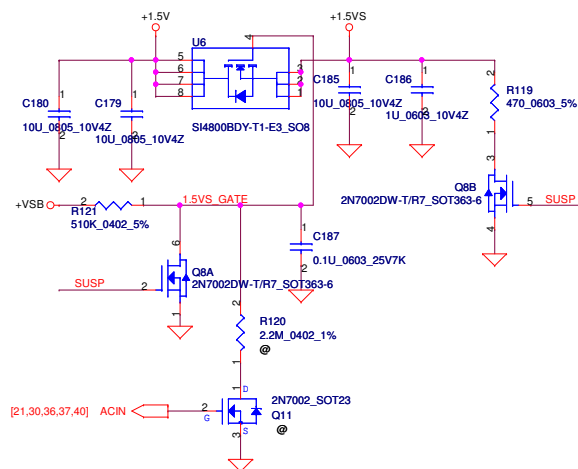
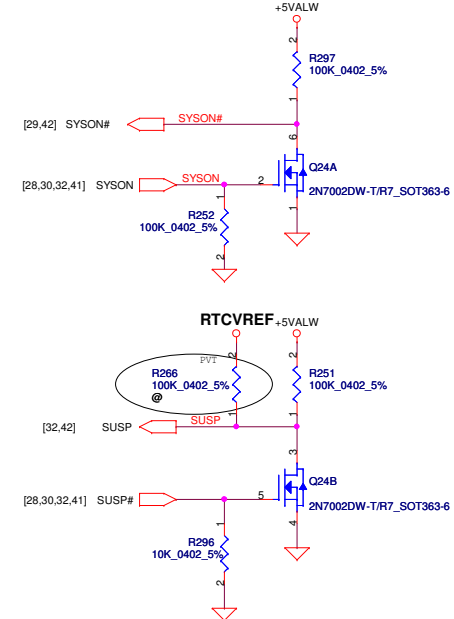
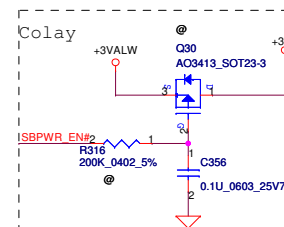
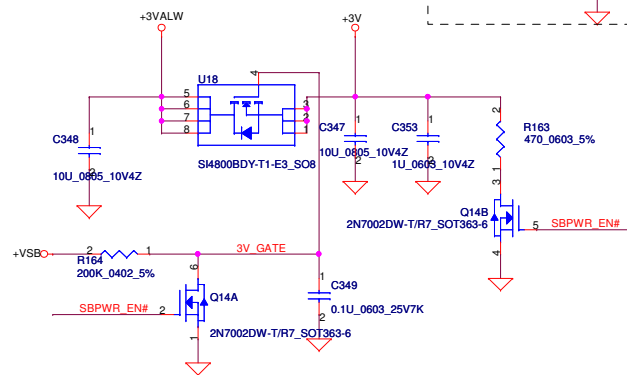
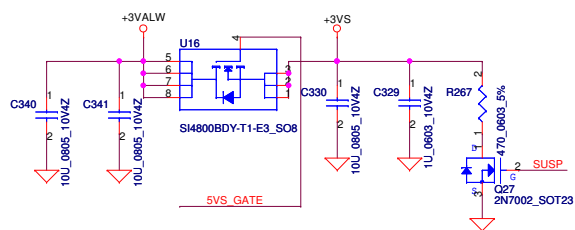
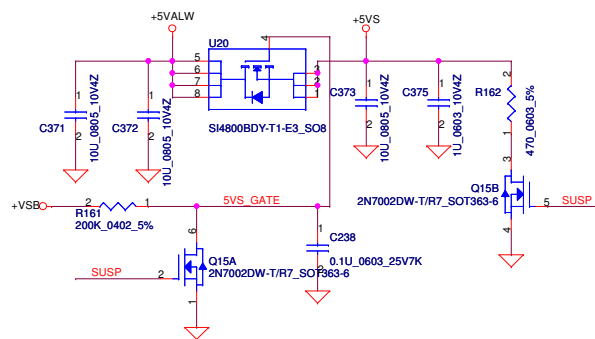
Gain= 10dB

Int. Speaker Conn.

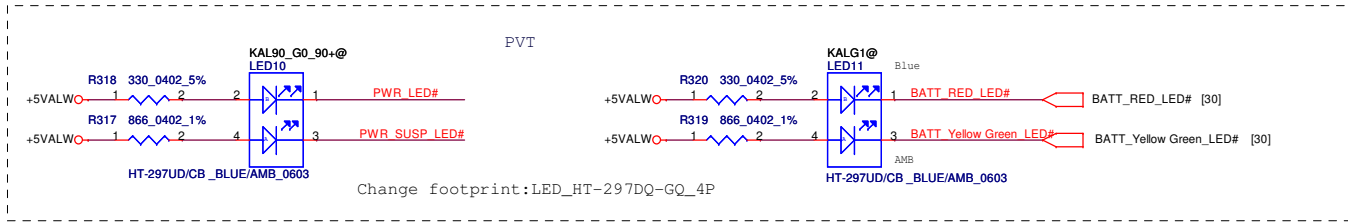
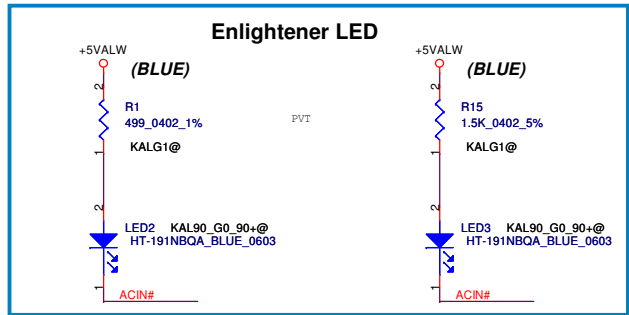
(HDA Jack)
MIC JACK

(HDA Jack)
LINE-IN JACK

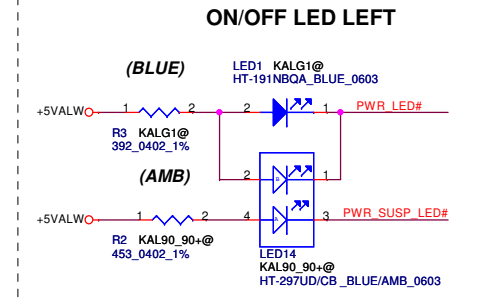
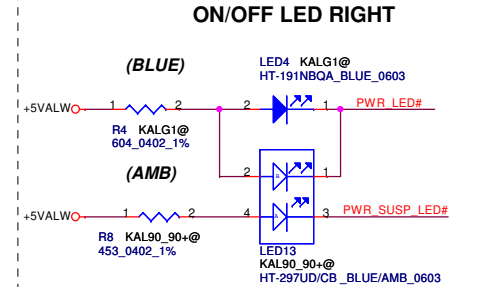
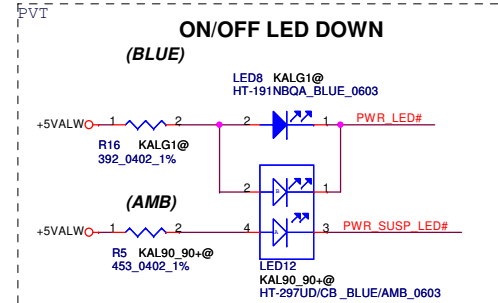
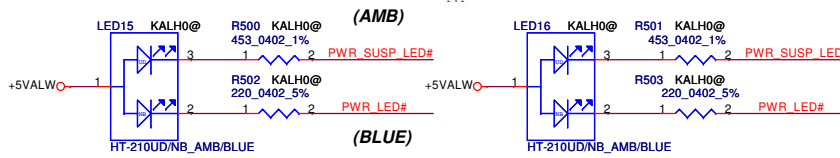
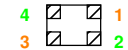
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Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title	
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Customer				Document Number	KALG1
Date				Tuesday, March 24, 2009	Sheet 34 of 45



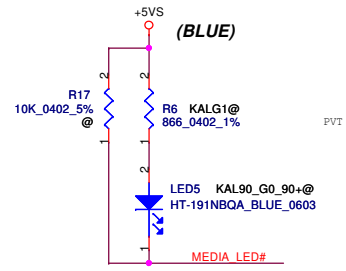
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Issued Date	2008/11/10	Deciphered Date	2008/11/24	Title	DC Interface & Screw Hole
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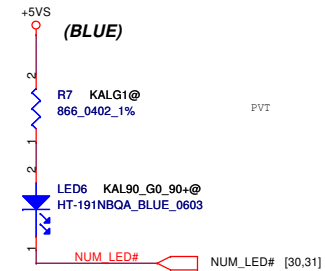
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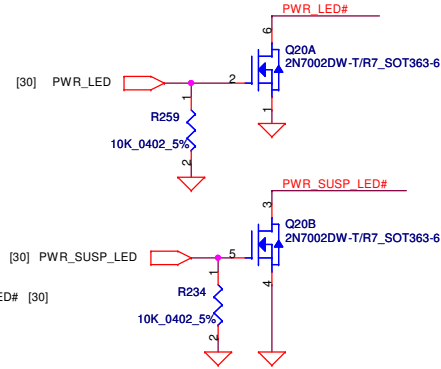
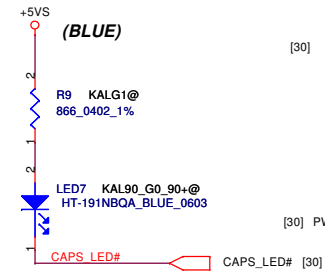
MEDIA_LED



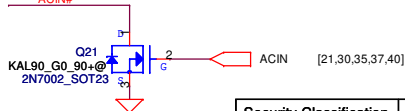
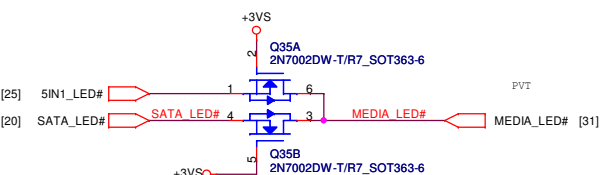
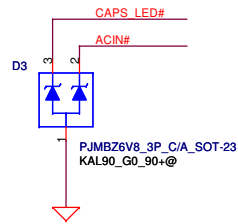
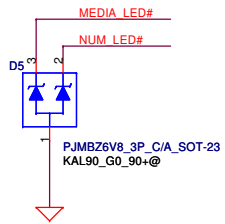
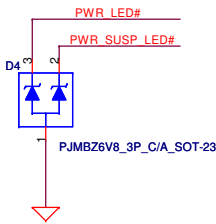
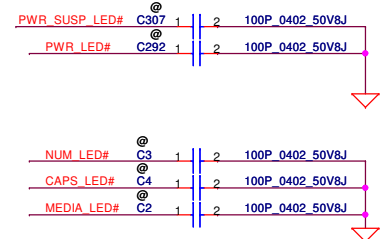
NUM_LED



CAPS_LED

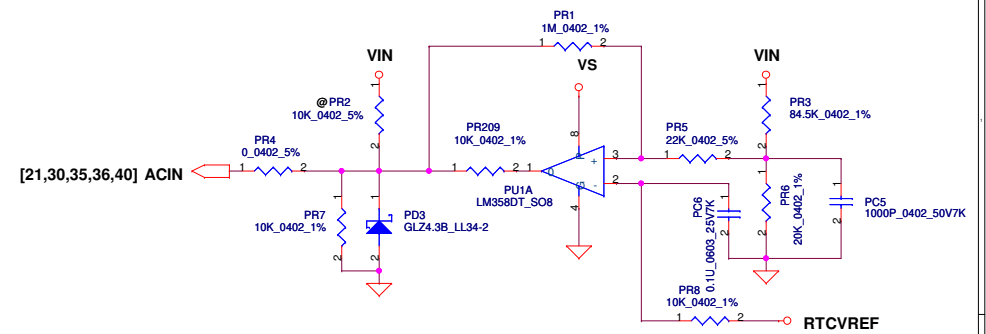
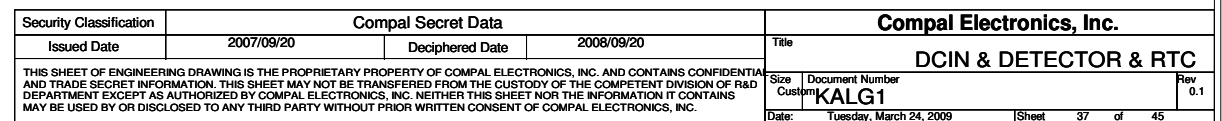
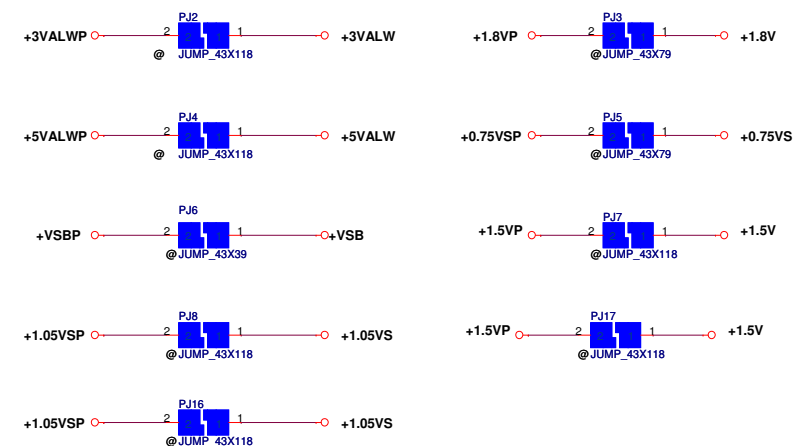


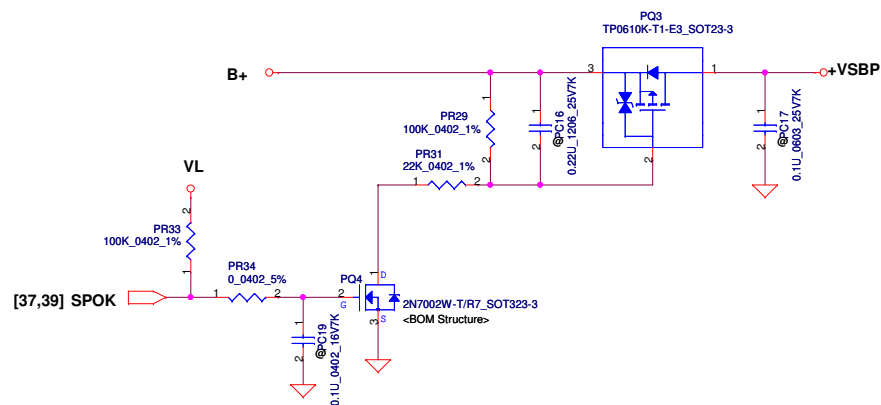
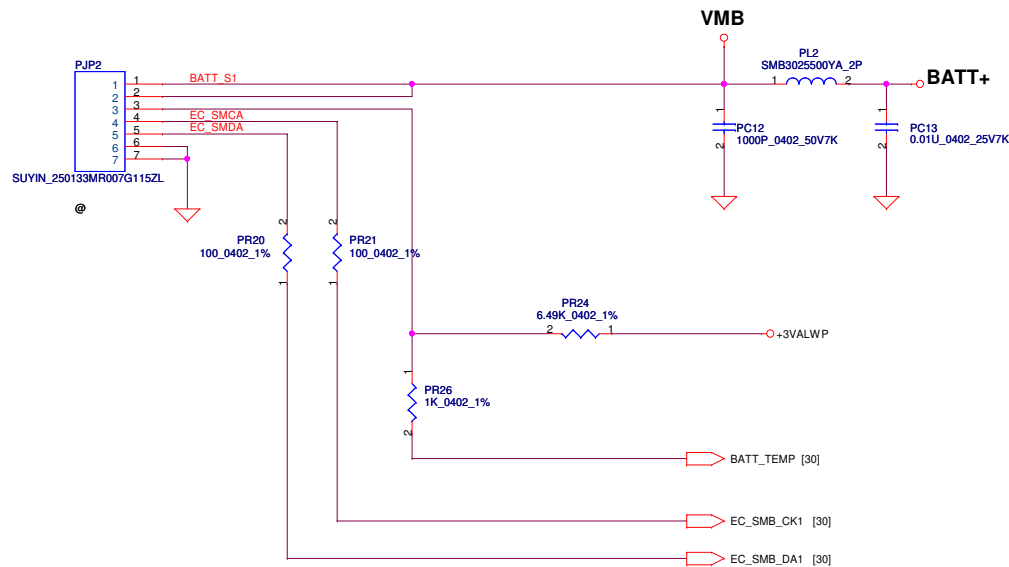
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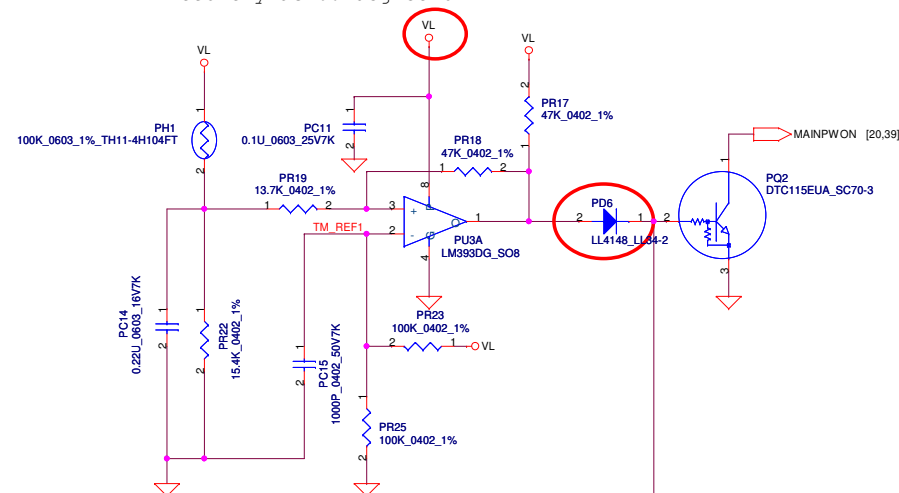
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SINGA 2DC-G756I200

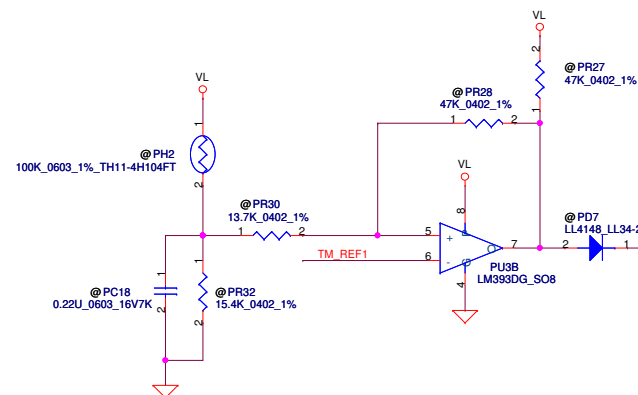
RTC Conn



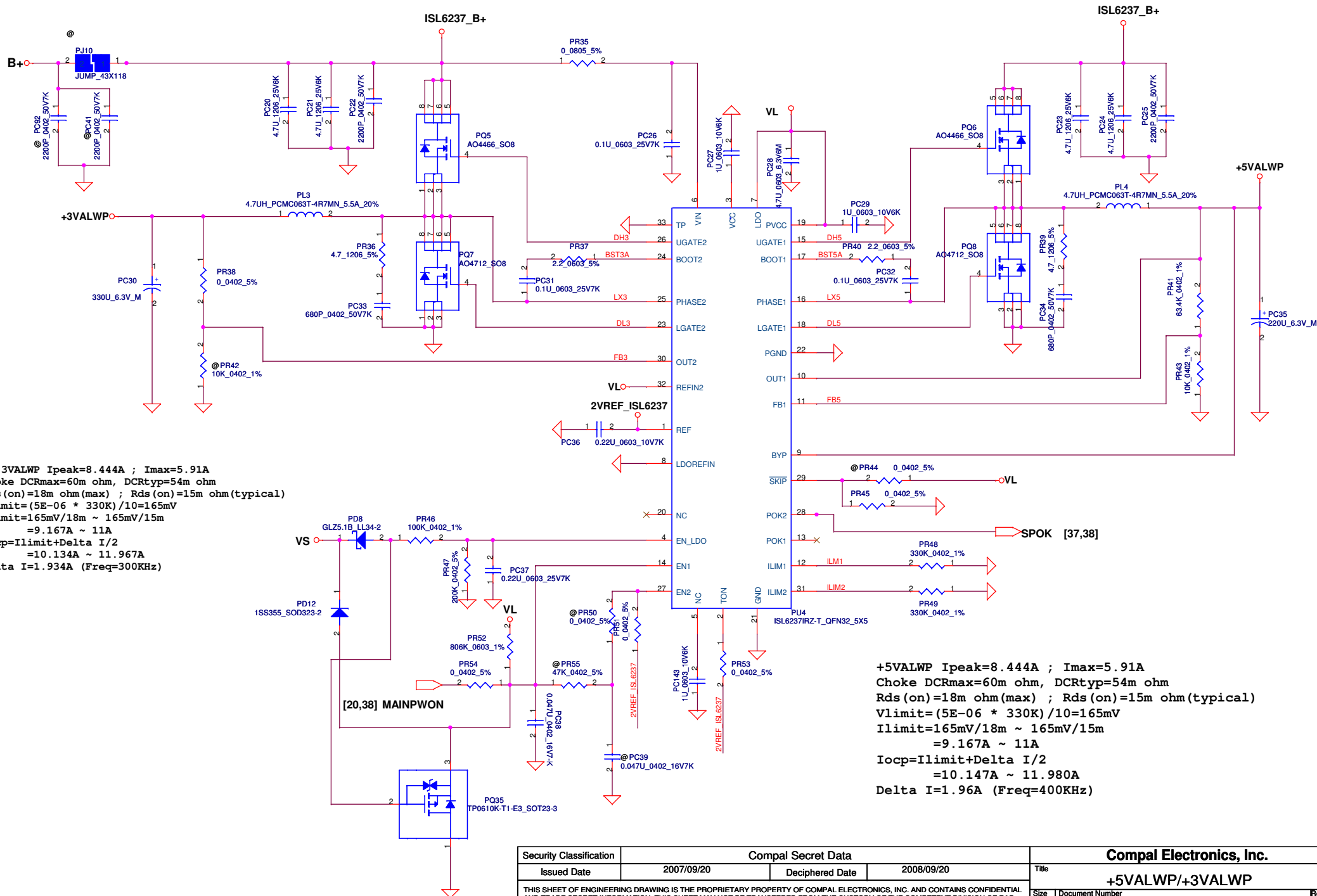
PH1 under CPU botten side :
 CPU thermal protection at 96 degree C
 Recovery at 60 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 47 degree C



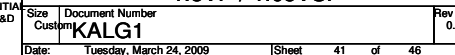
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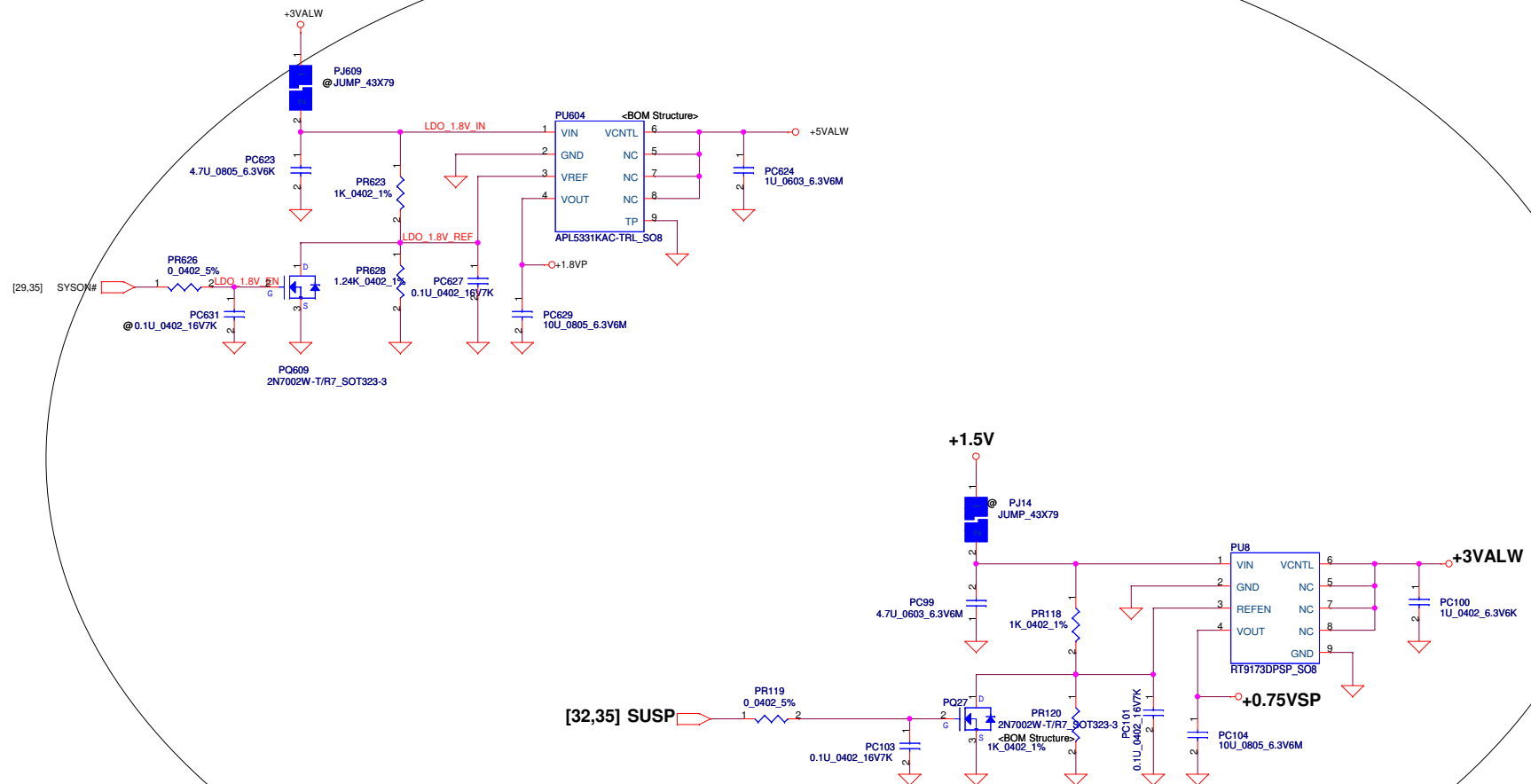


+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add 3/5V boost resister for EMI request			Change PR37 and PR40 to 2.2 OHM		
2		Modify 1.5V and 1.05V choke to cyntec for eff.			PL501 & PL502		
3		Modify 1.5V and 1.05V frequnce from 336K to 264K for eff.			Change PR525 & PR501 from 240K to 300K		
4		Modify 1.5V and 1.05V low side mos for eff.			Change PQ506 & PQ508 from FDS6670 to A04456		
5		Add CPU_core boost resister for EMI request			Change PR138 and PR158 to 2.2 OHM		
6		Modify 1.5V & 1.05V OCP to 14A			Change PR530 & PR522 to 5.9K		
7		Modify 3V & 5V choke to 4.7UH for eff.			Change PL3 & PL4 from 8.2UH to 4.7UH		
8		Modify 5V output cap to OS-CON for costdown			Change PC35		
9		Modify 3V output cap to OS-CON for costdown			Change PC30		
10		Modify dischager mos to A04407A for rating risk			Change PQ12		
11		Add 30K OHM to TPS51117 EN pin , Disable SMPS mode			ADD PR910 & PR911		
12							
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hexainf@hotmail.com
GRATIS - FOR FREE

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PCB



LA-5271P MB Rev0: DA60000C500

PCB 08Y LA-5271P REV0 M/B

North Bridge

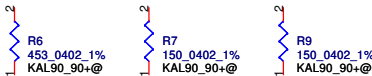


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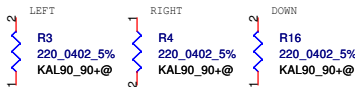
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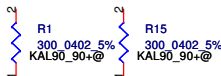
MEDIA_LED NUM_LED CAPS_LED



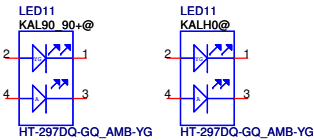
ON/OFF LED Risiter



Enlightener LED



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				Size	Document Number	Rev
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