

Compal Confidential

KBLG0/NBLG0 Schematics Document

AMD Puma (JV40-PU) : Griffin Processor with RS780MN/SB700/M92-M2 XT
Tigris (JV40-TR) : Caspian Processor with RS880M/SB710/M92-M2 XT

2009-03-11

REV:1.0

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				401679	C
Date: Thursday, March 26, 2009				Sheet	1 of 57

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	DN	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
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EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (CPU)	1001 100X b	98H
			GMT G781-1 (GPU)	1001 101X b	9AH
			SB-Temp Sensor		9CH

SB700

SM Bus 0 address

Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2	New card	
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		
Mini card				

EC SM Bus2 address

SB700

SM Bus 1 address

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@
M92-M2 XT	M92@
VRAM STRAP	VRAM@
LAN 8121	8121@
LAN 8131	8131@
HDT debug	HDT@
JMB385 CR	JMB385@
RTS5159 CR	RTS5159@
FOR PUMA	PUMA@
FOR TIGRIS	TIGRIS@
FOR TEST	UB@

	SB700	SB700	RS780MN	DISPLAY OUTPUT
	PX_GPIO0	PX_GPIO1	PX_GPIO2	
Function Description	dGPU_Reset	dGPU_PWR_Enable	PX Mode Switch	
IGP only mode	X	X	X	
PowerXpress mode	H : Enable	H : Enable	L : IGPU(DC) / H : dGPU(AC)	LVDS / CRT

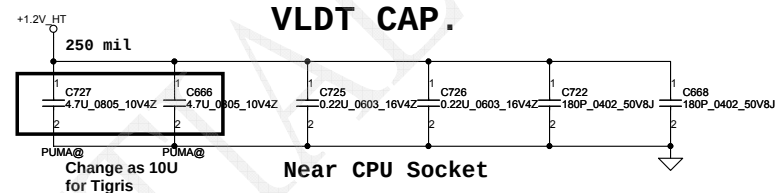
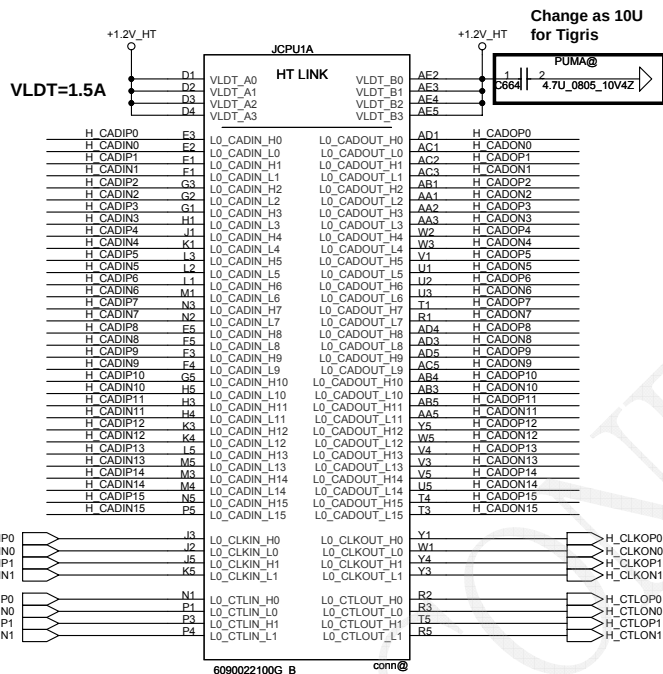
	KB926					
	PX_GPIO1	PX_GPIO2	PX_+3VS	PX_+1.8VS	PX_+VGA_CORE	PX_GPIO2_NB
Function Description	Enable +1.1VS_PX	PX MODE SWITCH	Enable +3VS_DELAY	Enable +1.8VS_PX	Enable +VGA_CORE	Trigger from SB
IGP only mode	X	X	X	X	X	X
PowerXpress mode	H : Enable	Reserved	H : Enable	H : Enable	H : Enable	Reserved

	KB926	
	PX_GPIO1_SB	
Function Description	Trigger from SB to Enable (PX_GPIO1/PX_+3VS/PX_+1.8VS/PX_+VGA_CORE)	
IGP only mode	X	
PowerXpress mode	H : Enable	

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				401679		
				Date: Thursday, March 26, 2009 Sheet 3 of 57		

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10 H_CADIN[0..15] H_CADIN[0..15]

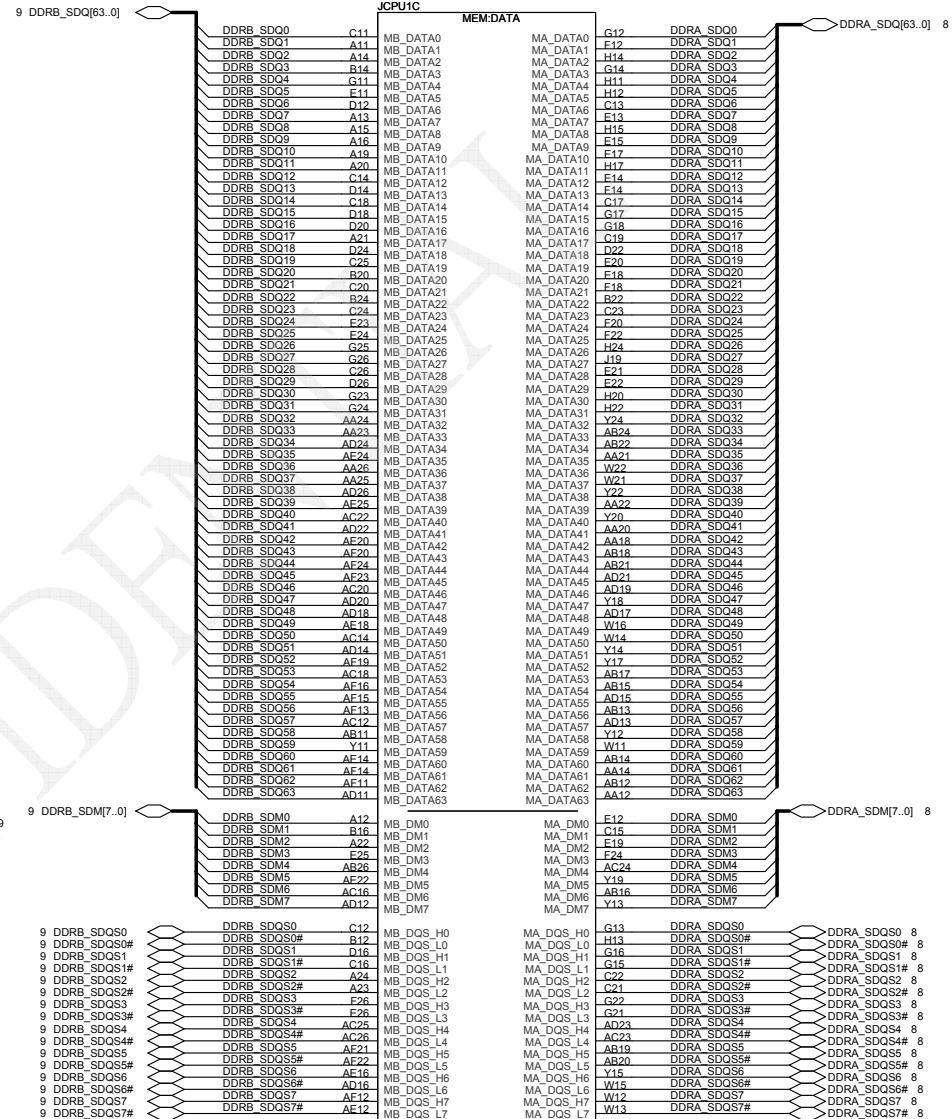
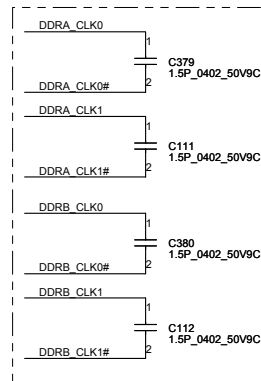
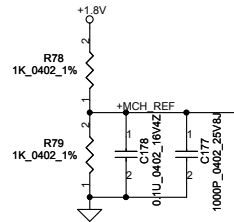
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H_CADON[0..15] H_CADON[0..15] 10



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				Date	Thursday, March 26, 2009
				Sheet	4 of 57
				Rev	C

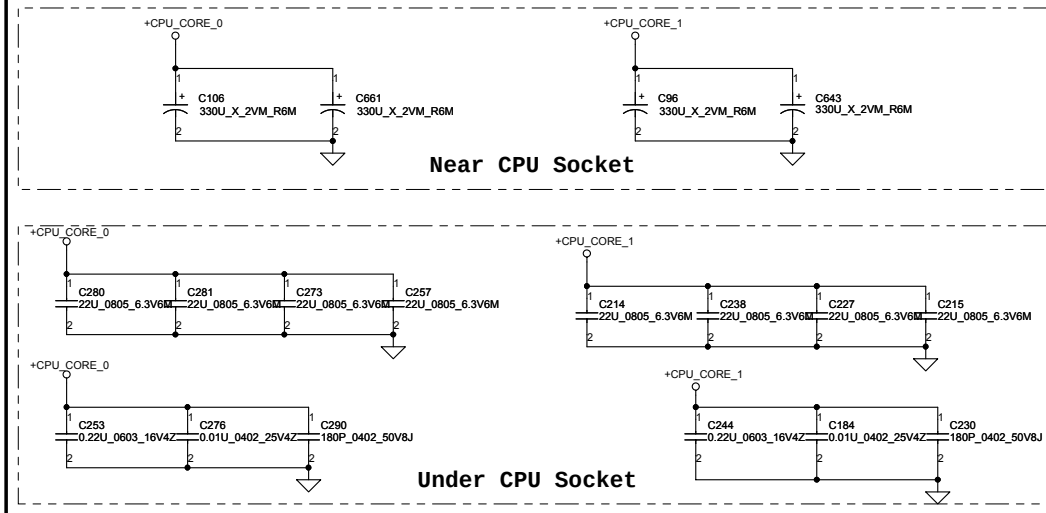
Processor DDR2 Memory Interface

PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

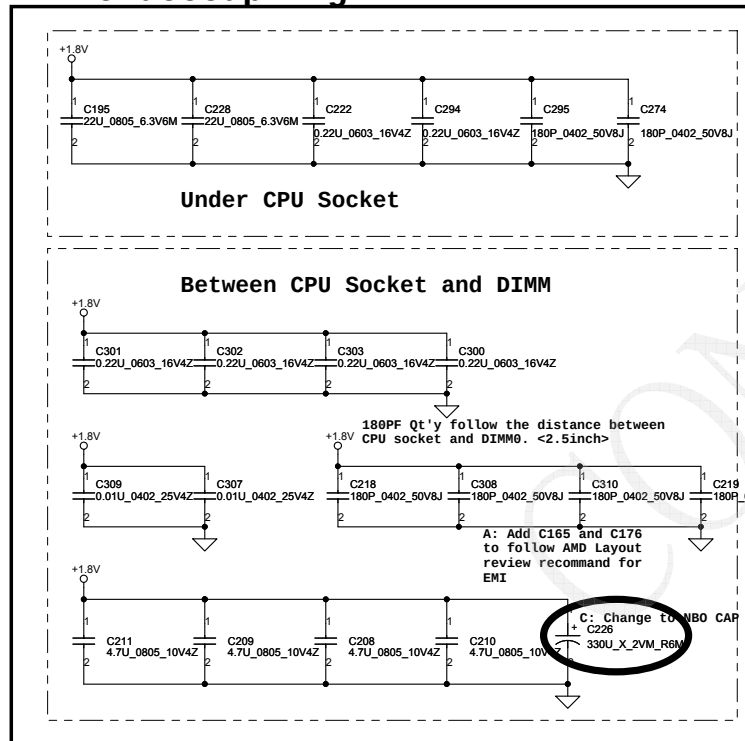
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Date: Thursday, March 26, 2009				Sheet	5 of 57

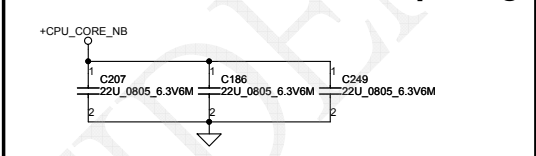
VDD(+CPU_CORE) decoupling.



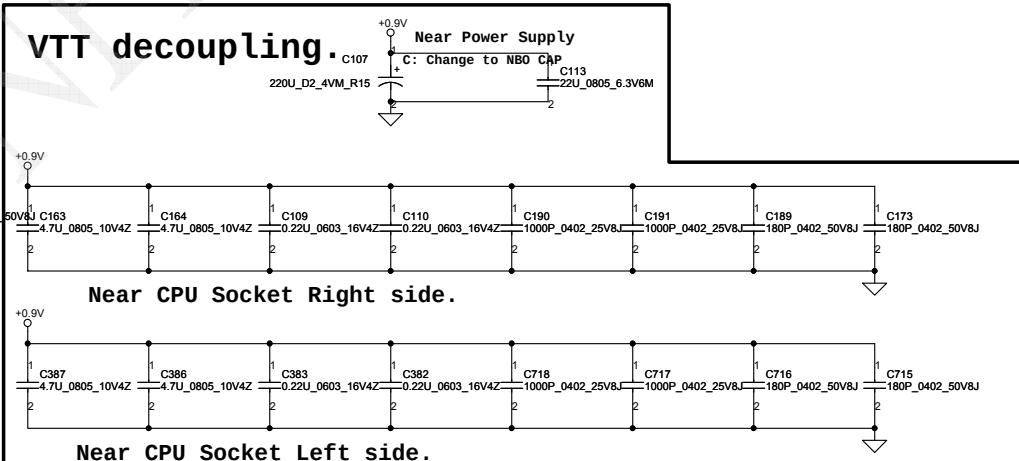
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VTT decoupling.



VDD0 = 18A

VDD1 = 18A

JCPU1F

VDDNB=4A
(For Tigris)

VDDNB=3A

+CPU_CORE_NB

VDDIO=3A

6090022100G_B
Athlon 64 S1
Processor Socket
conn@

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Athlon 64 S1
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Date: Thursday, March 26, 2009				Rev C

14 PCIE_GTX_C_MRX_P[0..15] PCIE GTX C MRX P[0..15]
14 PCIE_GTX_C_MRX_N[0..15] PCIE GTX C MRX N[0..15]

PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15] 14
PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15] 14

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PCIE_MTX_GRX_P[0..3] PCIE_MTX_GRX_P[0..3] 25

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PCIE GTX C MRX N0 C4
PCIE GTX C MRX N1 A3
PCIE GTX C MRX P1 B3
PCIE GTX C MRX P2 C2
PCIE GTX C MRX N2 C1
PCIE GTX C MRX P3 F3
PCIE GTX C MRX N3 F6
PCIE GTX C MRX P4 G5
PCIE GTX C MRX N4 G6
PCIE GTX C MRX P5 H6
PCIE GTX C MRX N5 H6
PCIE GTX C MRX N6 I J6
PCIE GTX C MRX P6 I J5
PCIE GTX C MRX P7 J7
PCIE GTX C MRX N7 J8
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PCIE GTX C MRX N11 M6
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PCIE GTX C MRX N12 P8
PCIE GTX C MRX P13 R6
PCIE GTX C MRX N13 P6
PCIE GTX C MRX P14 P4
PCIE GTX C MRX N14 P3
PCIE GTX C MRX P15 T4
PCIE GTX C MRX N15 T3

U38
PART 2 OF 6
PCIE I/F GFX
GFX_RX0P
GFX_RX0N
GFX_RX1P
GFX_RX1N
GFX_RX2P
GFX_RX2N
GFX_RX3P
GFX_RX3N
GFX_RX4P
GFX_RX4N
GFX_RX5P
GFX_RX5N
GFX_RX6P
GFX_RX6N
GFX_RX7P
GFX_RX7N
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GFX_RX11P
GFX_RX11N
GFX_RX12P
GFX_RX12N
GFX_RX13P
GFX_RX13N
GFX_RX14P
GFX_RX14N
GFX_RX15P
GFX_RX15N

A5 PCIE_MTX_GRX_P0
B5 PCIE_MTX_GRX_N0
C461 1 2
B4 PCIE_MTX_GRX_N1
C468 1 2
C3 PCIE_MTX_GRX_P2
C650 1 2
D2 PCIE_MTX_GRX_N3
C652 1 2
E2 PCIE_MTX_GRX_P4
C655 1 2
F1 PCIE_MTX_GRX_N4
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C658 1 2
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C659 1 2
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C641 1 2
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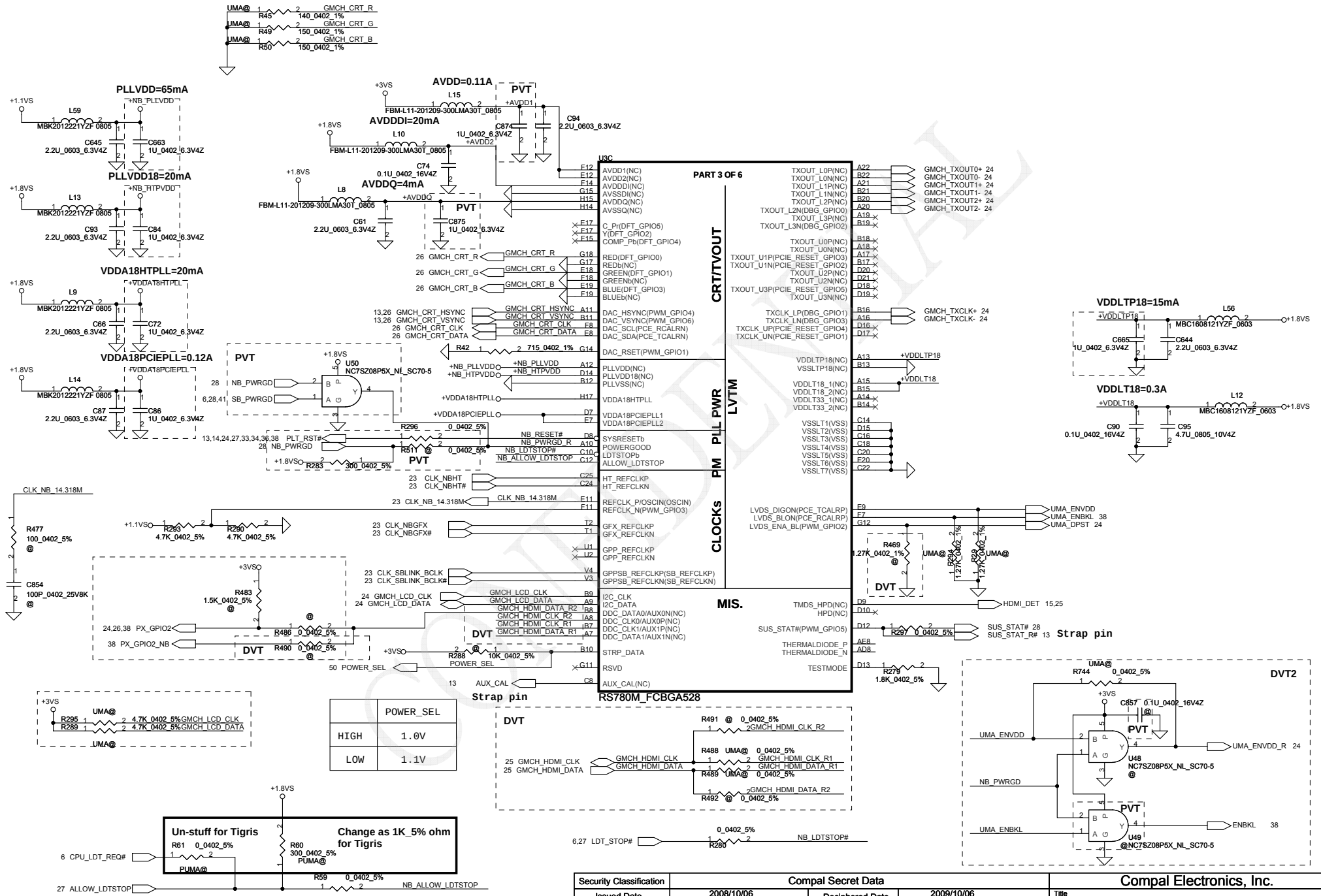
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AE3
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U17

PCIE I/F GPP
GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
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For RS780M A13
RED: Connected to GND through two separate 140ohm 1% resistor



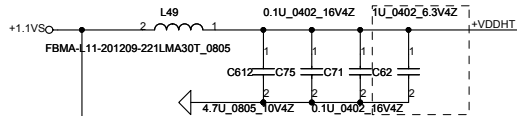
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Compal Electronics, Inc.	
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				Date: Thursday, March 26, 2009	Sheet 11 of 57

SCHEMATIC A4921P

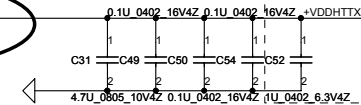
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Thursday, March 26, 2009

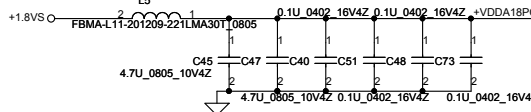
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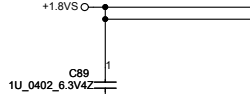
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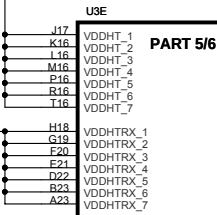
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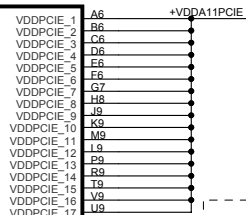


PART 5/6

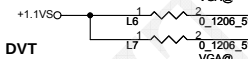


POWER

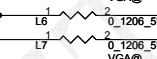
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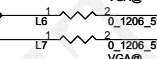
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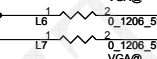
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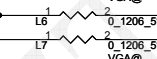
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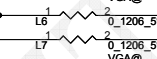
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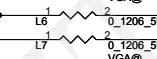
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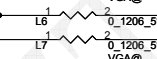
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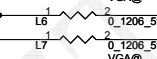
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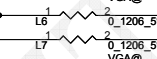
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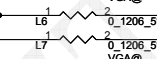
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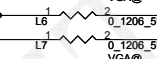
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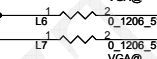
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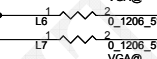
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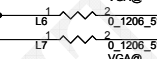
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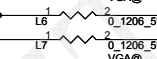
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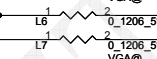
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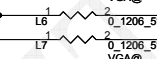
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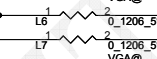
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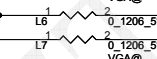
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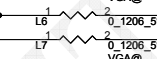
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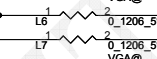
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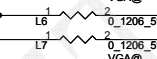
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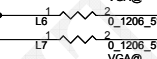
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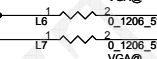
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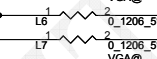
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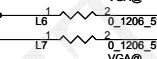
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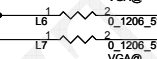
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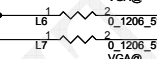
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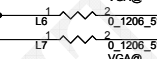
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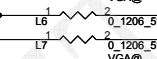
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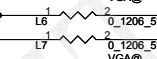
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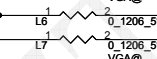
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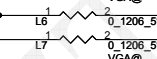
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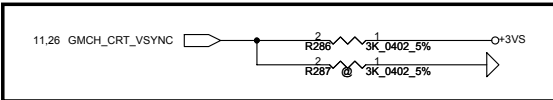


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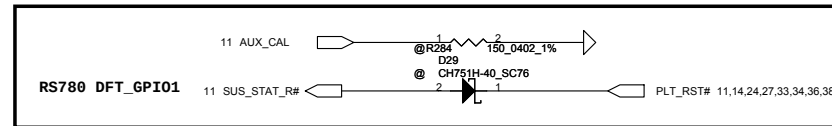
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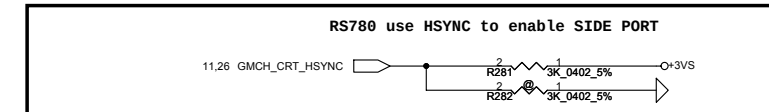
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

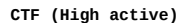
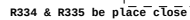
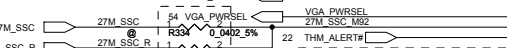
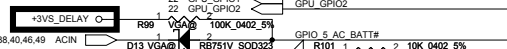
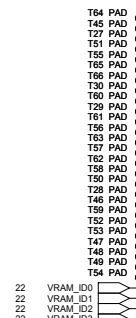


RS780 use HSYNC to enable SIDE PORT

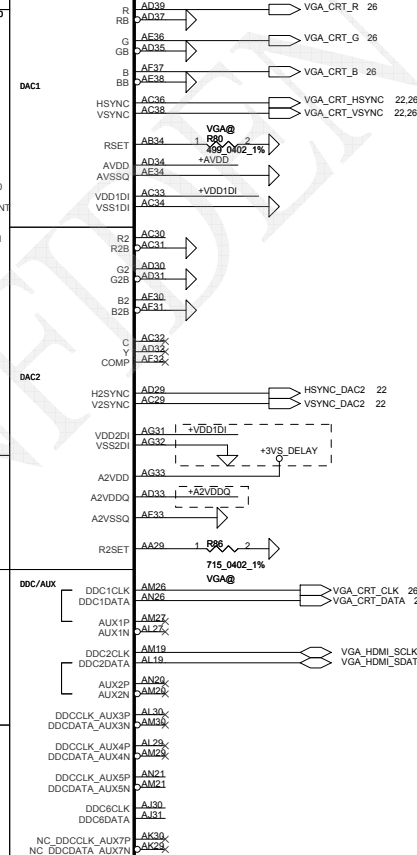
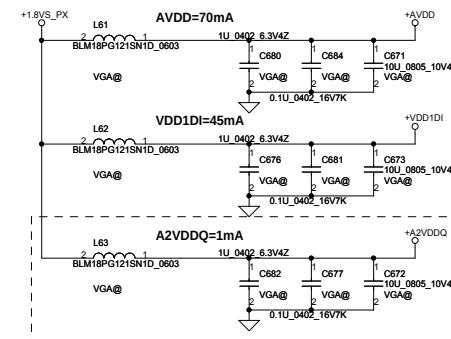
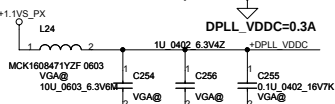
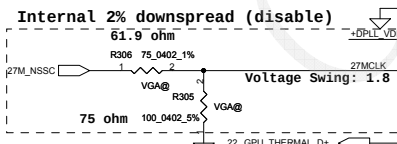
RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
0. Enable (RS780)
1 : Disable(RS780)

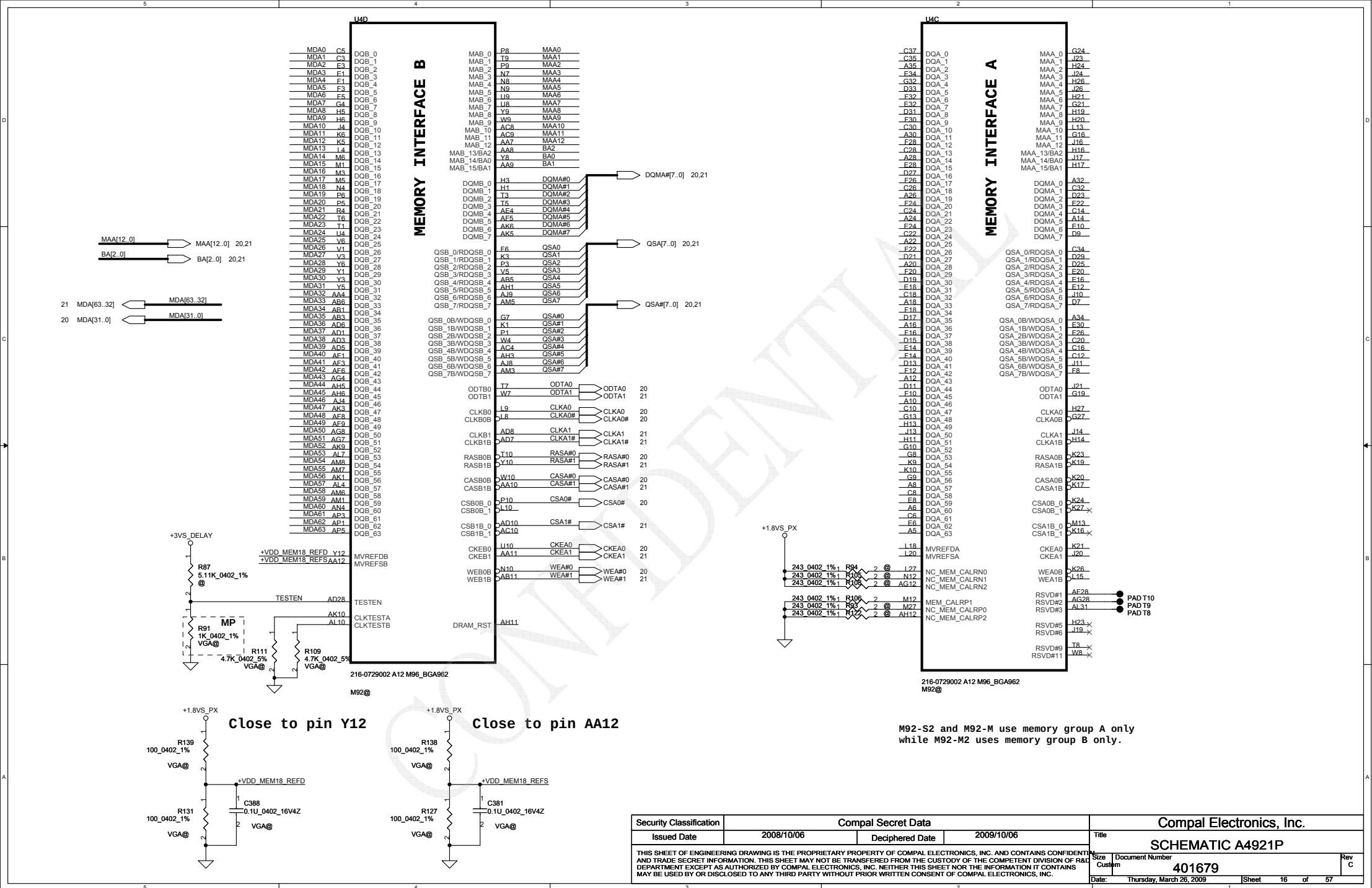
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	SCHEMATIC A4921P
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				Date	Thursday, March 26, 2009
				Sheet	13 of 57

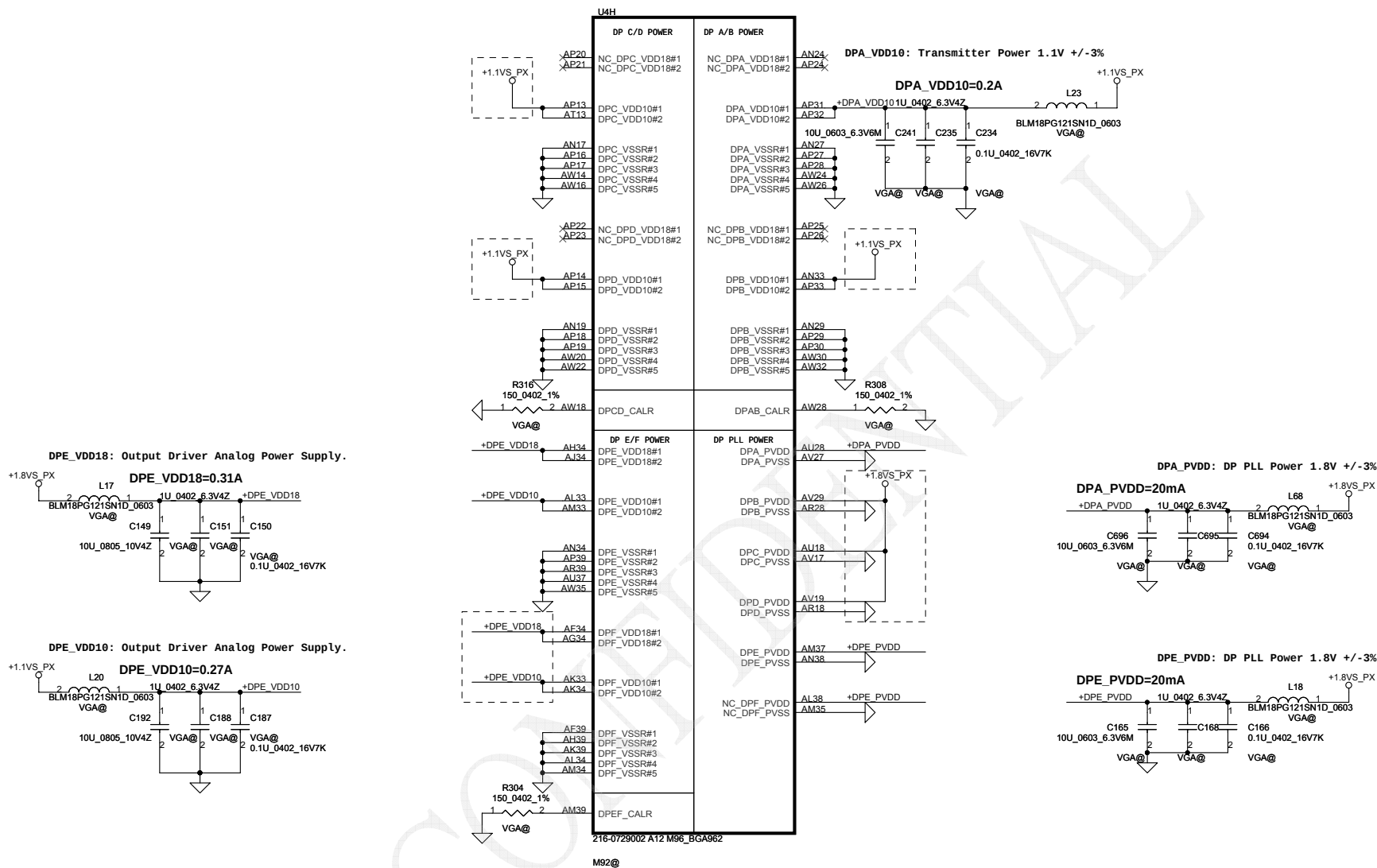
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Issued Date		2008/10/06		Deciphered Date		2009/10/06		Title		
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						Size	Document Number		Rev	
						Custom	401679		C	
						Date:	Thursday, March 26, 2009		Sheet 14 of 57	



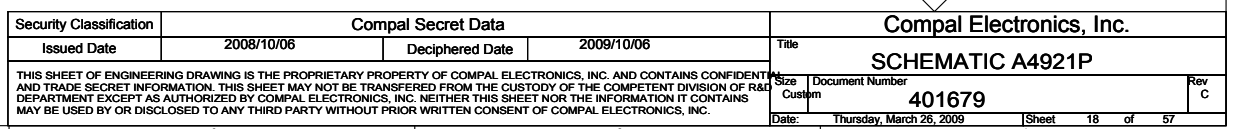
The diagram shows the +3V3_DELAY pin configuration. The pin is connected to a 3V3 supply through a 10K resistor (R95). The pin is also connected to a 1K resistor (R96) which is connected to ground. The pin is labeled GPIO24 TRSTB.

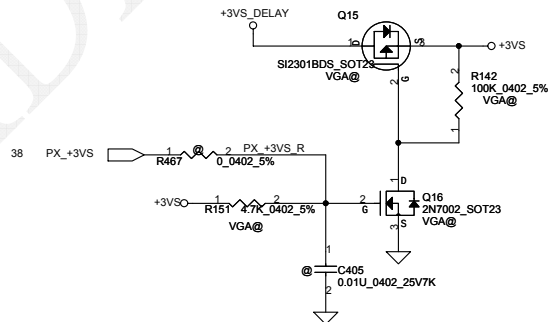
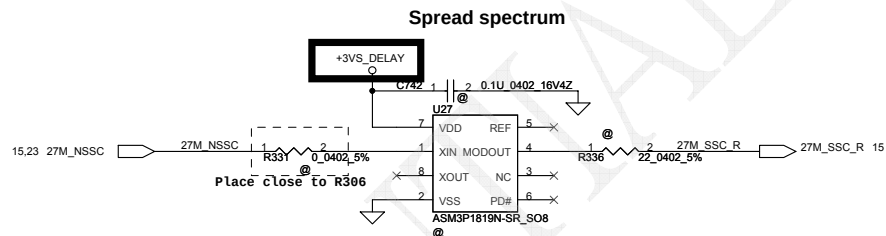
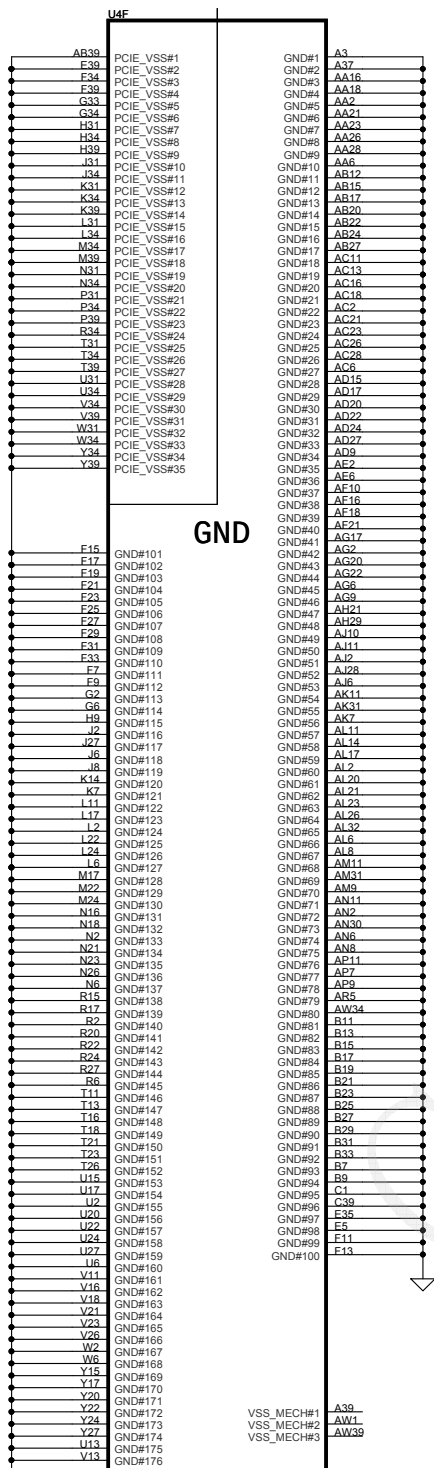






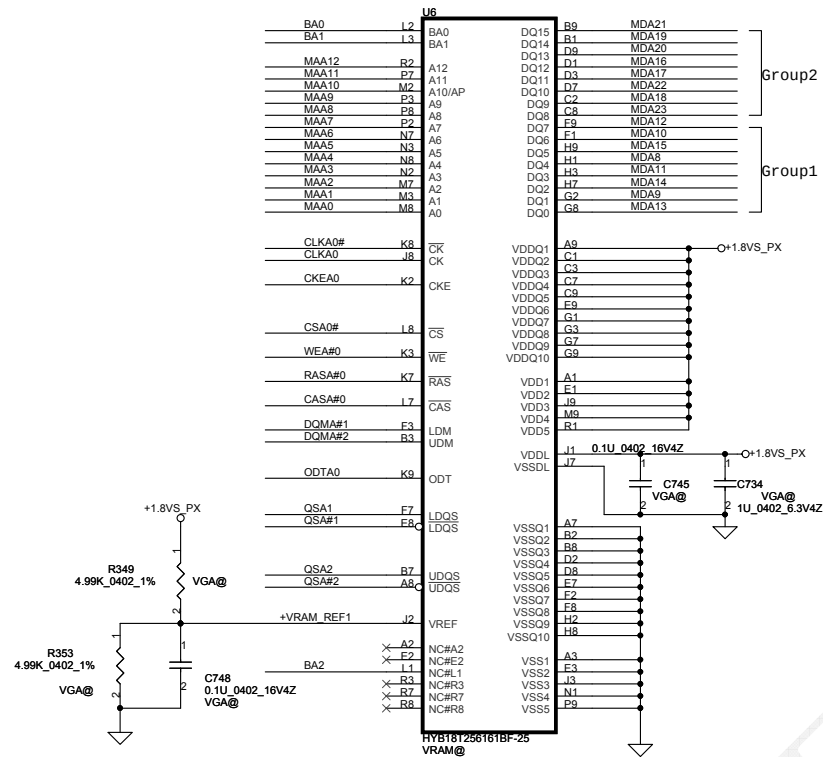
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Size		Document Number		Rev
Custom		401679		C
Date:		Thursday, March 26, 2009		Sheet 17 of 57



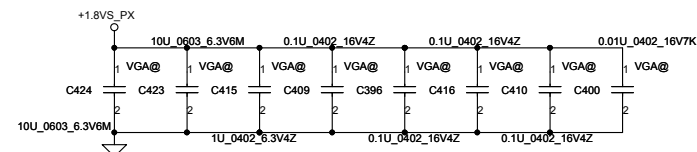
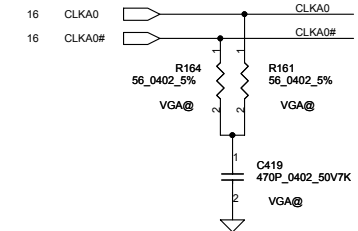
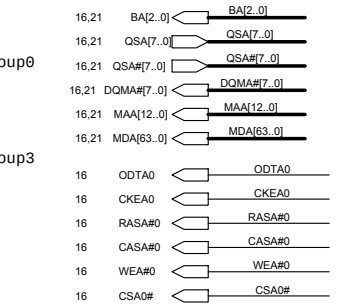
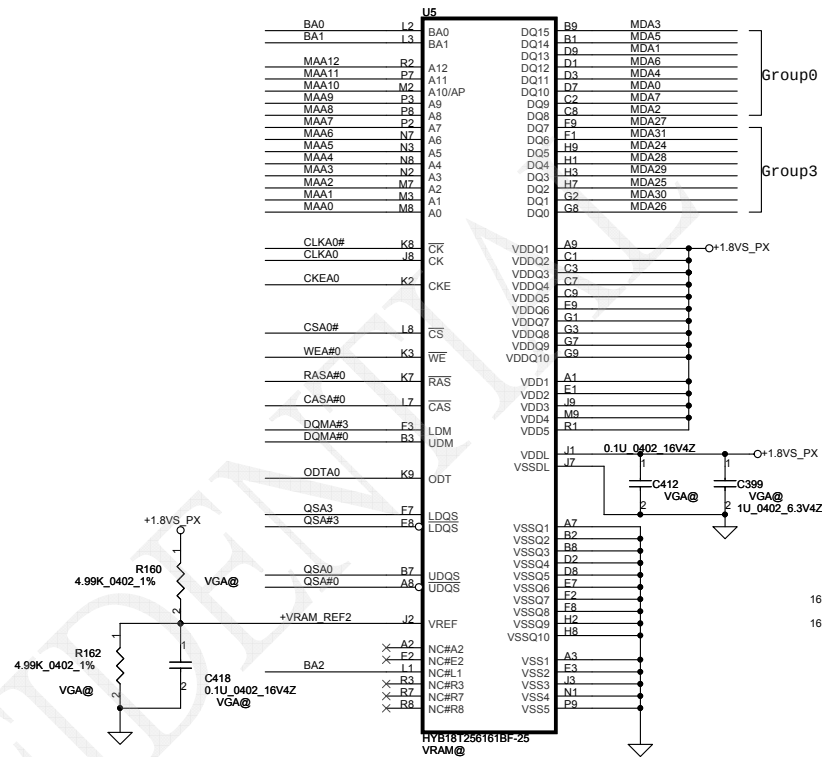
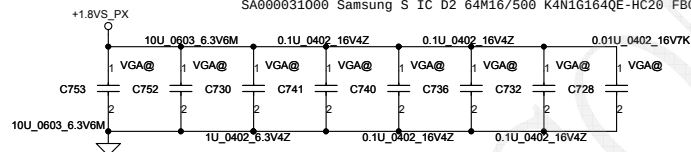


Use Delay 3.3V BUS (VDDR3) for GPIO/DDC Pull up to reduce Leakage to VDDR3 Bus.

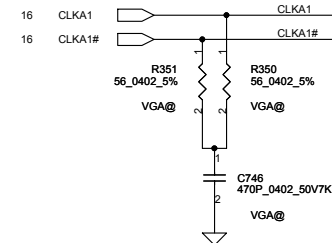
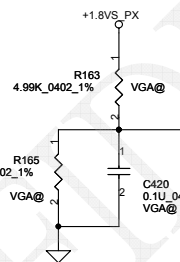
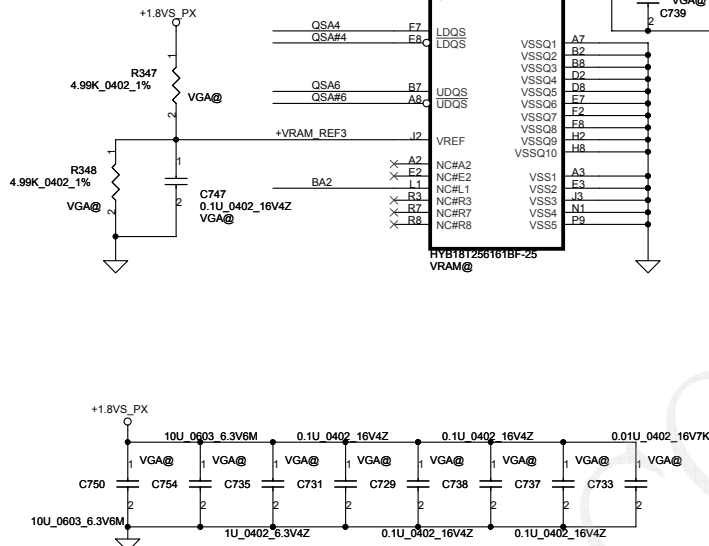
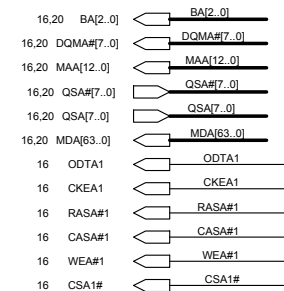
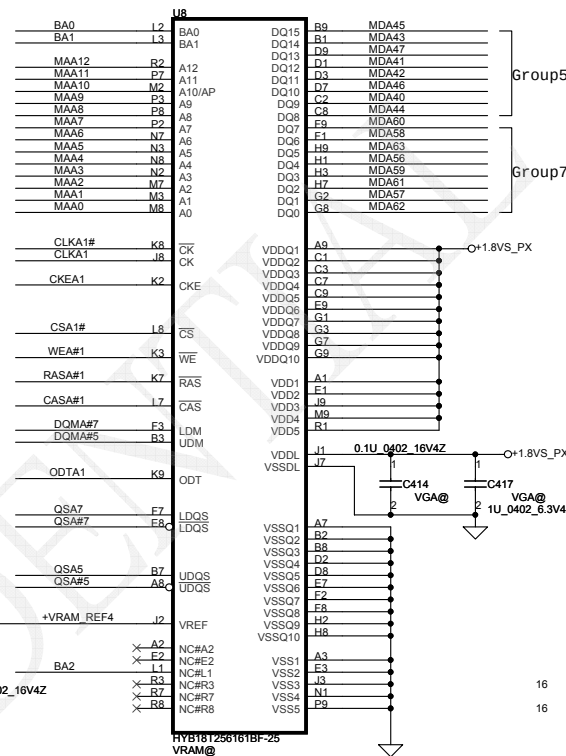
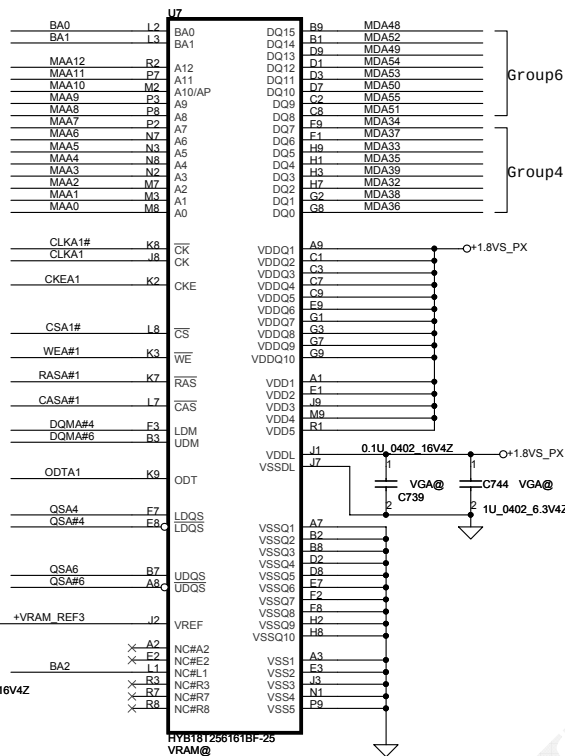
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								Custm		401679		C	
								Date:		Thursday, March 26, 2009		Sheet 19 of 57	



SA00002UH00 HYNIX S IC D2 64M16/500 H5PS1G63EFR-20L FBGA84
 SA00002MF00 Qimonda S IC D2 64M16/500 HYB18T1G161C2F-20
 SA00002MD00 Samsung S IC D2 64M16/500 K4N1G1640Q-HC20 FBGA84
 SA000031000 Samsung S IC D2 64M16/500 K4N1G164QE-HC20 FBGA 84P

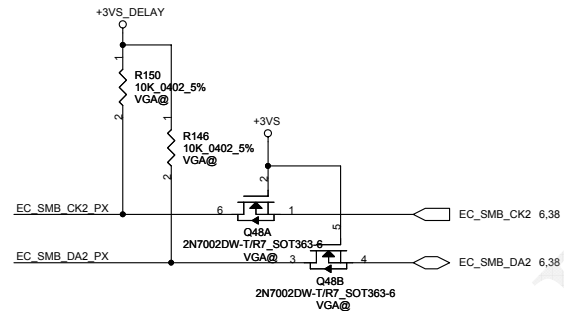
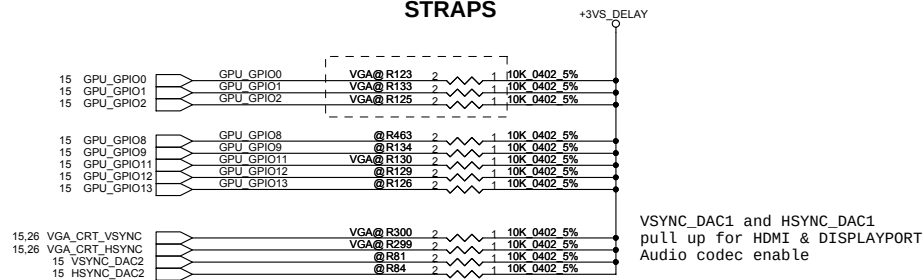


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				Date	Thursday, March 26, 2009
				Sheet	20 of 57
				Rev	C

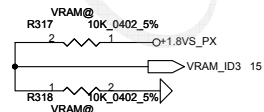
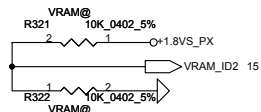
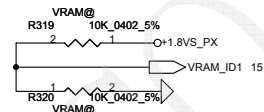
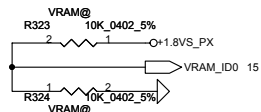
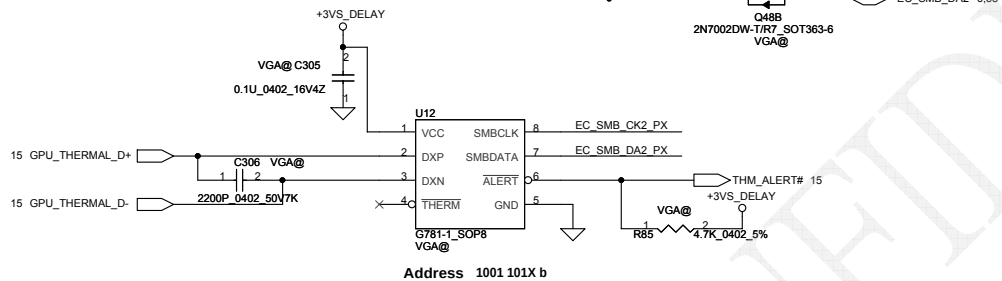


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						Document Number			
						401679			
						Date			
						Thursday, March 26, 2009			
						Sheet			
						21 of 57			
						Rev			
						C			

STRAPS



External VGA Thermal Sensor



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable	1 : PCIe bus Full Tx output swing 0 : PCIe bus 50% Tx output swing
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable	1 : Tx de-emphasis enabled 0 : Tx de-emphasis disabled
BIF_GEN2_EN_A	GPIO2	PCIe GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 (5.0 GT/s capability will be controlled by software)
VGA_DIS	GPIO9	VGA Disable determines whether or not the card will be recognized as the system's VGA controller	0 : VGA Controller capacity enabled 1 : The device will not be recognized as the system's VGA controller
CONFIG(2:0)	GPIO[13:11]	Size of the primary memory apertures	0 0 1
VIP_DEVICE_STRAP_EN	V2SYNC		0
RESERVED	H2SYNC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11
RESERVED	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		0: Disable external BIOS ROM device 1: Enable external BIOS ROM device
CCBPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0

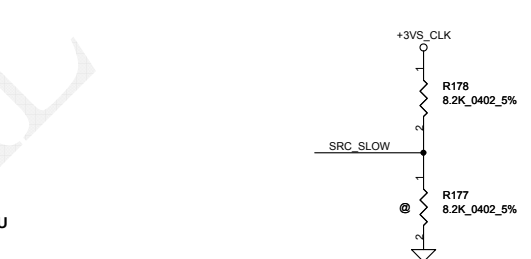
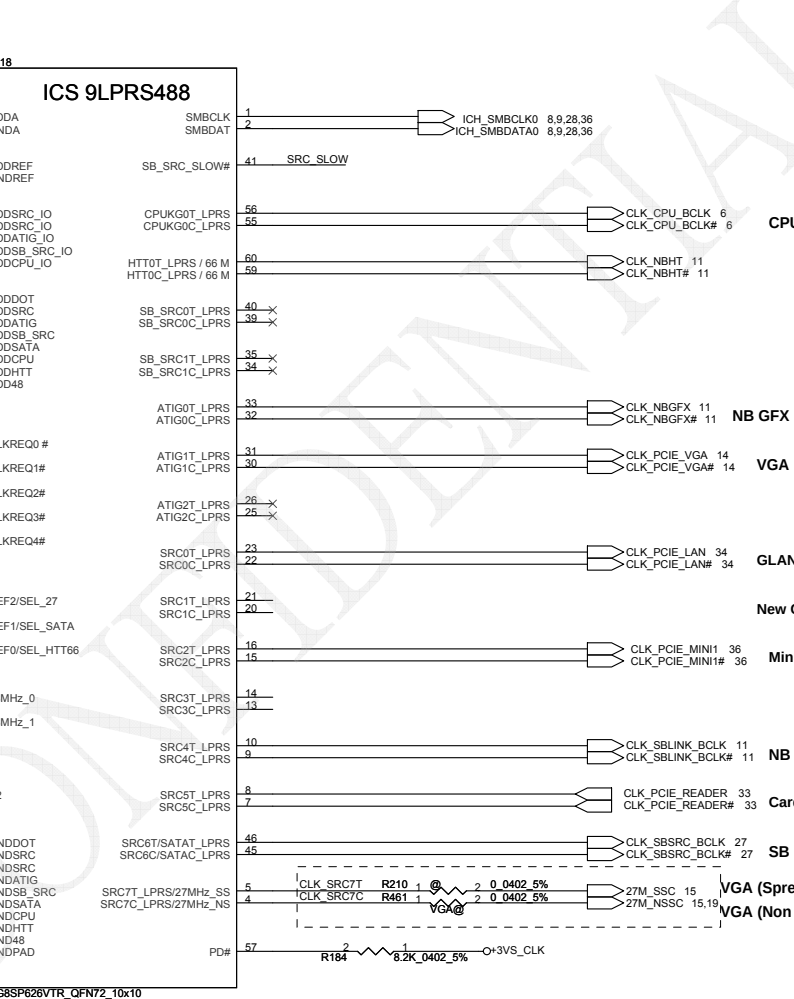
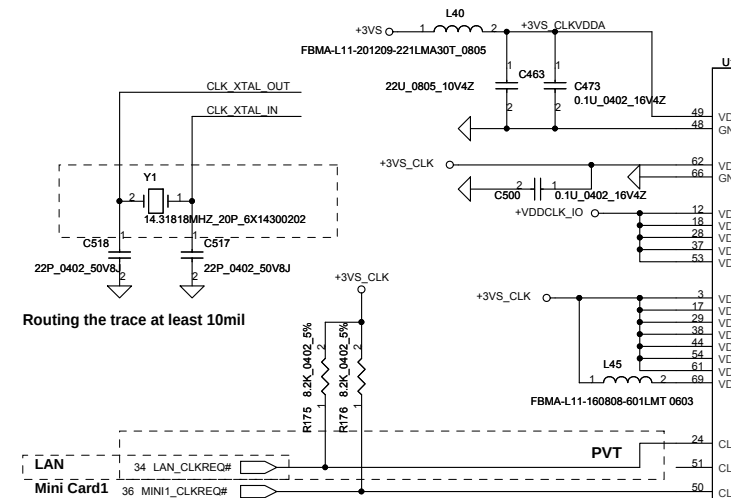
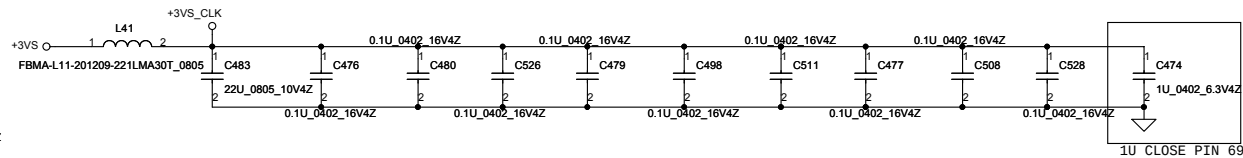
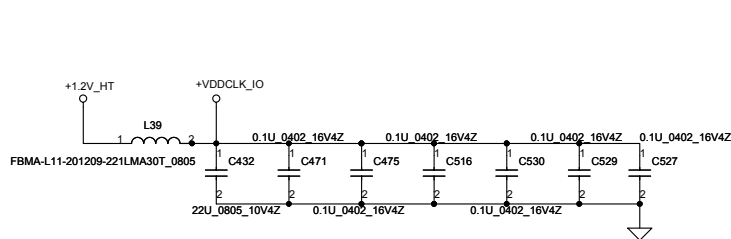
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

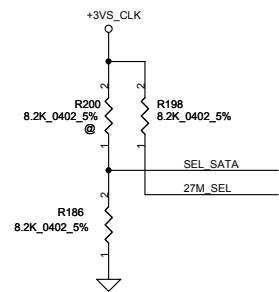
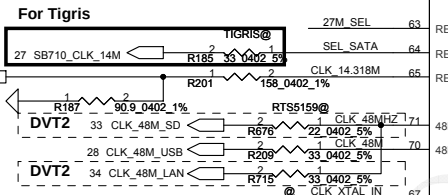
H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPI0_28_TDO	GPI021_BB_EN

STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (23,22,21,20)	M92-M2 XT	JV40-PU_KBLG0	512M(x4)	Samsung 64Mx16 1.8V (Q-die)	SA00002MD00	0 0 0 0
			JV40-PU_KBLG0	512M(x4)	Hynix 64Mx16 1.8V	SA00002UH20	0 0 0 1
			JV40-PU_KBLG0	512M(x4)	Qimonda 64Mx16 1.8V	SA00002MF0PVT	0 0 1 0
			JV40-PU_KBLG0	512M(x4)	Samsung 64Mx16 1.8V (E-die)	SA000031O10	0 1 0 0

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				401679	
Date:	Thursday, March 26, 2009	Sheet	22	of	57



CLK_NB_14.318M
RS780



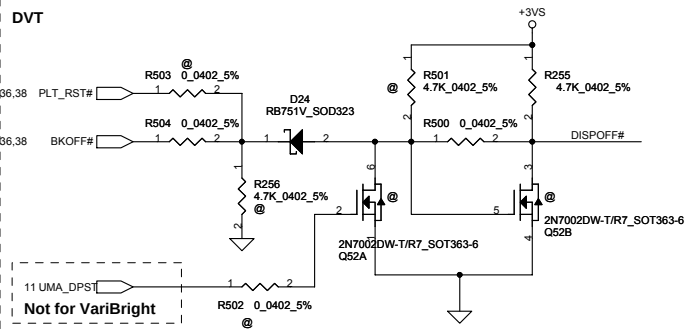
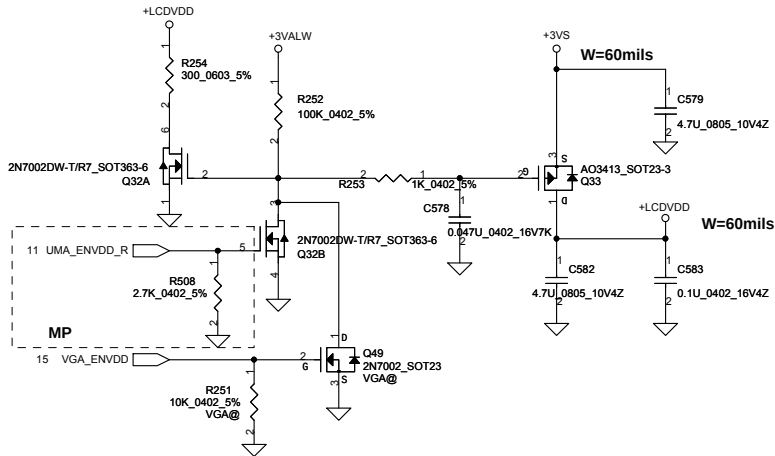
1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN
2nd (ICS) : SA000023H10 S IC ICS9LPRS488CLKLT MLF 72P CLK GEN

NB CLOCK INPUT TABLE

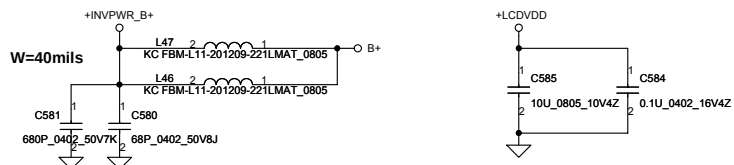
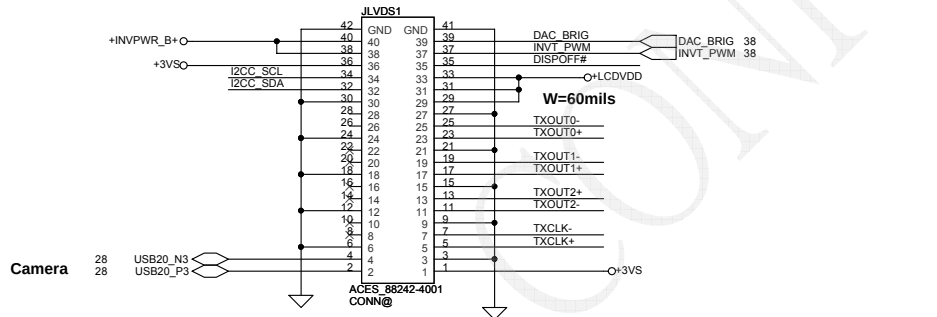
NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	68M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)
GPP_REFCLK	NC	100M DIFF	NC
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

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Date		Thursday, March 26, 2009		Sheet		23		of 57			

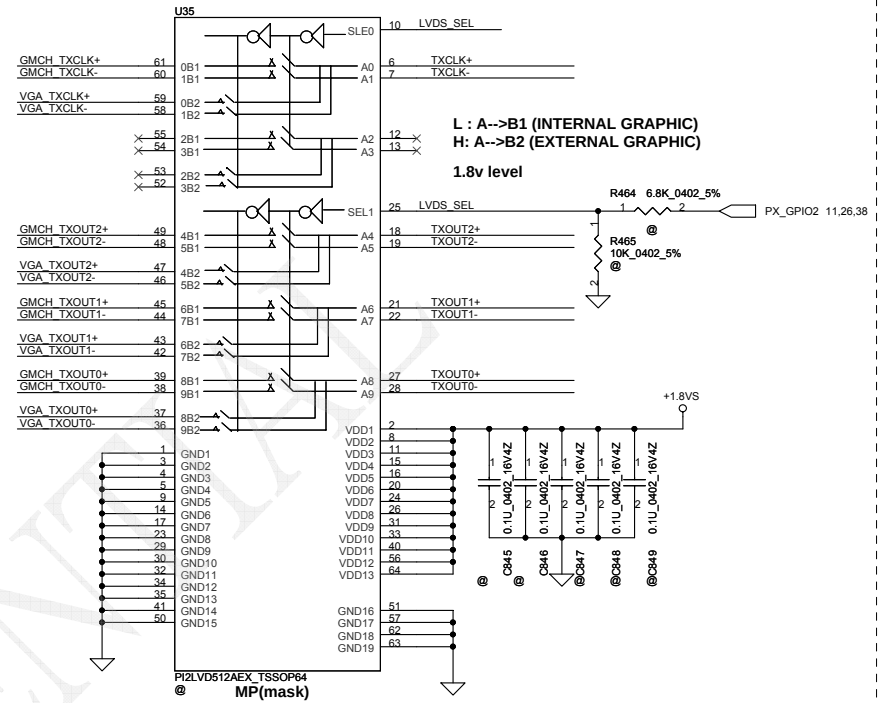
LCD POWER CIRCUIT



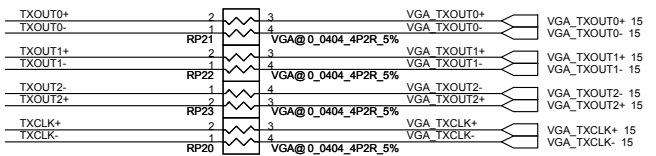
LCD/PANEL BD. Conn.



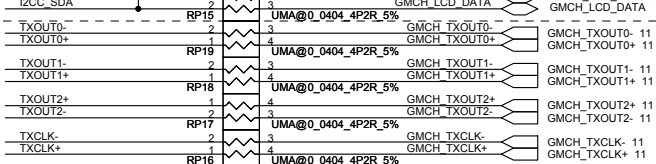
DVT



DVT

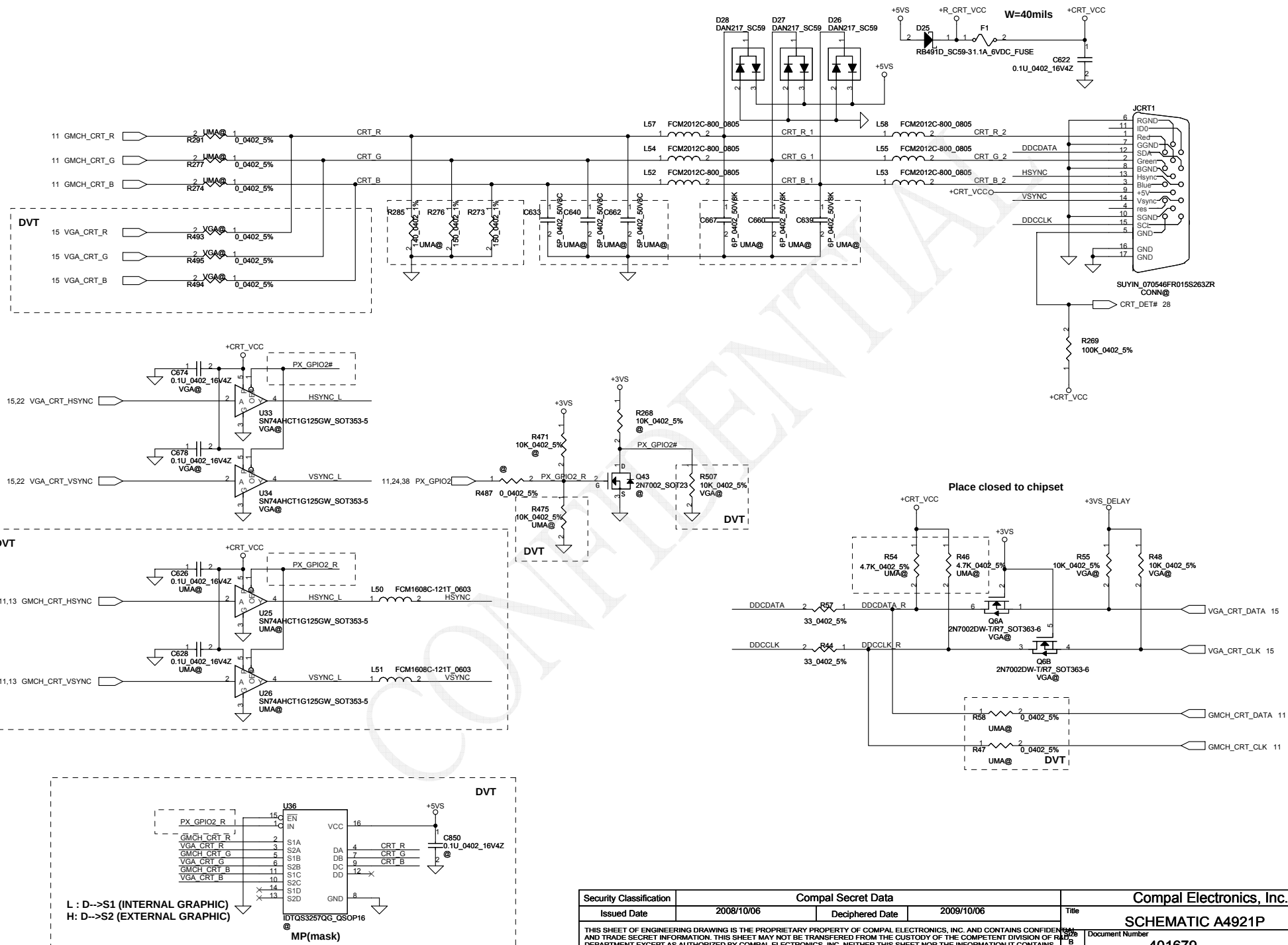


DVT



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								Document Number		401679		Rev C	
								Date		Thursday, March 26, 2009		Sheet 24 of 57	

CRT CONNECTOR

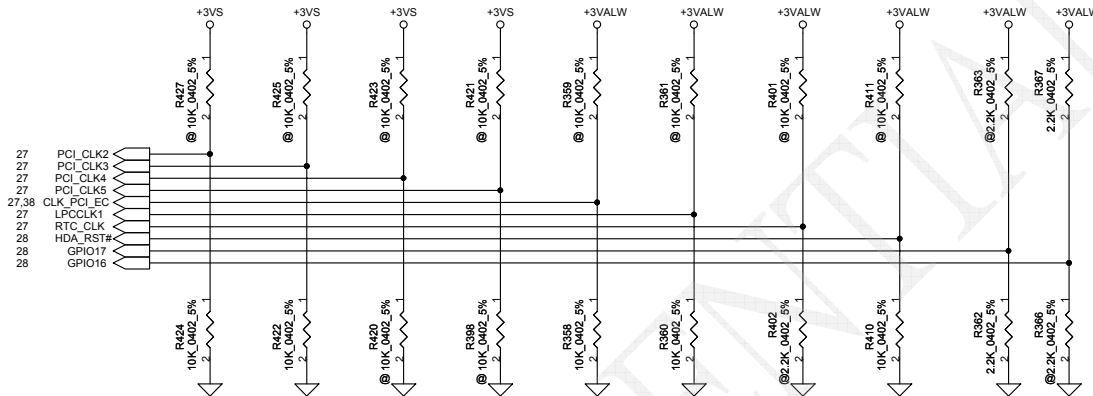


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				A	401679
Date:		Thursday, March 26, 2009		Sheet	26 of 57

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

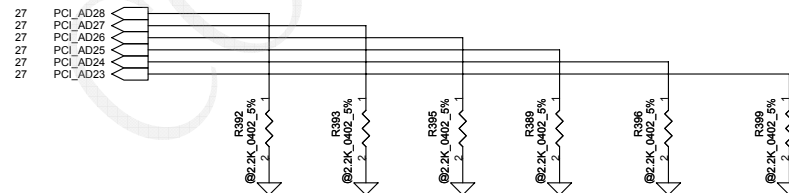
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	L,H = LPC ROM (Default L,NC) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



DEBUG STRAPS

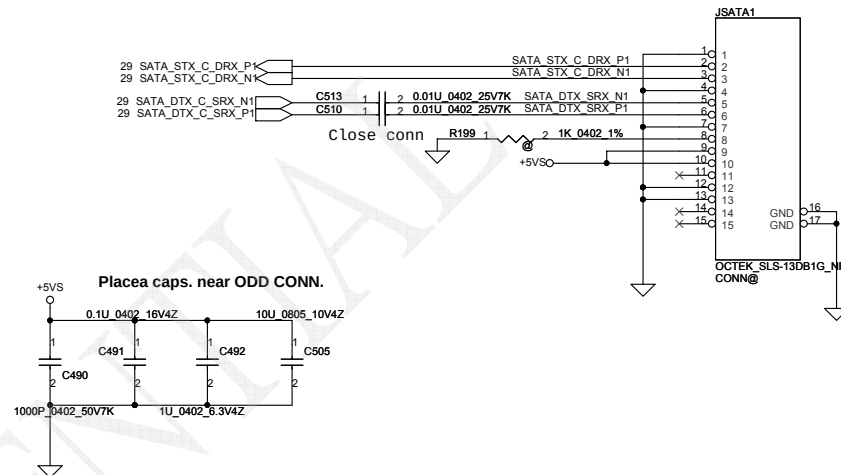
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

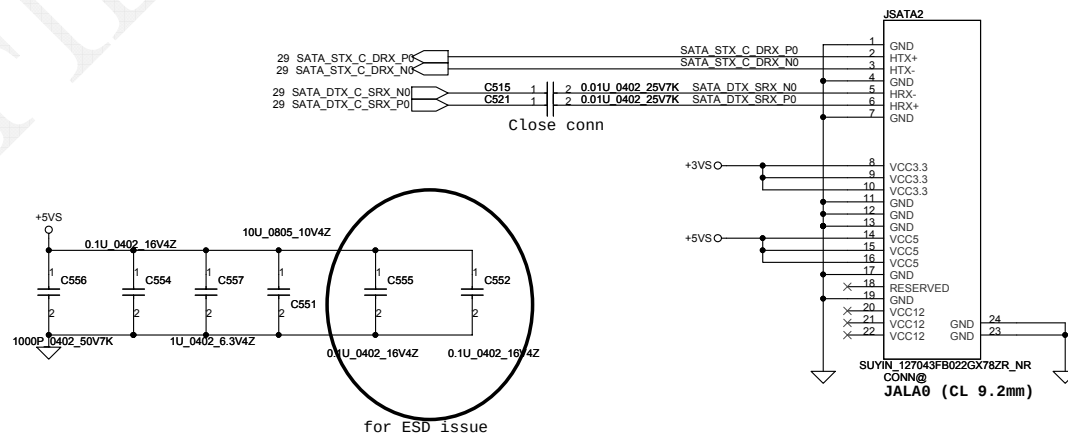


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				Date	Thursday, March 26, 2009
				Sheet	31 of 57

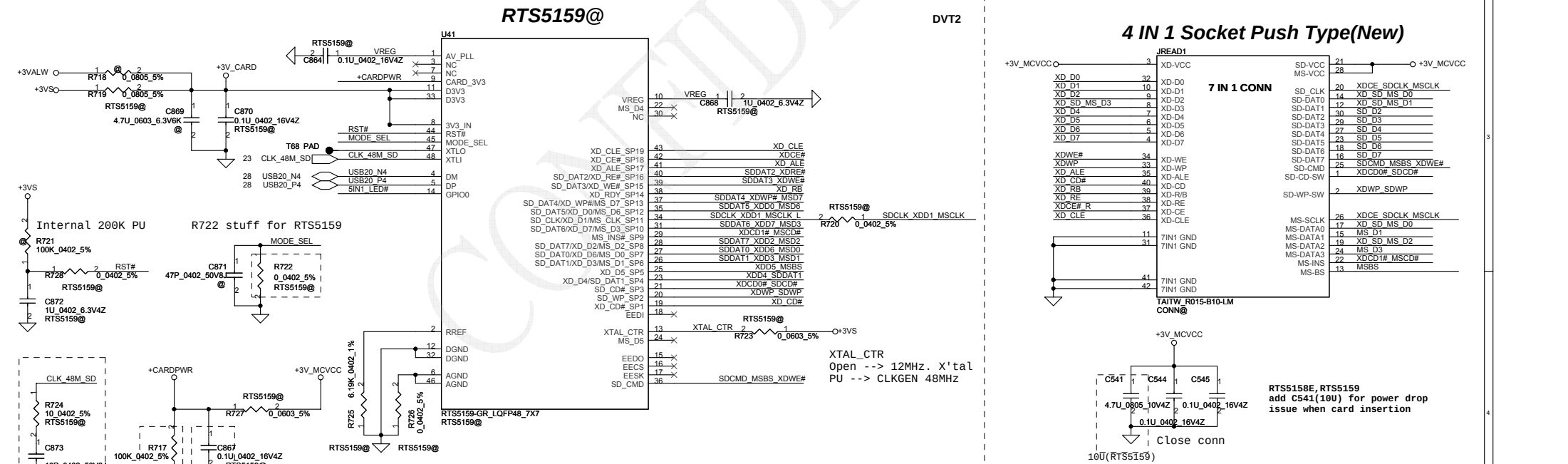
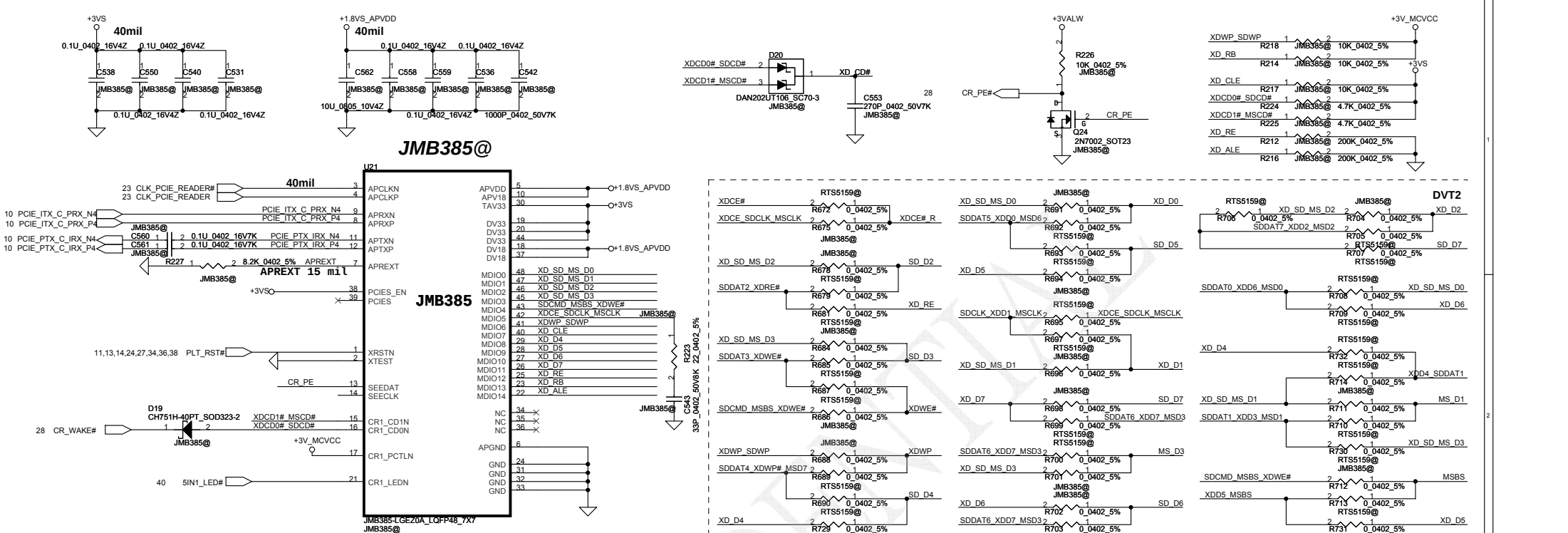
SATA ODD Conn.

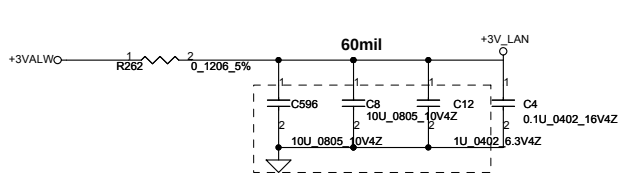


SATA HDD Conn.

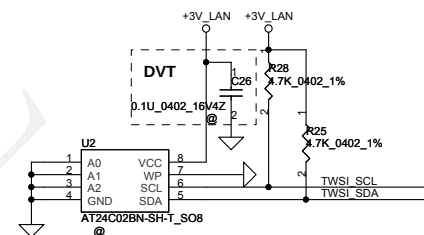
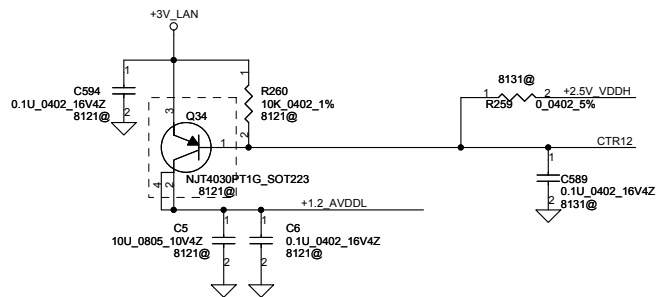


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						B		401679		C	
DATE						Thursday, March 26, 2009		Sheet		32 of 57	

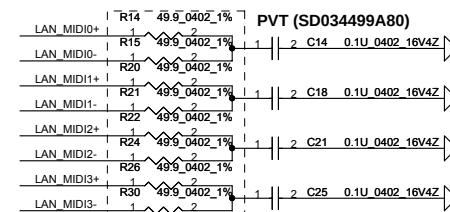




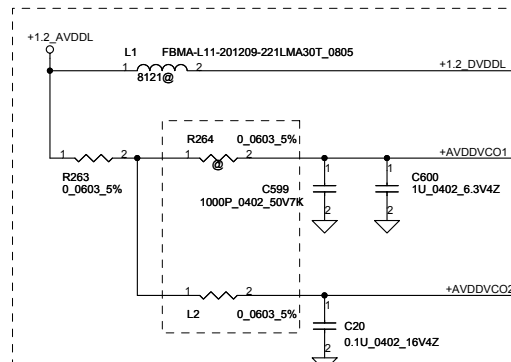
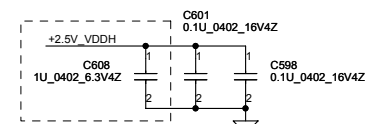
Place Close to Pin 2



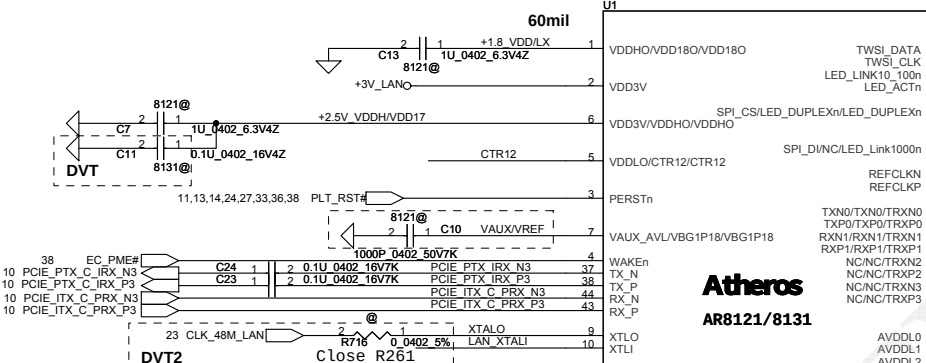
Place Close to LAN chip



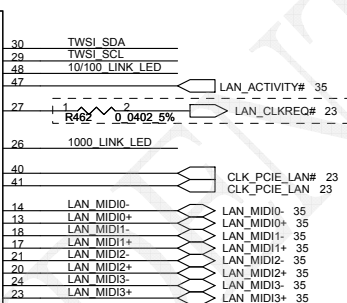
Place Close to Pin15, 19, 25
C608 close to Pin15



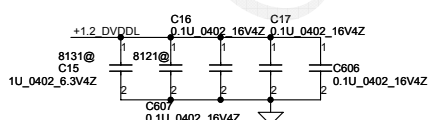
If overclocking, R264 , L2 stuffed and R263 removed.
If not overclocking, R263 , L2 stuffed and R264 removed.
AR8131:L2=80hm (more power saving mode)



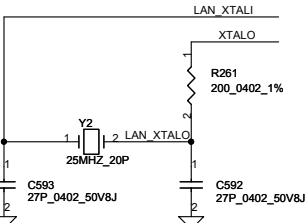
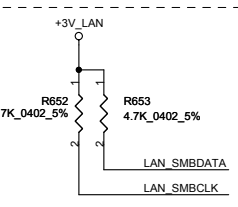
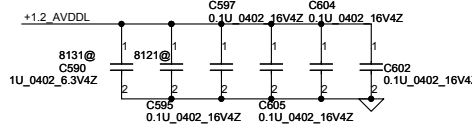
Atheros
AR8121/8131



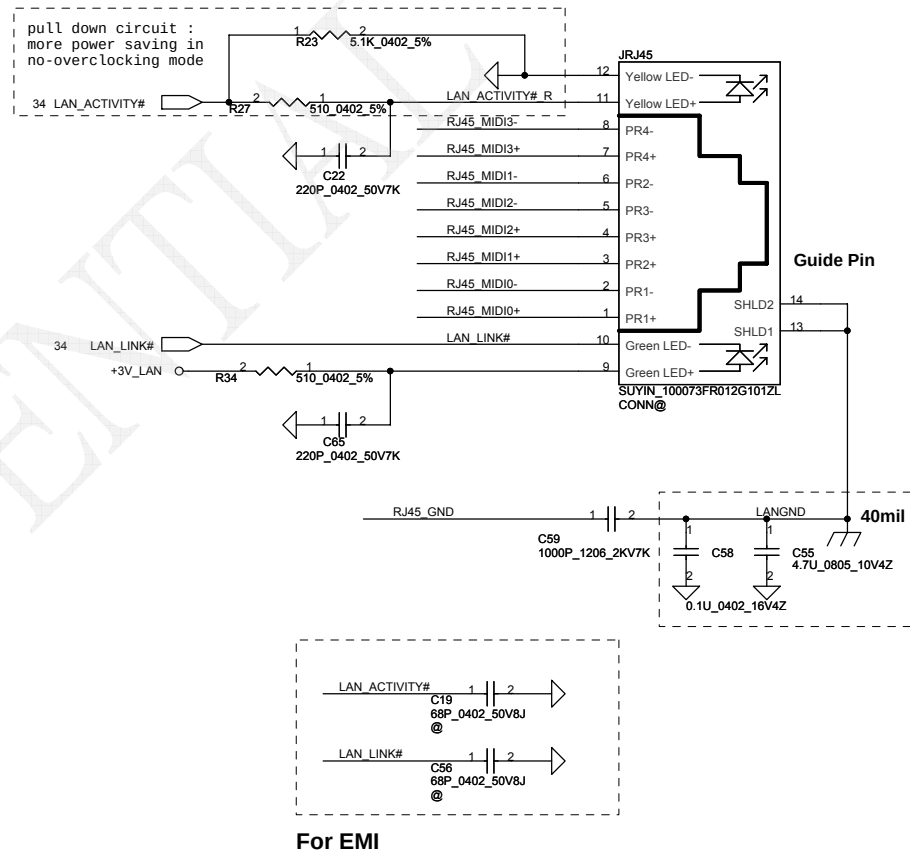
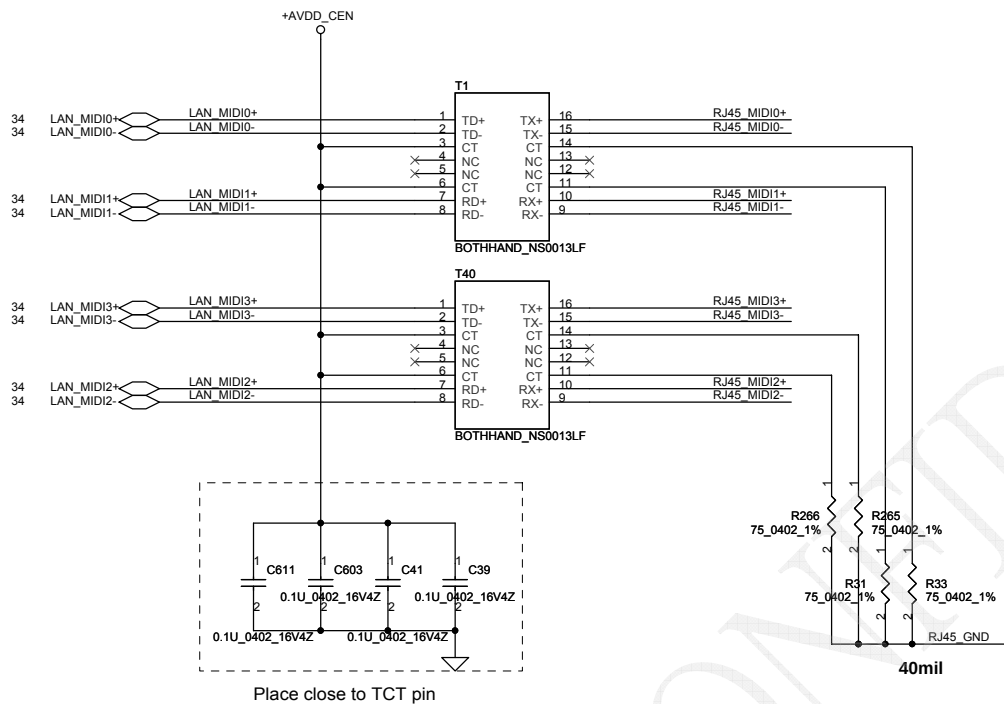
Place Close to Pin 28, 32, 45, 46
C15 and C607 close to Pin46
C16 close to Pin45



Place Close to Pin8, 16, 22, 36, 39
C590 and C595 close to Pin8

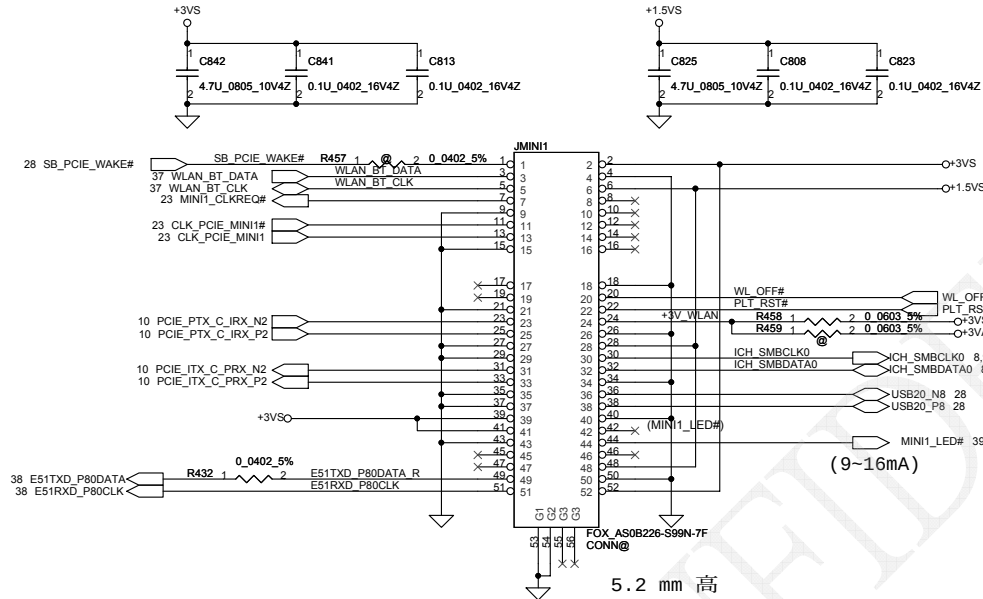


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				401679	C
				Date: Thursday, March 26, 2009	Sheet 34 of 57



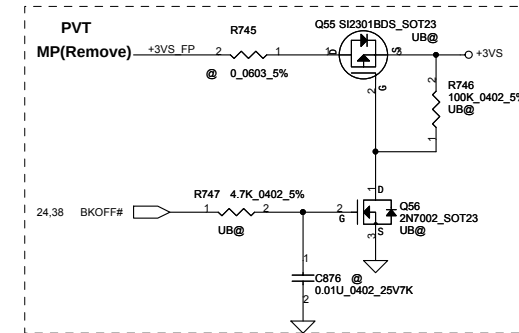
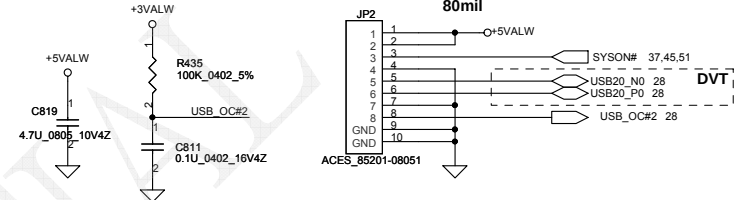
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				Date	Thursday, March 26, 2009
				Sheet	35 of 57

For Wireless LAN

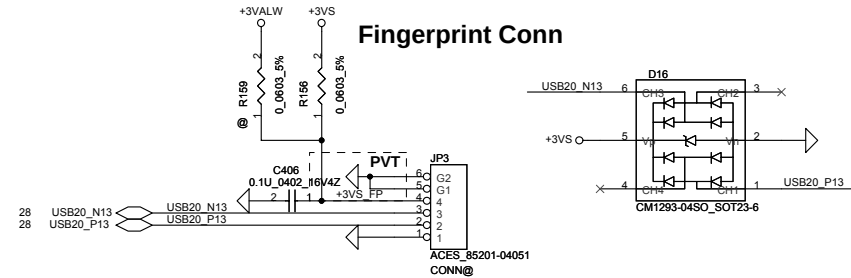


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	
+3VS	1000	750	Normal
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

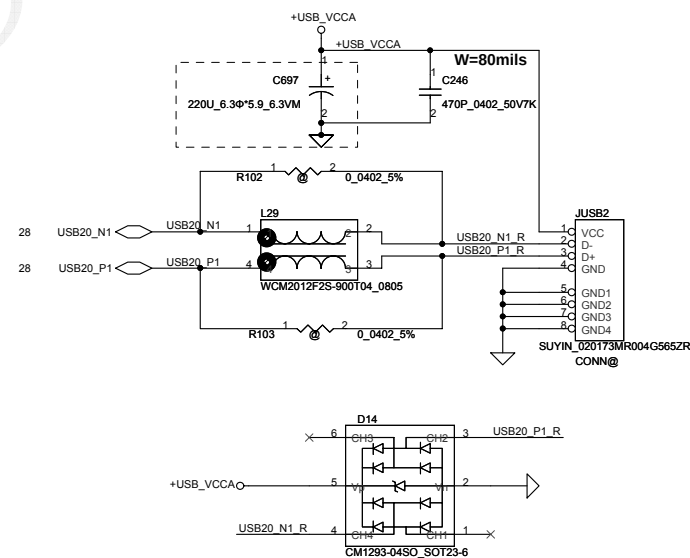
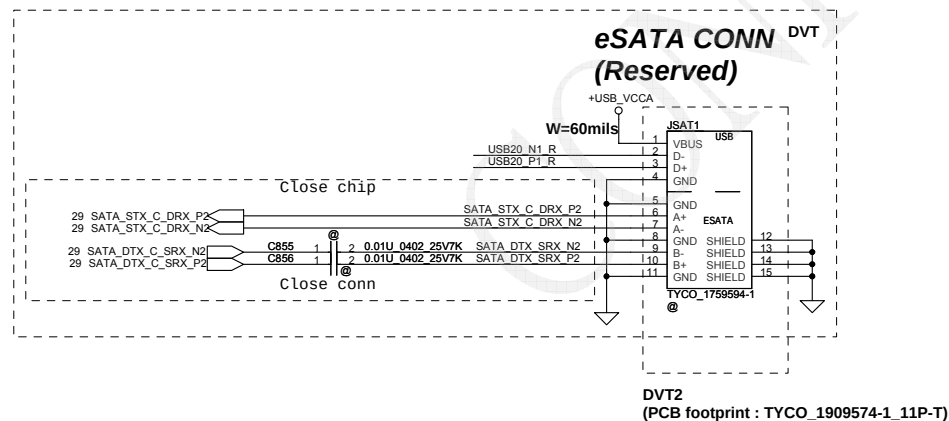
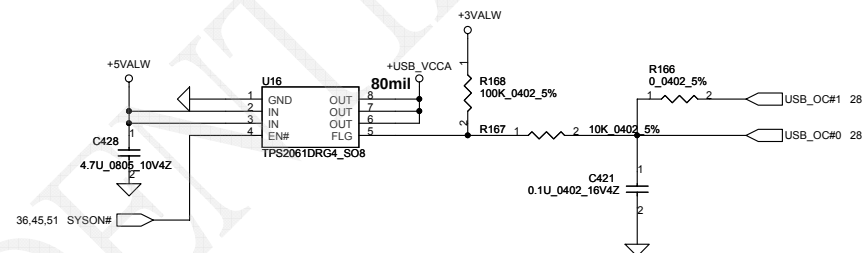
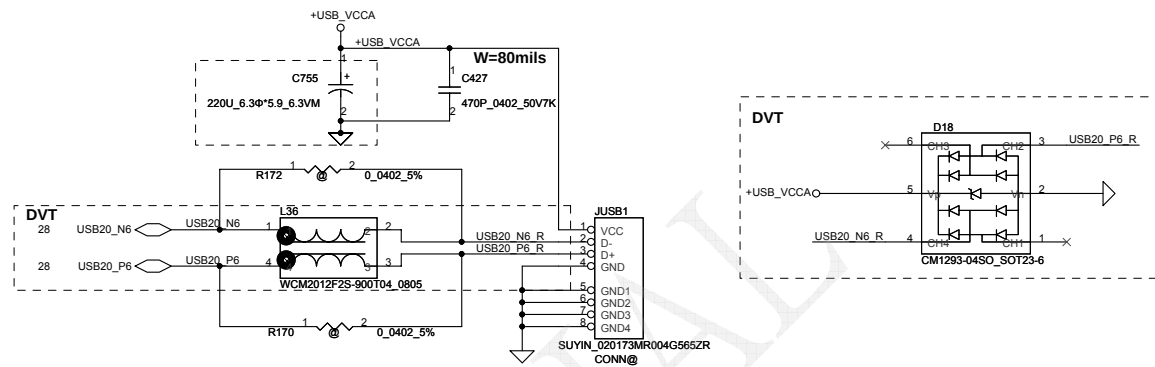
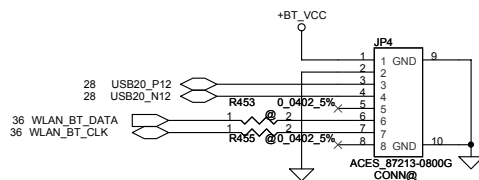
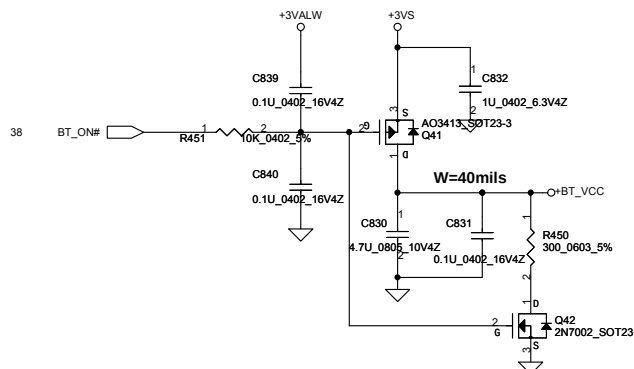
To USB/B Connector



Fingerprint Conn

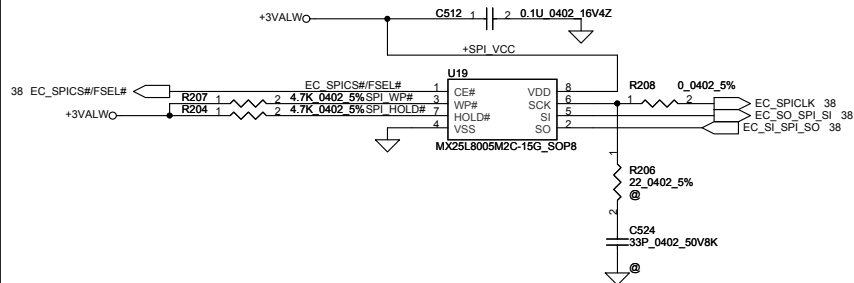


Bluetooth Conn.

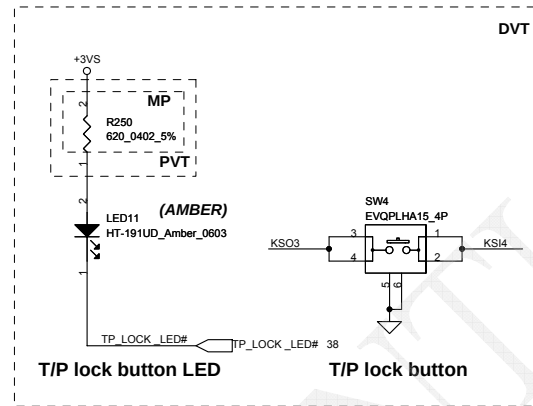
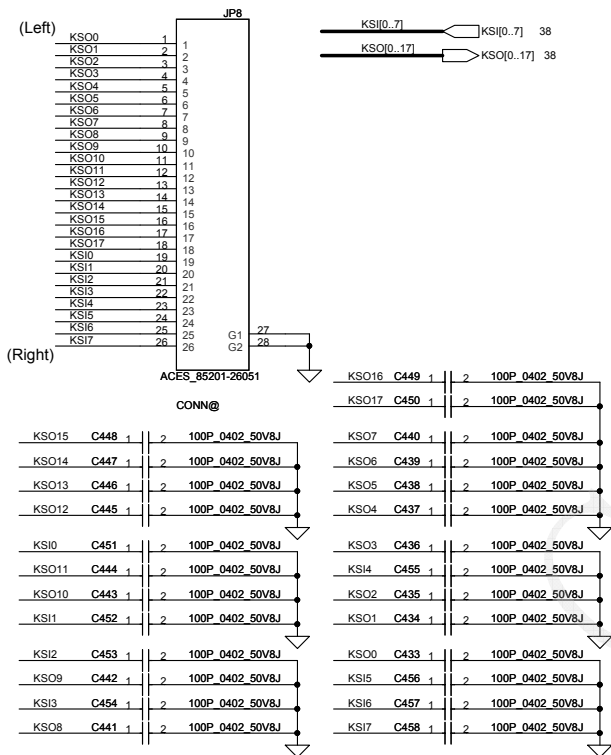


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				401679	
				Date	Thursday, March 26, 2009
				Sheet	37 of 57

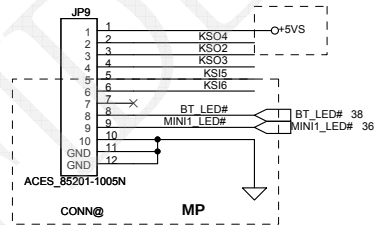
BIOS(SYS / EC / VGA)



INT_KBD Conn.

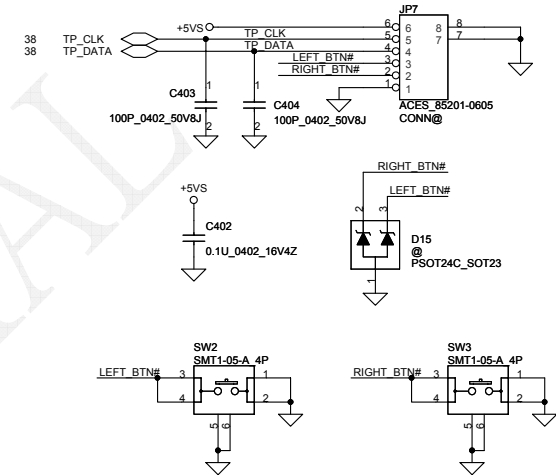


To FUN/B Conn (10PIN)

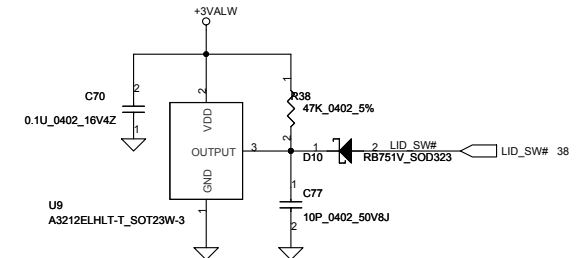


	KSO4	KSO2	KSO3
KSI5	WL_BTN#	Volume Down	Back Up
KSI6	BT_BTN#	Volume Up	Program (KBLG0) Battery (KALG0)
KSI4			T/P lock

To TP/B Conn.

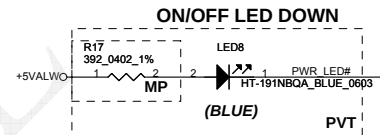
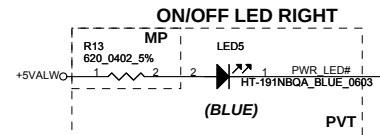
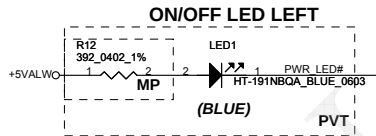
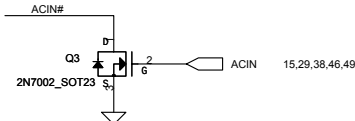
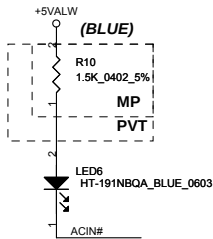
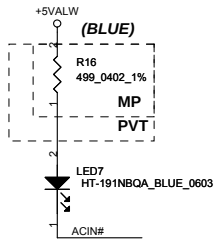


Lid Switch (Hall Effect Switch)

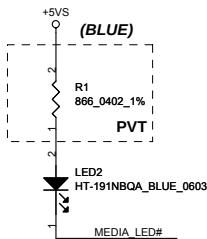


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				Date	Thursday, March 26, 2009
				Sheet	39 of 57

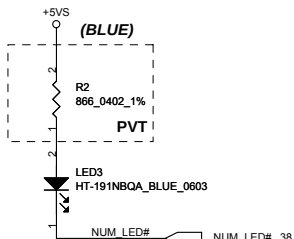
Enlightener LED



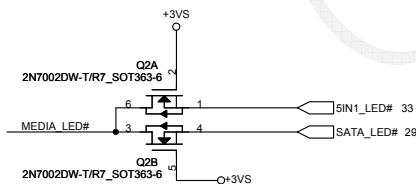
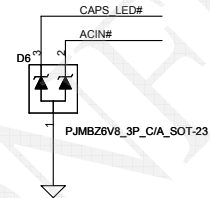
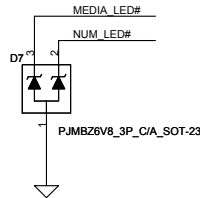
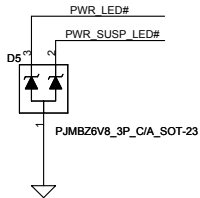
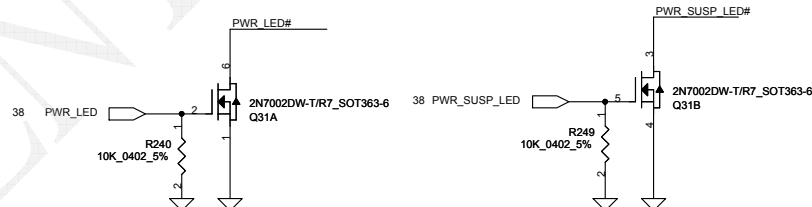
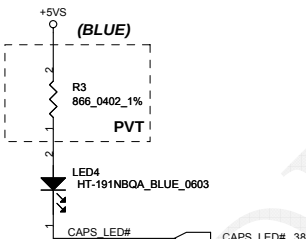
MEDIA_LED



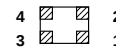
NUM_LED



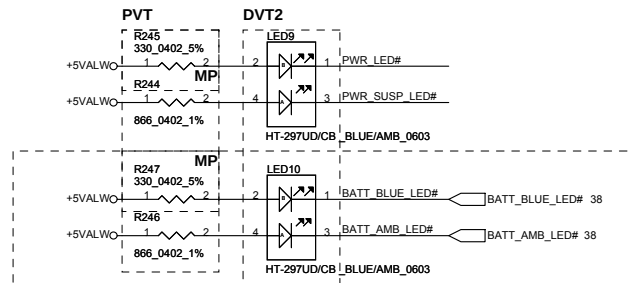
CAPS_LED



Compal Footprint



Footprint : LED_HT-297DQ-GQ_4P

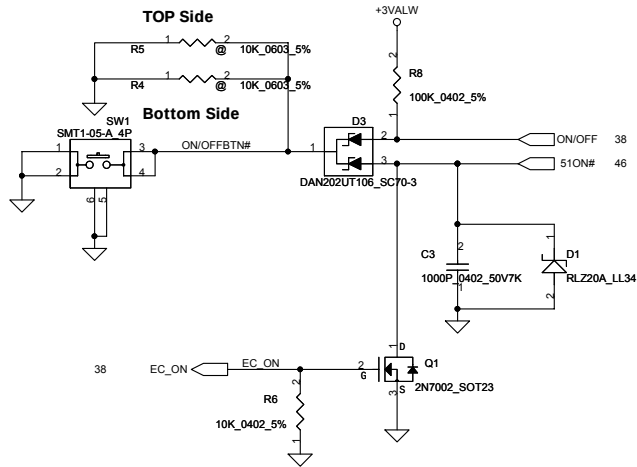


BLUE/AMBER

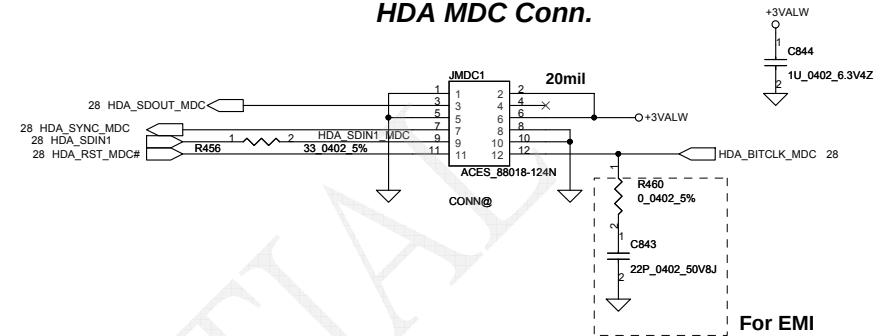
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				Date	Thursday, March 26, 2009	Sheet 40 of 57

Power Button

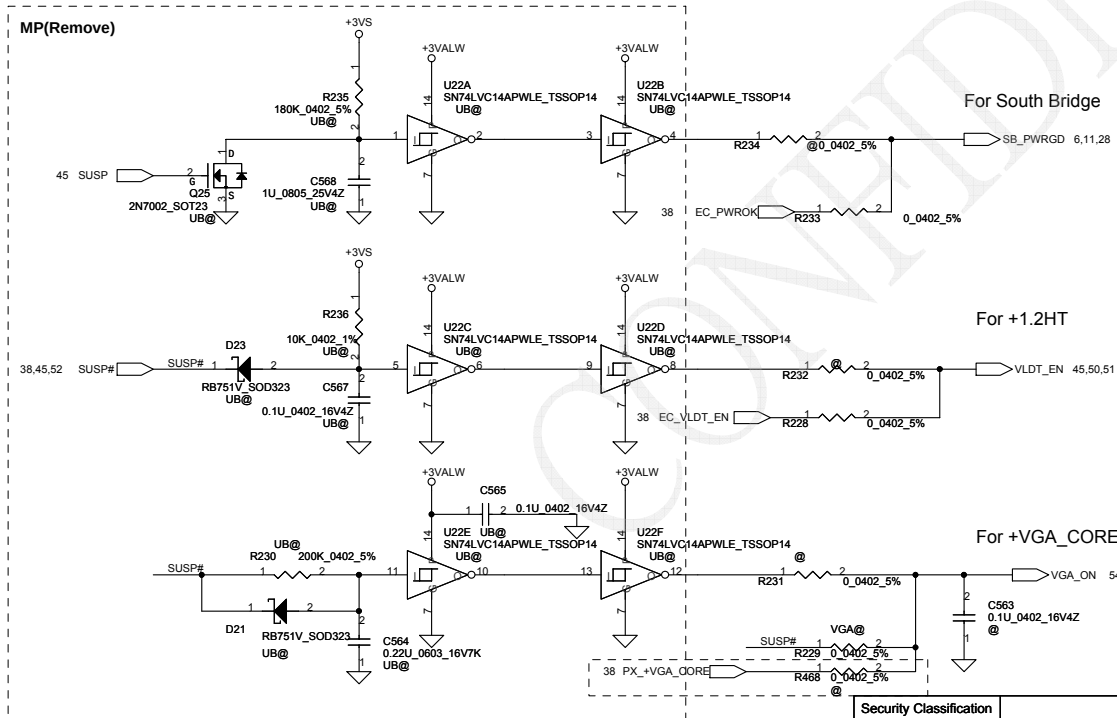
ON/OFF switch



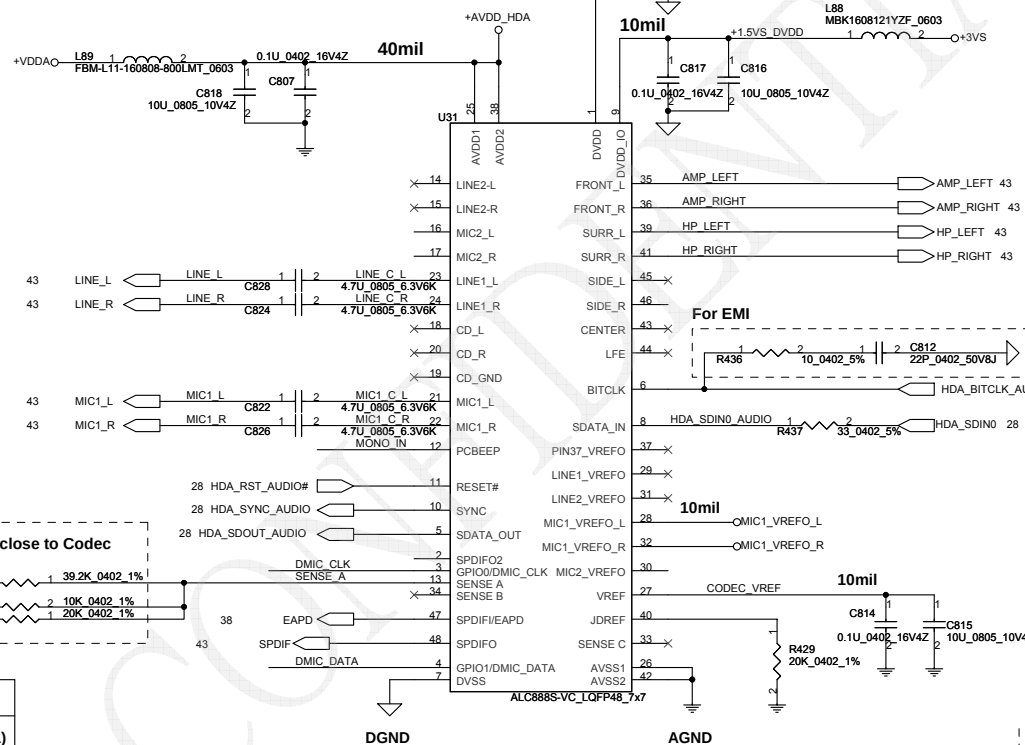
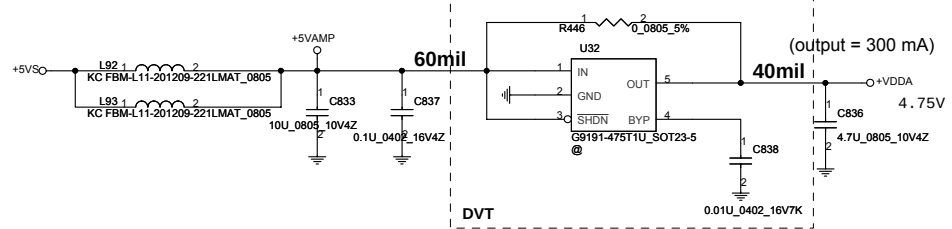
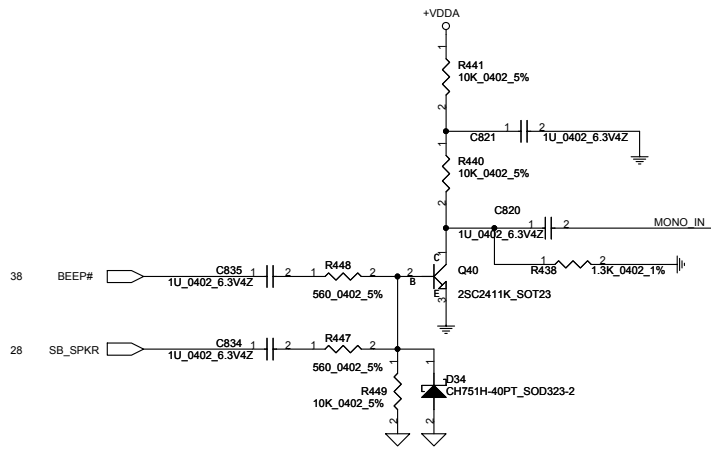
HDA MDC Conn.



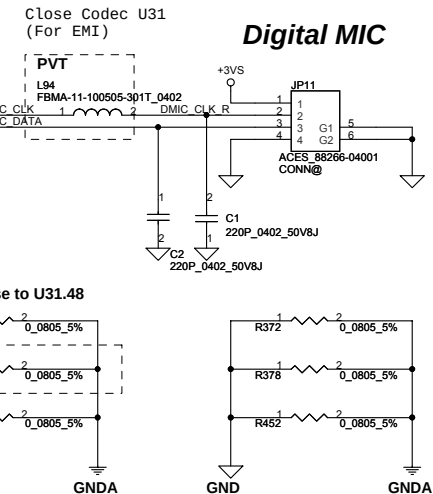
Power ON Circuit



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				Date	Thursday, March 26, 2009	Sheet 41 of 57



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



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				401679				Rev C			
				Date: Thursday, March 26, 2009				Sheet 42 of 57			

0mil
C_FAN1

D12
BAS16_SOT23-3
C121
10U_0805_10V4Z
C119
1000P_0402_50V7K

JP13
ACES_85205-03001
CONN@

H21
H_3P2

H10
H_3P2

H22
H_3P2

H26
H_3P2

H23
H_3P2

H27
H_3P2

H7
H_4P2

H14
H_4P2

H13
H_4P2

H9
H_4P2

H6
H_3P7N

H20
H_3P2

H12
H_3P2

H4
H_3P2

H3
H_3P2

H2
H_3P2

H15
H_3P2

H1
H_3P2

H16
H_3P2

H11
H_4P7X3P7N

H24
H_5P1X4P1N

H8
H_10P0X6P0N

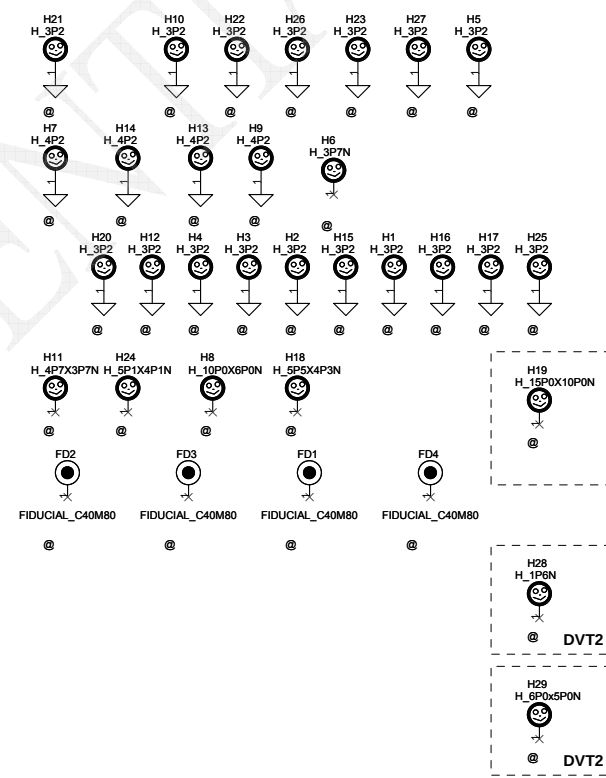
H18
H_5P5X4P3N

FD2
FIDUCIAL_C40M80

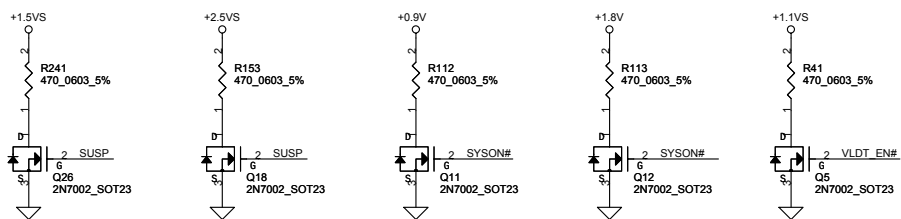
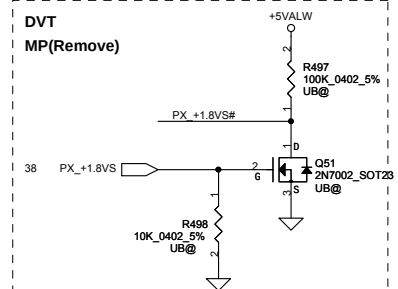
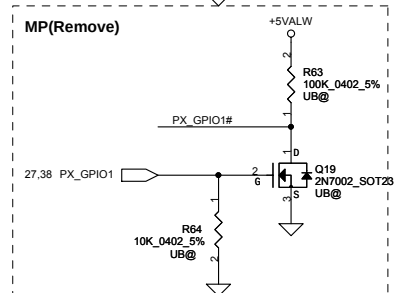
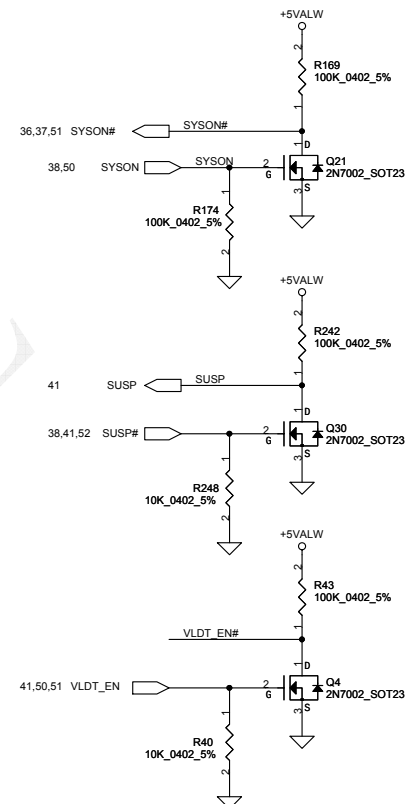
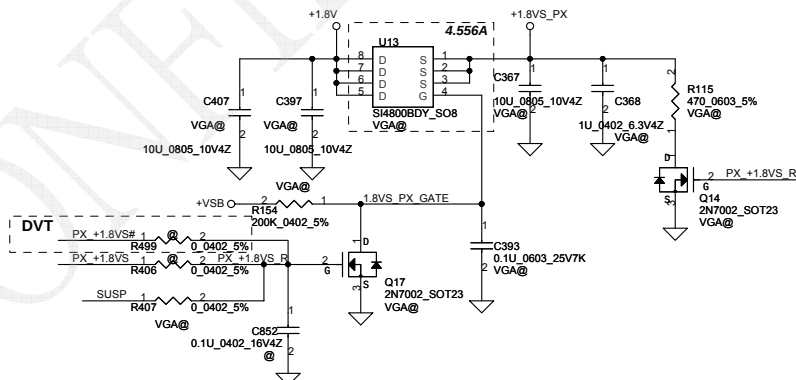
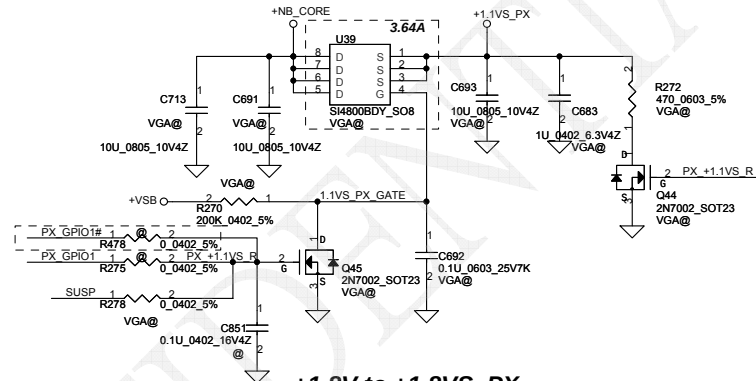
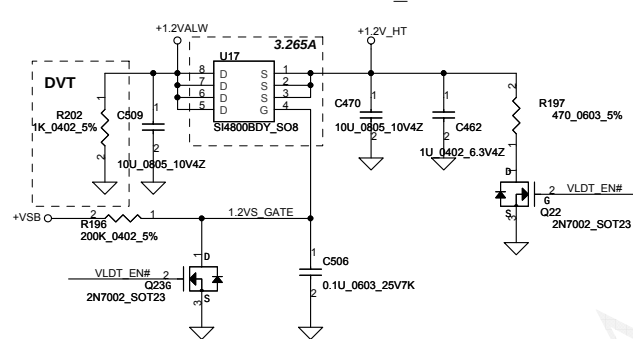
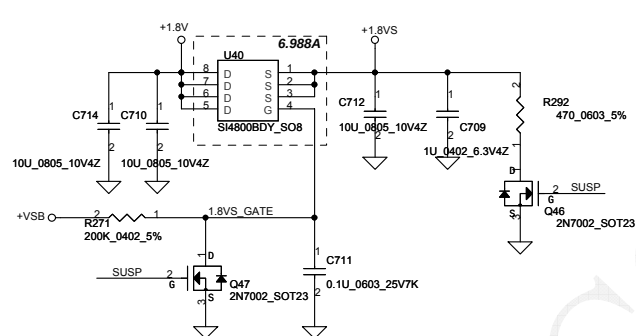
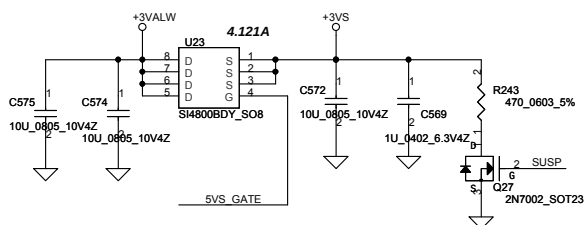
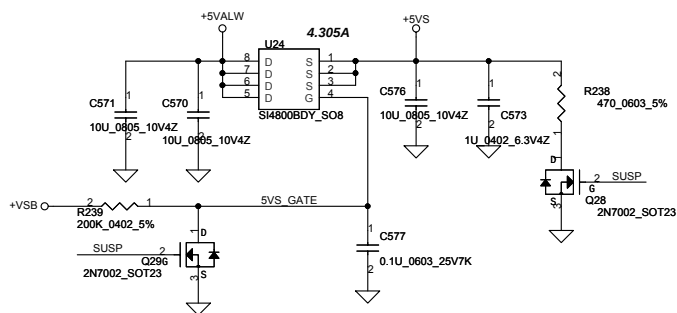
FD3
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FD1
FIDUCIAL_C40M80

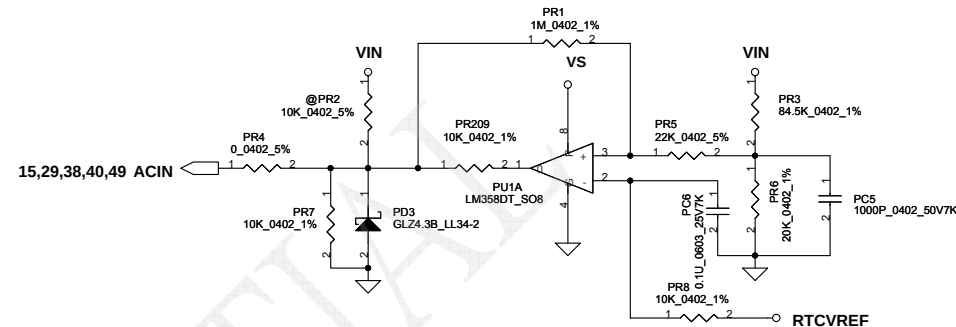
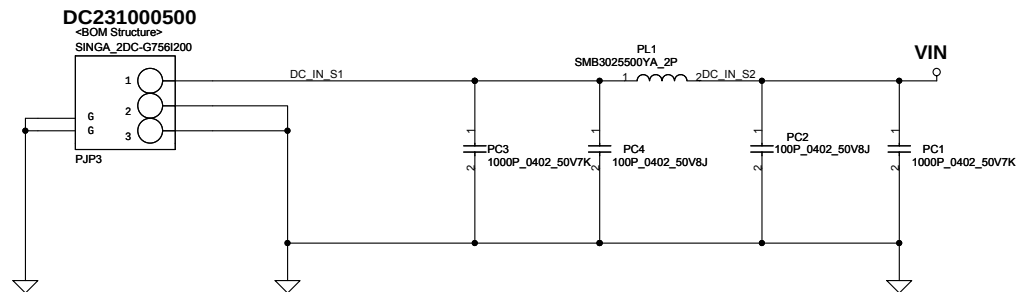
FD4
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				401679	
Date: Thursday, March 26, 2009		Sheet 44 of 57			

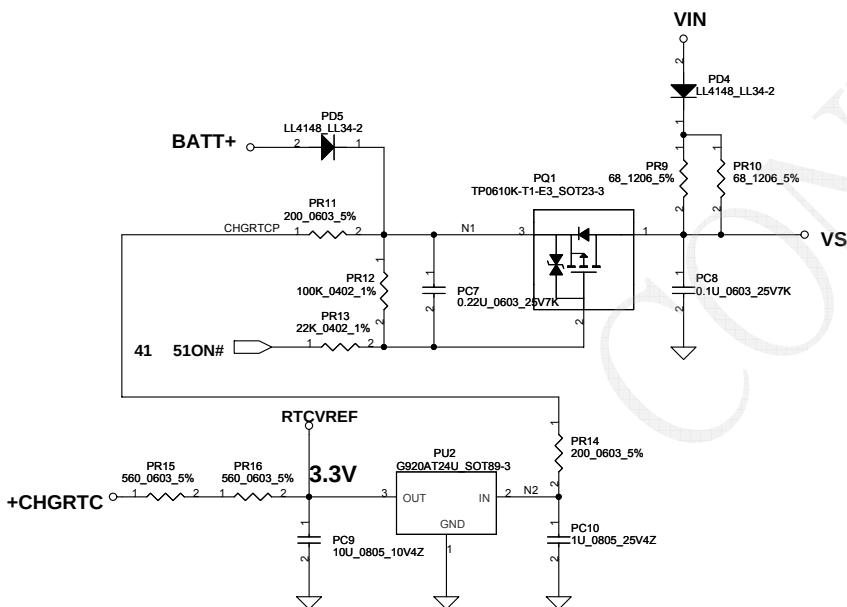
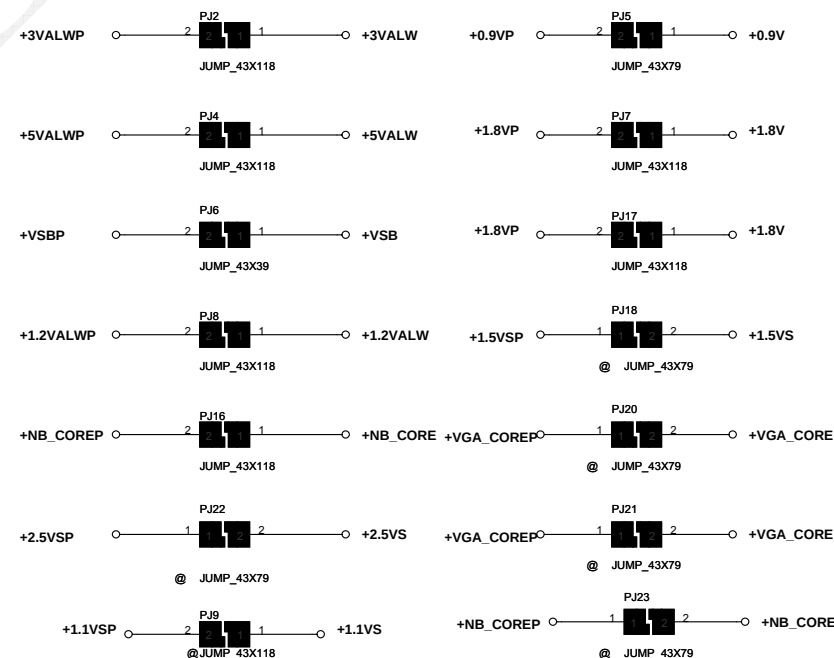
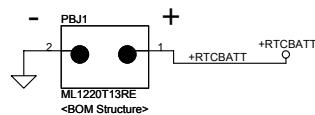


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				Date	Thursday, March 26, 2009	
				Sheet	45	of 57

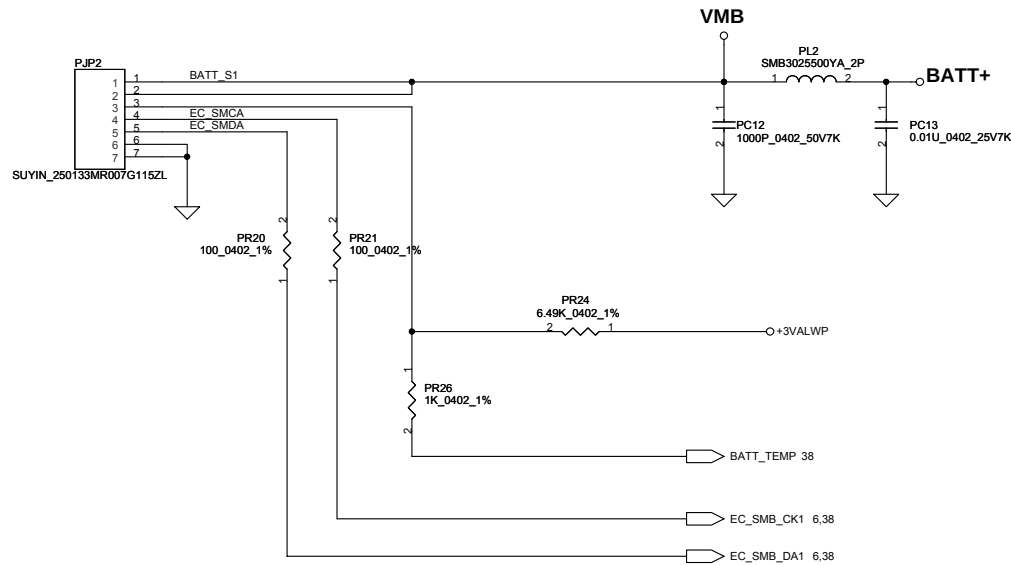


Vin Dectector

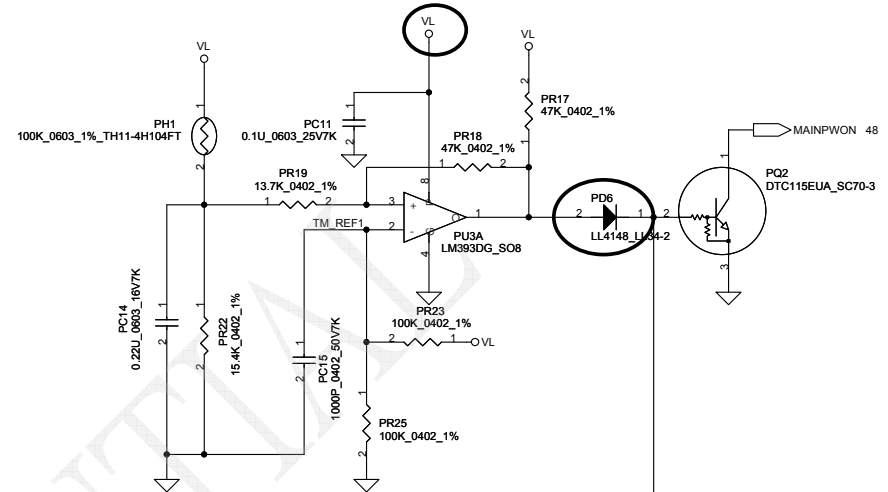
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



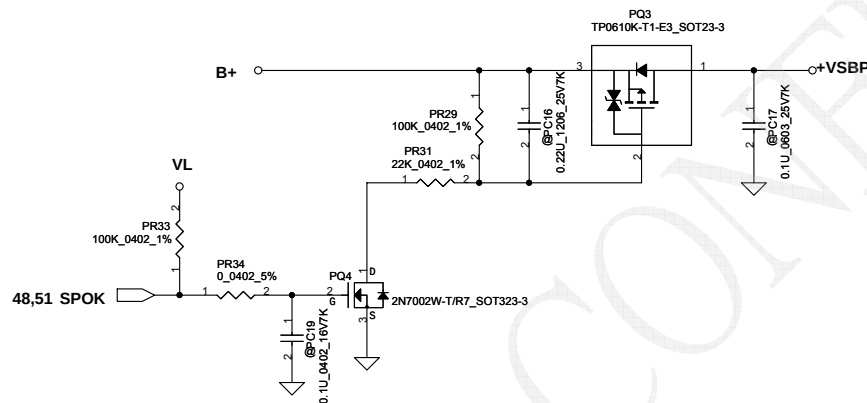
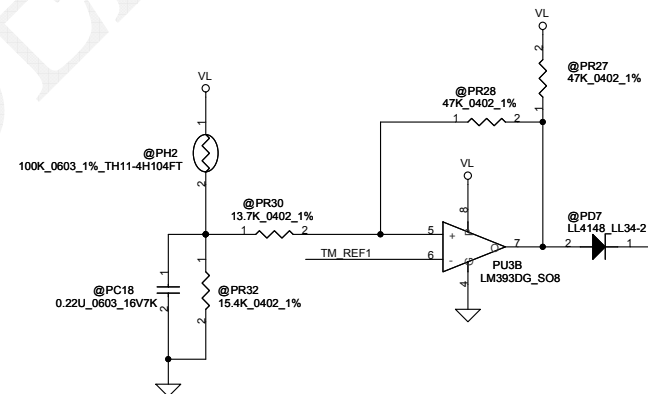
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				401679
				Rev C
				Date: Thursday, March 26, 2009
				Sheet 46 of 57



PH1 under CPU botten side :
CPU thermal protection at 93 degree C
Recovery at 57 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 47 degree C



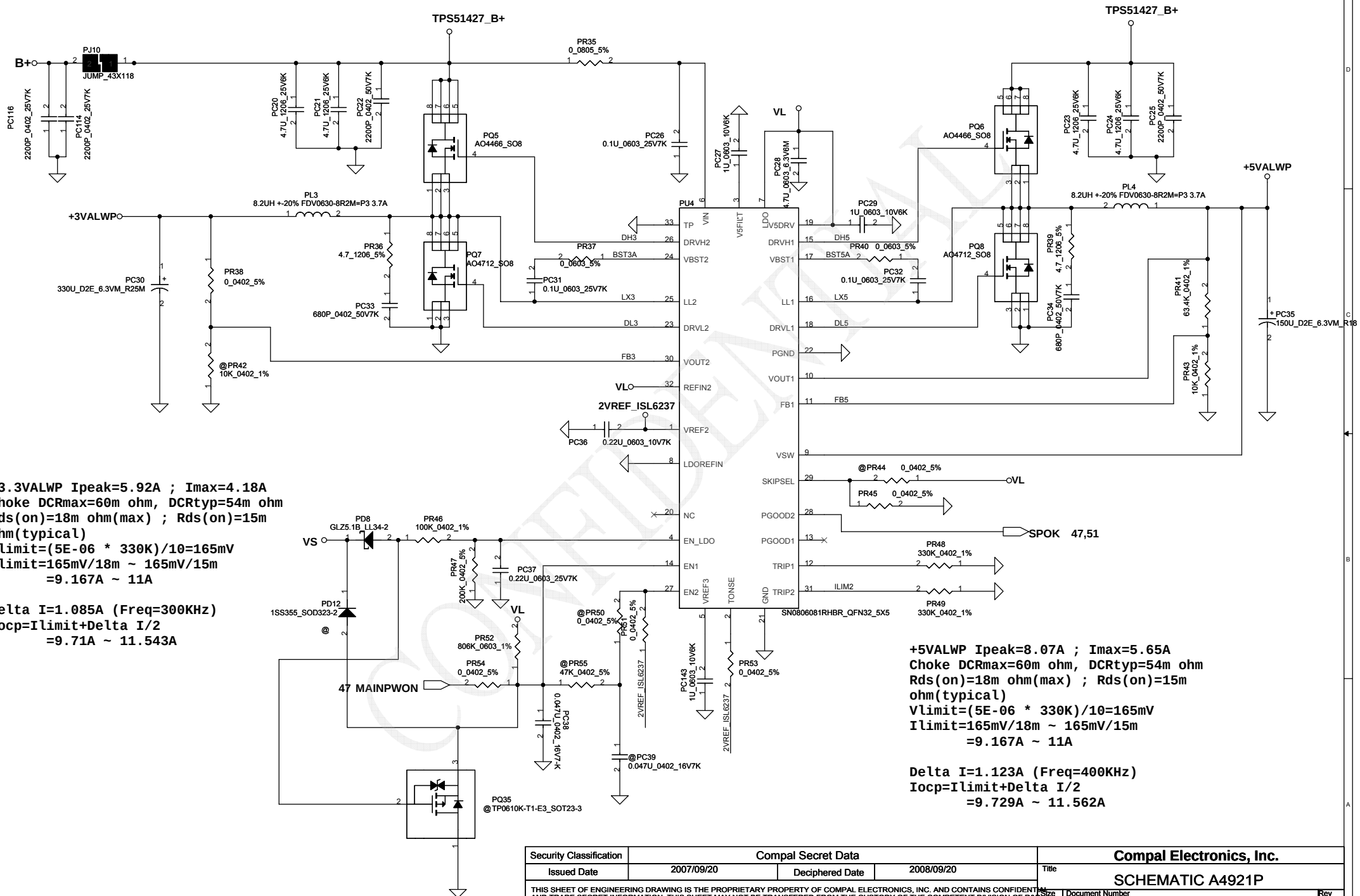
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				Date	Thursday, March 26, 2009
				Sheet	47 of 57
				Rev	C

+3.3VALWP Ipeak=5.92A ; Imax=4.18A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m$
 $= 9.167A \sim 11A$

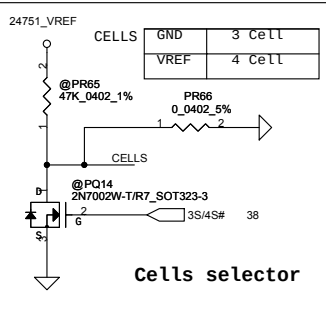
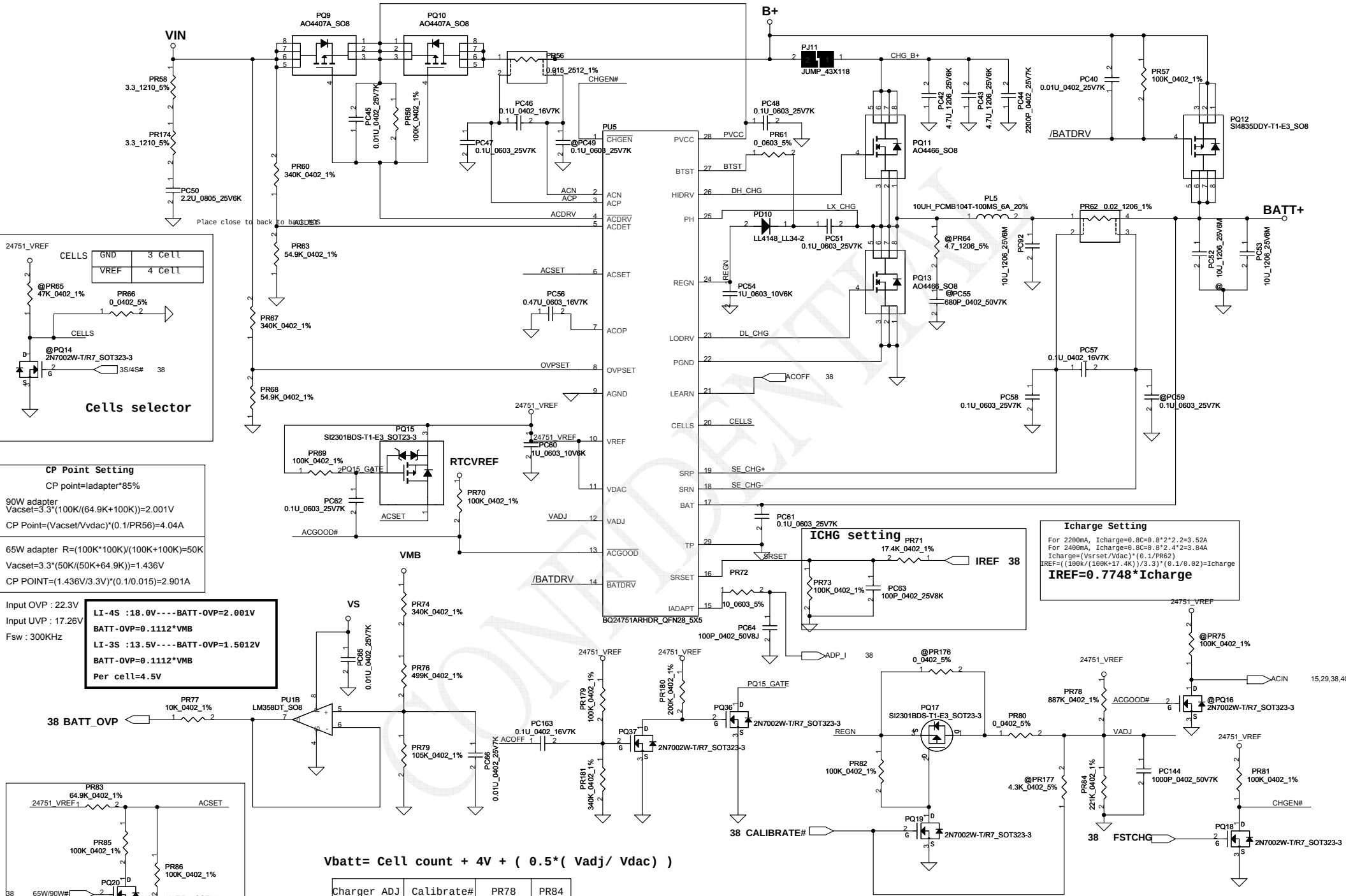
Delta I=1.085A (Freq=300KHz)
 $I_{ocp} = I_{limit} + \Delta I / 2$
 $= 9.71A \sim 11.543A$

+5VALWP Ipeak=8.07A ; Imax=5.65A
 Choke DCRmax=60m ohm, DCRtyp=54m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m$
 $= 9.167A \sim 11A$

Delta I=1.123A (Freq=400KHz)
 $I_{ocp} = I_{limit} + \Delta I / 2$
 $= 9.729A \sim 11.562A$

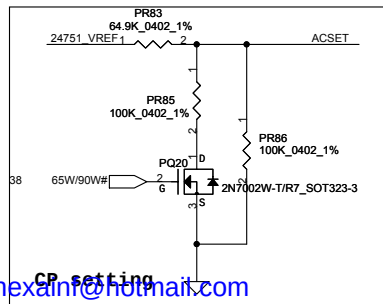


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				Rev	C
				Date:	Thursday, March 26, 2009
				Sheet	48 of 57



CP Point Setting
CP point=ladapter*85%
90W adapter
Vacset=3.3*(100K/(64.9K+100K))=2.001V
CP Point=(Vacset/Vdadc)*(0.1/PR56)=4.04A
65W adapter R=(100K*100K)/(100K+100K)=50K
Vacset=3.3*(50K/(50K+64.9K))=1.436V
CP POINT=(1.436V/3.3V)*(0.1/0.015)=2.901A

Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz
LI-4S : 18.0V---BATT-OVP=2.001V
BATT-OVP=0.1112*VMB
LI-3S : 13.5V---BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V

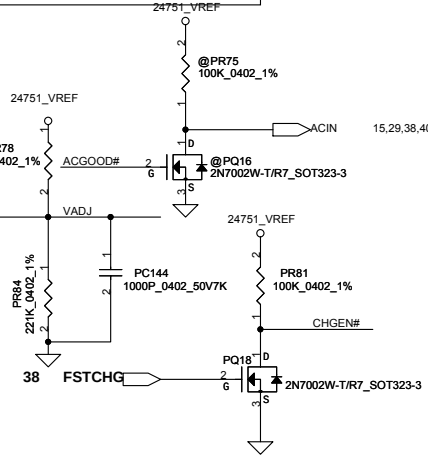
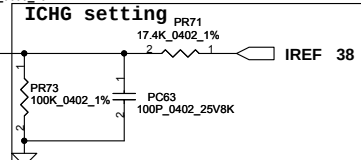


Vbatt= Cell count + 4V + (0.5*(Vadj/ Vdadc))

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V(1.32)	H	@	@

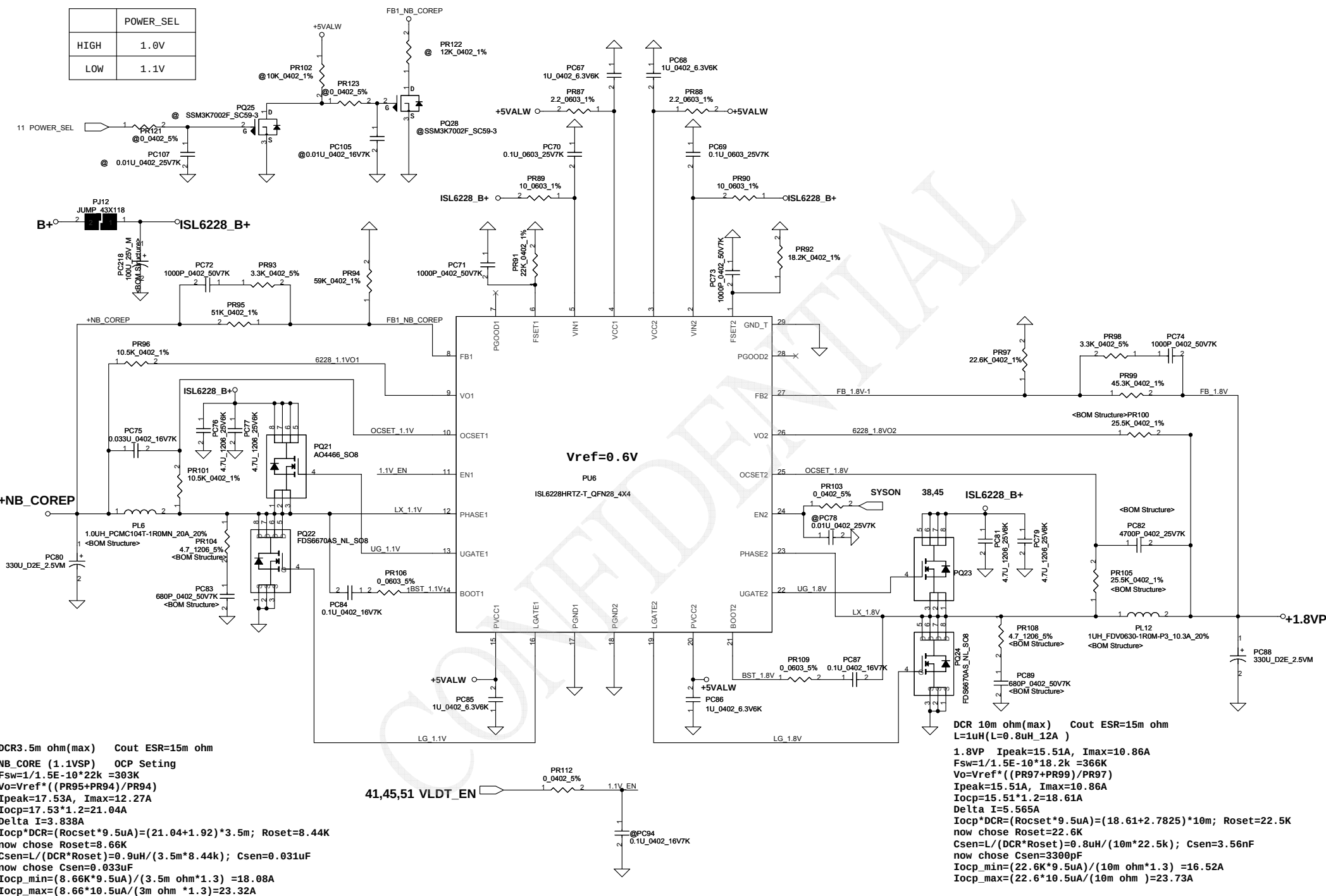
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Icharge Setting
For 2200mA, Icharge=0.8C=0.8*2.2=3.52A
For 2400mA, Icharge=0.8C=0.8*2.4=3.84A
Icharge=(Vsrset/Vdadc)*(0.1/PR62)
IREF=((100K/(100K+17.4K))/3.3)*(0.1/0.02)=Icharge
IREF=0.7748*Icharge

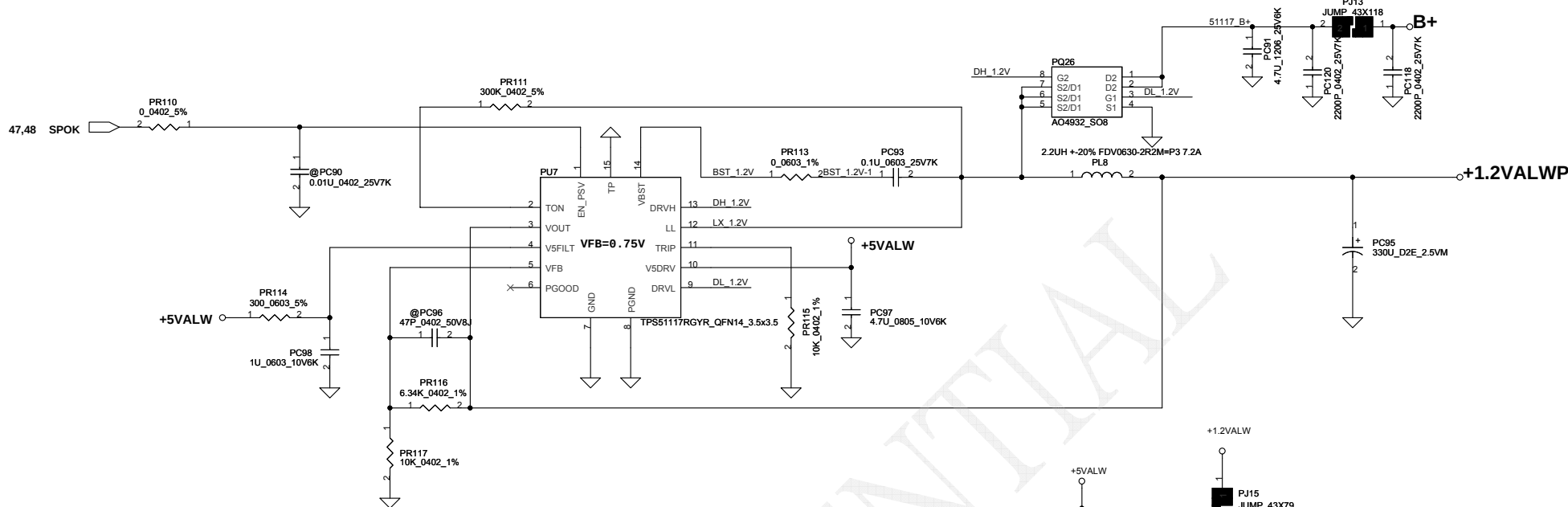


Compal Electronics, Inc.	
SCHEMATIC A4921P	
Customer	Document Number
401679	401679
Date: Thursday, March 26, 2009	Sheet 49 of 57

	POWER_SEL
HIGH	1.0V
LOW	1.1V

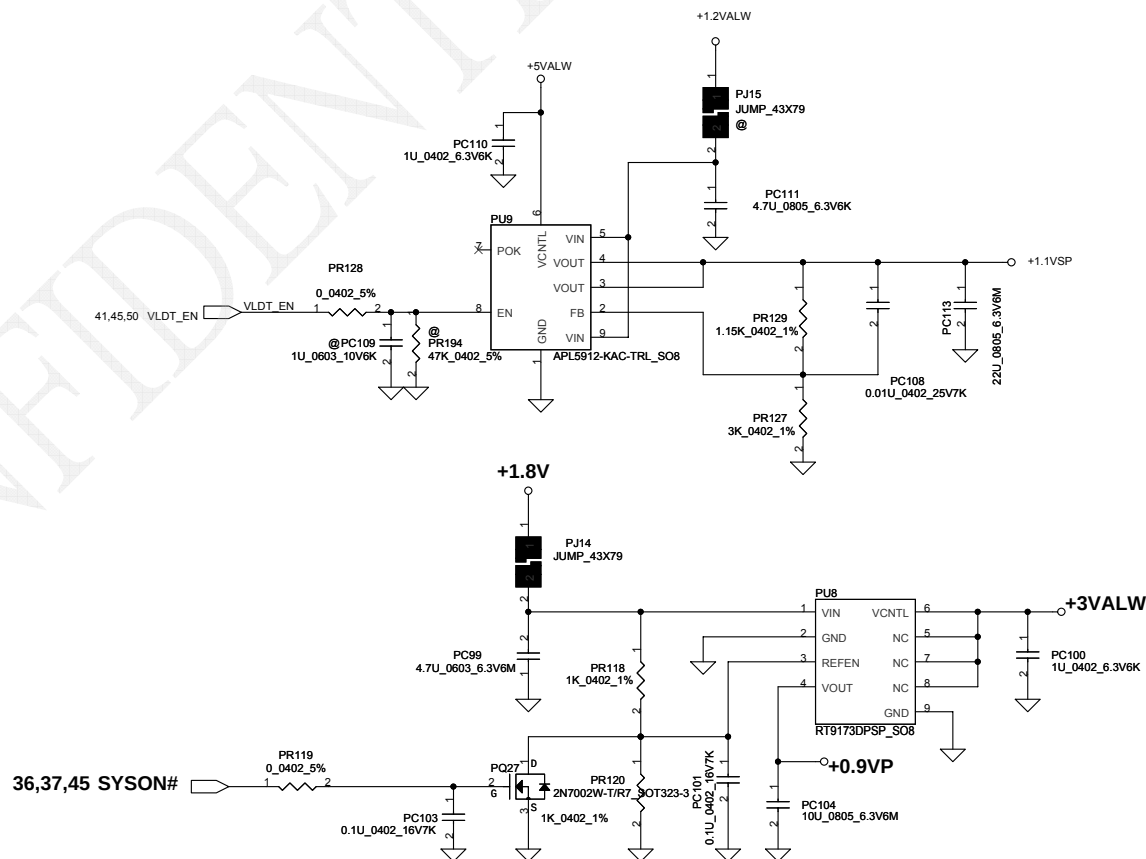


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				Customer 401679	
Date:		Thursday, March 26, 2009		Sheet	50 of 57

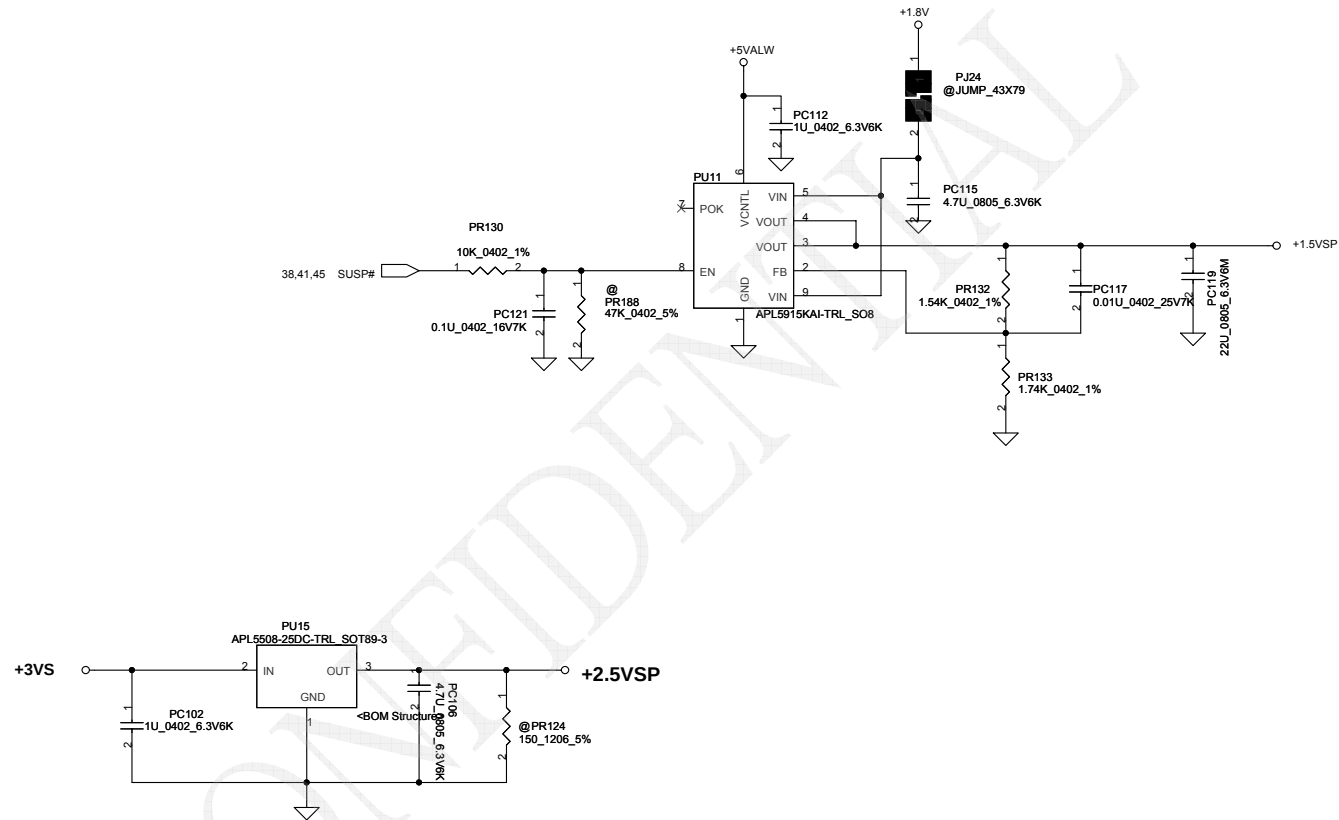


VFB=0.75V
 $V_o = VFB \cdot (1 + PR116/PR117) = 0.75 \cdot (1 + 10K/10K) = 1.5V$
 $Ton = 19E-12 \cdot Ron \cdot ((2/3) \cdot Vo + 100mV) / v_{in} + 50ns = 3.2E-7$
 $Fsw = 200KHz$

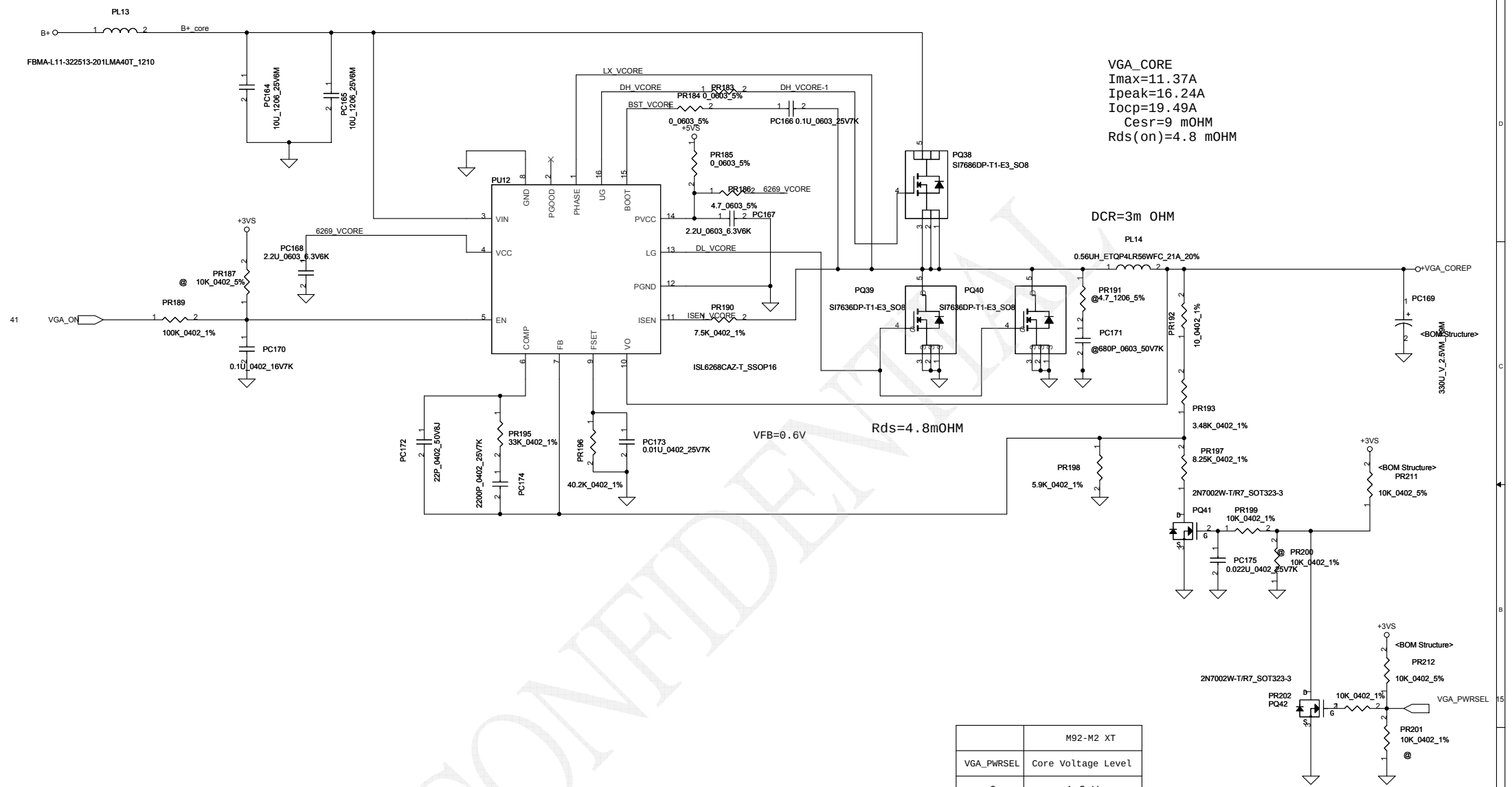
$C_{out} ESR = 15m \text{ ohm}$
 $I_{peak} = 3.58A, I_{max} = 2.51A$
 $\Delta I = ((19-1.2) \cdot (1.2/19)) / (L \cdot Fsw) = 2.59A$
 $\Rightarrow 1/2 \Delta I = 1.295A$
 $V_{trip} = R_{trip} \cdot I_{0uA} = 10K \cdot 10uA = 0.1V$
 $I_{ocp_min} = V_{trip} / R_{dsonmax} \cdot 1.4 + 1.295A$
 $= 0.1 / (0.0196 \cdot 1.4) + 1.295 = 3.644A + 1.295A = 4.939A$
 $I_{ocpmax} = (0.1 / (0.016 \cdot 1.2)) + 1.1.295A = 5.208A + 1.295A = 6.503A$
 $I_{ocp} = 6.503A - 4.939A$



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Customer				Document Number
36,37,45 SYSON#				401679
Date				Thursday, March 26, 2009
Sheet				51 of 57



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Issued Date	2007/09/20	Deciphered Date	2008/09/20	Title
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				Document Number
				401679
				Rev C
				Date: Thursday, March 26, 2009
				Sheet 52 of 57



Version change list (P.I.R. List)

Page 1 of 2
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	ADD circuit	Switch NB_core voltage	0.1	50	ADD PC107, PC105, PR121, PR123, PR122, PR102, PQ25, PQ28 at UMA Sku	2009/01/04	DVT
2	ADD circuit	Switch NB_core voltage	0.1	51	ADD PC110, PC111, PC108, PC109, PC1113, PR1128, PR194, PR129, PR127 at UMA Sku	2009/01/04	DVT
3	ADD snubber	EMI requestmrnt	0.1	50	Add PR104 4.7 ohm and PC83 680p	2009/01/04	DVT
4	ADD snubber	EMI requestmrnt	0.1	50	Add PR108 4.7 ohm and PC89 680p	2009/01/04	DVT
5	ADD CPU boot	EMI requestmrnt	0.1	53	Add PR229 2.2 ohm	2009/01/04	DVT
6	ADD CPU boot	EMI requestmrnt	0.1	53	Add PR243 2.2 ohm	2009/01/04	DVT
7	Change resistance value	Switch NB_core voltage	0.1	50	Change PR95 from 51 Kohm to 39.2 Kohm	2009/01/04	DVT
8	Change resistance value	Switch NB_core voltage	0.1	50	Change PR122 from 12 Kohm to 226 Kohm	2009/01/04	DVT
9	Change resistance value	soft start of Switch NB_core voltage	0.1	50	Change PR123 from 0 ohm to 10 Kohm	2009/01/04	DVT
10	Change capacitor value	soft start of Switch NB_core voltage	0.1	50	Change PC105 from 0.01 uF to 0.1 uF	2009/01/04	DVT
11	Change IC part number	Change IC part number	0.1	48	Change PU4 part number to SA00002V400	2009/01/04	DVT

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				Custom	401679	C
				Date:	Thursday, March 26, 2009	Sheet 55 of 57

		5	4	3	2	1																												
PHASE	PAGE	MODIFICATION LIST			PURPOSE																													
D	DVT	P.6	Reserve R484/R485(0ohm_0402) for CPU SB temp sensor		Reserved EC SMBUS1 due to +3VS leakage when S3 entry with SMBUS2																													
		P.8	Add C174/C175/C176 (0.1u_0402)		EMI request																													
		P.10	C646/C647/C648/C649/C650/C651/C652/C653 with VGA@		BOM error																													
		P.11	Add R488/R489 (0ohm_0402) & reserve R491/R492 (0ohm_0402)		UMA HDMI I2C bus mainly to RS780MN DDC port1 & reserve to port0																													
		P.11	Reserve R490(0ohm_0402)		NA																													
C		P.12	Change L6/L7 from 0ohm_0805 as 0ohm_1206 & with VGA@		For DIS +1.1VS power source from fixed +NB_CORE																													
		P.22	Remove VRAM Samsung(Q-die) & Qimonda type		Customer request																													
		P.24	U35/R464/R465/C845/C846/C847/C848/C849 with @ & RP15 with UMA@		Separately as DIS sku only & UMA sku only																													
		P.24	Add RP20/RP21/RP22/RP23(0ohm_0404_4P2R) with VGA@		For DIS sku only																													
		P.24	Reserve Q52/R501/R502/R503		Reserve for UMA sku white screen flash when boot issue check																													
		P.25	Change JHDMI1 from SMD type as DIP type(DC232000800)		DFX request																													
		P.25	Change single MOS as 2 dual N-ch MOS(Q53/Q54) & reserve R506		NA (Just no need to modify)																													
		P.26	R47/R58/U25/U26/C626/C628/R475 with UMA@ & R507 with VGA@ , U36/C850 with @ & delete R466 , add R493/R494/R495 with VGA@		Separately as DIS sku only & UMA sku only																													
		P.27	Add R496 with @ & R476/R482 with @		NA																													
	B		P.28	Add R509 with VGA@ & R510 with UMA@		Reserve SKU ID for SW even SW check device ID instead currently																												
		P.29	Reserve C862/C863/C855/C856		Reserve eSATA function for future request																													
		P.37	Change JUSB1 as SB700 USB port6		Dedicated HS port on lower-left position																													
		P.38	Change U20 as KB926 D3 version (SA00001J580)		NA																													
		P.38	D41 with VGA@ & D42 with UMA@		Separately as DIS sku only & UMA sku only																													
A		P.38	U20.85 defined as TP_LOCK_LED# feature		LED control simultaneously with Tutch-Pad locked function																													
		P.38	Change R194 as 8.2kohm_0402		Change board ID as 1 (PCB revision : 0.2)																													
		<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td colspan="2">Compal Electronics, Inc.</td></tr><tr><td>Issued Date</td><td colspan="2">2008/10/06</td><td>Deciphered Date</td><td colspan="2">2009/10/06</td></tr><tr><td colspan="6">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td></tr></table>				Security Classification	Compal Secret Data			Compal Electronics, Inc.		Issued Date	2008/10/06		Deciphered Date	2009/10/06		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						<table><tr><td>Title</td><td colspan="2">SCHEMATIC A4921P</td></tr><tr><td>Document Number</td><td colspan="2">401679</td></tr><tr><td>Date:</td><td>Thursday, March 26, 2009</td><td>Sheet 56 of 57</td></tr></table>		Title	SCHEMATIC A4921P		Document Number	401679		Date:	Thursday, March 26, 2009	Sheet 56 of 57
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