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NAL90/NALG0 M/B Schematics Document

Intel Auburndale/Clarksfield Processor with DDRIII + Ibex Peak-M

2009-10-20

REV:1.0

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Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title: Cover Page
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				Date: Friday, October 23, 2009; Sheet 1 of 60

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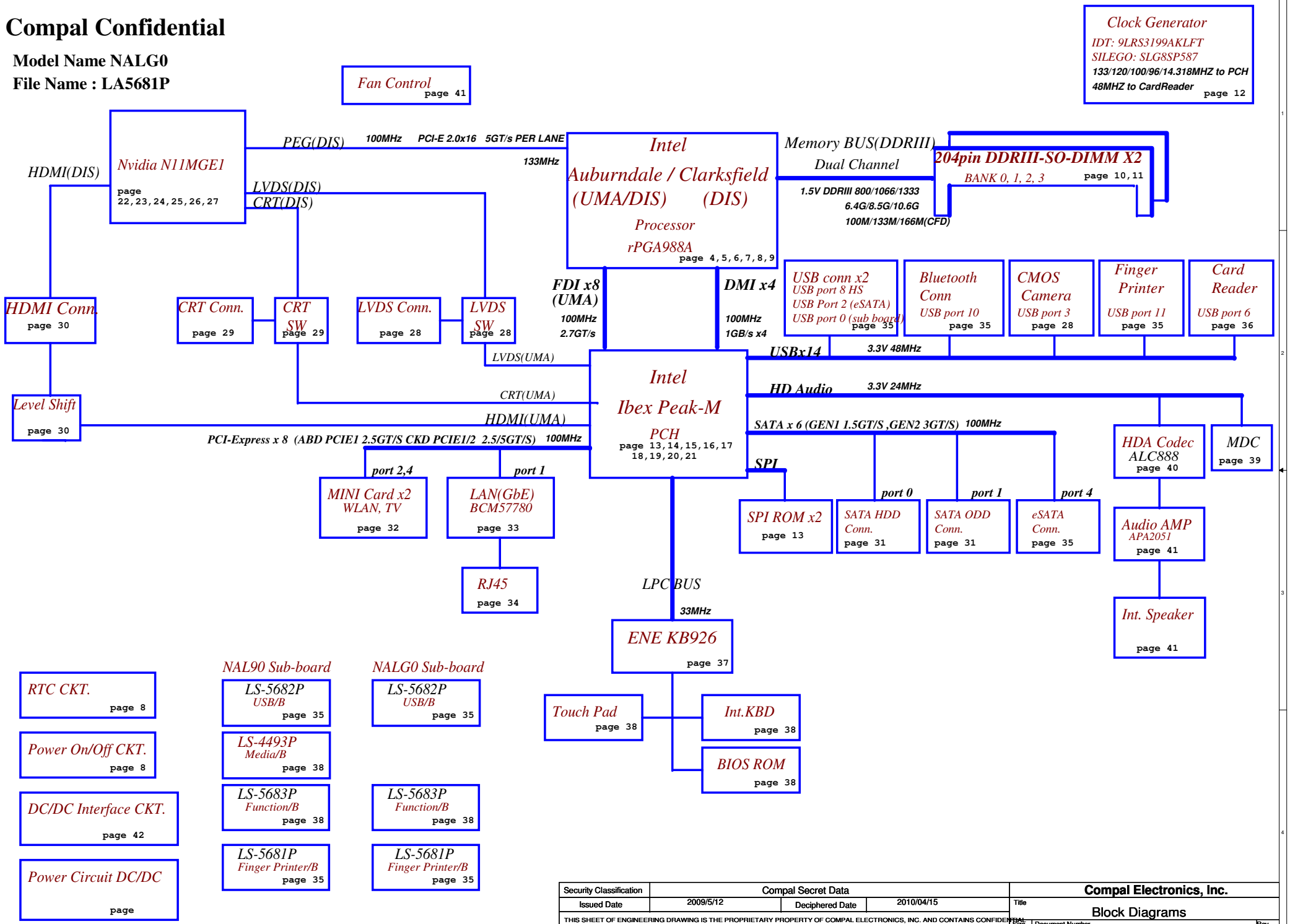
Model Name NALG0
File Name : LA5681P



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+GFX_core	Core voltage for CPU	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+VGA_CORE	Core voltage for N11M VGA	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5VS	1.5V power rail for DDRIII	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
PCH	
VGA	

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
Mini card	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA only	UMA only@
DIS	DIS@
DIS Only	DIS only@
Switchable	SG@
	XDP@
	NonSG@
	MINI2@
	FP@
	eDriver@
	Dmic@
	Caps@
	X76@
	HDCP@
	AMIC@
S3 power	S3@
	non S3@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	Ext4 HS USB
		1	sub Board
	UHCI1	2	
		3	Camera
	UHCI2	4	1st Min-Card
		5	2st Min-Card
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Ext4 HS USB
		9	Card Reader
	UHCI5	10	Blue Tooth
		11	Finger Print
	UHCI6	12	
		13	

BOM Config
UMA only
UMA@/UMA only@/FP@/Dmic@/XDP@/S3@

DIS ONLY
DIS@/DIS only@/FP@/Dmic@/XDP@/S3@

Switchable Graphics
SG@/UMA@/DIS@/FP@/Dmic@/XDP@/S3@

Note:do cost BOM add X76@

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Title	Notes List		
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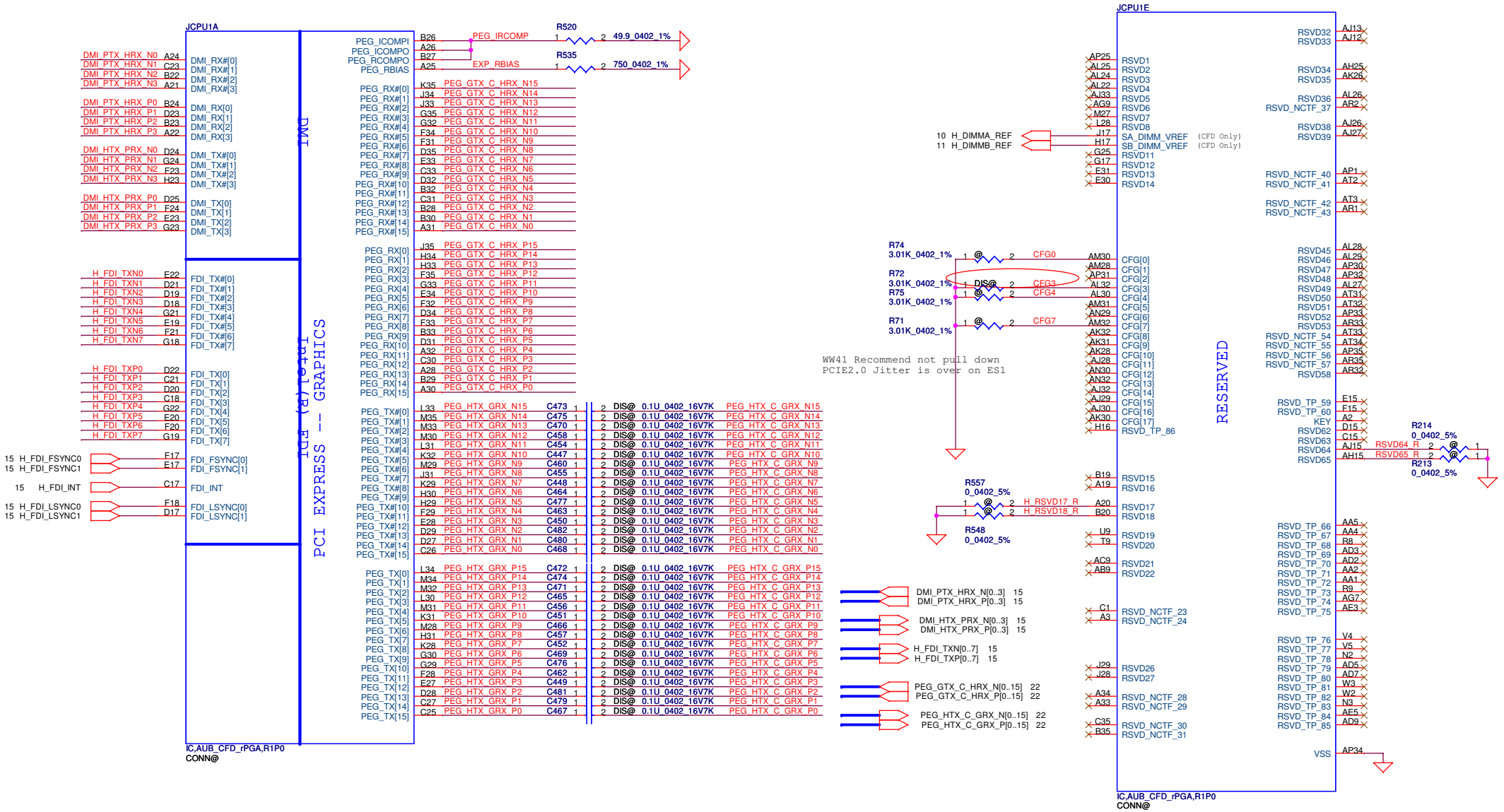

eDP Signals MAPPING

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

CheckList0.8 1.22
Auburndale Graphics Disable

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Title: PROCESSOR (1/6) DMI,FDI,PEG

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B	NALG0 M/B LA-5681P Schematic	1.0

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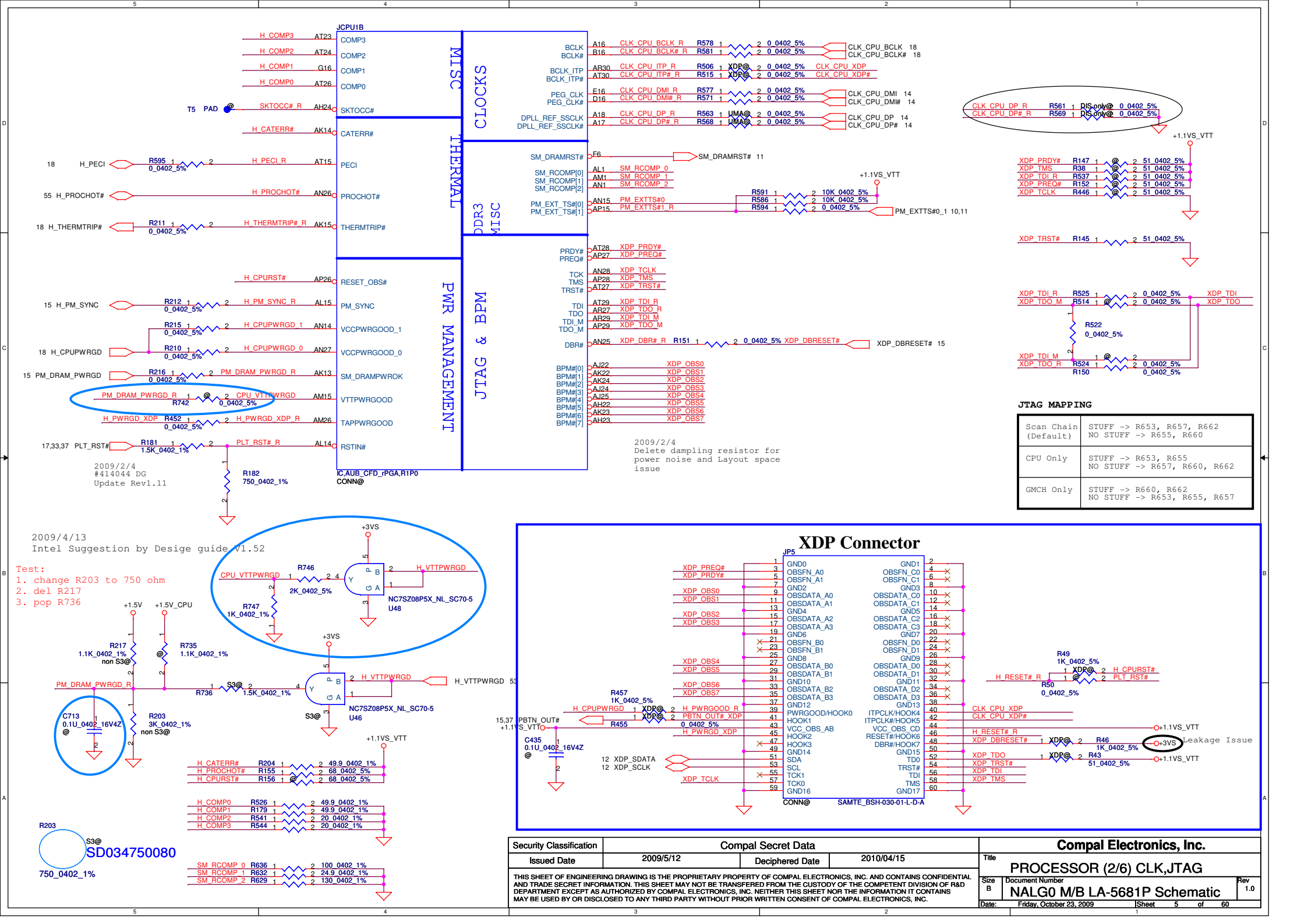

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Title: PROCESSOR (2/6) CLK,JTAG

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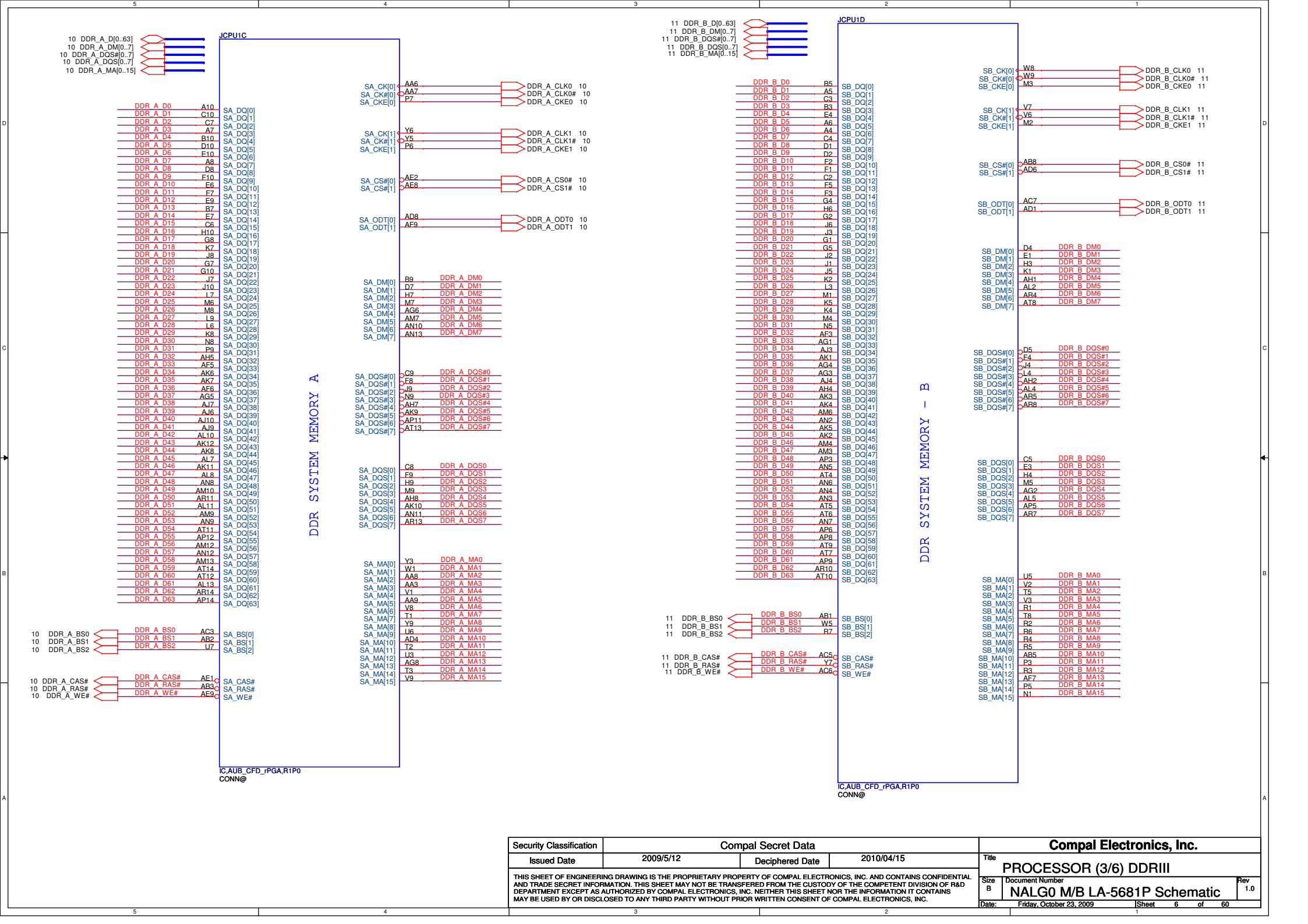

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Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	NALG0 M/B LA-5681P Schematic	1.0

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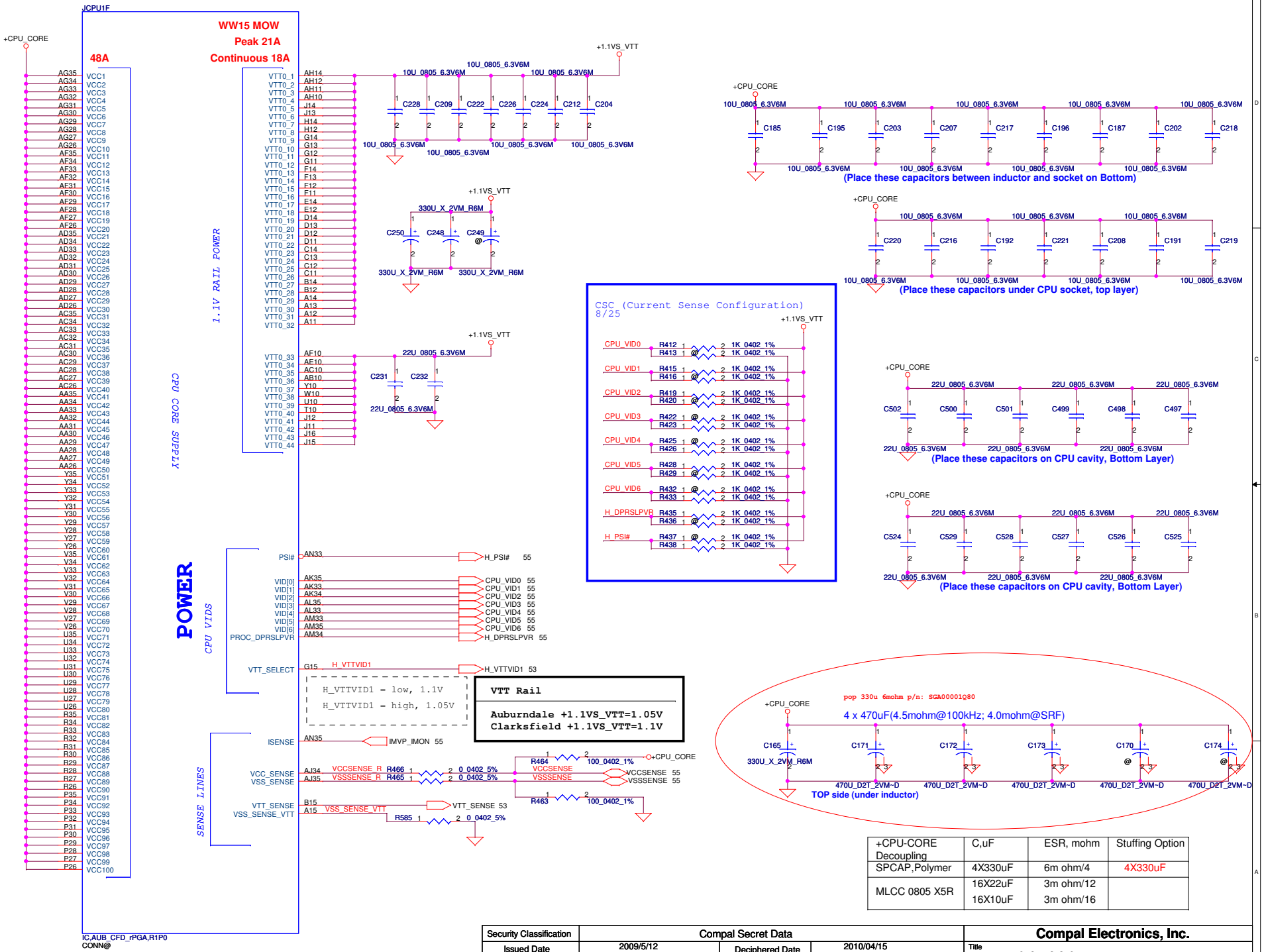

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X330uF	6m ohm/4	4X330uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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Title: PROCESSOR (4/6) PWR,Bypass

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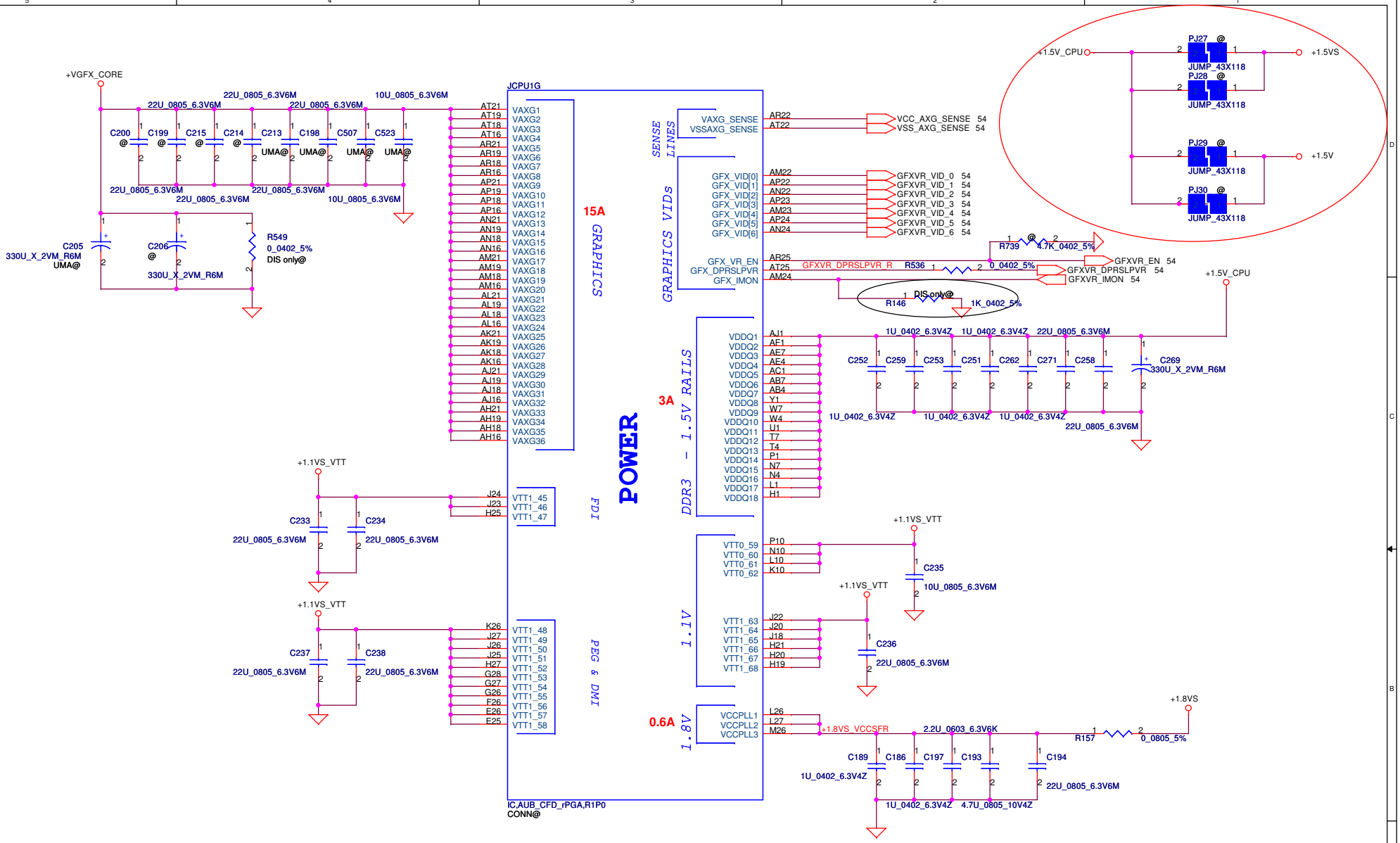

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Title: PROCESSOR (5/6) PWR

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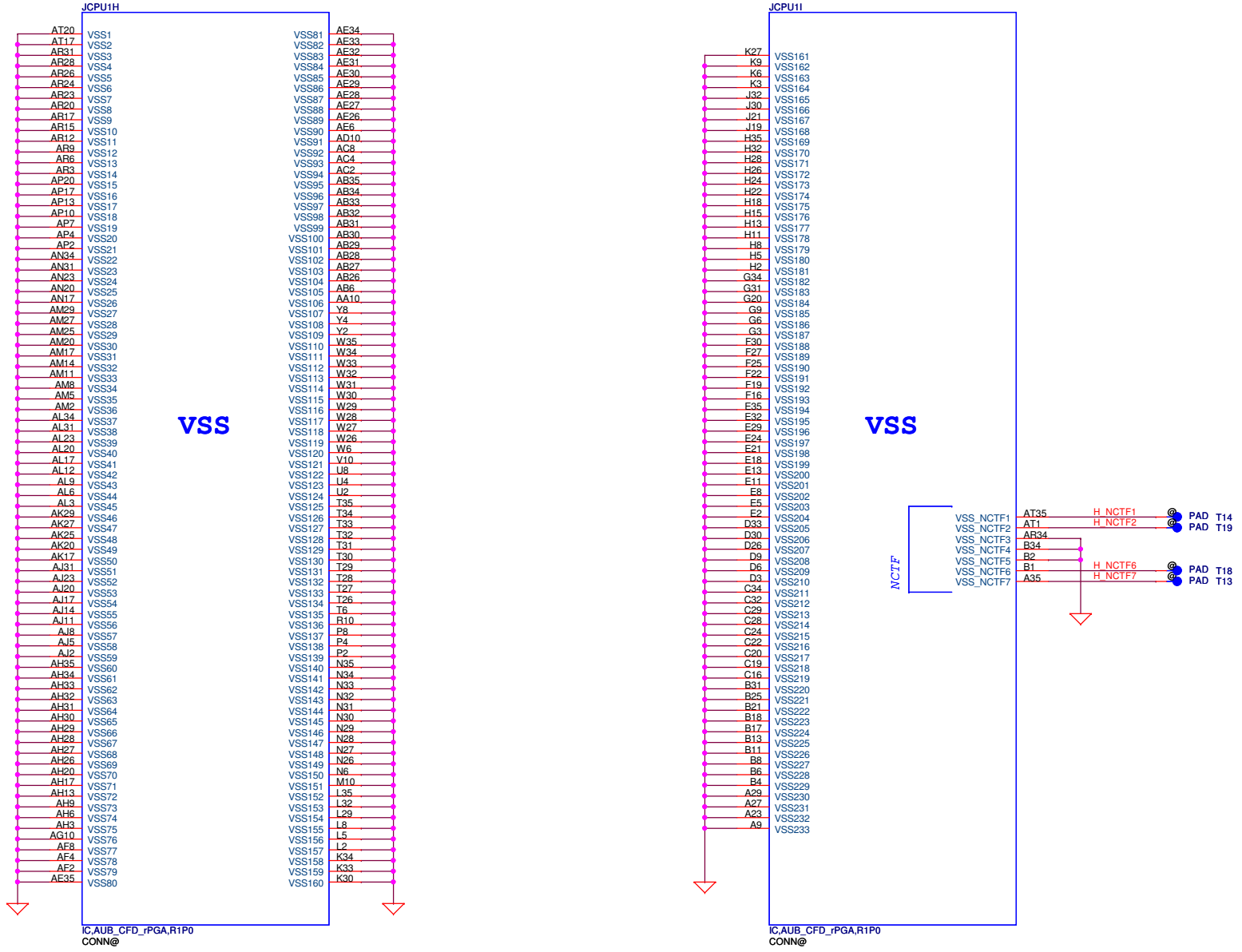

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Title: PROCESSOR (6/6) VSS

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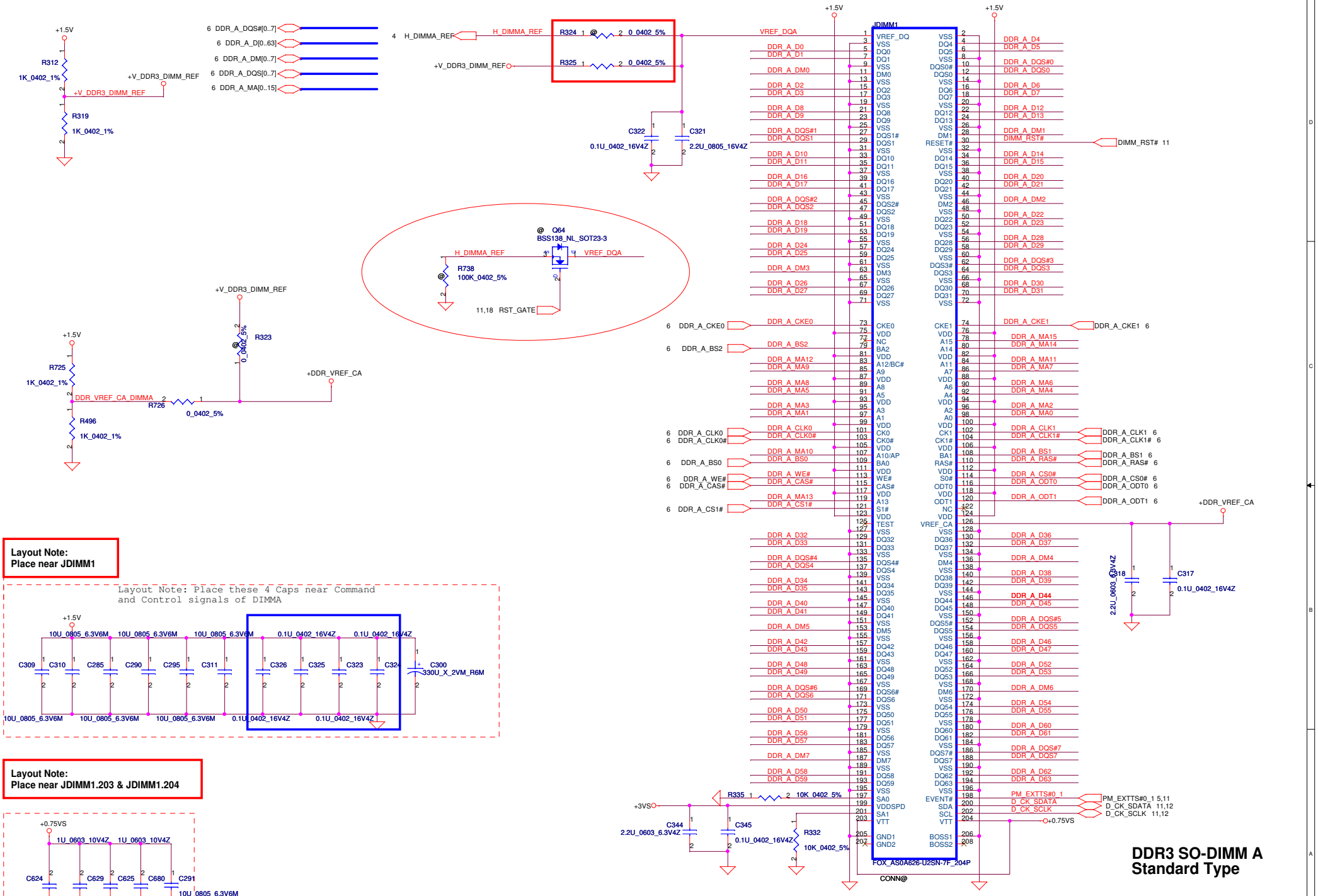

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Compal Electronics, Inc.			
Title: DDRIII-SODIMM SLOT1			
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2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

2009/04/13
For Arrandale ,it should be use M1 Circuit (pop R328)
For Clarksfield ,it should be use M3 Circuit (pop R327)
DG V1.52

6 DDR_B_DQS#[0..7]
6 DDR_B_D[0..63]
6 DDR_B_DM[0..7]
6 DDR_B_DQS[0..7]
6 DDR_B_MA[0..15]
12,14,32 PCH_SMBCLK
12,14,32 PCH_SMBDATA

4 H_DIMMB_REF
+V_DDR3_DIMM_REF
R327 0_0402_5%
R328 0_0402_5%
VREF_DQB

C335 2.2U_0805_16V4Z
C336 0.1U_0402_16V4Z

JDIMM2
TYCO_2-2013310-1_204P
CONN@

@ Q63 BSS138_NL_SOT23-3
R737 100K_0402_5%
C714 0.047U_0402_16V7K
10,18 RST_GATE

R734 0_0402_5%
R732 1K_0402_1%
BSS138_NL_SOT23-3 Q62
5 SM_DRAMRST#
DIMM_RST#
DIMM_RST# 10
R294 100K_0402_5%
C711 0.1U_0402_16V4Z
C712 0.047U_0402_16V7K

Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
10U_0805_6.3V6M
0.1U_0402_16V4Z
C660 C657 C659 C655 C656 C658 C331 C330 C329 C333 C307 330U_X_2VM_R6M

Layout Note:
Place near JDIMM2.203 & JDIMM2.204

+0.75VS
1U_0603_10V4Z
C667 C666 C671 C665 C690 10U_0805_6.3V6M

R685 10K_0402_5%
R686 10K_0402_5%
+3VS
C661 2.2U_0603_6.3V4Z
C663 0.1U_0402_16V4Z

C334 2.2U_0603_6.3V4Z
C332 0.1U_0402_16V4Z
+DDR_VREF_CA

DDR3 SO-DIMM B
Standard Type

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Title: DDRIII-SODIMM SLOT2
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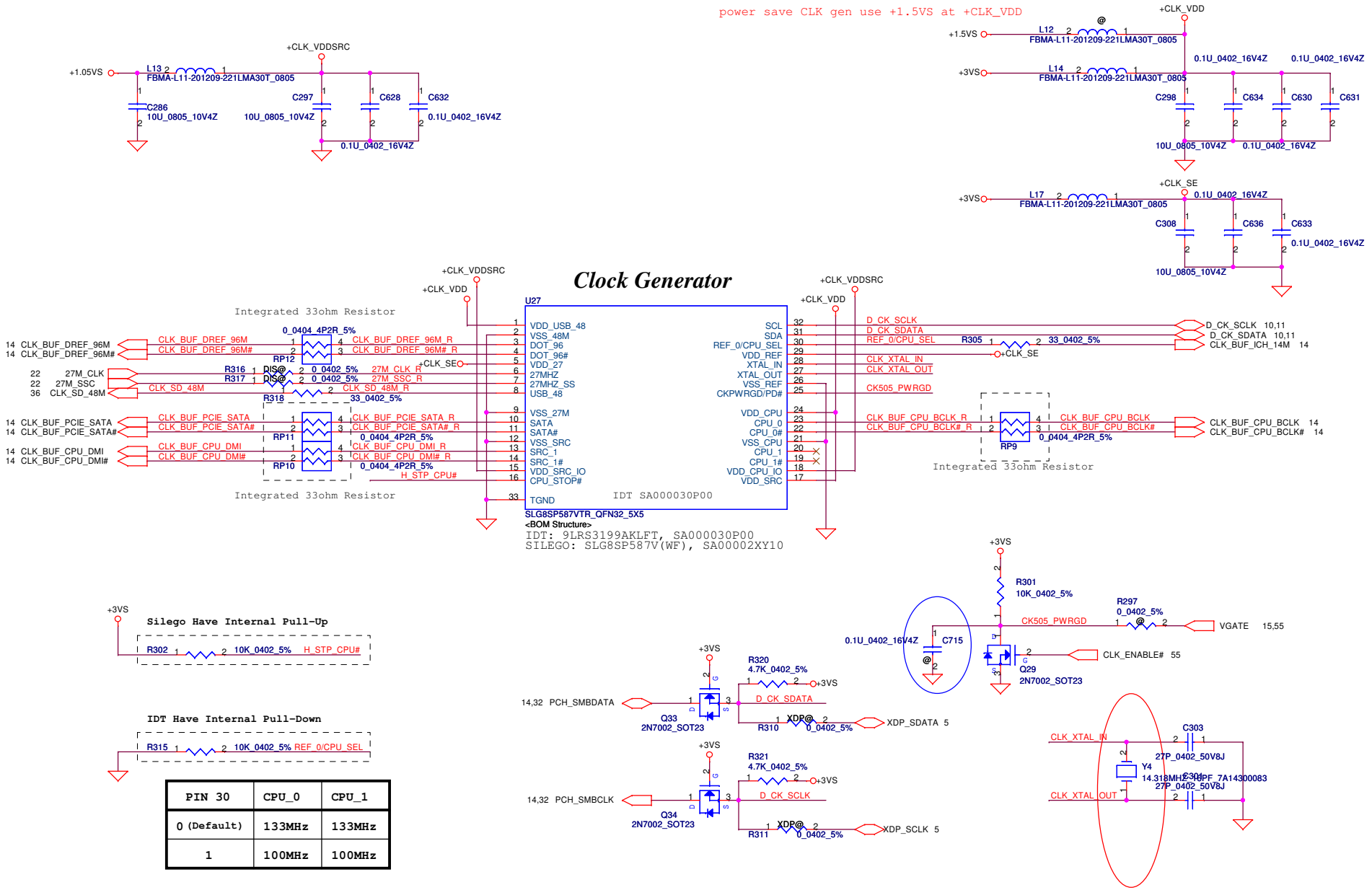
power save CLK gen use +1.5VS at +CLK_VDD
Clock Generator
Integrated 33ohm Resistor
IDT SA000030P00
SLG8SP587VTR_QFN32_5X5
<BOM Structure>
IDT: 9LRS3199AKLFT, SA000030P00
SILEGO: SLG8SP587V(WF), SA00002XY10
Silego Have Internal Pull-Up
IDT Have Internal Pull-Down
PIN 30 | CPU_0 | CPU_1
0 (Default) | 133MHz | 133MHz
1 | 100MHz | 100MHz
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Clock Generator (CK505)
NALG0 M/B LA-5681P Schematic
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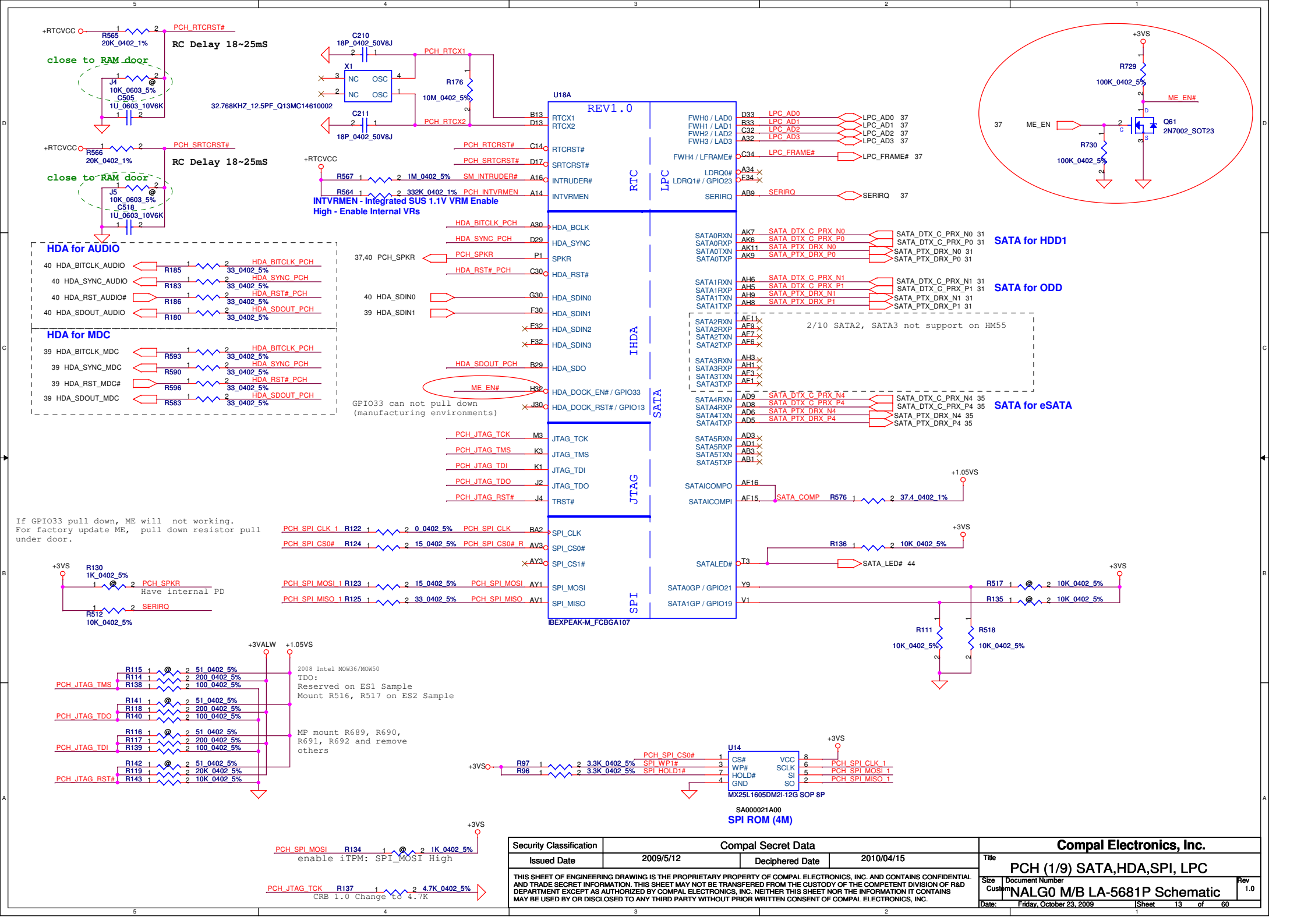

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Title: PCH (1/9) SATA,HDA,SPI, LPC

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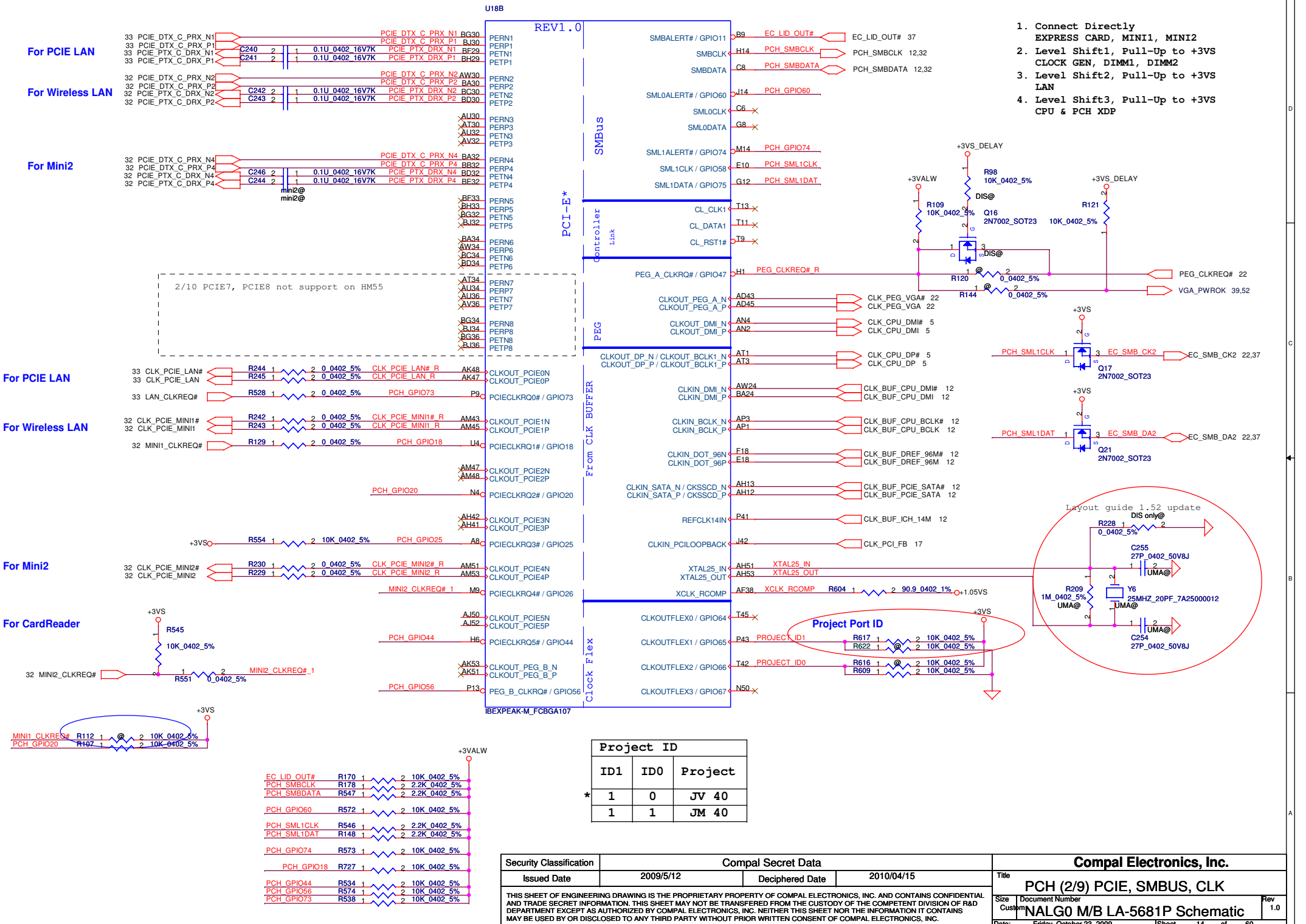
U18B
REV1.0
IBEXPEAK-M_FCBGA107
PCI_E*
SMBus
PEG
From CLK BUFFER
Clock Flex
Controller Link
For PCIE LAN
For Wireless LAN
For Mini2
For CardReader
2/10 PCIE7, PCIE8 not support on HM55
1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP
Layout guide 1.52 update
Project Port ID
Project ID
ID1 ID0 Project
* 1 0 JV 40
1 1 JM 40
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Title
PCH (2/9) PCIE, SMBUS, CLK
Size Custom
Document Number NALG0 M/B LA-5681P Schematic
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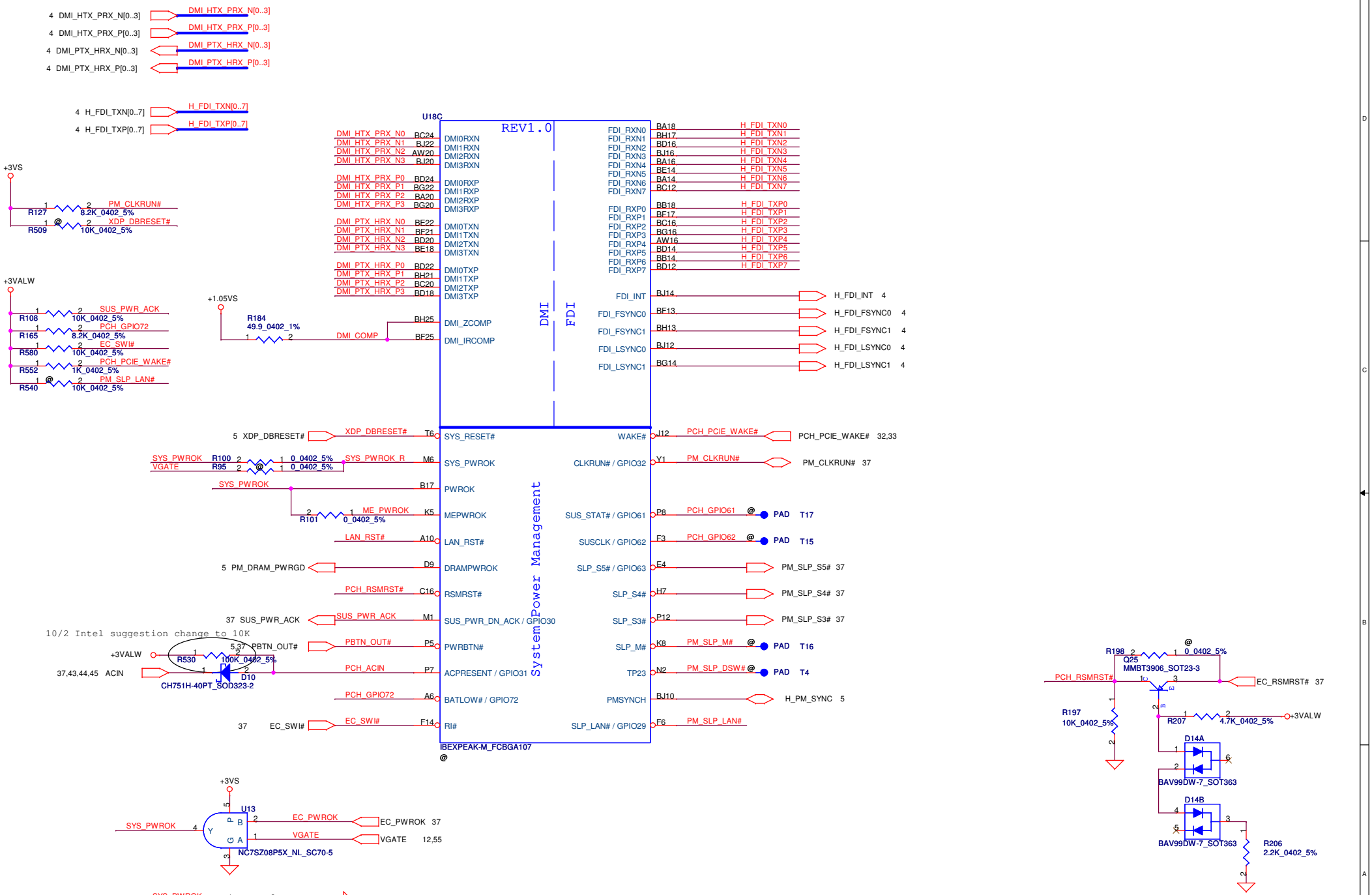

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Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

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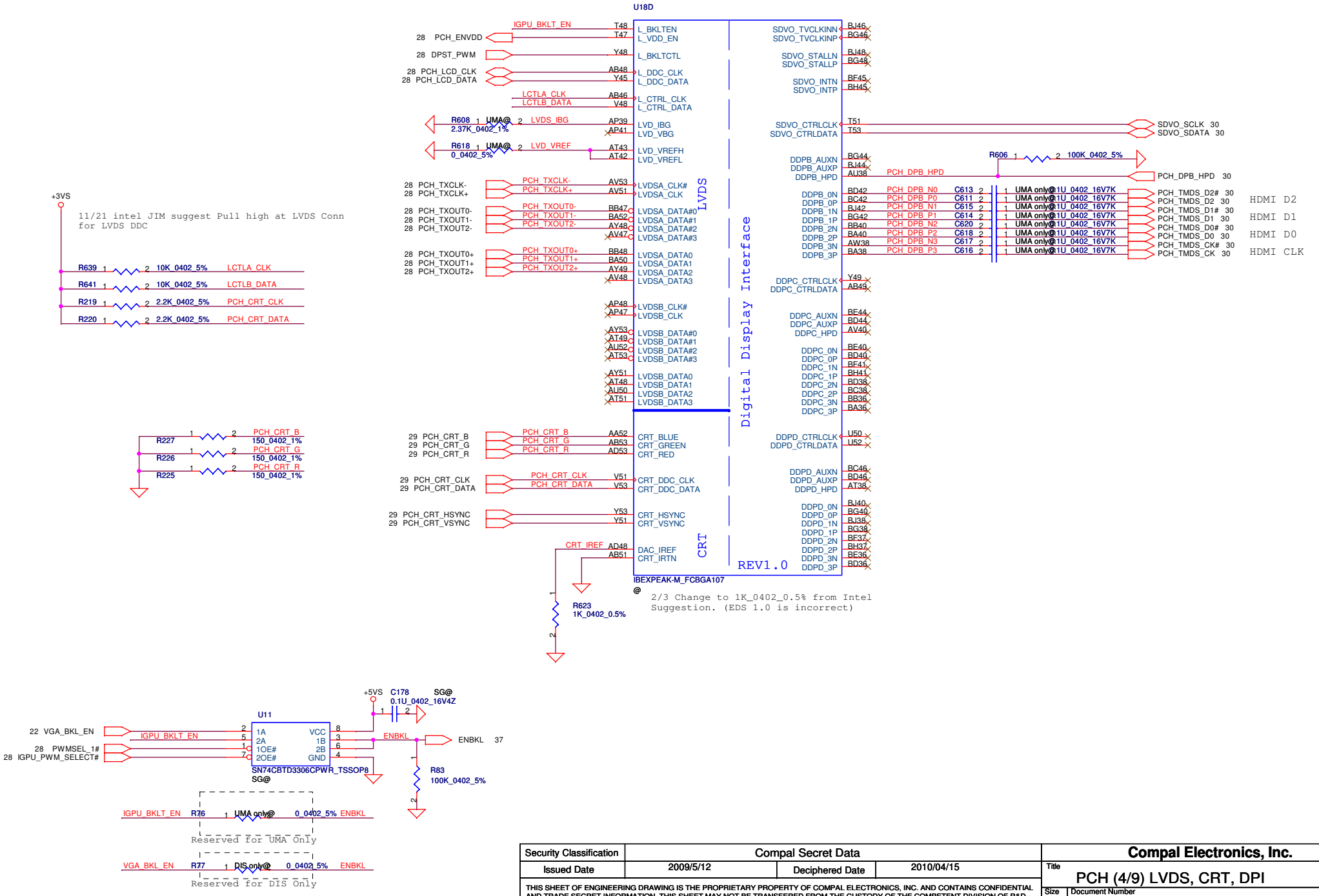

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Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

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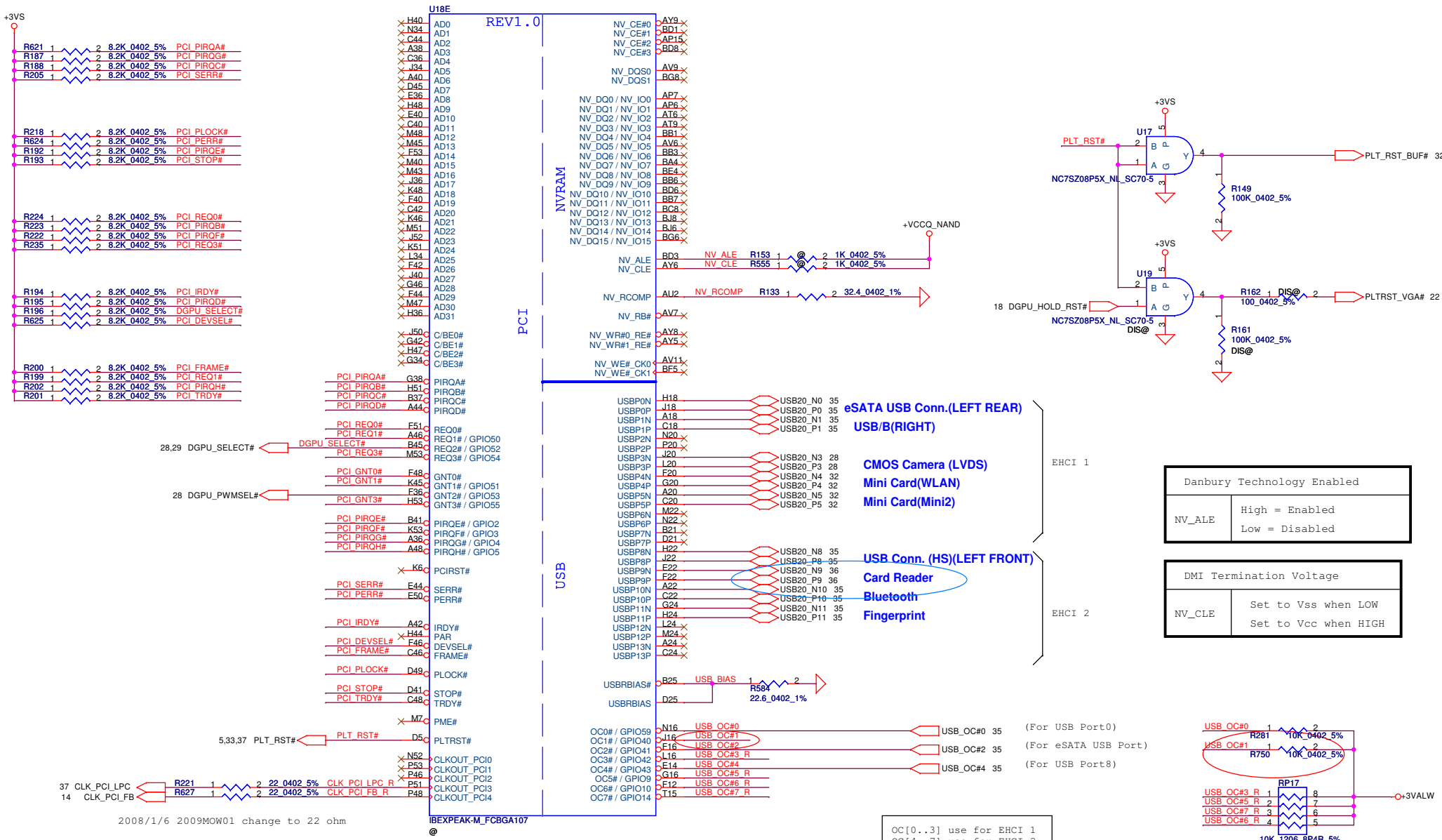

Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled

DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

*

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

PCI_GNT0# R638 1 @ 2 1K_0402_5%
Have internal PU
PCI_GNT1# R620 1 @ 2 1K_0402_5%
Have internal PU
PCI_GNT3# R238 1 @ 2 1K_0402_5%
Have internal PU

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Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

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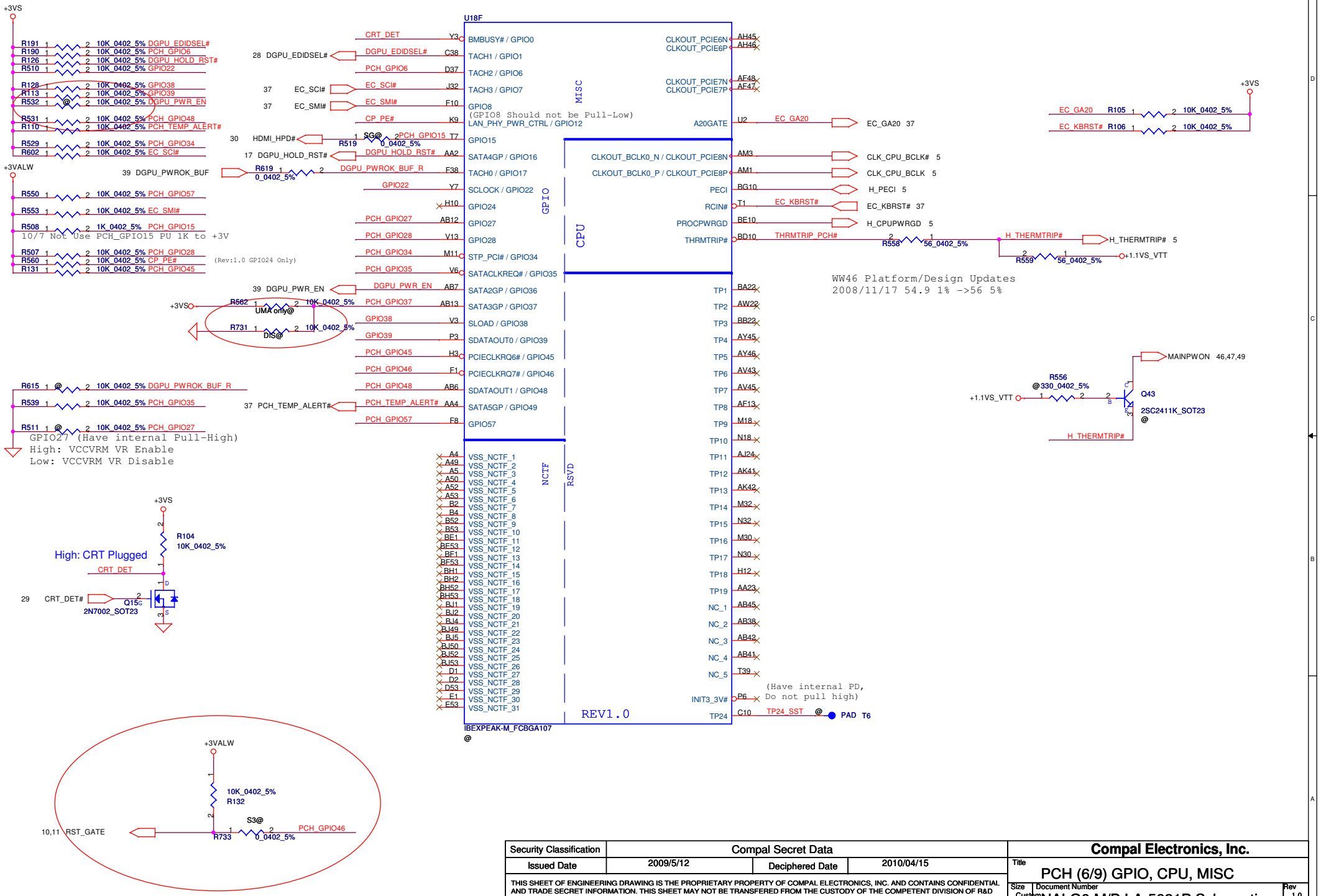

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Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

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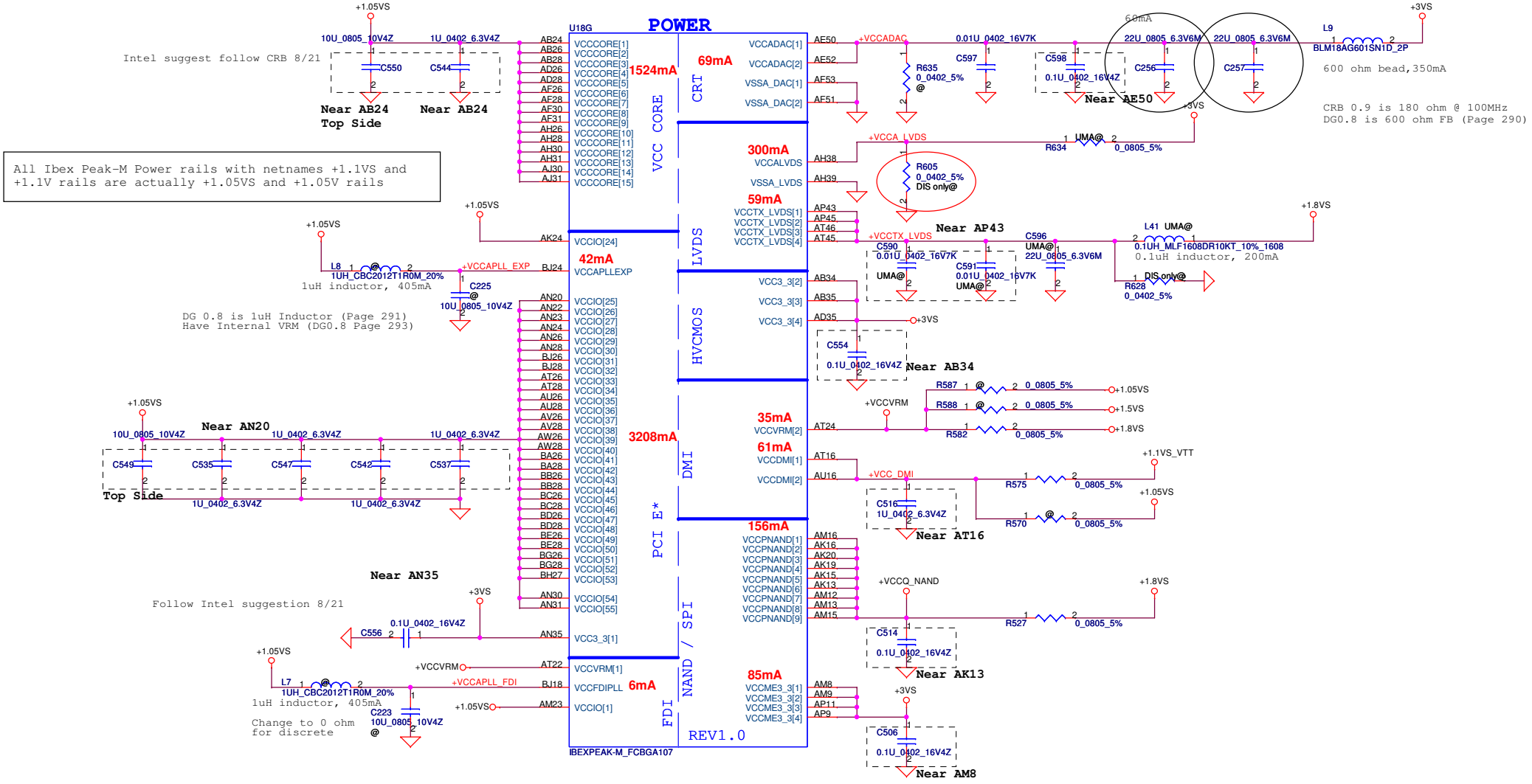

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Compal Electronics, Inc.

Title: PCH (7/9) PWR

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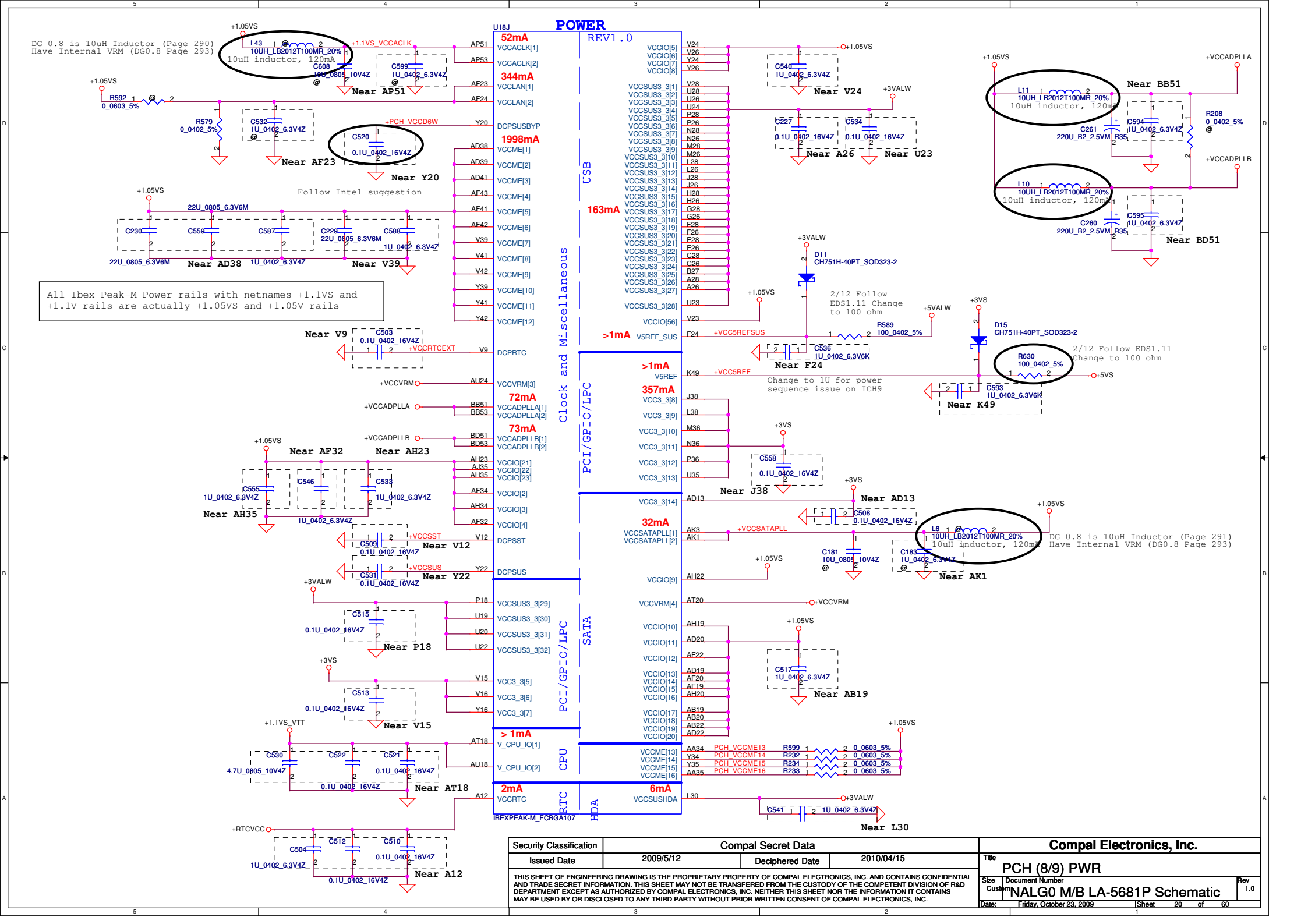

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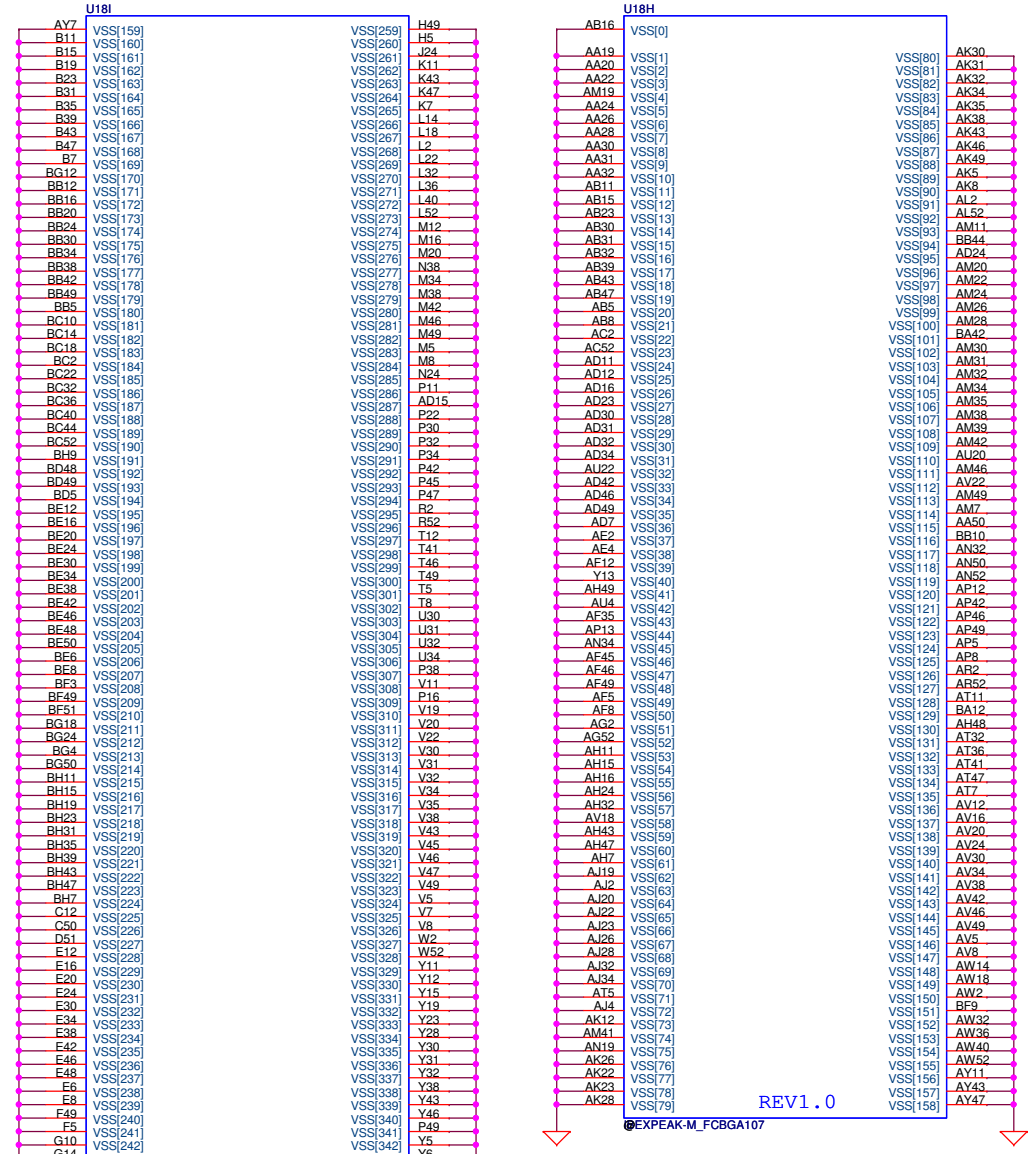
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 20 of 60



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

Size	Document Number	Rev
Custom	NALG0 M/B LA-5681P Schematic	1.0

Date: Friday, October 23, 2009 Sheet 21 of 60

GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	N/A
GPIO8	IN	L	N/A
GPIO9	OUT	L	N/A
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A

External Spread Spectrum

If External Spread Spectrum not stuff then stuff resistor

DIS@ N11M-GE1-B-A2_BGA969

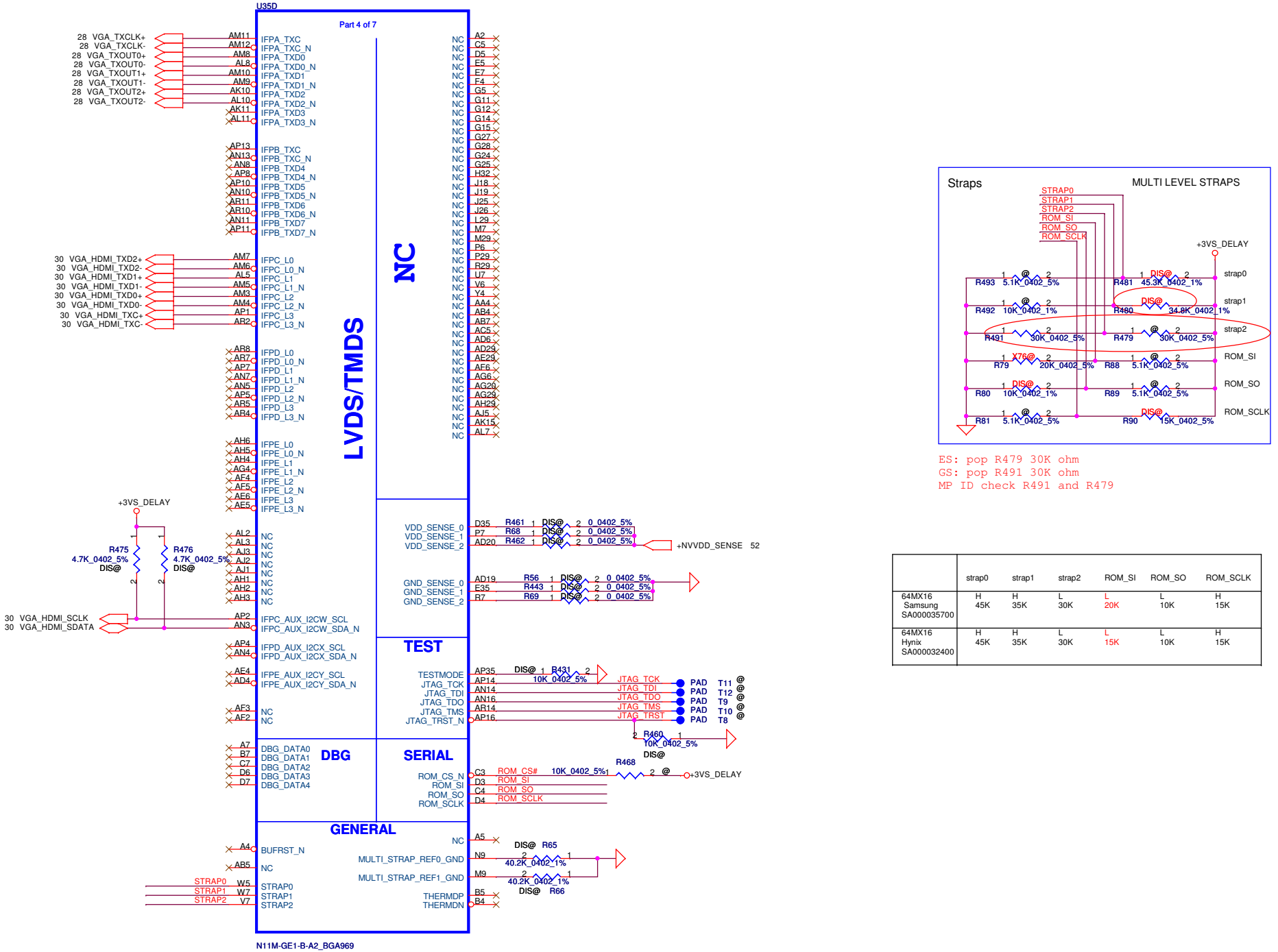
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: N11M PEG 1/6

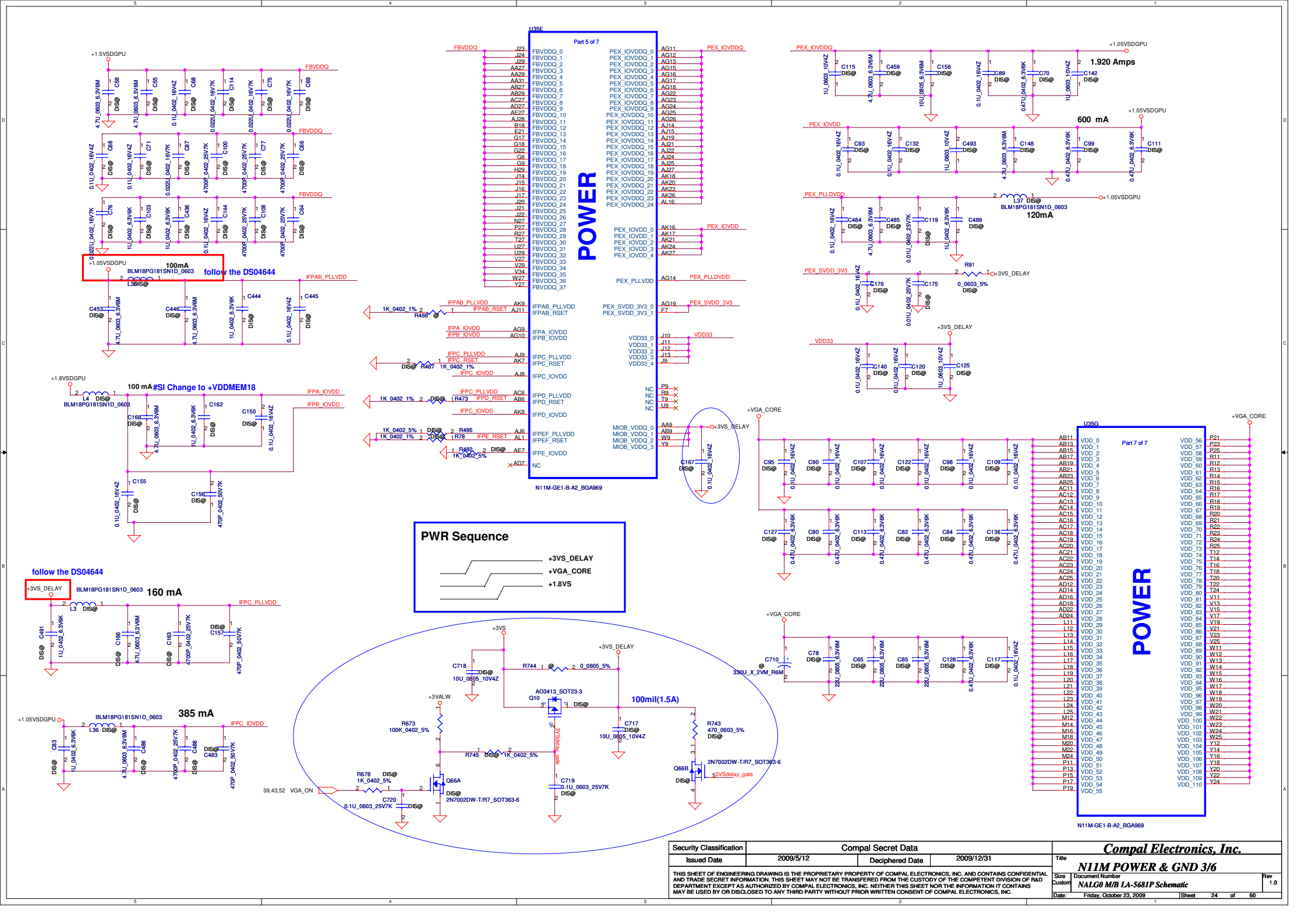
Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 22 of 60



	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	H 35K	L 30K	L 20K	L 10K	H 15K
64MX16 Hynix SA000032400	H 45K	H 35K	L 30K	L 15K	L 10K	H 15K

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/5/12	Deciphered Date 2010/04/15	Title: N11M LVDS 2/6
			Size: Custom; Document Number: NALG0 M/B LA-5681P Schematic; Rev:
			Date: Friday, October 23, 2009; Sheet 23 of 60



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

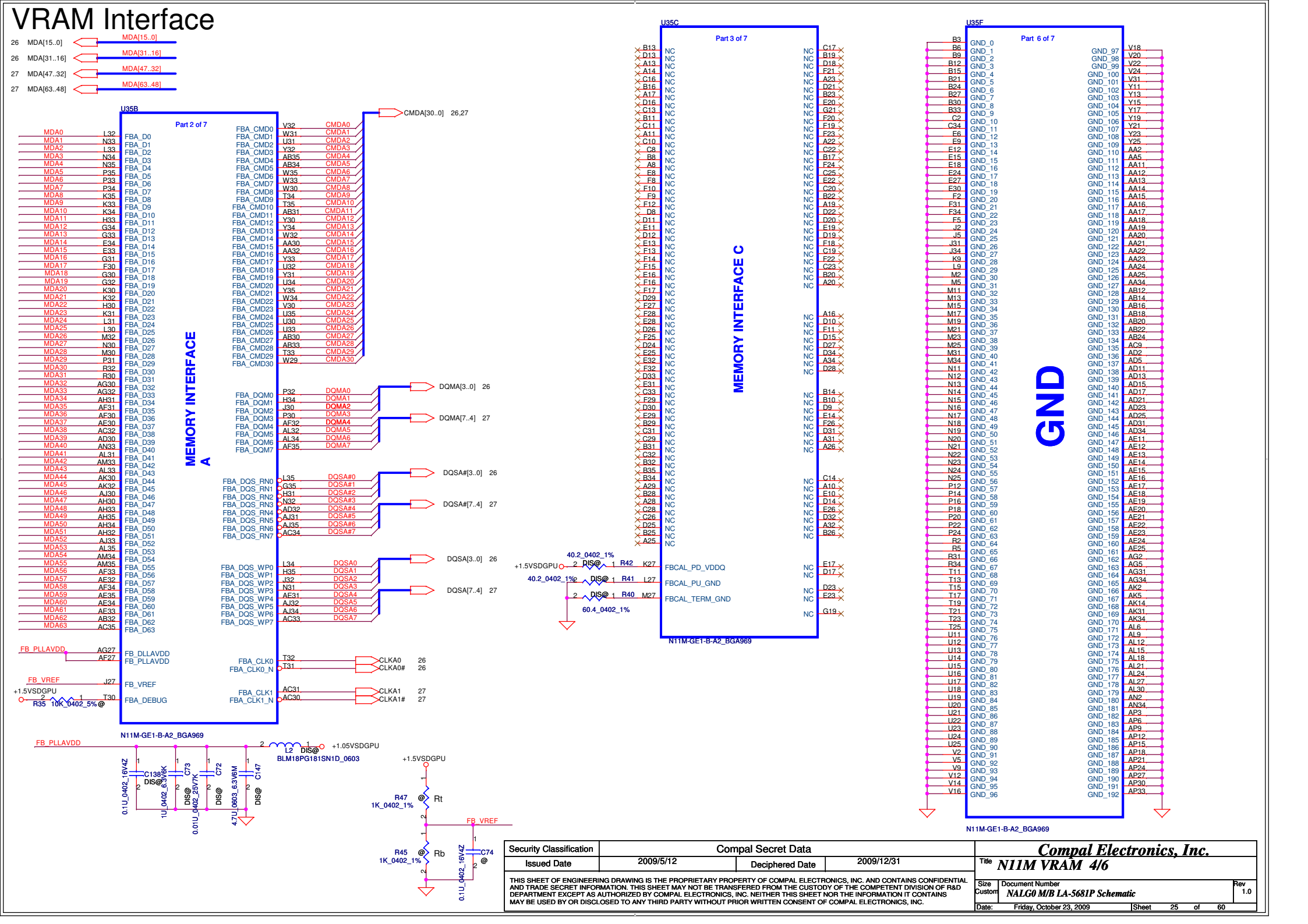
Compal Electronics, Inc.

Title: **N11M POWER & GND 3/6**

Size	Document Number	Rev
Custom	NALG0 M/B LA-5681P Schematic	1.0

Date: Friday, October 23, 2009 | Sheet 24 of 60

VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.
Title: N11M VRAM 4/6
Size: Custom
Document Number: NALG0 M/B LA-5681P Schematic
Rev: 1.0
Date: Friday, October 23, 2009
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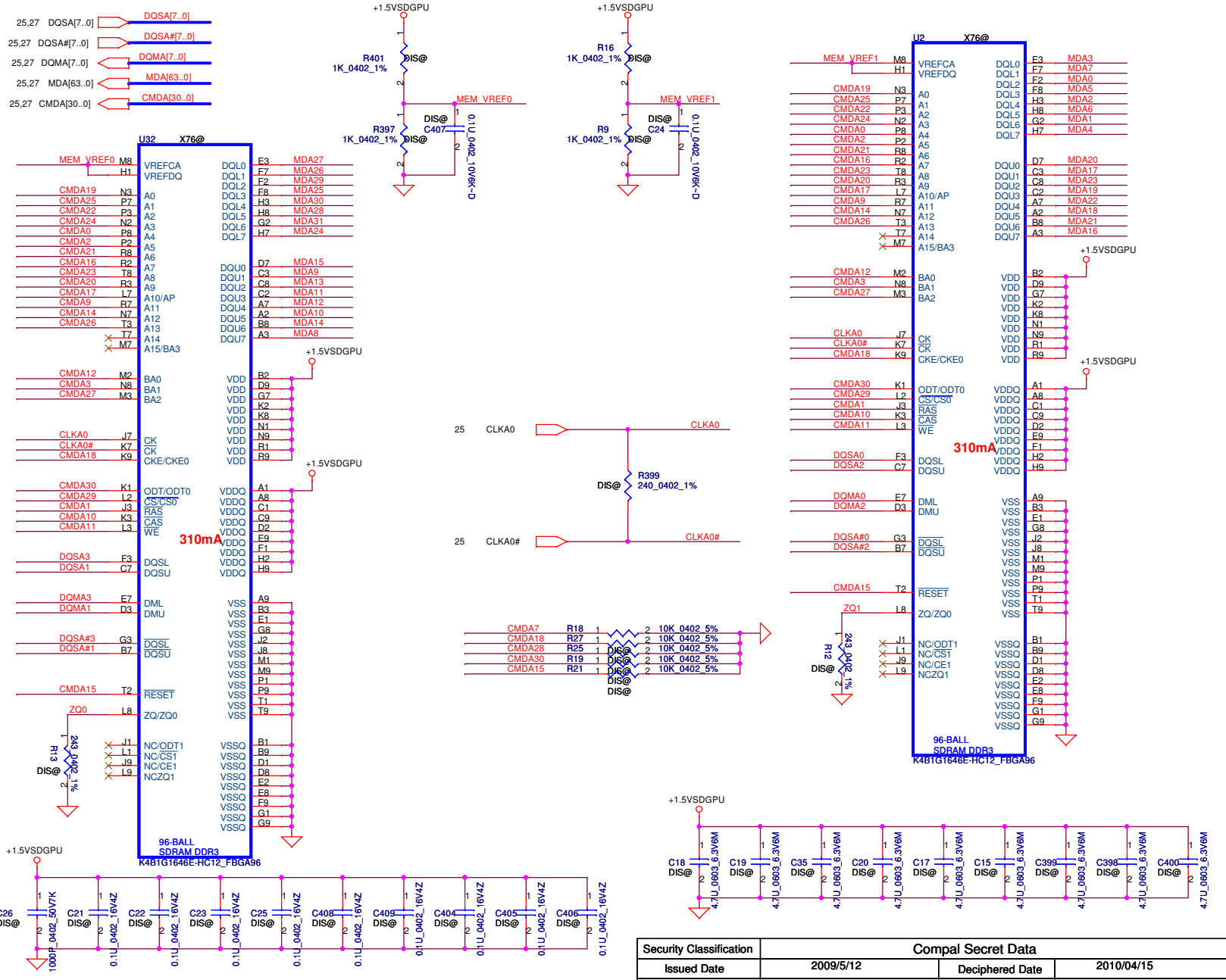
VRAM gDDR3 chips (256MB & 512MB)

32Mx16 gDDR2 *4==>256MB
64Mx16 gDDR3 *4==>512MB



Address	0..31	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS#	
CMD30	ODT	
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: N11M gDDR3 5/6

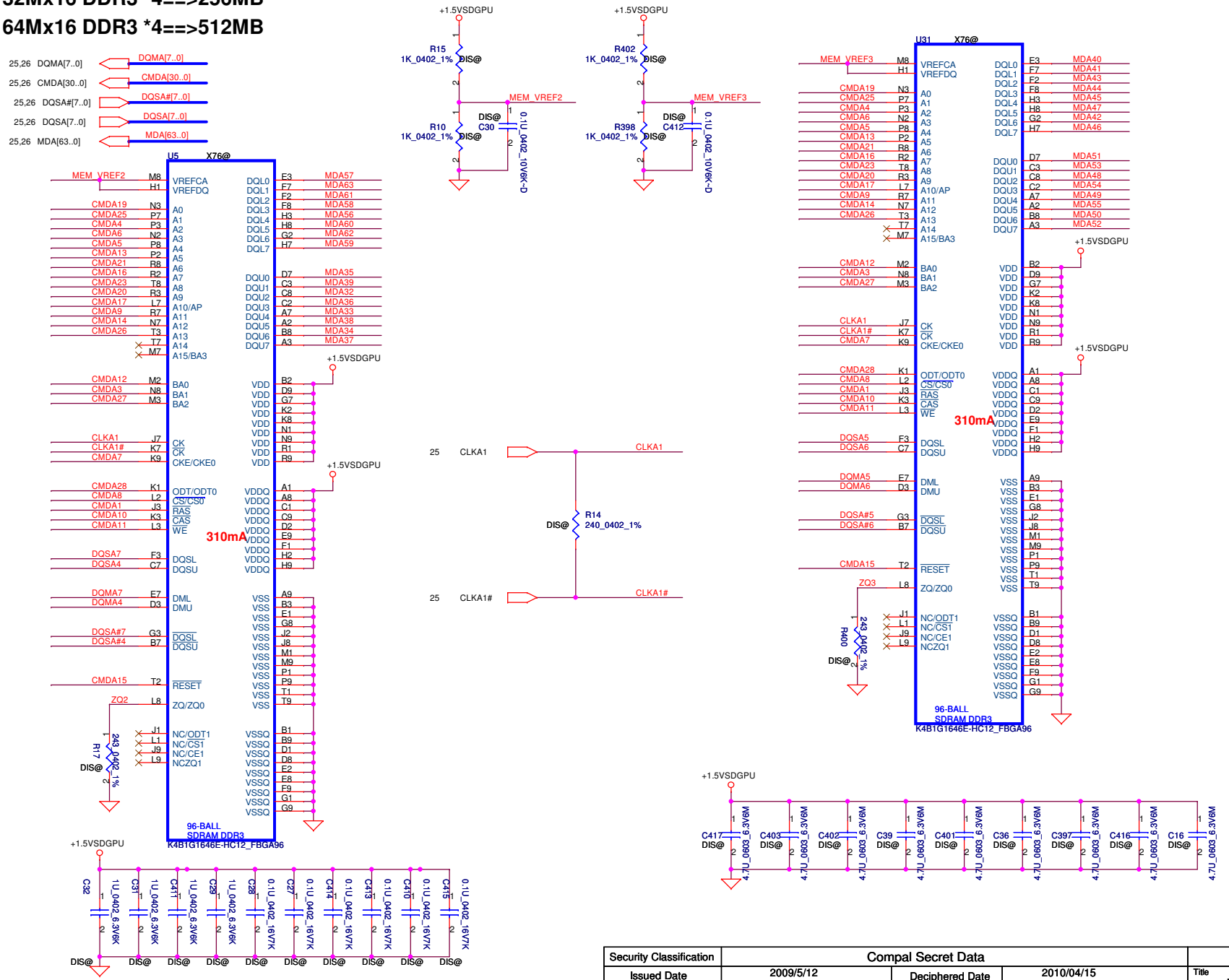
Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev:

Date: Friday, October 23, 2009 | Sheet 26 of 60

VRAM DDR3 chips (256MB & 512MB)

32Mx16 DDR3 *4==>256MB

64Mx16 DDR3 *4==>512MB



Address	0..31	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS#	
CMD30	ODT	
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

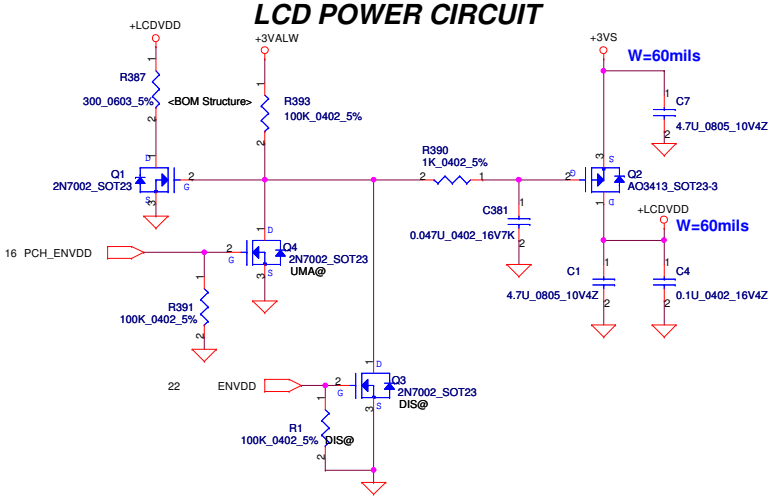
Compal Electronics, Inc.

Title: N11M gDDR3 6/6

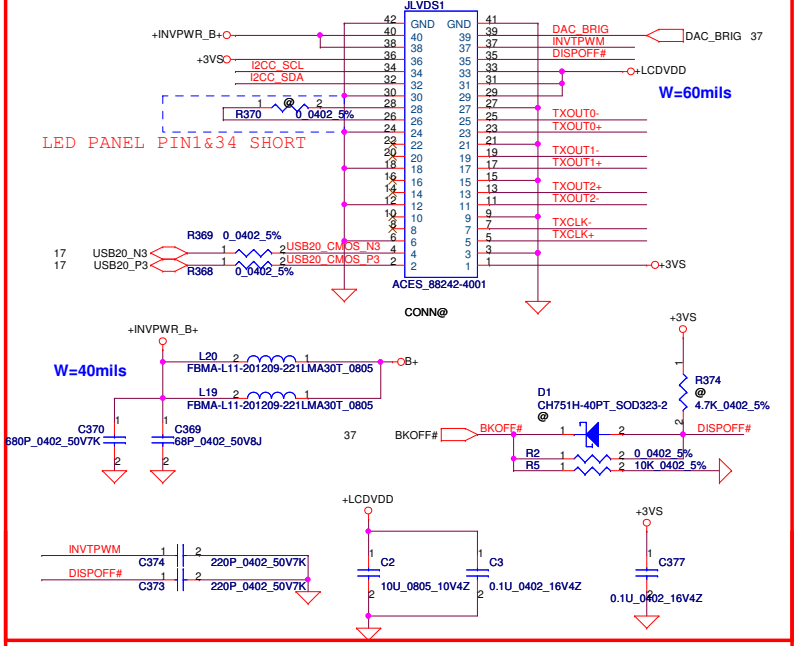
Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 27 of 60

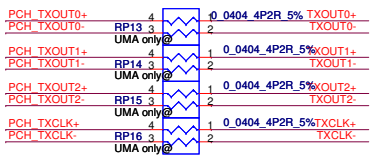
LCD POWER CIRCUIT



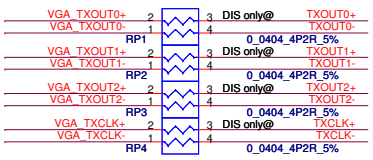
LED PANEL Conn.

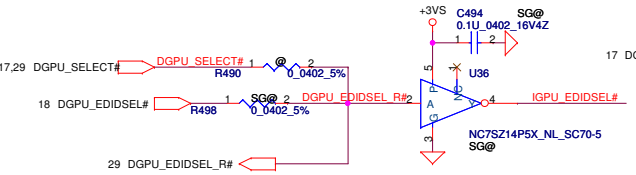


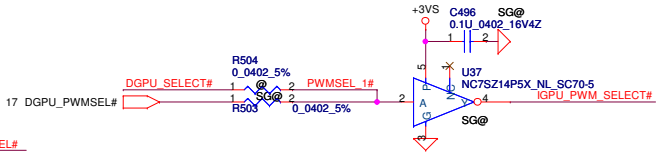
UMA ONLY

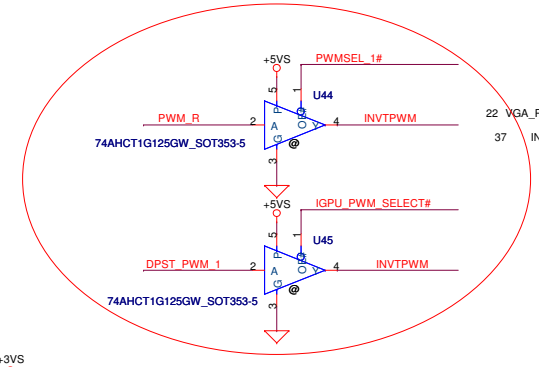


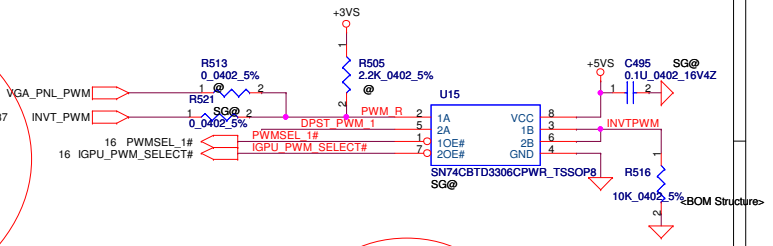
DIS ONLY

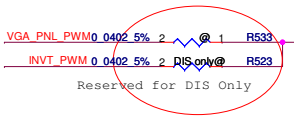


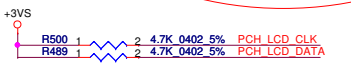


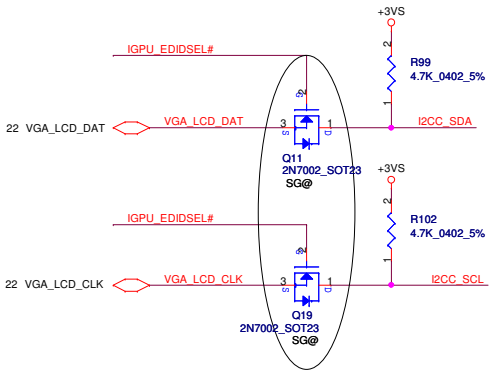


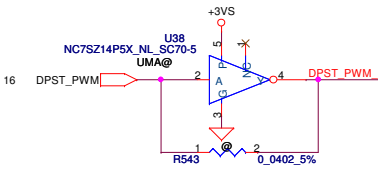


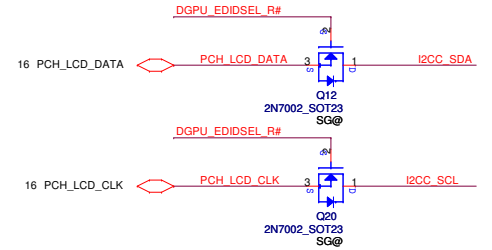






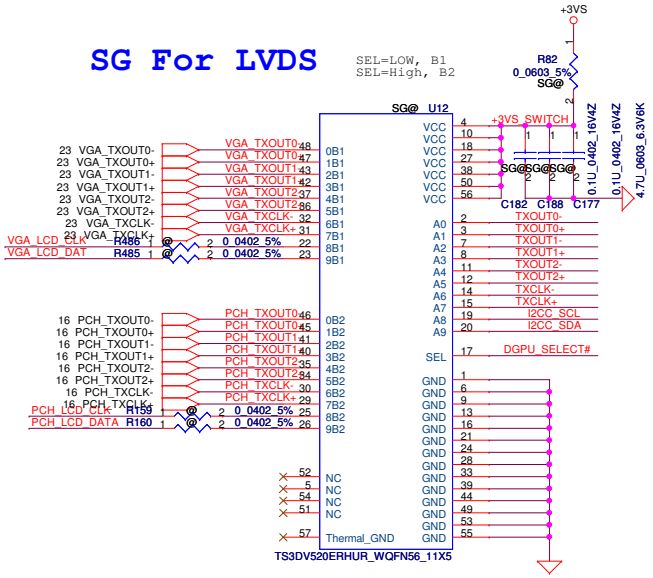






SG For LVDS

SEL=LOW, B1
SEL=High, B2



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

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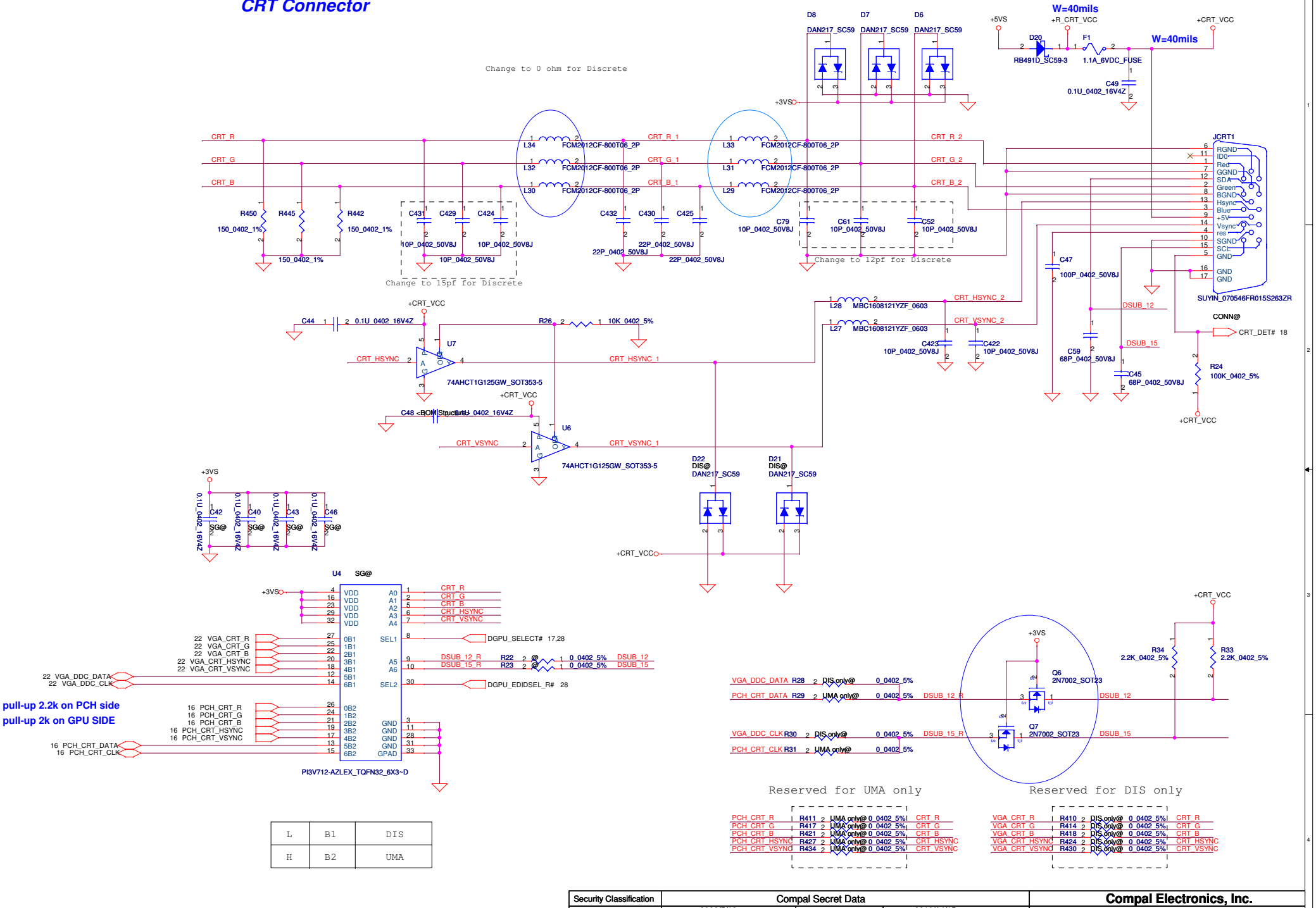
CRT Connector



L	B1	DIS
H	B2	UMA

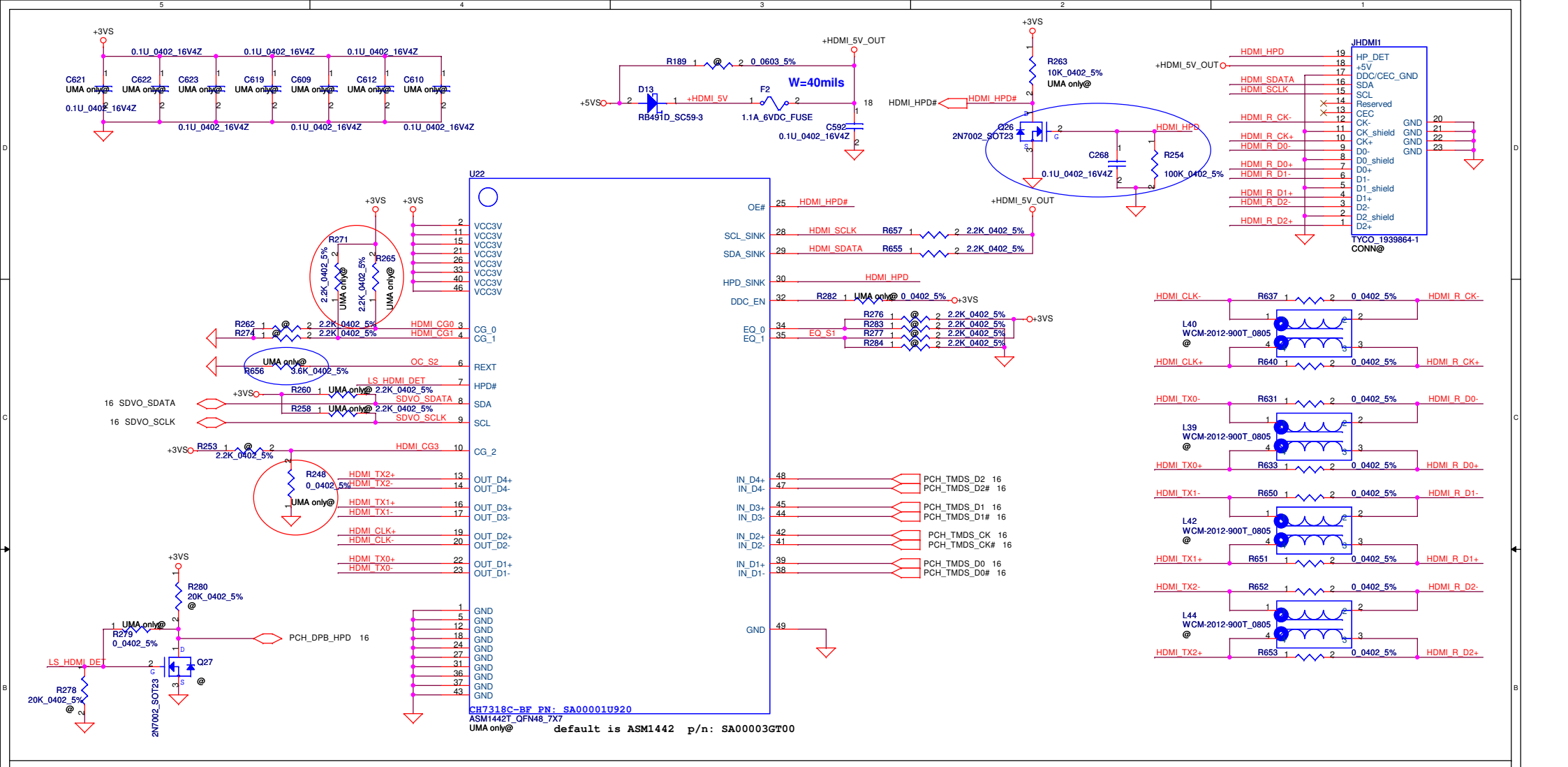
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 29 of 60



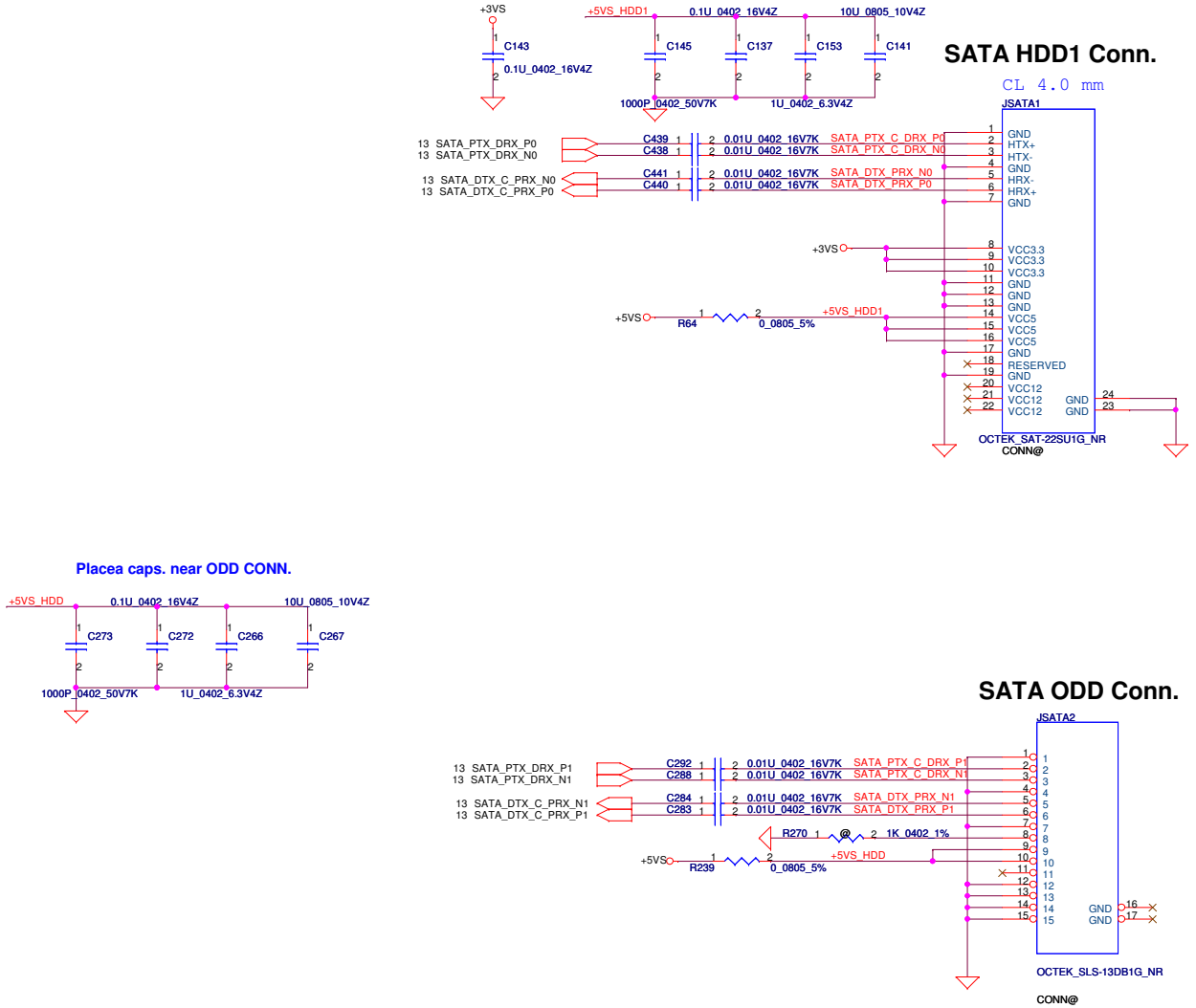
Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: HDMI Level Shife & Conn

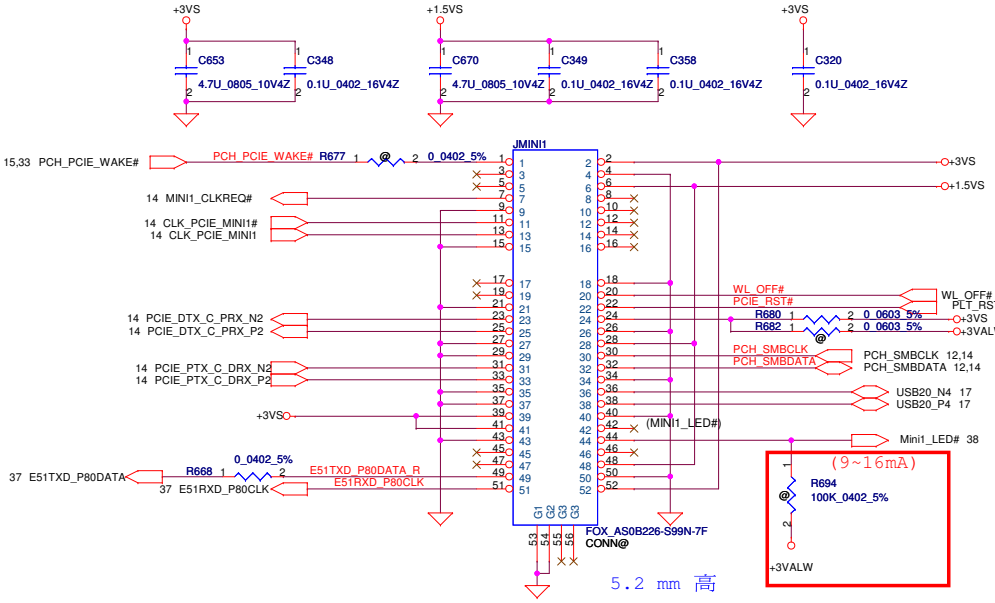
Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 30 of 60

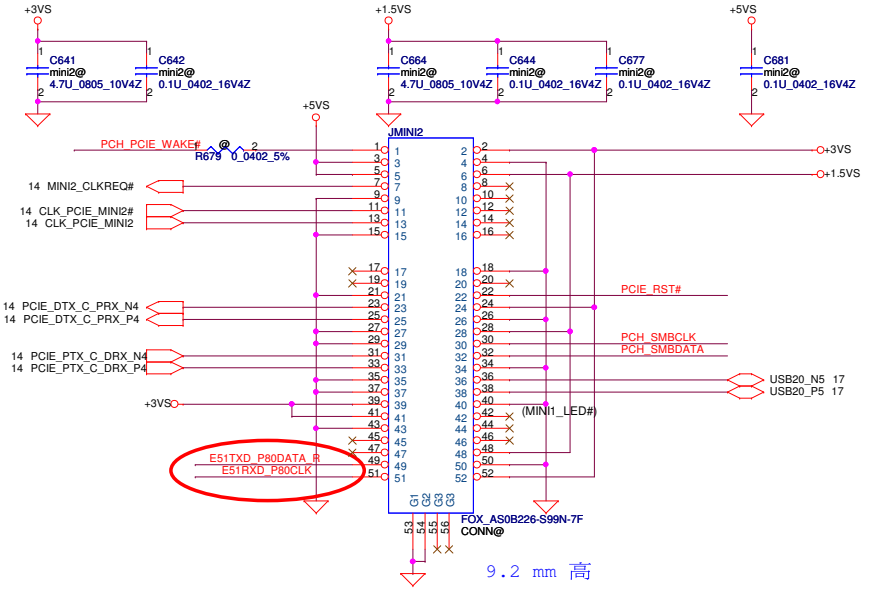


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/5/12	Deciphered Date 2010/04/15	Title: HDD & ODD & MINI CARD &CARDREADER Connector
			Size: B; Document Number: NALG0 M/B LA-5681P Schematic; Rev: 1.0
			Date: Friday, October 23, 2009; Sheet 31 of 60

For Wireless LAN



For TV-Tuner/HW MPEG



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/5/12	Deciphered Date 2007/12/25	Title: MINI CARD (WLAN & TV-Tuner)
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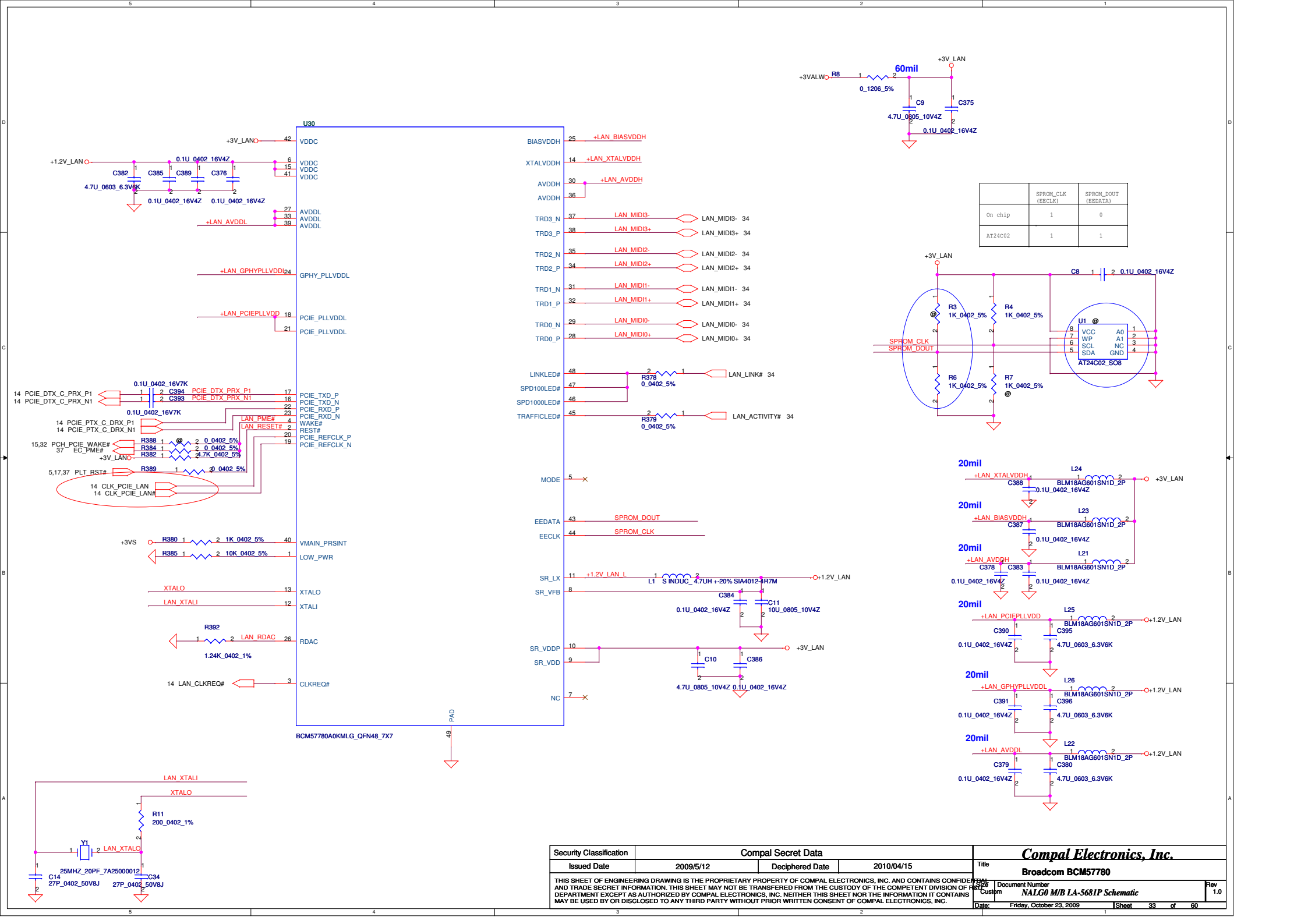
			Date: Friday, October 23, 2009; Sheet 32 of 60



	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

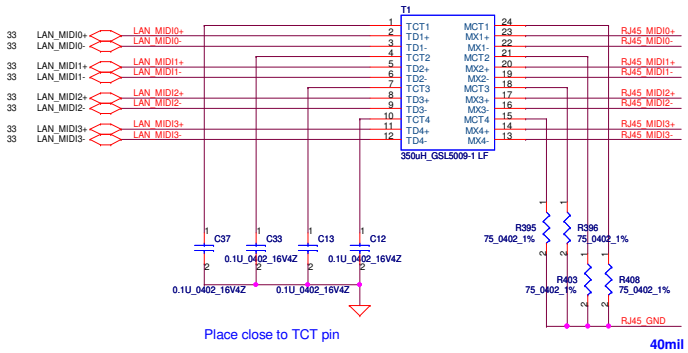
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

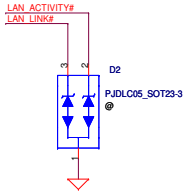
Compal Electronics, Inc.

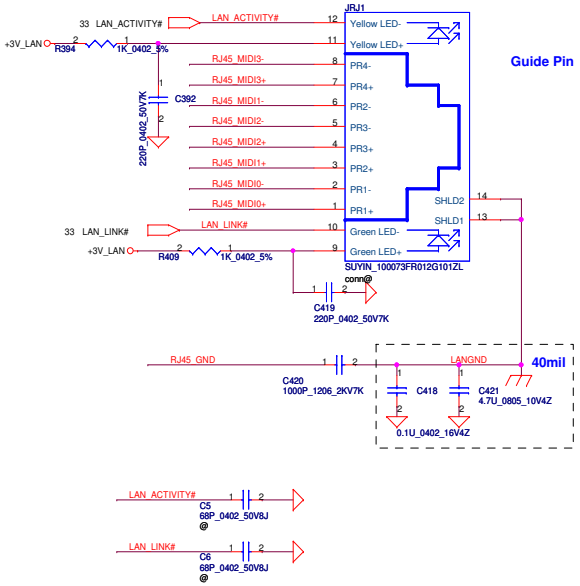
Title: Broadcom BCM57780

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 33 of 60



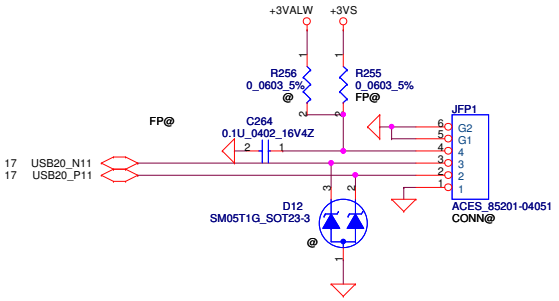




Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

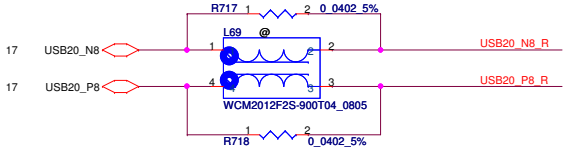
Compal Electronics, Inc.			
Title	LAN Magnetic & RJ45		
Size	Document Number	NALG0 M/B LA-5681P Schematic	Rev 1.0
Date: Friday, October 23, 2009	Sheet 34 of 60		

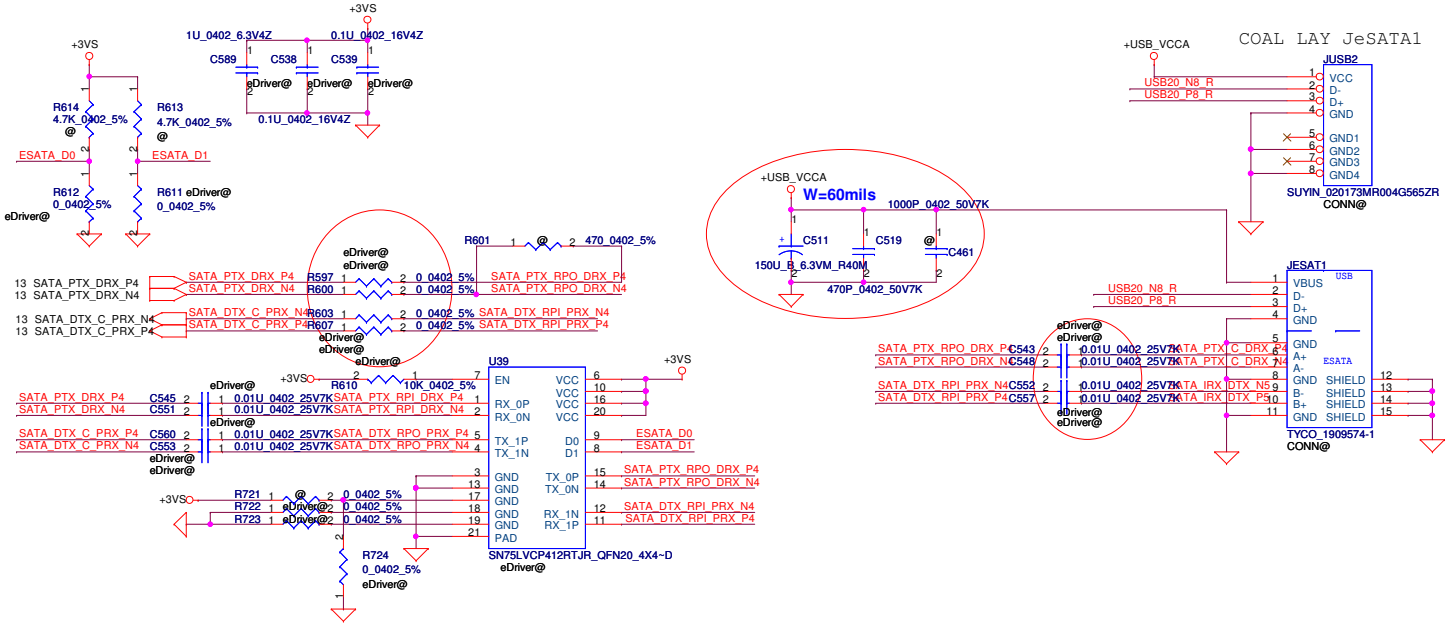
Finger Print Conn.



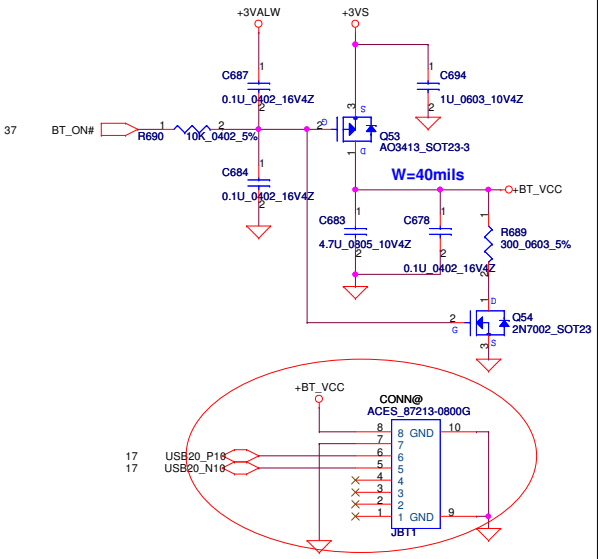
ESATA CONN

D0	D1	Function
0	0	defalut; CH0/CH1 ->0dB
0	1	CH0->2.5dB pre-emphasis;CH1->0dB
1	0	CH1->2.5dB pre-emphasis;CH0->0dB
1	1	CH0/CH1->2.5dB pre-emphasis

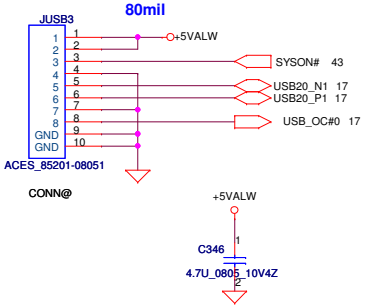




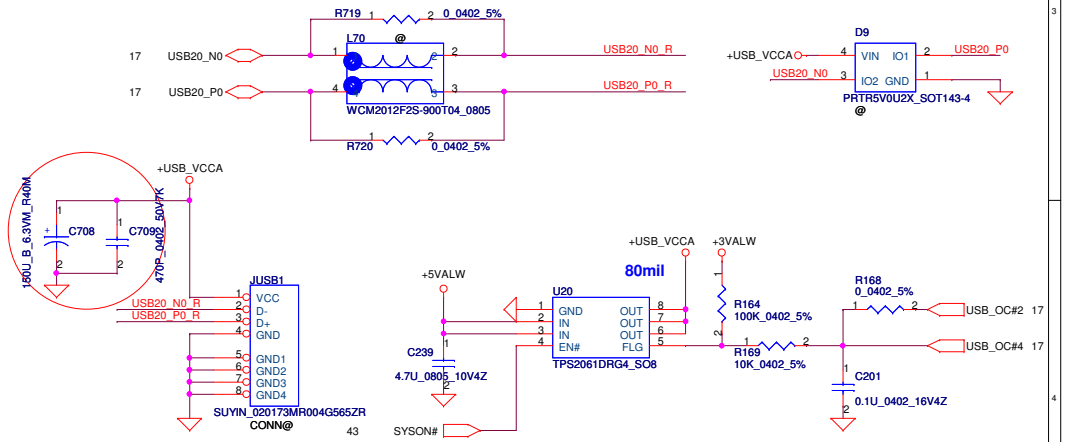
Bluetooth Conn.



To USB/B Connector



USB CONN.



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: NEW CARD & eSATA Connector

Size: B | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

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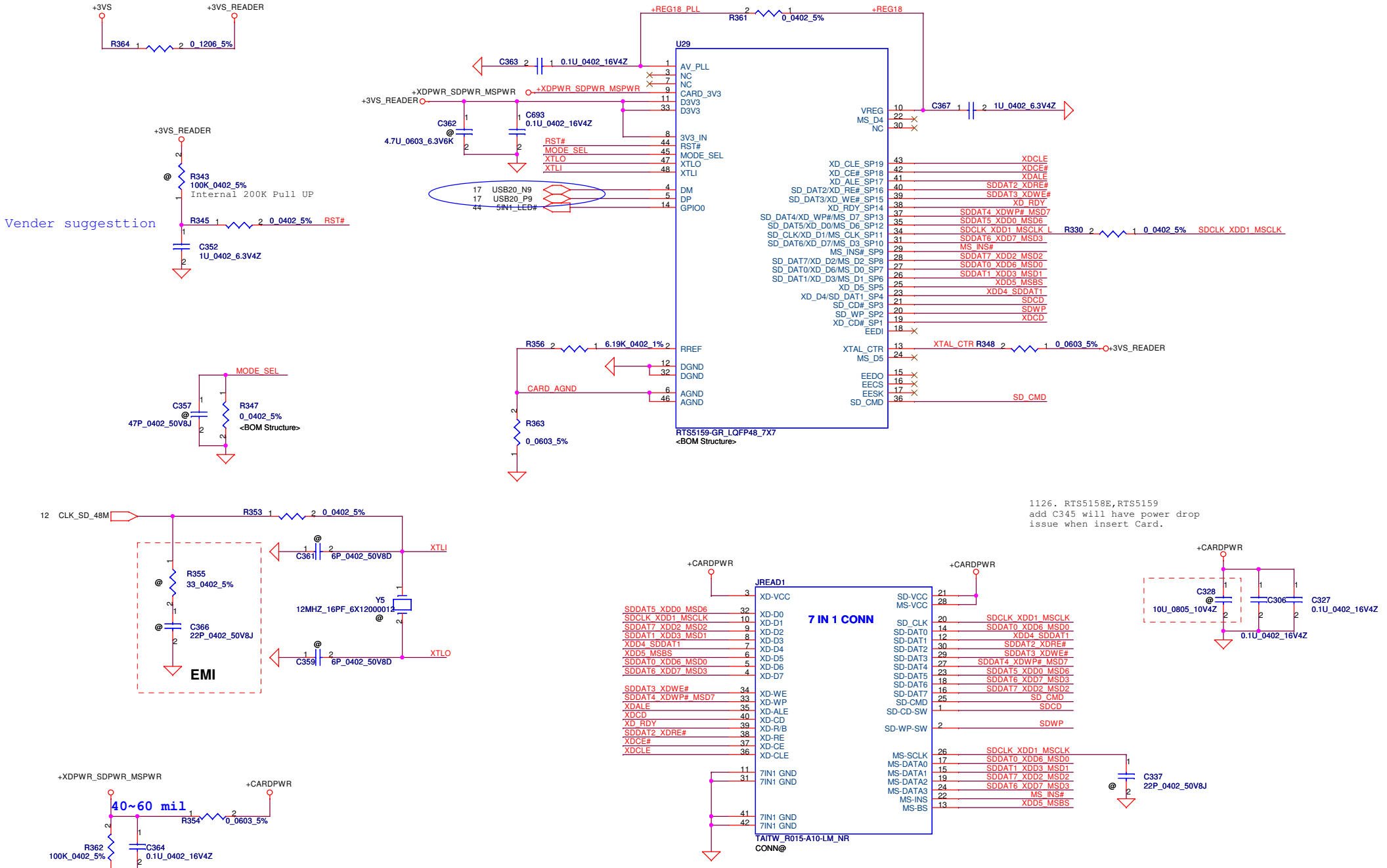


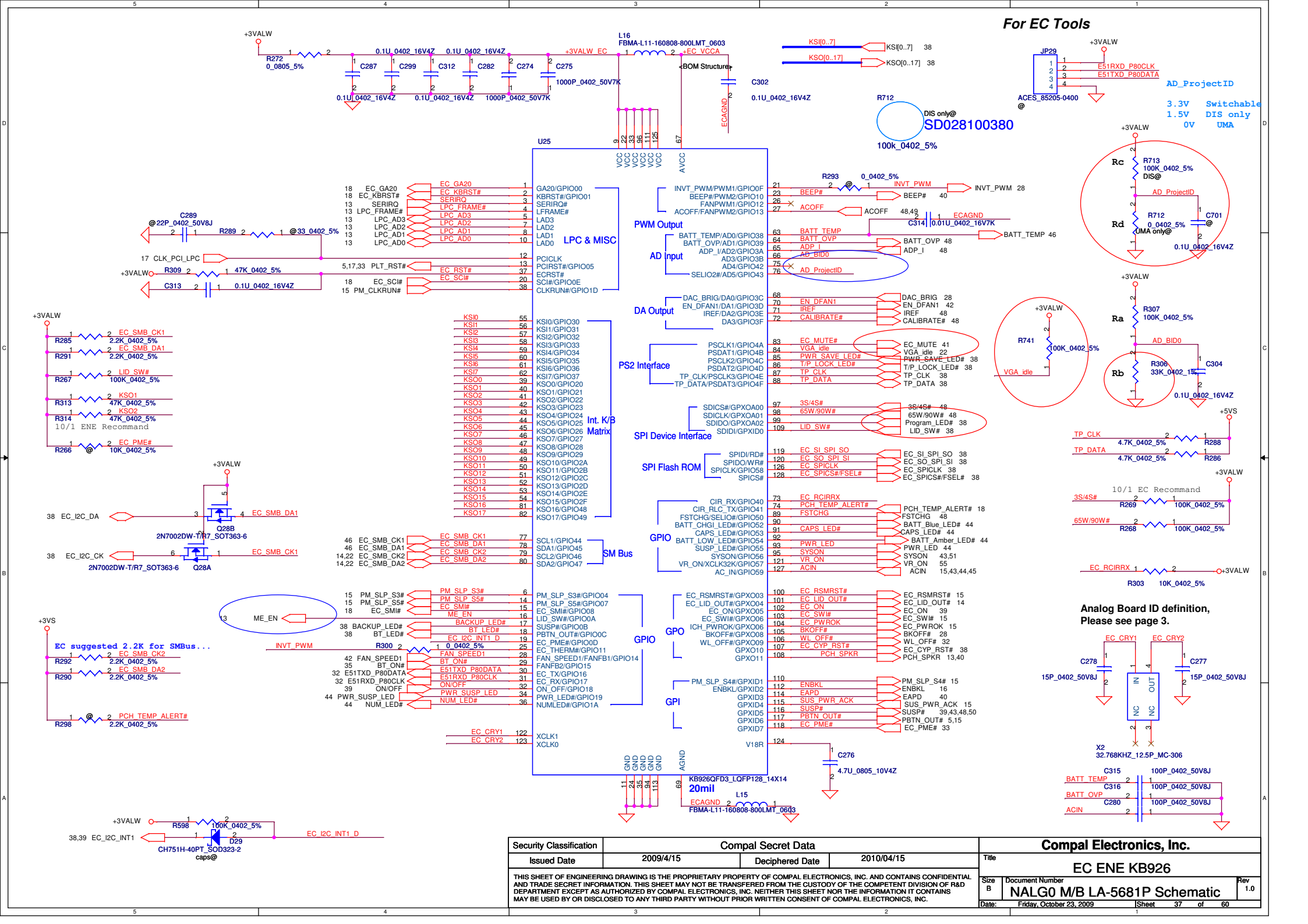
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/08/10

Compal Electronics, Inc.

Title: Card Reader RTS5159

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 36 of 60


For EC Tools
U25
KB926QFD3_LQFP128_14X14
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
AD_ProjectID
3.3V Switchable
1.5V DIS only
0V UMA
SD028100380
DIS only@
100k_0402_5%
Analog Board ID definition,
Please see page 3.
EC suggested 2.2K for SMBus...
10/1 ENE Recommand
10/1 EC Recommand
Compal Electronics, Inc.
EC ENE KB926
NALG0 M/B LA-5681P Schematic
Compal Secret Data
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2010/04/15
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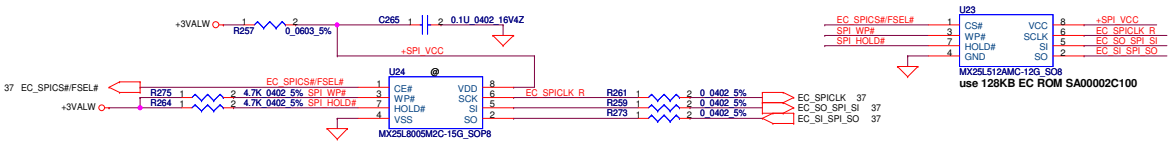
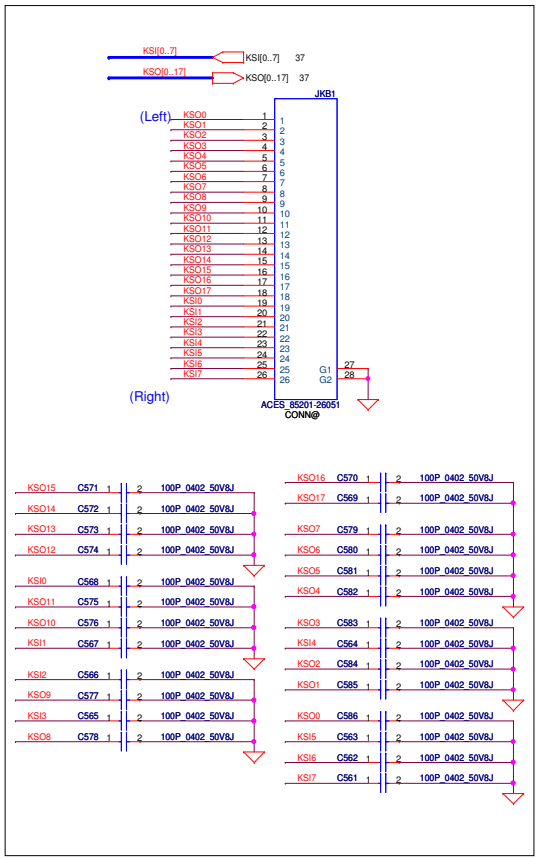
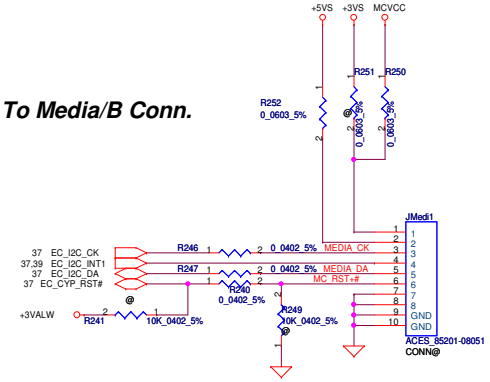


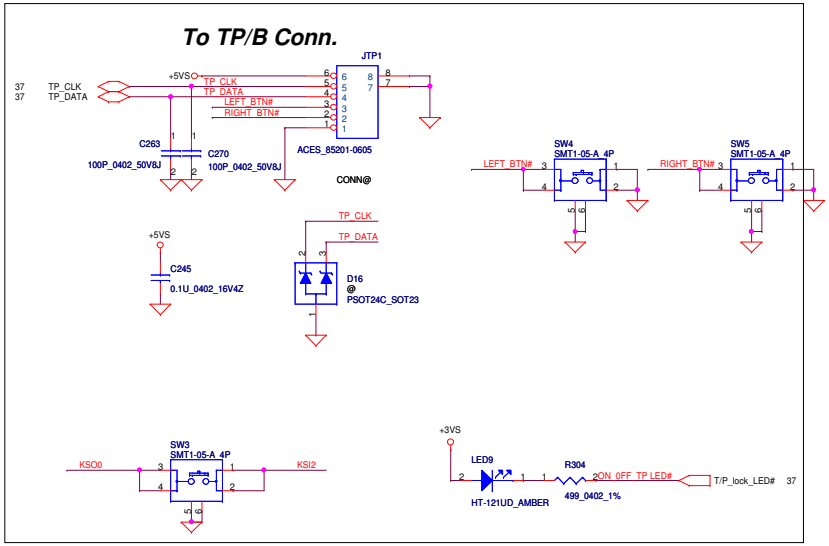
ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz



To Media/B Conn.



To TP/B Conn.

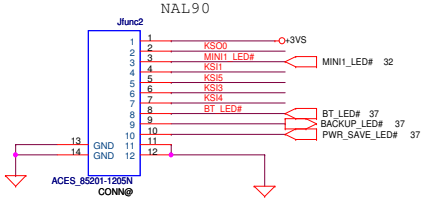


To BTN/B Conn.

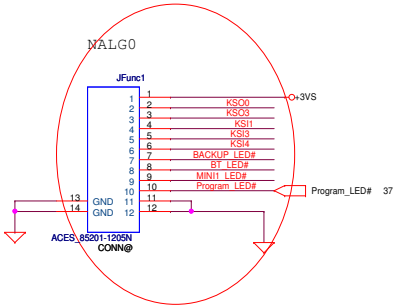
	KSO0	KSO3
KSI1	WL_BTN#	Program_BTN#
KSI2	T/P lock_BTN#	
KSI3	Back up_BTN#	Volum up_BTN#
KSI4	BT_BTN#	Volum down_BTN#
KSI5	Power save_BTN#	

FN/B

NAL90

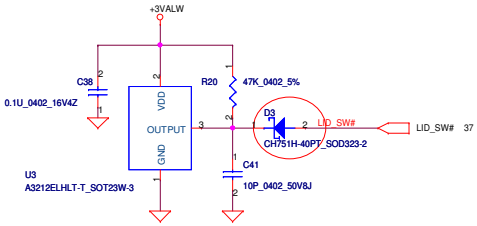


NALG0



Lid Switch

(Hall Effect Switch)



Anpec p/n:SA00003B900

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

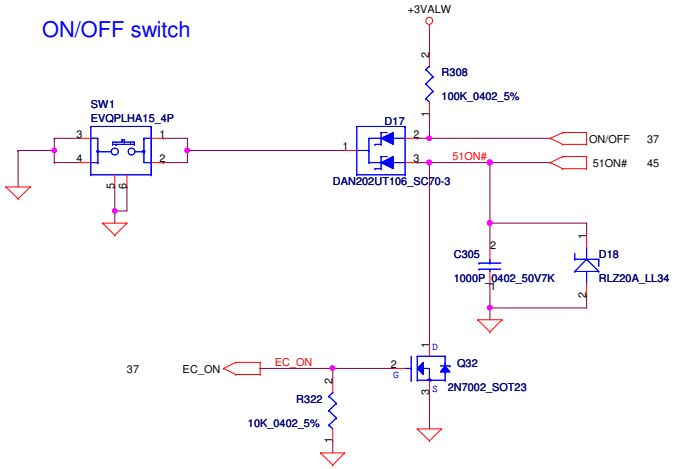
Title: BIOS, I/O Port & K/B Connector

Size: C | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 0.3

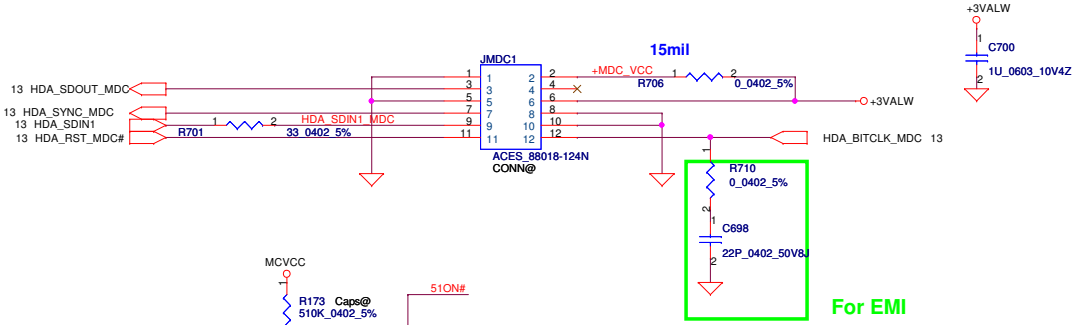
Date: Friday, October 23, 2009 | Sheet 38 of 60

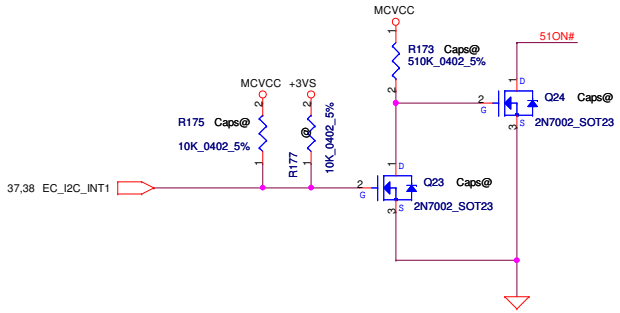
Power Button

ON/OFF switch

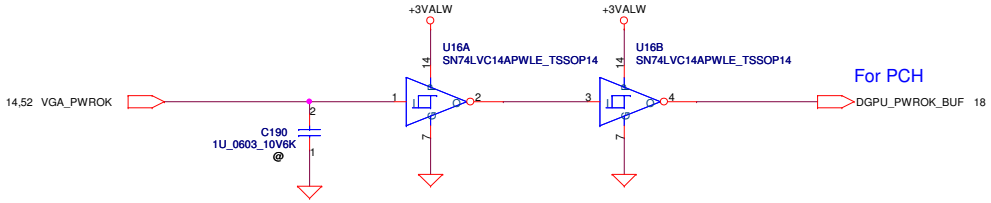


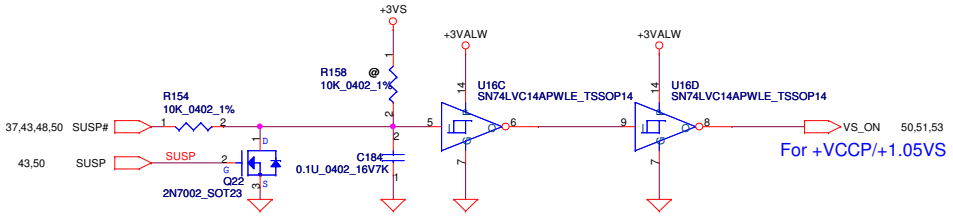
HDA MDC Conn.

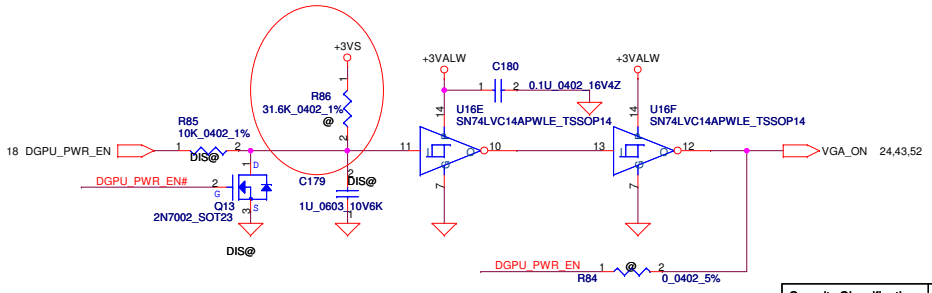


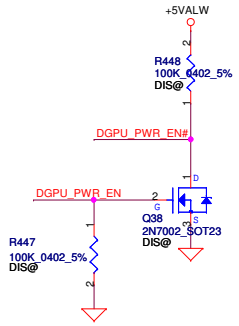


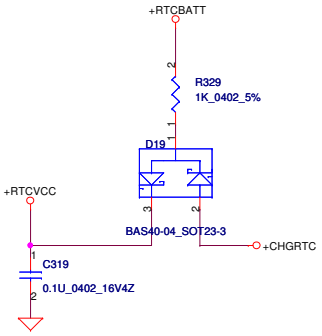
Power ON Circuit











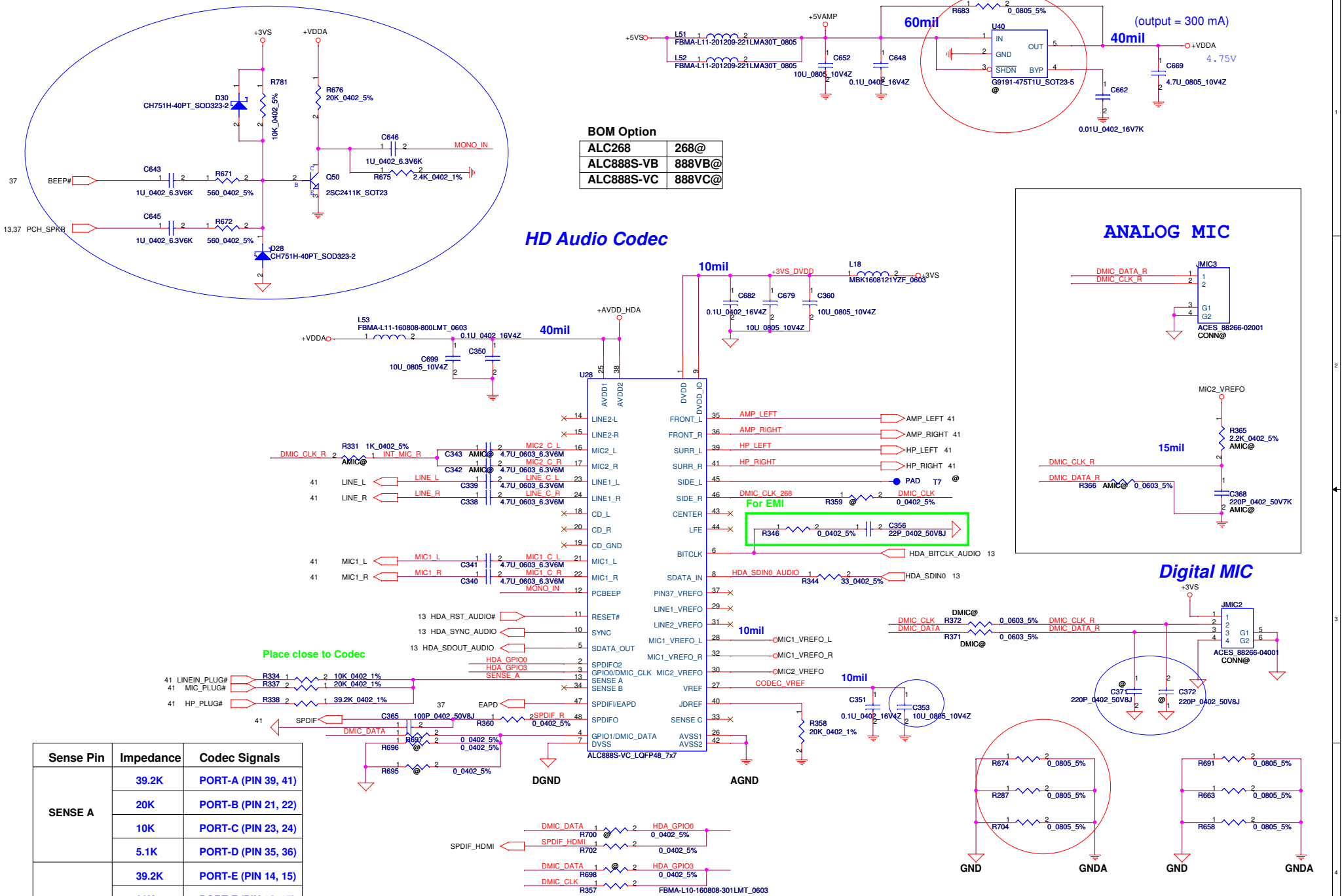
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: Power OK, Reset,RTC, CIR, MDC

Size: B | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

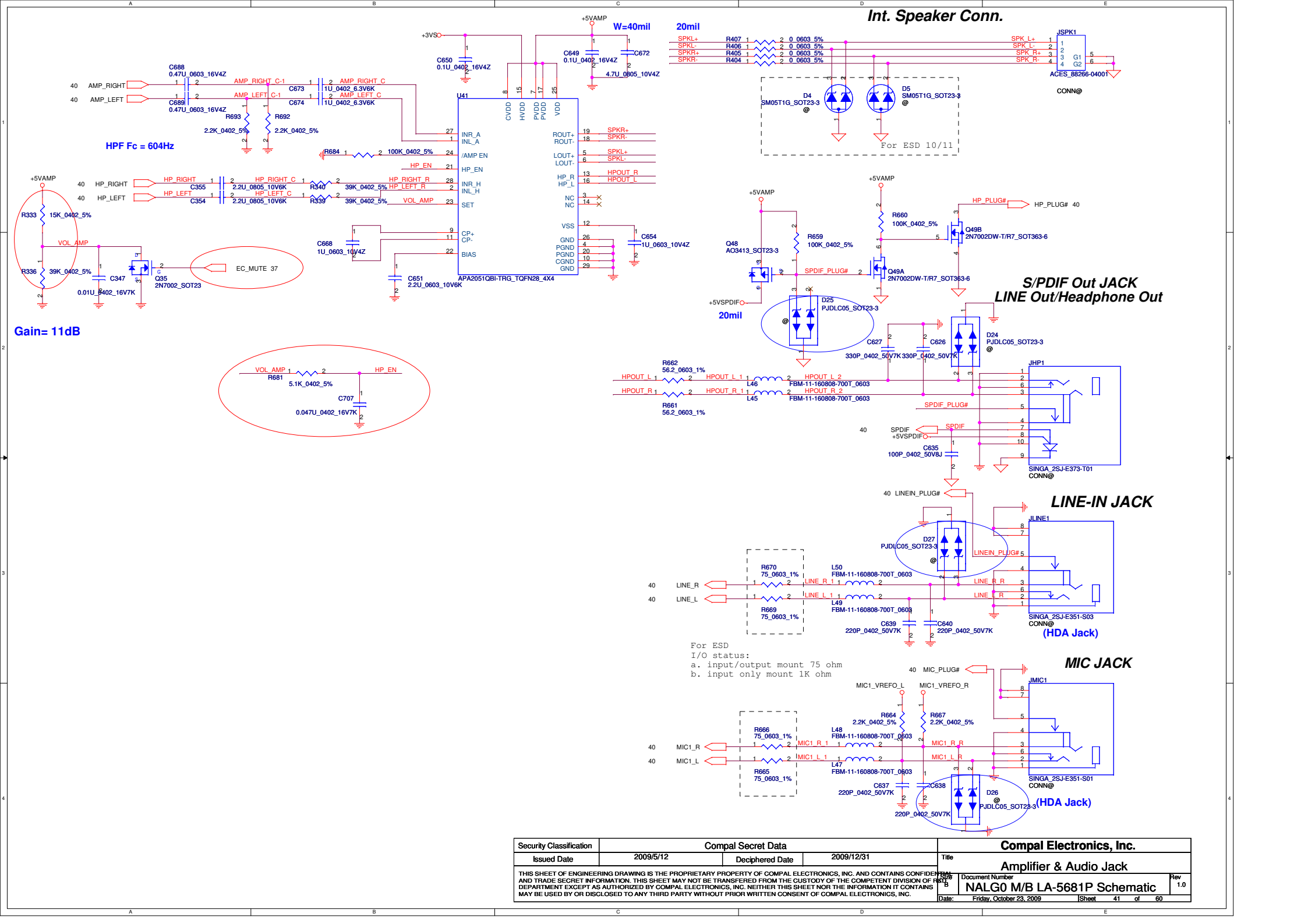
Date: Friday, October 23, 2009 | Sheet 39 of 60



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.	
Title	HD Audio Codec ALC888S-VC
Size B	Document Number NALG0 M/B LA-5681P Schematic
Rev	1.0
Date: Friday, October 23, 2009	Sheet 40 of 60



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

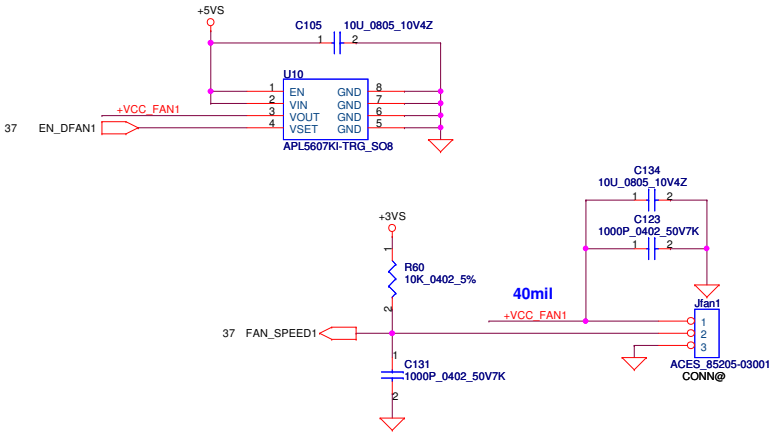
Compal Electronics, Inc.

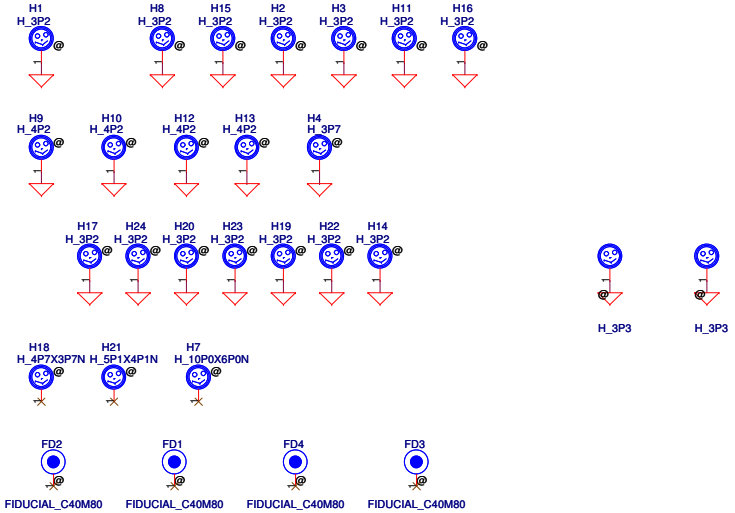
Title: Amplifier & Audio Jack

Size: B | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 41 of 60

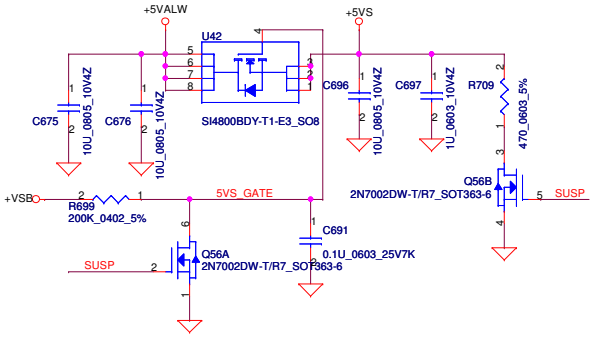
FAN1 Conn



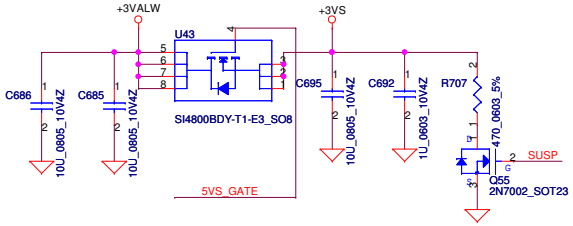


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/5/12	Deciphered Date	2009/12/31
Title	FAN & COVER LIGHT& Screw Hole		
Size B	Document Number NALG0 M/B LA-5681P Schematic		Rev 1.0
Date: Friday, October 23, 2009	Sheet 42 of 60		

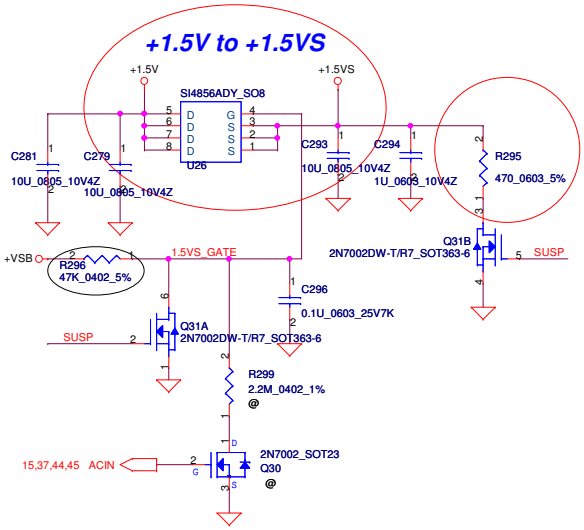
+5VALW TO +5VS



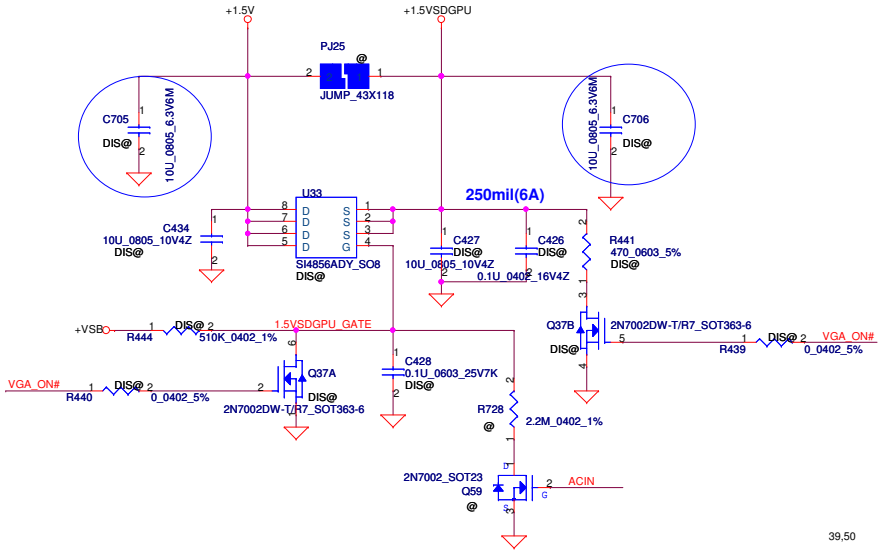
+3VALW TO +3VS



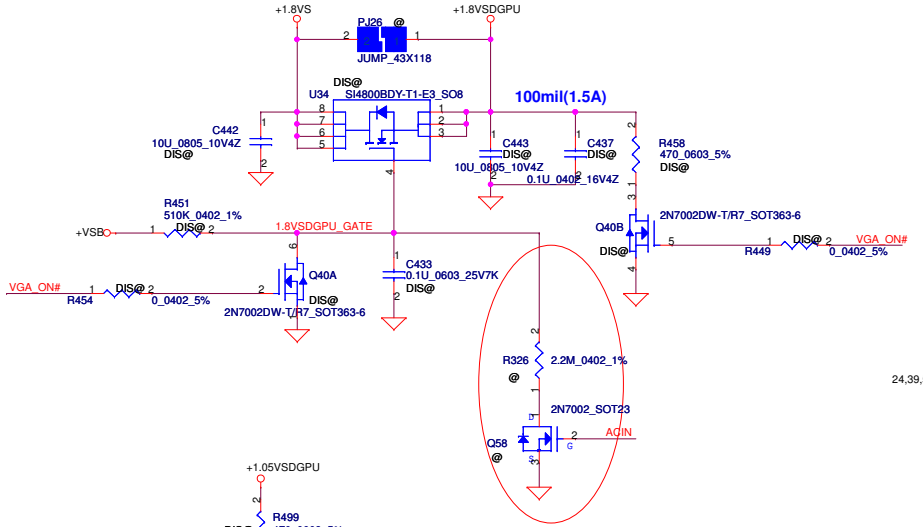
+1.5V to +1.5VS

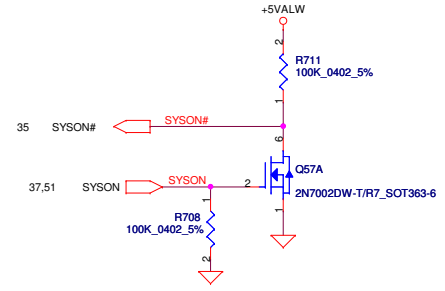


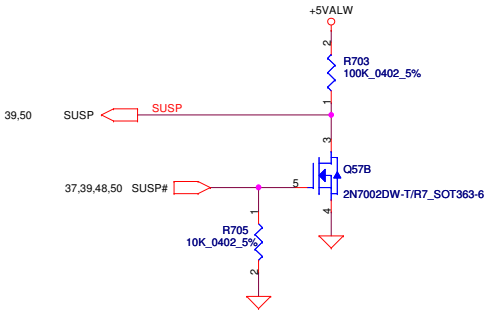
+1.5V to +1.5VSDGPU Transfer

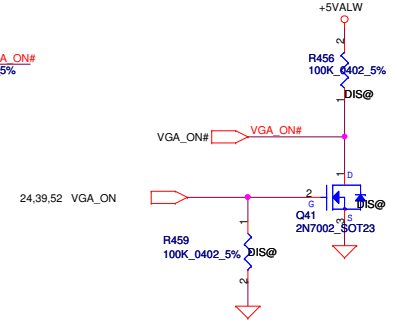


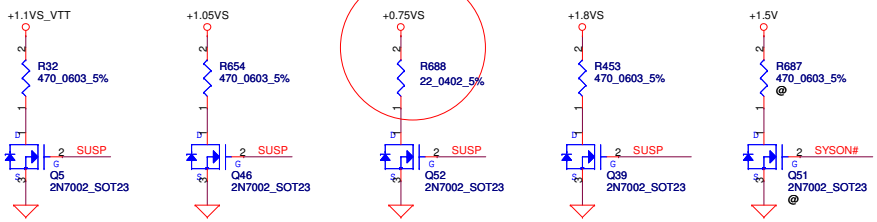
+1.8VS to +1.8VSDGPU Transfer

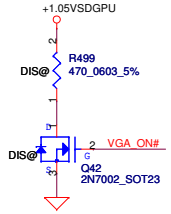












Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

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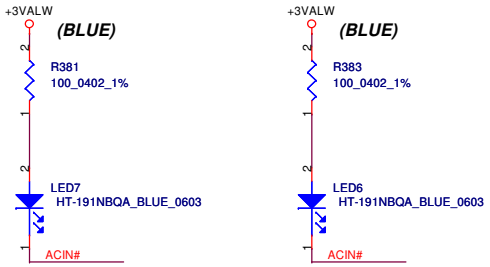
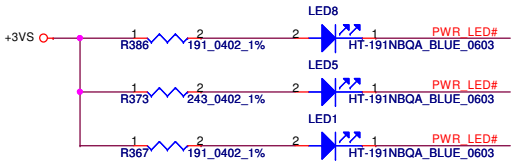
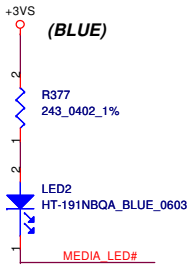
Enlightener LED



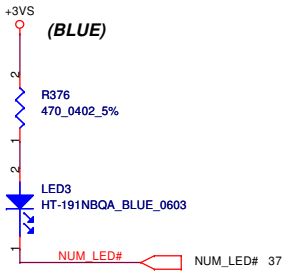
ON/OFF LED LEFT



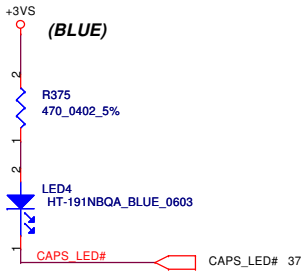
MEDIA_LED

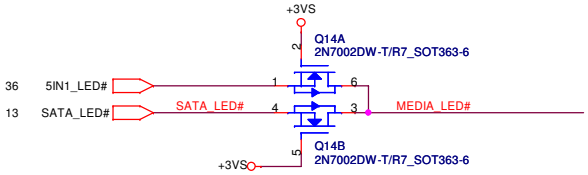


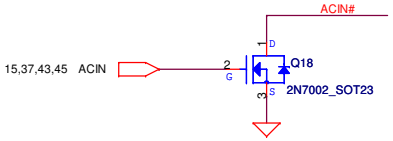
NUM_LED

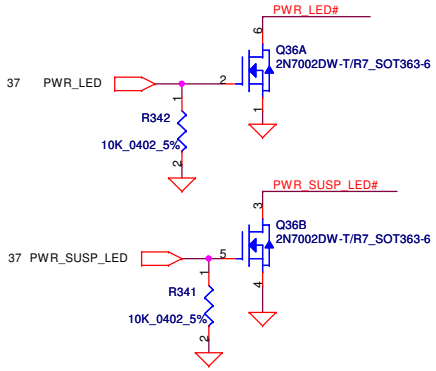


CAPS_LED

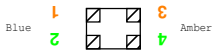


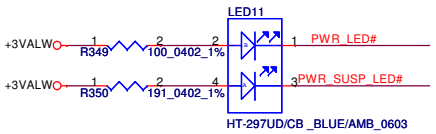


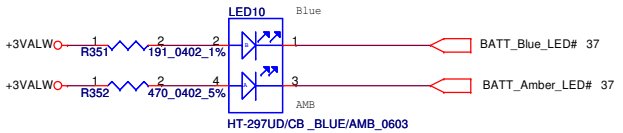




Compal Footprint







Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: PWR/B

Size	Document Number	Rev
Custom	NALG0 M/B LA-5681P Schematic	1.0

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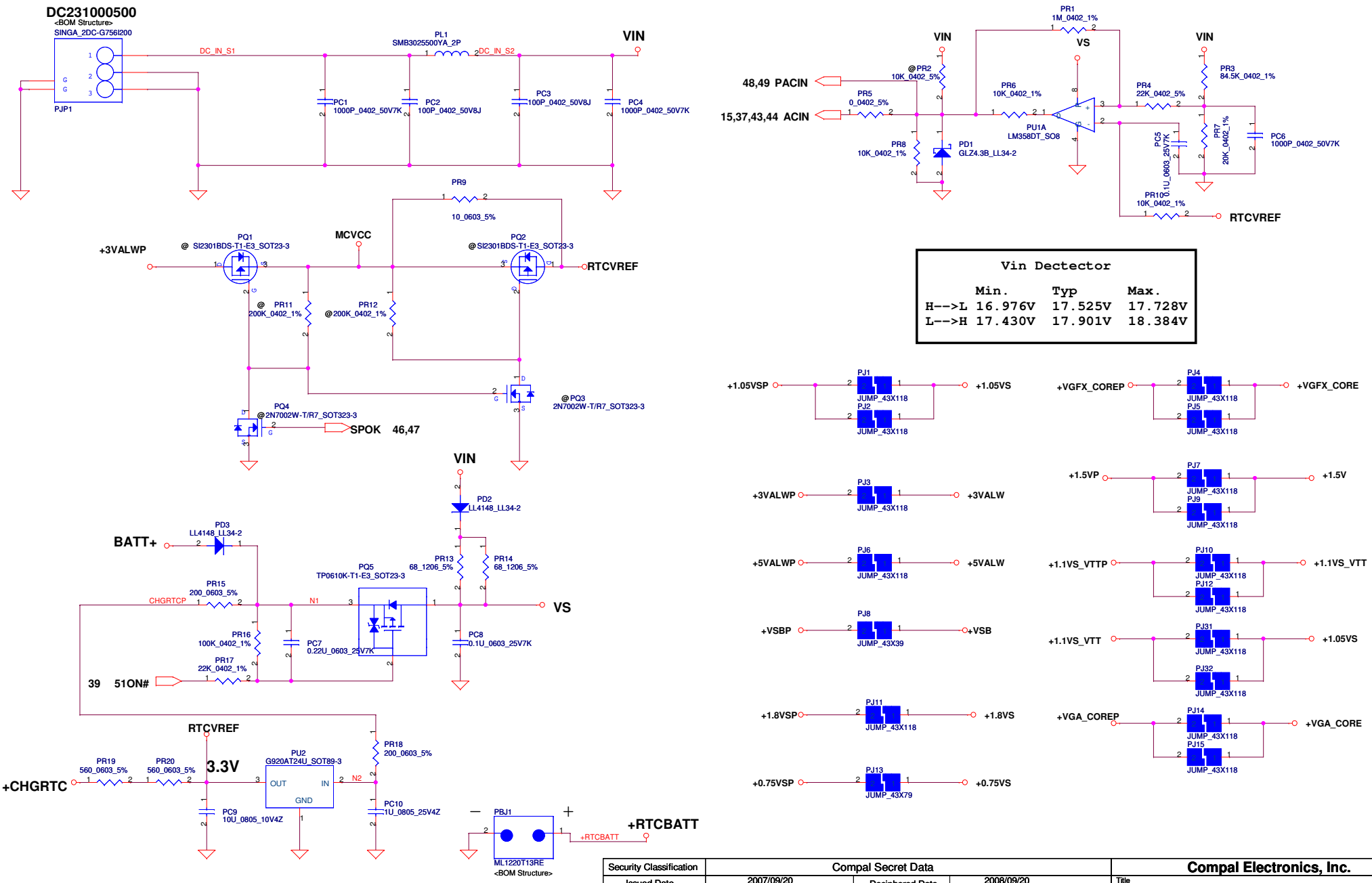

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size: Custom | Document Number: NALG0 | Rev: 0.1

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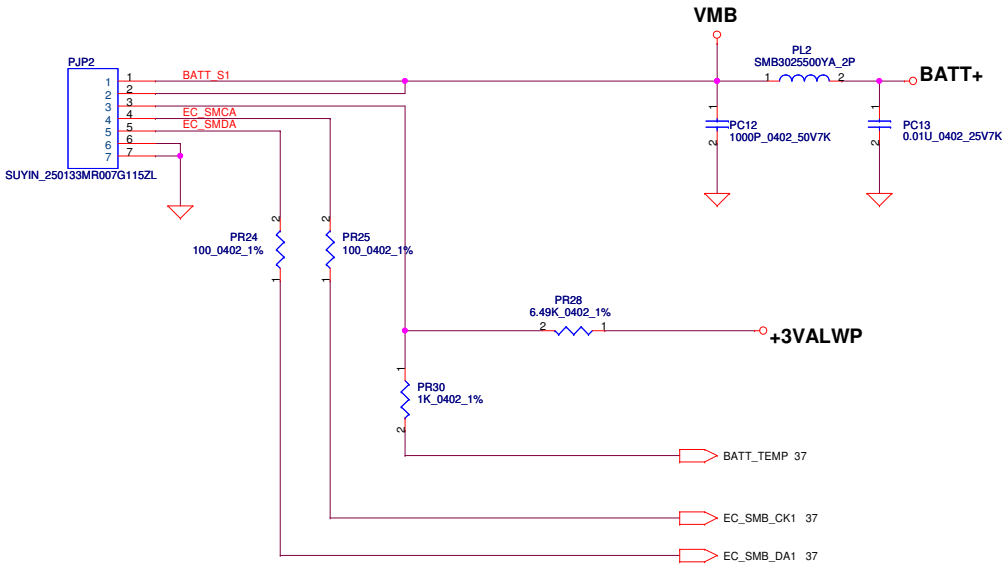
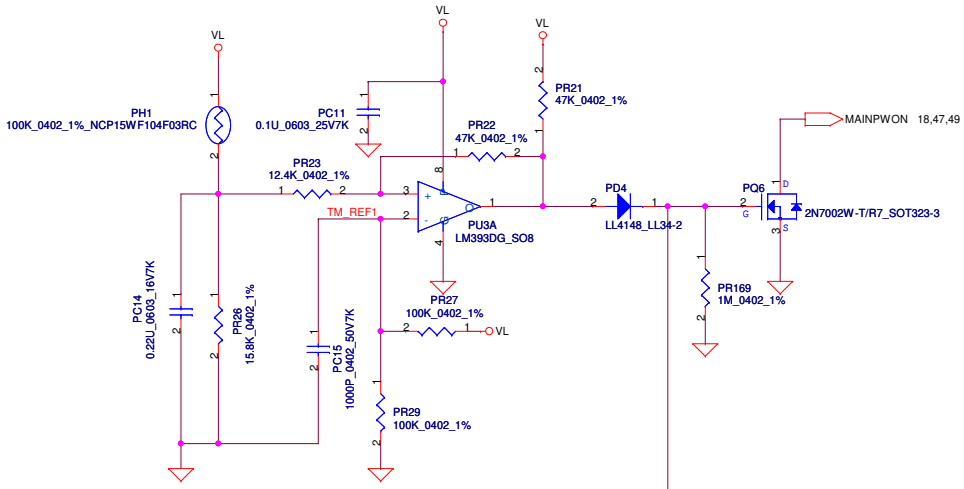
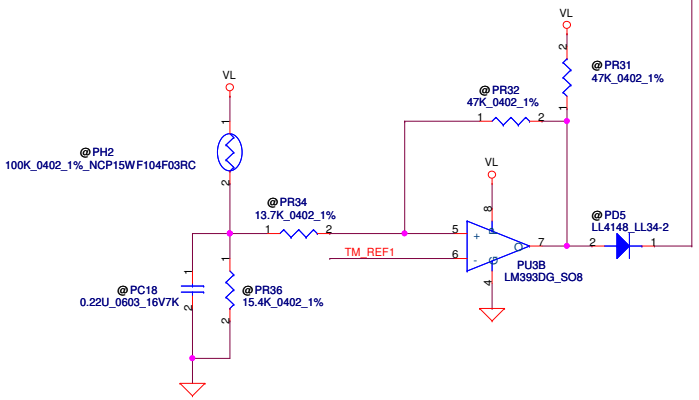
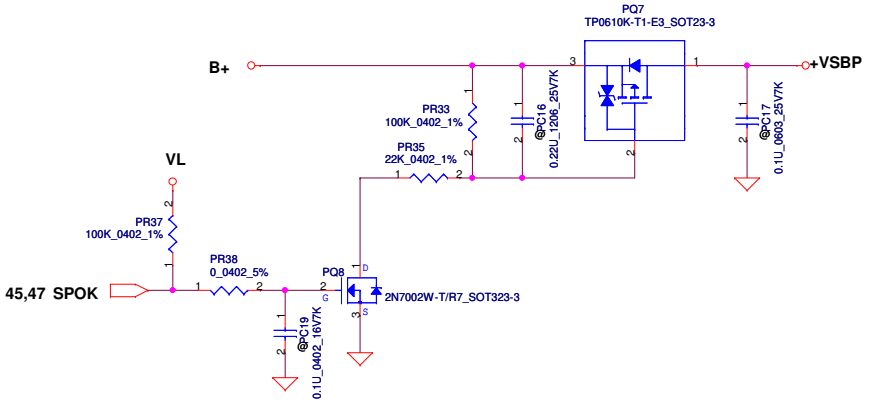
PH1 under CPU botten side :
CPU thermal protection at 92 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C





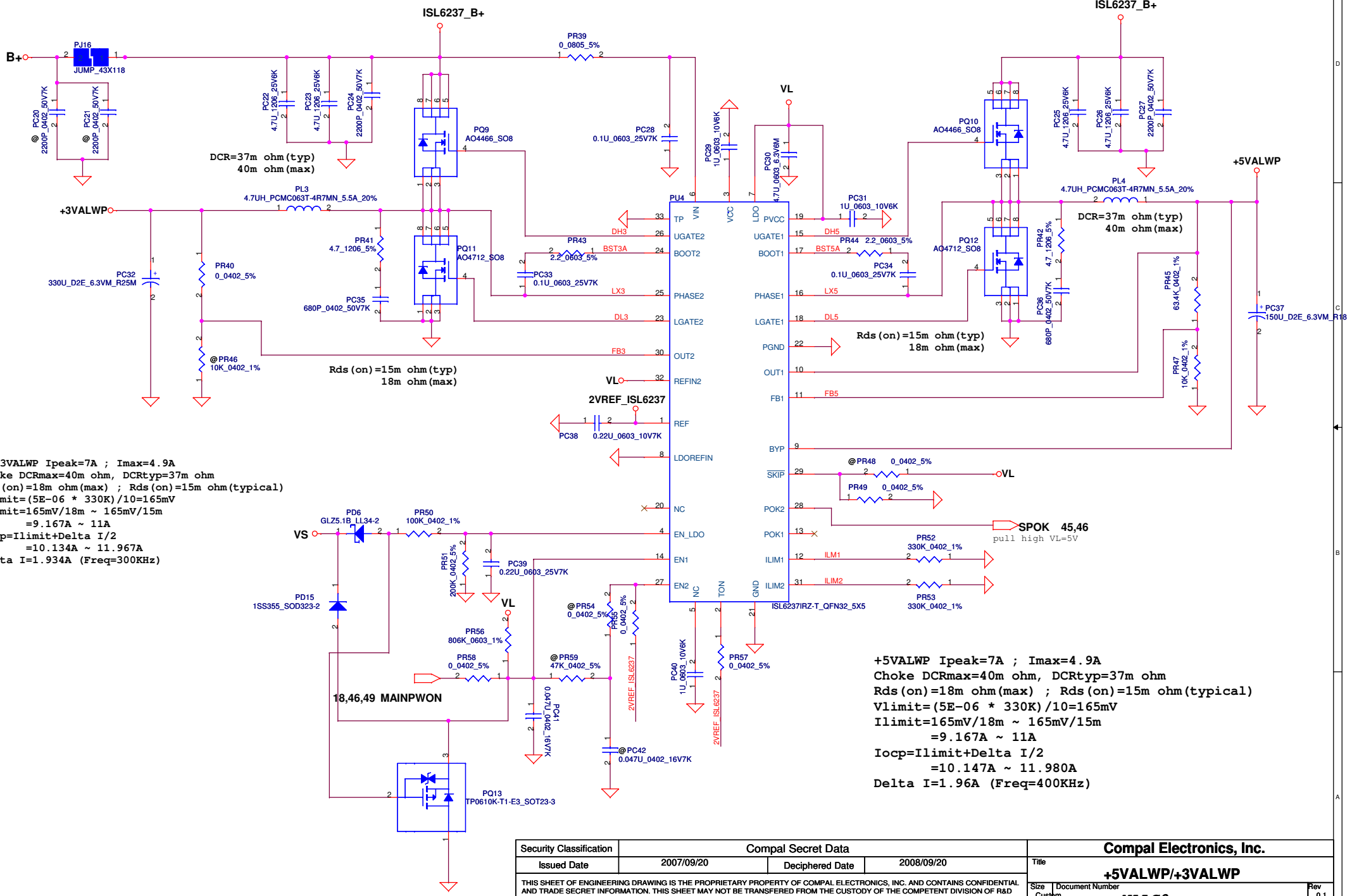
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
Custom	NALG0	0.1

Date: Friday, October 23, 2009 | Sheet 46 of 60



Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: **+5VALWP/+3VALWP**

Size	Document Number	Rev
Custom	NALG0	0.1

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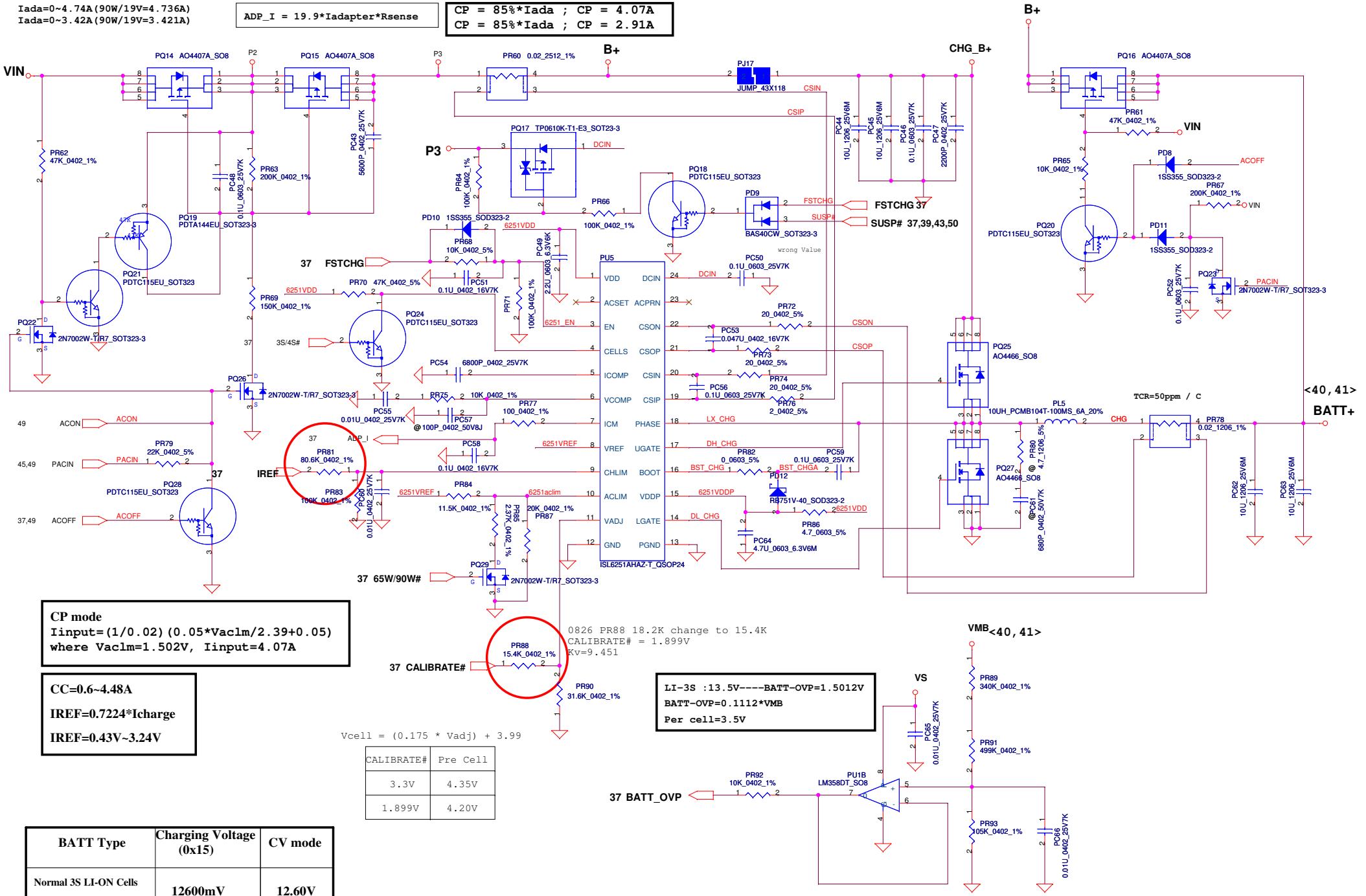
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

0826 PR88 18.2K change to 15.4K
CALIBRATE# = 1.899V
Kv=9.451

Vcell = (0.175 * Vadj) + 3.99

CALIBRATE#	Pre Cell
3.3V	4.35V
1.899V	4.20V

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: NALG0 | Rev: 0.1

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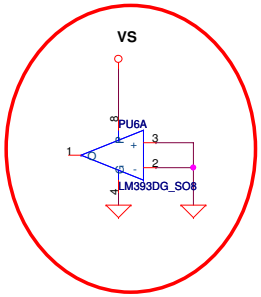

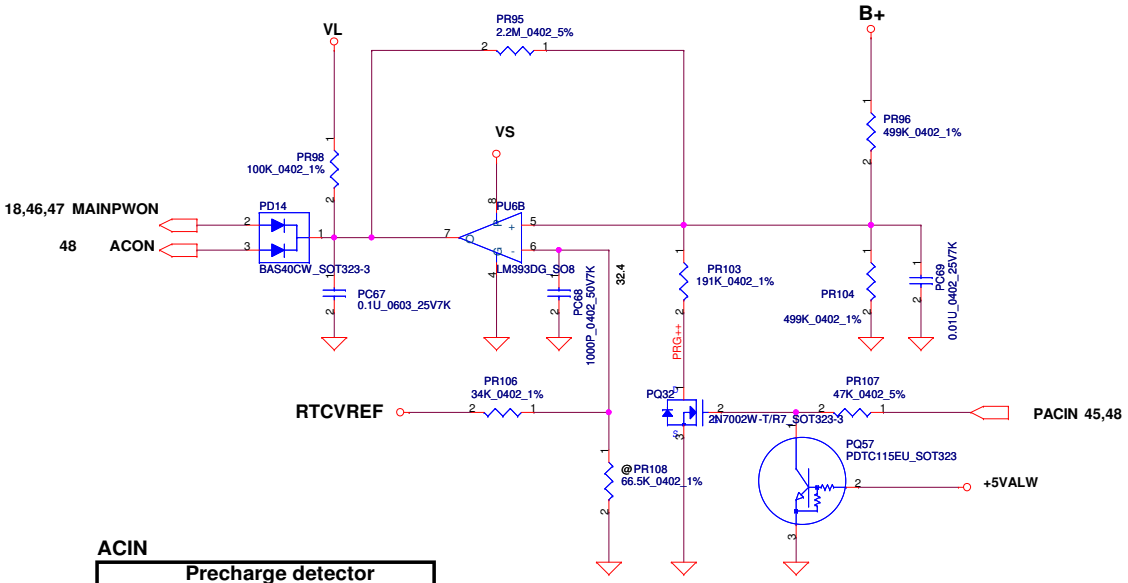

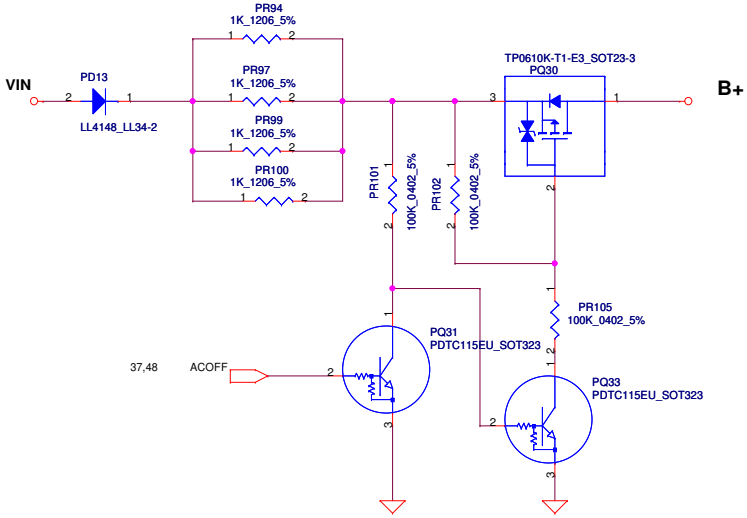

ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.			
Title: PRECHARGE			
Size: Custom	Document Number: NALG0		Rev: 0.1
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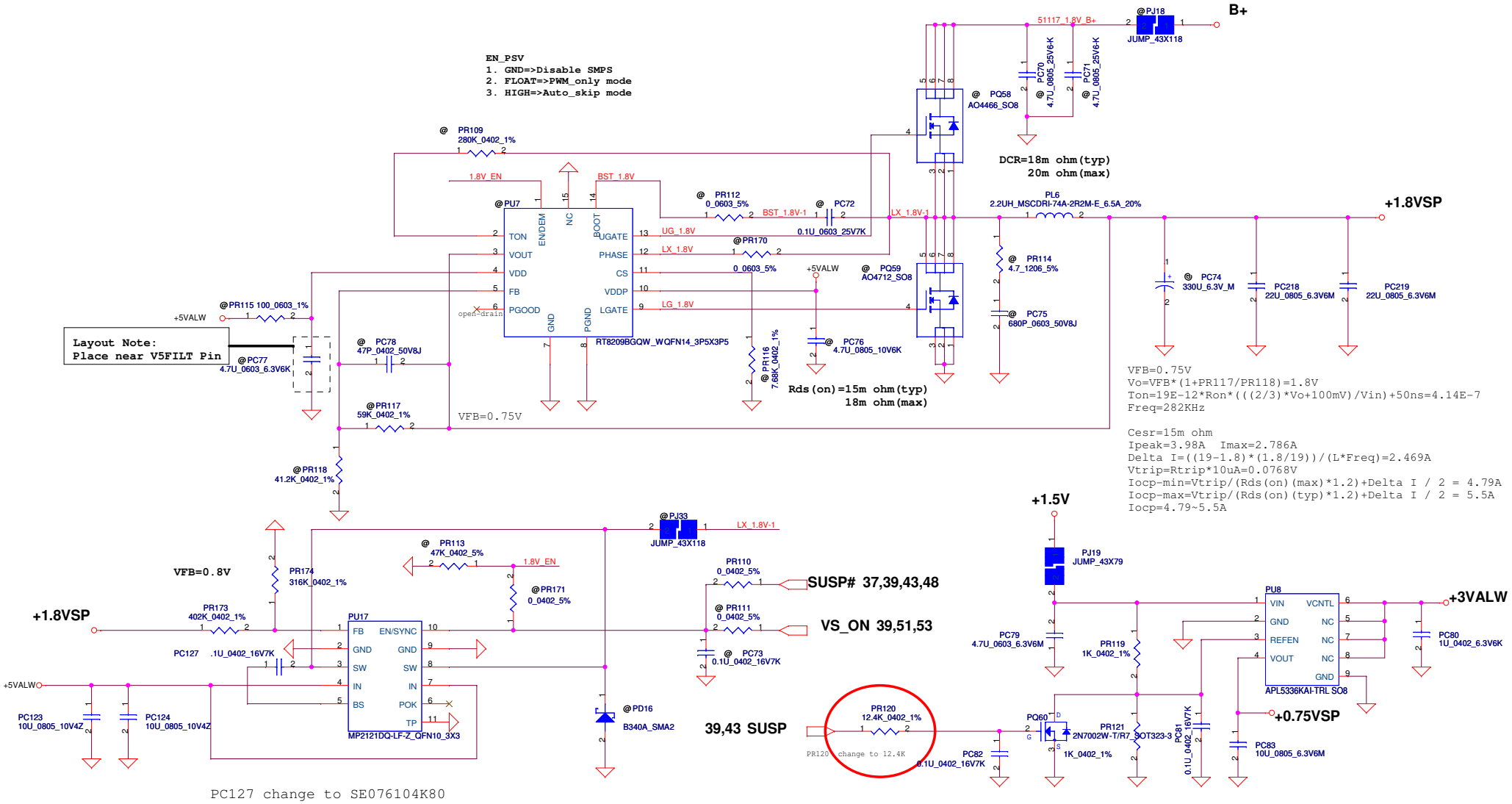

PC127 change to SE076104K80

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

Compal Electronics, Inc.			
Title	+1.8VSP/+0.75VSP		
Size: Custom	Document Number: NALG0		Rev: 0.1
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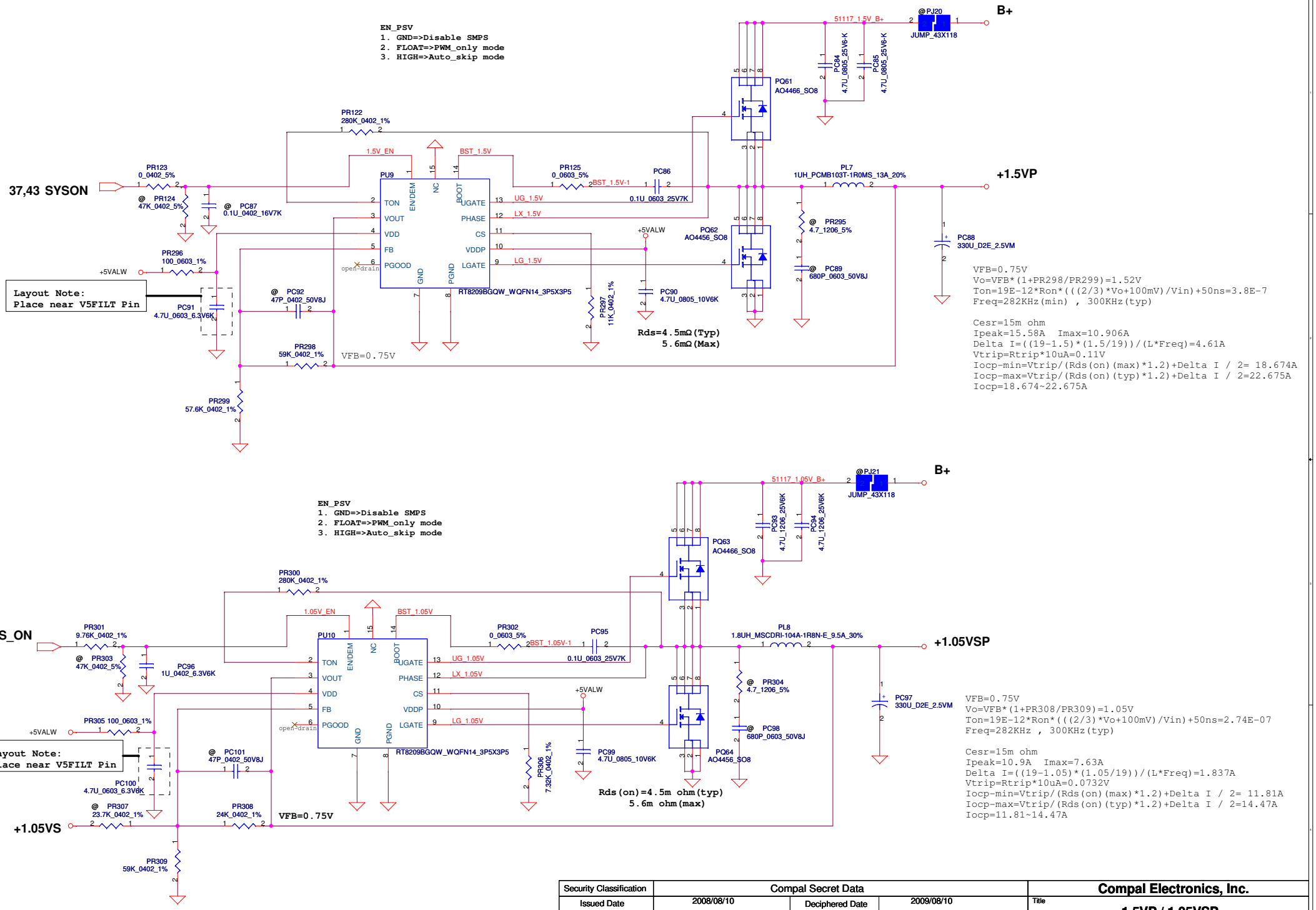

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

Compal Electronics, Inc.

Title: **1.5VP / 1.05VSP**

Size	Document Number	Rev
Custom	NALG0	0.1

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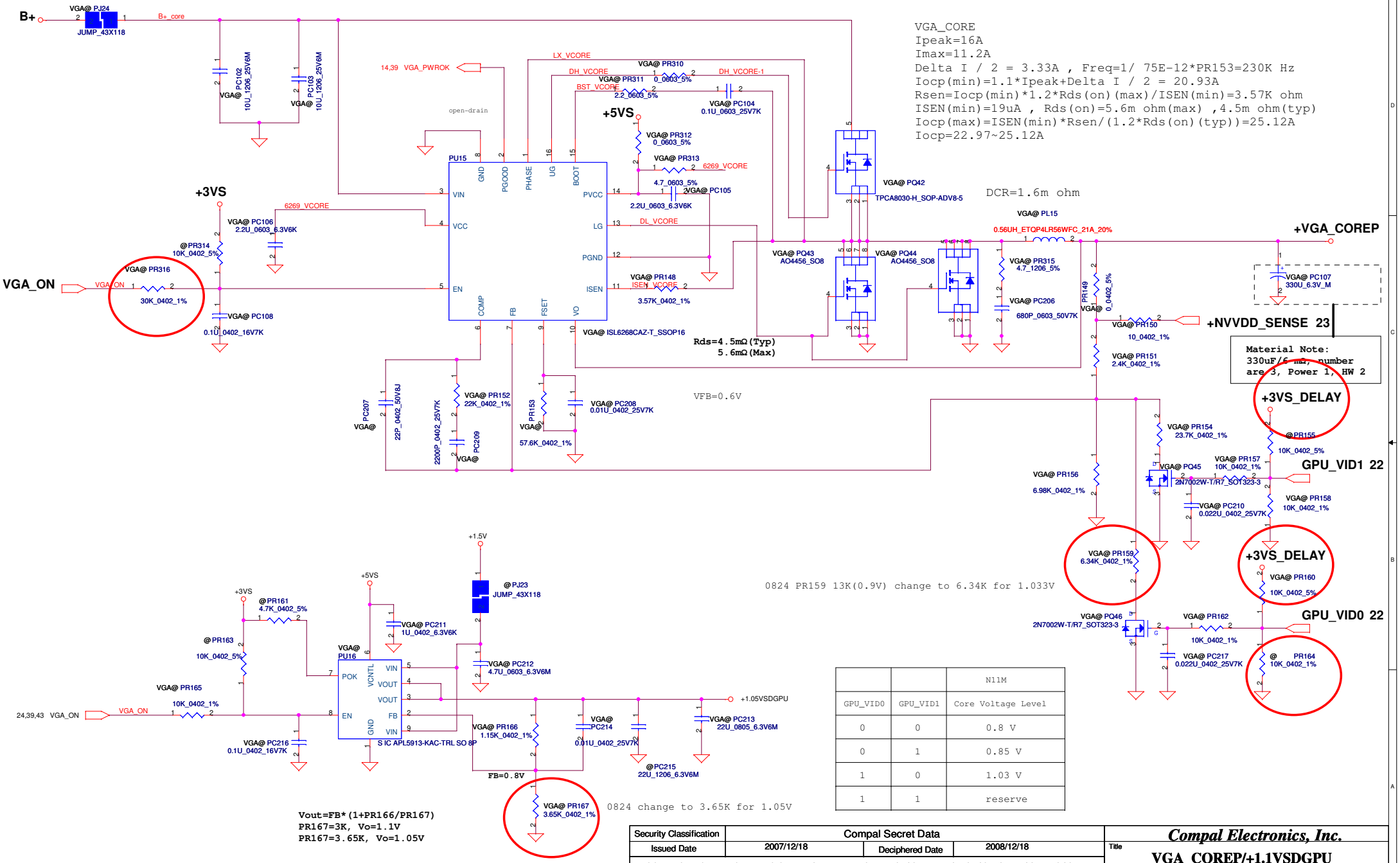


VGA_CORE
Ipeak=16A
Imax=11.2A
Delta I / 2 = 3.33A , Freq=1/ 75E-12*PR153=230K Hz
Iocp(min)=1.1*Ipeak+Delta I / 2 = 20.93A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=3.57K ohm
ISEN(min)=19uA , Rds(on)=5.6m ohm(max) ,4.5m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=25.12A
Iocp=22.97~25.12A

DCR=1.6m ohm

Material Note:
330uF/6 m2, number are 3, Power 1, HW 2

0824 PR159 13K(0.9V) change to 6.34K for 1.033V

		N11M
GPU_VID0	GPU_VID1	Core Voltage Level
0	0	0.8 V
0	1	0.85 V
1	0	1.03 V
1	1	reserve

Vout=FB*(1+PR166/PR167)
PR167=3K, Vo=1.1V
PR167=3.65K, Vo=1.05V

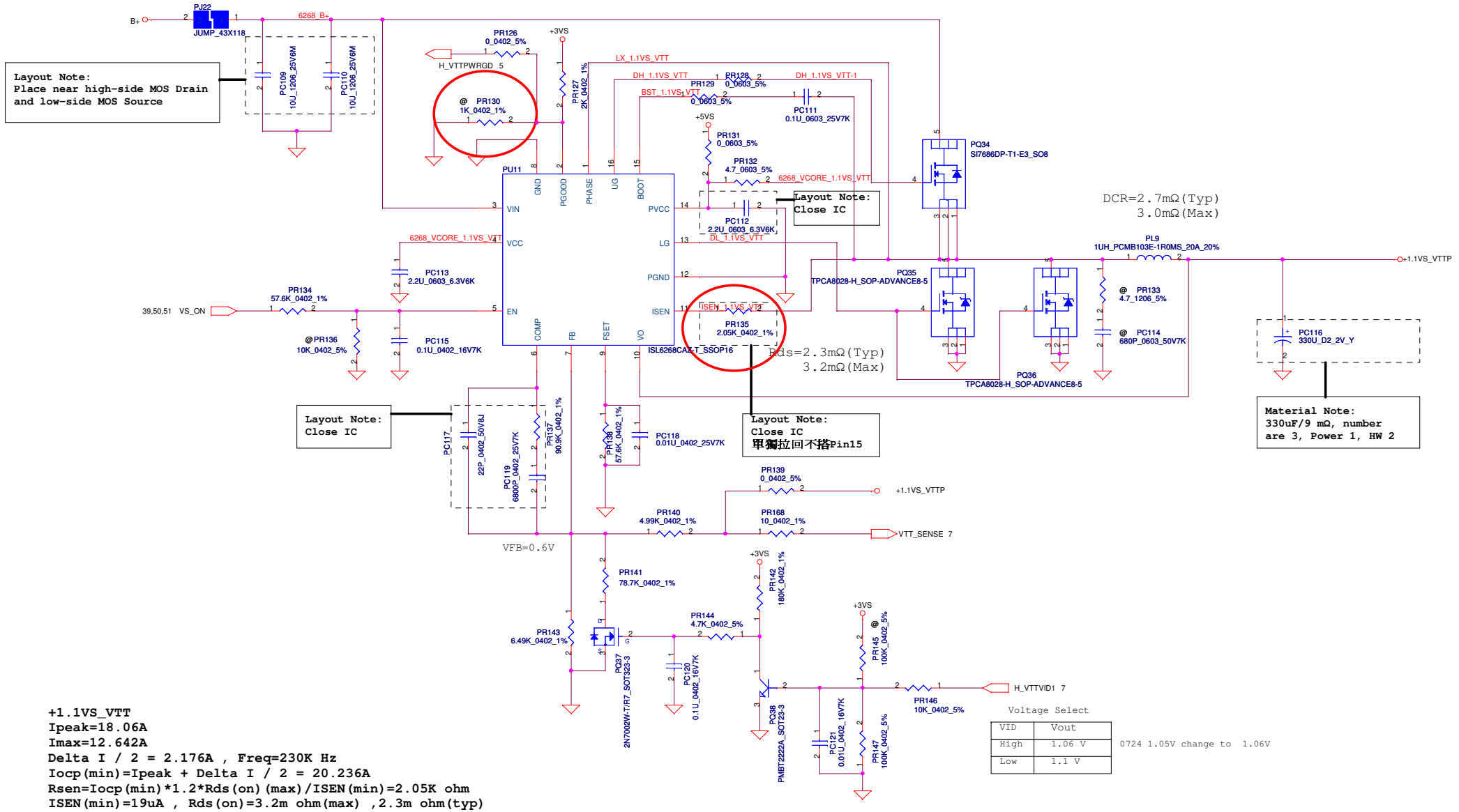
0824 change to 3.65K for 1.05V

Security Classification	Compal Secret Data		
Issued Date	2007/12/18	Deciphered Date	2008/12/18

Compal Electronics, Inc.

Title: VGA_COREP/+1.1VSDGPU

Size: Custom	Document Number: NALG0	Rev: 0.1
Date: Friday, October 23, 2009	Sheet 52 of 60	



+1.1VS_VTT
Ipeak=18.06A
Imax=12.642A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=Ipeak + Delta I / 2 = 20.236A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=2.05K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) ,2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=28.225A
Iocp=20.236~28.225A

Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: +1.1VS_VTTP

Size: Custom	Document Number: NALG0	Rev: 0.1
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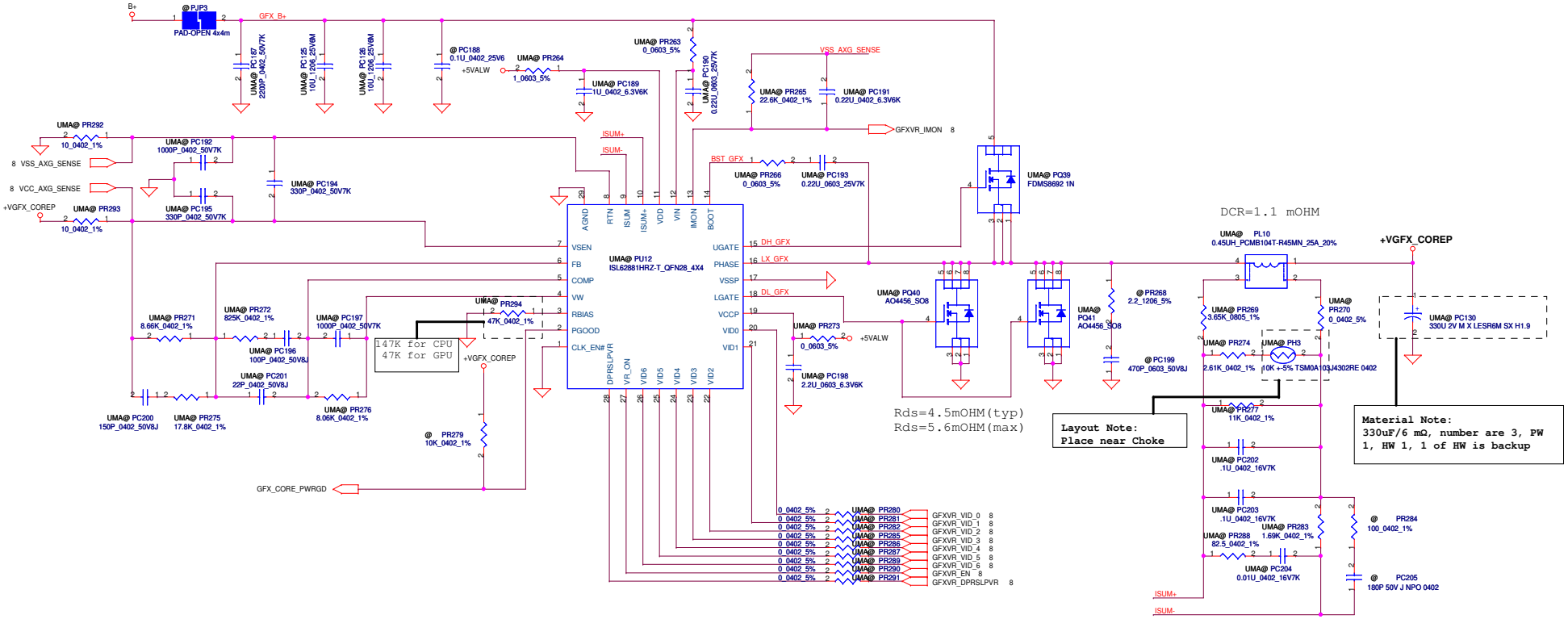
Intel Auburndale CPU(Integrate Graphics) Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: GFX_COREP

Size	Document Number	Rev
C	NALG0	0.1

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Intel Auburndale CPU(Integrate Graphics) , Ipeak = 48A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum/2)=0.763
where Rn=PR258 // (PR251+PH6)=5.875k ohm
Rsum=PR221, PR253 =3.65k ohm
LL = 2*Rdroop*G1*(DCR/2)/Ri = 1.81mV/A
where Rdroop=PR239=2.61k ohm , Ri=PR256=1.21k ohm
Iocp= OCP Threshold*Rdroop/LL=40E-06*2.61E03/1.81E-03=57.68A

Layout Note:
PH5 place near Phase1 L-MOS

Layout Note:
Place near Phase1 Choke

Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: +CPU_CORE

Size	Document Number	Rev
C	NALG0	0.1

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify chager circuit	design change	0.1	48	Change PR60 to SD000001F00(0.02_2512_1%) Cahnge PR115 to SD014100080 (S RES 1/10W 100 +-1% 0603)	09/06/23	EVT
2	Modify 1.8V V5FILT PIN	Avoid 2'nd source RT8209B can no power on	0.1	50	Cahnge PC77 to SE107475K80 (S CER CAP 4.7U 6.3V K X5R 0603)	09/07/21	DVT
3	Modify 1.5V V5FILT PIN	Avoid 2'nd source RT8209B can no power on	0.1	51	Cahnge PR296 to SD014100080 (S RES 1/10W 100 +-1% 0603) Cahnge PC91 to SE107475K80 (S CER CAP 4.7U 6.3V K X5R 0603)	09/07/21	DVT
4	Modify 1.05V V5FILT PIN	Avoid 2'nd source RT8209B can no power on	0.1	51	Cahnge PR305 to SD014100080 (S RES 1/10W 100 +-1% 0603) Cahnge PC100 to SE107475K80 (S CER CAP 4.7U 6.3V K X5R 0603)	09/07/21	DVT
5	Modify VGA_COREP circuit	design change	0.1	52	Cahnge PR149 to SD028000080 (S RES 1/16W 0 +-5% 0402) Cahnge PR150 to SD034100A80 (S RES 1/16W 10 +-1% 0402)	09/06/23	EVT
6	Modify +1.1VS_VTTP circuit	design change	0.1	53	Cahnge PR139 to SD028000080 (S RES 1/16W 0 +-5% 0402) Cahnge PR168 to SD034100A80 (S RES 1/16W 10 +-1% 0402)	09/06/23	EVT
7	Modify OTP circuit	Link right component	0.1	46	Add PH1 to SL210031F00 (S THERM_ 100K +-1% TH11-4H104FT 0603)	09/06/25	EVT
8	Modify 5V/3V circuit	Delete component	0.1	47	Delete PC42 to SE076473K80 (S CER CAP .047U 16V K X7R 0402)	09/06/25	EVT
9	Modify 1.1VSDGPU circuit	design change	0.1	52	Change PU16, PR165, PR166, PR167, PC211, PC212, PC213, PC214, PC215, PC216 BOM structure to VGA@	09/06/26	EVT
10	Modify chager circuit	design change	0.1	48	Change PR78 to SD012200D80(S RES 1/2W 0.02 +-1% 1206)	09/06/26	EVT
11	Modify VGA_COREP circuit	design change(Voltage Level)	0.1	52	Cahnge PR151 to SD034240180 (S RES 1/16W 2.4K +-1% 0402) Cahnge PR156 to SD000002680 (S RES 1/16W 6.98K +-1% 0402)	09/06/30	EVT
12	Modify VGA_COREP circuit	design change(Voltage Level)	0.1	52	Cahnge PR154 to SD034237280 (S RES 1/16W 23.7K +-1% 0402) Cahnge PR159 to SD034130280 (S RES 1/16W 13K +-1% 0402)	09/06/30	EVT
13	Modify OTP circuit	design change	0.2	46	Cahnge PQ6 to SB000006800 (S TR 2N7002W T/R7 1N SOT-323) Add PR169 to SD034100480 (S RES 1/16W 1M +-1% 0402)	09/07/13	DVT
14	Modify 1.5VP circuit	design change	0.2	51	Change PL7 to SH000009U00(S COIL 1UH +-20% FDUE1040D-1R0M=P3 21.3A)	09/07/20	DVT
15	Modify VGA_COREP circuit	design change	0.2	52	Cahnge PR153 to SD034576280 (S RES 1/16W 57.6K +-1% 0402)	09/07/20	DVT
16	Modify +1.1VS_VTTP circuit	design change	0.2	53	Cahnge PQ35 to SB00006L00 (S TR TPCA8028-H 1N SOP ADVANCE) Cahnge PQ36 to SB00006L00 (S TR TPCA8028-H 1N SOP ADVANCE)	09/07/20	DVT
17	Modify VGA_COREP circuit	design change	0.2	52	Cahnge PC107 to SF000002000 (S ELE CAP 330U 6.3V M 6.3X5.9 LESR15M VU)	09/07/20	DVT
18	Modify 1.8V circuit	design change	0.2	50	Cahnge PC74 to SF000002000 (S ELE CAP 330U 6.3V M 6.3X5.9 LESR15M VU) and BOM structure to @	09/07/20	DVT
19	Modify CPU circuit	design change	0.2	55	Cahnge PR226 to SD00009O80 (S RES 1/16W 1.91K +-1% 0402)	09/07/20	DVT
20	Modify +1.1VS_VTTP circuit	design change	0.2	53	Cahnge PC116 to SGA20331E10 (S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	09/07/21	DVT
21	Modify CPU circuit	design change	0.2	55	Cahnge PC179 to SE026683K80 (S CER CAP .068U 16V K X7R 0603)	09/07/22	DVT
22	Modify chager circuit	design change	0.2	48	Cahnge PC53 to SE076473K80 (S CER CAP .047U 16V K X7R 0402) Cahnge PC64 to SE107475M80 (S CER CAP 4.7U 6.3V M X5R 0603 H0.8)	09/07/22	DVT
23	Modify 1.1VSDGPU circuit	design change	0.2	52	Cahnge PC212 to SE107475M80 (S CER CAP 4.7U 6.3V M X5R 0603 H0.8)	09/07/22	DVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Modify GFX_COREP circuit	design change	0.2	54	Cahnge PC189 to SE000000K80 (S CER CAP 1U 6.3V K X5R 0402)	09/07/22	DVT
25	Modify 1.8V circuit	design change	0.2	50	Add PR170 to SD013000080 (S RES 1/10W 0 +-5% 0603)and BOM structure to @ Change PR109, PR117, PC72, PQ58, PQ59 BOM structure to @	09/07/28	DVT
26	Modify 1.8V circuit	design change	0.2	50	Add PU17 to SA00003KL00(S IC MP2121DQ-LF-Z QFN 10P PWM) Add PD16 to SCS00001I80(S SCH DIO B340A SMA VISHAY) BOM structure to @ ~~Add PR173 to SD034402380(S RES 1/16W 402K +-1% 0402)~~	09/07/28	DVT
27	Modify 1.8V circuit	design change	0.2	50	Add PR174 to SD034316380(S RES 1/16W 316K +-1% 0402) Add PR171 to SD028000080(S RES 1/16W 0 +-5% 0402)BOM structure to @	09/07/28	DVT
28	Modify 1.8V circuit	design change	0.2	50	~~Add PR113 to SD028470280(S RES 1/16W 47K +-5% 0402)~~ Add PC123,PC124 to SE053106Z80(S CER CAP 10U 10V Z Y5V 0805) Add PC127 to SE076103K80(S CER CAP .01U 16V K X7R 0402)	09/07/28	DVT
29	Modify 1.8V circuit	design change	0.2	50	Add PC218, PC219 to SE000000I10(S CER CAP 22UF 6.3V M X5R 0805 H1.25) ~~Add PR41, PR42 to SD001470B80(S RES 1/4W 4.7 +-5% 1206)~~	09/07/28	DVT
30	Modify 5V/3V circuit	add snubber(PR42 PC36),(PR41 PC35) add boost PR43, PR44	0.2	47	Add PC35, PC36 to SE074681K80(S CER CAP 680P 50V K X7R 0402) Add PR43, PR44 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	09/07/28	DVT
31	Modify VGA_COREP circuit	add snubber(PR315 PC206) add boost PR311	0.2	52	Add PR311 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)and BOM structure to VGA@ Change PR315 PC206 BOM structure to VGA@	09/07/28	DVT
32	Modify CPU circuit	add snubber(PR220 PC158),(PR252 PC184) add boost PR217, PR249	0.2	55	Add PR220, PR252 to SD011220B80(S RES 1/4W 2.2 +-5% 1206) Add PC158, PC184 to SE074681K80(S CER CAP 680P 50V K X7R 0402) ~~Add PR217, PR249 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)~~	09/07/28	DVT
33	Modify +1.1VS_VTTP circuit	design change	0.2	53	Cahnge PR141 to SD034787280(S RES 1/16W 78.7K +-1% 0402) Cahnge PR143 to SD034649180(S RES 1/16W 6.49K +-1% 0402)	09/07/28	DVT
34	Modify OTP circuit	design change	0.2	46	Cahnge PH1 to SL200000U00(S THERM_ 100K +-1% TSM0B104F4251RZ 0402) Cahnge PH2 to SL200000U00(S THERM_ 100K +-1% TSM0B104F4251RZ 0402)	09/07/28	DVT
35	Modify +1.1VS_VTTP circuit	design change(OCP)	0.2	53	Cahnge PR135 to SD034280180(S RES 1/16W 2.8K +-1% 0402)	09/07/29	DVT
36	Modify GFX_COREP circuit	design change	0.2	54	Cahnge PH3 to SL200000Y00(10K +-5% TSM0A103J4302RE 0402)	09/07/29	DVT
37	Modify CPU circuit	design change	0.2	55	Cahnge PH6 to SL200000W00(10K +-1% TSM0A103F34D1RZ 0402)	09/07/29	DVT
38	Modify 1.5V circuit	Change to 3mm height choke for thermal issue	0.2	51	Cahnge PL7 to SH00000AB00(S COIL 1UH +-20% PCMB103T-1R0MS 13A)	09/08/06	DVT
39	Modify VGA_COREP circuit	design change (GS sample define 1.03V,+1.05VSDGPU Vo=1.05V)	0.3	52	Cahnge PR159 to SD034634180(S RES 1/16W 6.34K +-1% 0402) Cahnge PR167 to SD034365180(S RES 1/16W 3.65K +-1% 0402)	09/08/24	PVT
40	Modify 1.8V circuit	design change	0.3	50	Cahnge PC127 to SE076104K80(S CER CAP .1U 16V K X7R 0402)	09/08/24	PVT
41	Modify chager circuit	design change	0.3	48	Cahnge PR88 to SD034154280(S RES 1/16W 15.4K +-1% 0402) Change PR81 to SD034154380(S RES 1/16W 154K +-1% 0402)	09/08/26	PVT
42	Modify VGA_COREP circuit	design change	0.3	52	Change PR160 BOM structure to VGA@ VID pull high voltage change to +3VS_DELAY	09/09/03	PVT
43	Modify +1.1VS_VTTP circuit	design change	0.3	53	Change PR130 BOM structure to @	09/09/03	PVT
44	Modify 0.75V circuit	design change	0.3	50	Cahnge PR120 to SD034280180(S RES 1/16W 2.8K +-1% 0402)	09/09/11	PVT
45	Modify VGA_COREP circuit	design change	0.3	52	Cahnge PR316 to SD034300280(S RES 1/16W 30K +-1% 0402) Change PR164 BOM structure to @	09/09/11	PVT
46	Modify +1.1VS_VTTP circuit	design change	0.3	53	Cahnge PR135 to SD034205180(S RES 1/16W 2.05K +-1% 0402)		

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Title: PIR (PWR)			
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
47	Modify OTP circuit	design change	0.3	46	Change PR23 to SD00000AJ80(S RES 1/16W 12.4K +-1% 0402) Change PR26 to SD034158280(S RES 1/16W 15.8K +-1% 0402)	09/09/14	PVT
48	Modify 1.8V circuit	design change	0.3	50	Change PL6 to SH000009Q00(S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A)	09/09/16	PVT
49	Modify 5V/3V circuit	design change	0.3	47	Change PU4 to SA00001TN00(S IC ISL6237IRZ-T QFN 32P)	09/09/16	PVT
50	Modify 0.75V circuit	design change	0.3	50	Change PR120 to SD00000AJ80(S RES 1/16W 12.4K +-1% 0402)	09/10/08	PVT
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Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number | Rev: 0.1

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1				4	R72 bom structure	7/23	0.2
2				5	reserve R735	7/23	0.2
3				8	rename CPU VDDQ from +1.5V to +1.5V_CPU	7/23	0.2
4				8	R146 BOM structure	7/23	0.2
5				11	reserve S3 power consumptiosn circuit	7/23	0.2
6				12	change Y1 Y4 Y6 footprint	7/23	0.2
7				13	add ME_EN# from EC to PCH	7/23	0.2
8				14	pop Y6,C254,C255 , and project ID pin	7/23	0.2
9				17	change USB port 8 to port 1 , port 2 to port 8	7/23	0.2
10				18	GPIO35 pin(VGa presetnt) modfiy	7/23	0.2
11				19	R605 and R628 BOM structure modify	7/23	0.2
12				22	add VGA thermal sensor from EC to VGA	7/23	0.2
13				23	pop R479,del R491	7/23	0.2
14				29	L29~L34 change from 0805 to 0603	7/23	0.2
15				30	Q45,Q47 gate voltage change from +3VS to +3VS_delay	7/23	0.2
16				37	change R306 to 8.2K, add D29, rename EC_MUTE	7/23	0.2
17				38	Jfun1 pin3 change form KSO1 to KSO3	7/23	0.2
18				39	del SW2	7/23	0.2
19				41	change R333, R336 to 39k,15k, add R681,C707	7/23	0.2
20				43	reserve Q58,Q59,R728,R326, change U26,R688	7/23	0.2
21				24	reserve C710	7/23	0.2
22				28	reserve U44,U45	7/23	0.2
23				19	update L7,L8,L10,L11 footprint	7/23	0.2

Compal Electronics, Inc.
Title: PIR (HW)
Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 0.2
Date: Friday, October 23, 2009 | Sheet 59 of 60

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1				30	pop R248, R271,R265	7/23	0.2
2				7	pop C165, del C170	7/23	0.2
3				18	unpop R532, R86	7/23	0.2
4				5	add R472 and C713	8/31	0.3
5				11	add C714	8/31	0.3
6				12	add C715	8/31	0.3
7				17	USB20 port 6 change to USB20 port 9	8/31	0.3
8				24	3VS_delay related circuit	8/31	0.3
9				30	del R236,C257 , pop R254,C268 in all sku	8/31	0.3
10				33	unpop R3 , U1, pop R6 , change R306 to 18K	8/31	0.3
11				37	ME_EN change from U25,75 to U25.16	8/31	0.3
12				29	pop Q6,Q7 in all sku	8/31	0.3
13				29	change L29~L34 footprint	8/31	0.3
14				41	del D25,D26,D27	8/31	0.3
15				43	update C705,C706 BOM structure	8/31	0.3
16				14	unpop R112	8/31	0.3
17				7	change C165 p/n	8/31	0.3
18				40	pop C353	9/10	0.3
19					change R157,R527,R570,R575,R582,R634,R239,R64 to 0 ohm		0.3
20				5	add R746,R747	9/10	0.3
21				12	U27 clk gen change to siligo	9/10	0.3
22				40	del C371,C372	9/10	0.3
23				3	Modify BOM Config add S3@ on all SKU	10/20	1.0

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1				14	Change R209,C254,C255,Y6 BOM config to UMA@	10/20	1.0
2				19	Added C257	10/20	1.0
3				22	Change N11 to A2 (P/N SA00003HZ10)	10/20	1.0
4				22	Added R748 and R749 as I2C pull high resistor.	10/20	1.0
5				22	Pop R36,R37 as DIS@	10/20	1.0
6				28	Change Q11,Q19 BOM config to SG@	10/20	1.0
7				28	Change R502,R484 BOM config to DIS only@	10/20	1.0
8				37	Change R306 to 33k(Board ID)	10/20	1.0
9				38	Change LED9 PN to SC5191UD00	10/20	1.0
10				43	Change R296 to 47K,R295 to 470	10/20	1.0
11				44	Change LED Resistors:	10/20	1.0
12					R373 to 243,R381 and R383 to 100,R377 to 243,		
13					R375 and R376 to 470,R349 to 100,R350 to 191		
14					R304 to 499		1.0
15				17	Change C256 to 22u	10/22	
16				18	ADD R750 10K pull hig resistor	10/22	1.0
17							
18							
19							
20							
21							
22							
23							

Compal Electronics, Inc.
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