

Compal Confidential

KAL90/KALH0 M/B Schematics Document

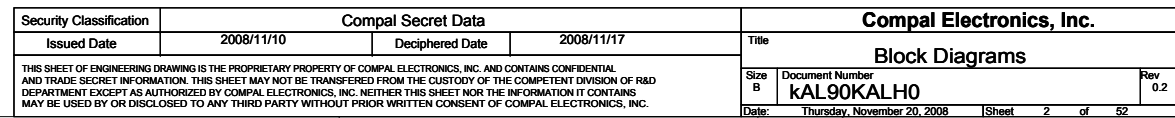
Intel Penryn Processor with Cantiga + DDRII + ICH9M

2008-12-17

REV:1.0

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Model Name : KAL90/KALH0



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Device	IDSEL#	REQ#/GNT#	Interrupts
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
MEDIA CONSOLE	1010 000X b	NB9M THERMAL SENSOR	

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
MEDIA CONSOLE	1010 000X b	NB9M THERMAL SENSOR	

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

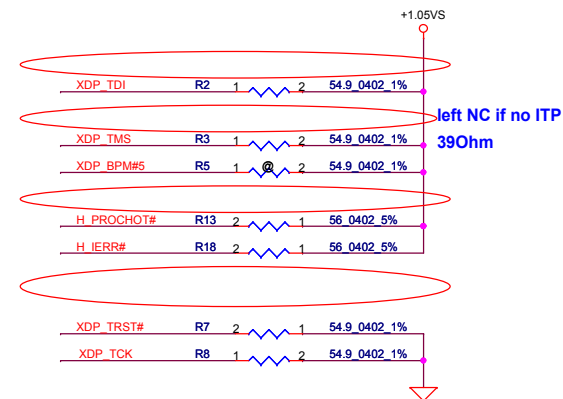
BTO Option Table

BTO Item	BOM Structure
KAL90	JAL90@
UMA	GM@
PM@	PM@
ALC888VC	888VC@
ALC888VB	888VB@
AR8121	8121@
AR8112	8112@
ALC268	268@
GL40	GL40@
GM45	GM45@

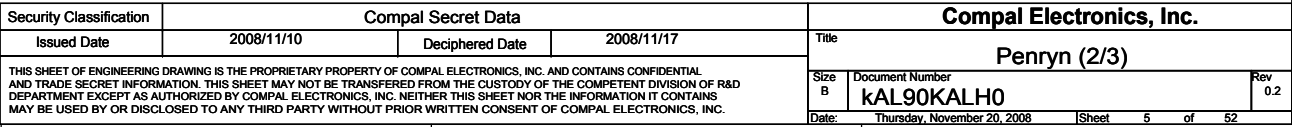
BOM Configuration Table

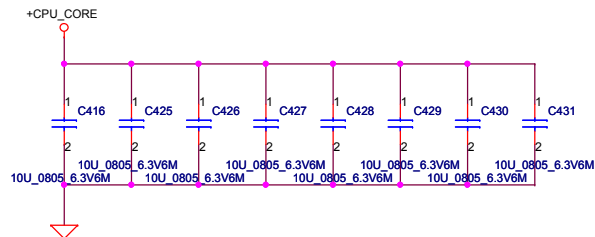
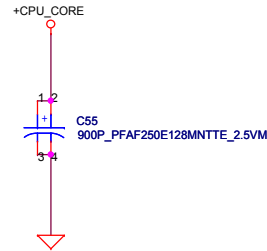
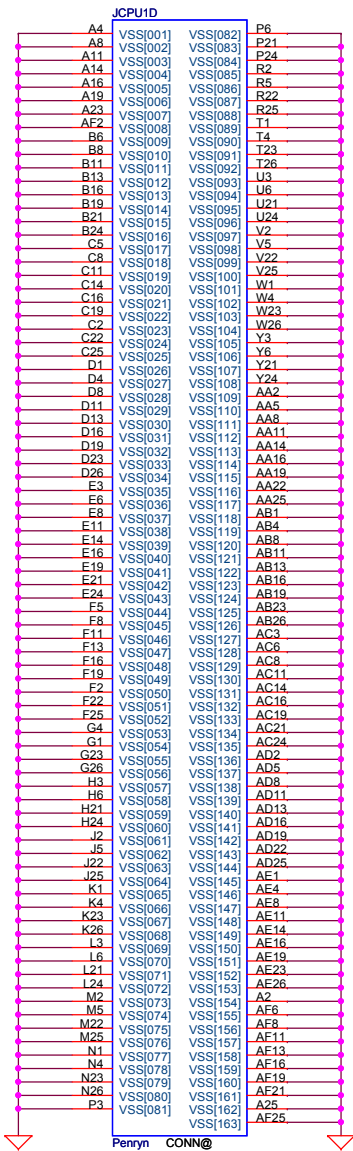
Project	BOM Configuration
KAL90-UMA	XXXXXXXXXX:KAL90@/GM@/888VC@/8121@/GM45@
KAL90-Dis	XXXXXXXXXX:KAL90@/PM@/888VC@/8121@
KAL90-GM45	XXXXXXXXXX:KALH0@/GM@/888VC@/8121@/GM45@
KAL90-GL40	XXXXXXXXXX:KALH0@/GM@/888VC@/8121@/GL40@
KAL90-PM45	XXXXXXXXXX:KALH0@/PM@/888VC@/8121@

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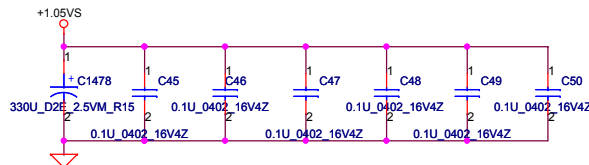


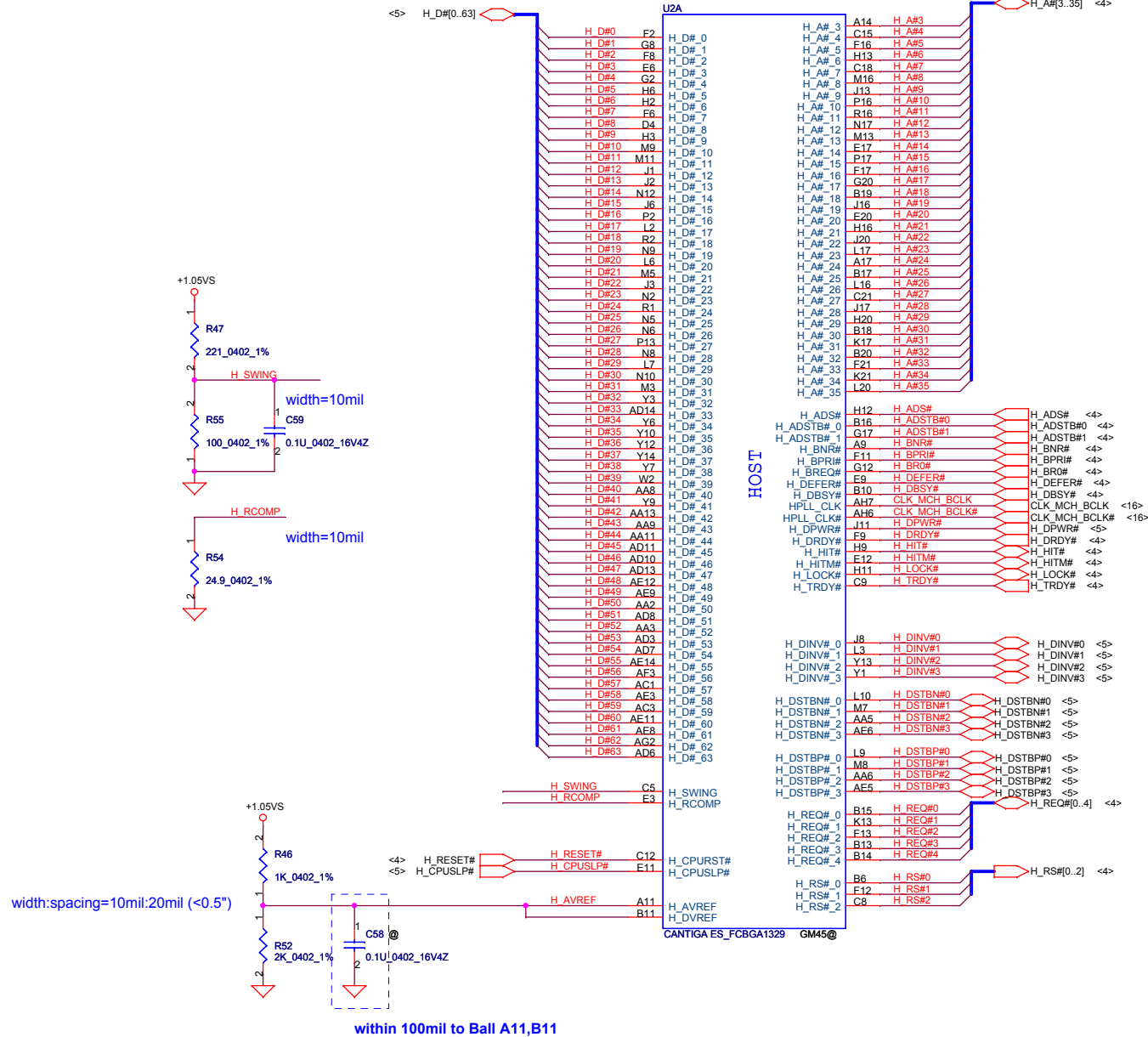
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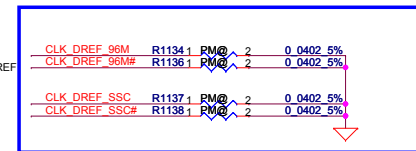
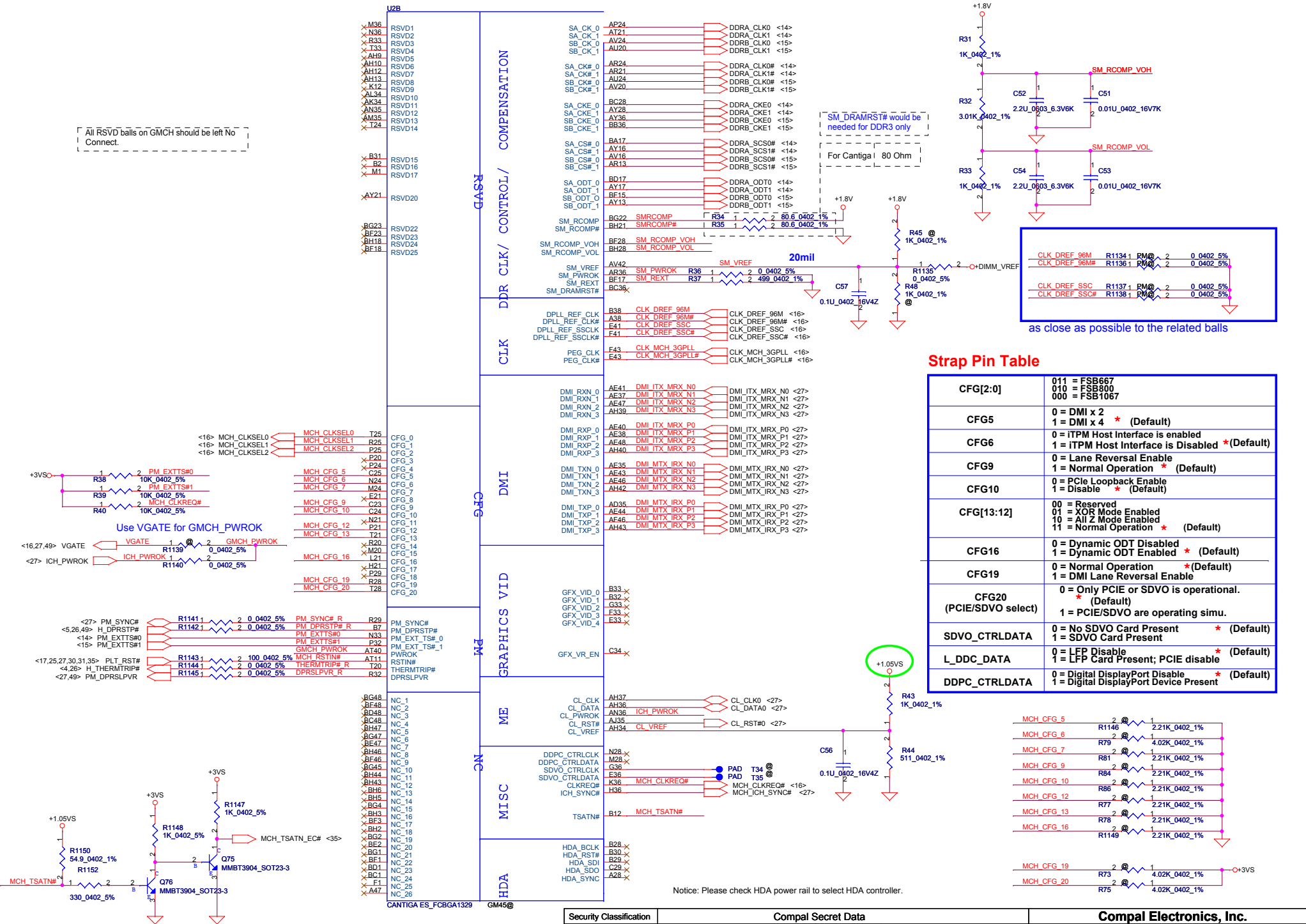
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32





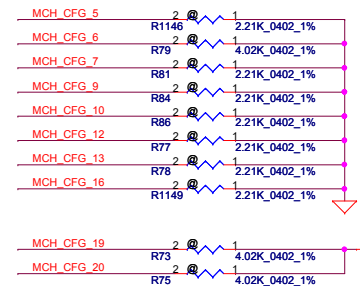
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All RSVD balls on GMCH should be left No Connect.



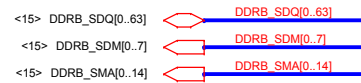
Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable 1 = LFP Card Present; PCIe disable * (Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable 1 = Digital DisplayPort Device Present * (Default)

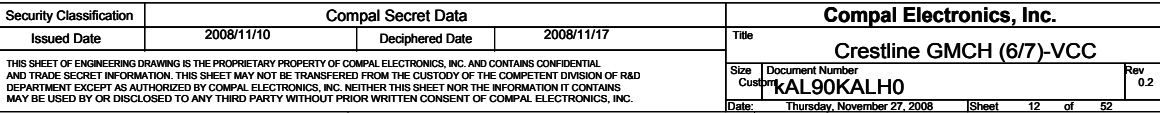


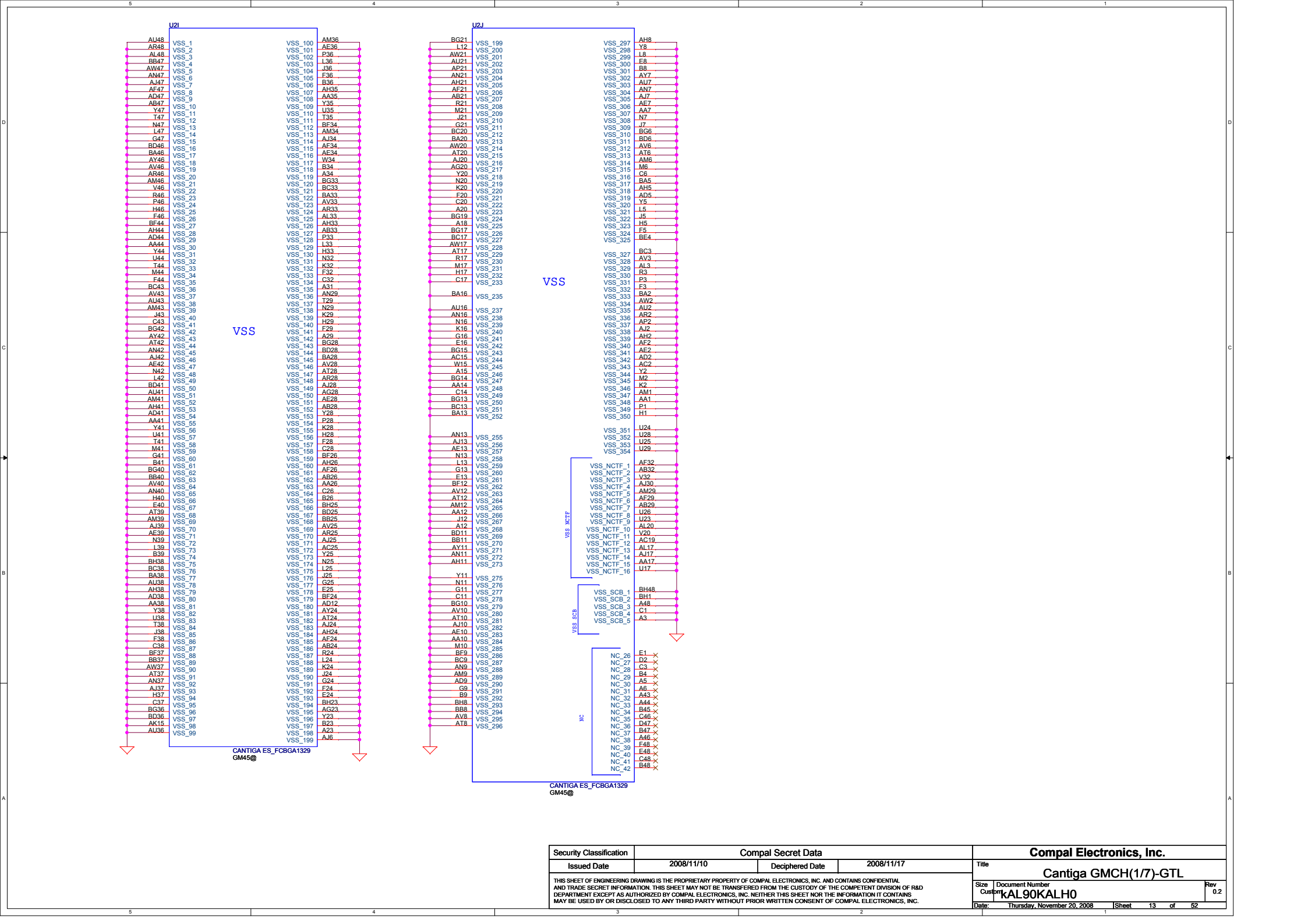
Notice: Please check HDA power rail to select HDA controller.

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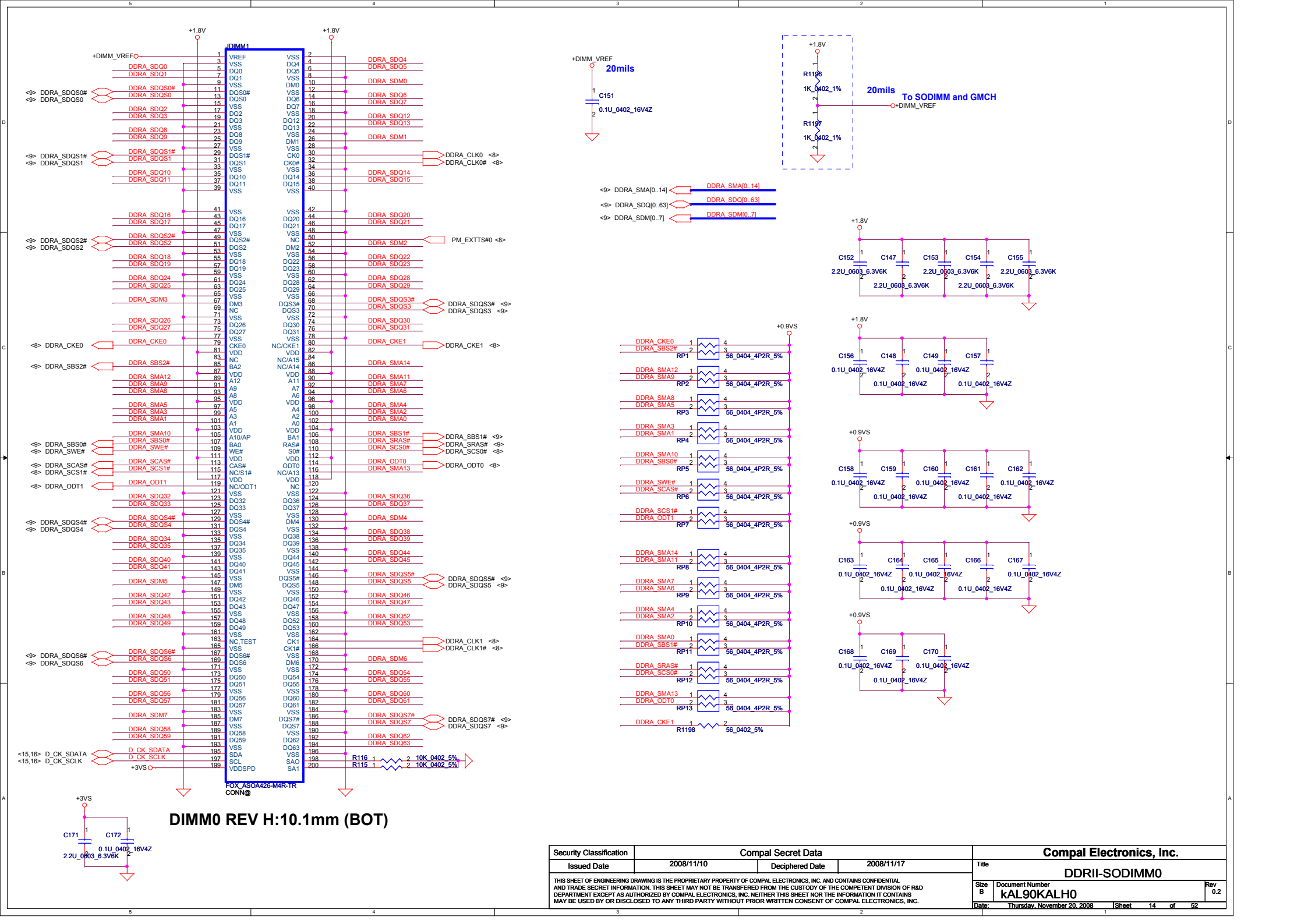


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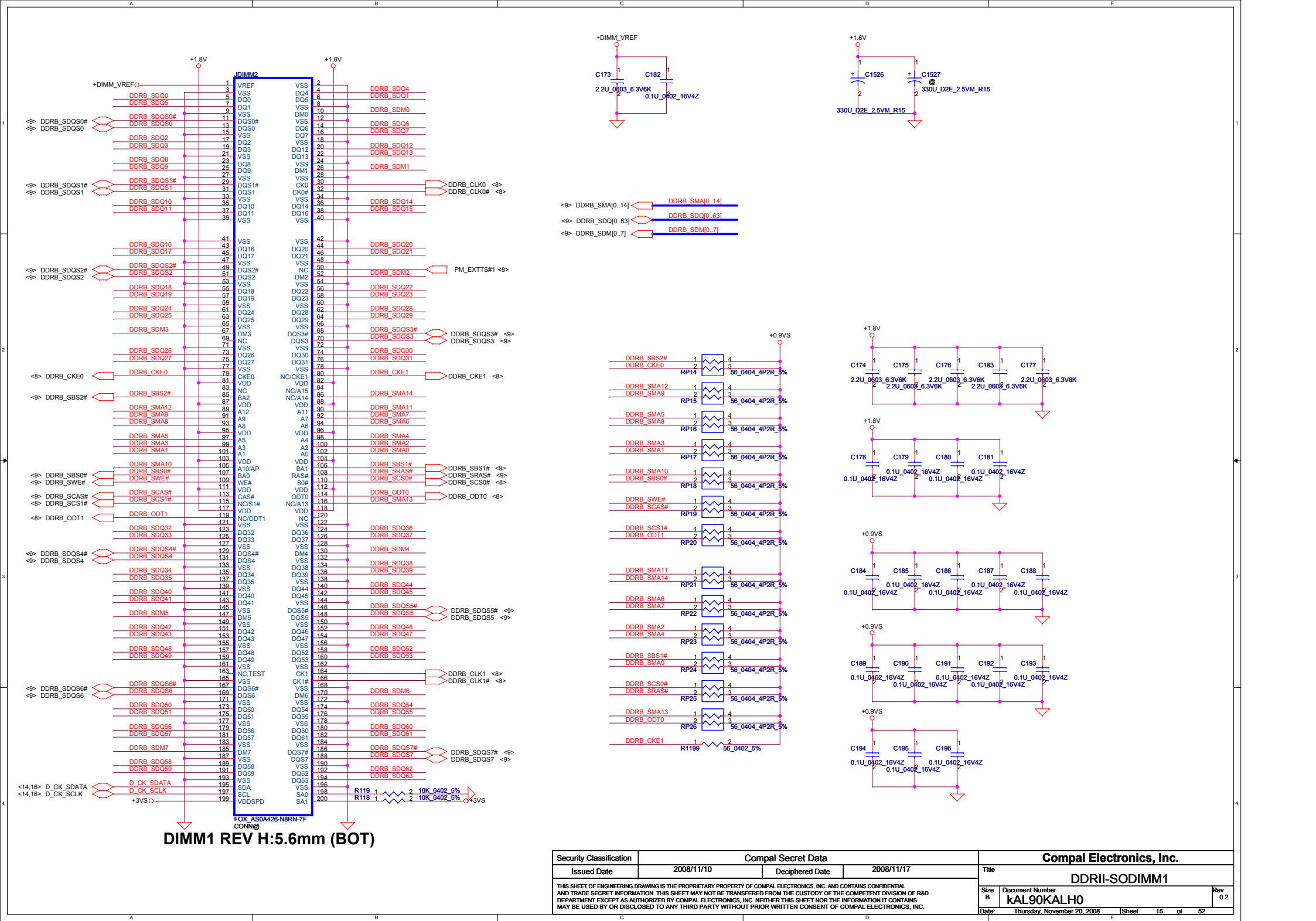




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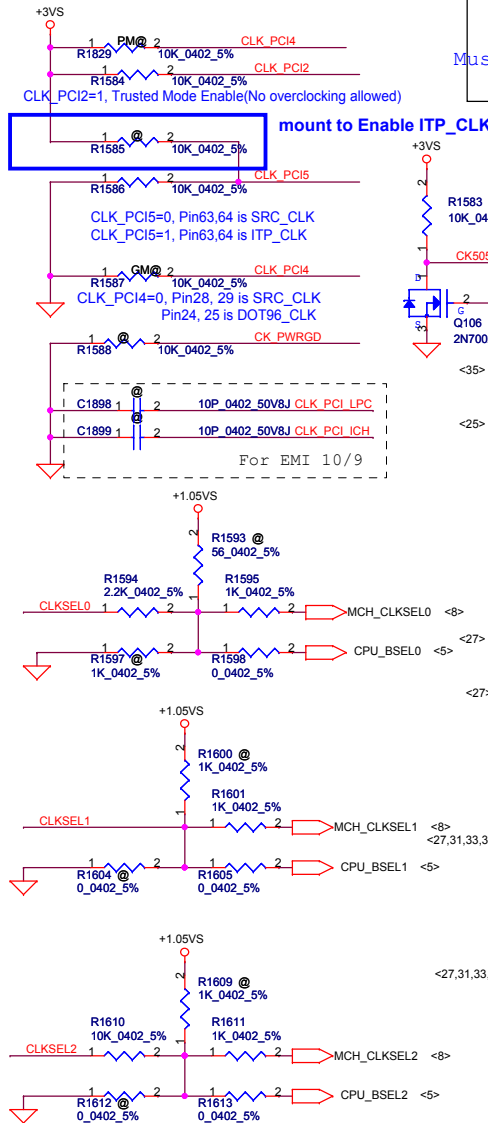
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				DDRII-SODIMM1	

FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRCT7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]



Must Close to CLKGEN PIN 28,29

mount to Enable ITP_CLK

CLK_PCIE4=0, Pin63,64 is SRC_CLK
CLK_PCIE5=1, Pin63,64 is ITP_CLK

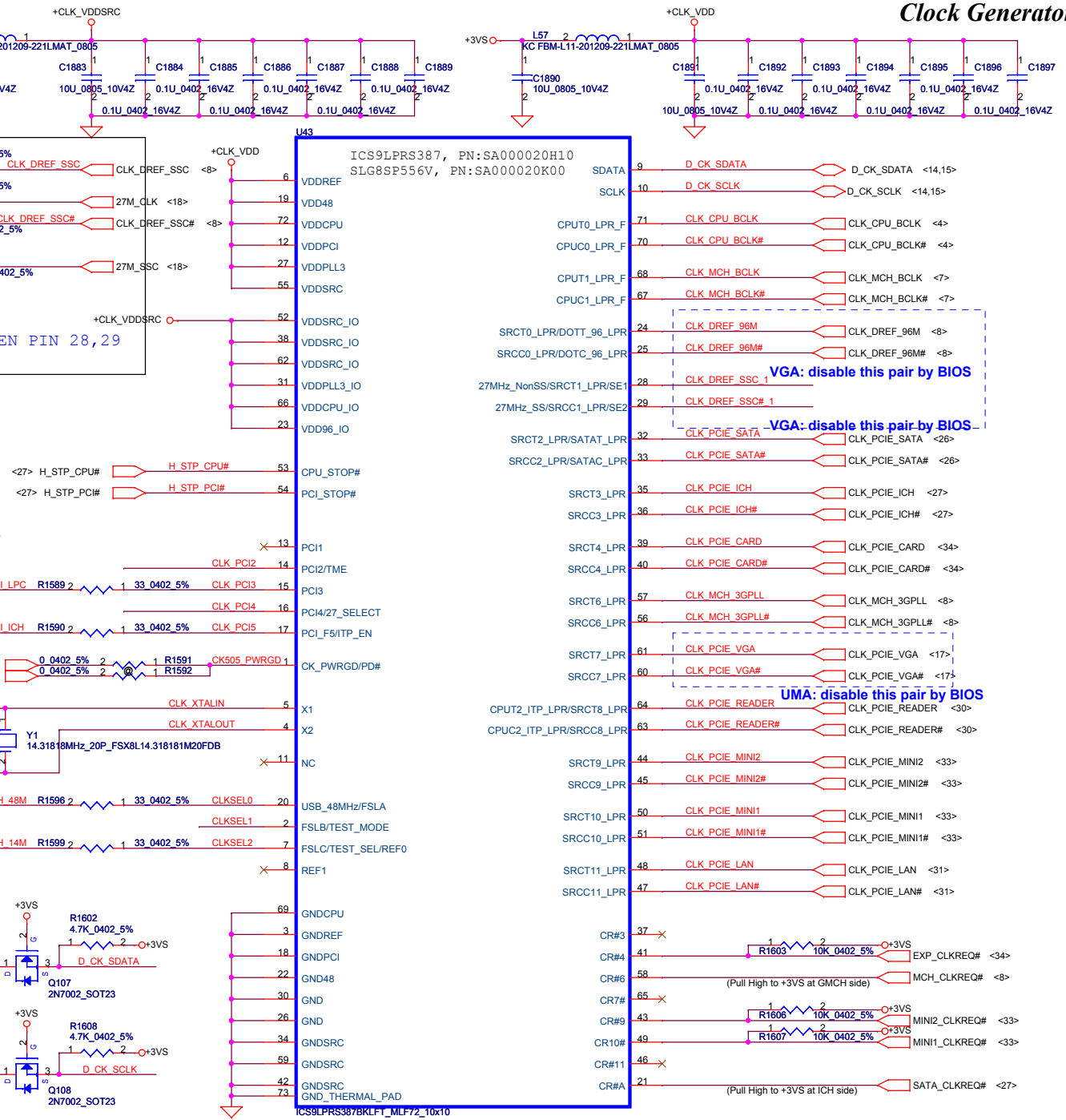
For EMI 10/9

CLK_ICH_48M
CLK_ICH_14M

CLK_ICH_48M
CLK_ICH_14M

CLK_ICH_48M
CLK_ICH_14M

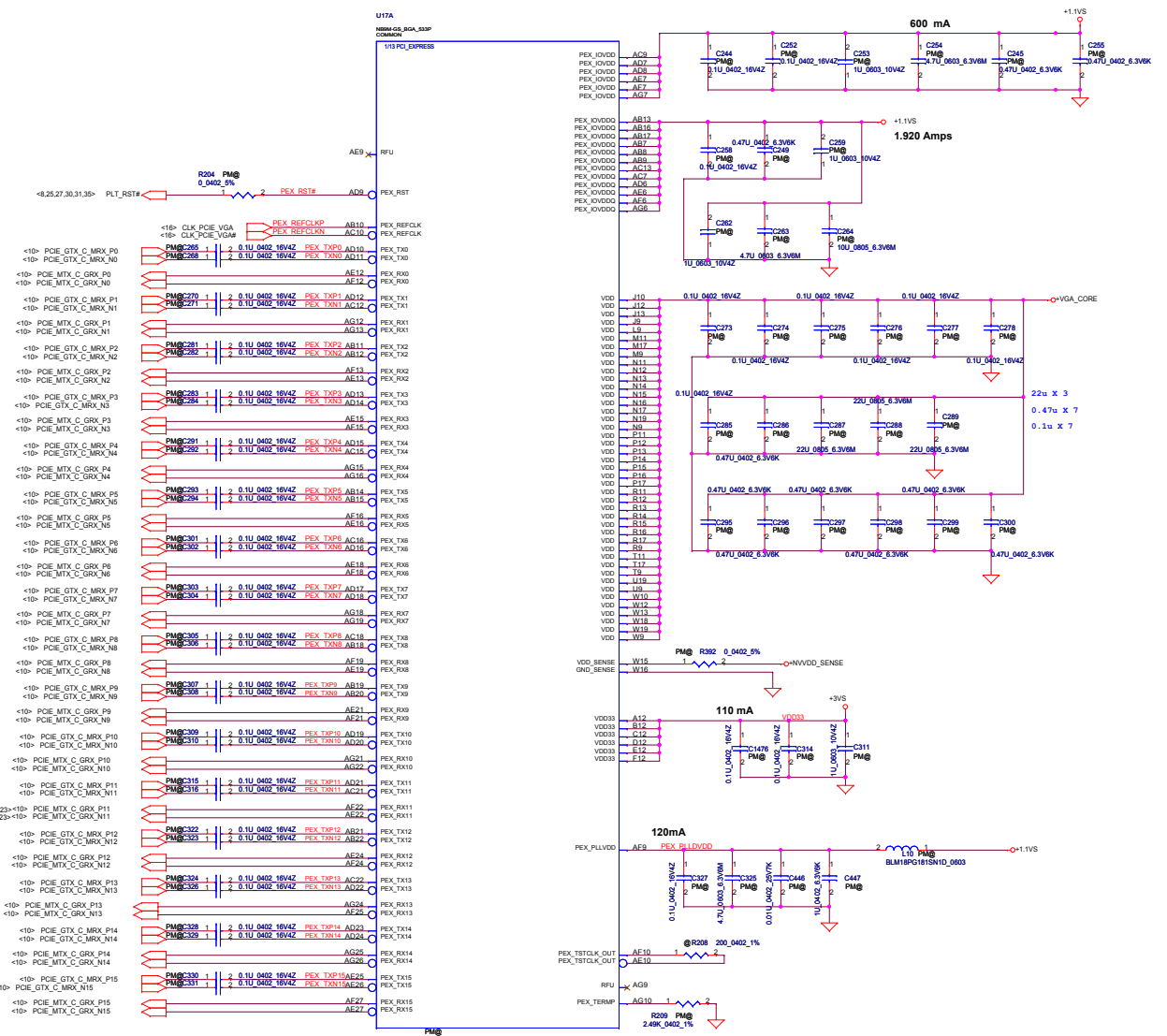
CLK_ICH_48M
CLK_ICH_14M



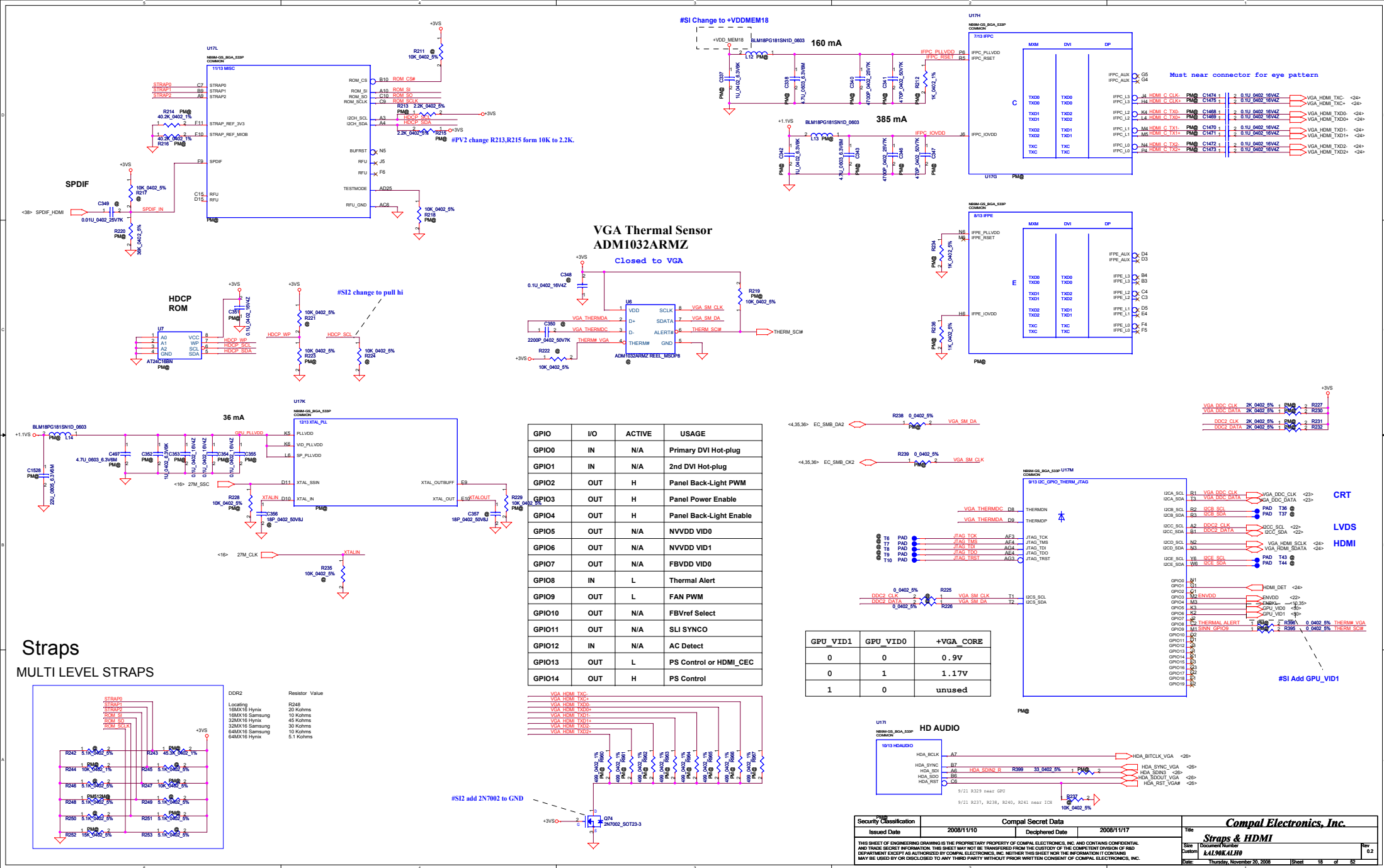
Clock Generator

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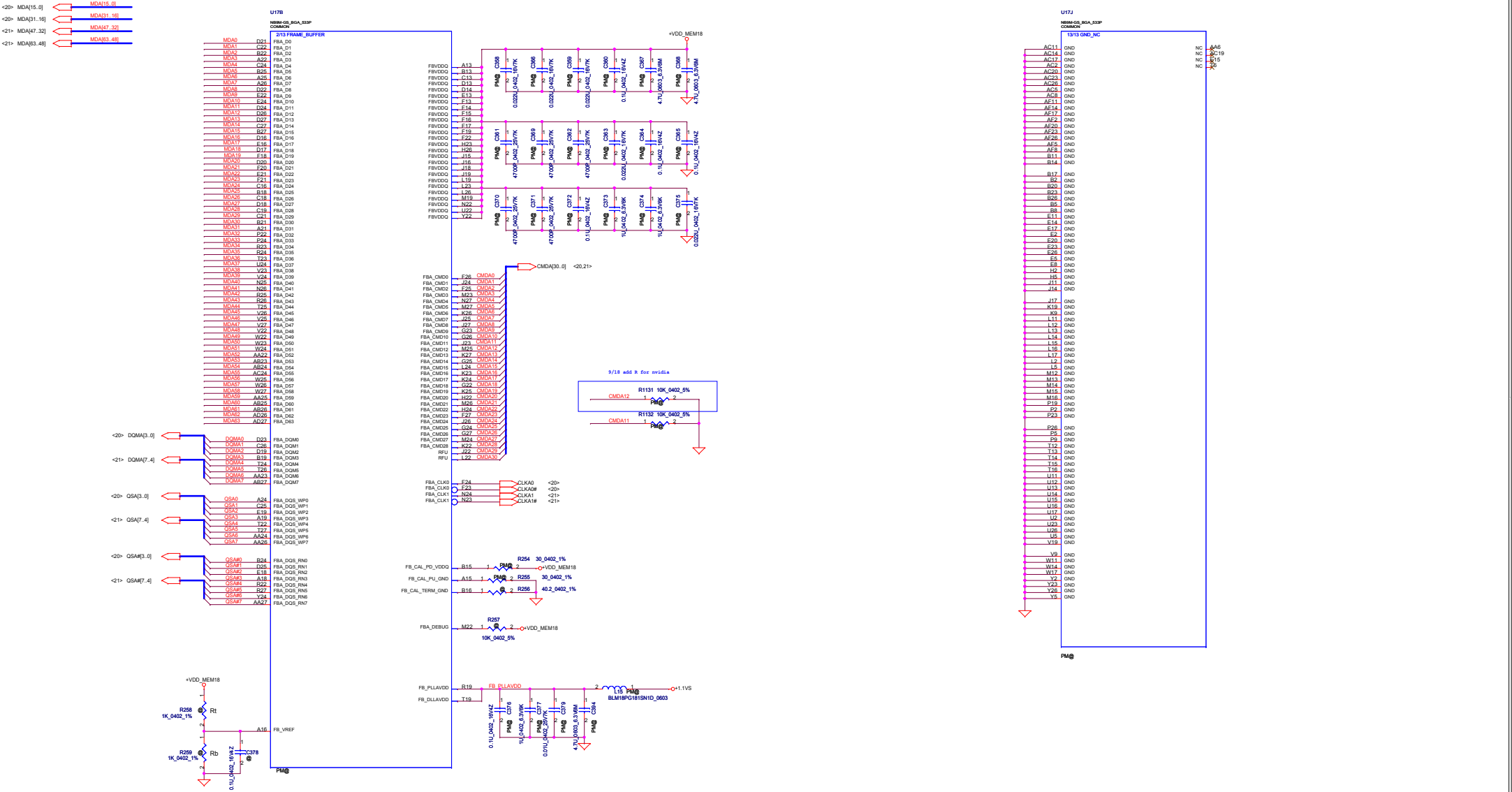
PEG Interface



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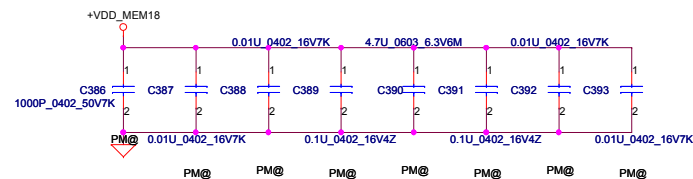
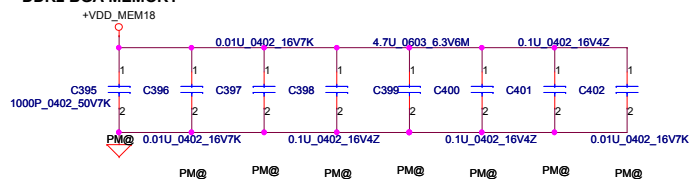


VRAM Interface



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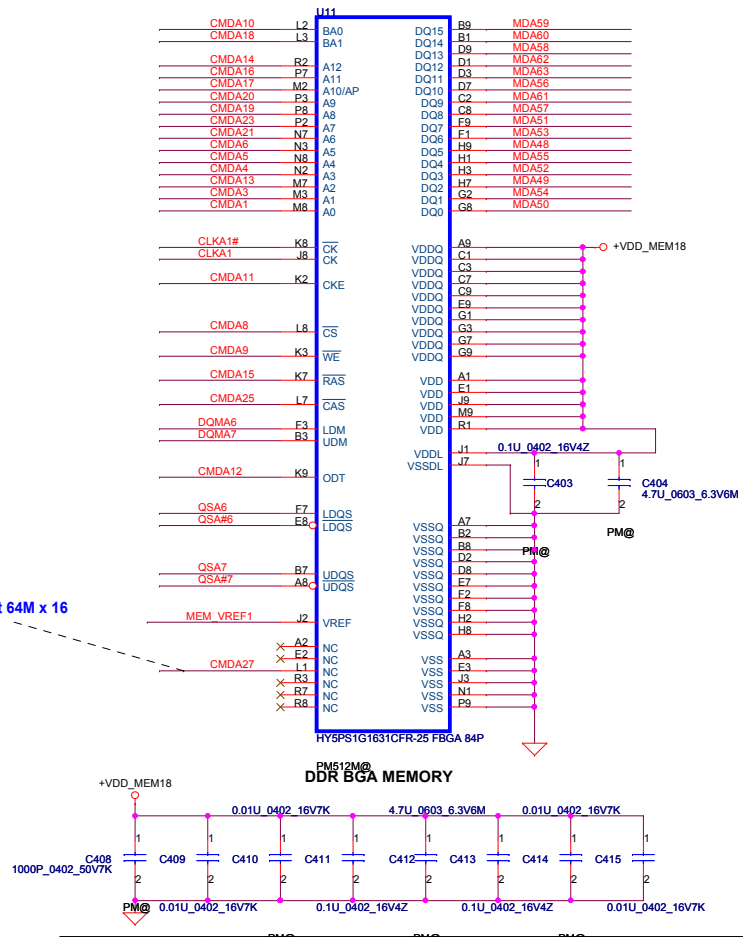
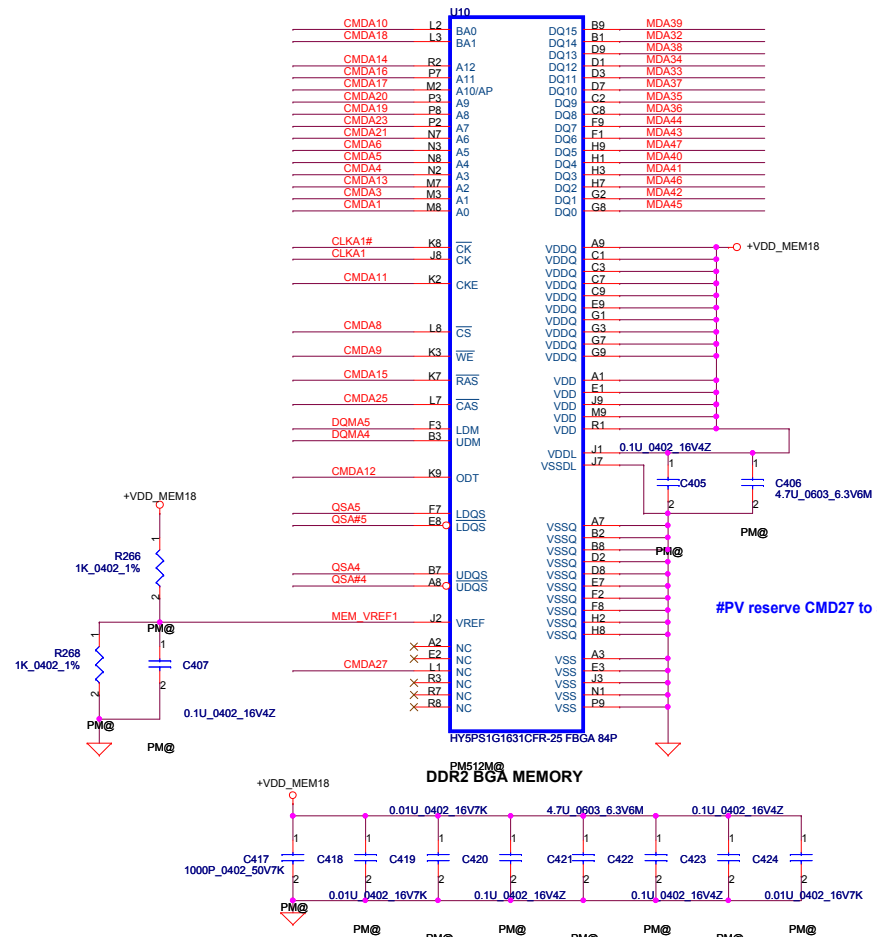
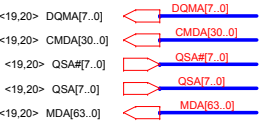
64Mx16 DDR2 400MHz*4==>512MB



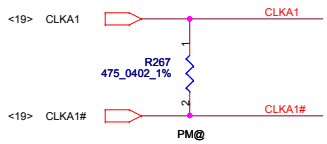
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

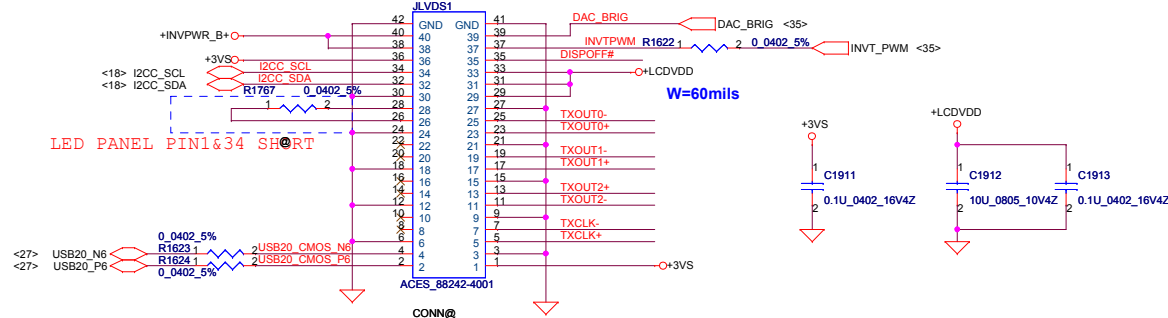
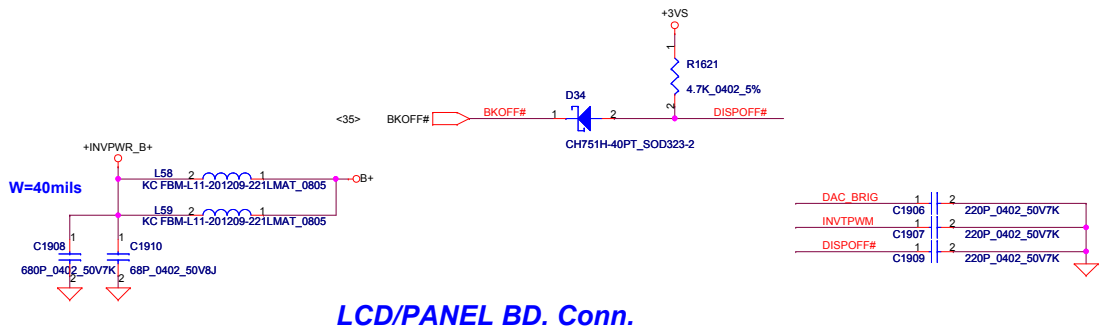
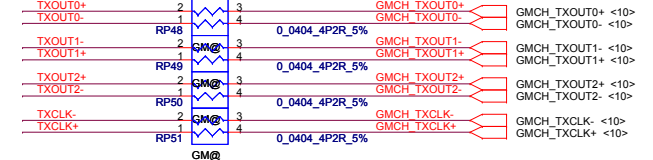
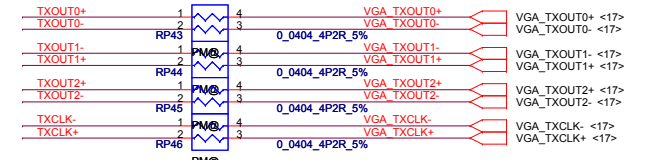
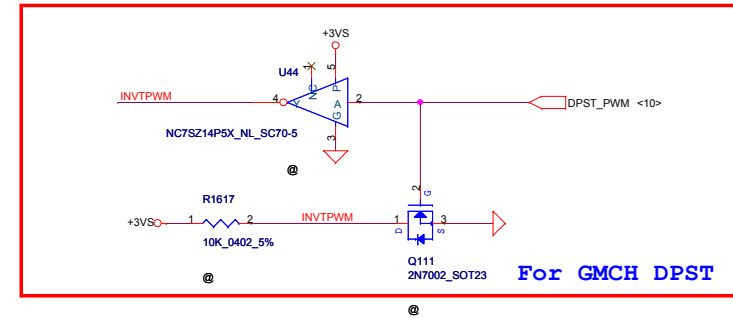
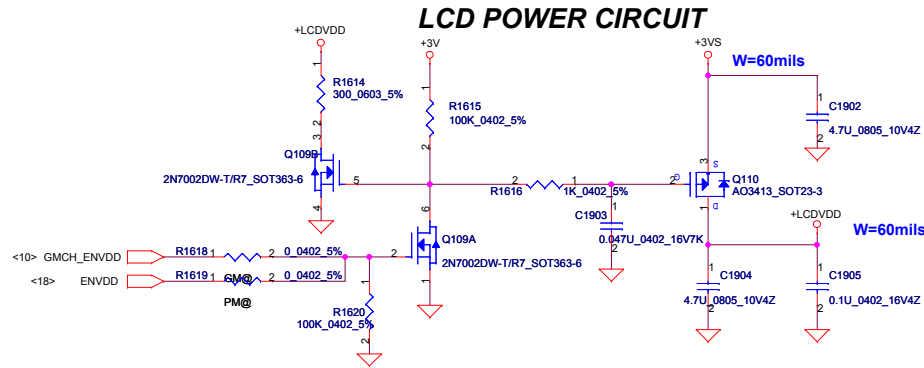
64Mx16 DDR2 400MHz*4==>512MB



DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

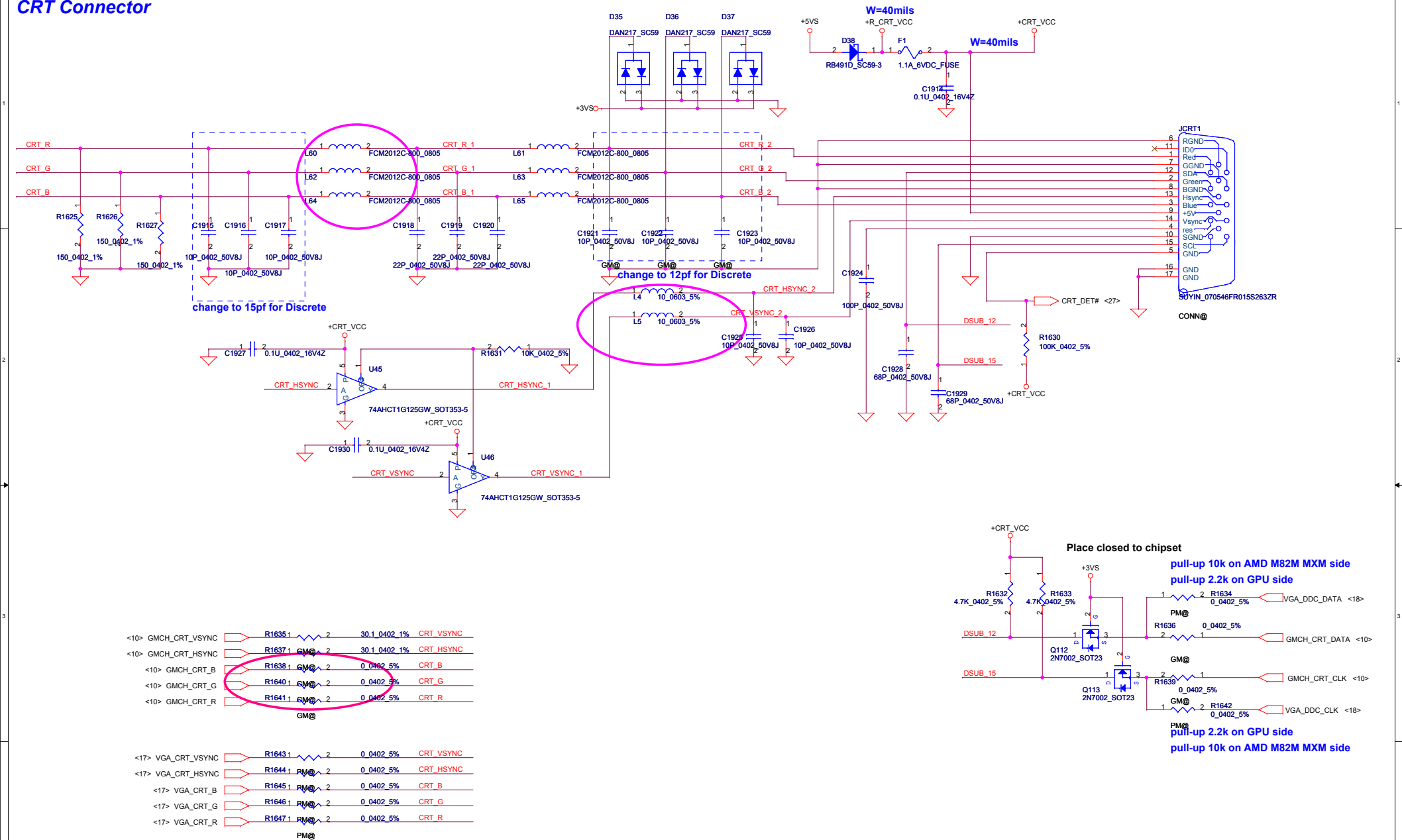


Security Classification	PM@	PM@	PM@	PM@	PM@	PM@	PM@	Compal Secret Data	
Issued Date	2008/11/10				Deciphered Date		2008/11/17		Title
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								VRAM 2	
								Size	Document Number
								KAL90	Rev 0.1
Date: Thursday, November 20, 2008								Sheet	8 of 16

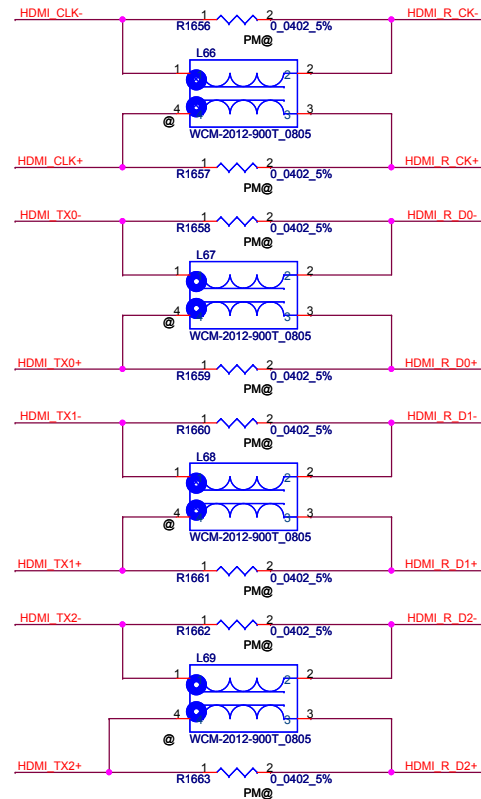
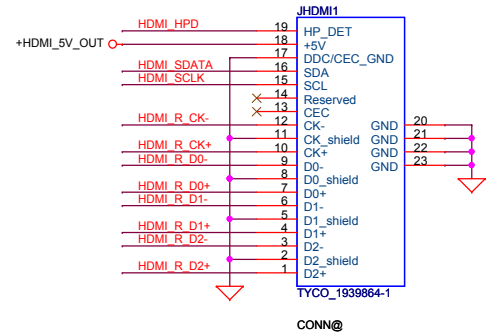
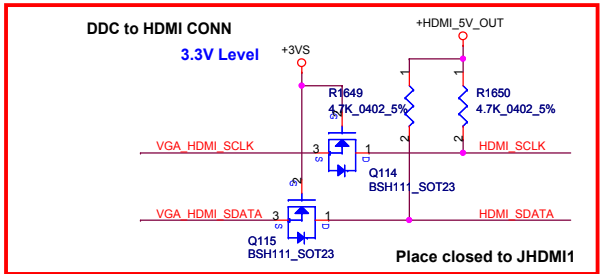
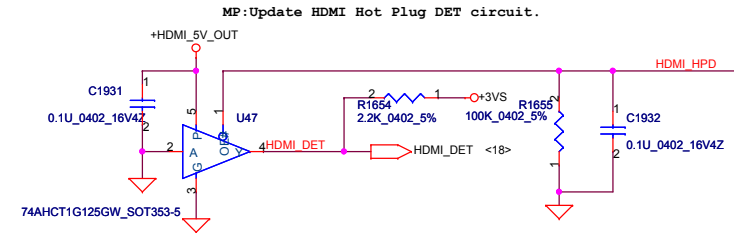
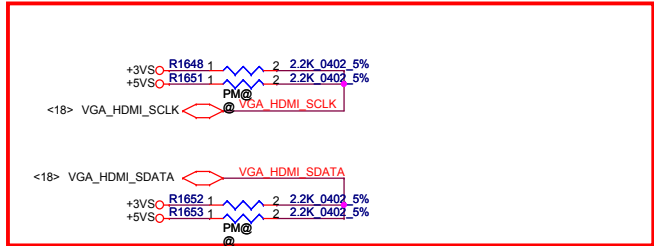


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				Custom	kAL90KALH0
				Date	Thursday, November 20, 2008
				Sheet	22 of 52
				Rev	0.2

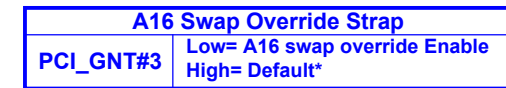
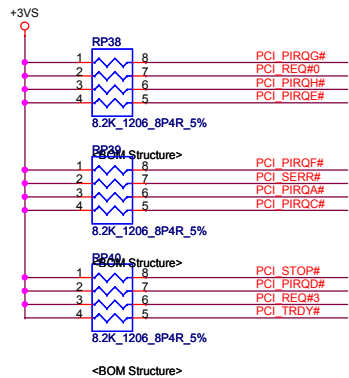
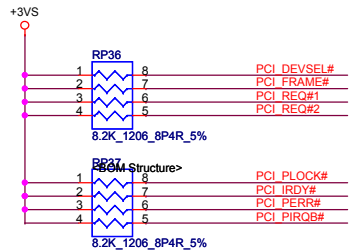
CRT Connector



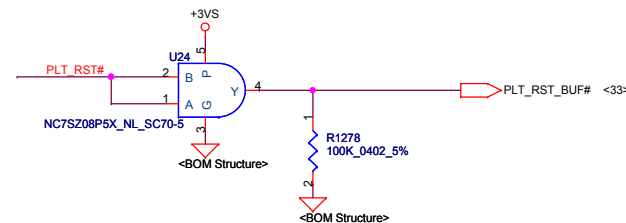
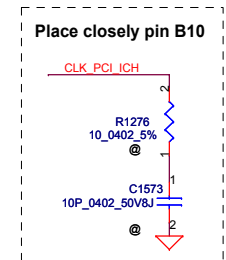
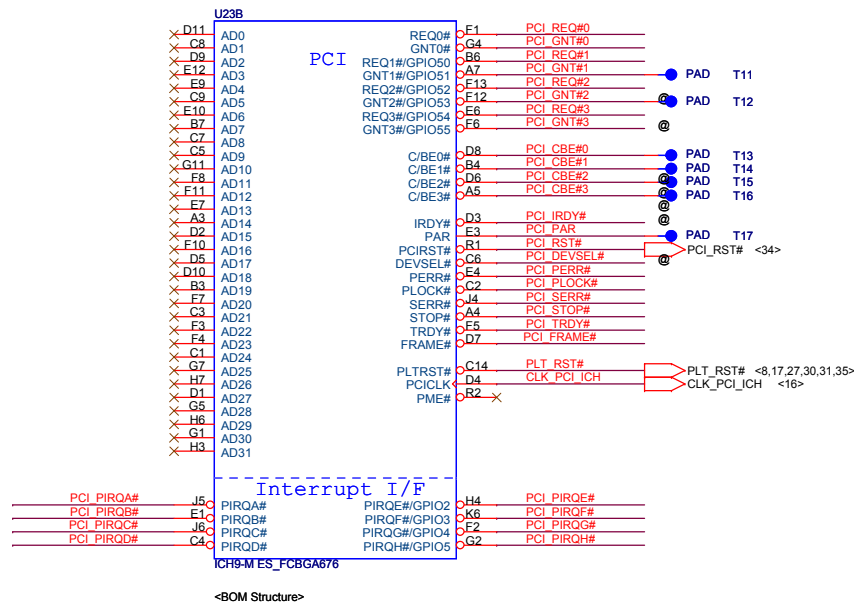
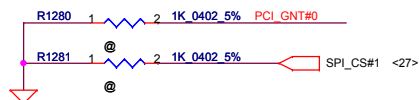
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Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title CRT Connector		
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				KAL90KALH0		0.2
				Date: Thursday, November 20, 2008		Sheet 23 of 52



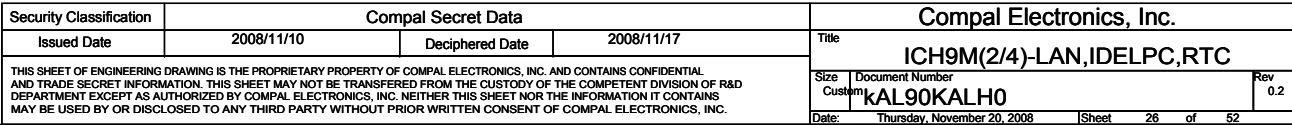
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Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title	
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Size		Document Number		Rev	
Custom		KAL90KALH0		0.2	
Date:		Thursday, November 20, 2008		Sheet 24 of 52	

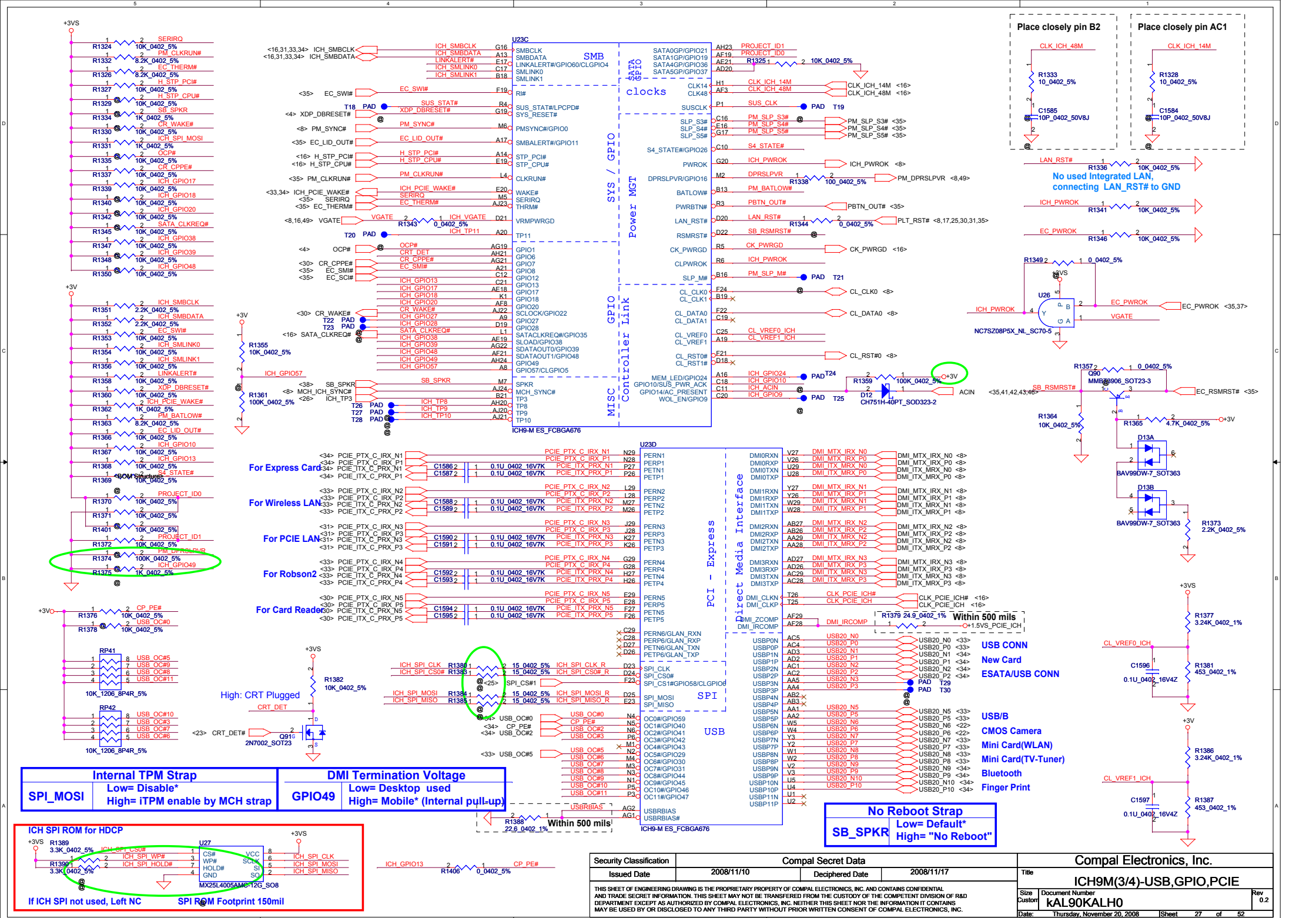


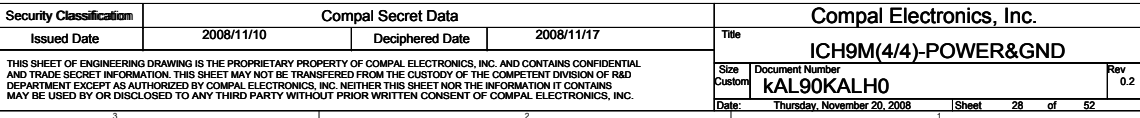
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

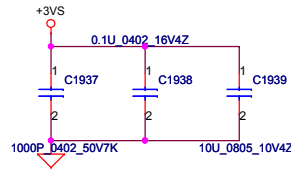


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				Size	Document Number			Rev	
				KAL90KALH0				0.2	
				Date:				Thursday, November 20, 2008	Sheet 25 of 52

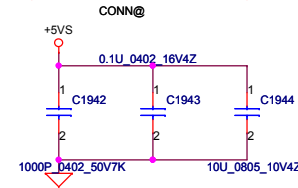
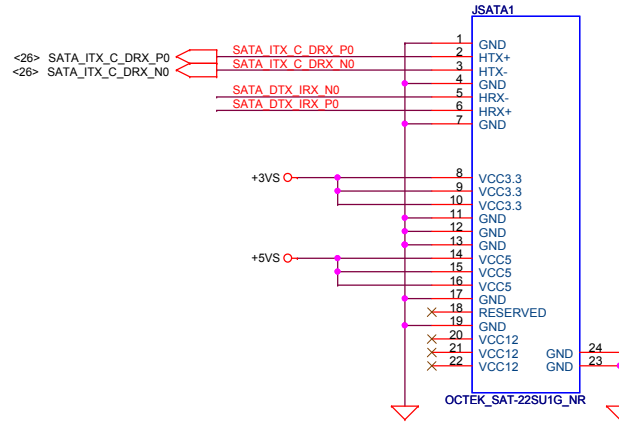
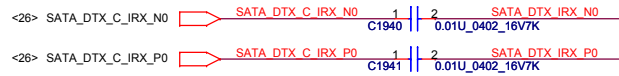




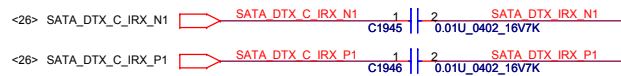
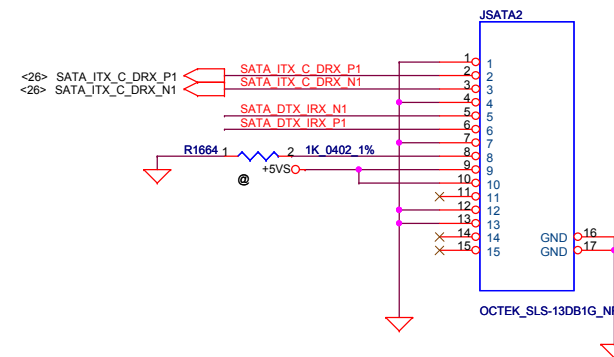




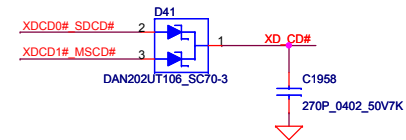
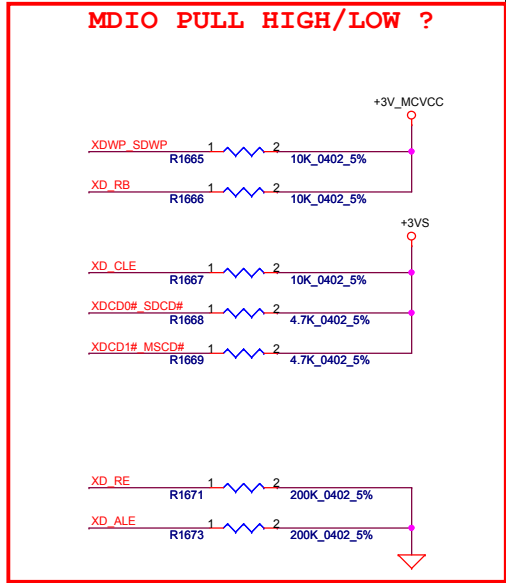
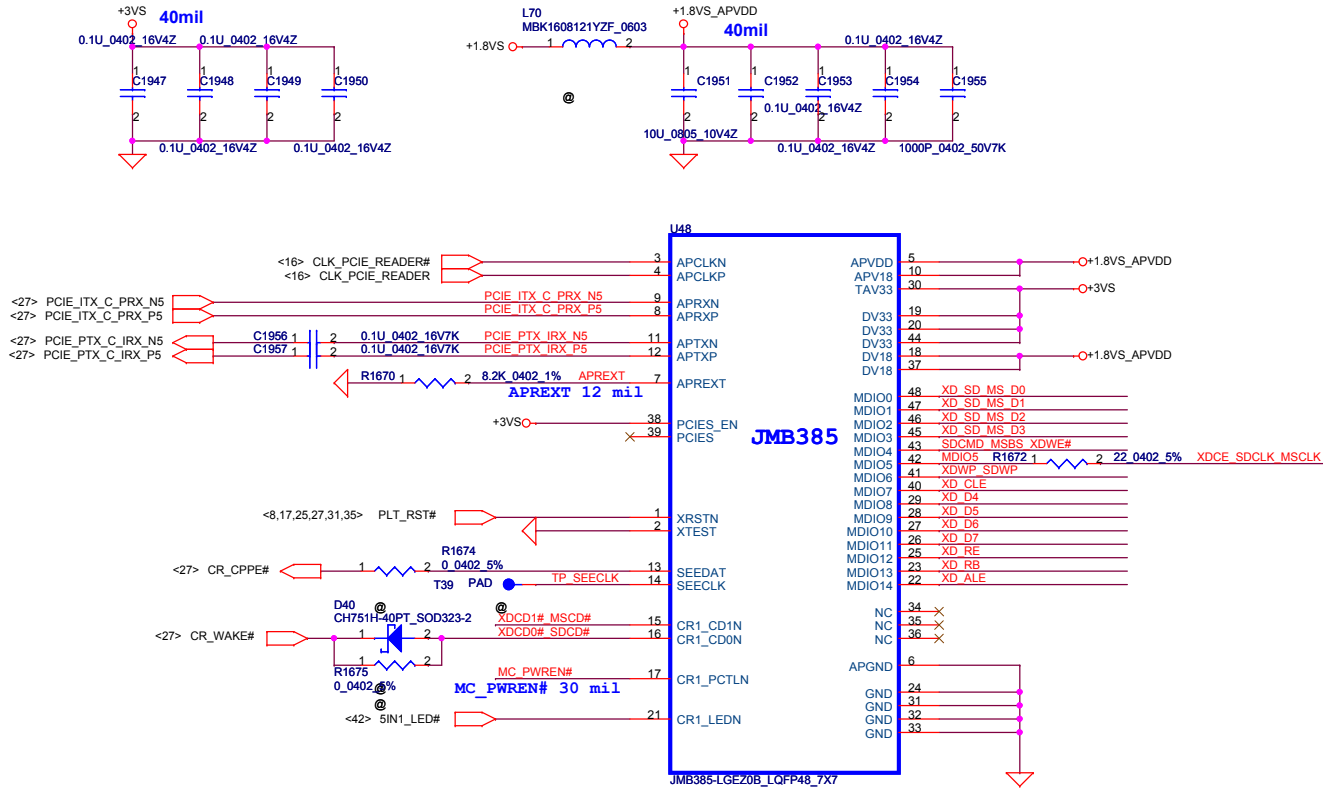
SATA HDD Conn.



SATA ODD Conn.

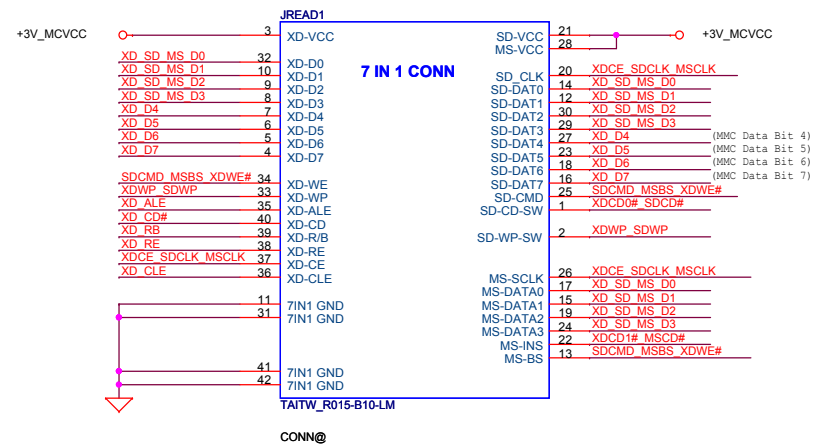
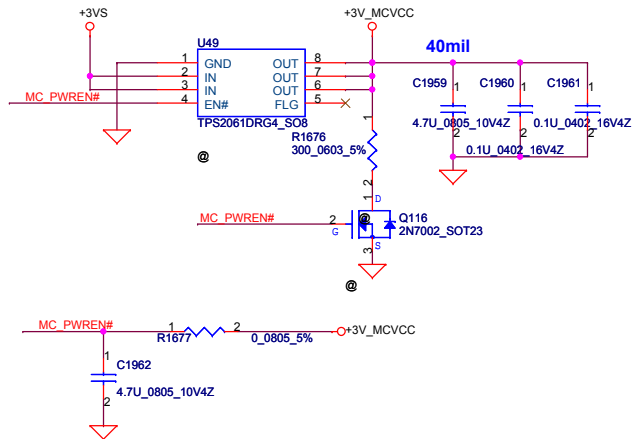


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				Custom	KAL90KALH0
				Date	Thursday, November 20, 2008
				Sheet	29 of 52
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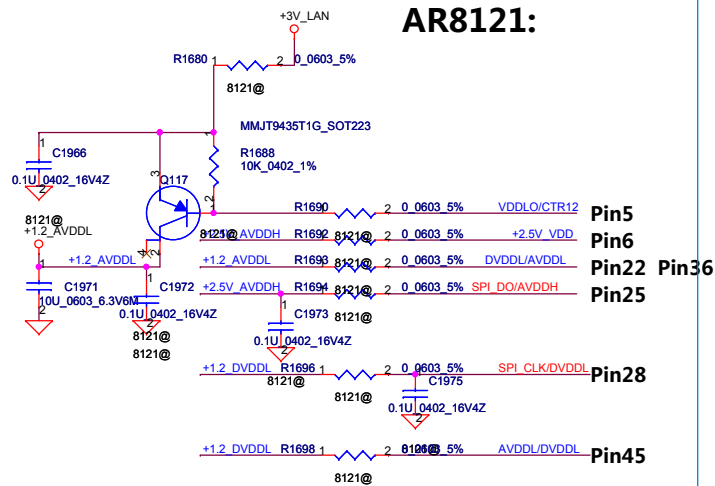
4 IN 1 Socket Push Type(New)

Memory Card Power Switch

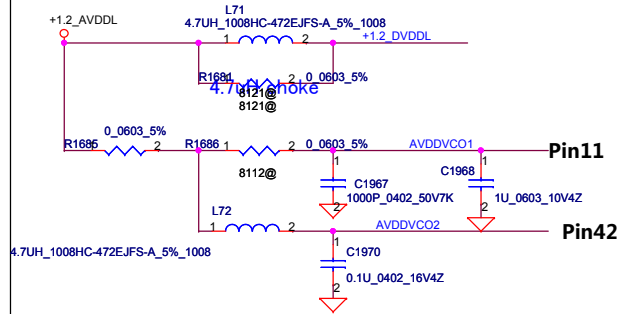
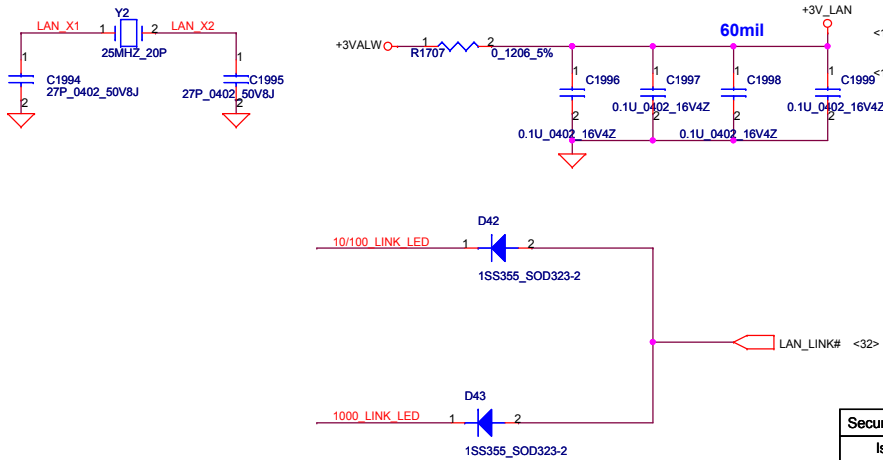
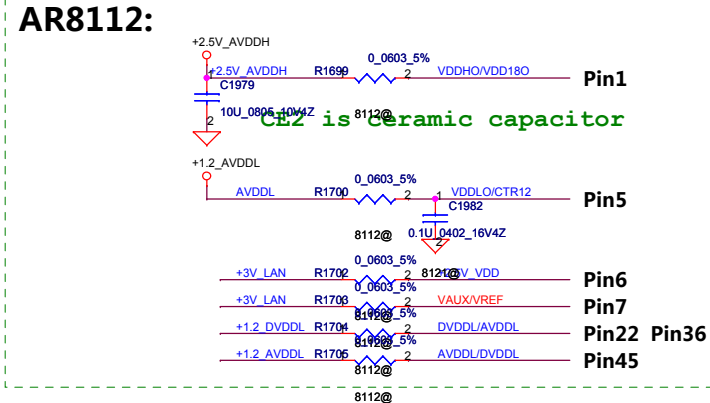


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Size	Document Number	Rev		0.2	
Customer	KAL90KALH0	Date		Thursday, November 20, 2008	
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AR8121:

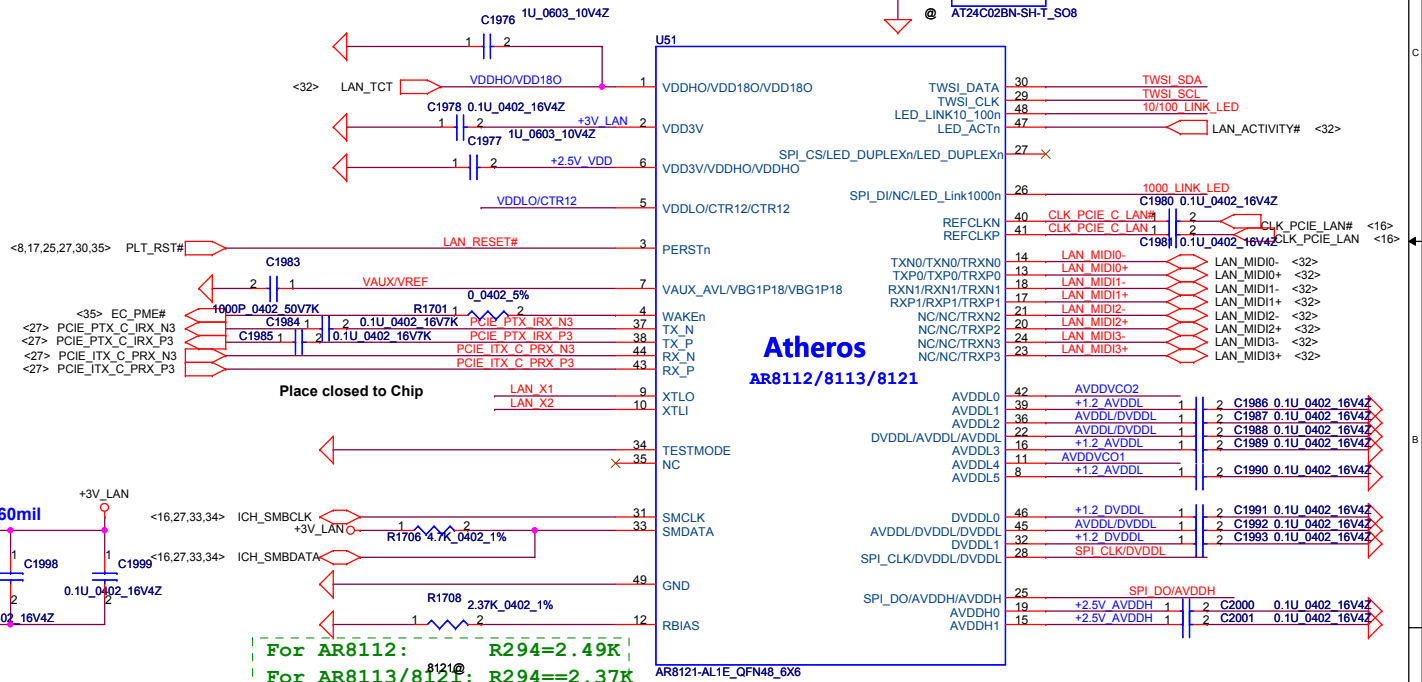


AR8112:

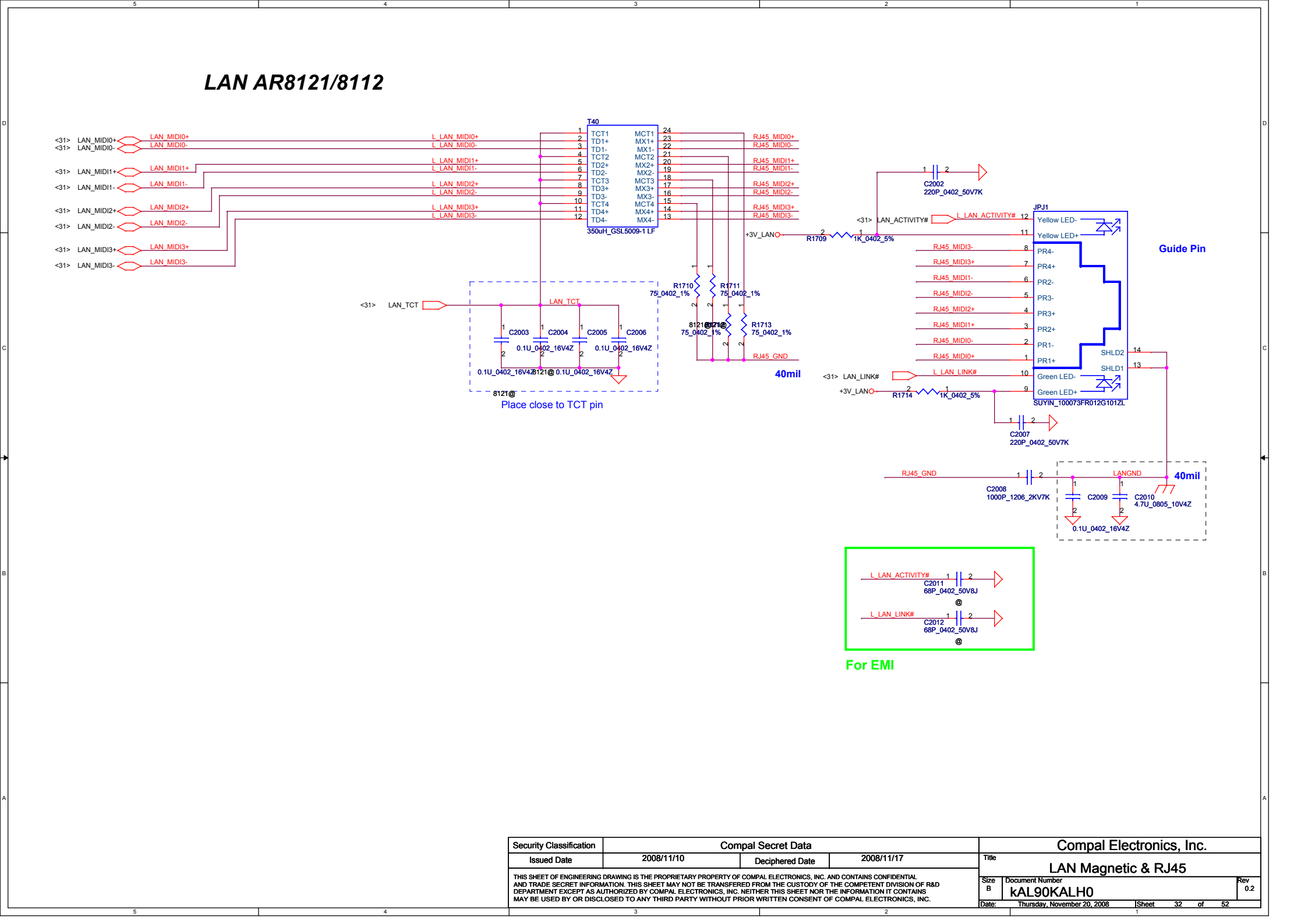


AR8113/AR8121: If overclocking, R592, L49 stuffed and removed. If not overclocking, R591, L49 stuffed and R592 removed.

AR8112: Stuff R591, R48 and L49 for all mode.



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				Custm	KAL90KALH0	0.2	
				Date:	Thursday, November 20, 2008	Sheet 31 of 52	

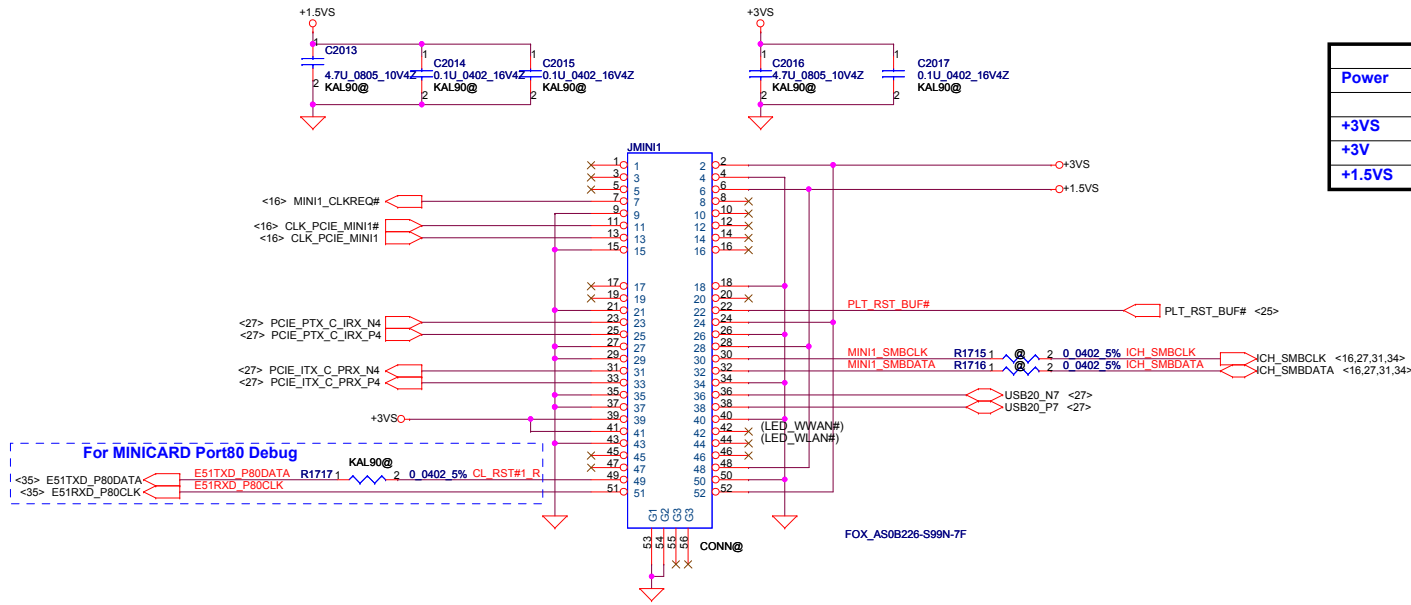
[illegible]

LAN AR8121/8112

The schematic diagram illustrates the internal wiring of the LAN AR8121/8112 module. It features a central T40 transformer with 24 pins, connected to RJ45 ports (RJ45_MIDIO+, RJ45_MIDIO-, RJ45_MIDI1+, RJ45_MIDI1-, RJ45_MIDI2+, RJ45_MIDI2-, RJ45_MIDI3+, RJ45_MIDI3-) and a LAN_TCT pin. The transformer is connected to a network of capacitors (C2002, C2003, C2004, C2005, C2006, C2007, C2008, C2009, C2010, C2011, C2012) and resistors (R1709, R1710, R1711, R1713, R1714). The RJ45 connector is shown with pins 1 through 14, including Yellow LED+, Yellow LED-, Green LED+, Green LED-, and SHLD1, SHLD2. A 40mil trace is shown for the LAN_ACTIVITY# and LAN_LINK# signals. A note indicates to place the 8121 component close to the TCT pin. A table at the bottom provides security classification and document information.

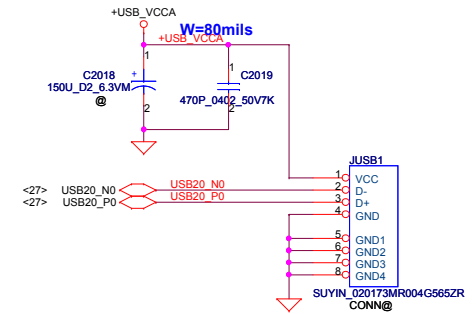
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Size	B	Document Number	kAL90KALH0	Rev	0.2
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For Robson2

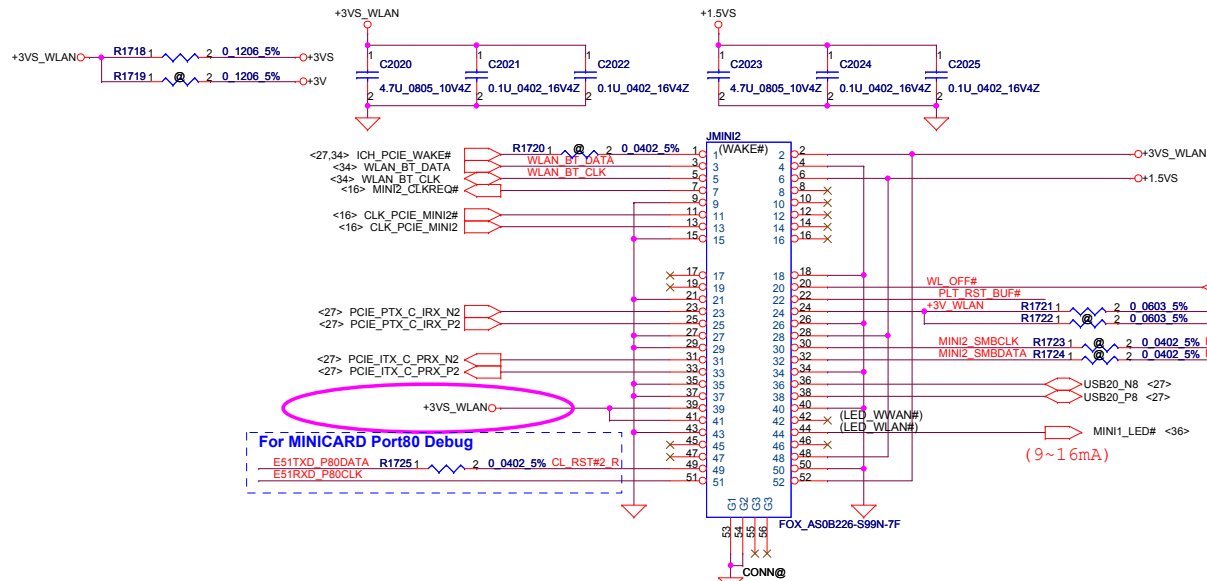


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

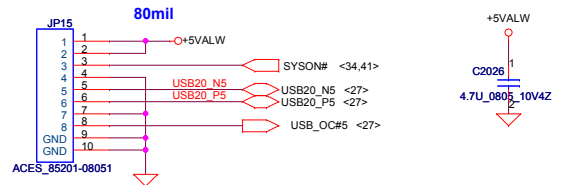
USB CONN.



For Wireless LAN

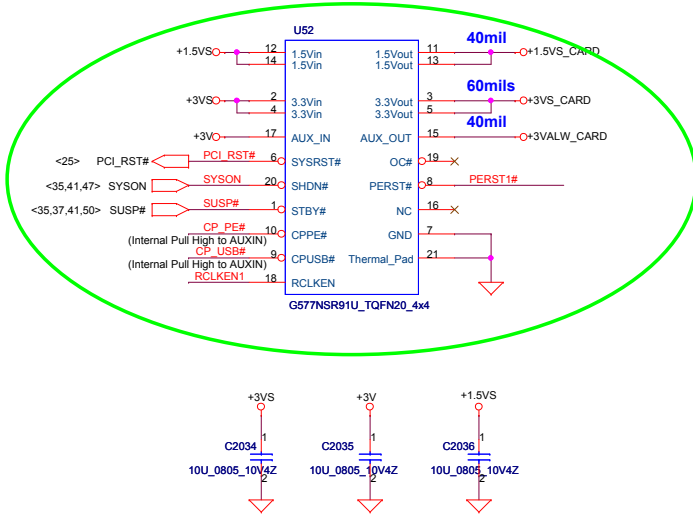


To USB/B Connector

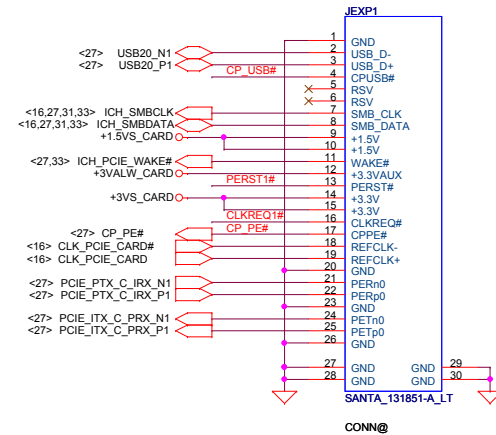


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				Size B	Document Number kAL90KALH0	Rev 0.2
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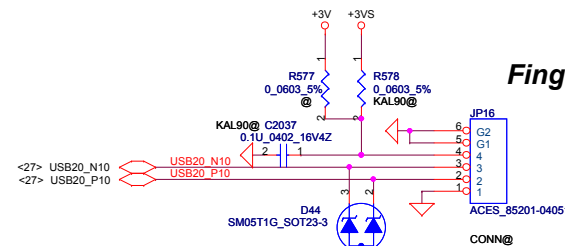
New Card Power Switch



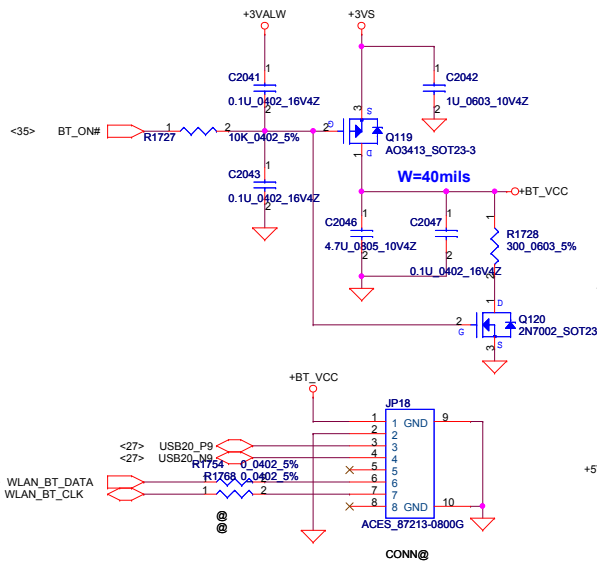
New Card Socket (Left/TOP)



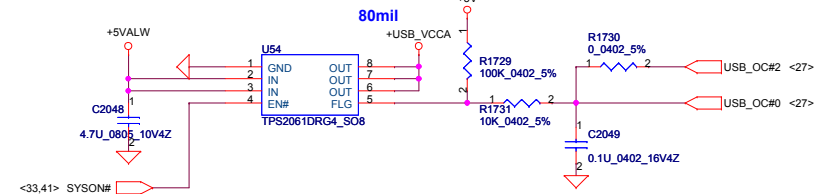
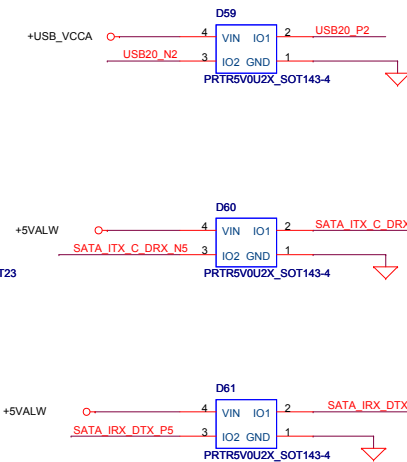
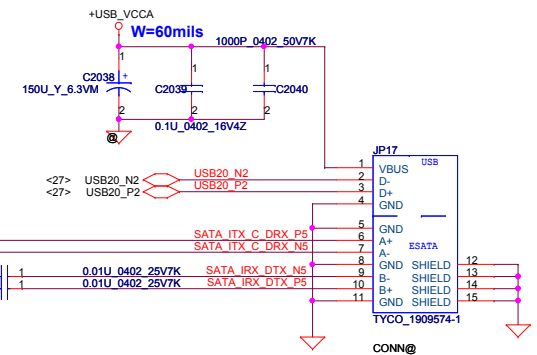
Finger Print Conn.



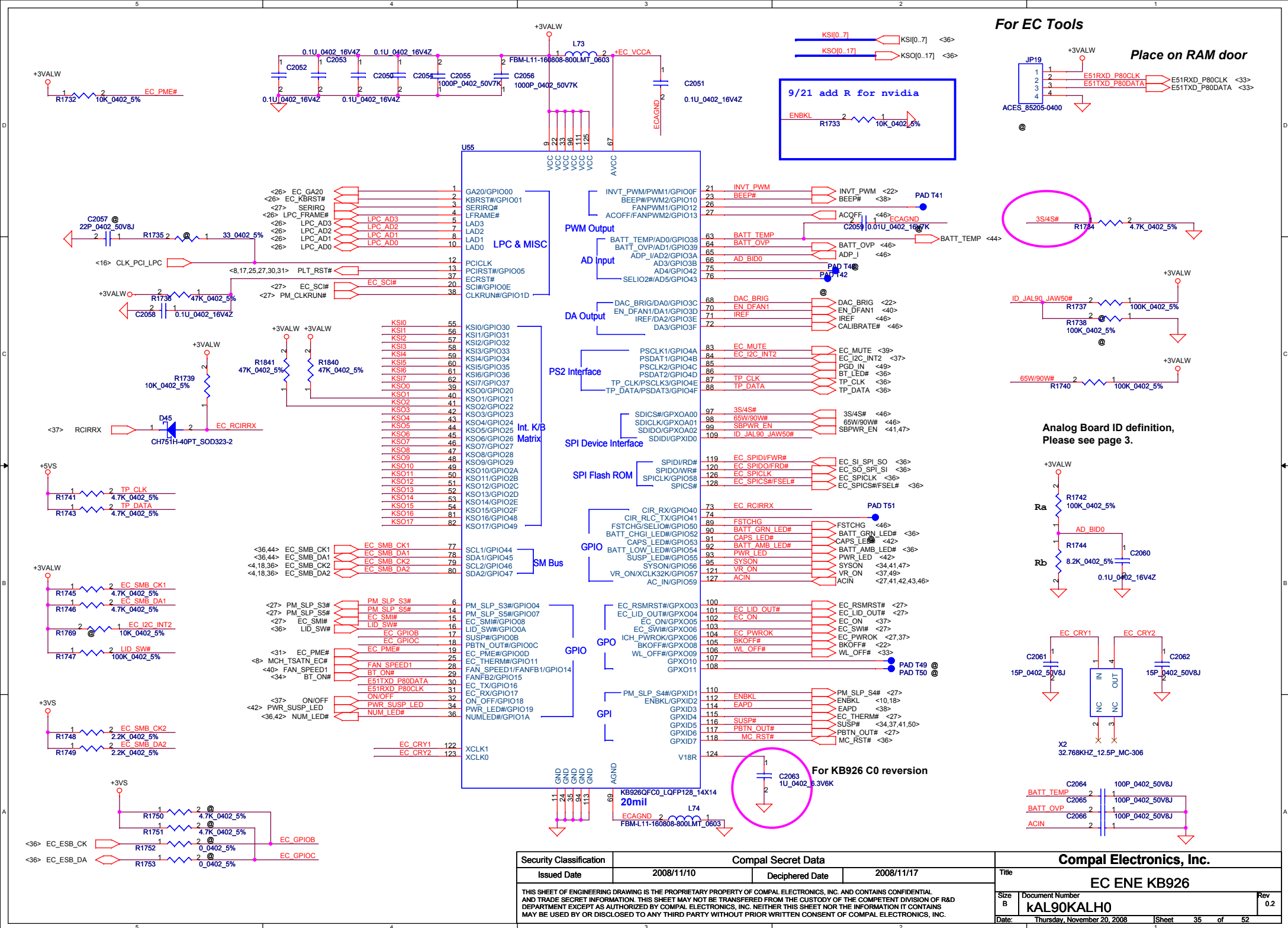
Bluetooth Conn.



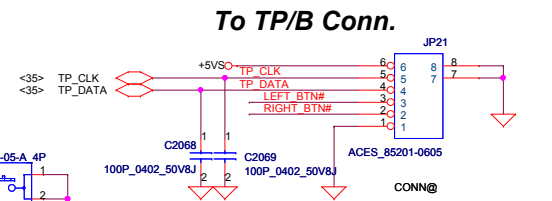
ESATA CONN



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Size	B	Document Number	kAL90KALH0	Rev	0.2
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Issued Date	2008/11/10	Deciphered Date	2008/11/17	EC ENE KB926			
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				Size	Document Number	Rev	
				B	KAL90KALH0	0.2	
				Date:	Thursday, November 20, 2008	Sheet	35 of 52



The schematic diagram illustrates the PCB layout for the TP module. It features three SW5 SMT1-05-A 4P switches and one D46 PSOT24C_SOT23 diode. The switches are connected to RIGHT_BTN#3, LEFT_BTN#, and RIGHT_BTN#3. The diode is connected to TP_CLK and TP_DATA. A +5VS supply is connected to a C2070 0.1U_0402_16V4Z capacitor.

Diagram of JP25 connector pinout:

- Pin 1: KSO0
- Pin 2: KSI5
- Pin 3: Connected to a common ground
- Pin 4: E&T_6905-E04N-00R

CONN@

	KSO0
KS11	WL_BTN#
KS12	BT_BTN#
KS13	EMAIL_BTN#
KS14	IE_BTN#
KS15	E-KEY_BTN#

Pinout diagram for J28 connector:

- Pin 1: +5VS
- Pin 2: (Crossed out)
- Pin 3: +3VS
- Pin 4: MINI1_LED# <33>
- Pin 5: FB KS14
- Pin 6: BT_LED#
- Pin 7: FB KS15
- Pin 8: BT_LED# <35>
- Pin 9: GND
- Pin 10: GND

Connector: J28
Label: CONN@
Part Number: ACES_85201-08051

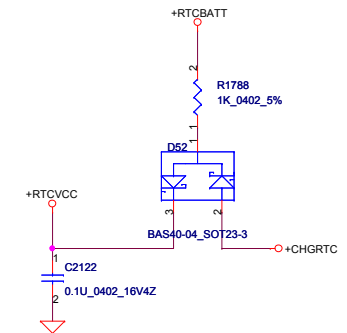
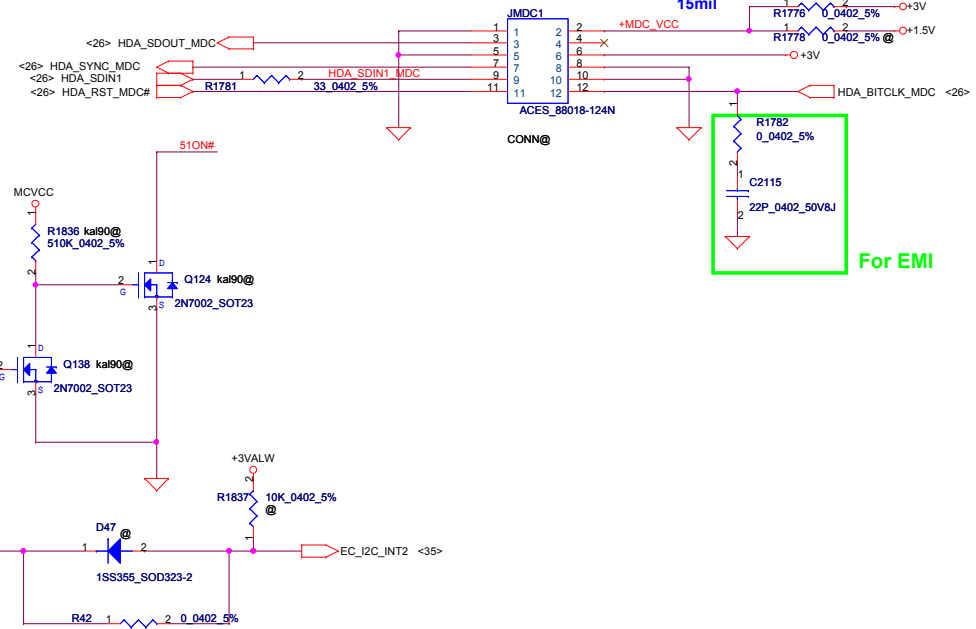
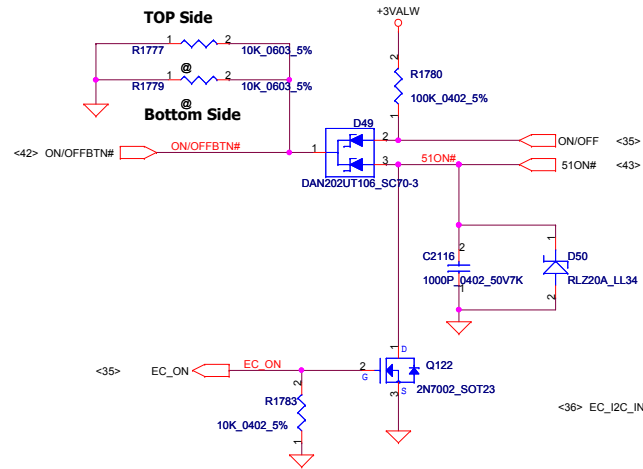
Pinout diagram for the JP26 header of the ES 8520T-1005N module:

- Pin 1: +5VS
- Pin 2: +3VS
- Pin 3: MINI1_LED#
- Pin 4: KS1
- Pin 5: FB KS14
- Pin 6: KSO0
- Pin 7: KS12
- Pin 8: BT_LED#
- Pin 9: FB KS13
- Pin 10: (Empty)
- Pin 11: GND
- Pin 12: GND

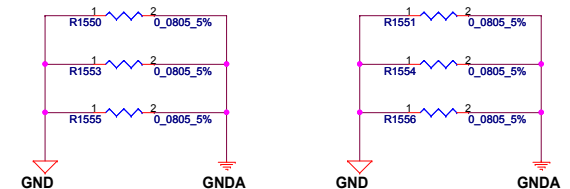
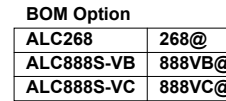
Notes: MINI1_LED# and BT_LED# are active-low signals.

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					Size	Document Number	Rev
					kAL90KALH0		0.2
Date		Tuesday, January 06, 2009		ISheet	36	of 52	

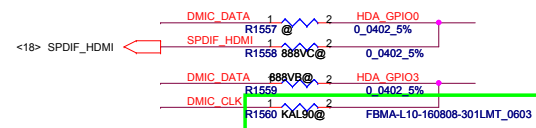
ON/OFF switch



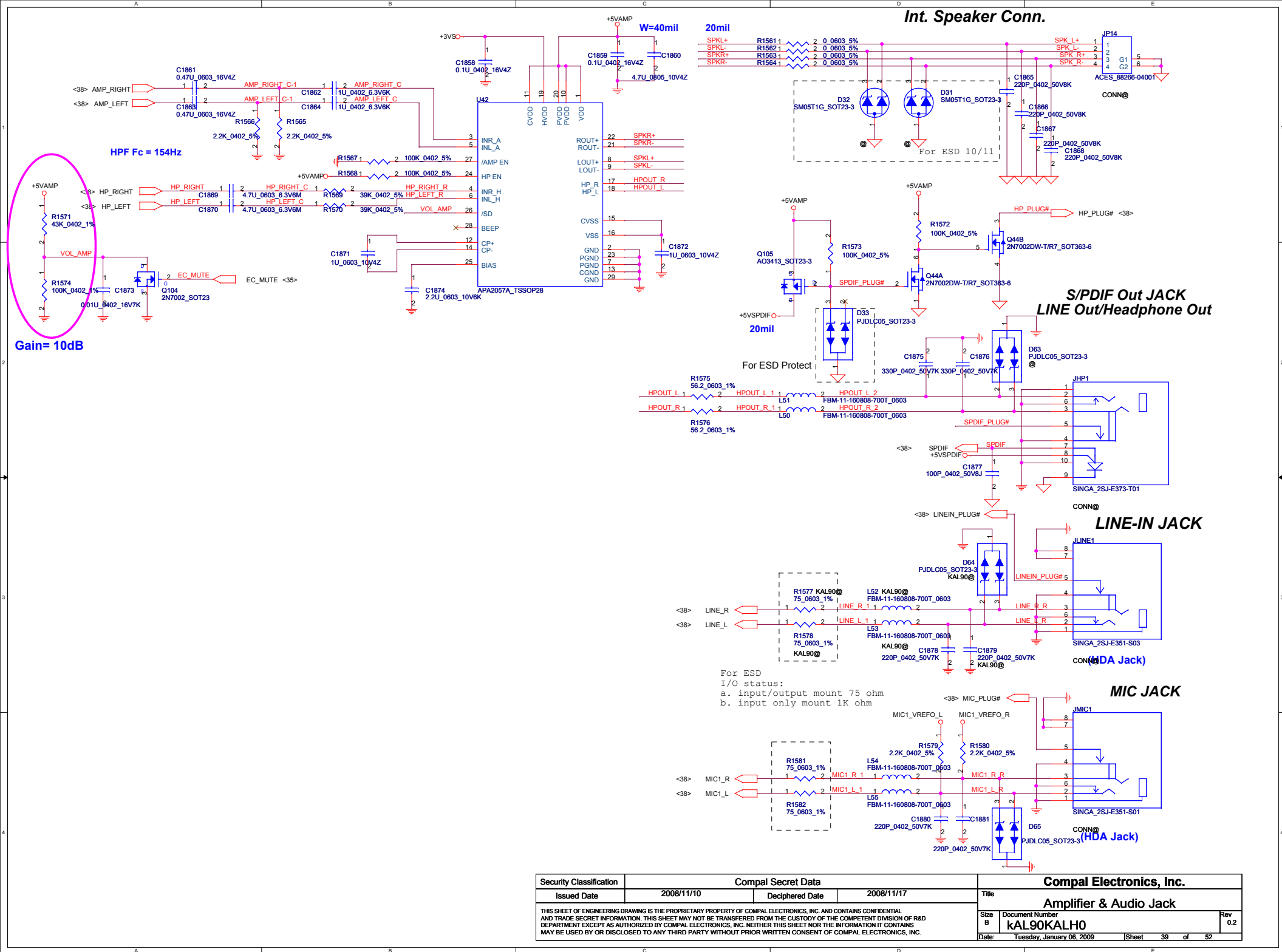
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title Power OK, Reset,RTC, CIR, MDC			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B	Document Number KAL90KALH0	Rev 0.2	
				Date Thursday, November 20, 2008	Sheet 37	of 52	



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

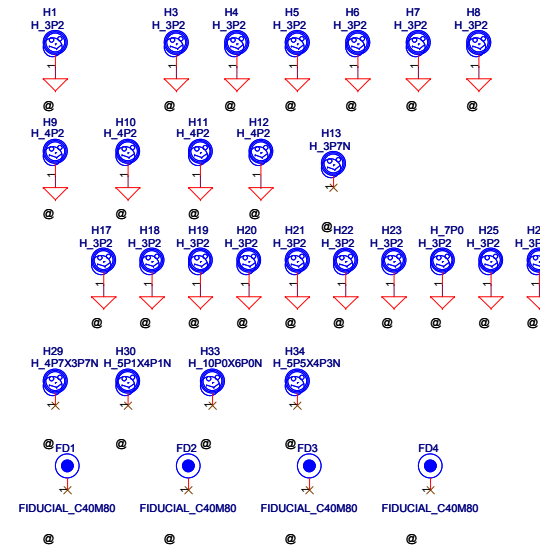


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				KAL90KALH0	
				Date: Wednesday, December 10, 2008	Sheet 38 of 52

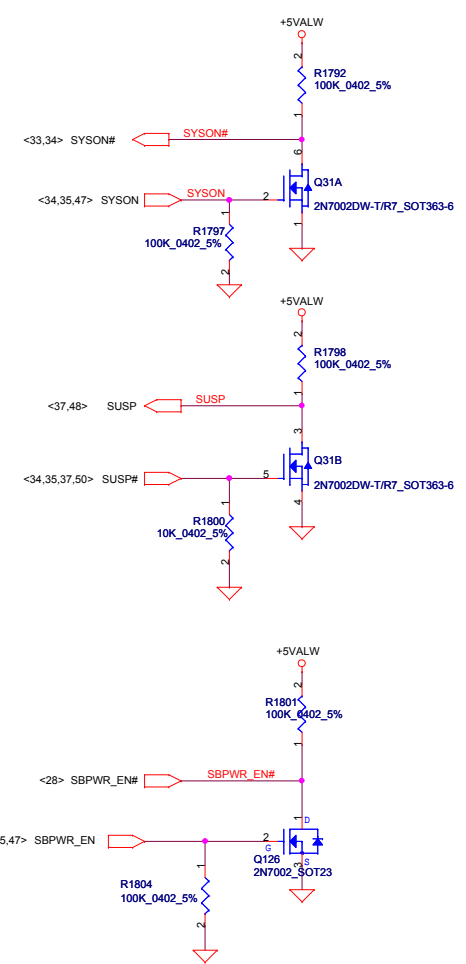
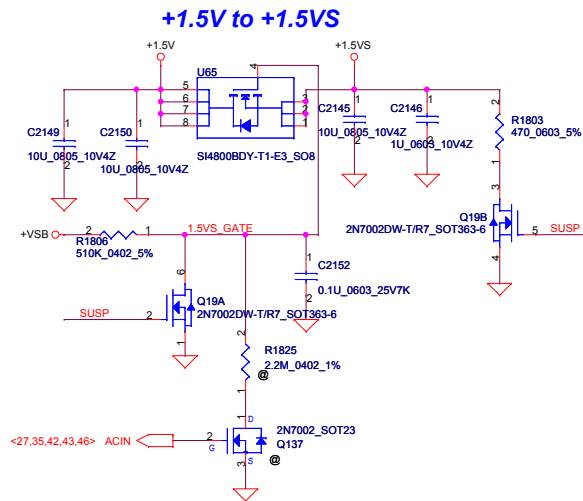
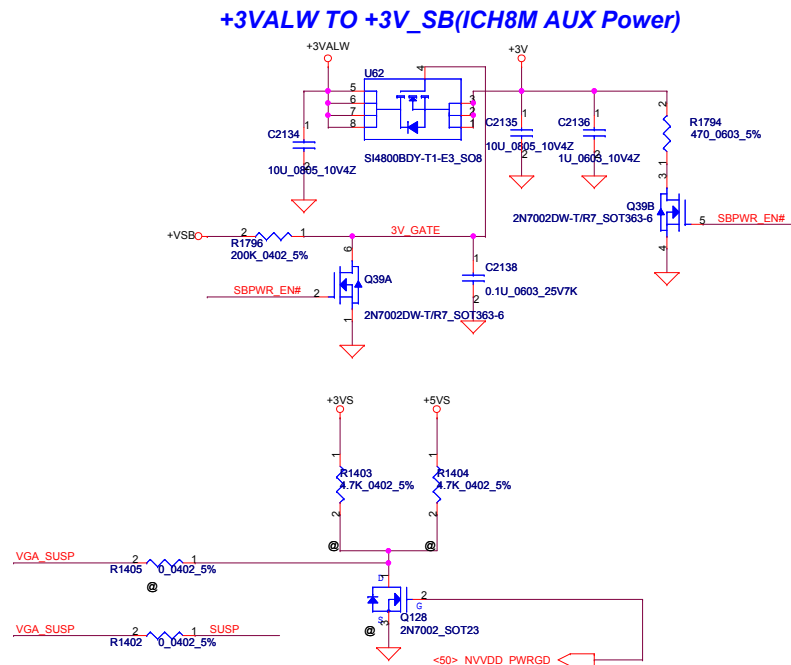
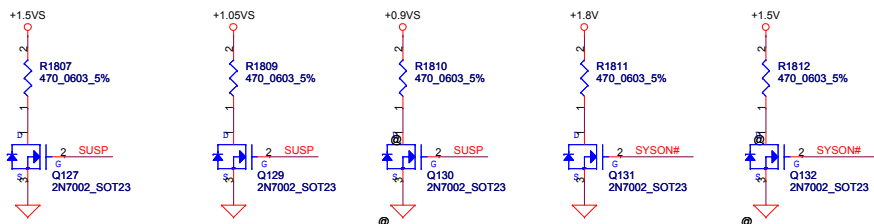


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Size	Document Number	Rev		Date	
B	KAL90KALH0	0.2		Tuesday, January 06, 2009	
Sheet		39		of 52	

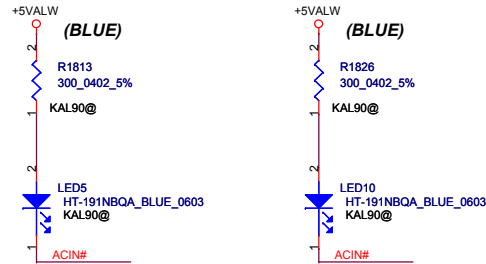
The schematic diagram illustrates the fan speed control circuit. It features a 5V power supply connected to a 100uF 0805 10V4Z capacitor (C214). The circuit includes a 300 ohm 0402 5% resistor (R41) and a 0.1uF 0402 16V4Z capacitor (C60). A 10K 0402 5% resistor (R1791) is connected to a 1000pF 0402 50V7K capacitor (C2127). The output is labeled FAN_SPEED1. The circuit is connected to a 40mil PCB and a J27 connector. The output is labeled FAN_SPEED1.



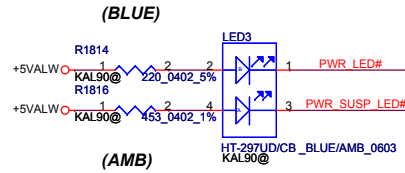
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2008/11/10	Deciphered Date		2008/11/17	
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				Size B	Document Number	Rev 0.2
				kAL90KALHO		
				Date: Thursday, November 20, 2008 Sheet 40 of 52		



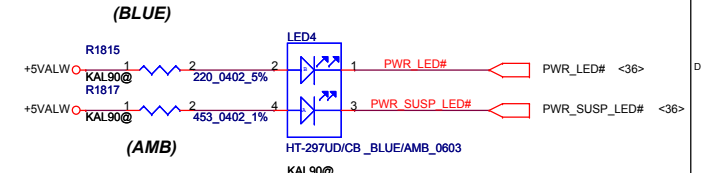
Enlightener LED



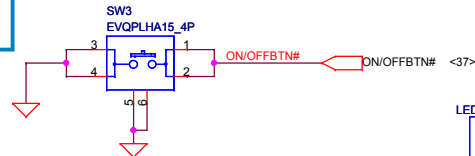
ON/OFF LED LEFT



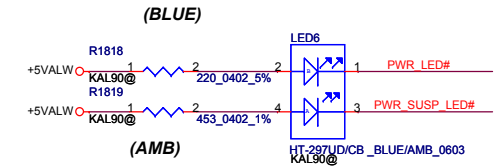
ON/OFF LED RIGHT



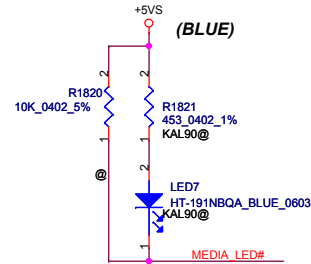
ON/OFF Button



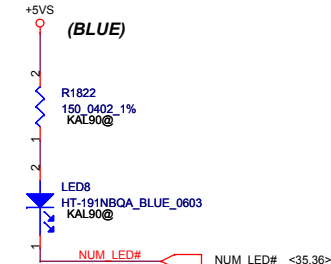
ON/OFF LED DOWN



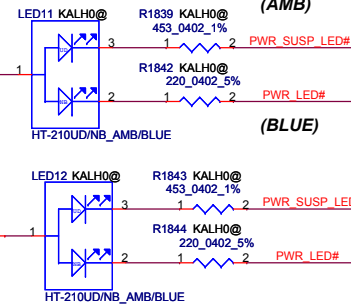
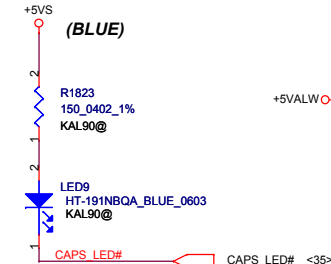
MEDIA_LED



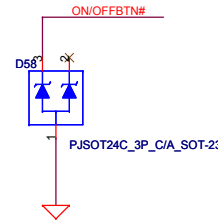
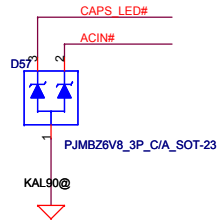
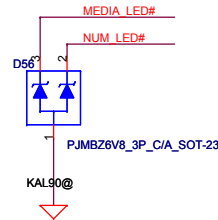
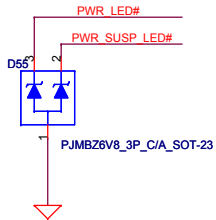
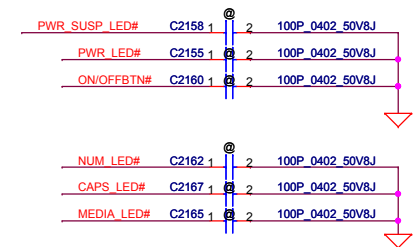
NUM_LED



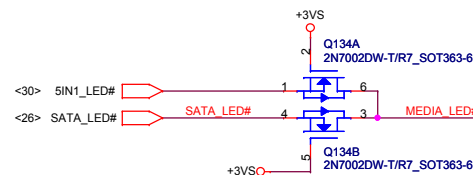
CAPS_LED



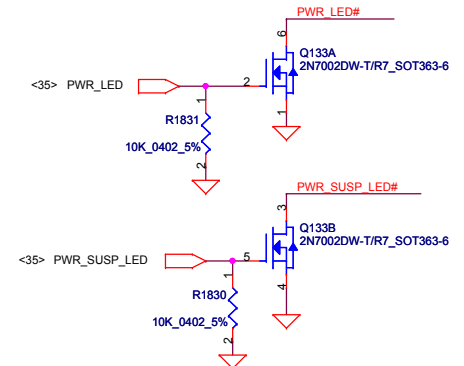
FOR EMI



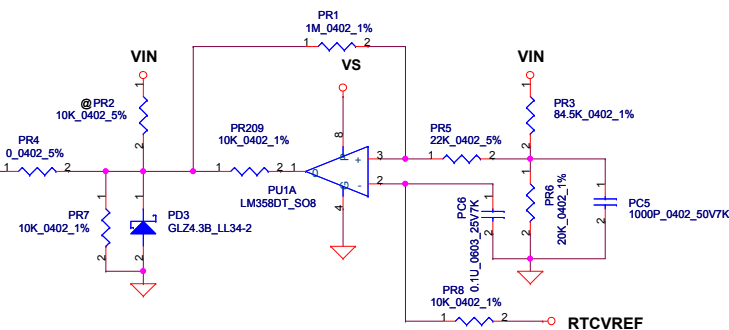
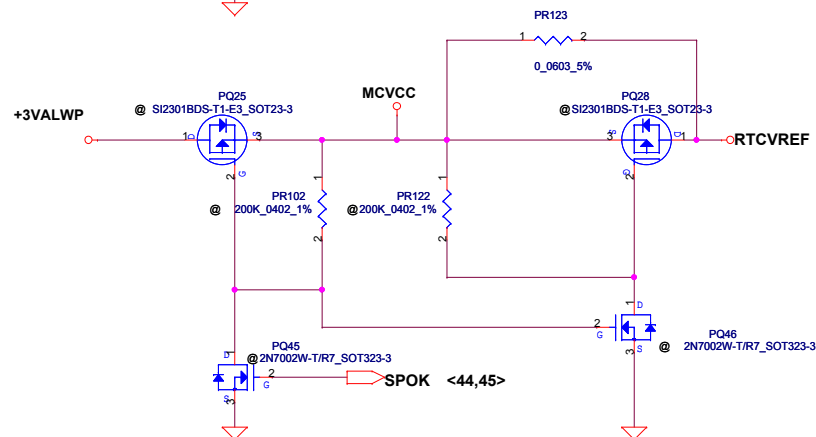
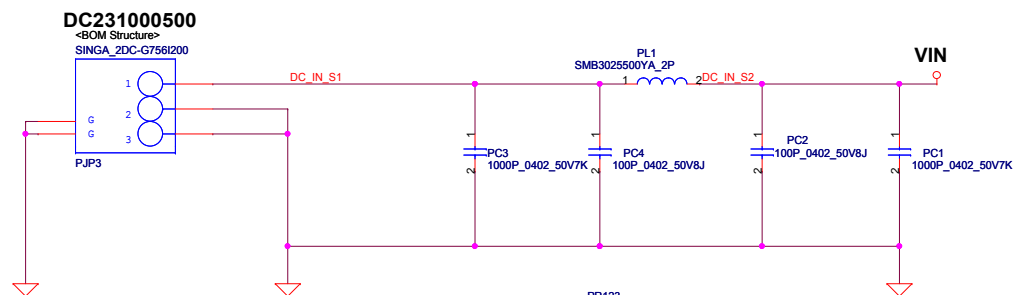
D1 D2 D3 USE PANJIT PJMBZ6V8
SCA00000I00
6.8V



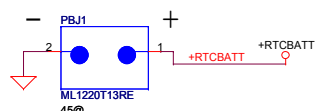
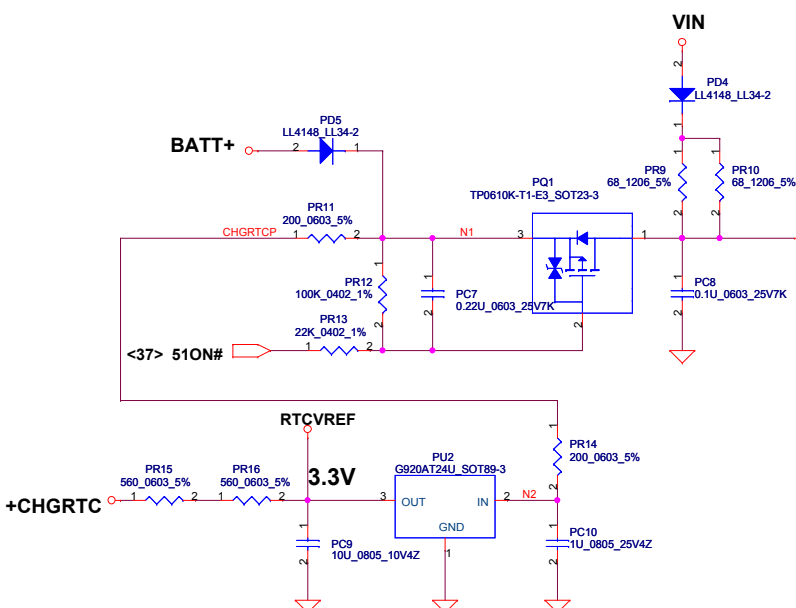
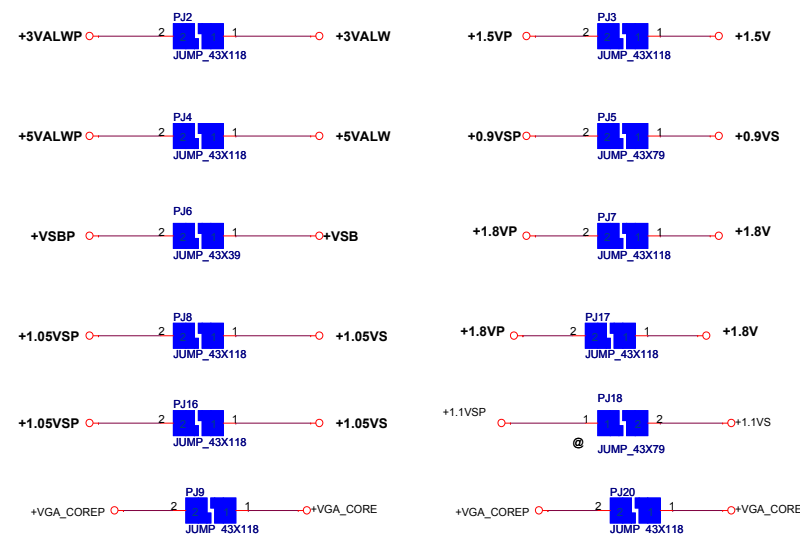
D4 USE
PJSOT24C 3P C/A SOT-23
SCA00000E00
24V



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								Size	Document Number	Rev
								Custom	KAL90KALH0	0.2
								Date:	Wednesday, December 24, 2008	Sheet 42 of 52

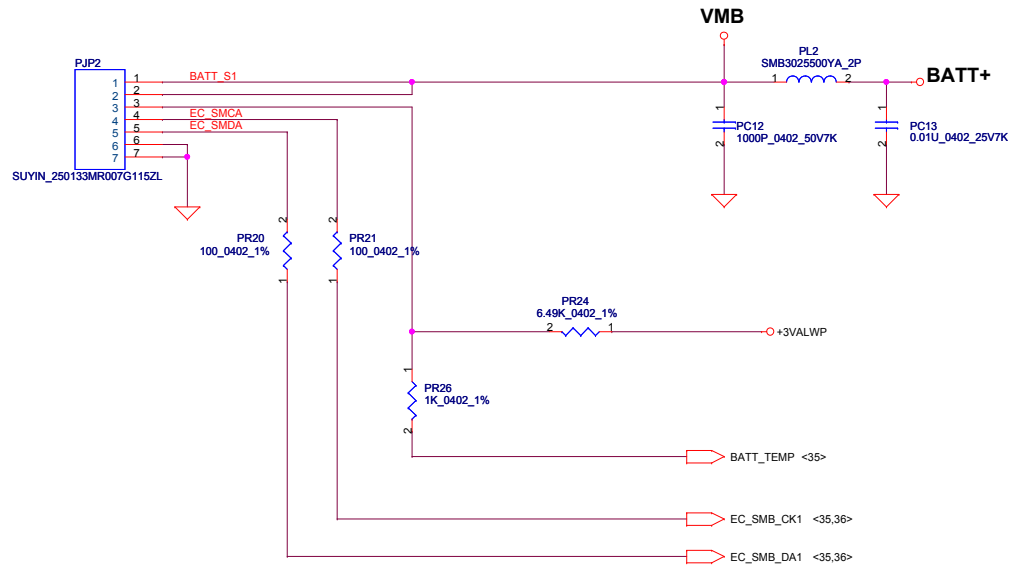


Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

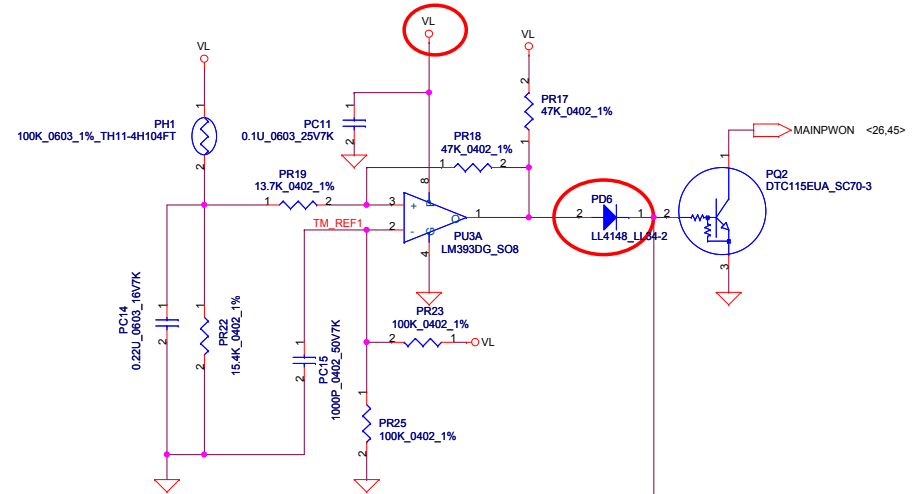


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Issued Date				2008/11/10				Title			
Deciphered Date				2008/11/17				DCIN & DETECTOR			
Size				Document Number				Rev			
Customer				KAL90KALH0				0.2			
Date				Tuesday, December 09, 2008				Sheet			
				43				of			
				52							

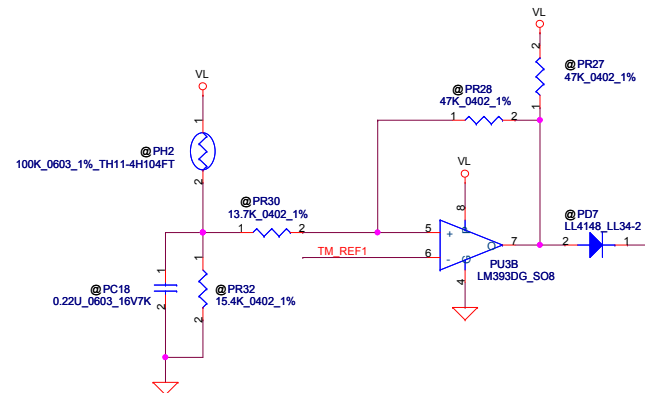
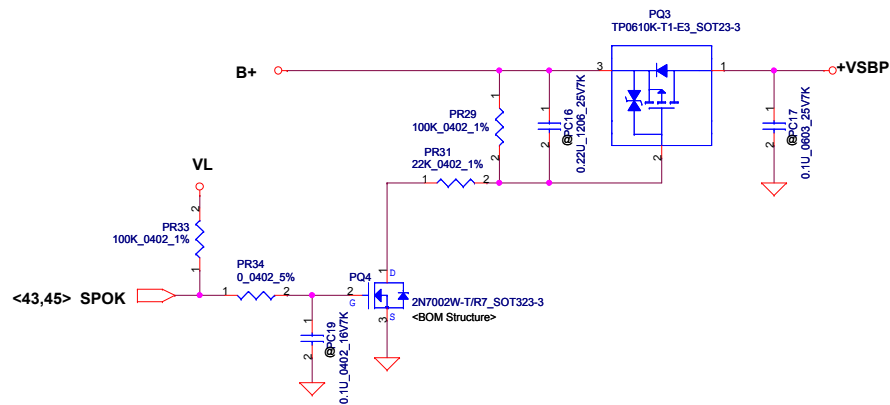
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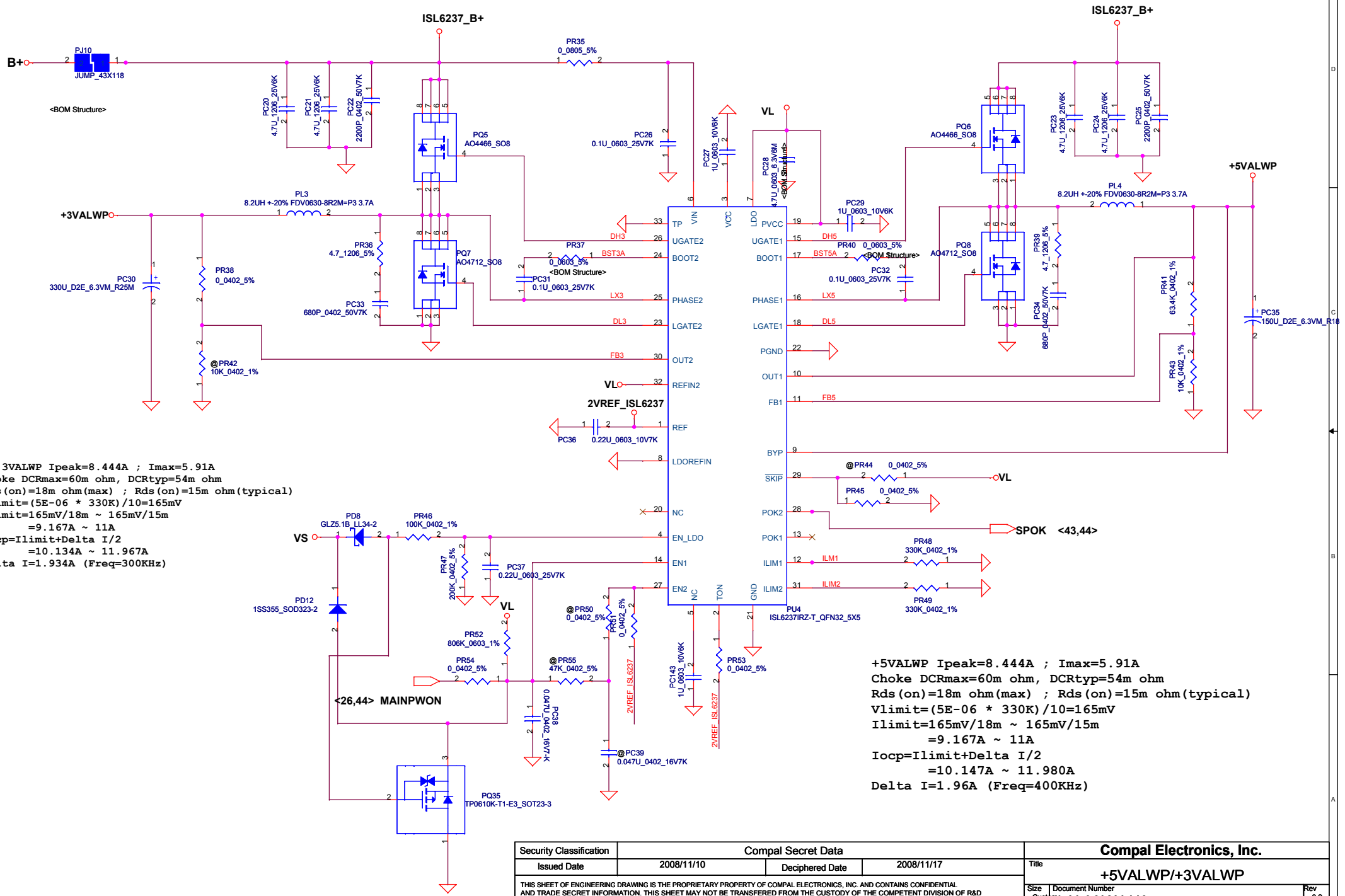
PH1 under CPU botten side :
CPU thermal protection at 96 degree C
Recovery at 60 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 47 degree C



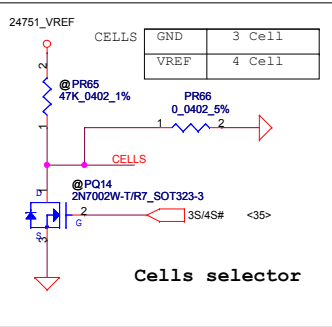
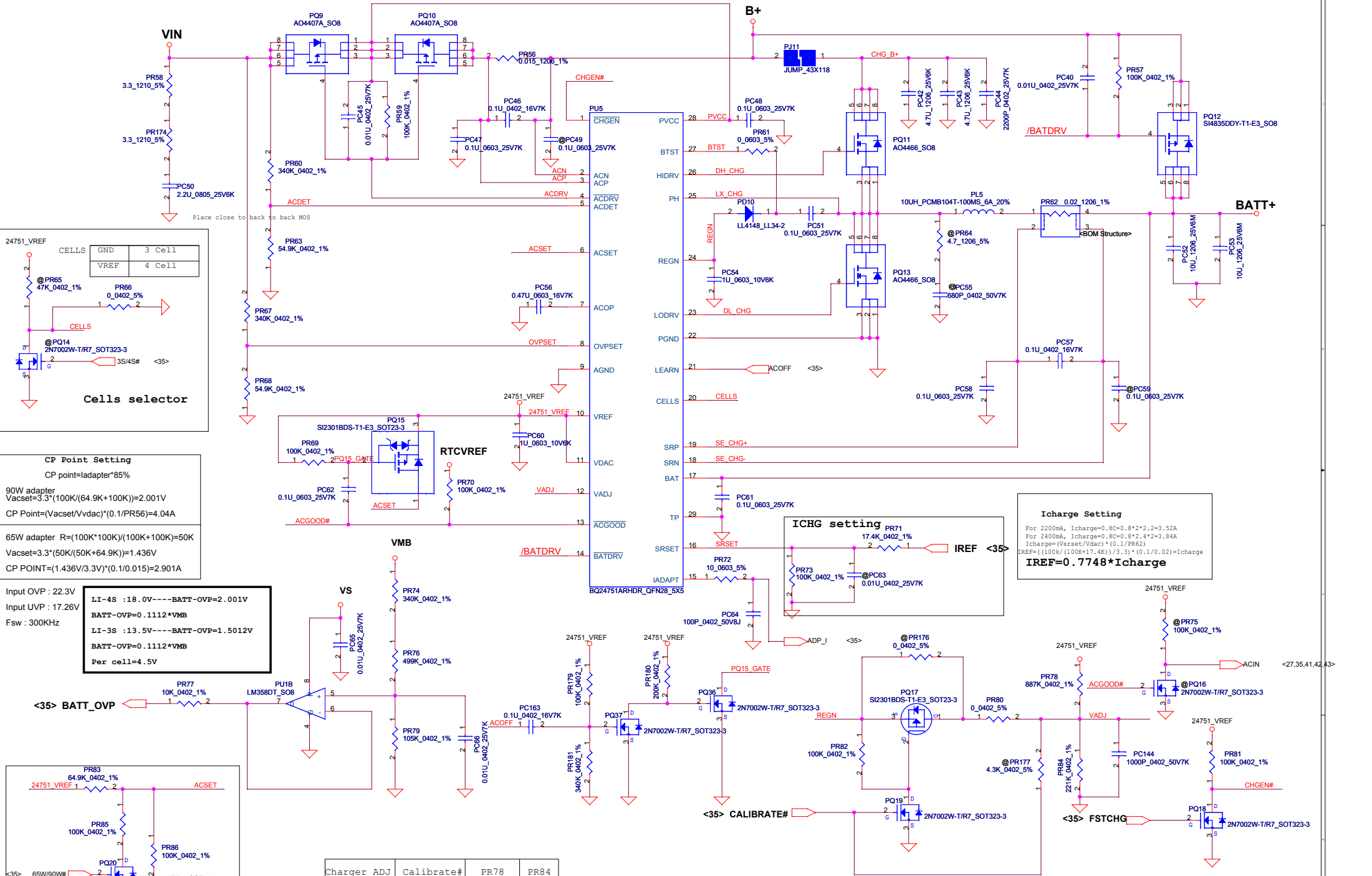
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Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title	
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Size	Document Number	Rev			0.2
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+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title	
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				Date	Thursday, November 20, 2008
				Sheet	45 of 52
				Rev	0.2



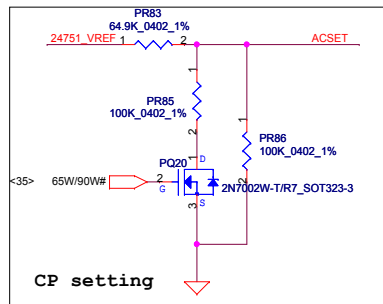
CP Point Setting
CP point=lapter*85%

90W adapter
 $V_{acset}=3.3 \cdot (100K/(64.9K+100K))=2.001V$
CP Point=(V_{acset}/V_{vdac})*(0.1/PR56)=4.04A

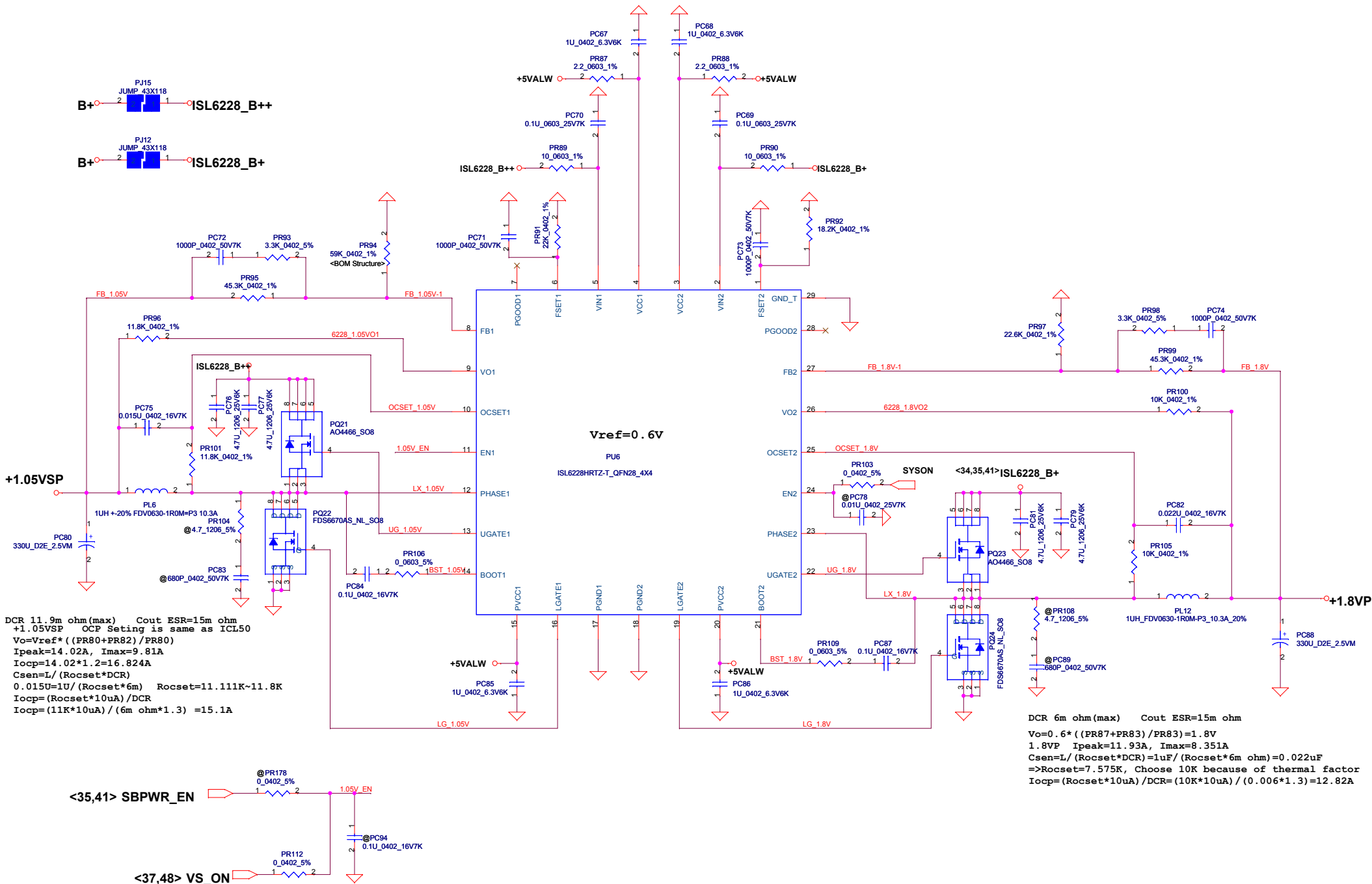
65W adapter $R=(100K \cdot 100K)/(100K+100K)=50K$
 $V_{acset}=3.3 \cdot (50K/(50K+64.9K))=1.436V$
CP POINT=($1.436V/3.3V$)*(0.1/0.015)=2.901A

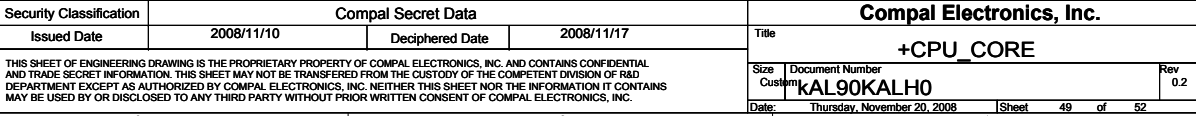
Input OVP : 22.3V
Input UVP : 17.26V
Fsw : 300KHz

LI-4S : 18.0V----BATT-OVP=2.001V
BATT-OVP=0.1112*VMB
LI-3S : 13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V



Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@





Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	cpu load line fail	Measure cpu load line can't fit spec	0.2	49	change the resistance value of pr173.from 4.42k to 3.83k	2008/08/08	DVT
2	Change resistance size	EMI request	0.2	49	Change pc116 and pc117 size from 0402 to 0603	2008/08/08	DVT
3	Change p-mos part number	Vender change EOL	0.2	46	PQ12 part number from 4835bdy to 483500y	2008/08/08	DVT
4	Change device size	device too large can't fit layout space	0.2	44-50	PQ4, PQ14, PQ16, PQ18, PQ19, PQ20, PQ27, PQ36, PQ37, PQ41, PQ42 change to sot323-3	2008/08/12	DVT
5	Change resistance value	1.05V tranient fail	0.2	47	PR94 from 60.4k to 59k	2008/08/12	DVT
6	change resistance	for hdmi	0.2	45	pr41 change from 61.3k to 63.4k	2008/08/14	DVT

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Issued Date		2008/11/10		Deciphered Date	
		2008/11/17		Title	
				PIR (PWR)	
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A --> C Change List

1120-----
Page 35,Chang
R1745,R1746 to 4.7K SD028470180

1120-----
Page 36,Add
R106,R109,R1846,R1847 to 0R

1120-----
Page 37,Add
R1845 to 10K

1120-----
Page 37,Add
R49 to 1K, JP24 to ACES_88266_02001

1217-----
Page 42,Delete
R1814,R1815,R1816,R1817,R1818,R1819

0106-----
Page 39, Delete D63 for Microsoft certification;
Page 36, Delelte R1773, modify value or R1774, R1775 for LED color.

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Issued Date	2008/11/10	Deciphered Date	2008/11/17	Title	HW PIR1
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				Date	Tuesday, January 06, 2009
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