

Compal Confidential

HCW51 Schematics Document

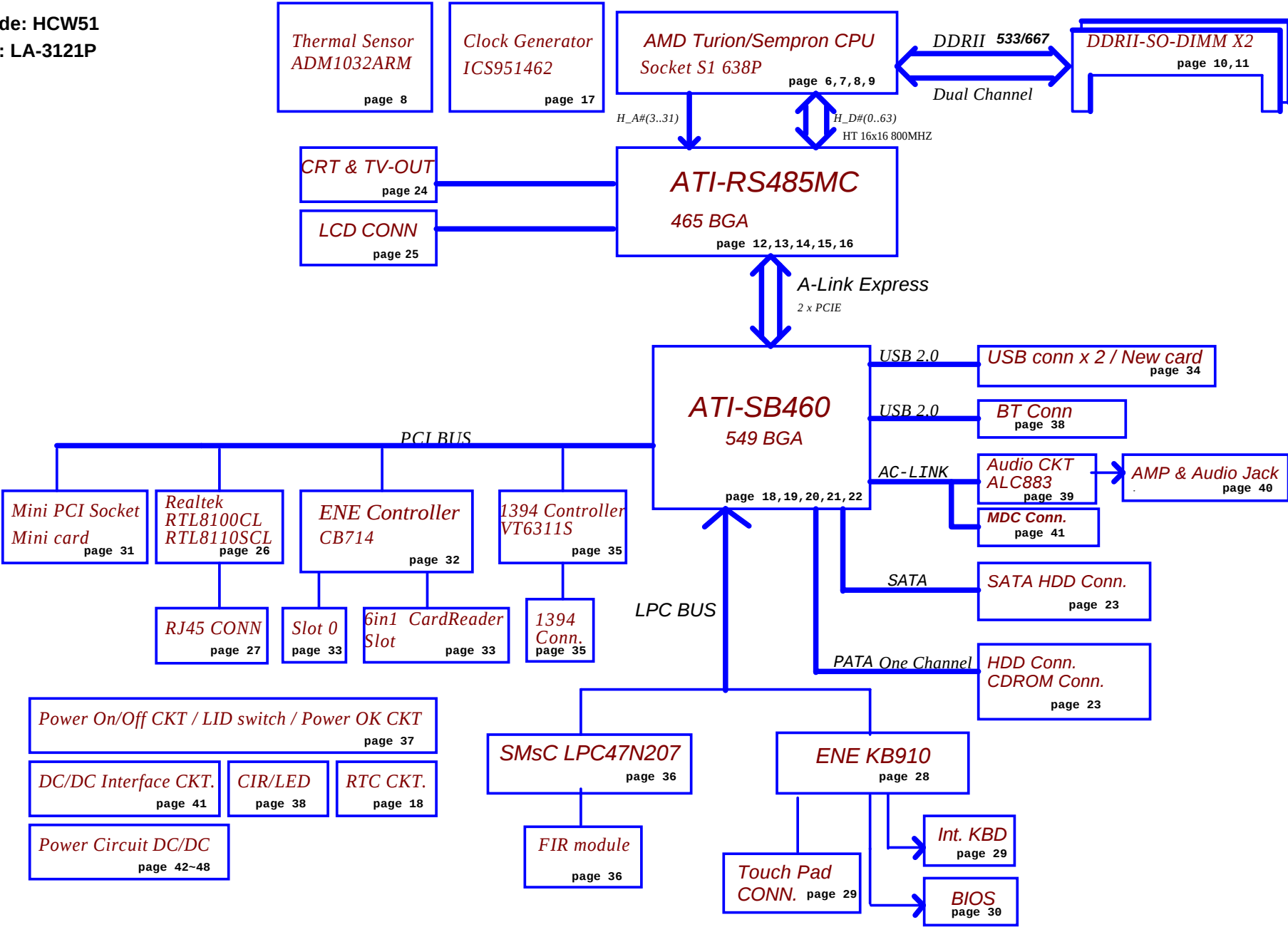
AMD/Sempron/ATI RS485MC/SB460

2006 / 04 / 27 Rev:1.0 FOR MP

Security Classification		Compal Secret Data		Compal Electronics, inc.	
Issued Date	2005/05/09	Deciphered Date	2006/03/08	Title	SCHEMATIC, M/B LA-3121P
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Project Code: HCW51
File Name : LA-3121P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.2VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VS	VS always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		
(24C04)	1011 000X b		

EC SM Bus2 address

SB460 SM Bus address

Device	Address
Clock Generator (ICS951462)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	UMA
1	DISCRETE
2	
3	
4	
5	
6	
7	

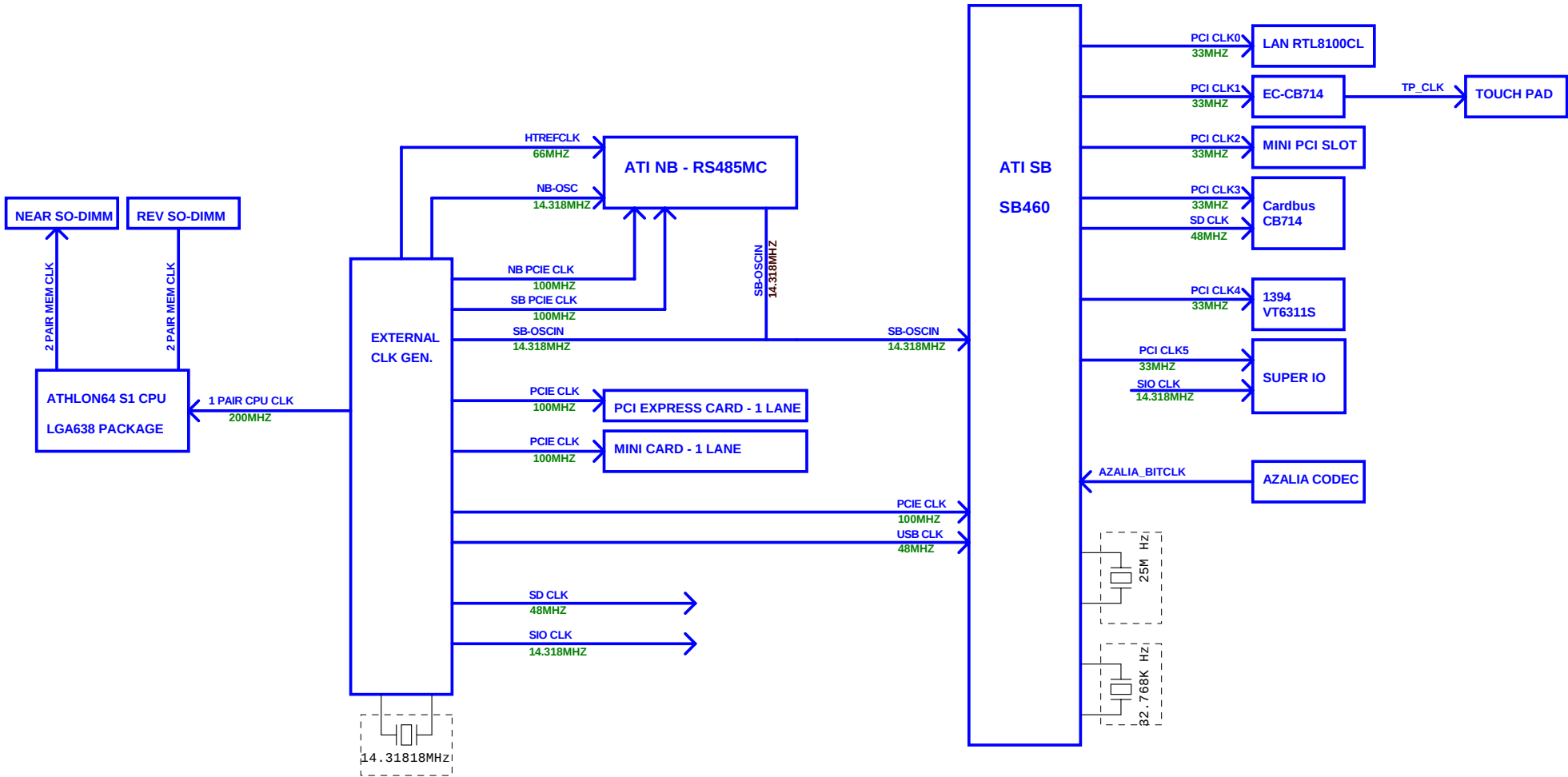
BTO Option Table

BTO Item	BOM Structure
WITH TV-OUT	TV@
WITH FIR	FIR@
WITH CARD READER	61@
WITH 1394	1394@
WITH EXPRESS CARD	EXPRESS@
WITH CIR	CIR@
WITH LAN(10/100)	100@
WITH LAN(10/100/1000)	GIGA@
WITH GIGA LAN(8110SBL)	8110SB@
WITH GIGA LAN(8110SCL)	8110SC@
WITH PATA HDD	PATA@
WITH SATA HDD	SATA@
WITH BLUETOOTH	BT@
WITH USBx2	USB2@
WITH LPC47N207	SI01@
WITH SI01036	SI02@
WITH SI0 BOTH	SI0ALL@
WITH SSC	SPREAD@
W/O SSC	NOSPREAD@
DIP CAP	45@

SKU ID Table

SKU ID	SKU
0	W/O SATA
1	WITH SATA
2	
3	
4	
5	
6	
7	

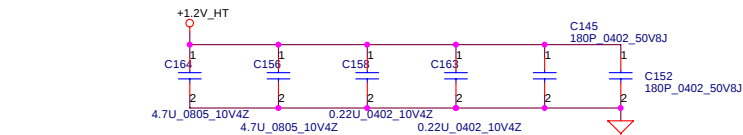
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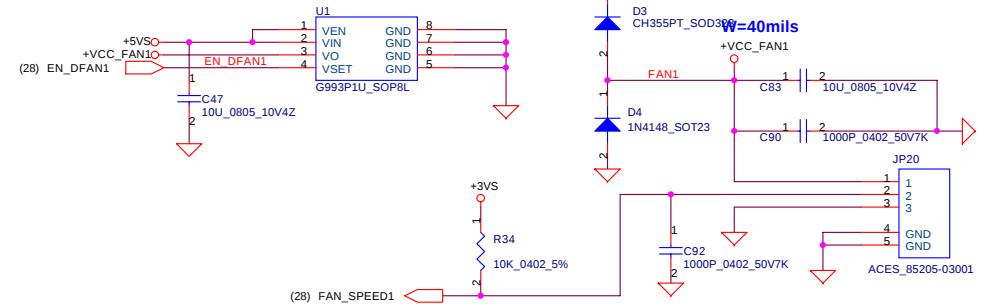
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VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY
TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY
TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



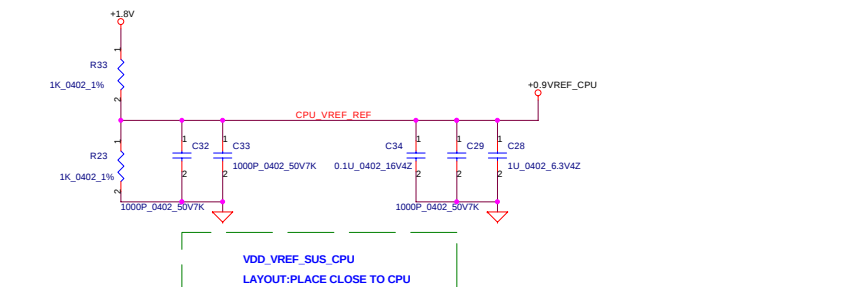
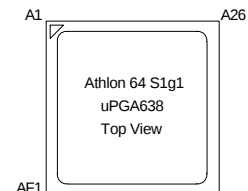
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JP23C

(11) DDR_B_DM[3..0]	DDR_B_D03	AD11	MA_DAT663	AA12	DDR_A_D03	DDR_A_DM[3..0] (10)
	DDR_B_D02	AE11	MA_DAT662	AA12	DDR_A_D02	
	DDR_B_D01	AE14	MA_DAT661	AA14	DDR_A_D01	
	DDR_B_D00	AE14	MA_DAT660	AA14	DDR_A_D00	
	DDR_B_D59	Y11	MA_DAT659	W11	DDR_A_D59	
	DDR_B_D58	AE11	MA_DAT658	Y12	DDR_A_D58	
	DDR_B_D57	AE11	MA_DAT657	C13	DDR_A_D57	
	DDR_B_D56	AE13	MA_DAT656	AB13	DDR_A_D56	
	DDR_B_D55	AE15	MA_DAT655	AD15	DDR_A_D55	
	DDR_B_D54	AE16	MA_DAT654	AB15	DDR_A_D54	
	DDR_B_D53	AC18	MA_DAT653	AB17	DDR_A_D53	
	DDR_B_D52	AE19	MA_DAT652	Y17	DDR_A_D52	
	DDR_B_D51	AD14	MA_DAT651	Y14	DDR_A_D51	
	DDR_B_D50	AC14	MA_DAT650	W16	DDR_A_D50	
	DDR_B_D49	AE10	MA_DAT649	AD17	DDR_A_D49	
	DDR_B_D48	AD18	MA_DAT648	Y18	DDR_A_D48	
	DDR_B_D47	AD20	MA_DAT647	AD18	DDR_A_D47	
	DDR_B_D46	AC20	MA_DAT646	AD21	DDR_A_D46	
	DDR_B_D45	AE23	MA_DAT645	AB21	DDR_A_D45	
	DDR_B_D44	AE24	MA_DAT644	AB18	DDR_A_D44	
	DDR_B_D43	AE20	MA_DAT643	AB18	DDR_A_D43	
	DDR_B_D42	AE20	MA_DAT642	AA20	DDR_A_D42	
	DDR_B_D41	AC22	MA_DAT641	Y20	DDR_A_D41	
	DDR_B_D40	AC22	MA_DAT640	AA22	DDR_A_D40	
	DDR_B_D39	AE23	MA_DAT639	Y22	DDR_A_D39	
	DDR_B_D38	AD26	MA_DAT638	W21	DDR_A_D38	
	DDR_B_D37	AA25	MA_DAT637	C22	DDR_A_D37	
	DDR_B_D36	AA26	MA_DAT636	AA21	DDR_A_D36	
	DDR_B_D35	AE24	MA_DAT635	AA21	DDR_A_D35	
	DDR_B_D34	AD24	MA_DAT634	AB22	DDR_A_D34	
	DDR_B_D33	AA23	MA_DAT633	B24	DDR_A_D33	
	DDR_B_D32	AA24	MA_DAT632	Y24	DDR_A_D32	
	DDR_B_D31	CA4	MA_DAT631	CA4	DDR_A_D31	
	DDR_B_D30	CA3	MA_DAT630	E20	DDR_A_D30	
	DDR_B_D29	D26	MA_DAT629	E22	DDR_A_D29	
	DDR_B_D28	C26	MA_DAT628	E21	DDR_A_D28	
	DDR_B_D27	G26	MA_DAT627	J19	DDR_A_D27	
	DDR_B_D26	G25	MA_DAT626	H24	DDR_A_D26	
	DDR_B_D25	E24	MA_DAT625	E23	DDR_A_D25	
	DDR_B_D24	E23	MA_DAT624	E20	DDR_A_D24	
	DDR_B_D23	CA4	MA_DAT623	C23	DDR_A_D23	
	DDR_B_D22	B24	MA_DAT622	B22	DDR_A_D22	
	DDR_B_D21	C20	MA_DAT621	F18	DDR_A_D21	
	DDR_B_D20	B20	MA_DAT620	F18	DDR_A_D20	
	DDR_B_D19	C25	MA_DAT619	E20	DDR_A_D19	
	DDR_B_D18	D24	MA_DAT618	D22	DDR_A_D18	
	DDR_B_D17	CA2	MA_DAT617	C19	DDR_A_D17	
	DDR_B_D16	D20	MA_DAT616	G18	DDR_A_D16	
	DDR_B_D15	D18	MA_DAT615	G17	DDR_A_D15	
	DDR_B_D14	C18	MA_DAT614	C17	DDR_A_D14	
	DDR_B_D13	D14	MA_DAT613	F14	DDR_A_D13	
	DDR_B_D12	C14	MA_DAT612	F14	DDR_A_D12	
	DDR_B_D11	A20	MA_DAT611	H17	DDR_A_D11	
	DDR_B_D10	A19	MA_DAT610	E17	DDR_A_D10	
	DDR_B_D09	A16	MA_DAT609	E15	DDR_A_D09	
	DDR_B_D08	A15	MA_DAT608	H15	DDR_A_D08	
	DDR_B_D07	A13	MA_DAT607	E13	DDR_A_D07	
	DDR_B_D06	D12	MA_DAT606	C13	DDR_A_D06	
	DDR_B_D05	E11	MA_DAT605	H12	DDR_A_D05	
	DDR_B_D04	G11	MA_DAT604	H11	DDR_A_D04	
	DDR_B_D03	B14	MA_DAT603	G14	DDR_A_D03	
	DDR_B_D02	A14	MA_DAT602	H14	DDR_A_D02	
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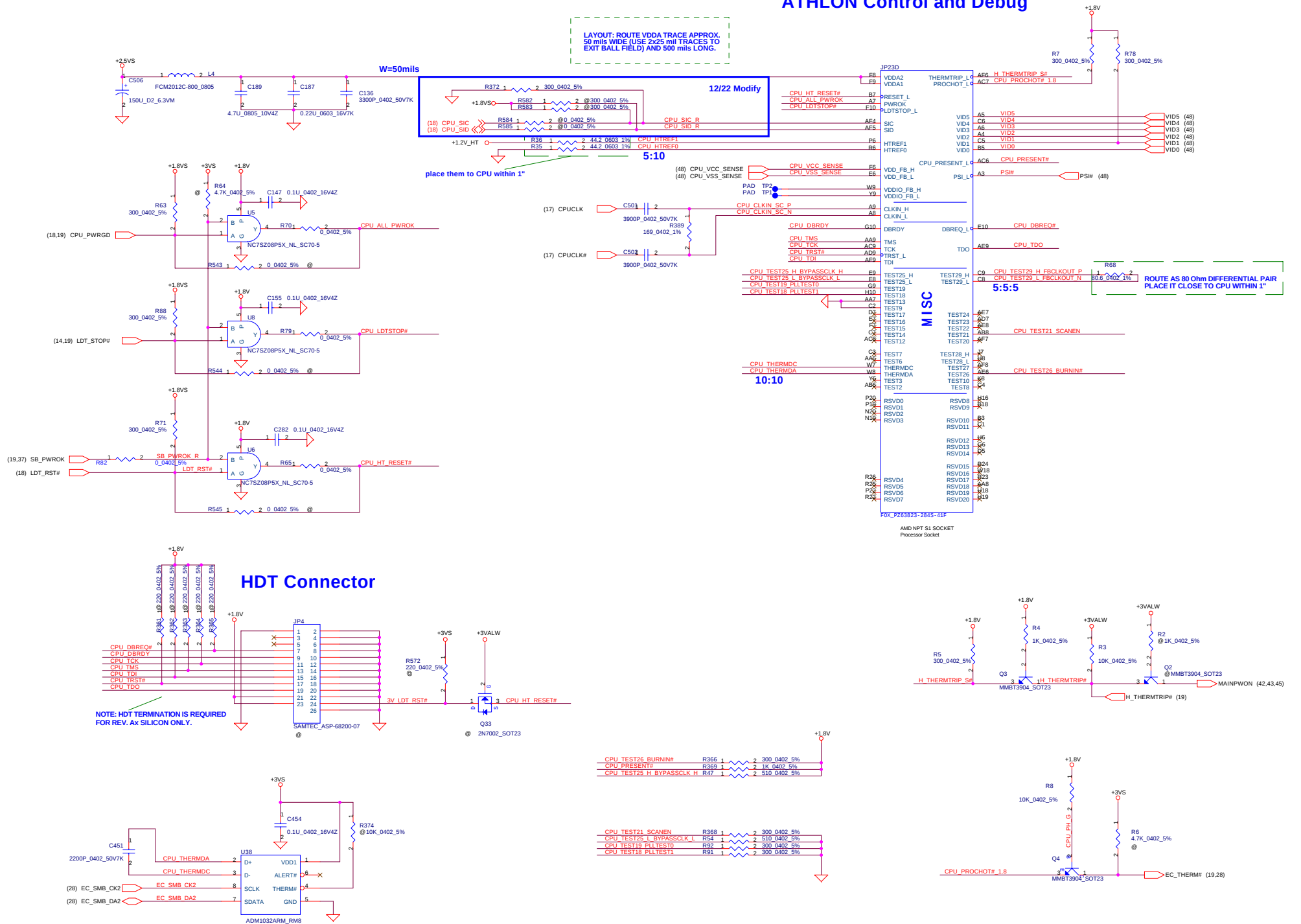
DDR I Data

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	DDR_B_DM5	AE22 <td>MA_DM5</td> <td>MA_DM5</td> <td>Y19</td> <td>DDR_A</td>	MA_DM5	MA_DM5	Y19	DDR_A

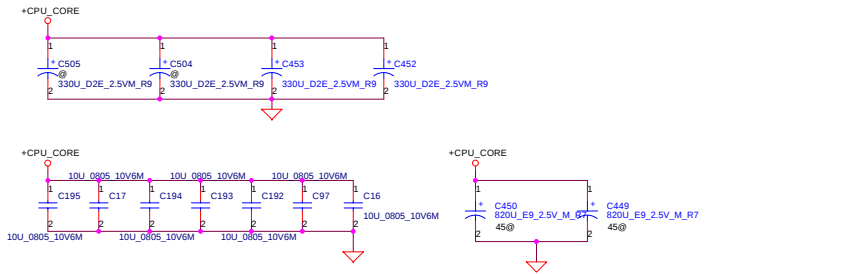
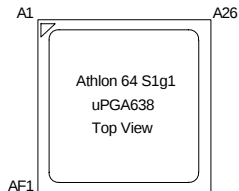
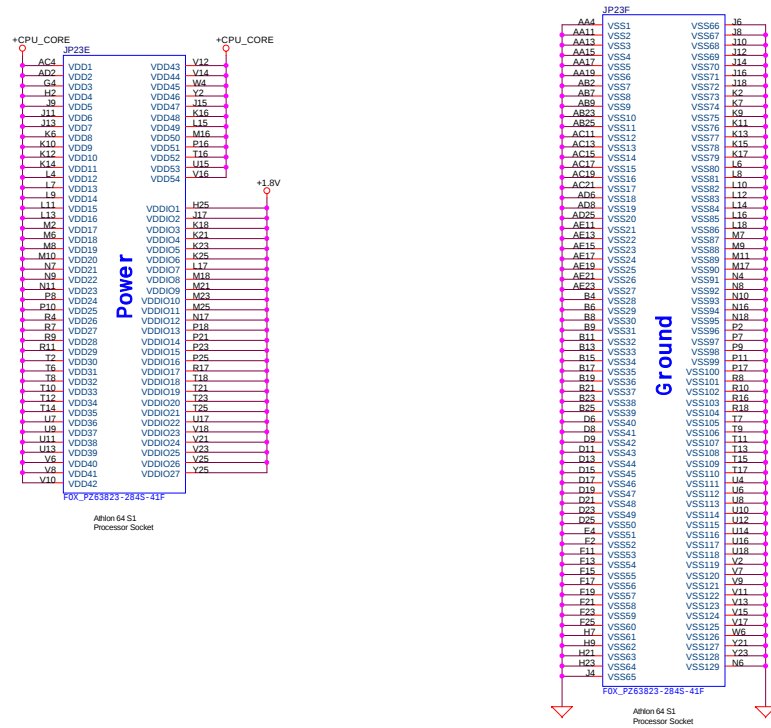


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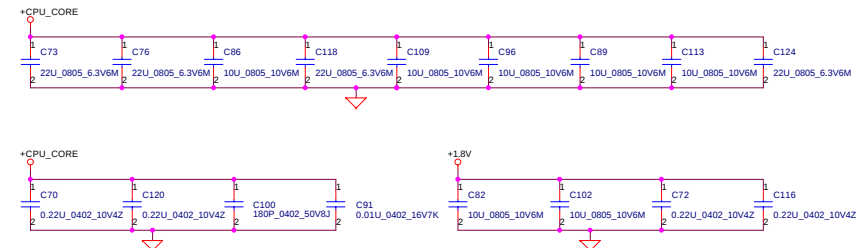
ATHLON Control and Debug



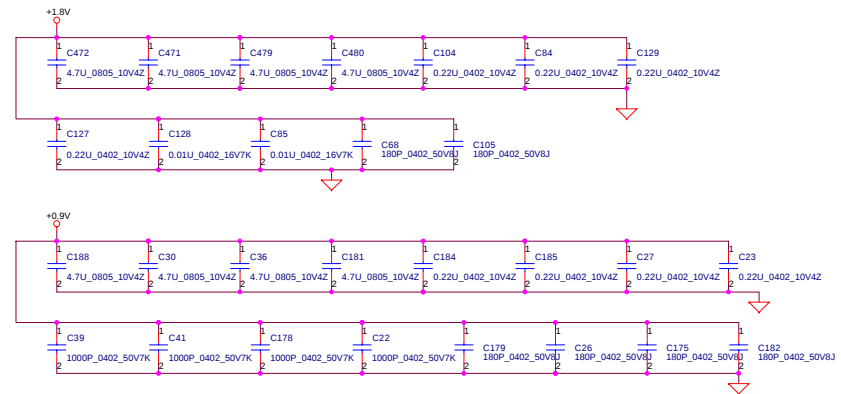
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CPU SOCKET S1 DECOUPLING

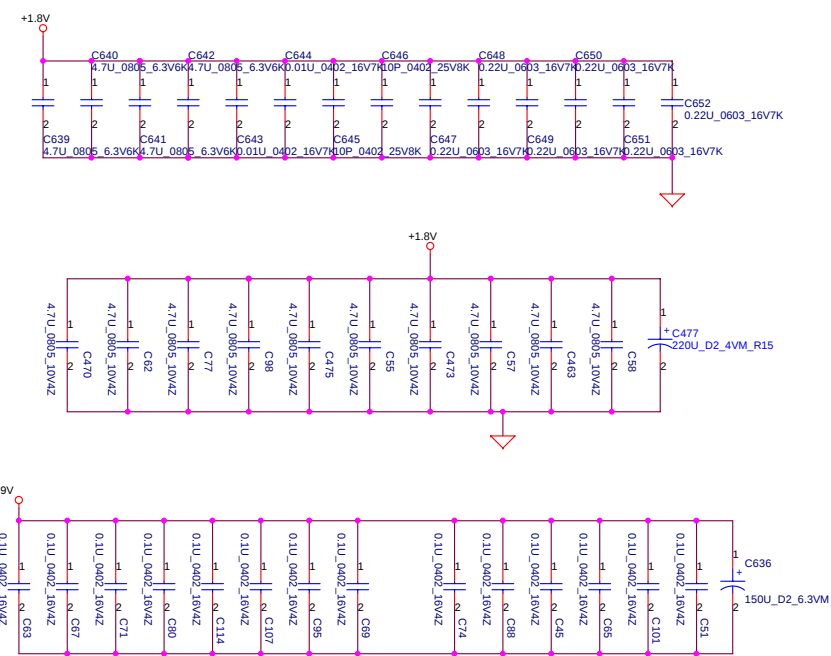
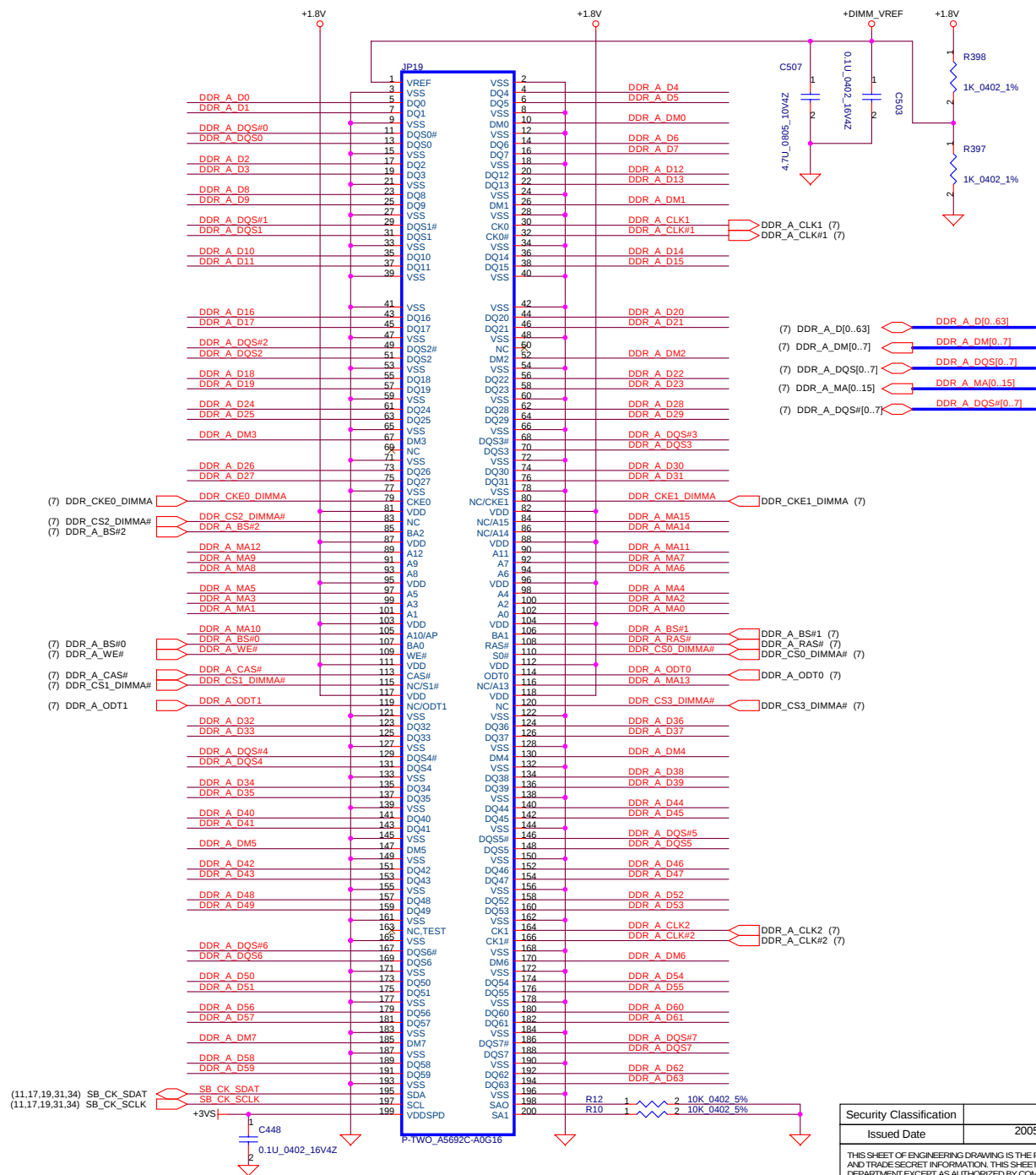


DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE

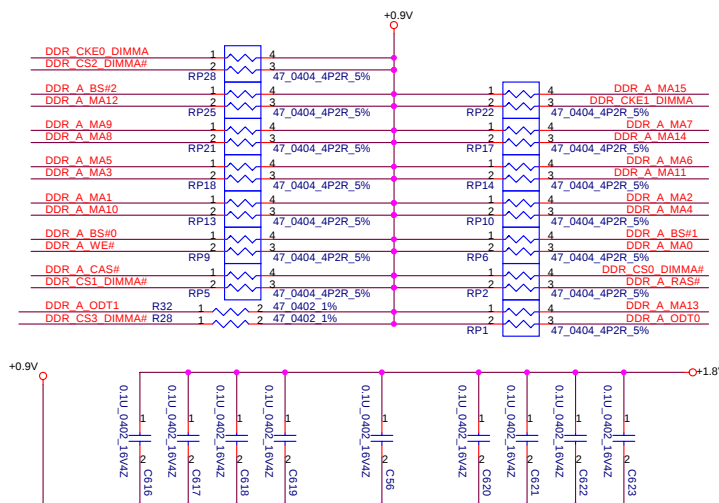


PROCESSOR POWER AND GROUND

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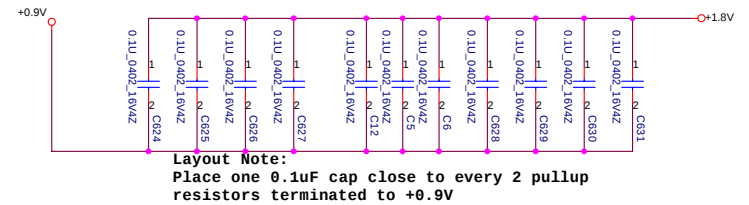
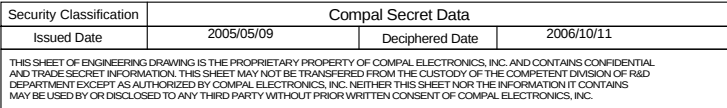


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V

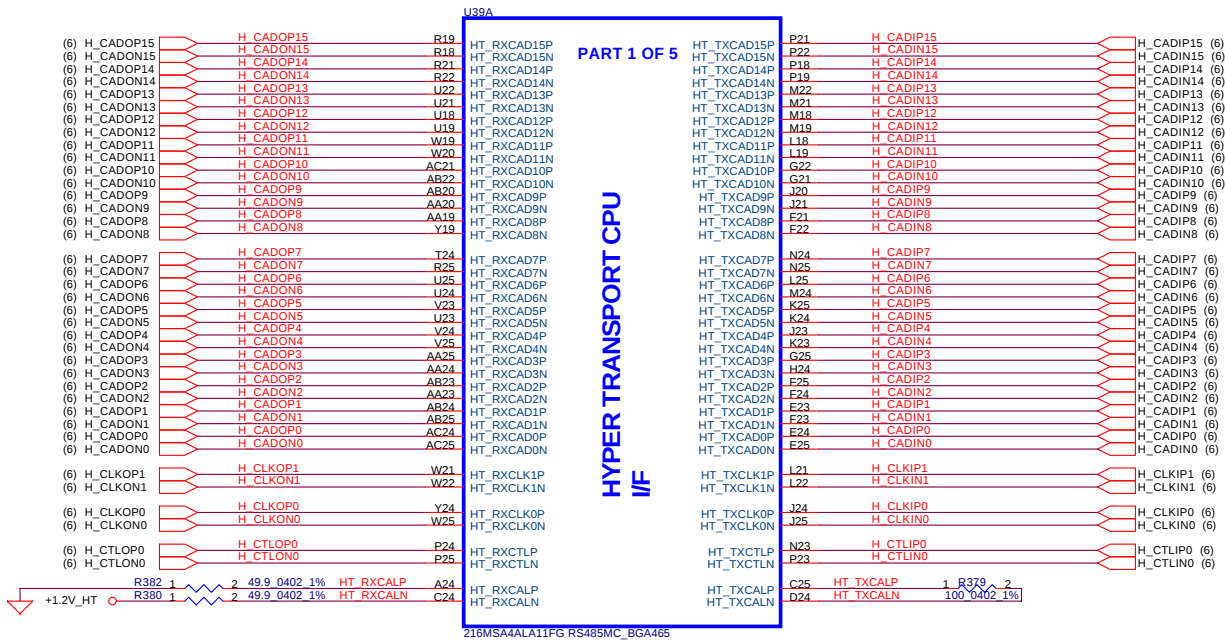


Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

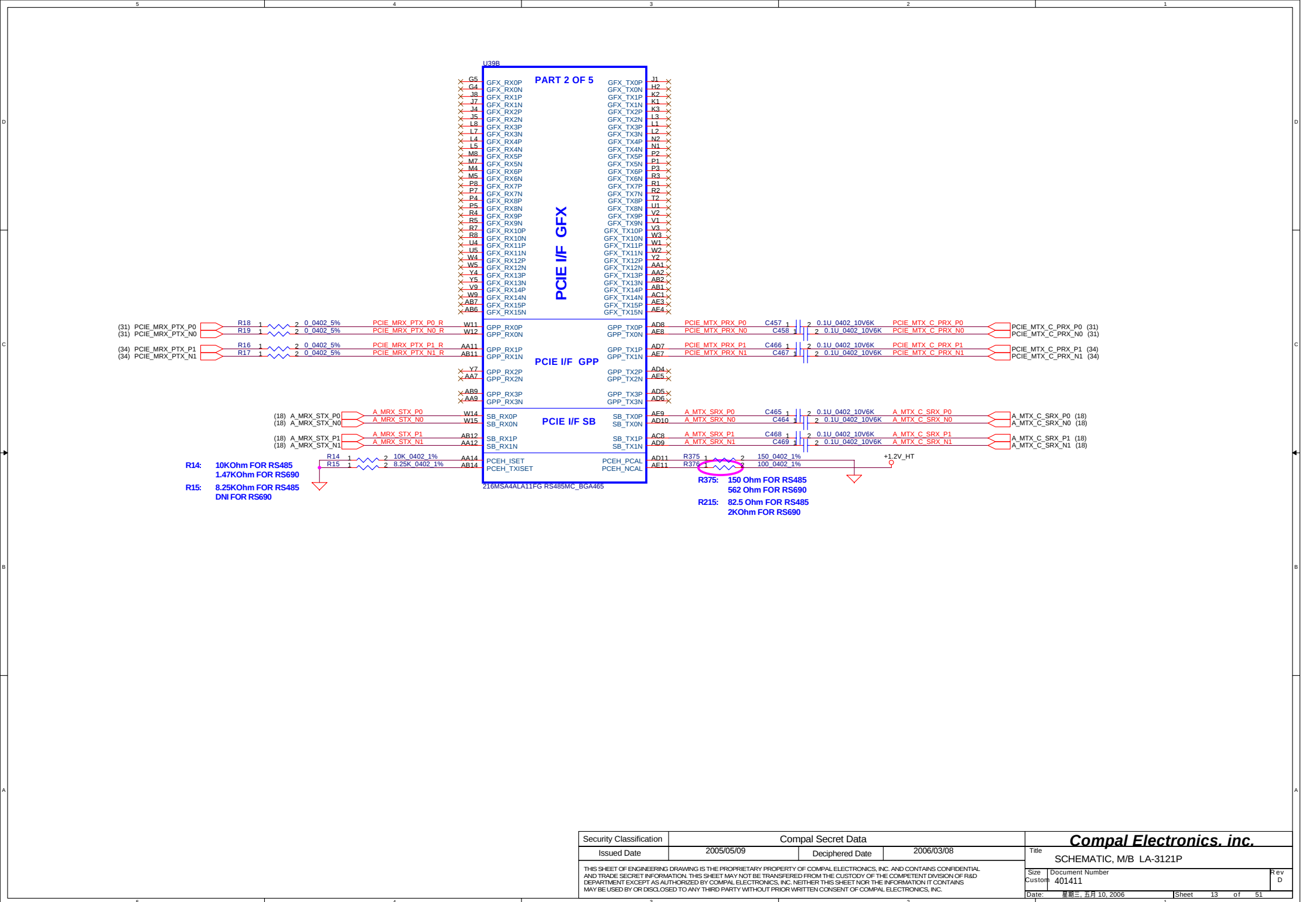
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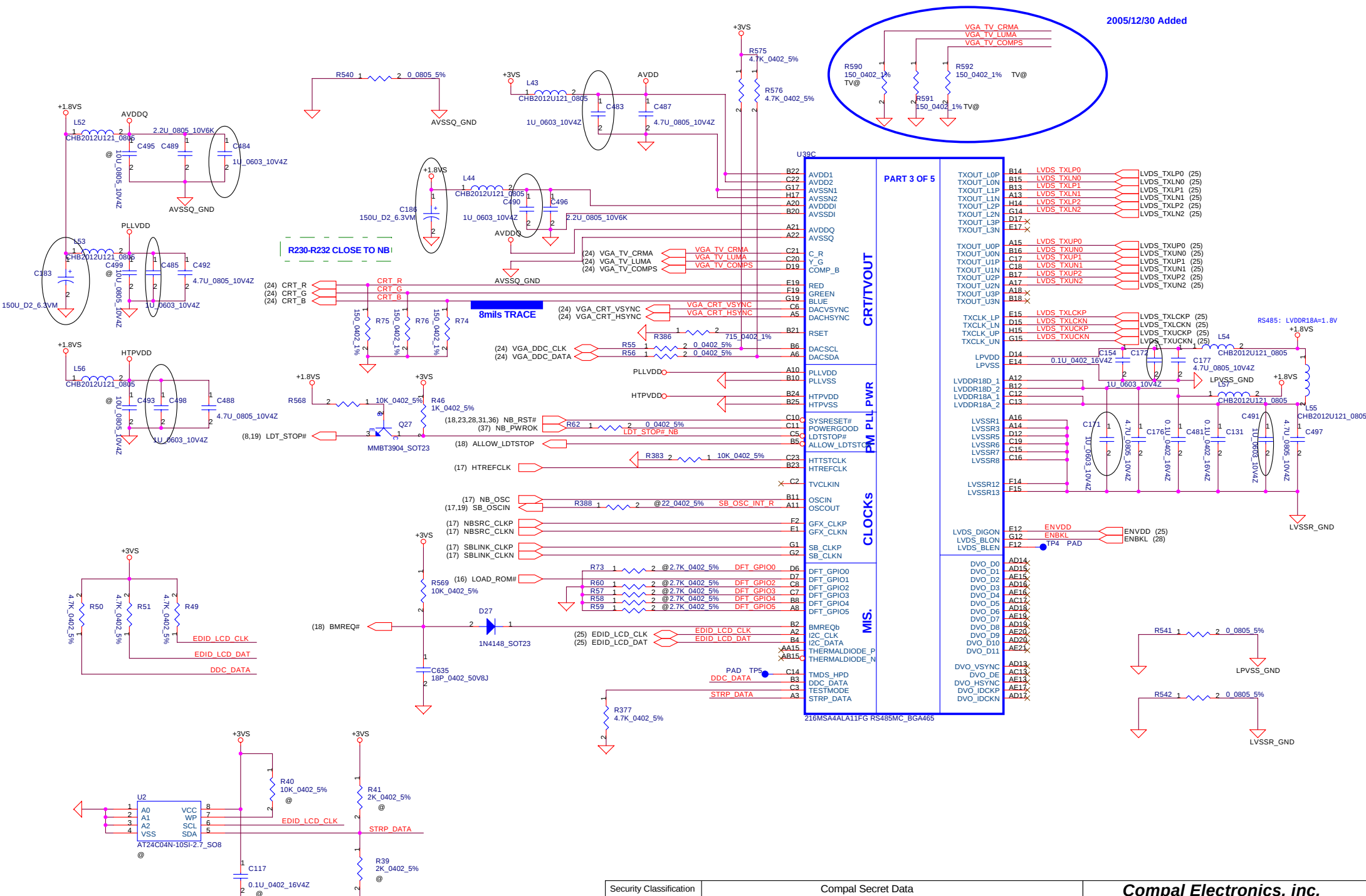


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2005/12/30 Added

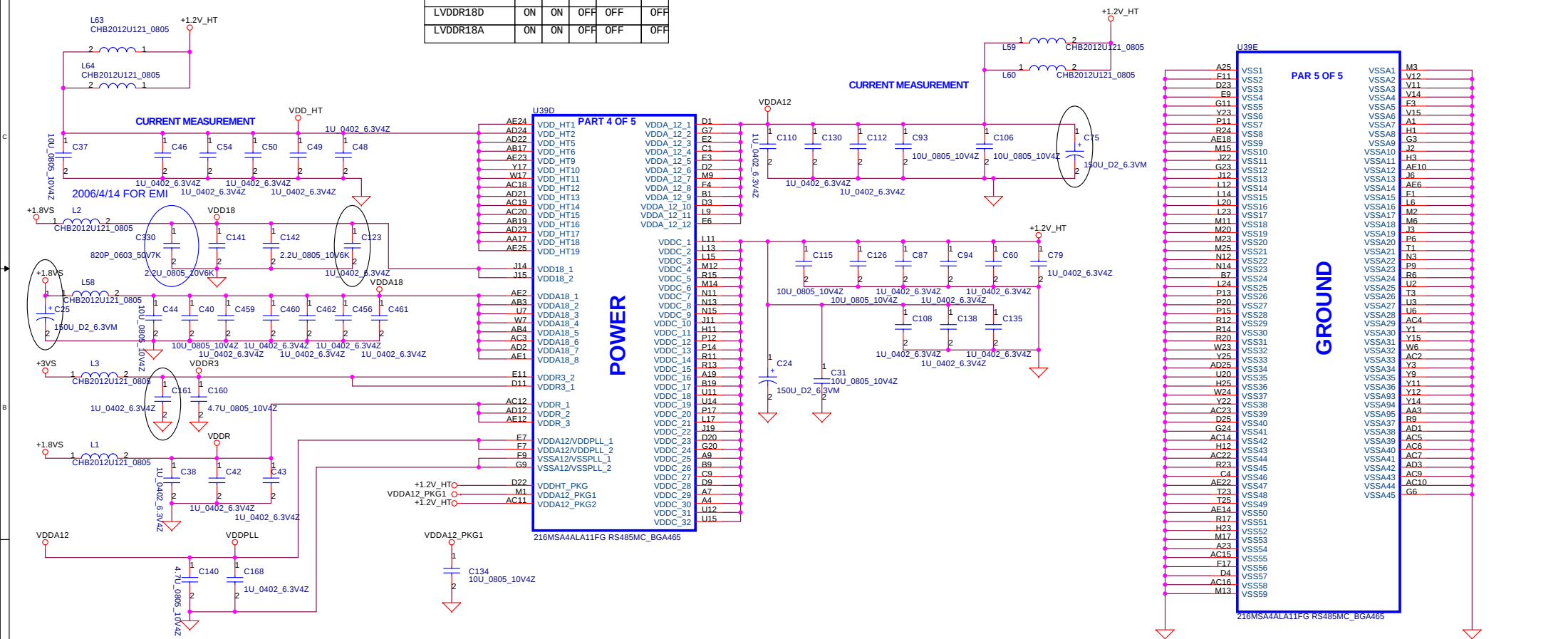


NOTE: ACCESS TO STRAP_DATA AND I2C_CLK PINS IS MANDATORY.

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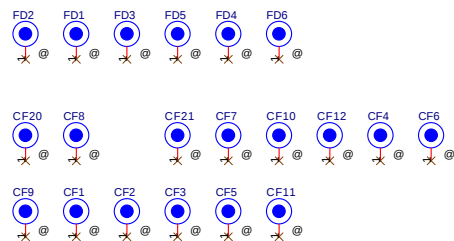
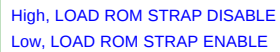
NB RS485 POWER STATES

Power	Signal	S0	S1	S3	S4/S5	G3
VDDHT		ON	ON	OFF	OFF	OFF
VDDR		ON	ON	OFF	OFF	OFF
VDD18		ON	ON	OFF	OFF	OFF
VDDC		ON	ON	OFF	OFF	OFF
VDDA18		ON	ON	OFF	OFF	OFF
VDDA12		ON	ON	OFF	OFF	OFF
AVDD		ON	ON	OFF	OFF	OFF
AVDDDI		ON	ON	OFF	OFF	OFF
PLLVDD		ON	ON	OFF	OFF	OFF
HTPVDD		ON	ON	OFF	OFF	OFF
VDDR3		ON	ON	OFF	OFF	OFF
LPVDD		ON	ON	OFF	OFF	OFF
LVDDR18D		ON	ON	OFF	OFF	OFF
LVDDR18A		ON	ON	OFF	OFF	OFF



RS485: 0 Ohm RESISTOR
RS690: 220 Ohm 500mA FERRITE BEAD

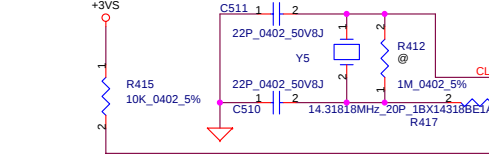
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- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Parallel Resonance Crystal

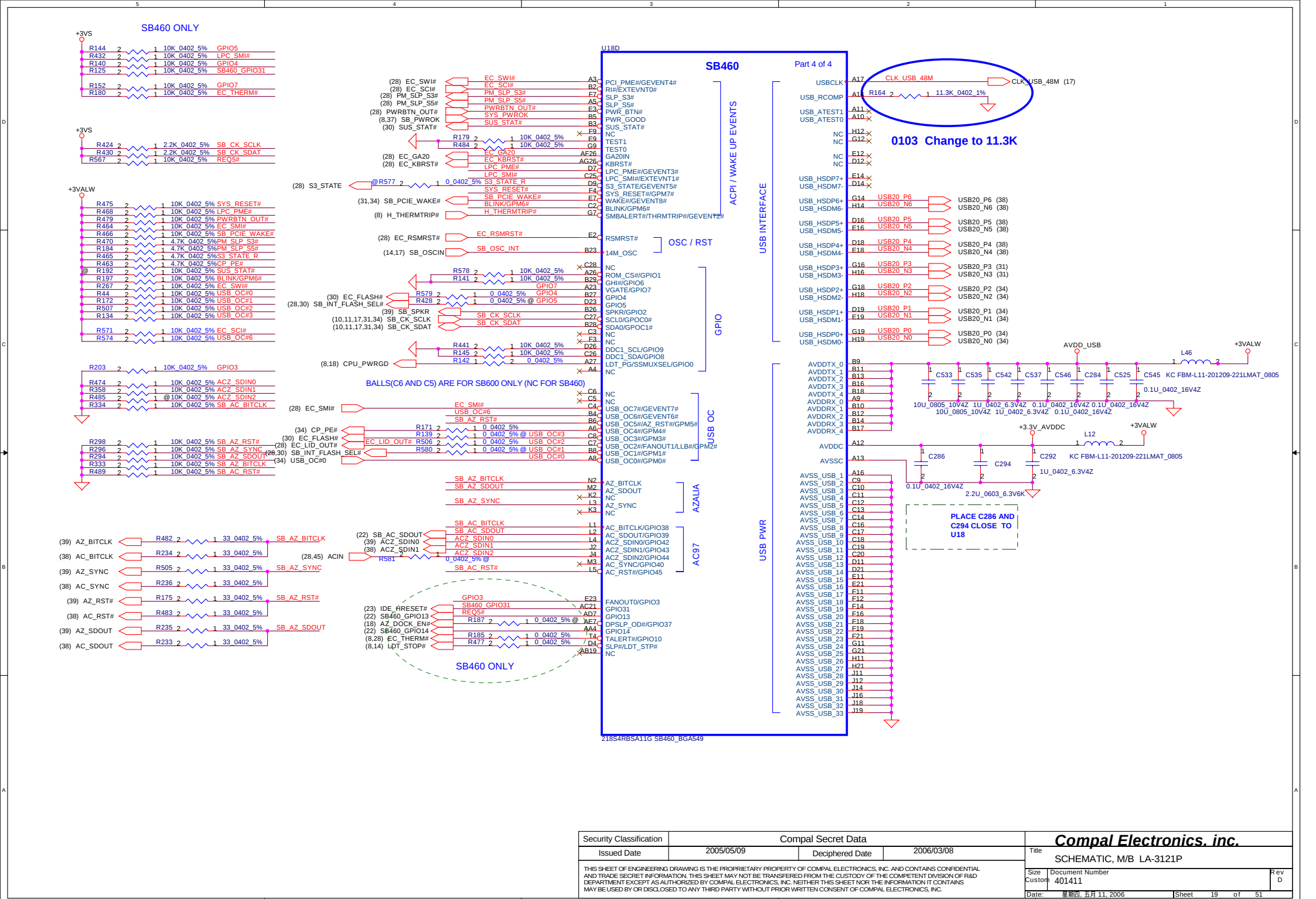


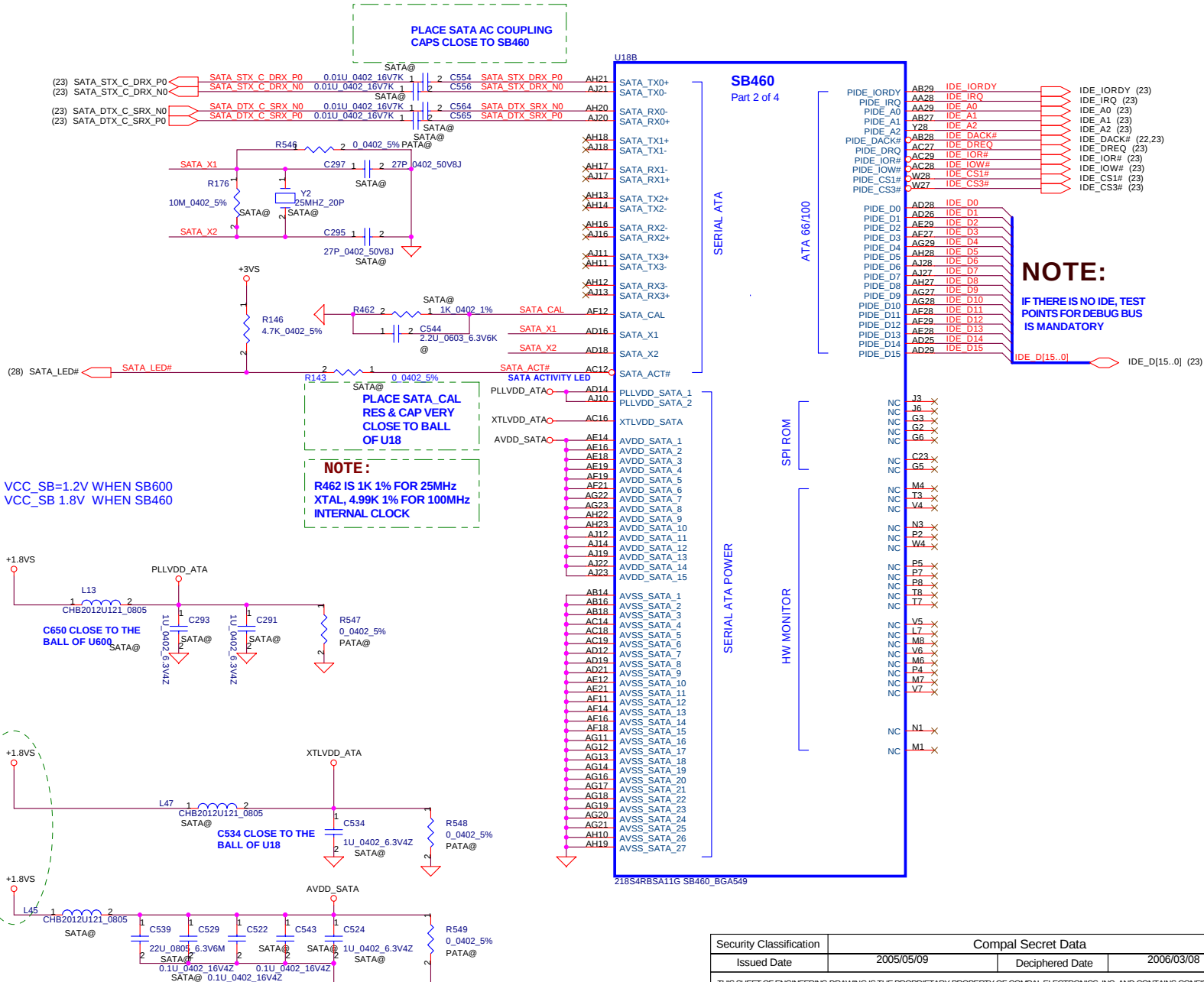
$I_{oh} = 5 * I_{ref}$
 $(2.32mA)$
 $V_{oh} = 0.71V @ 60 ohm$

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

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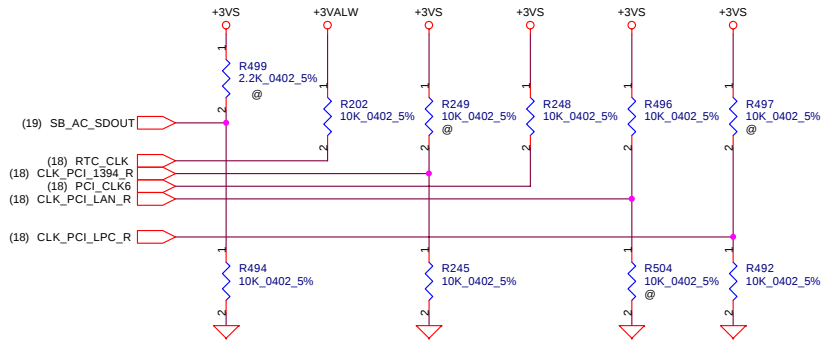




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REQUIRED STRAPS

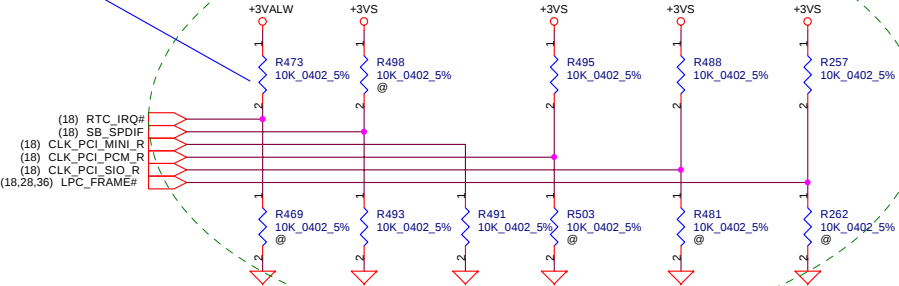
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED



	SB600				SB460	
	AC_SDOUT	RTC_CLK	PCI_1394_R	PCI_CLK6	PCI_LAN_R	PCI_LPC_R
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT	DEFAULT

NOTE: R751 PU RESISTOR FOR
RTC_IRQ# IS REQUIRED FOR SB600
TO KEEP THE INPUT FROM FLOATING.

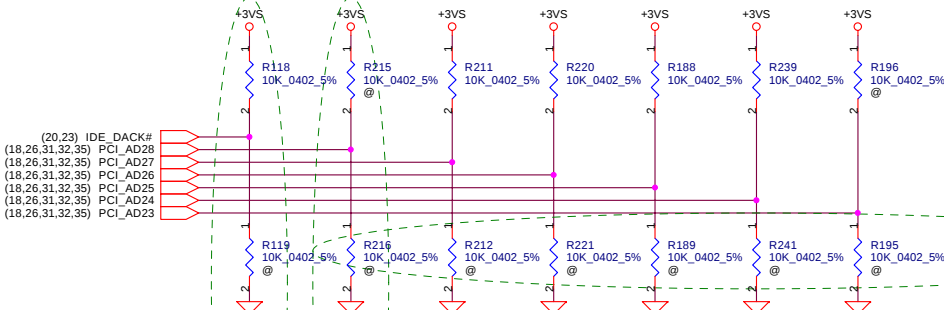
SB460 ONLY



	ACPWRON	SPDIF_OUT	PCI_MINI_R	PCI_PCM_R	PCI_SIO_R	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHZ	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHZ DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB460 ONLY

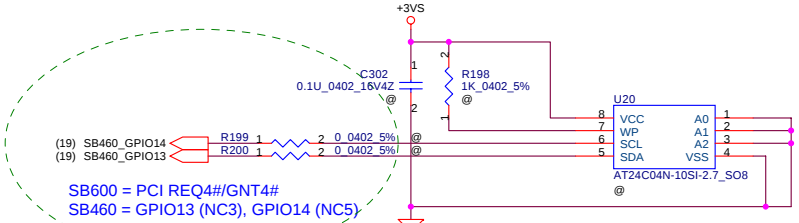
SB600 ONLY

SB600 ONLY

NOTE: FOR
SB460,
PCI_AD23 IS
RESERVED



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

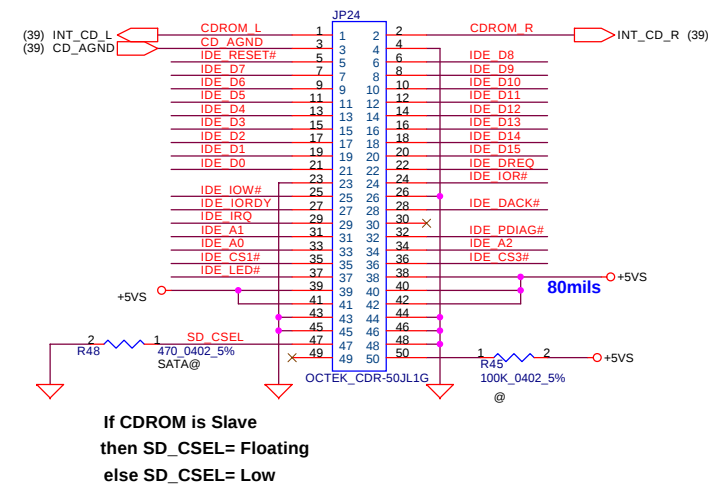


SB PCIE EEPROM STRAPS

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(20) IDE_D[0..15] IDE_D[0..15]

(20) IDE_A[0..2] IDE_A[0..2]

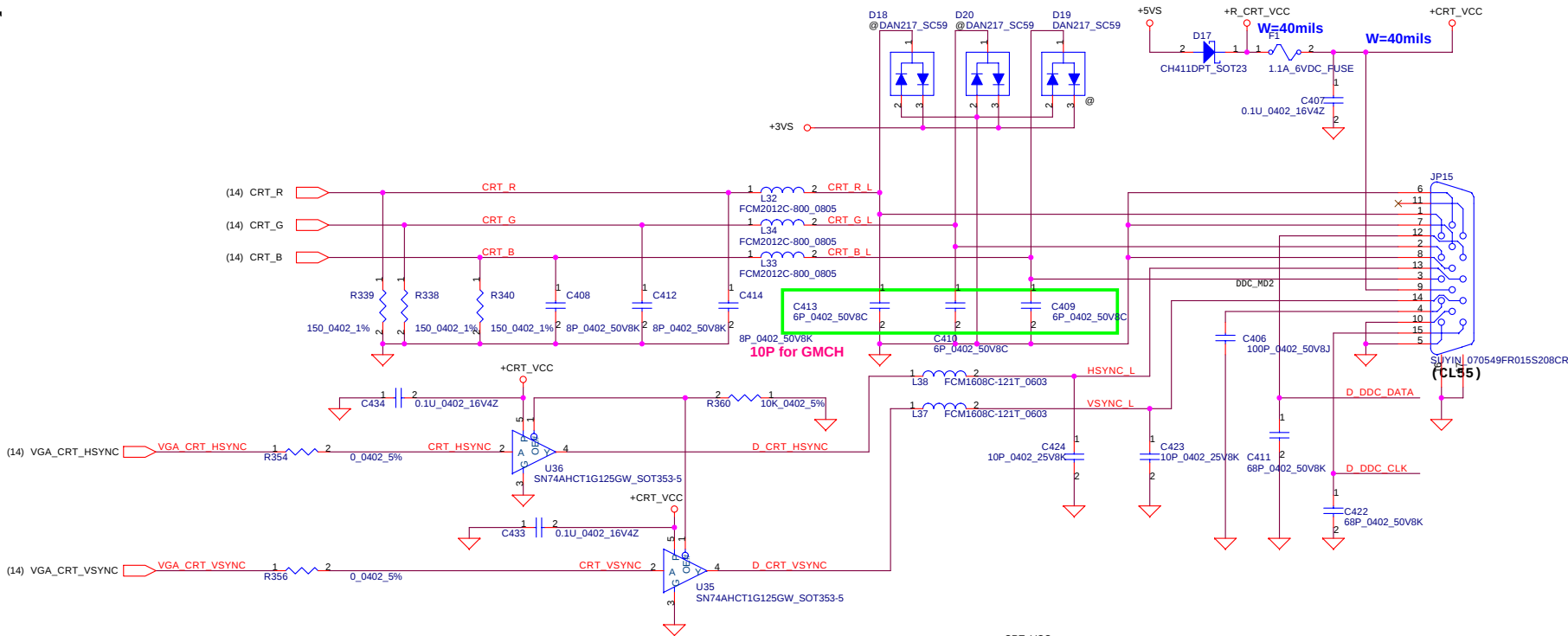


```

If CDROM is Slave
then SD_CSEL= Floating
else SD_CSEL= Low

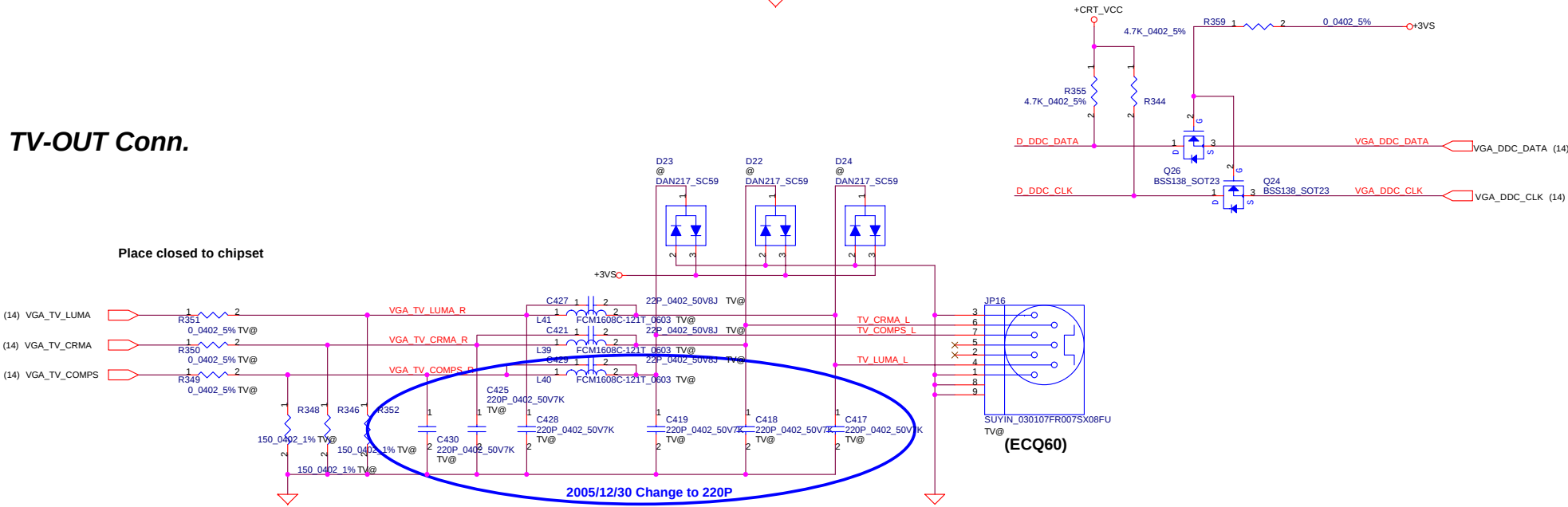
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CRT Connector



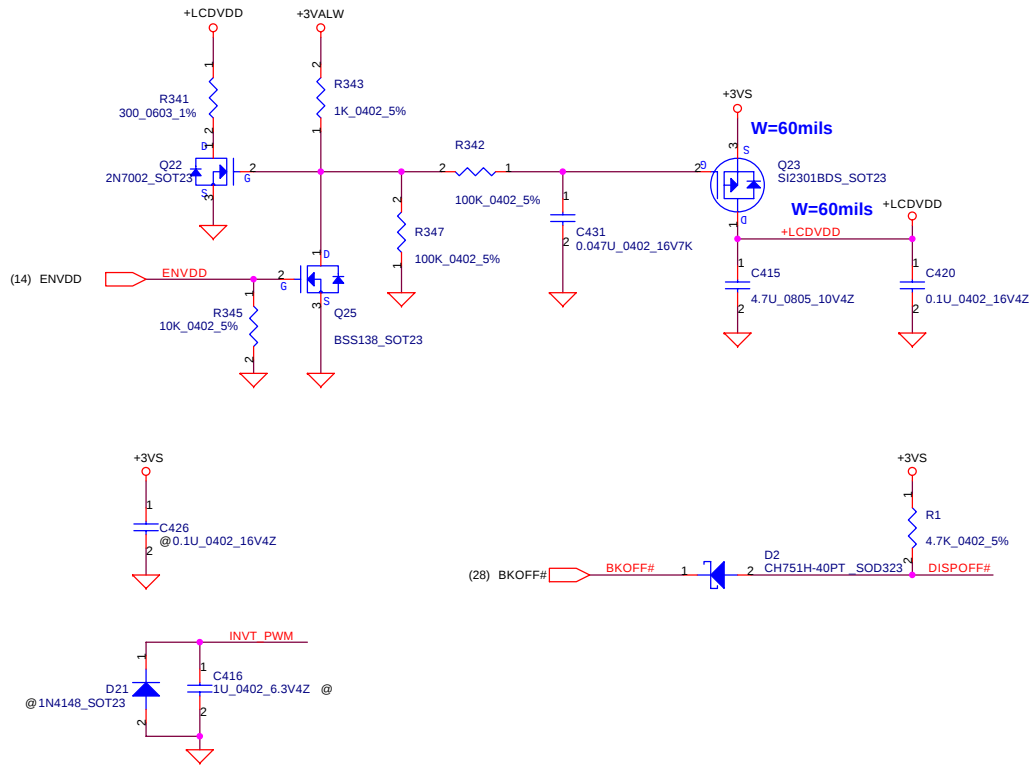
TV-OUT Conn.

Place closed to chipset



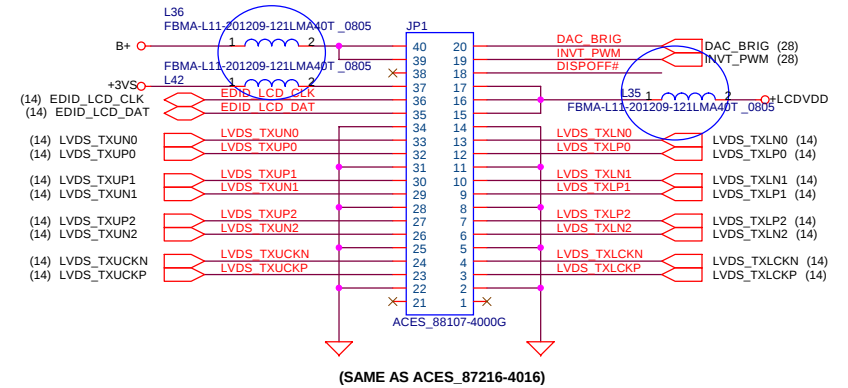
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LCD POWER CIRCUIT



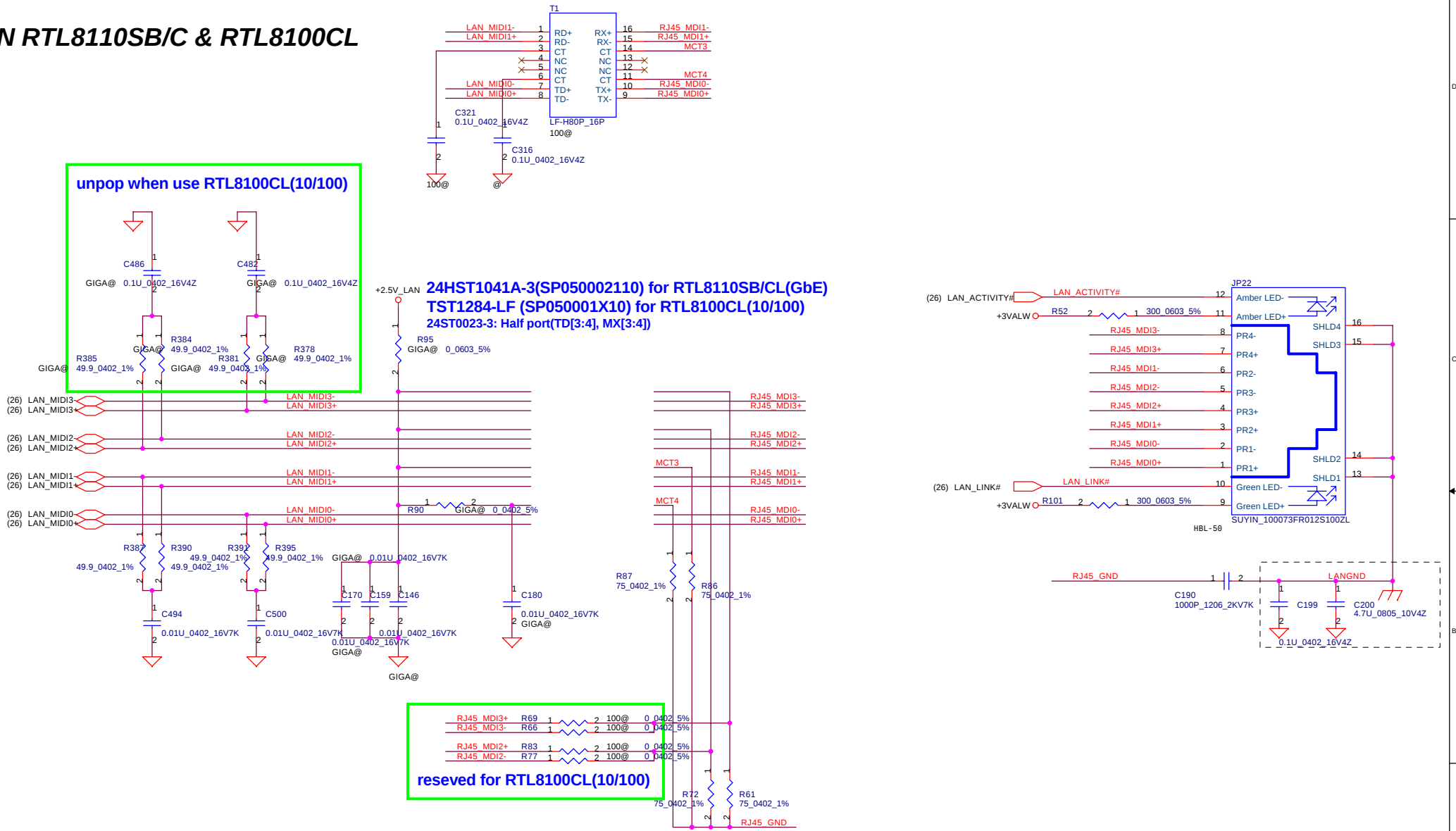
LCD/PANEL CONN.

04/17 modify

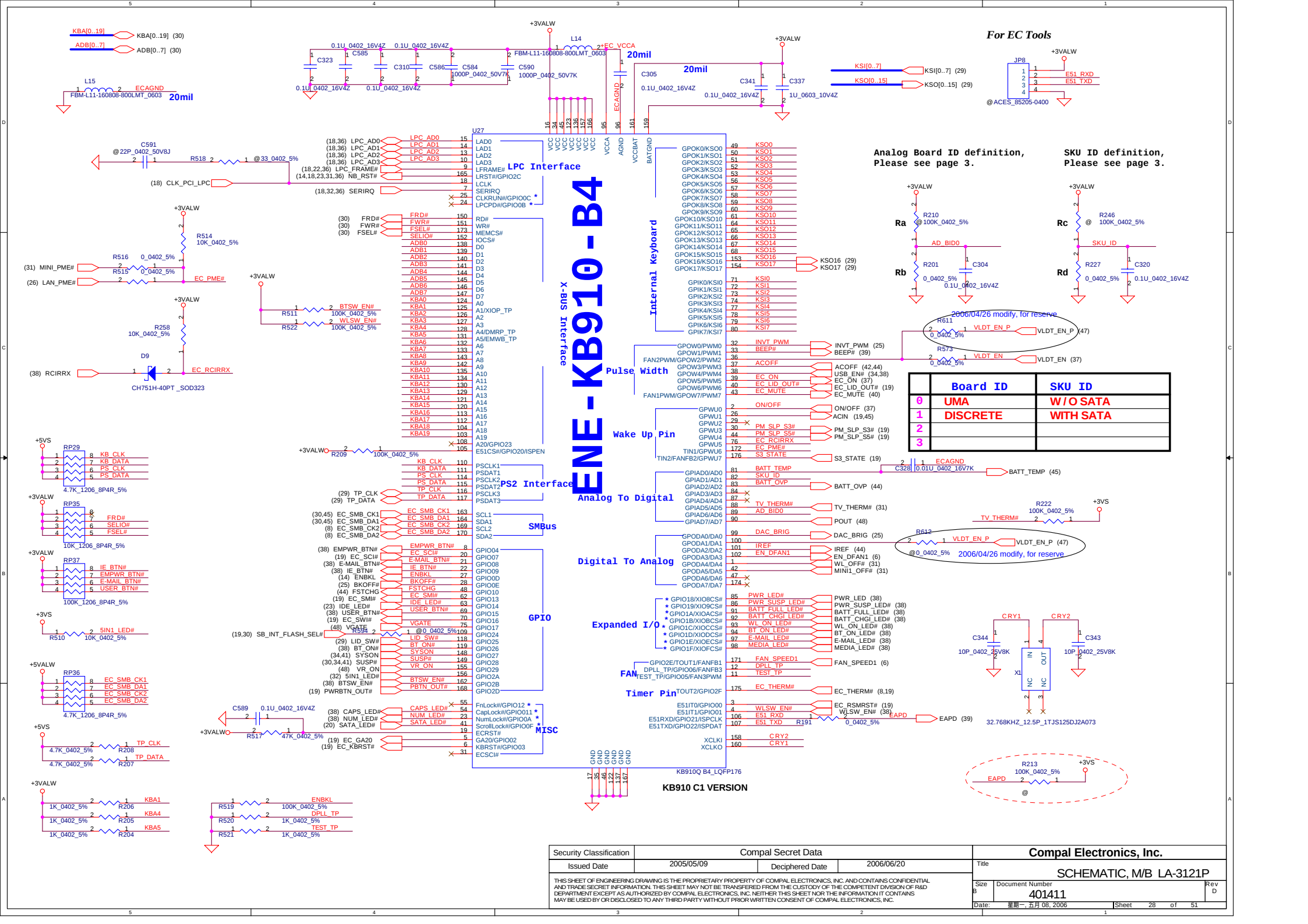


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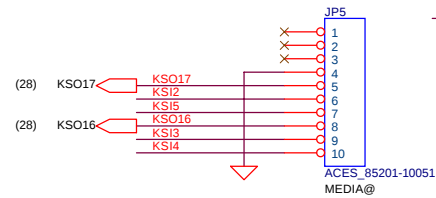
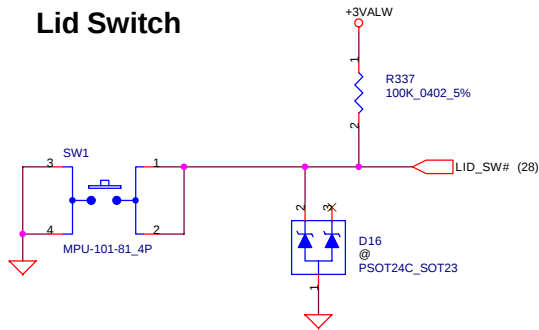
LAN RTL8110SB/C & RTL8100CL



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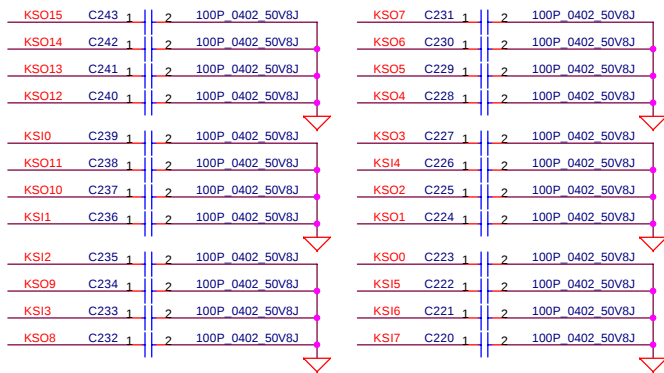


Lid Switch

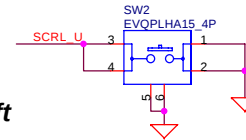


	KSO16	KSO17
KSI2	PLAY	VOL_UP
KSI3	STOP	VOL_DOWN
KSI4	NEXT	ARCADE_TV
KSI5	REV	

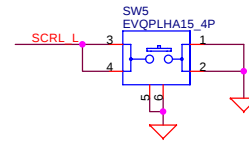
INT_KBD Conn.



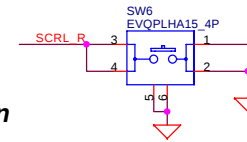
Scroll Up



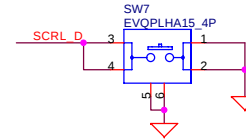
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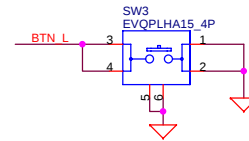
Scroll Right



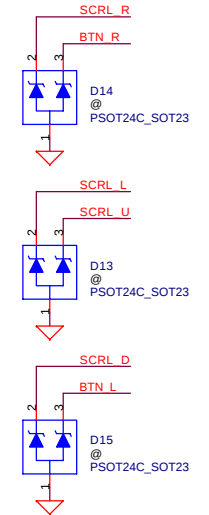
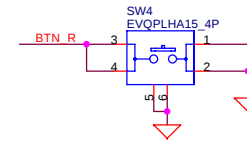
Scroll Down



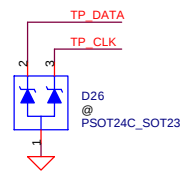
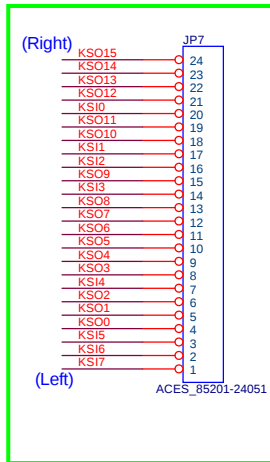
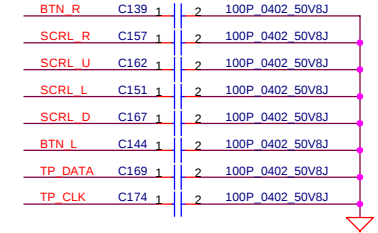
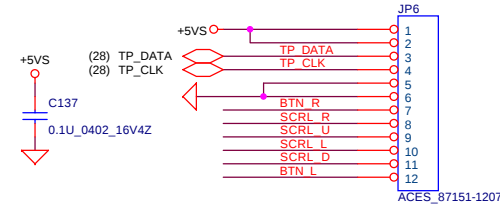
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Right

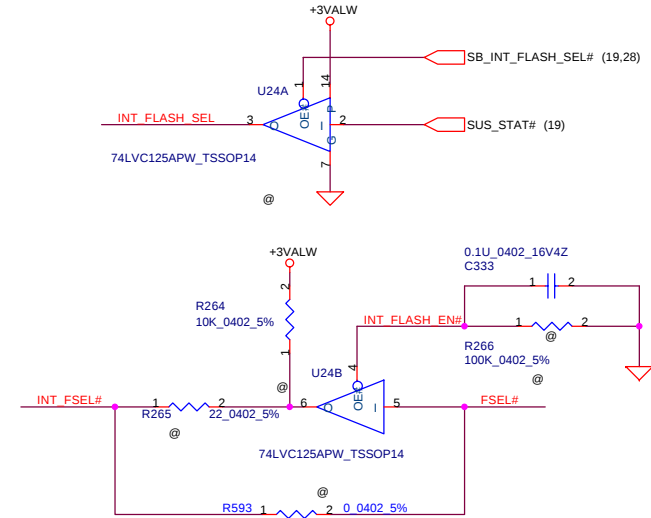
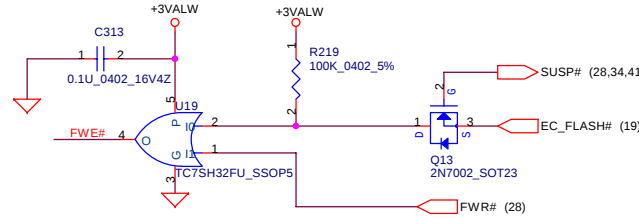
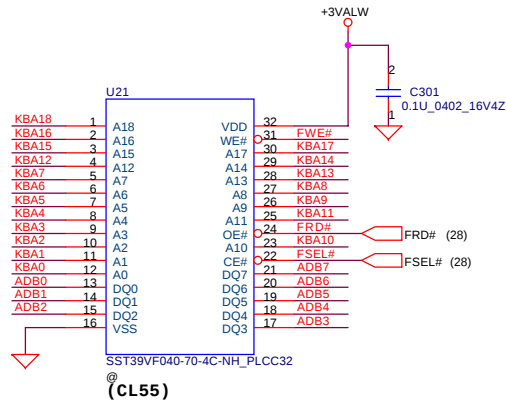


To TP/B Conn.

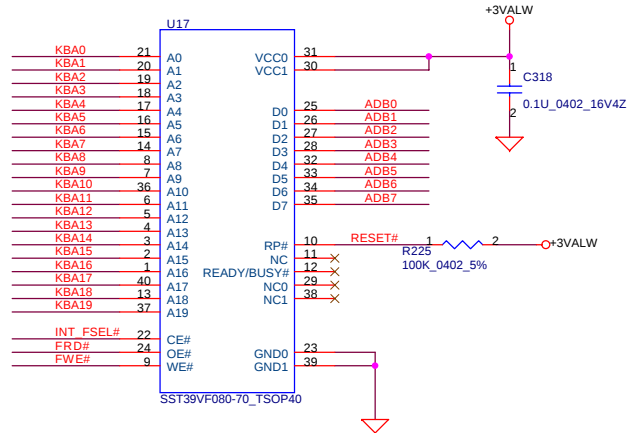


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(28) KBA[0..19] KBA[0..19]
 (28) ADB[0..7] ADB[0..7]

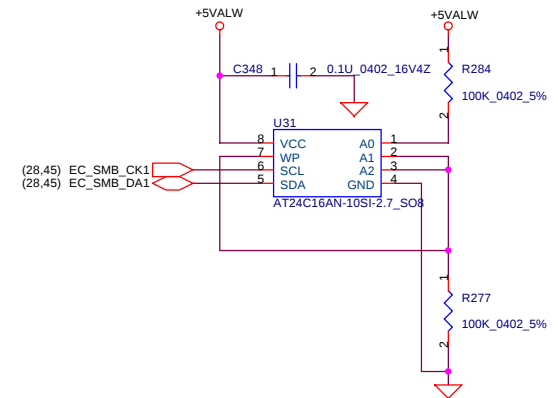
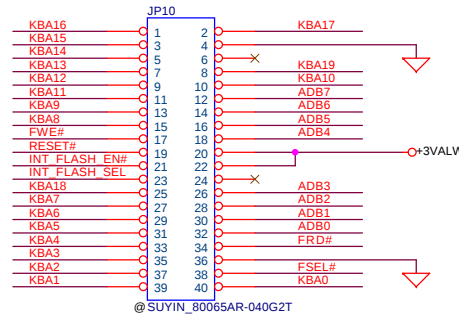


1MB Flash ROM

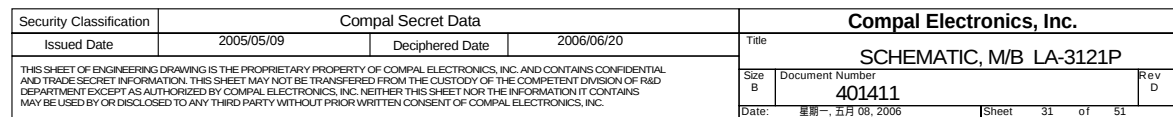
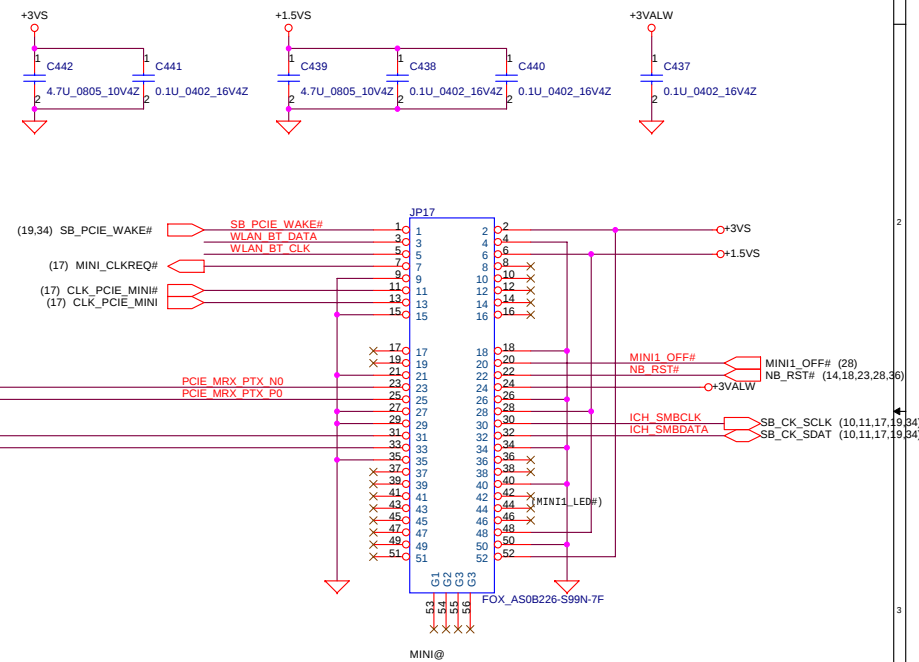
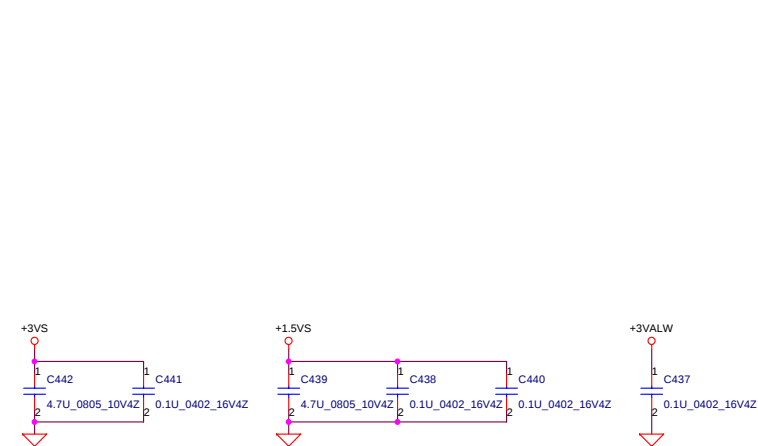


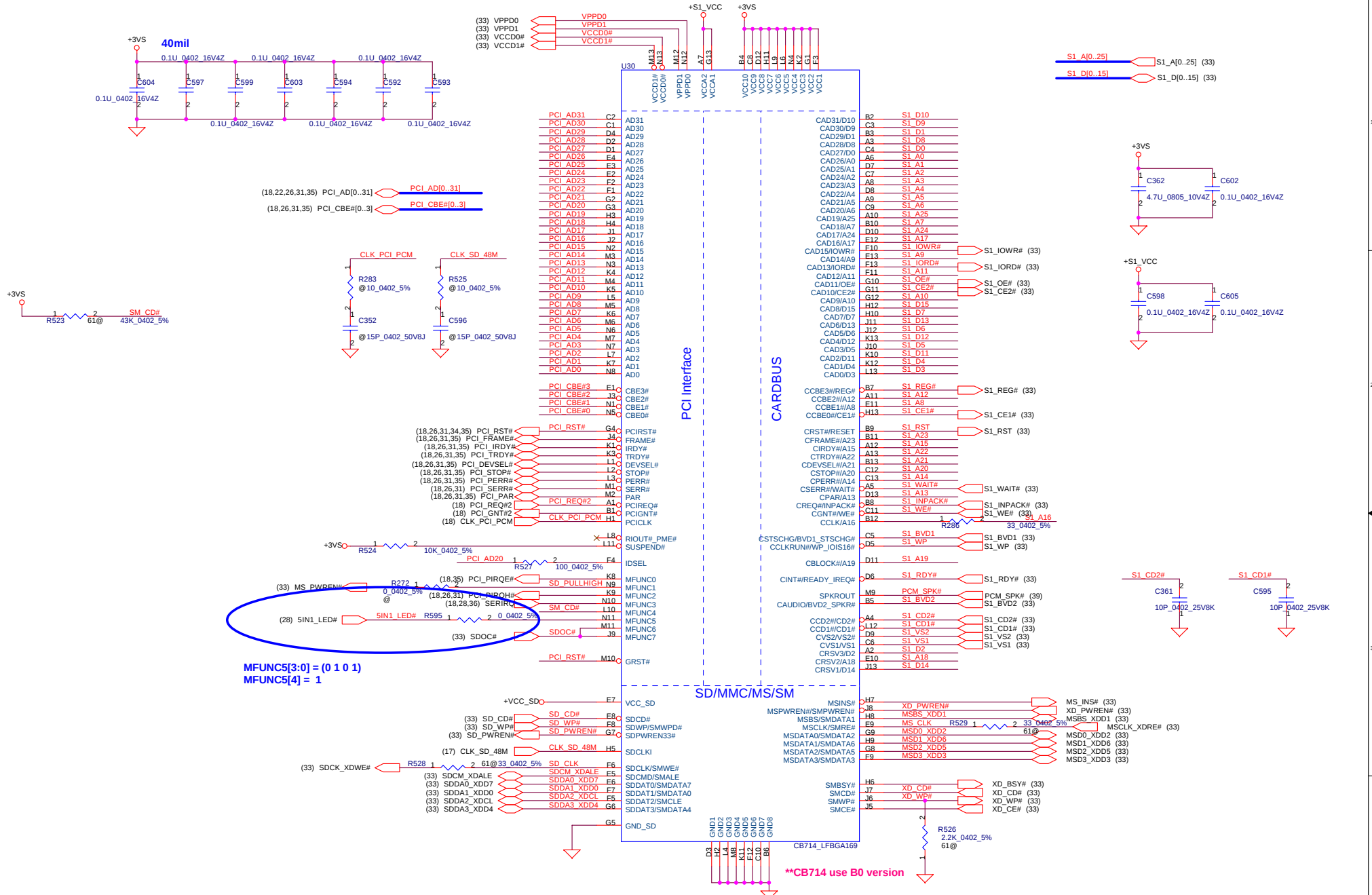
SST part : SA390800000
 MXIC part : SA290080120

1MB ROM Socket



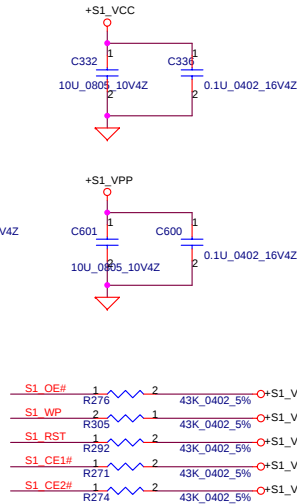
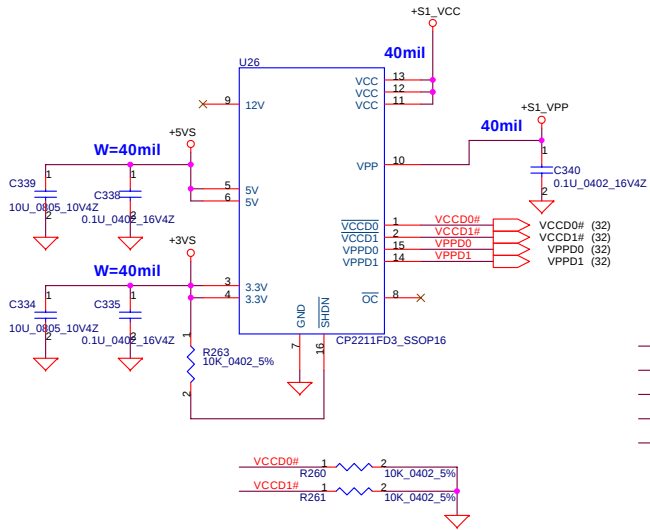
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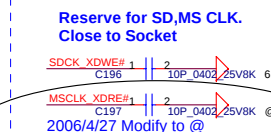
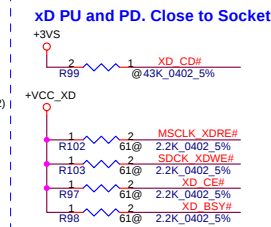
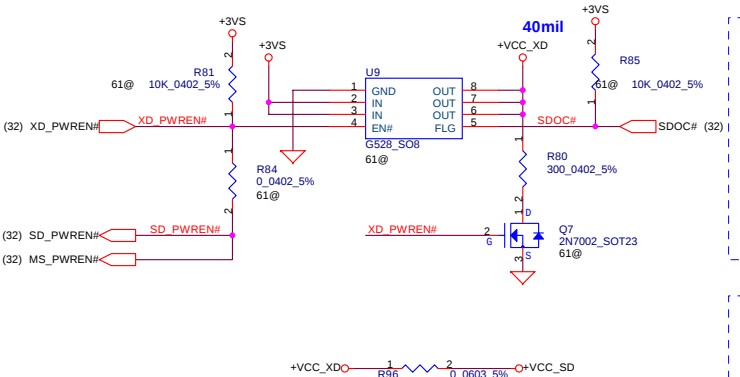
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PCMCIA Power Control



(32) S1_A[0..25] S1_A[0..25]
(32) S1_D[0..15] S1_D[0..15]

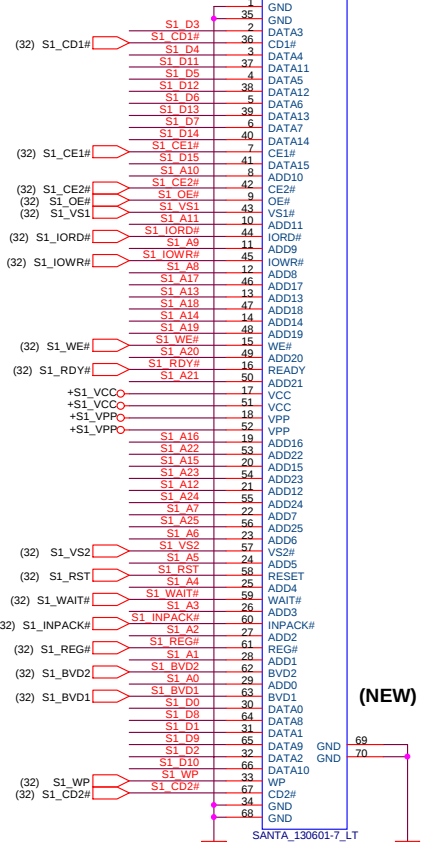
SD/MS Power Control XD Power Control



2006/4/27 Modify to @

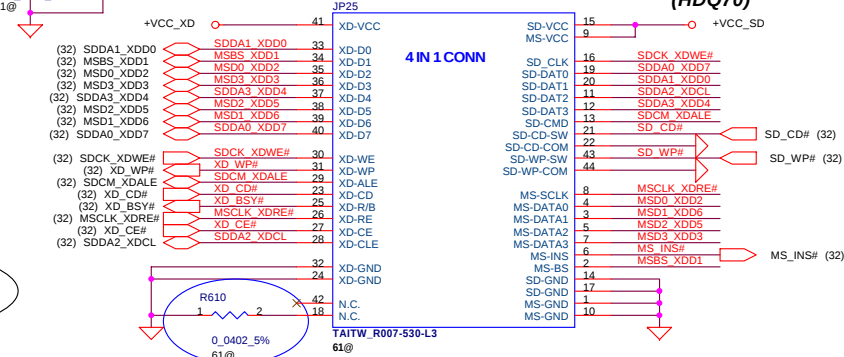
2006/4/13 modify

PCMCIA Socket



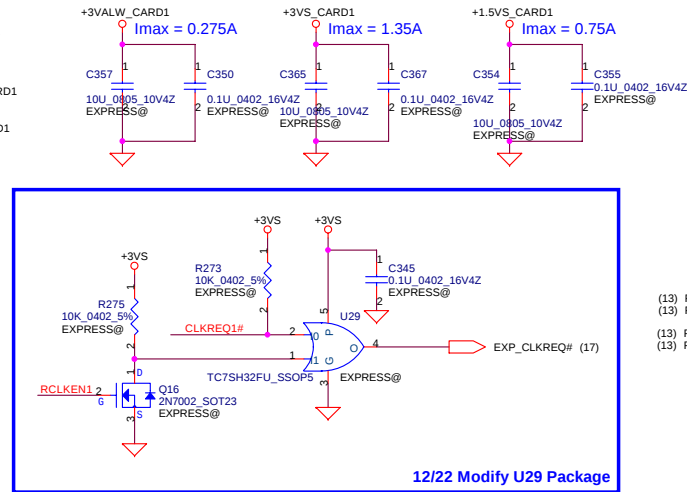
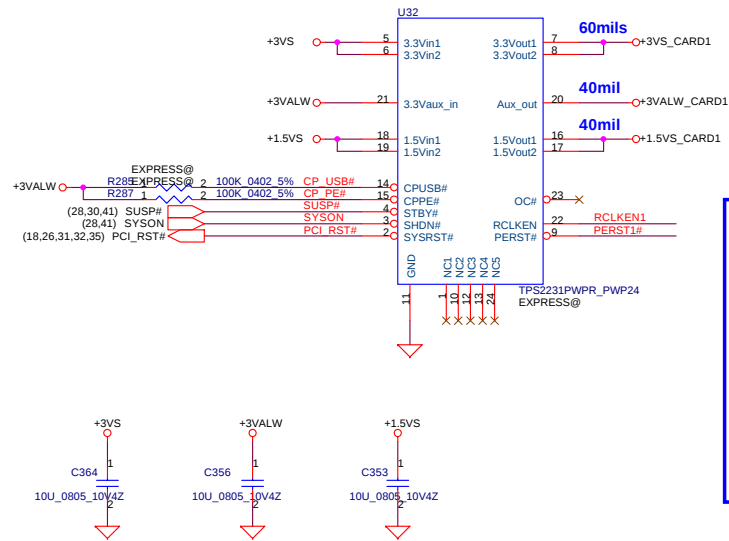
(NEW)

6 IN 1 Socket (HDQ70)

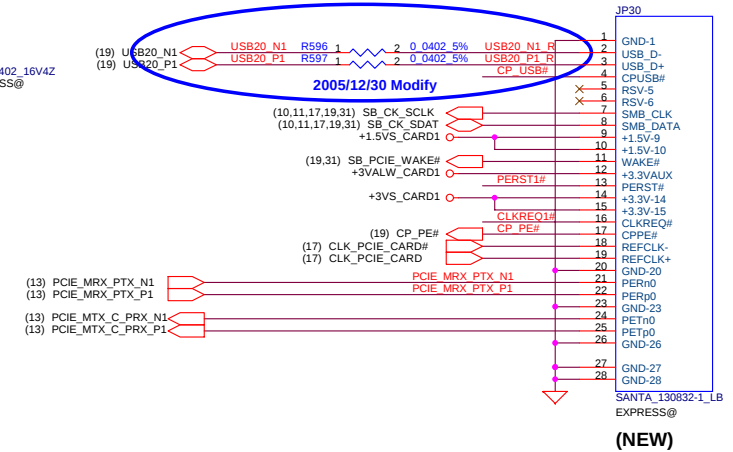


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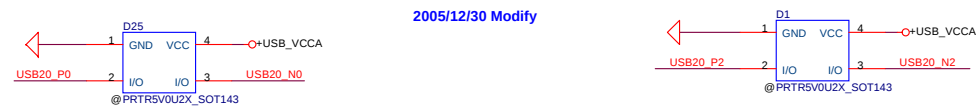
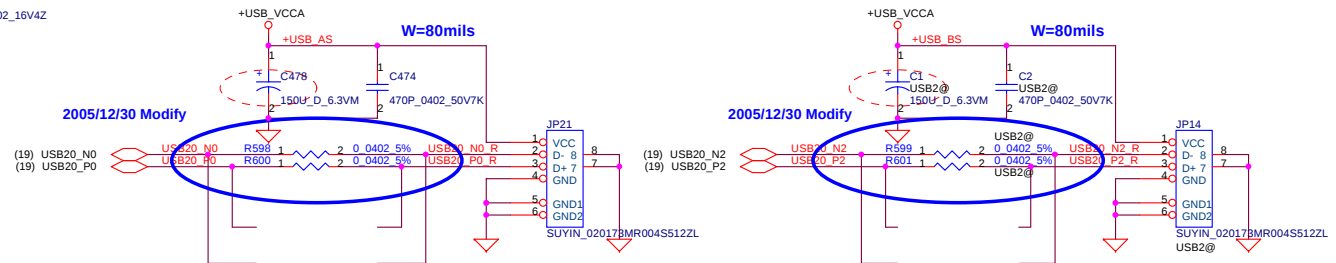
New Card Power Switch



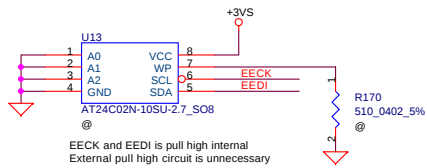
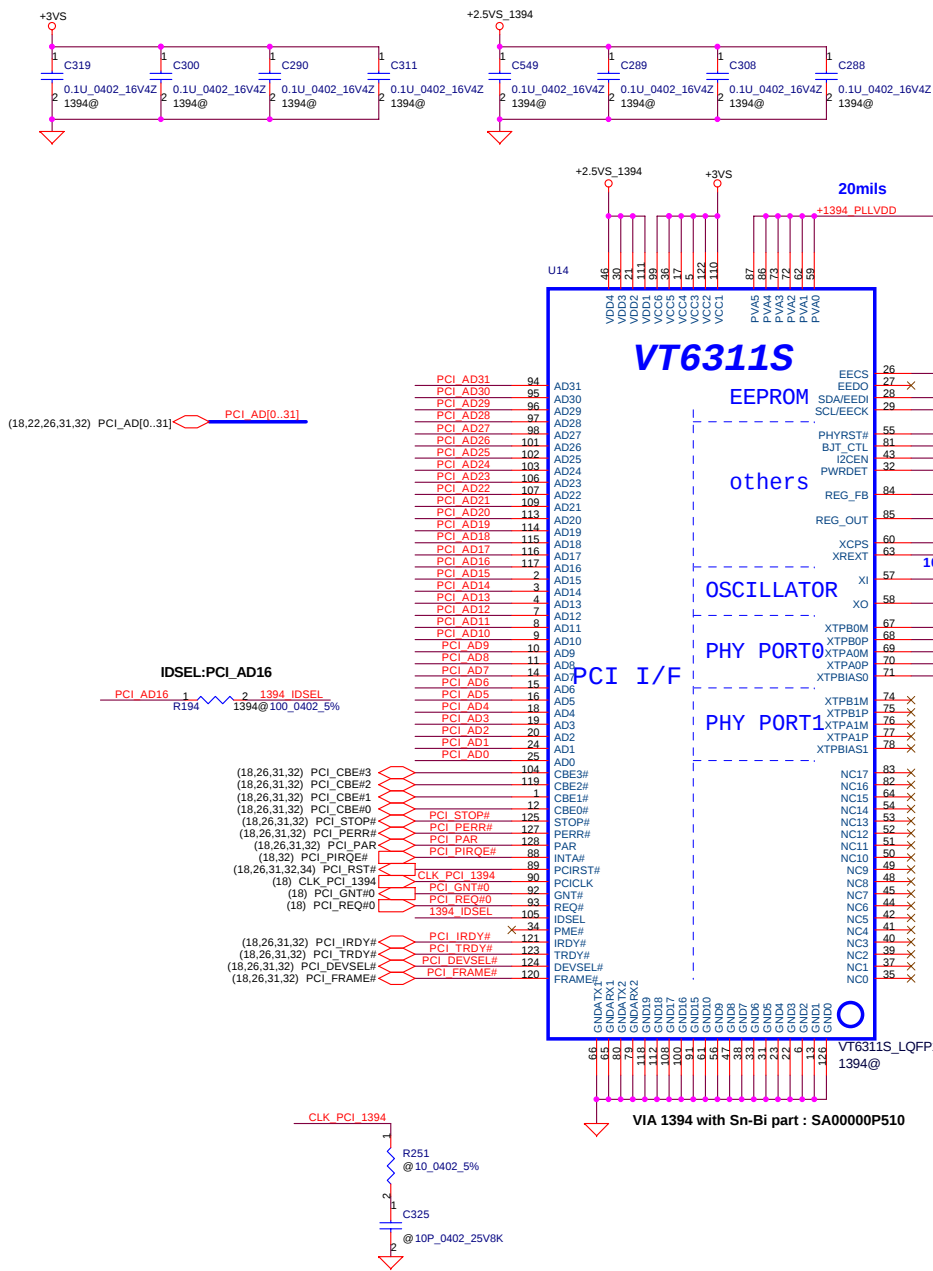
New Card Socket (Left)



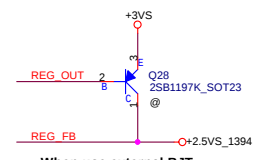
USB CONN. 1 & 2



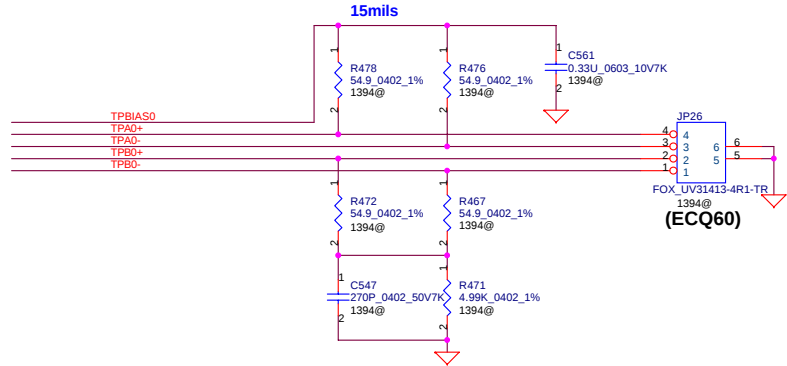
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When use external EEPROM
Populate U13, R170, R186
Un-populate R169



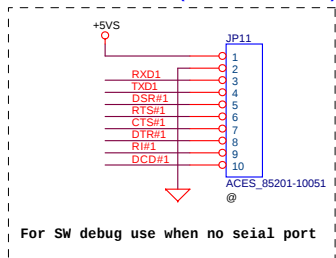
When use external BJT
Populate Q28, R490



(ECQ60)

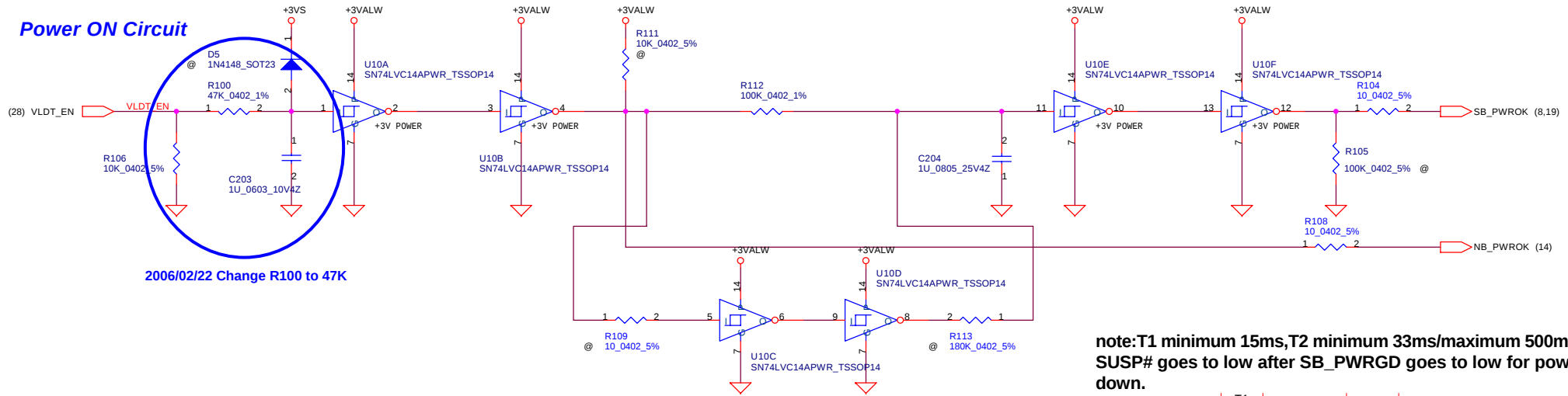
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Deciphered Date				2006/06/20				Schematic, M/B LA-3121P			
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SUPER I/O SMsC LPC47N207

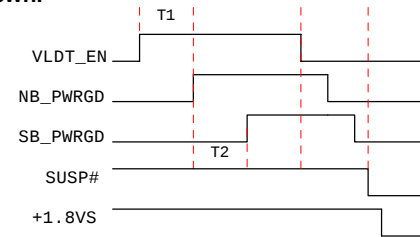


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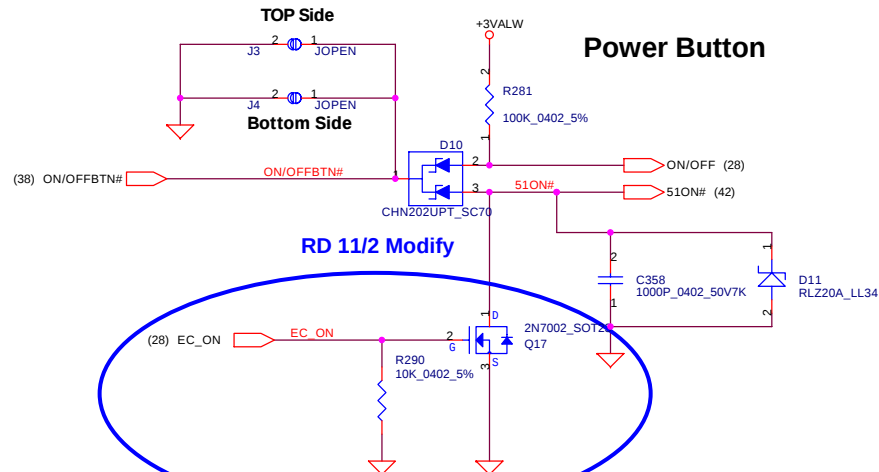
Power ON Circuit



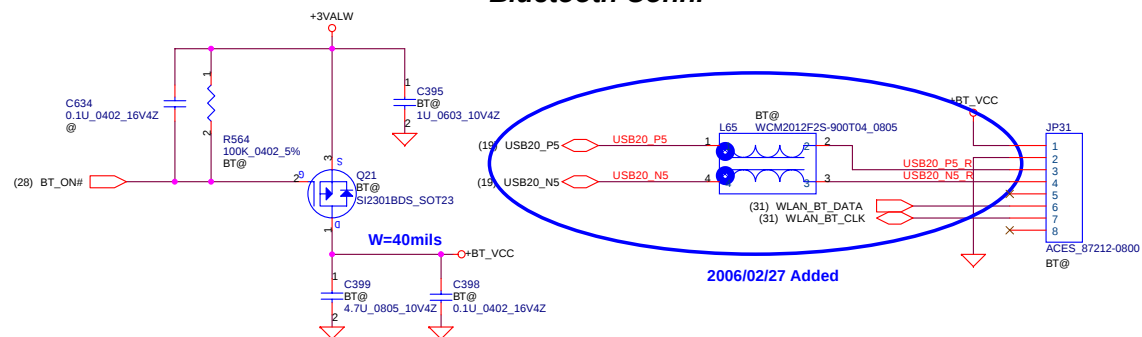
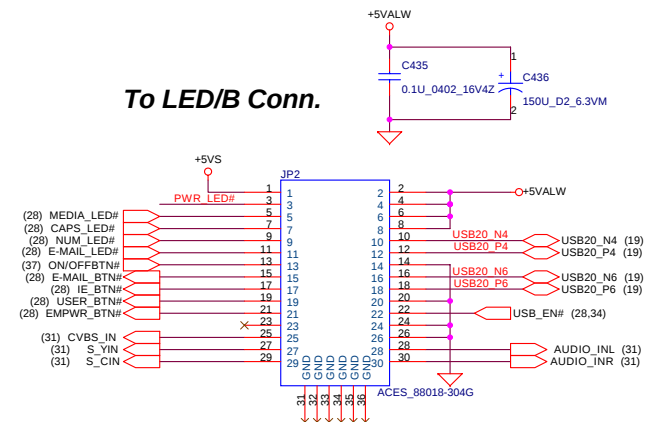
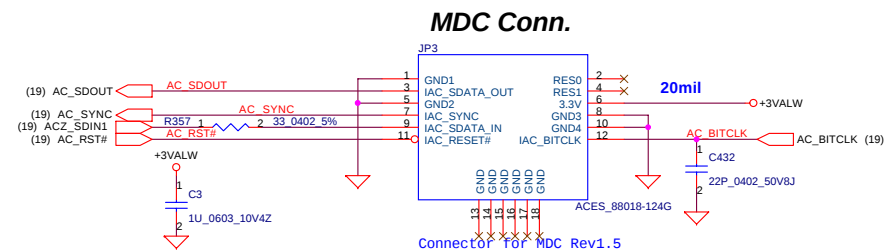
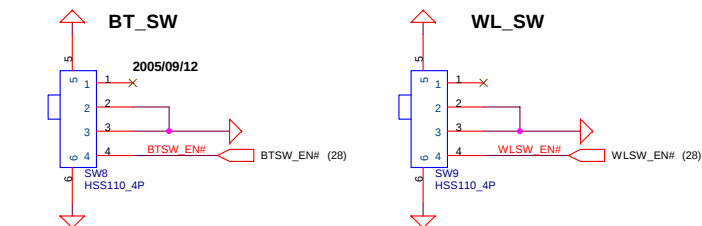
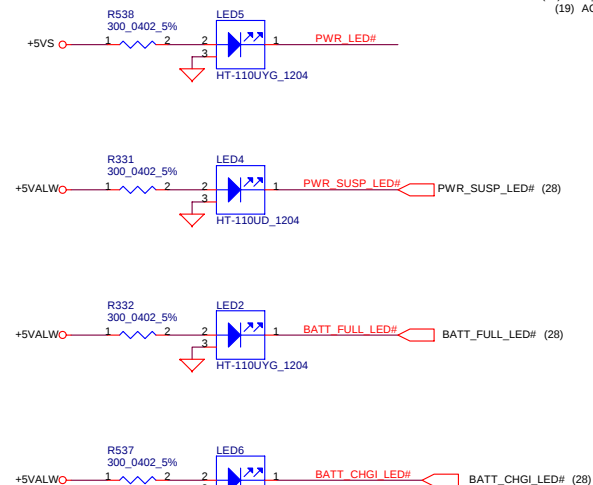
note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWROK goes to low for power down.



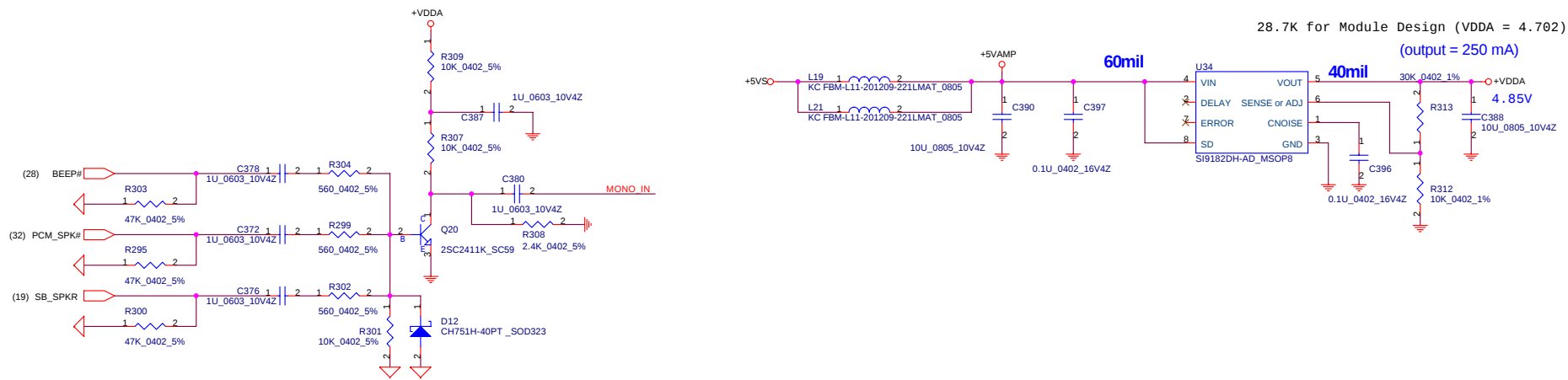
Power Button



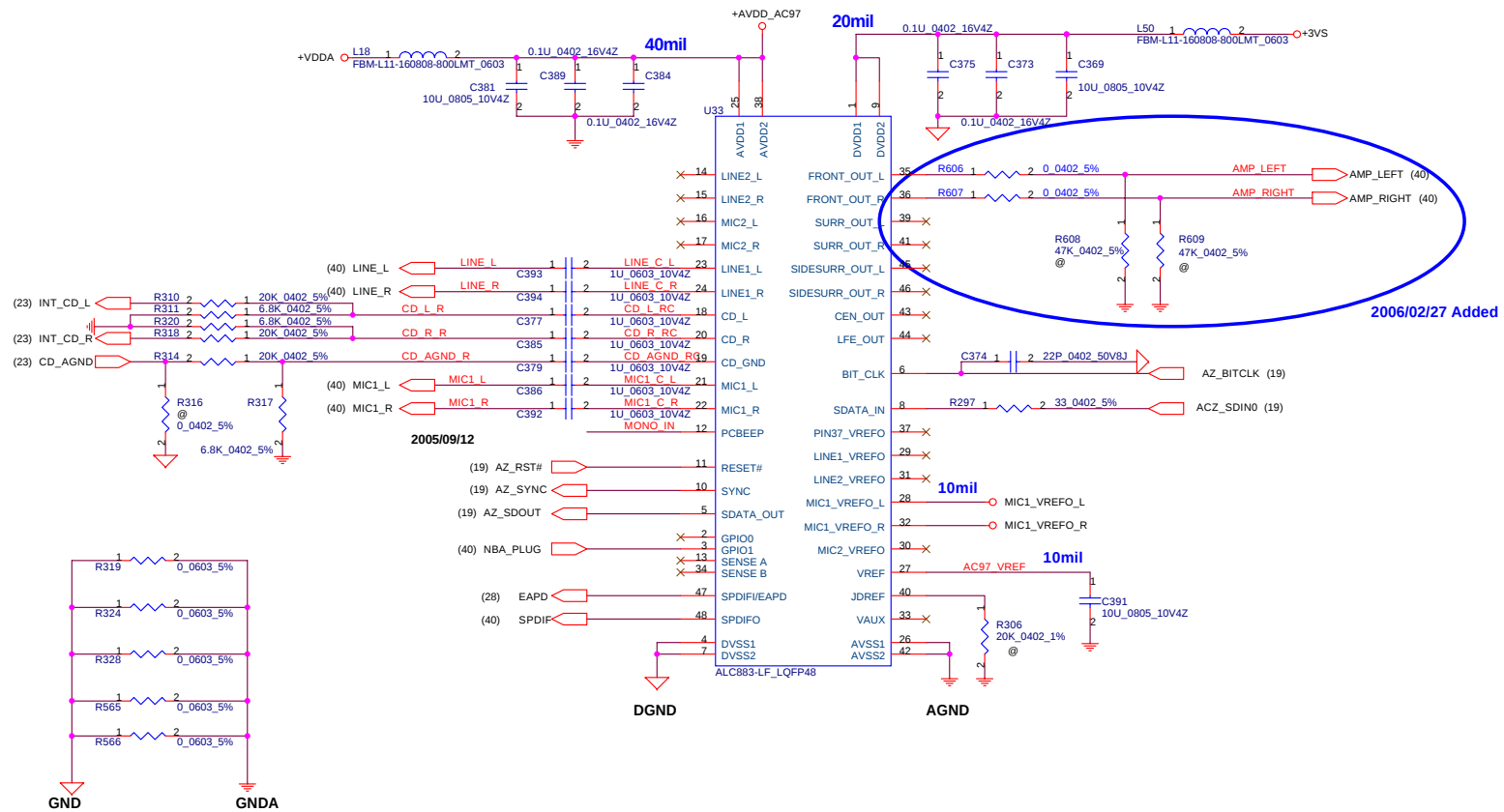
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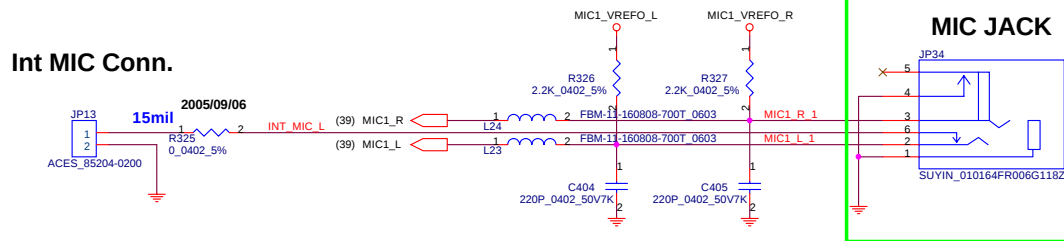
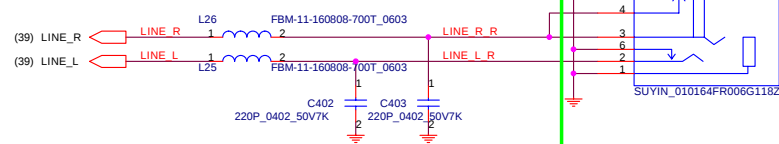
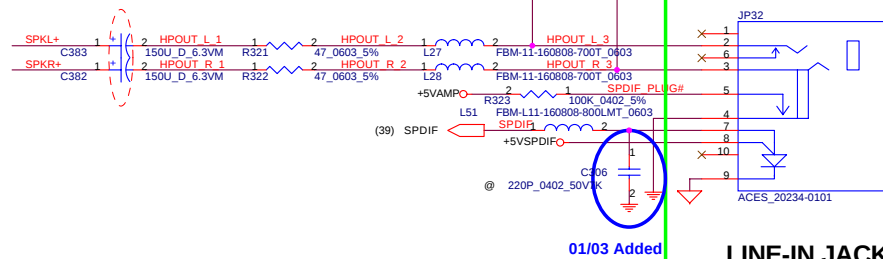
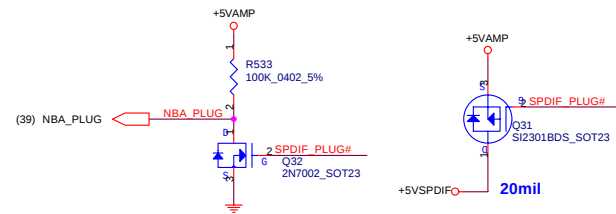
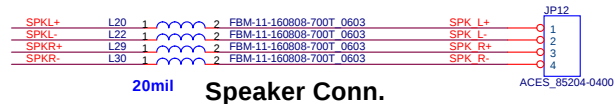
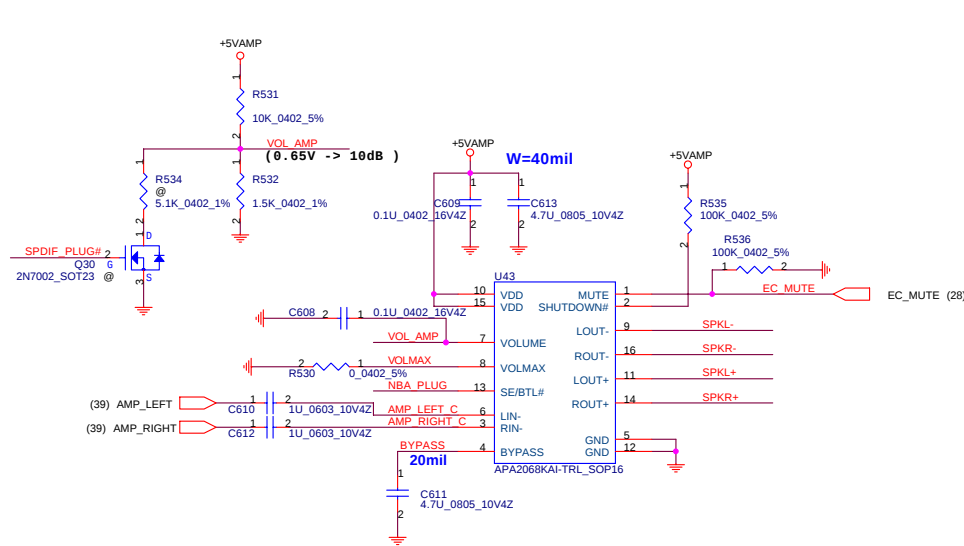
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HD Audio Codec

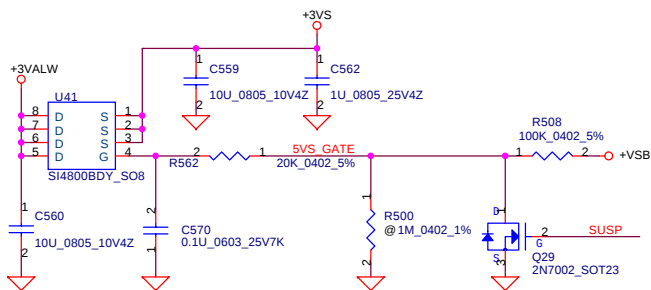


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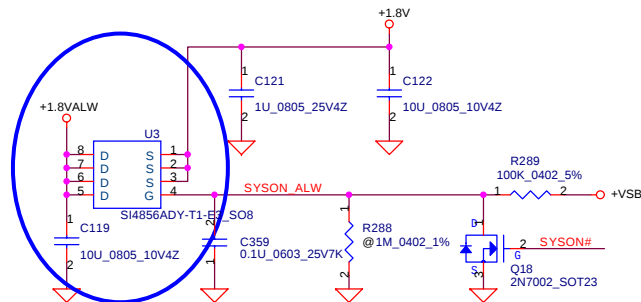


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+3VALW TO +3VS

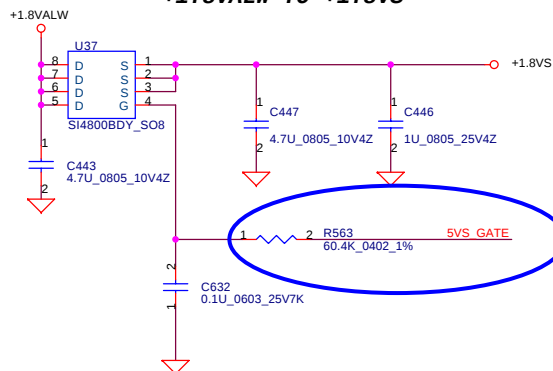


+1.8VALW TO +1.8V



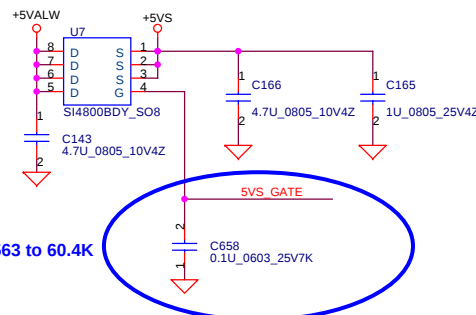
12/30 Change U3 to SI4856ADY

+1.8VALW TO +1.8VS



12/30 Change R563 to 60.4K

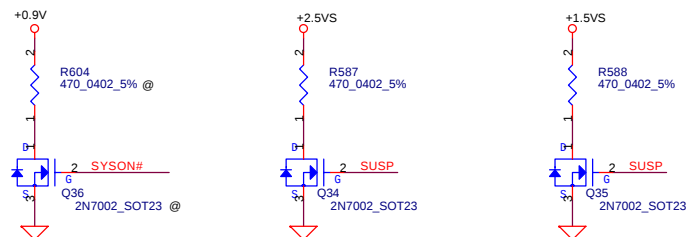
+5VALW TO +5VS



2006/2/22 Add C658 0.1uF

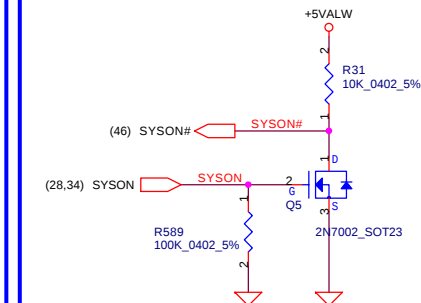
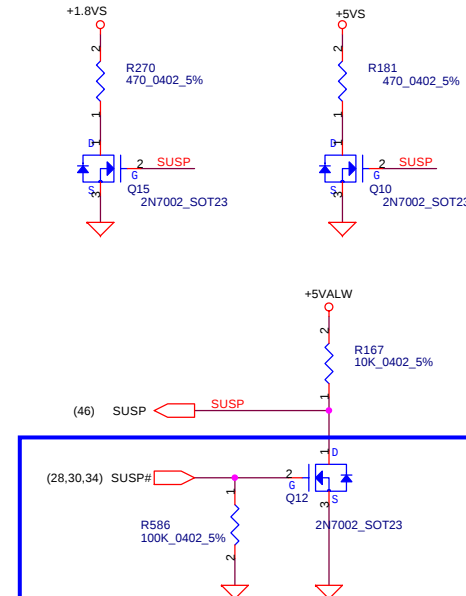
2006/4/13 modify package for lead-free part

12/22 Added



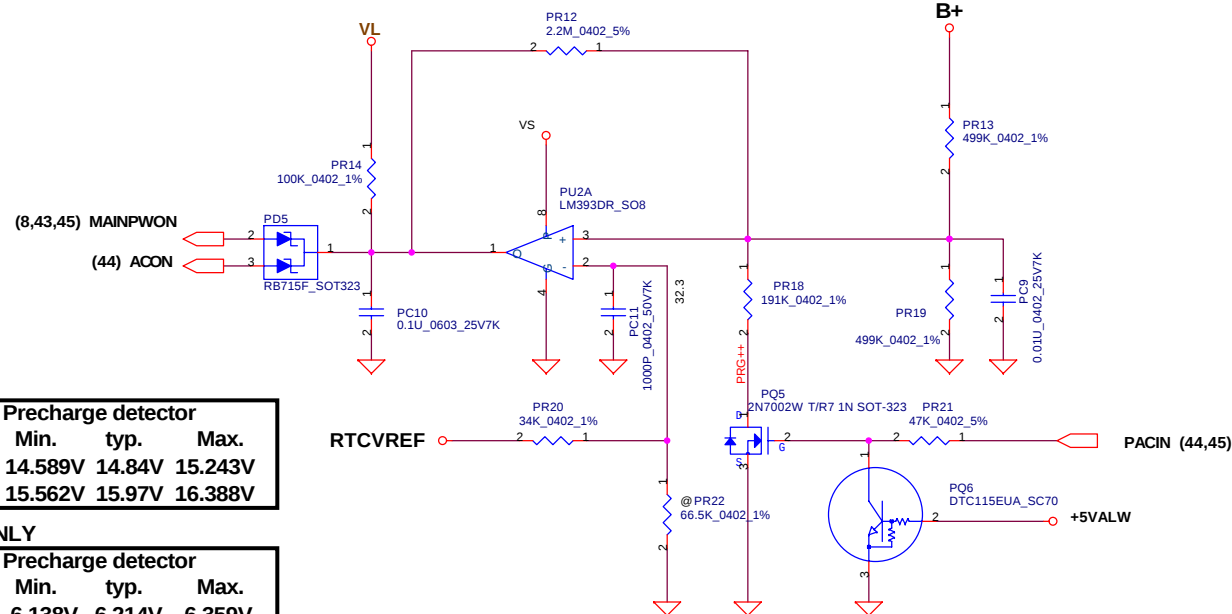
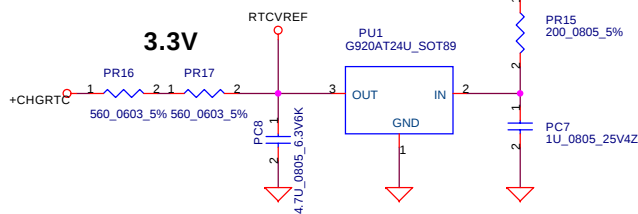
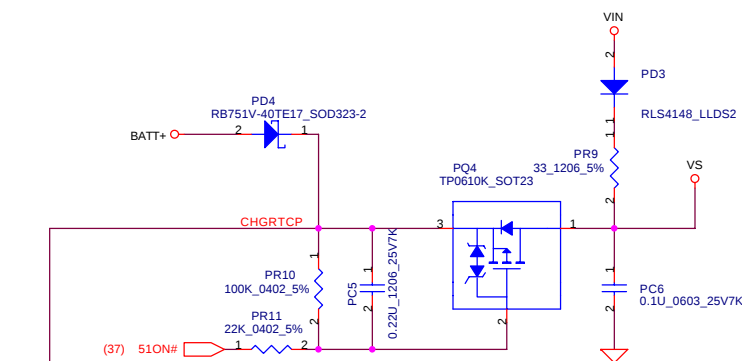
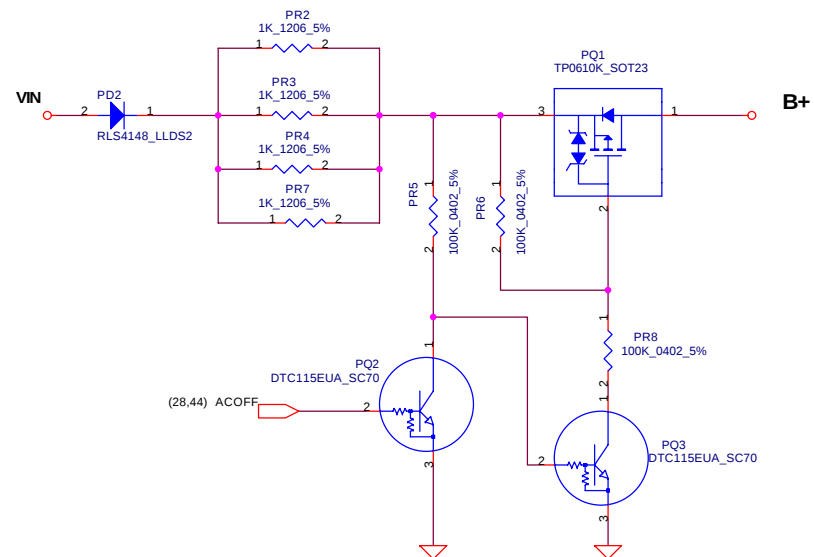
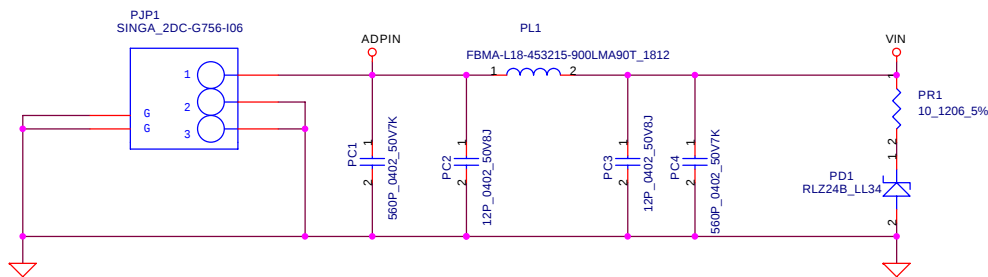
Near PU8

Near PU12



12/22 Change Q5,Q12 to 2N7002

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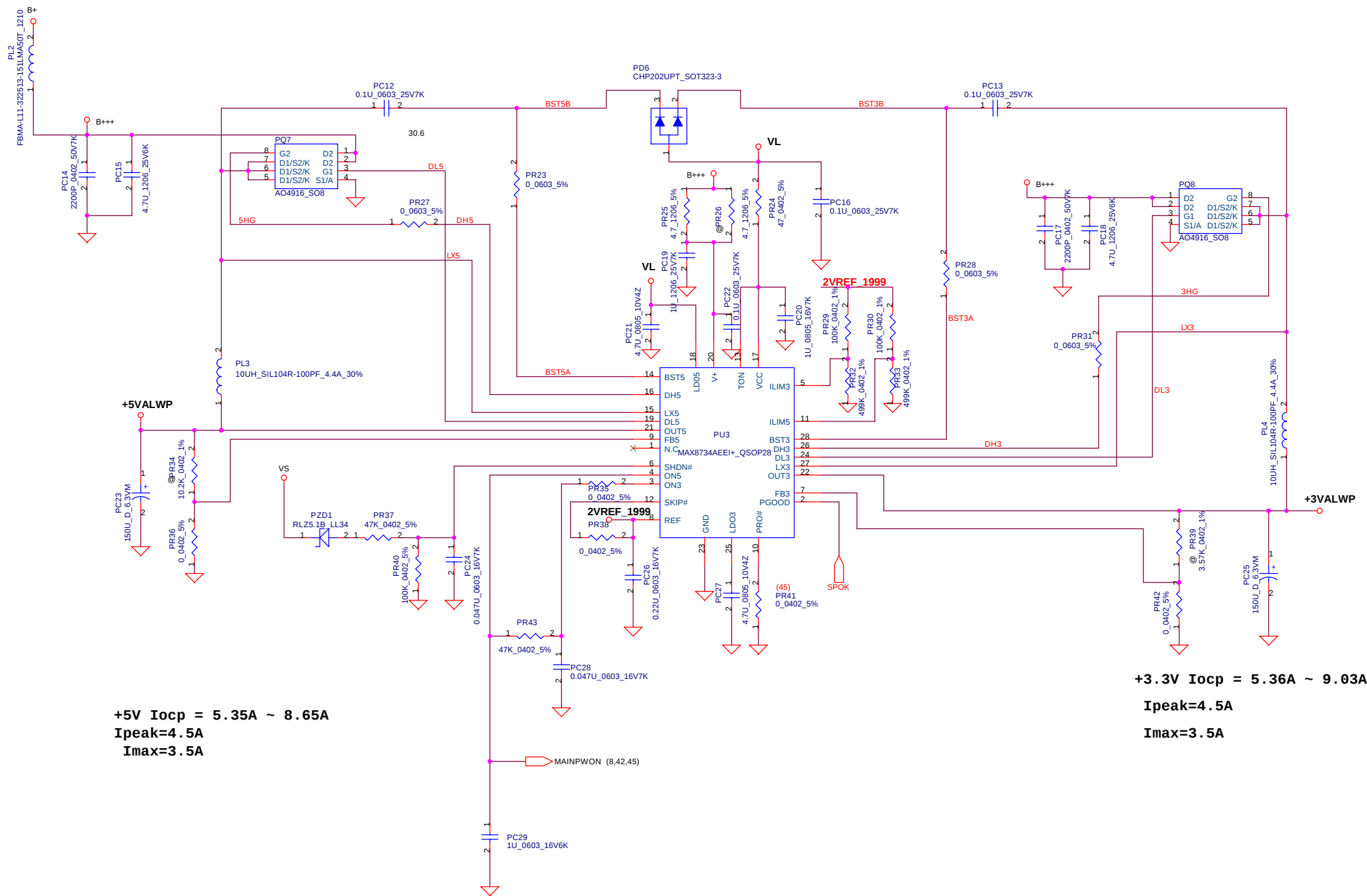
ACIN

	Precharge detector		
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

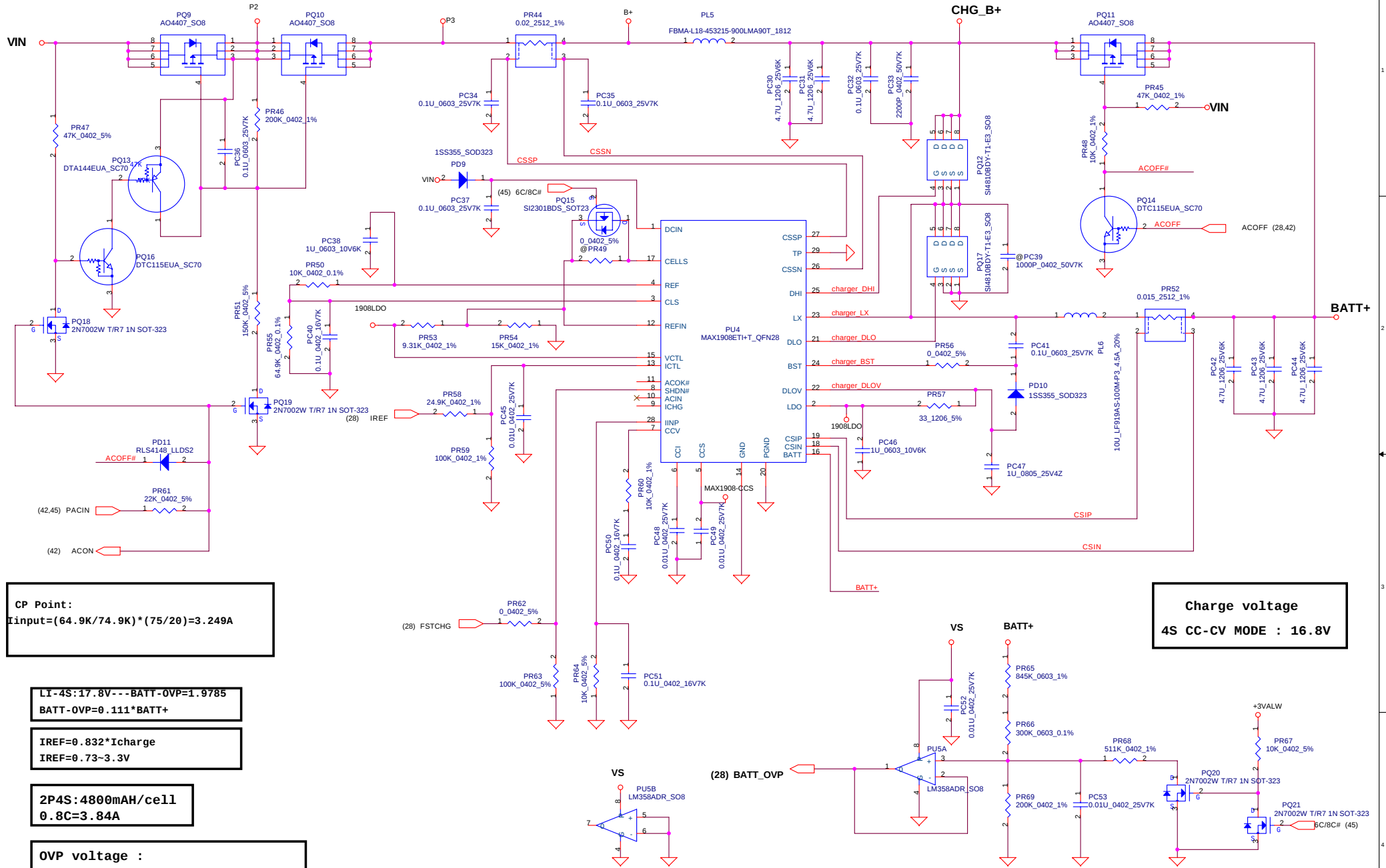
	Precharge detector		
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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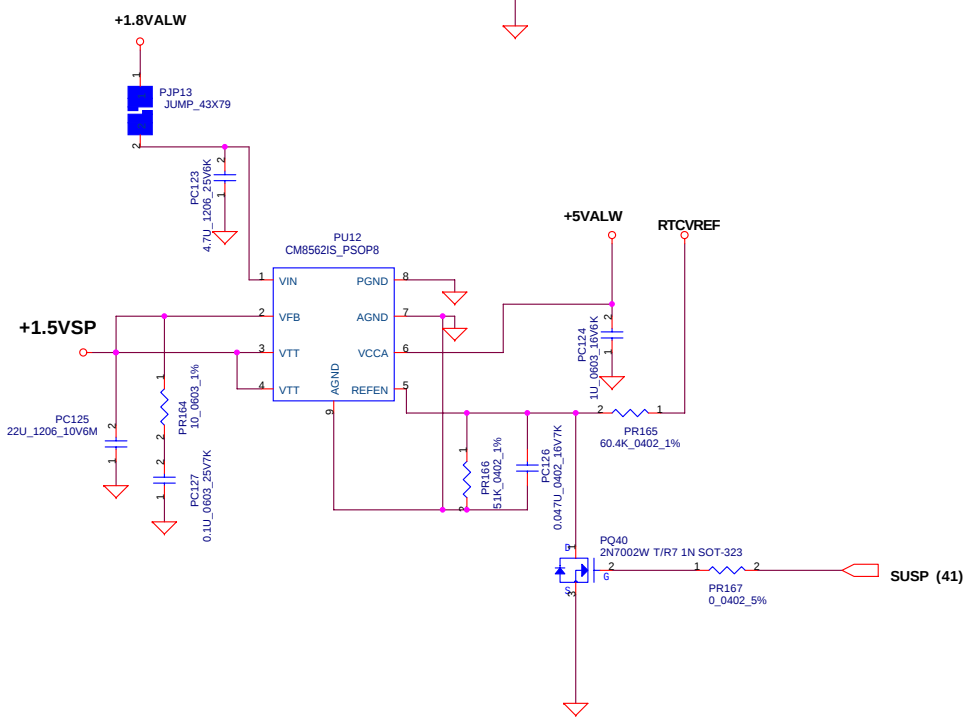
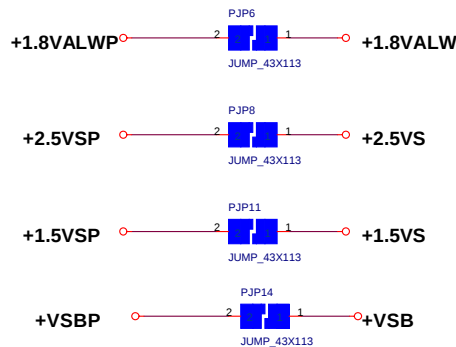
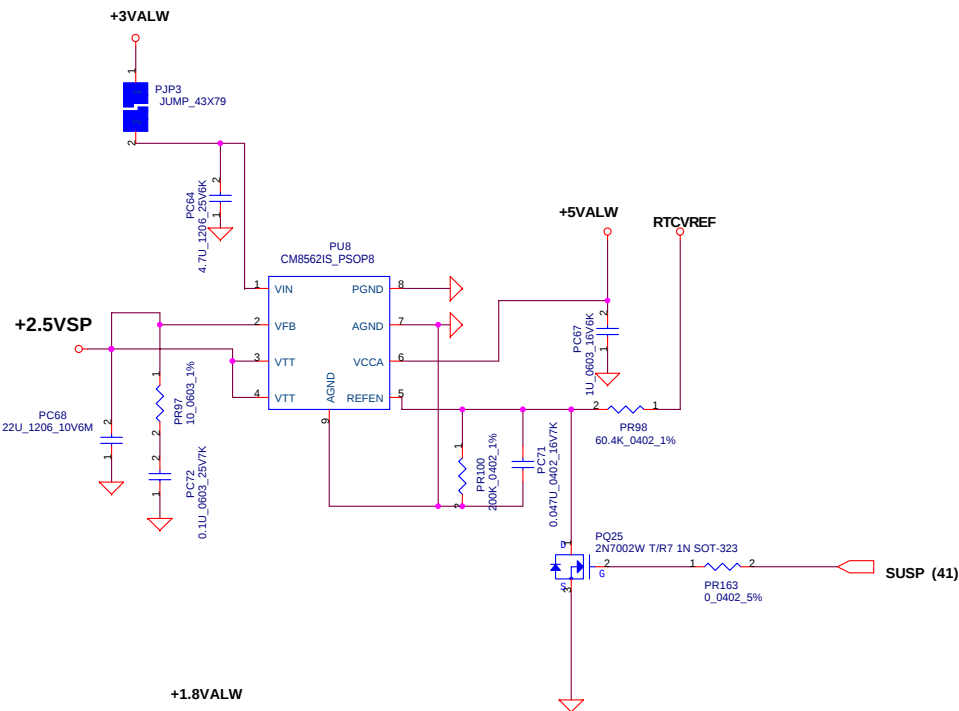
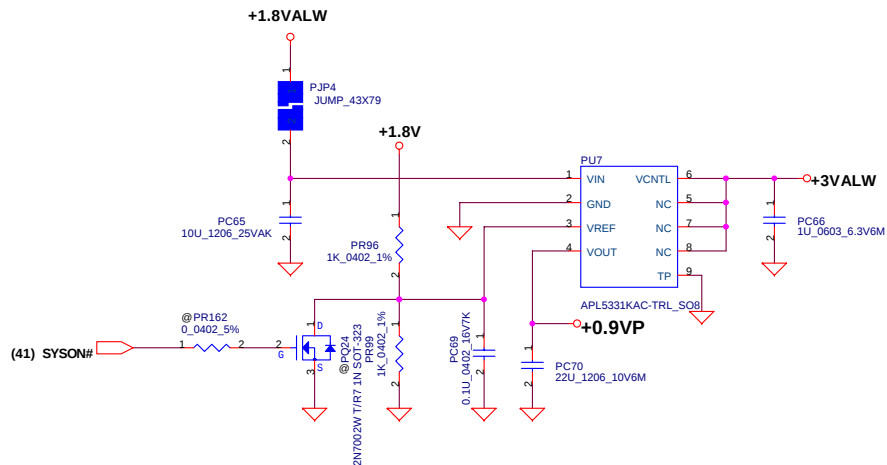


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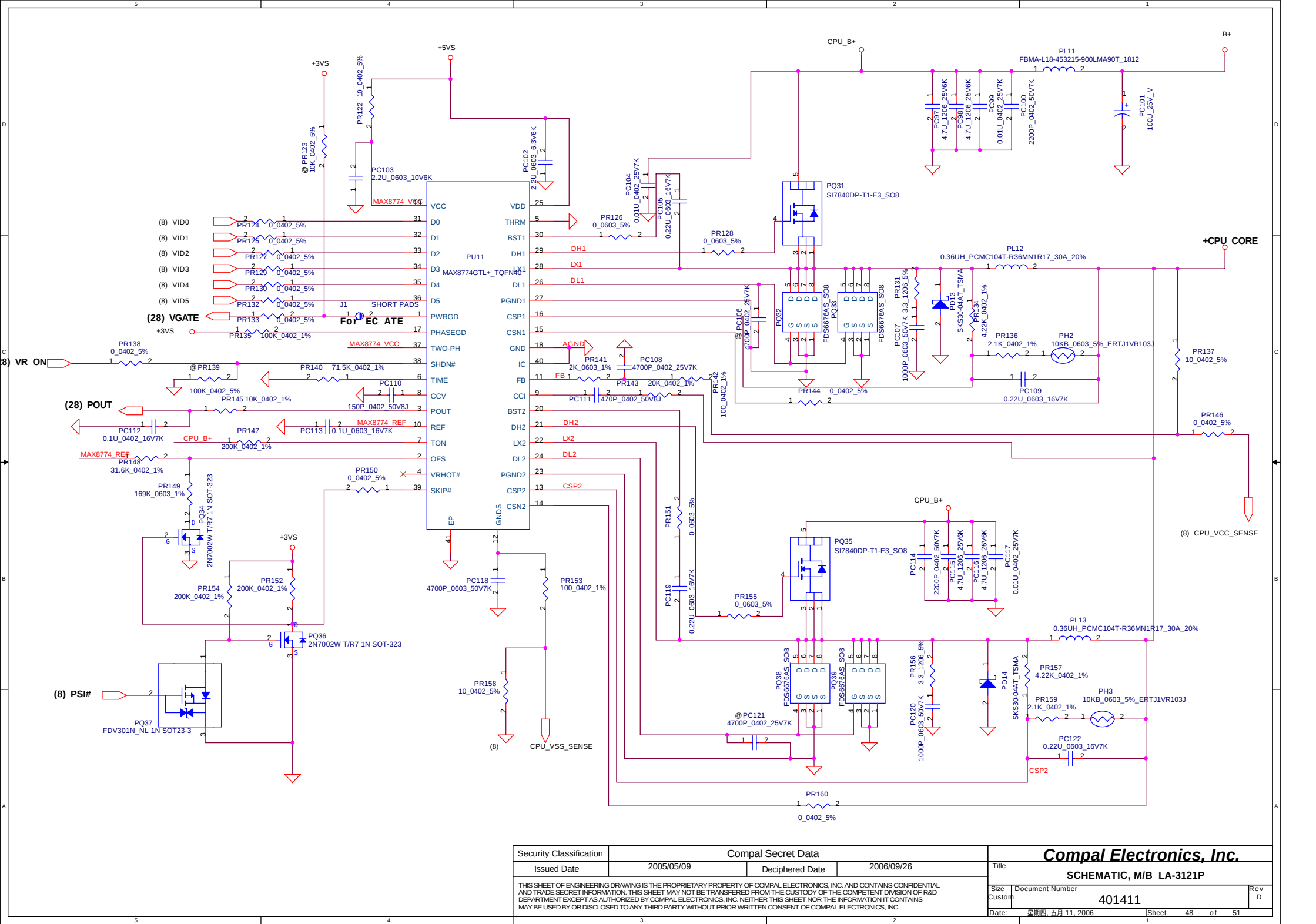
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	VER	Phase
1	Schematic update.	Because schematic update, we don't need this two parts.	0.1	46	Delete PQ24 SB000005M10.	0.1	EVT
2	Schematic update.	Because schematic update, we don't need this two parts.	0.1	46	Delete PR162 SD028000080.	0.1	EVT
3	BOM error	BOM error	0.1	44	Change PQ15 from SB923010010 to SB923010020.	0.1	EVT
4	BOM error	BOM error	0.1	48	Change PQ37 from SB503010004 to SB503010010	0.1	EVT
5	MOSFET thermal issue	Because we need to reduce MOSFET teperature of high side mos.	0.1	48	Change PQ31 and PQ35 from SB562940000 to SB578400080.	0.1	EVT
6	BOM error	BOM error	0.1	42	Change PL1,PL5,PL7 and PL11 form SM010018210 to SM010020720.	0.1	EVT
7	BOM error	BOM error	0.1	47	Change PR121 from SD000001500 to SD000001580.	0.1	EVT
8	BOM error	BOM error	0.1	48	Change PR149 from SD014169300 to SD014169380.	0.1	EVT
9	BOM error	BOM error	0.1	44	Change PR55 from SD034100380 to SD034100280.	0.1	EVT
10	BOM error	BOM error	0.1	44	Change PR50 from SD034576280 to SD034140280.	0.1	EVT
11	BOM error	BOM error	0.1	48	Change PR148 from SD034316200 to SD034316280.	0.1	EVT
12	BOM error	BOM error	0.1	44	Change PC52,PC53,PC54,PC87,PC88,PC93 and PC94 from SE075103Z00 to SE075103K80.	0.1	EVT
13	BOM error	BOM error	0.1	46	Change PC70 from SE153106K80 to SE116226M80.	0.1	EVT
14	High limit issue.	Because the high is limited, we need to reduce space.	0.1	48	Change PC101 from SF22004M210 to SF10004M080.	0.1	EVT
15	BOM error	BOM error	0.1	48	Add PR137 and PR158 SD028100A80.	0.1	EVT
16	Power sequence adjust.	Power sequence adjust.	0.1	47	Add PR168 SD034100280.	0.1	EVT
17	Power sequence adjust.	Power sequence adjust.	0.1	47	Delete PR115 SD034100280.	0.1	EVT
18	BOM cost issue.	BOM cost issue.	0.1	42	Change PQ5, PQ18, PQ19, PQ20, PQ21, PQ23, PQ25, PQ34, PQ36, PQ40 from SB000005M10 to SB000006800.	0.1	EVT

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	VER	Phase
1	Charger accuracy issue.	Increase changer accuracy to meet customer request.	0.2	44	Change PR44 from SE000001E00 to SE000001F00.	0.1	EVT
2	Charger accuracy issue.	Increase changer accuracy to meet customer request.	0.2	44	Change PR50 form SD034140280 to SD000008B00.	0.1	EVT
3	Charger accuracy issue.	Increase changer accuracy to meet customer request.	0.2	44	Change PR55 from SD034100280 to SD00000CL80.	0.1	EVT
4	Improve IC risk.	Improve IC risk.	0.2	44	Change PR60 from SD034100180 to SD034100280.	0.1	EVT
5	Improve OCP point.	Improve OCP point.	0.3	43	Change PR29 and PR30 from SD034200380 to SD034100380	0.1	EVT
6	Improve OCP point.	Improve OCP point.	0.3	47	Change PR120 from SD034499280 to SD000001580.	0.1	EVT
7	Improve ripple voltage.	Improve ripple voltage.	0.4	46	Change PC68 and PC125 from SE142475K80 to SE116226M80.	0.2	DVT
8	Incresr +1.2VP_HT voltage.	Incresr +1.2VP_HT voltage.	0.4	47	Change PR108 from SD034340180 to SH034348180.	0.2	DVT
9	Incresr +1.8VALWP voltage.	Incresr +1.8VALWP voltage.	0.4	47	Change PR113 from SD034100280 to SD028102280.	0.2	DVT
10	Improve thermal issue.	Improve thermal issue.	0.4	48	Change PQ32, PQ33, 38, PQ39 from SB000003W00 to SB578320010	0.2	DVT
11	Improve thermal issue.	Improve thermal issue.	0.4	48	Change PL12, PL13 from SH12056BM00 to SH000005680.	0.2	DVT
12	Improve +CPU_CORE OCP point.	Improve +CPU_CORE OCP point.	0.4	48	Change PR134, PR157 from SD034150280 to SD034422180	0.2	DVT
13	Improve +CPU_CORE OCP point.	Improve +CPU_CORE OCP point.	0.4	48	Change PR136 and PR159 from SD034150280 to SH034210180.	0.2	DVT
14	Improve +CPU_CORE OCP point.	Improve +CPU_CORE OCP point.	0.4	48	Change PC109 and PC122 from SE042333K80 to SE026224K80	0.2	DVT
15	Improve CPU load line	Improve CPU load line	0.4	48	Change PR141 from SD014255180 to SD014200180	0.2	DVT
16	Improve CPU load line	Improve CPU load line	0.4	48	Change PR142 and PR153 from SD034100A80 to SD034100080.	0.2	DVT
17							
18							

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Item	Fixed Issue	PG #	Modify List	VER	Phase
1	ATI Recommend.	13	Change R376 82.5 ohm to 100 ohm.	0.2	DVT
2	TV-OUT 阻抗匹配.	14	Increase R590,R591,R592 150 ohm pull down resister.	0.2	DVT
3	解決PCI_RST# 漏電問題.	18	Change U15,U16 voltage source +3VS to +3VALW.	0.2	DVT
4	Fixed USB2.0 EYE Diagram .	19	Change R164 11.8K ohm to 11.3K ohm.	0.2	DVT
5	IMPROVE TV-OUT SIGNAL QUALITY.	24	Change C417,C418,C419,C425,C428,C430 to 220P.	0.2	DVT
6	SB_INT_FLASH_SEL# 改為EC可以控制.	28	Add R594.	0.2	DVT
7	解 M插AC電源, LED會閃一下的問題.	41	Add R586,R589,Q5,Q12 change to 2N7002.	0.2	DVT
8	增加+1.5VS, +2.5VS, +0.9V 放電線路.	41	Add R587,Q34(+2.5VS), R588,Q35(+1.5VS), R604,Q36(+0.9V).	0.2	DVT
9	1W窗.	41	Add C658 0.1uF	0.3	PVT
10	Sometimes run S3 test program will interrupt .	37	Change R100 to 47K(Ori : 100K)	0.3	PVT
11	改 ?+2.5V_LAN Power.	26	C281 change to 10uF	0.3	PVT
12	改善 LAN 訊號品質 ?	27	Change R387,R390,R391,R395,C494,C500 placement to near Transformer.	0.3	PVT
13	減少 Speaker 訊號增益(預留).	39	Add R606(0 ohm),R607(0 ohm),R608(47K未上),R609(47K未上)	0.3	PVT
14	Add Camera Connect.	31	Add R605,C657,JP35	0.3	PVT
15	Bluetooth 加 chock.	38	Add L65	0.3	PVT
16	For EMI request	15	Add C330	0.4	PVT2
17	JP25 5-in-1 connector Spec update (Pin18 from NC to SD-GND)	33	Add R610	0.4	PVT2
18	Modify Package for Lead-free part	41	Modify C658 package from 0402 to 0603	0.4	PVT2
19	Reserve	28	Add R611, R612, EC_Pin-100	1.0	MP
20	for solve MS detect issue	33	Remove C197	1.0	MP