

Compal Confidential

HBL51 Schematics Document

Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M

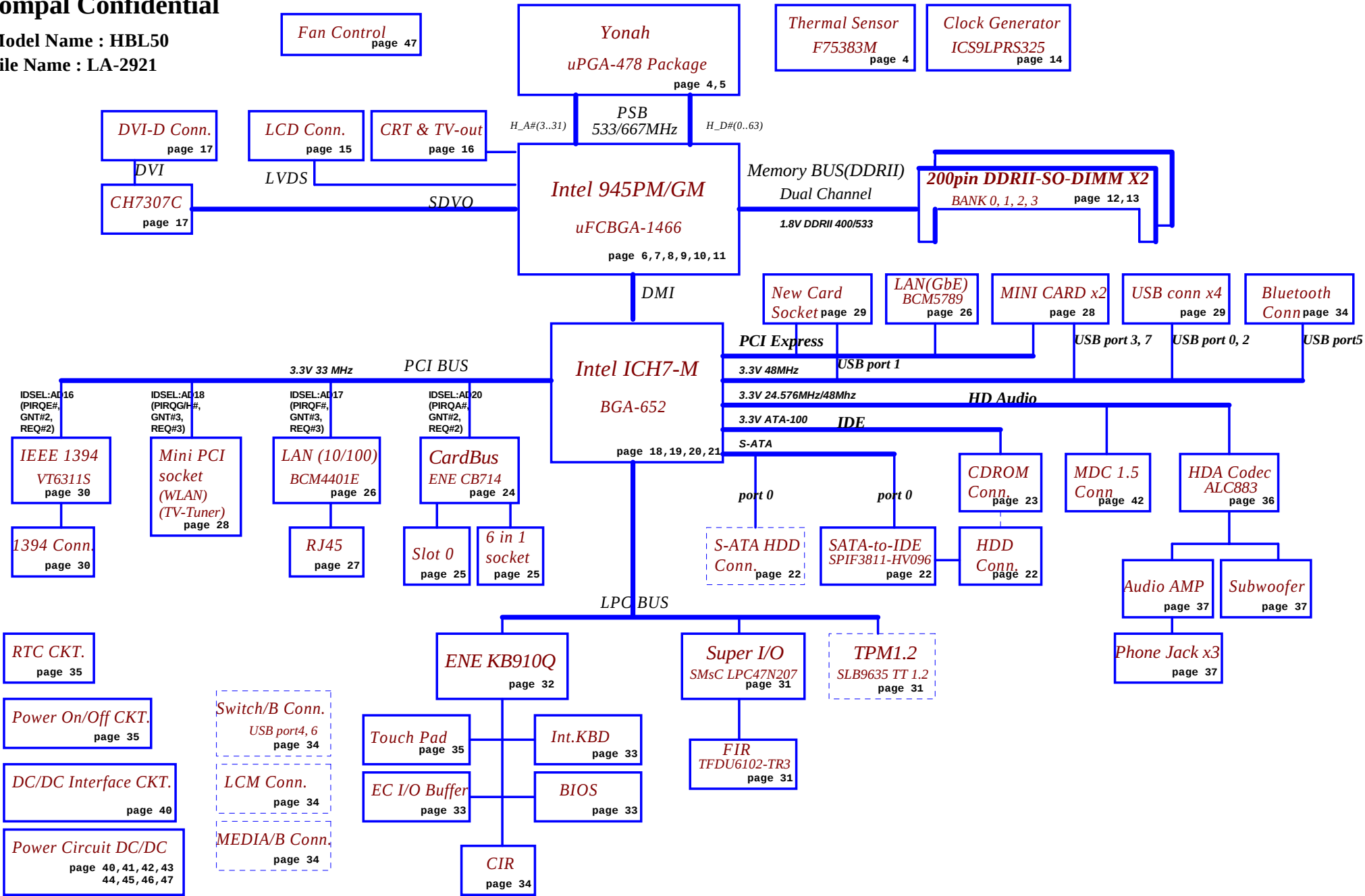
2005-11-03

REV: 0.2

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Model Name : HBL50
File Name : LA-2921



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

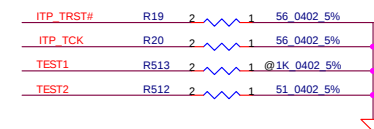
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	
1	GM
2	
3	
4	
5	
6	
7	

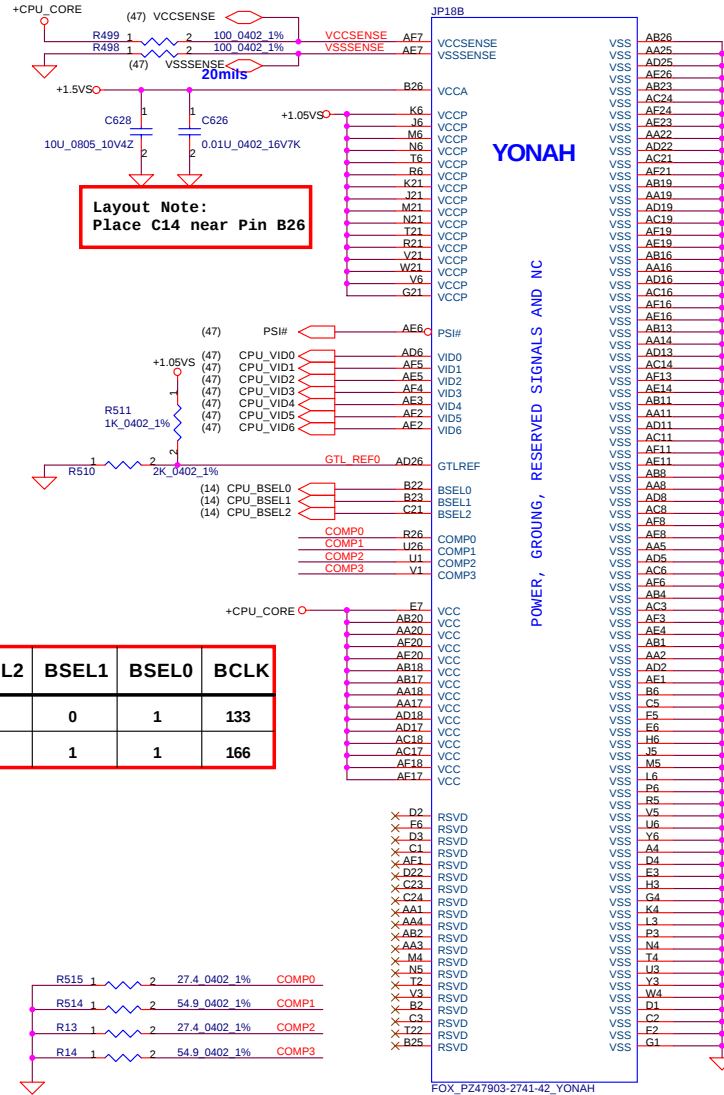
BTO Option Table

BTO Item	BOM Structure
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI CARD1	MINI1@
MINI CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
LCM	LCM@
TVOUT	TVOUT@
1394	6311S@
CARDREADER	4IN1@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@



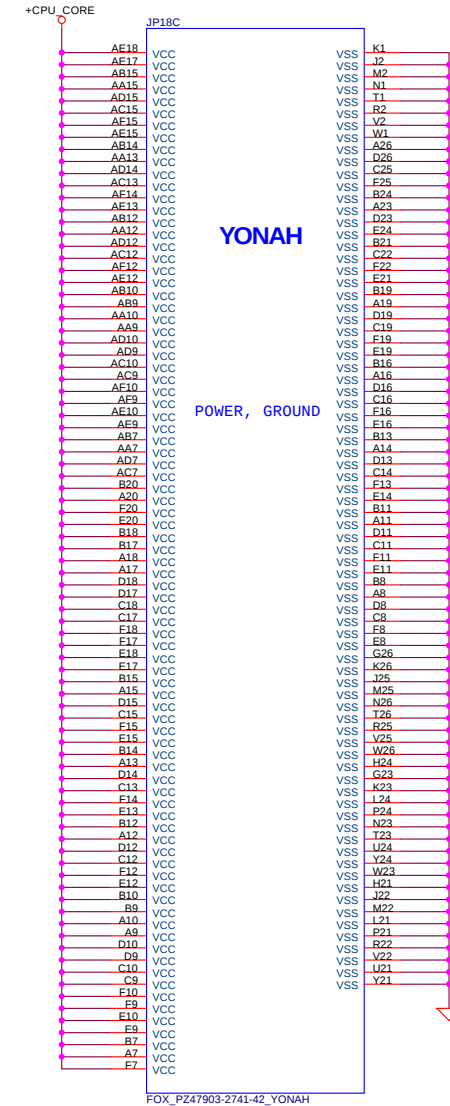
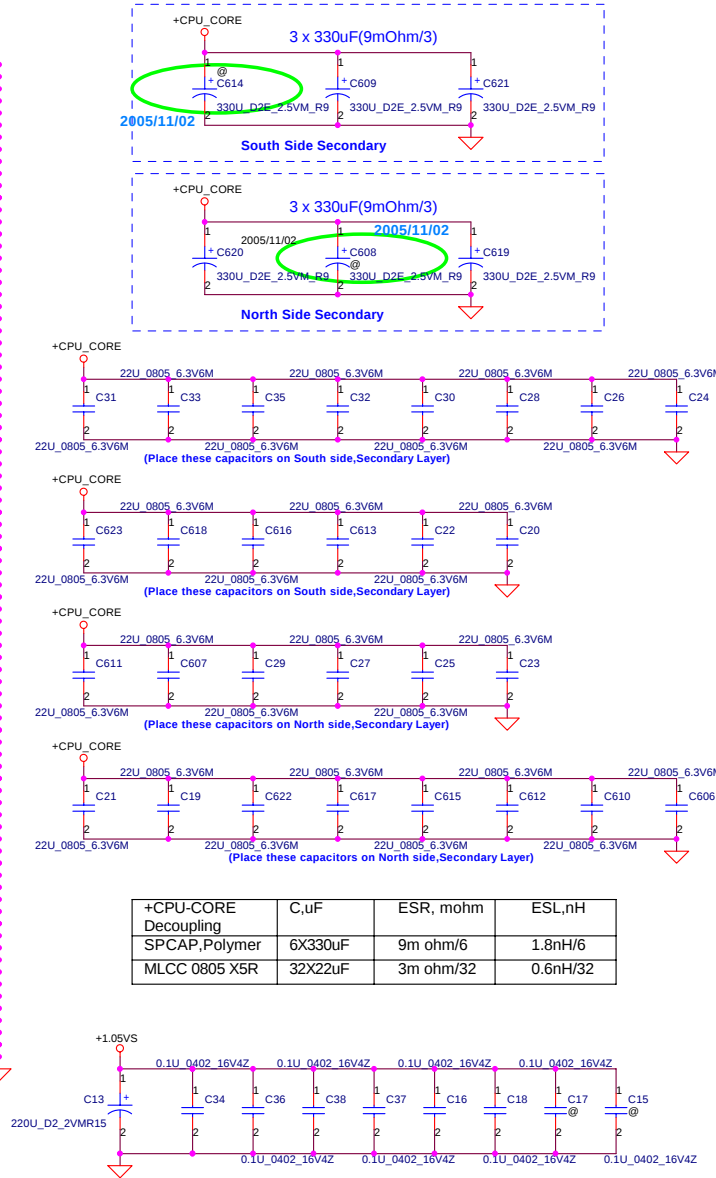
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title Yonah (1/2)			
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Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.40hms
with 50 mil spacing.
Place PU and PD within 1 inch of CPU.

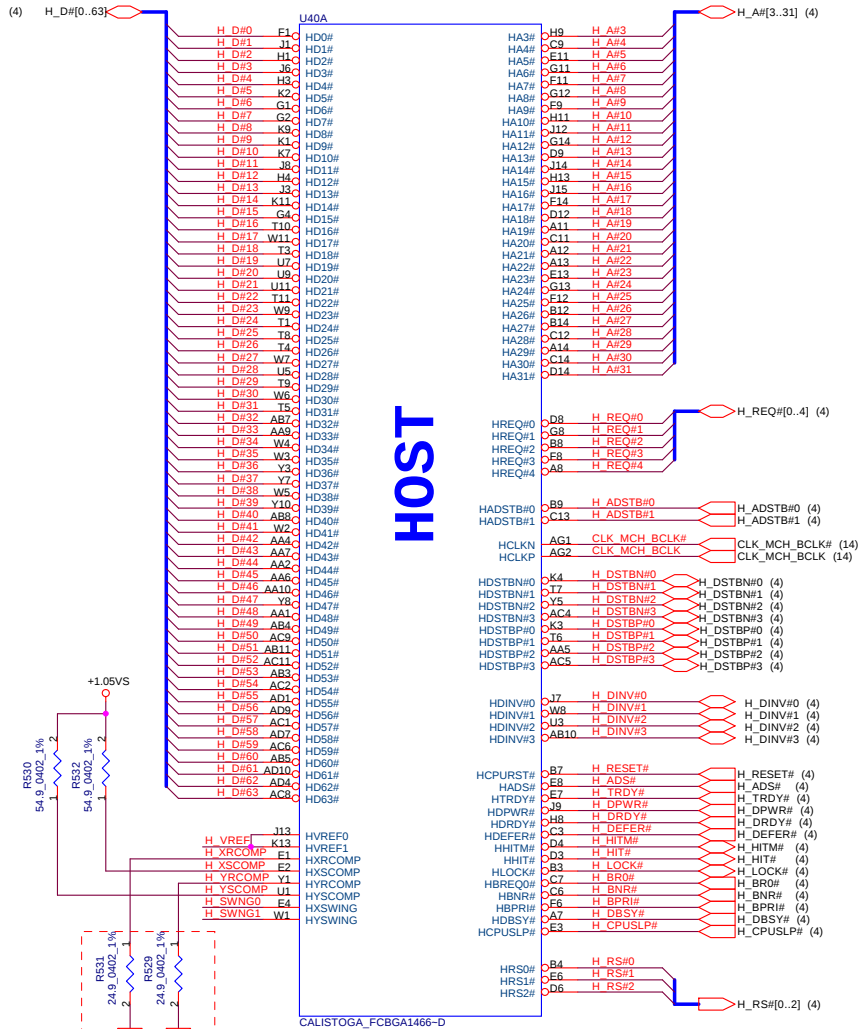


TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.40hms)
COMP1, COMP3 layout : Space 25mils (550hms)



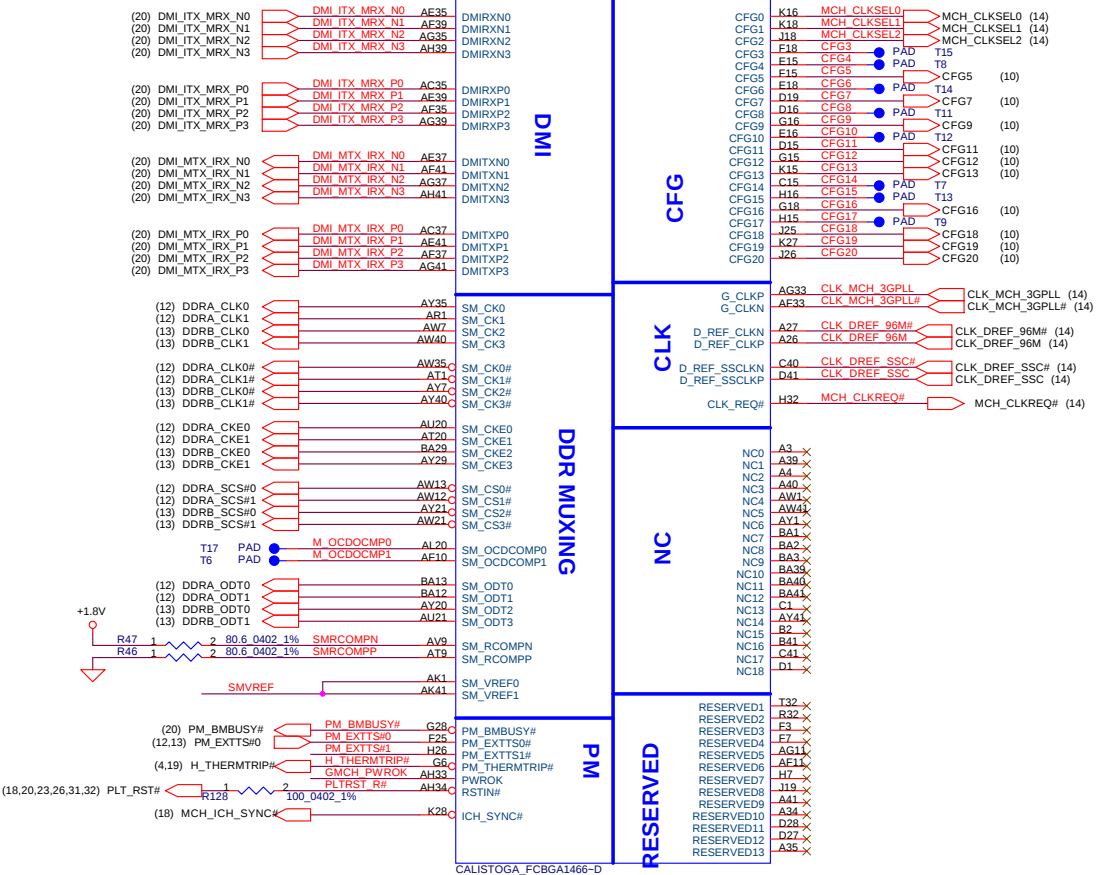
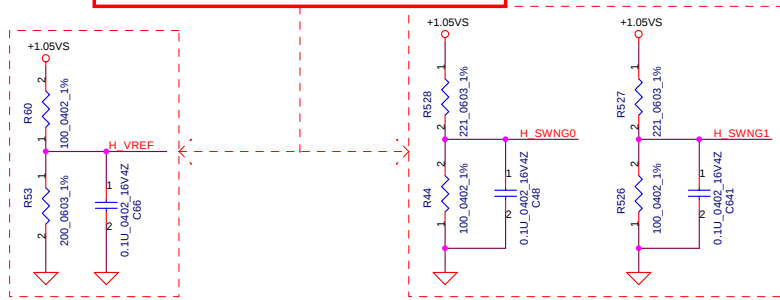
945GM(A-1)(QJ15)[ES2]: SA000005970
945GM(A-2)(QK44)[ES3]: SA000005980
945PM(A-2)(QK46)[ES3]: SA00000UV10



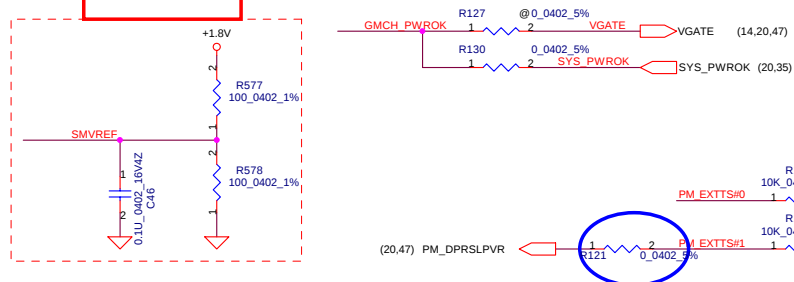
HOST

CALISTOGA_FCBGA1466-D

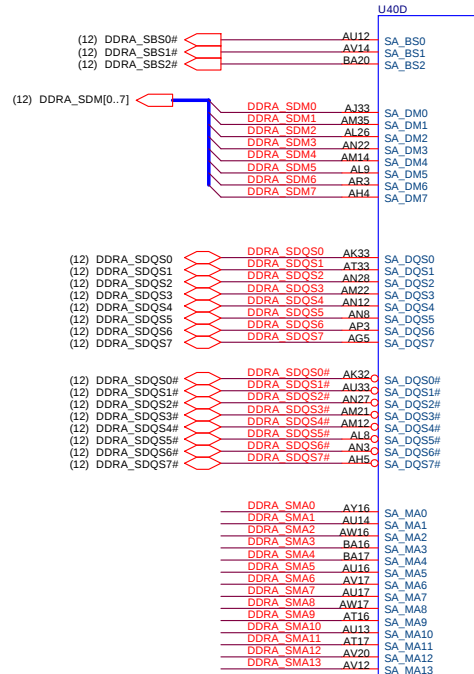
Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 10/20.



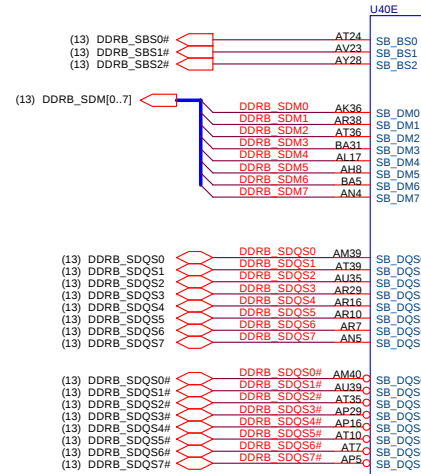
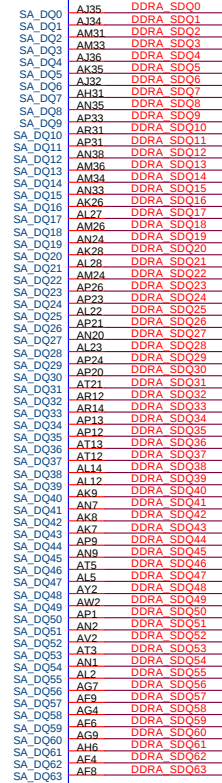
Layout Note:
SMVREF trace width and spacing is 20/20.



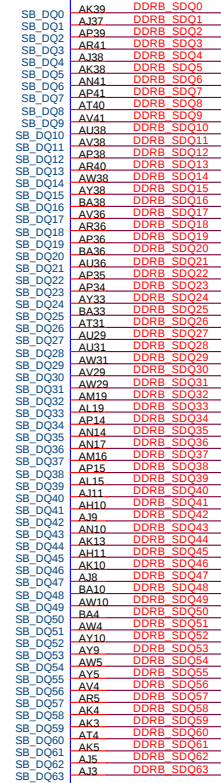
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DDR SYS MEMORY A

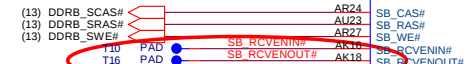


DDR SYS MEMORY B



check layout

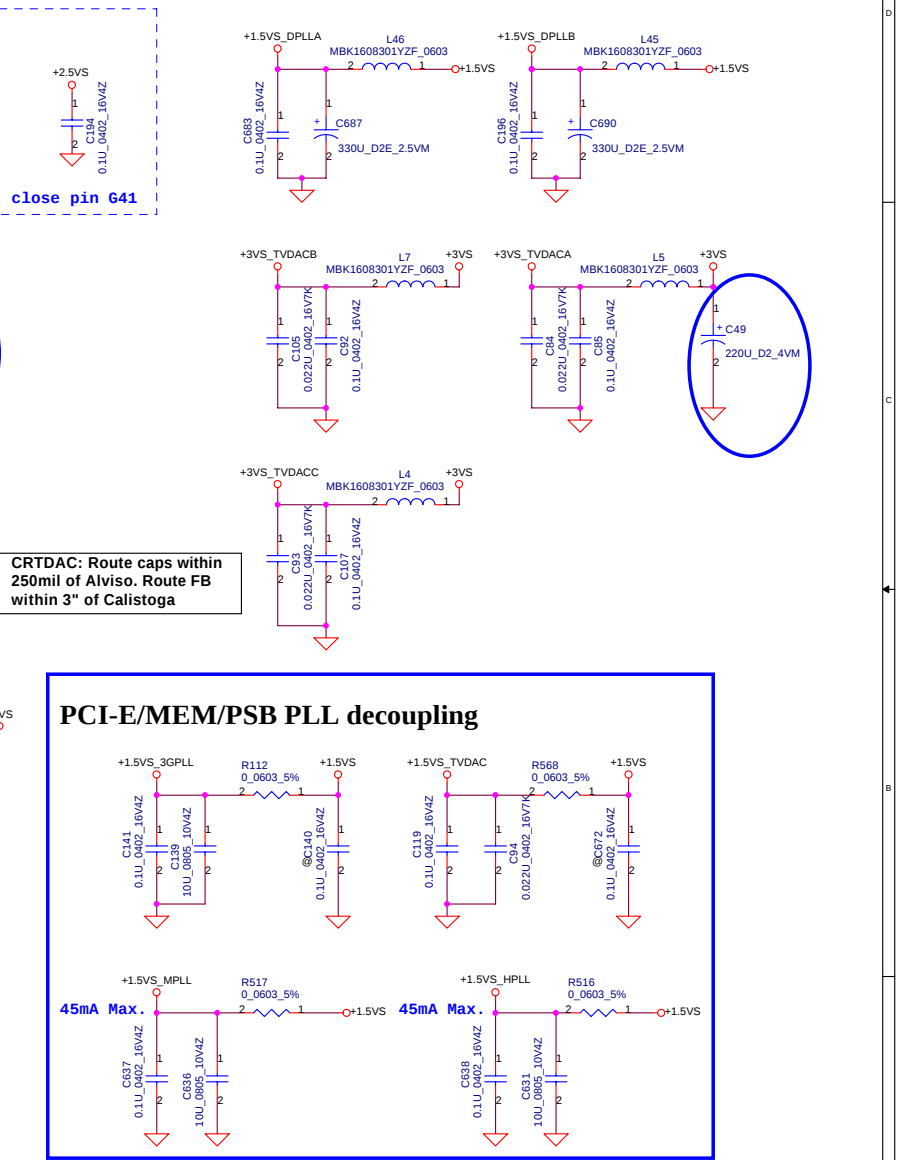
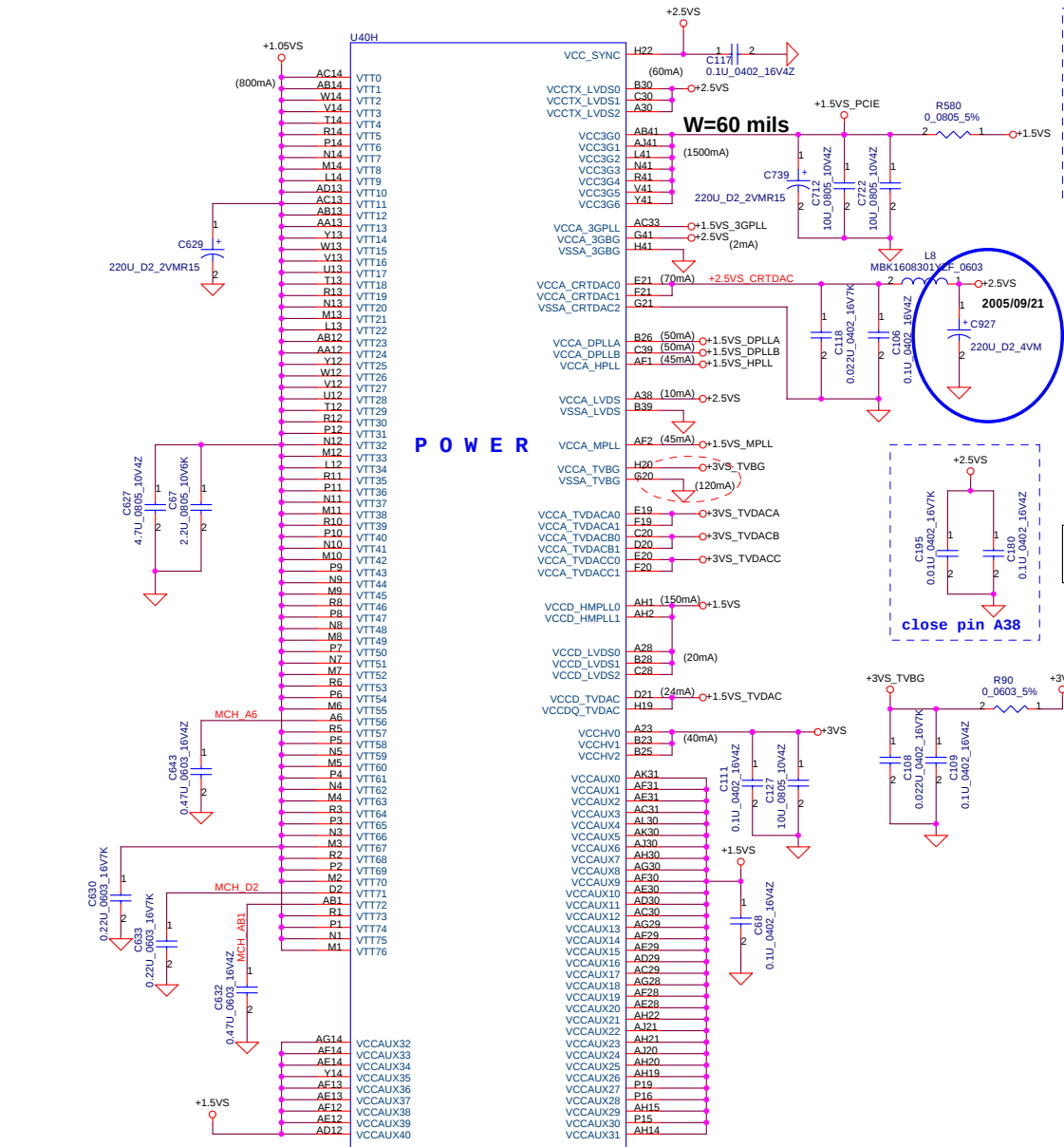
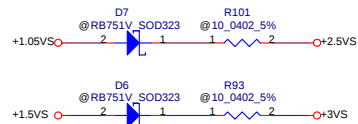
CALISTOGA_FCBGA1466-D



check layout

CALISTOGA_FCBGA1466-D

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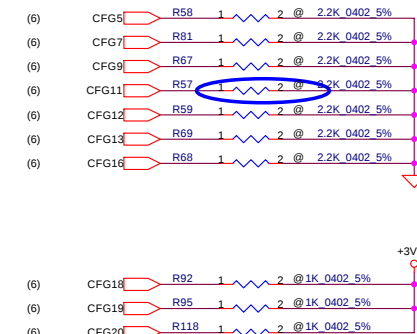
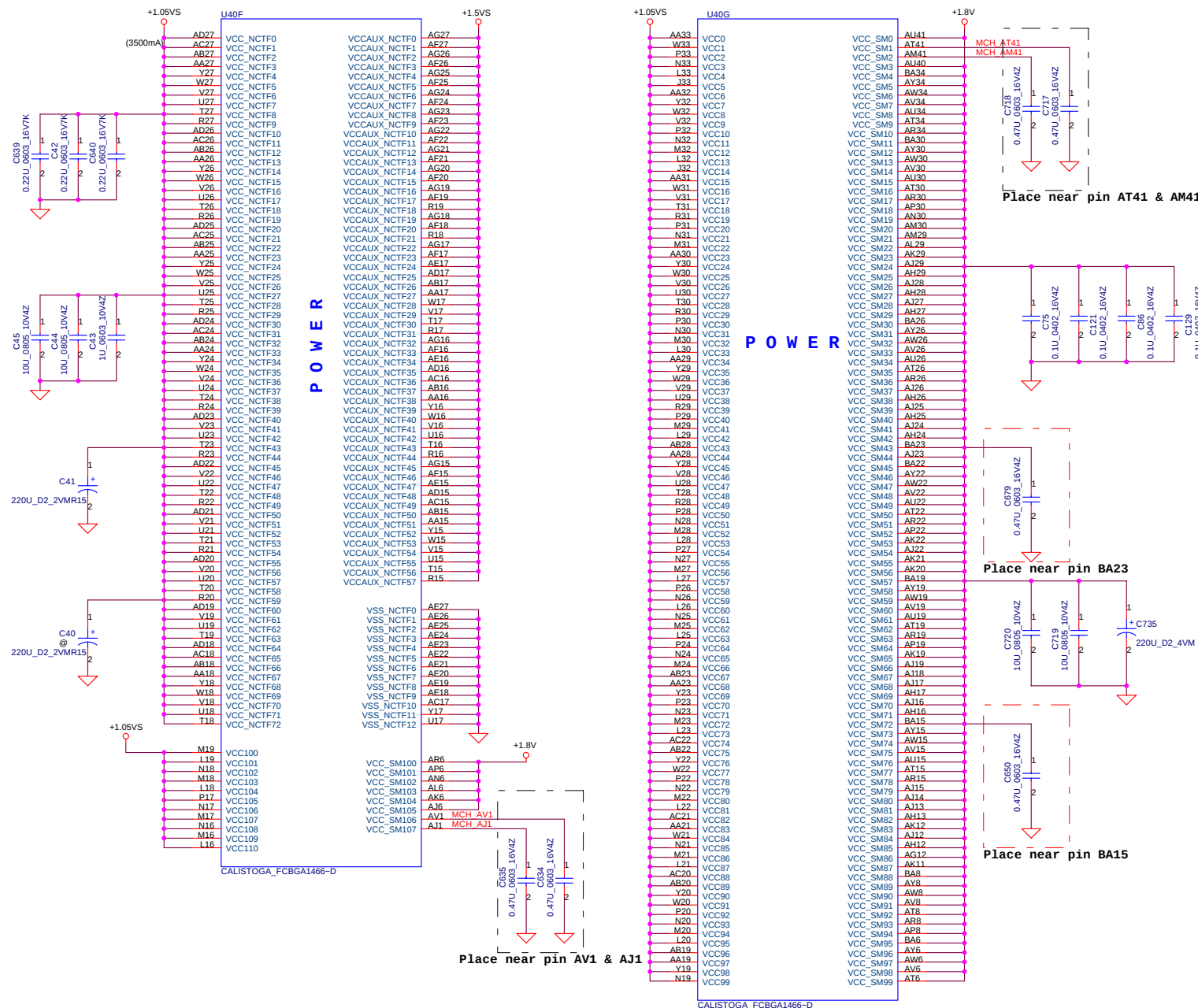


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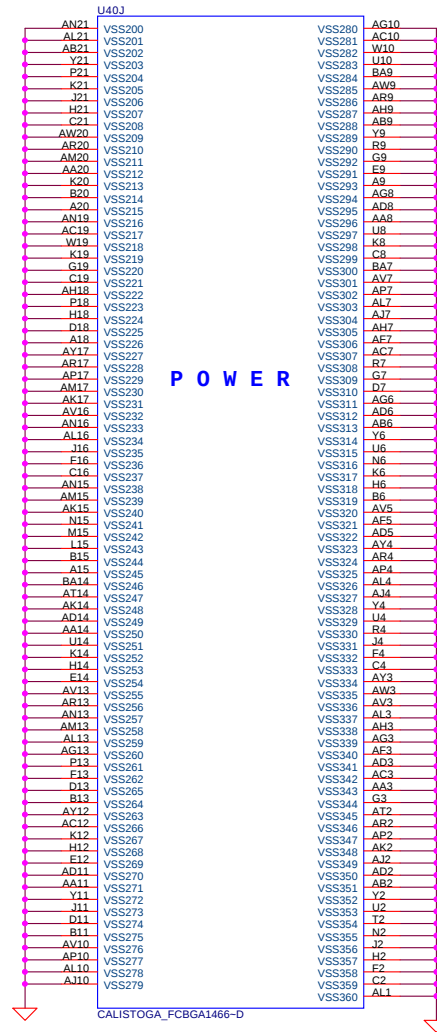
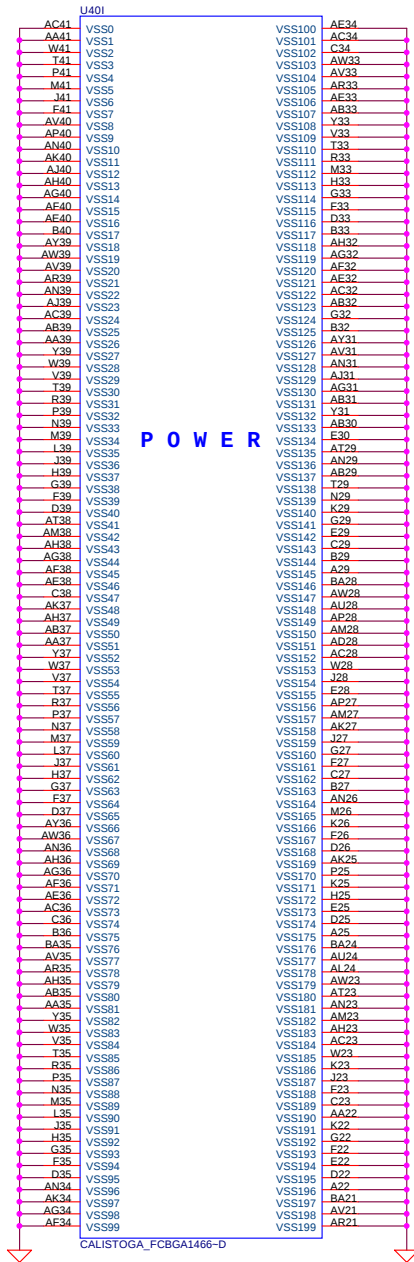
Strap Pin Table

CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

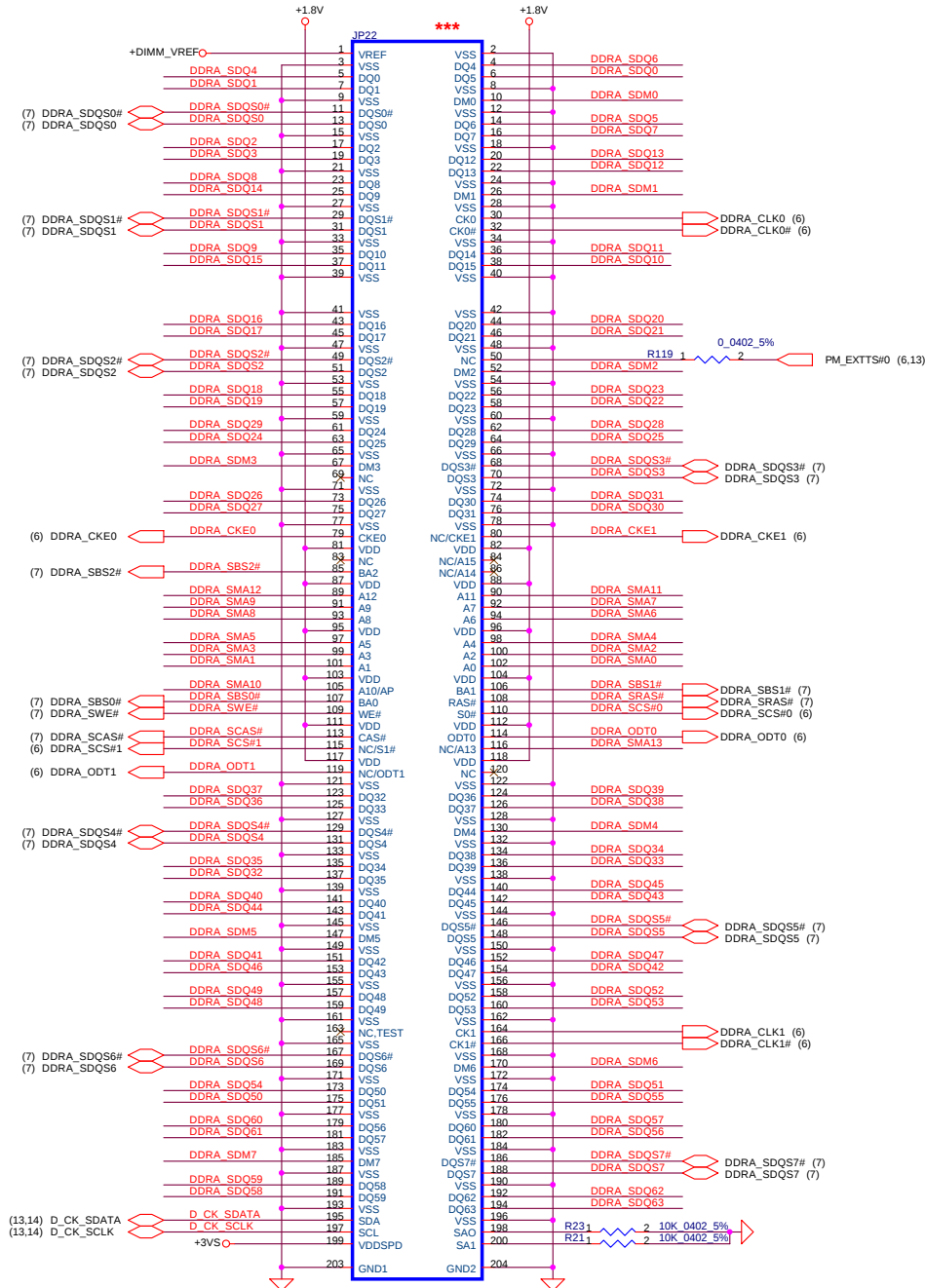
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG11	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.95V *(Default) 1 = 1.5V
CFG19	0 = No SDVO Device Present *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



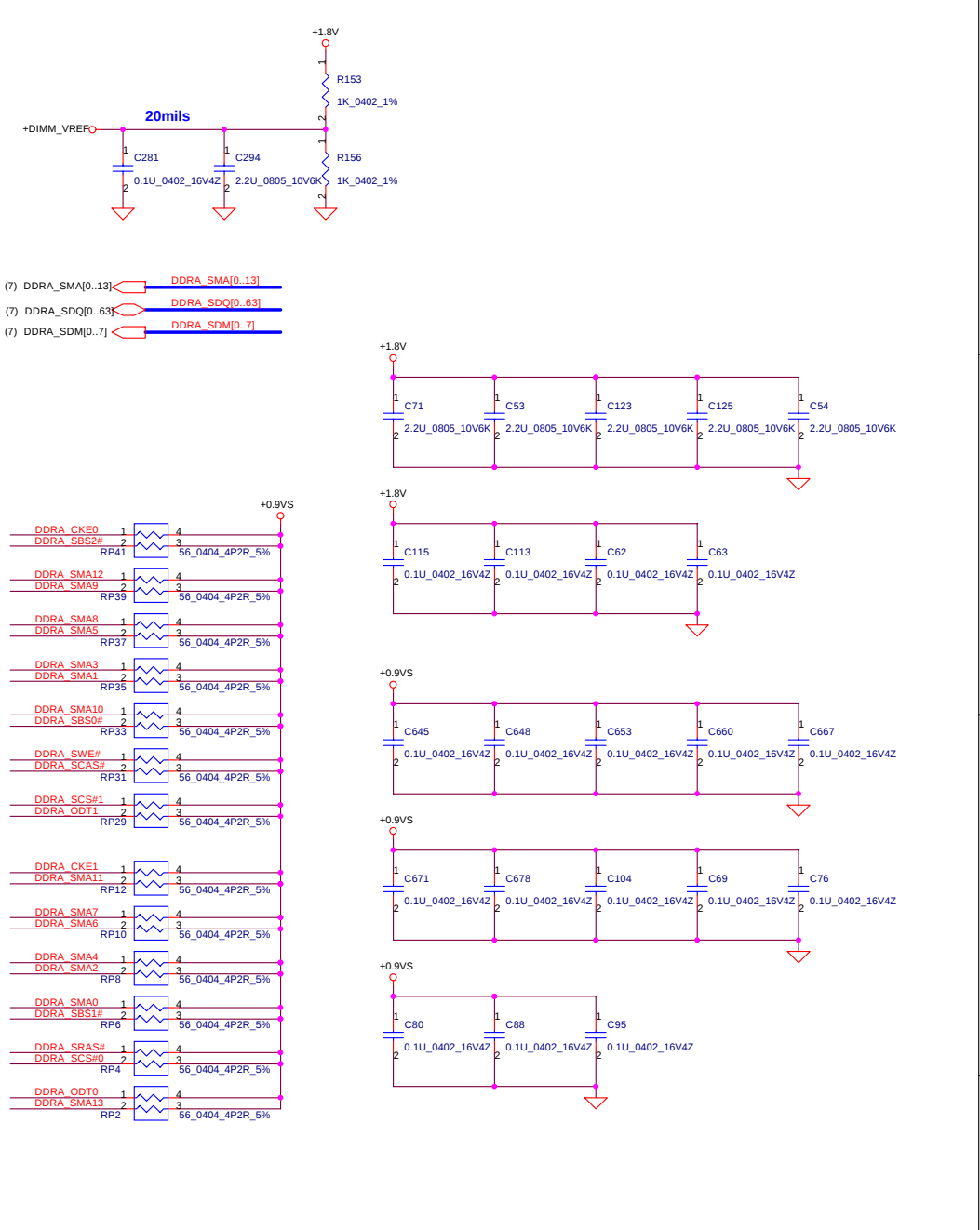
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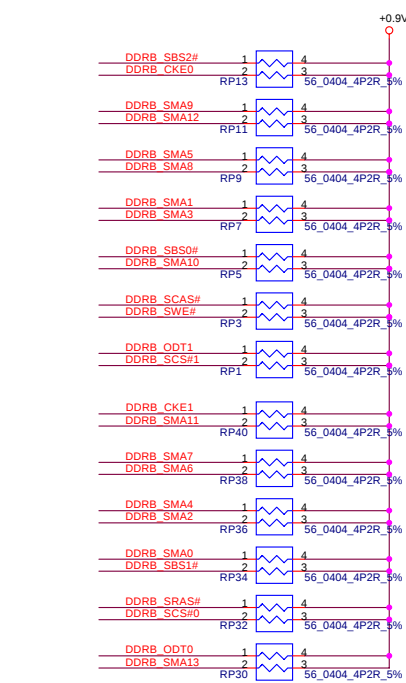
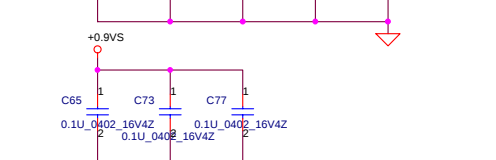
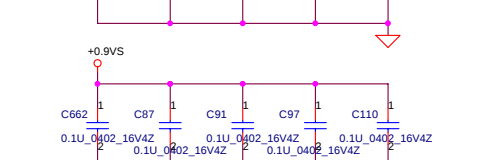
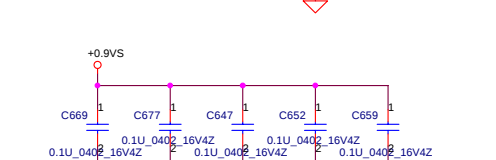
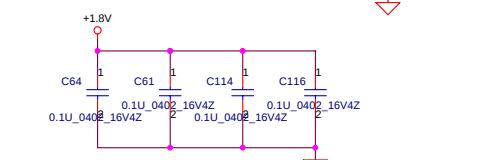
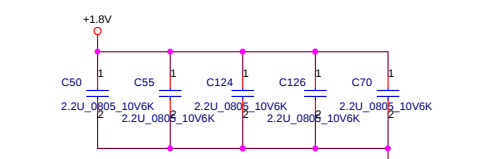
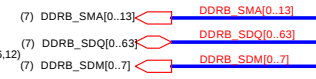
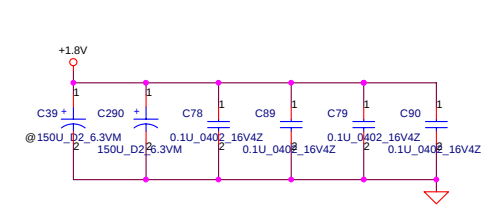
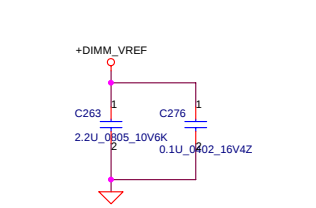
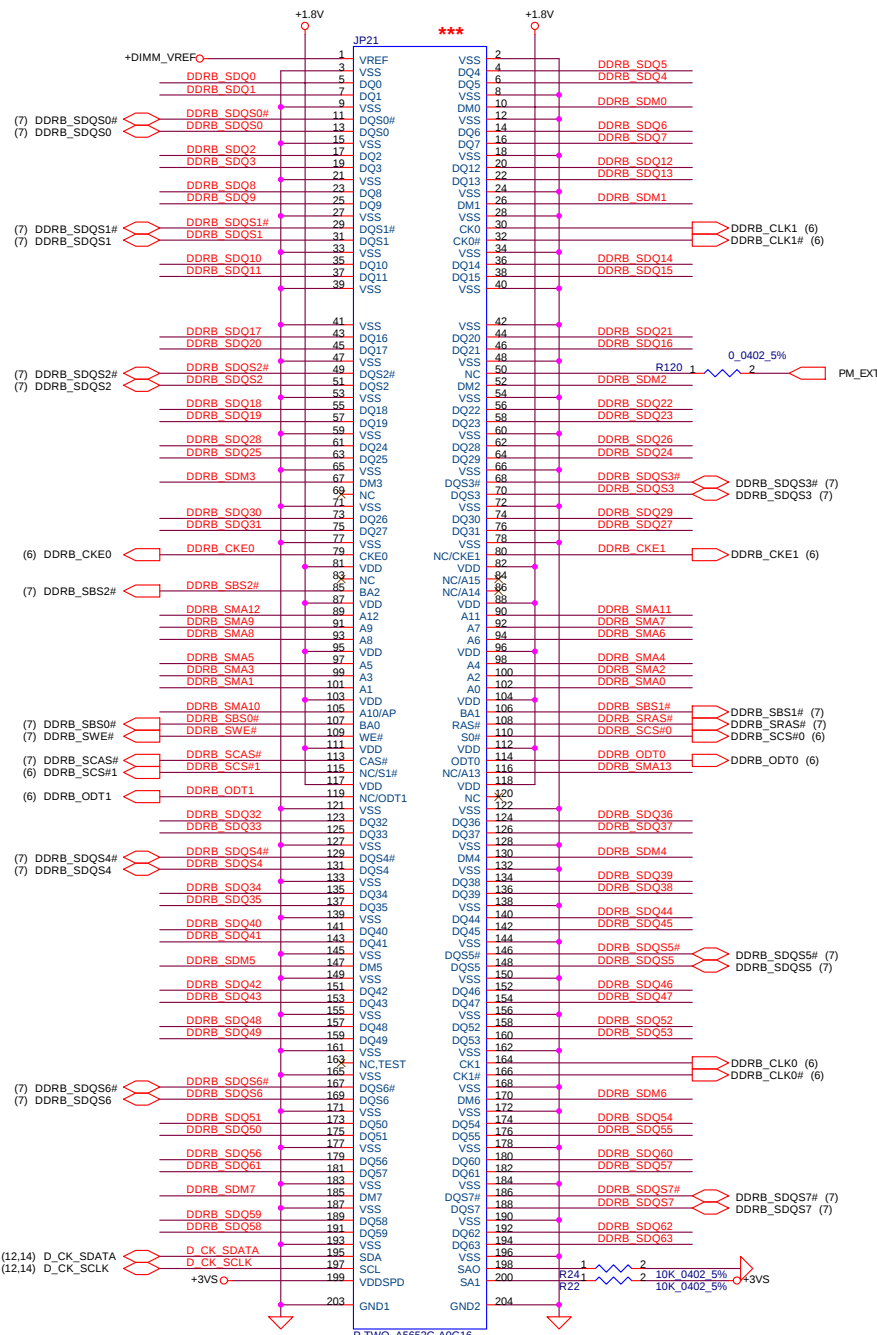


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DIMM0 STD H:9.2mm (BOT)

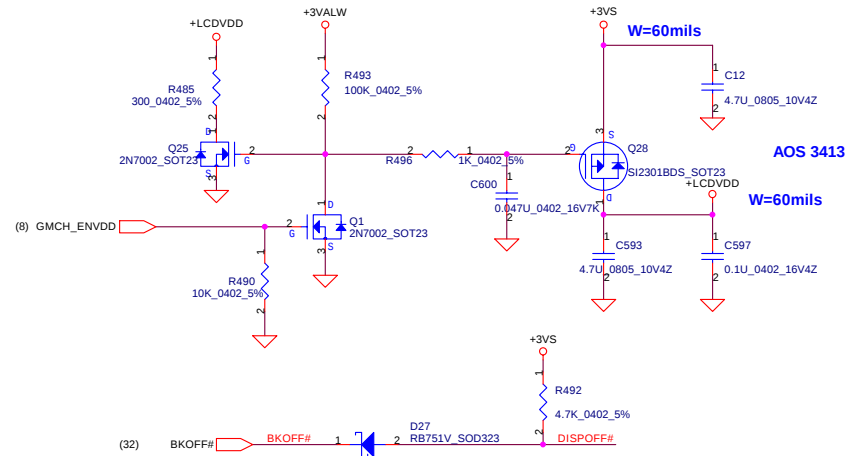




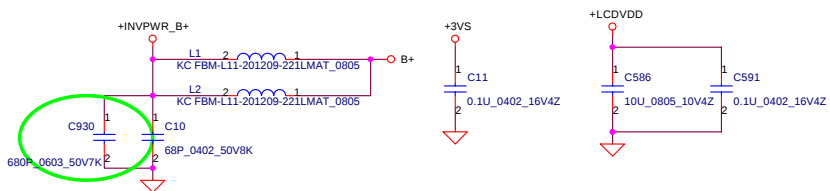
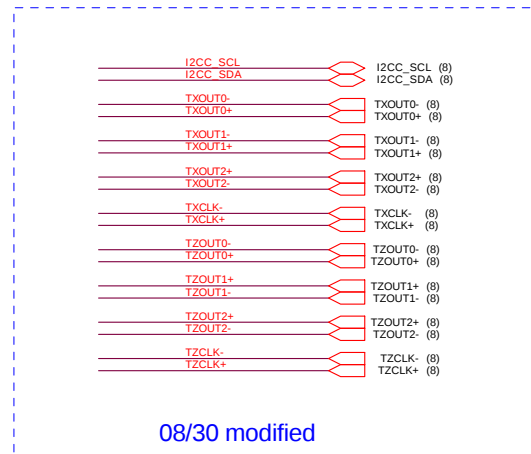
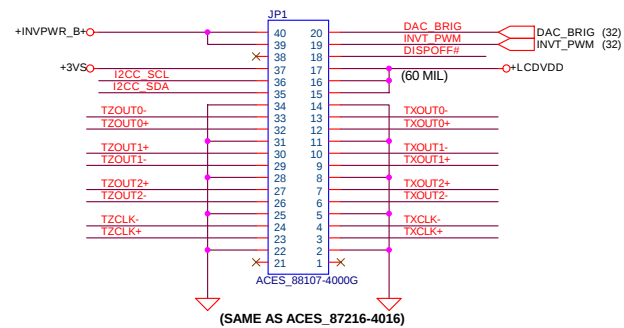
DIMM1 STD H:5.2mm (BOT)

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LCD POWER CIRCUIT

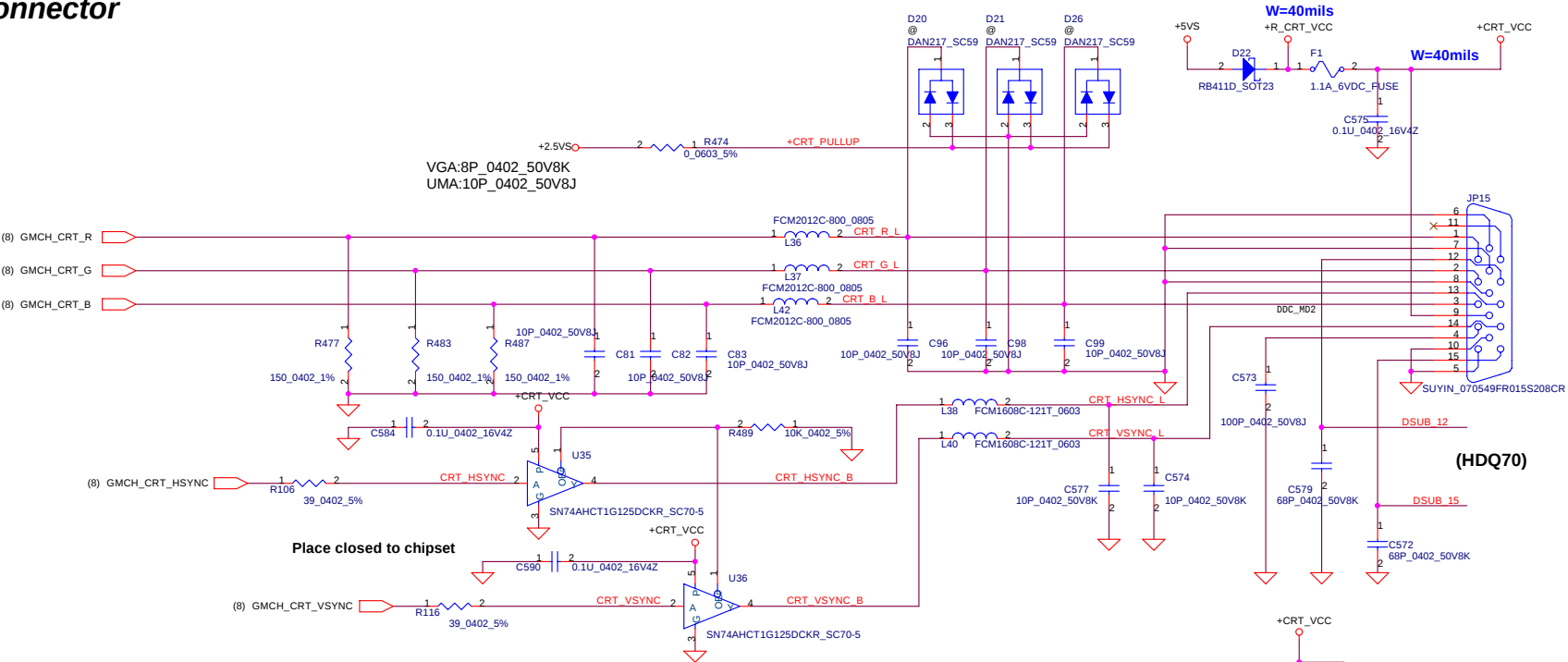


LCD/PANEL BD. Conn.

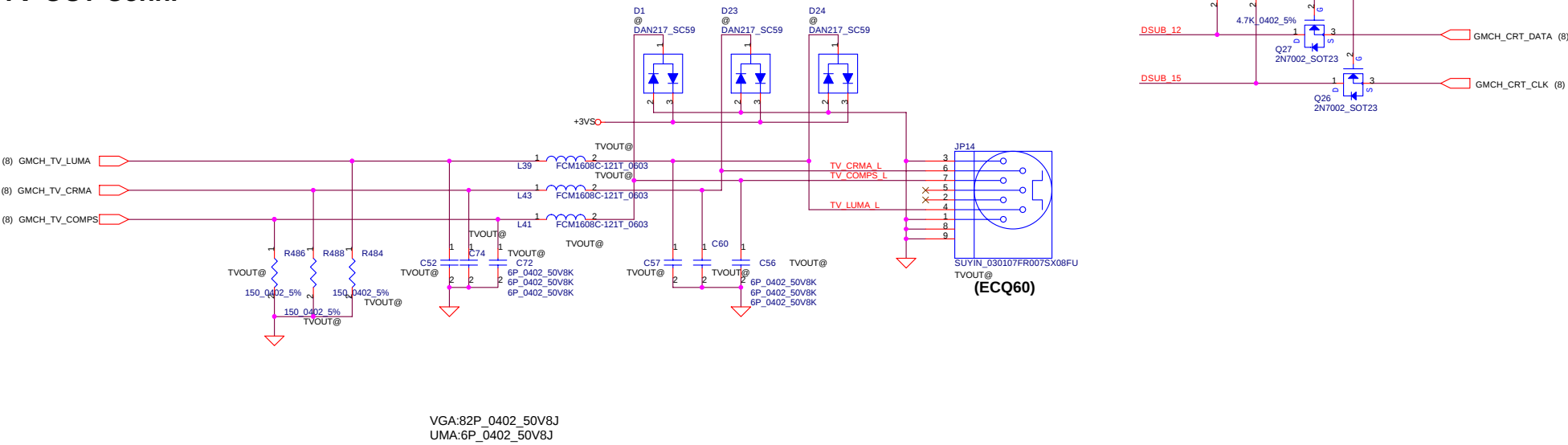


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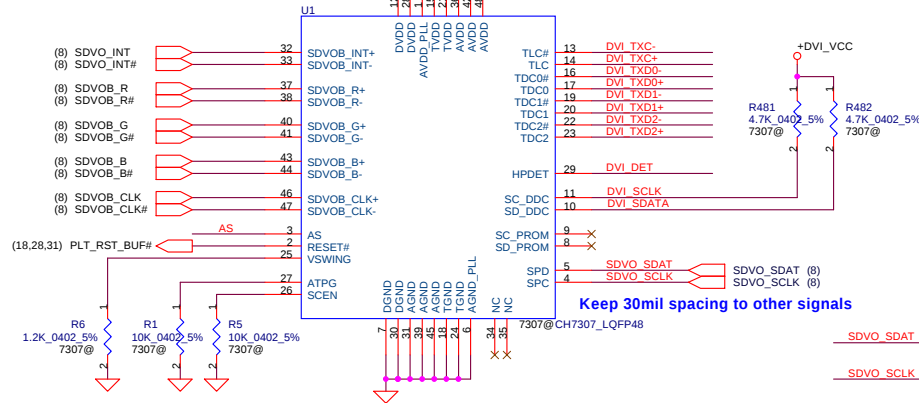
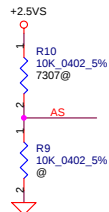
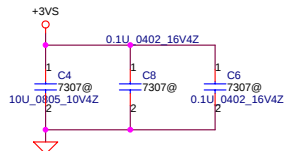
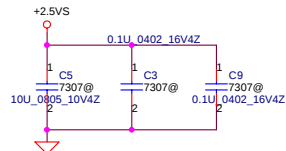
CRT Connector



TV-OUT Conn.



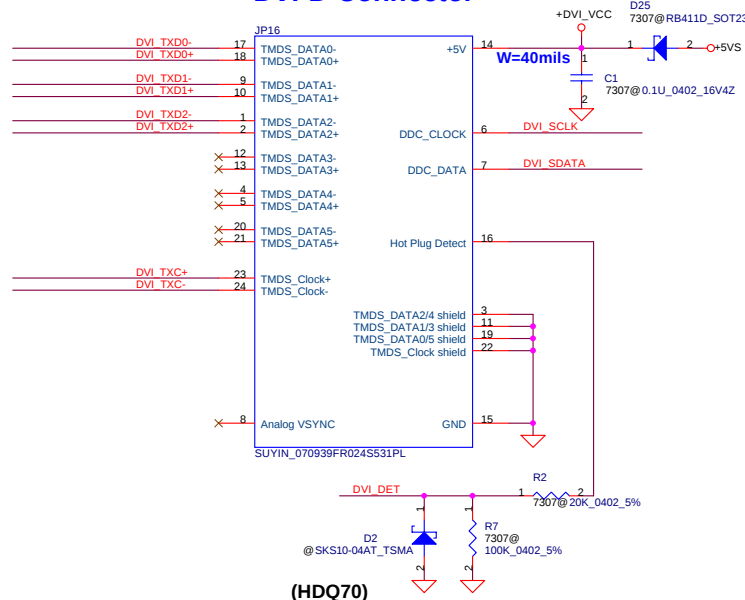
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BOM structure	DVI from SDVO
7307@	Stuff
@	No_Stuff

Keep 30mil spacing to other signals

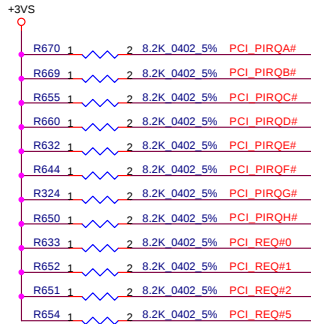
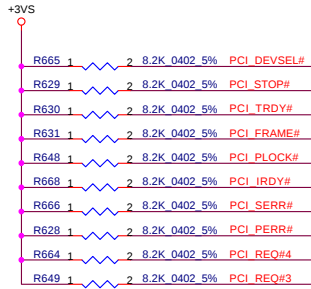
DVI-D Connector



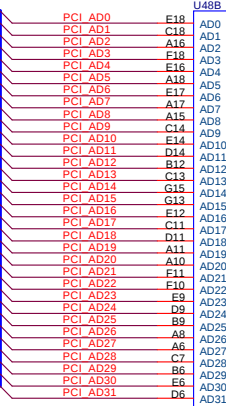
(HDQ70)

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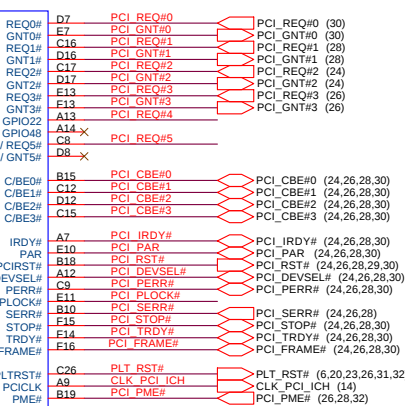
ICH7M(B-0) (QK17) [ES3] : SA00000JK30



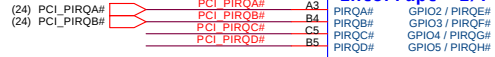
(24,26,28,30) PCI_AD[0..31]



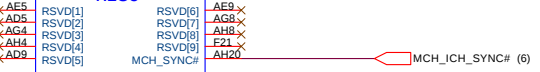
PCI



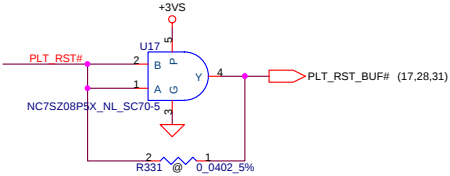
Interrupt I/F



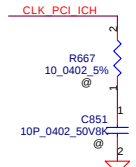
MISC



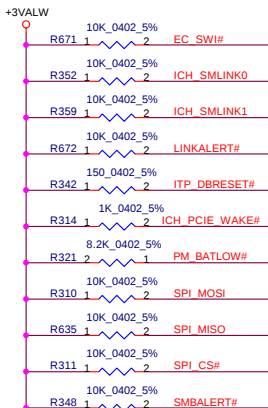
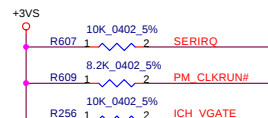
ICH7_BGA652-D



Place closely pin A9



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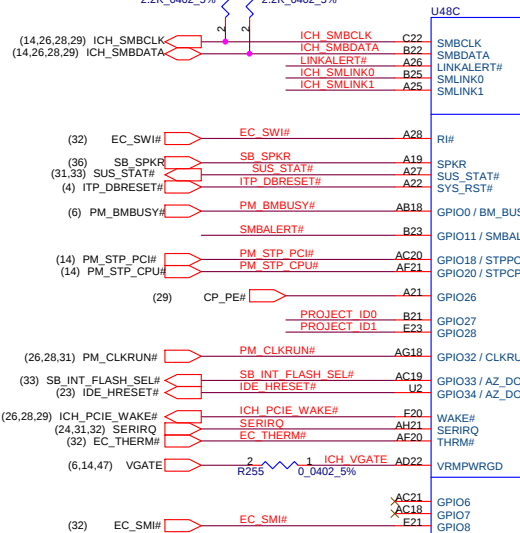
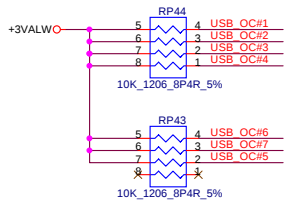
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PROJECT_ID1

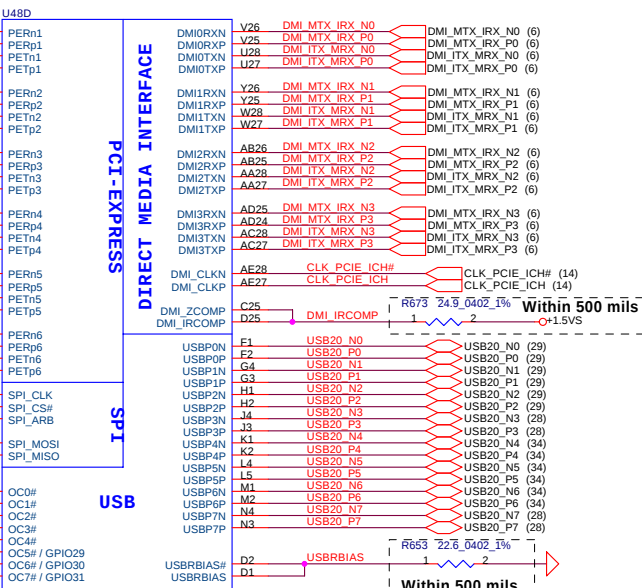
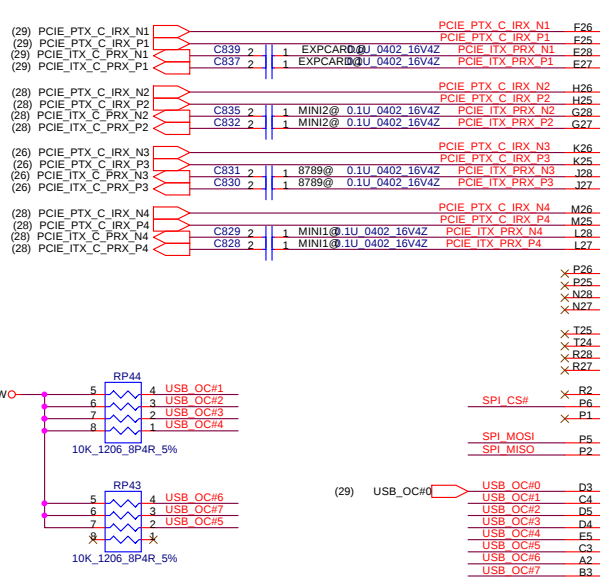
PM DPRSLPVR

SUS_CLK

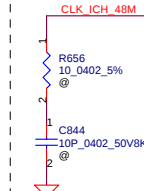
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01	Geneva
10	HBL51_PATA



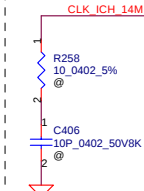
Need update symbol



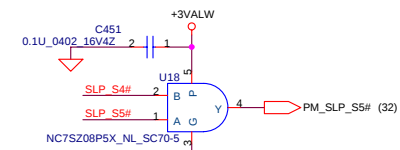
Place closely pin B2



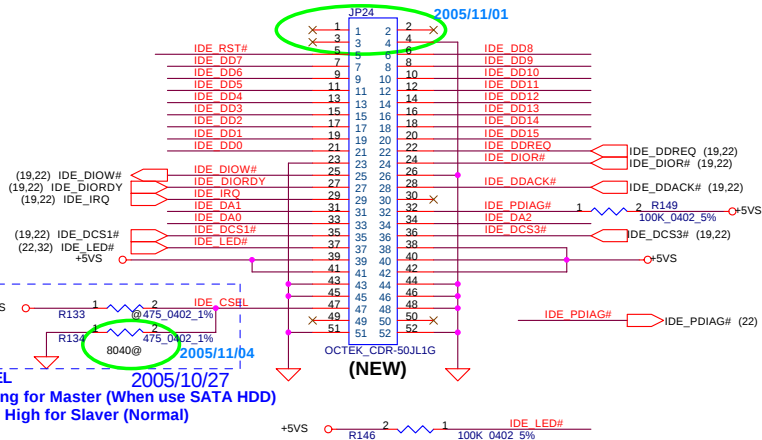
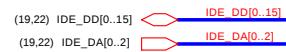
Place closely pin AC1



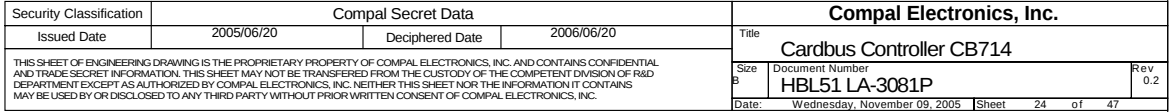
PM DPRSLPVR : Need to series a 500ohm resistor to IMVP6



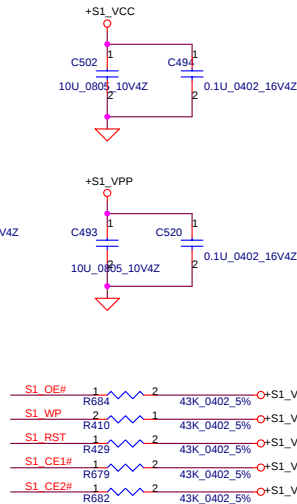
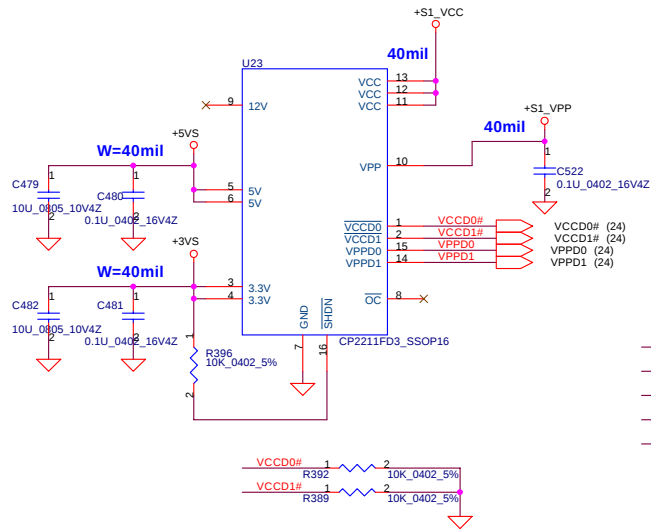
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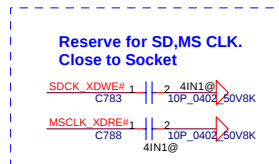
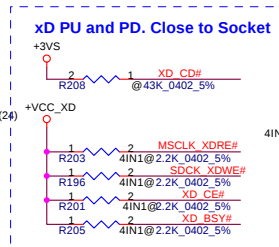
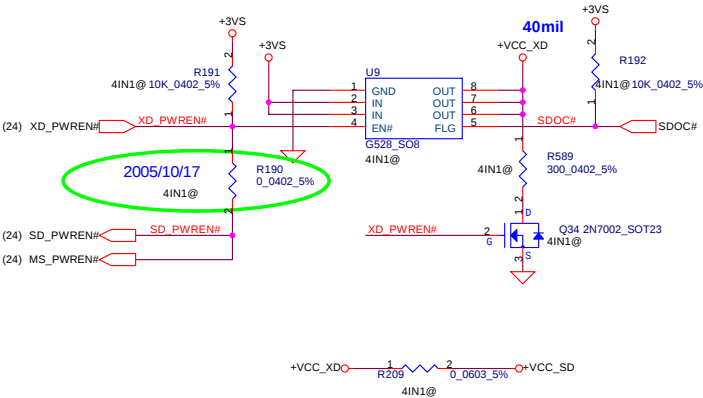
Security Classification		Compal Secret Data		Compal Electronics, Inc.				
Issued Date		2005/06/20	Deciphered Date	2006/06/20	Title	ODD & SATA HDD Connector		
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						HBL51 LA-3081P		
						Date:	Wednesday, November 09, 2005	



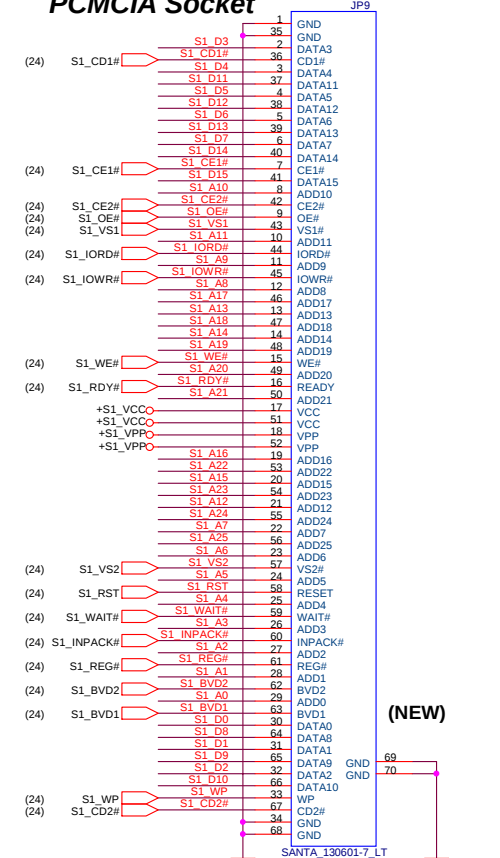
PCMCIA Power Control



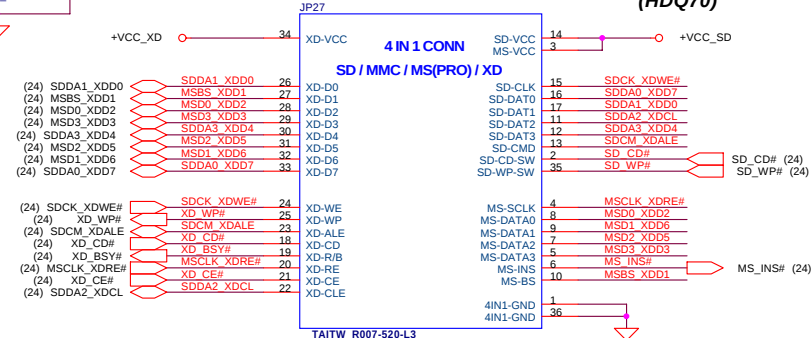
SD/MS Power Control



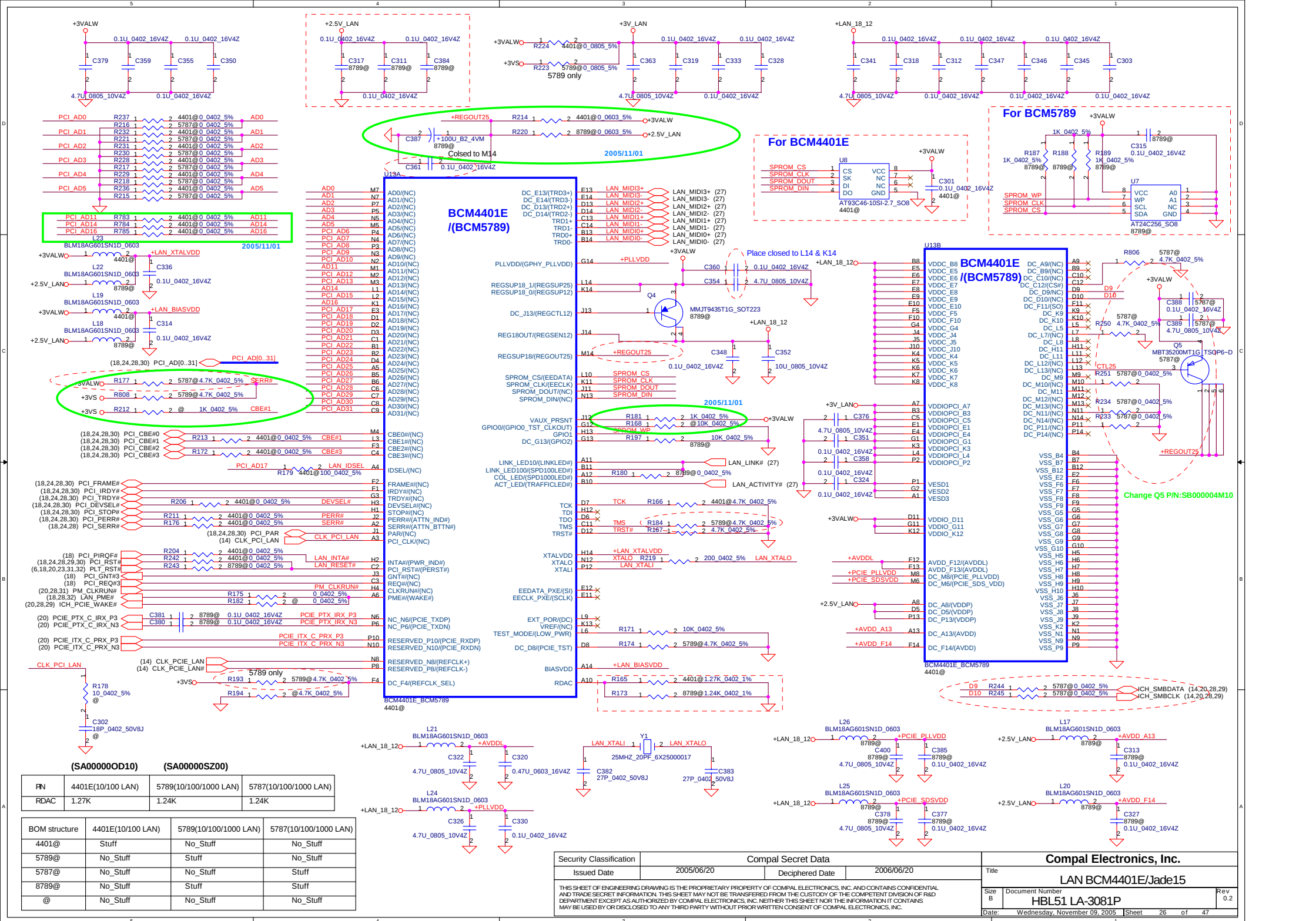
PCMCIA Socket



4 IN 1 Socket (HDQ70)

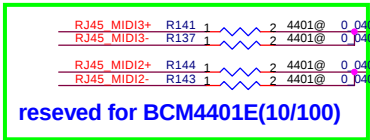


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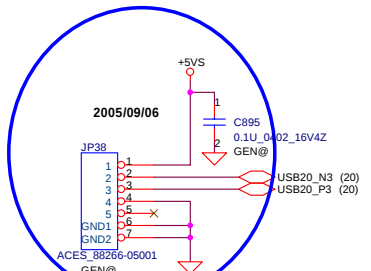
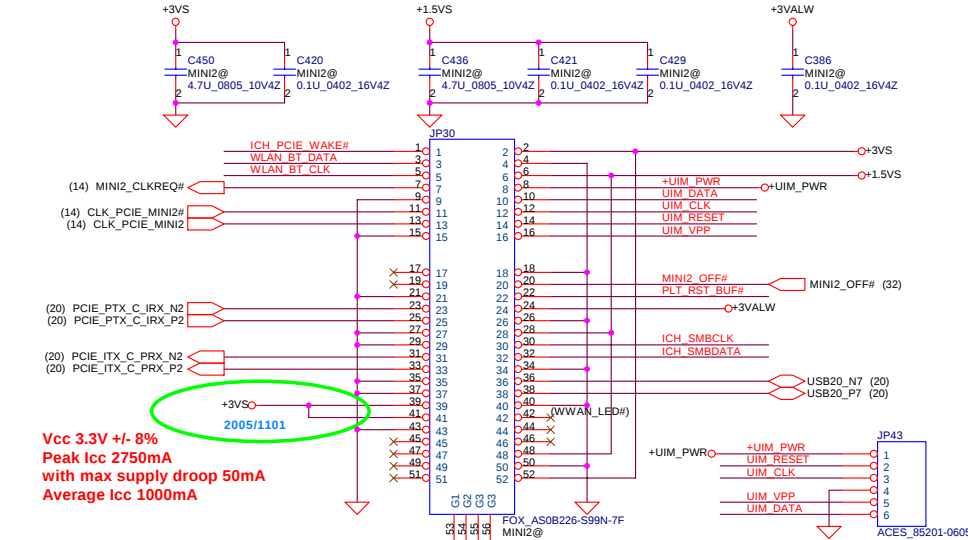
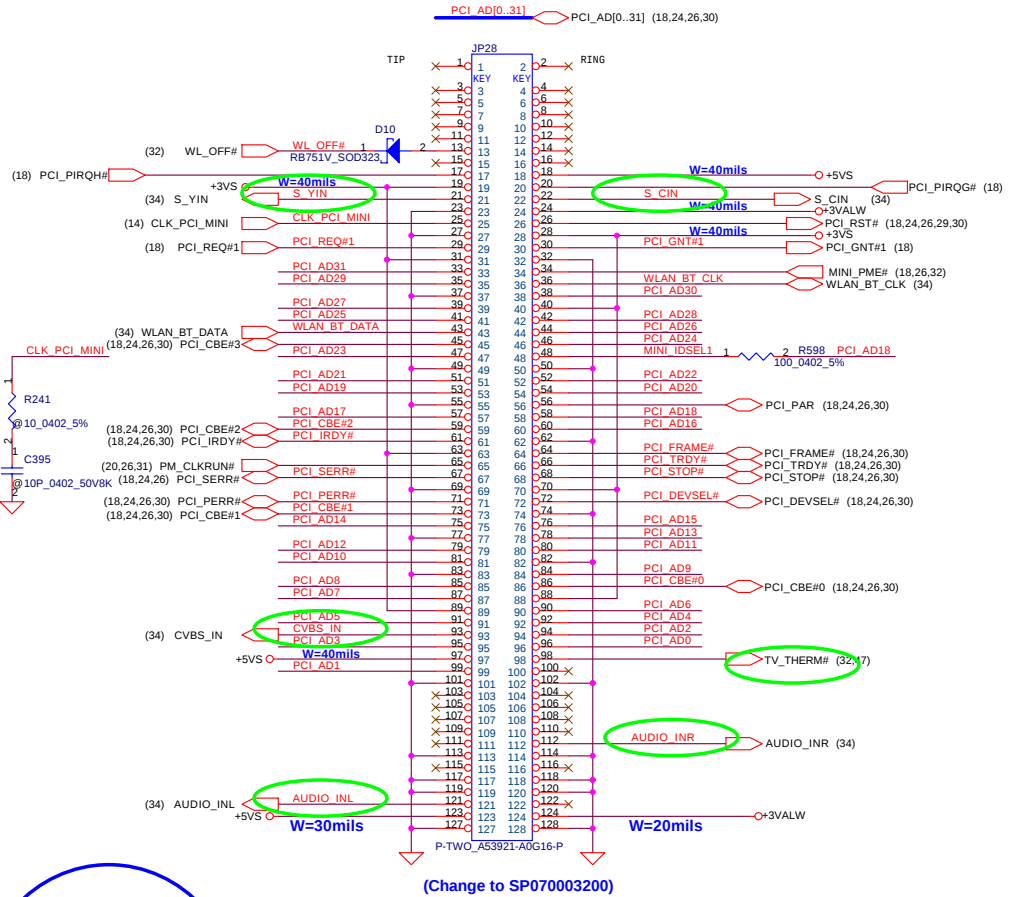
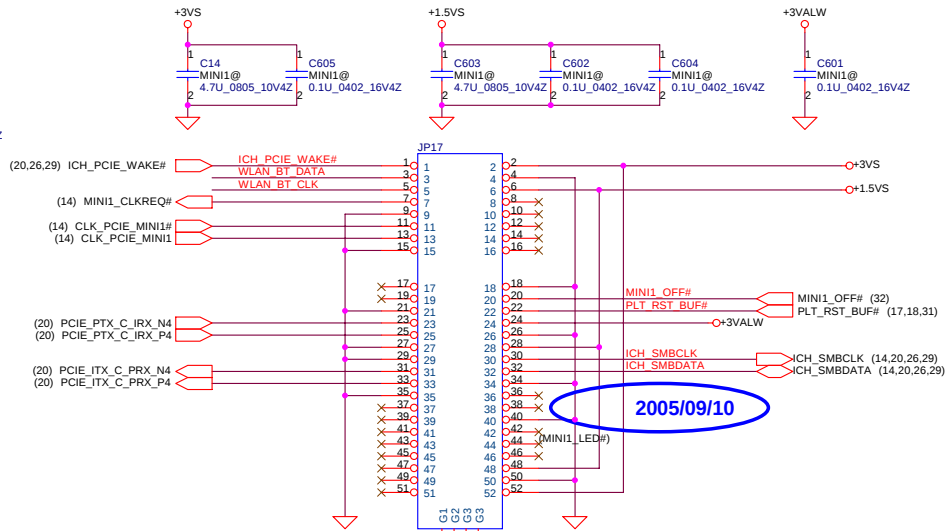
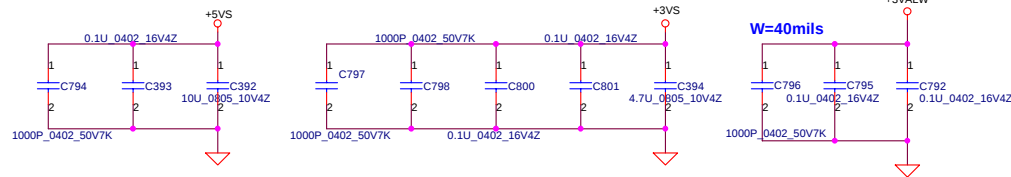


Place these components colsed to LAN chip

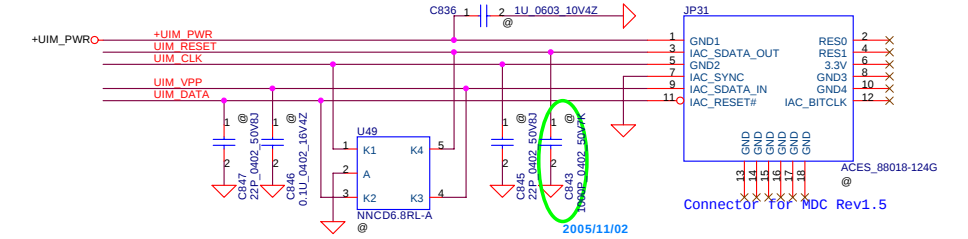
unpop when use BCM4401E(10/100)



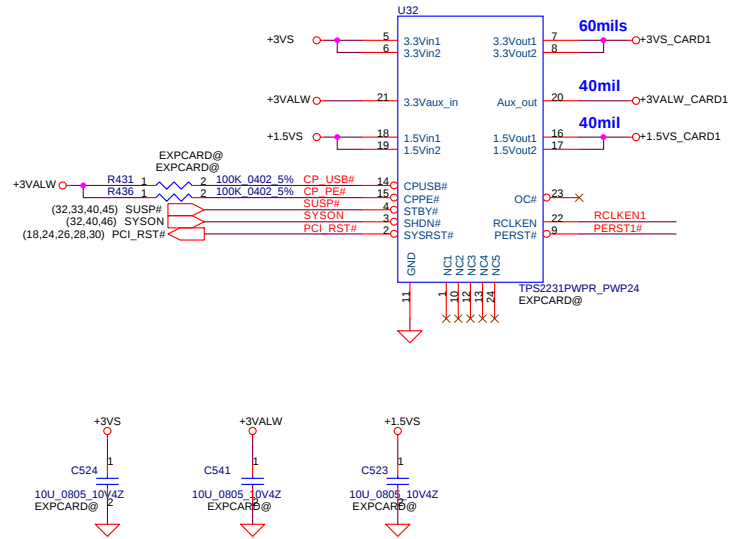
Security Classification	Compal Secret Data			Compal Electronics, Inc.			
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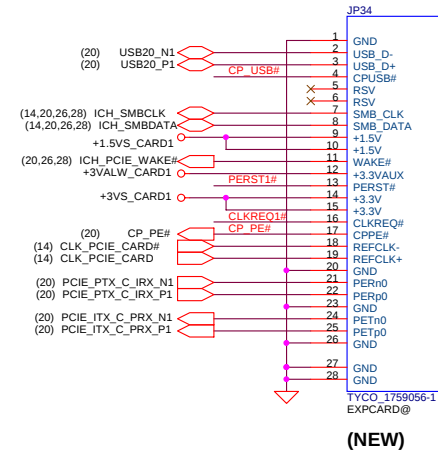
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	
+3VS	1000	750	Normal
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



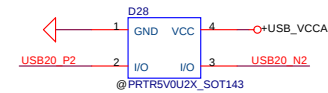
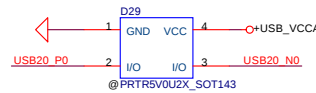
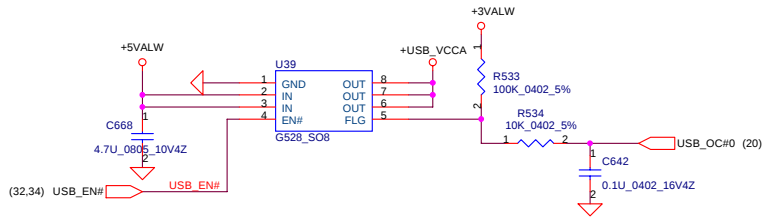
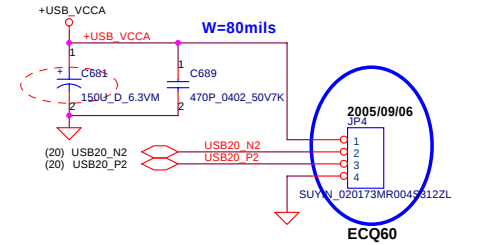
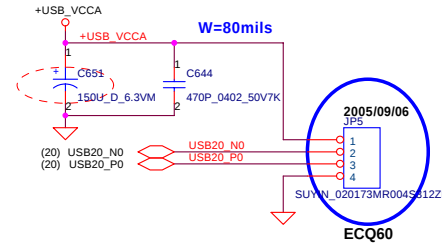
New Card Power Switch



New Card Socket (Left)



USB CONN. 1 & 2

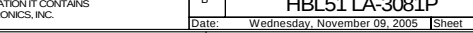
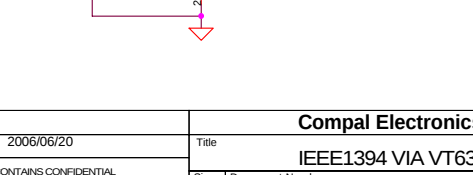
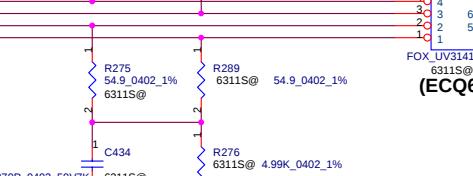
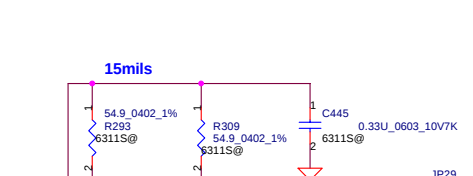
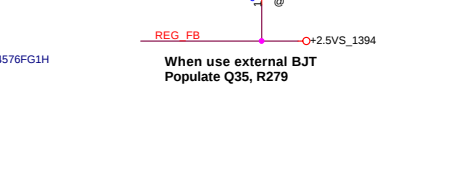
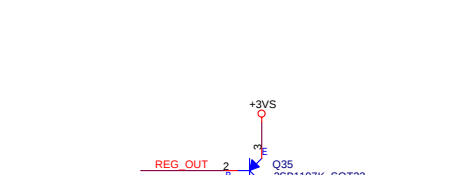
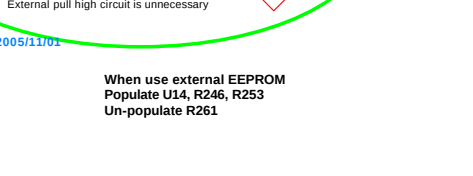
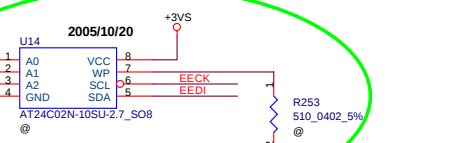
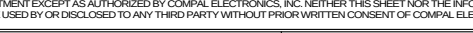
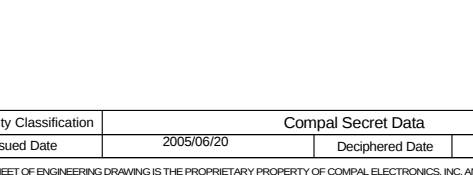
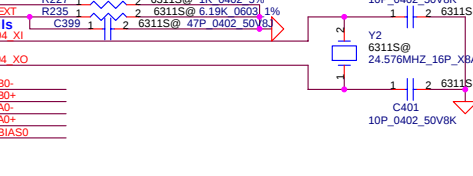
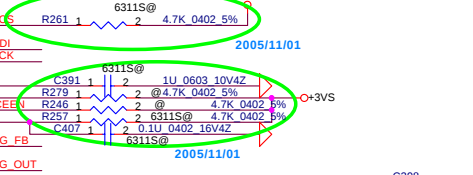
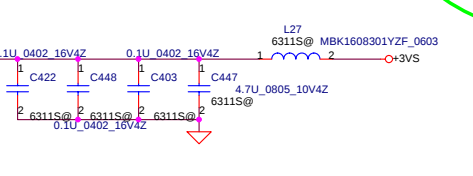
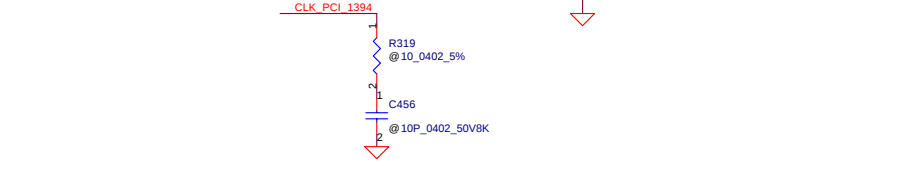
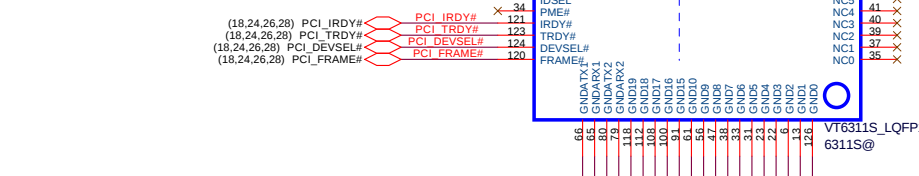
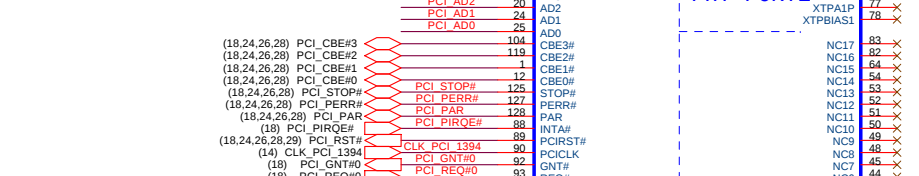
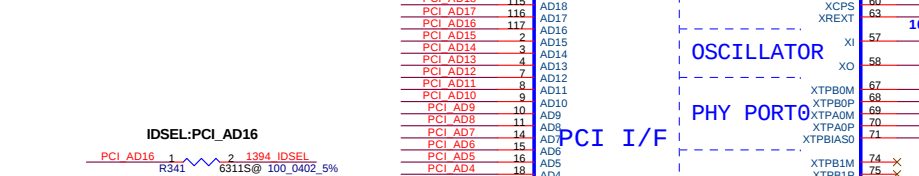
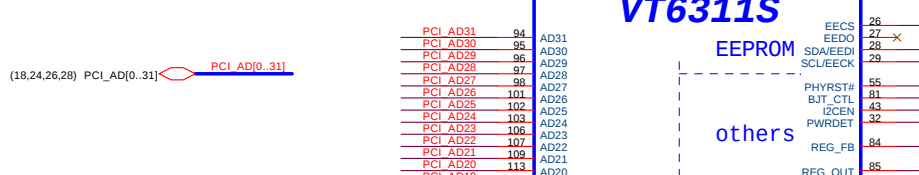
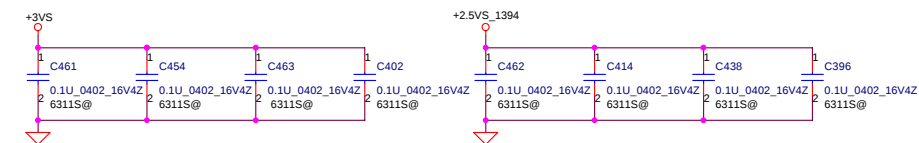


SUYIN_020173MR004G533ZR_4P

SUYIN_020173MR004G533ZR_4P

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xyaxim@hotmail.com



VT6311S

EEPROM

others

OSCILLATOR

PHY PORT0

PHY PORT1

PCI I/F

VT6311S_LQFP128

6311S@

6311S@

6311S@

6311S@

6311S@

6311S@

6311S@

6311S@

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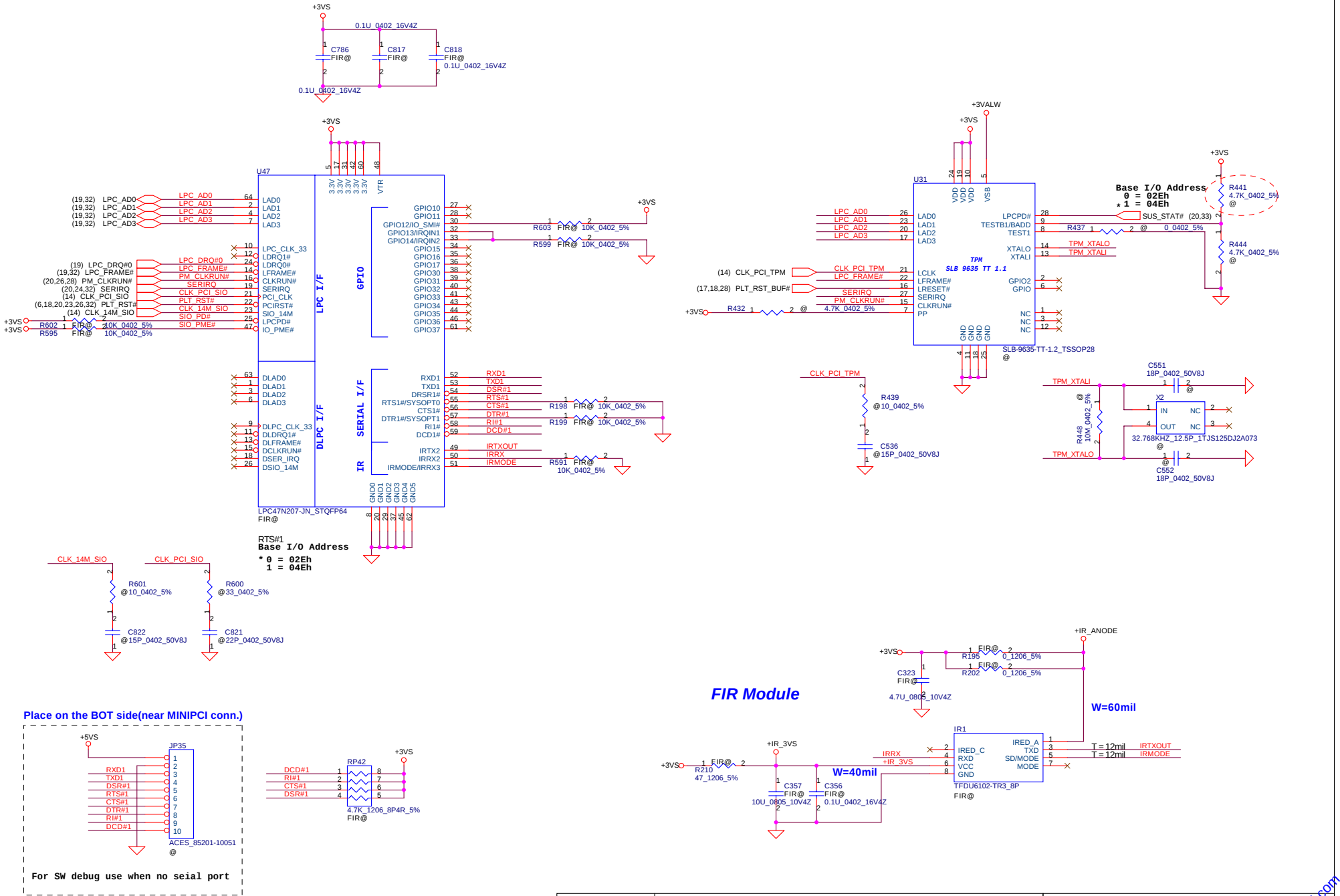
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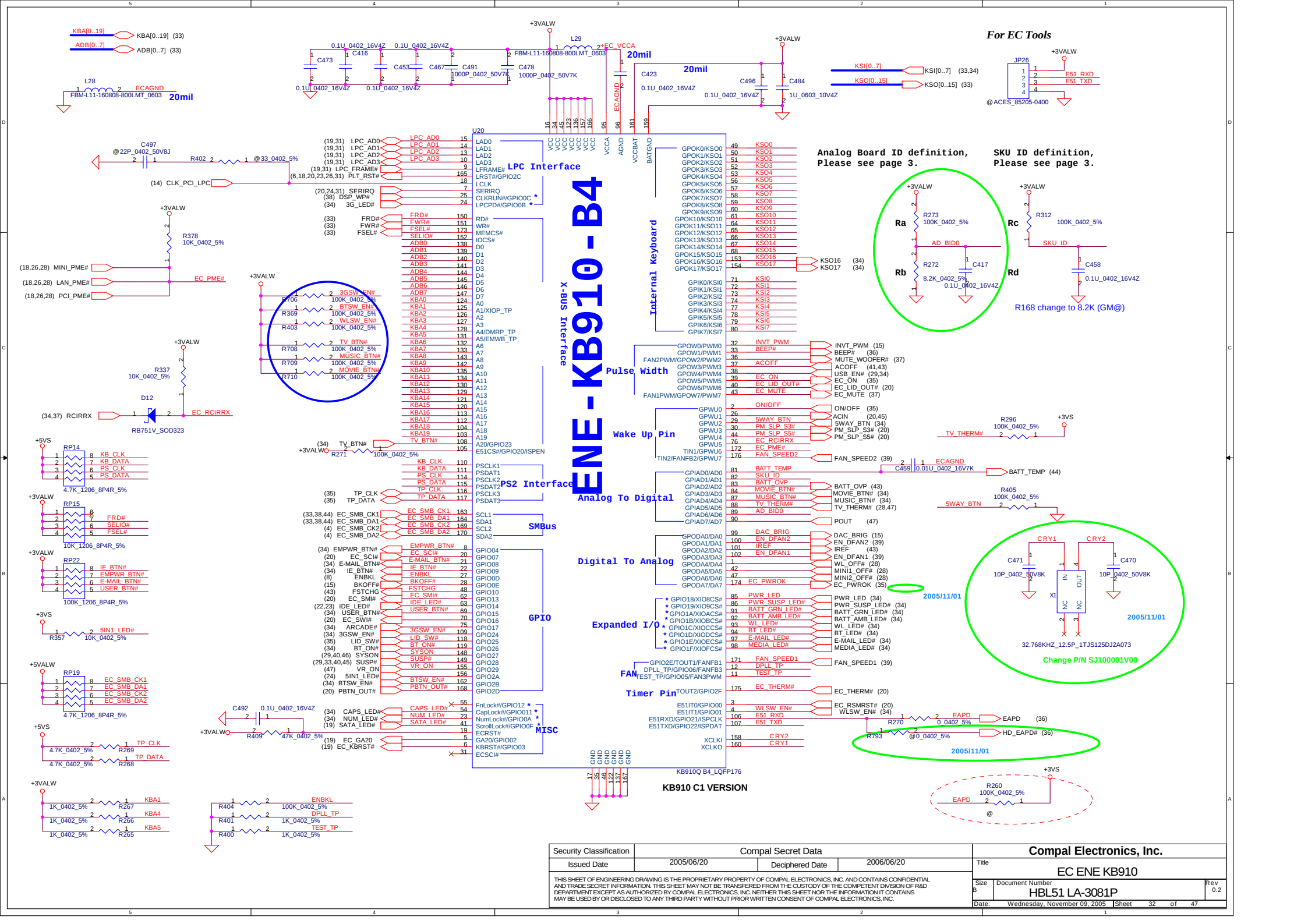
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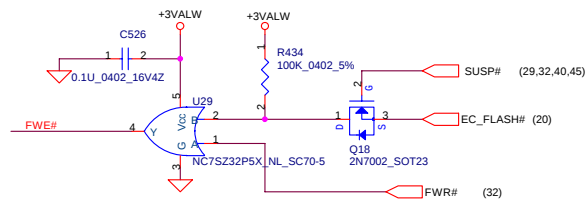
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				Rev	0.2

SUPER I/O SMsC LPC47N207

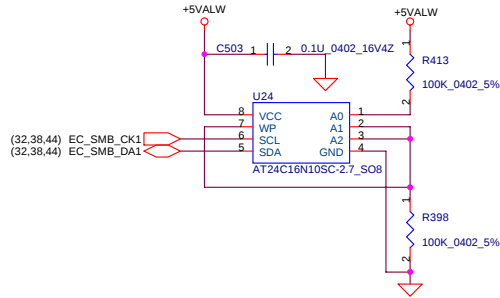


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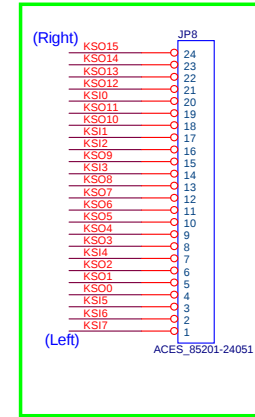
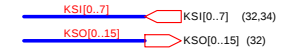




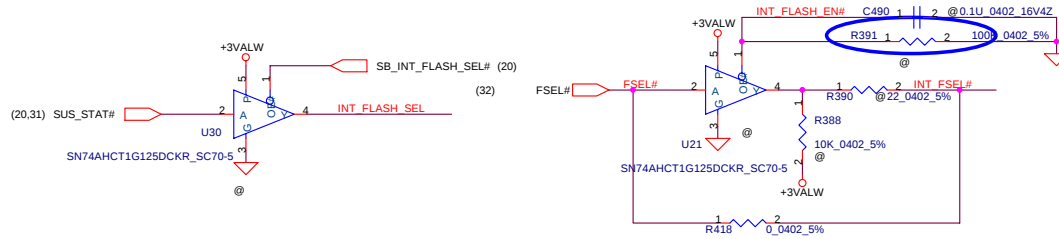
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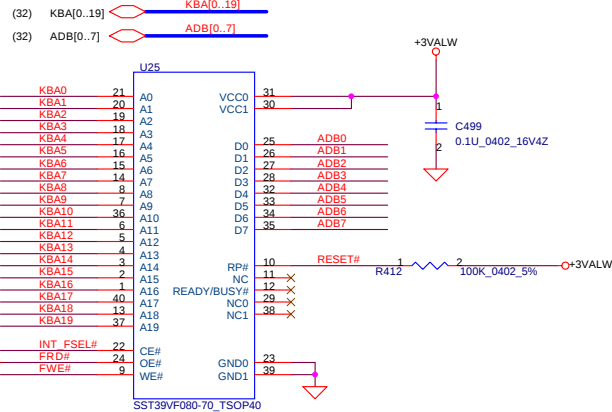
INT_KBD Conn.



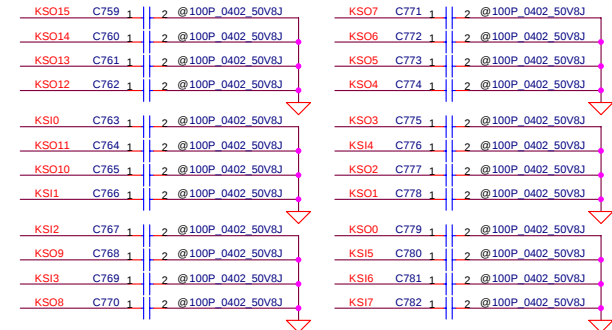
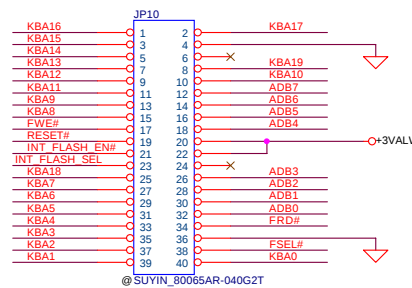
2005/11/03



1MB Flash ROM



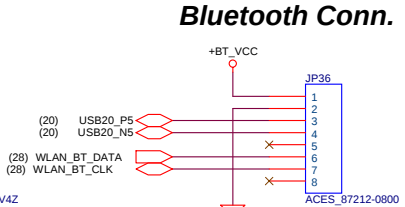
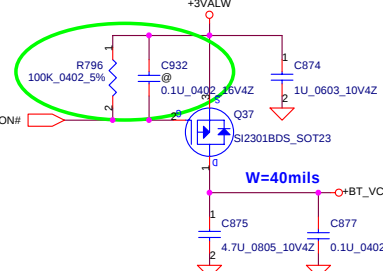
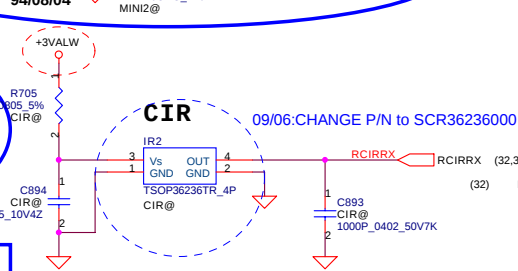
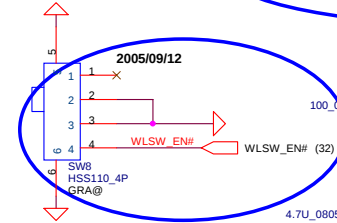
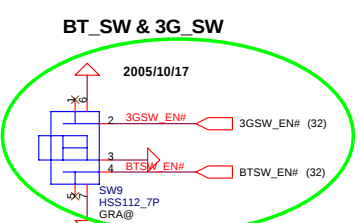
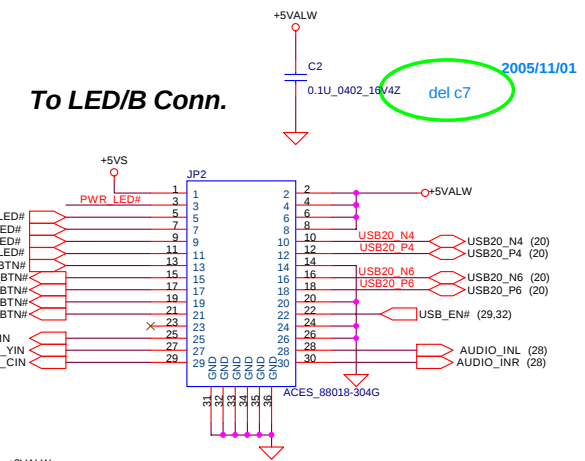
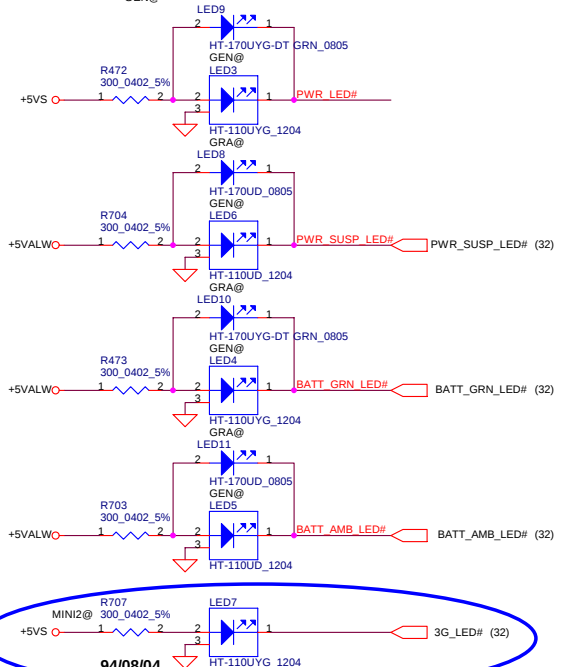
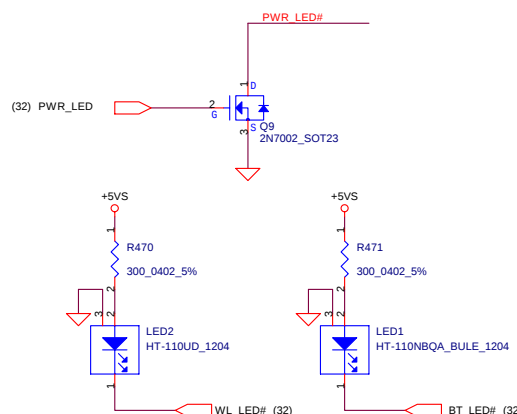
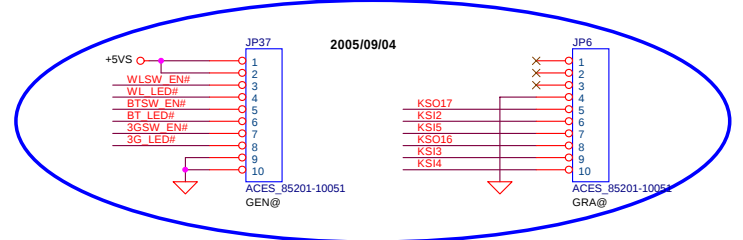
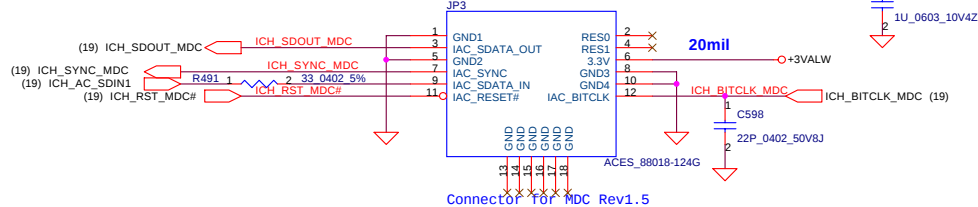
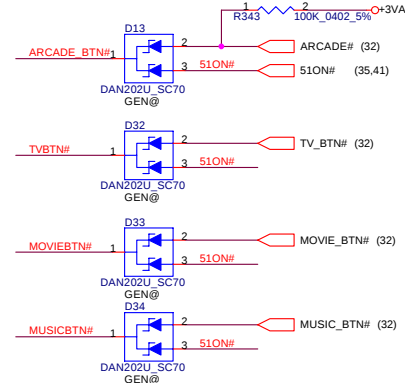
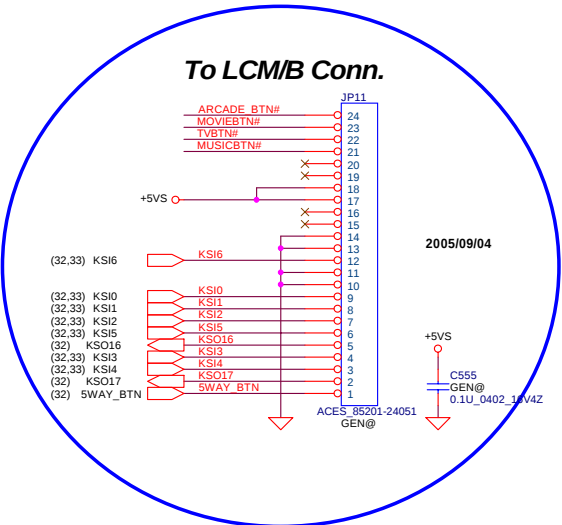
1MB ROM Socket



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				Deciphered Date				BIOS, I/O Port & K/B Connector			
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								Document Number			
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								47			

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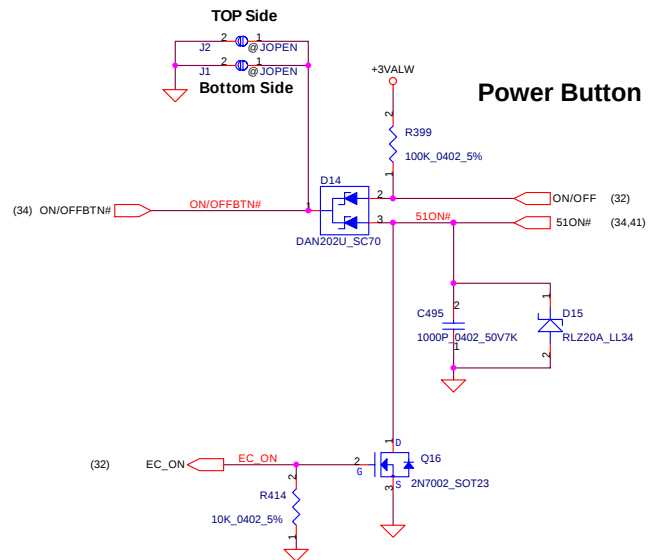
Printed on 11/9/2005



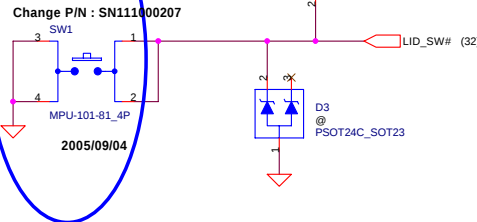
Geneva			Grapevine		
	KSO16	KSO17		KSO16	KSO17
KSI0	VOL_UP	LEFT			
KSI1	RIGHT	VOL_DOWN			
KSI2	PLAY	ENTER			
KSI3	STOP			PLAY	VOL_UP
KSI4	NEXT			STOP	VOL_DOWN
KSI5	REV			NEXT	ARCANE_TV
KSI6		RECORD		REV	

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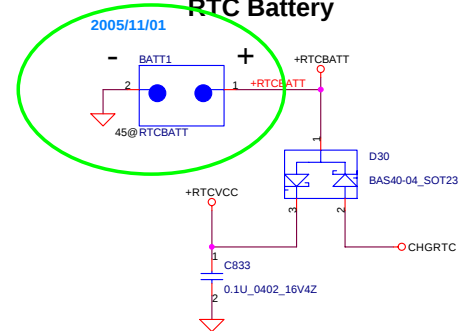
ON/OFF switch



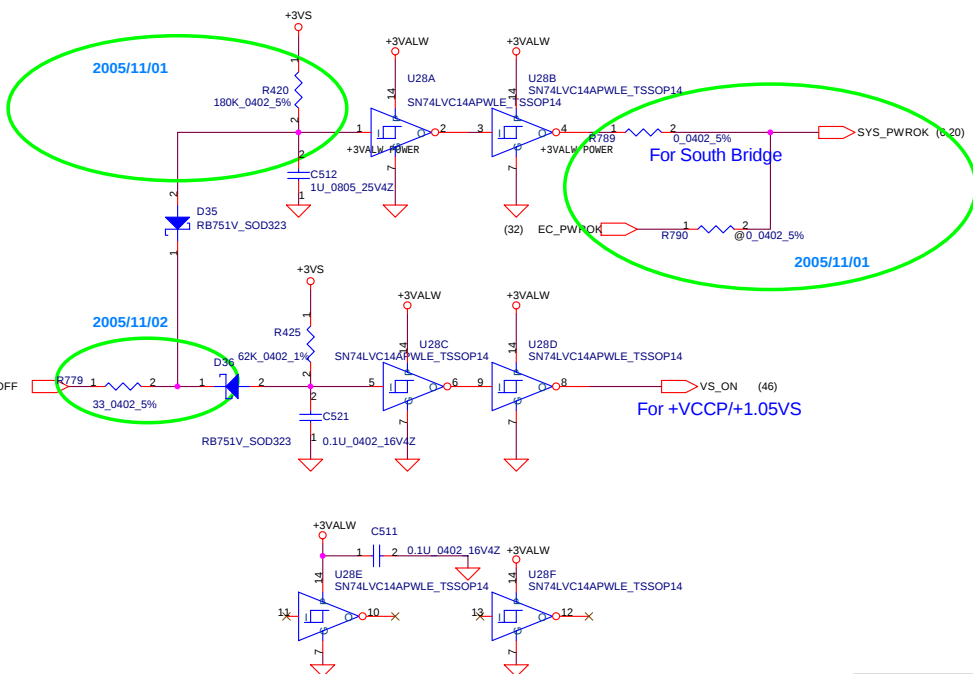
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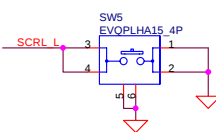
RTC Battery



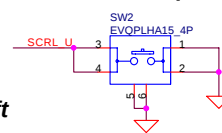
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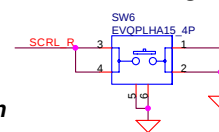
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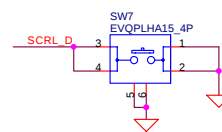
Scroll Up



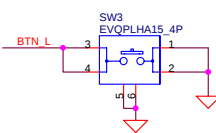
Scroll Right



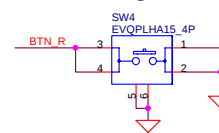
Scroll Down



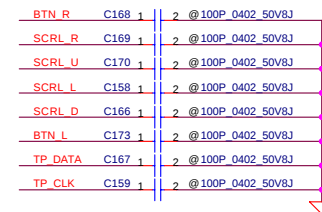
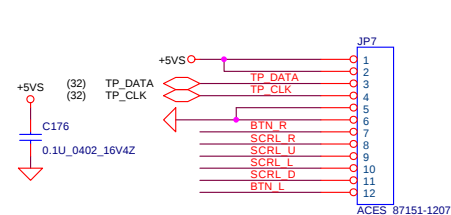
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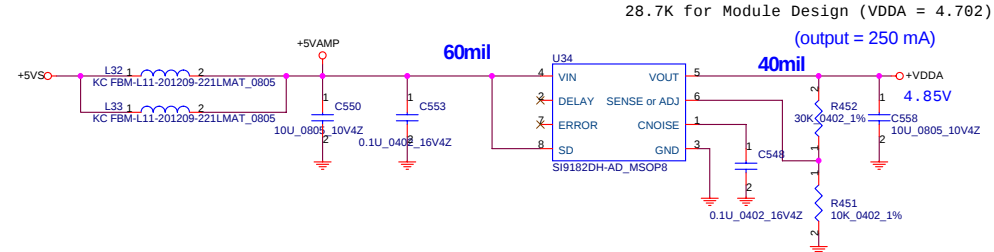
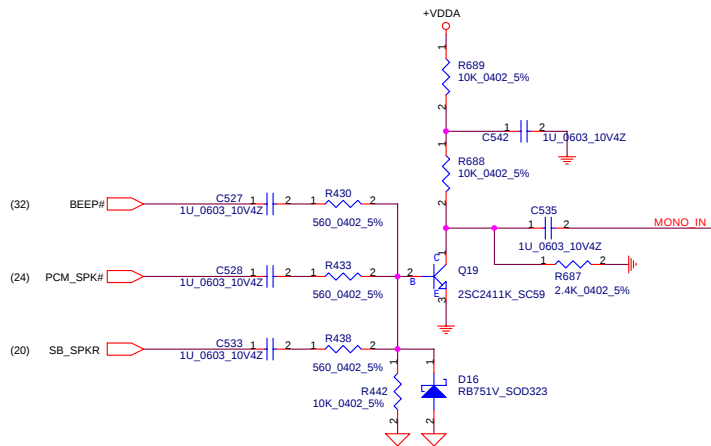
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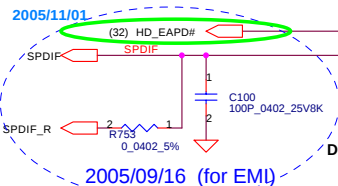
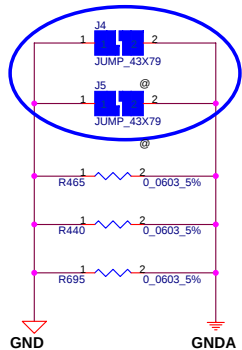
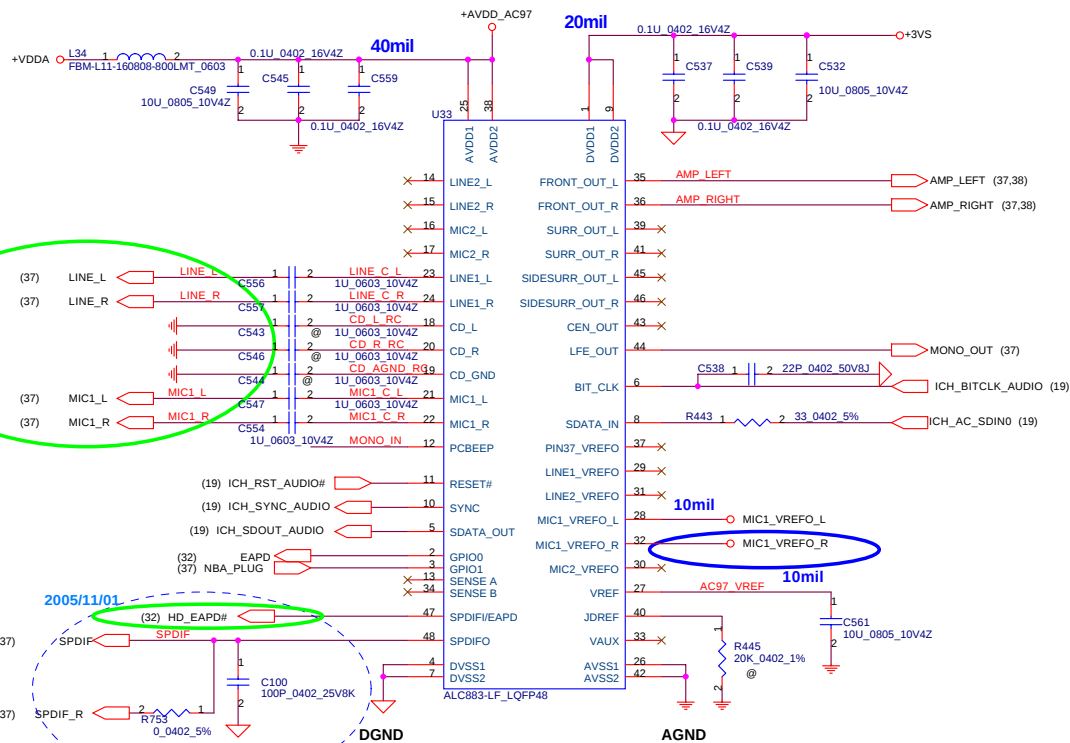
To TP/B Conn.



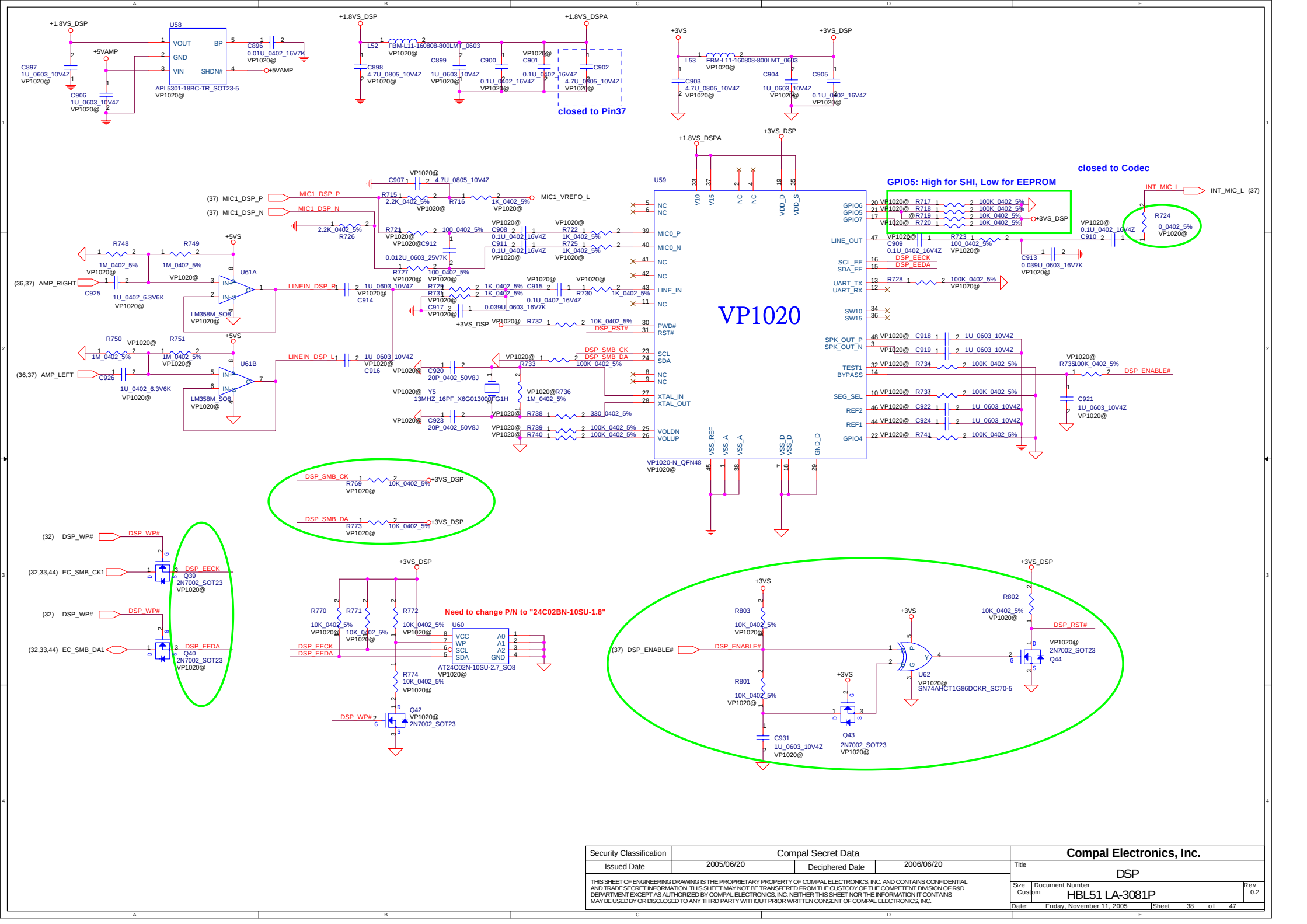
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HD Audio Codec



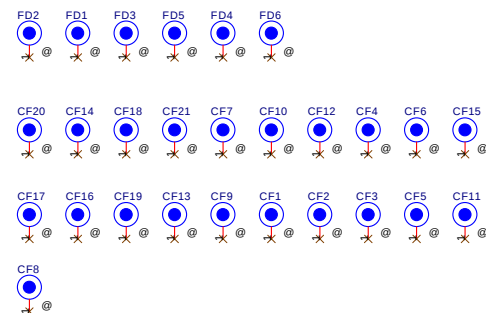
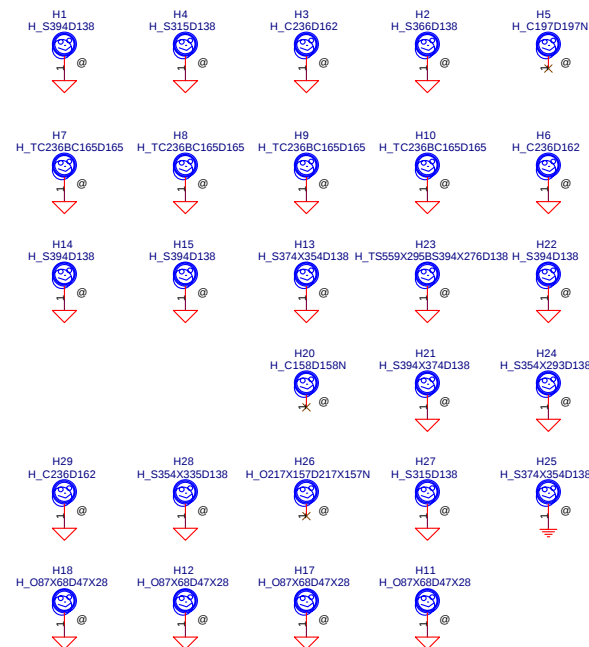
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				Size Custom	Document Number HBL51 LA-3081P Rev 0.2
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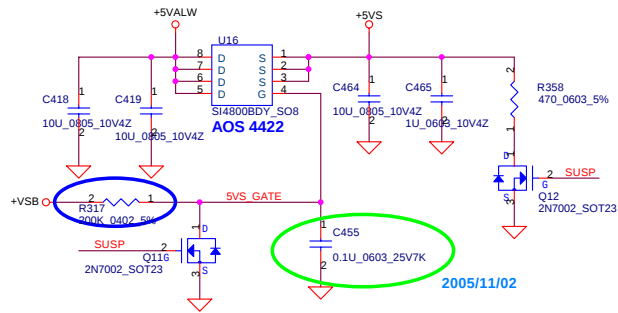
The schematic diagram illustrates the fan speed control circuit. It features a 5V power supply connected to a 10uF 1206 16V4Z capacitor (C47). The circuit includes a 993P1UF_SOP8 op-amp (U2) configured with its non-inverting input (VIN) connected to the 5V supply and its inverting input (VEN) connected to the output. The op-amp's output is connected to a 3V power supply through a 10K 0402 5% resistor (R45). The 3V supply is also connected to a 1000P_0402_50V7K capacitor (C59). A 1N4148 diode (D5) is connected between the 3V supply and the output. A 1SS355 diode (D4) is connected between the 5V supply and the output. A 10uF 1206 16V4Z capacitor (C51) and a 1000P_0402_50V7K capacitor (C58) are connected between the 5V supply and the output. The output is connected to a JF19 connector. The circuit is labeled with 40mil and ACES_85205-03001.

The schematic diagram illustrates the fan speed control circuit. It features a 5V power supply connected to a 10uF 1206 16V4Z capacitor (C338). The circuit includes a 10k 0402 5% resistor (R207) and a 1000pF 0402 50V7K capacitor (C344). A 1000pF 0402 50V7K capacitor (C343) is also present. A 10uF 1206 16V4Z capacitor (C339) is connected to the output. A 1N4148 SOT23 diode (D9) and a 1SS355 SOD323 diode (D8) are used for signal conditioning. The output is connected to a 40mil trace. The circuit is powered by +5V and +3V. The output is connected to a 40mil trace. The circuit is labeled with component values and part numbers.

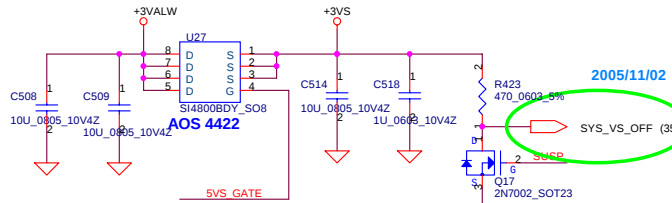


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						Size B	Document Number			Rev
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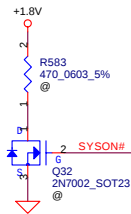
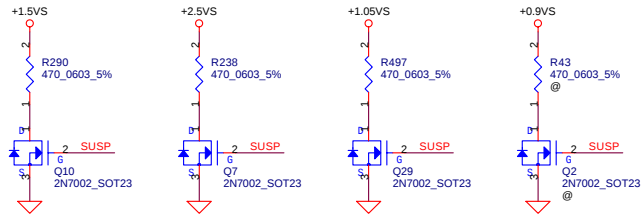
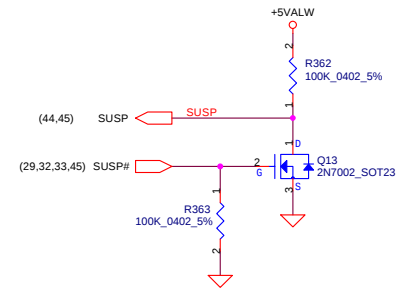
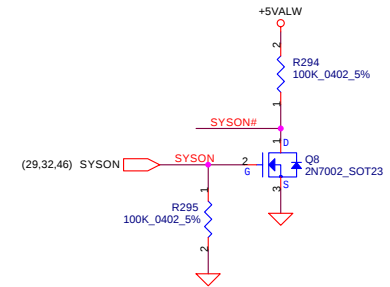
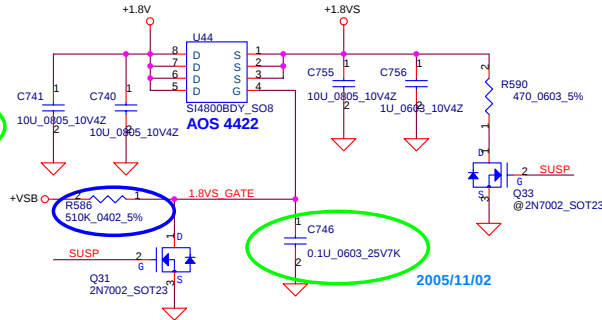
+5VALW TO +5VS



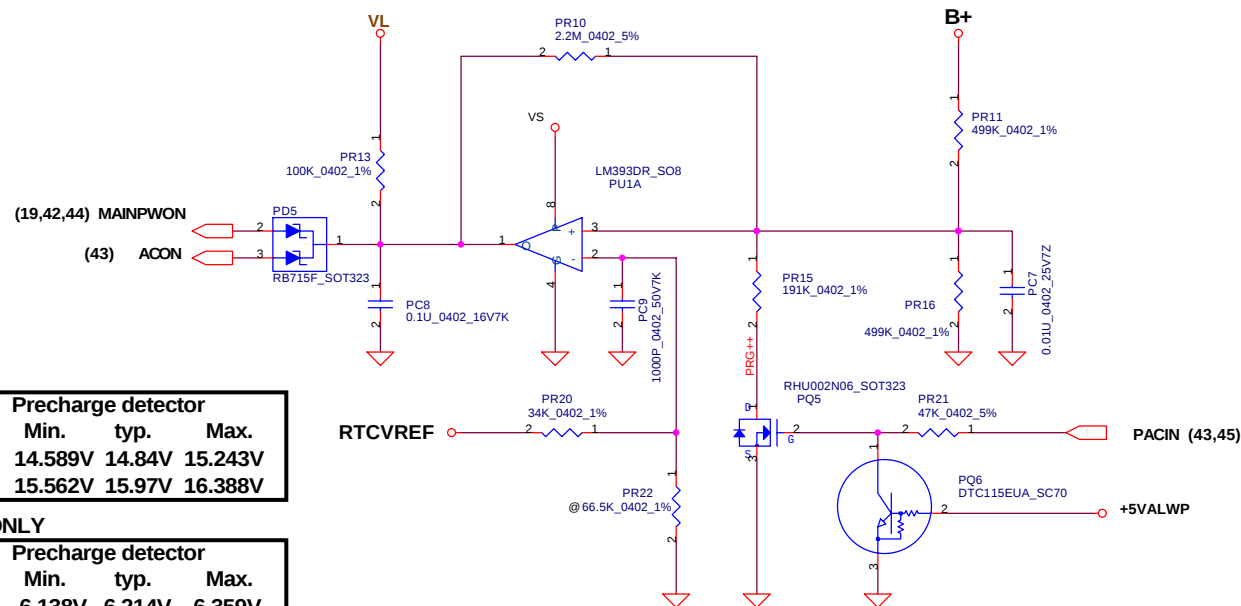
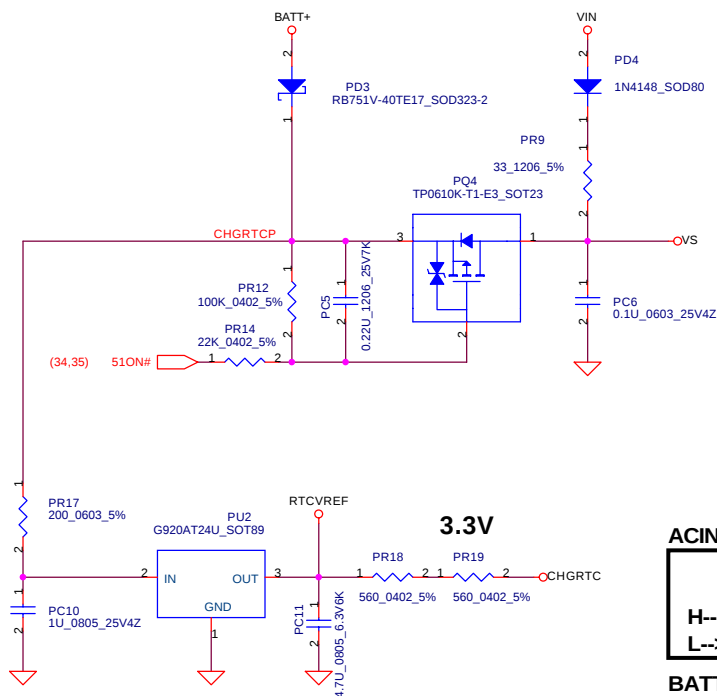
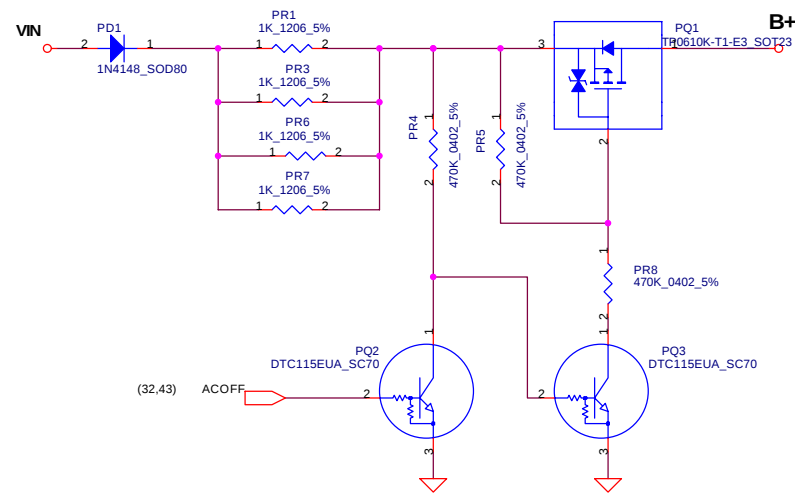
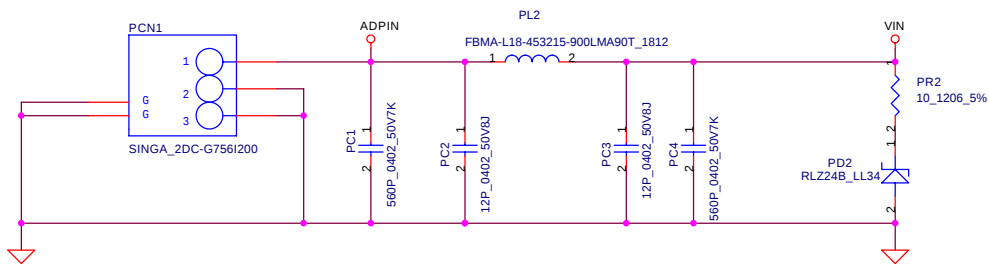
+3VALW TO +3VS



+1.8V to +1.8VS



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ACIN

Precharge detector

	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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Compal Electronics, Inc.

Title

DCIN/DECTOR/RTC

Size

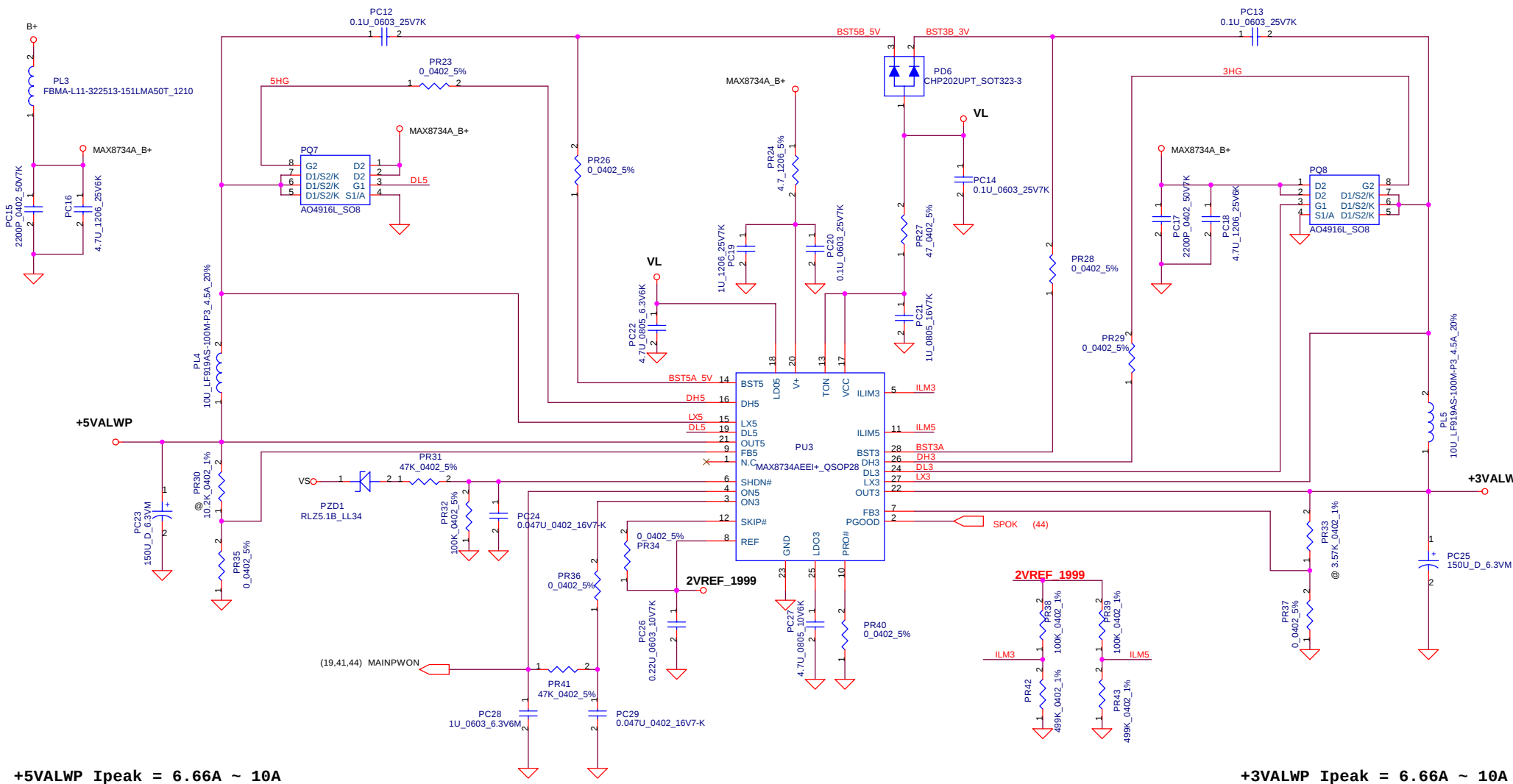
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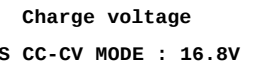
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				Size	Document Number
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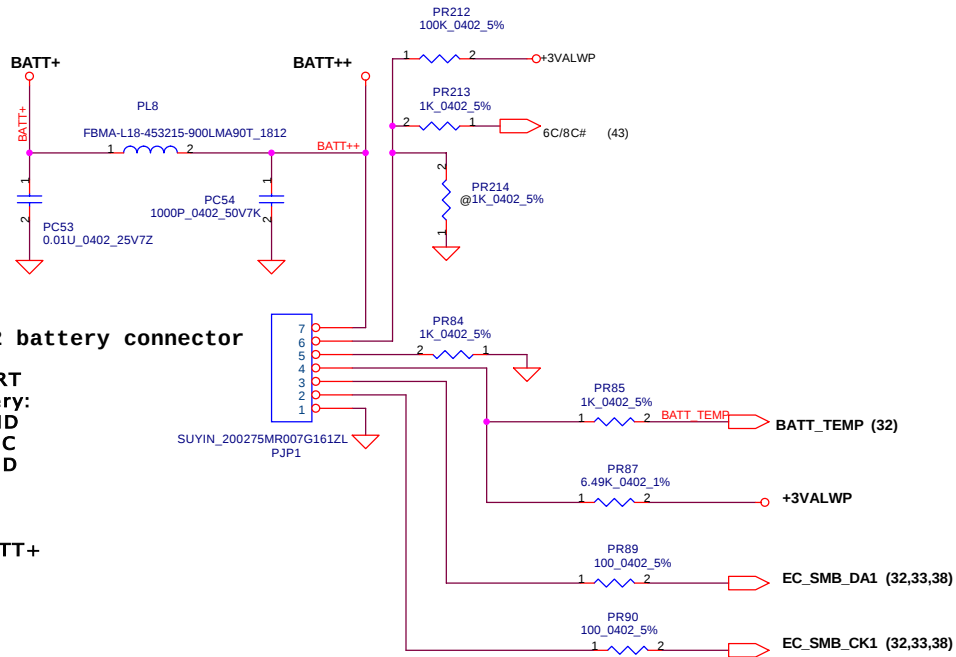


LI-3S :17.8V----BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

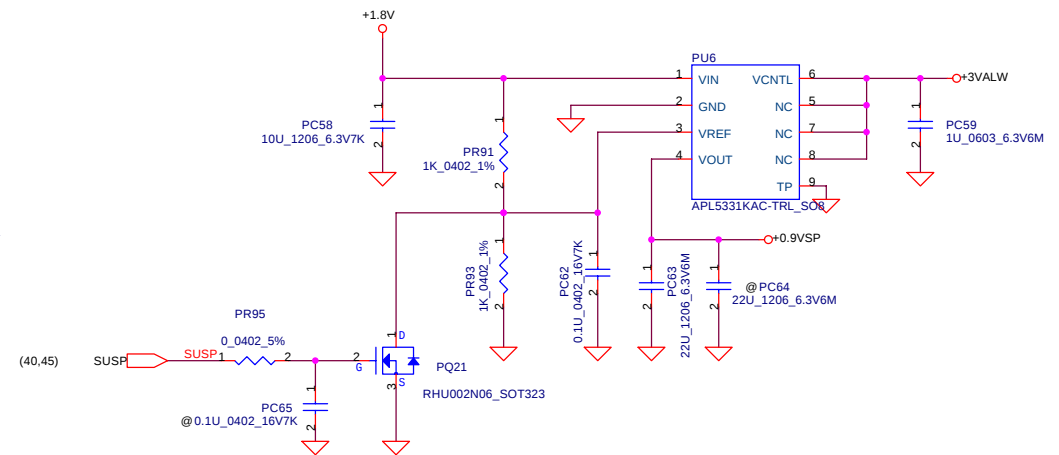
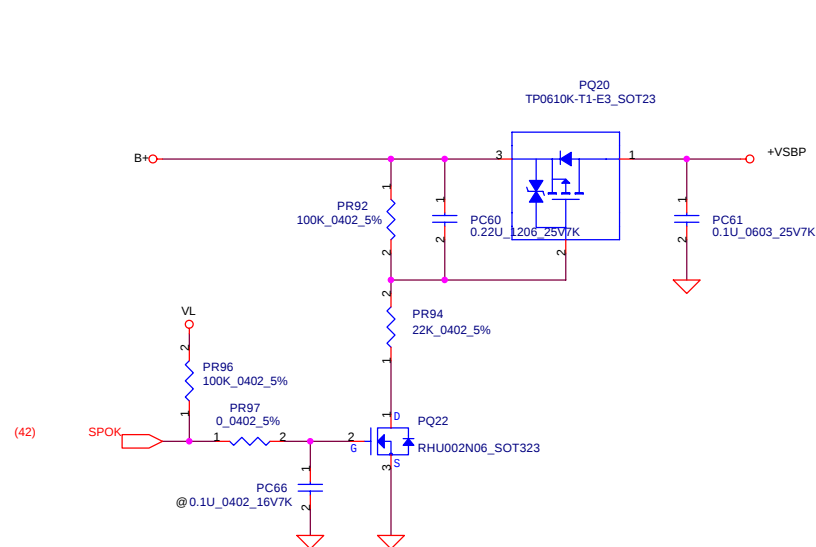
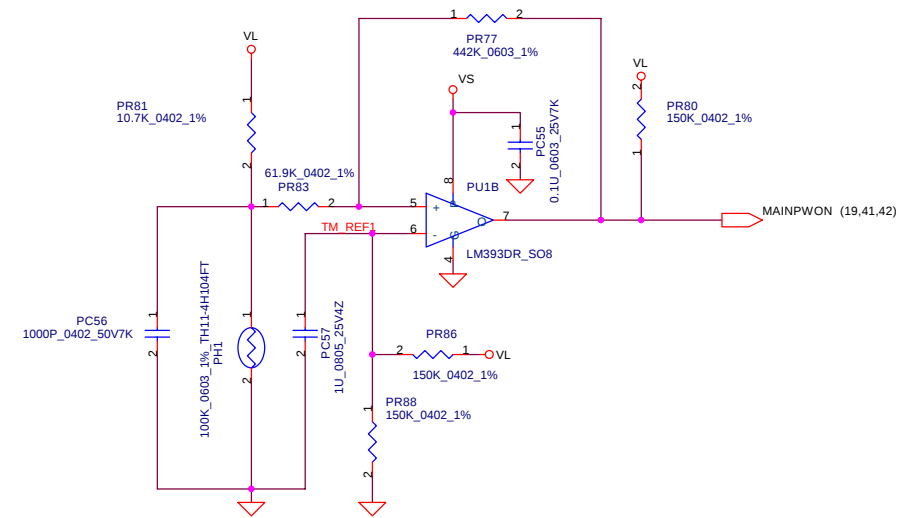
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PJP2 battery connector

SMART Battery:
 1.GND
 2.SMC
 3.SMD
 4.TS
 5.B/I
 6.ID
 7.BATT+

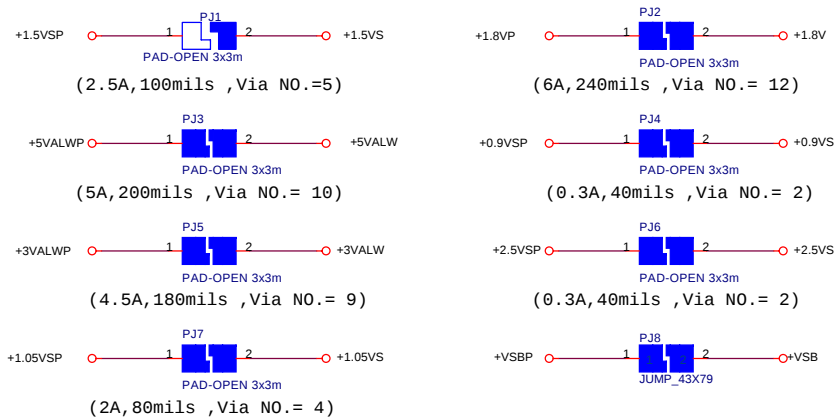


PH1 under CPU botten side :
 CPU thermal protection at 80 degree C
 Recovery at 44(45) degree C

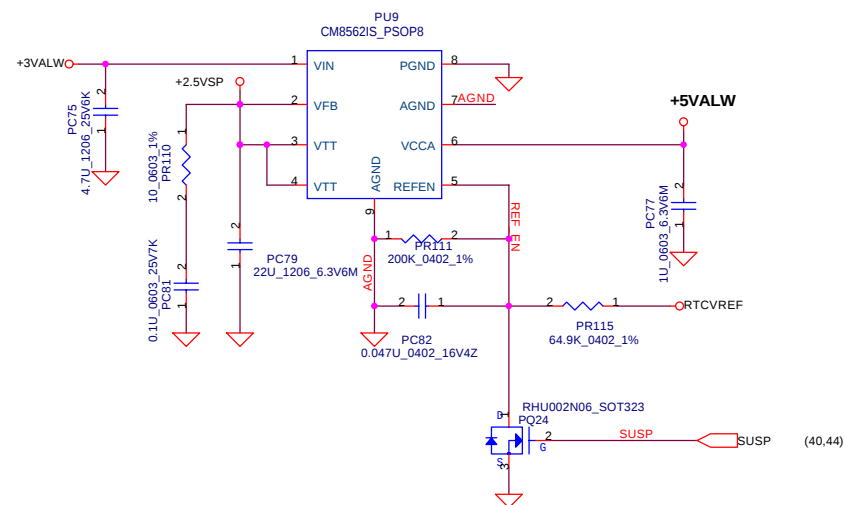
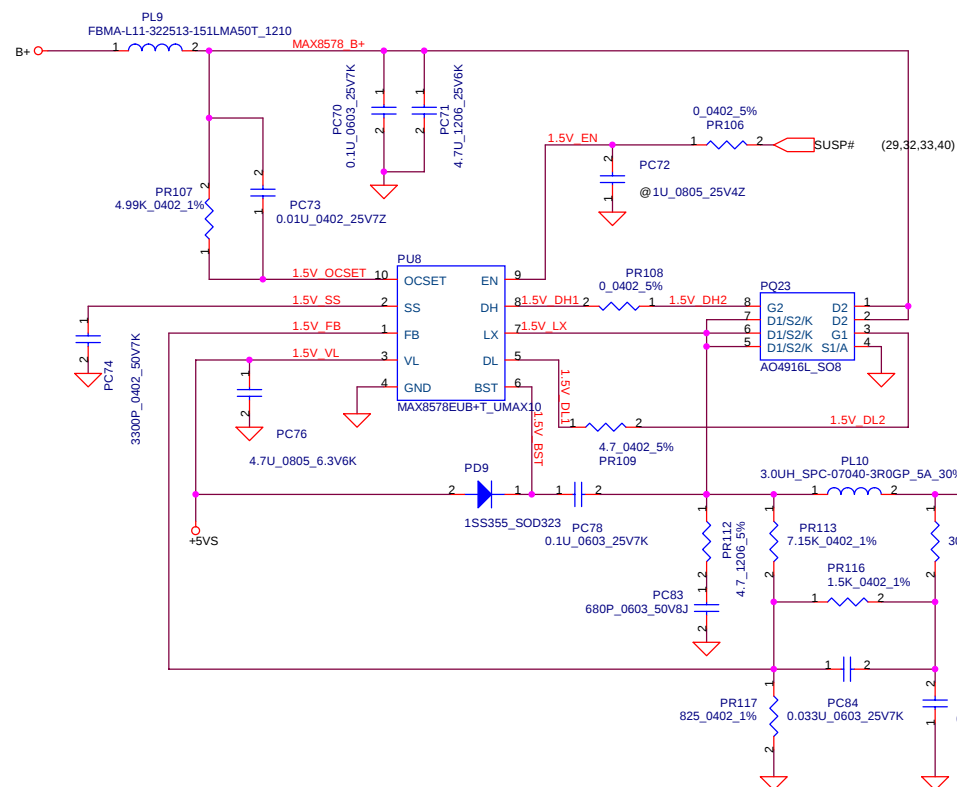
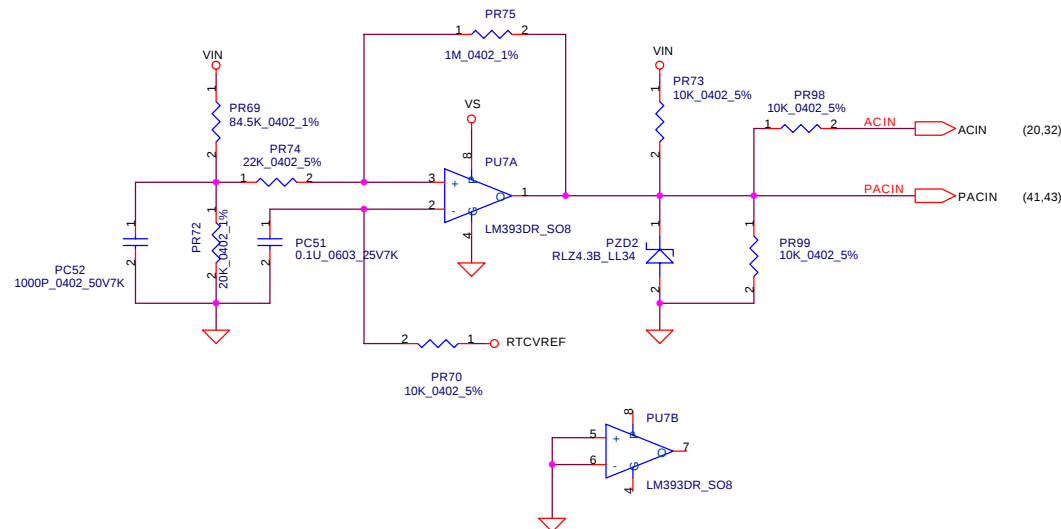


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AC Adapter Detector



Vin Detector 17.90V/17.24V



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