

Compal Confidential

Model Name : P5WE0

File Name : LA-6901P

BOM P/N:43

Compal Confidential

P5WE0 M/B Schematics Document

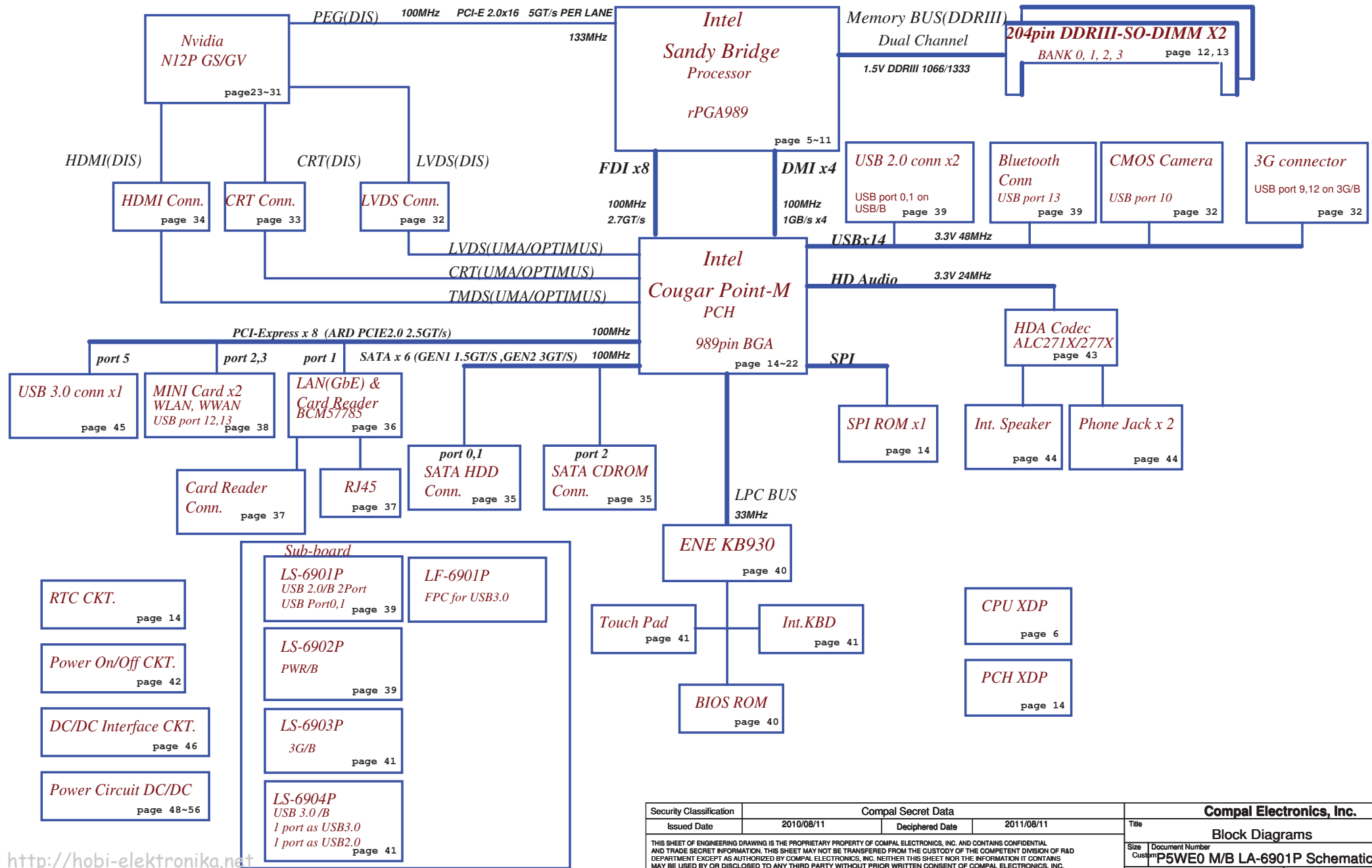
Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
Nvidia N12P GS/GV

2010-08-11

REV : 0 . 1

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Fan Control
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & BT & USB30 & USB20 Config

3G SKU: 3G@ **USB30 SKU:** USB30@ **OPTIMUS SKU:** OPT@
BT SKU: BT@ **USB20 SKU:** USB20@ **Non-OPTIMUS SKU:** NOPT@
LAN Chip A0 version: A0@
LAN chip B0 Version: B0@

BOM Config

UMA Only: BT@/3G@/USB30@/UMA@/UMAO@/NOPT@/A0@
OPTIMUS: BT@/3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@
DIS Only: BT@/3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@

VRAM BOM Config

X76*BOL01:** Samsung
X76*BOL02:** Hynix

VRAM P/N :

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

<http://hobi-elektronika.net>

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EVT
DVT
PVT
Pre-MP

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

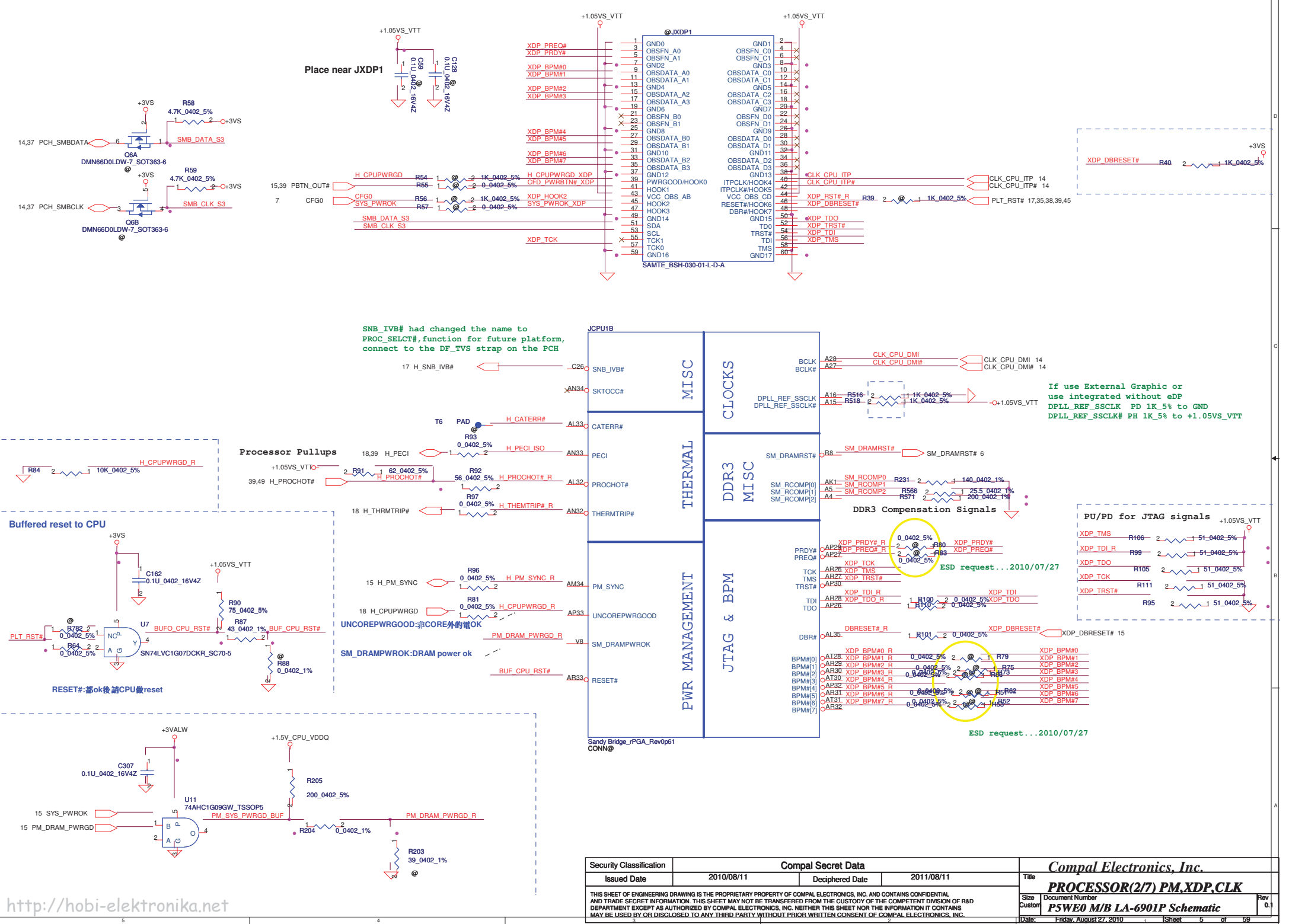
BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
Dis with OPTIMUS	DIS@
DIS Only	DISO@
OPTIMUS	OPT@
Non-OPTIMUS	NOPT@
3G	3G@
Blue Tooth	BT@
USB2.0	USB20@
USB3.0	USB30@
VRAM	X76@
Connector	CONN@
Unpop	@
LAN Chip A0 version	A0@
LAN Chip B0 version	B0@

USB Port Table

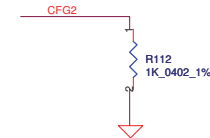
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
		2	USB 2.0 & USB3.0 Conn.
	UHCI1	3	
		4	
		5	
EHCI2	UHCI2	6	
		7	
		8	Mini Card 1(WLAN)
	UHCI3	9	3G/B(WWAN)
		10	Camera
		11	Mini Card 2(Reserved)
	UHCI6	12	SIM Card (3G/B)
		13	Blue Tooth

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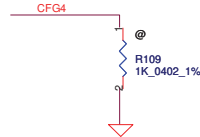


Security Classification		Compal Secret Data		Compal Electronics, Inc. PROCESSOR(2/7) PM,XDP,CLK					
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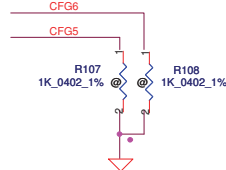
CFG Straps for Processor



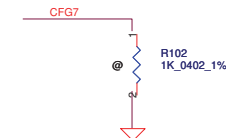
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



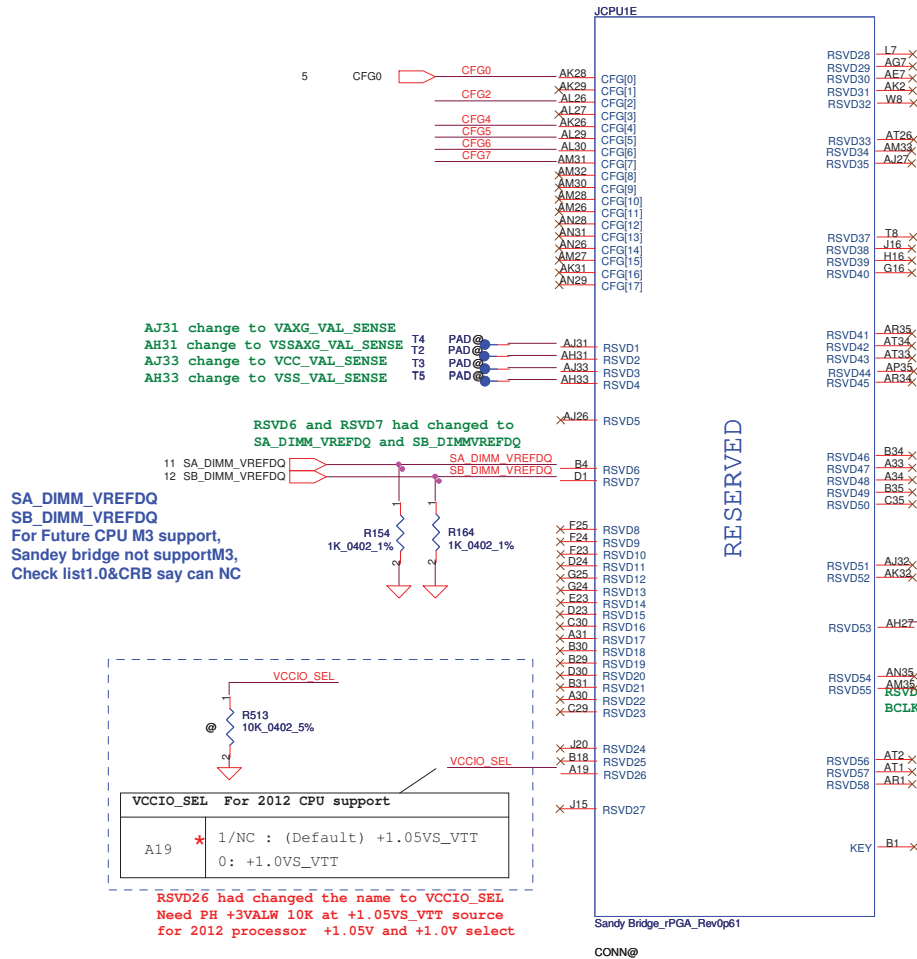
Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

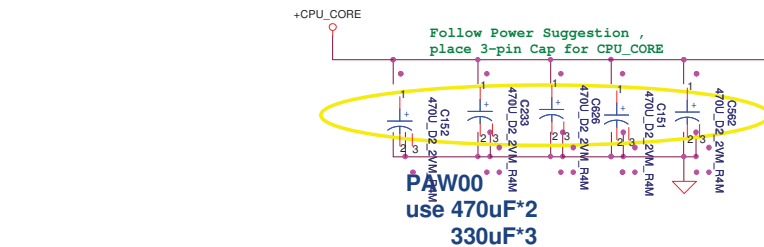


RSVD26 had changed the name to VCCIO_SEL
Need PH +3VALW 10K at +1.05VS_VTT source
for 2012 processor +1.05V and +1.0V select

Sandy Bridge_rPGA_Rev0p61
CONN@

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INTEL Recommend
4*470uF,16*22uF and 10*10uF
from PDDG 1.0



SV type CPU

QC 94A
DC 53A

JCPU1F

POWER

PEG AND DDR

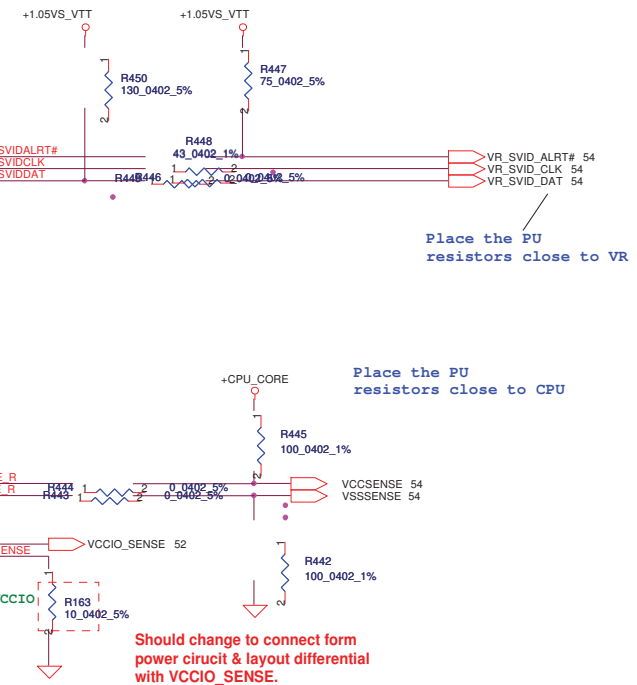
CORE SUPPLY

SVID

SENSE LINES

8.5A

INTEL Recommend
2*330uF,12*22uF
from PDDG 1.0



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QC 33A
DC 26A



+V_SM_VREF should have 20 mil trace width

10A

**INTEL Recommend
1*330uF,3*10uF
from PDDG 1.0**

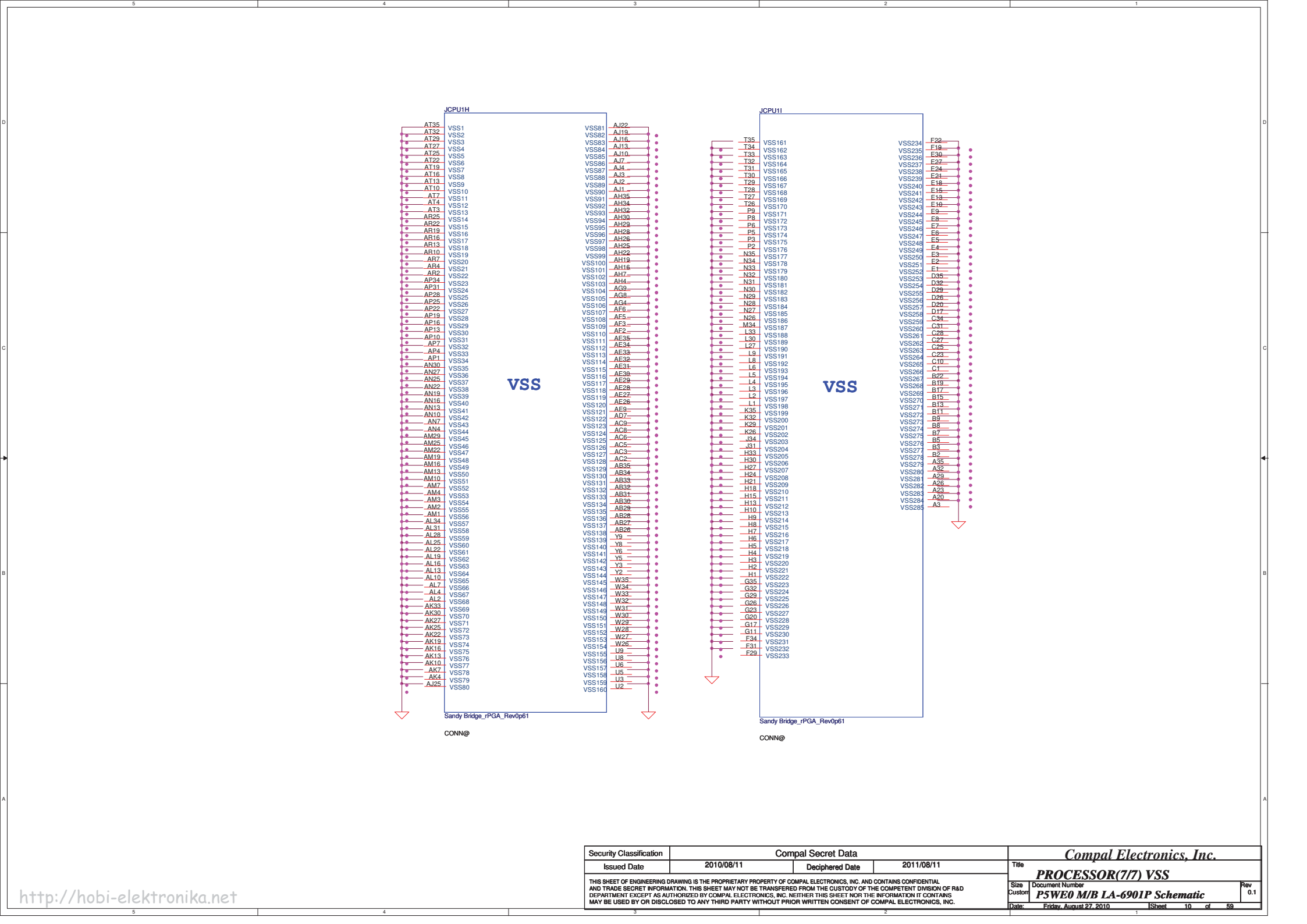
Short for +1.5VS to +1.5V_1
INTEL Recommend
1*330uF,6*10uF
from PDDG 1.0

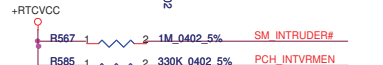
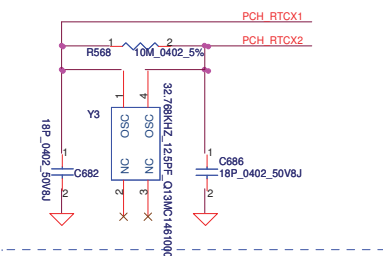
If possible, use os-con cap
if not, use the D2 size

VCCSA				
VID0	VID1	Vout	2011CPU	2012CPU
0	0	0.9V	V	V
0	1	0.8V	V	V
1	0	0.725V	X	V
1	1	0.675V	X	V

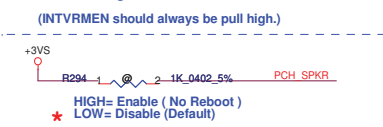
**INTEL Recommend
1*330uF, 1*10uF and 2*1uF(0402)
from PDDG 1.0**

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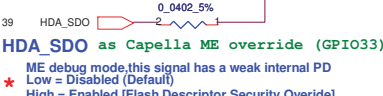




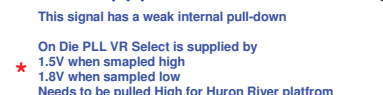
INTVRMEN
 * H : Integrated VRM enable
 L : Integrated VRM disable
 (INTVRMEN should always be pull high.)



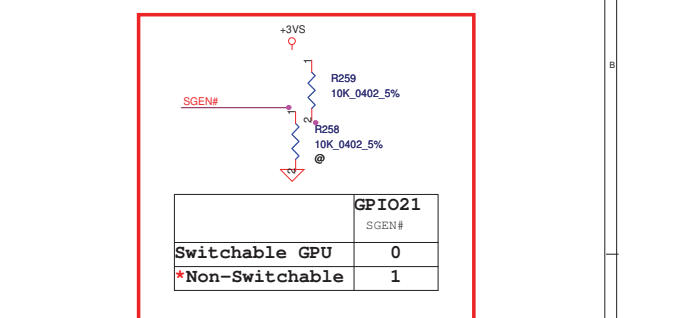
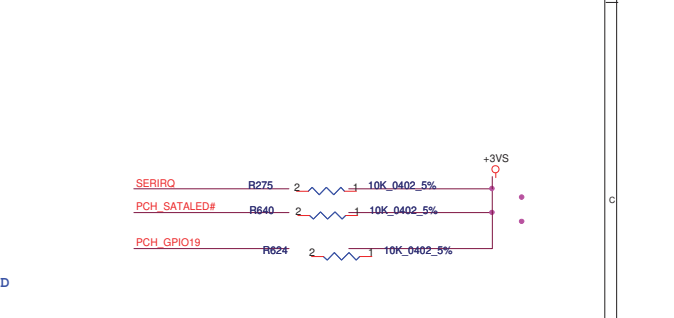
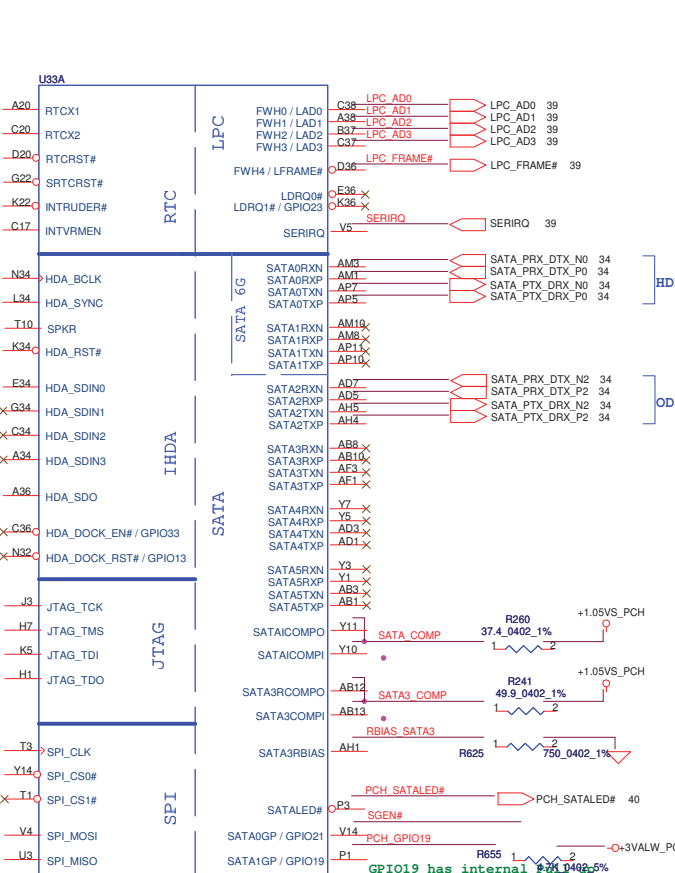
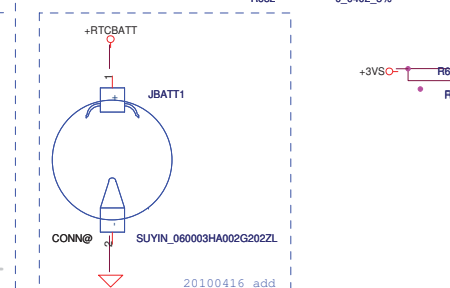
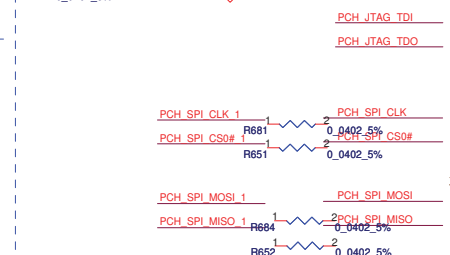
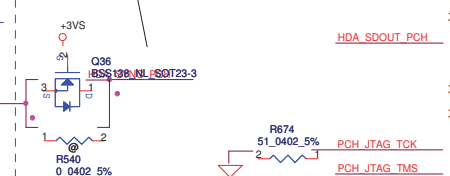
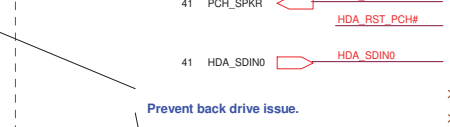
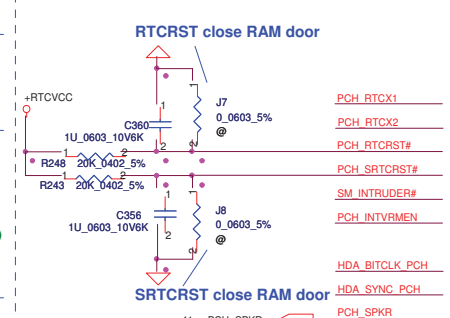
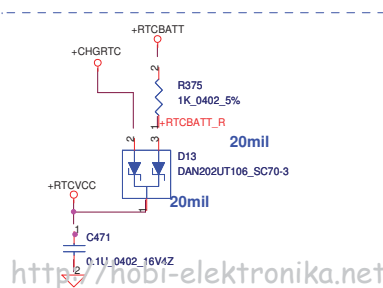
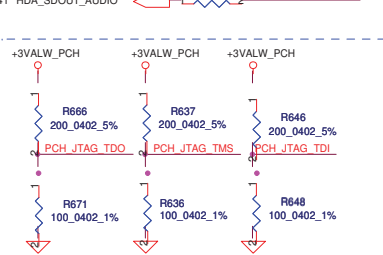
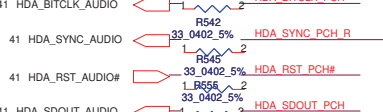
HIGH= Enable (No Reboot)
 LOW= Disable (Default)



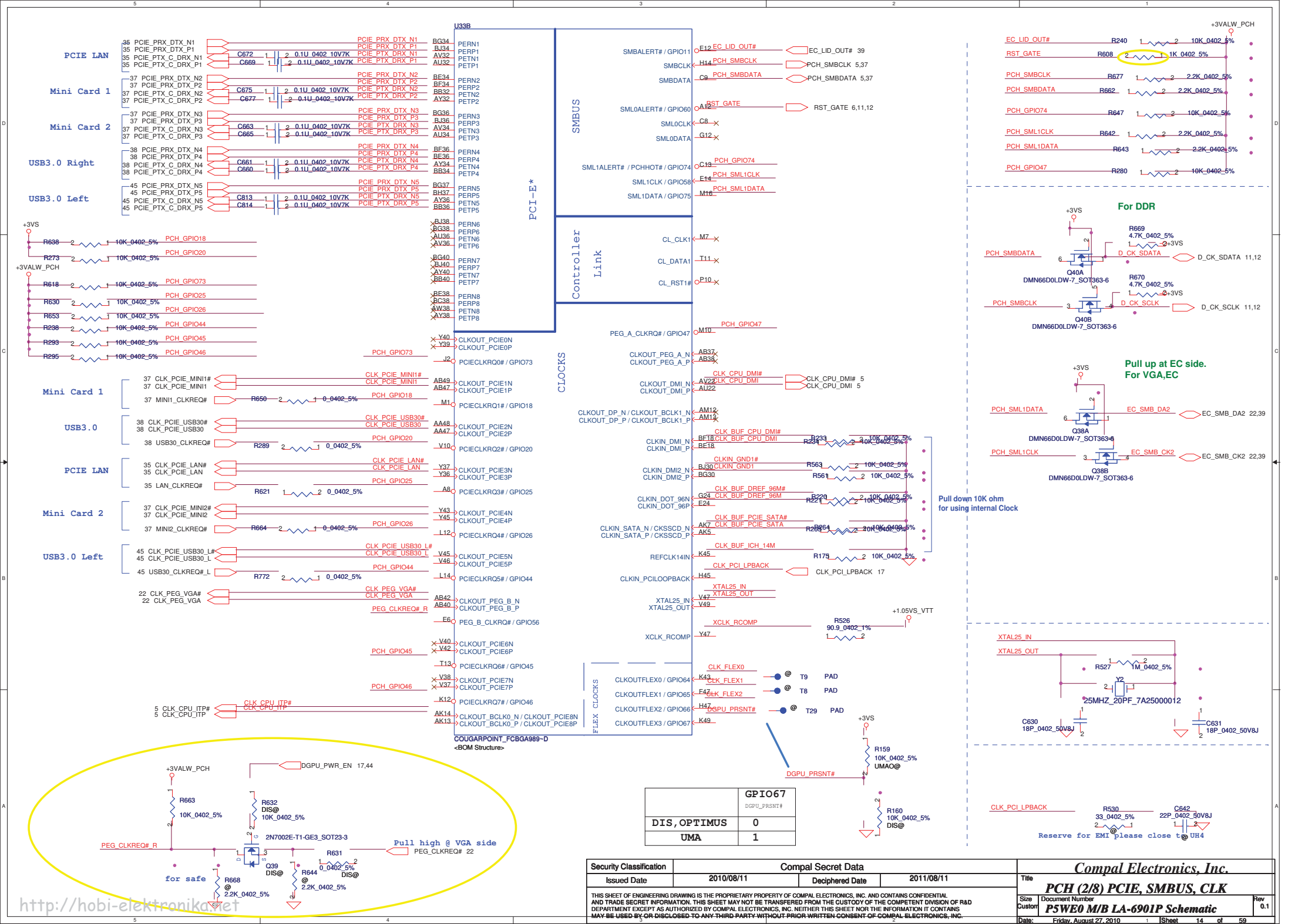
HDA_SDO as Capella ME override (GPIO33)
 ME debug mode, this signal has a weak internal PD
 Low = Disabled (Default)
 High = Enabled [Flash Descriptor Security Override]



This signal has a weak internal pull-down
 On Die PLL VR Select is supplied by 1.5V when smaped high 1.8V when sampled low
 Needs to be pulled High for Huron River platform

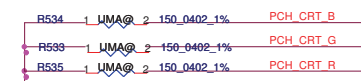
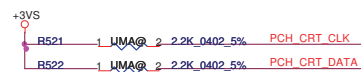
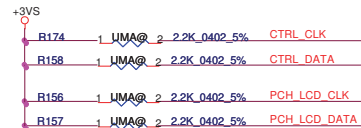
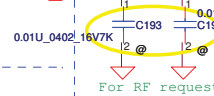


Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
* SPI	1	1



22.39 ENBKL ENBKL R532 2 0.0402 5% IGPU_BKLT_EN
UMA@

31 PCH_LCD_CLK
31 PCH_LCD_DATA

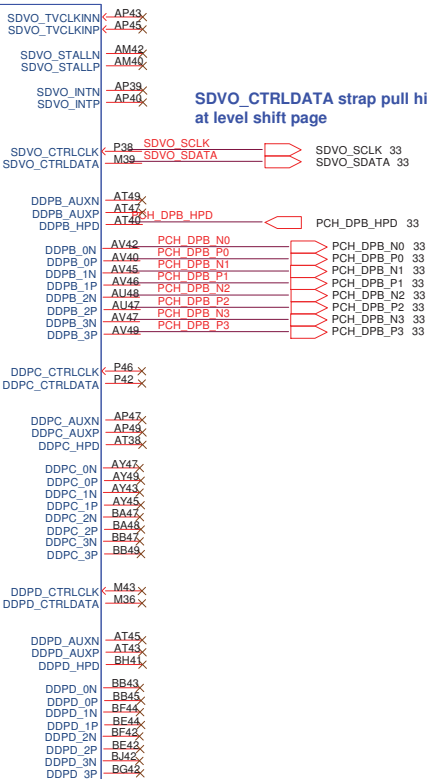


Pull high at LVDS conn side.



U33D

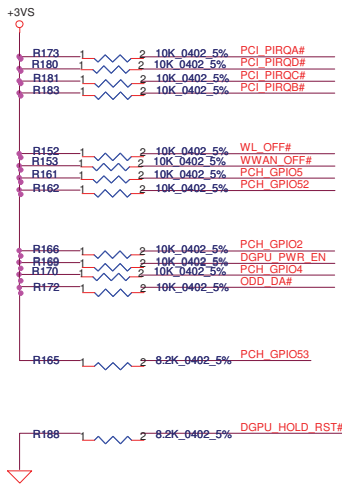
Digital Display Interface



SDVO_CTRLDATA strap pull high at level shift page

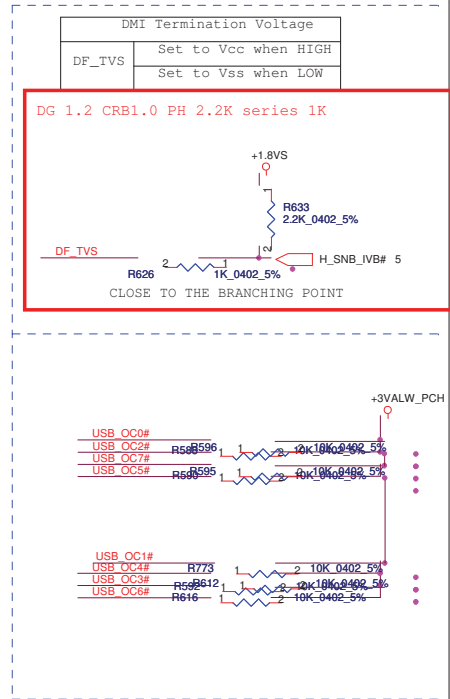
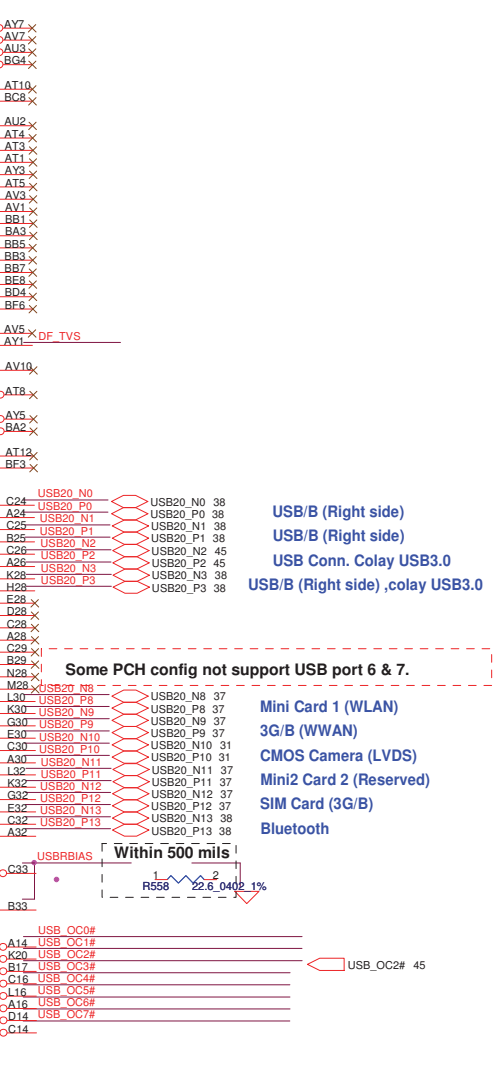
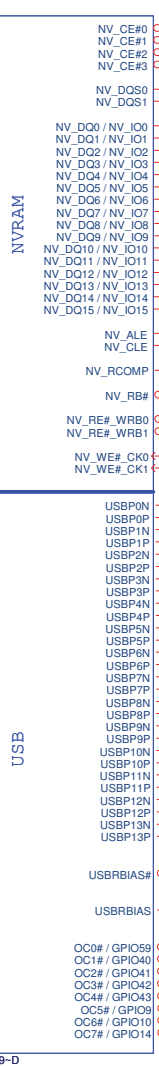
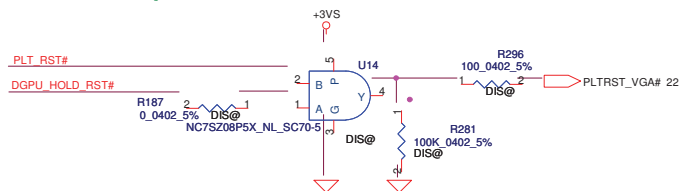
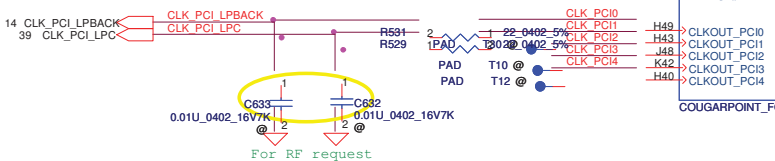
HDMI D2
HDMI D1
HDMI D0
HDMI CLK

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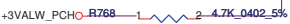
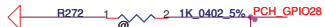
GPIO51 Internal pull high

Boot BIOS Strap bit1 BBS1			
GNT1#/ GPIO51	Bit11	Bit10	Boot BIOS Destination
	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC

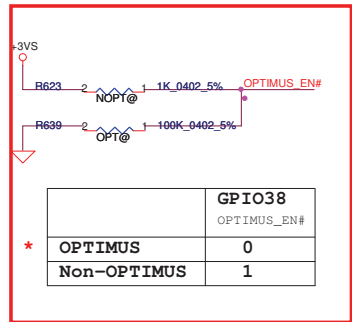
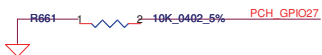


HDA_SYNC PH (PLL =+1.5VS)
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

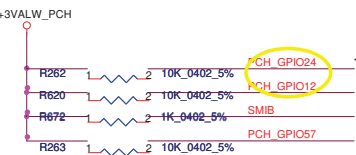
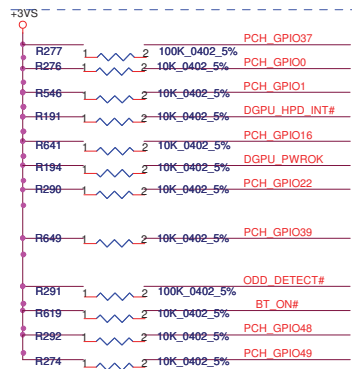
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

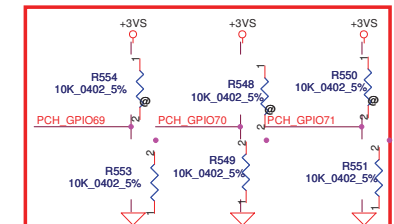
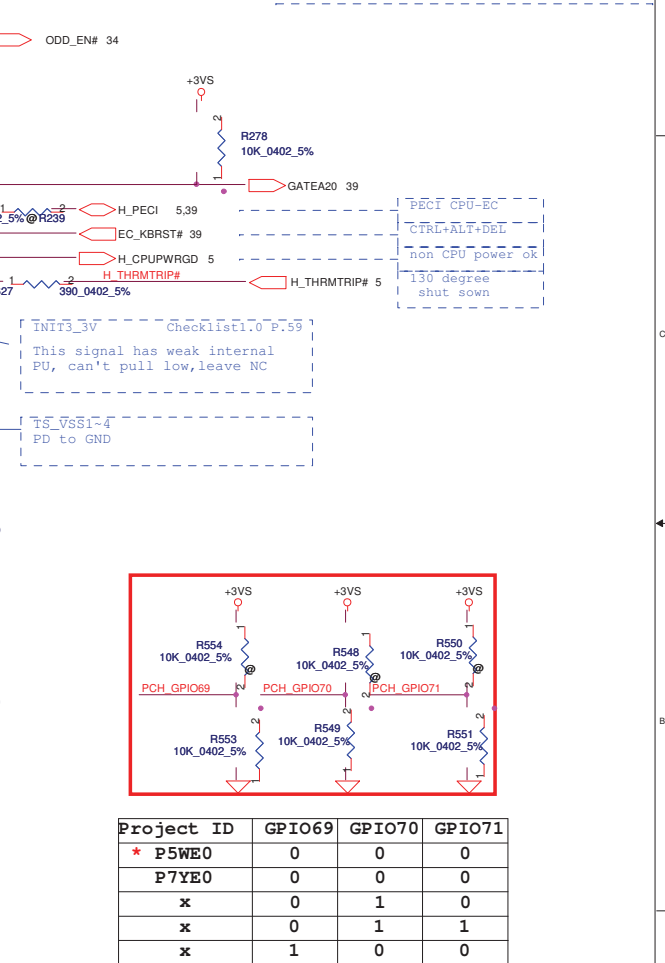
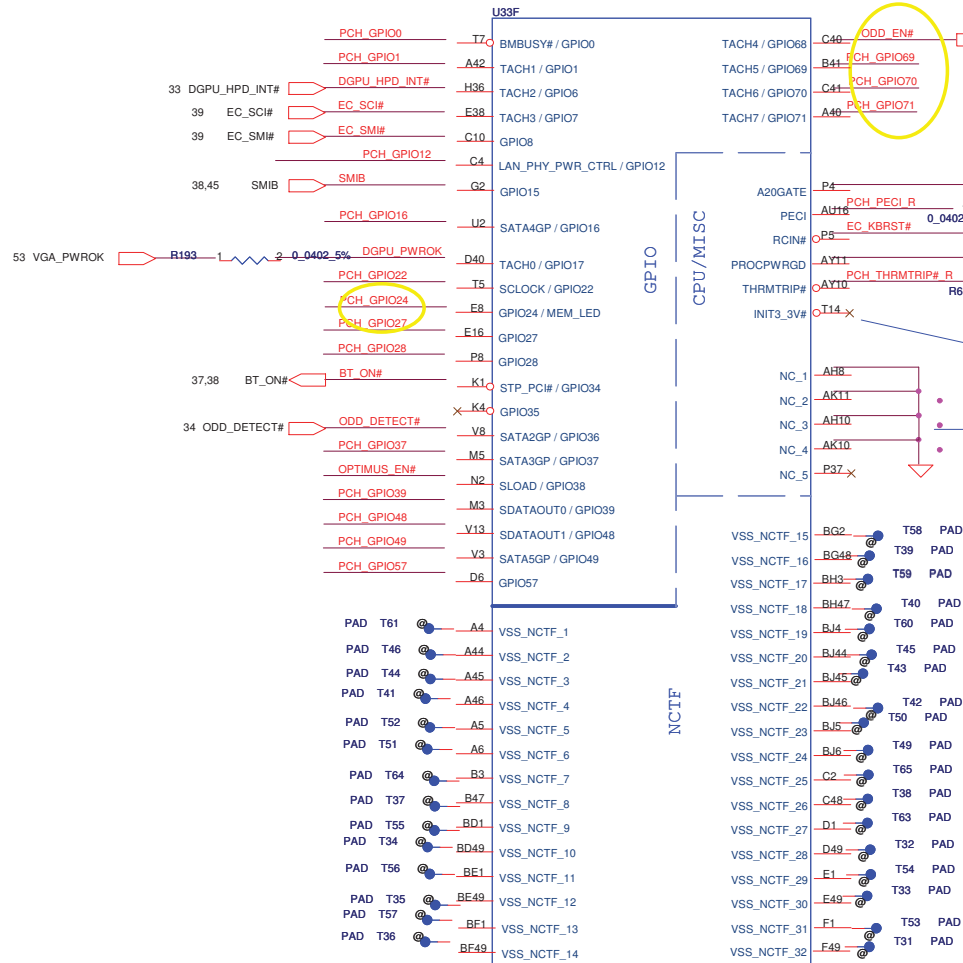


	GPIO38
OPTIMUS	0
Non-OPTIMUS	1



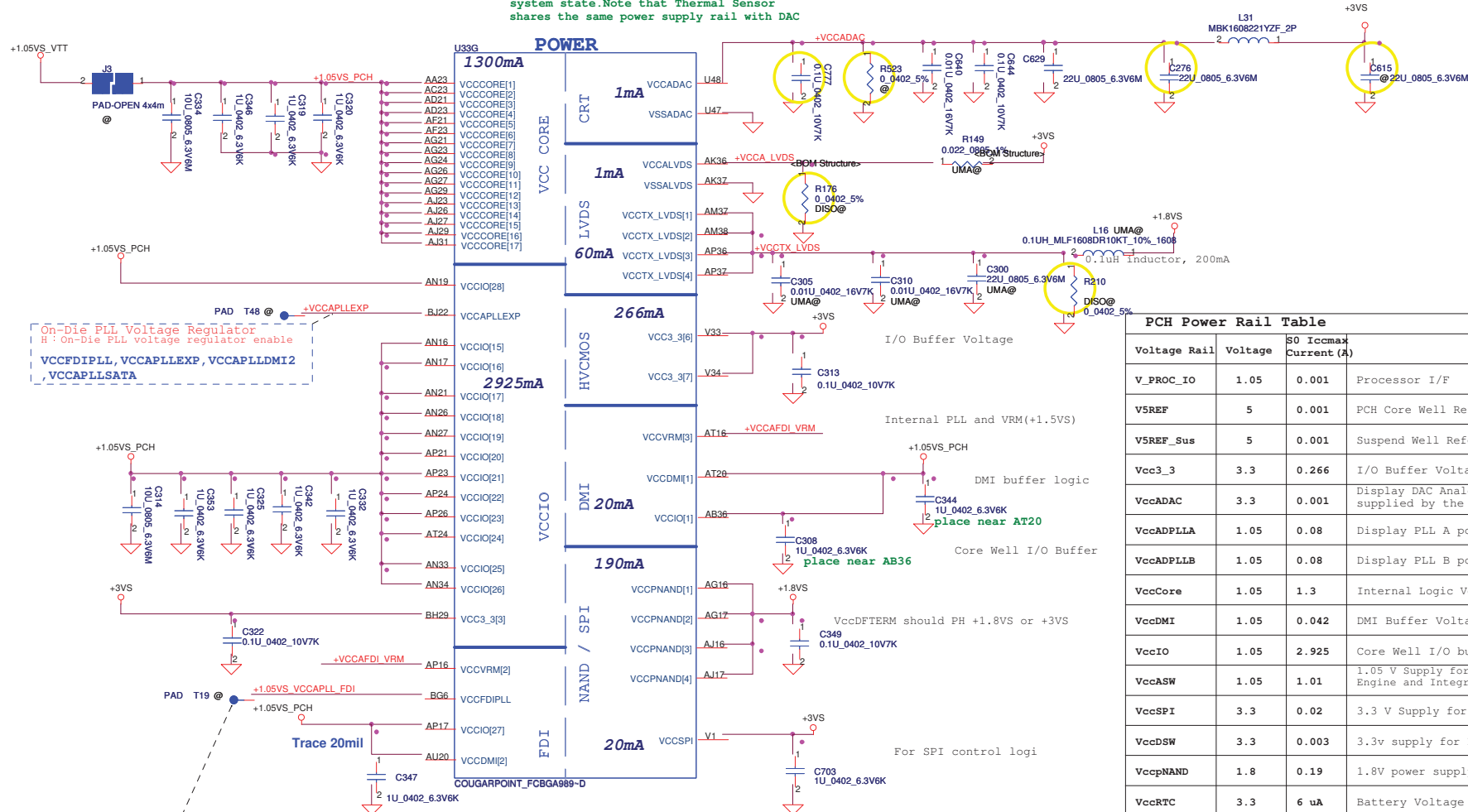
GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

CRB1.0 PH10K to +3VALW

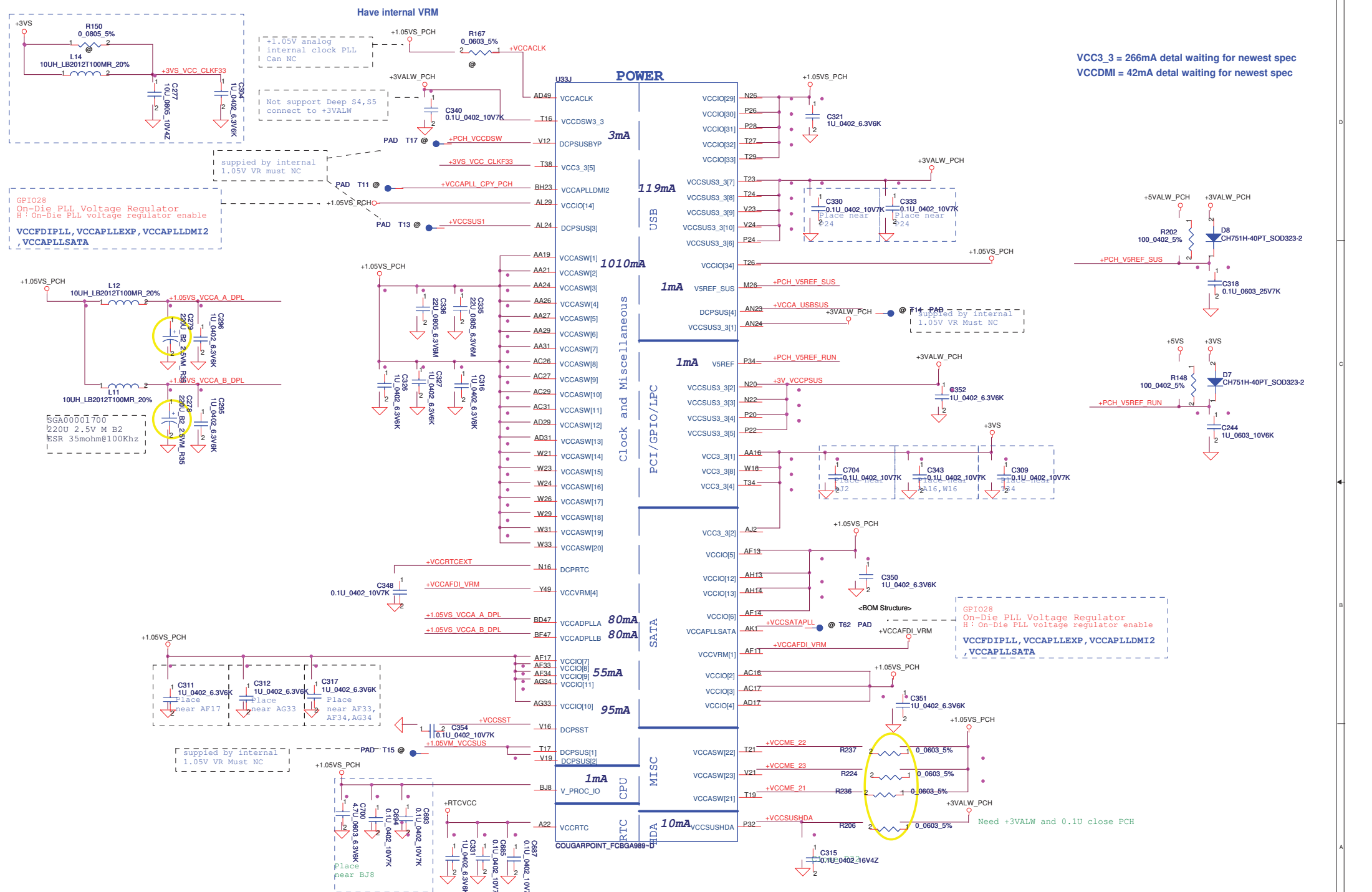


Project ID	GPIO69	GPIO70	GPIO71
★ P5WE0	0	0	0
P7YE0	0	0	0
x	0	1	0
x	0	1	1
x	1	0	0
x	0	0	1
x	0	1	0
x	0	1	1
x	1	0	0
x	1	0	1
x	1	1	0
x	1	1	1

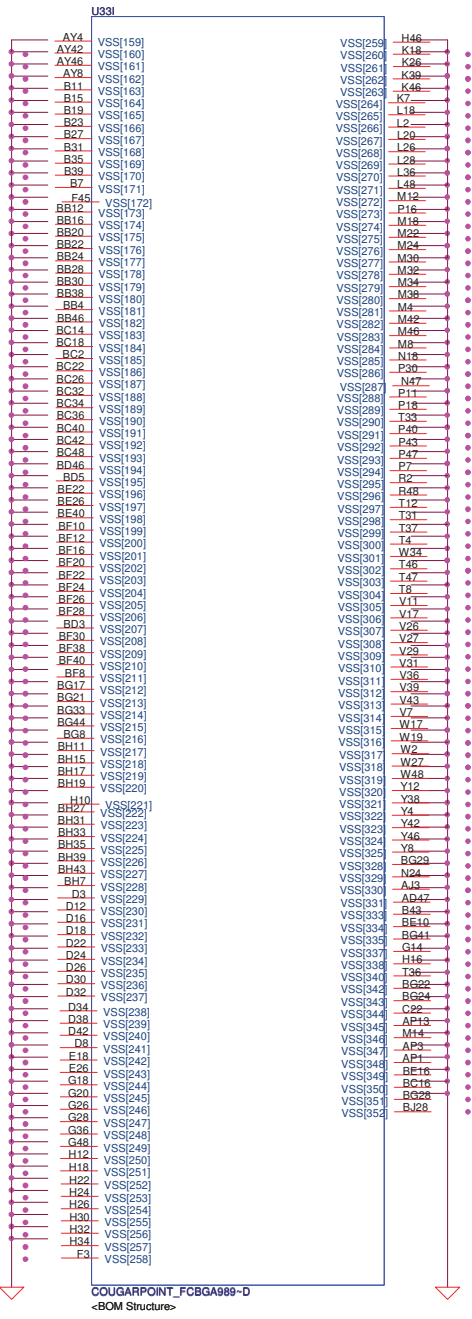
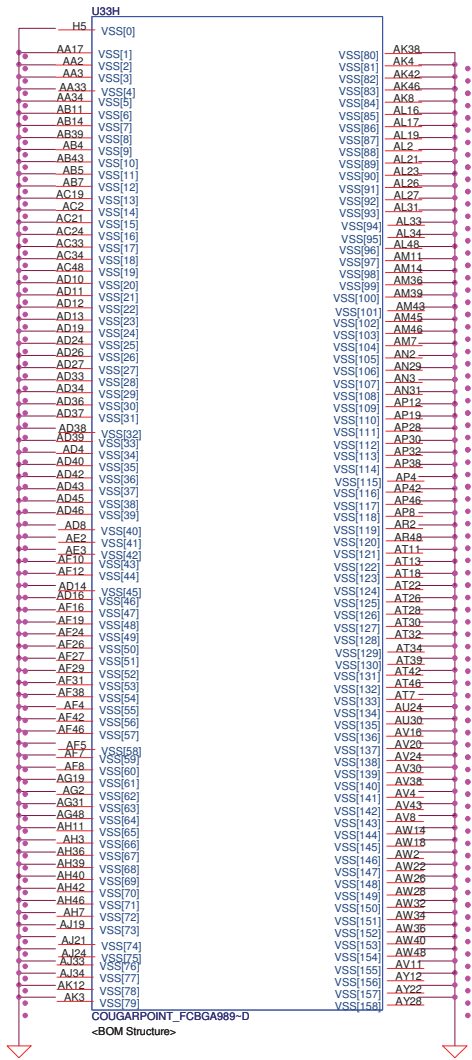
+VCCADAC should be powered up during S0 system state. Note that Thermal Sensor shares the same power supply rail with DAC



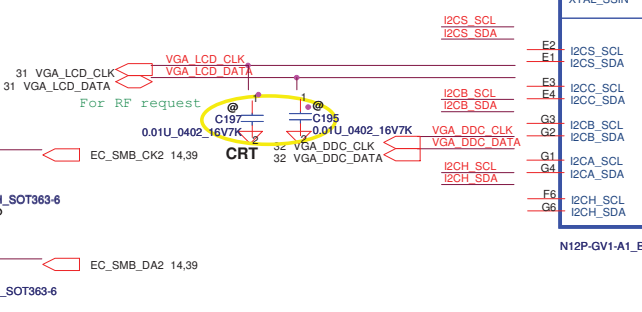
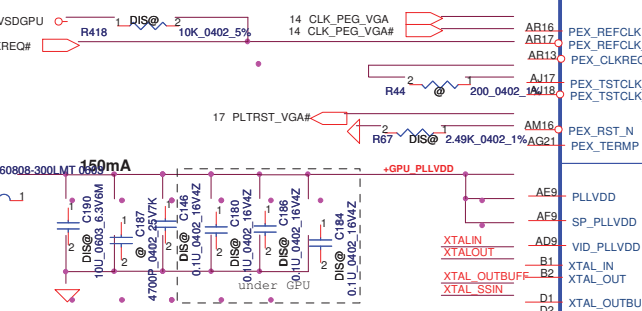
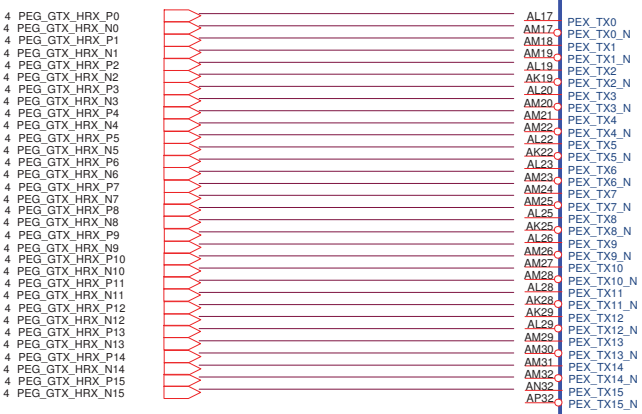
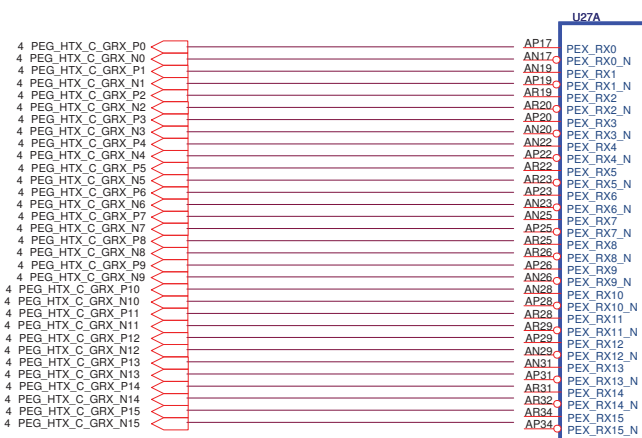
Voltage Rail	Voltage	S0 Iccmax Current (A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltage
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)



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GPIO

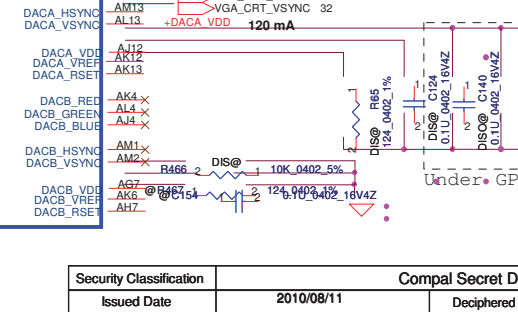
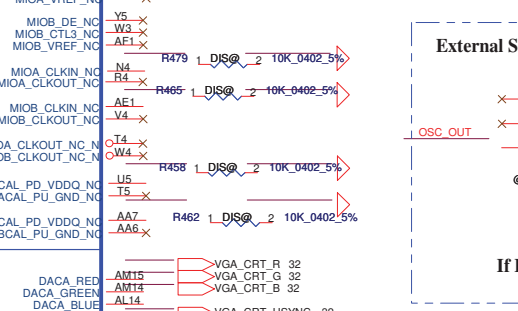
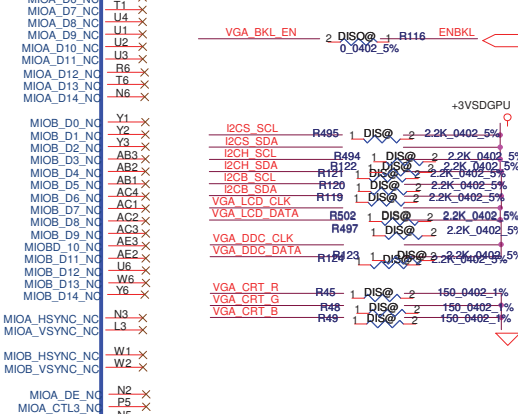
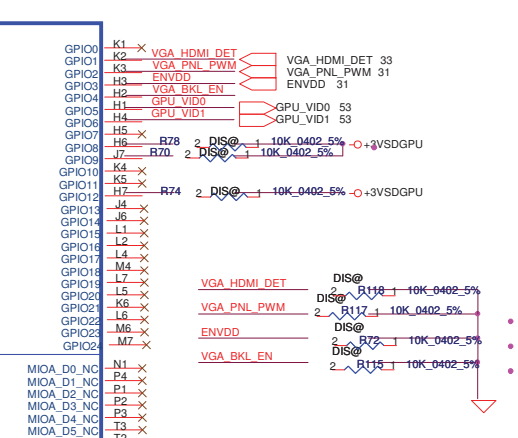
PCI EXPRESS

DVO

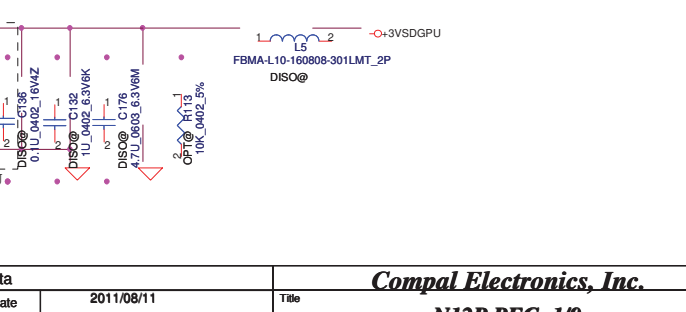
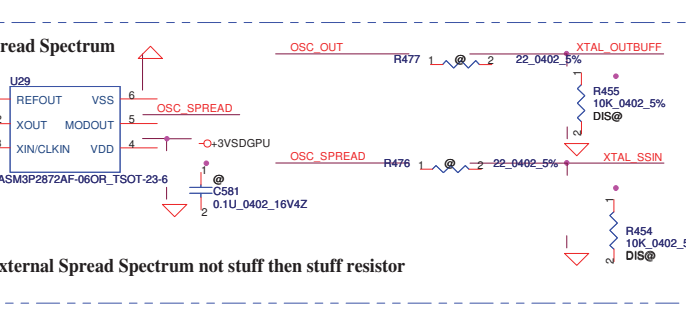
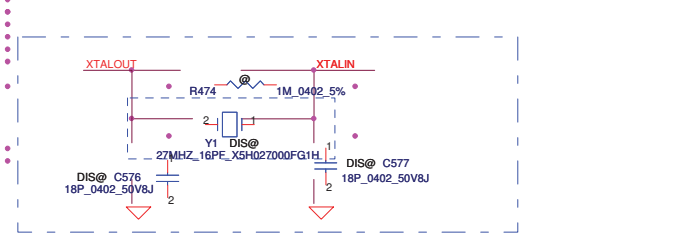
CLK

I2C

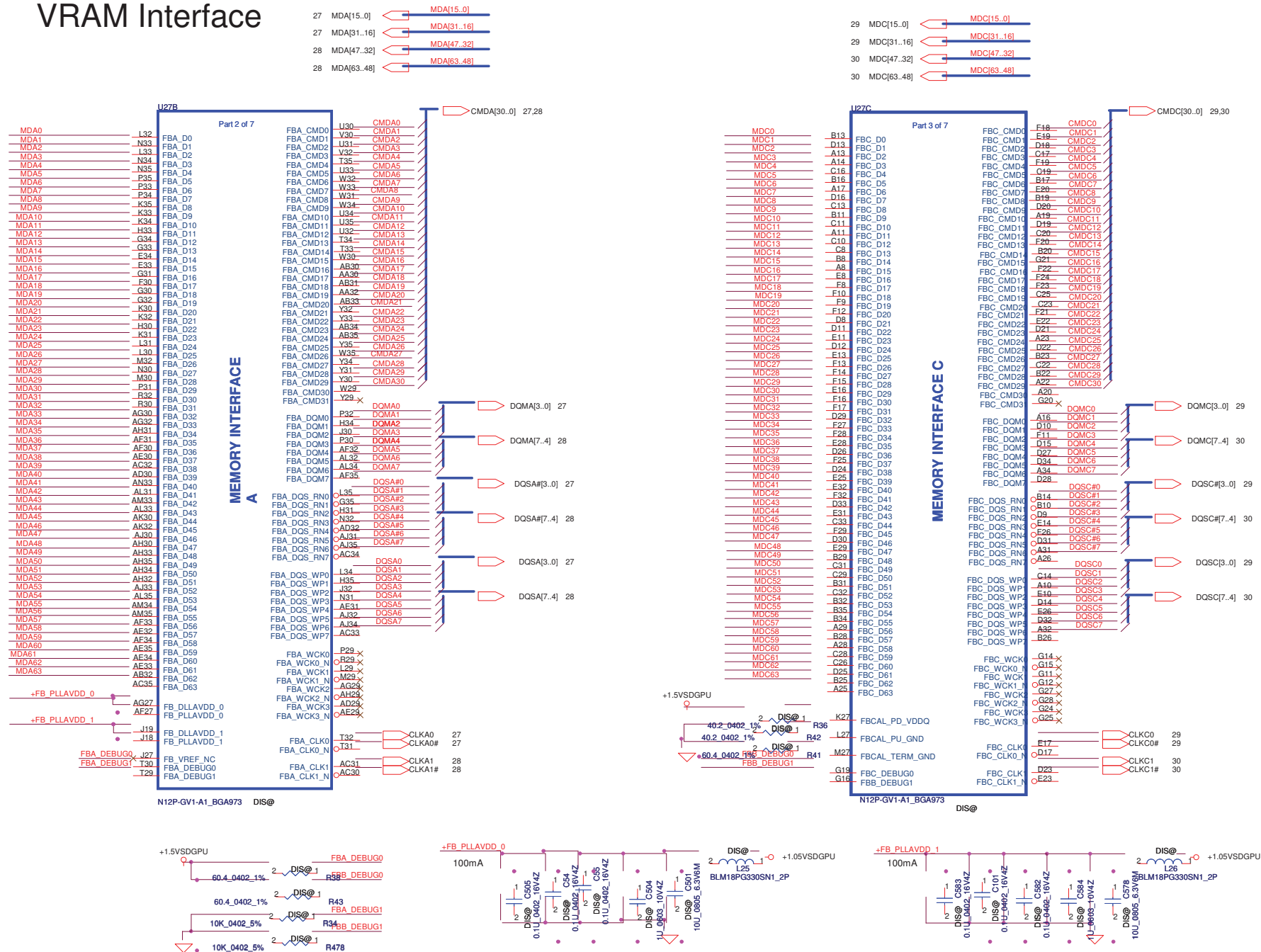
DACs



GPIO	I/O	USAGE
GPIO0	IN	N/A
GPIO1	IN	HPD_IFPC
GPIO2	OUT	N/A
GPIO3	OUT	N/A
GPIO4	OUT	N/A
GPIO5	OUT	GPU Core VID0
GPIO6	OUT	GPU Core VID1
GPIO7	OUT	N/A
GPIO8	IN	OVERT
GPIO9	OUT	ALERT
GPIO10	OUT	N/A
GPIO11	OUT	N/A
GPIO12	IN	PWR_LEVEL
GPIO13	OUT	N/A
GPIO14	OUT	N/A

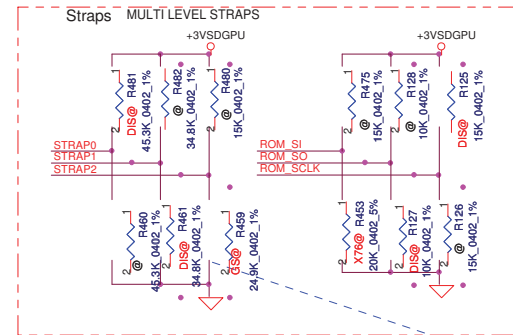
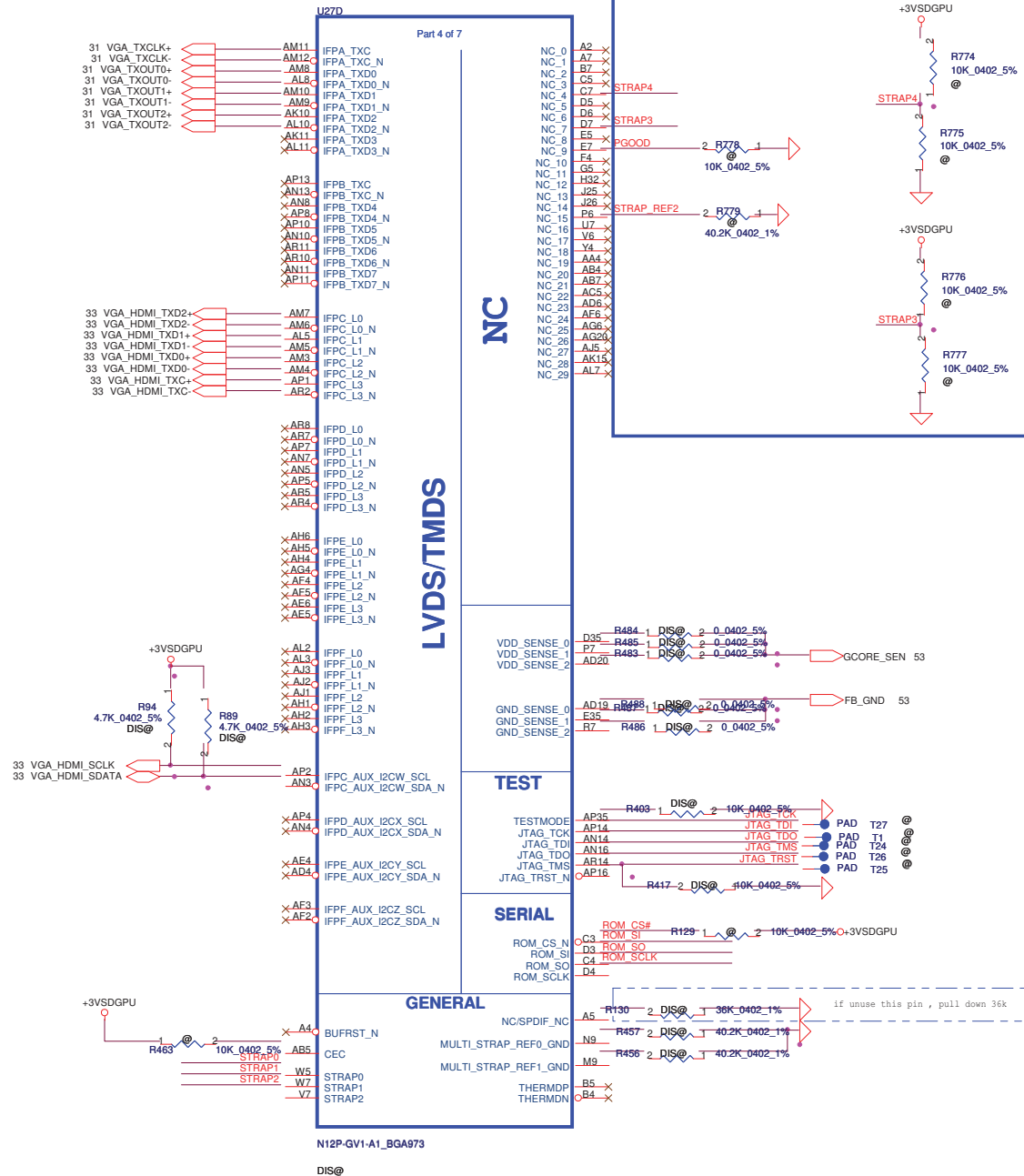


VRAM Interface



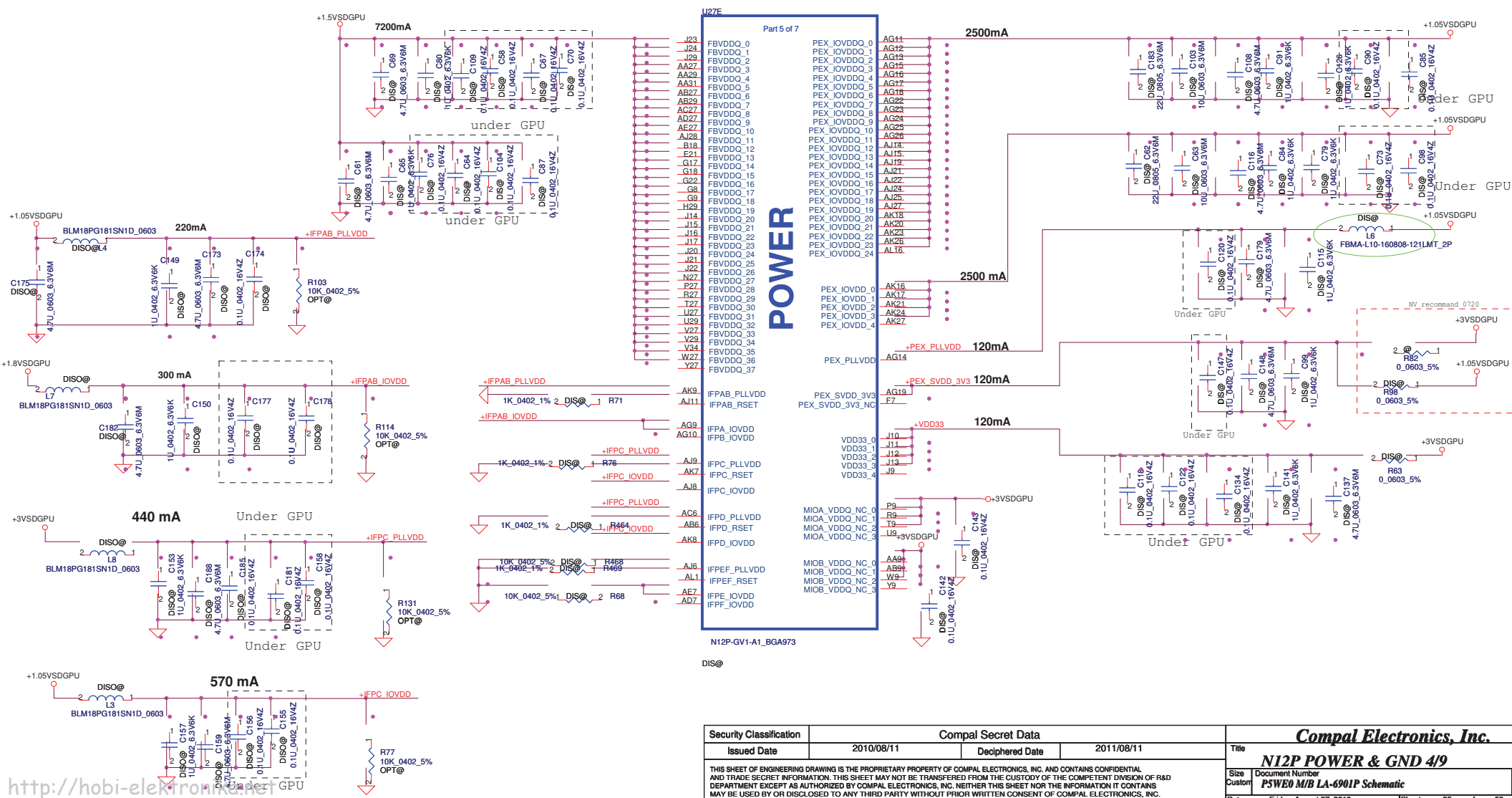
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For GB2-128 & GB2b-128 colayout....

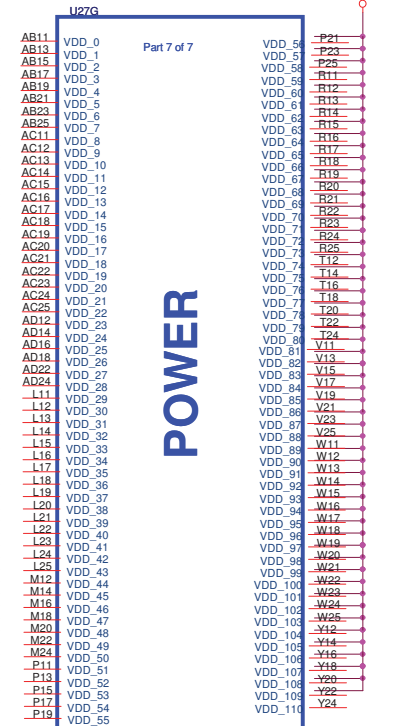
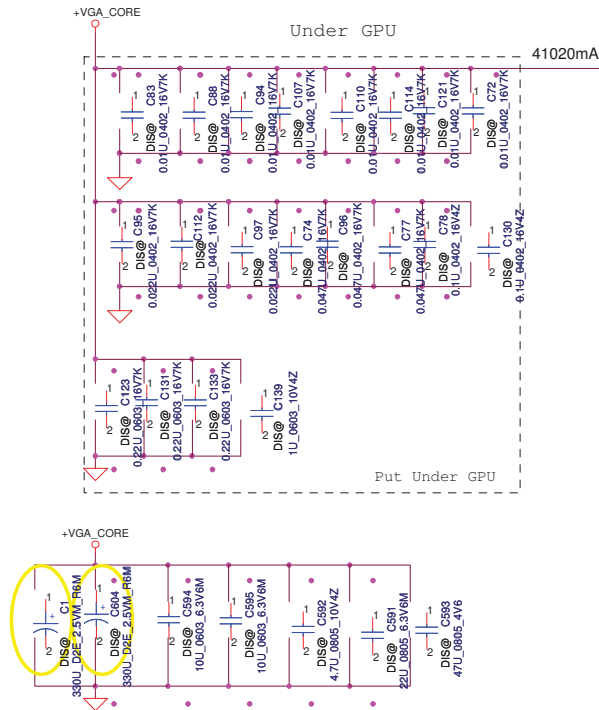
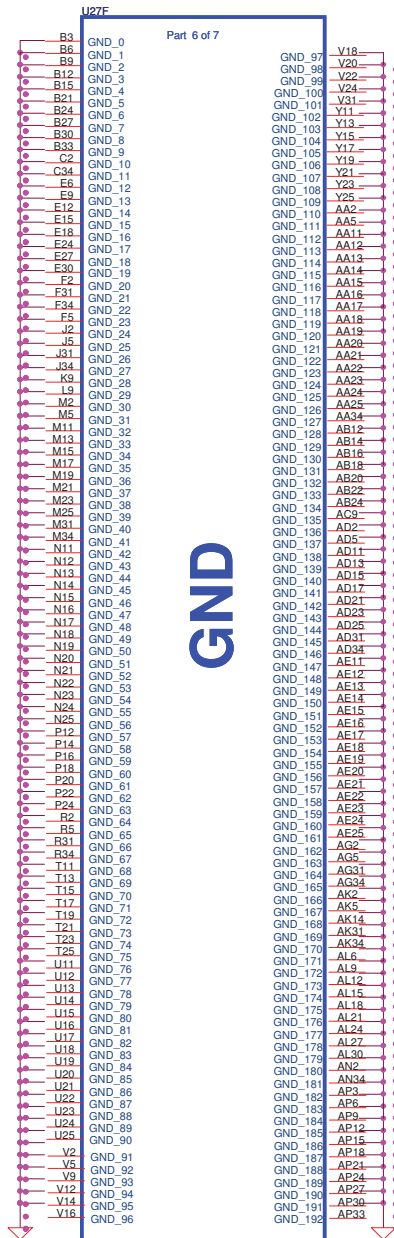


N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	L 35K	L 25K	L 20K	L 10K	H 15K
64MX16 Hynix SA000032400	H 45K	L 35K	L 25K	L 15K	L 10K	H 15K
128MX16 Samsung	H 45K	L 35K	L 25K	L 45K	L 10K	H 15K
128MX16 Hynix SA00003VS10	H 45K	L 35K	L 25K	L 35K	L 10K	H 15K

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				N12P LVDS 3/9 P5WE0 M/B LA-6901P Schematic
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						Size		Document Number		Rev	
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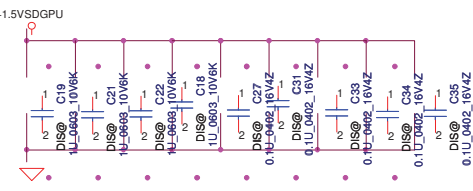
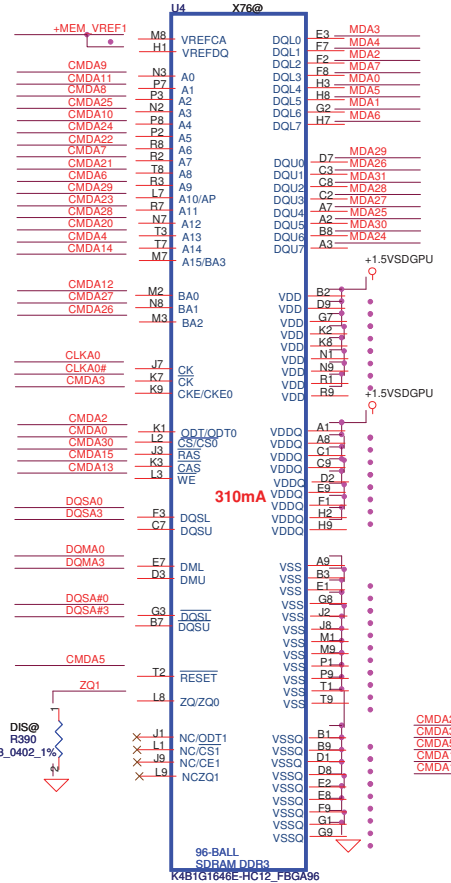
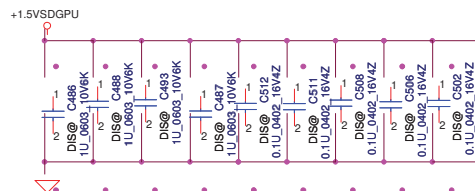
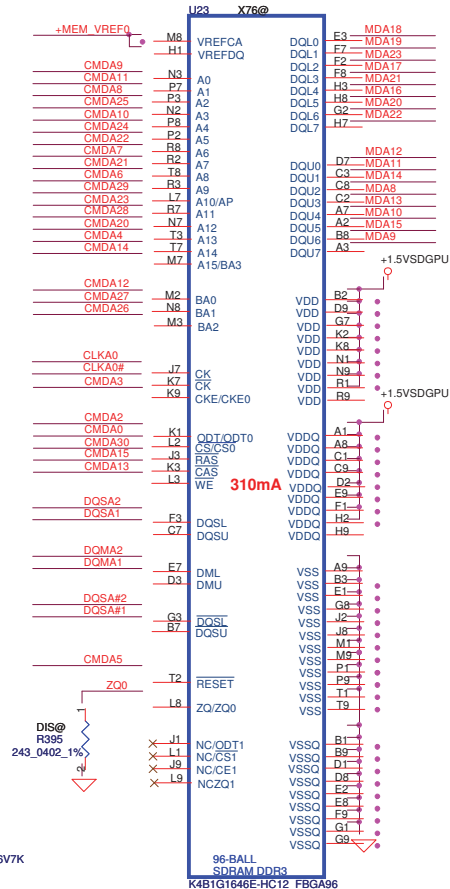
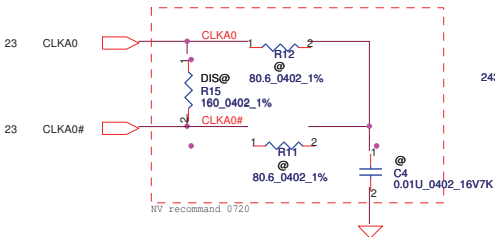
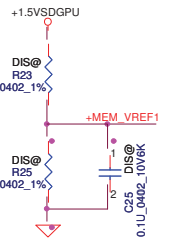
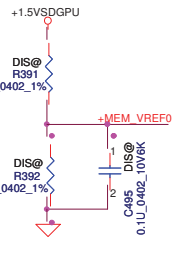


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VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

23,28 DQSA[7..0] DQSA#7..0
23,28 DQSA#7..0 DQSA#7..0
23,28 DQMA[7..0] DQMA#7..0
23,28 MDA[63..0] MDA#63..0
23,28 CMDA[30..0] CMDA#30..0

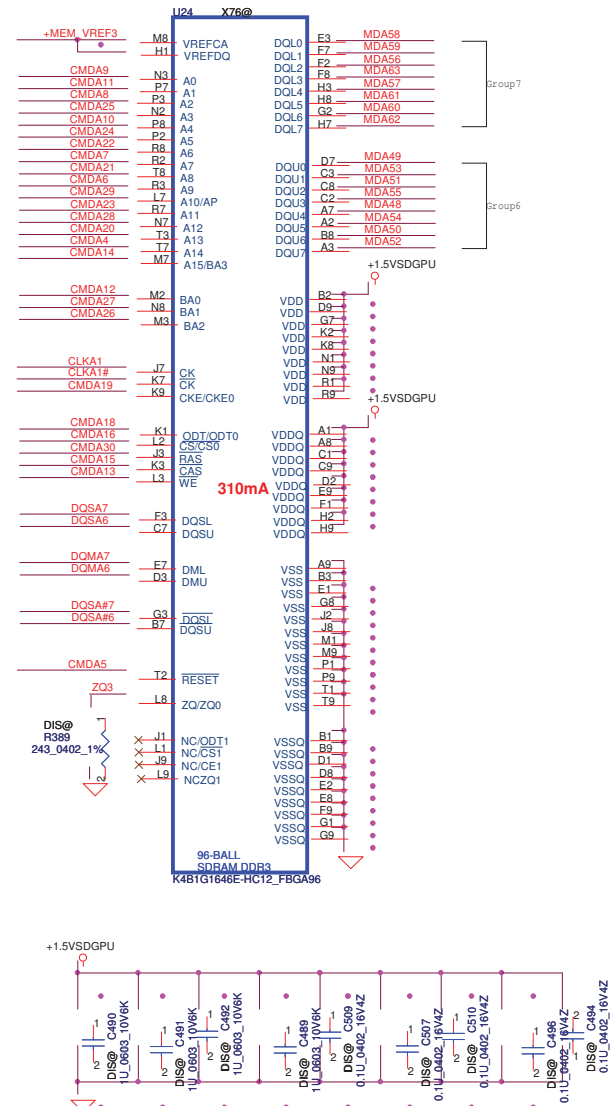
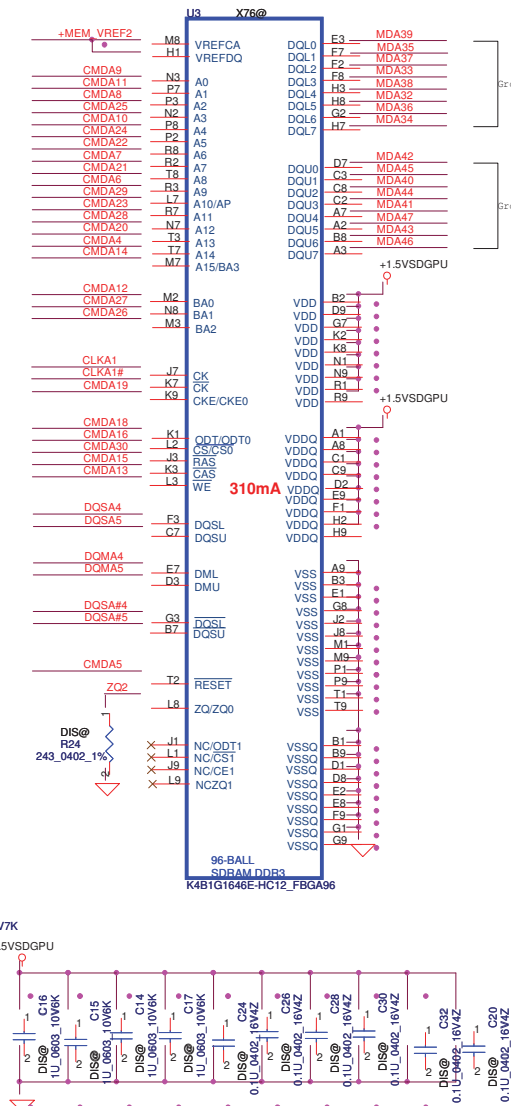


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16	CS0_H#	
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CAS*	No Termination

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD : SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFPGA 96P 1.5V)

64Mx16 DDR3 *8==>1GB



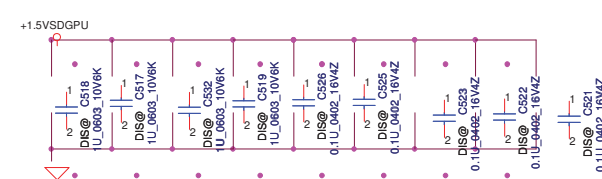
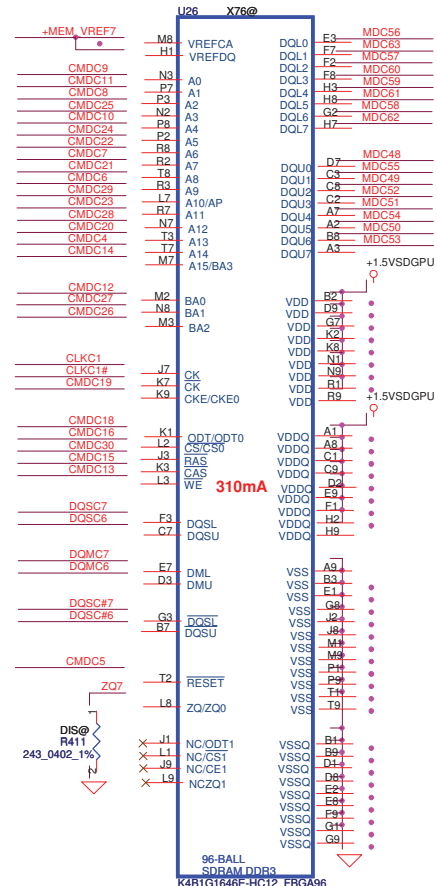
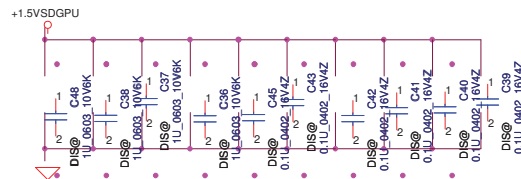
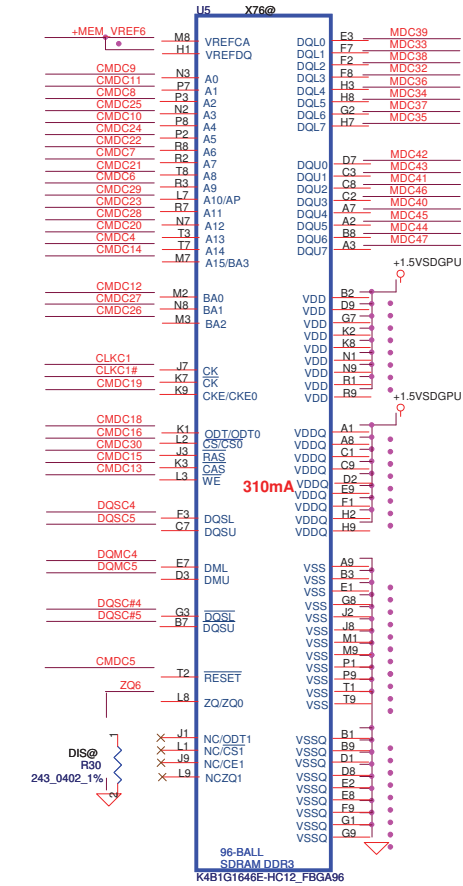
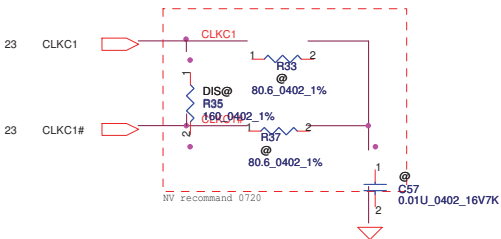
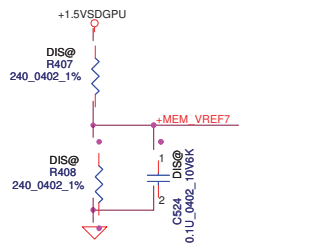
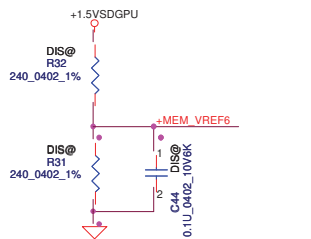
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CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

64Mx16 DDR3 *8==>1GB

VRAM DDR3 chips (1GB)

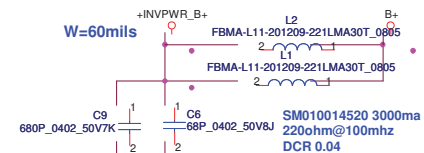
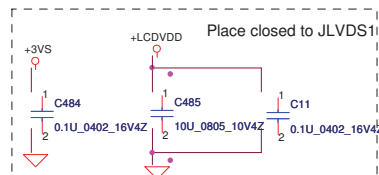
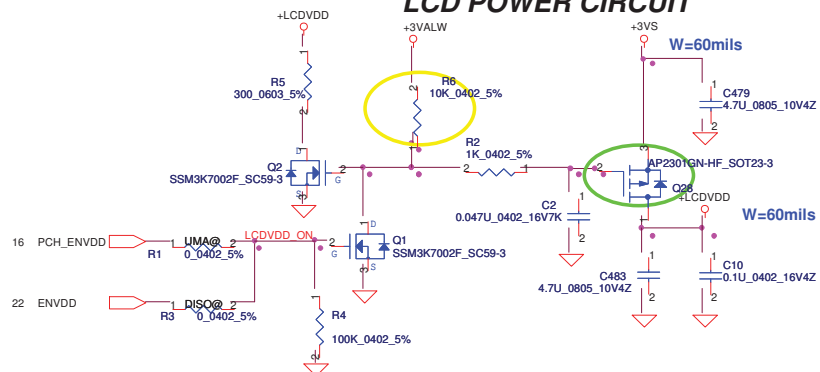
64Mx16 DDR3 *8==>1GB

23.29 DQMC[7..0] $\rightarrow$ DQMC[7..0]
23.29 CMDC[30..0] $\rightarrow$ CMDC[30..0]
23.29 DQSC#7[7..0] $\rightarrow$ DQSC#7[7..0]
23.29 DQSC[7..0] $\rightarrow$ DQSC[7..0]
23.29 MDC[63..0] $\rightarrow$ MDC[63..0]

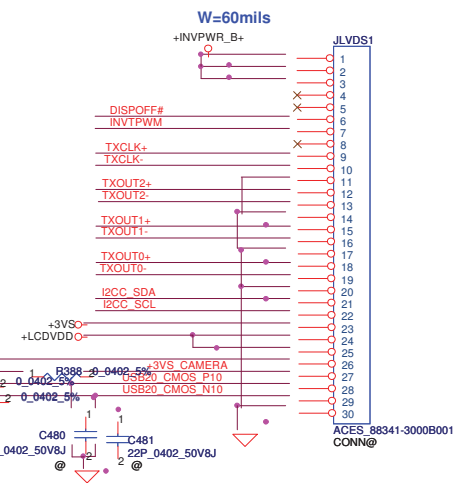
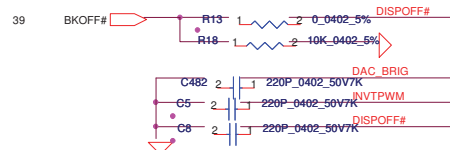


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available	LOW	HIGH

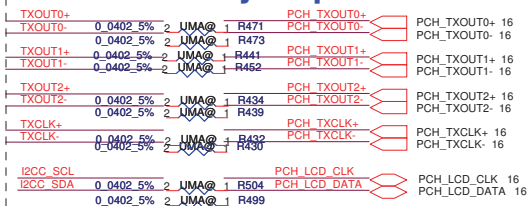
LCD POWER CIRCUIT



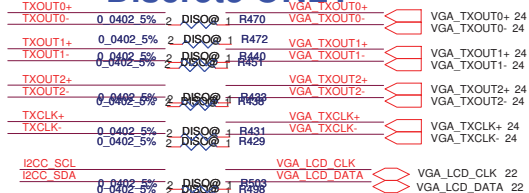
LCD/LED PANEL Conn.



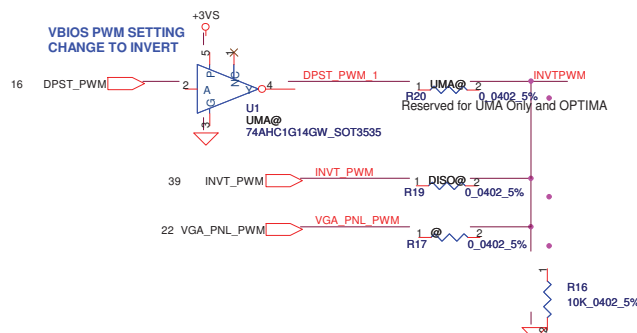
UMA Only / Optimus



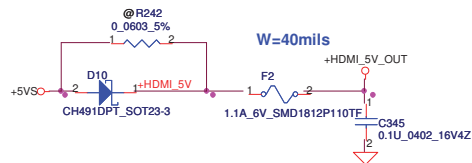
Discrete ONLY



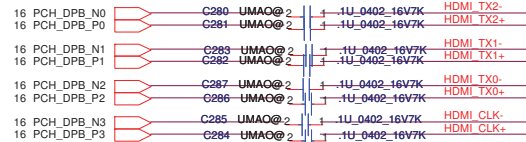
VBIOS PWM SETTING CHANGE TO INVERT



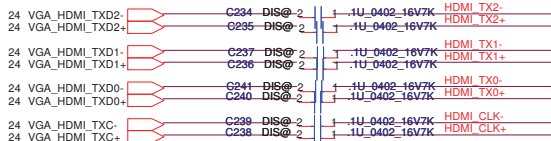
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/08/11	Deciphered Date	2011/08/11	Title	LVDS Connector
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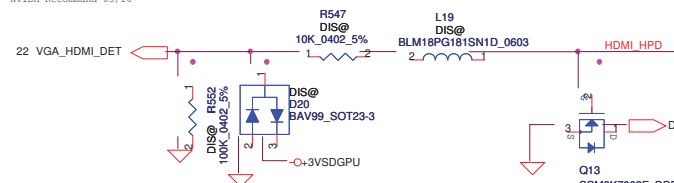
UMA



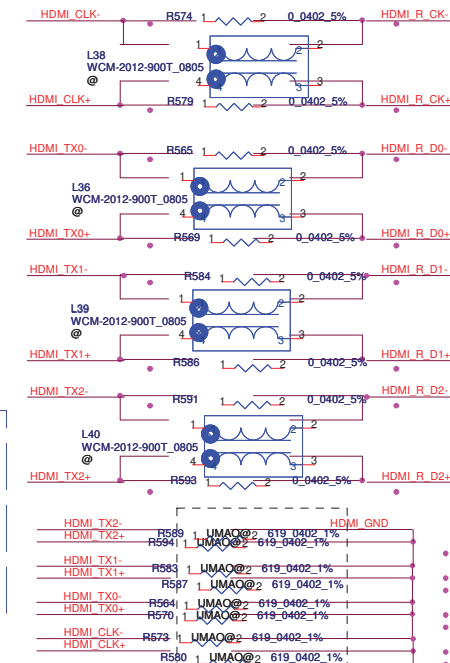
DIS



NVIDIA Recommend 05/10



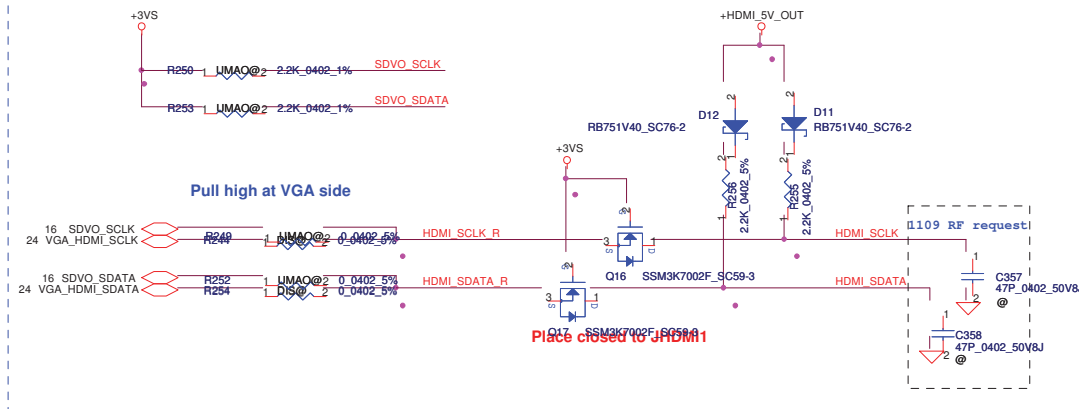
SMO70001310 400ma 90ohm@100mhz DCR 0.3



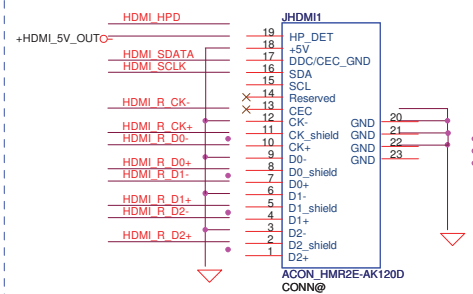
INTEL use 619 Ohm for termination

NV use 499 Ohm for termination

Pull high at VGA side



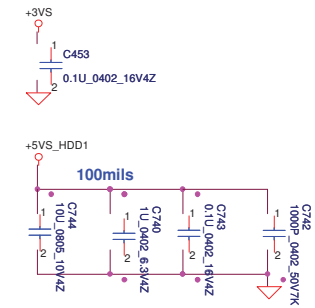
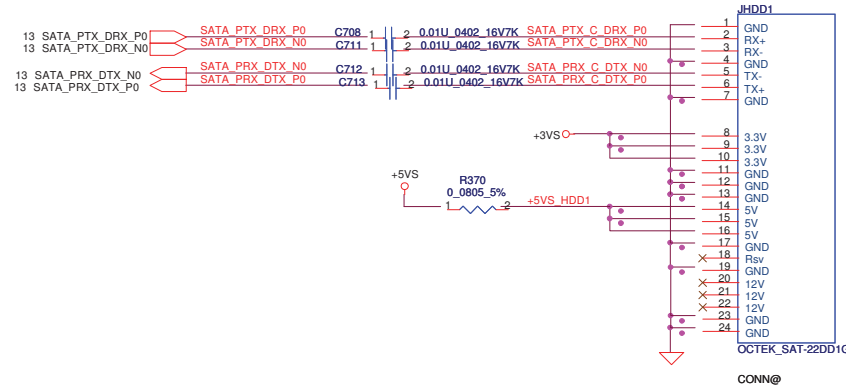
HDMI connector



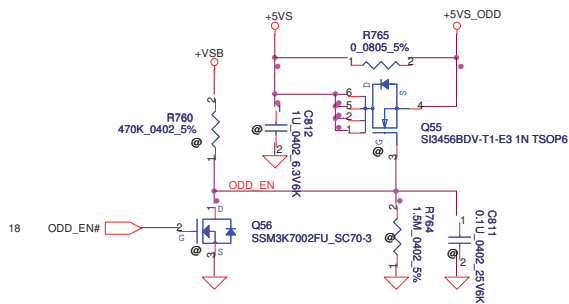
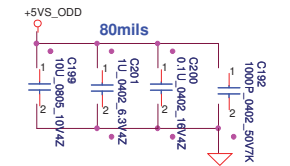
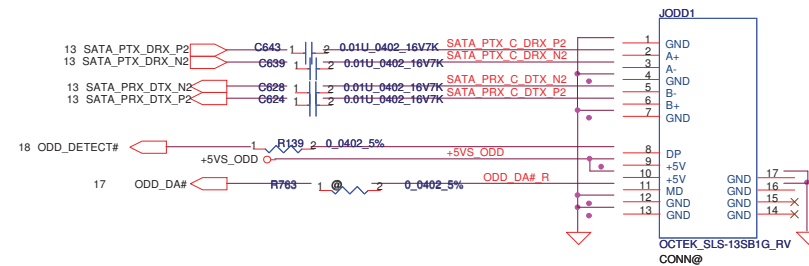
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Issued Date	2010/08/11	Deciphered Date	2011/08/11	Title	HDMI Conn
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SATA HDD1 Conn.

CL 4.0 mm



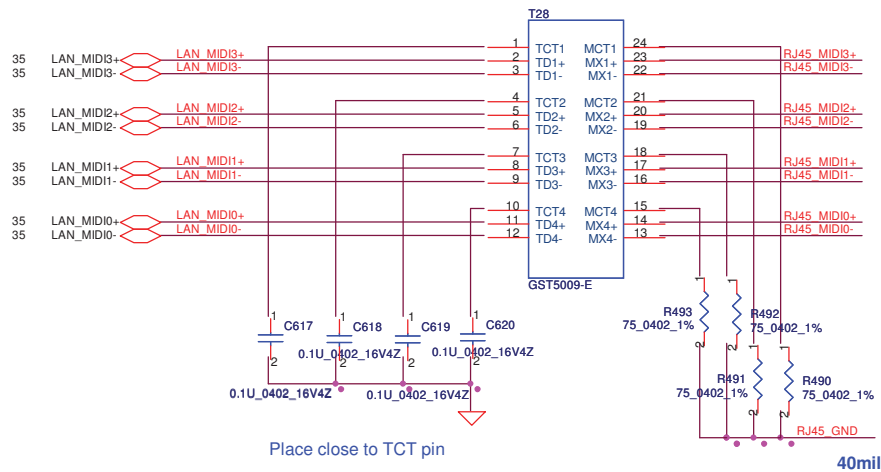
SATA ODD Conn.



Security Classification			Compal Secret Data		Compal Electronics, Inc.	
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				Custom	P5WE0 M/B LA-6901P Schematic	0.1
				Date	Friday, August 27, 2010	Sheet 34 of 50

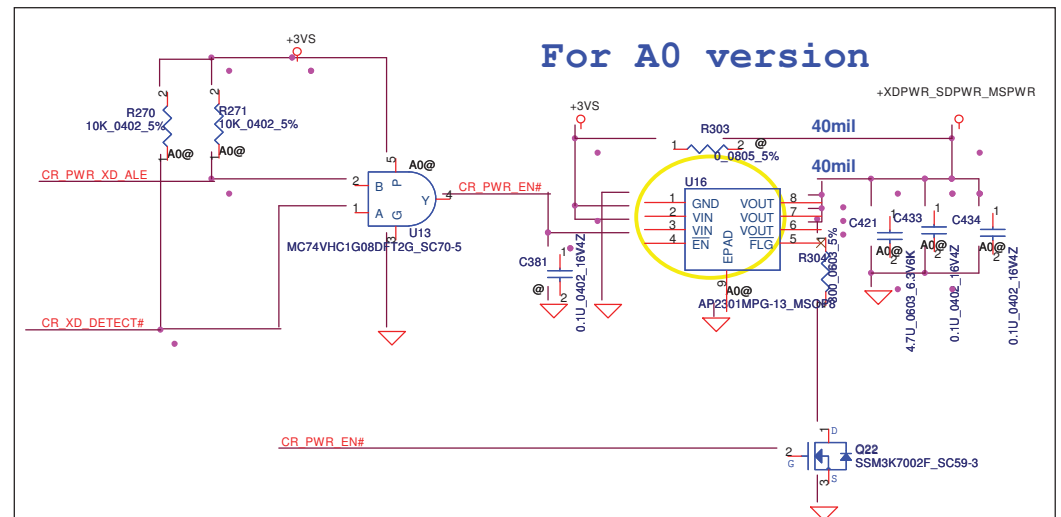
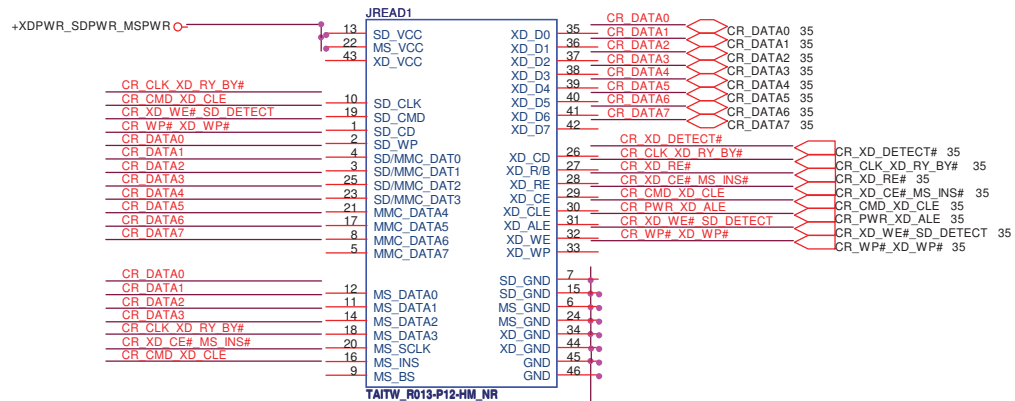


LAN Connector



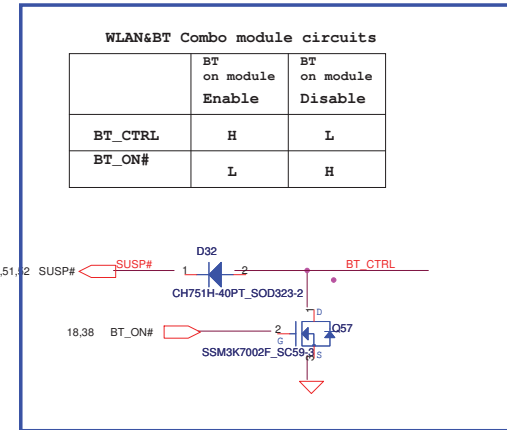
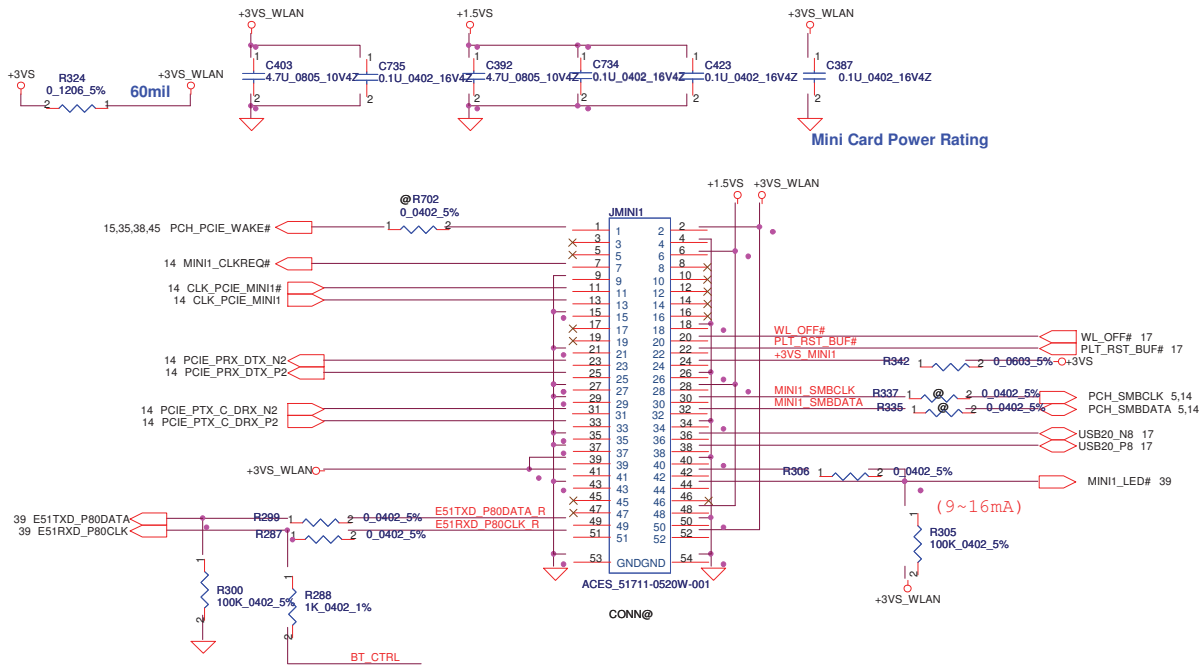
BOTH HAND: S X'FORM_GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_IH-160 LAN, SP050006F00

Card Reader Connector

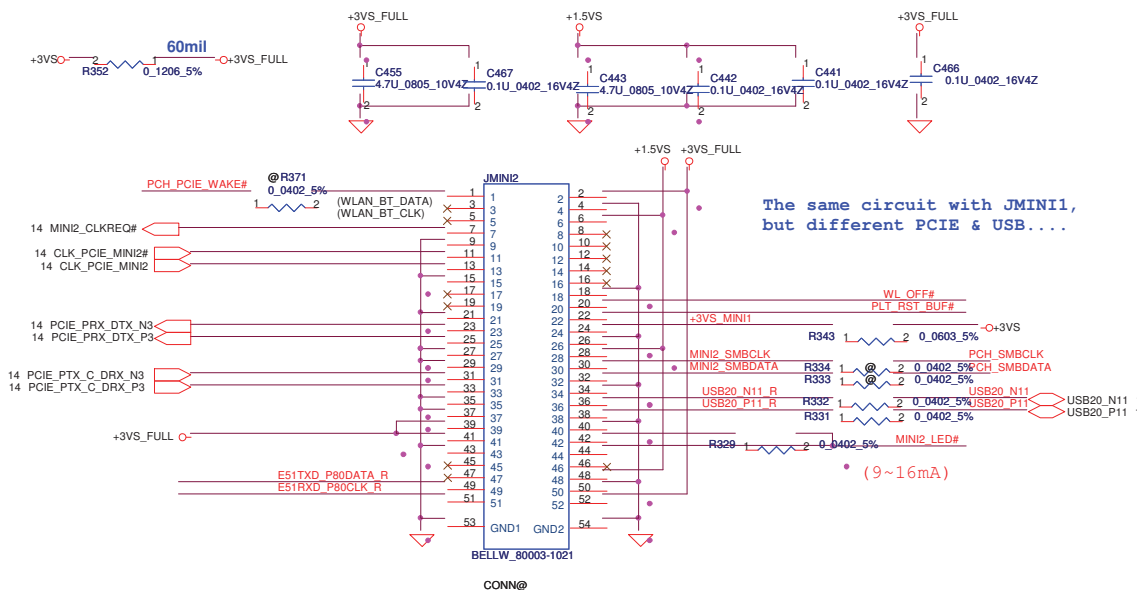


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Size	Document Number	Customer	P5WE0 M/B LA-6901P Schematic	Rev	0.1
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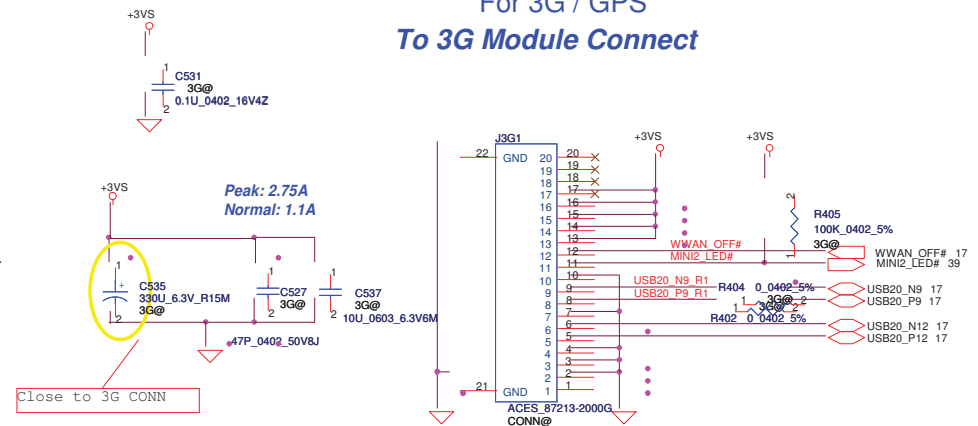
For Wireless LAN



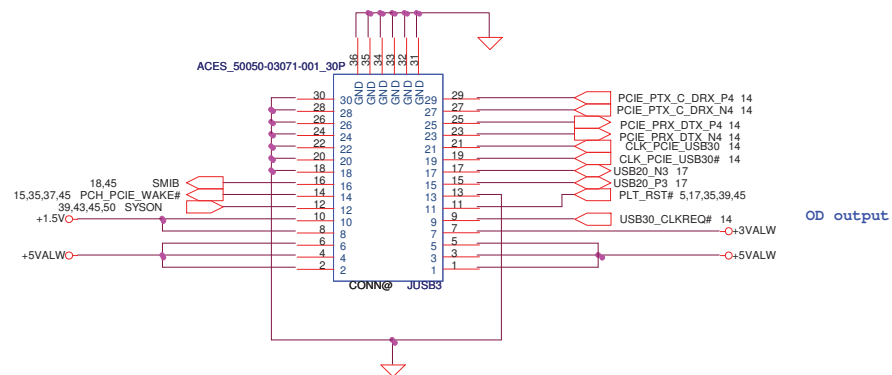
Reserve



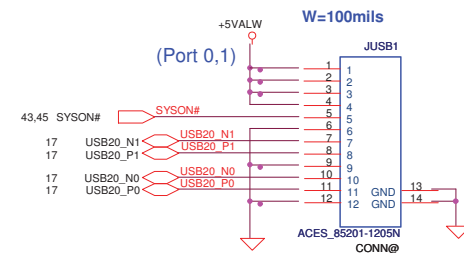
For 3G / GPS To 3G Module Connect



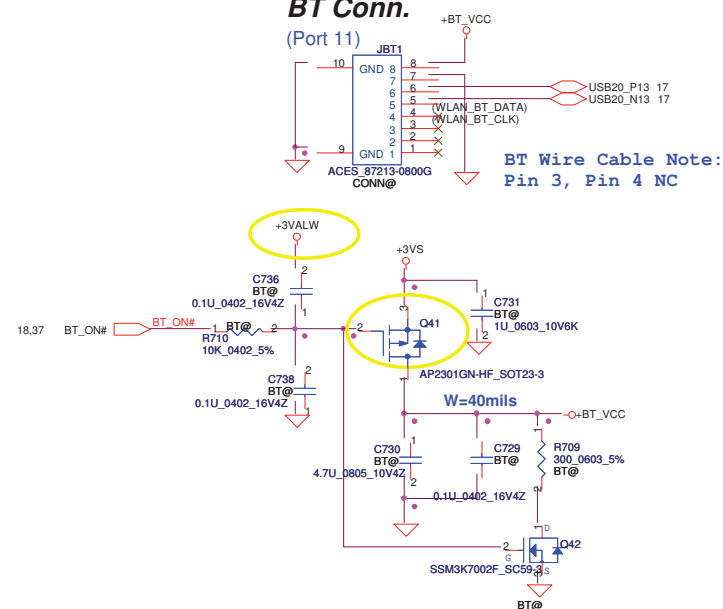
USB3.0 Conn.



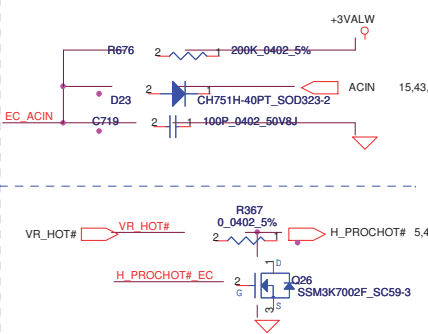
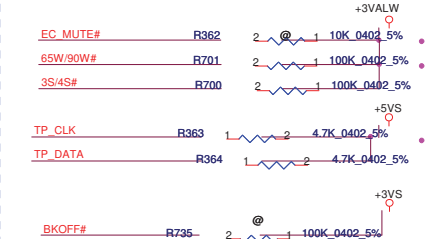
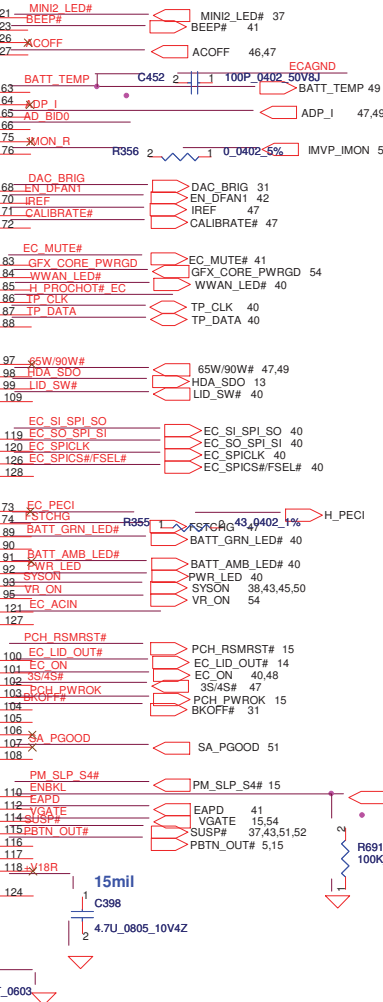
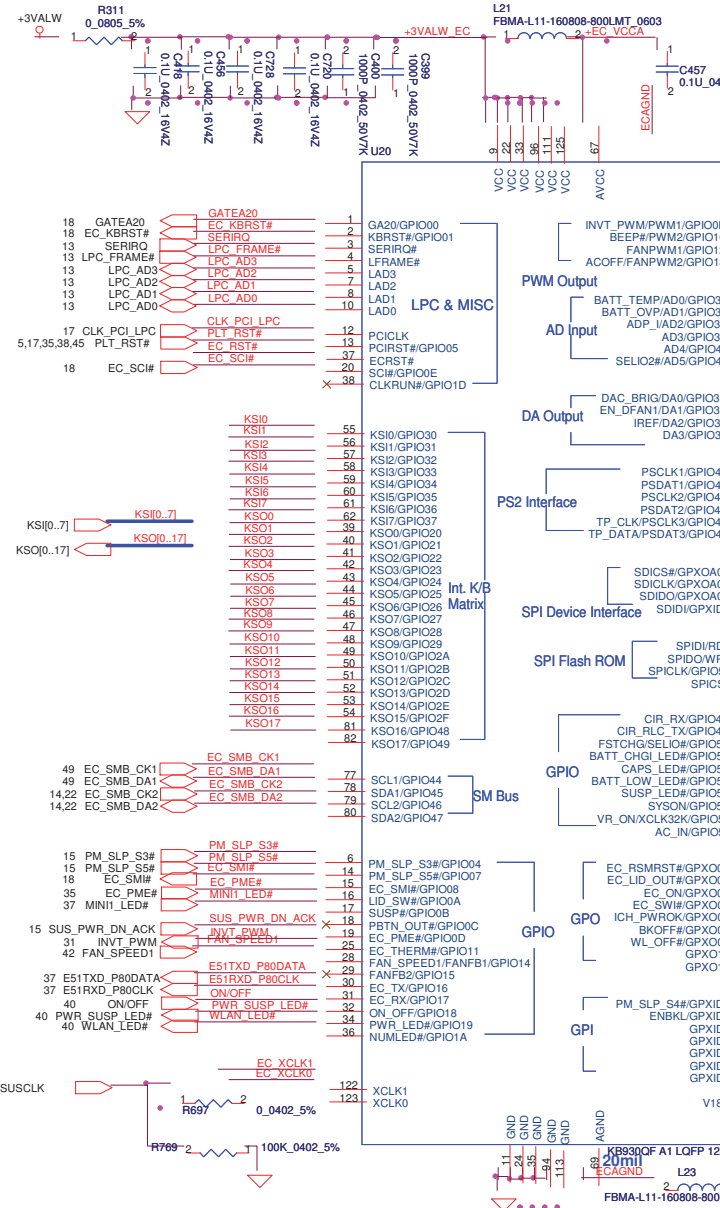
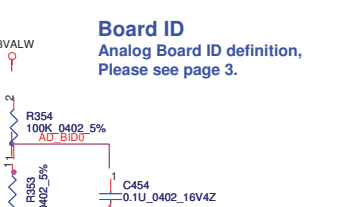
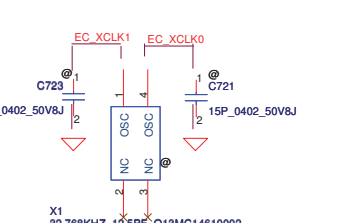
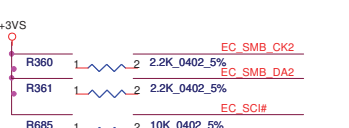
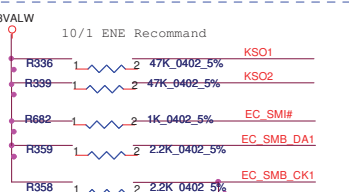
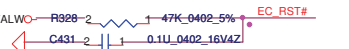
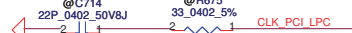
USB/B Conn.



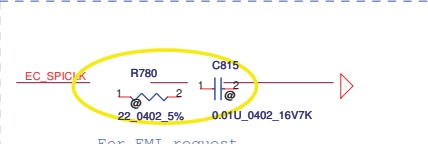
BT Conn.



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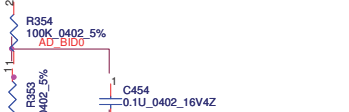
Latest design guide suggest change QE1 to 74LVC1G06.



For EMI request

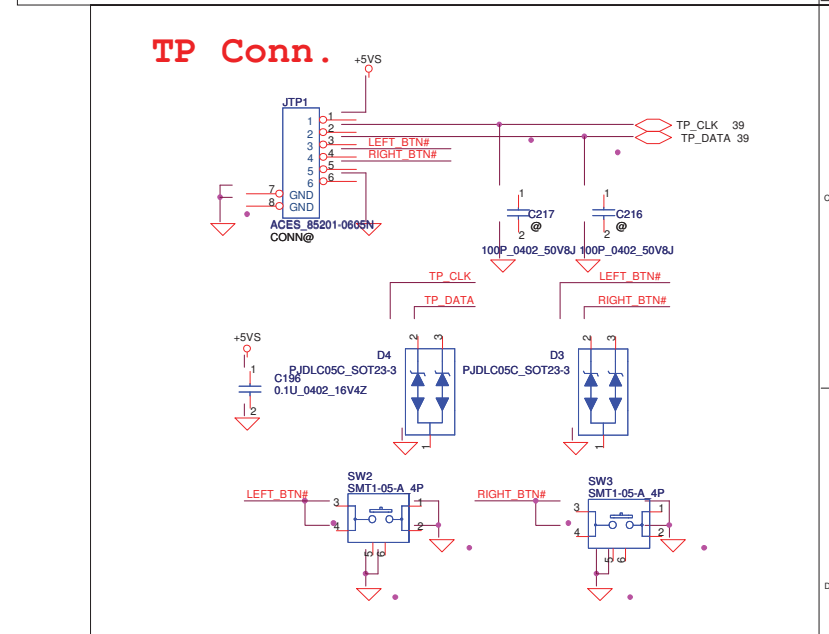
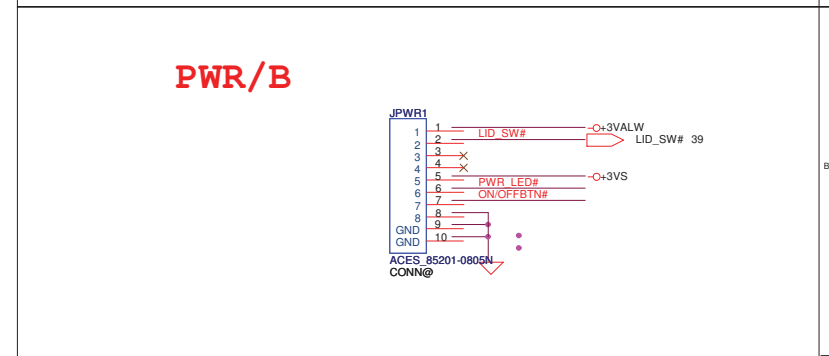
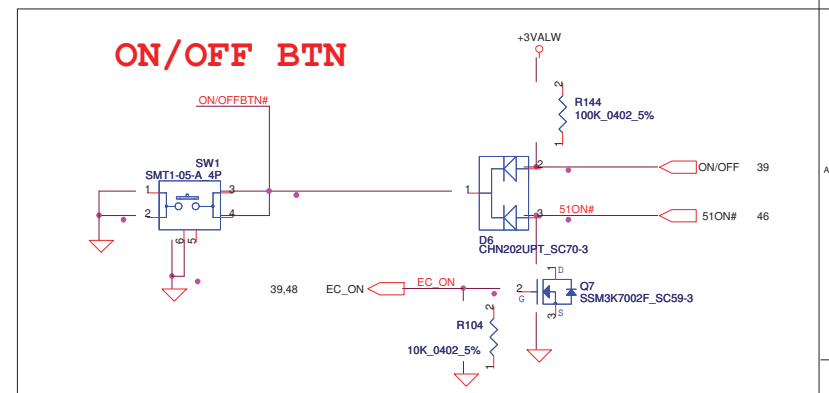
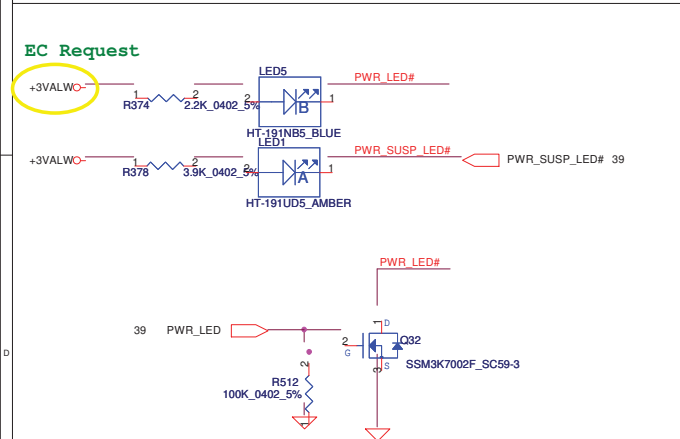
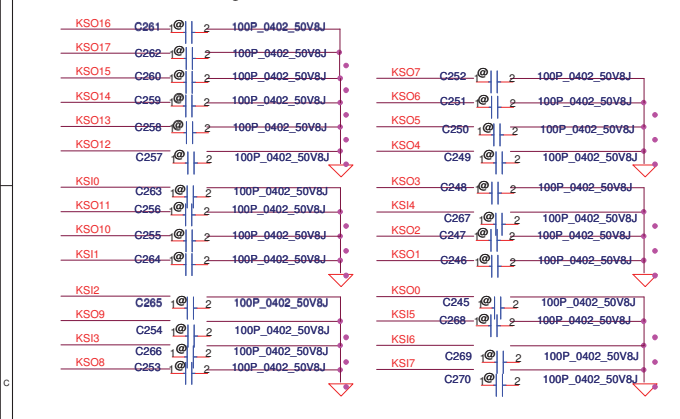
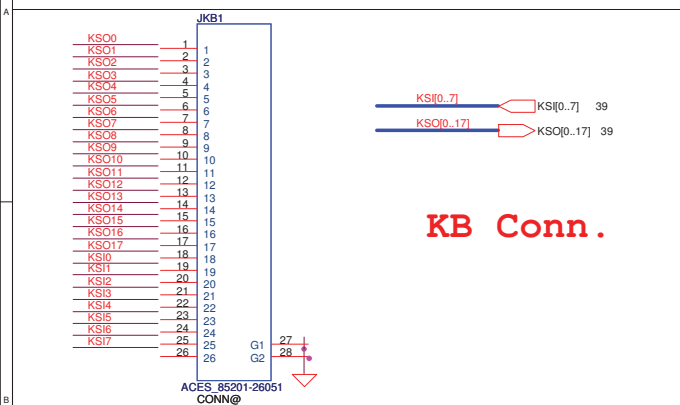
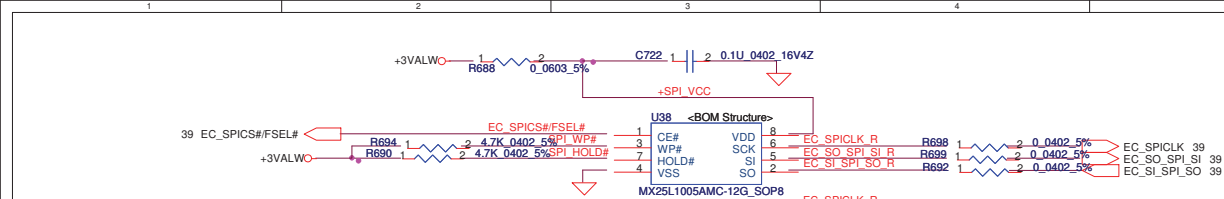


Board ID
Analog Board ID definition,
Please see page 3.

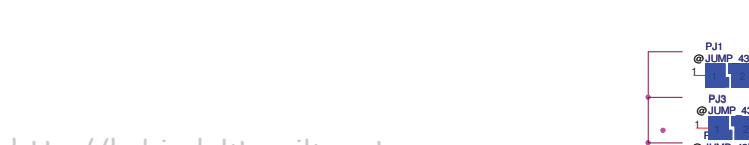
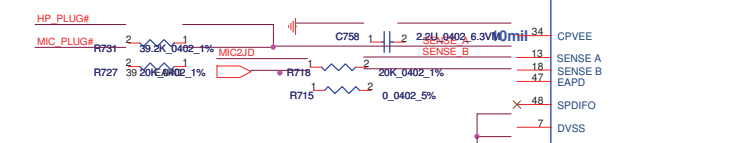
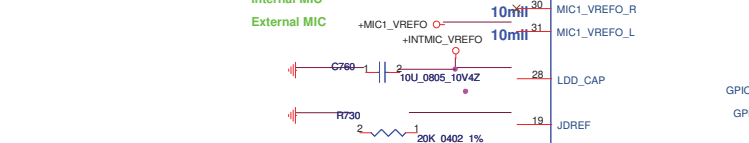
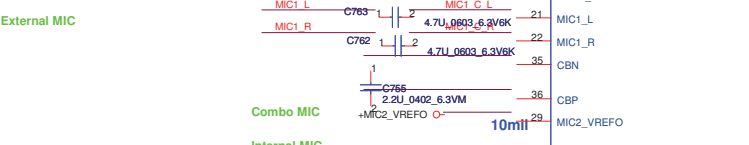
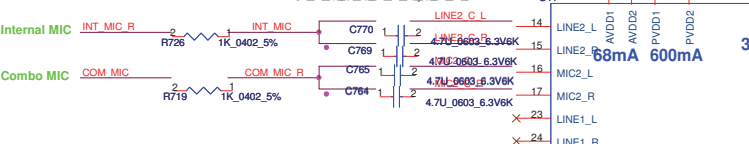
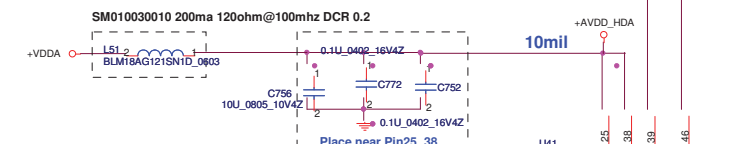
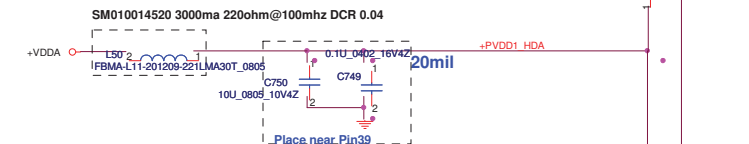
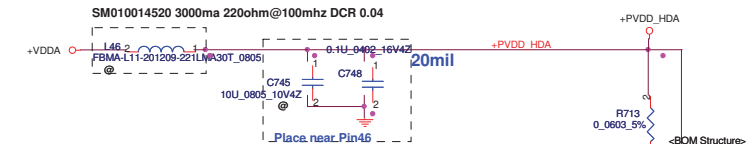
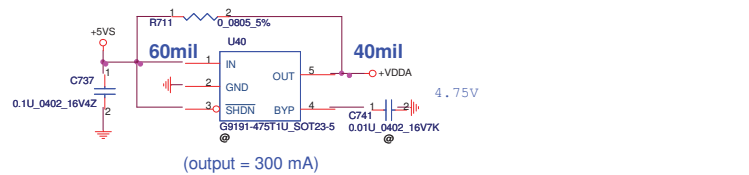


http://nobi-elektronika.net

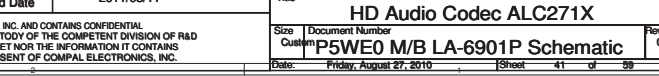
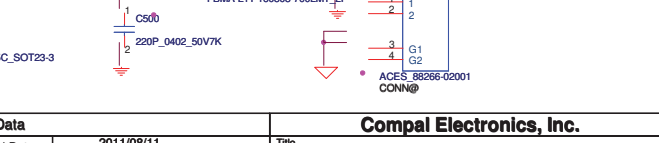
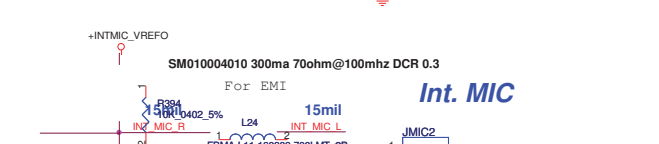
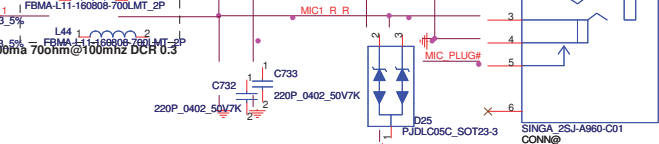
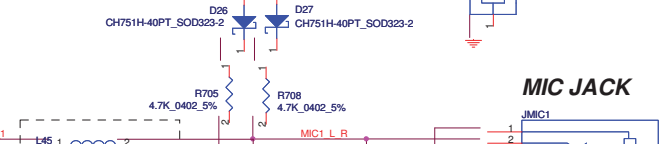
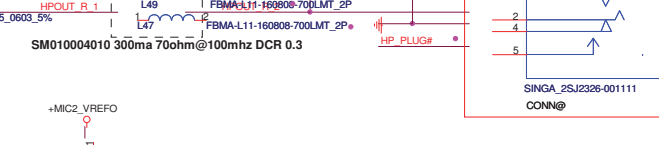
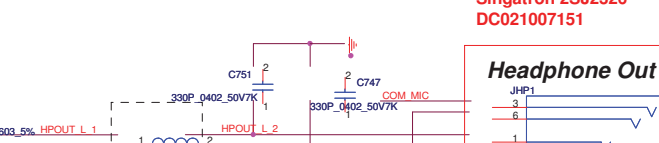
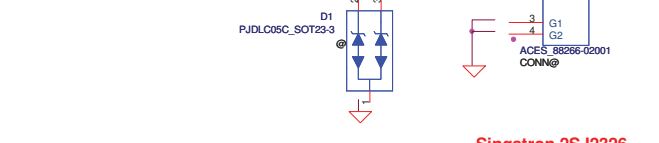
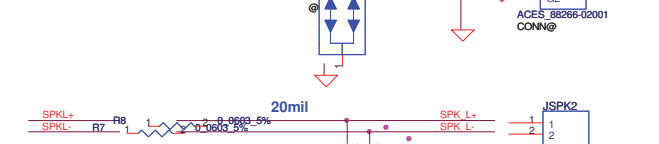
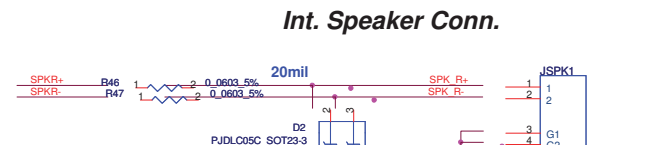
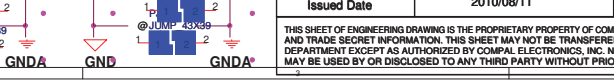
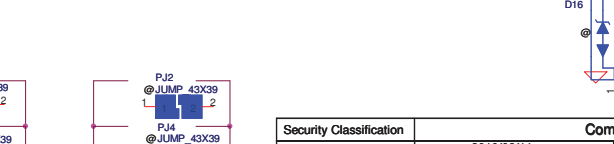
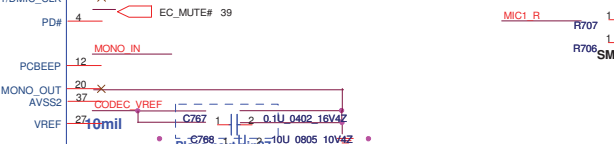
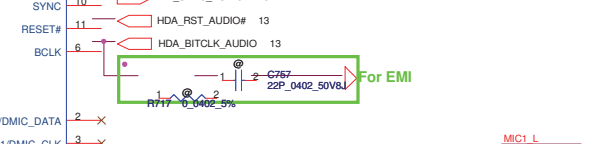
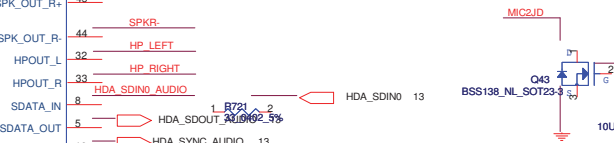
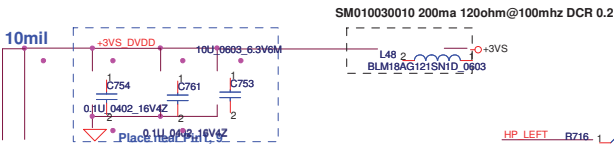
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Issued Date	2010/08/11	Deciphered Date	2011/08/11	Title	EC ENE-KB930
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				Size	Document Number
				Customer	P5WE0 M/B LA-6901P Schematic
				Date	Friday, August 27, 2010
				Sheet	40 of 59



HD Audio Codec



Int. Speaker Conn.

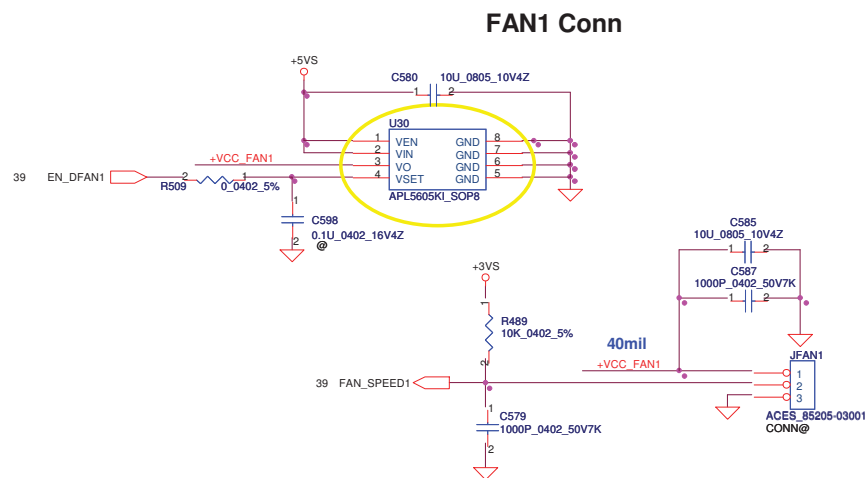
Singatron 2SJ2326
DC021007151

Headphone Out

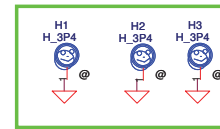
MIC JACK

Int. MIC

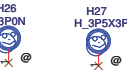
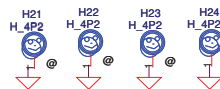
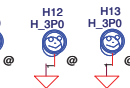
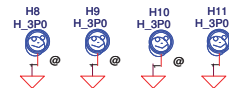
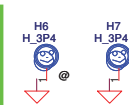
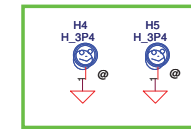
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Issued Date	2010/08/11	Deciphered Date	2011/08/11	Title	
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				Size Document Number	
				P5WE0 M/B LA-6901P Schematic	
				Date: Friday, August 27, 2010	
				Sheet 41 of 98	



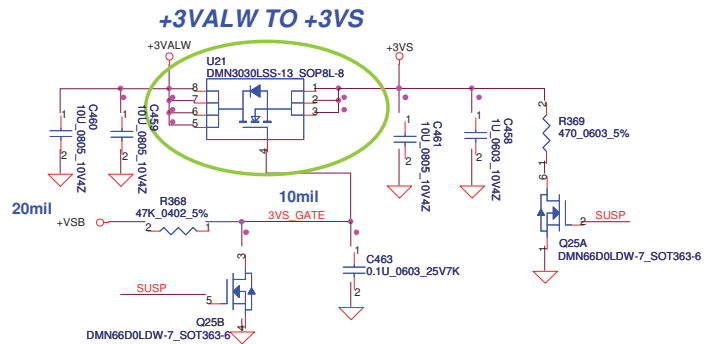
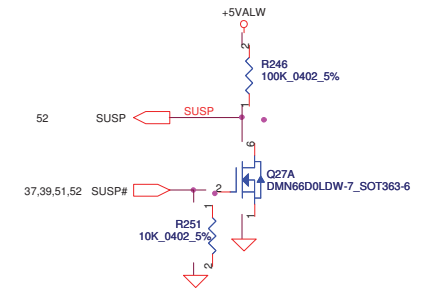
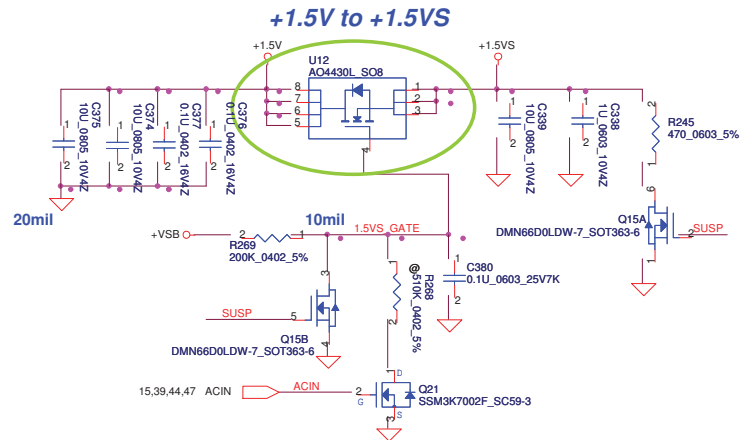
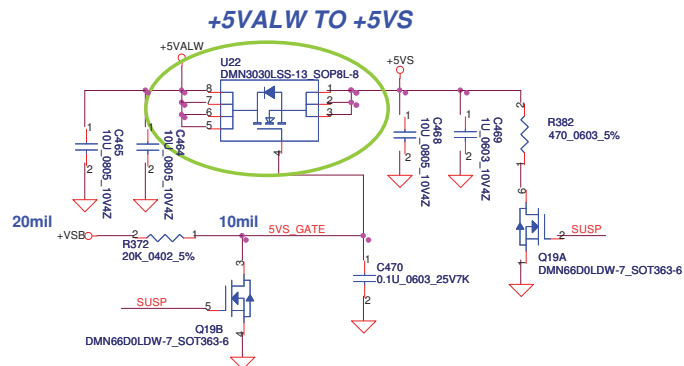
FAN Stand-Off



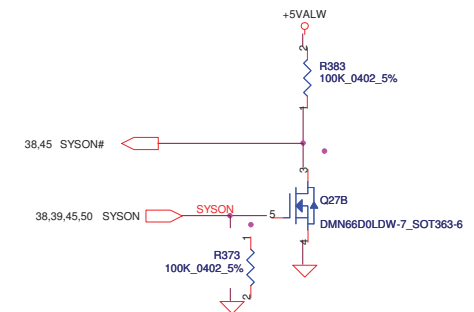
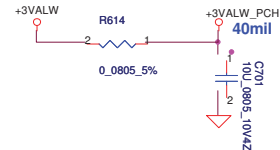
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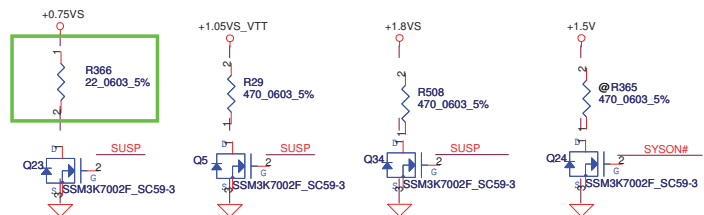
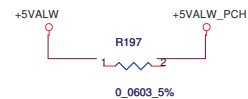
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				Size	Document Number
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				Date:	Friday, August 27, 2010
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+3VALW TO +3VALW_PCH(PCH AUX Power)

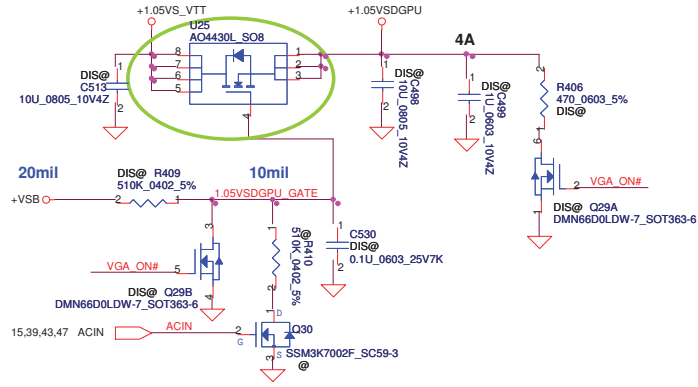


+5VALW TO +5VALW_PCH(PCH AUX Power)

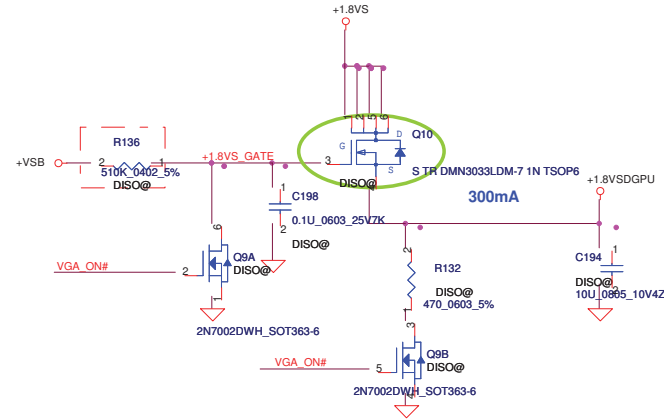


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59		59		59		59	

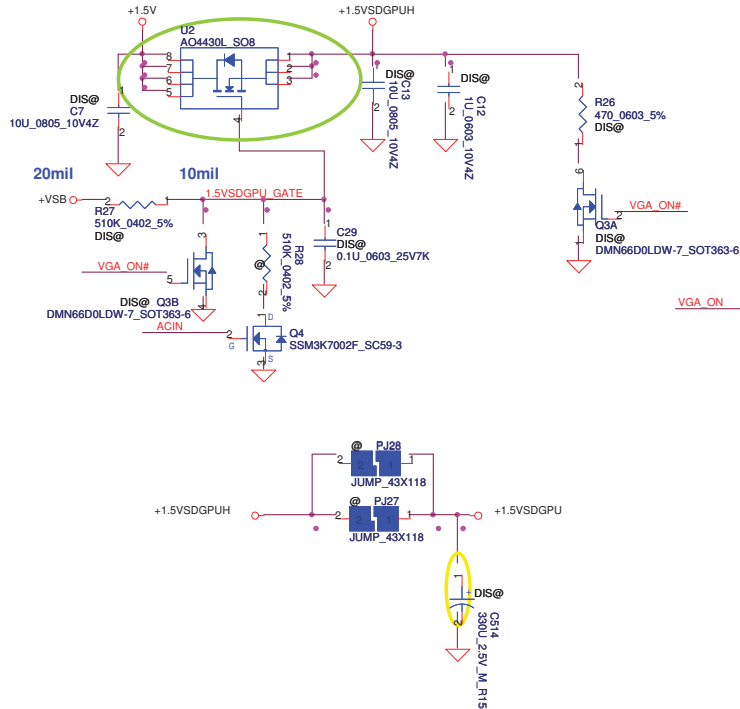
+1.05VS_VTT to +1.05VSDGPU for GPU



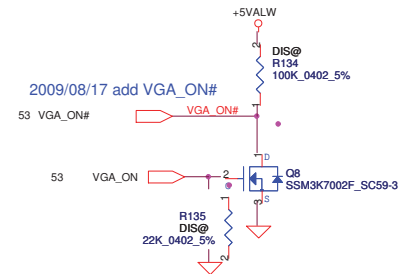
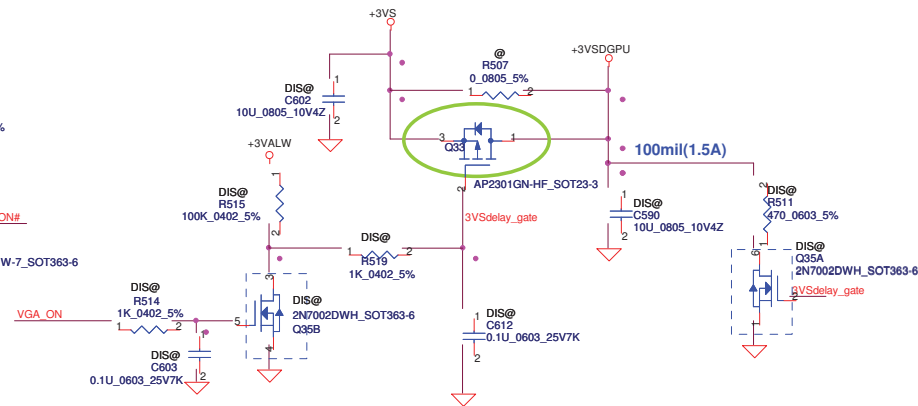
+1.8VS to +1.8VSDGPU for GPU



+1.5V to +1.5VSDGPUH for GPU

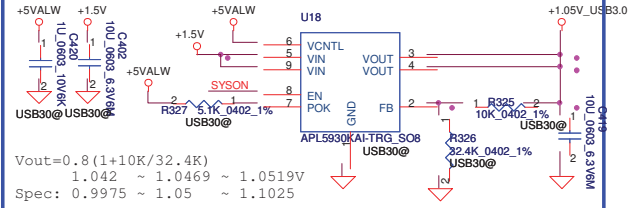


+3VS to +3VSDGPU for GPU

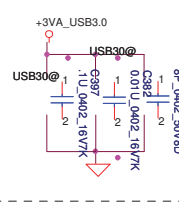


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					Size	Document Number	Rev
					Customer	P5WE0 M/B LA-6901P Schematic	0.1
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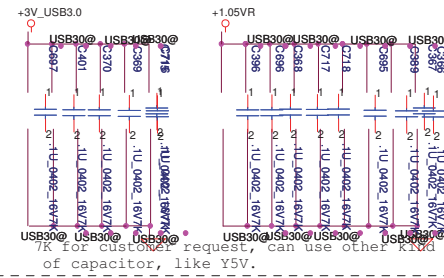
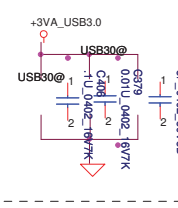
+1.5V to +1.05V Transfer



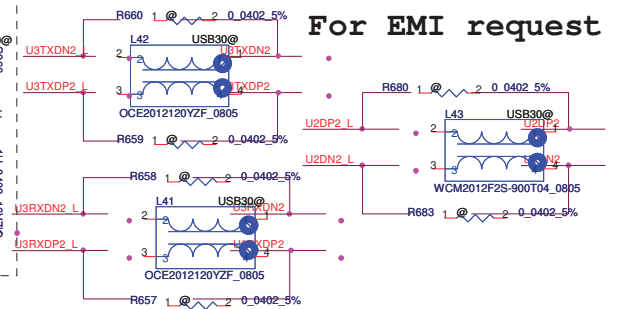
Close to U3.D7



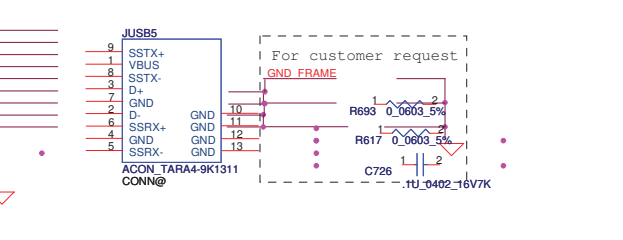
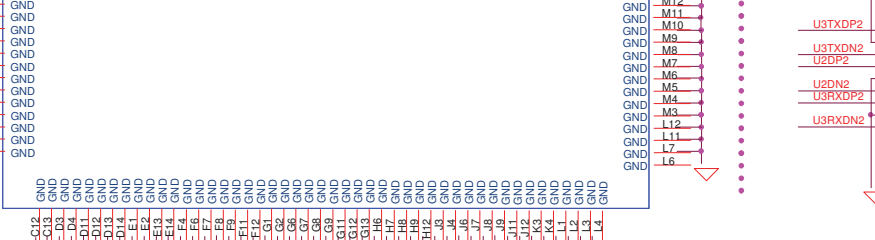
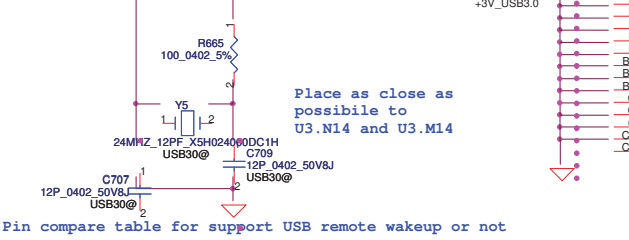
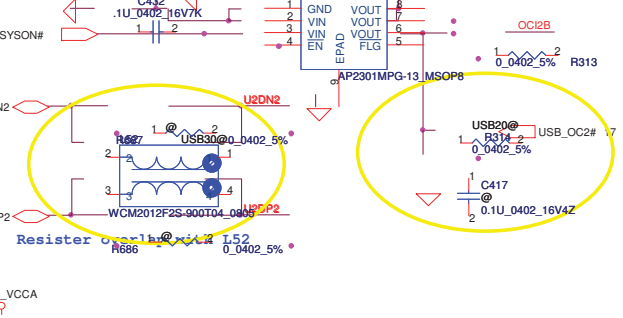
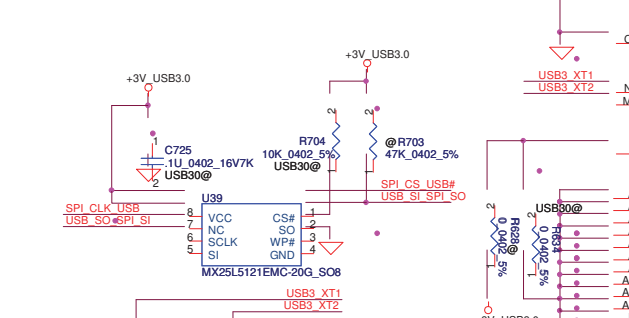
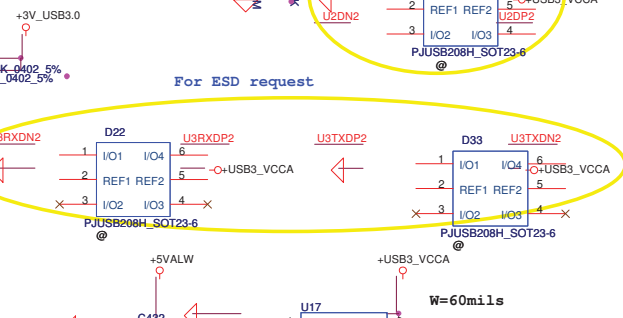
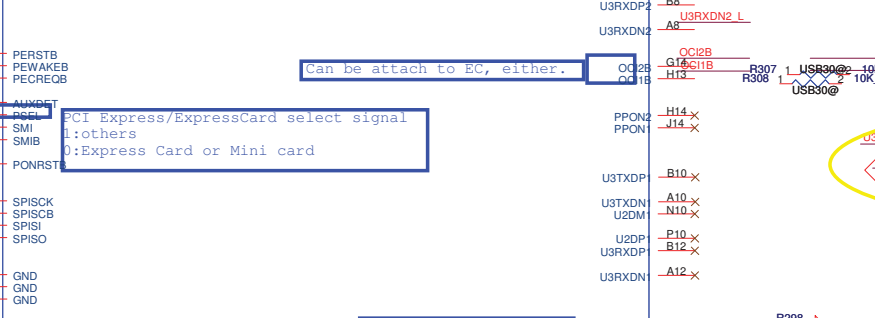
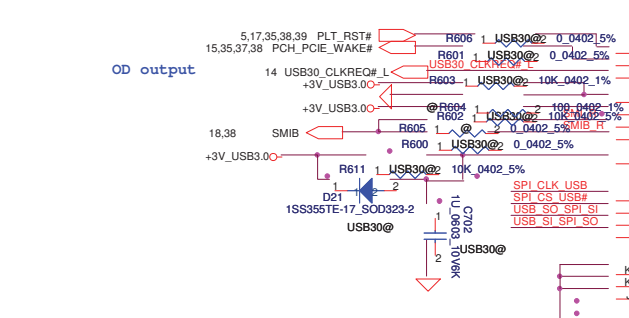
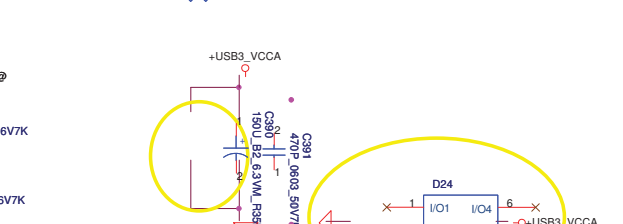
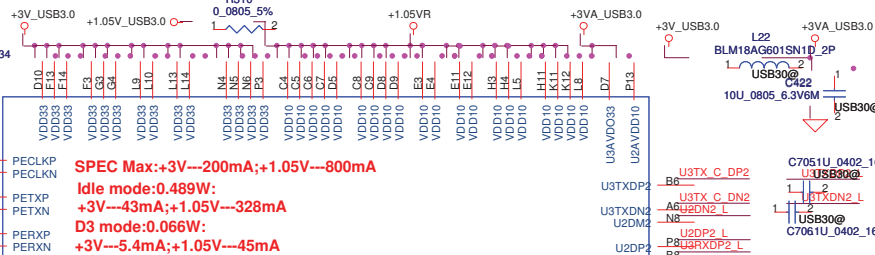
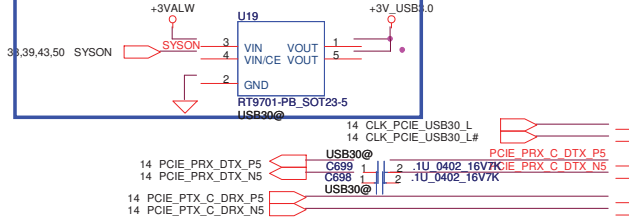
Close to U3.P13



For EMI request



+3VALW to +3V Transfer

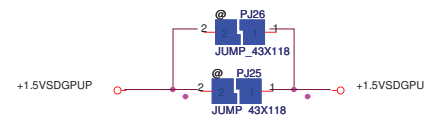
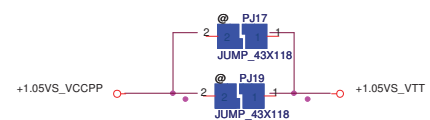
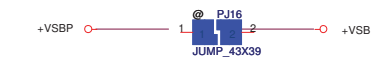
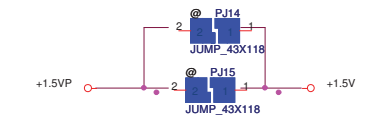
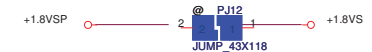
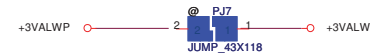
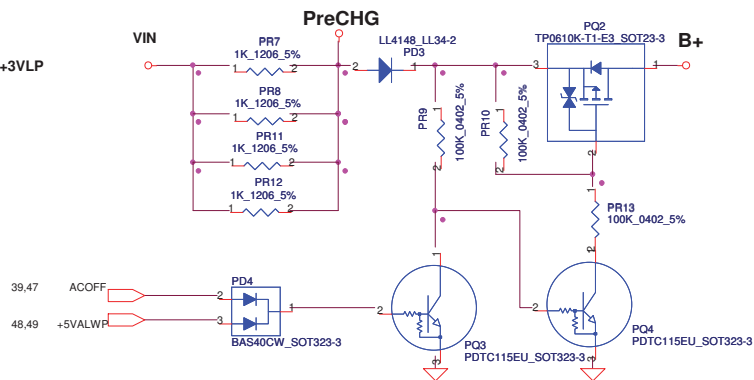
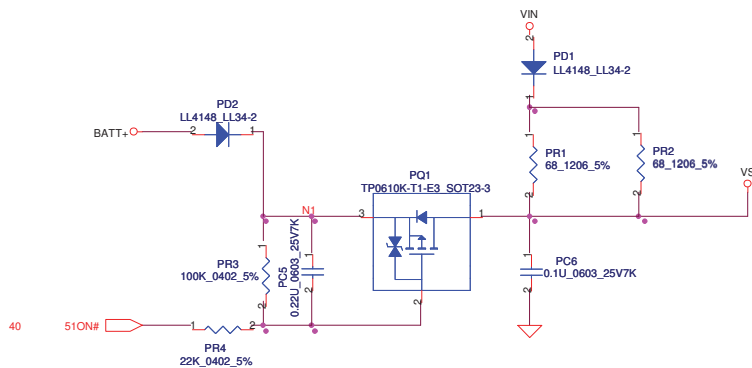
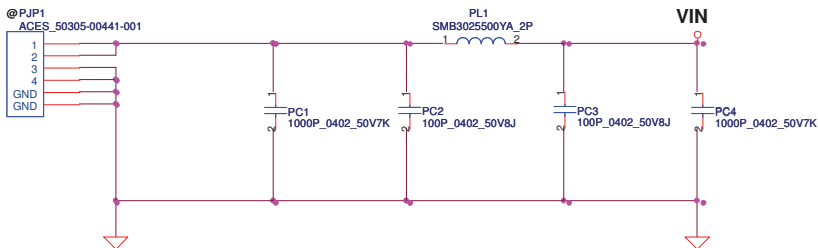


Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
No support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

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Title		USB3.0 PD720200	
Size	Document Number	Rev	0.1
Date	Friday, August 27, 2010	Sheet	45 of 59

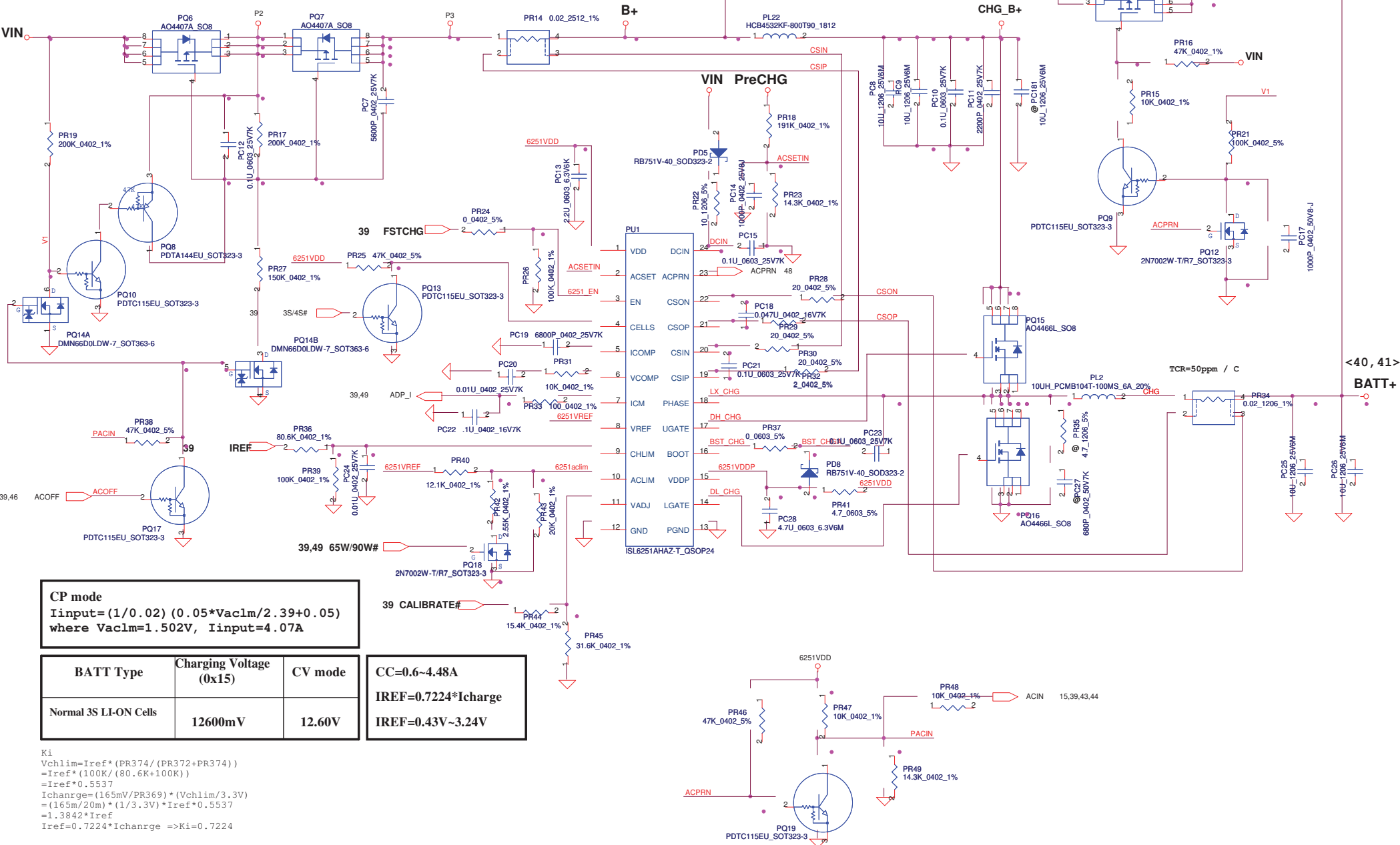


Iada=0~4.74A (90W/19V=4.736A)

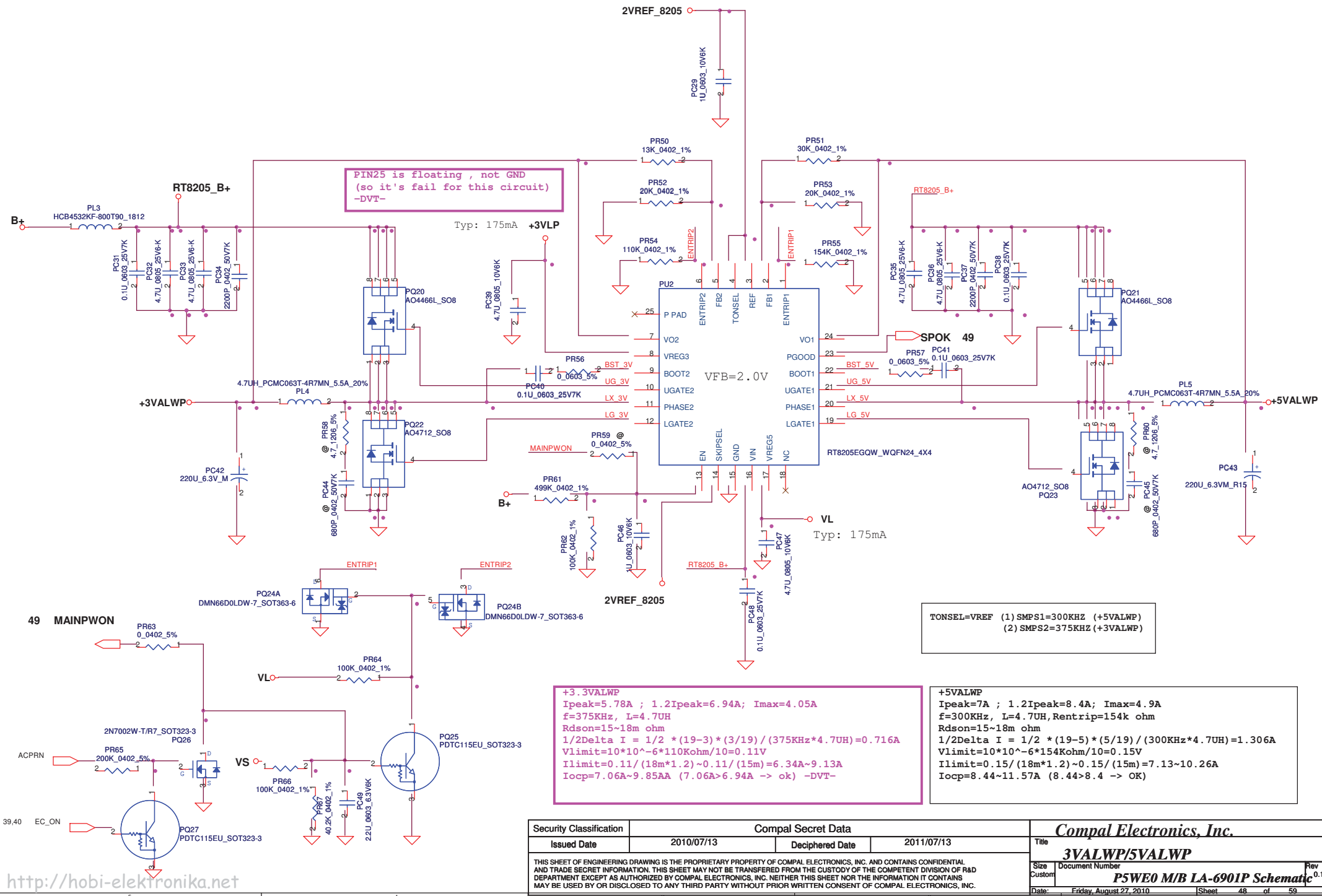
ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A

PC181 reserve for EMI Isen solution



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				Rev	0.1



PIN25 is floating , not GND
(so it's fail for this circuit)
-DVT-

Typ: 175mA +3VLP

VFB=2.0V

Typ: 175mA

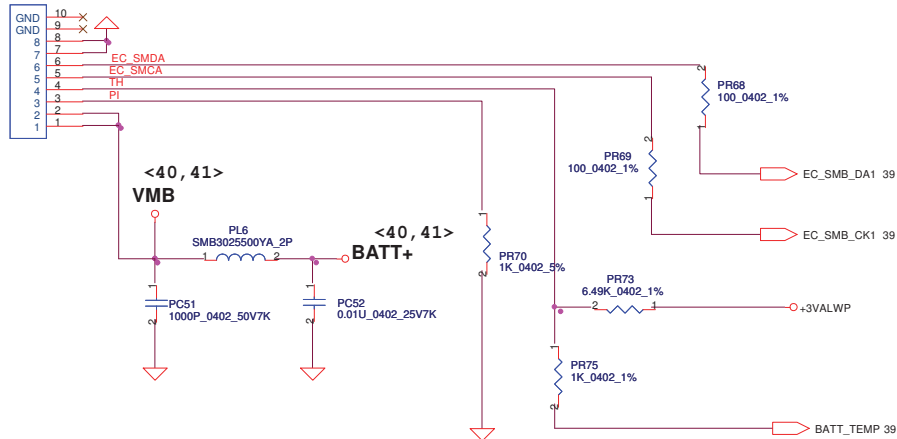
TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)

+3.3VALWP
Ipeak=5.78A ; 1.2Ipeak=6.94A; Imax=4.05A
f=375KHz, L=4.7UH
Rdson=15~18m ohm
1/2Delta I = 1/2 * (19-3) * (3/19) / (375KHz*4.7UH) = 0.716A
Vlimit=10*10^-6*110Kohm/10=0.11V
Ilimit=0.11/(18m*1.2)~0.11/(15m)=6.34~9.13A
Iocp=7.06A~9.85AA (7.06A>6.94A -> ok) -DVT-

+5VALWP
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A
f=300KHz, L=4.7UH, Rentrip=154k ohm
Rdson=15~18m ohm
1/2Delta I = 1/2 * (19-5) * (5/19) / (300KHz*4.7UH) = 1.306A
Vlimit=10*10^-6*154Kohm/10=0.15V
Ilimit=0.15/(18m*1.2)~0.15/(15m)=7.13~10.26A
Iocp=8.44~11.57A (8.44>8.4 -> OK)

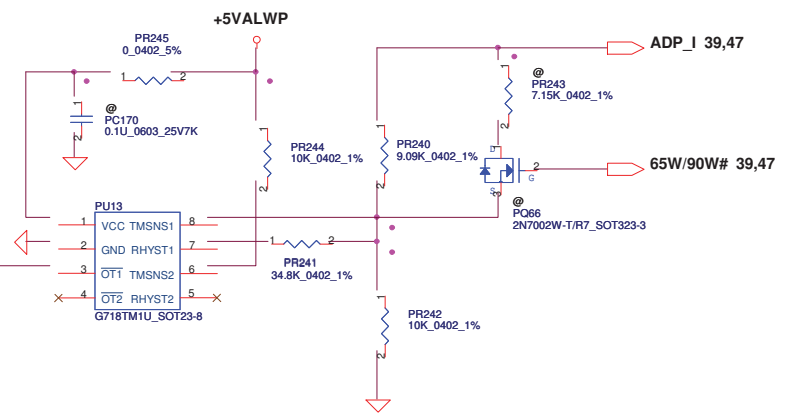
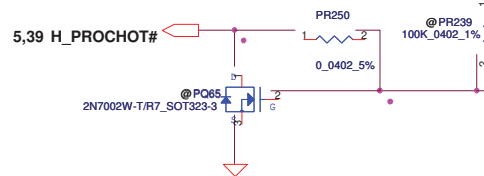
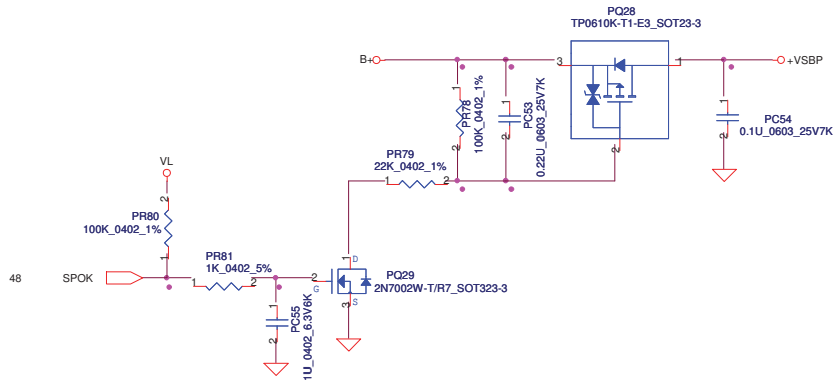
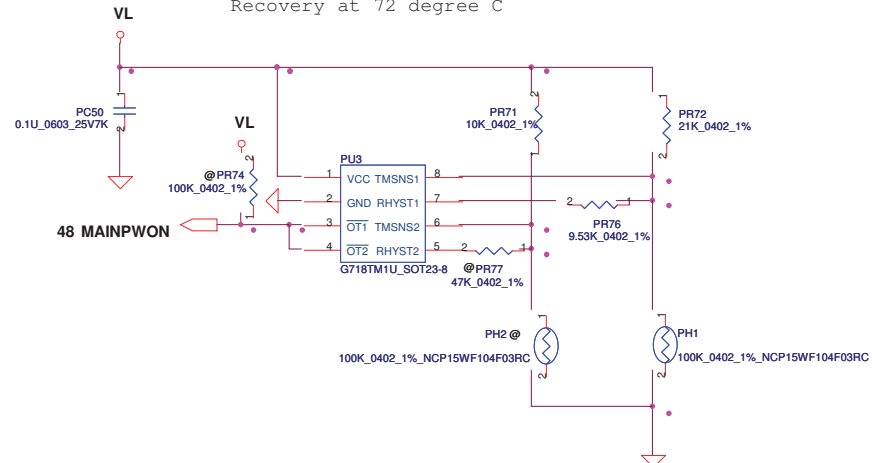
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/07/13	Deciphered Date	2011/07/13	Title	3VALWP/5VALWP	
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				Custom	P5WE0 M/B LA-6901P Schematic	0.1
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PJP2
SUYIN_200275GR008G13GZR

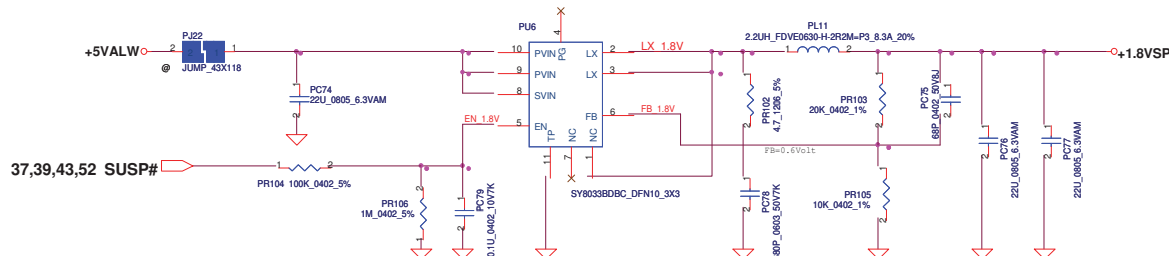


PH1 under CPU botten side :

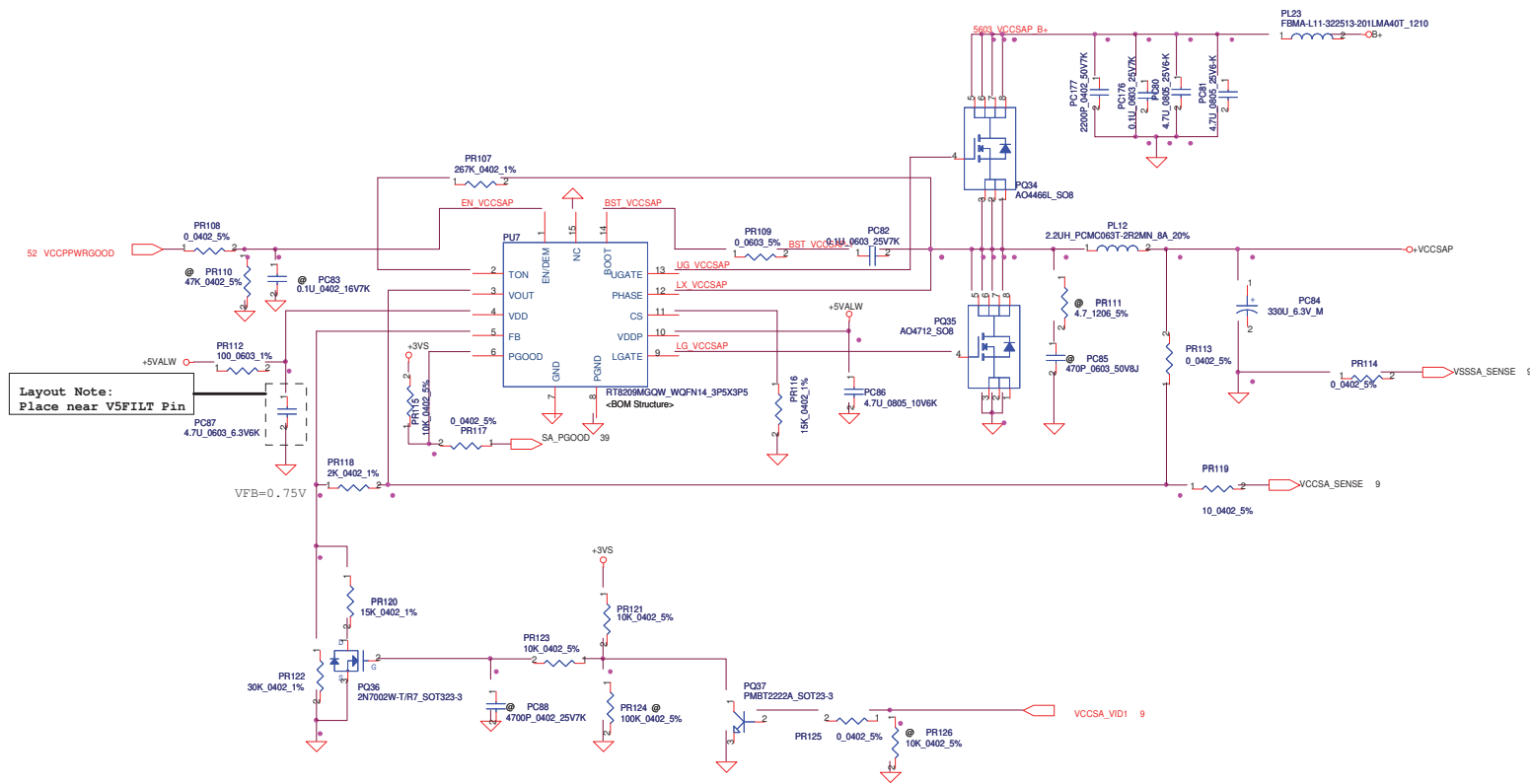
CPU thermal protection at 92 degree C
Recovery at 72 degree C



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				Size	Document Number	Rev
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1.8VSP
 $I_{peak}=3.35A$; $1.2I_{peak}=4.02$; $I_{max}=2.345A$
 $V_{out}=0.6 \cdot (1 + (20K/10K)) = 1.8V$
 -DVT-



Layout Note:
 Place near V5FILT Pin

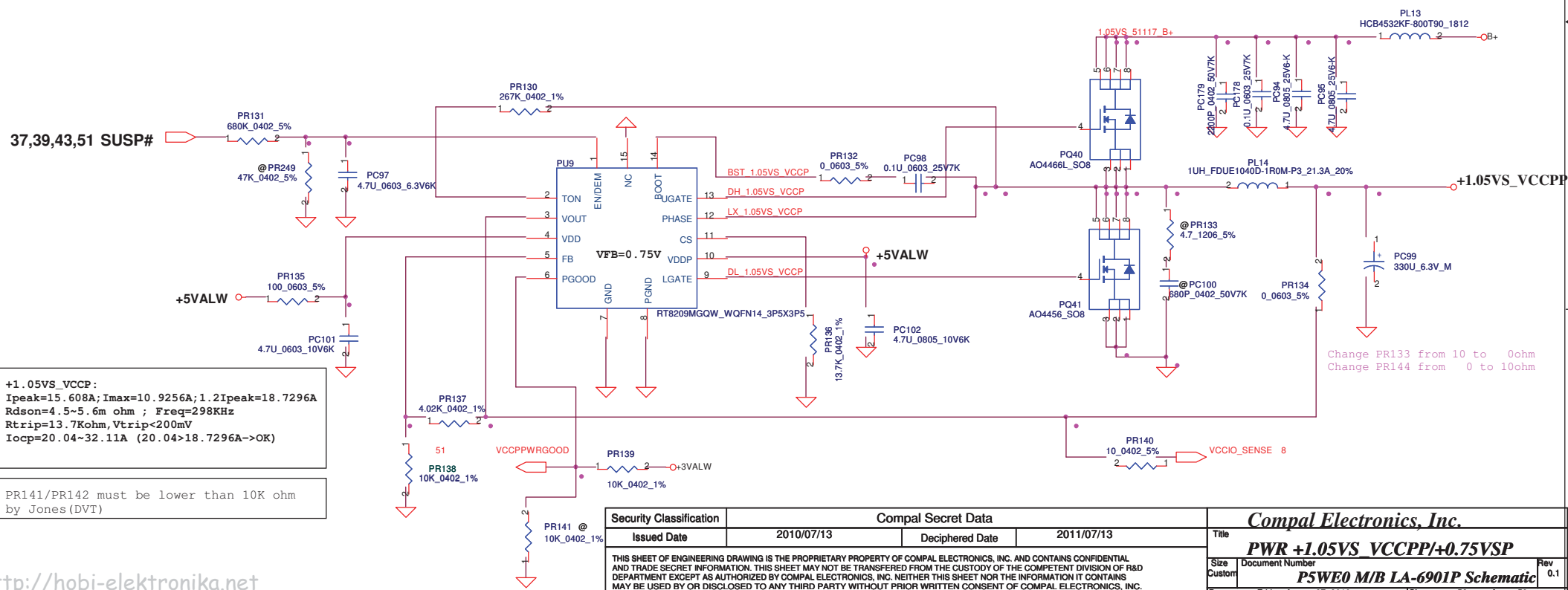
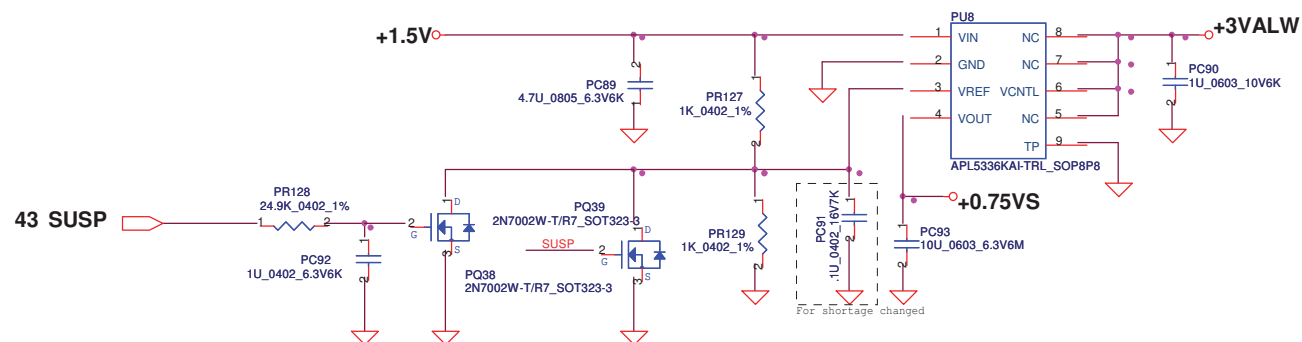
$V_{FB}=0.75V$
 $V_o = V_{FB} \cdot (1 + PR156/PR150) = 1.1V$
 $T_{on} = 19E-12 \cdot Ron \cdot ((2/3) \cdot V_o + 150mV) / V_{in} + 50ns = 2.4E-7$
 $Freq = 282KHz$
 $C_{esr} = 15m \text{ ohm}$
 $I_{peak} = 4.60A$ $I_{max} = 2.70A$
 $\Delta I = ((19.5 - 1.0) \cdot (1.0/19.5)) / (L \cdot Freq) = 1.48A$
 $V_{trip} = R_{trip} \cdot I_{peak} = 0.0787V$
 $I_{ocp_min} = 5.96A$
 $I_{ocp_max} = 6.01A$
 $I_{ocp} = 5.96 - 6.01A$

VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012	Required
0	0	0.9 V	Yes/Yes	
0	1	0.8 V	Yes/Yes	
1	1	0.75V	No/Yes	
1	1	0.65V	No/Yes	

Note: Use VCCSA_SEL to switch High & Low Level for VID[1]
 (ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

+VCCSAP
 $I_{peak}=6A$, $I_{max}=4.2A$, $1.2I_{peak}=7.2A$
 $DCR = 9 \text{ m} (typ) \sim 10 \text{ m} (max)$
 $R_{limit}=12K$, $R_{dson}=15-18mohm$
 $I_{limit}=10uA$
 $I_{ocp}=R_{limit}/R_{dson} \cdot 10^{-5} = 7.59 - 10.654A$

the resistor change
 from @ to pop component
 Add two jumpers on the HW's output cap of the
 +VCCSA's P1W(+) and P1N(-) to sense the
 feedback voltage for VCCSA_SENSE & VSSA_SENSE.



+1.05VS_VCCPP:
 $I_{peak}=15.608A$; $I_{max}=10.9256A$; $1.2I_{peak}=18.7296A$
 $R_{dson}=4.5\sim 5.6m\ ohm$; $Freq=298KHz$
 $R_{trip}=13.7Kohm$, $V_{trip}<200mV$
 $I_{ocp}=20.04\sim 32.11A$ ($20.04>18.7296A\rightarrow OK$)

PR141/PR142 must be lower than 10K ohm
 by Jones (DVT)

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Item	Fixed Issue	Reason for change	Rev	PG#	Modify List	Date	Phase
1	Shut down for PWM3 pin floating	IF the PWM3 no used, please pull high it for +5VS and not floating	0.1	P.55	(1)Add PR638(0_0603_5%) between PWM3 and +5VS (2)connect the ISNG to +5VS	2010-03-29	DVT
2	OVP problem with PWR and HW side	If the HW side is 0V, through the jumper will cause the sense pin to over the votage setting and it may happen OVP problem.	0.1	P.55	Change the +VGFX_CORE to +VGFX_COREP	2010-03-29	DVT
3							

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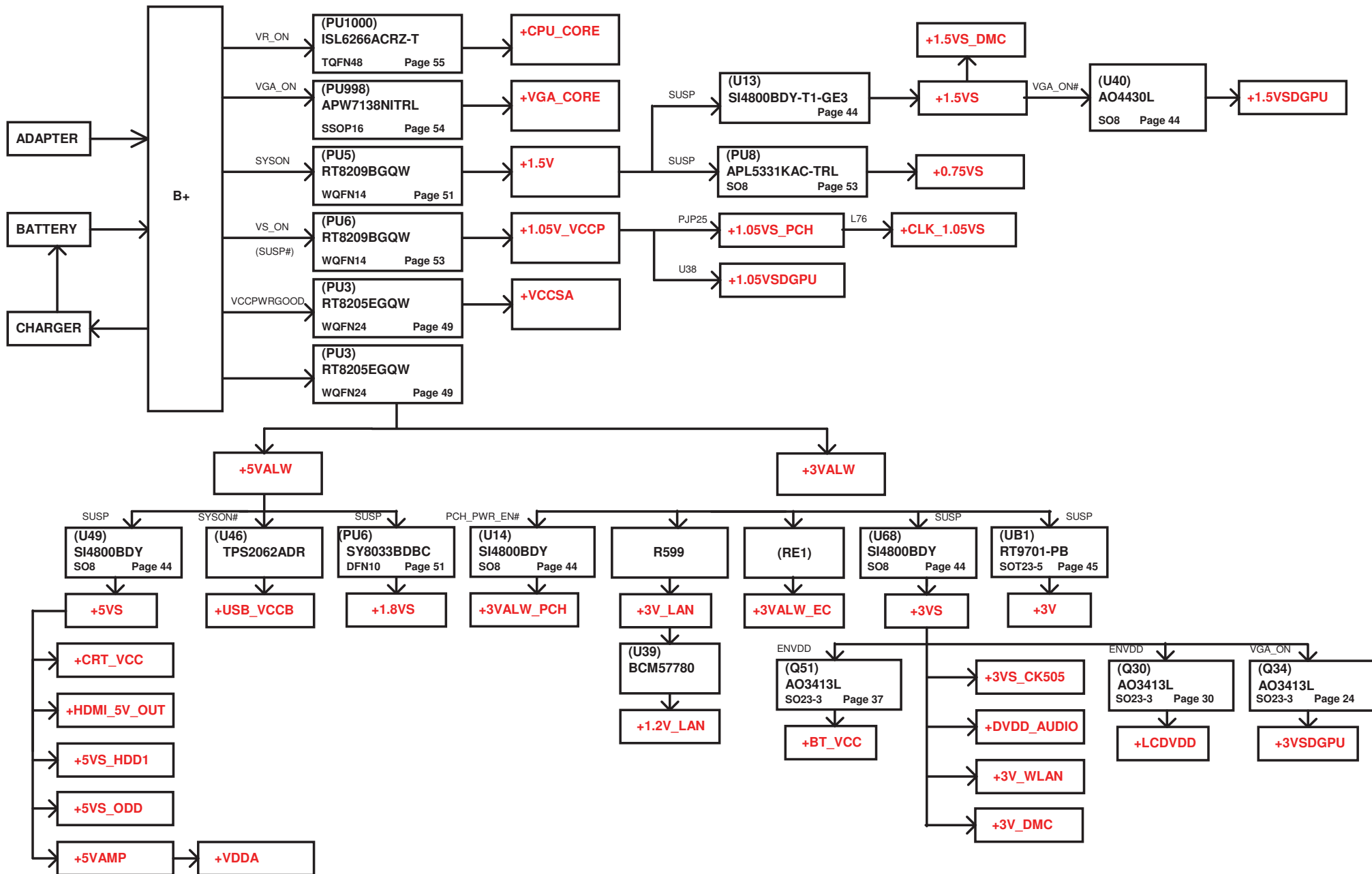
Title <Title> PIR POWER1

Size A

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Rev 0.1

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				Custom	0.1
				Document Number P5WE0 M/B LA-6901P Schematic	
Date:	Friday, August 27, 2010	Sheet	59	of	59