Compal Confidential

KAWE0 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

2008-07-28

REV:1.0

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Title	SCHEMATICS, MB A4431		
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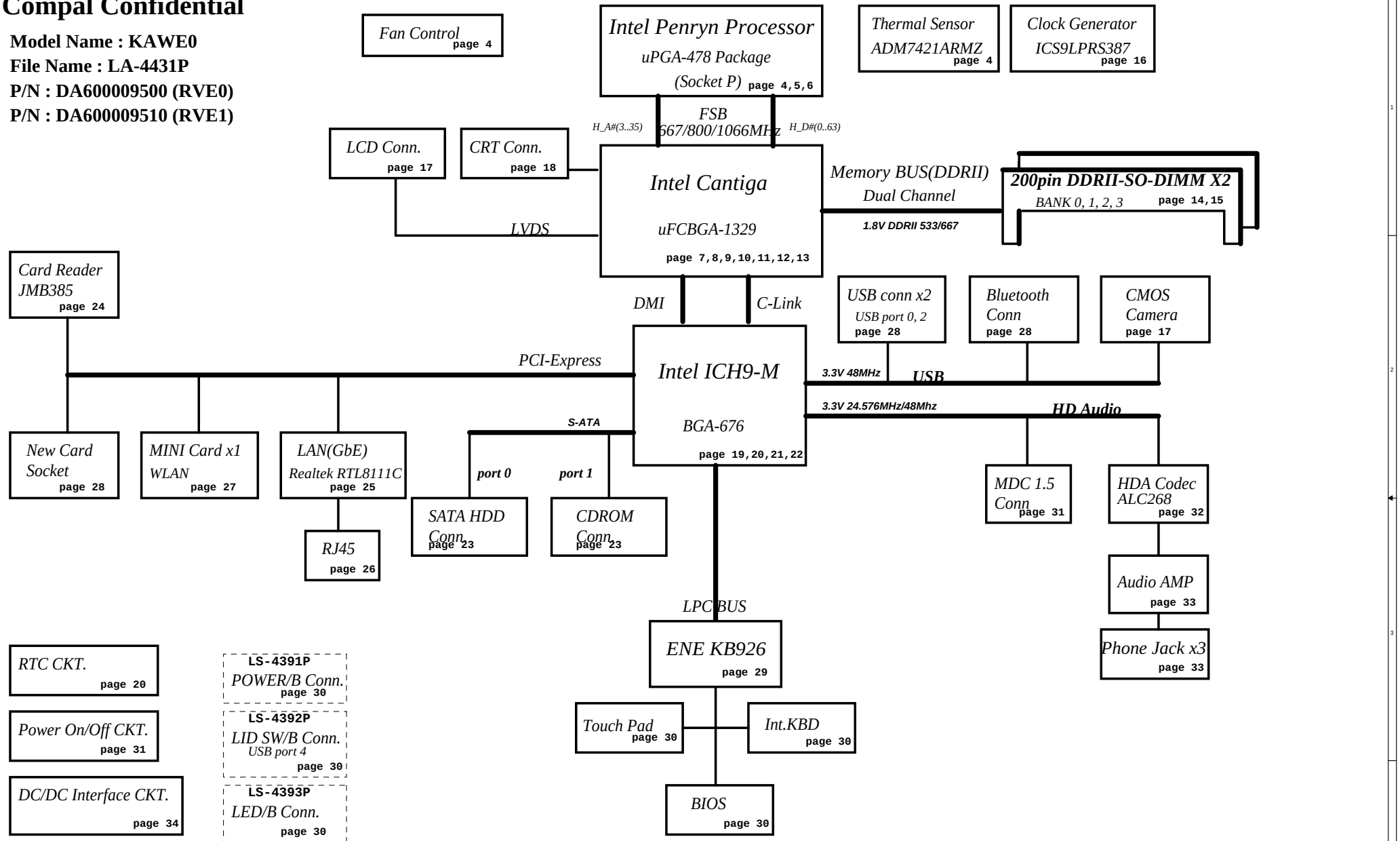
Model Name : KAWE0
File Name : LA-4431P
P/N : DA600009500 (RVE0)
P/N : DA600009510 (RVE1)



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
ADI ADT7421	1001 100X b

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
8111C	8111C@
8102E	8102E@

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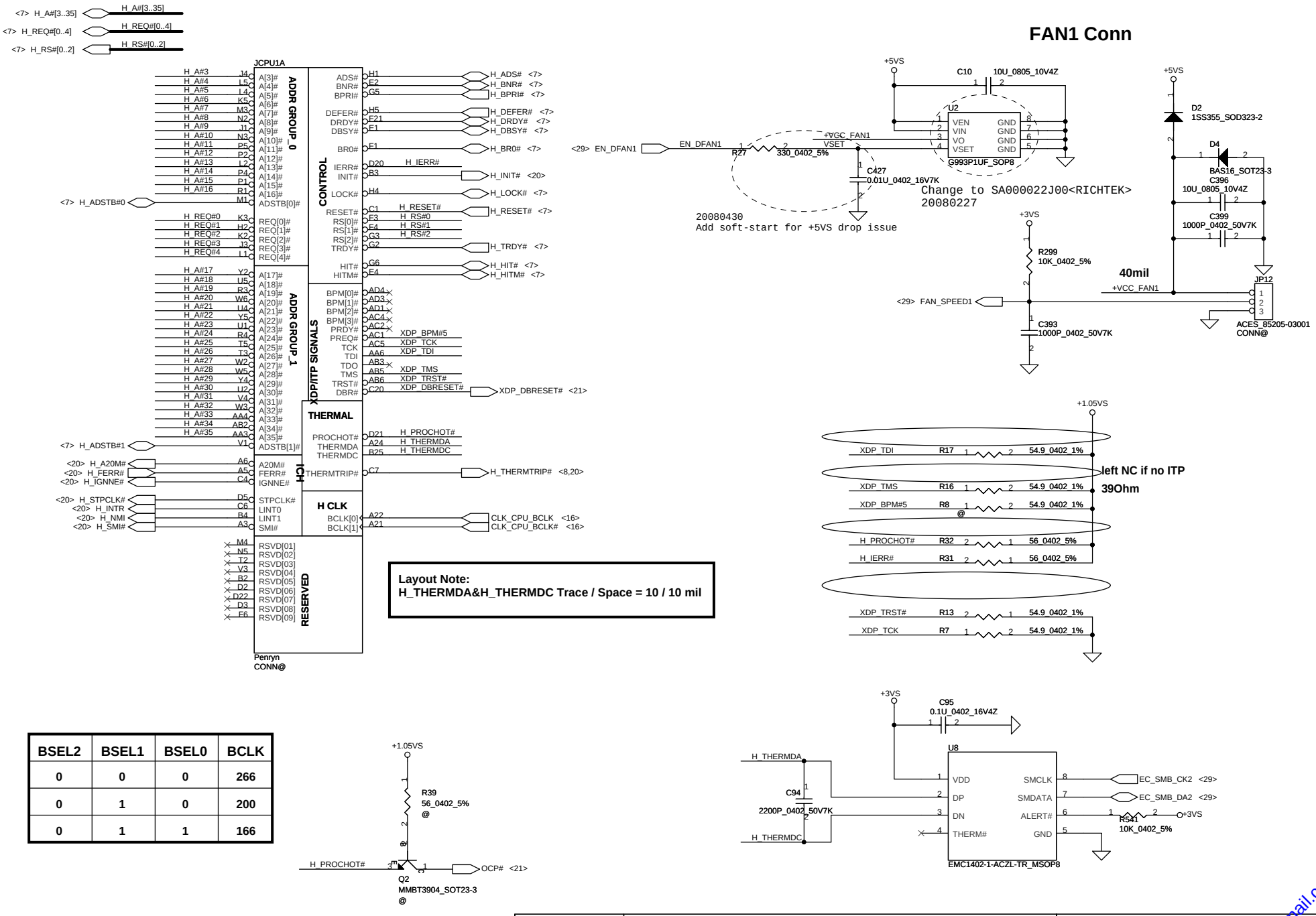

BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

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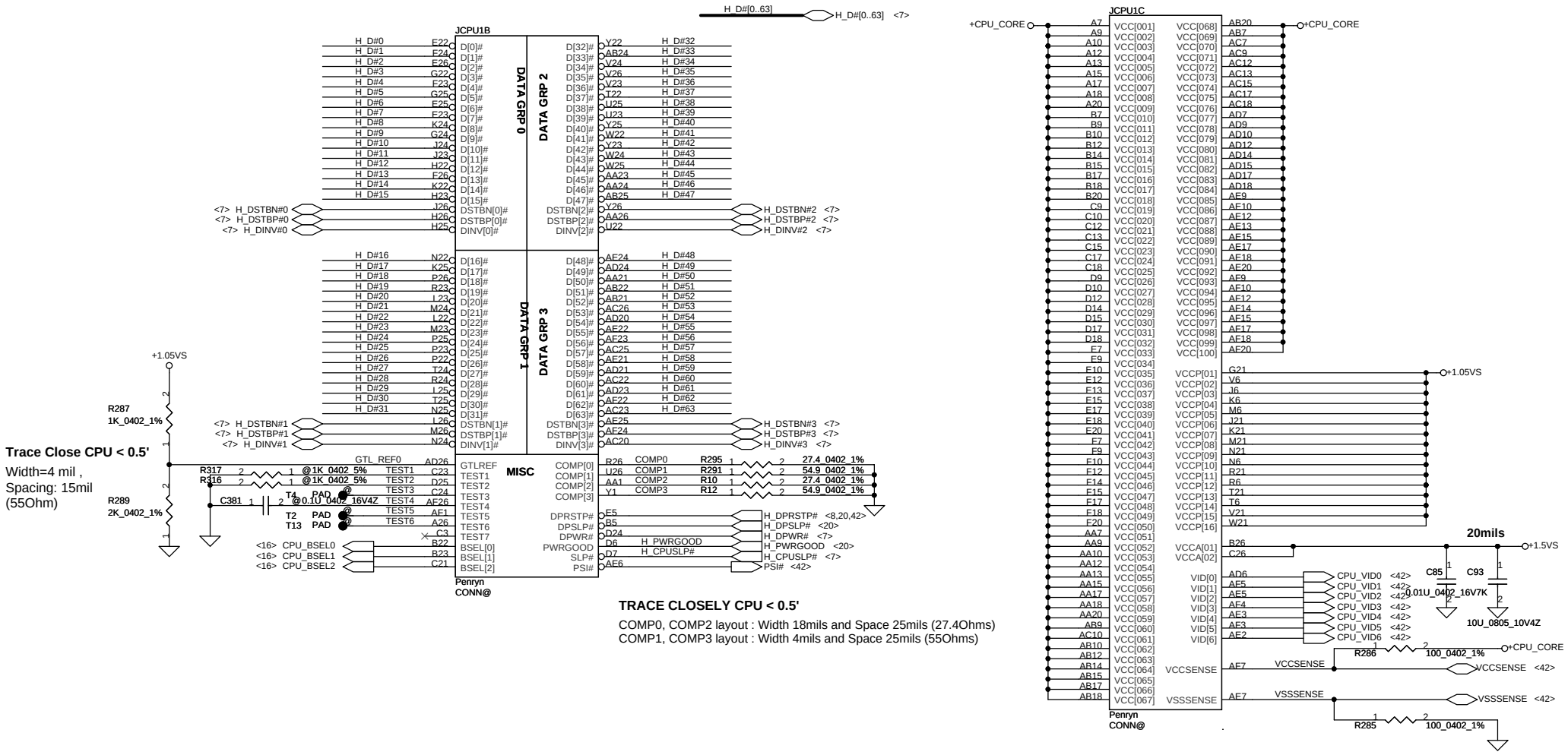

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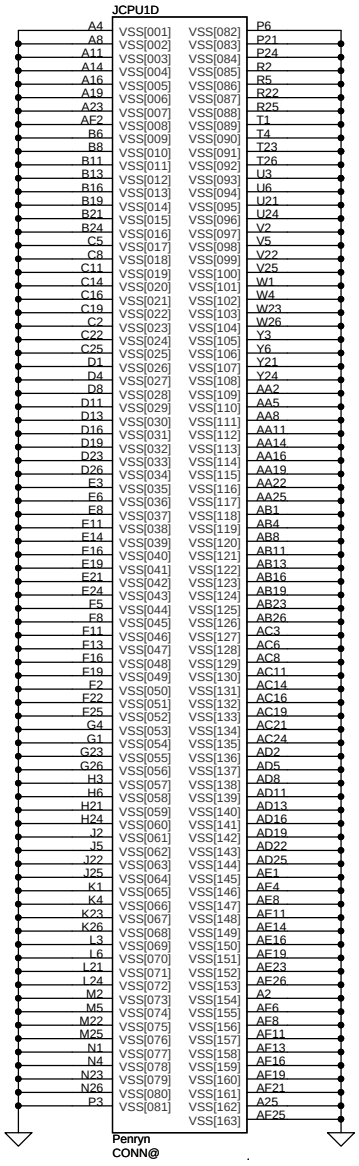
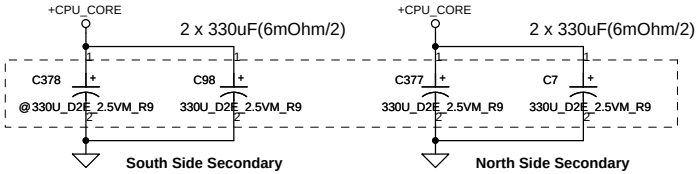
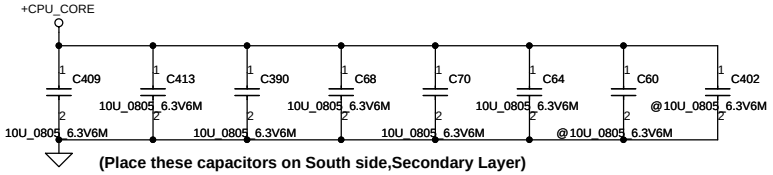
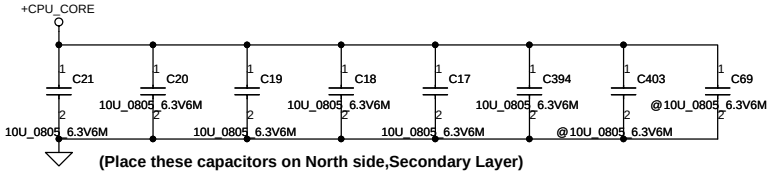
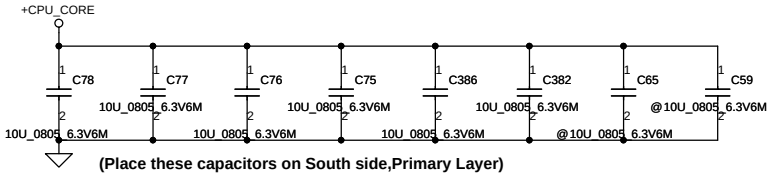
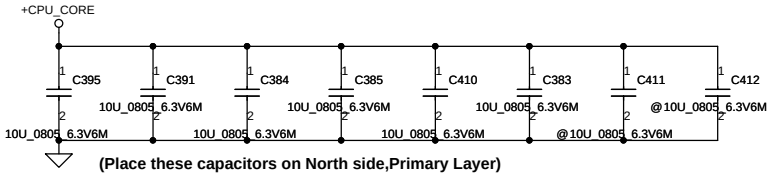




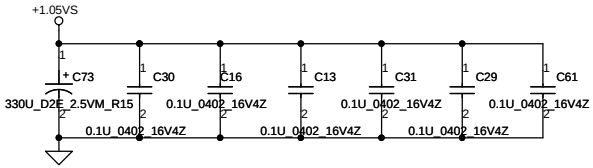








+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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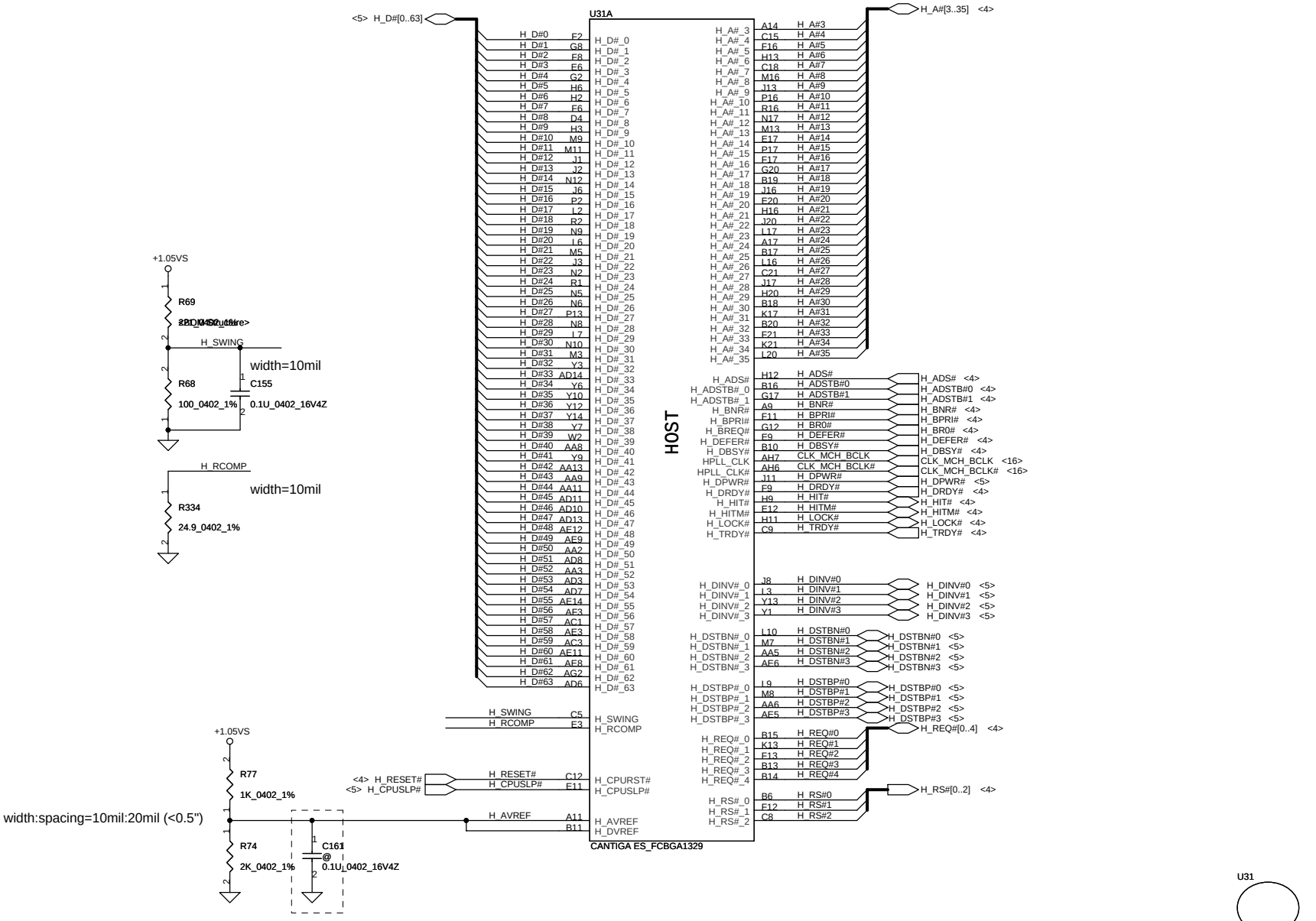

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U31B

All RSVD balls on GMCH should be left No Connect.

RSVD: M36 RSVD1, N36 RSVD2, R33 RSVD3, T33 RSVD4, AH9 RSVD5, AH10 RSVD6, AH12 RSVD7, AH13 RSVD8, K12 RSVD9, AL34 RSVD10, AK34 RSVD11, AN35 RSVD12, AM35 RSVD13, T24 RSVD14, B31 RSVD15, B2 RSVD16, M1 RSVD17, AY21 RSVD20, BG23 RSVD22, BF23 RSVD23, BH18 RSVD24, BF18 RSVD25

DDR CLK/ CONTROL/ COMPENSATION:
SA_CK_0 AP24 DDRA_CLK0 <14>; SA_CK_1 AT21 DDRA_CLK1 <14>; SB_CK_0 AV24 DDRB_CLK0 <15>; SB_CK_1 AU20 DDRB_CLK1 <15>
SA_CK#_0 AR24 DDRA_CLK0# <14>; SA_CK#_1 AR21 DDRA_CLK1# <14>; SB_CK#_0 AU24 DDRB_CLK0# <15>; SB_CK#_1 AV20 DDRB_CLK1# <15>
SA_CKE_0 BC28 DDRA_CKE0 <14>; SA_CKE_1 AY28 DDRA_CKE1 <14>; SB_CKE_0 AY36 DDRB_CKE0 <15>; SB_CKE_1 BB36 DDRB_CKE1 <15>
SA_CS#_0 BA17 DDRA_SCS0# <14>; SA_CS#_1 AY16 DDRA_SCS1# <14>; SB_CS#_0 AV16 DDRB_SCS0# <15>; SB_CS#_1 AR13 DDRB_SCS1# <15>
SA_ODT_0 BD17 DDRA_ODT0 <14>; SA_ODT_1 AY17 DDRA_ODT1 <14>; SB_ODT_O BE15 DDRB_ODT0 <15>; SB_ODT_1 AY13 DDRB_ODT1 <15>
SM_RCOMP BG22 SMRCOMP; SM_RCOMP# BH21 SMRCOMP#
SM_RCOMP_VOH BF28 SM_RCOMP_VOH; SM_RCOMP_VOL BH28 SM_RCOMP_VOL
SM_VREF AV42; SM_PWROK AR36; SM_REXT BF17; SM_DRAMRST# BC36

SM_DRAMRST# would be needed for DDR3 only

For Cantiga 80 Ohm

R386 80.6_0402_1%; R383 80.6_0402_1%

+1.8V
R392 1K_0402_1%
SM_RCOMP_VOH
C491 2.2U_0603_6.3V6K; C492 0.01U_0402_16V7K
R390 3.01K_0402_1%
SM_RCOMP_VOL
R389 1K_0402_1%; C483 2.2U_0603_6.3V6K; C482 0.01U_0402_16V7K

R146 1K_0402_1% @
SM_VREF
20mil
R125 0_0402_5%; R375 499_0402_1%
C212 0.1U_0402_16V4Z
R147 0_0402_5%
R145 1K_0402_1% @
+DIMM_VREF

CLK DDR CLK/ CONTROL/ COMPENSATION:
DPLL_REF_CLK B38 CLK_DREF_96M; DPLL_REF_CLK# A38 CLK_DREF_96M#; DPLL_REF_SSCLK E41 CLK_DREF_SSC; DPLL_REF_SSCLK# F41 CLK_DREF_SSC#
PEG_CLK F43 CLK_MCH_3GPLL; PEG_CLK# E43 CLK_MCH_3GPLL#

DMI:
DMI_RXN_0 AE41 DMI_ITX_MRX_N0; DMI_RXN_1 AE37 DMI_ITX_MRX_N1; DMI_RXN_2 AE47 DMI_ITX_MRX_N2; DMI_RXN_3 AH39 DMI_ITX_MRX_N3
DMI_RXP_0 AE40 DMI_ITX_MRX_P0; DMI_RXP_1 AE38 DMI_ITX_MRX_P1; DMI_RXP_2 AE48 DMI_ITX_MRX_P2; DMI_RXP_3 AH40 DMI_ITX_MRX_P3
DMI_TXN_0 AE35 DMI_MTX_IRX_N0; DMI_TXN_1 AE43 DMI_MTX_IRX_N1; DMI_TXN_2 AE46 DMI_MTX_IRX_N2; DMI_TXN_3 AH42 DMI_MTX_IRX_N3
DMI_TXP_0 AD35 DMI_MTX_IRX_P0; DMI_TXP_1 AE44 DMI_MTX_IRX_P1; DMI_TXP_2 AE46 DMI_MTX_IRX_P2; DMI_TXP_3 AH43 DMI_MTX_IRX_P3

GRAPHICS VID:
GFX_VID_0 B33; GFX_VID_1 B32; GFX_VID_2 G33; GFX_VID_3 F33; GFX_VID_4 E33
GFX_VR_EN C34

ME:
CL_CLK AH37 CL_CLK0 <21>; CL_DATA AH36 CL_DATA0 <21>; CL_PWROK AN36 ICH_PWROK; CL_RST# AJ35 CL_RST#0 <21>; CL_VREF AH34

MISC:
DDPC_CTRLCLK N28; DDPC_CTRLDATA M28; SDVO_CTRLCLK G36; SDVO_CTRLDATA E36; CLKREQ# K36 MCH_CLKREQ#; ICH_SYNC# H36 MCH_ICH_SYNC# <21>
TSATN# B12 MCH_TSATN#

HDA:
HDA_BCLK B28; HDA_RST# B30; HDA_SDI B29; HDA_SDO C29; HDA_SYNC A28

+1.05VS
R128 1K_0402_1%
C198 0.1U_0402_16V4Z
R129 511_0402_1%

CFG:
<16> MCH_CLKSEL0 MCH_CLKSEL0 T25; <16> MCH_CLKSEL1 MCH_CLKSEL1 R25; <16> MCH_CLKSEL2 MCH_CLKSEL2 P25
+3VS: R118 10K_0402_5% PM_EXTTS#0; R121 10K_0402_5% PM_EXTTS#1; R126 10K_0402_5% MCH_CLKREQ#
MCH_CFG_5 C25; MCH_CFG_6 N24; MCH_CFG_7 M24; MCH_CFG_9 C23; MCH_CFG_10 C24; MCH_CFG_12 P21; MCH_CFG_13 T21; MCH_CFG_16 L21; MCH_CFG_19 R28; MCH_CFG_20 T28
CFG_0 P20; CFG_1 P24; CFG_2 C25; CFG_3 N24; CFG_4 M24; CFG_5 F21; CFG_6 C23; CFG_7 C24; CFG_8 N21; CFG_9 P21; CFG_10 R20; CFG_11 M20; CFG_12 L21; CFG_13 H21; CFG_14 P29; CFG_15 R28; CFG_16 T28; CFG_17; CFG_18; CFG_19; CFG_20

Use VGATE for GMCH_PWROK
<16,21,42> VGATE — R143 0_0402_5% — GMCH_PWROK
<21> ICH_PWROK — R144 0_0402_5% — MCH_CFG_16

PM:
<21> PM_SYNC# — R82 0_0402_5% — PM_SYNC# B7
<5,20,42> H_DPRSTP# — R73 0_0402_5% — PM_DPRSTP# B7
<14> PM_EXTTS#0 — PM_EXTTS#0 N33
<15> PM_EXTTS#1 — PM_EXTTS#1 P32
GMCH_PWROK AT40
<19,21,24,25,29> PLT_RST# — R75 100_0402_5% — MCH_RSTIN# AT11
<4,20> H_THERMTRIP# — R85 0_0402_5% — THERMTRIP# R T20
<21,42> PM_DPRSLPVR — R80 0_0402_5% — DPRSLPVR R32
PM_SYNC# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR

NC: BG48 NC_1; BF48 NC_2; BD48 NC_3; BC48 NC_4; BH47 NC_5; BG47 NC_6; BF47 NC_7; BH46 NC_8; BF46 NC_9; BG45 NC_10; BH44 NC_11; BH43 NC_12; BH6 NC_13; BH5 NC_14; BG4 NC_15; BH3 NC_16; BF3 NC_17; BH2 NC_18; BG2 NC_19; BF2 NC_20; BG1 NC_21; BF1 NC_22; BD1 NC_23; BC1 NC_24; F1 NC_25; A47 NC_26

CANTIGA ES_FCBGA1329

+1.05VS
R371 54.9_0402_1%
R366 330_0402_5%
MCH_TSATN#
Q18 MMBT3904_SOT23-3
+3VS
R202 1K_0402_5%
R210 1K_0402_5%
Q21 MMBT3904_SOT23-3
MCH_TSATN_EC# <29>

MCH_CFG_5 R110 @2.21K_0402_1%
MCH_CFG_6 R86 @4.02K_0402_1%
MCH_CFG_7 R92 @2.21K_0402_1%
MCH_CFG_9 R103 @2.21K_0402_1%
MCH_CFG_10 R98 @2.21K_0402_1%
MCH_CFG_12 R89 @2.21K_0402_1%
MCH_CFG_13 R90 @2.21K_0402_1%
MCH_CFG_16 R88 @2.21K_0402_1%
MCH_CFG_19 R96 @4.02K_0402_1%
MCH_CFG_20 R95 @4.02K_0402_1%
+3VS

Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable * (Default) 1 = LFP Card Present; PCIE disable
DDPC_CTRLDATA	0 = Digital DisplayPort Disable * (Default) 1 = Digital DisplayPort Device Present

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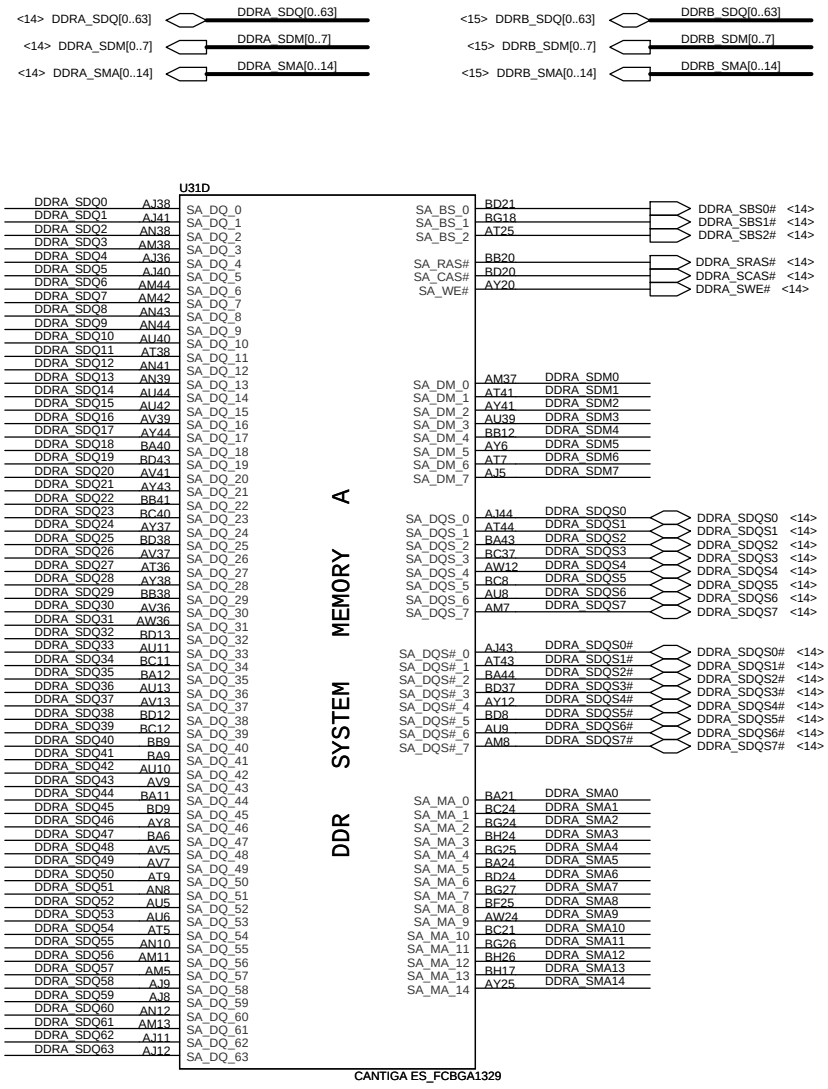

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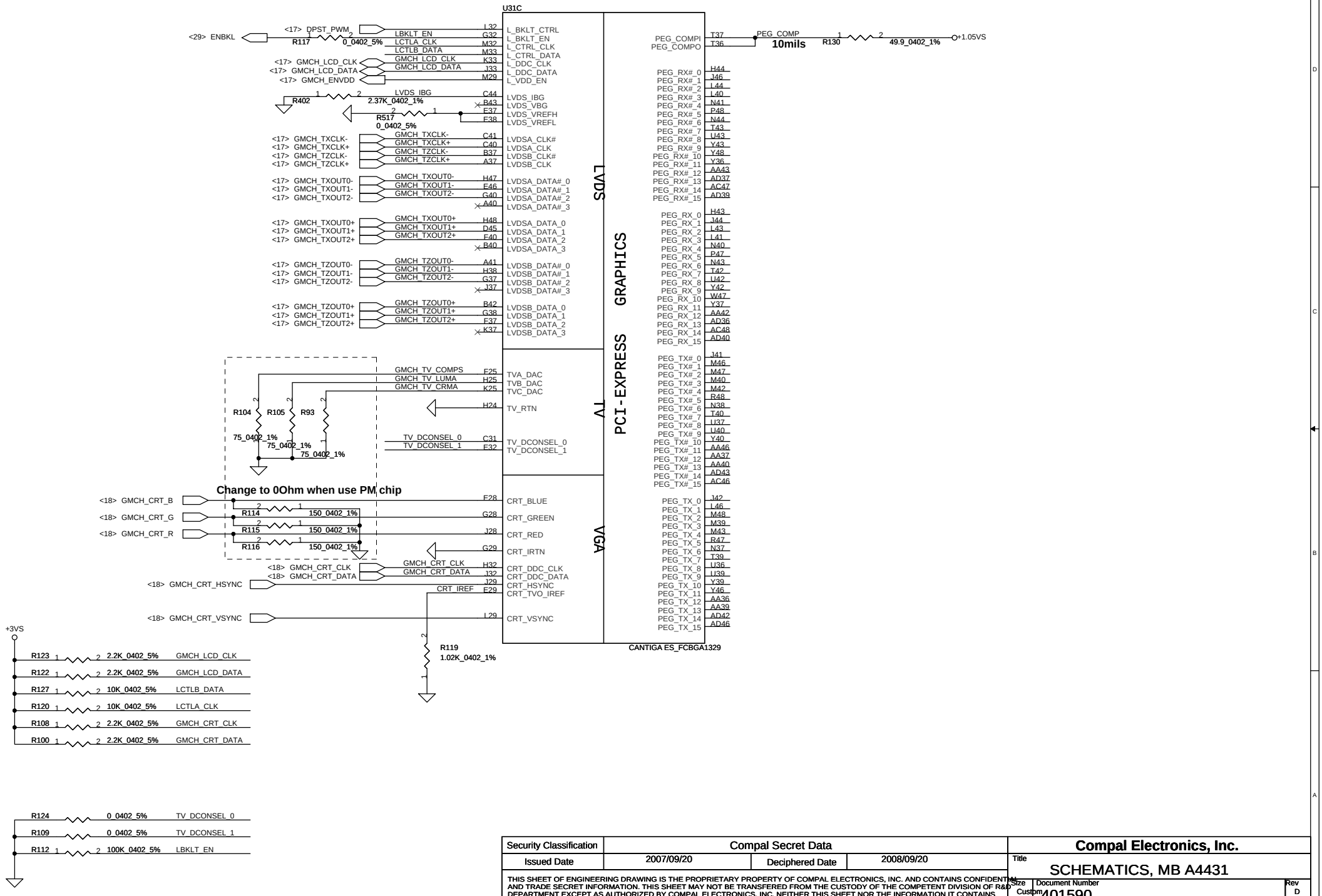

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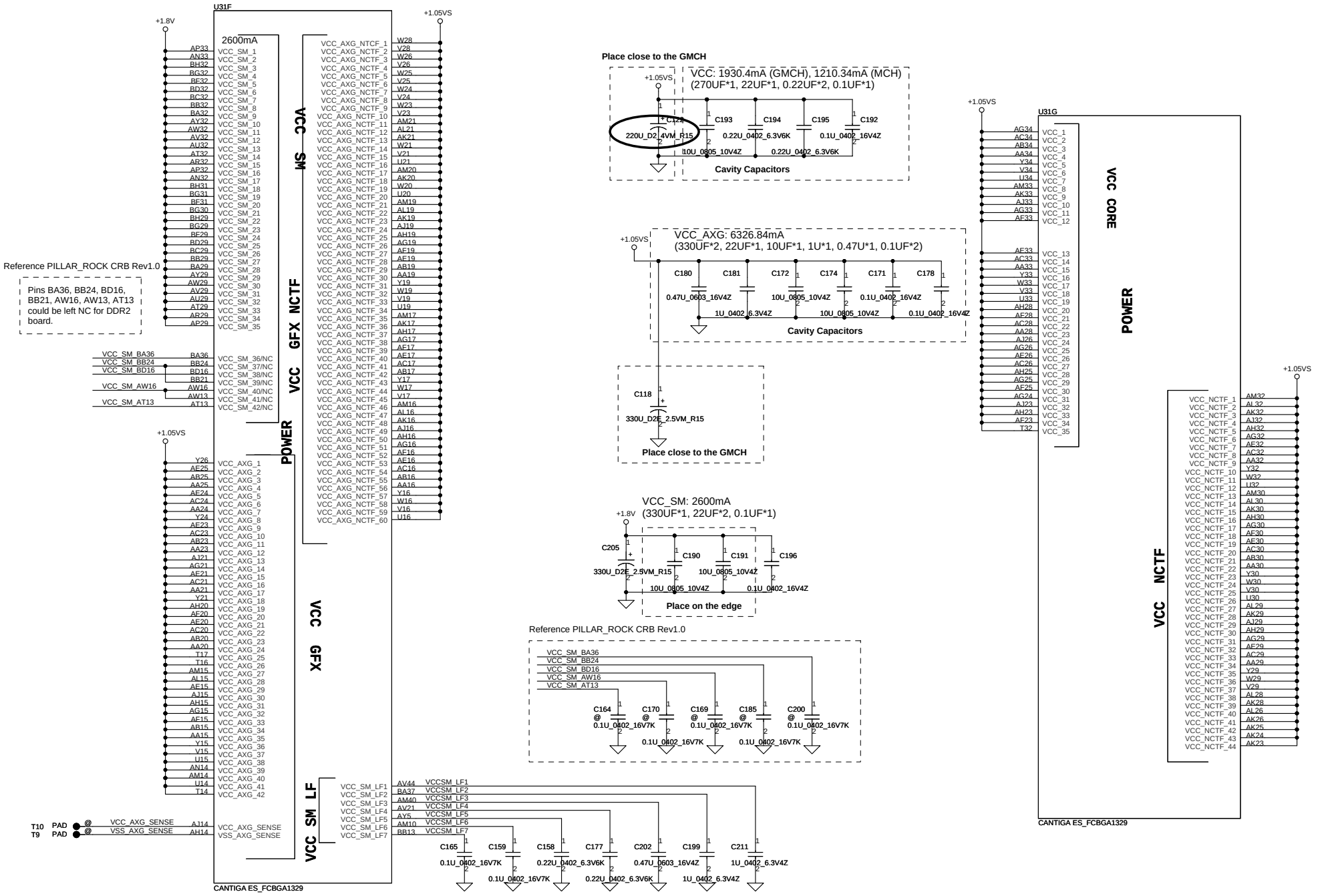

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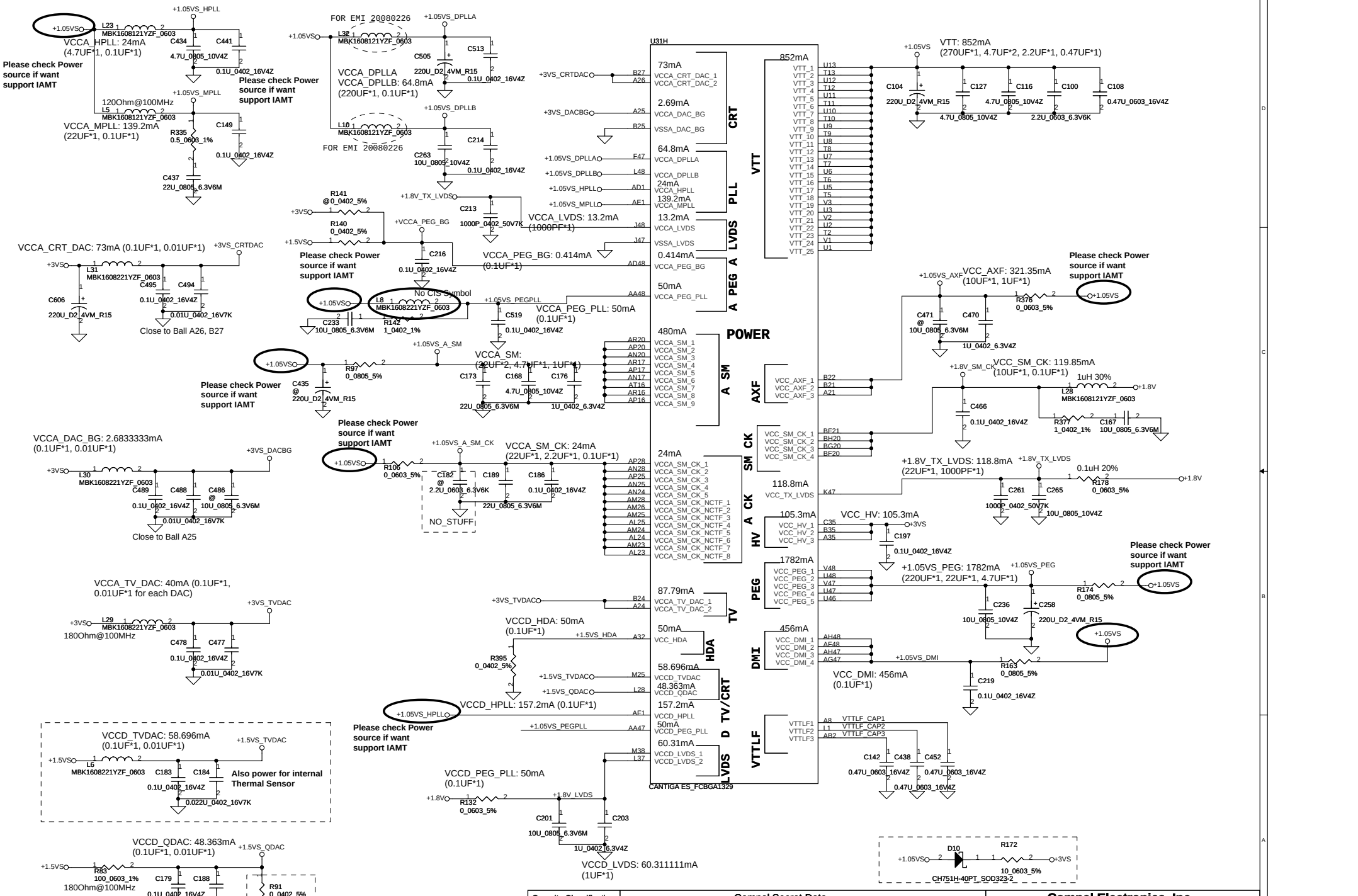

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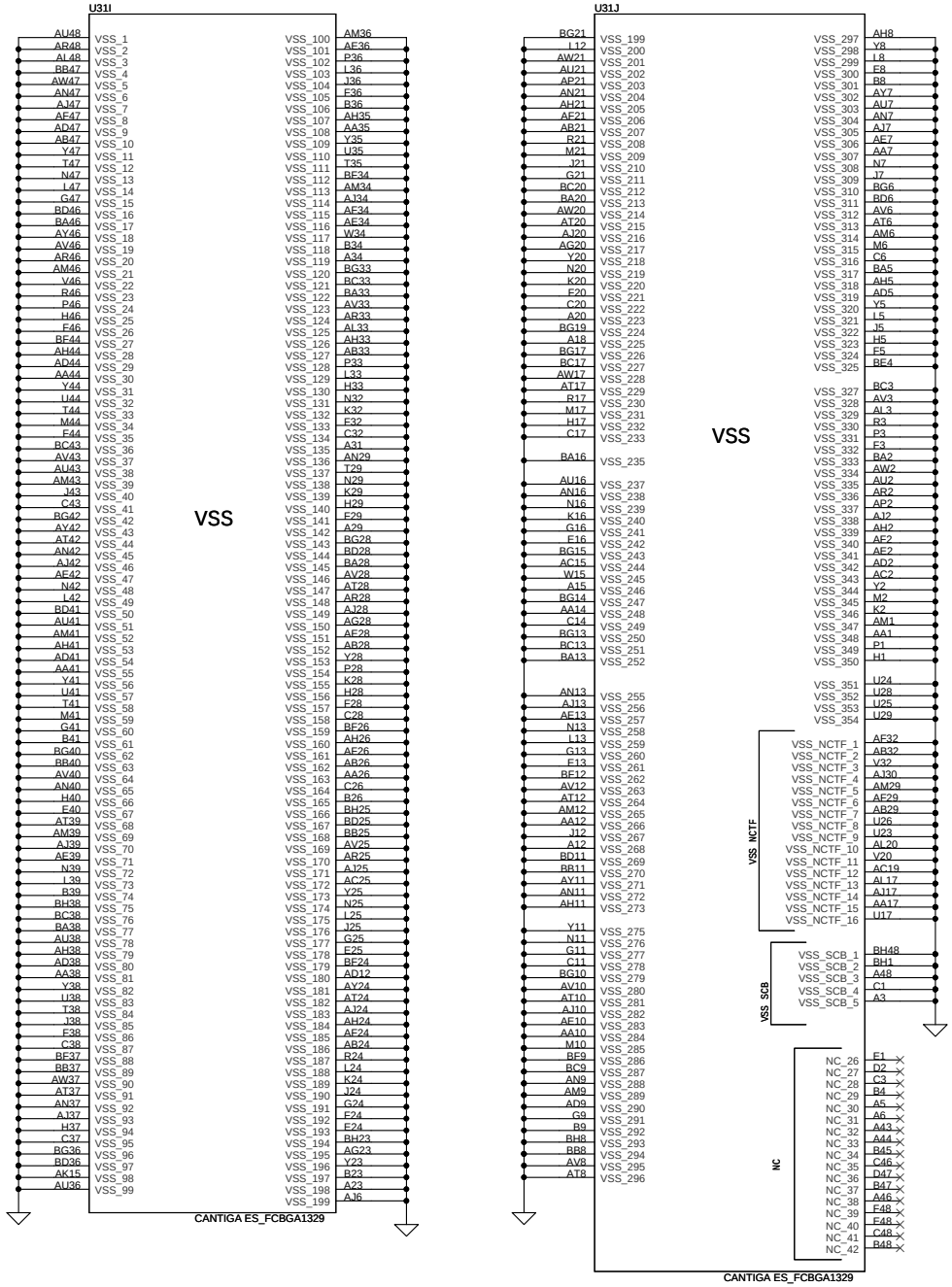

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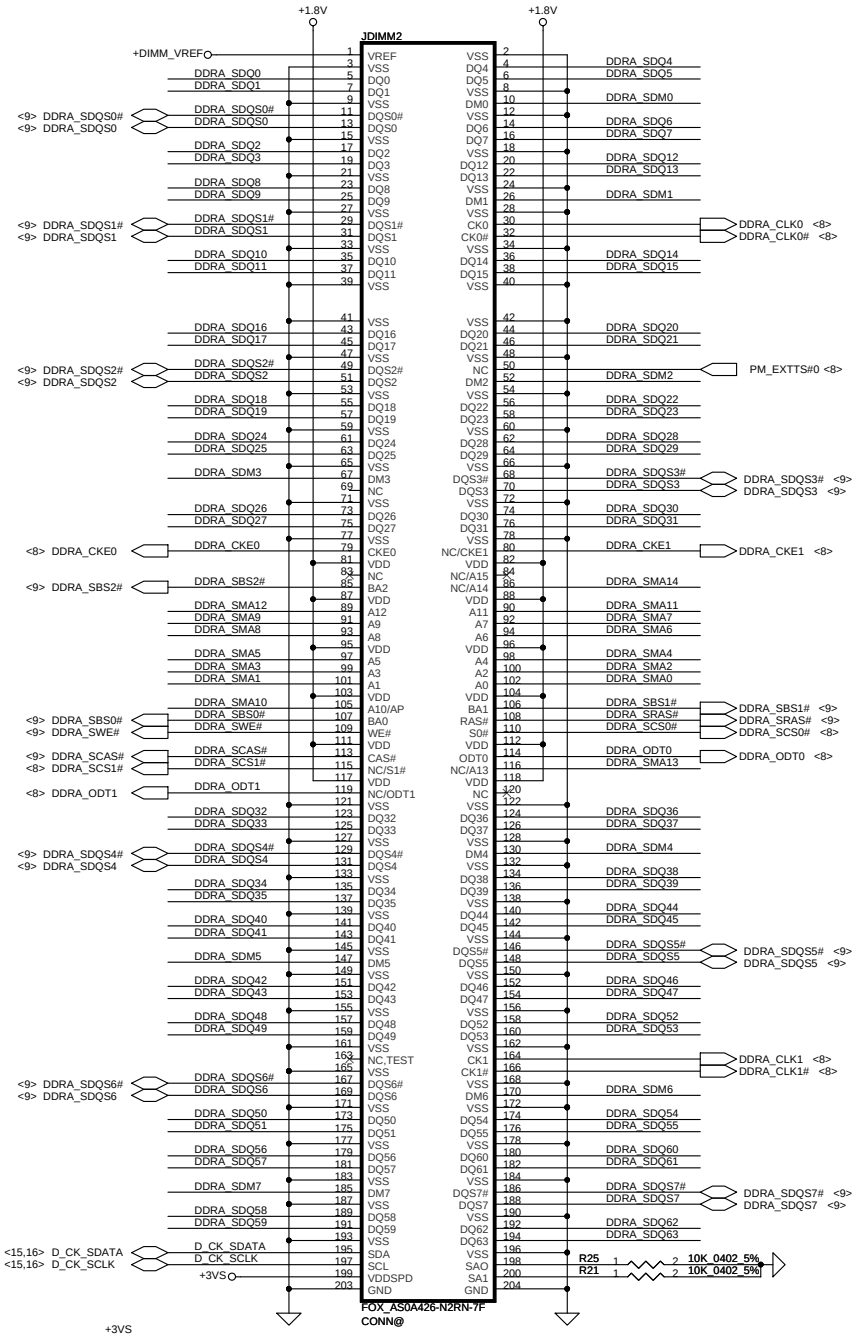
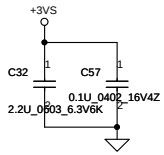
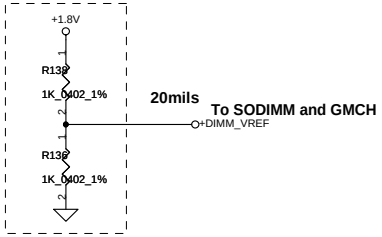
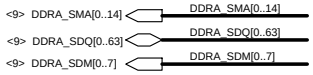
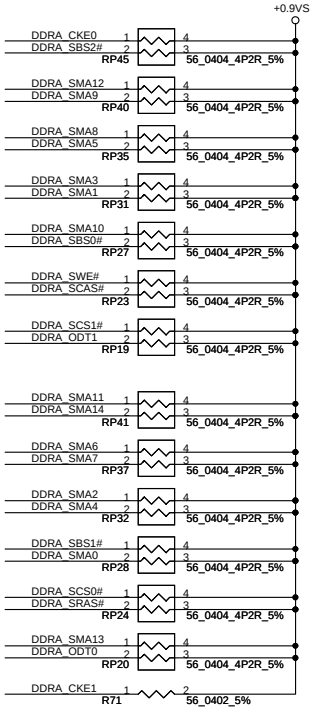


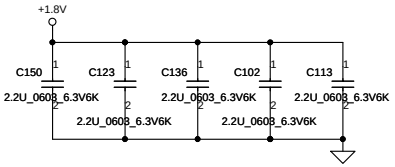
DIMM0 REV H:5.2mm (BOT)

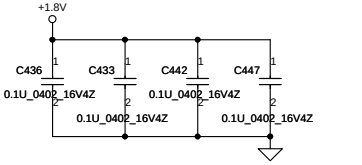


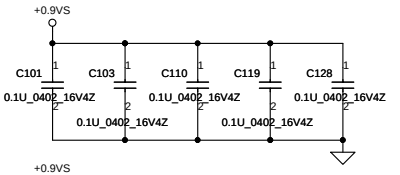


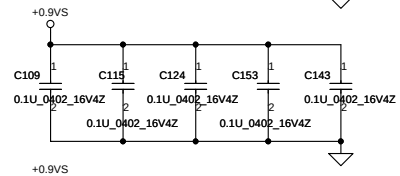


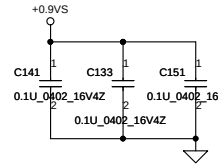












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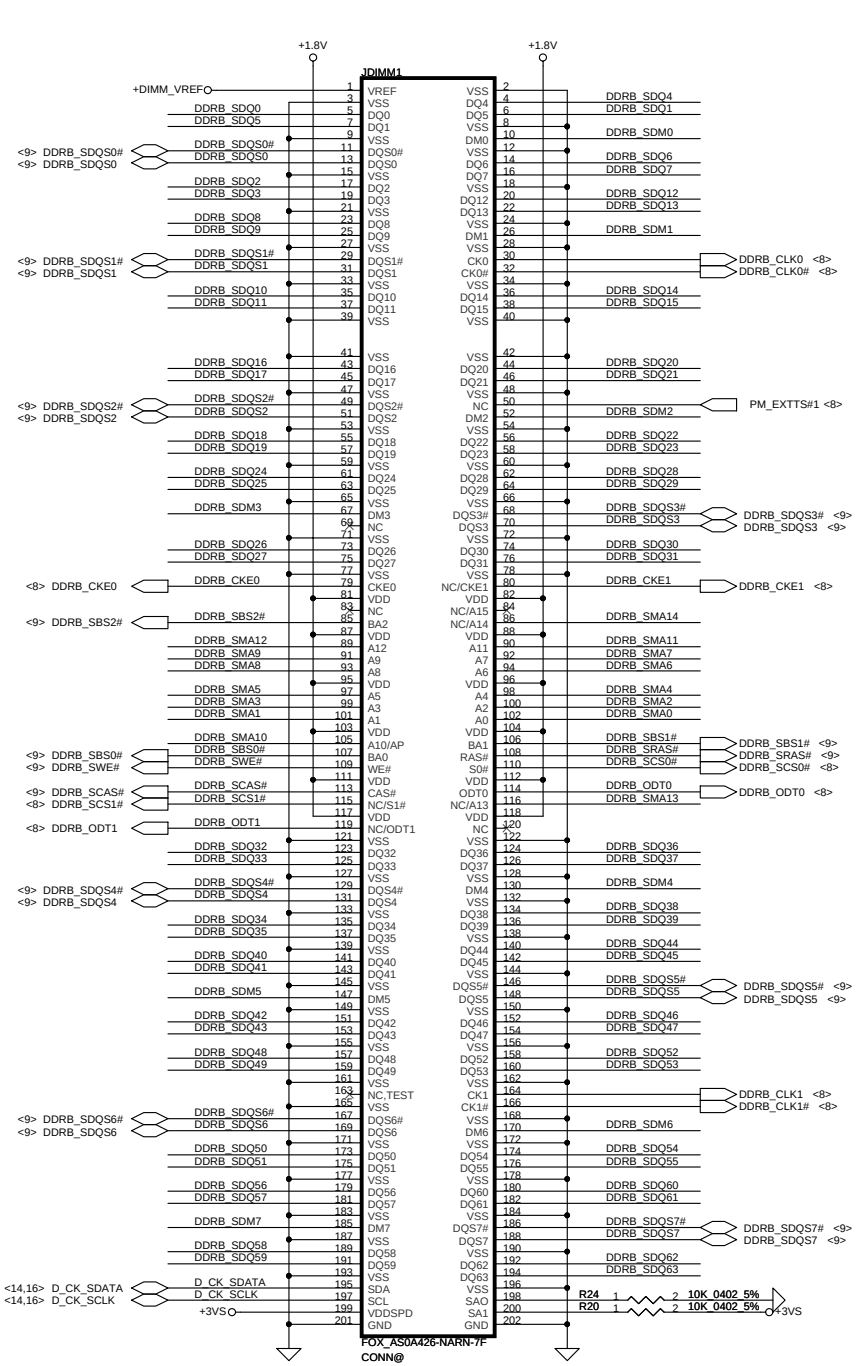
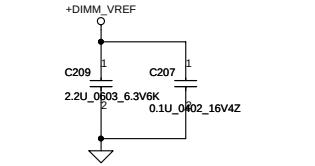
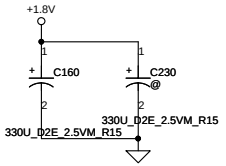
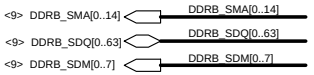
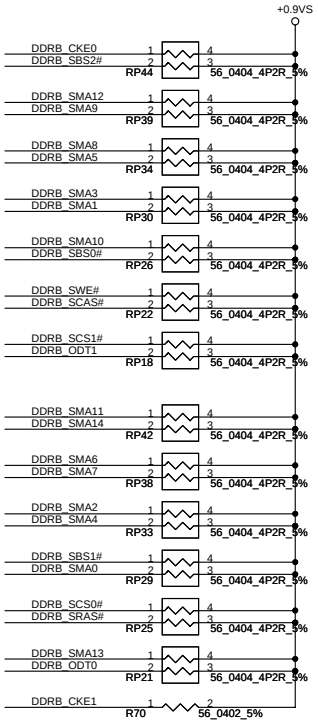


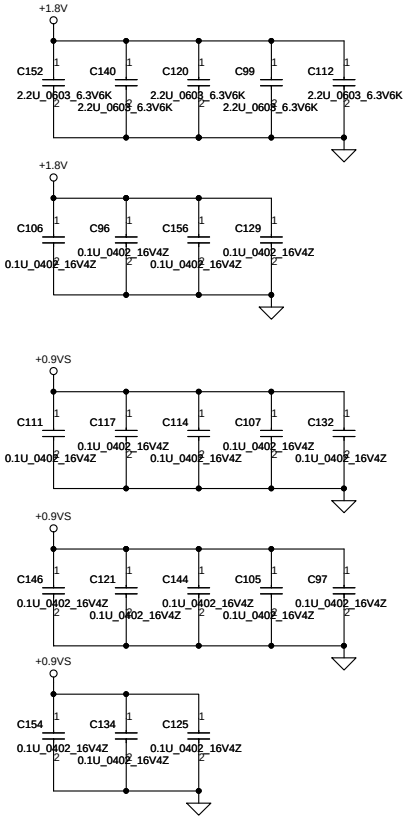
DIMM1 REV H:9.2mm (BOT)











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Clock Generator

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

+3VS — R466 10K_0402_5% — CLK_PCI2

CLK_PCI2=1, Trusted Mode Enable(No overclocking allowed)

R475 @10K_0402_5% — **mount to Enable ITP_CLK**

R474 10K_0402_5% — CLK_PCI5

CLK_PCI5=0, Pin63,64 is SRC_CLK
CLK_PCI5=1, Pin63,64 is ITP_CLK

R471 10K_0402_5% — CLK_PCI4

CLK_PCI4=0, Pin28, 29 is SRC_CLK
Pin24, 25 is DOT96_CLK

R197 @10K_0402_5% — CK_PWRGD

C309 @ 10P_0402_50V8J CLK_PCI_LPC
C321 @ 10P_0402_50V8J CLK_PCI_ICH
For EMI 10/9

+1.05VS — R233 @56_0402_5% — R231 2.2K_0402_5% — R240 1K_0402_5% — CLKSEL0 — MCH_CLKSEL0 <8>
R232 @1K_0402_5% — R241 0_0402_5% — CPU_BSEL0 <5>

+1.05VS — R456 @1K_0402_5% — R459 1K_0402_5% — CLKSEL1 — MCH_CLKSEL1 <8>
R455 @0_0402_5% — R461 0_0402_5% — CPU_BSEL1 <5>

+1.05VS — R465 @1K_0402_5% — R463 10K_0402_5% — R462 1K_0402_5% — CLKSEL2 — MCH_CLKSEL2 <8>
R464 @0_0402_5% — R470 0_0402_5% — CPU_BSEL2 <5>

+1.05VS — L11 FBMA-L11-201209-221LMA30T_0805 — C275 10U_0805_10V4Z
+CLK_VDDSRC — C280 10U_0805_10V4Z — C289 0.1U_0402_16V4Z — C288 0.1U_0402_16V4Z — C315 0.1U_0402_16V4Z — C327 0.1U_0402_16V4Z — C297 0.1U_0402_16V4Z — C329 0.1U_0402_16V4Z

+3VS — L14 FBMA-L11-201209-221LMA30T_0805 — C333 10U_0805_10V4Z
+CLK_VDD — C331 10U_0805_10V4Z — C286 0.1U_0402_16V4Z — C305 0.1U_0402_16V4Z — C300 0.1U_0402_16V4Z — C330 0.1U_0402_16V4Z — C287 0.1U_0402_16V4Z — C328 0.1U_0402_16V4Z

C301, C296 33p change to 27p for RTC issue 20080625

C301 27P_0402_50V8J — CLK_XTALIN
Y1 14.31818MHz_20P_FSX8L14.318181M20FDB
C296 27P_0402_50V8J — CLK_XTALOUT

<21> CLK_ICH_48M — CLK_ICH_48M R484 33_0402_5% — CLKSEL0
<21> CLK_ICH_14M — CLK_ICH_14M R212 33_0402_5% — CLKSEL2

<29> CLK_PCI_LPC — CLK_PCI_LPC R216 33_0402_5% — CLK_PCI3
<19> CLK_PCI_ICH — CLK_PCI_ICH R219 33_0402_5% — CLK_PCI5

<21> CK_PWRGD / <8,21,42> VGATE — 0_0402_5% R199 — CK505_PWRGD
0_0402_5% R204

<21> H_STP_CPU# — H_STP_CPU#
<21> H_STP_PCI# — H_STP_PCI#

+3VS — R454 10K_0402_5% @ — CK505_PWRGD — Q16 2N7002_SOT23 @ — CLK_ENABLE# <42>

+3VS — R228 4.7K_0402_5% — Q48 2N7002_SOT23 — <21,27,28> ICH_SMBDATA — D_CK_SDATA
+3VS — R221 4.7K_0402_5% — Q49 2N7002_SOT23 — <21,27,28> ICH_SMBCLK — D_CK_SCLK

U15

ICS9LPRS387, PN:SA000020H10
SLG8SP556V, PN:SA000020K00

6	VDDREF		
19	VDD48		
72	VDDCPU		
12	VDDPCI		
27	VDDPLL3		
55	VDDSRC		
52	VDDSRC_IO		
38	VDDSRC_IO		
62	VDDSRC_IO		
31	VDDPLL3_IO		
66	VDDCPU_IO		
23	VDD96_IO		
53	CPU_STOP#		
54	PCI_STOP#		
13	PCI1		
14	PCI2/TME		
15	PCI3		
16	PCI4/27_SELECT		
17	PCI_F5/ITP_EN		
1	CK_PWRGD/PD#		
5	X1		
4	X2		
11	NC		
20	USB_48MHz/FSLA		
2	FSLB/TEST_MODE		
7	FSLC/TEST_SEL/REF0		
8	REF1		
69	GNDCPU		
3	GNDREF		
18	GNDPCI		
22	GND48		
30	GND		
26	GND		
34	GNDSRC		
59	GNDSRC		
42	GNDSRC		
73	GND_THERMAL_PAD		
9	SDATA	D_CK_SDATA	D_CK_SDATA <14,15>
10	SCLK	D_CK_SCLK	D_CK_SCLK <14,15>
71	CPUT0_LPR_F	CLK_CPU_BCLK	CLK_CPU_BCLK <4>
70	CPUC0_LPR_F	CLK_CPU_BCLK#	CLK_CPU_BCLK# <4>
68	CPUT1_LPR_F	CLK_MCH_BCLK	CLK_MCH_BCLK <7>
67	CPUC1_LPR_F	CLK_MCH_BCLK#	CLK_MCH_BCLK# <7>
24	SRCT0_LPR/DOTT_96_LPR	CLK_DREF_96M	CLK_DREF_96M <8>
25	SRCC0_LPR/DOTC_96_LPR	CLK_DREF_96M#	CLK_DREF_96M# <8>
28	27MHz_NonSS/SRCT1_LPR/SE1	CLK_DREF_SSC	CLK_DREF_SSC <8>
29	27MHz_SS/SRCC1_LPR/SE2	CLK_DREF_SSC#	CLK_DREF_SSC# <8>
32	SRCT2_LPR/SATAT_LPR	CLK_PCIE_SATA	CLK_PCIE_SATA <20>
33	SRCC2_LPR/SATAC_LPR	CLK_PCIE_SATA#	CLK_PCIE_SATA# <20>
35	SRCT3_LPR	CLK_PCIE_ICH	CLK_PCIE_ICH <21>
36	SRCC3_LPR	CLK_PCIE_ICH#	CLK_PCIE_ICH# <21>
39	SRCT4_LPR	CLK_PCIE_CARD	CLK_PCIE_CARD <28>
40	SRCC4_LPR	CLK_PCIE_CARD#	CLK_PCIE_CARD# <28>
57	SRCT6_LPR	CLK_MCH_3GPLL	CLK_MCH_3GPLL <8>
56	SRCC6_LPR	CLK_MCH_3GPLL#	CLK_MCH_3GPLL# <8>
61	SRCT7_LPR		
60	SRCC7_LPR		
64	CPUT2_ITP_LPR/SRCT8_LPR	CLK_PCIE_READER	CLK_PCIE_READER <24>
63	CPUC2_ITP_LPR/SRCC8_LPR	CLK_PCIE_READER#	CLK_PCIE_READER# <24>
44	SRCT9_LPR	CLK_PCIE_MINI2	CLK_PCIE_MINI2 <27>
45	SRCC9_LPR	CLK_PCIE_MINI2#	CLK_PCIE_MINI2# <27>
50	SRCT10_LPR		
51	SRCC10_LPR		
48	SRCT11_LPR	CLK_PCIE_LAN	CLK_PCIE_LAN <25>
47	SRCC11_LPR	CLK_PCIE_LAN#	CLK_PCIE_LAN# <25>
37	CR#3		
41	CR#4		R214 10K_0402_5% +3VS — EXP_CLKREQ# <28>
58	CR#6		MCH_CLKREQ# <8> (Pull High to +3VS at GMCH side)
65	CR#7		
43	CR#9		R213 10K_0402_5% +3VS — MINI2_CLKREQ# <27>
49	CR10#		R211 10K_0402_5% +3VS
46	CR#11		
21	CR#A		SATA_CLKREQ# <21> (Pull High to +3VS at ICH side)

ICS9LPRS387BKLFT_MLF72_10x10

VGA: disable this pair by BIOS

VGA: disable this pair by BIOS

UMA: disable this pair by BIOS

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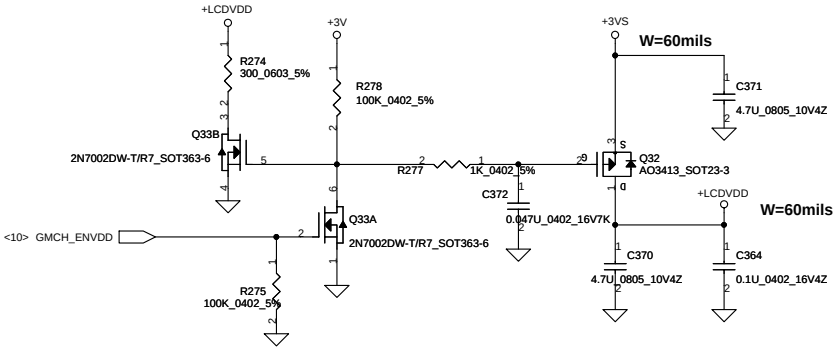
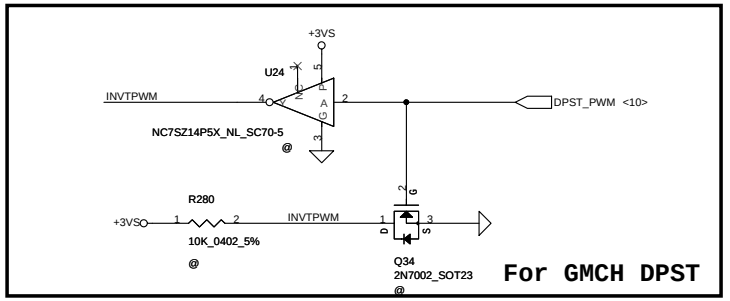
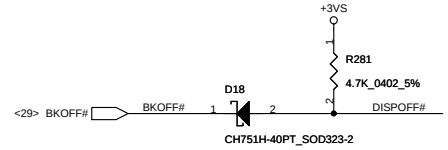
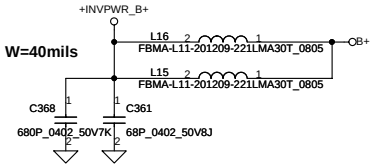
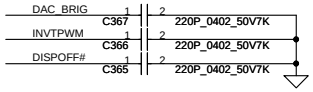
LCD POWER CIRCUIT



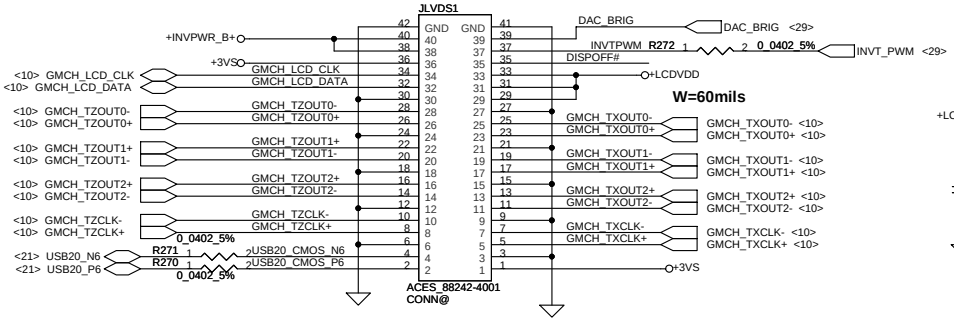


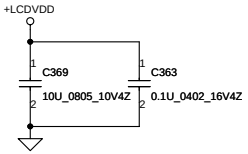


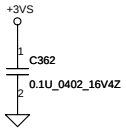




LCD/PANEL BD. Conn.







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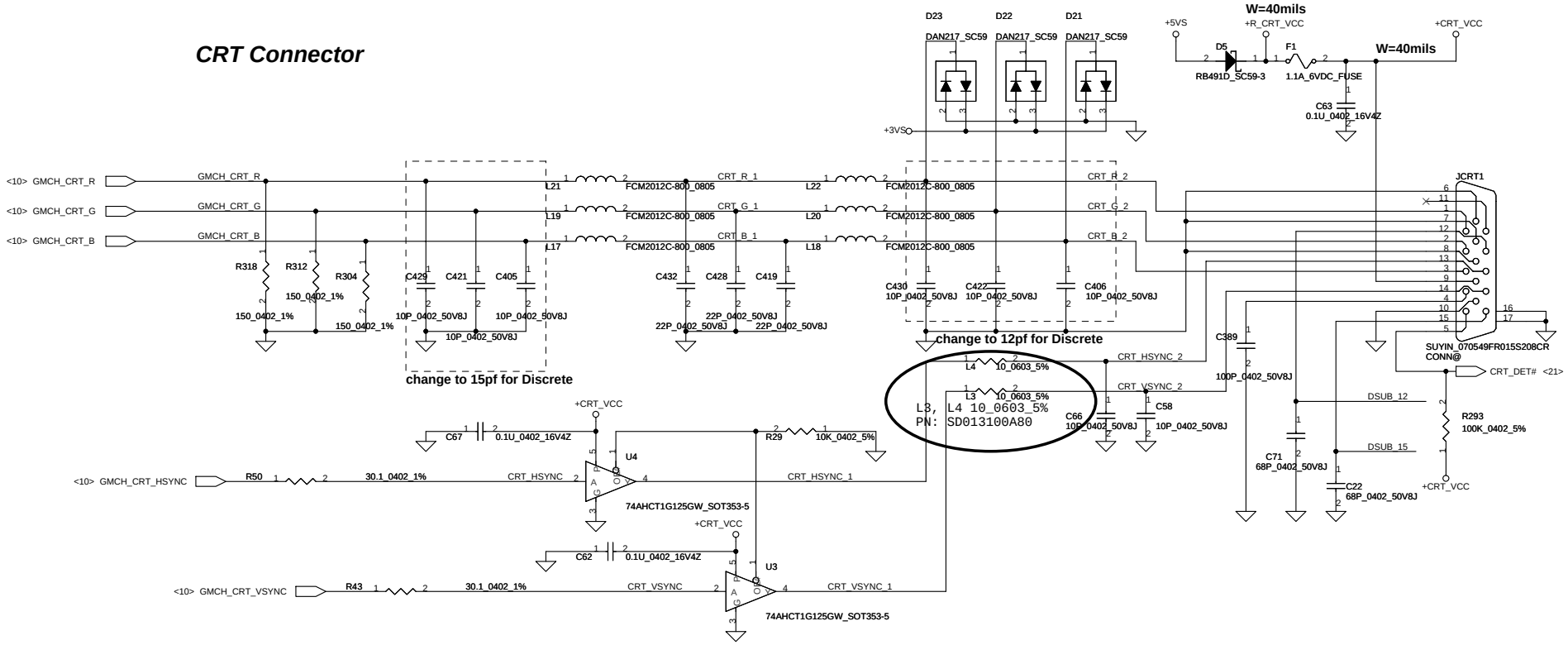
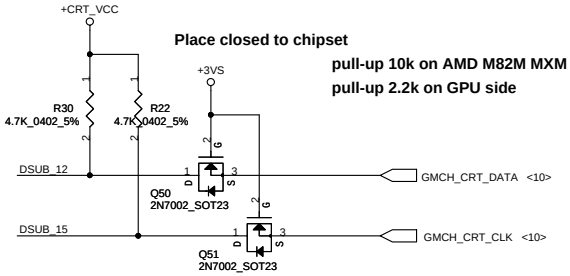
CRT Connector





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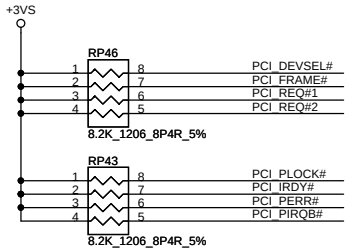
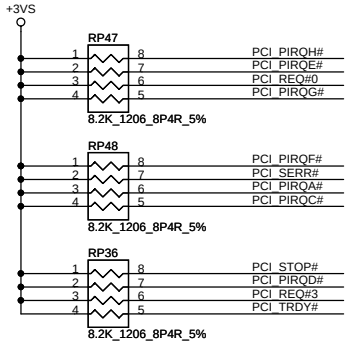
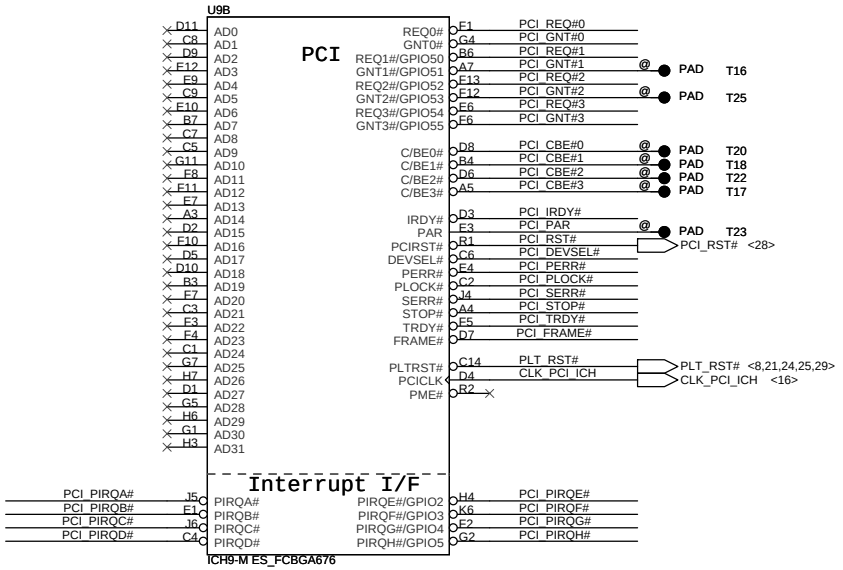
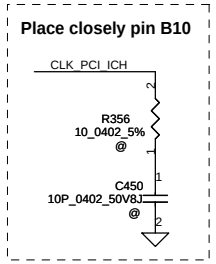
DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)

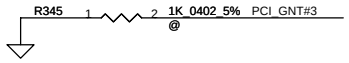




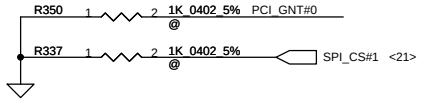


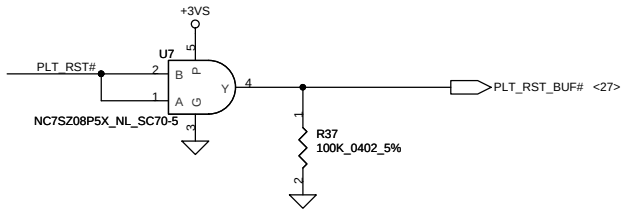


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*



Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*





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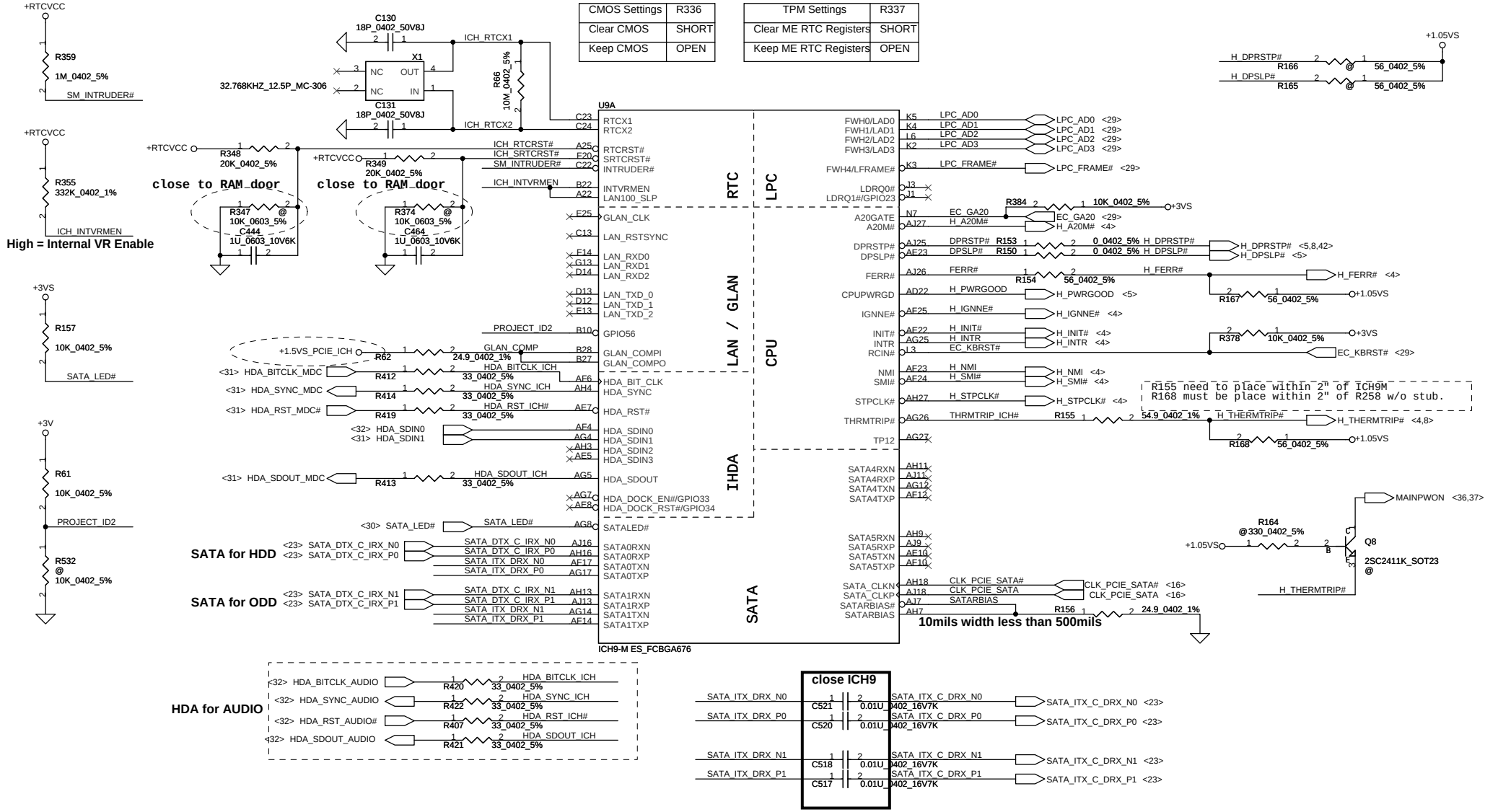
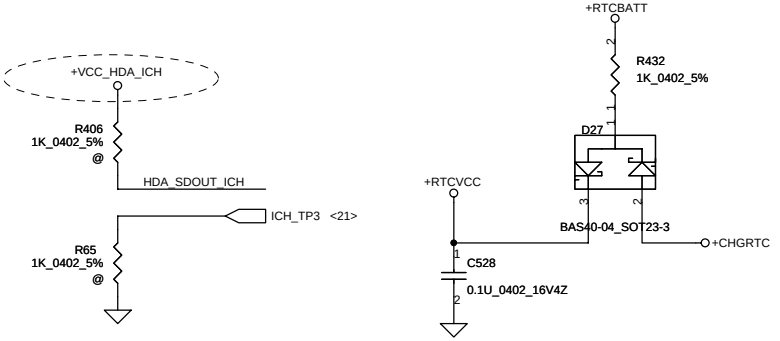
CMOS Settings	R336
Clear CMOS	SHORT
Keep CMOS	OPEN

TPM Settings	R337
Clear ME RTC Registers	SHORT
Keep ME RTC Registers	OPEN





XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

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Compal Electronics, Inc.

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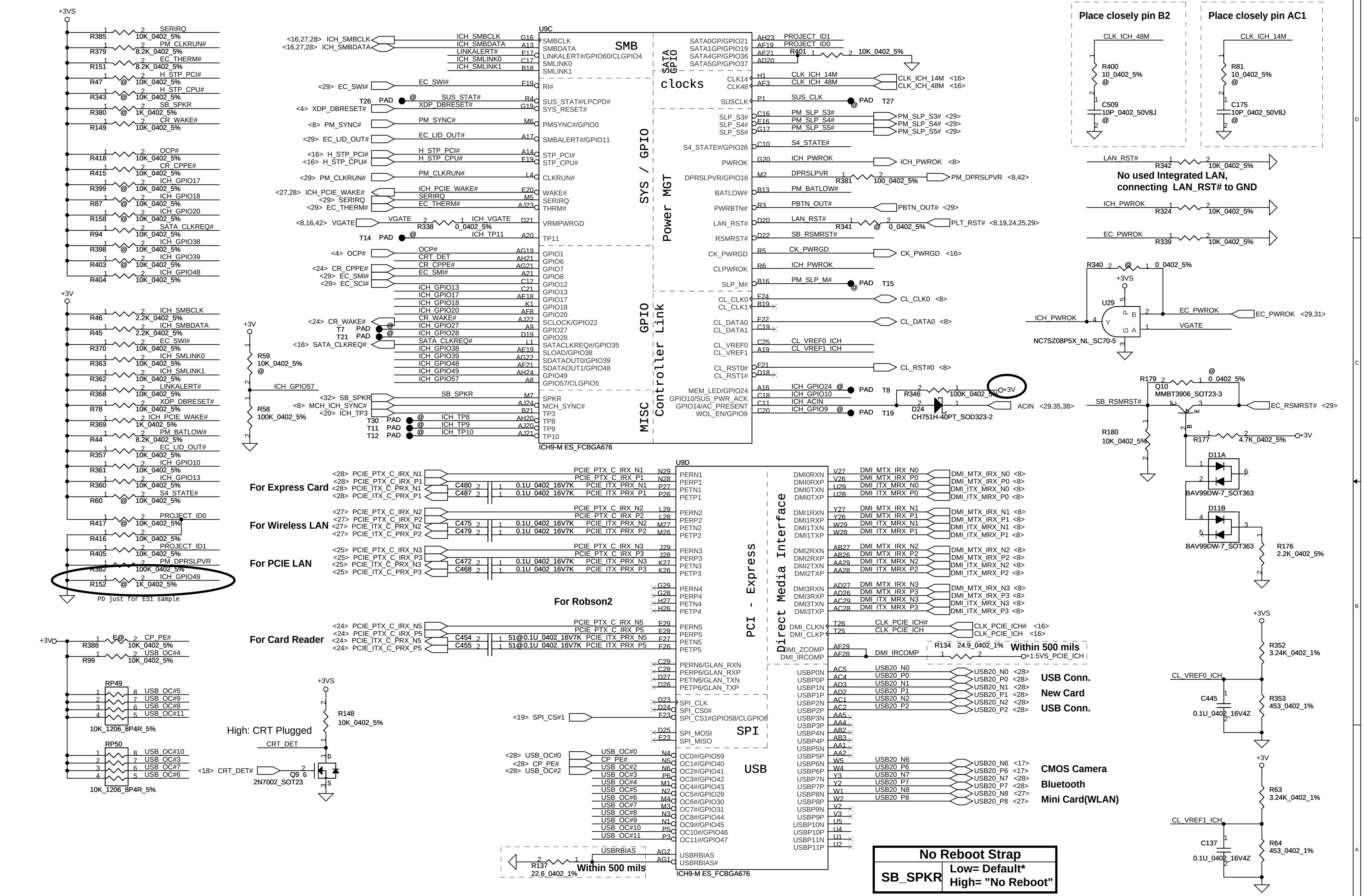

No Reboot Strap	
SB_SPKR	Low= Default* High= "No Reboot"

Internal TPM Strap	
SPI_MOSI	Low= Disable* High= iTPM enable by MCH strap

DMI Termination Voltage	
GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

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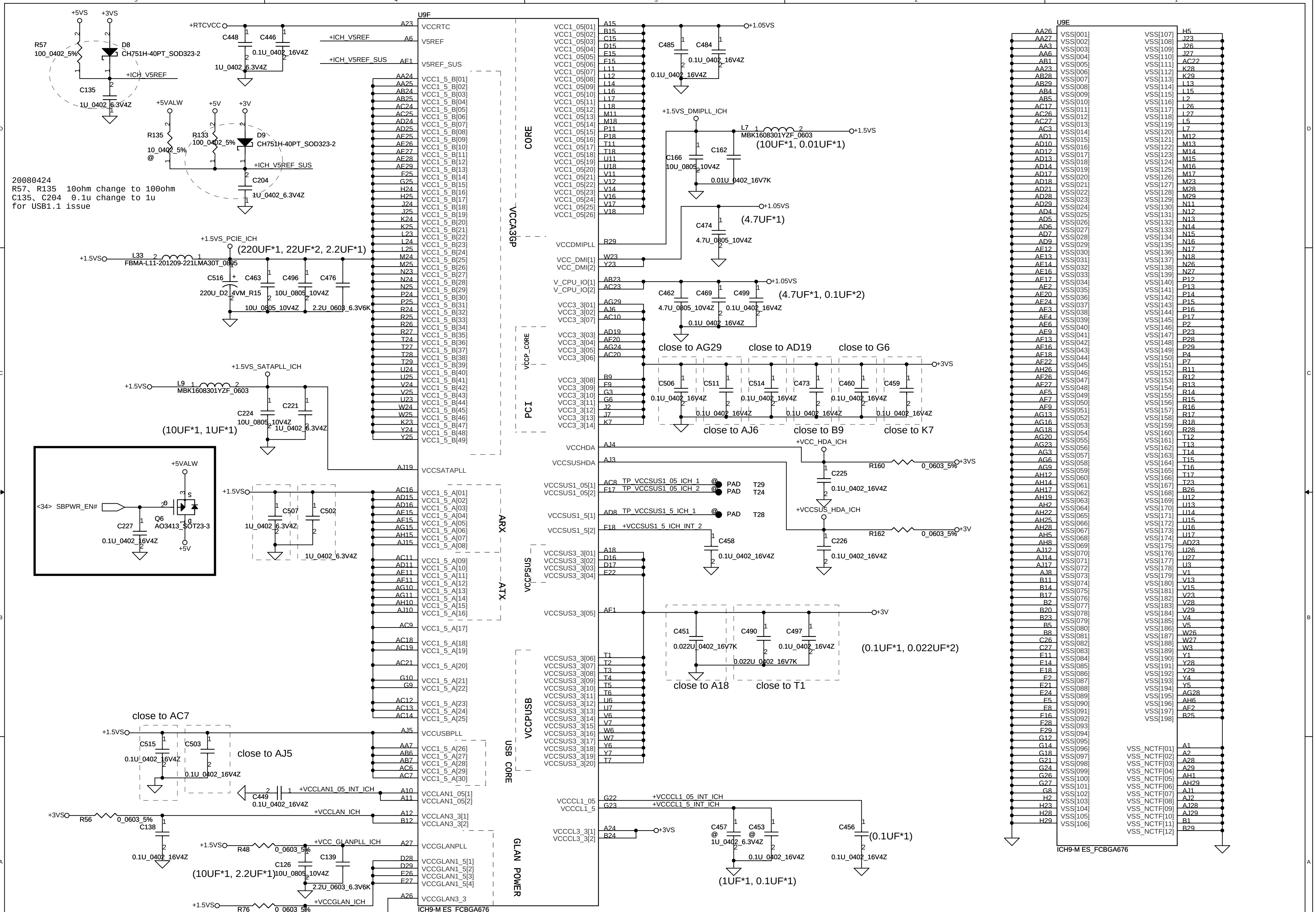
U9F
20080424
R57、R135 10ohm change to 100ohm
C135、C204 0.1u change to 1u
for USB1.1 issue
CORE
VCCA3GP
VCCP_CORE
PCI
ARX
ATX
VCCPSUS
VCCPUSB
USB CORE
GLAN POWER
(220UF*1, 22UF*2, 2.2UF*1)
(10UF*1, 1UF*1)
(10UF*1, 0.01UF*1)
(4.7UF*1)
(4.7UF*1, 0.1UF*2)
close to AG29
close to AD19
close to G6
close to AJ6
close to B9
close to K7
(0.1UF*1, 0.022UF*2)
close to A18
close to T1
close to AC7
close to AJ5
(10UF*1, 2.2UF*1)
(0.1UF*1)
(1UF*1, 0.1UF*1)
ICH9-M ES_FCBGA676
U9E

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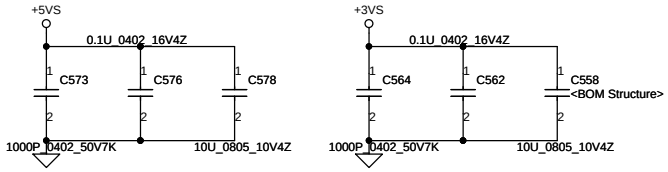
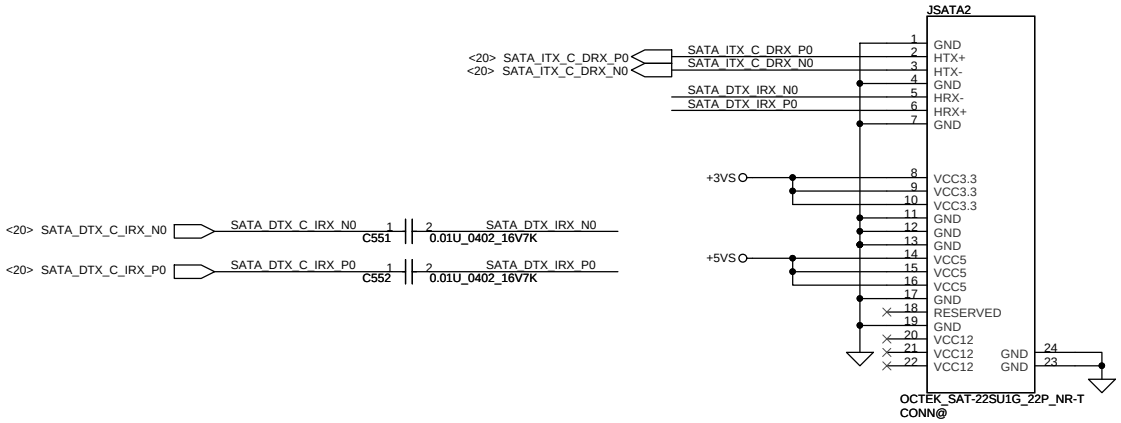
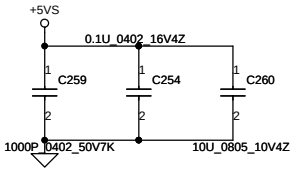
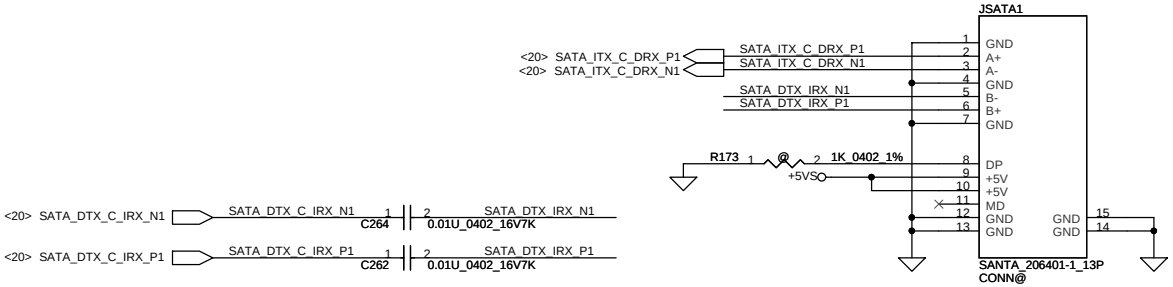


SATA HDD Conn.





SATA ODD Conn.



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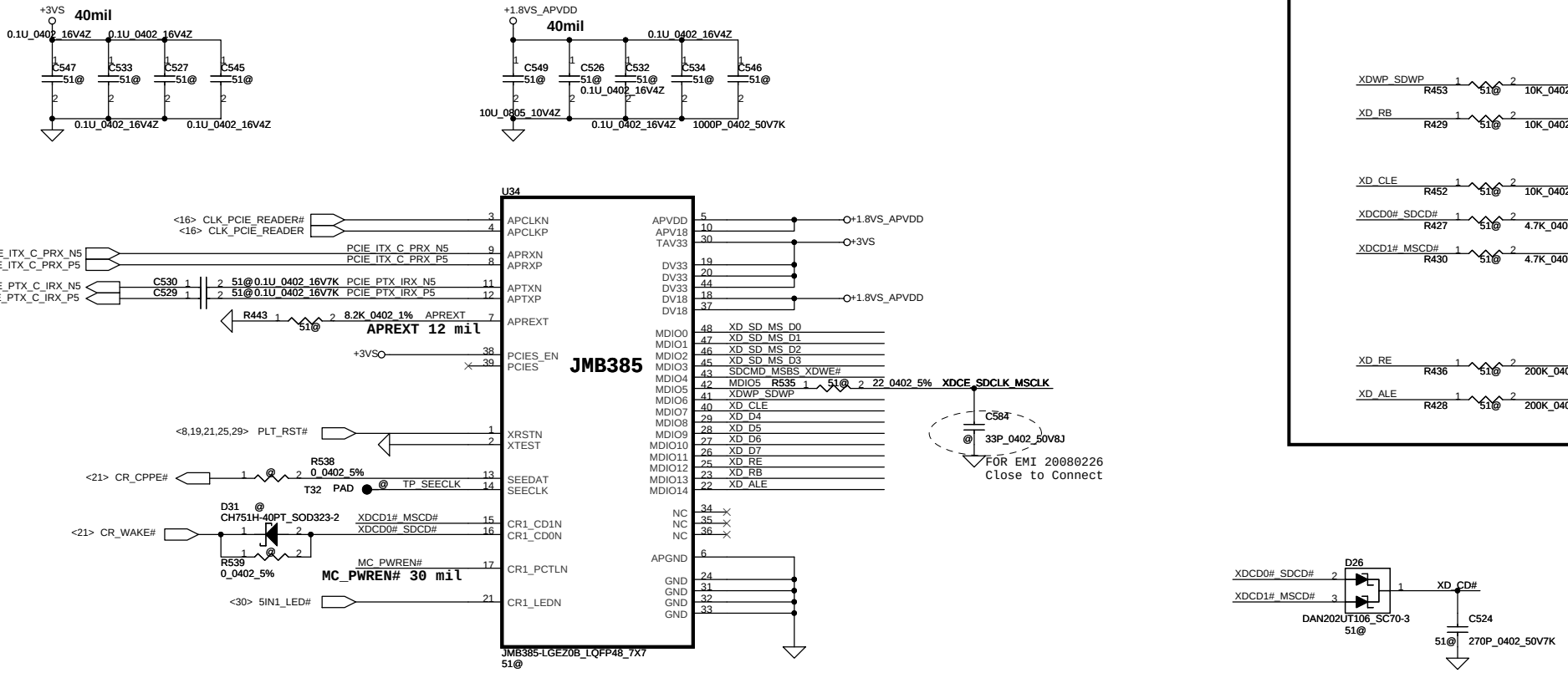
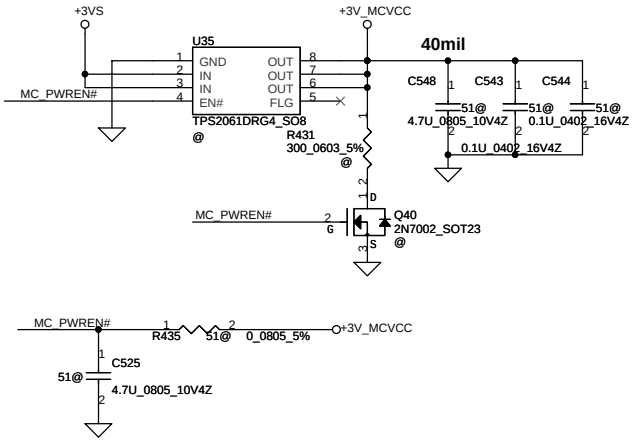
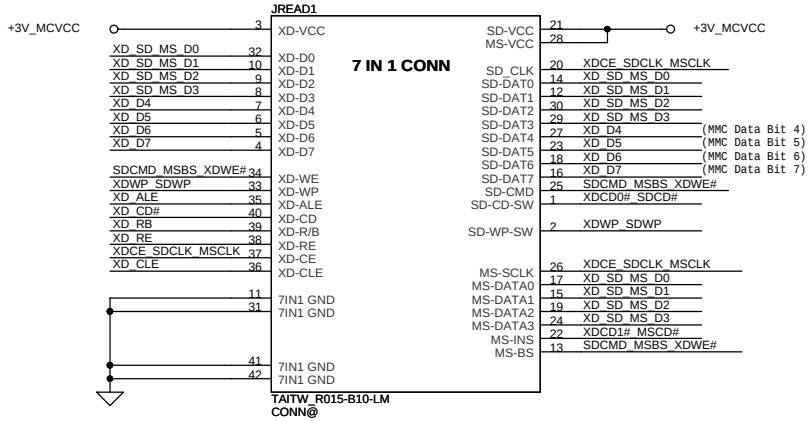


Memory Card Power Switch



4 IN 1 Socket Push Type(New)



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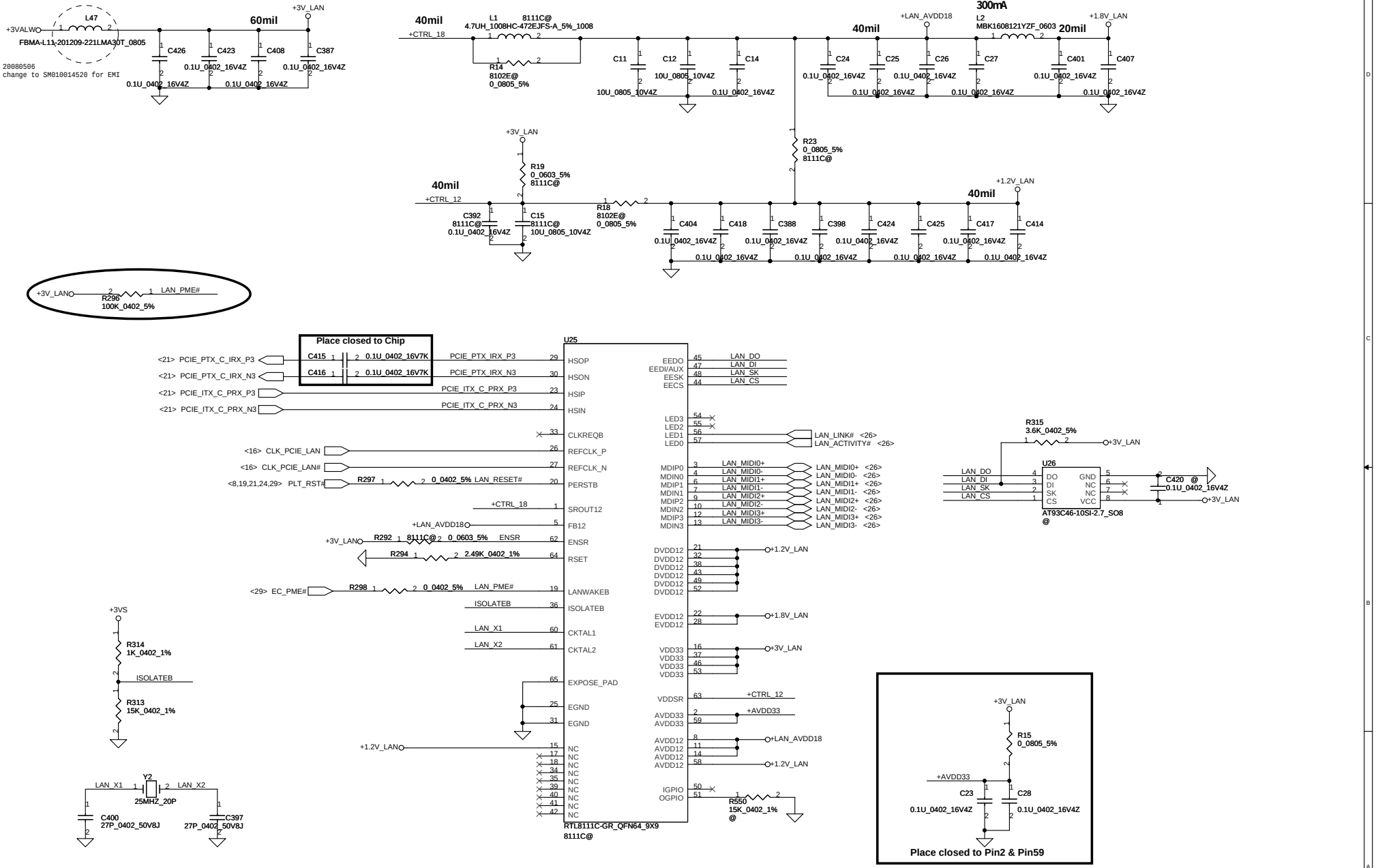
LAN RTL8111C/8102E



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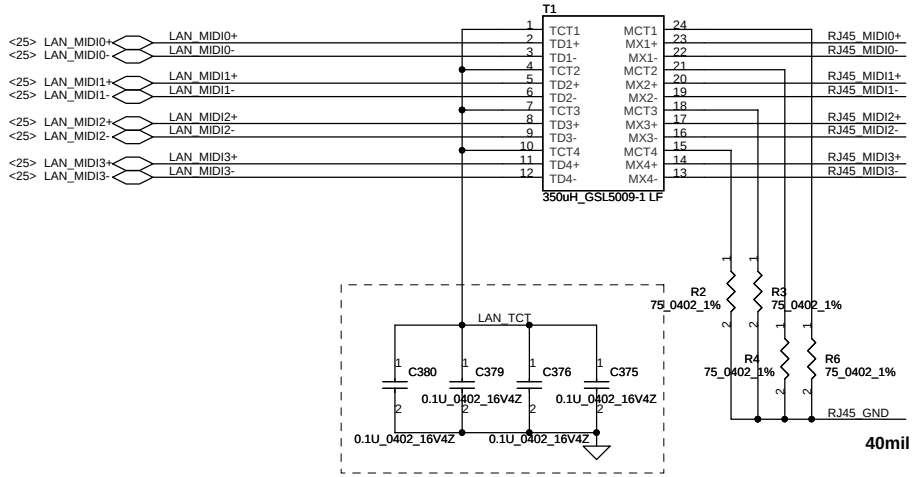
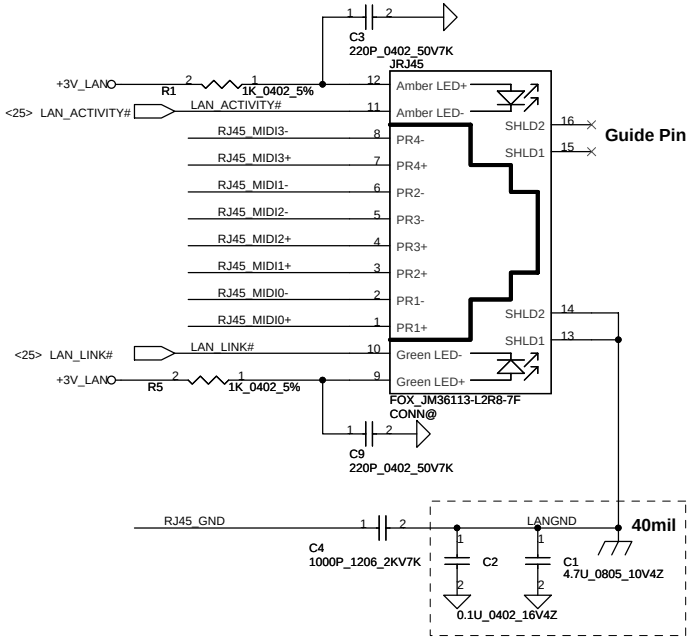
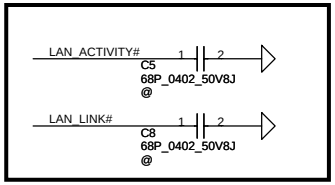
LAN RTL8111C/8102E







For EMI

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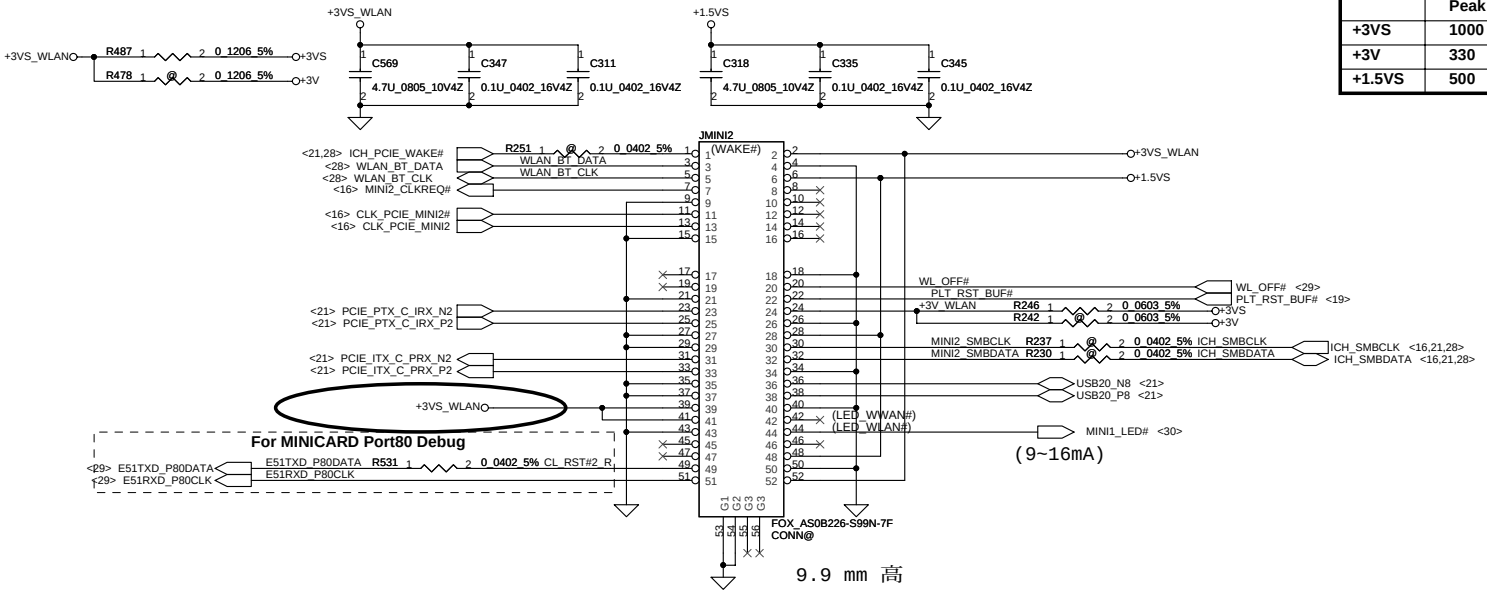
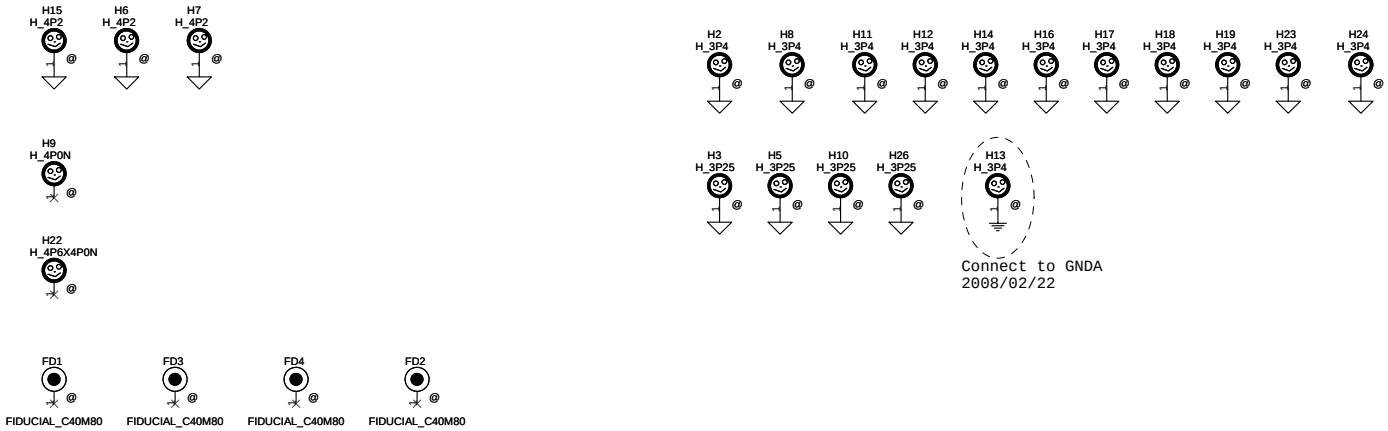
For Wireless LAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)





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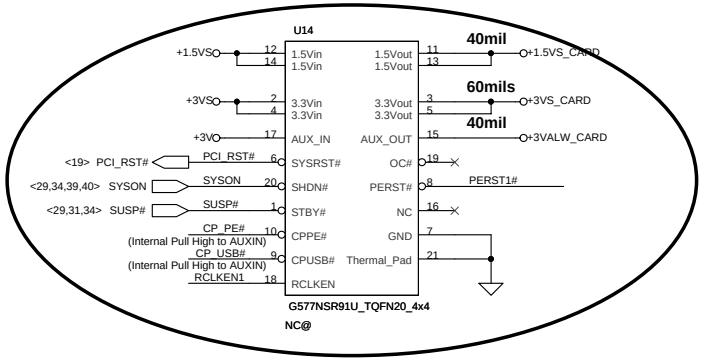
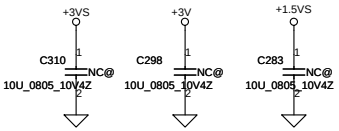
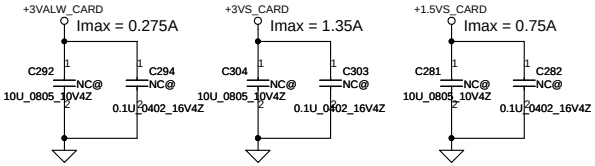
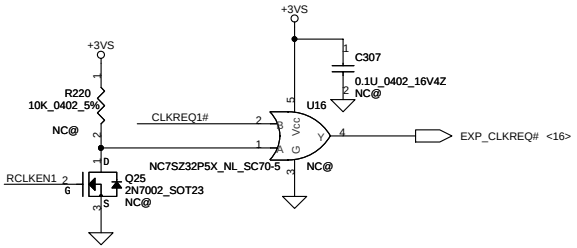
New Card Power Switch

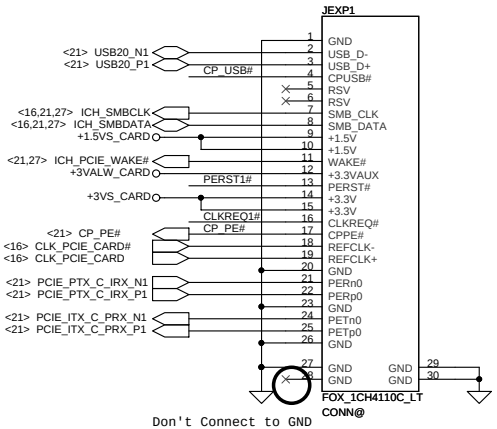






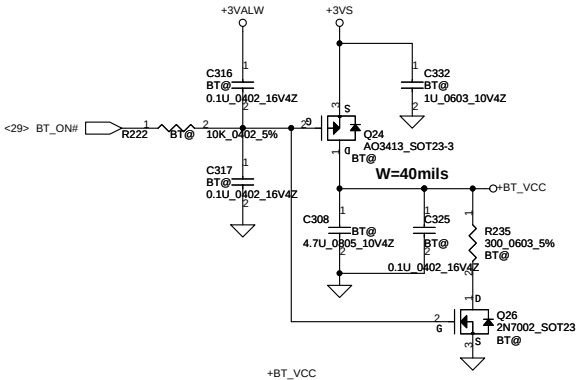


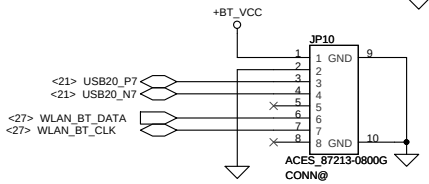
New Card Socket (Left/TOP)



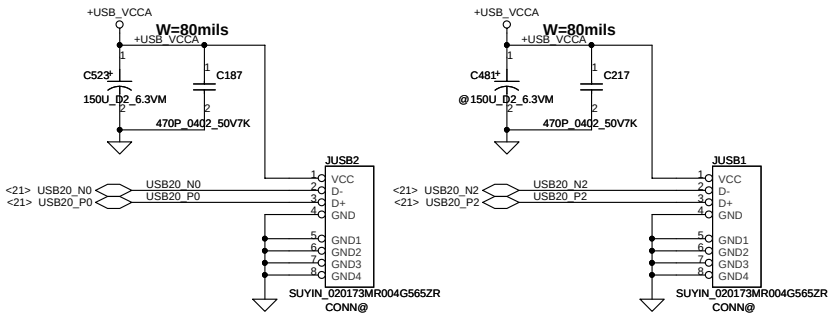
Don't Connect to GND
2008/02/22

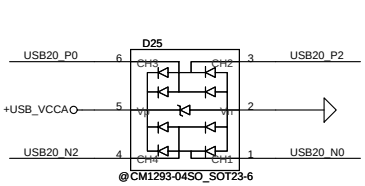
Bluetooth Conn.

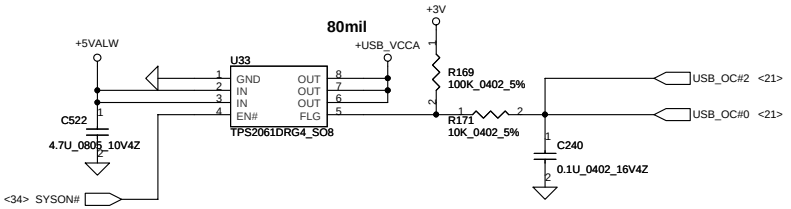




USB CONN. (Stack-up Type)







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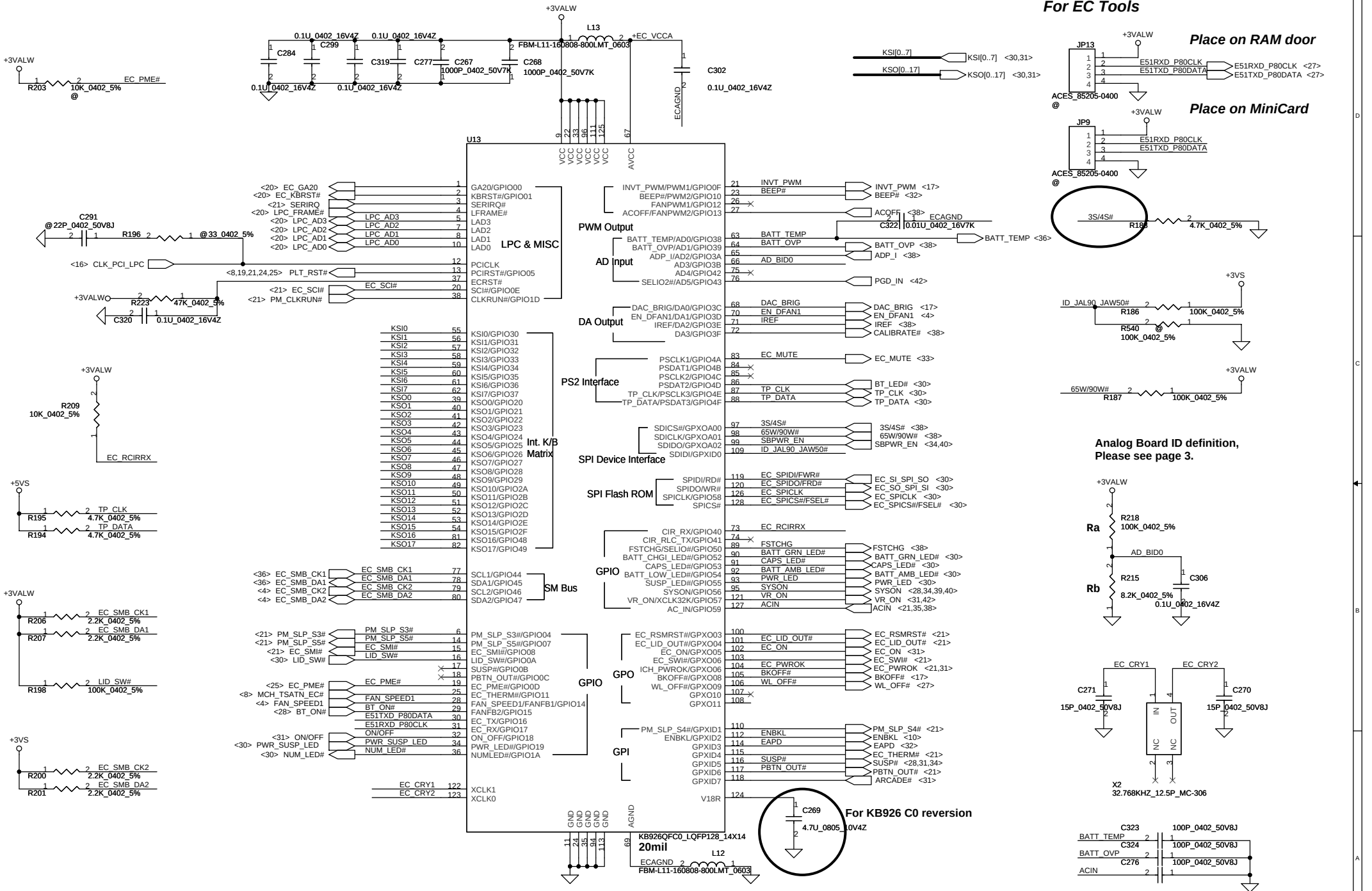

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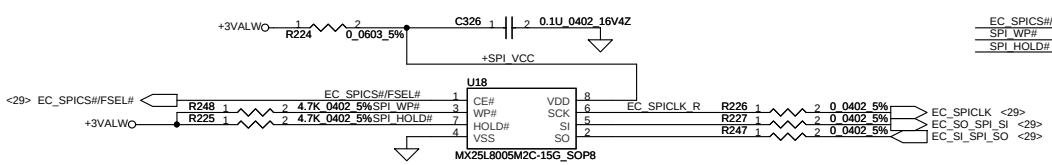
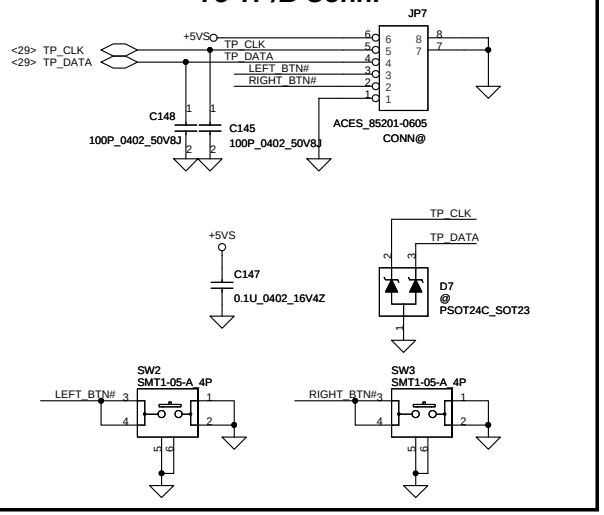
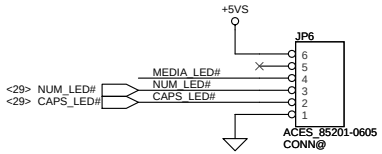


ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz

To TP/B Conn.

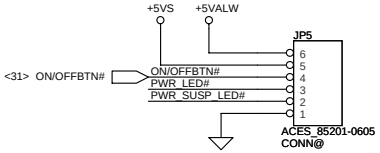


To LED/B



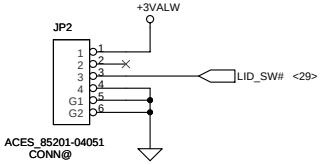
(4pin)

To POWER/B



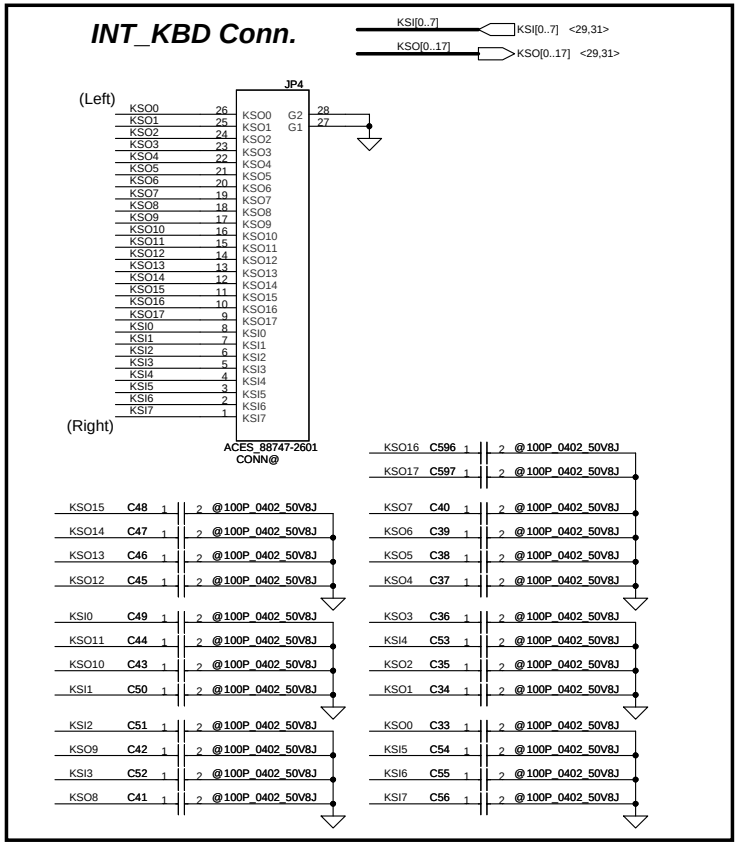
(6pin)

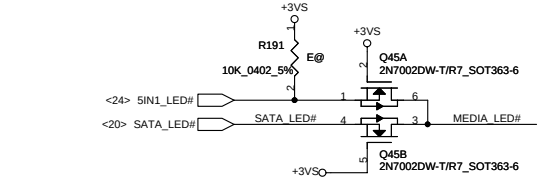
To LID SW/B

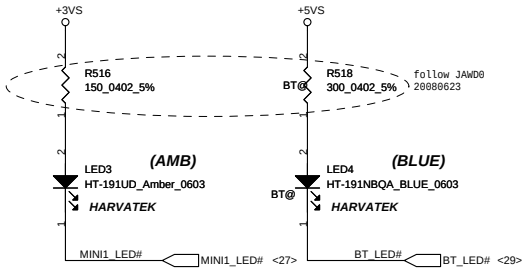


(4pin)

INT_KBD Conn.

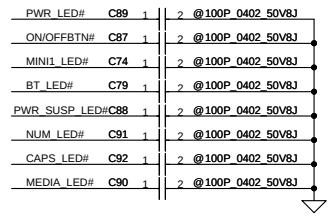




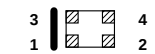


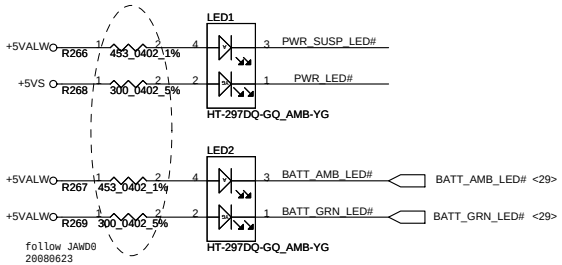
Wireless LED **Bluetooth LED**

FOR EMI



Compal Footprint





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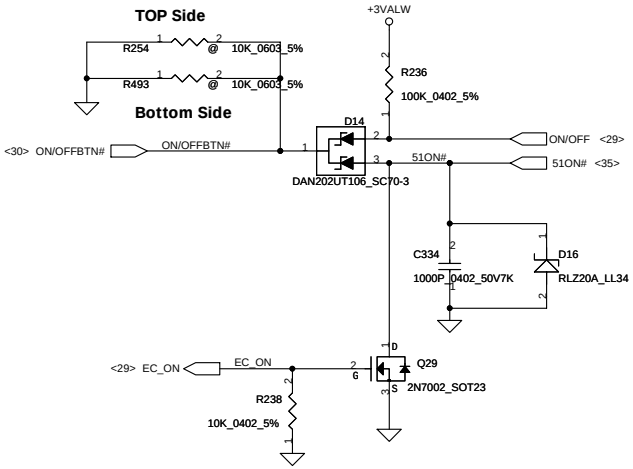
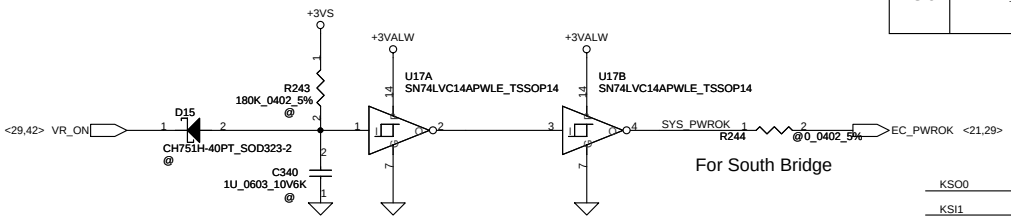
Power Button

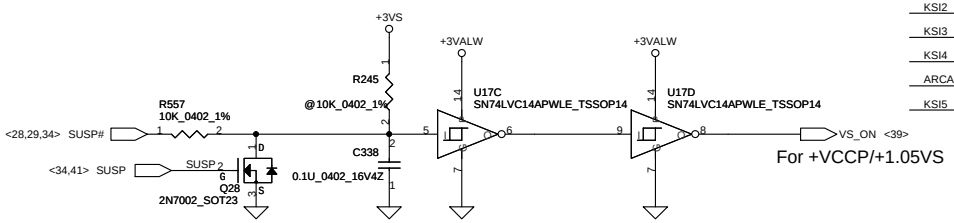
ON/OFF switch



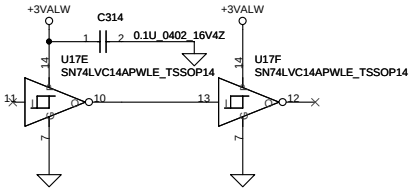
Power ON Circuit



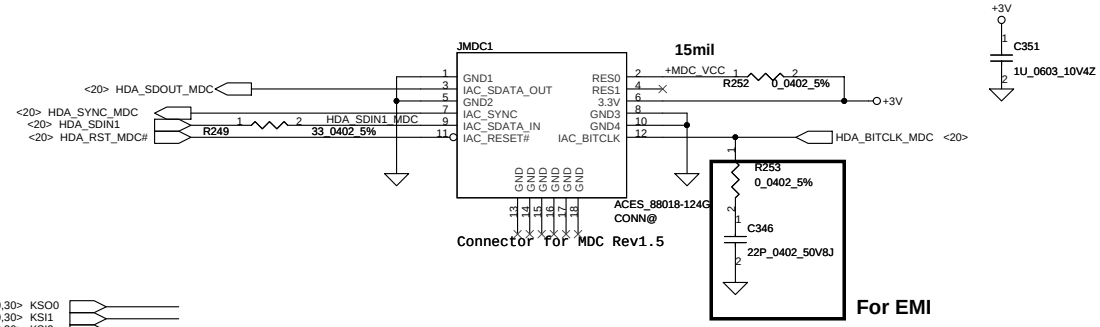
For South Bridge



For +VCCP/+1.05VS



HDA MDC Conn.



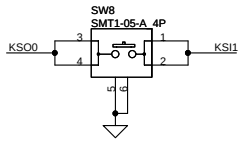
For EMI

<29,30> KSO0
<29,30> KSI1
<29,30> KSI2
<29,30> KSI3
<29,30> KSI4
<29,30> KSI5

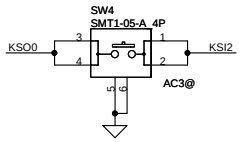
To BTN/B Conn.

	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#

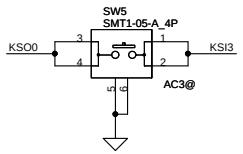
Wireless Button



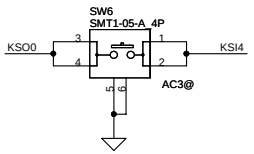
Bluetooth Button

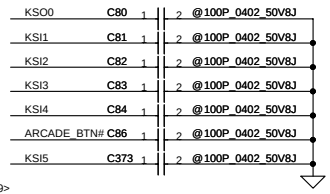


Volume UP BTN

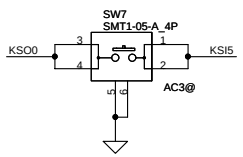


Volume DOWN BTN

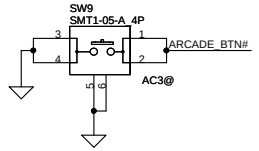


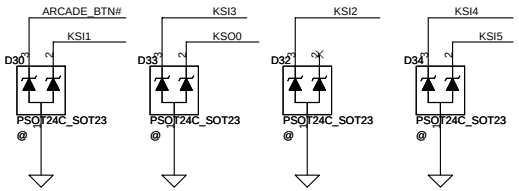


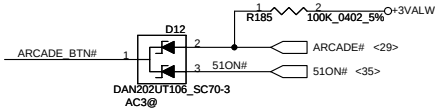
e-Key BTN



ARCADE BTN







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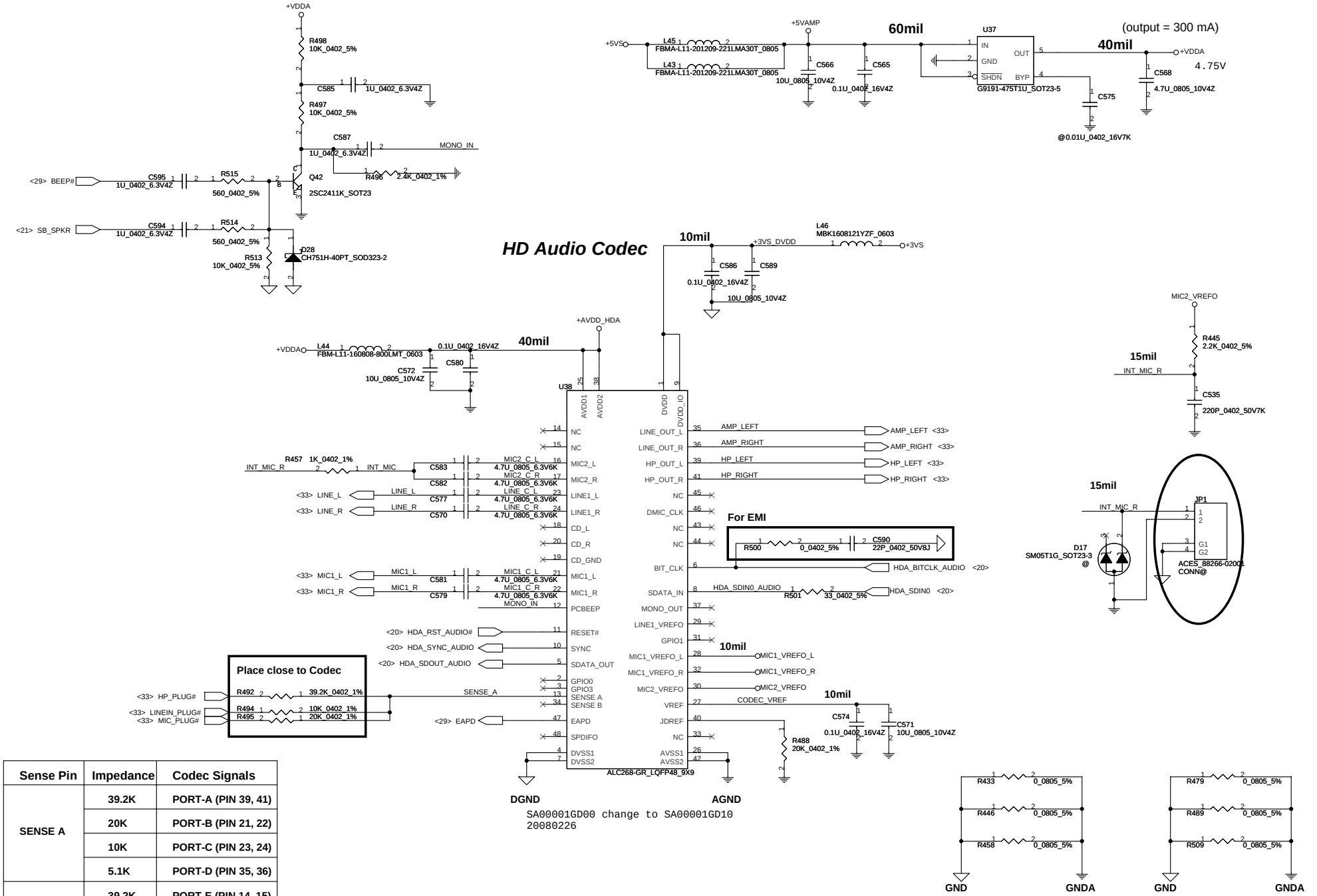

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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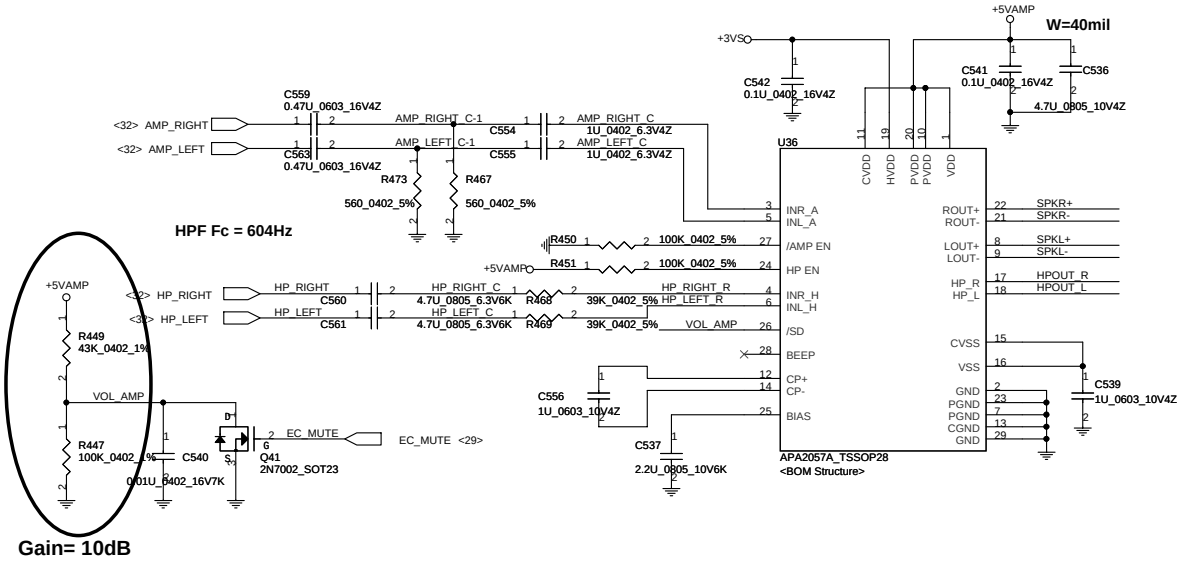
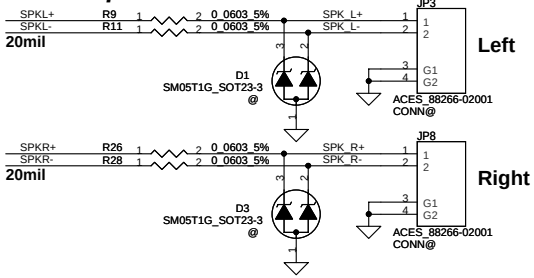
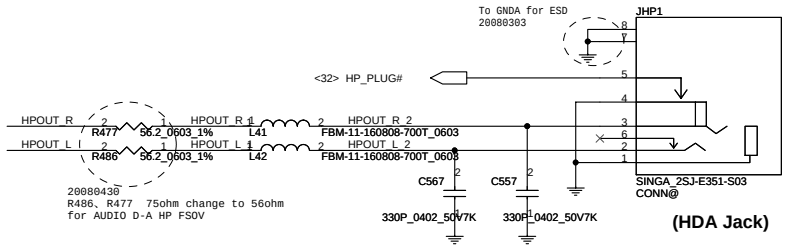


Int. Speaker Conn.

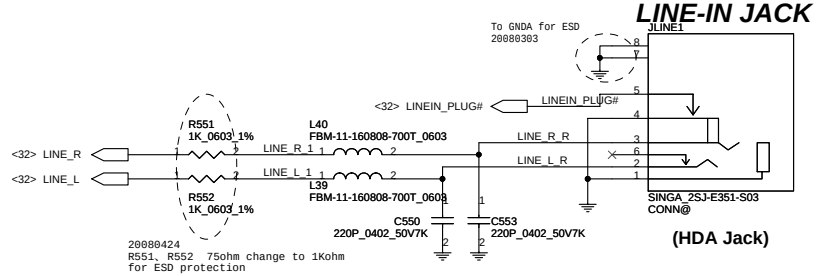


HP JACK



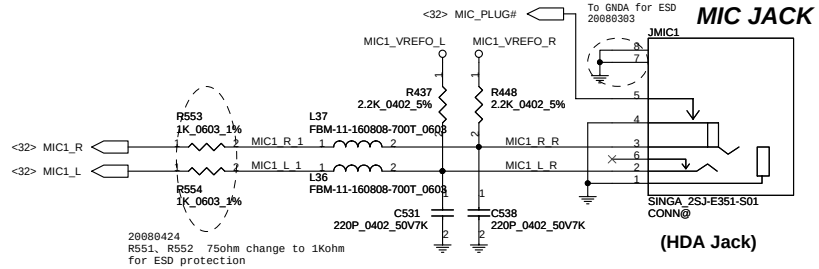
(HDA Jack)

LINE-IN JACK



(HDA Jack)

MIC JACK



(HDA Jack)

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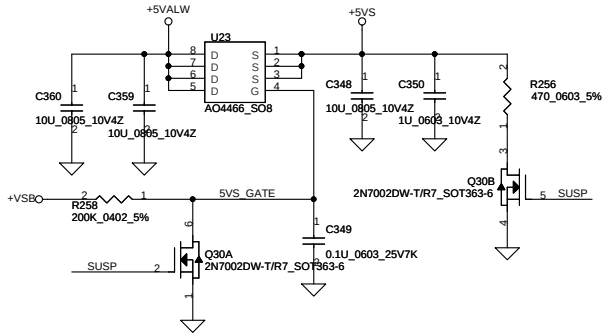
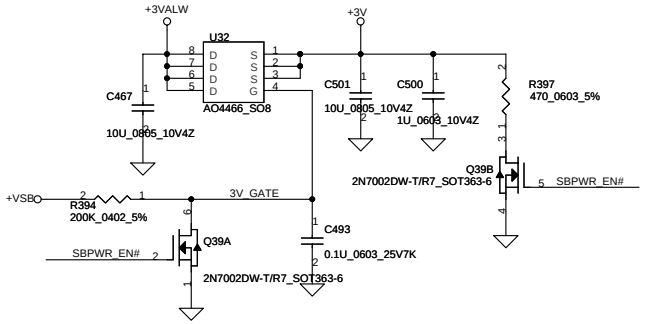
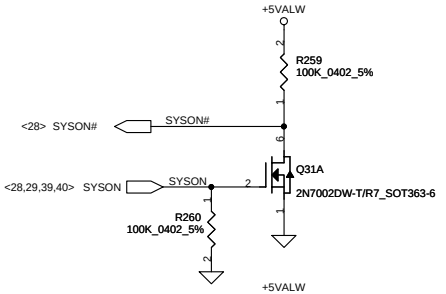
+5VALW TO +5VS

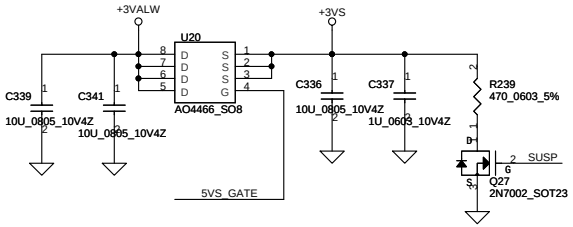


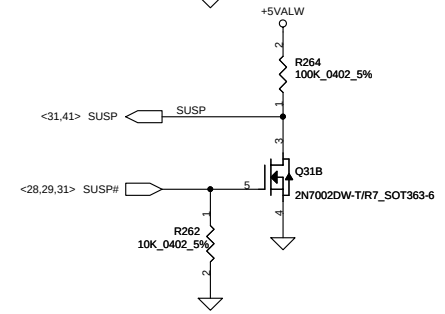
+3VALW TO +3V_SB(ICH8M AUX Power)



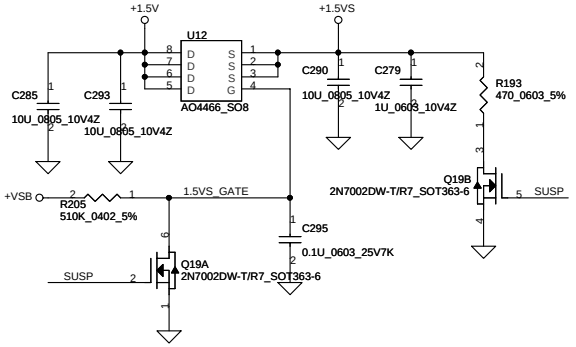


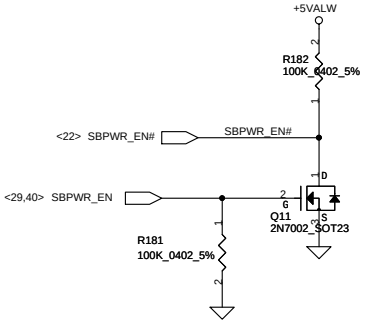
+3VALW TO +3VS

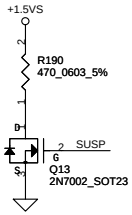


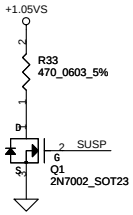


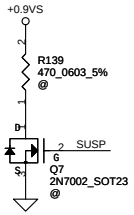
+1.5V to +1.5VS

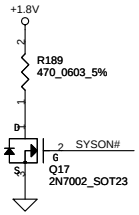


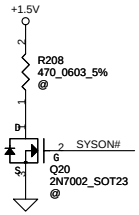












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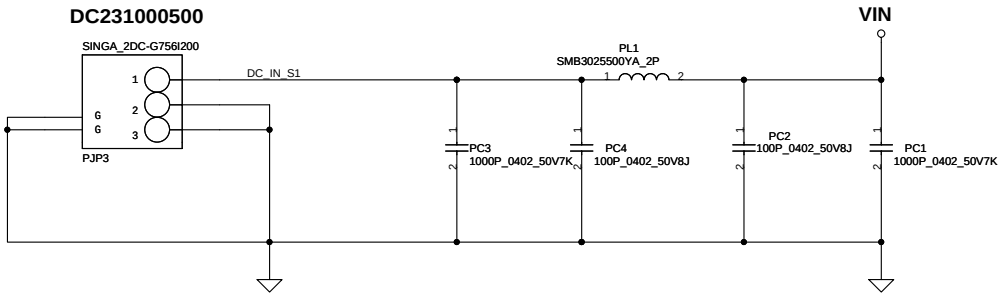
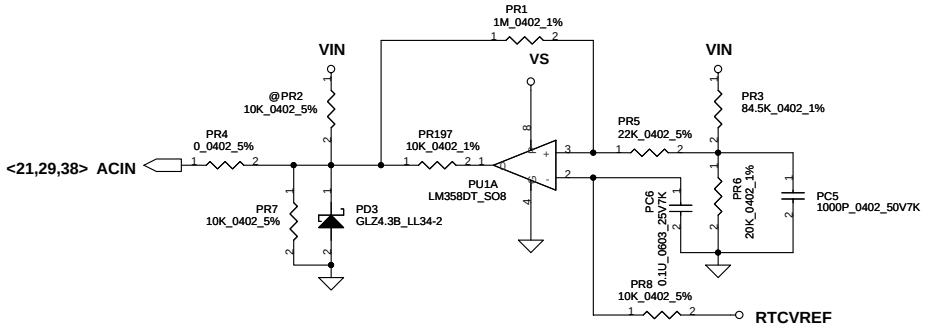
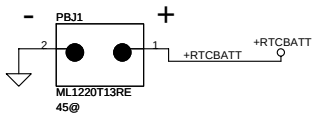
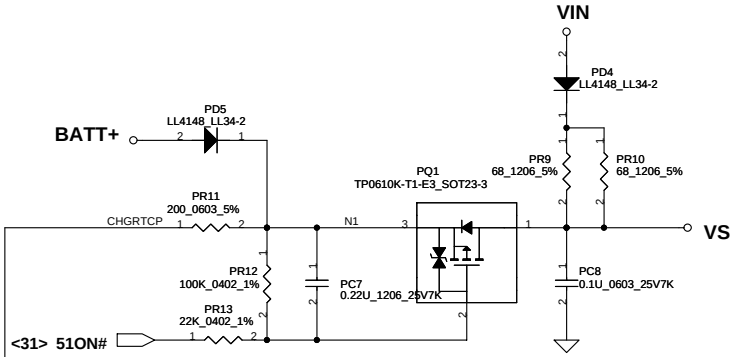


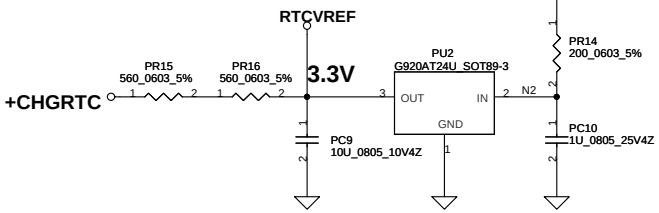


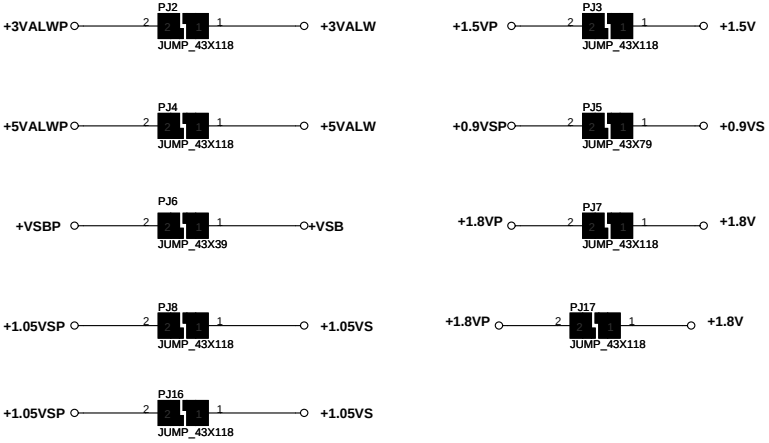


Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V







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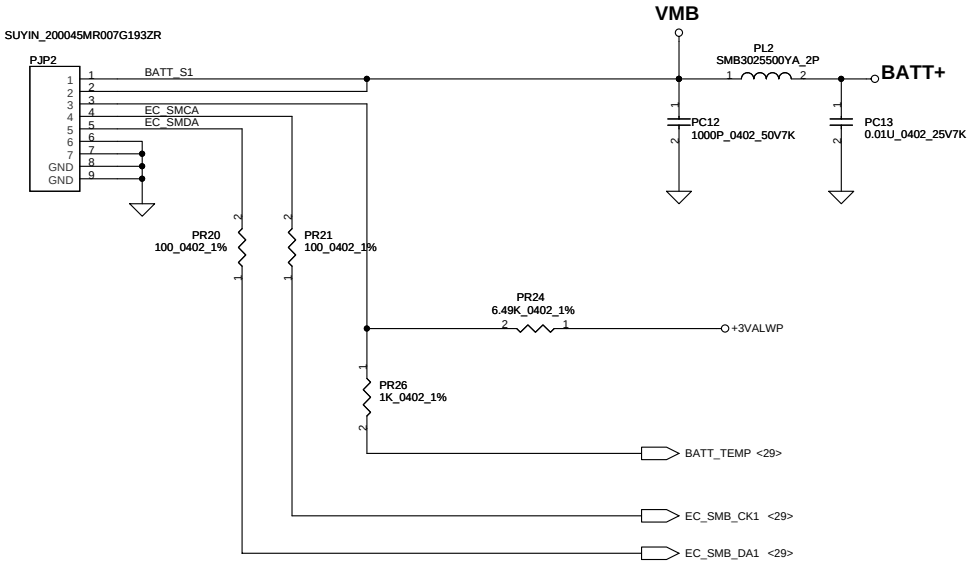
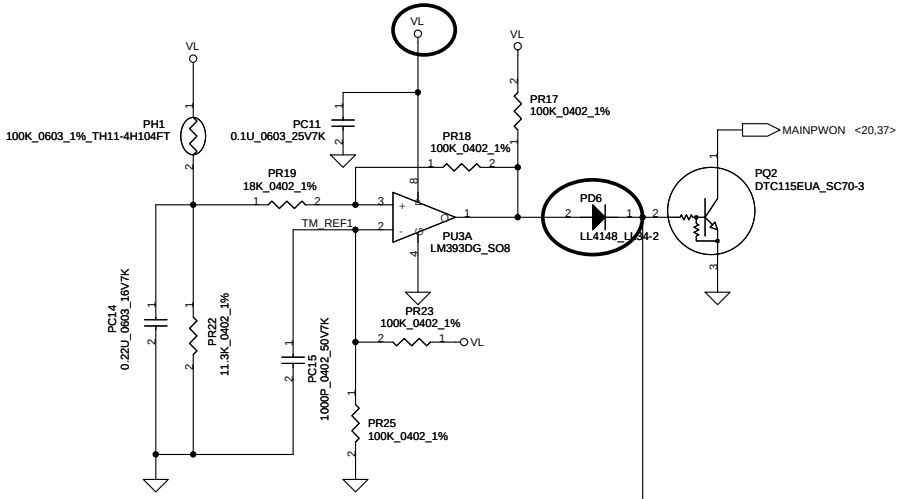
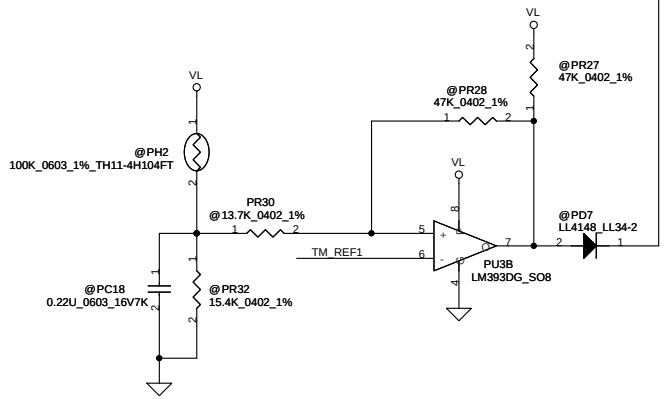
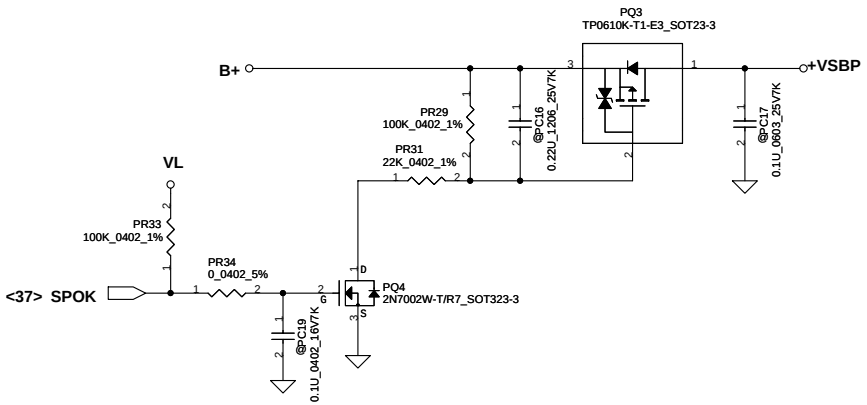
PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 70 degree C





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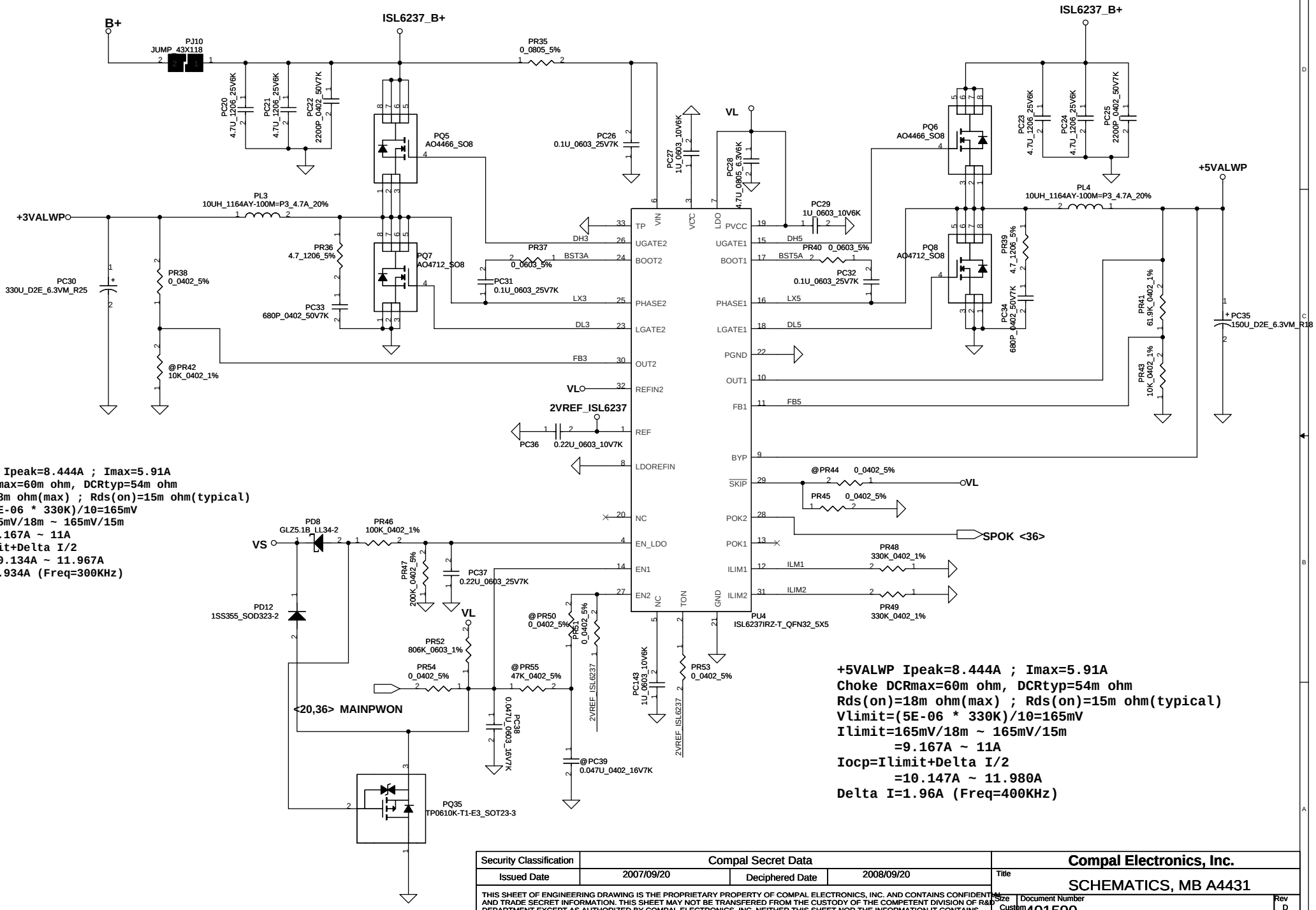

+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.134A ~ 11.967A
Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
Choke DCRmax=60m ohm, DCRtyp=54m ohm
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=10.147A ~ 11.980A
Delta I=1.96A (Freq=400KHz)

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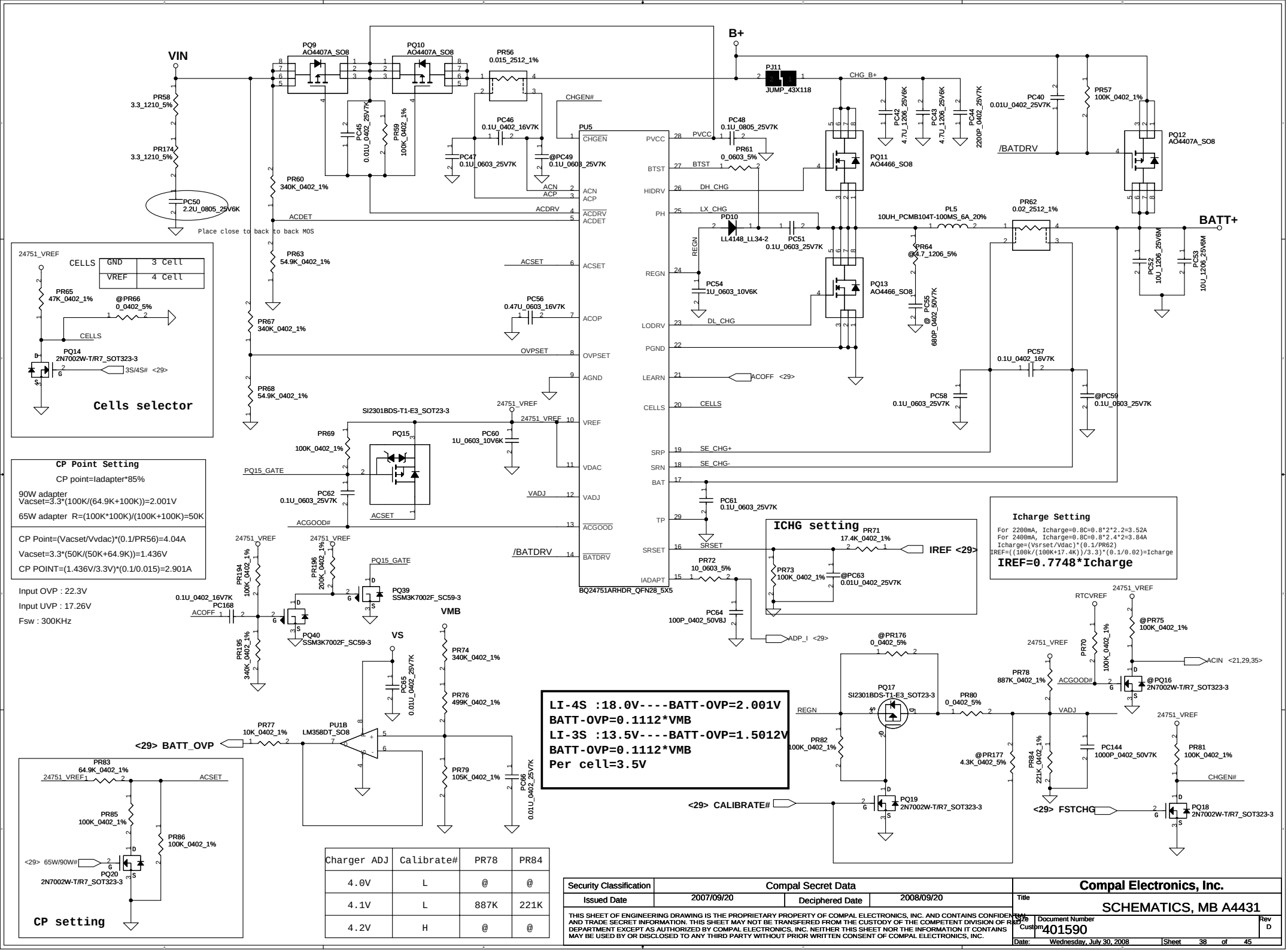

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@

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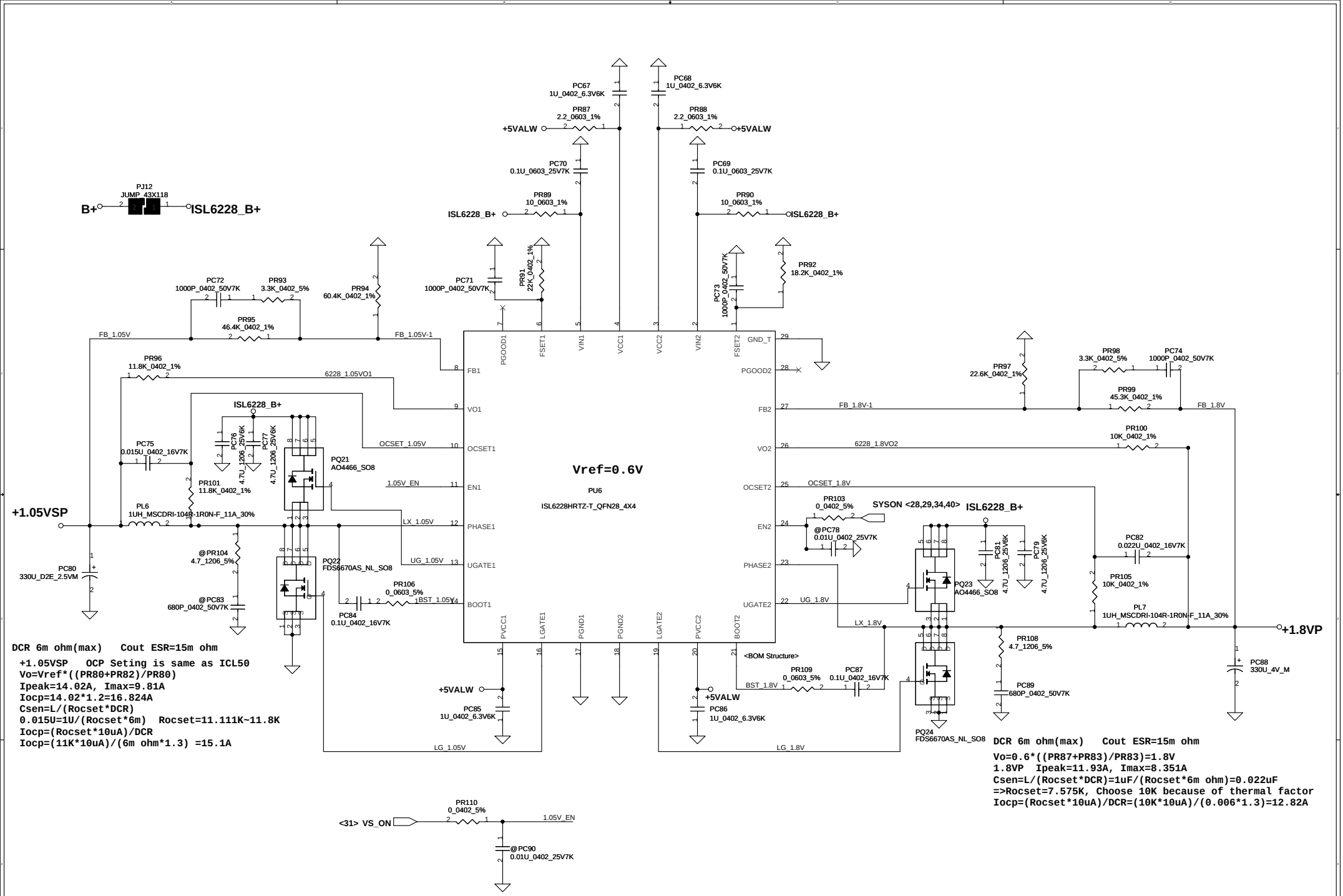

DCR 6m ohm(max) Cout ESR=15m ohm

+1.05VSP OCP Seting is same as ICL50
Vo=Vref*((PR80+PR82)/PR80)
Ipeak=14.02A, Imax=9.81A
Iocp=14.02*1.2=16.824A
Csen=L/(Rocset*DCR)
0.015U=1U/(Rocset*6m) Rocset=11.111K~11.8K
Iocp=(Rocset*10uA)/DCR
Iocp=(11K*10uA)/(6m ohm*1.3) =15.1A

DCR 6m ohm(max) Cout ESR=15m ohm

Vo=0.6*((PR87+PR83)/PR83)=1.8V
1.8VP Ipeak=11.93A, Imax=8.351A
Csen=L/(Rocset*DCR)=1uF/(Rocset*6m ohm)=0.022uF
=>Rocset=7.575K, Choose 10K because of thermal factor
Iocp=(Rocset*10uA)/DCR=(10K*10uA)/(0.006*1.3)=12.82A

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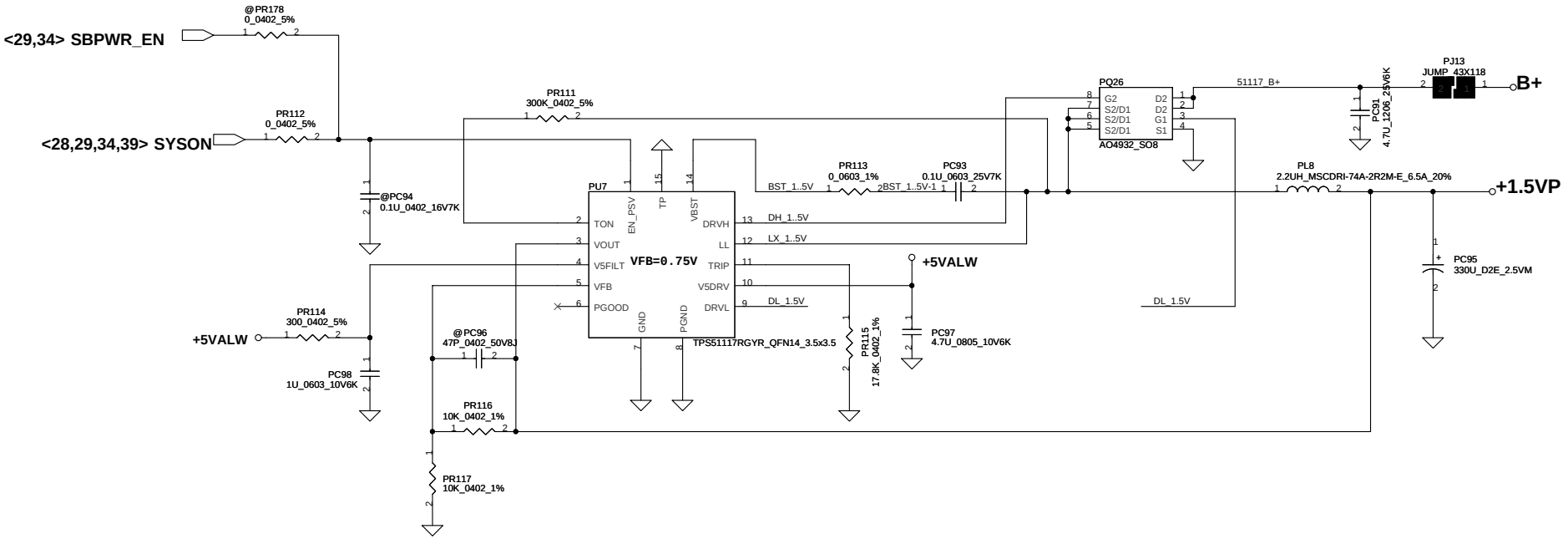

VFB=0.75V
Vo=VFB*(1+PR87/PR88)=0.75*(1+10K/10K)=1.5V
Ton=19*e-12*143000(((2/3)*Vo+100mV)/19)+50ns
=2.645e-7 us
=>Vo/Vin=D=Ton/Ts =>Ts=3.35us
Fsw=298KHz

Cout ESR=15m ohm
Ipeak=4.71A, Imax=3.297A, Iocp=5.652A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=2.107A
=>1/2DeltaI=1.053A
Vtrip=Rtrip*10uA=17.8K*10uA=0.178V
Iocpmin=Vtrip/Rdsonmax*1.2+1.053A
=0.178/(0.027*1.2)+1.053=5.493A+1.053A=6.546A
Iocpmax=(0.178/(0.021*1.1))+1.053A=7.705A+1.053A
=8.758A
Iocp=6.546A~8.758A

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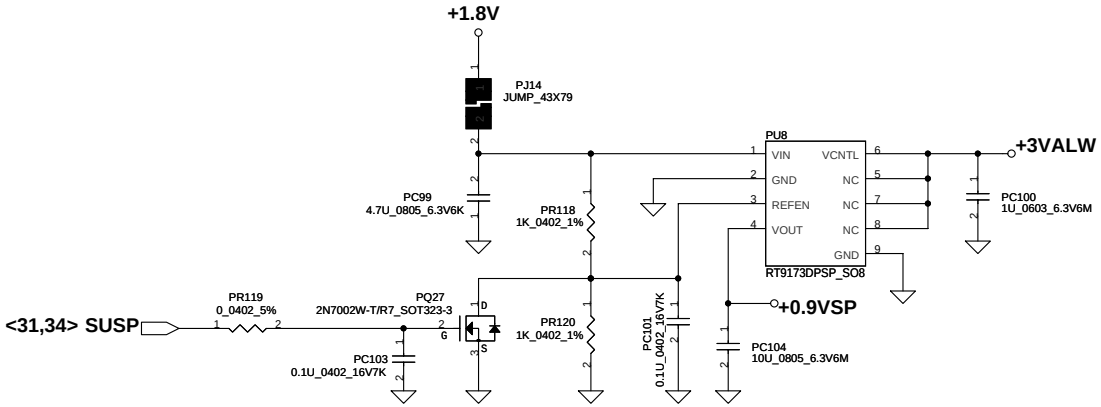

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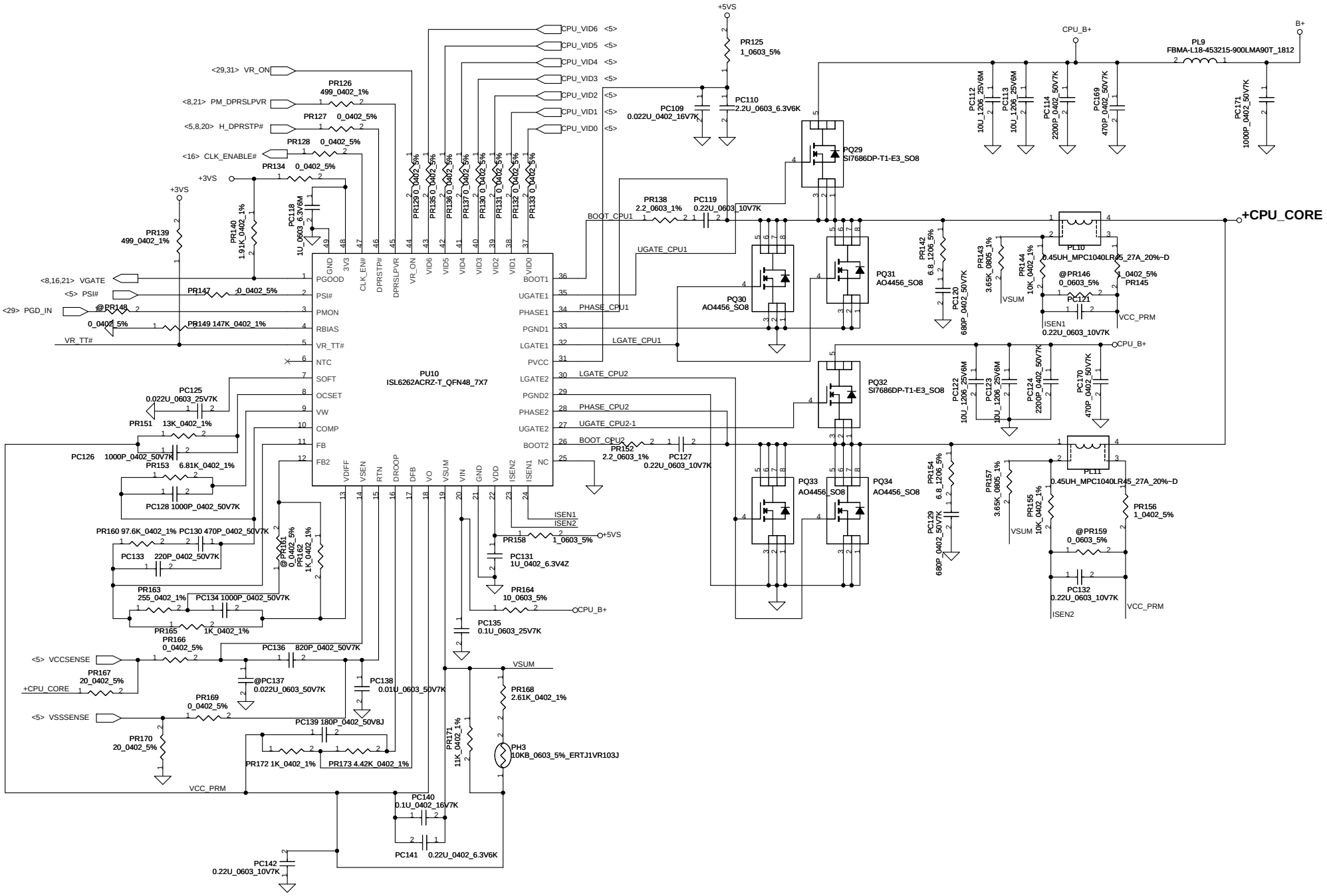

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ISL6237 can't shutdown while battery only.	ISL6237 can't shutdown while battery only.	0.1	41	Add PQ35 SB906100210 TP0610K.	20071031	EVT
2	Delete PD1	Because we can cost down and B+ has another one.	0.2	39	Delete PD1 SCSB540C080 (S SCH DIO B540C-13-F SMC)	20071115	DVT
3	Change PQ9,PQ10,PQ12 to AO4407A	Change PQ9,PQ10,PQ12 to AO4407A	0.2	38	Change PQ9,PQ10,PQ12 to AO4407A	20080509	DVT
4	Fixed ACIN signal level	Fixed ACIN signal level	0.3	37	PD2 change to PR197 10K 0402 %1	20080509	DVT
5	Fixed ACIN signal level	Fixed ACIN signal level	0.3	37	PR2 unpop	20080509	DVT
6	Fixed ACIN signal level	Fixed ACIN signal level	0.3	37	PR4 change to 0 0402 %5	20080509	DVT
7	Change PR65	Cells voltage must over 2.5V	0.4	38	PR65 change to 47K 0402 %1	20080613	PVT
8	Node of PR70 is changed	Node of PR70 is changed	0.5	38	Node of PR70_100K_0402_1% change from VREF to RTCVREF	20080620	PVT
9	Add PC89,PR108	for EMI solution	0.6	39	Add PC89:680P_0402_50V7K PR108:4.7_1206_5%	20080620	PVT
10	Add PC169,PC170 on CPUB+	for EMI solution	0.6	42	Add PC169,PC170(470P_0402_50V7K) on CPUB+	20080620	PVT
11	Add PC171 on B+	for EMI solution	0.6	42	Add PC171(1000P_0402_50V7K) on B+	20080620	PVT
12	Change PR138 ,PR152	for EMI solution	0.6	42	PR138 ,PR152 change to 2.2_0603_1%	20080620	PVT
13	Change PR95	pull up the output voltage from 1.05v to 1.06 v	0.7	39	Change PR95 from 45.3K_0402_1% to 46.4K_0402_1%	20080623	PVT
14	Change PR17,PR18,PR19,PR22	Thermal protection 90oC & Recovery at 70oC	0.8	36	Change PR17 and PR18 to 100K_0402_1% Change PR19 to 18K_0402_1% and PR22 to 11.3K_0402_1%	20080701	PVT
15							
16							
17							
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A --> B Change List

4/24
<Page 22>
-R57、R133 10ohm change to 100ohm
-C135、C204 0.1u change to 1u
for ICH9 USB1.1 issue
<Page 33>
-R551、R552、R553、R554 75ohm change to 1K
for Audio ESD protection

4/30
-Update Power SCH
<Page 4>
-Add R27、C427
for +5VS drop issue
-R541 pull high 3.3V
<Page 33>
-R486、R477 75ohm change to 56.2ohm
for AUDIO D-A HP FSOV

5/2
-Bluetooth USBP5P/5N change to USBP7P/7N

5/5
-Modify LED test value
-Add 51@、NC@、GL@

5/6
-Update Power SCH
<Page 25>
-R290 change to L47(SM010014520)
for EMI

5/7
-add BT@、GM@

B --> C Change List

6/25
<Page 16>
-C301、C296 33p change to 27p
for RTC issue

C --> Pre MP Change List

7/14
<Page 16>
-U31 SA00002Q830(QU37) change SA00002Q810(QU56)

7/28
-update Power SCH

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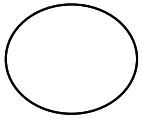
ZZZ



PCB KAWE0 LA-4431P LS-4391P/4392P/4393P

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