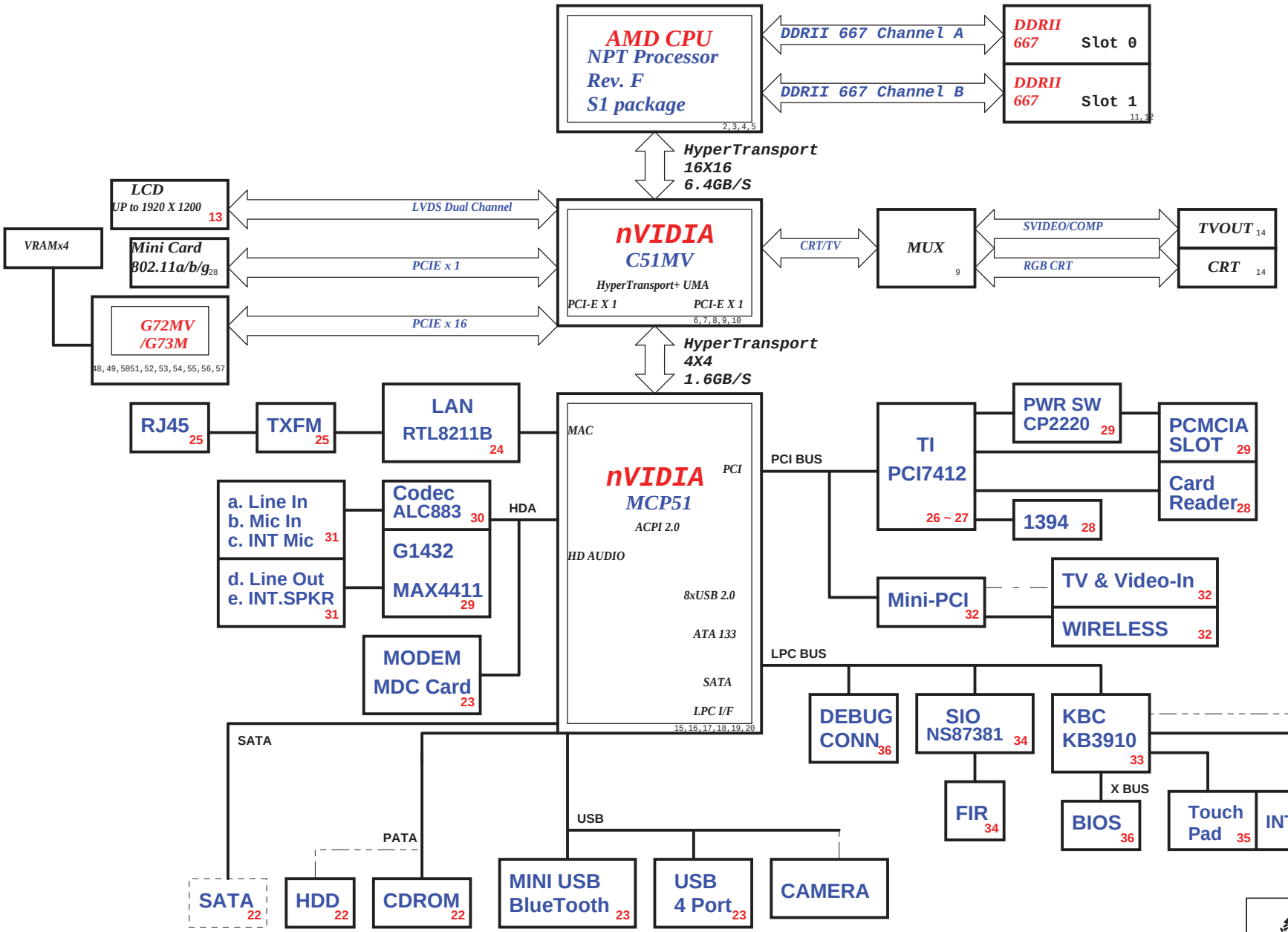
MYALL M Block Diagram

Project Code: 91.4Q901.001
Project Name: MYALL M
PCB Number: 06211-SA



SYSTEM DC/DC MAX8734A	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D2V_HT_S0 1D2V_CORE_S0

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8760	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 1.35V 35A

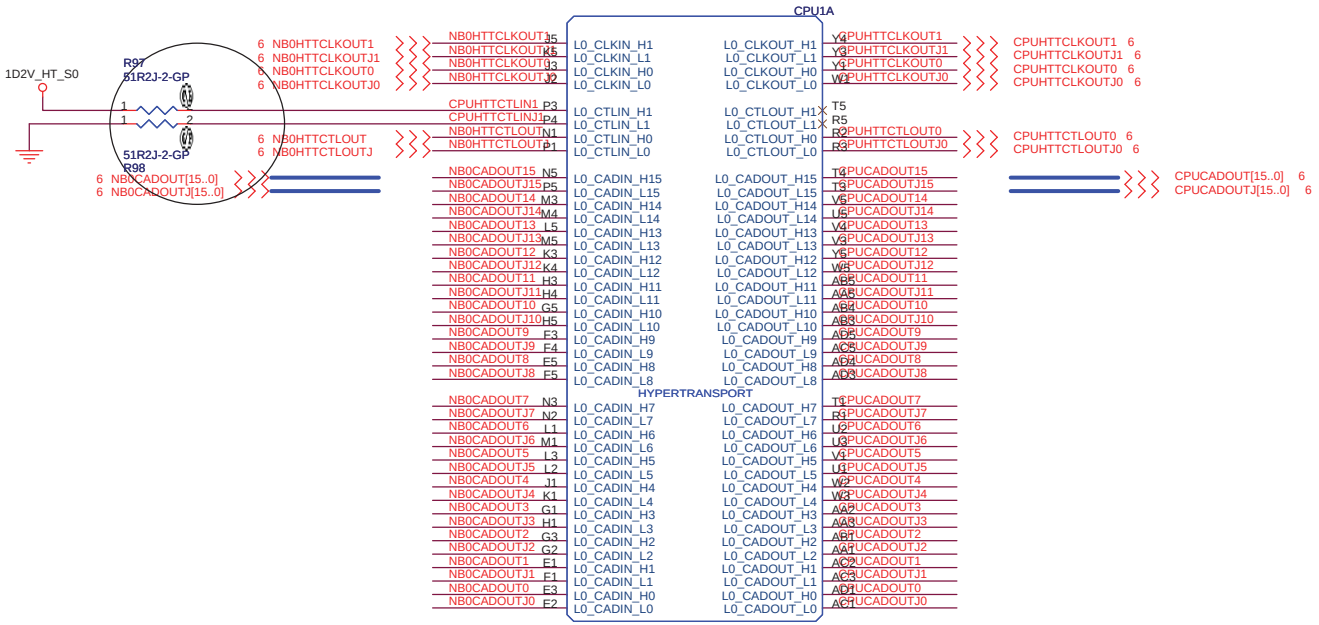
PCB LAYER
L1:SIGNAL 1
L2:GND
L3:SIGNAL 2
L4:SIGNAL 3
L5:VCC
L6:SIGNAL 4

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size	Document Number	Rev
Custom	MYALL M	SA

Date: Friday, June 16, 2006 Sheet 1 of 59



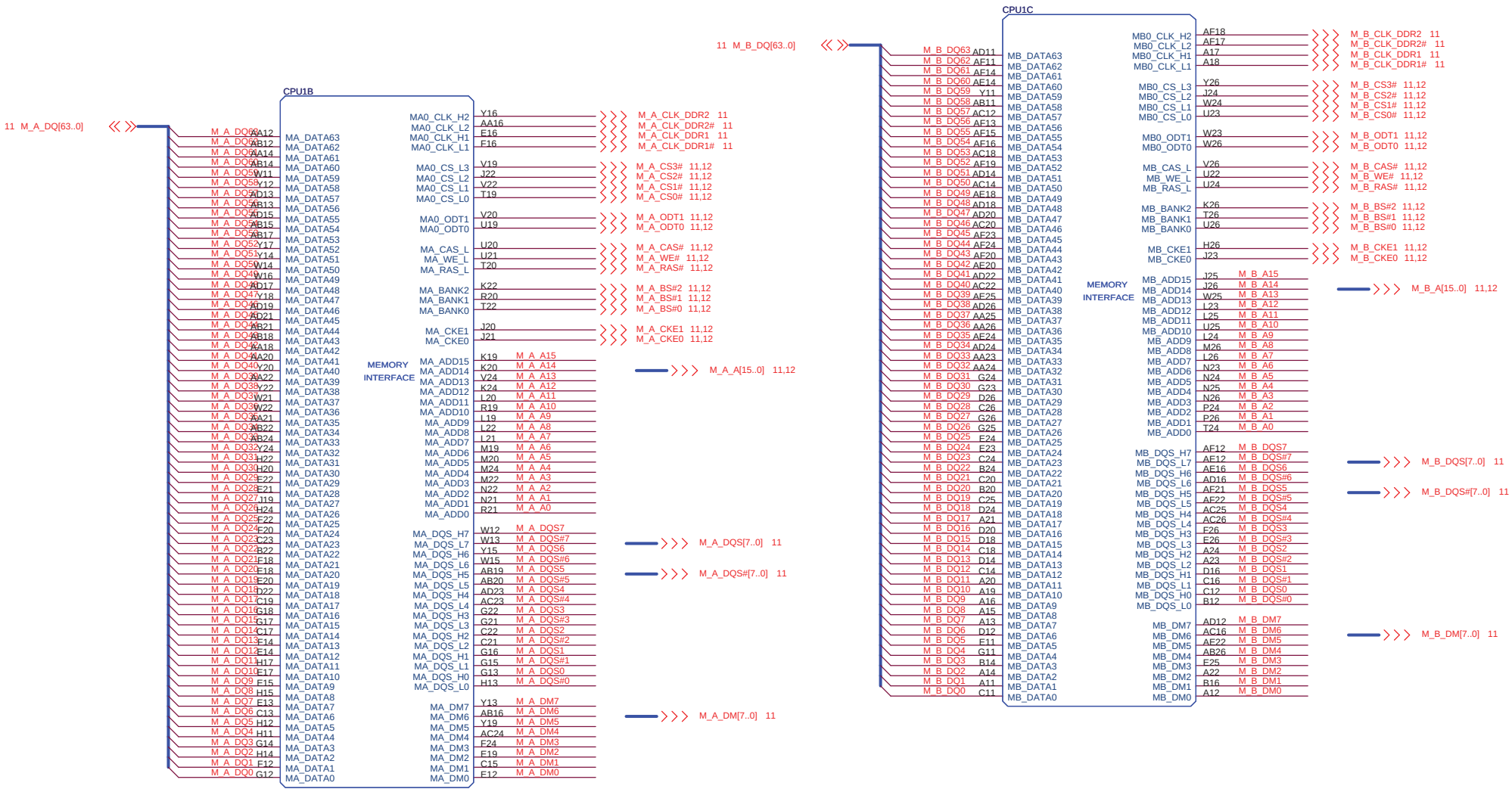
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(1/4) HT

Size: A3 | Document Number: MYALL M | Rev: SA

Date: Friday, June 16, 2006 | Sheet 2 of 59



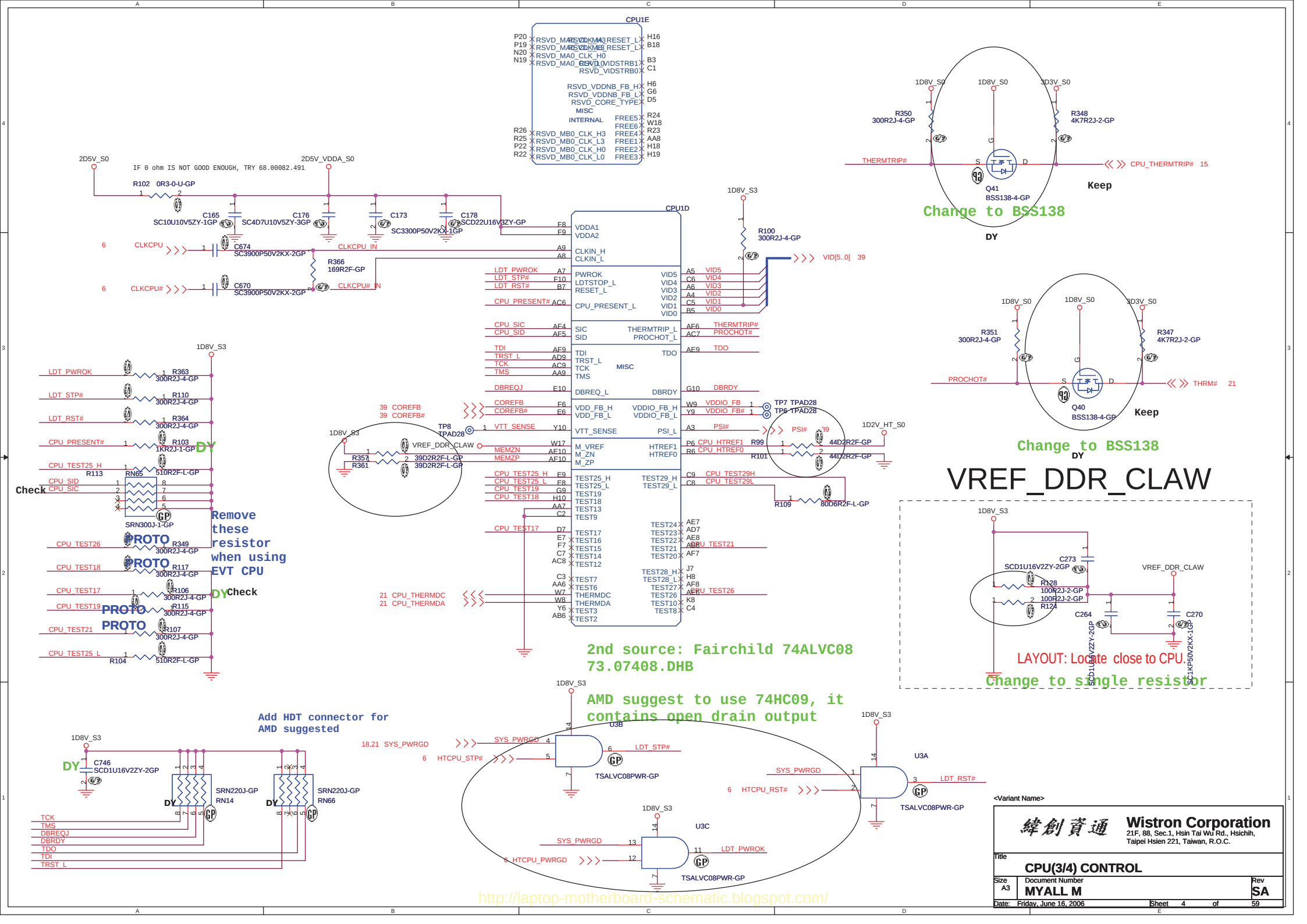
<Variant Name>

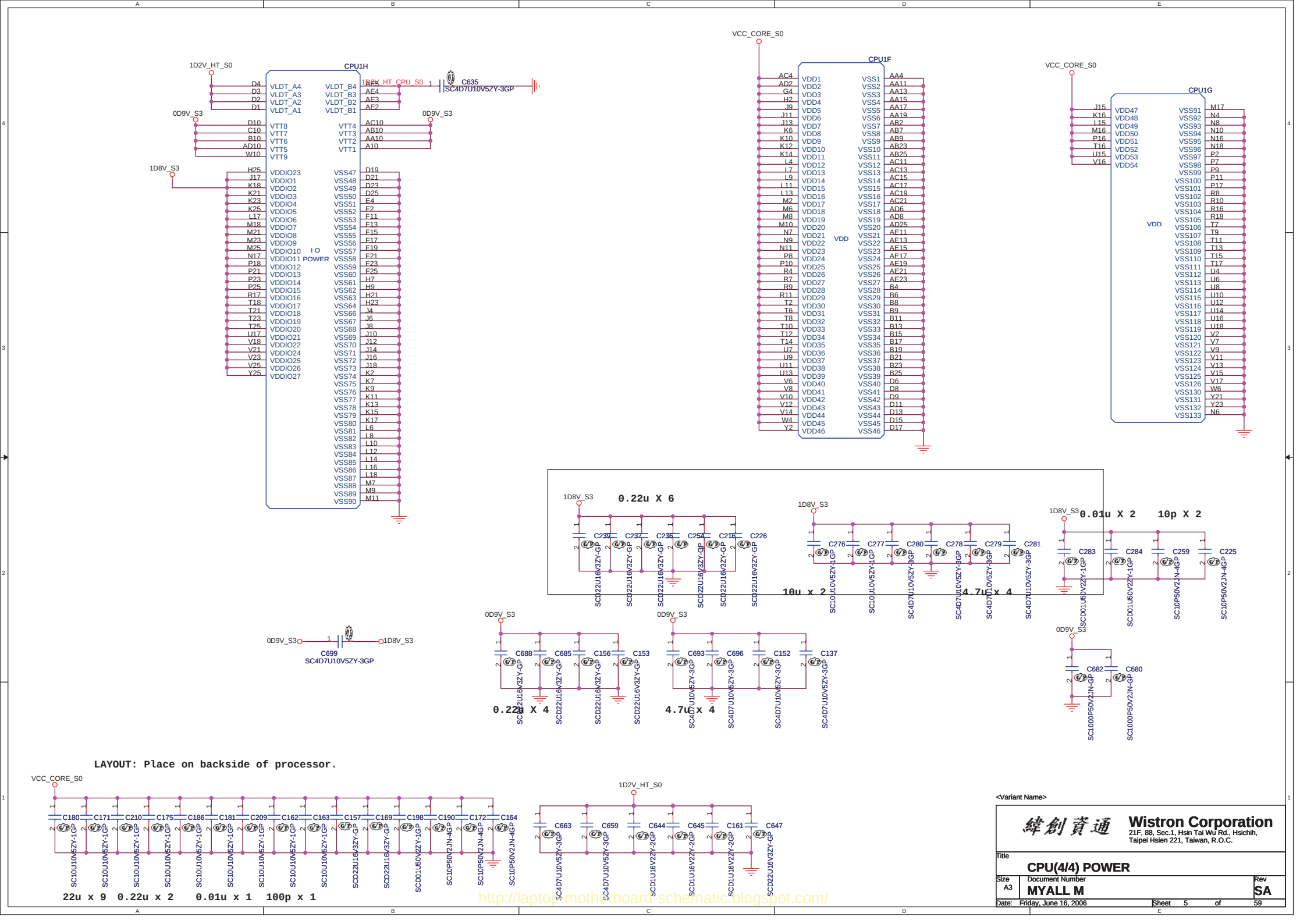
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

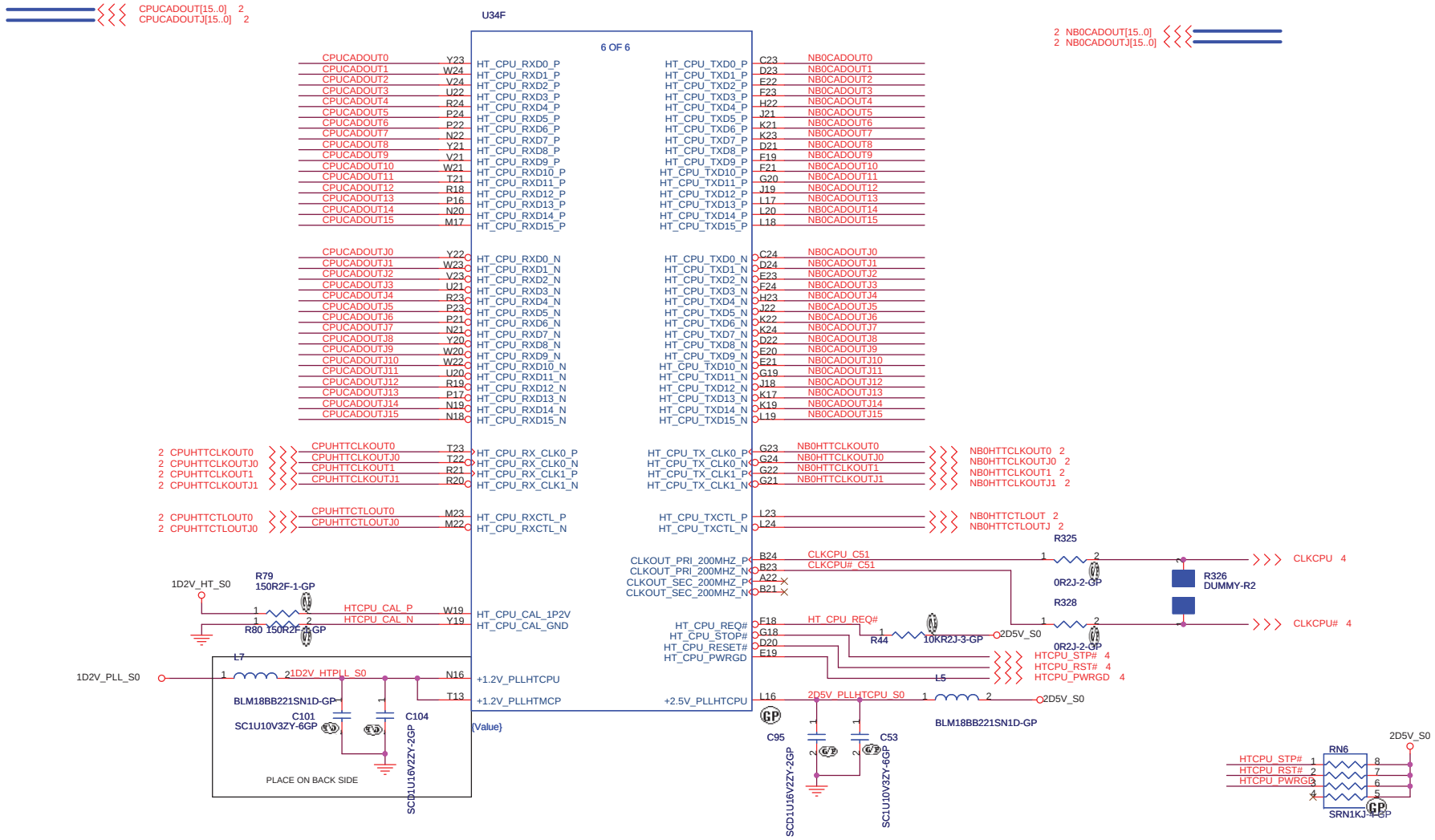
Title: CPU(2/4) DDR II

Size	Document Number	Rev
A3	MYALL M	SA

Date: Friday, June 16, 2006 Sheet 3 of 59


CPU1E
CPU1D
IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491
2D5V_S0
2D5V_VDDA_S0
1D8V_S3
R102 0R3-0-U-GP
C165 SC10U10V5ZY-1GP
C4D7U10V5ZY-3GP
C173 SC3300P50V2KX-1GP
C178 SCD22U16V3ZY-GP
C674 SC3900P50V2KX-2GP
C670 SC3900P50V2KX-2GP
R366 169R2F-GP
CLKCPU
CLKCPU#
CLKCPU_IN
CLKCPU#_IN
R100 300R2J-4-GP
VID[5..0] 39
LDT_PWROK
LDT_STP#
LDT_RST#
CPU_PRESENT#
CPU_SIC
CPU_SID
TDI
TRST_L
TCK
TMS
DBREQJ
DBRDY
COREFB
COREFB#
VTT_SENSE
MEMZN
MEMZP
VREF_DDR_CLAW
R357 39D2R2F-L-GP
R361 39D2R2F-L-GP
TP8 TPAD28
TP7 TPAD28
TP6 TPAD28
VDDIO_FB
VDDIO_FB#
PSI#
R99 44D2R2F-GP
R101 44D2R2F-GP
1D2V_HT_S0
CPU_HTREF1
CPU_HTREF0
R109 80D6R2F-L-GP
CPU_TEST25_H
CPU_TEST25_L
CPU_TEST19
CPU_TEST18
CPU_TEST17
CPU_TEST29H
CPU_TEST29L
CPU_TEST21
CPU_TEST26
21 CPU_THERMDC
21 CPU_THERMDA
R363 300R2J-4-GP
R110 300R2J-4-GP
R364 300R2J-4-GP
R103 1KR2J-1-GP
R113 510R2F-L-GP
RN65 SRN300J-1-GP
R349 300R2J-4-GP
R117 300R2J-4-GP
R106 300R2J-4-GP
R115 300R2J-4-GP
R107 300R2J-4-GP
R104 510R2F-L-GP
DY
Check
PROTO
Remove these resistor when using EVT CPU
2nd source: Fairchild 74ALVC08
73.07408.DHB
AMD suggest to use 74HC09, it contains open drain output
Add HDT connector for AMD suggested
C746 SCD1U16V2ZY-2GP
SRN220J-GP RN14
SRN220J-GP RN66
TCK
TMS
DBREQJ
DBRDY
TDO
TDI
TRST_L
18,21 SYS_PWRGD
6 HTCPU_STP#
6 HTCPU_RST#
6 HTCPU_PWRGD
LDT_STP#
LDT_RST#
LDT_PWROK
U3B
U3A
U3C
TSALVC08PWR-GP
R350 300R2J-4-GP
R348 4K7R2J-2-GP
Q41 BSS138-4-GP
THERMTRIP#
CPU_THERMTRIP# 15
Keep
Change to BSS138
R351 300R2J-4-GP
R347 4K7R2J-2-GP
Q40 BSS138-4-GP
PROCHOT#
THRM# 21
VREF_DDR_CLAW
C273 SCD1U16V2ZY-2GP
R128 100R2J-2-GP
R124 100R2J-2-GP
C264
C270
LAYOUT: Locate close to CPU.
Change to single resistor
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU(3/4) CONTROL
Size A3
Document Number MYALL M
Rev SA
Date: Friday, June 16, 2006
Sheet 4 of 59
http://laptop-motherboard-schematic.blogspot.com/





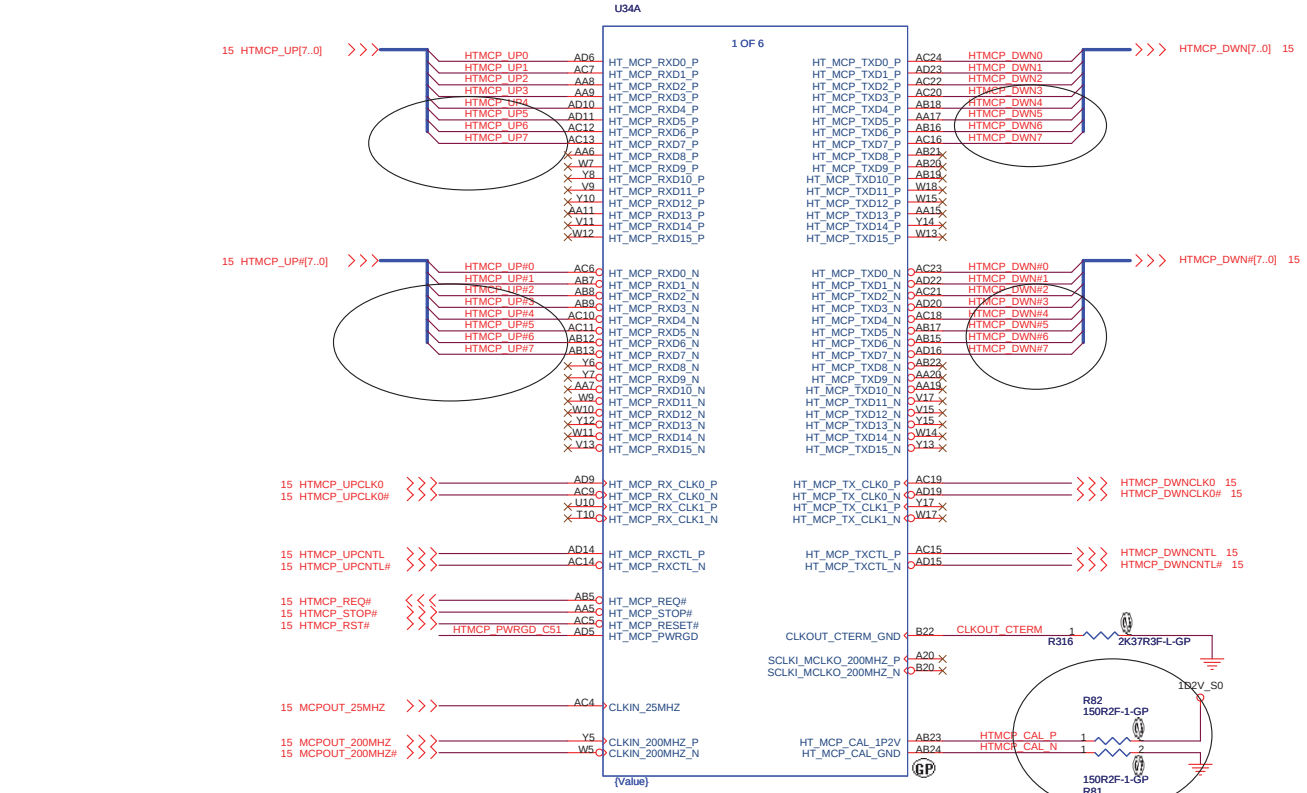
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: C51M(1/5) HT CPU

Size	Document Number	Rev
A3	MYALL M	SA

Date: Friday, June 16, 2006 Sheet 6 of 59



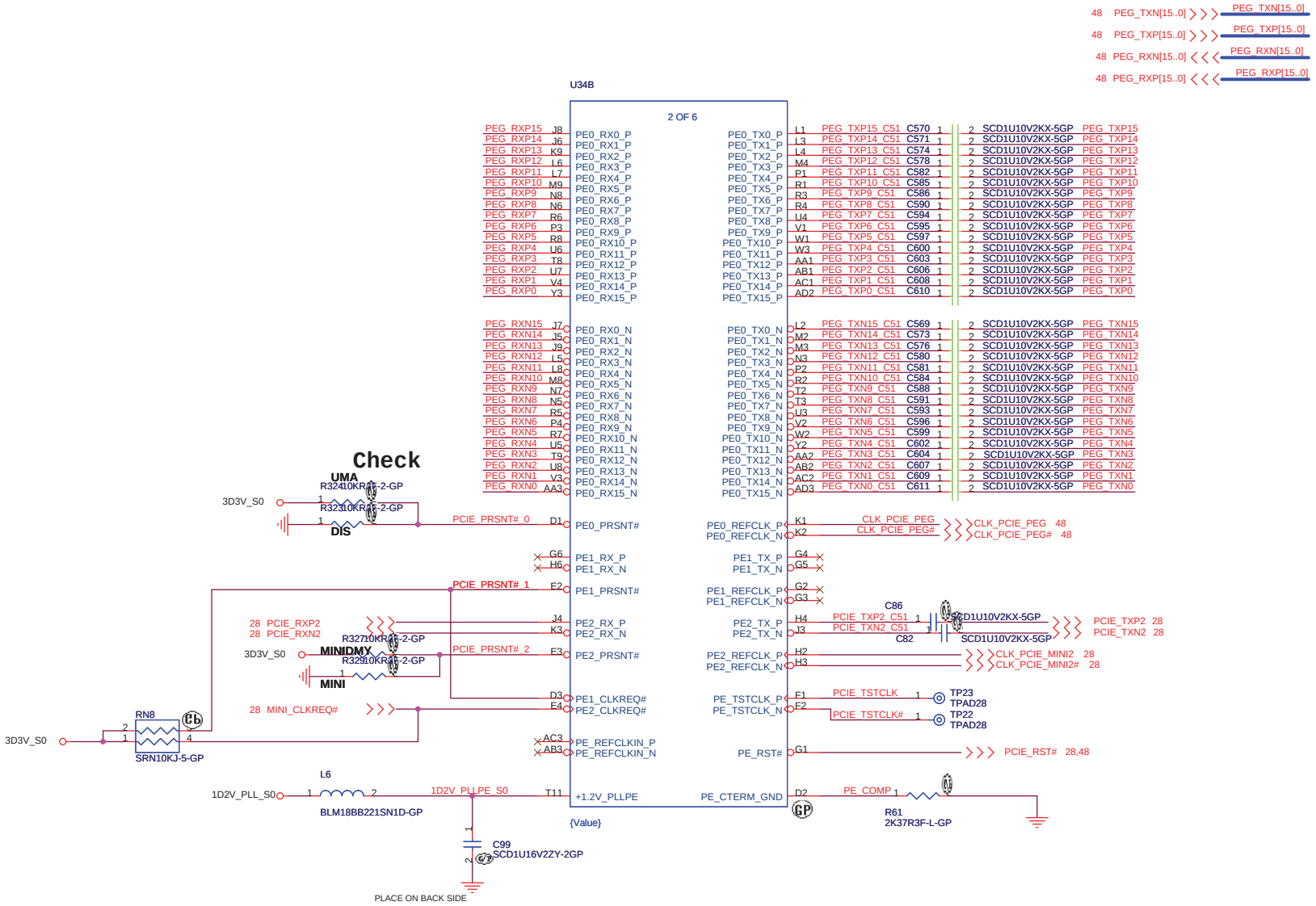
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: C51M(2/5)HT MCP

Size: Custom | Document Number: MYALL M | Rev: SA

Date: Friday, June 16, 2006 | Sheet 7 of 59



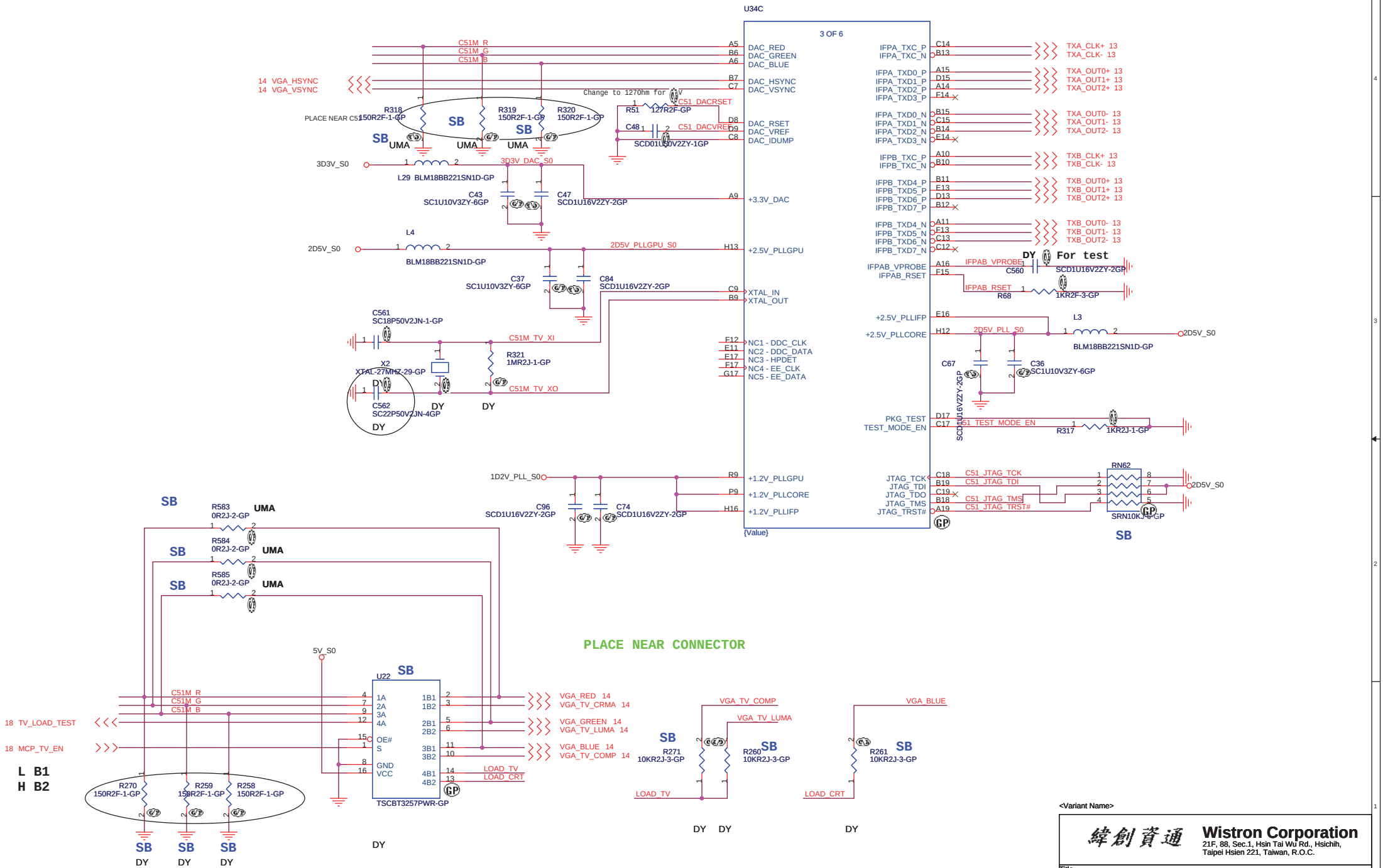
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: C51M(3/5)PCIE

Size: A3 | Document Number: MYALL M | Rev: SA

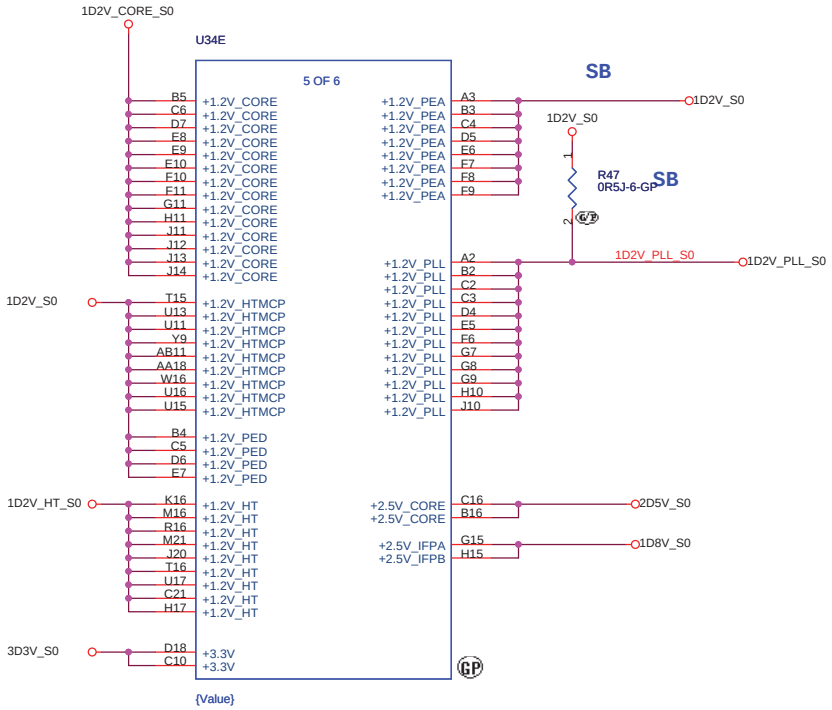
Date: Friday, June 16, 2006 | Sheet 8 of 59

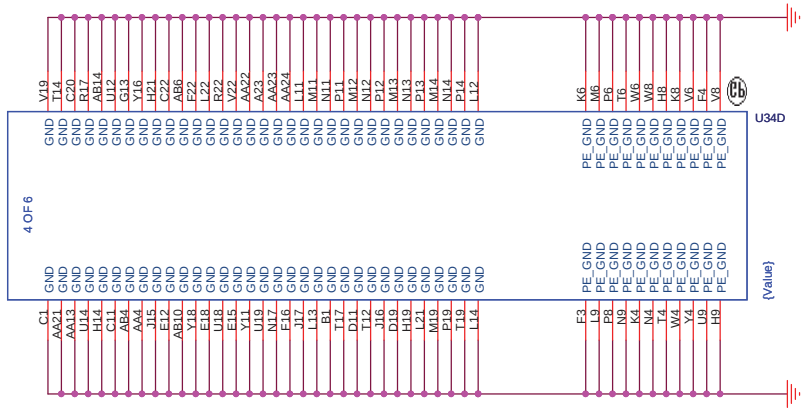


<Variant Name>

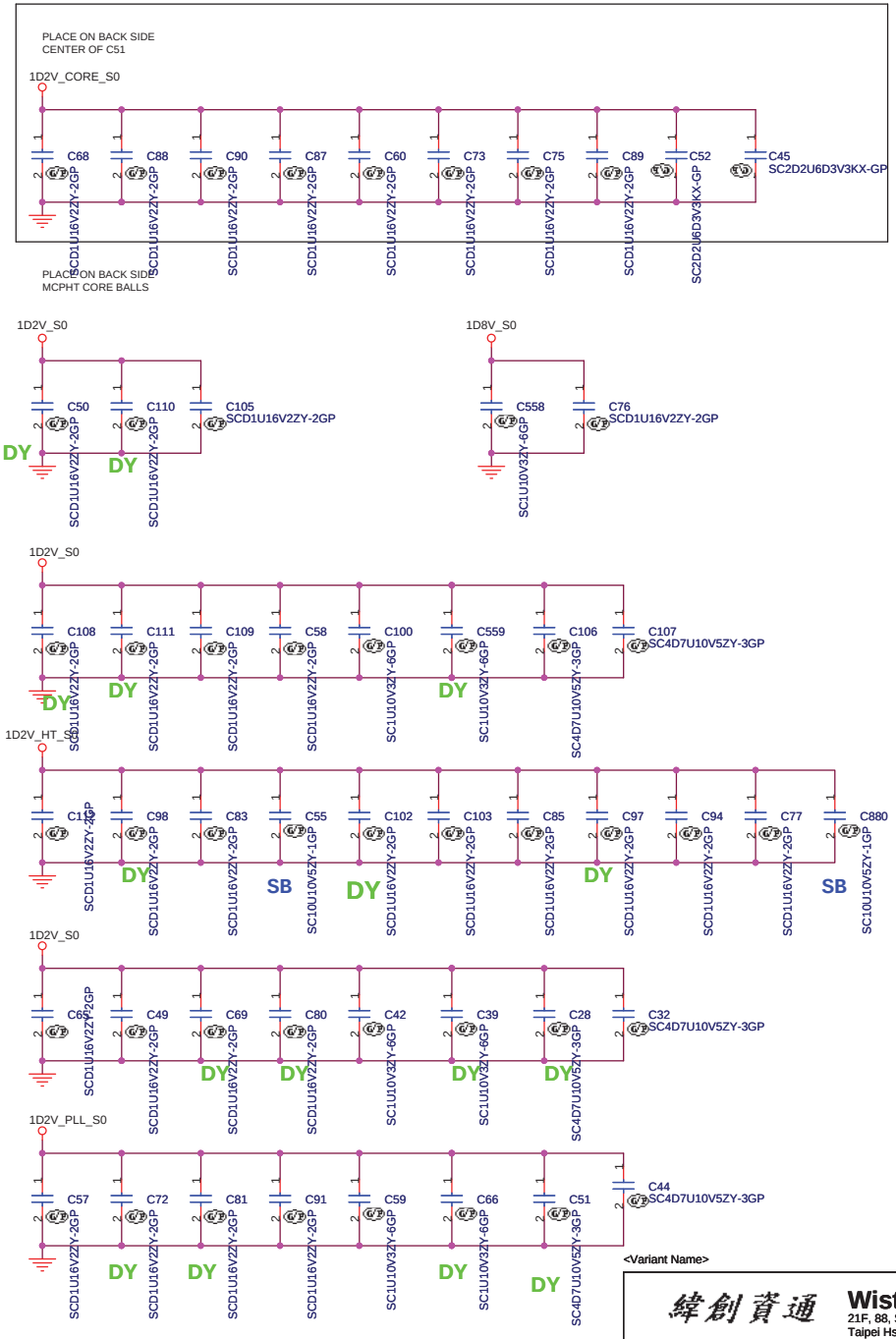
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: C51M(4/5)CRT/LVDS
Size: A3
Document Number: MYALL M
Rev: SA
Date: Friday, June 16, 2006
Sheet 9 of 59





C51 DECOUPLING



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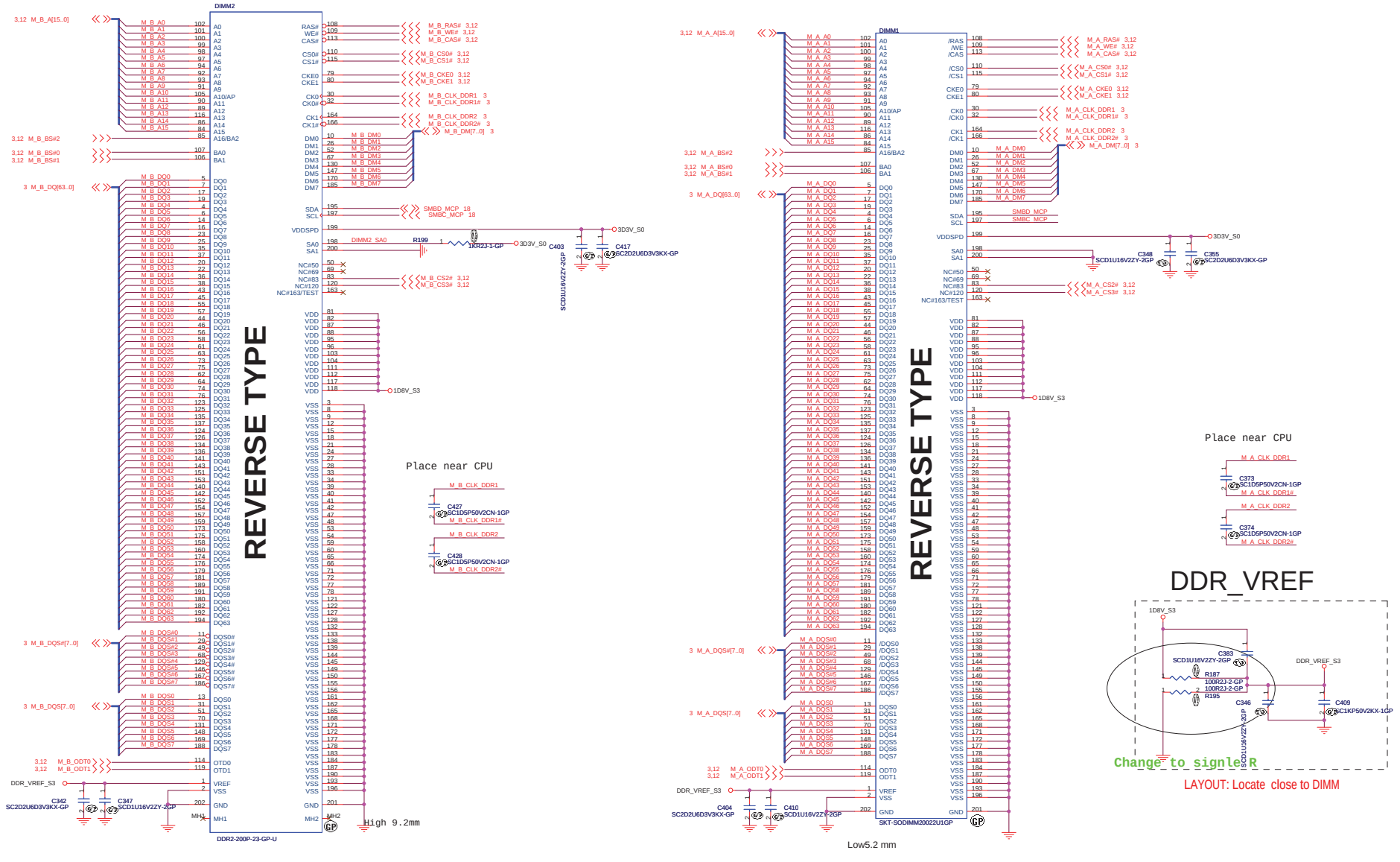
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**C51M(5/5)POWER**	
Size A3	Document Number **MYALL M**	Rev **SA**
Date: Friday, June 16, 2006	Sheet 10 of 59	



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

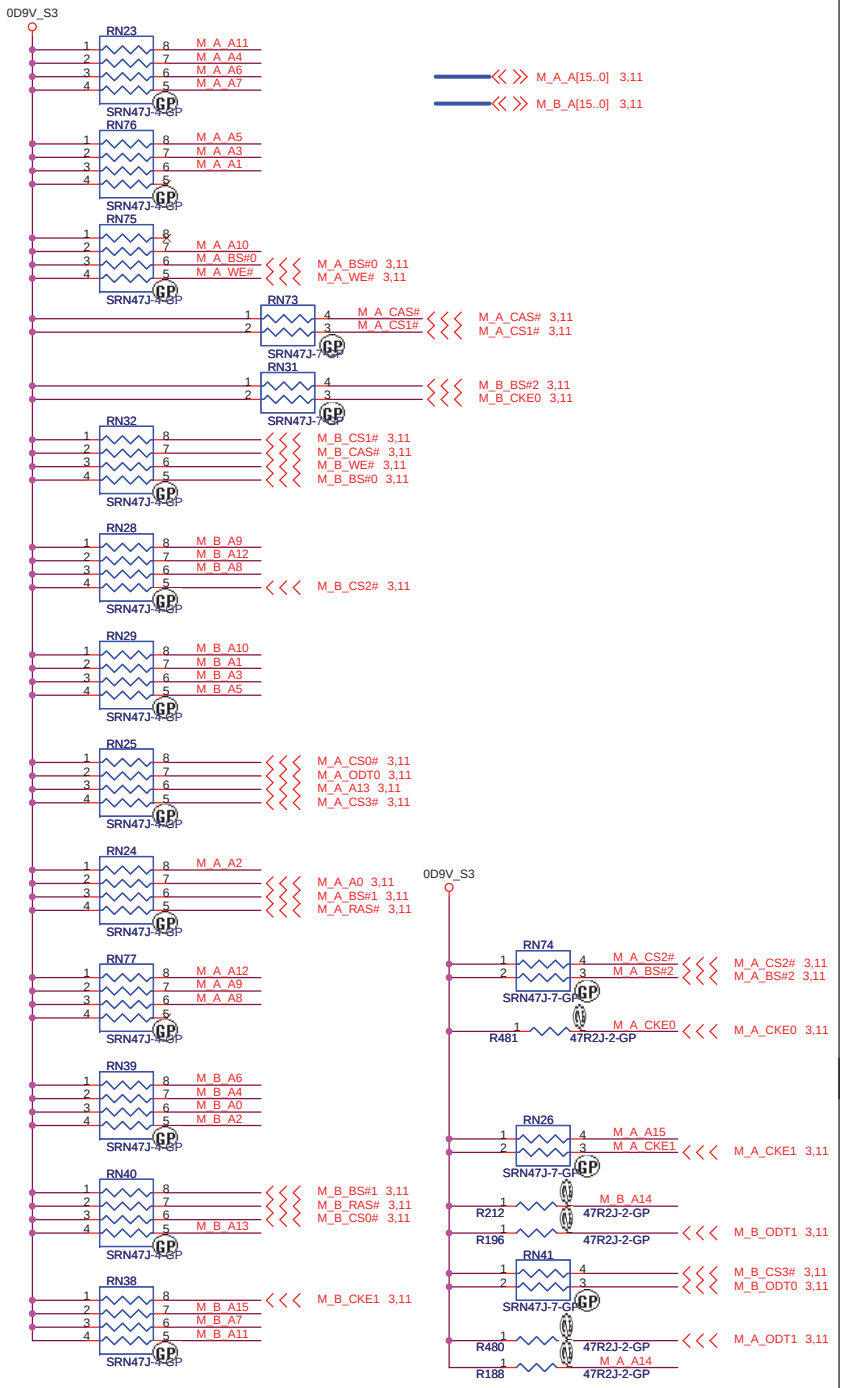
Title: DDR2-SOCKET

Size: A2 | Document Number: MYALL M | Rev: SA

Date: Friday, June 16, 2006 | Sheet 11 of 59

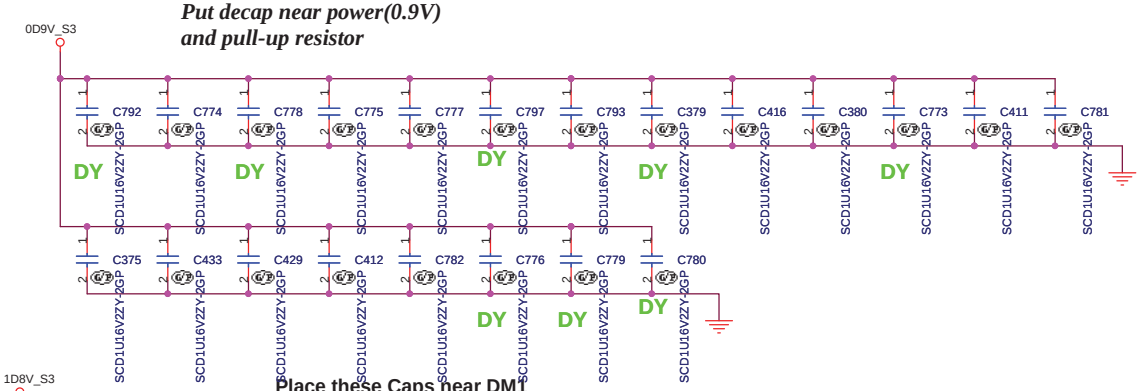
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

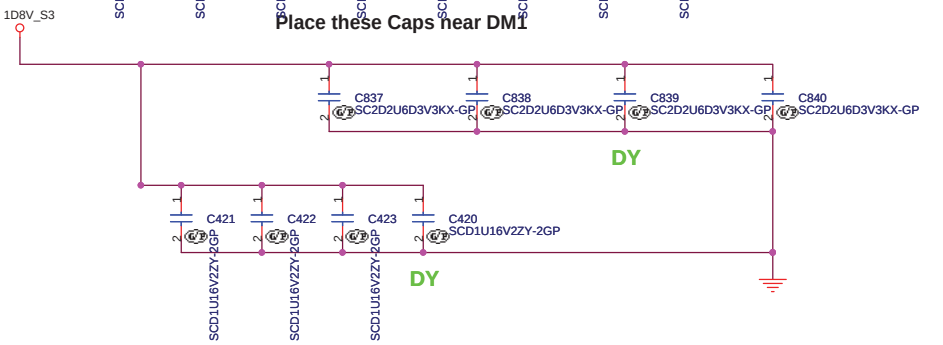


Decoupling Capacitor

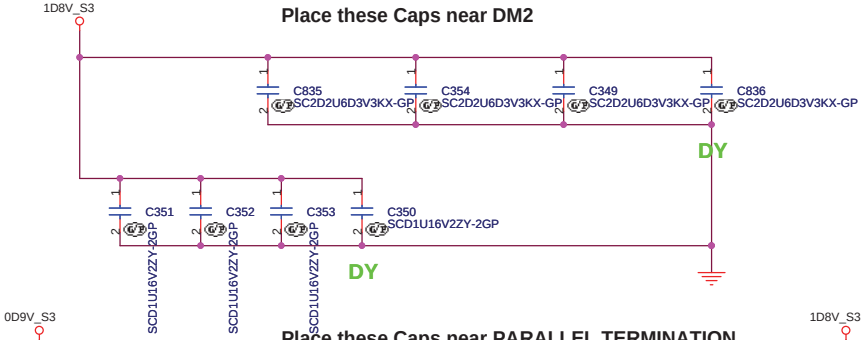
Put decap near power(0.9V) and pull-up resistor



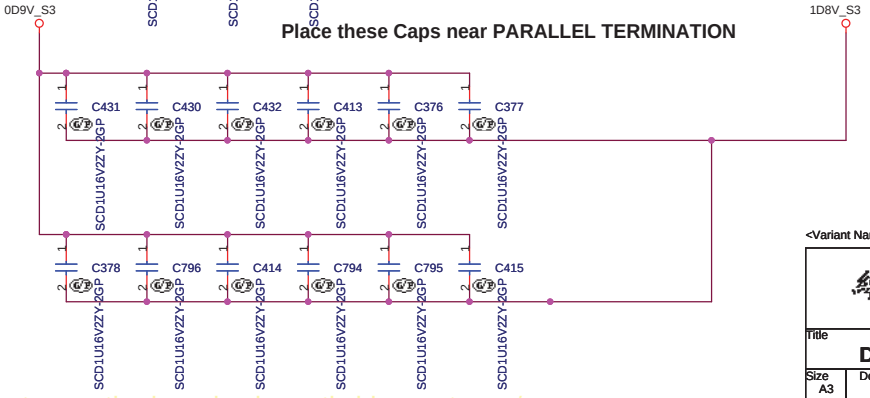
Place these Caps near DM1



Place these Caps near DM2



Place these Caps near PARALLEL TERMINATION



<Variant Name>

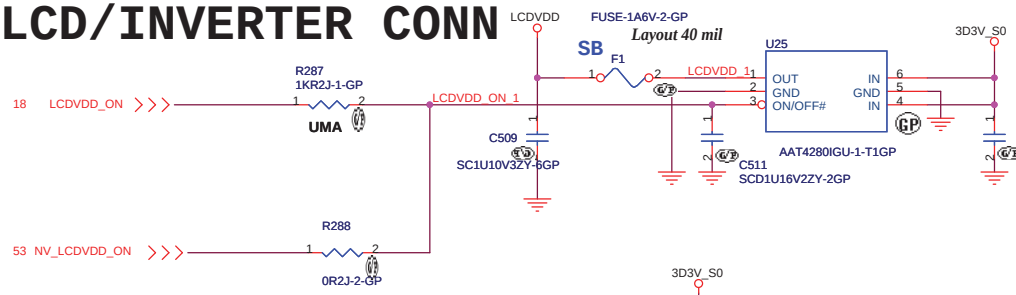
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2-RESISTOR

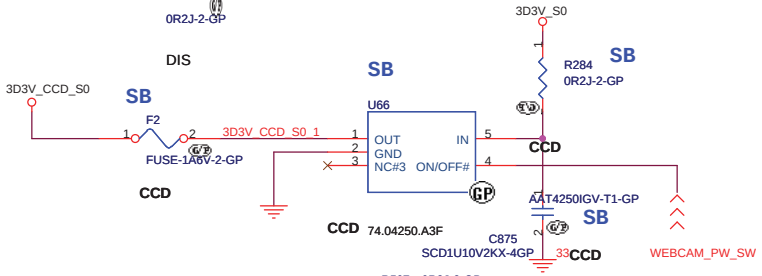
Size: A3 | Document Number: MYALL M | Rev: SA

Date: Friday, June 16, 2006 | Sheet 12 of 59

LCD/INVERTER CONN

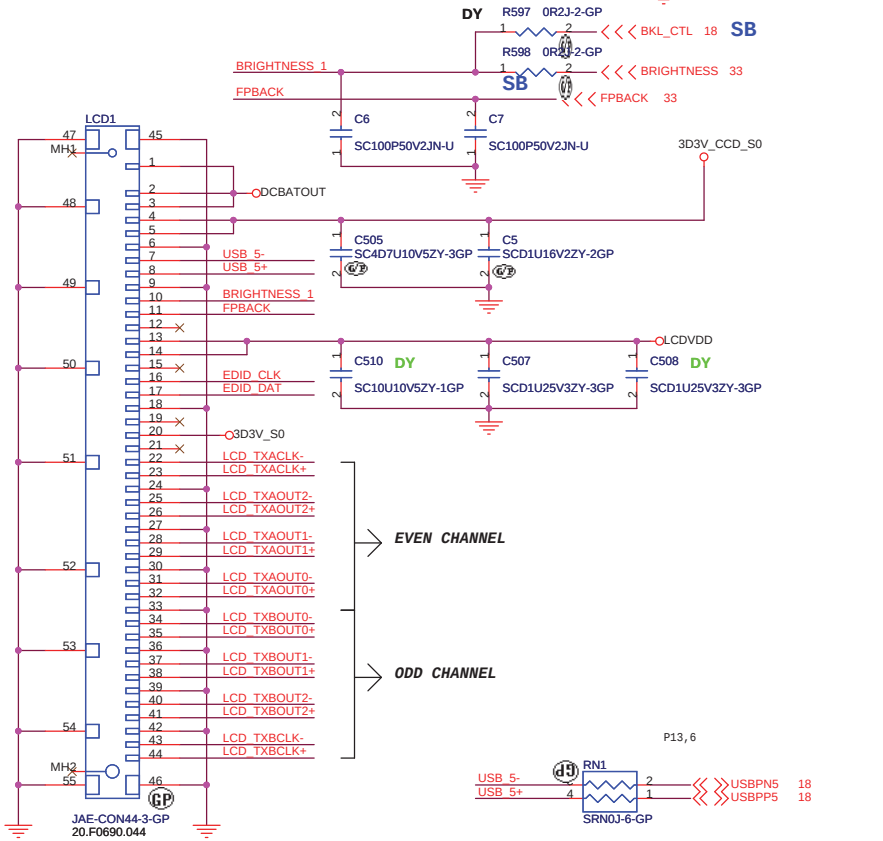


DIS

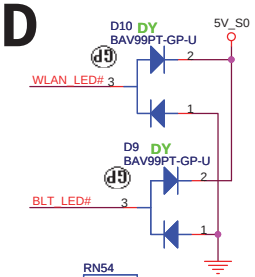


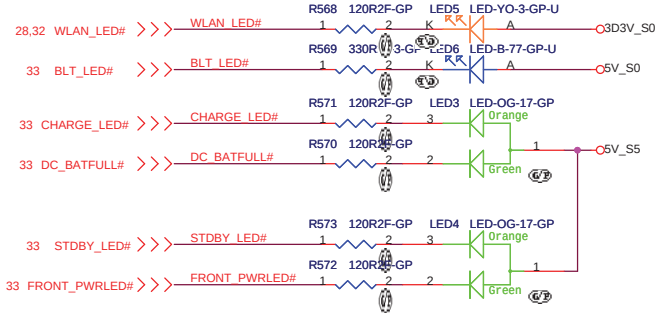
CCD

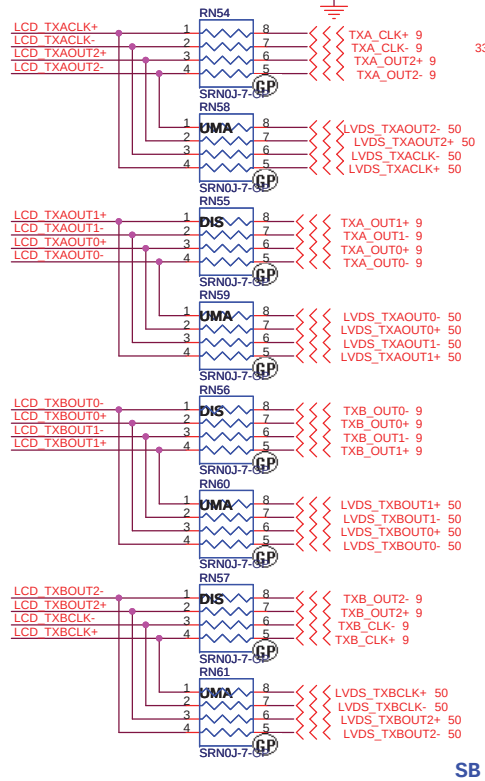
CCD 74.04250.A3F



LED







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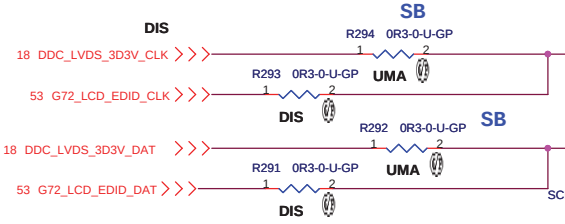
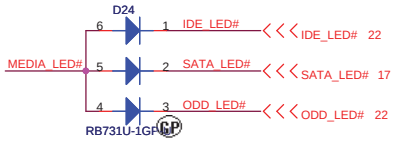
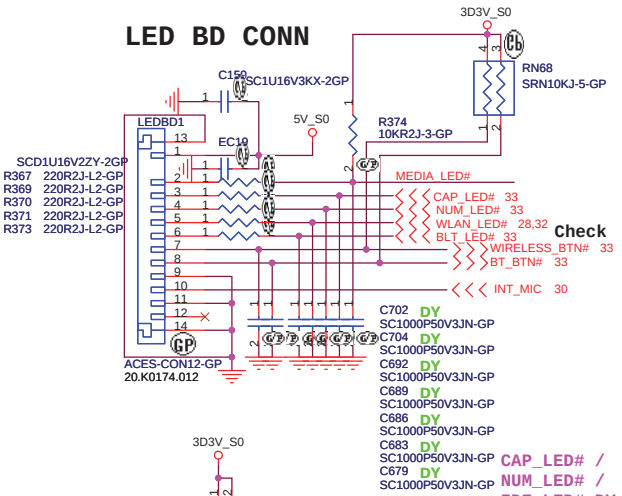
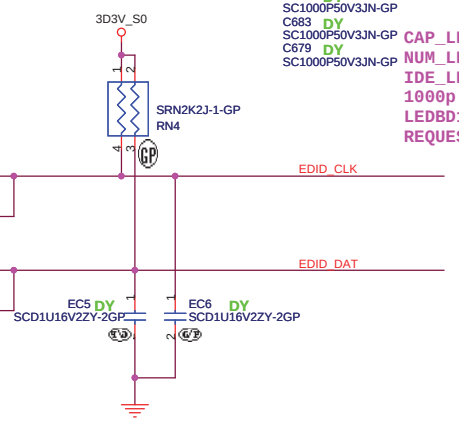




LED BD CONN



CAP_LED# / NUM_LED# / IDE_LED# DY 1000p near LEDBD1 BY EMI REQUEST



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & LED

Size | Document Number: MYALL M | Rev: SA

Date: Friday, June 16, 2006 | Sheet 13 of 59

CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

CRT_RED, VGA_RED, CRT_GREEN, VGA_GREEN, CRT_BLUE, VGA_BLUE
R274, R266, R273, R265, R272, R264 — DIS / UMA — 0R2J-2-GP
R580, R581, R582 — 150R2F-1-GP
C500 — SC10P50V2JN-4GP
C499 — SC10P50V2JN-4GP
C498 — SC10P50V2JN-4GP
RED L24, GREEN L23, BLUE L22 — IND-68NH-1-GP
C485, C484, C483 — SC2P50V2CN-GP
CRT_R, CRT_G, CRT_B
SB SB SB
DY DY DY

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT1
VIDEO-15-21-U3-GP
20.20334.015
CRT_R, CRT_G, CRT_B, CRT_HSYNC, CRT_VSYNC, DAT_DDC1_5, CLK_DDC1_5, 5V_CRT_S0, CRT_IN#_1
C488 SC22P50V2JN-4GP DY
C490 SC33P50V2JN-3GP DY
C489 SCD01U16V2KX-3GP
C491 SC33P50V2JN-3GP DY
C487 SC22P50V2JN-4GP DY
3D3V_S0
R256 10KR2J-3-GP
R257 470R2J-2-GP
33 CRT_IN#
C486 SC100P50V2JN-3GP

Hsync & Vsync level shift

9 VGA_HSYNC, 49 HSYNC, 9 VGA_VSYNC, 49 VSYNC
R278, R279, R281, R280 — UMA / DIS — 0R2J-2-GP
HSYNC_4, VSYNC_4
U21A TSAHCT125PW-GP
U21B TSAHCT125PW-GP
5V_S0
C482 SCD1U16V2ZY-2GP
R4, R3 — 33R2J-2-GP
CRT_HSYNC1, CRT_VSYNC1, CRT_HSYNC2, CRT_VSYNC2
L2, L1 — 0R2J-2-GP
CRT_HSYNC, CRT_VSYNC

DDC_CLK & DATA level shift

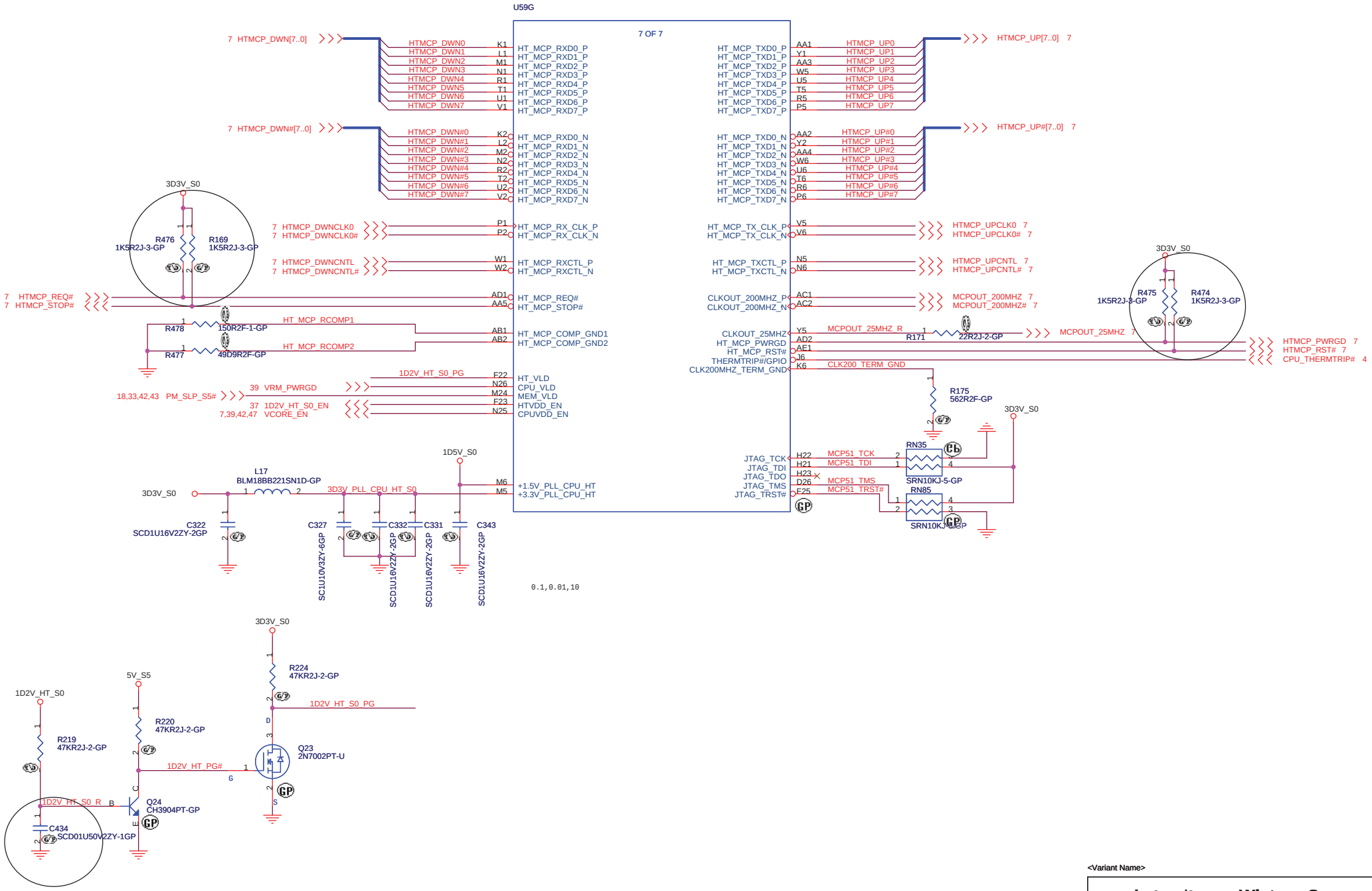
18 DDC_VGA_5V_DAT, 49 G72_CRT_EDID_DAT, 49 G72_CRT_EDID_CLK, 18 DDC_VGA_5V_CLK
R282, R262, R263, R283 — UMA / DIS — 0R2J-2-GP
RN46 SRN2K7J-3-GP
RN44 SRN2K7J-3-GP
3D3V_S0
5V_S0
5V_CRT_S0
D18 CH751H-40PT
Q29 FDN337N-1-GP
Q28 FDN337N-1-GP
DAT_DDC1_5, CLK_DDC1_5

TV CONN

49 G72_TV_LUMA, 9 VGA_TV_LUMA
49 G72_TV_CRMA, 9 VGA_TV_CRMA
49 G72_TV_COMP, 9 VGA_TV_COMP
R277, R269 — DISTV / UMATV — 0R2J-2-GP
R275, R267 — DISTV / UMATV — 0R2J-2-GP
R276, R268 — DISTV / UMATV — 0R2J-2-GP
DACB, DACC, DACA
C497 SC8P250V2CC-GP
C495 SC8P250V2CC-GP
C496 SC8P250V2CC-GP
L27, L25, L26 — IND-D56UH-16-GP
C503, C501, C502 — SC82P50V2JN-3GP
C494, C492, C493 — SC82P50V2JN-3GP
R577, R578, R579 — 150R2F-1-GP SB
LUMA_1, CRMA_1, COMP_1
TVOUT1
LUMA, CRMA, COMP, NC#2, GND, GND, GND, GND, NC#5
MINDIN7-19-GP-U2
22.10021.H61
D1, D3, D2 BAV99PT-GP-U DY
D17, D16, D15 BAV99PT-GP-U DY
RED, GREEN, BLUE
3D3V_S0

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV Connector
Size | Document Number: MYALL M | Rev: SA
Date: Friday, June 16, 2006 | Sheet 14 of 59



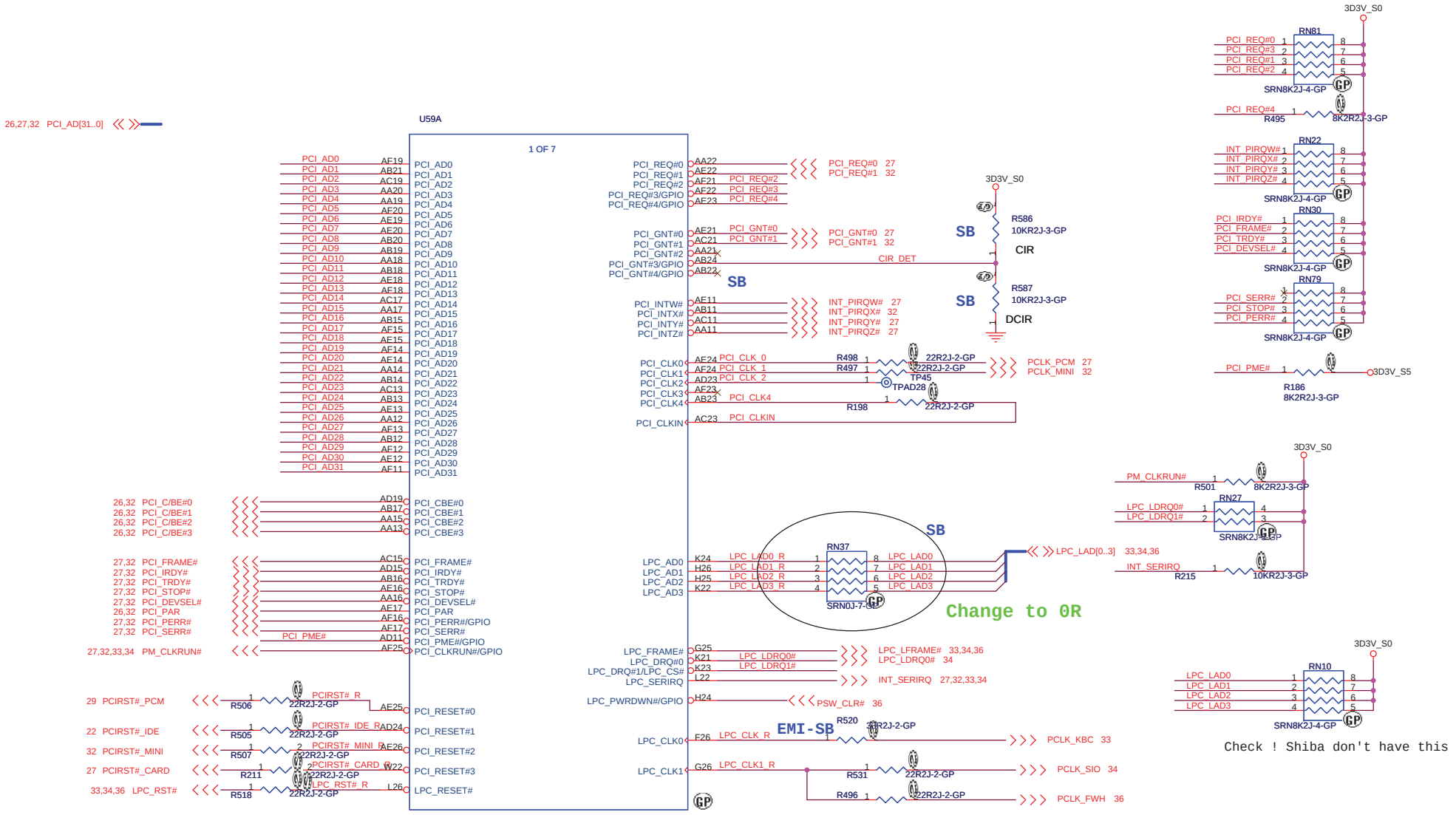
<Variant Name>

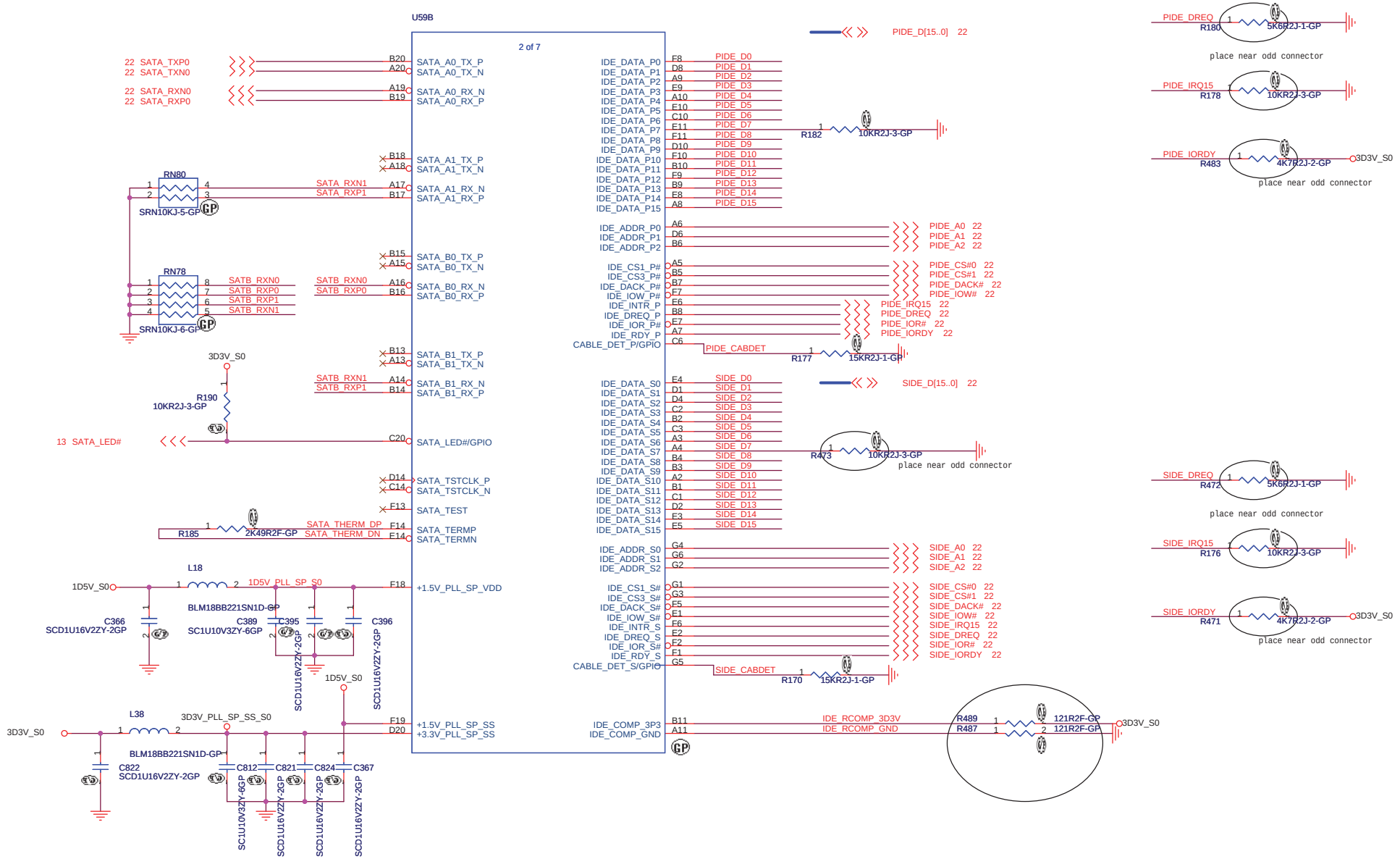
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MCP51(1/6)HT**

Size	Document Number	Rev
A3	MYALL M	SA

Date: Friday, June 16, 2006 Sheet 15 of 59





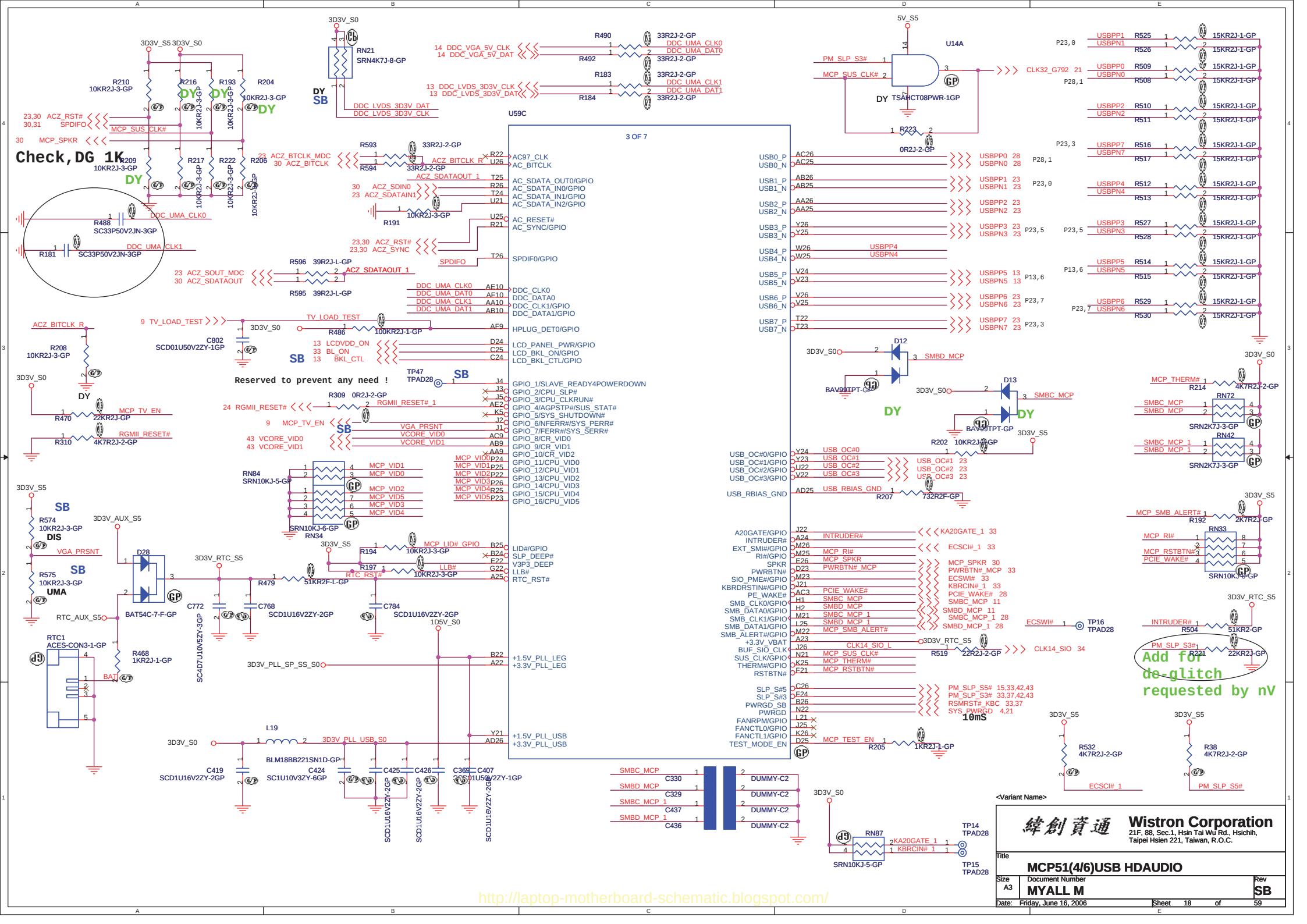
<Variant Name>

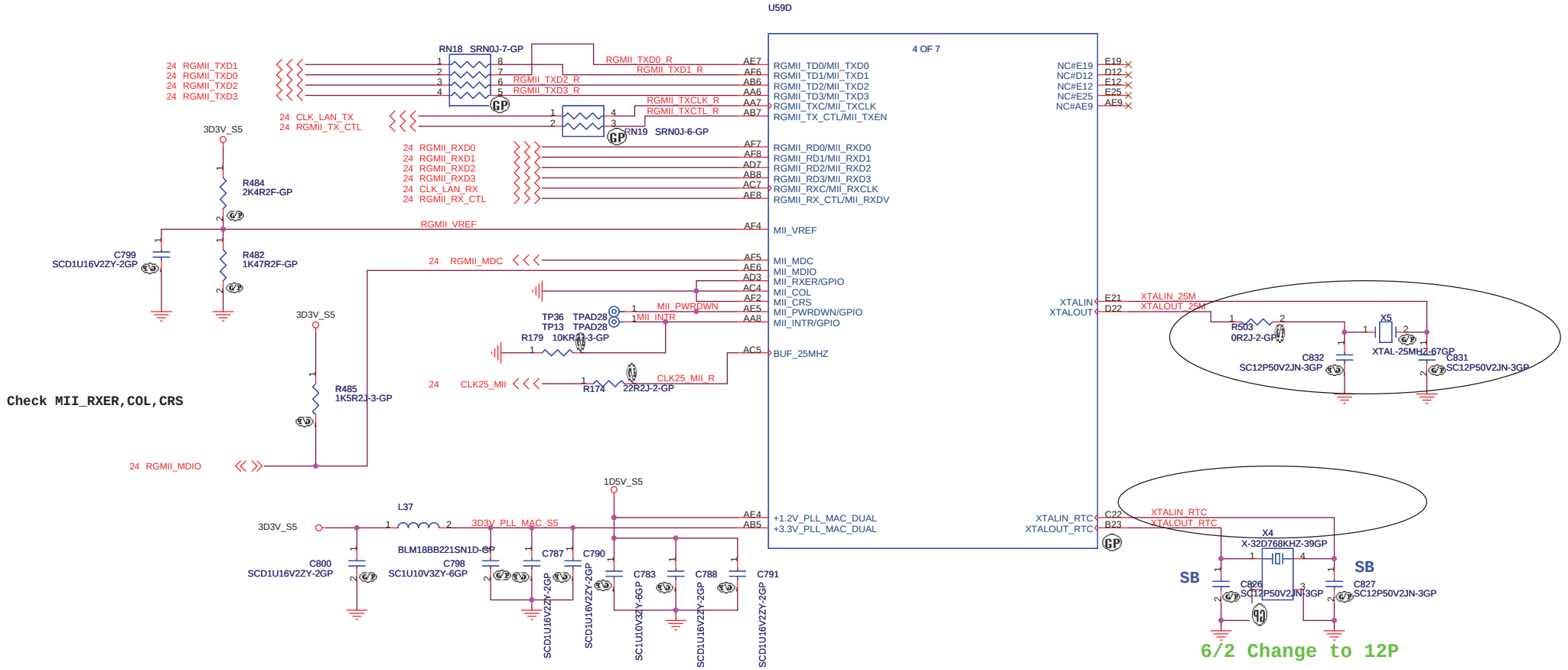
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MCP51(3/6)SATA/PATA

Size	Document Number	Rev
A3	MYALL M	SA

Date: Friday, June 16, 2006 Sheet 17 of 59

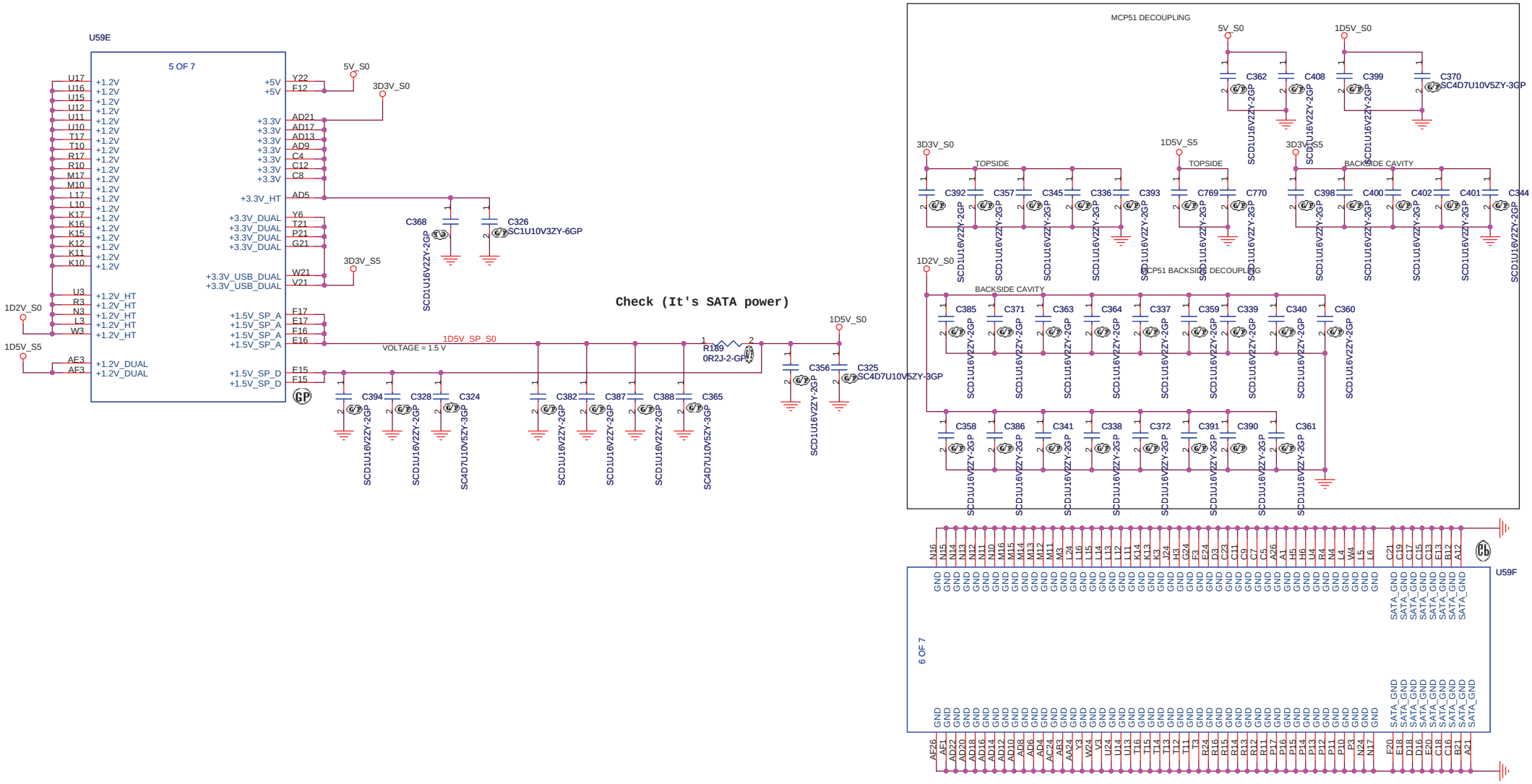

Check,DG 1K
U59C
3 OF 7
U14A
Reserved to prevent any need !
Add for de-glitch requested by nV
10mS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
MCP51(4/6)USB HDAUDIO
MYALL M
Friday, June 16, 2006
http://laptop-motherboard-schematic.blogspot.com/



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MCP51(5/6)RGMII	
Size A3	Document Number MYALL M	Rev SB
Date: Friday, June 16, 2006	Sheet 19 of 59	



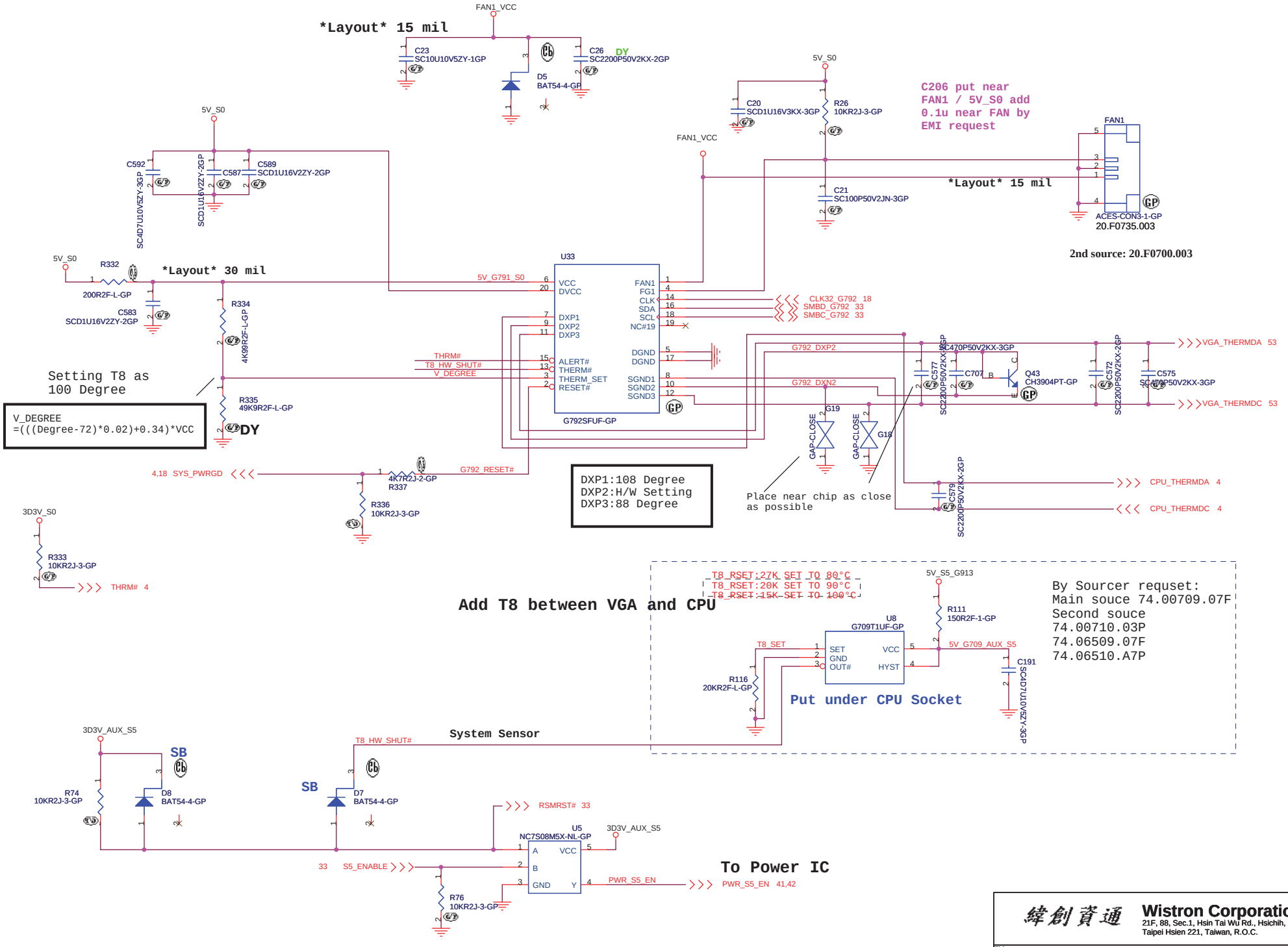
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MCP51(6/6)POWER

Size	Document Number	Rev
A3	MYALL M	SA

Date: Friday, June 16, 2006 Sheet 20 of 59



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

Size	Document Number	Rev
	MYALL M	SA

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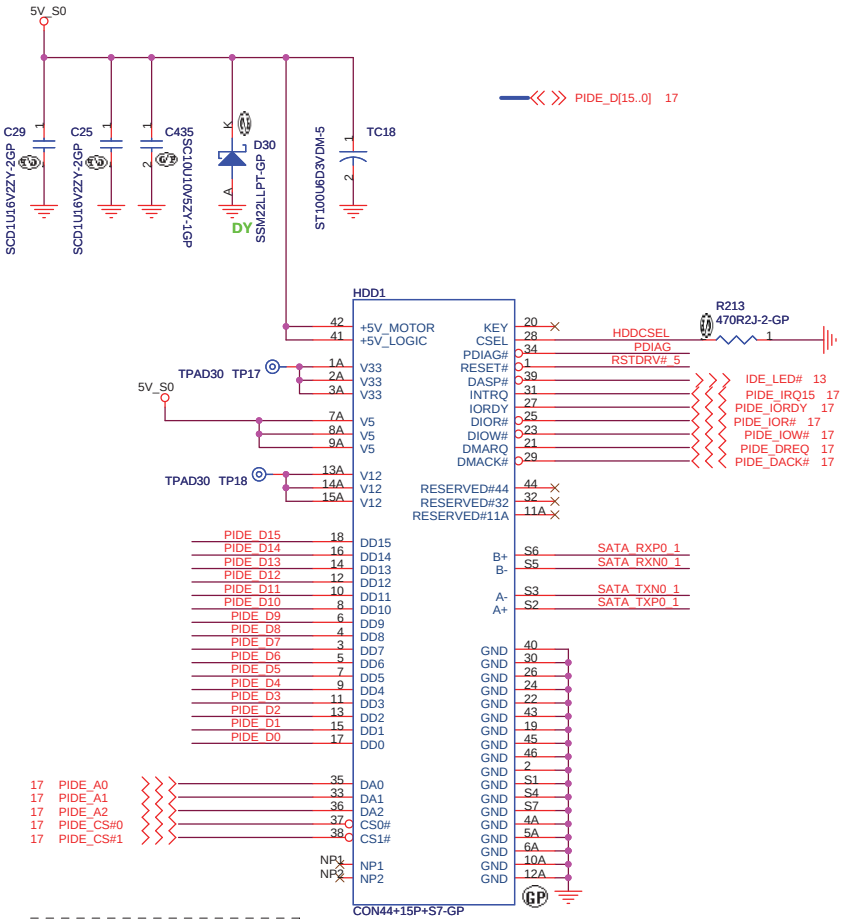
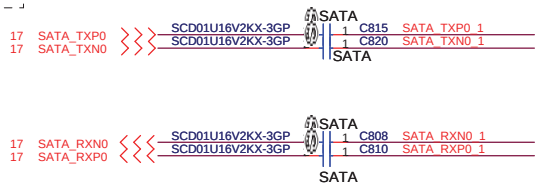
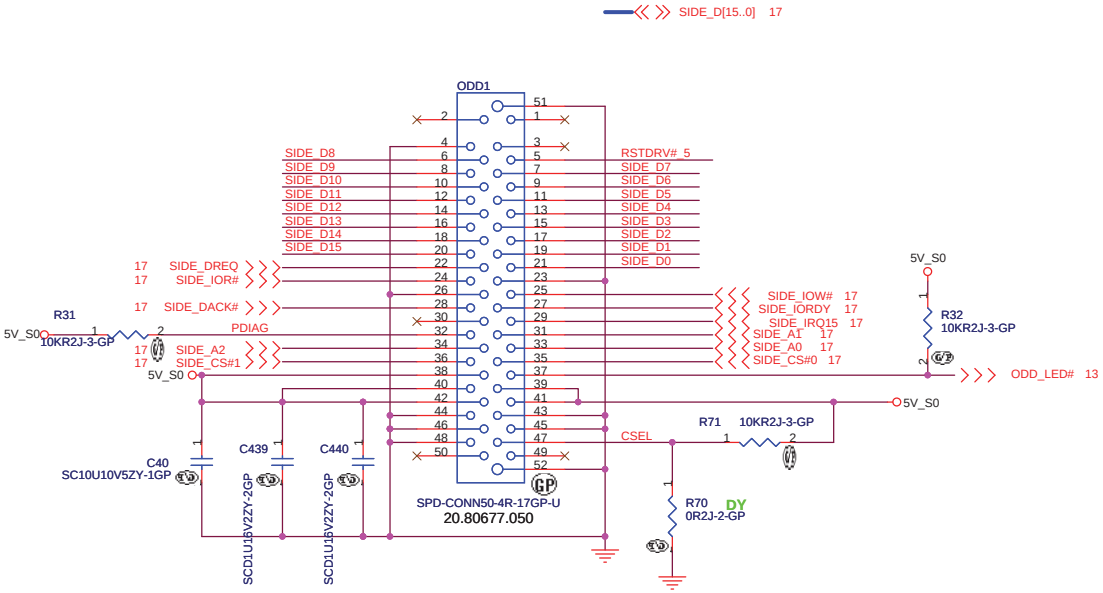
HDD Connector



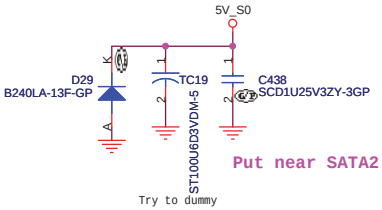
SATA PN : 20.F0883.001
PATA PN : 21.E0021.222



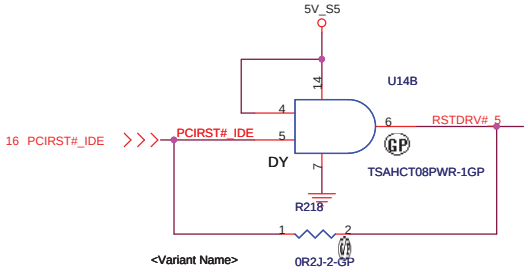
CD-ROM Connector



For HDD & SATA both



Put near SATA2 Connector



<Variant Name>

ME : 20.F0777.022

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD and CDROM		
Size	Document Number	Rev
	MYALL M	SA
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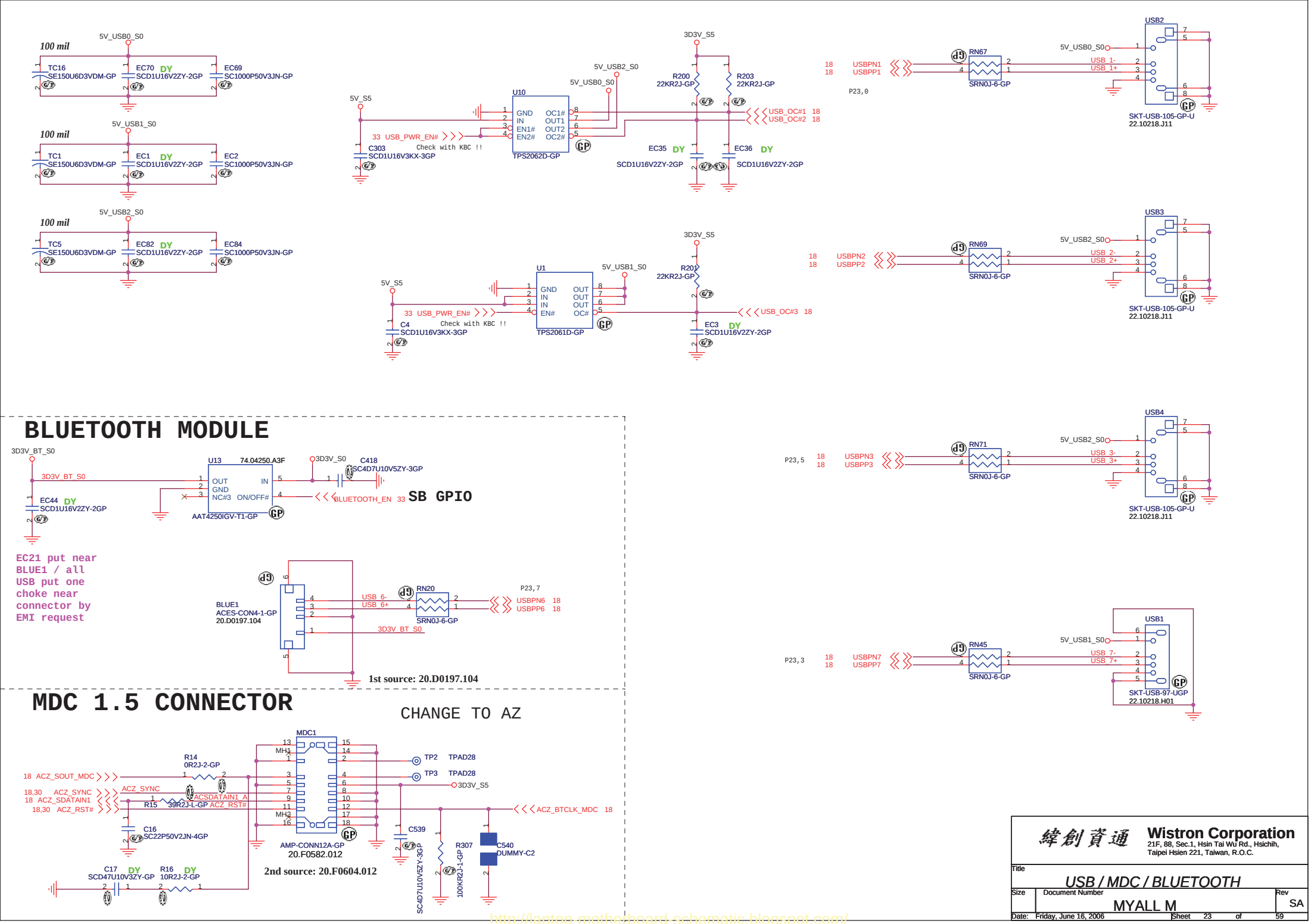
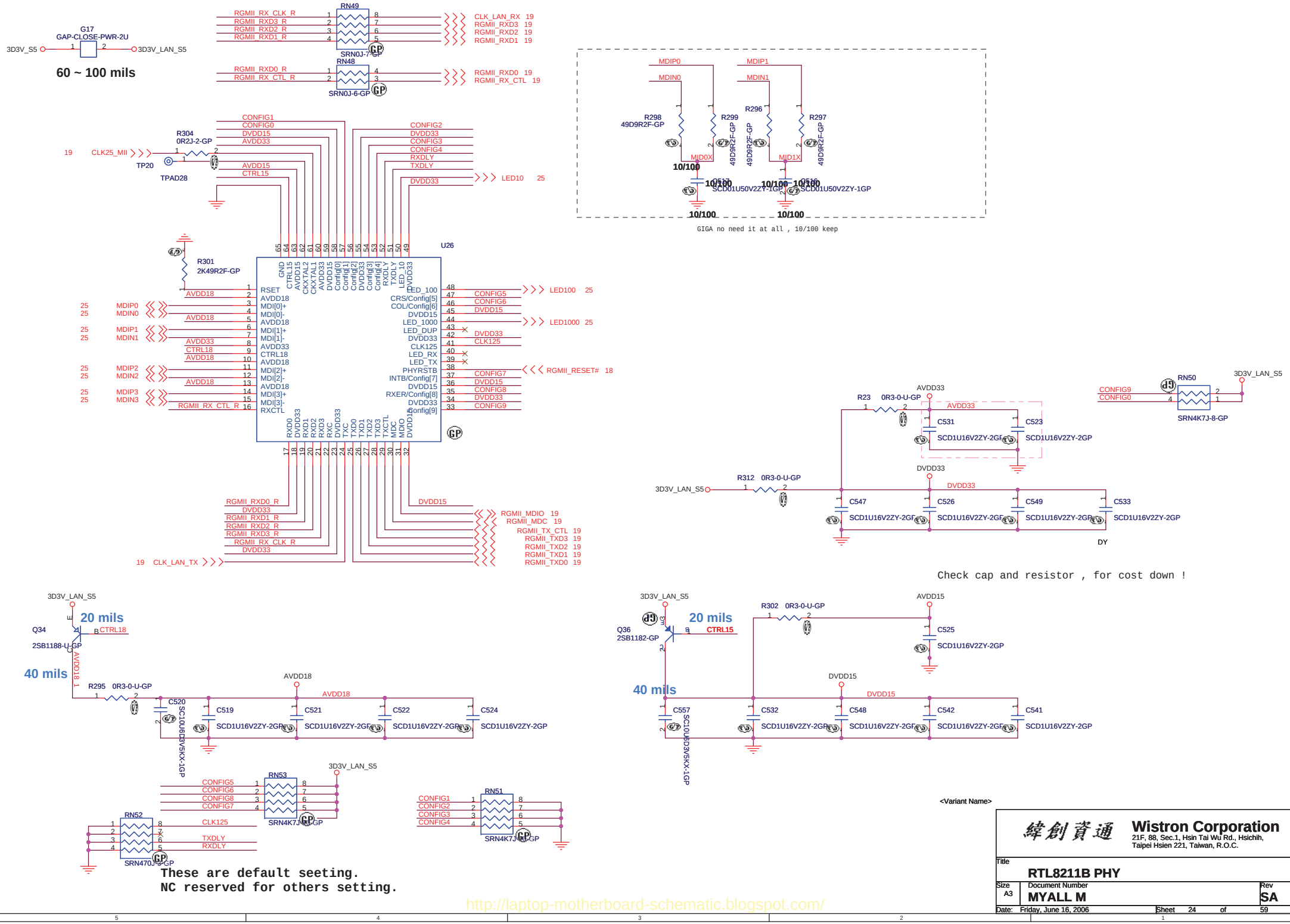
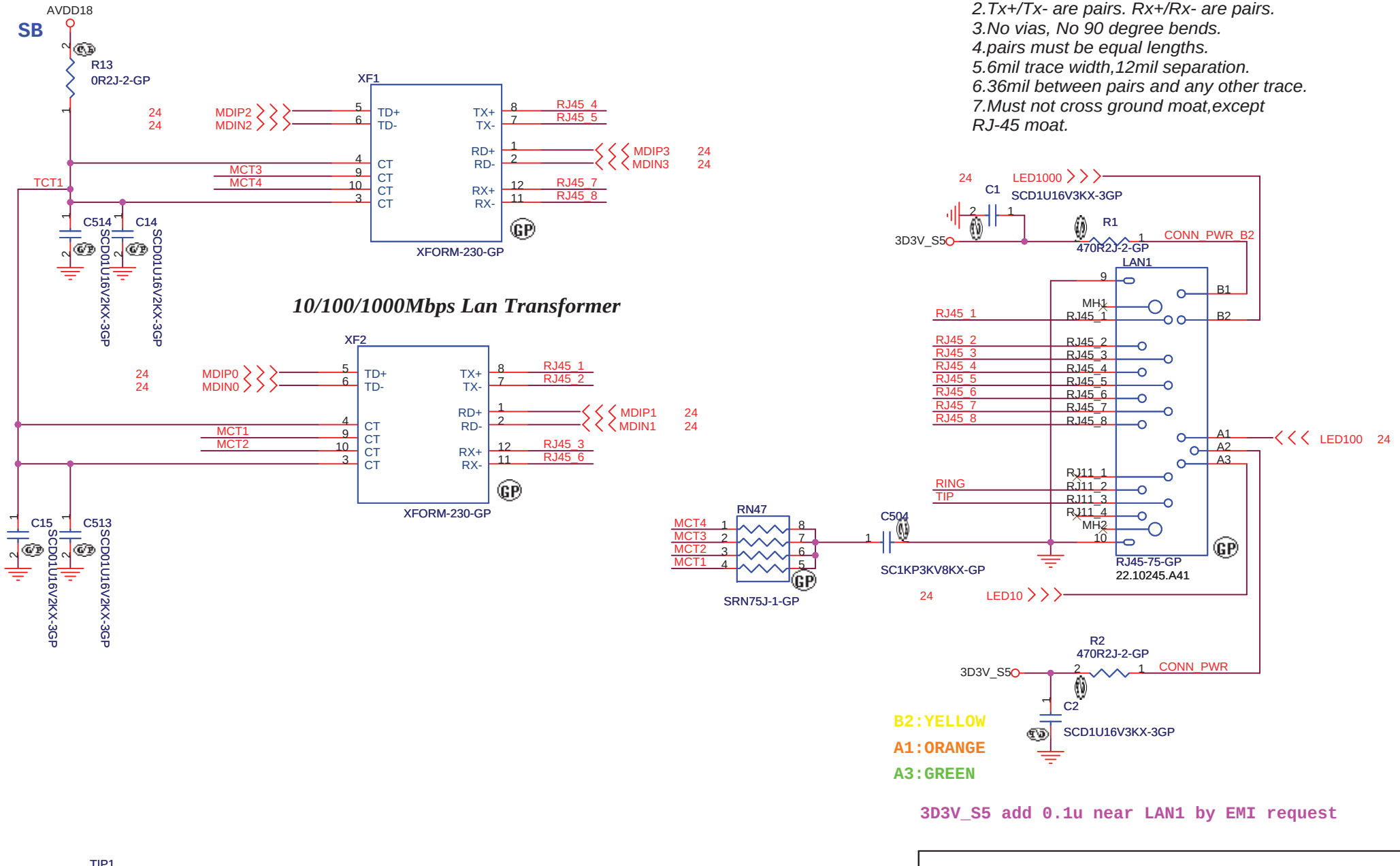




1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *LAN CONN*

Size	Document Number	Rev
	MYALL M	SA

Date: Friday, June 16, 2006 Sheet 25 of 59

C782 should close Pin-P15
and Pin-R17.

TI PCI7412

U62A

1 0F 2

71.07412.B0U

PCI7412ZHK-GP

* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible

Bypass/Decupoling Capacitors
Should be places as close to
PCI7412 as possible

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: TI PCI7412 (1 of 2)	
Size	Document Number: MYALL M
Rev: SA	
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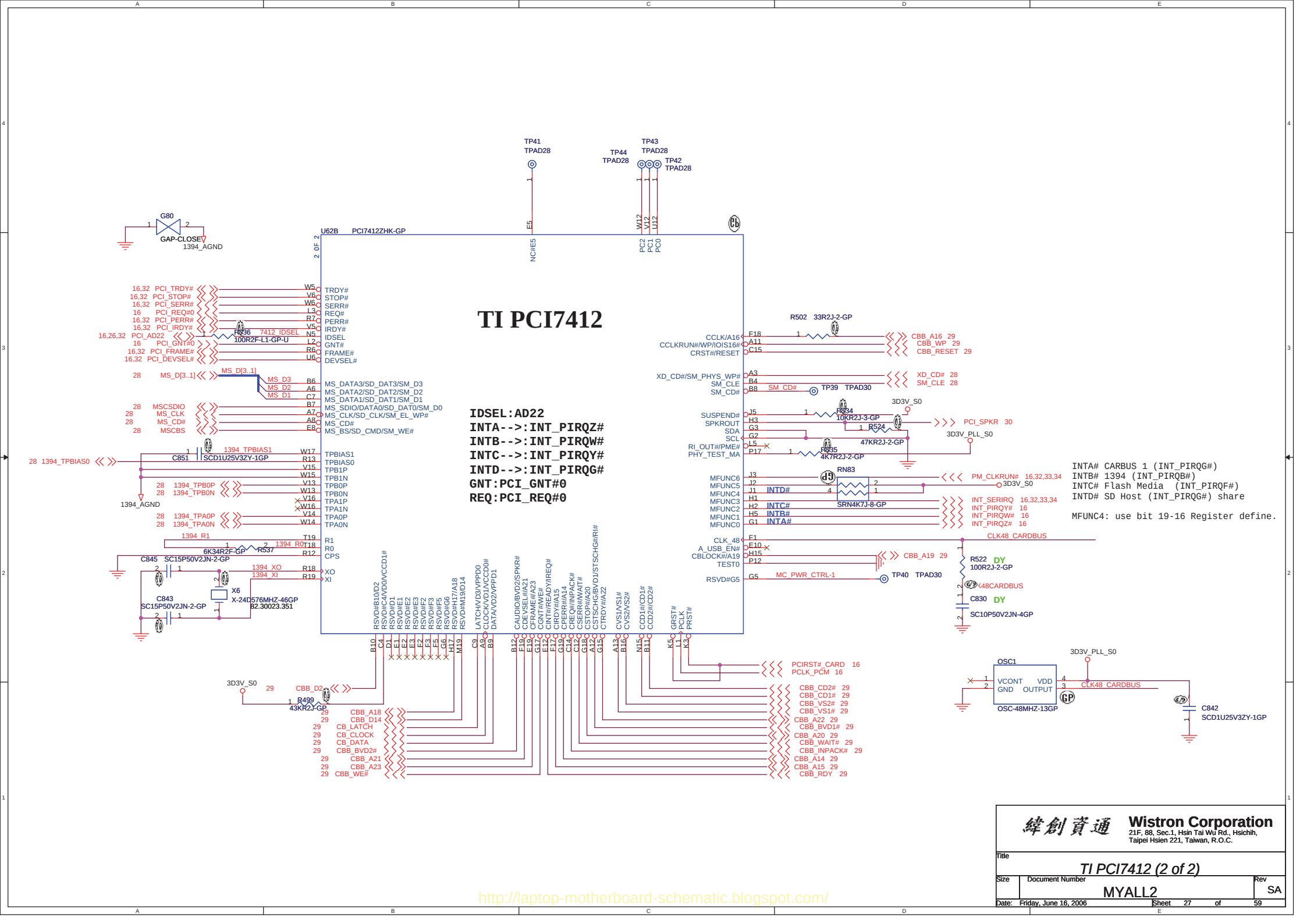
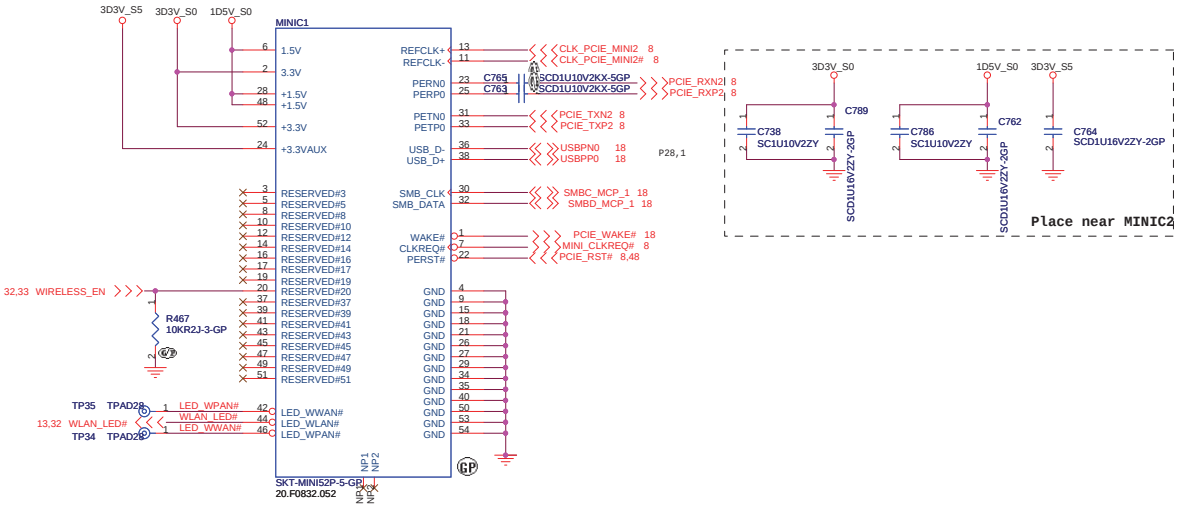
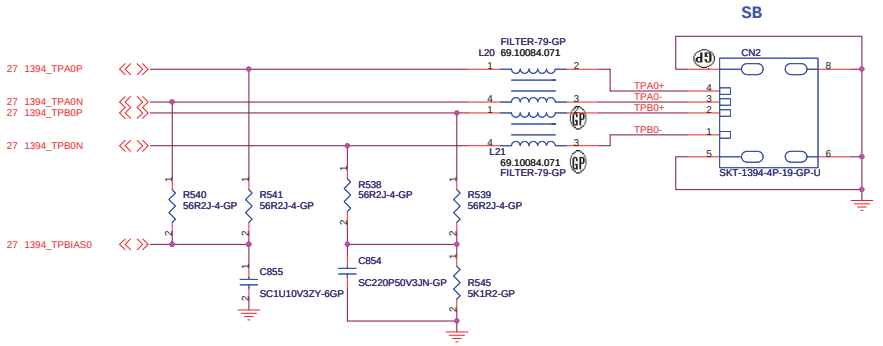
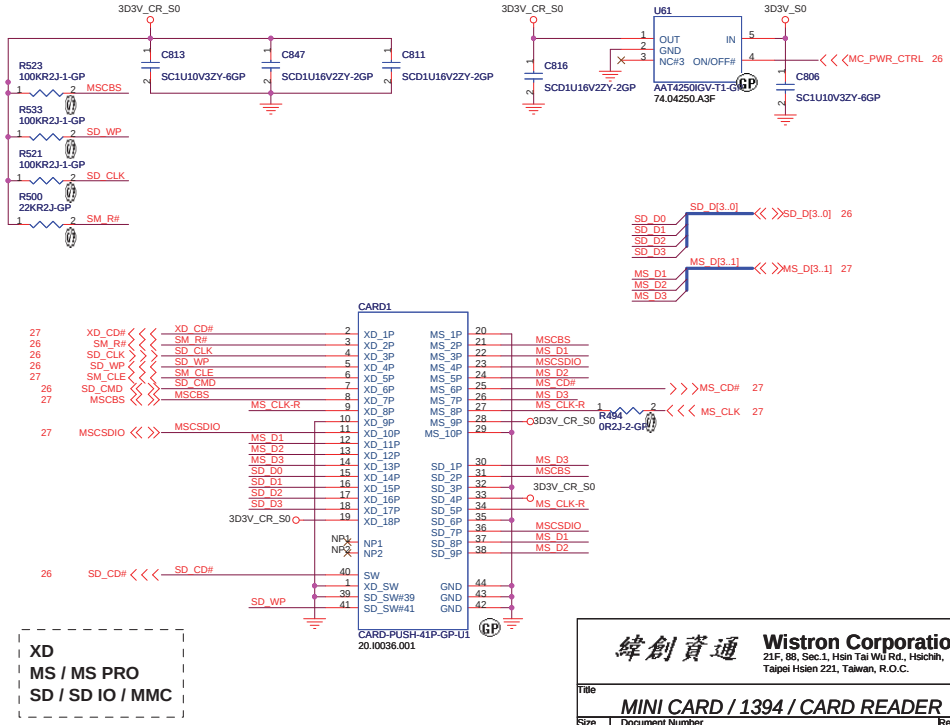


Mini Card Connector



1394 Connector





緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD / 1394 / CARD READER

Size | Document Number: MYALL M | Rev: SA

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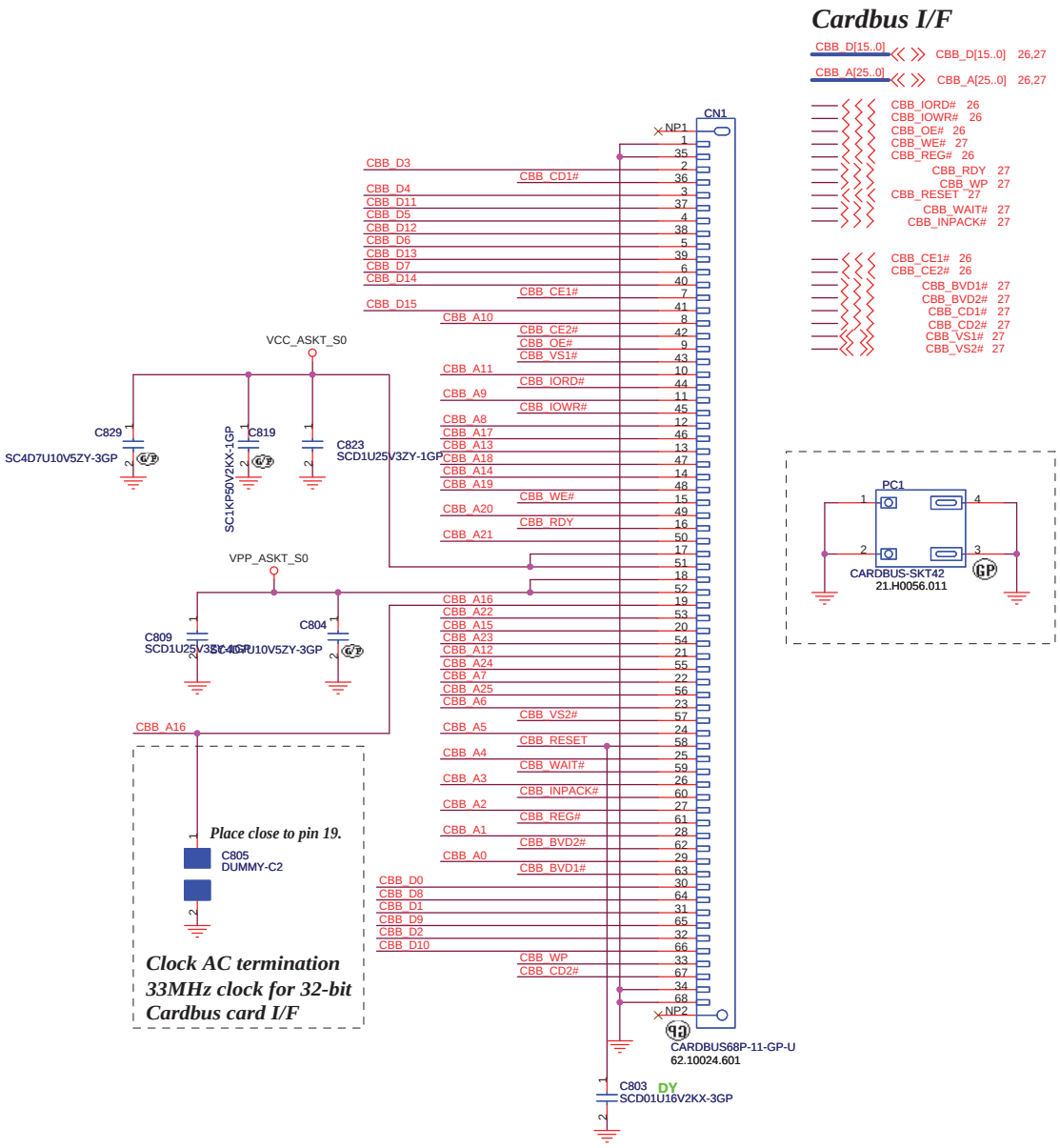
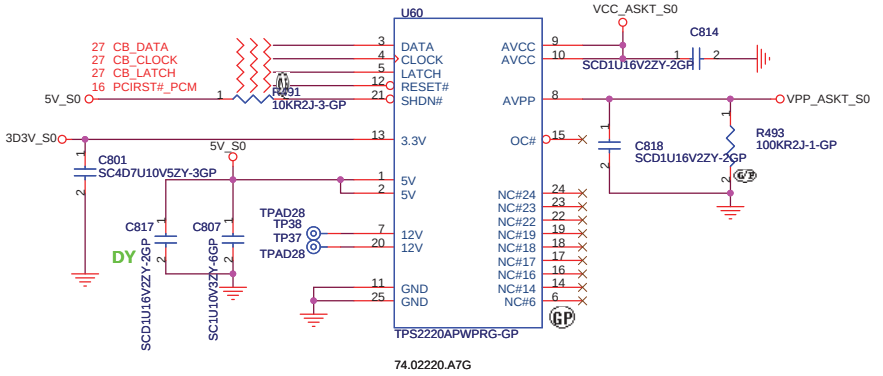
PCMCIA Socket



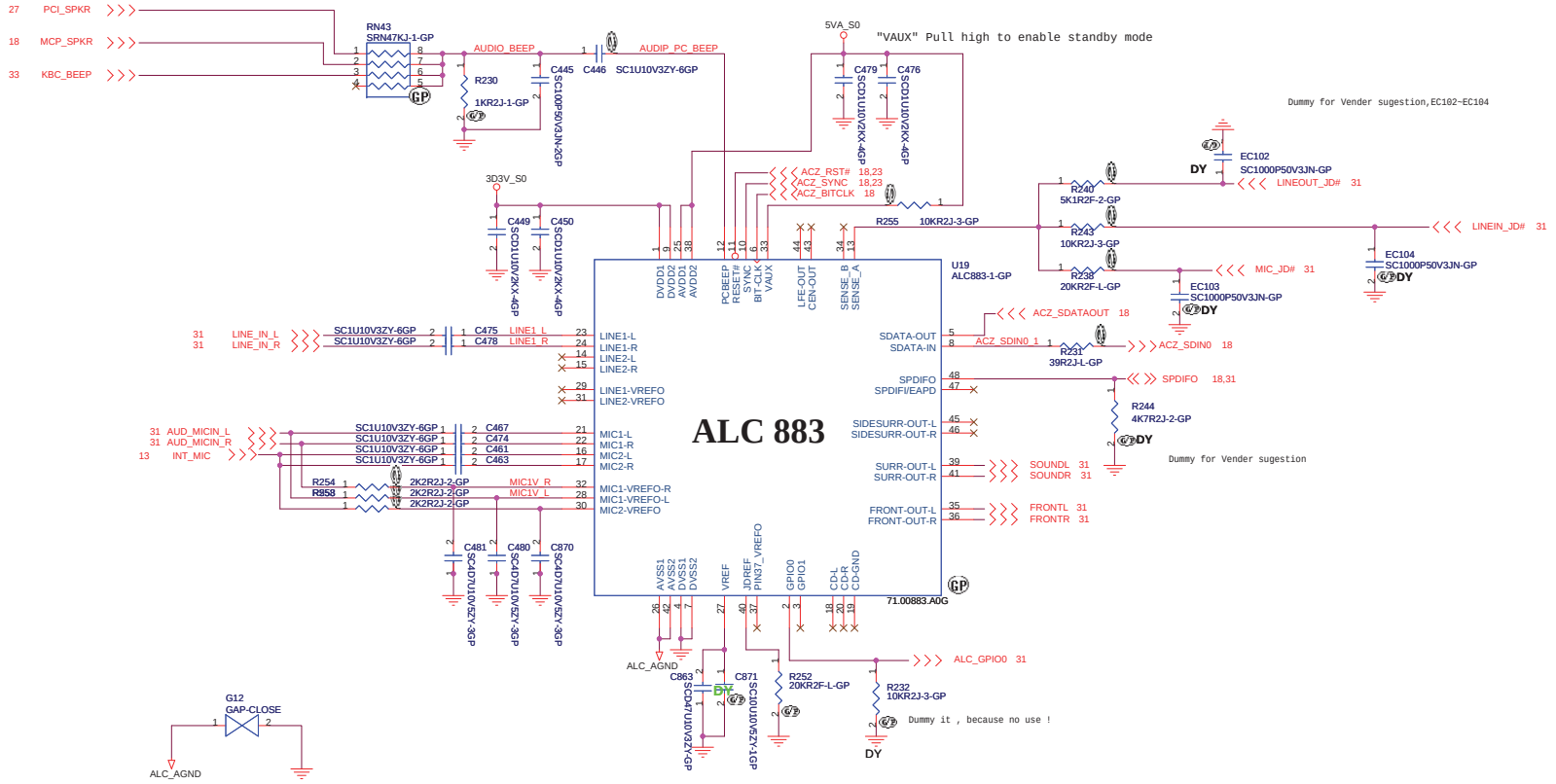
Cardbus I/F

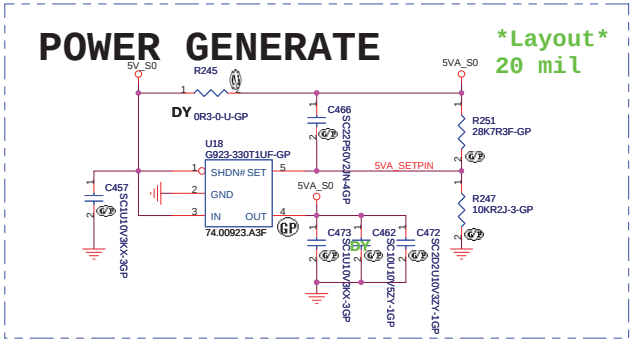
Power switch



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCMCIA	
Size	Document Number: MYALL M	Rev: SA
Date: Friday, June 16, 2006	Sheet 29 of 59	





Pin	Symbol		
35/36	FRONT		
39/41	SURR	X	
43/44	CEN/LEFT	X	
45/46	SIDESURR	X	
23/24	LINE1		
21/22	MIC1	Location	Re-tasking
14/15	LINE2	XMP,Jack1	AMP output, line input
16/17	MIC2		X
			SURR-VREFO-L/R
			SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
		Jack 2	Line input, line output
		Jack 3	Mic input, line output
			X
		Int. Mic	Mic input

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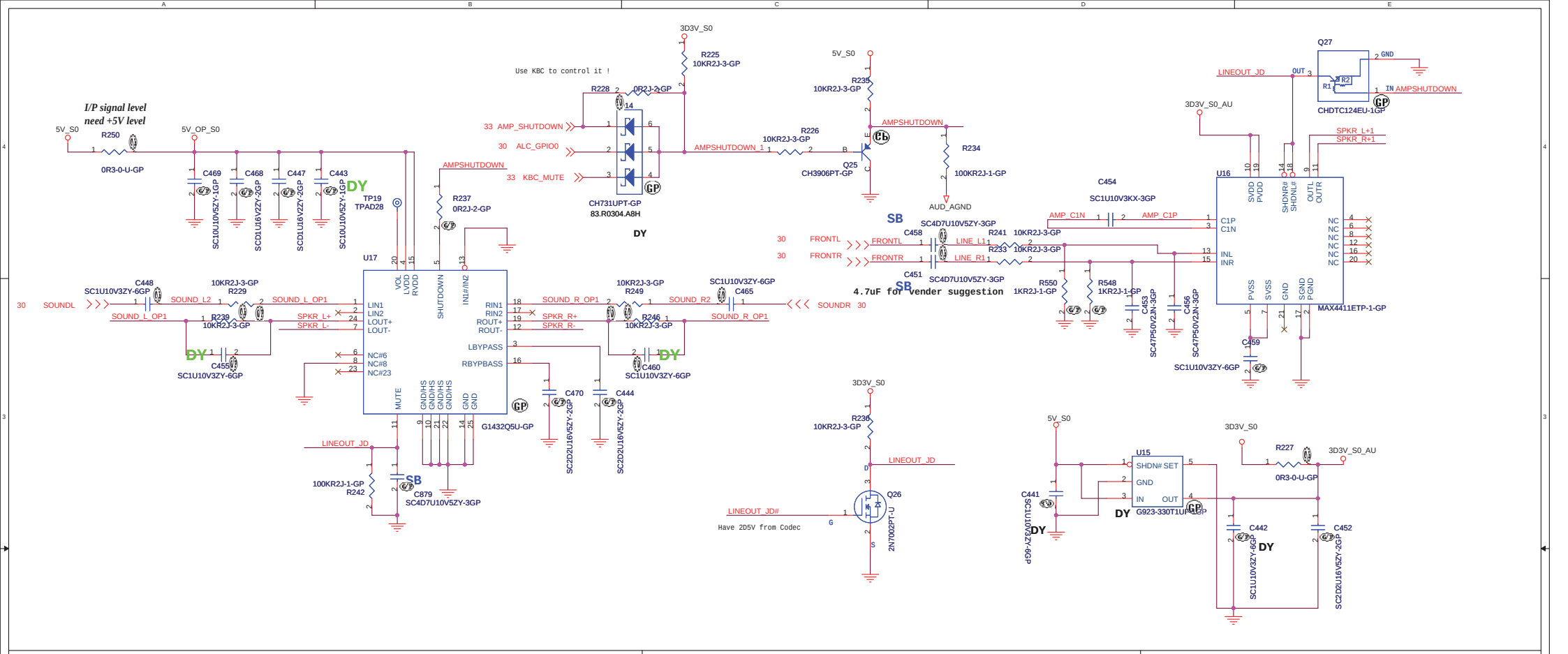
Title: AUDIO (1/2) -- CODEC ALC883
Size: Custom | Document Number: MYALL M | Rev: SA
Date: Friday, June 16, 2006 | Sheet 30 of 59



緯創資通 Wistron Corporation
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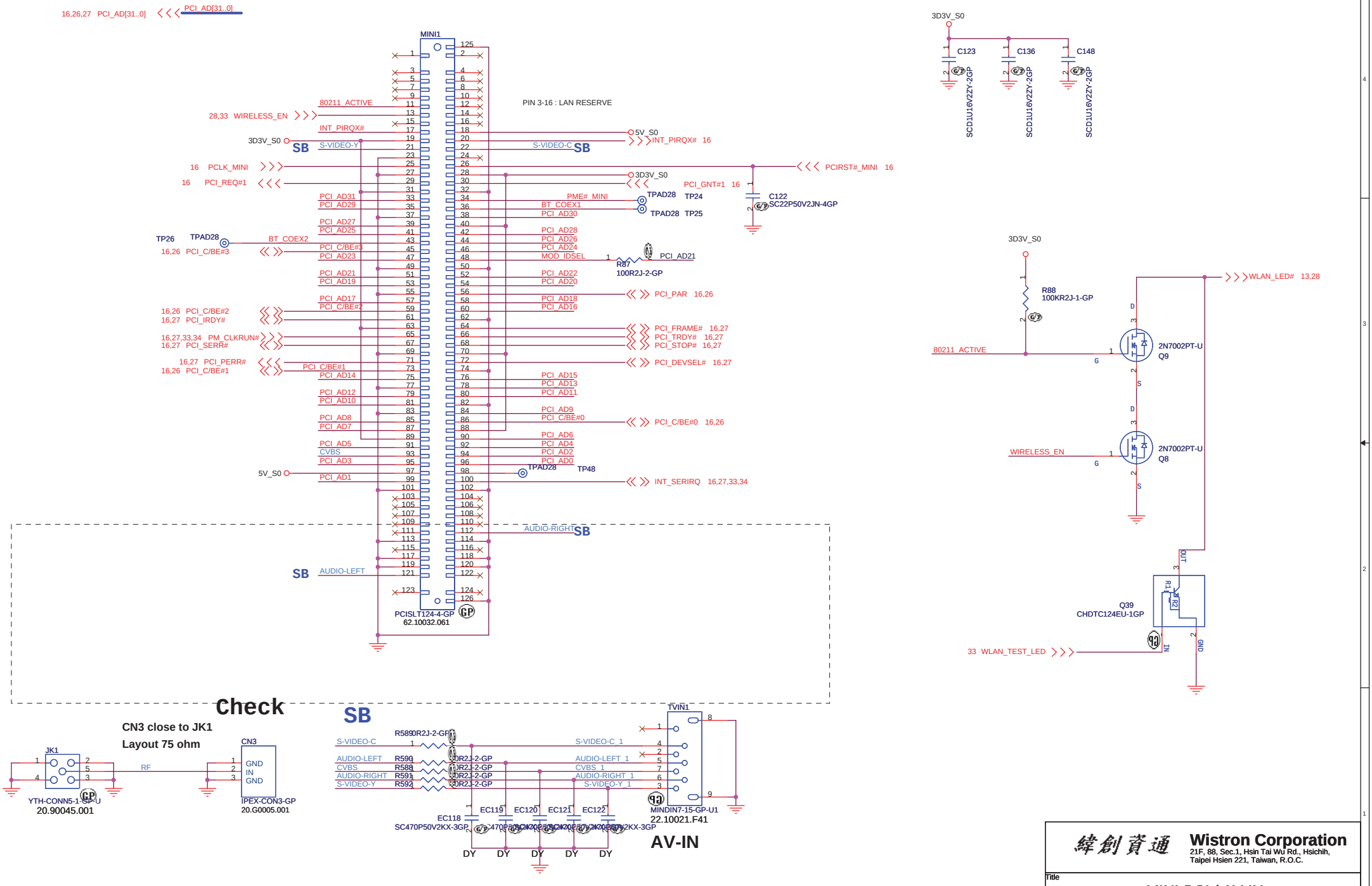
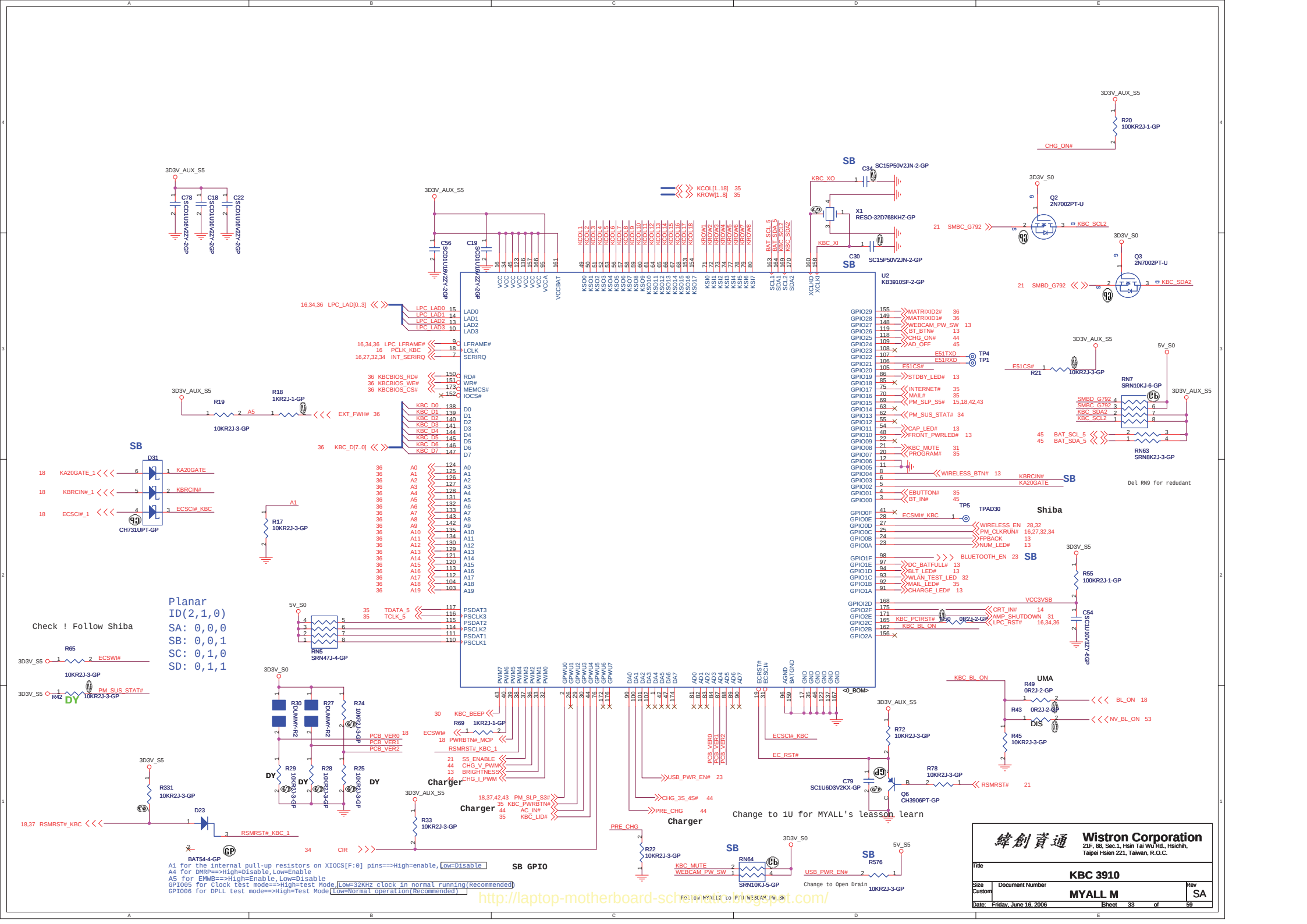
Taipei Hsien 221, Taiwan, R.O.C.

<core Design>

Title	AUDIO AMP AND JACK		
Size: Custom	Document Number: MYALL M		Rev: SB
Date: Friday, June 16, 2006	Sheet 31 of 59		




Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
Check ! Follow Shiba
SB GPIO
Change to 1U for MYALL's lesson learn
Change to Open Drain
Shiba
UMA
DIS
Charger
Del RN9 for redudant
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable, Low=Disable
A4 for DMRP==>High=Disable, Low=Enable
A5 for EMWB==>High=Enable, Low=Disable
GPIO05 for Clock test mode==>High=test Mode, Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode, Low=Normal operation(Recommended)
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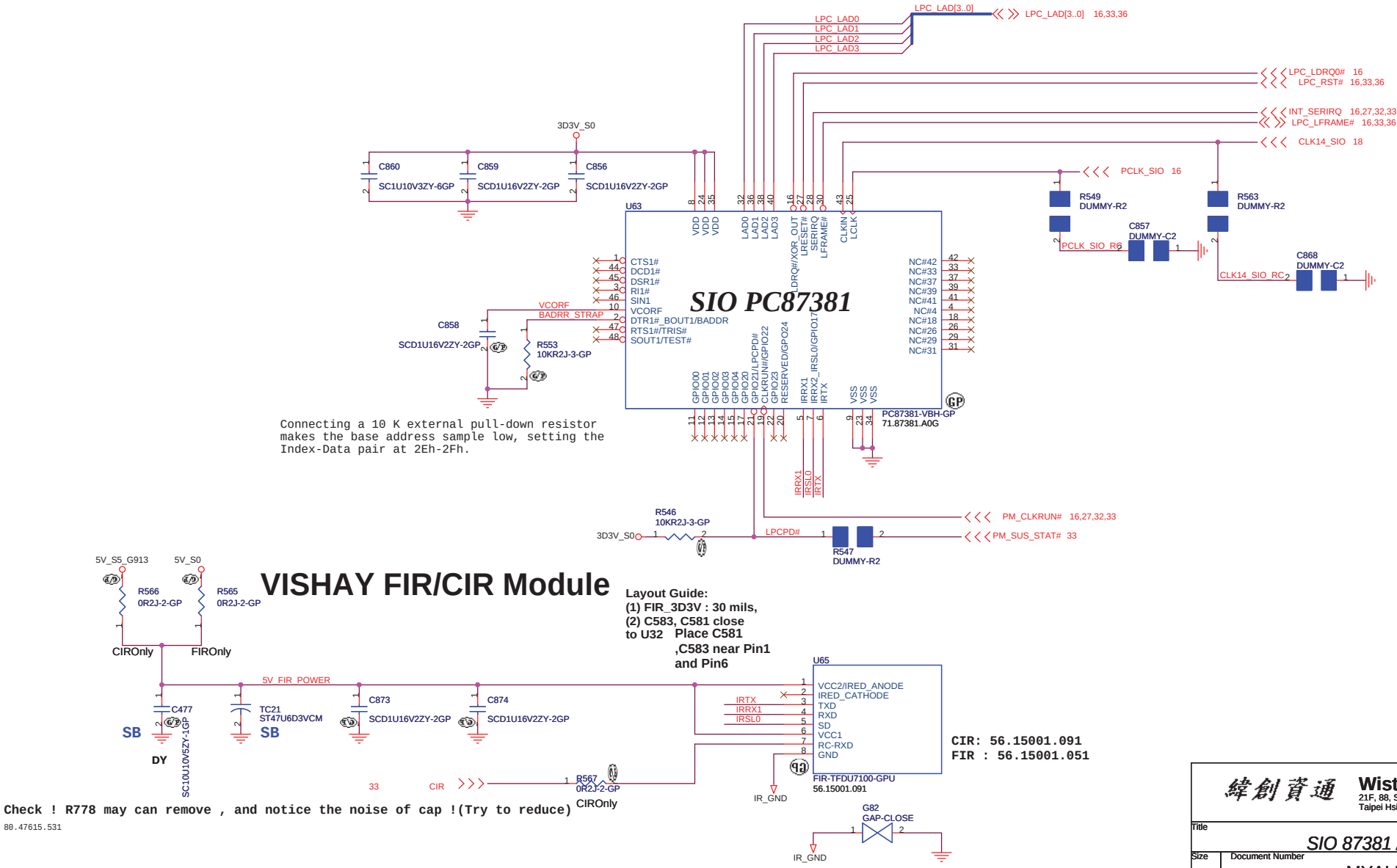
KBC 3910
MYALL M
SA
Friday, June 16, 2006
33
59
http://laptop-motherboard-schematic.blogspot.com/



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SIO 87381 / IR	
Size	Document Number: MYALL M	Rev: SA
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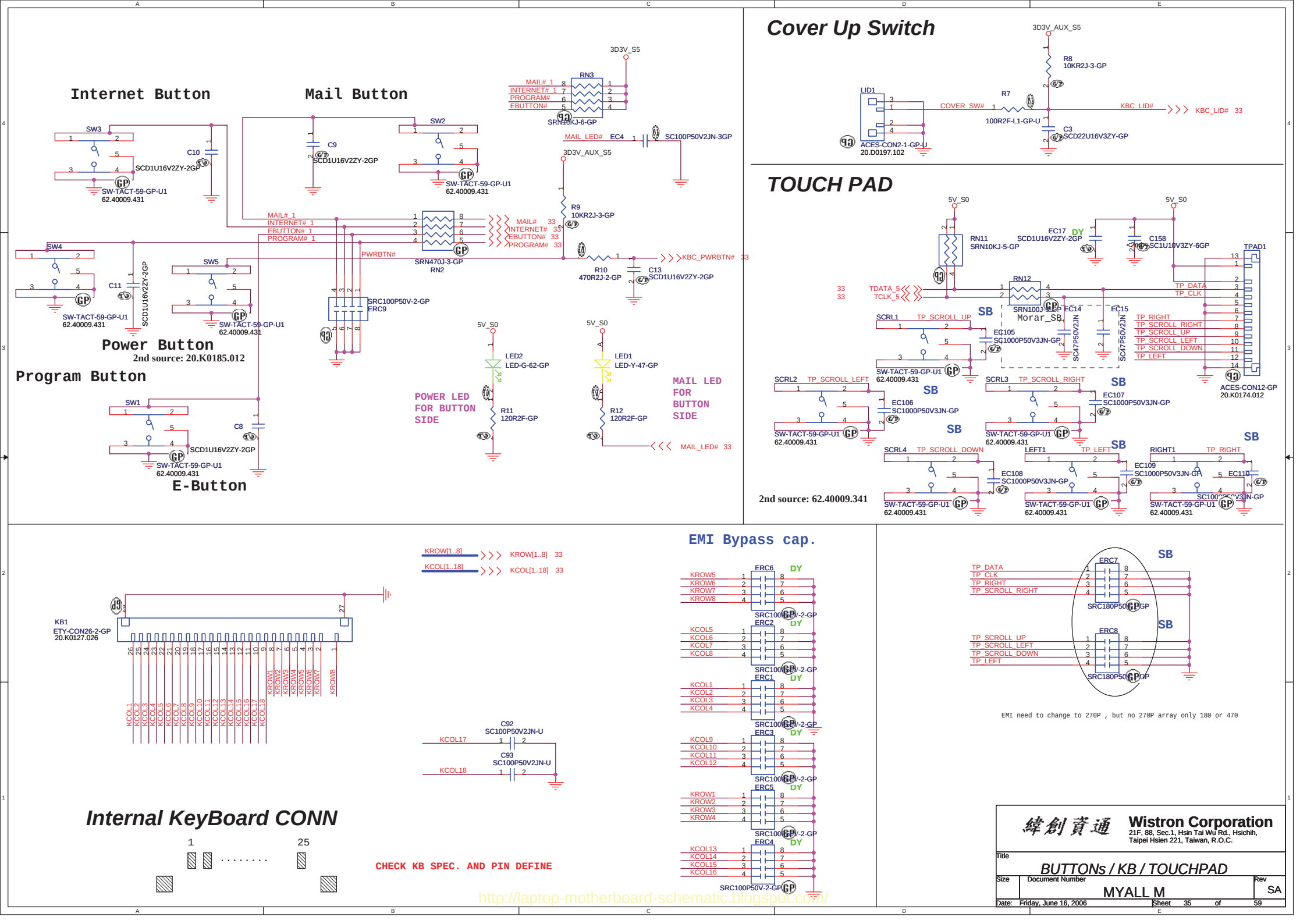

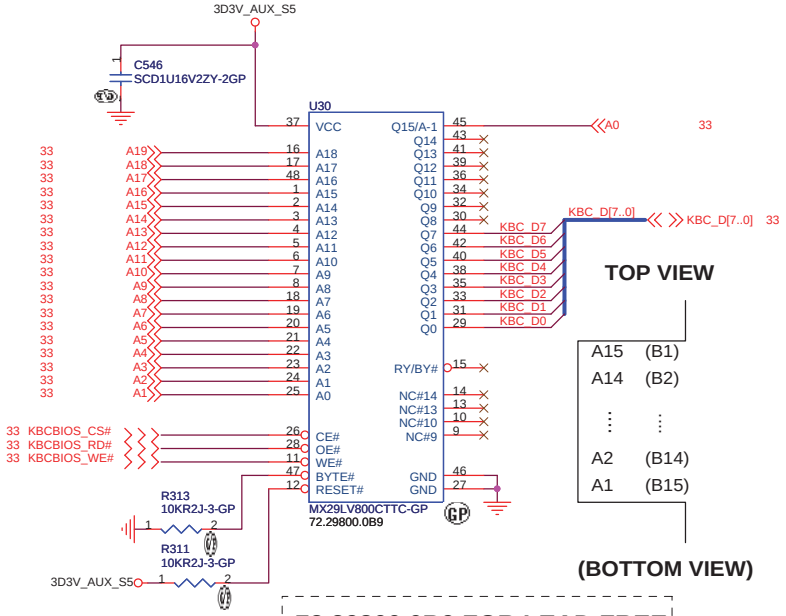

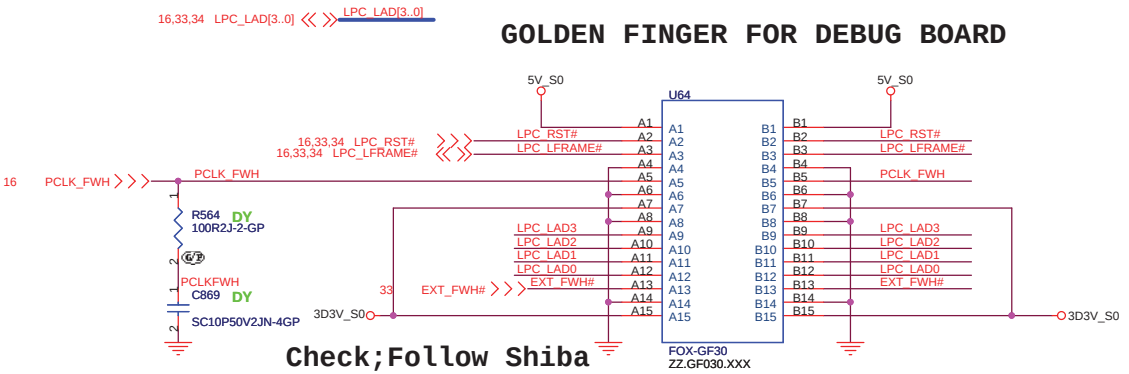

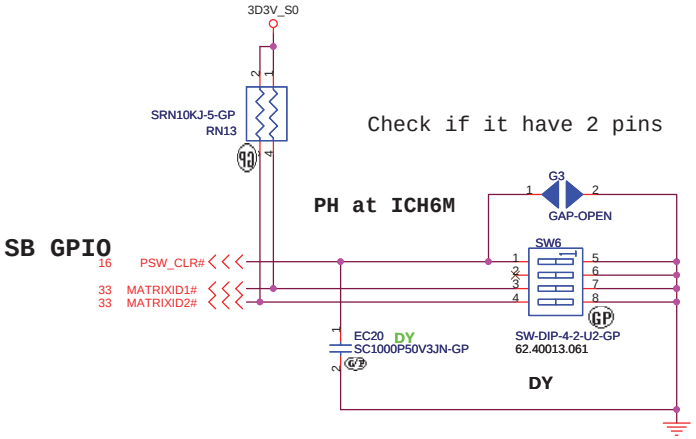

Wistron Corporation 緯創資通		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BIOS		
Size	Document Number: MYALL M	Rev: SA
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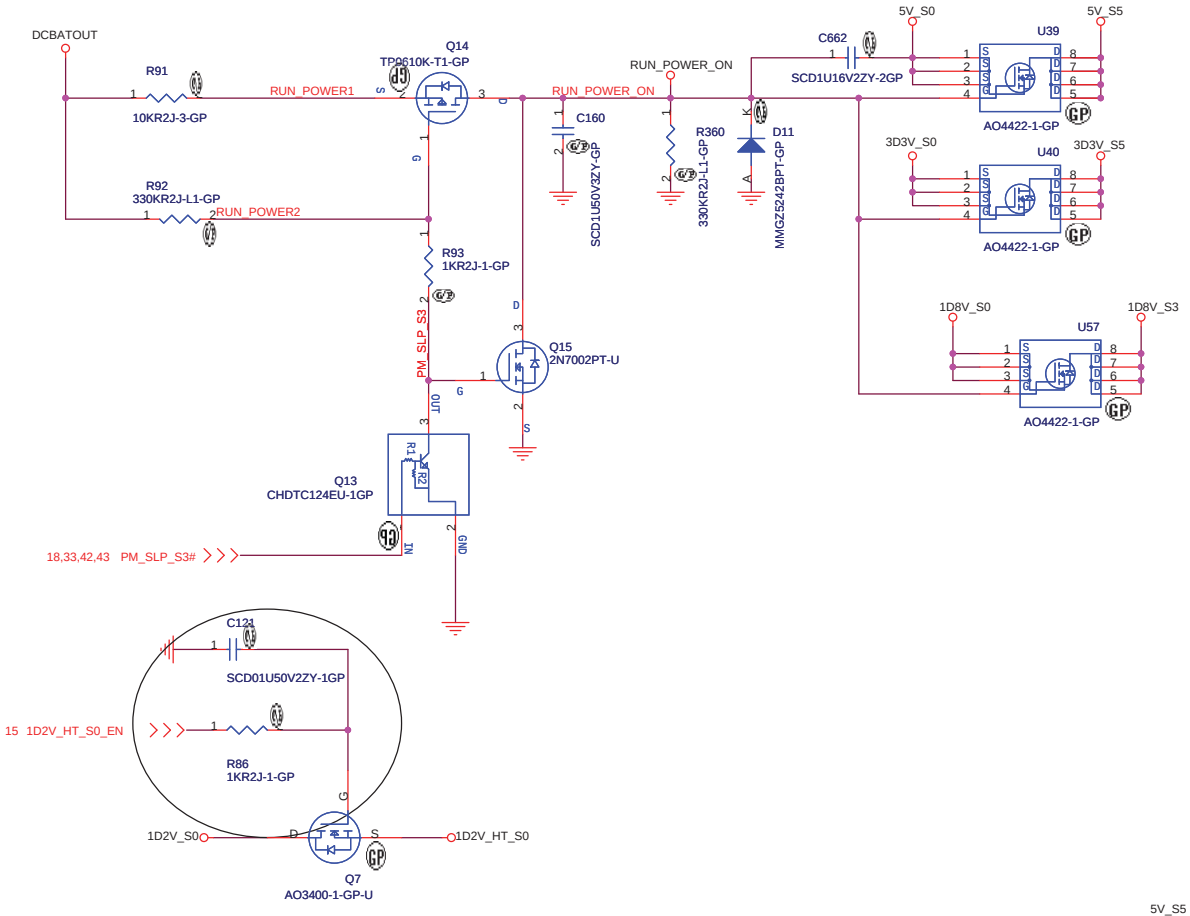
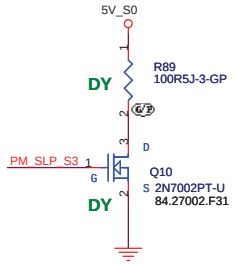
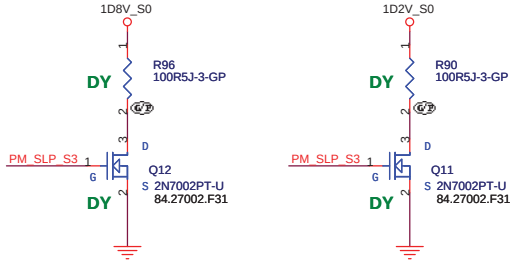
Run Power

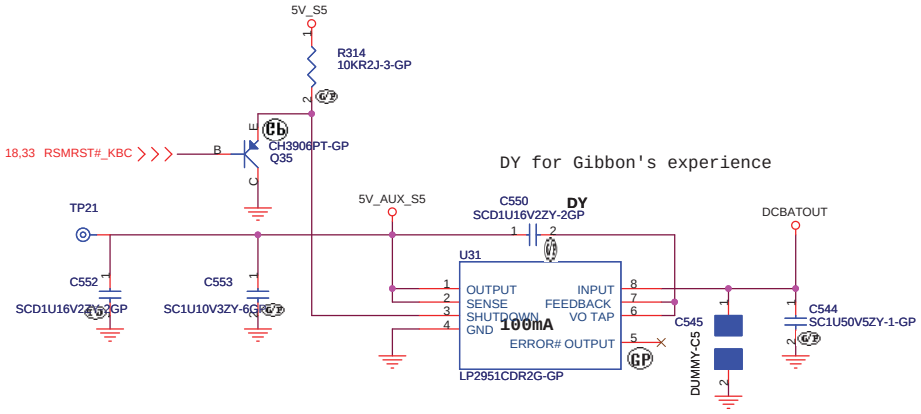


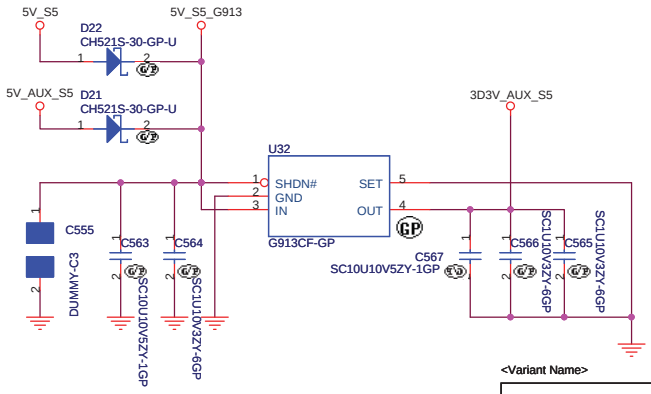




Aux Power

3D3V_AUX_S5





<Variant Name>

緯創資通 Wistron Corporation
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Title	RUN POWER and 3D3V_AUX_S5	
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CPU_CORE
MAX8760

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6

PSI#
CPUCORE_ON
PM_DPRSLPVR
H_DPRSTP#

VCC_SENSE
VSS_SENSE

DCBATOUT_8760
5V_S0
3D3V_S0

VID Setting
VID0(I / 1.05V)
VID1(I / 1.05V)
VID2(I / 1.05V)
VID3(I / 1.05V)
VID4(I / 1.05V)
VID5(I / 1.05V)
VID6(I / 1.05V)

Input Signal
PSI# (I / 3.3V)
PGD_IN (I / 3.3V)
DPRSLPVR (I / 3.3V)
DPRSTP# (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RTN(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD(OD / 3.3V) → 8760_PWRGOOD
CLK_EN#(O) → CLK_EN#

Output Power
VCC_CORE_PWR(O) → VCC_CORE_S0(Imax=48A)

Max8744 3D3V/5V

DCBATOUT

Input Power
VIN

Input Signal
Max8744_ON3 → ON3
Max8744_ON5 → ON5

Output Signal
PGOOD1(OD / 5V)
PGOOD2(OD / 5V)

Output Power
5V(O) → 5V_DC_S5 (5A)
3D3V(O) → 3D3V_DC_S5 (5A)

0D9V_S3

5V_S5
1D8V_S0
PM_SLP_S3#
PM_SLP_S5#

VIN
VLDOIN
S3
S5

VTT
VTTREF

G2997

ISL6269_VGA_Core 1D1V

5V_S5
DCBATOUT
PM_SLP_S3#
PGOOD

Input Power
VCC
VIN

Input Signal
EN

Output Signal
PG

Output Power
1D0V (O) → 1D0V (7.2A)

Charger_ISL6255

CHG_ON#/OFF
BAT_IN#
KBC_SCL0
KBC_SDA0
CHG_I_PRE_SEL
AC_IN
AD+

Input Signal
EN (I / 3.3V)
THM (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
CHLIM (IO / 5V)
PB0/MOSI/AIN0

Input Power
DCIN (I)

Output Signal
ACPRN (O / 3.3V) → AC_IN
XTAL2/PB4 (O/5V) → CHARGE_LED#

Output Power
VCC (O) → DCBATOUT
VCC (O) → BT+

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O) → DC_IN+

Output Power
VCC(O) → AD+

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram
Size | Document Number: MYALL M | Rev: SA
Date: Friday, June 16, 2006 | Sheet 38 of 59

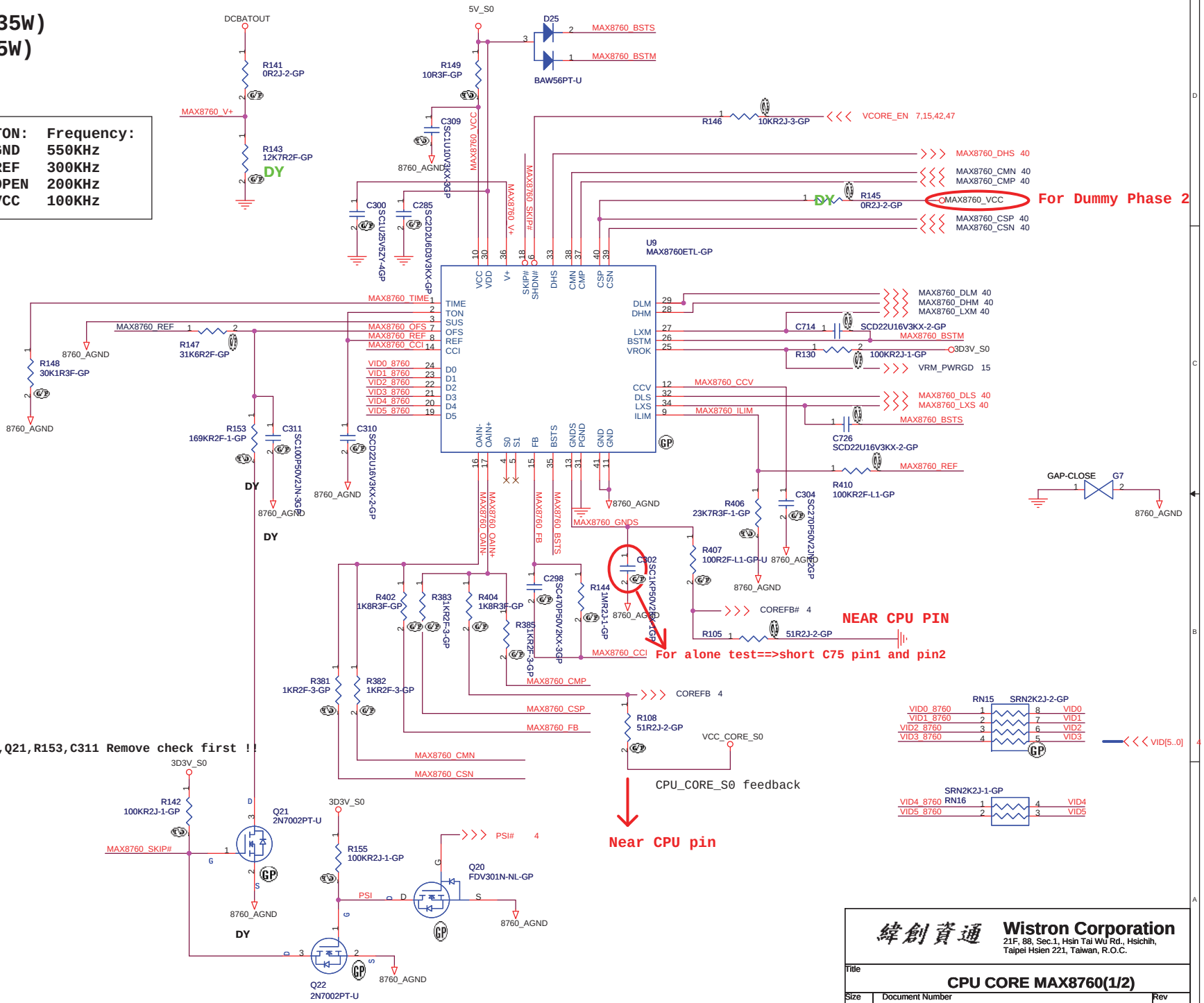
CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375

TON:	Frequency:
GND	550KHz
REF	300KHz
OPEN	200KHz
VCC	100KHz

R404,R402 change to 1K82F,Q21,R153,C311 Remove check first !!

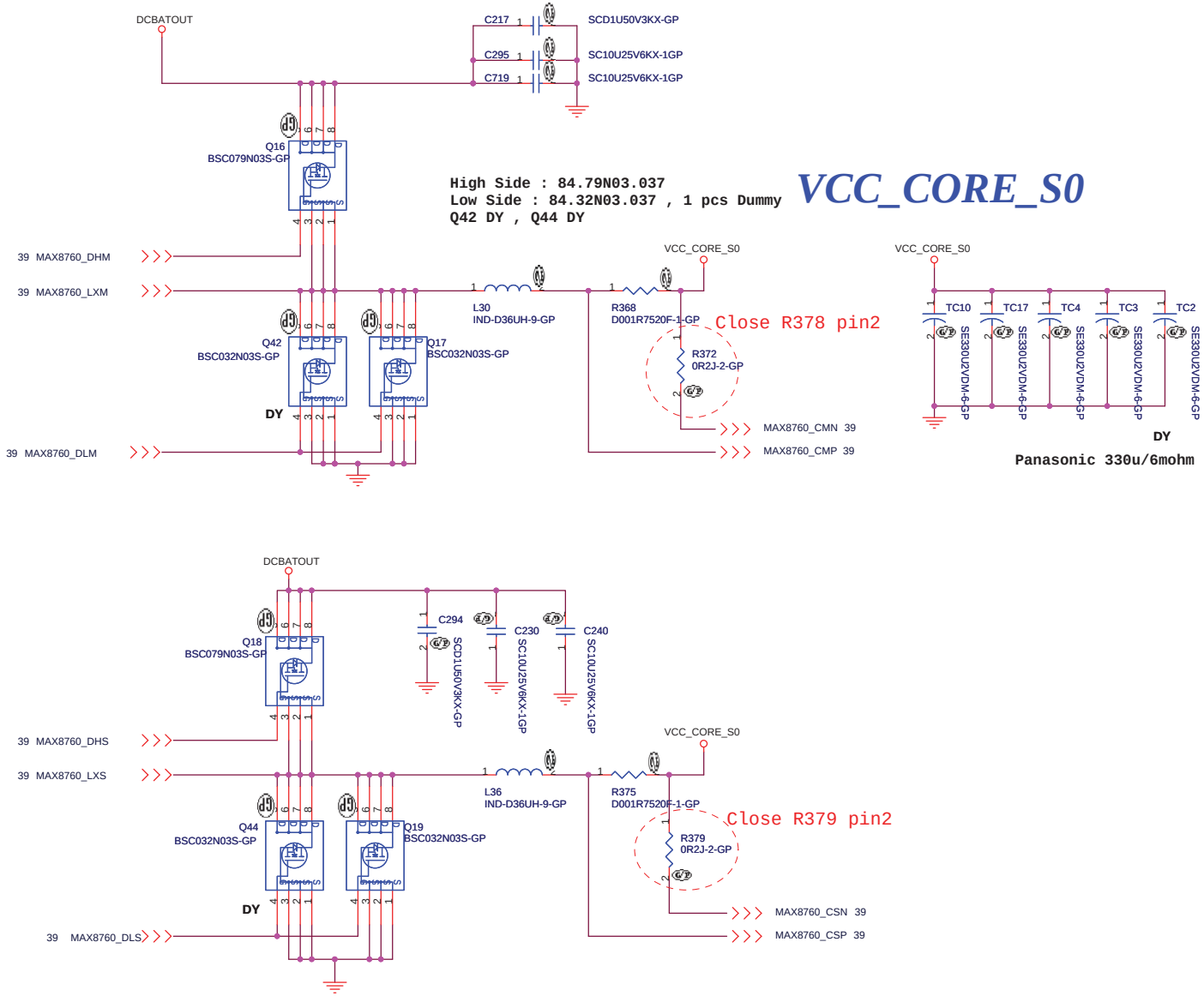


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU CORE MAX8760(1/2)

Size: A3 | Document Number: MYALL M | Rev: SA

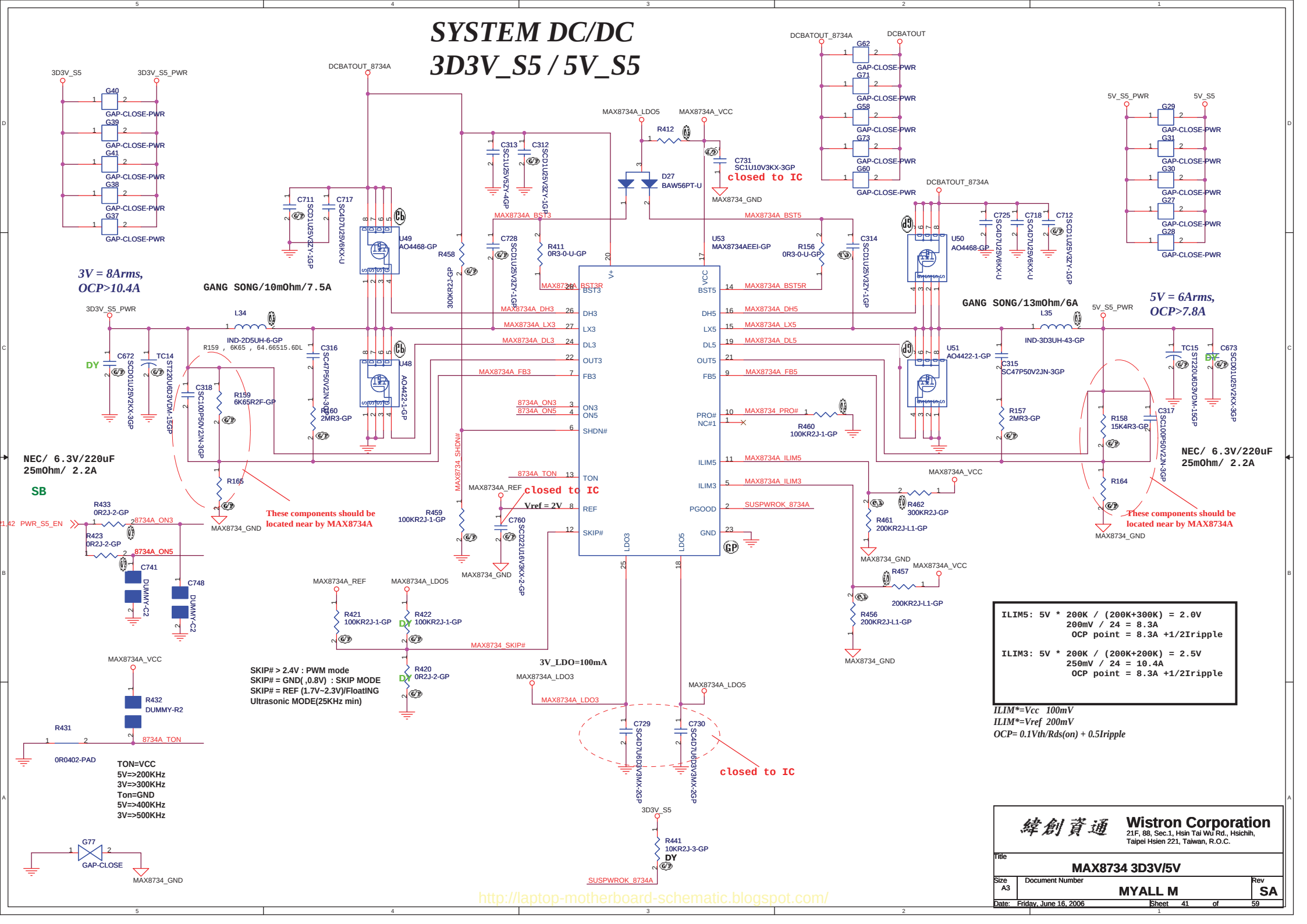
Date: Friday, June 16, 2006 | Sheet 39 of 59



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

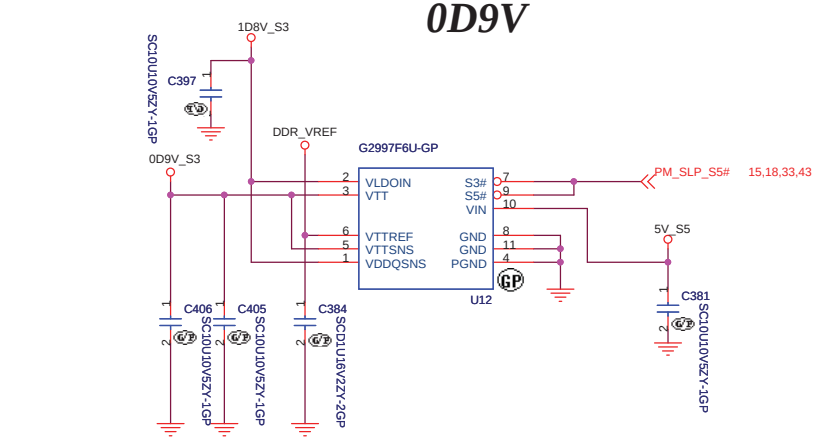
Title	CPU CORE MAX8760(2/2)	
Size A3	Document Number MYALL M	Rev SA
Date: Friday, June 16, 2006	Sheet 40 of 59	

SYSTEM DC/DC
3D3V_S5 / 5V_S5

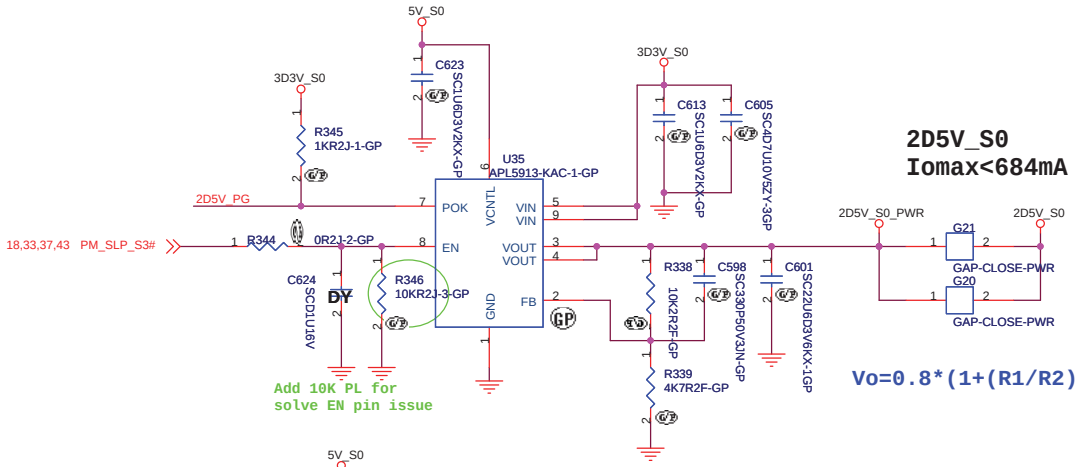


Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: MAX8734 3D3V/5V		
Size: A3	Document Number: MYALL M	Rev: SA
Date: Friday, June 16, 2006	Sheet 41 of 59	

0D9V

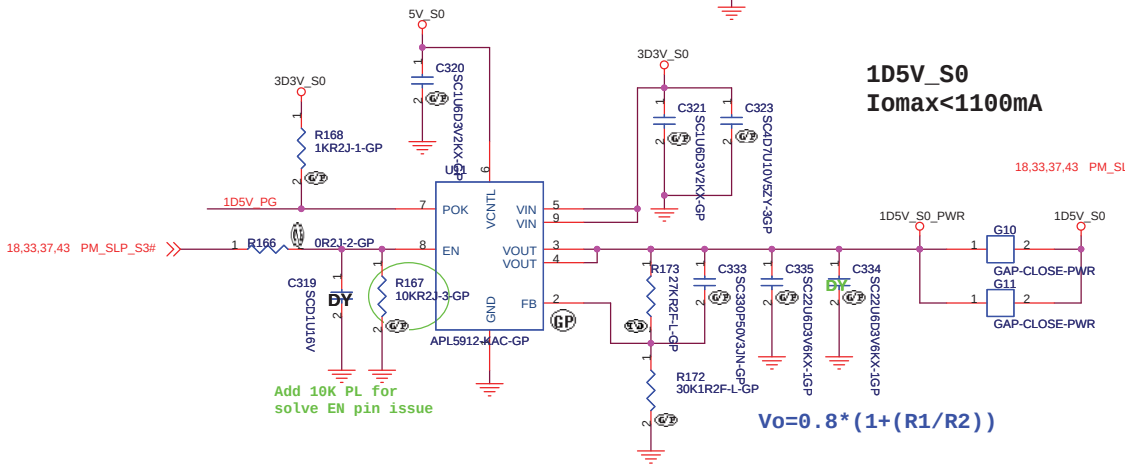


2D5V_S0
Iomax<684mA



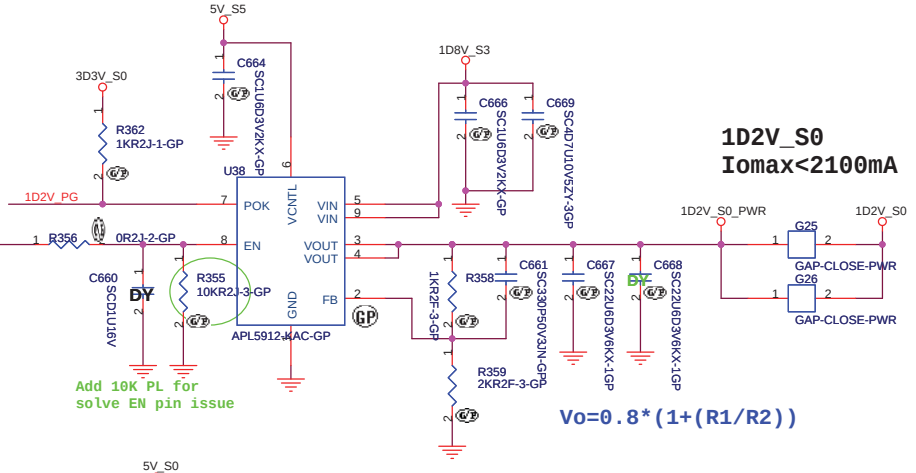
Vo=0.8*(1+(R1/R2))

1D5V_S0
Iomax<1100mA



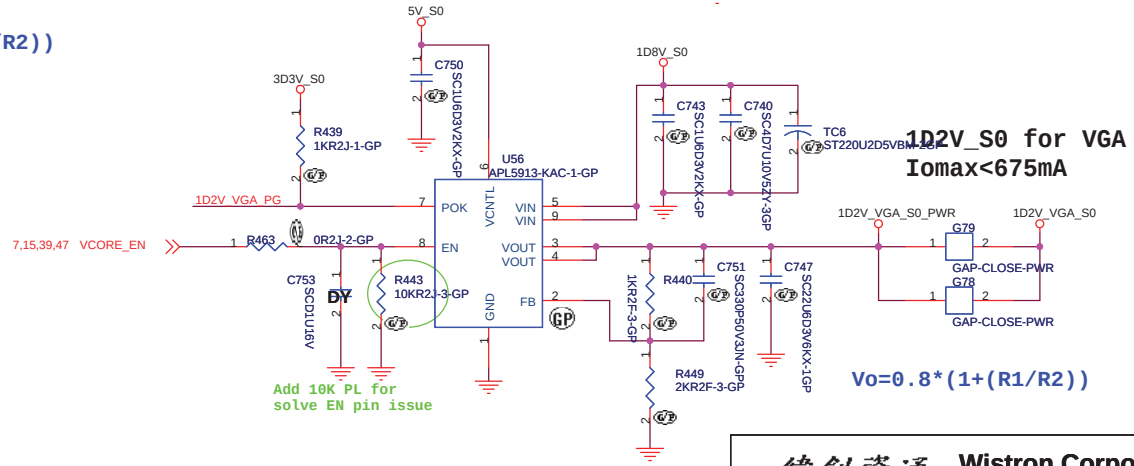
Vo=0.8*(1+(R1/R2))

1D2V_S0
Iomax<2100mA



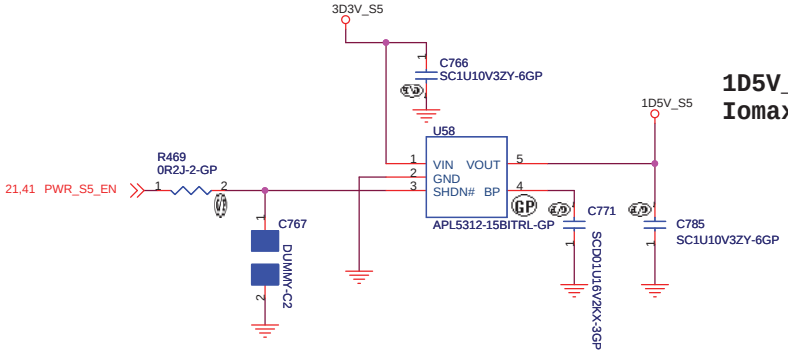
Vo=0.8*(1+(R1/R2))

1D2V_S0 for VGA
Iomax<675mA

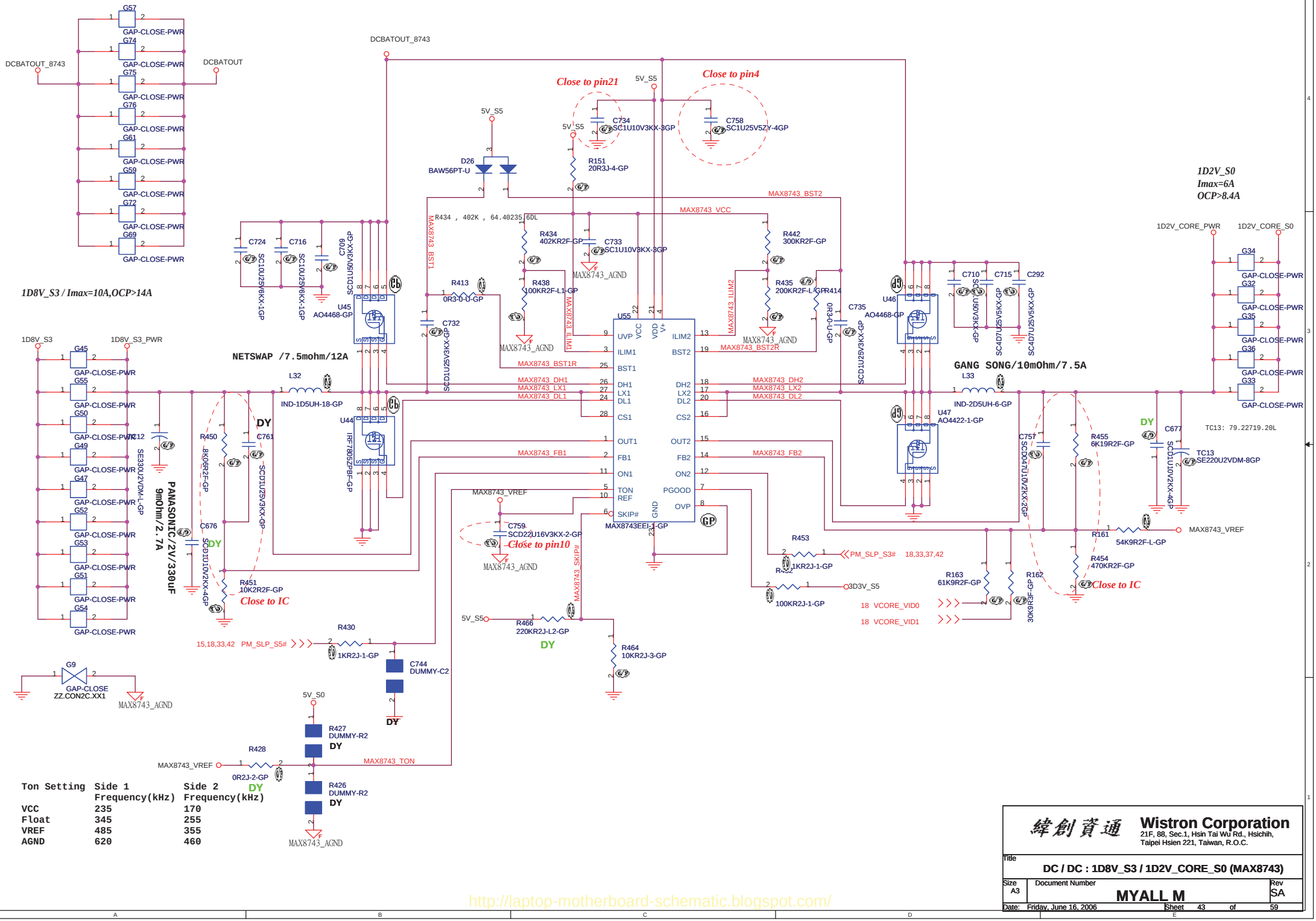


Vo=0.8*(1+(R1/R2))

1D5V_S5
Iomax<100mA



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	2D5V_S0/1D5V_S0/0D9V/1D2(LD	
Size A3	Document Number: MYALL M	Rev SA
Date: Friday, June 16, 2006	Sheet 42 of 59	

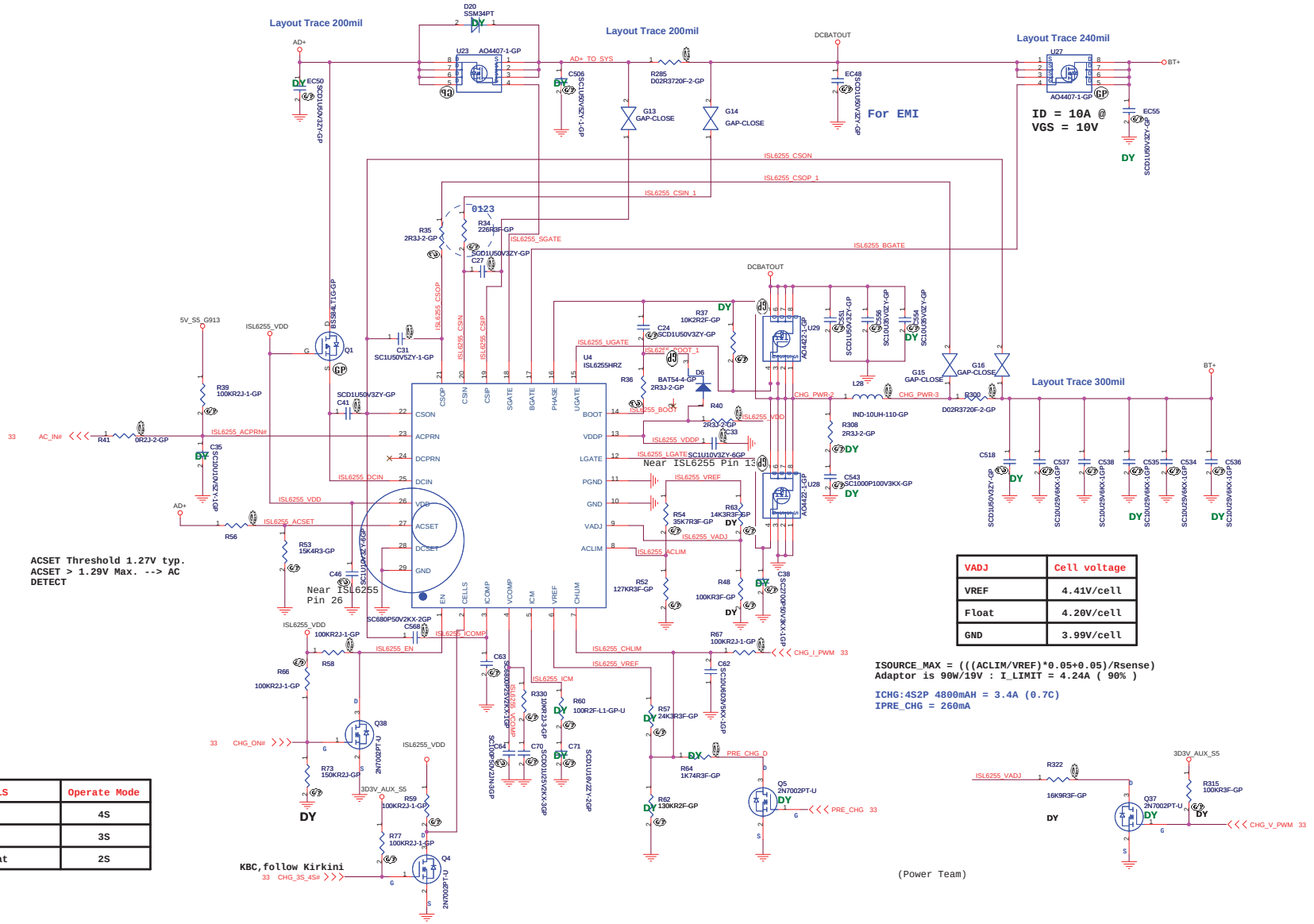


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC / DC : 1D8V_S3 / 1D2V_CORE_S0 (MAX8743)

Size: A3 | Document Number: MYALL M | Rev: SA

Date: Friday, June 16, 2006 | Sheet 43 of 59



VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

<Variant Name>

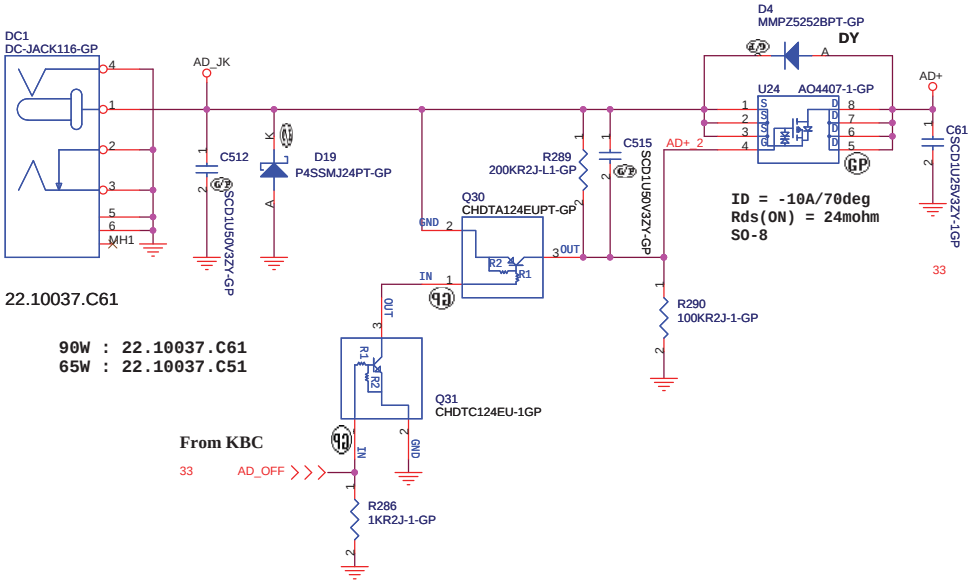
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL6255

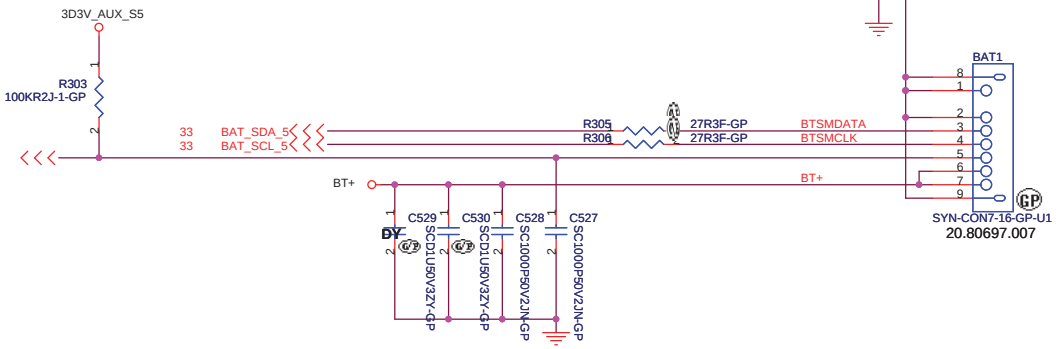
Size: A2 | Document Number: MYALL M | Rev: SA

Date: Friday, June 16, 2006 | Sheet 44 of 59

Adaptor-In to generate DCBATOUT

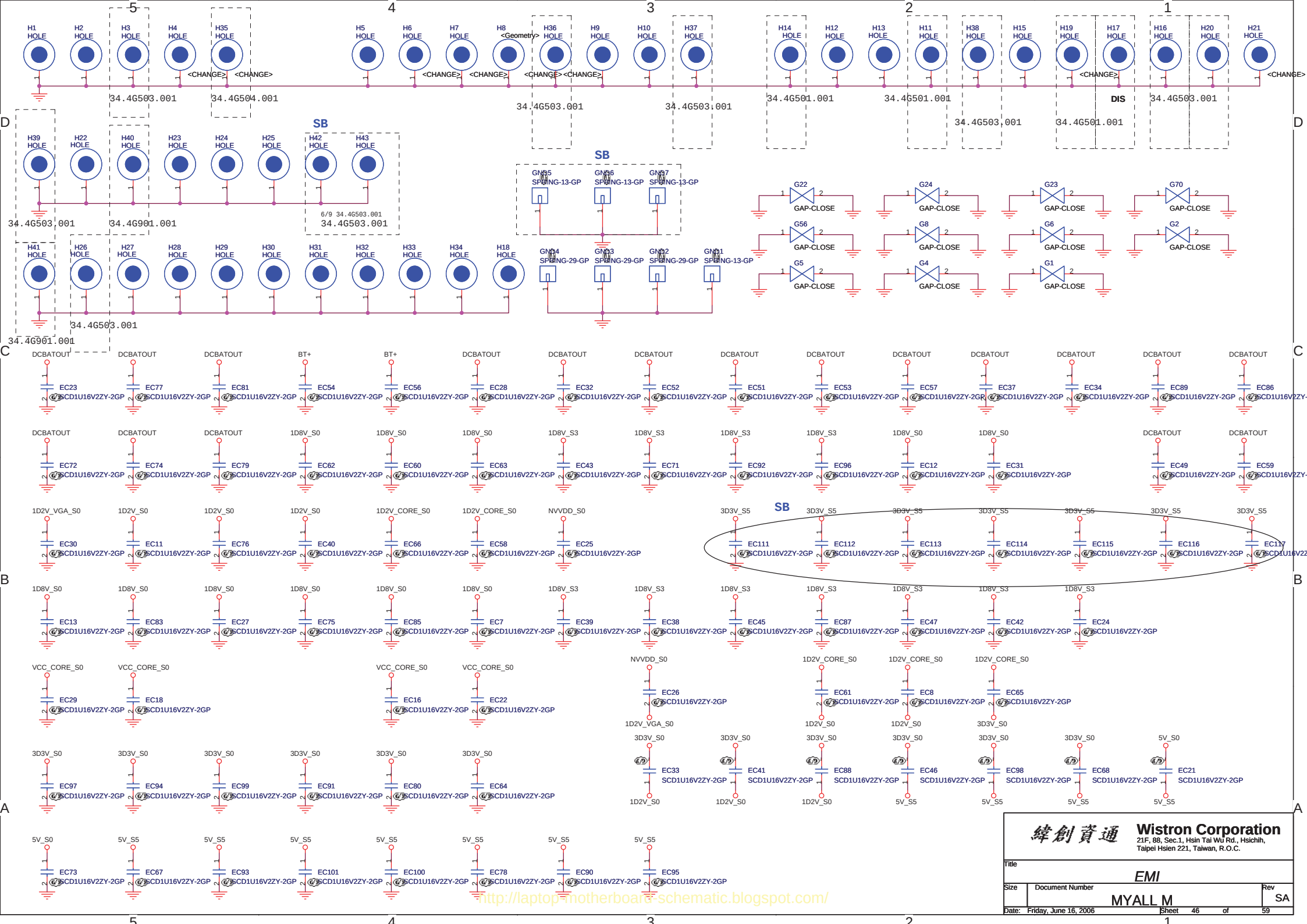


Battery connector



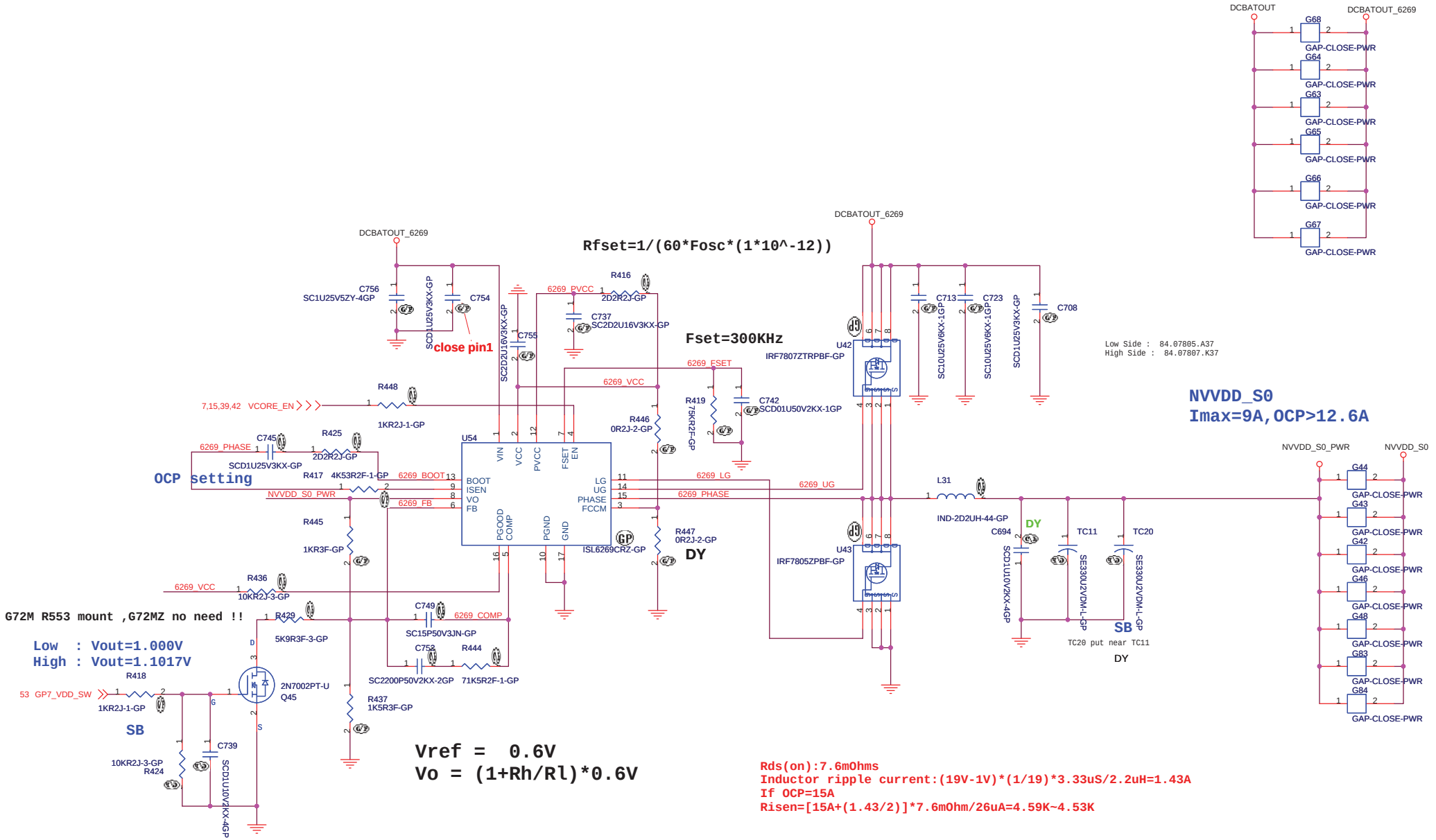
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size	Document Number: MYALL M	Rev: SA
Date: Friday, June 16, 2006	Sheet 45 of 59	

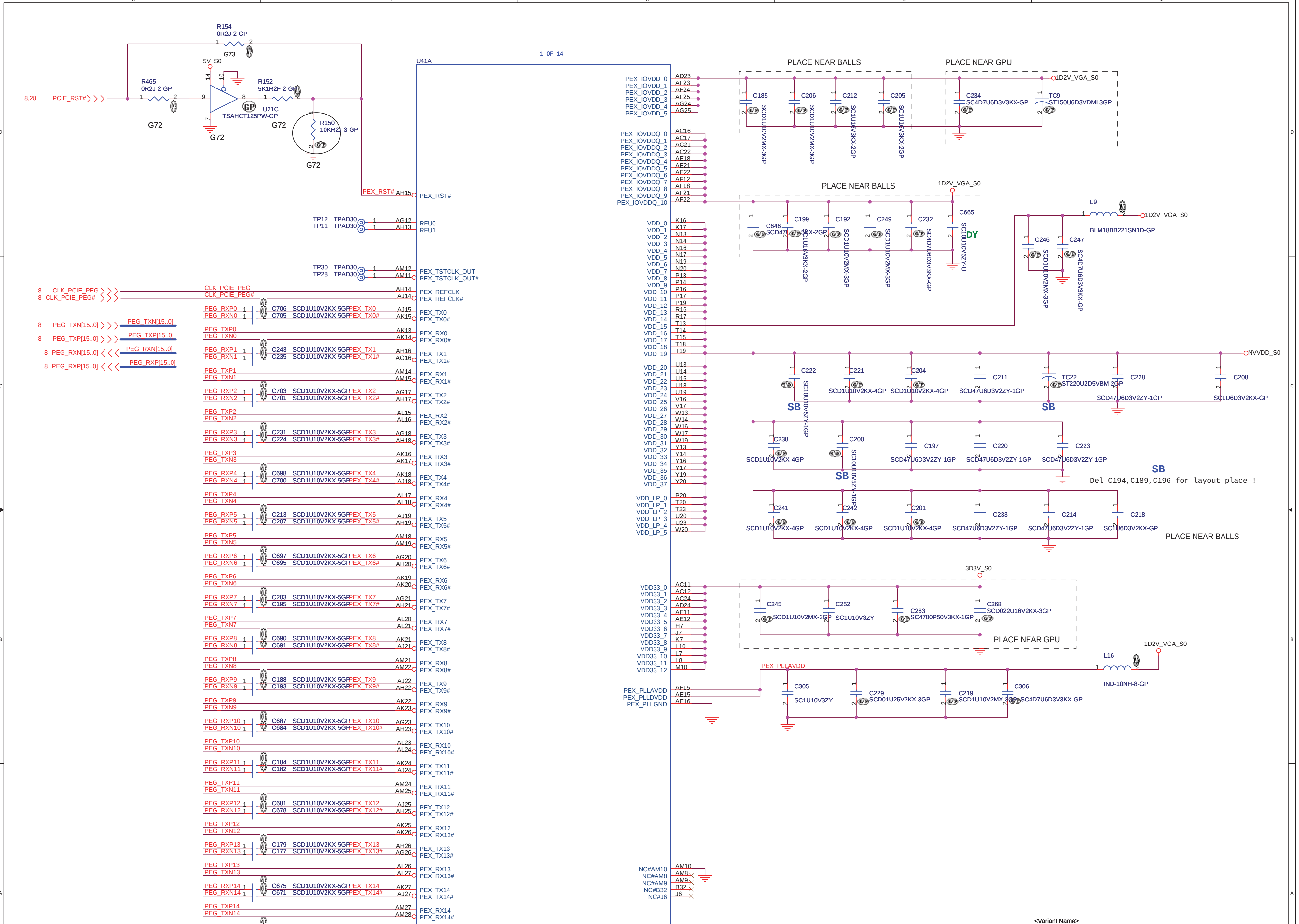


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	EMI	
Size	Document Number: MYALL M	Rev: SA
Date: Friday, June 16, 2006	Sheet 46 of 59	



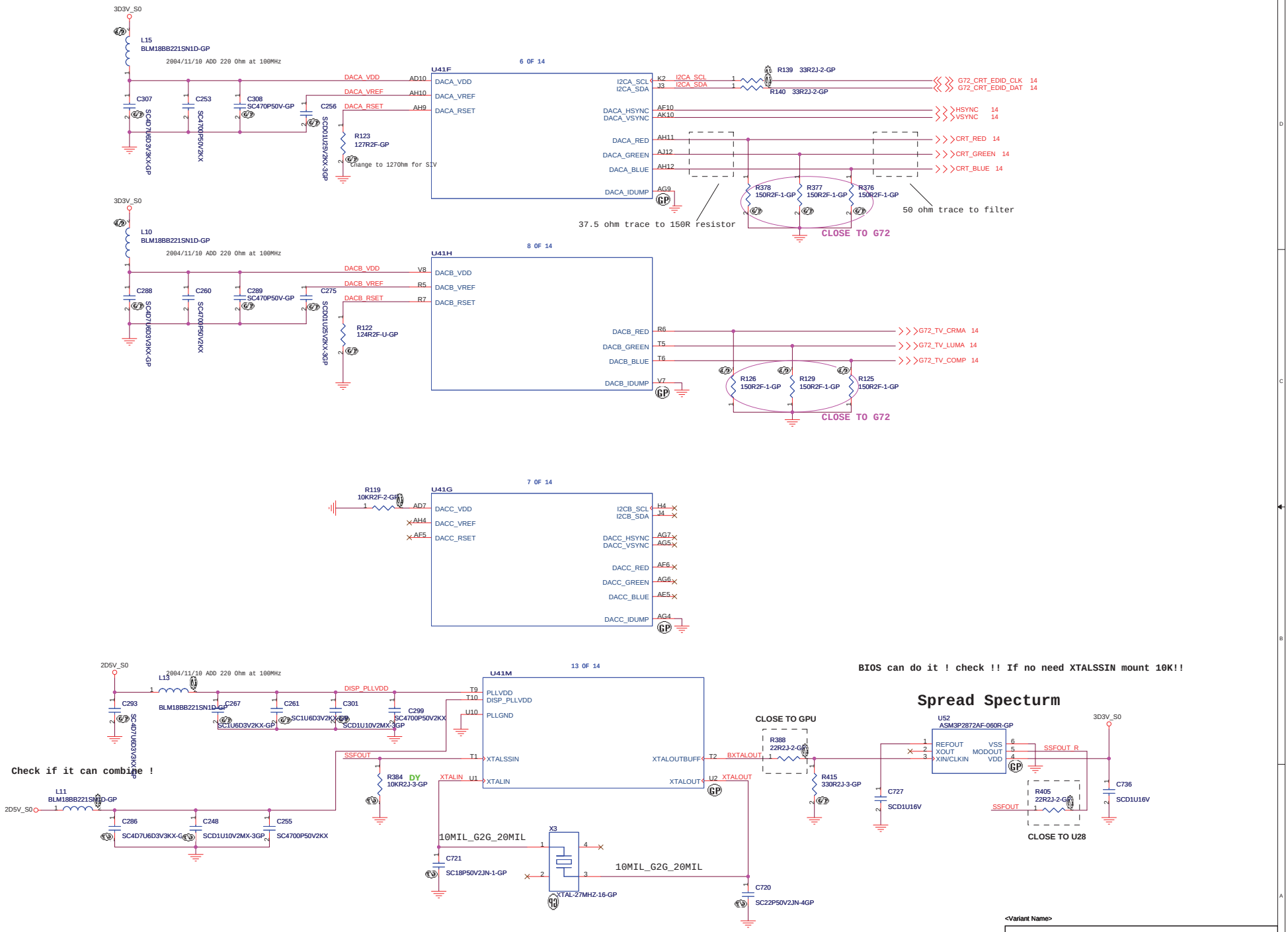
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DC/DC NVVDD_S0(ISL6269)		
Size A3	Document Number MYALL M		Rev SA
Date: Friday, June 16, 2006	Sheet 47 of 59		



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

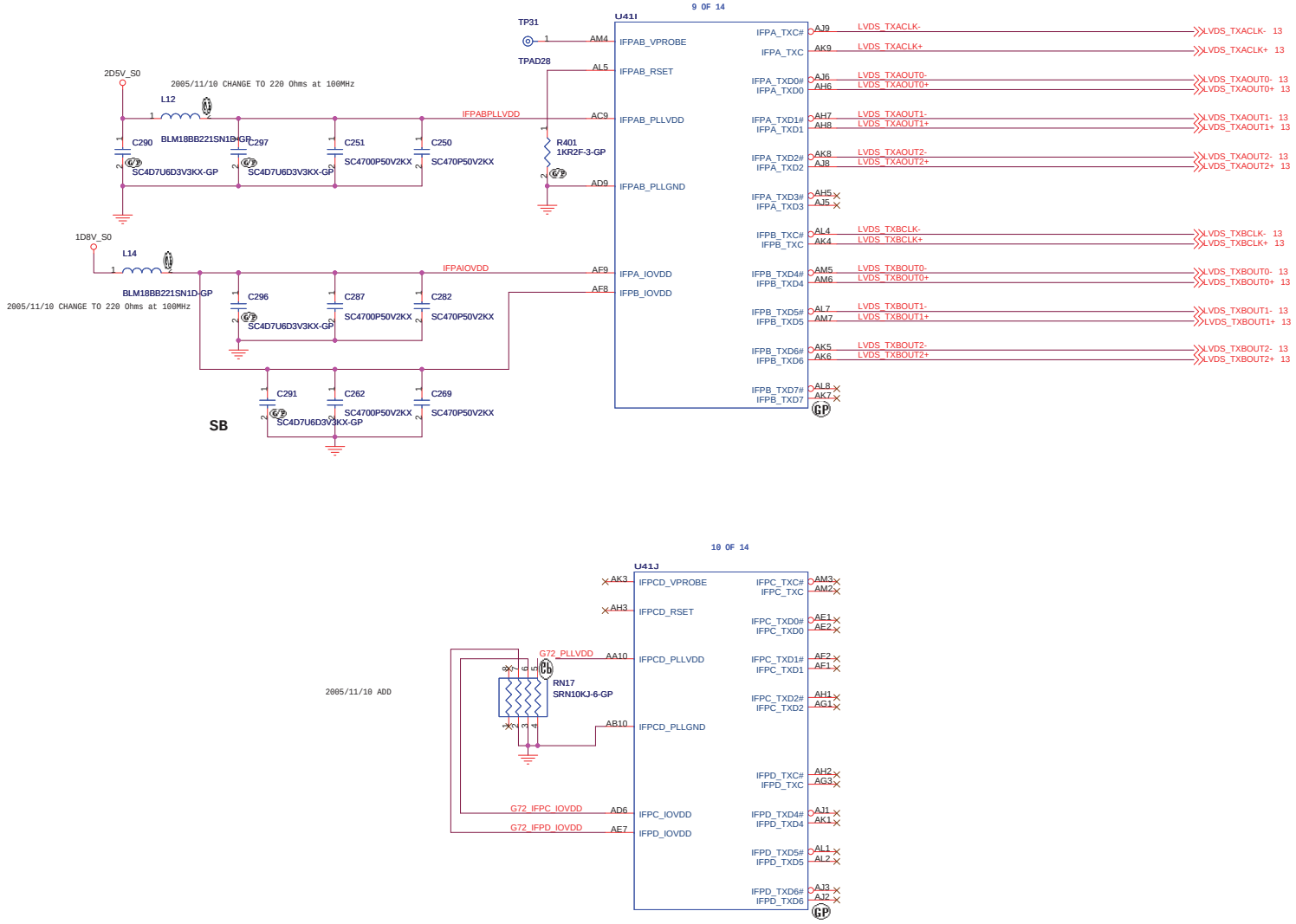
Title	G72M PCIE	
Size	Document Number: MYALL M	Rev: SA
Date: Friday, June 16, 2006	Sheet 48 of 59	



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G72M CRT & TV OUT	
Size	Document Number: MYALL M	Rev: SA
Date: Friday, June 16, 2006	Sheet 49 of 59	



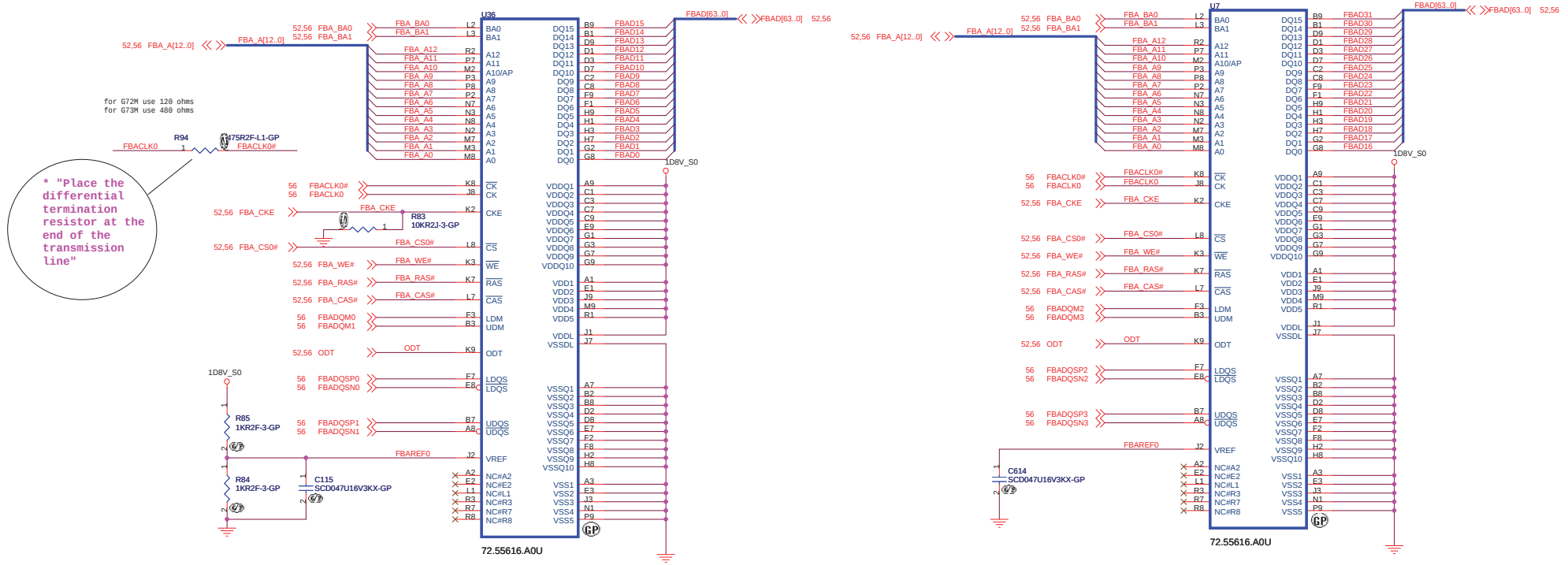
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

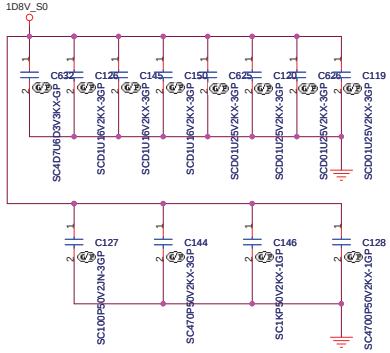
Title: G72M LVDS & TMDS

Size | Document Number: MYALL M | Rev: SA

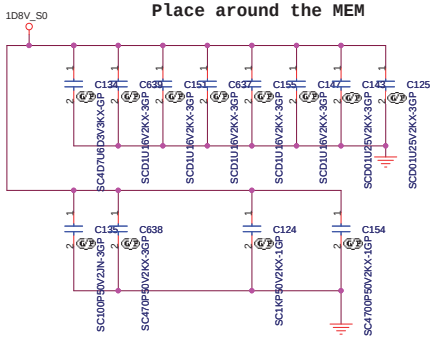
Date: Friday, June 16, 2006 | Sheet 50 of 59



Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M*16, 400Mhz)
72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGAby Hynix (16M*16, 400Mhz)
72.18512.A0U IC VRAM HY5PS121621BFP-25 FBGA by Infineon (32M*16, 400Mhz)
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA, by Infineon(16M*16, 400Mhz)

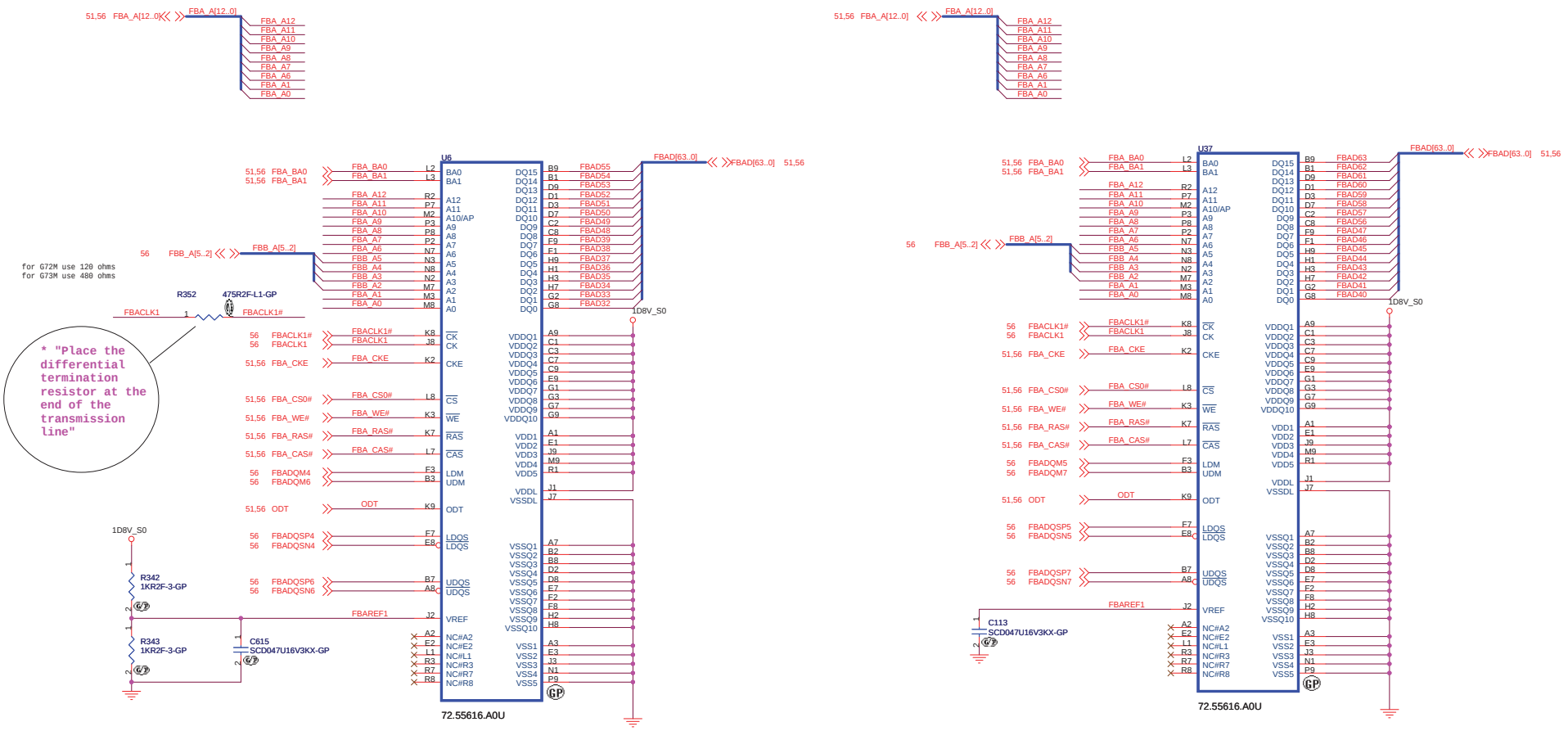
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

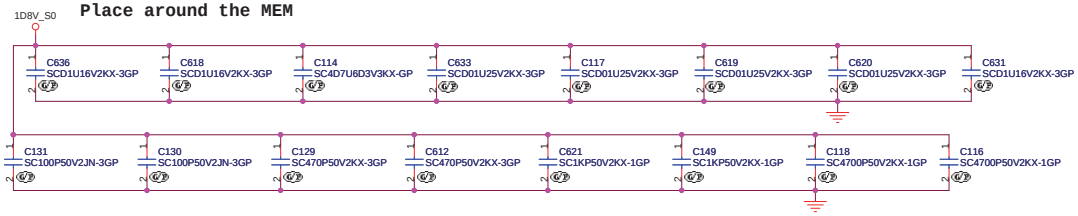
Title: G72M VRAM (1ST 1/2)

Size	Document Number	Rev
	MYALL M	SA

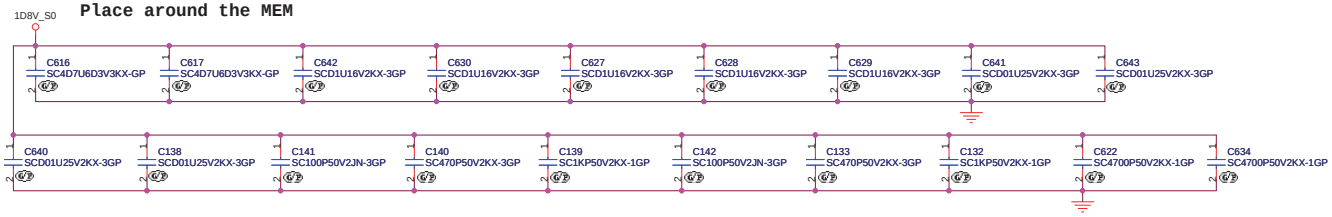
Date: Friday, June 16, 2006 Sheet 51 of 59



Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



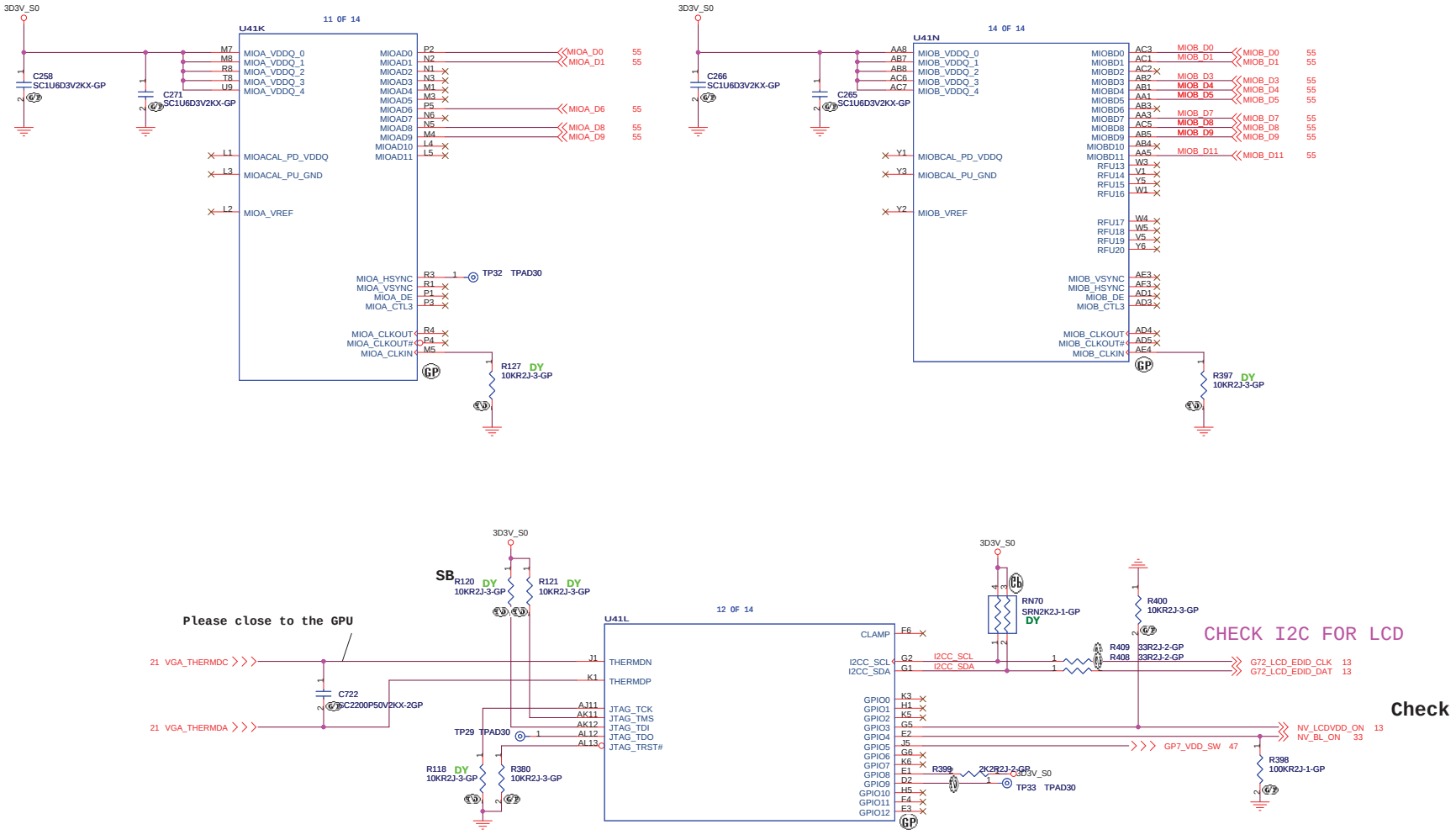
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M VRAM (1ST 2/2)

Size | Document Number: MYALL M | Rev: SA

Date: Friday, June 16, 2006 | Sheet 52 of 59



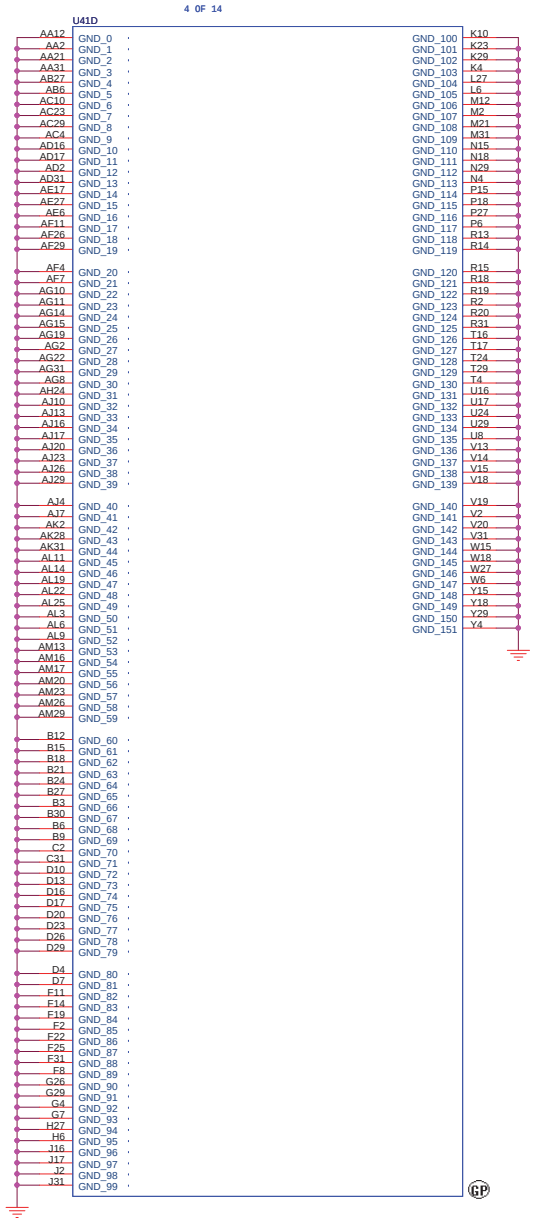
<Variant Name>

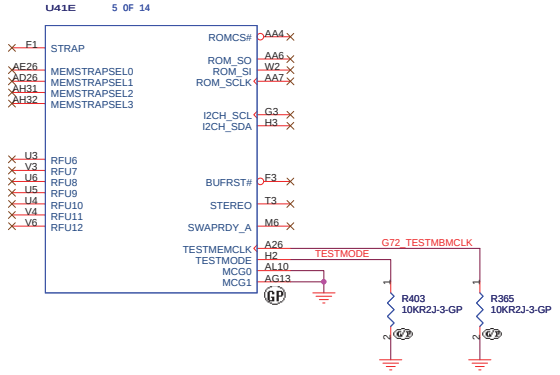
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M THERMAL

Size	Document Number	Rev
	MYALL M	SA

Date: Friday, June 16, 2006 Sheet 53 of 59





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M ROM & Spread Specturm

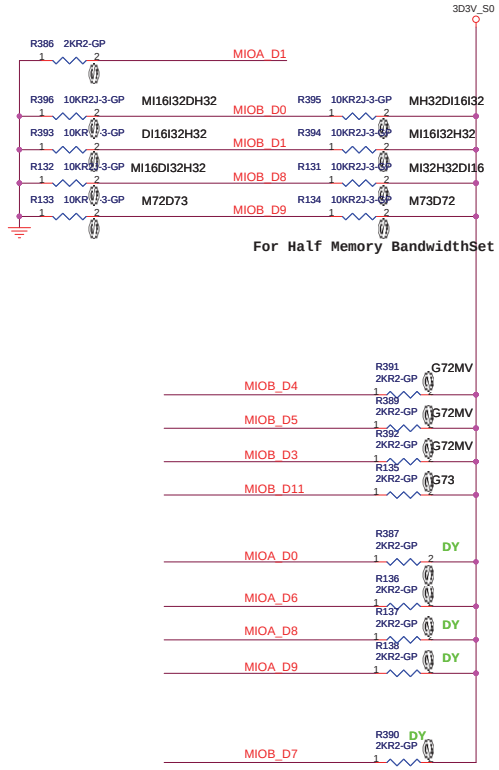
Size	Document Number	Rev
	MYALL M	SA

Date: Friday, June 16, 2006 Sheet 54 of 59

STRAPS, Mechanical Parts

Check

Hynix256MB :	R364_0	R93_1	R86_1	R91_1
Hynix128MB :	R364_0	R370_0	R86_1	R91_1
Hynix64MB :	R85_1	R370_0	R86_1	R91_1
Infineon256MB :	R364_0	R93_1	R86_1	R369_0
Infineon128MB :	R364_0	R370_0	R86_1	R369_0
Infineon64MB :	R85_1	R370_0	R86_1	R369_0



53	MIOA_D0	MIOA_D0
53	MIOA_D1	MIOA_D1
53	MIOA_D6	MIOA_D6
53	MIOA_D8	MIOA_D8
53	MIOA_D9	MIOA_D9

53	MIOB_D0	MIOB_D0
53	MIOB_D1	MIOB_D1
53	MIOB_D3	MIOB_D3
53	MIOB_D4	MIOB_D4
53	MIOB_D5	MIOB_D5
53	MIOB_D7	MIOB_D7
53	MIOB_D8	MIOB_D8
53	MIOB_D9	MIOB_D9
53	MIOB_D11	MIOB_D11

	Bit Signal	Values	
MIOA_D1:	SUB_VENDOR	0 NO_BIOS 1 READ FROM BIOS	
MIOB_D0: MIOB_D1: MIOB_D8: MIOB_D9:	RAM_CFG_0 RAM_CFG_1 RAM_CFG_2 RAM_CFG_3	0000 RFU 0001 8Mx32 BGA 1.8V 0010 RFU 0011 RFU 0100 4Mx32 BGA 1.8V 0101 RFU 0110 RFU 0111 RFU 0011 16MX16	1000 RFU 1001 RFU 1010 RFU 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 RFU
MIOB_D2: MIOB_D6:	CRYSTAL_0 CRYSTAL_1	00 13.500 MHz 01 14.31818 MHz 10 27.000 MHz 11 UNKNOWN	
MIOA_D7: MIOA_D10:	TV_MODE_0 TV_MODE_1	00 SECAM 01 NTSC 10 PAL 11 CRT	
MIOB_D4: MIOB_D5: MIOB_D3: MIOB_D11:	PCI_DEVID_0 PCI_DEVID_1 PCI_DEVID_2 PCI_DEVID_3	1000 (default 0x00FC) 0111 G72MV	**G72MZ=6,G73=8**
MIOA_D0:	PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED	
MIOA_D6: MIOA_D8: MIOA_D9:	3GIO_PADCFG_LUT_ADDR[0] 3GIO_PADCFG_LUT_ADDR[1] 3GIO_PADCFG_LUT_ADDR[2]	0 DESKTOP 1 MOBILE 010 DEFAULT	
MIOB_D7:	MOBILE_GPIO	0 GPIO_PULLDN 1 GPIO_FLOAT	

For MEM strapping, Please use below table:

RAM_CFG[3:0]	Config	FB Bus Width	Definitions
0000	16Mx16 DDR2	64-bit	Elpida
0001	16Mx16 DDR2	64-bit	Samsung
0010	16Mx16 DDR2	64-bit	Infineon
0011	16Mx16 DDR2	64-bit	Hynix
0100	32Mx16 DDR2	64-bit	Elpida
0101	32Mx16 DDR2	64-bit	Samsung
0110	32Mx16 DDR2	64-bit	Infineon
0111	32Mx16 DDR2	64-bit	Hynix

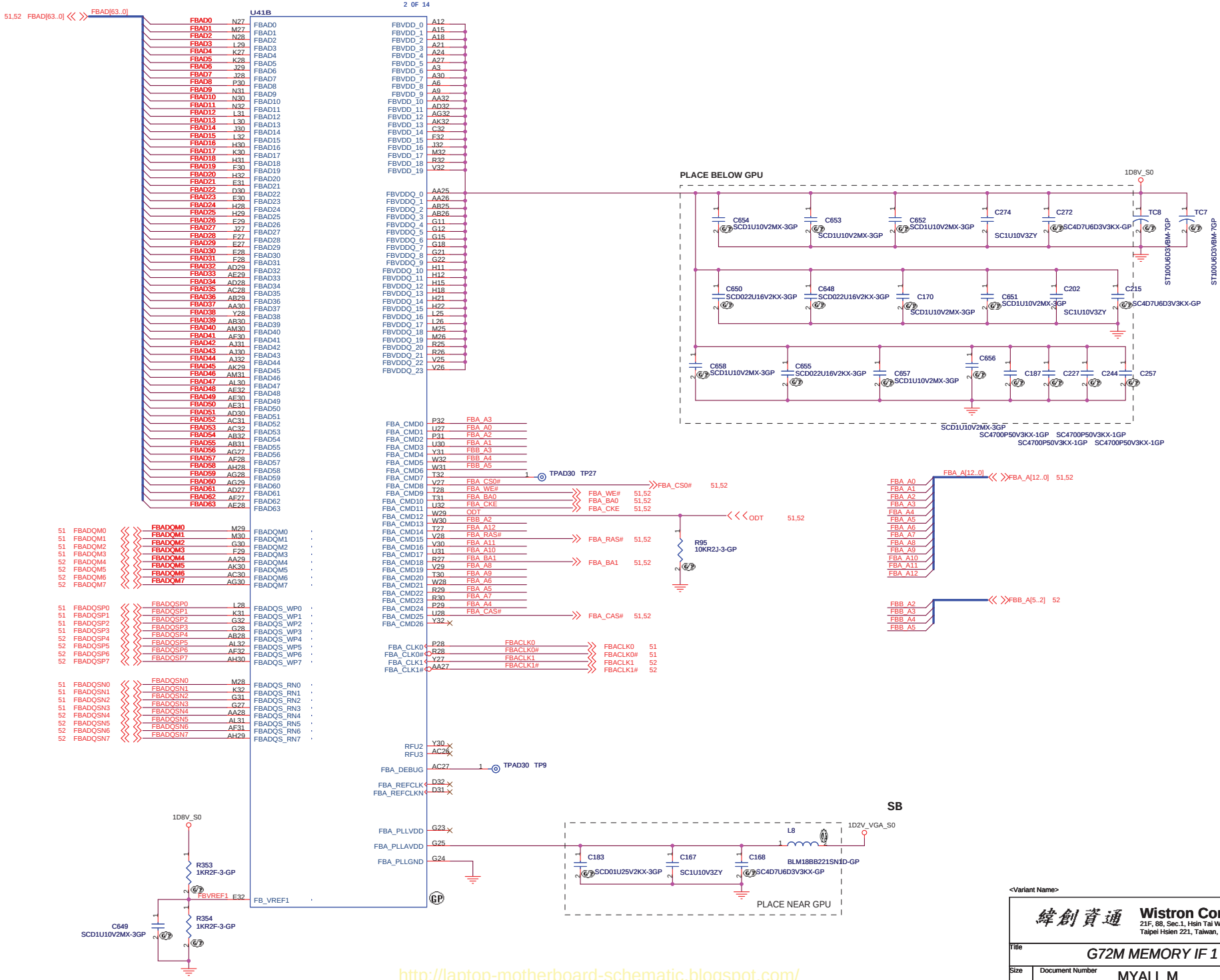
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *G72M STRAPPING*

Size | Document Number: MYALL M | Rev: SA

Date: Friday, June 16, 2006 | Sheet 55 of 59



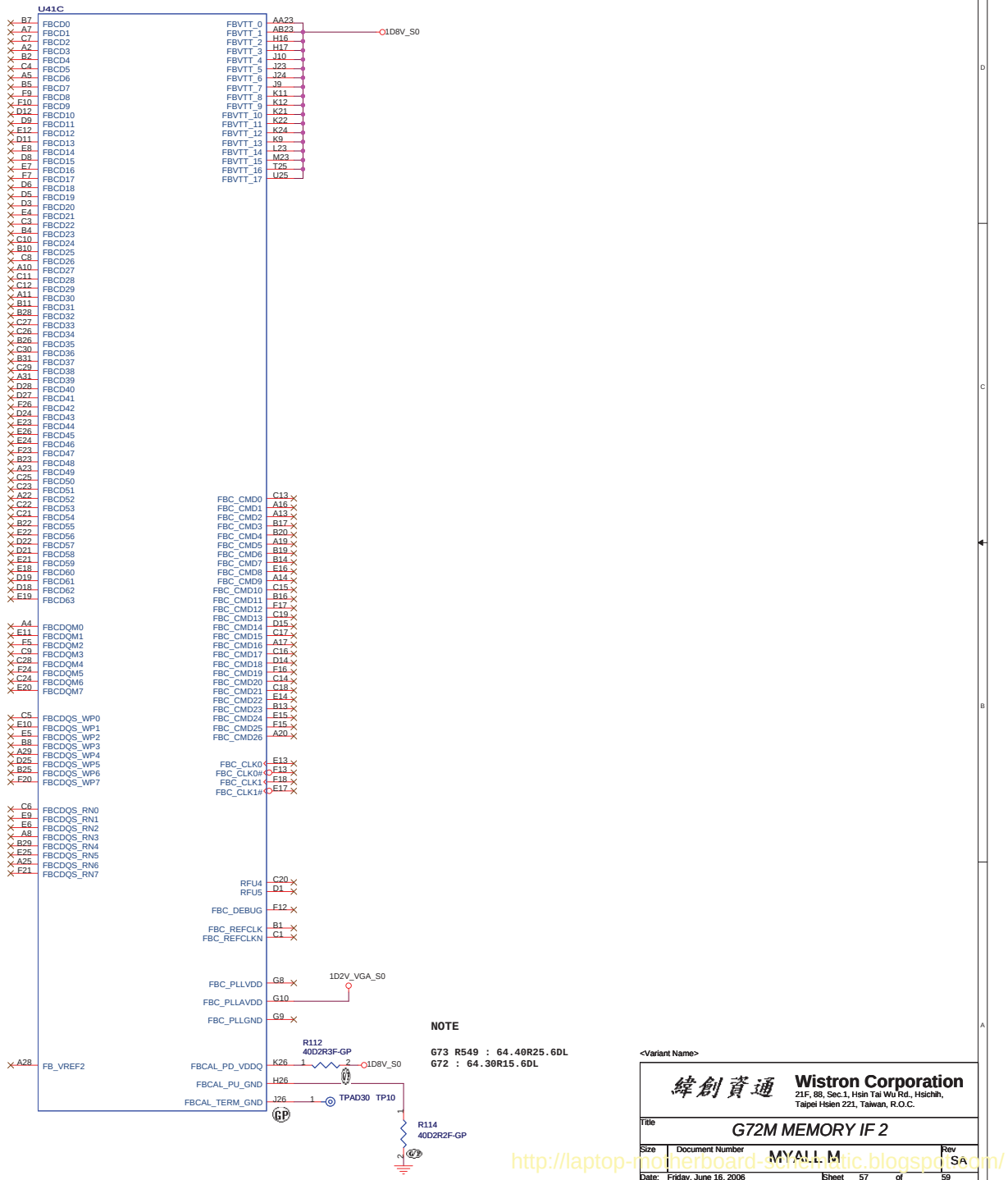
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *G72M MEMORY IF 1*

Size | Document Number: MYALL M | Rev: SA

Date: Friday, June 16, 2006 | Sheet 56 of 59



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M MEMORY IF 2

Size	Document Number	Rev
	MYALL M	SA

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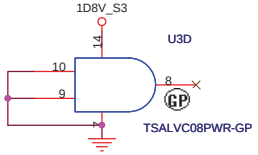

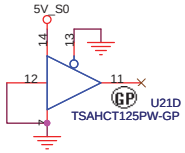

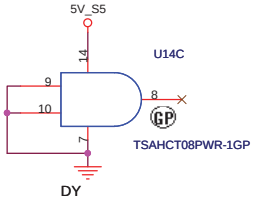

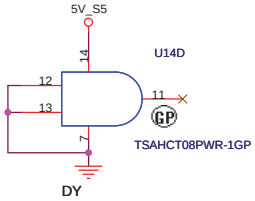

<Variant Name>

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SA

4/18 Add R414~R417 for headphone sound decrease

4/21 Add R718~R720,Q45~Q47 for discharge circuit
Add U68,R721~R725 ,C917~C923 for 1D2V_S0
Add U69,R726~R730,C924~C929 for 1D2V_VGA_S0

4/24 Update GPIO ,check Lan , Add bead into NB,SB's power

4/26 Correct CRT,TV bead and cap , Add EMI cap ,Change Transformer according vender's suggest

4/28 Change spec to Phy

5/4 Reduce Lan cap

SB

5/18 R144 chang to 64.30R15.6DL,Correct SB P/N

5/25 Correct VRAM setting; D9 become mount , C79 become 1u for sometimes can't power on !

6/1 Del RN9 for redudant ; Correct BTSMDATA,BTSMCLK;Dummy R244,EC102~EC104; Change C451,C458 to 4.7u ! ; U20 mount , R248 Dummy; Del RN64-1 AMP_SHUTDOWN;
Change XF1 and XF2 CT to AVDD18 for WOL ;Change C504 to 78.1022N.24L; Add WEBCAM_PW_SW at KBC GPIO27, and U66,F1,F2,C875,R284
6/5 Power , CPU High Side : 84.79N03.037,Low Side : 84.32N03.037 ,Dummy Q42, Q44 ; R159 , 64.66515.6DL ;TC13 change to 79.22719.20L;
R434 change to 64.40235.6DL;R404,R402 change to 64.18015.55L;Q21,R153,C311 Dummy ; Change SKU;Change U49,U50,U45,U46 to 84.04468.037
6/8 Q39 change to 84.27002.F31 ! Add D31,RN87,R576 for Leakage !(Ask KBC change DA2 to open drain);Change R111 source power to 5V_S5_G913

6/9 Add R577~R579 for Dis impedance; Add H42,H43 for ME request;Correct AV-IN pin ;

6/10~13 Add U66,F1,F2,R284,C875 for power switch ! ; add R597,R598 for brightness choice from KBC or SB ; Del Q33,Q32 to reduce MOS ; Change RN37 to 0 Ohm;
Bluetooth_EN change to KBC control; Add CIR_DET(R586,R587);DY RN21 for redudant;Change X4 for vender's suggestion;change C34 and C30 for vender's suggestion;
Add TC21 for accoustic noise;add EC105~EC111,Mount ERC7,ERC8,GND5~GND7 for EMI request;

6/14 Del R46,Change R47 to bigger one ,Change C55 to 10U,add C880 --> for 1D2V_S0 power quality

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