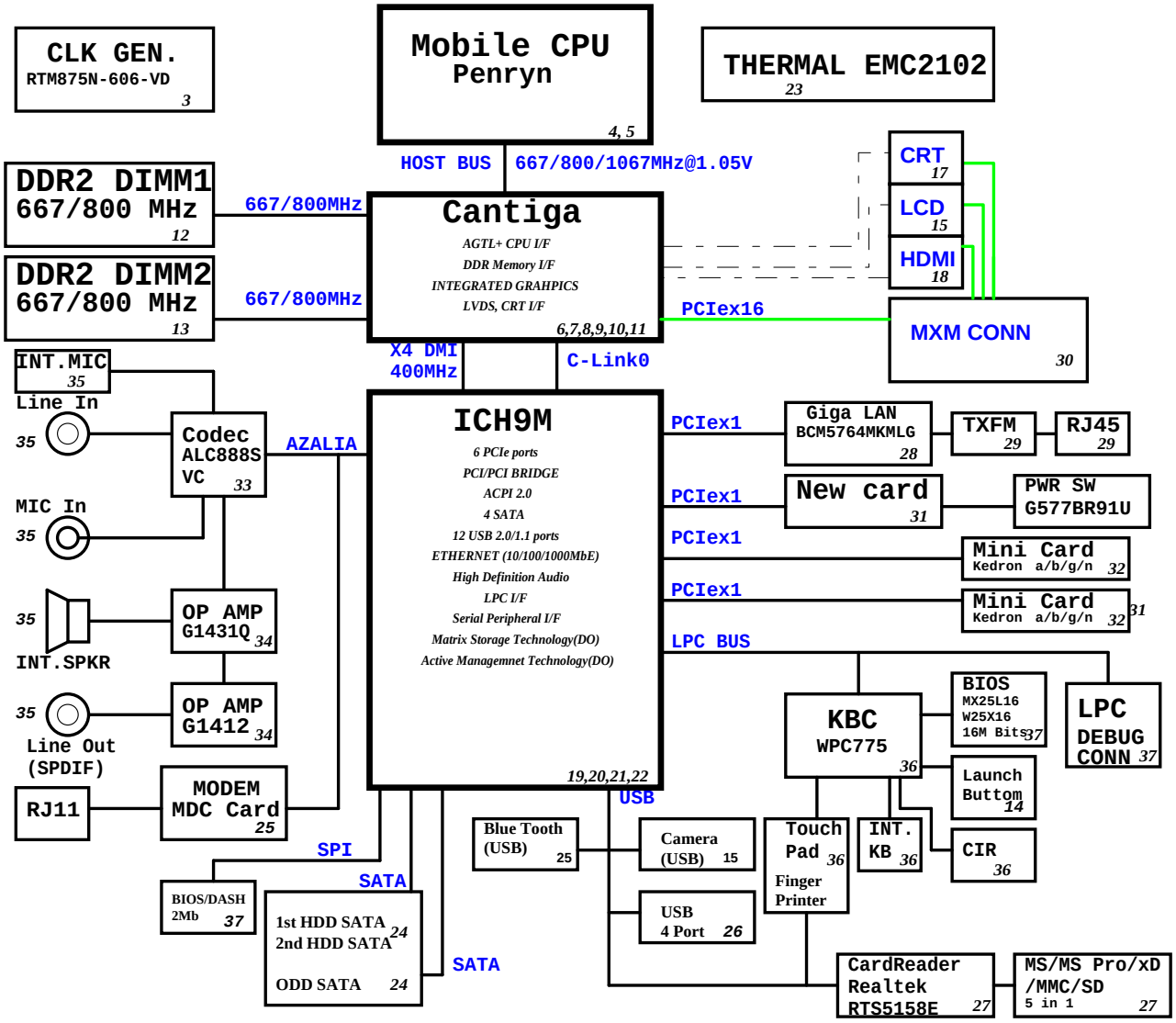
Big Bear 2 Block Diagram

Project code: 91.4AV01.001
PCB P/N : 48.4AV01.
REVISION : -1



PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

RT9026 44	
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

RT9018A 44	
1D8V_S3	1D5V_S0

G9131 44	
3D3V_S0	2D5V_S0

GFXCORE DC/DC ISL6263 46	
INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V

CPU DC/DC ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER BQ24745 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

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Title: BLOCK DIAGRAM

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

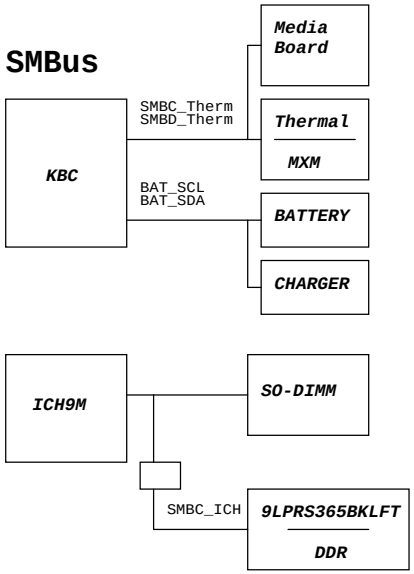
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN/TV
LANE4	JMB385 Card Reader
LANE5	NewCard
LANE6	*NC*

USB Table

USB	
Pair	*Device*
0	*USB1*
1	*USB4*
2	*USB2*
3	*USB5(DOCK)*
4	*USB3*
5	*Bluetooth*
6	*FP*
7	*MINIC1*
8	*WEBCAM*
9	*NEW1*
10	*MINIC2*
11	*NC*

SMBus



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Title: ***Reference***

Size: A3 | Document Number: **Big Bear 2** | Rev: **-1**

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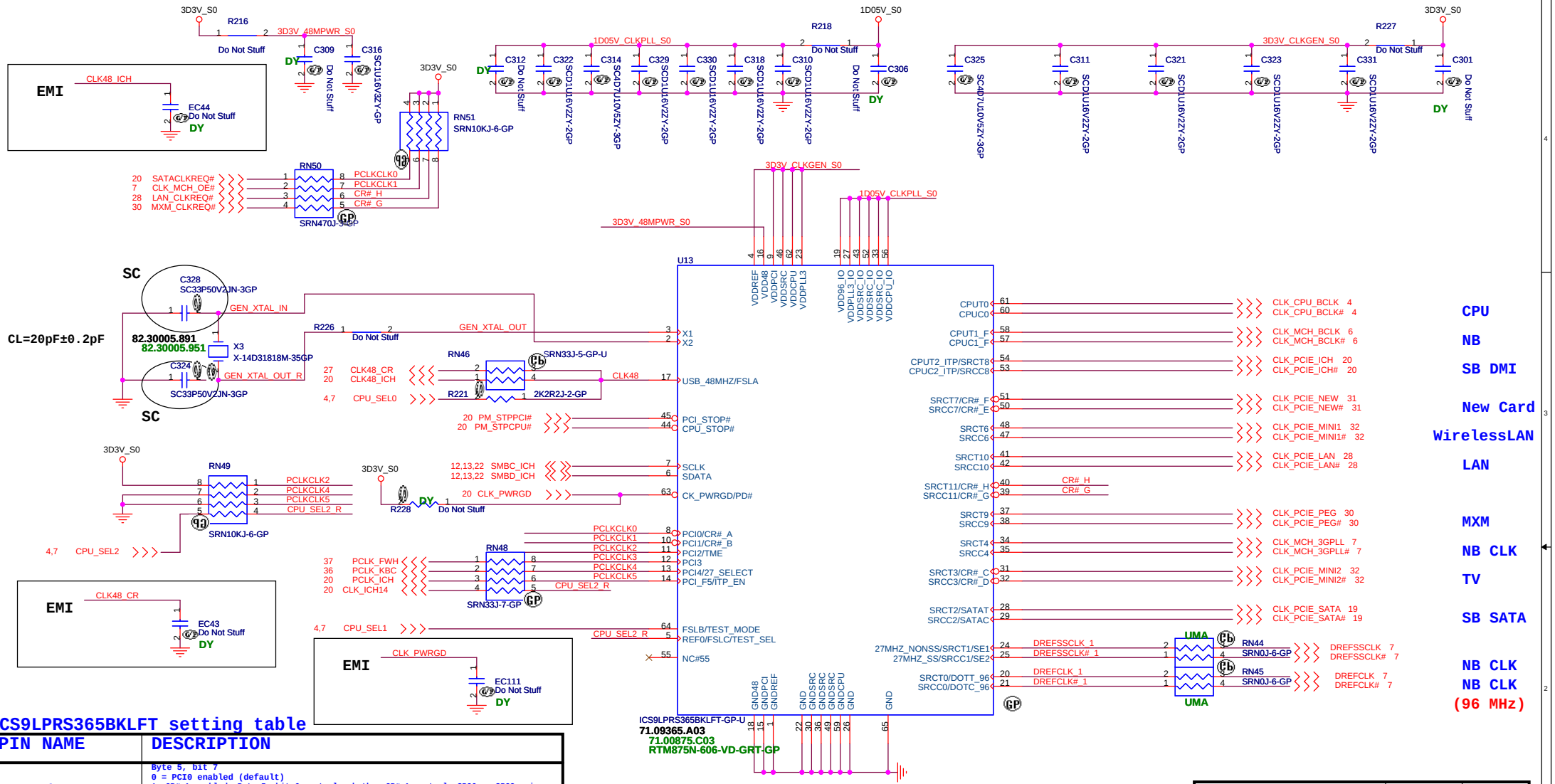

ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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Title: Clock Generator

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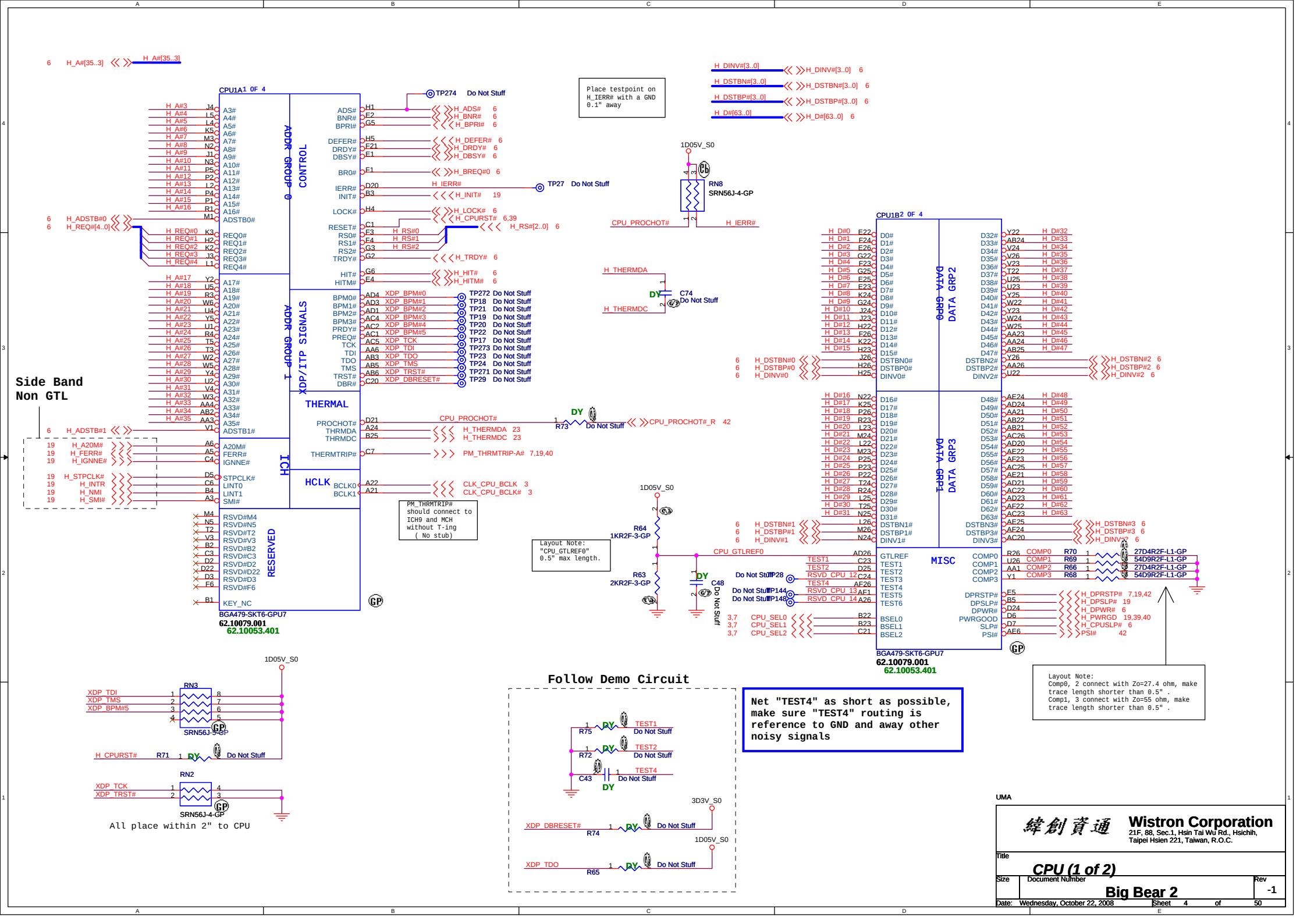
CPU1A 1 OF 4
CPU1B 2 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
DATA GRP2
DATA GRP0
DATA GRP3
DATA GRP1
MISC
BGA479-SKT6-GPU7
62.10079.001
62.10053.401
Side Band
Non GTL
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
Layout Note: "CPU_GTLREF0" 0.5" max length.
Follow Demo Circuit
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
All place within 2" to CPU
RN8 SRN56J-4-GP
RN3 SRN56J-5-GP
RN2 SRN56J-4-GP
Do Not Stuff
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Title
CPU (1 of 2)
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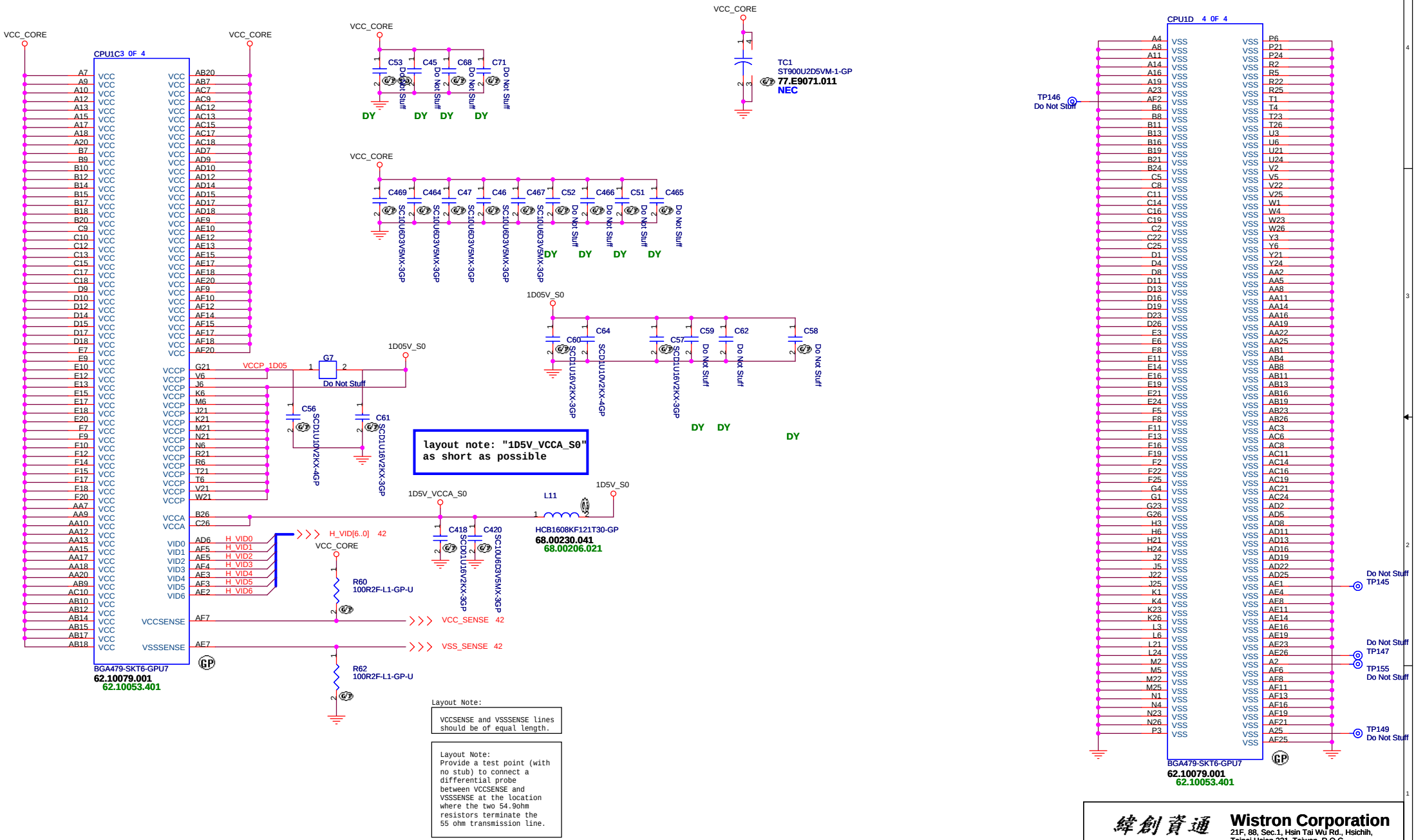

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Title: CPU (2 of 2)	
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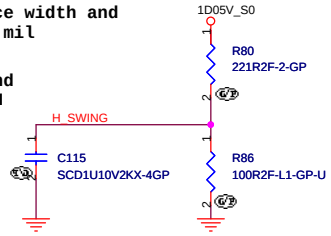
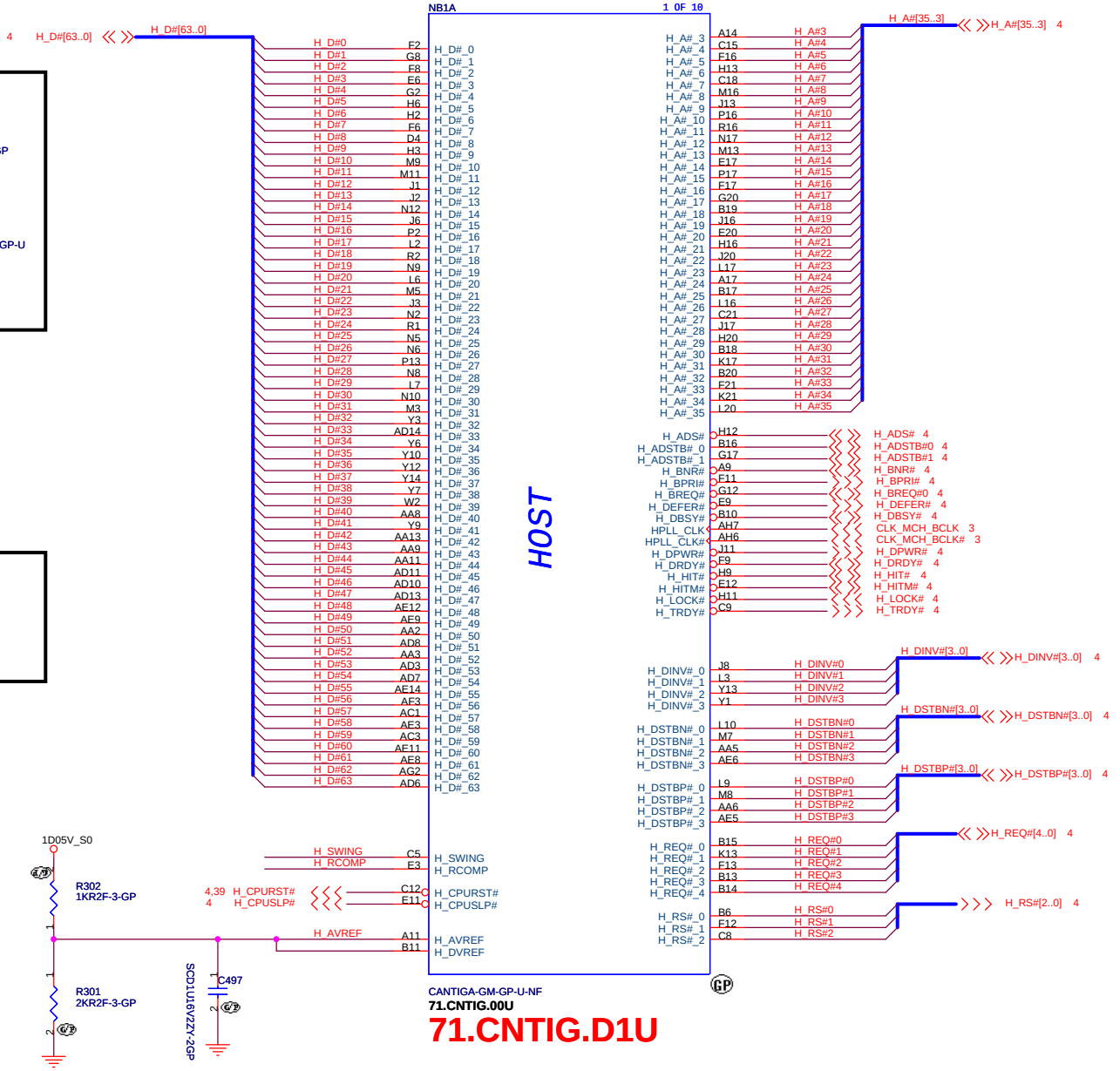
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



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Title: Cantiga (1 of 6)

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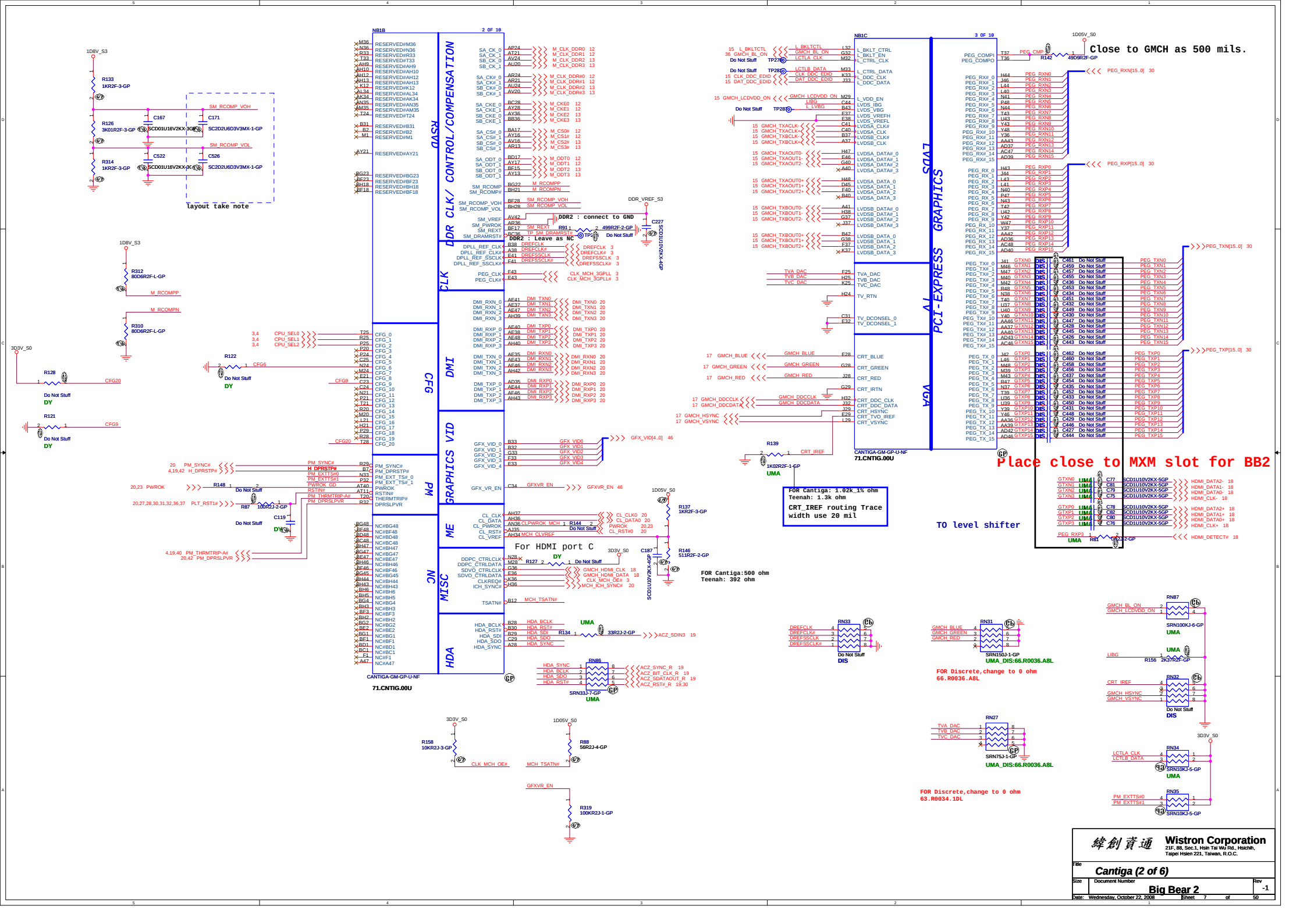
NB1B
2 OF 10
RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
HDA
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
NB1C
3 OF 10
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
Close to GMCH as 500 mils.
Place close to MXM slot for BB2
layout take note
DDR2 : connect to GND
DDR2 : Leave as NC
For HDMI port C
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
TO level shifter
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Discrete,change to 0 ohm
66.R0636.A8L
UMA_DIS:66.R0036.A8L
FOR Discrete,change to 0 ohm
63.R0034.1DL
UMA_DIS:66.R0036.A8L
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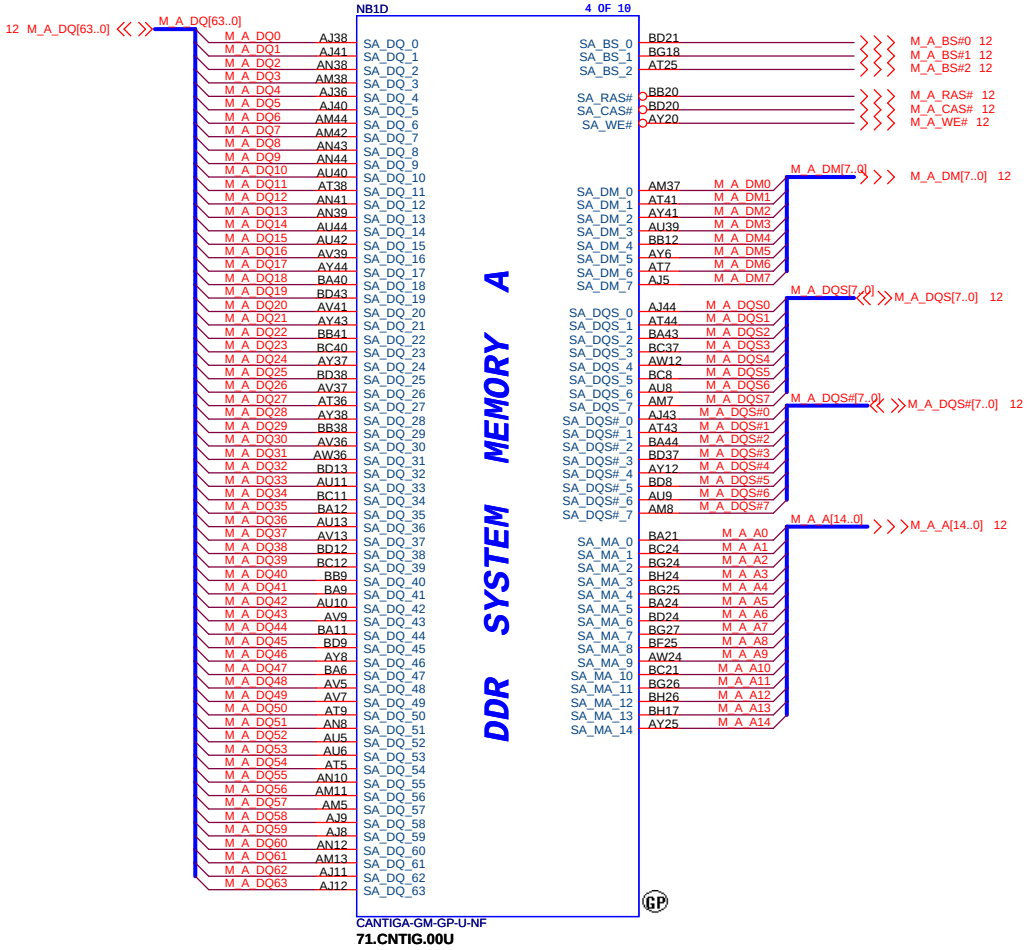
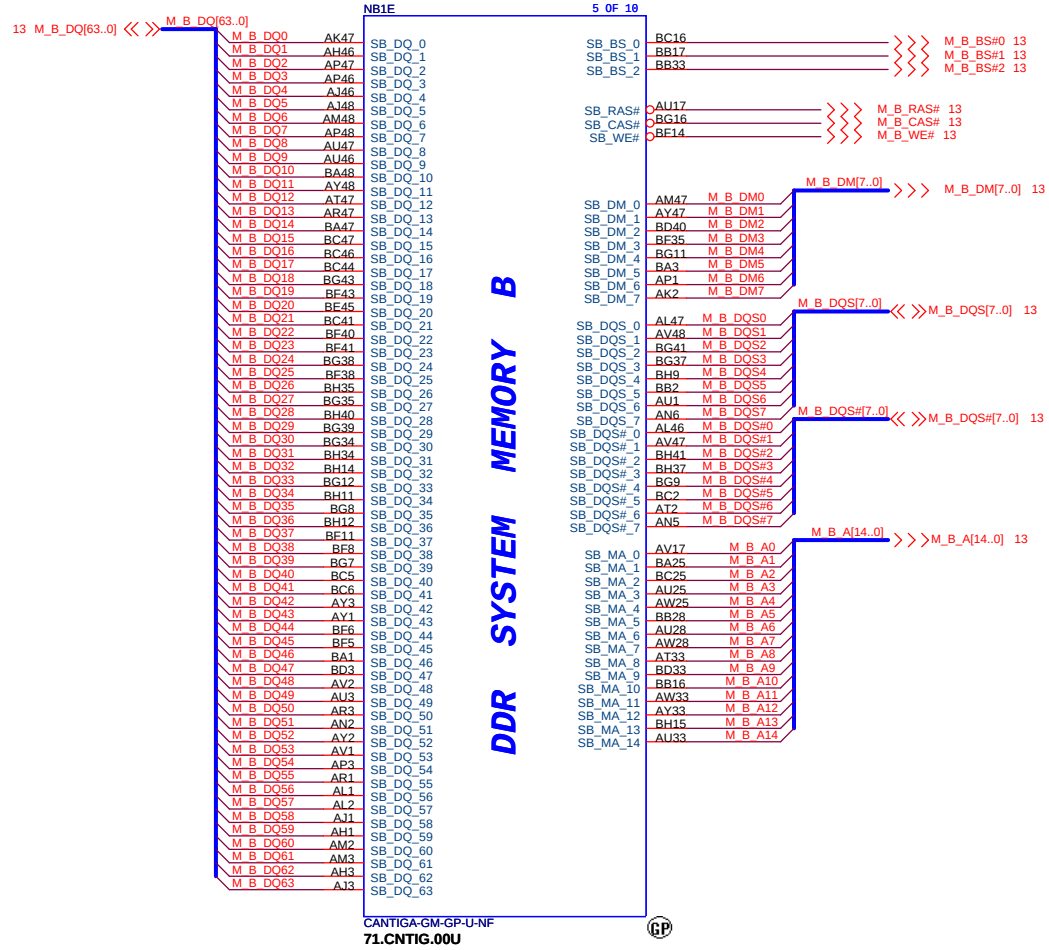
Cantiga (2 of 6)
Big Bear 2
Wednesday, October 22, 2008





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Title: Cantiga (3 of 6)

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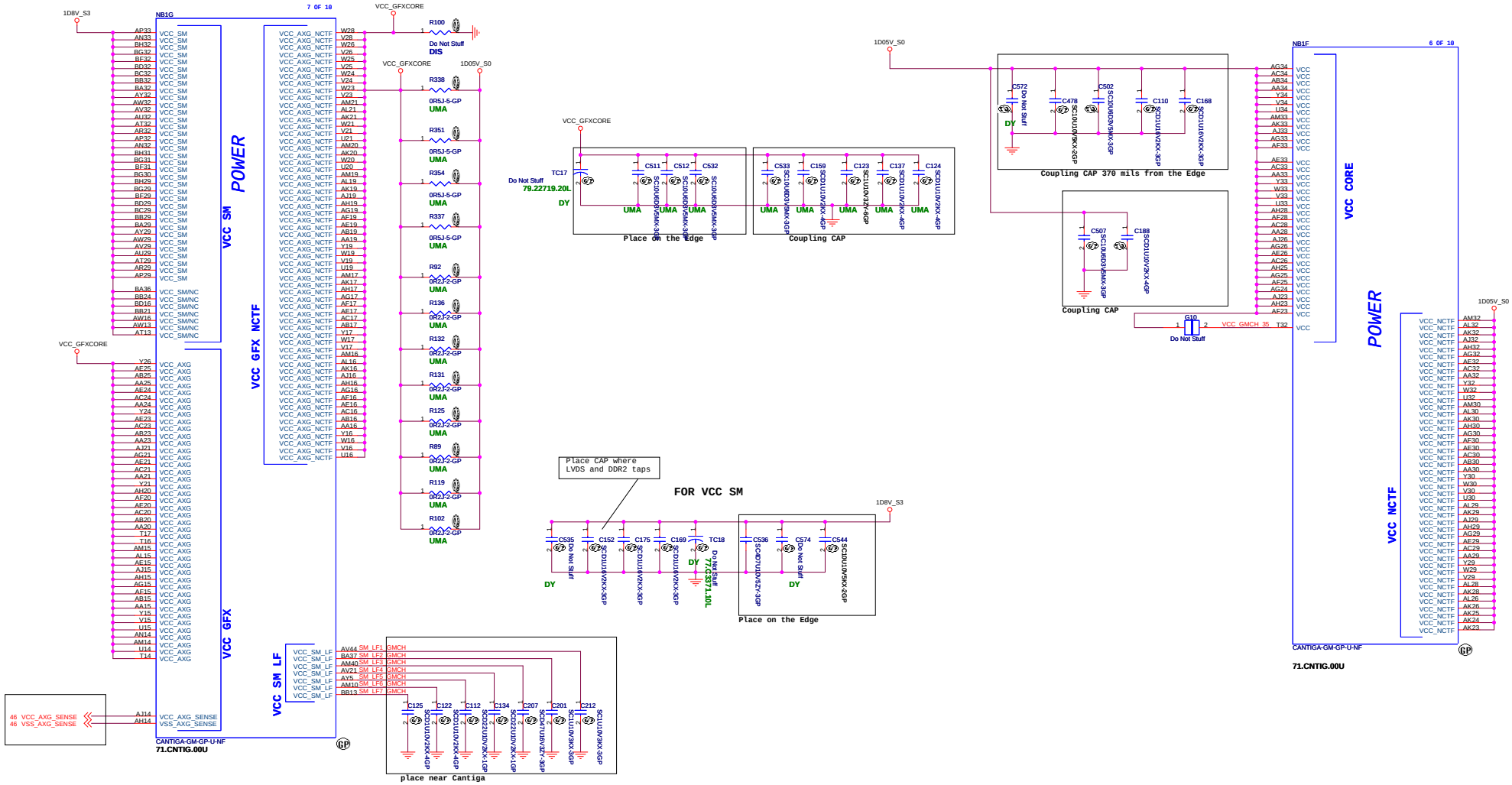

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Title	***Cantiga (4 of 6)***	
Size	Document Number: **Big Bear 2**	Rev: -1
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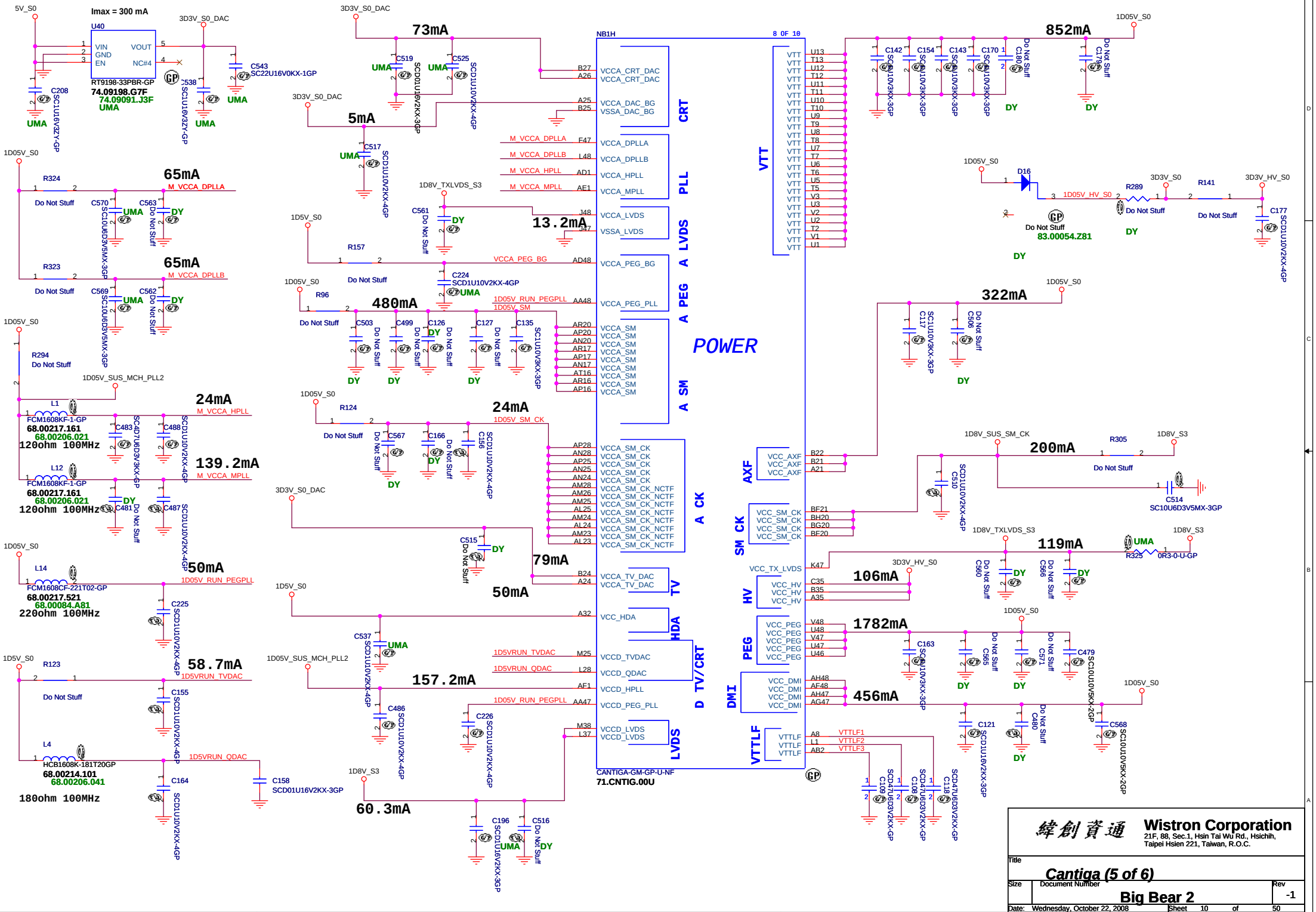
POWER
NB1H
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
Imax = 300 mA
RT9198-33PBR-GP
74.09198.G7F
74.09091.J3F
73mA
5mA
65mA
65mA
13.2mA
480mA
24mA
139.2mA
50mA
79mA
50mA
58.7mA
157.2mA
60.3mA
852mA
322mA
200mA
119mA
106mA
1782mA
456mA
FCM1608KF-1-GP
68.00217.161
68.00206.021
120ohm 100MHz
FCM1608CF-221T02-GP
68.00217.521
68.00084.A81
220ohm 100MHz
HCB1608K-181T20GP
68.00214.101
68.00206.041
180ohm 100MHz
83.00054.Z81
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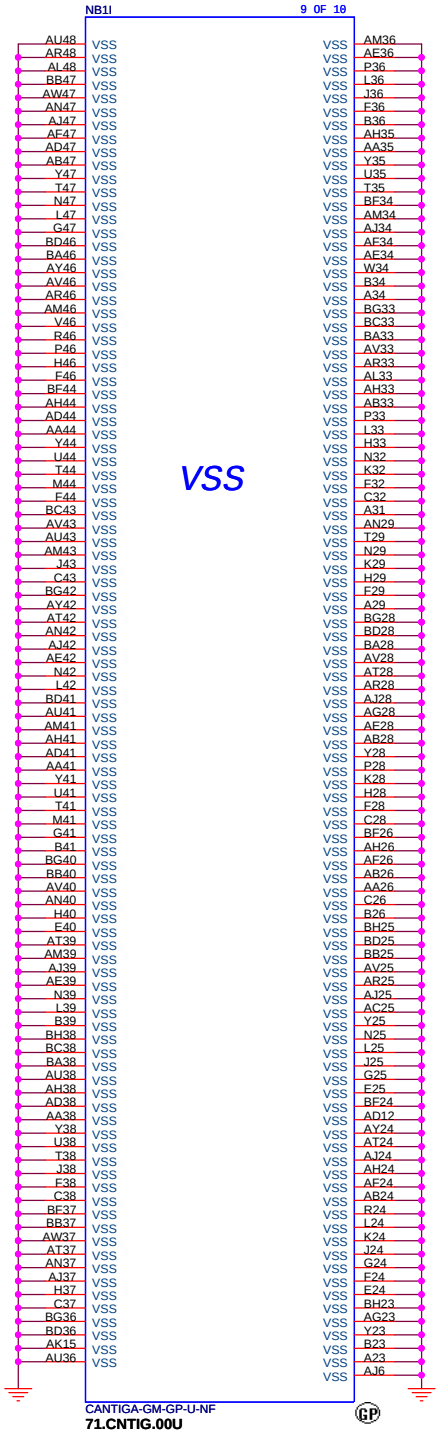
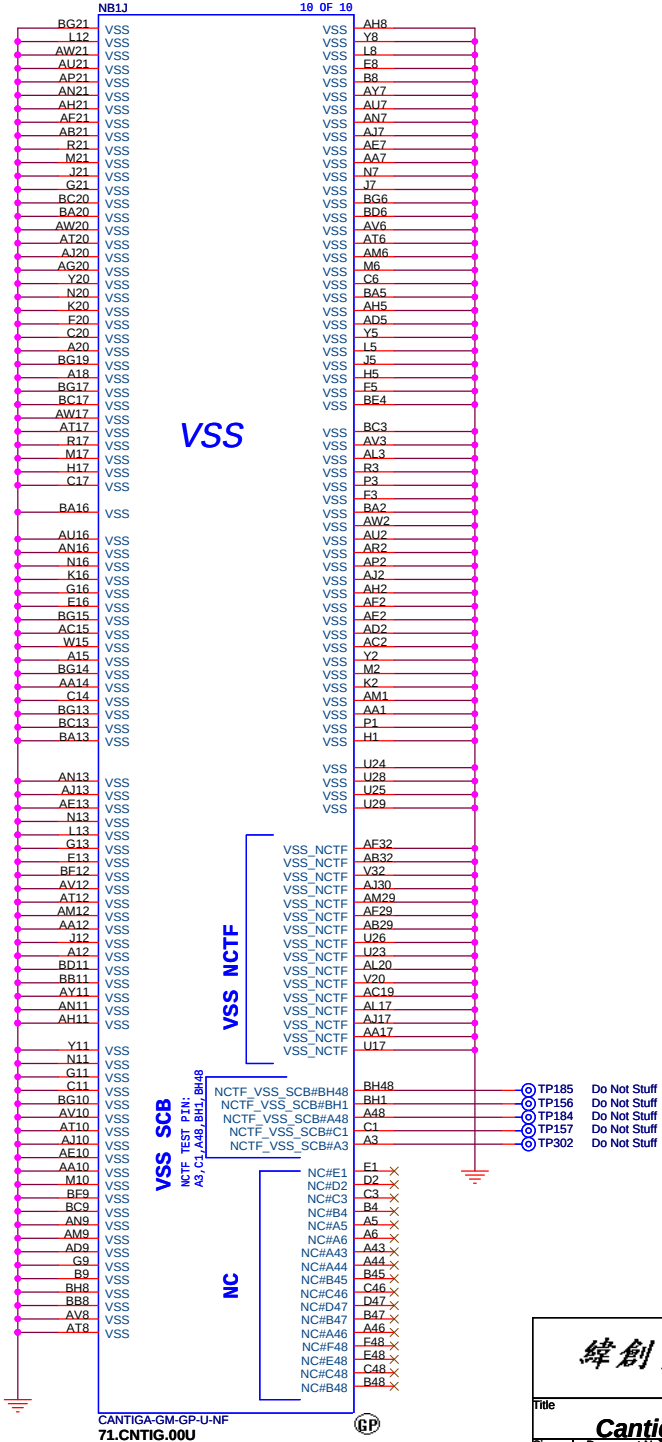
Cantiga (5 of 6)
Big Bear 2
Wednesday, October 22, 2008





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Title: Cantiga (6 of 6)

Size | Document Number: Big Bear 2 | Rev: -1

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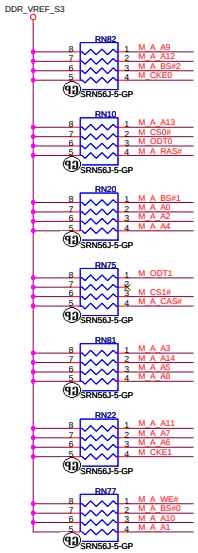
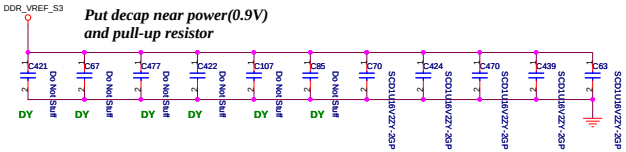
PARALLEL TERMINATION

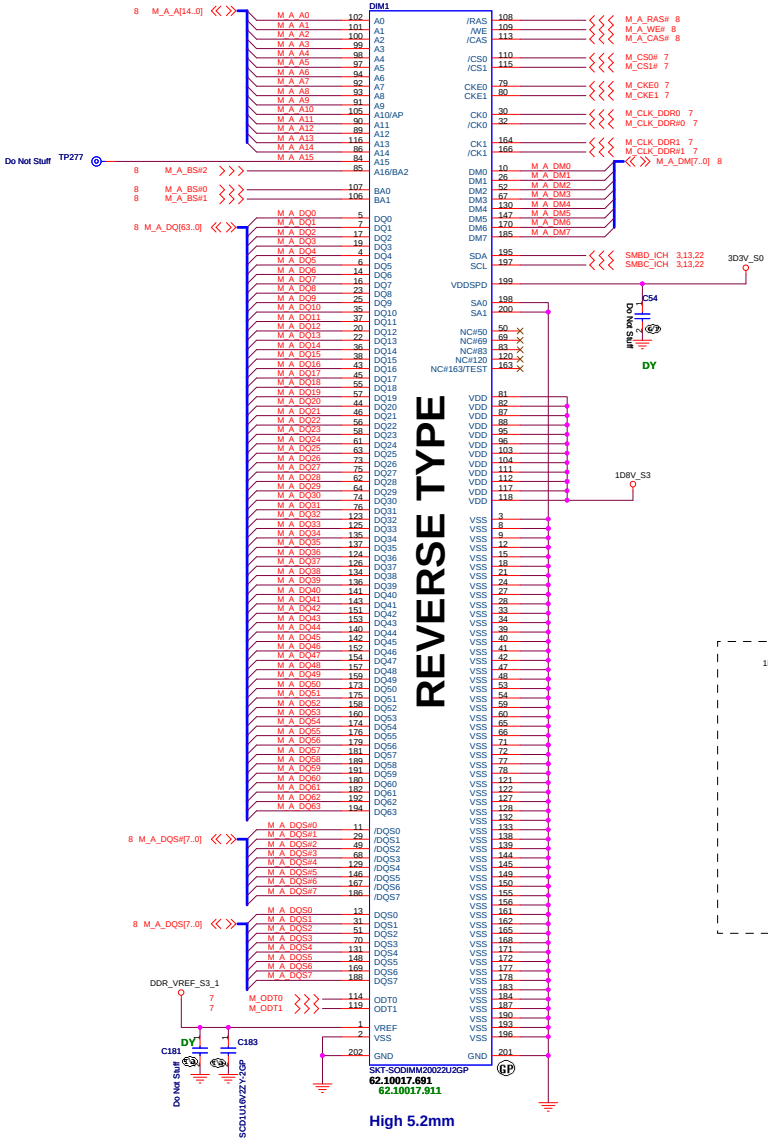
Put decap near power(0.9V) and pull-up resistor

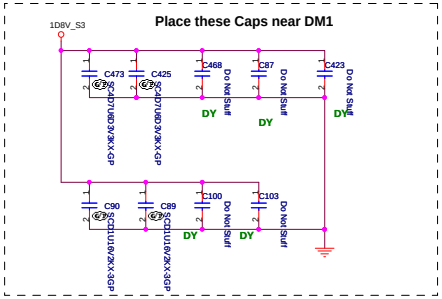


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor







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Title: DDR2 Socket 0 (DM1)			
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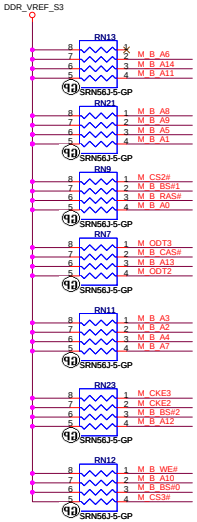
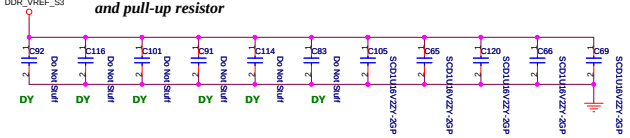
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

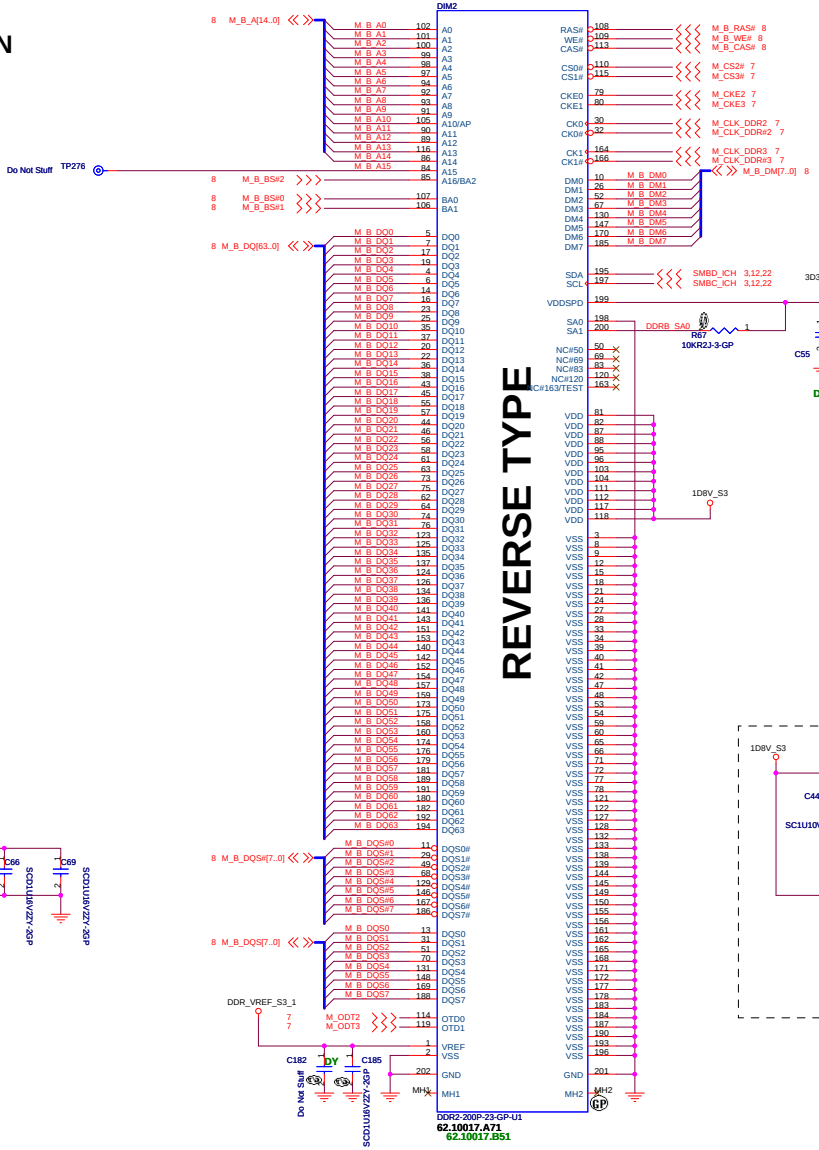


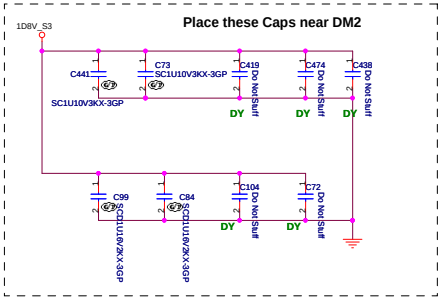
Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

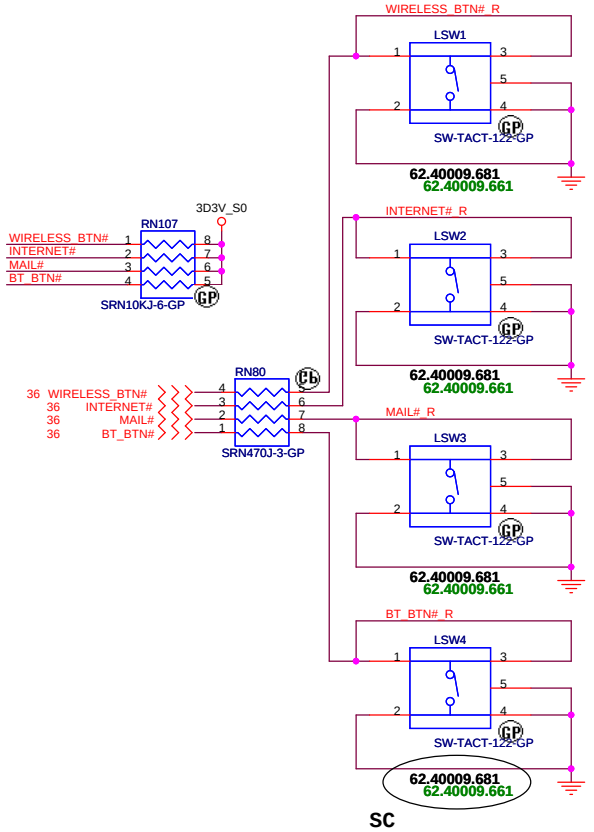


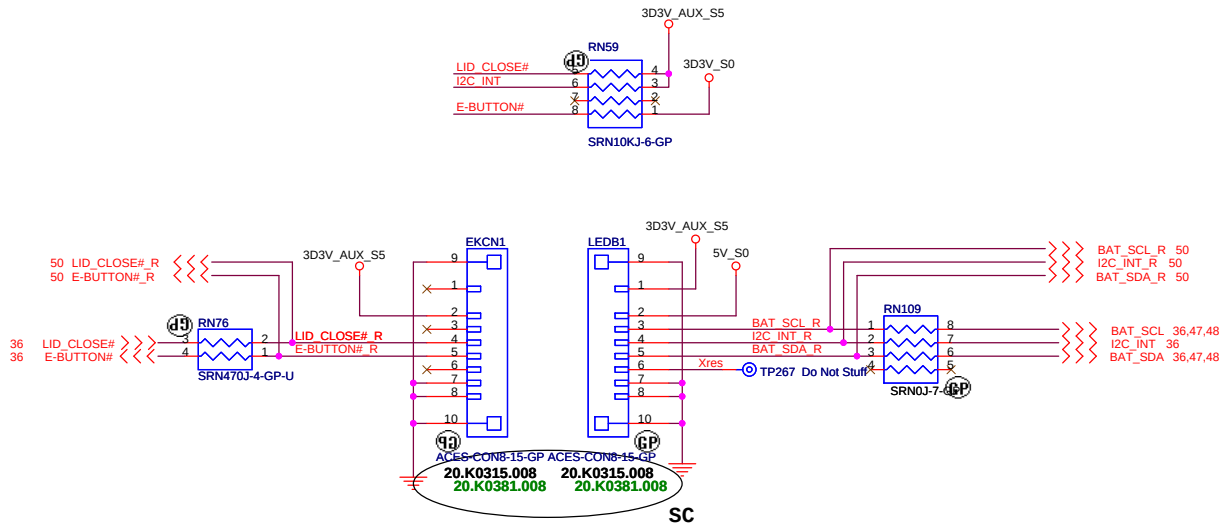
REVERSE TYPE





緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DDR2 Socket 1 (DM2)***	
Size	Document Number **Big Bear 2**	Rev -1
Date: Wednesday, October 22, 2008	Sheet 13 of 50	





UMA

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Taipei Hsien 221, Taiwan, R.O.C.

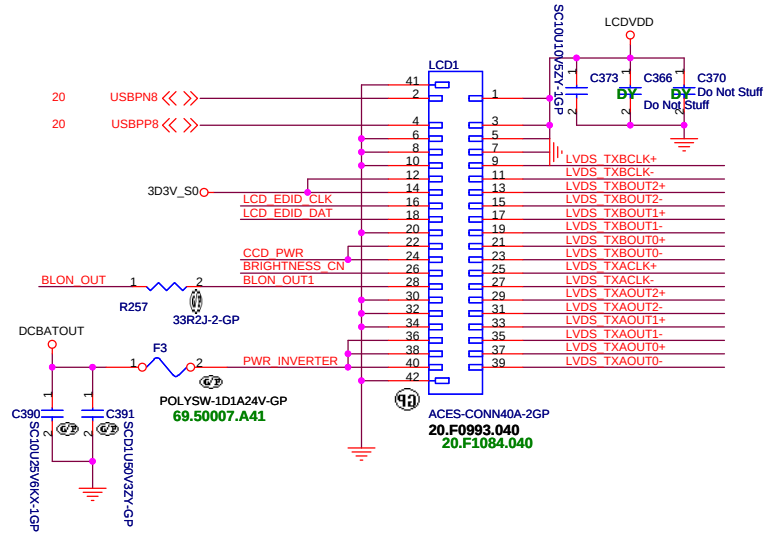
Title: ***LAUNCH***

Size | Document Number: **Big Bear 2** | Rev: -1

Date: Wednesday, October 22, 2008 | Sheet 14 of 50

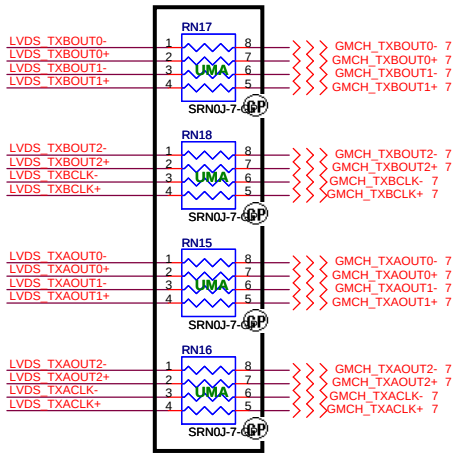
LCD/INVERTER/CCD CONN

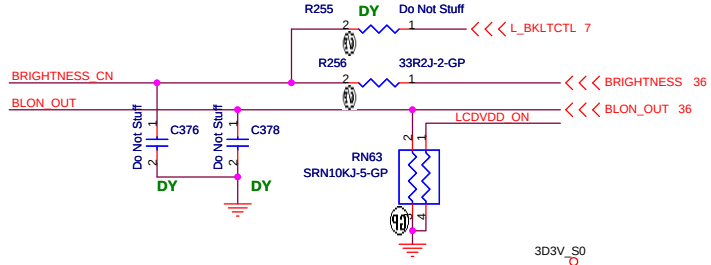
Place close to MXM slot for BB2

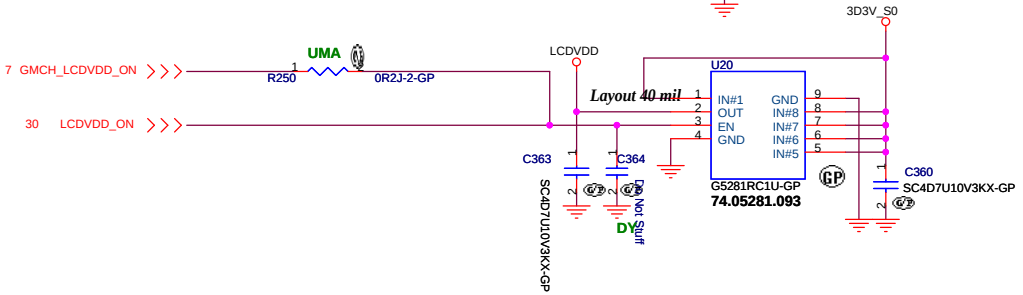


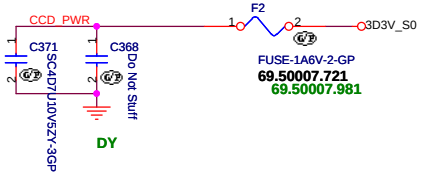
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

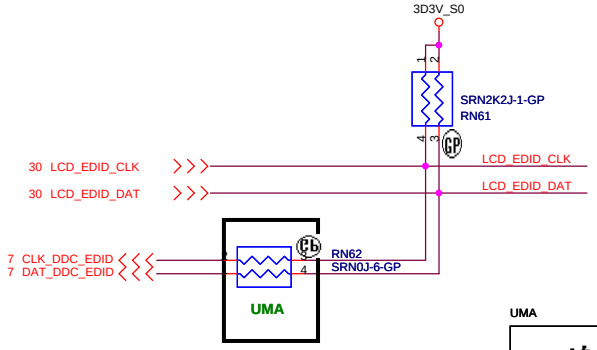
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND











Place close to MXM slot for BB2

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LCD CONN		
Size	Document Number	Rev
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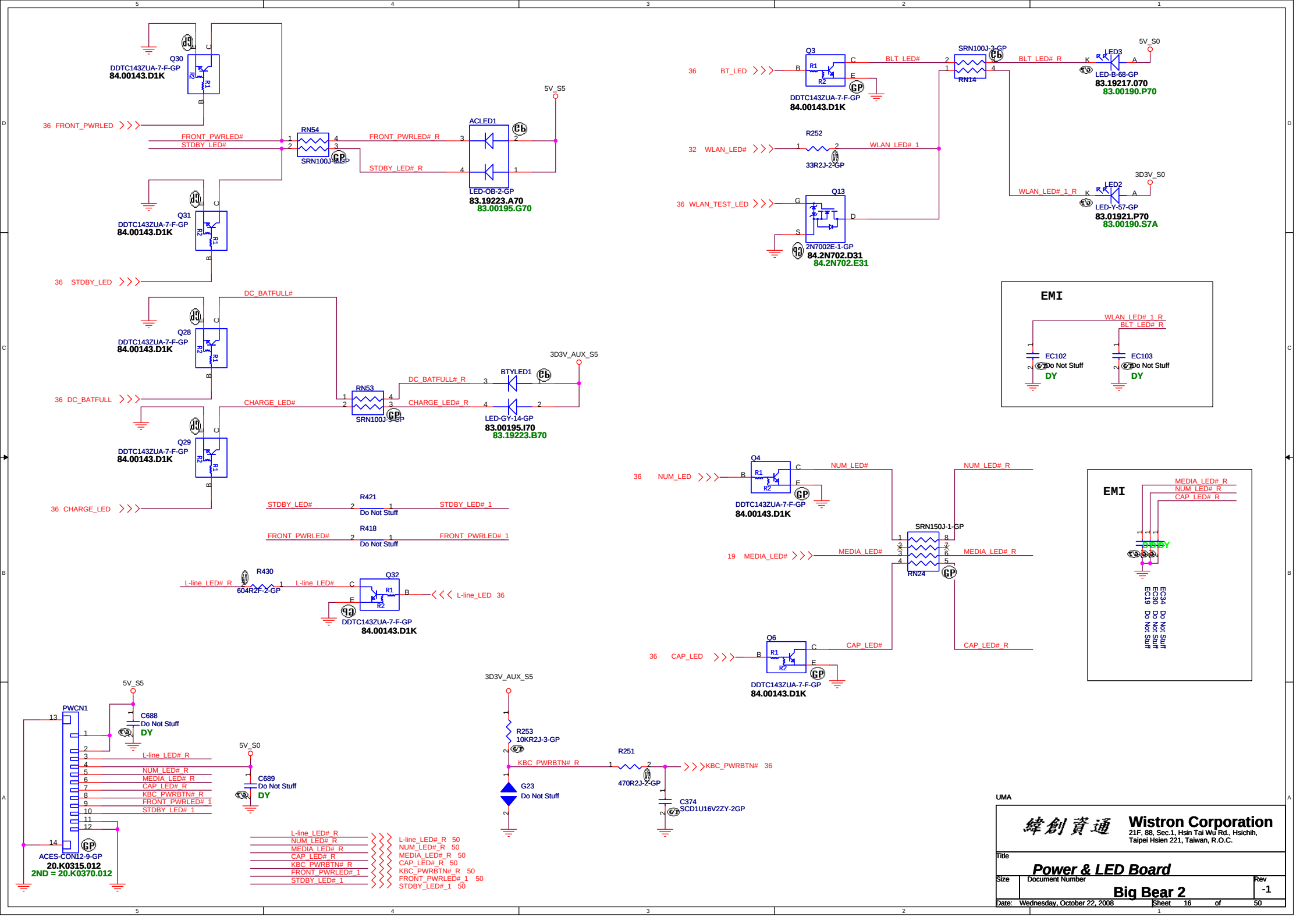
Q30
DDTC143ZUA-7-F-GP
84.00143.D1K
36 FRONT_PWRLED
FRONT_PWRLED#
STDBY_LED#
RN54
SRN100J-3-GP
FRONT_PWRLED#_R
STDBY_LED#_R
ACLED1
LED-OB-2-GP
83.19223.A70
83.00195.G70
5V_S5
Q31
DDTC143ZUA-7-F-GP
84.00143.D1K
36 STDBY_LED
Q3
36 BT_LED
DDTC143ZUA-7-F-GP
84.00143.D1K
BLT_LED#
SRN100J-3-GP
RN14
BLT_LED#_R
LED3
LED-B-68-GP
83.19217.070
83.00190.P70
5V_S0
R252
32 WLAN_LED#
33R2J-2-GP
WLAN_LED#_1
Q13
36 WLAN_TEST_LED
2N7002E-1-GP
84.2N702.D31
84.2N702.E31
WLAN_LED#_1_R
LED2
LED-Y-57-GP
83.01921.P70
83.00190.S7A
3D3V_S0
DC_BATFULL#
Q28
DDTC143ZUA-7-F-GP
84.00143.D1K
36 DC_BATFULL
CHARGE_LED#
RN53
SRN100J-3-GP
DC_BATFULL#_R
CHARGE_LED#_R
BTYLED1
LED-GY-14-GP
83.00195.I70
83.19223.B70
3D3V_AUX_S5
Q29
DDTC143ZUA-7-F-GP
84.00143.D1K
36 CHARGE_LED
EMI
WLAN_LED#_1_R
BLT_LED#_R
EC102
Do Not Stuff
DY
EC103
Do Not Stuff
DY
STDBY_LED#
R421
Do Not Stuff
STDBY_LED#_1
FRONT_PWRLED#
R418
Do Not Stuff
FRONT_PWRLED#_1
L-line_LED#_R
R430
604R2F-2-GP
L-line_LED#
Q32
DDTC143ZUA-7-F-GP
84.00143.D1K
L-line_LED 36
Q4
36 NUM_LED
DDTC143ZUA-7-F-GP
84.00143.D1K
NUM_LED#
NUM_LED#_R
SRN150J-1-GP
19 MEDIA_LED#
MEDIA_LED#
MEDIA_LED#_R
RN24
Q6
36 CAP_LED
DDTC143ZUA-7-F-GP
84.00143.D1K
CAP_LED#
CAP_LED#_R
EMI
MEDIA_LED#_R
NUM_LED#_R
CAP_LED#_R
EC34 Do Not Stuff
EC30 Do Not Stuff
EC19 Do Not Stuff
5V_S5
PWCN1
C688
Do Not Stuff
DY
L-line_LED#_R
NUM_LED#_R
MEDIA_LED#_R
CAP_LED#_R
KBC_PWRBTN#_R
FRONT_PWRLED#_1
STDBY_LED#_1
ACES-CON12-9-GP
20.K0315.012
2ND = 20.K0370.012
5V_S0
C689
Do Not Stuff
DY
3D3V_AUX_S5
R253
10KR2J-3-GP
KBC_PWRBTN#_R
G23
Do Not Stuff
R251
470R2J-2-GP
KBC_PWRBTN# 36
C374
SCD1U16V2ZY-2GP
L-line_LED#_R 50
NUM_LED#_R 50
MEDIA_LED#_R 50
CAP_LED#_R 50
KBC_PWRBTN#_R 50
FRONT_PWRLED#_1 50
STDBY_LED#_1 50
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power & LED Board
Size
Document Number
Big Bear 2
Rev
-1
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CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

CRT_R_SYS → L9 FCB1608CF-GP 68.00230.021 68.00119.081 → CRT_R
CRT_G_SYS → L8 FCB1608CF-GP 68.00230.021 68.00119.081 → CRT_G
CRT_B_SYS → L7 FCB1608CF-GP 68.00230.021 68.00119.081 → CRT_B

R267 150R2J-L1-GP-U
R269 150R2J-L1-GP-U
R272 150R2J-L1-GP-U

C404 Do Not Stuff DY
C398 Do Not Stuff DY
C396 Do Not Stuff DY
C401 SC15P50V2JN-2-GP
C397 SC6D8P50V2DN-GP
C395 SC6D8P50V2DN-GP

RN73
30 CRT_RED
30 CRT_GREEN
30 CRT_BLUE
CRT_R_SYS
CRT_G_SYS
CRT_B_SYS
Do Not Stuff
DIS

RN6
7 GMCH_BLUE
7 GMCH_GREEN
7 GMCH_RED
CRT_B_SYS
CRT_G_SYS
CRT_R_SYS
SRN0J-7-GP
UMA

5V_S0
D10 CRT_R DY Do Not Stuff 83.00099.K11
D8 CRT_G DY Do Not Stuff 83.00099.K11
D7 CRT_B DY Do Not Stuff 83.00099.K11

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT1
CRT_R
CRT_G
CRT_B
DAT_DDC1_5
CRT_HSYNC1
CRT_VSYNC1
CLK_DDC1_5
VIDEO-15-42-GP-U
20.20378.015
20.20775.015

5V_CRT_S0
C27 SCD01U16V2KX-3GP
C393 SC100P50V2JN-3GP
C26 SC18P50V2JN-1-GP
C25 SC18P50V2JN-1-GP
C394 SC100P50V2JN-3GP

R265 36 CRT_DEC# 470R2J-2-GP
CRT_IN#_R
C392 Do Not Stuff DY
D5 5V_S0 Do Not Stuff 83.00099.K11

6 1 7 2 8 3 9 4 10 5

Hsync & Vsync level shift

5V_S0
C50 SCD1U16V2KX-3GP
CRT_HSYNC → U6A TSAHCT125PW-GP 73.74125.L13 73.74125.L12 → CRT_HSYNC2
R57 Do Not Stuff
CRT_HSYNC2 → CRT_HSYNC1

5V_S0
CRT_VSYNC → U6B TSAHCT125PW-GP 73.74125.L13 73.74125.L12 → CRT_VSYNC2
R56 Do Not Stuff
CRT_VSYNC2 → CRT_VSYNC1

For UMA CRT

7 GMCH_HSYNC
7 GMCH_VSYNC
RN72 SRN0J-6-GP UMA
CRT_HSYNC
CRT_VSYNC

For DIS CRT

30 CRT_HSYNC
30 CRT_VSYNC
CRT_HSYNC
CRT_VSYNC

5V_S0 → U6C TSAHCT125PW-GP 73.74125.L13 73.74125.L12
5V_S0 → U6D TSAHCT125PW-GP 73.74125.L13 73.74125.L12

DDC_CLK & DATA level shift

3D3V_S0
5V_CRT_S0
5V_S0
D6 CH551H-30PT-GP 83.R5003.H8H
F1 FUSE-1DTA6V-4GP-U 69.50007.691 69.50007.771
5V_CRT_DDC
RN70 SRN2K2J-1-GP
RN69 SRN2KJ-2-GP
Q15 2N7002EDW-GP 84.DMN66.03F
CRT_IN#_R
DAT_DDC1_5
CLK_DDC1_5

7 GMCH_DDCDATA
7 GMCH_DDCCLK
RN1 SRN0J-6-GP UMA
30 CRT_DDCDATA
30 CRT_DDCCLK

UMA

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Title: CRT Connector
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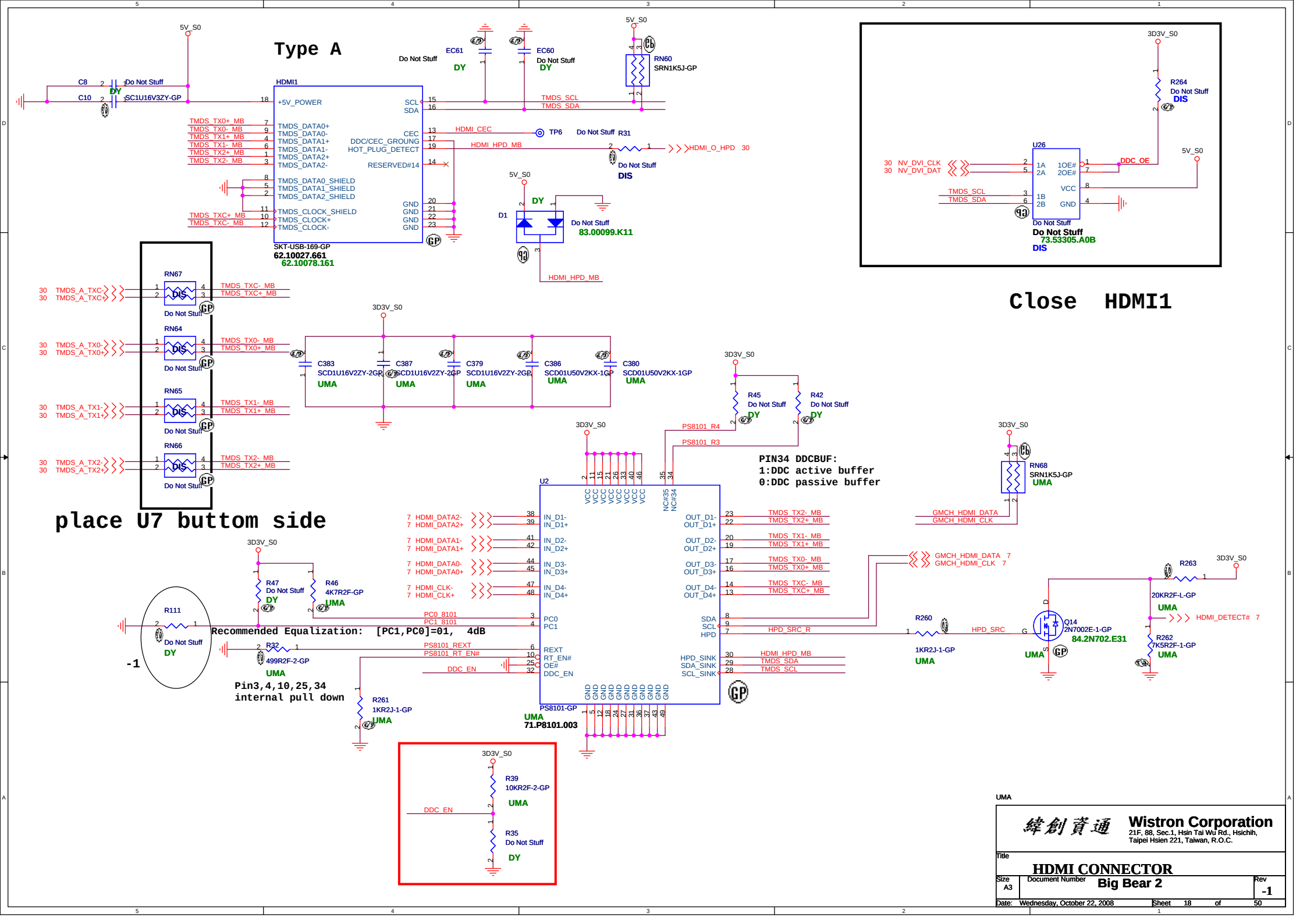
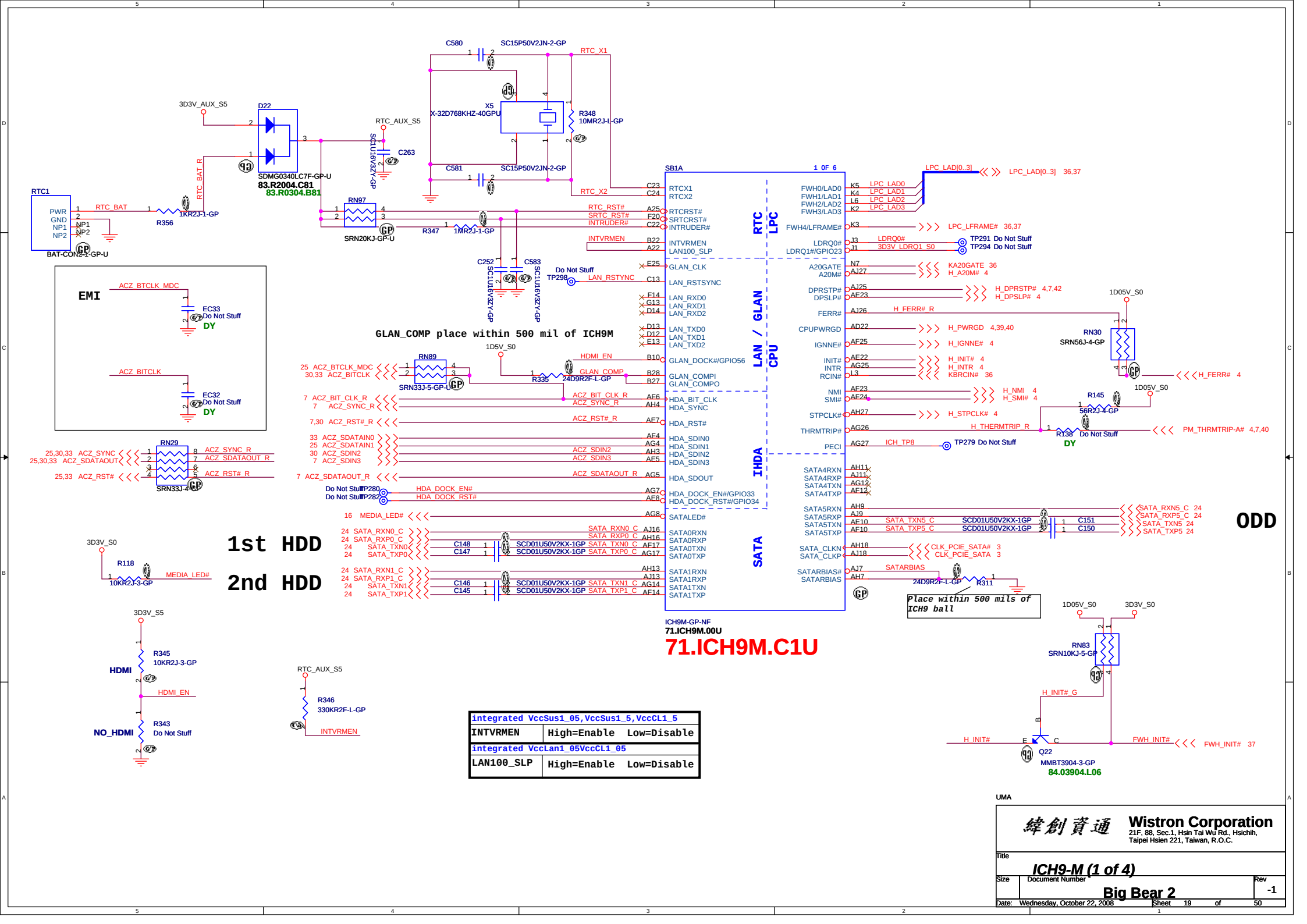

Type A
HDMI1
SKT-USB-169-GP
62.10027.661
62.10078.161
Close HDMI1
place U7 buttom side
PIN34 DDCBUF:
1:DDC active buffer
0:DDC passive buffer
Recommended Equalization: [PC1,PC0]=01, 4dB
Pin3,4,10,25,34
internal pull down
U2
PS8101-GP
UMA
71.P8101.003
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
HDMI CONNECTOR
Big Bear 2
Rev
-1
Wednesday, October 22, 2008


C580 SC15P50V2JN-2-GP
RTC_X1
X5
X-32D768KHZ-40GPU
R348 10MR2J-L-GP
C581 SC15P50V2JN-2-GP
RTC_X2
3D3V_AUX_S5
D22
SDMG0340LC7F-GP-U
83.R2004.C81
83.R0304.B81
RTC_AUX_S5
C263
SC1U16V3ZY-GP
RTC_BAT_R
RTC1
BAT-CON2-1-GP-U
RTC_BAT
R356 1KR2J-1-GP
RN97
SRN20KJ-GP-U
R347 1MR2J-1-GP
RTC_RST#
SRTC_RST#
INTRUDER#
INTVRMEN
C252 SC1U16V2ZY-GP
C583 SC1U16V2ZY-GP
Do Not Stuff
TP298
LAN_RSTSYNC
SB1A
1 OF 6
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
LPC_LAD[0..3]
LPC_LFRAME#
TP291 Do Not Stuff
TP294 Do Not Stuff
KA20GATE
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
KBRCIN#
H_NMI
H_SMI#
H_STPCLK#
H_THERMTRIP_R
ICH_TP8
TP279 Do Not Stuff
RN30 SRN56J-4-GP
R145 56R2J-4-GP
R138 Do Not Stuff
DY
PM_THRMTRIP-A#
SATA_TXN5_C
SATA_TXP5_C
SCD01U50V2KX-1GP
C151
C150
SATA_RXN5_C
SATA_RXP5_C
SATA_TXN5
SATA_TXP5
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATARBIAS
24D9R2F-L-GP
R311
Place within 500 mils of ICH9 ball
ICH9M-GP-NF
71.ICH9M.00U
71.ICH9M.C1U
GLAN_COMP place within 500 mil of ICH9M
HDMI_EN
GLAN_COMP
R335 24D9R2F-L-GP
RN89 SRN33J-5-GP-U
ACZ_BIT_CLK_R
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDATAOUT_R
HDA_DOCK_EN#
HDA_DOCK_RST#
MEDIA_LED#
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0
SATA_TXP0
SATA_RXN1_C
SATA_RXP1_C
SATA_TXN1
SATA_TXP1
C148
C147
C146
C145
SCD01U50V2KX-1GP
SATA_TXN0_C
SATA_TXP0_C
SATA_TXN1_C
SATA_TXP1_C
EMI
EC33 Do Not Stuff
EC32 Do Not Stuff
DY
ACZ_BTCLK_MDC
ACZ_BITCLK
RN29 SRN33J-4-GP
ACZ_SDATAIN0
ACZ_SDATAIN1
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDATAOUT
1st HDD
2nd HDD
3D3V_S0
R118 10KR2J-3-GP
3D3V_S5
R345 10KR2J-3-GP
HDMI
NO_HDMI
R343 Do Not Stuff
R346 330KR2F-L-GP
INTVRMEN
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
1D05V_S0
3D3V_S0
RN83 SRN10KJ-5-GP
H_INIT# G
H_INIT#
FWH_INIT#
Q22
MMBT3904-3-GP
84.03904.L06
ODD
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
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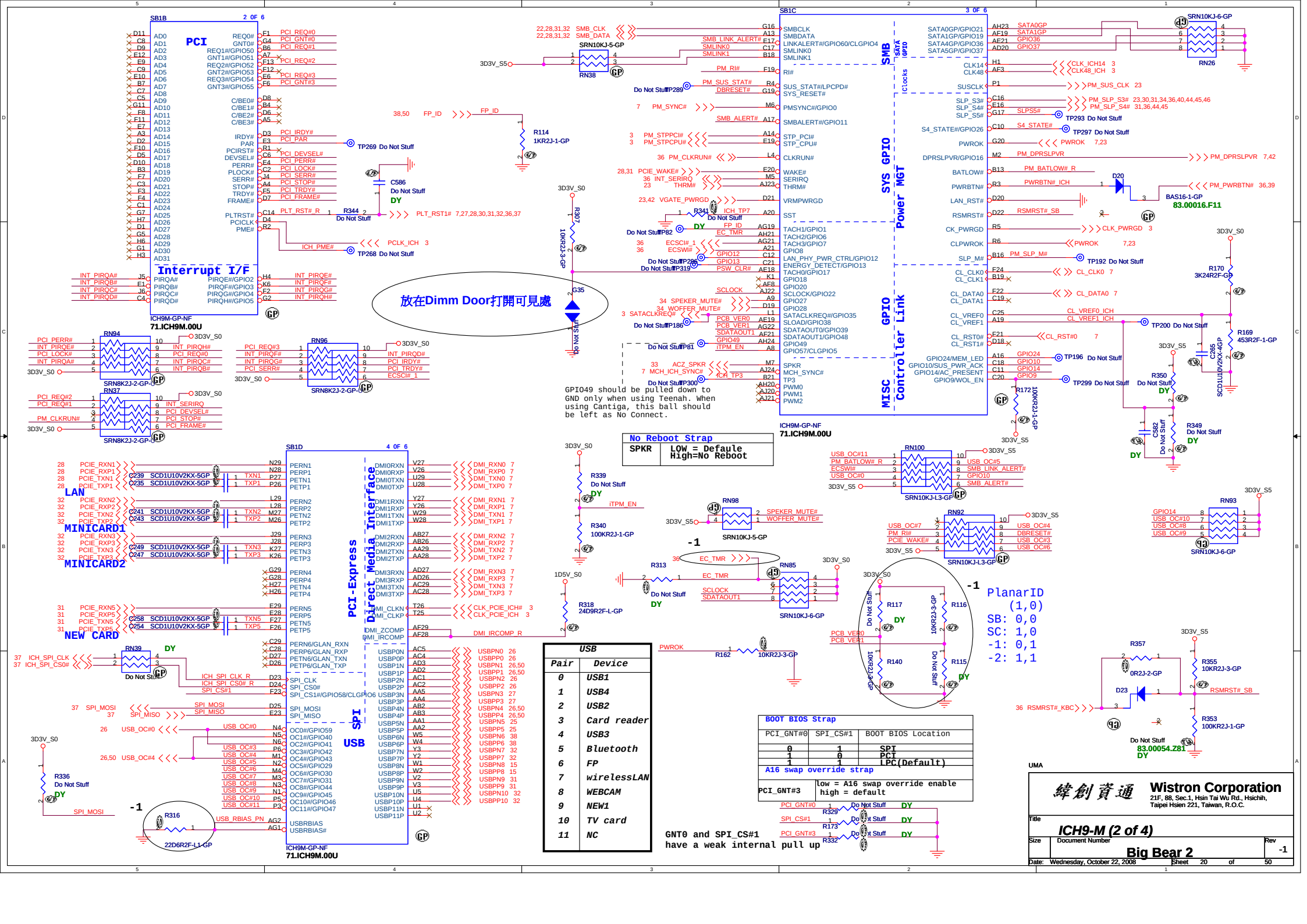
SB1B 2 OF 6
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SB1C 3 OF 6
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.00U
SB1D 4 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.00U
放在Dimm Door打開可見處
GPIO049 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
No Reboot Strap
SPKR | LOW = Defaule High=No Reboot
USB
Pair | Device
0 USB1
1 USB4
2 USB2
3 Card reader
4 USB3
5 Bluetooth
6 FP
7 wirelessLAN
8 WEBCAM
9 NEW1
10 TV card
11 NC
BOOT BIOS Strap
PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location
0 | 1 | SPI
1 | 0 | PCI
1 | 1 | LPC(Default)
A16 swap override strap
PCI_GNT#3 | low = A16 swap override enable high = default
GNT0 and SPI_CS#1 have a weak internal pull up
PlanarID (1,0)
SB: 0,0
SC: 1,0
-1: 0,1
-2: 1,1
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
Document Number
Big Bear 2
Rev
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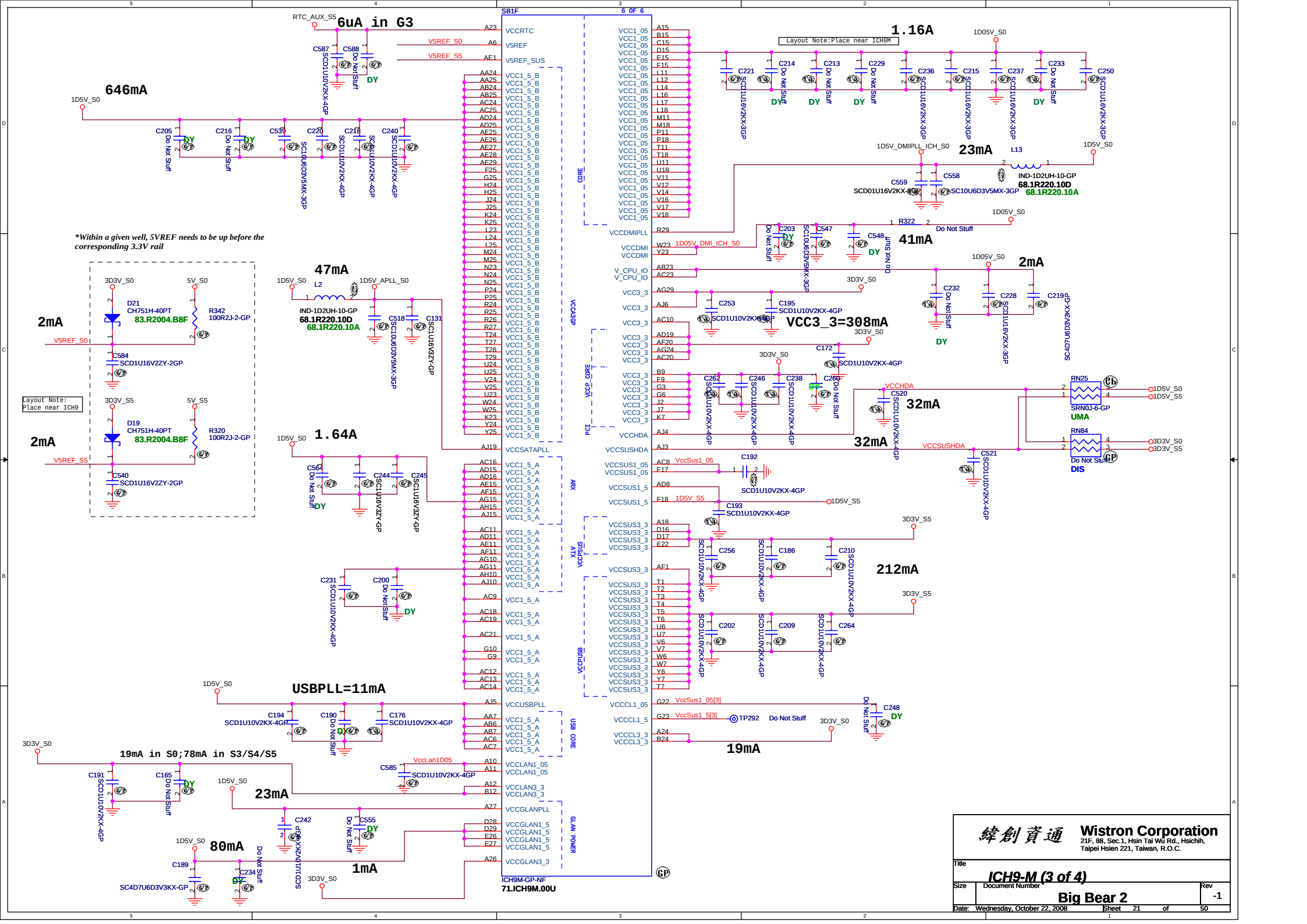
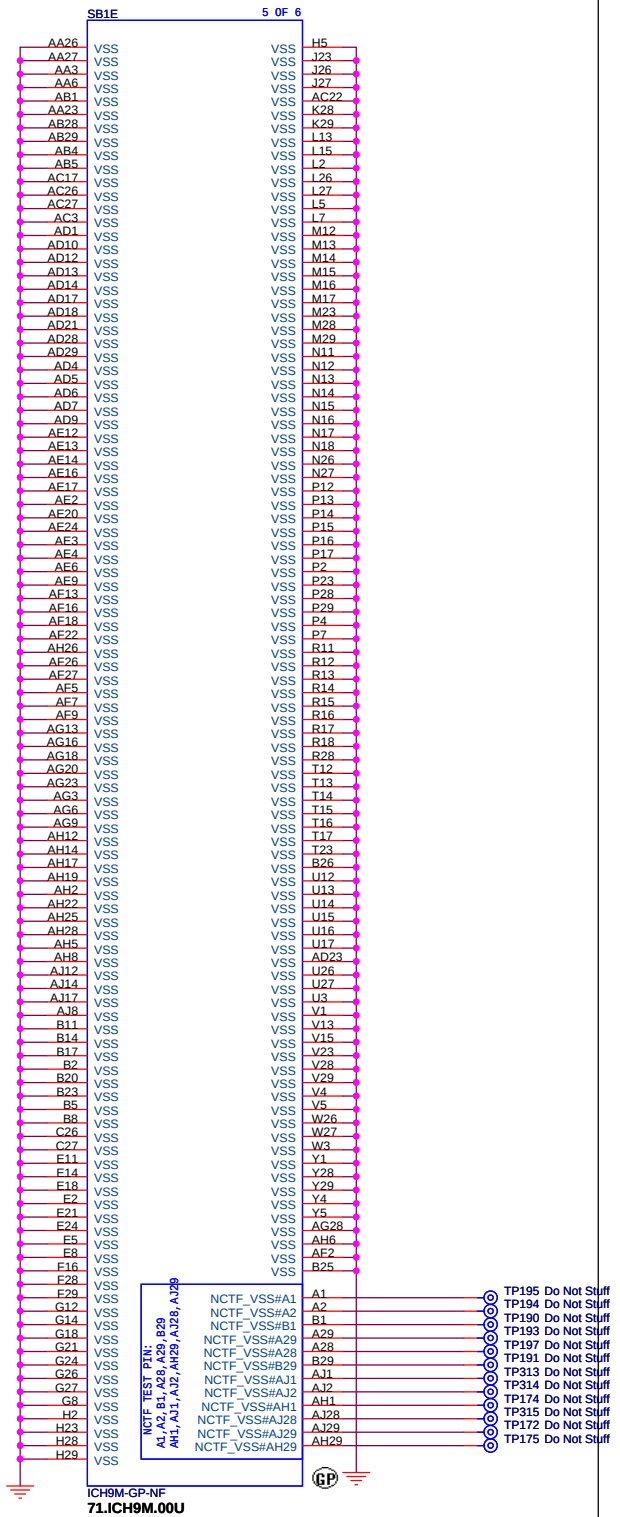
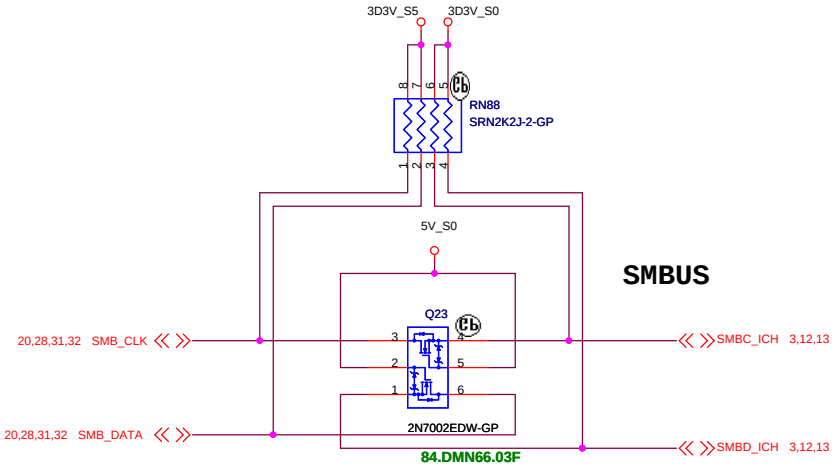

6uA in G3
646mA
1.16A
23mA
41mA
2mA
47mA
1.64A
VCC3_3=308mA
32mA
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
80mA
1mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
Do Not Stuff
UMA
DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
Big Bear 2
Wednesday, October 22, 2008





緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ICH9-M (4 of 4)***

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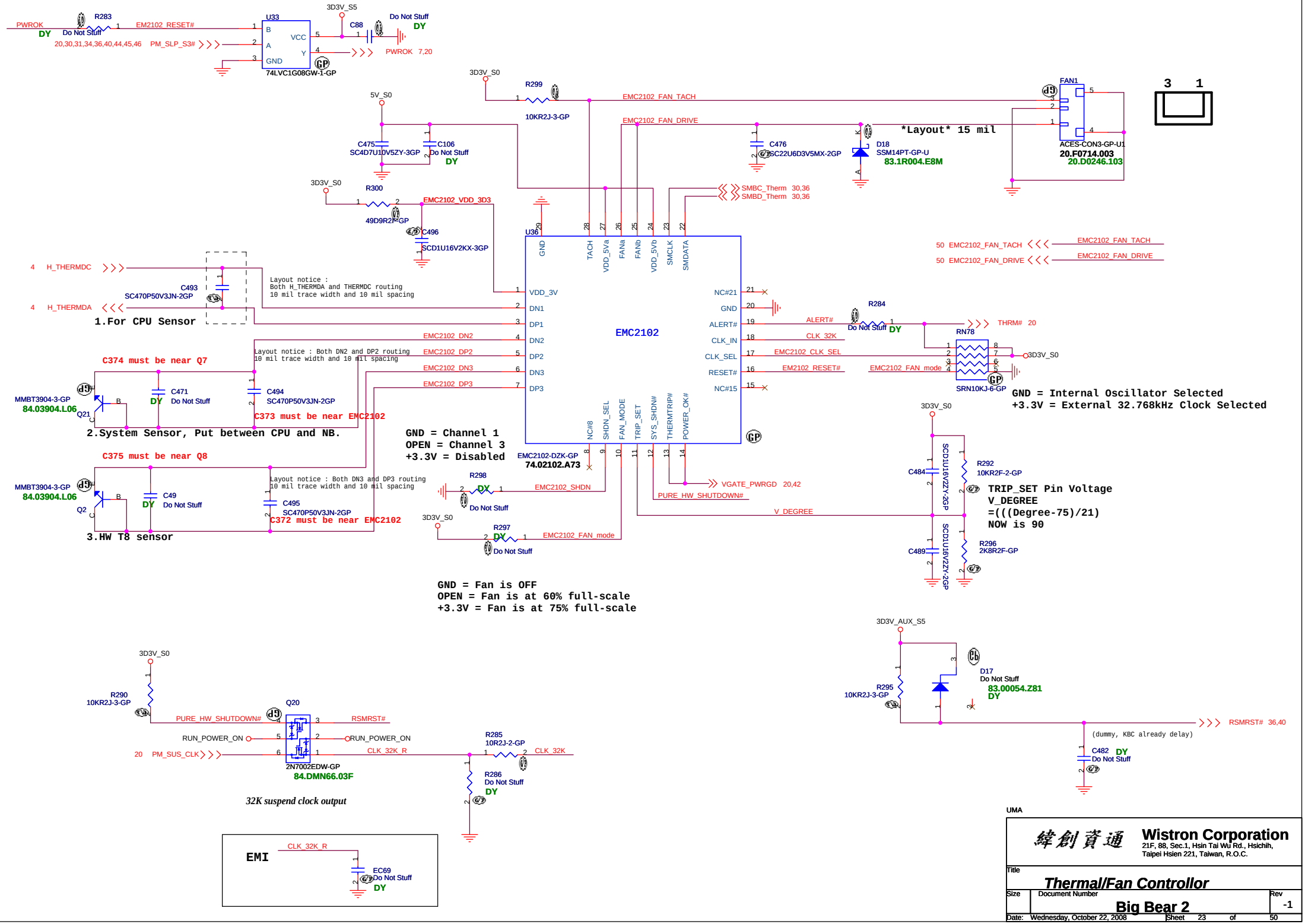
Date: Wednesday, October 22, 2008 | Sheet 22 of 50


PWROK
DY
R283
Do Not Stuff
EM2102_RESET#
20,30,31,34,36,40,44,45,46
PM_SLP_S3#
U33
B
A
GND
VCC
Y
74LVC1G08GW-1-GP
3D3V_S5
C88
Do Not Stuff
DY
PWROK 7,20
3D3V_S0
R299
10KR2J-3-GP
EMC2102_FAN_TACH
EMC2102_FAN_DRIVE
5V_S0
C475
SC4D7U10V5ZY-3GP
C106
Do Not Stuff
DY
C476
SC22U6D3V5MX-2GP
D18
SSM14PT-GP-U
83.1R004.E8M
Layout 15 mil
FAN1
ACES-CON3-GP-U1
20.F0714.003
20.D0246.103
3 1
SMBC_Therm 30,36
SMBD_Therm 30,36
3D3V_S0
R300
49D9R2F-GP
EMC2102_VDD_3D3
C496
SCD1U16V2KX-3GP
U36
GND
TACH
VDD_5Va
FANa
FANb
VDD_5Vb
SMCLK
SMDATA
50 EMC2102_FAN_TACH
50 EMC2102_FAN_DRIVE
4 H_THERMDC
4 H_THERMDA
C493
SC470P50V3JN-2GP
Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing
1.For CPU Sensor
VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3
EMC2102
NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15
R284
Do Not Stuff
DY
THRM# 20
RN78
SRN10KJ-6-GP
CLK_32K
EMC2102_CLK_SEL
EM2102_RESET#
EMC2102_FAN_mode
3D3V_S0
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
EMC2102_DN2
EMC2102_DP2
EMC2102_DN3
EMC2102_DP3
Layout notice : Both DN2 and DP2 routing
10 mil trace width and 10 mil spacing
C374 must be near Q7
MMBT3904-3-GP
84.03904.L06
Q21
C471
DY
Do Not Stuff
C494
SC470P50V3JN-2GP
C373 must be near EMC2102
2.System Sensor, Put between CPU and NB.
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
NC#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#
EMC2102-DZK-GP
74.02102.A73
C375 must be near Q8
MMBT3904-3-GP
84.03904.L06
Q2
C49
DY
Do Not Stuff
C495
SC470P50V3JN-2GP
C372 must be near EMC2102
Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing
3.HW T8 sensor
R298
DY
Do Not Stuff
EMC2102_SHDN
VGATE_PWRGD 20,42
PURE_HW_SHUTDOWN#
V_DEGREE
3D3V_S0
R297
DY
Do Not Stuff
EMC2102_FAN_mode
3D3V_S0
C484
SCD1U16V2ZY-2GP
R292
10KR2F-2-GP
TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)
NOW is 90
C489
SCD1U16V2ZY-2GP
R296
2K8R2F-GP
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
3D3V_AUX_S5
R295
10KR2J-3-GP
D17
Do Not Stuff
83.00054.Z81
DY
RSMRST# 36,40
(dummy, KBC already delay)
C482
DY
Do Not Stuff
3D3V_S0
R290
10KR2J-3-GP
PURE_HW_SHUTDOWN#
Q20
RSMRST#
RUN_POWER_ON
RUN_POWER_ON
20
PM_SUS_CLK
CLK_32K_R
2N7002EDW-GP
84.DMN66.03F
R285
10R2J-2-GP
CLK_32K
R286
Do Not Stuff
DY
32K suspend clock output
EMI
CLK_32K_R
EC69
Do Not Stuff
DY
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Document Number
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-1
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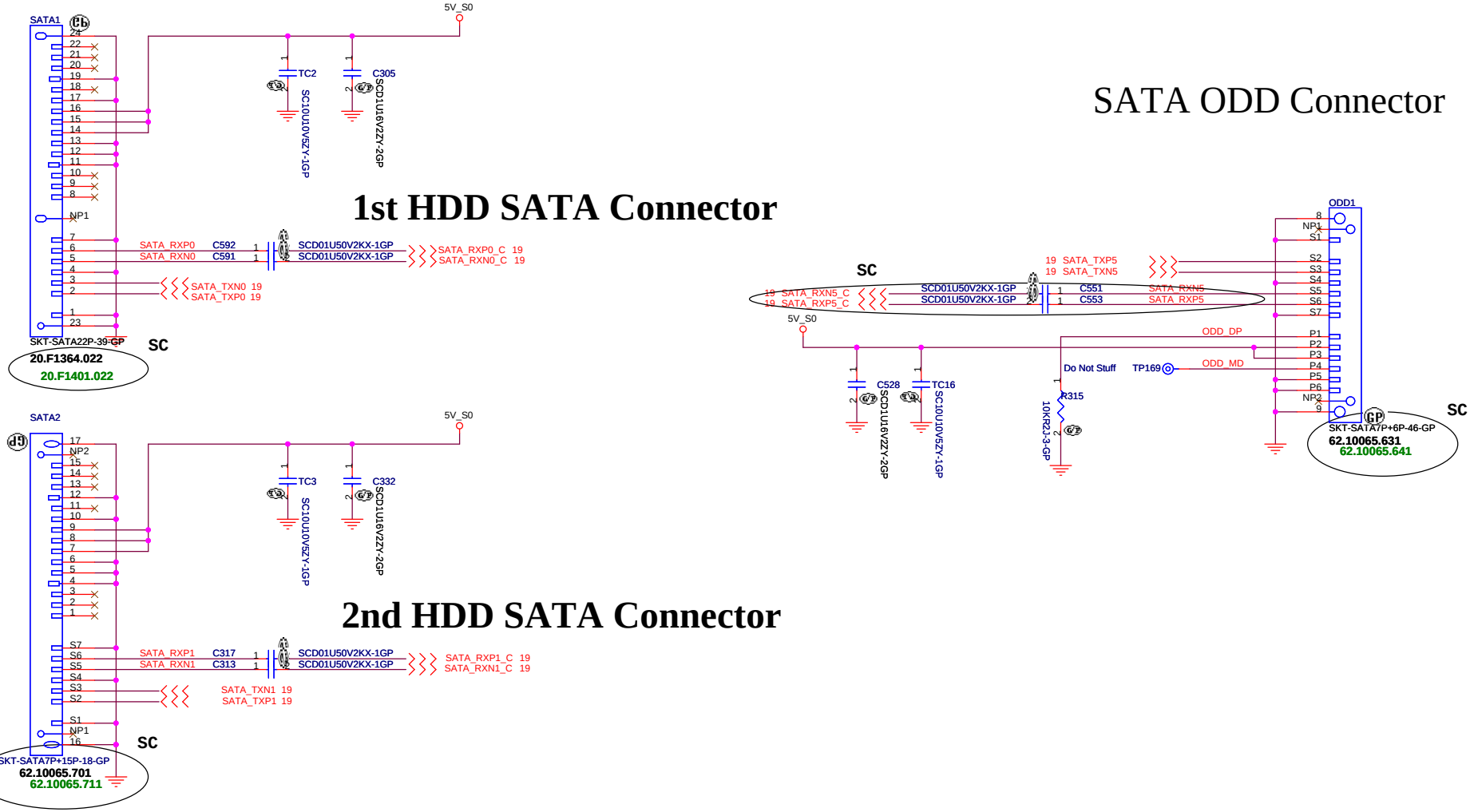
SATA ODD Connector



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***HDD & ODD***		
Size	Document Number: **Big Bear 2**	Rev: -1
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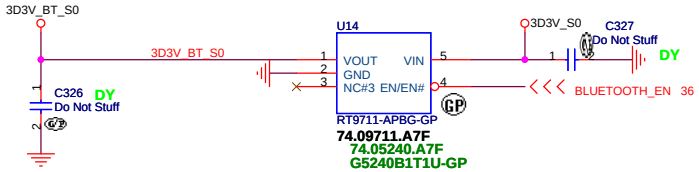
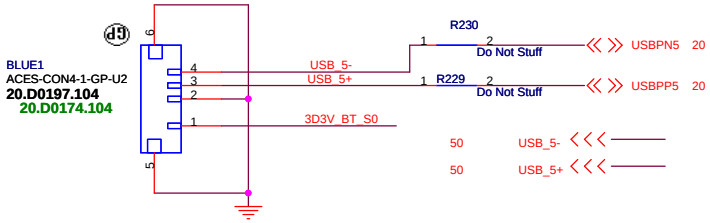
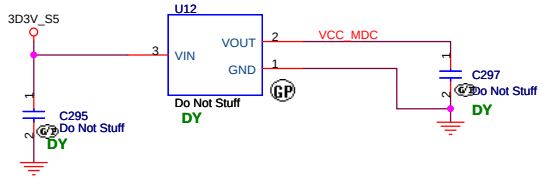
BLUETOOTH MODULE

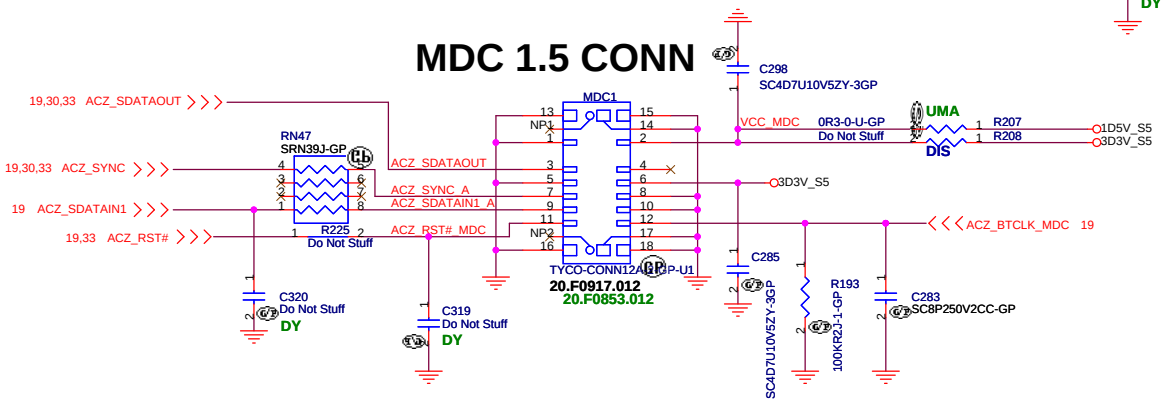
1.5A / High Active Voltage 2V

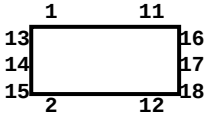






MDC 1.5 CONN





UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **BLUETOOTH & MDC**		
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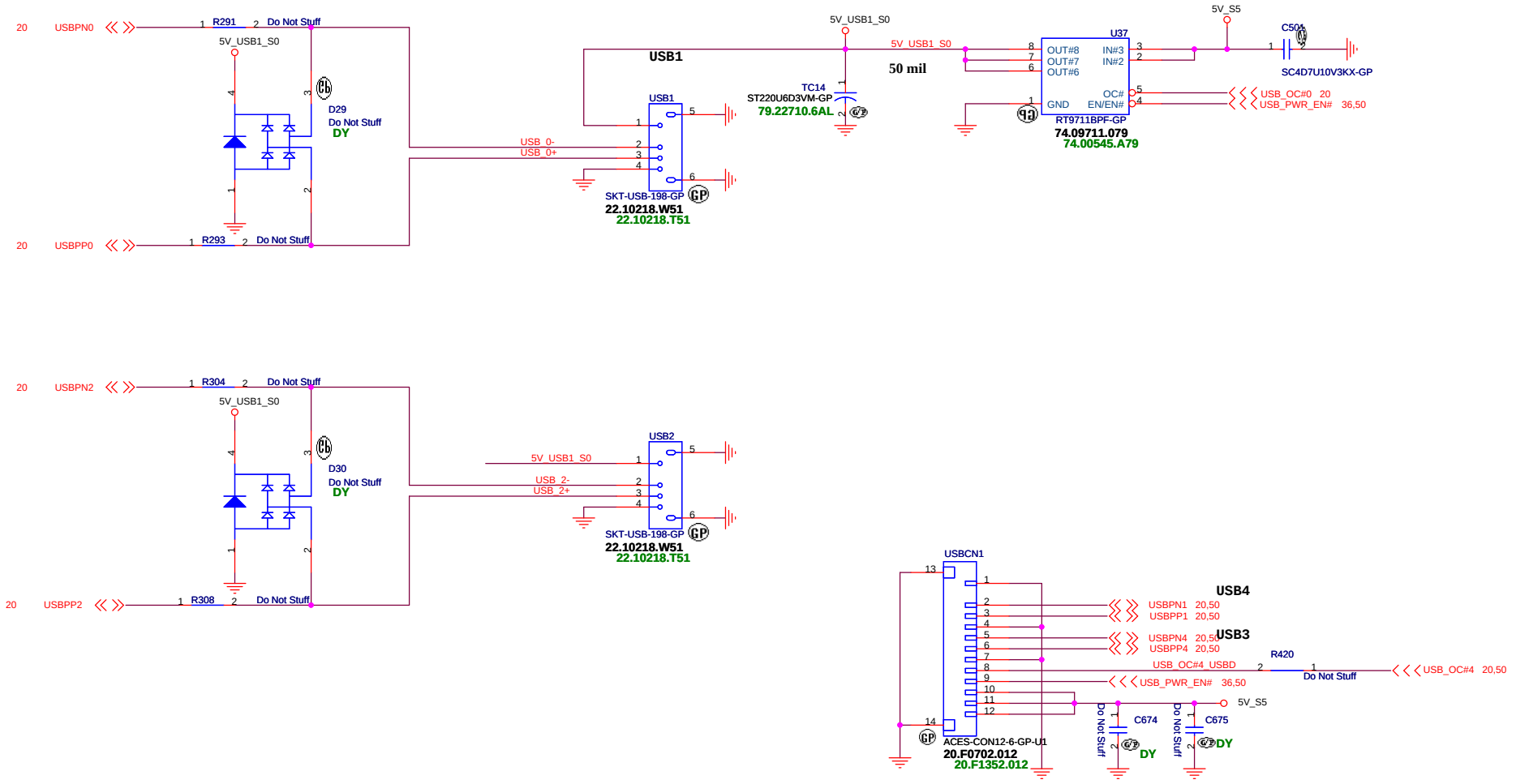

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB connector**

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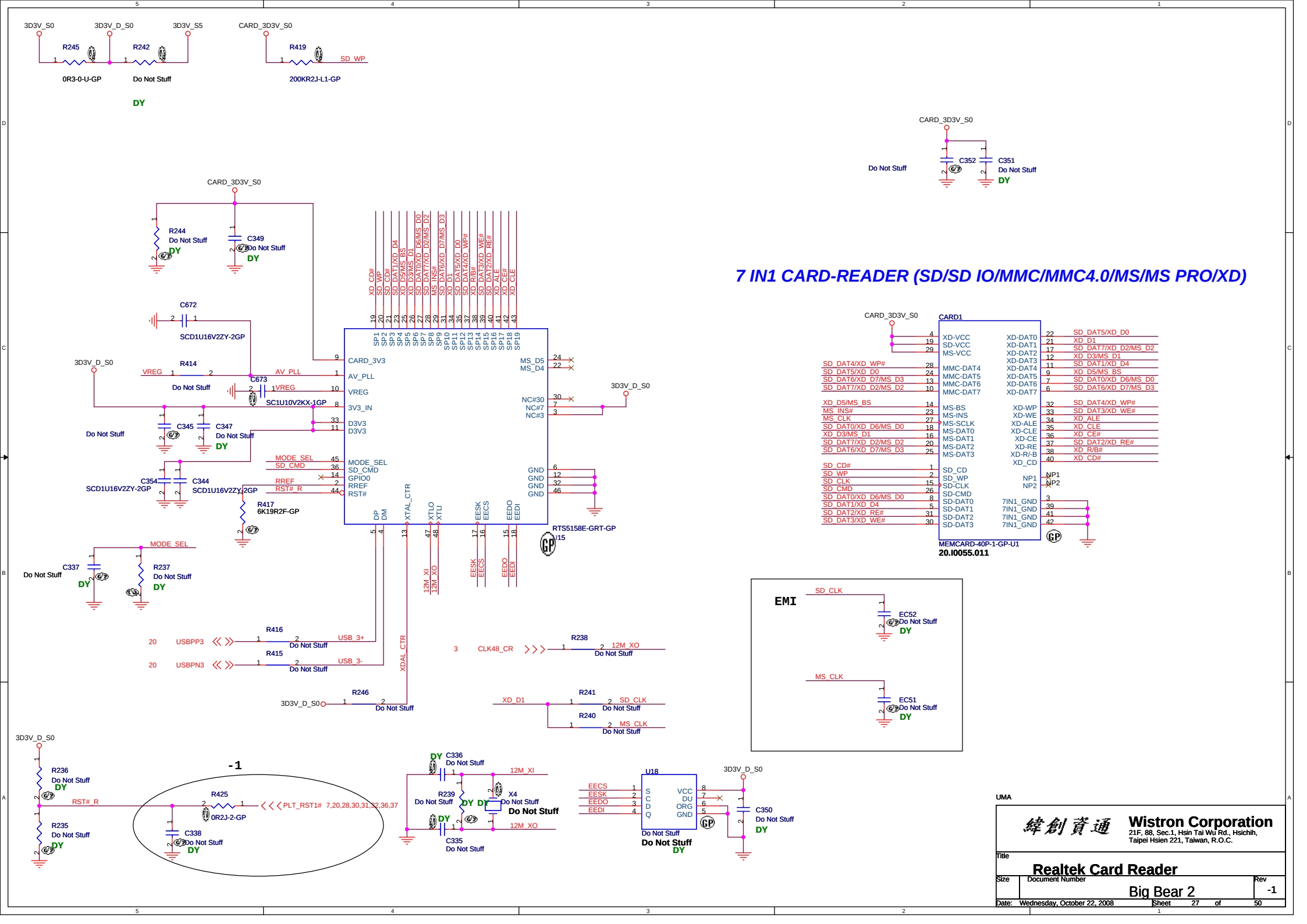
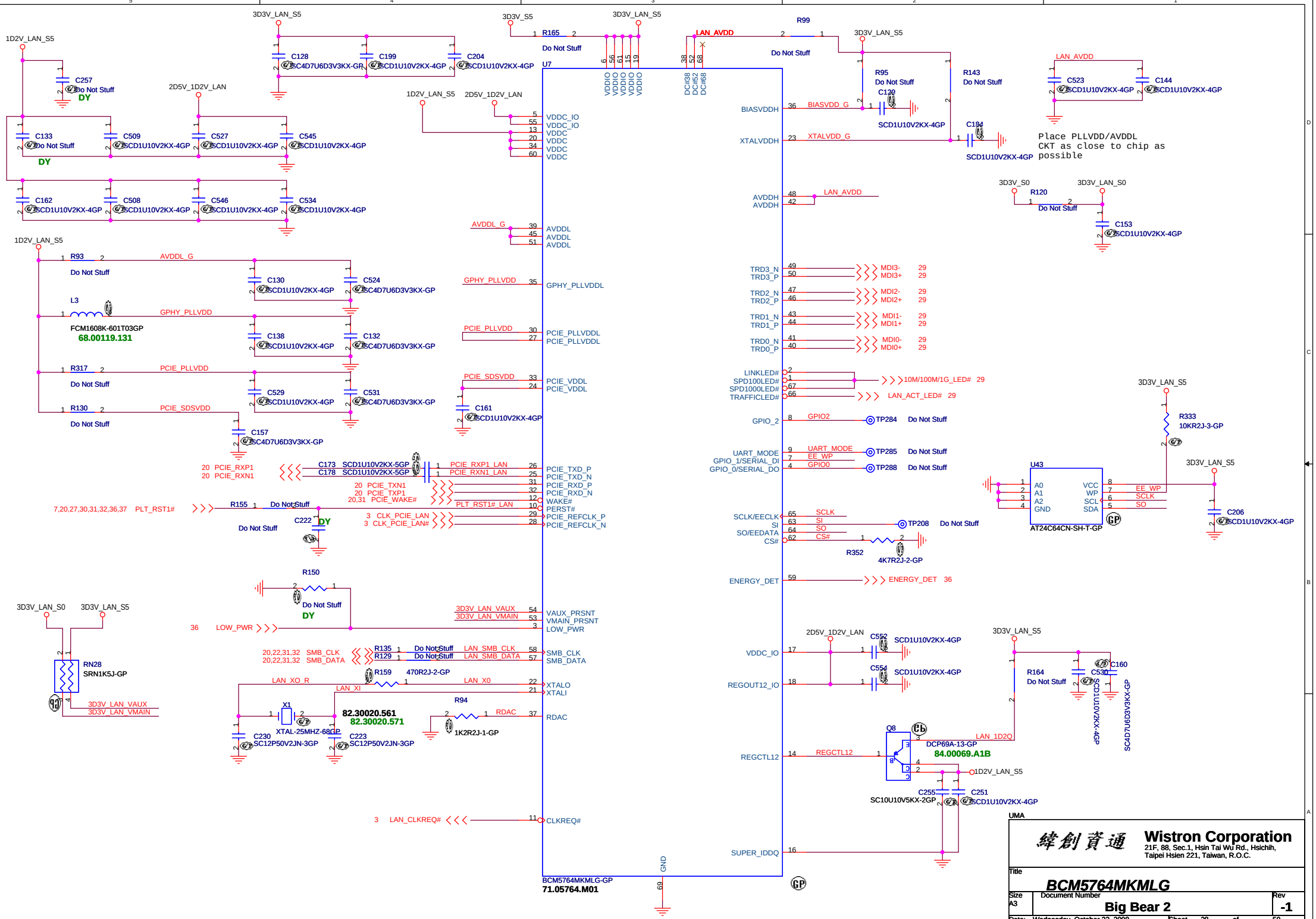

7 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)
RTS5158E-GRT-GP
U15
MEMCARD-40P-1-GP-U1
20.I0055.011
EMI
-1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Realtek Card Reader
Big Bear 2
Wednesday, October 22, 2008


U7
BCM5764MKMLG-GP
71.05764.M01
Place PLLVDD/AVDDL CKT as close to chip as possible
AT24C64CN-SH-T-GP
DCP69A-13-GP
84.00069.A1B
82.30020.561
82.30020.571
XTAL-25MHZ-68GP
FCM1608K-601T03GP
68.00119.131
SRN1K5J-GP
Do Not Stuff
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5764MKMLG
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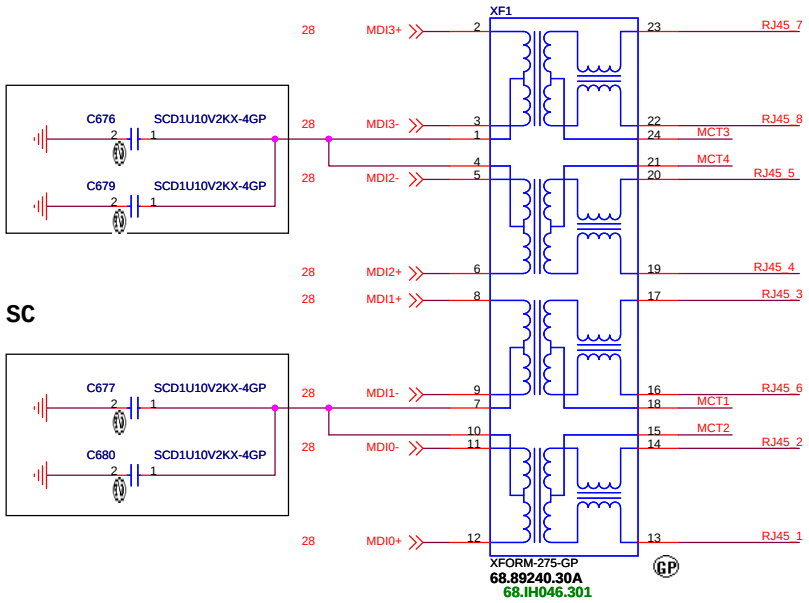
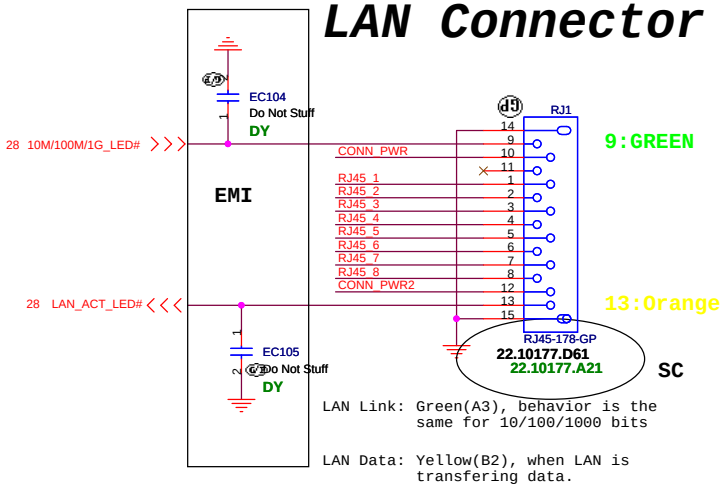
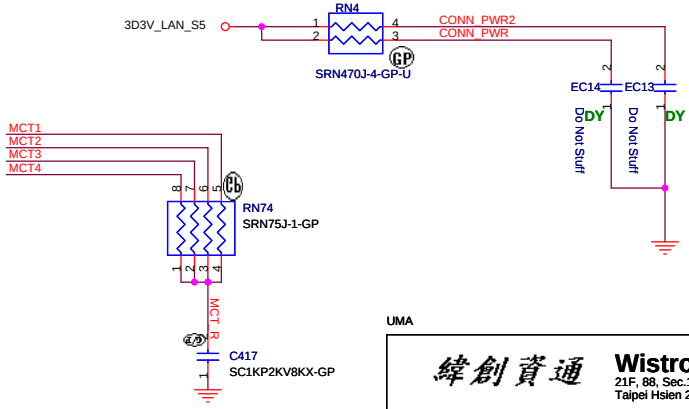
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.







UMA

緯創資通 **Wistron Corporation**
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Title	**LAN CONN**	
Size A3	Document Number **Big Bear 2**	Rev **-1**
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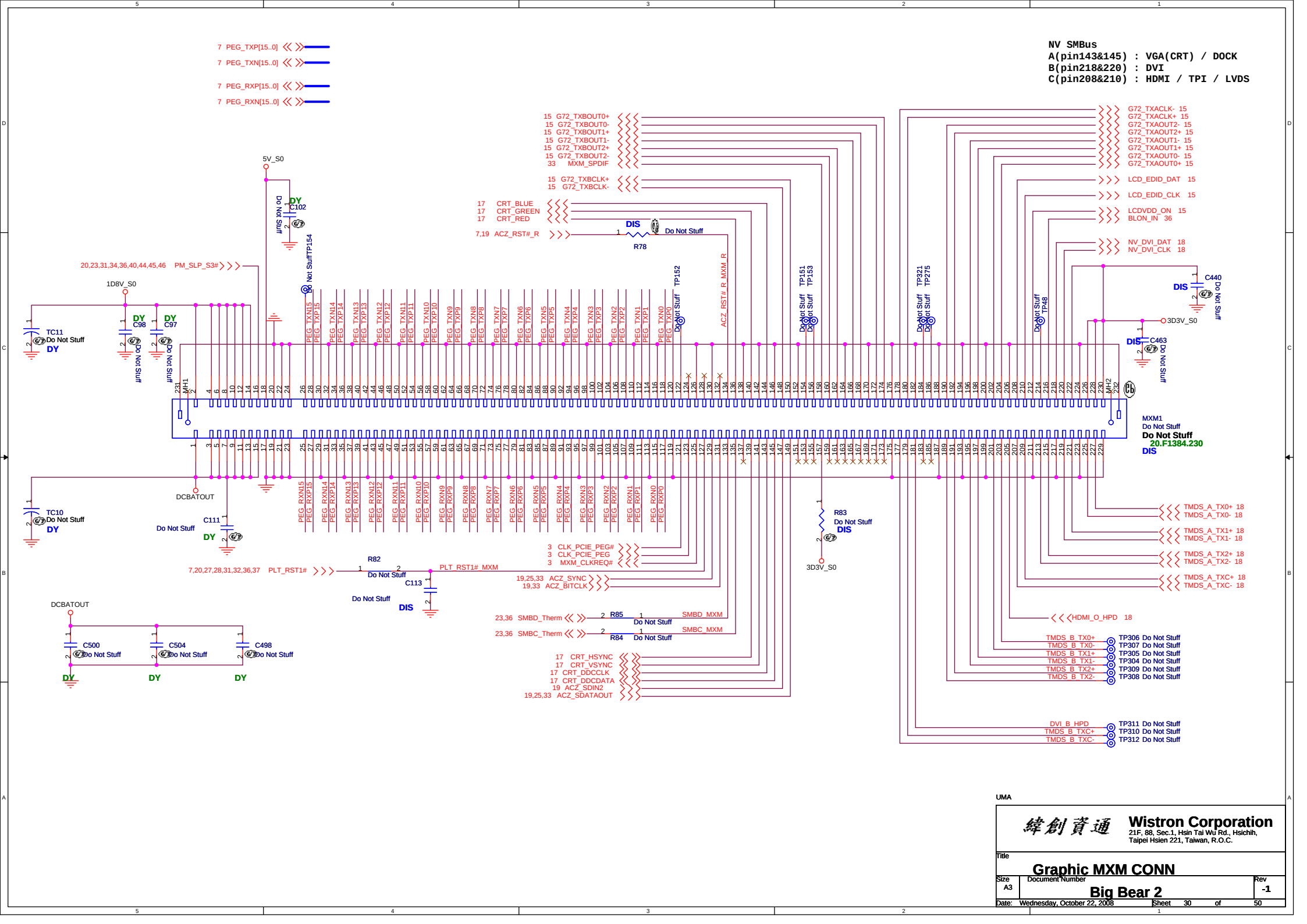
NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS
7 PEG_TXP[15..0]
7 PEG_TXN[15..0]
7 PEG_RXP[15..0]
7 PEG_RXN[15..0]
5V_S0
1D8V_S0
3D3V_S0
DCBATOUT
MXM1
Do Not Stuff
20.F1384.230
DIS
DY
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Graphic MXM CONN
Size A3
Document Number
Big Bear 2
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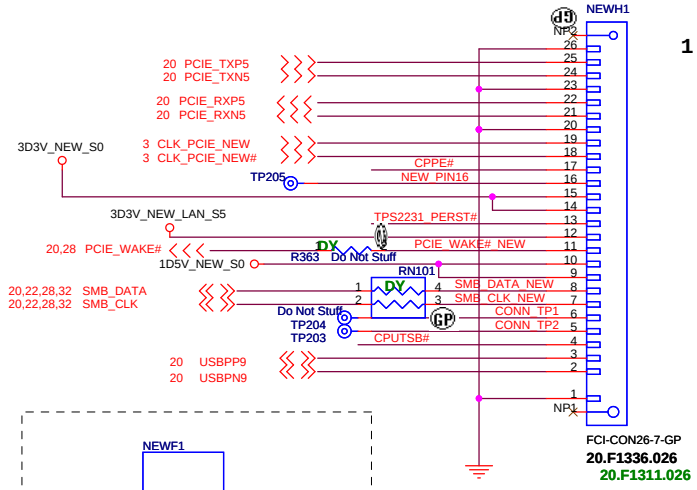
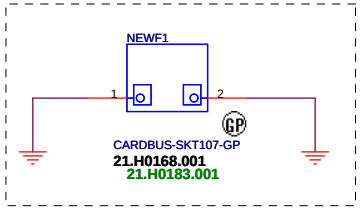
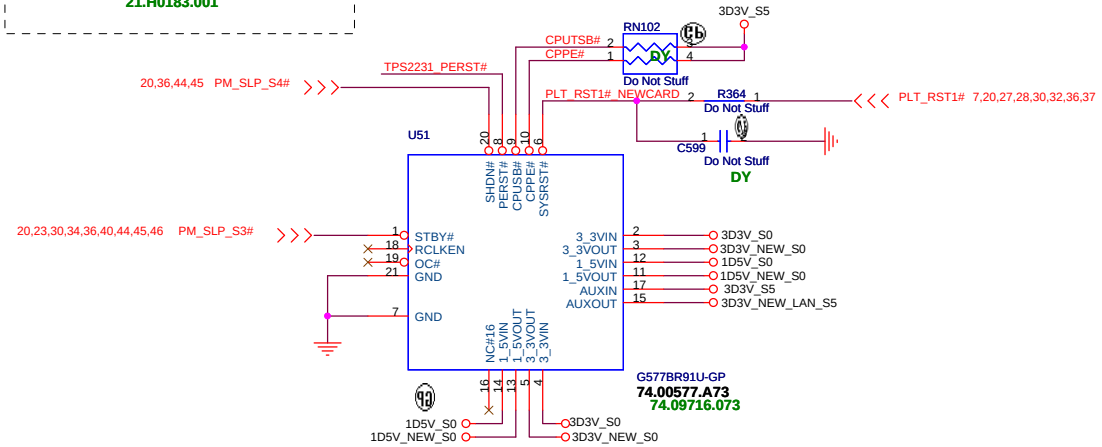
NEWCARD Connector

Reserve the symbol
for bottom side
connector

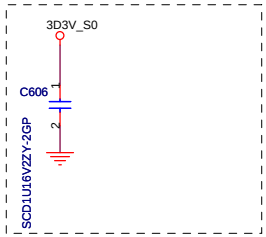
TOP VIEW



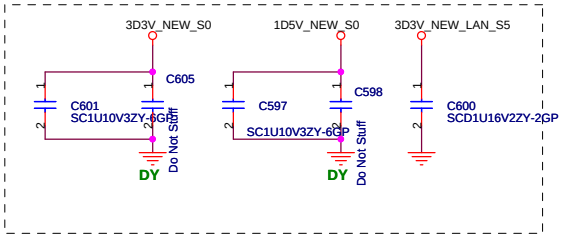




Place them Near to Chip



Place them Near to Connector



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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **NEW CARD**

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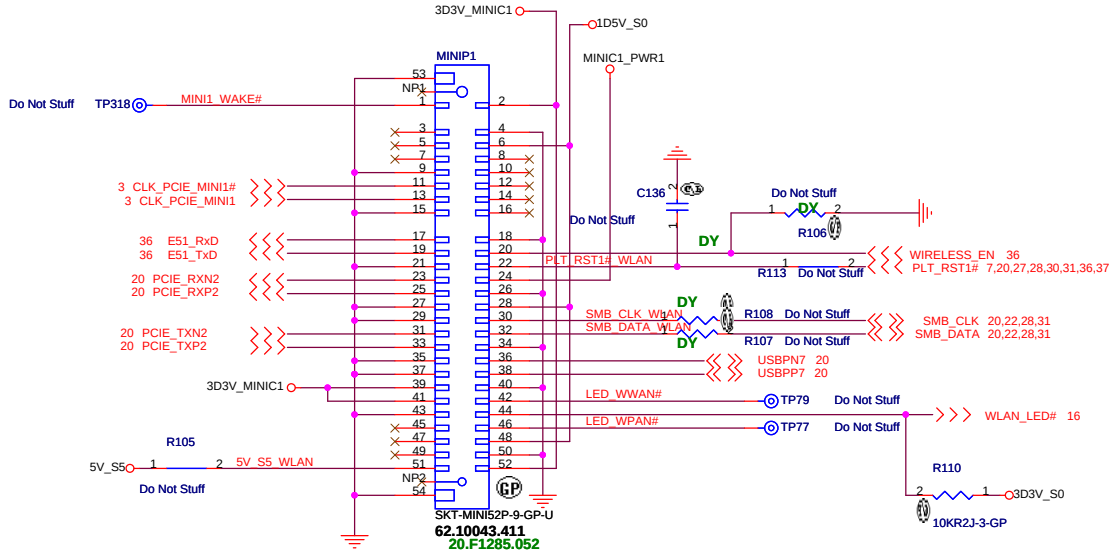
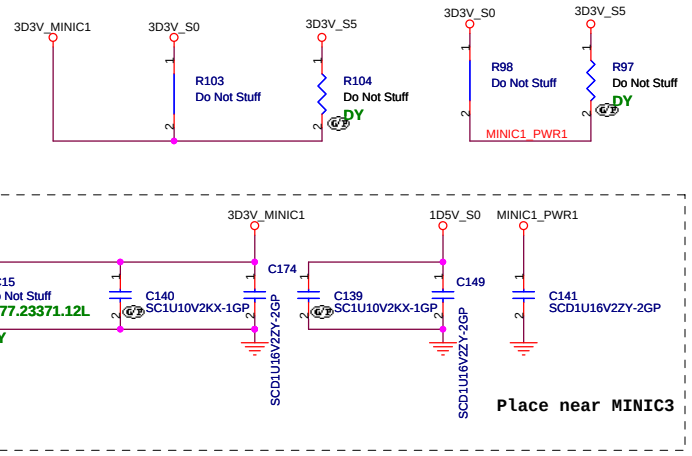
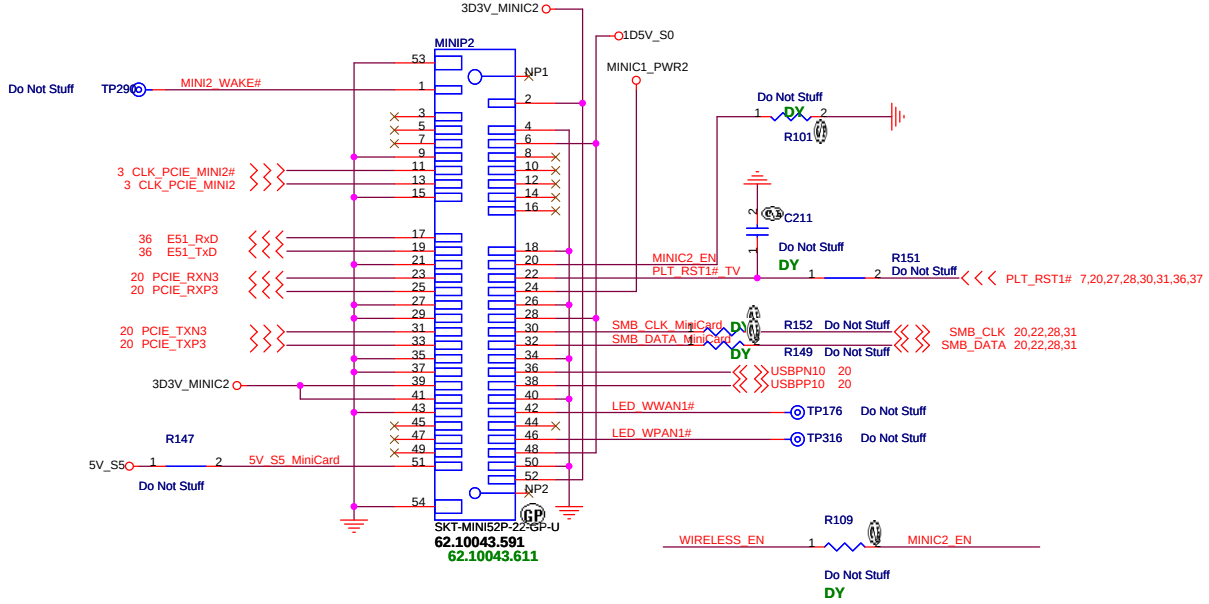
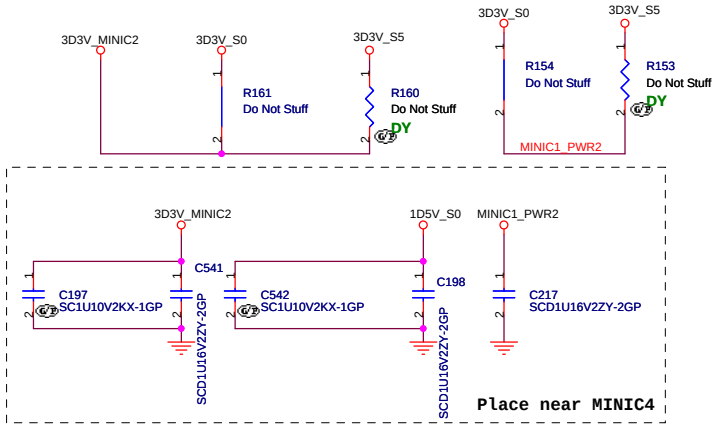
Mini Card Connector(WLAN)









UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
Size: A3	Document Number: Big Bear 2	Rev: -1
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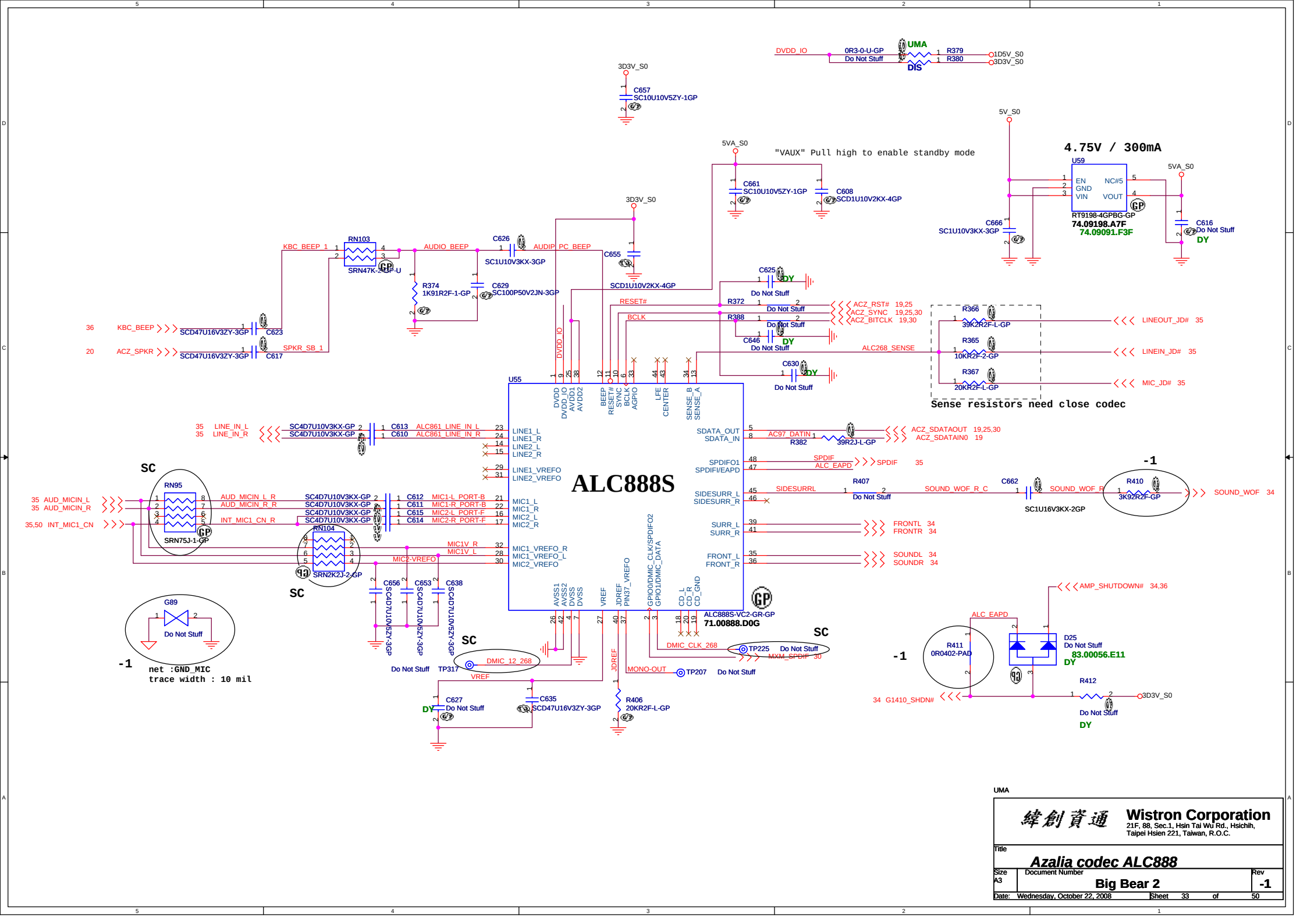
ALC888S
U55
DVDD_IO
0R3-0-U-GP
Do Not Stuff
UMA
DIS
R379
R380
1D5V_S0
3D3V_S0
C657
SC10U10V5ZY-1GP
5V_S0
4.75V / 300mA
U59
EN
GND
VIN
NC#5
VOUT
RT9198-4GPBG-GP
74.09198.A7F
74.09091.F3F
C666
SC1U10V3KX-3GP
C616
Do Not Stuff
DY
5VA_S0
"VAUX" Pull high to enable standby mode
C661
SC10U10V5ZY-1GP
C608
SCD1U10V2KX-4GP
RN103
SRN47K-2GP-U
KBC_BEEP_1
AUDIO_BEEP
C626
SC1U10V3KX-3GP
AUDIP_PC_BEEP
C655
SCD1U10V2KX-4GP
R374
1K91R2F-1-GP
C629
SC100P50V2JN-3GP
C625
Do Not Stuff
RESET#
R372
R388
ACZ_RST# 19,25
ACZ_SYNC 19,25,30
ACZ_BITCLK 19,30
BCLK
C646
Do Not Stuff
ALC268_SENSE
C630
Do Not Stuff
R366
39K2R2F-L-GP
R365
10KR2F-2-GP
R367
20KR2F-L-GP
LINEOUT_JD# 35
LINEIN_JD# 35
MIC_JD# 35
Sense resistors need close codec
36 KBC_BEEP
SCD47U16V3ZY-3GP
C623
20 ACZ_SPKR
SPKR_SB_1
C617
35 LINE_IN_L
35 LINE_IN_R
SC4D7U10V3KX-GP
C613 ALC861_LINE_IN_L
C610 ALC861_LINE_IN_R
LINE1_L
LINE1_R
LINE2_L
LINE2_R
LINE1_VREFO
LINE2_VREFO
SDATA_OUT
SDATA_IN
AC97_DATIN
R382
39R2J-L-GP
ACZ_SDATAOUT 19,25,30
ACZ_SDATAIN0 19
SPDIFO1
SPDIFI/EAPD
SPDIF
ALC_EAPD
SPDIF 35
SIDESURR_L
SIDESURR_R
SIDESURRL
R407
Do Not Stuff
SOUND_WOF_R_C
C662
SC1U16V3KX-2GP
SOUND_WOF_R
R410
3K92R2F-GP
SOUND_WOF 34
SURR_L
SURR_R
FRONTL 34
FRONTR 34
FRONT_L
FRONT_R
SOUNDL 34
SOUNDR 34
SC
RN95
SRN75J-1-GP
35 AUD_MICIN_L
35 AUD_MICIN_R
35,50 INT_MIC1_CN
AUD_MICIN_L_R
AUD_MICIN_R_R
INT_MIC1_CN_R
C612 MIC1-L_PORT-B
C611 MIC1-R_PORT-B
C615 MIC2-L_PORT-F
C614 MIC2-R_PORT-F
MIC1_L
MIC1_R
MIC2_L
MIC2_R
RN104
SRN2K2J-2-GP
MIC1V_R
MIC1V_L
MIC2-VREFO
MIC1_VREFO_R
MIC1_VREFO_L
MIC2_VREFO
C656
C653
C638
SC4D7U10V5ZY-3GP
G89
Do Not Stuff
-1
net :GND_MIC
trace width : 10 mil
DMIC_12_268
TP317
Do Not Stuff
VREF
C627
Do Not Stuff
DY
C635
SCD47U16V3ZY-3GP
JDREF
R406
20KR2F-L-GP
MONO-OUT
TP207
Do Not Stuff
GPIO0/DMIC_CLK/SPDIFO2
GPIO1/DMIC_DATA
DMIC_CLK_268
TP225
Do Not Stuff
MXM_SPDIF 30
ALC888S-VC2-GR-GP
71.00888.D0G
AMP_SHUTDOWN# 34,36
R411
0R0402-PAD
D25
Do Not Stuff
83.00056.E11
R412
Do Not Stuff
34 G1410_SHDN#
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Azalia codec ALC888
Size A3
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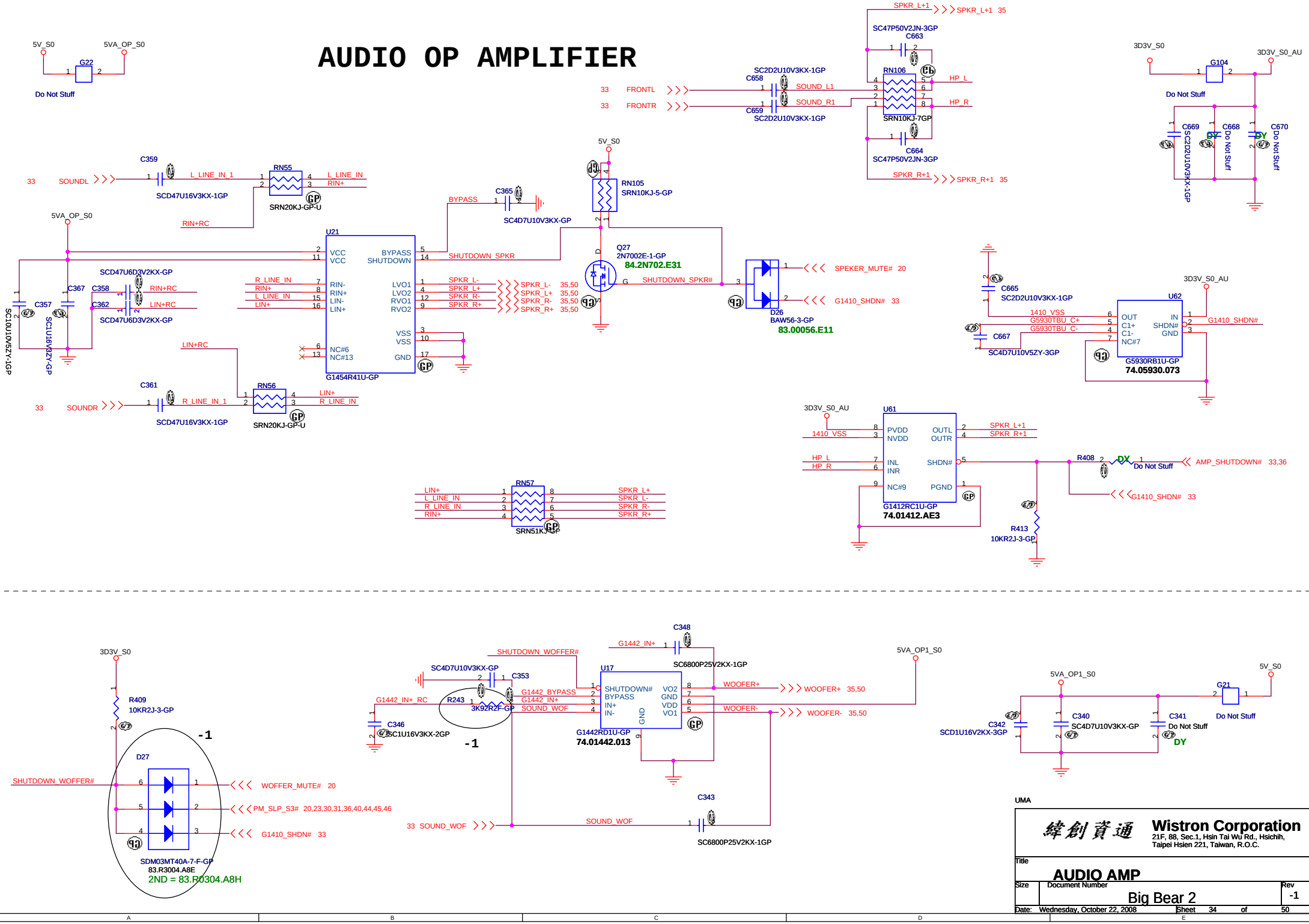
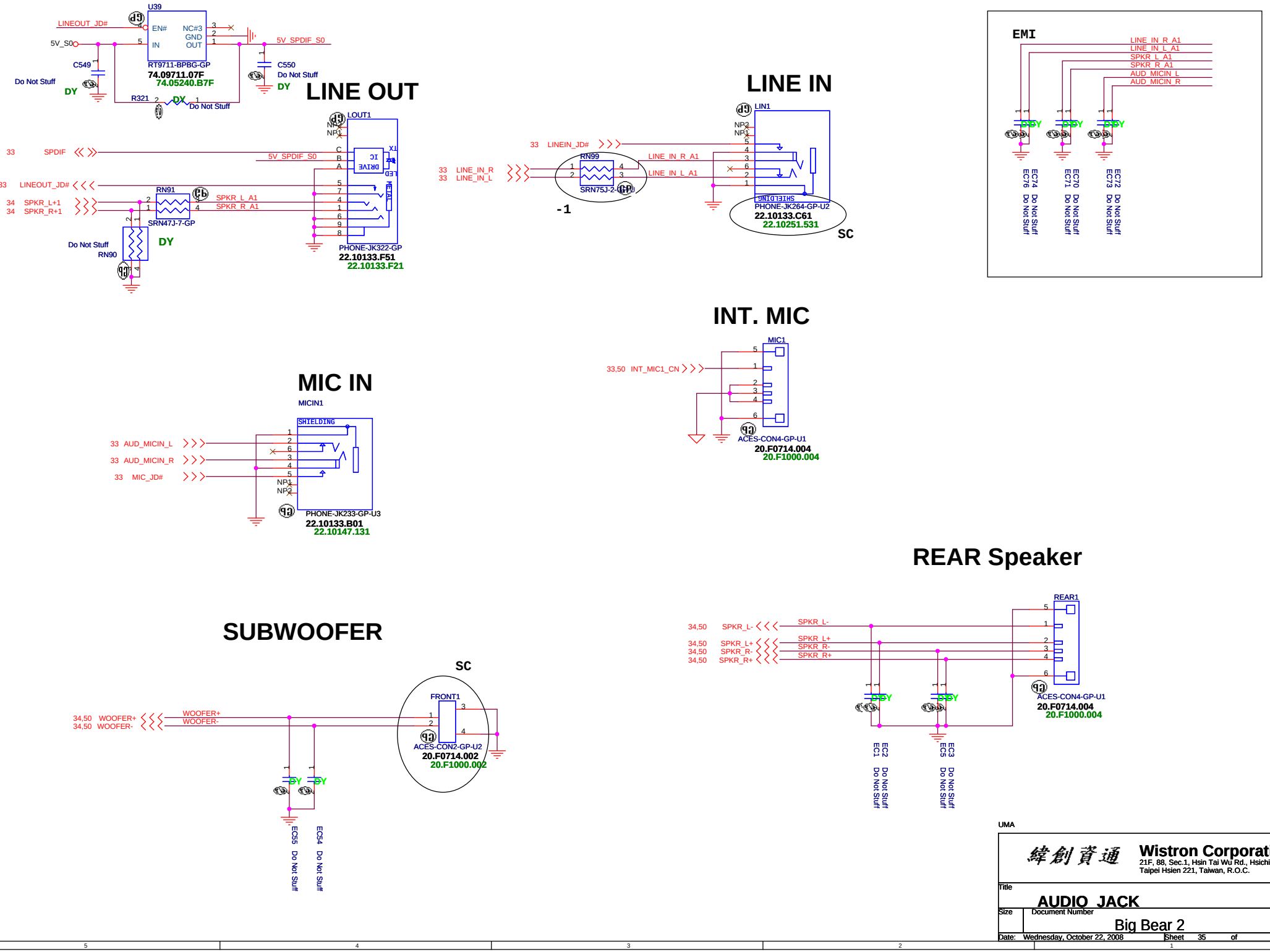
AUDIO OP AMPLIFIER





UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO_JACK**

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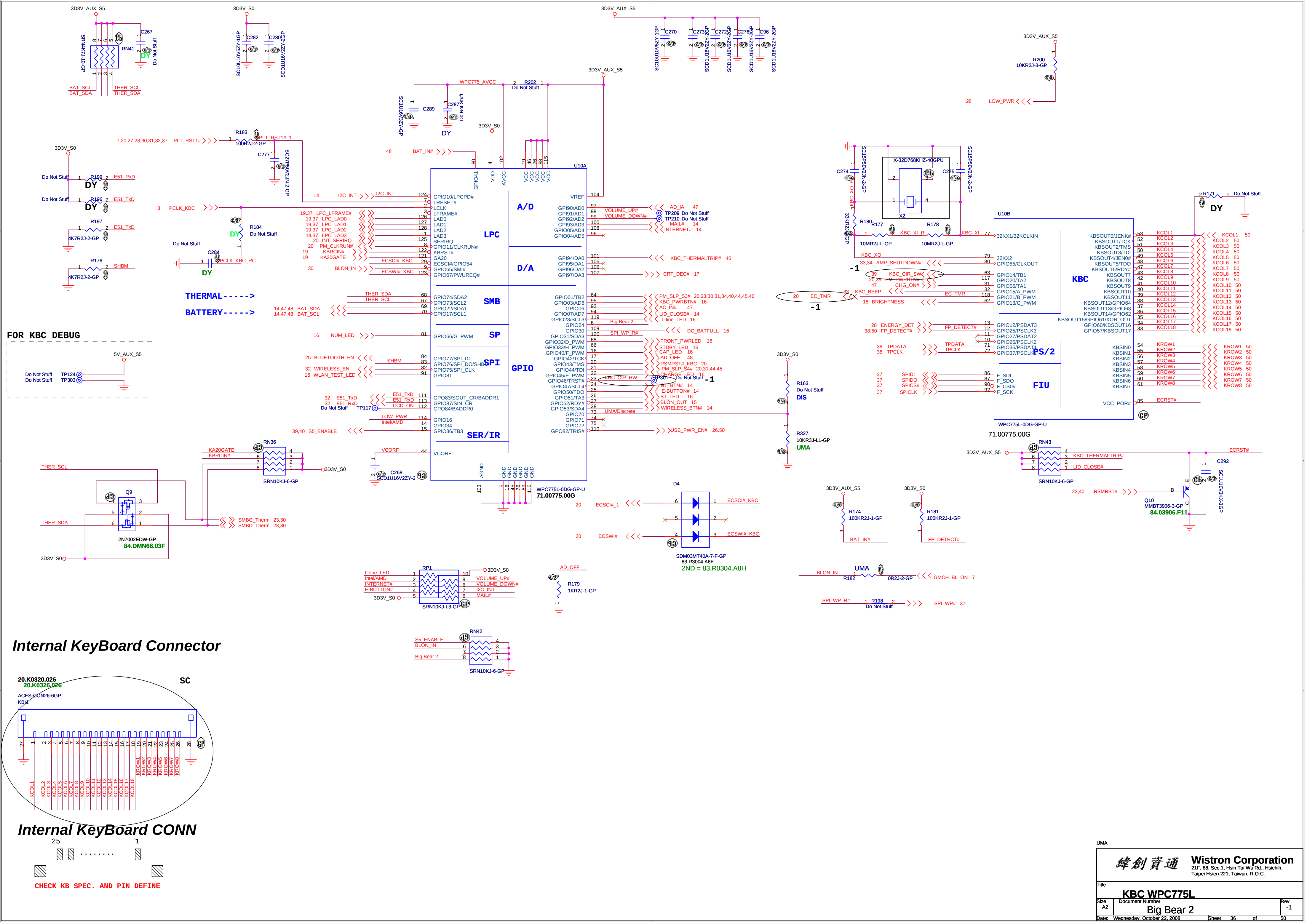
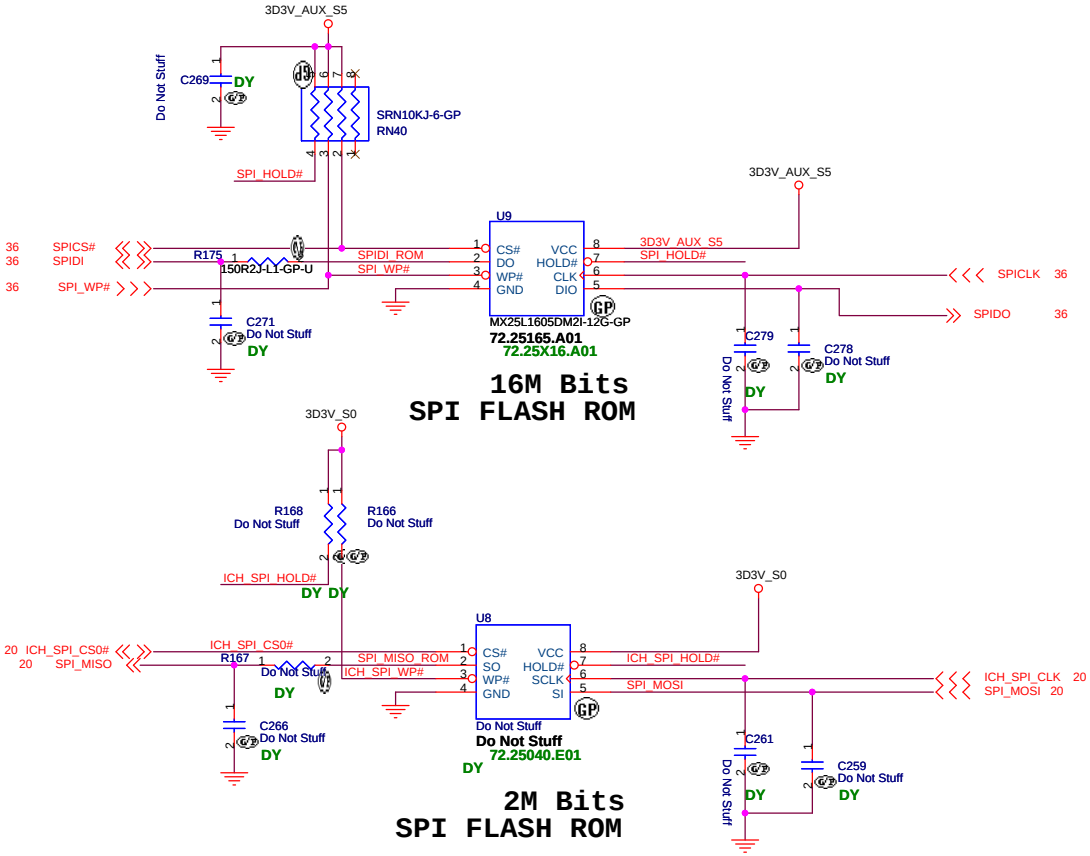
Date: Wednesday, October 22, 2008 Sheet 35 of 50

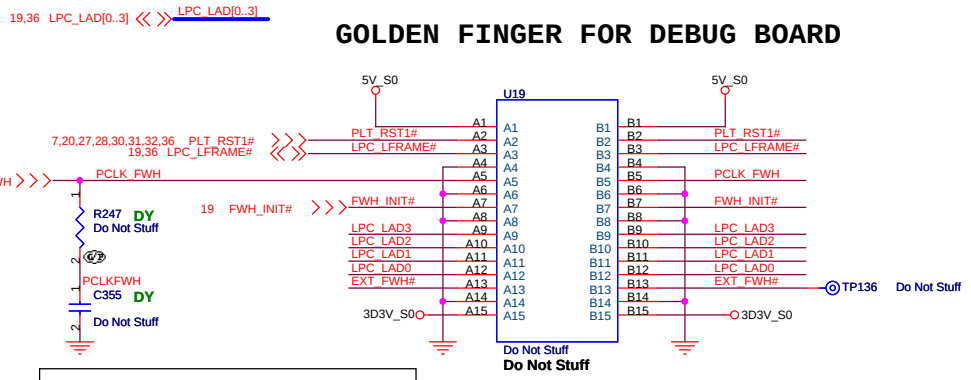

U10A
WPC775L-0DG-GP-U
71.00775.00G
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
U10B
KBC
PS/2
FIU
WPC775L-0DG-GP-U
71.00775.00G
X-32D768KHZ-40GPU
THERMAL----->
BATTERY----->
FOR KBC DEBUG
Internal KeyBoard Connector
20.K0320.026
20.K0326.026
ACES-CON26-6GP
KB1
SC
Internal KeyBoard CONN
25
1
CHECK KB SPEC. AND PIN DEFINE
2N7002EDW-GP
84.DMN66.03F
SDM03MT40A-7-F-GP
83.R3004.A8E
2ND = 83.R0304.A8H
MMBT3906-3-GP
84.03906.F11
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC WPC775L
Size A2
Document Number
Big Bear 2
Rev -1
Date: Wednesday, October 22, 2008
Sheet 36 of 50

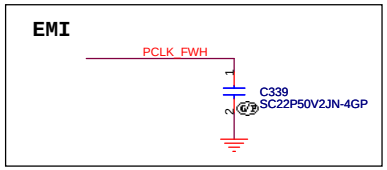


TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)





UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS**

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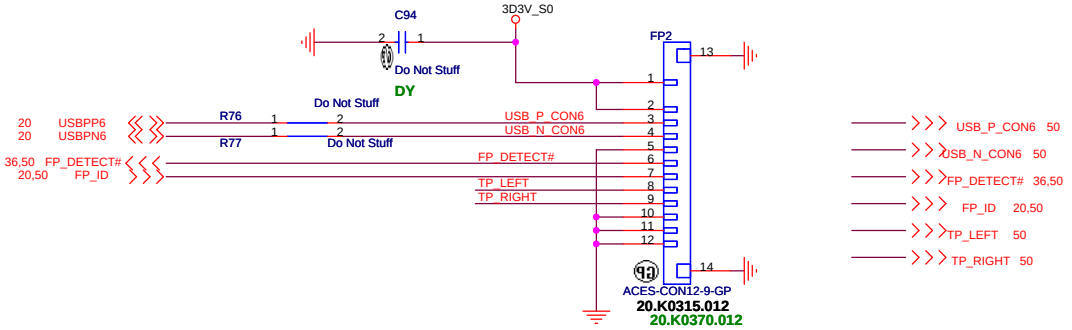
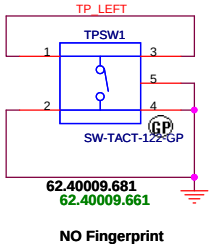
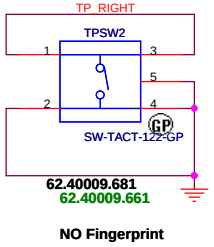
Date: Wednesday, October 22, 2008 Sheet 37 of 50

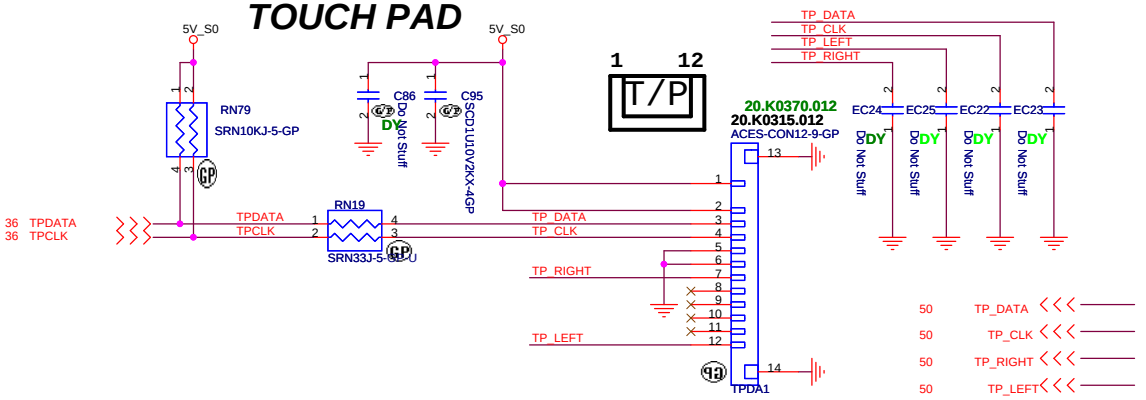
Finger printer







TOUCH PAD



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Finger Printer and Touch PAD**

Size	Document Number	Rev
A3	Big Bear 2	-1

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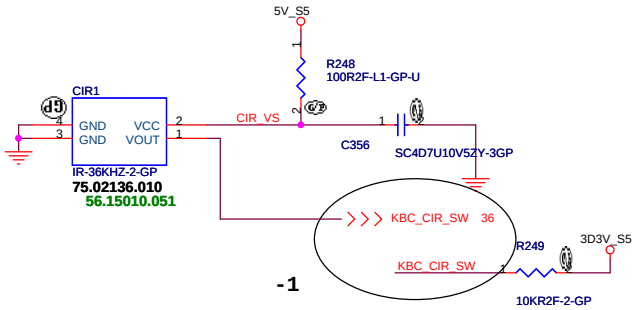
CIR Module



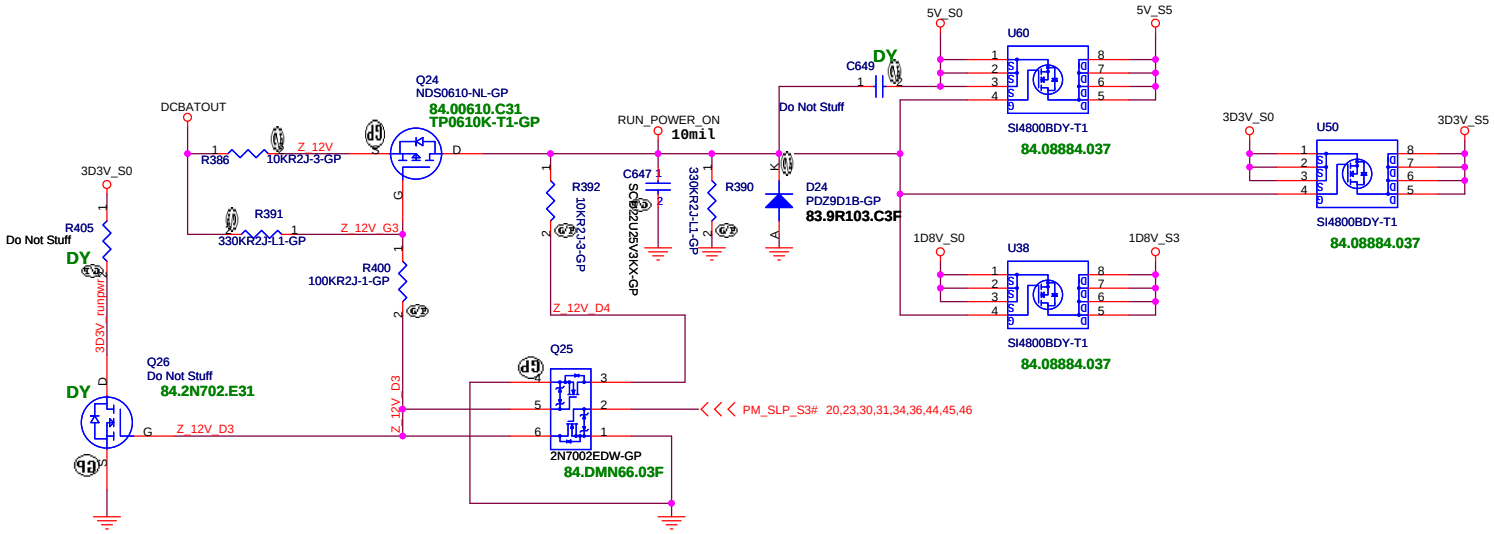
Check test point

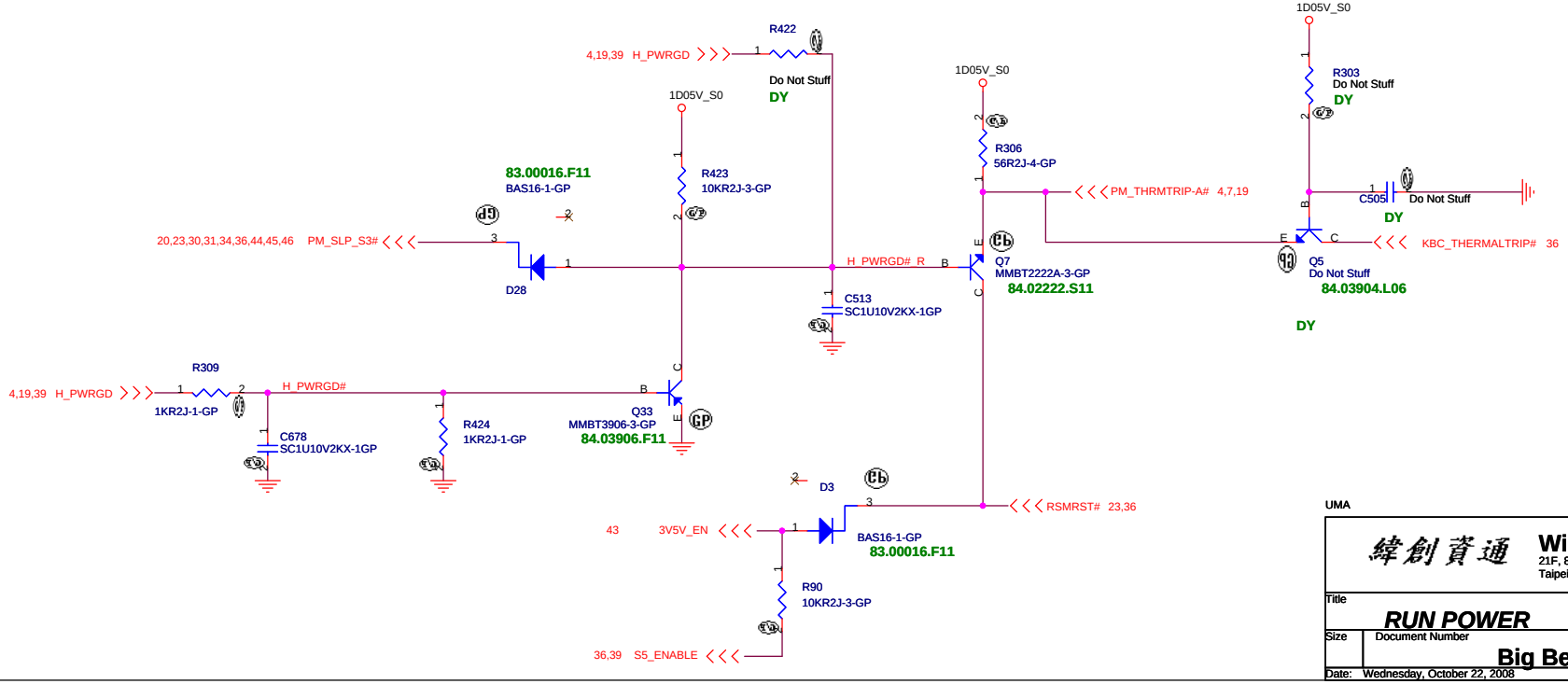
Test Point放在Dimm Door打開可量測處

UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CIR & test point		
Size: A3	Document Number: Big Bear 2	Rev: -1
Date: Wednesday, October 22, 2008	Sheet 39 of 50	

Run Power





UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER**

Size	Document Number	Rev
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CPU_CORE
ISL6266A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6266A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

VGATE_PWRGD

Output Power
VCC_CORE_PWR(O)

VCC_CORE(Imax=38A)

TPS51125
5V/3D3V

DCBATOUT_51125

PM_SLP_S4#

ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (6A)

RT9018A
1D5V_S0

1D8V_S3
PM_SLP_S3#

VIN
EN

1D5V(O)
PGOOD

1D5V_S0 (2.5A)
CPUCORE_ON

RT9026
0D9V_S0

5V_S5
1D8V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5

VTT
VTTREF

0D9V_S3 (1A)
0D9V_S3_1

GFX_CORE
ISL6263A

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Input Power
VDD
VIN

Input Signal
VR_ON

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

CPUCORE_ON

Output Power
VGFXCORE (O)

VCC_GFXCORE(5.5A)

G9131
2D5V_S0

3D3V_S0

INPUT
OUT

2D5V_S0(0.3A)

Charger BQ24750

CHG_ON#
24750_CELLS

AD+

Input Signal
CHGEN#
CELLS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA

BT+
DCBATOUT

TPS51124
1D8V/1D05V

5V_S5
DCBATOUT_51124

PM_SLP_S4#
PM_SLP_S3#

CPUCORE_ON

Input Power
VDD
VCC

Input Signal
EN1
EN2

Output Signal
PGOOD1
PGOOD2

Output Power
1D8V (O)
1D05V(O)

1D8V_S3 (10A)
1D05V_S0 (15A)

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

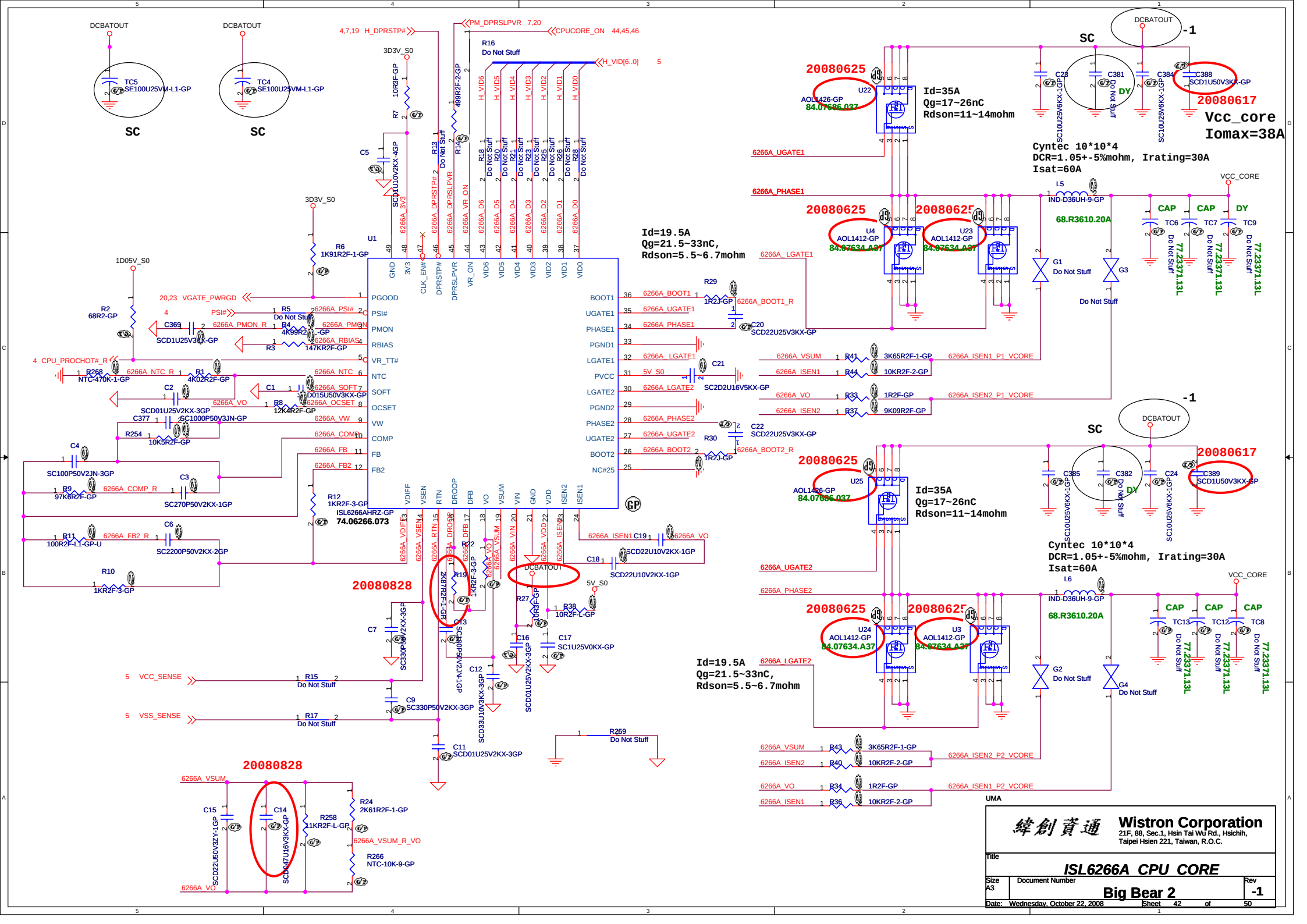
UMA

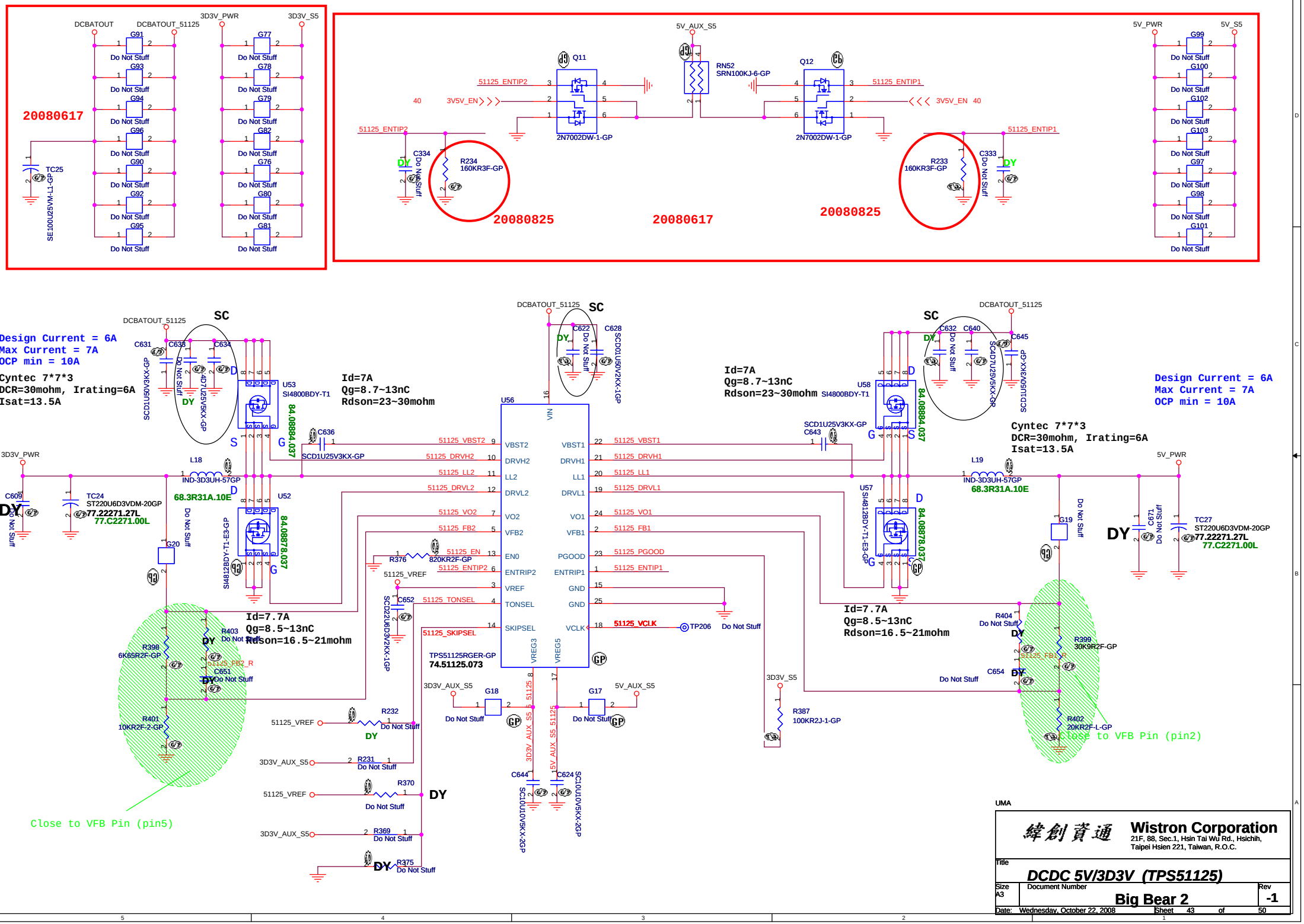
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Sequence Logic**

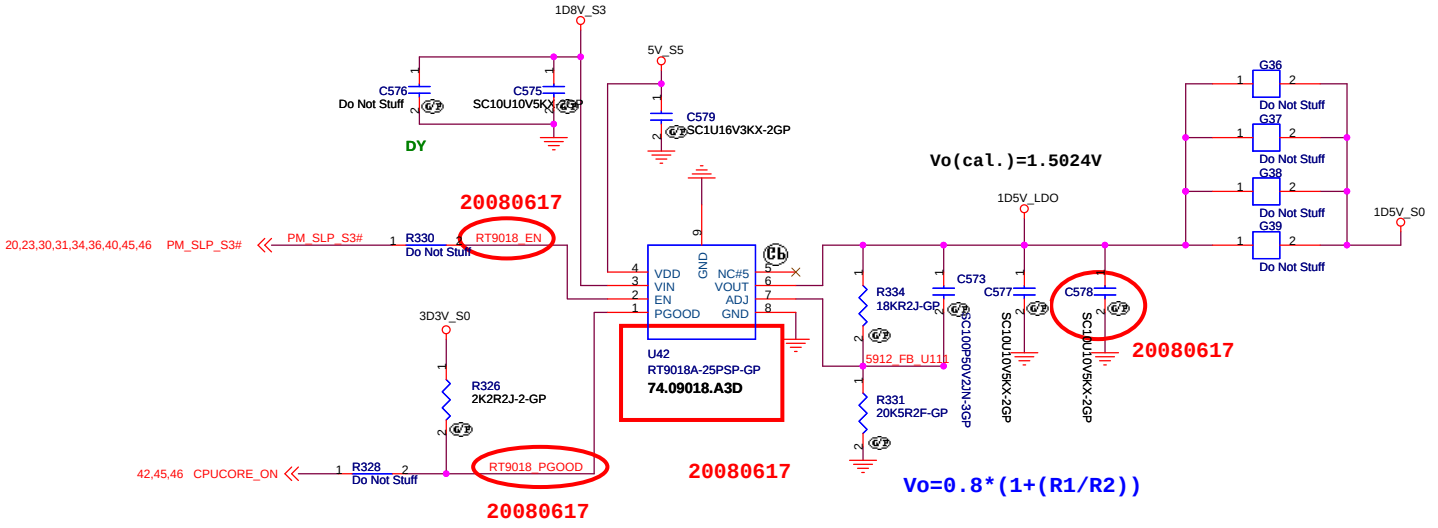
Size: B | Document Number: **Big Bear 2** | Rev: -1

Date: Wednesday, October 22, 2008 | Sheet 41 of 50

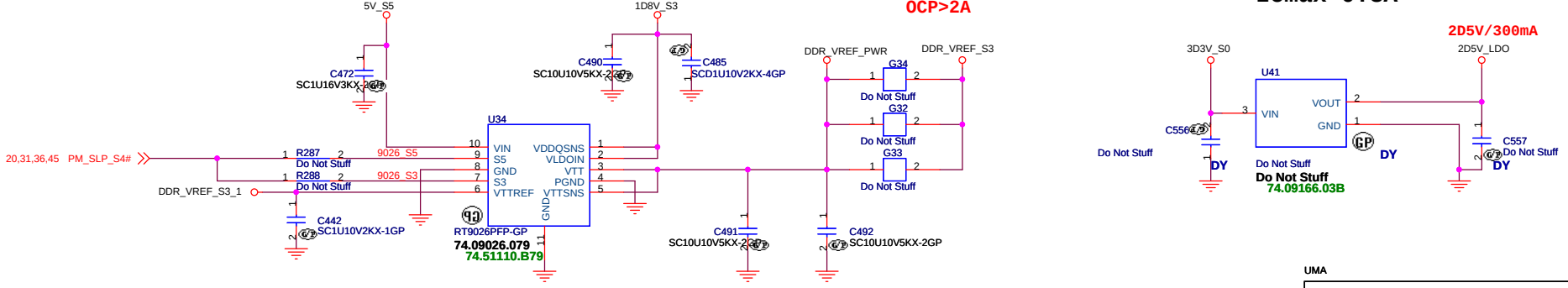

DCBATOUT
TC5
SE100U25VM-L1-GP
SC
DCBATOUT
TC4
SE100U25VM-L1-GP
SC
4,7,19 H_DPRSTP#
PM_DPRSLPVR 7,20
CPUCORE_ON 44,45,46
R16
Do Not Stuff
H_VID[6..0] 5
3D3V_S0
R7 10R3F-GP
499R2F-2-GP
R14
H_VID6
H_VID5
H_VID4
H_VID3
H_VID2
H_VID1
H_VID0
R18 R20 R21 R23 R25 R26 R28
Do Not Stuff
R13 Do Not Stuff
C5 SCD1U10V2KX-4GP
6266A_DPRSTP# 2
6266A_DPRSLPVR
6266A_VR_ON
6266A_D6
6266A_D5
6266A_D4
6266A_D3
6266A_D2
6266A_D1
6266A_D0
6266A_3V3
3D3V_S0
R6 1K91R2F-1-GP
U1
GND
3V3
CLK_EN#
DPRSTP#
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
VID2
VID1
VID0
1D05V_S0
R2 68R2-GP
20,23 VGATE_PWRGD
PSI# R5 Do Not Stuff
6266A_PSI#
6266A_PMON_R R4 4K99R2F-GP
6266A_PMON
6266A_RBIAS
R3 147KR2F-GP
4 CPU_PROCHOT#_R
R268 NTC-470K-1-GP
6266A_NTC_R
R1 4K02R2F-GP
6266A_NTC
C369 SCD1U25V3KX-GP
C2 SCD01U25V2KX-3GP
6266A_VO
C1 D015U50V3KX-GP
6266A_SOFT
6266A_OCSET
R8 12K4R2F-GP
C377 SC1000P50V3JN-GP
6266A_VW
R254 10K5R2F-GP
6266A_COMP
6266A_FB
6266A_FB2
C4 SC100P50V2JN-3GP
R9 97K6R2F-GP
6266A_COMP_R
C3 SC270P50V2KX-1GP
R12 1KR2F-3-GP
ISL6266AHRZ-GP
74.06266.073
C6 SC2200P50V2KX-2GP
R11 100R2F-L1-GP-U
6266A_FB2_R
R10 1KR2F-3-GP
PGOOD
PSI#
PMON
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC#25
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
GND
VDD
ISEN2
ISEN1
6266A_BOOT1
6266A_UGATE1
6266A_PHASE1
6266A_LGATE1
6266A_LGATE2
6266A_PHASE2
6266A_UGATE2
6266A_BOOT2
R29 1R2J-GP
6266A_BOOT1_R
C20 SCD22U25V3KX-GP
C21 SC2D2U16V5KX-GP
R30 1R2J-GP
6266A_BOOT2_R
C22 SCD22U25V3KX-GP
5V_S0
6266A_ISEN1
C19
6266A_VO
C18 SCD22U10V2KX-1GP
DCBATOUT1
R22 1KR2F-3-GP
R19 1KR2F-3-GP
R27 0R2F-GP
R38 10R2F-L-GP
C7 SC330P50V2KX-3GP
C13 SC680P50V2JN-1GP
C16 SCD01U25V2KX-3GP
C17 SC1U25V0KX-GP
C12 SCD33U10V3KX-3GP
C9 SC330P50V2KX-3GP
C11 SCD01U25V2KX-3GP
5 VCC_SENSE
R15 Do Not Stuff
5 VSS_SENSE
R17 Do Not Stuff
R259 Do Not Stuff
20080828
20080828
6266A_VSUM
C15 SCD22U50V3ZY-1GP
C14 SCD047U16V3KX-GP
R258 11KR2F-L-GP
R24 2K61R2F-1-GP
6266A_VSUM_R_VO
R266 NTC-10K-9-GP
6266A_VO
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
20080625
U22
AOL1426-GP
84.07686.037
Id=35A
Qg=17~26nC
Rdson=11~14mohm
6266A_UGATE1
6266A_PHASE1
6266A_LGATE1
20080625
U4
AOL1412-GP
84.07634.A37
20080625
U23
AOL1412-GP
84.07634.A37
L5
IND-D36UH-9-GP
68.R3610.20A
VCC_CORE
G1 Do Not Stuff
G3 Do Not Stuff
CAP TC6
CAP TC7
DY TC9
77.23371.13L
6266A_VSUM
R41 3K65R2F-1-GP
6266A_ISEN1
R44 10KR2F-2-GP
6266A_ISEN1_P1_VCORE
6266A_VO
R33 1R2F-GP
6266A_ISEN2
R37 9K09R2F-GP
6266A_ISEN2_P1_VCORE
C23
C381 Do Not Stuff
DY
C384
SC10U25V6KX-1GP
C388
SCD1U50V3KX-GP
20080617
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
-1
SC
DCBATOUT
20080625
U25
AOL1426-GP
84.07686.037
Id=35A
Qg=17~26nC
Rdson=11~14mohm
6266A_UGATE2
6266A_PHASE2
6266A_LGATE2
20080625
U24
AOL1412-GP
84.07634.A37
20080625
U3
AOL1412-GP
84.07634.A37
L6
IND-D36UH-9-GP
68.R3610.20A
VCC_CORE
G2 Do Not Stuff
G4 Do Not Stuff
CAP TC13
CAP TC12
CAP TC8
77.23371.13L
6266A_VSUM
R43 3K65R2F-1-GP
6266A_ISEN2
R40 10KR2F-2-GP
6266A_ISEN2_P2_VCORE
6266A_VO
R34 1R2F-GP
6266A_ISEN1
R36 10KR2F-2-GP
6266A_ISEN1_P2_VCORE
C385
C382 Do Not Stuff
DY
C24
SC10U25V6KX-1GP
C389
SCD1U50V3KX-GP
20080617
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
-1
SC
DCBATOUT
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A CPU CORE
Size A3
Document Number
Big Bear 2
Rev -1
Date: Wednesday, October 22, 2008
Sheet 42 of 50


20080617
20080825
20080617
20080825
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
TPS51125RGER-GP
74.51125.073
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Big Bear 2
Wednesday, October 22, 2008

1D5V_S0
Iomax=2.5A

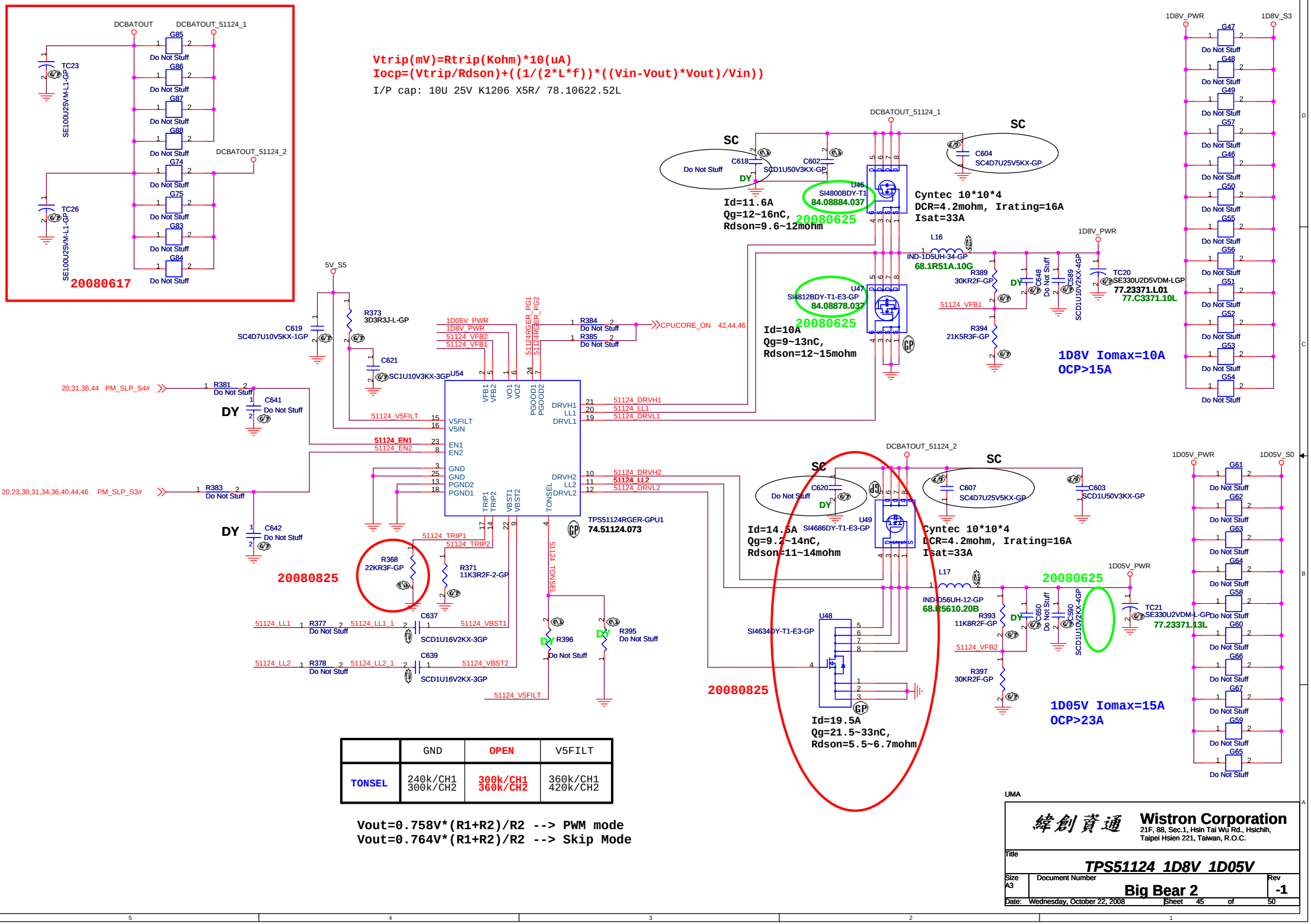


2D5V_S0
Iomax=0.3A

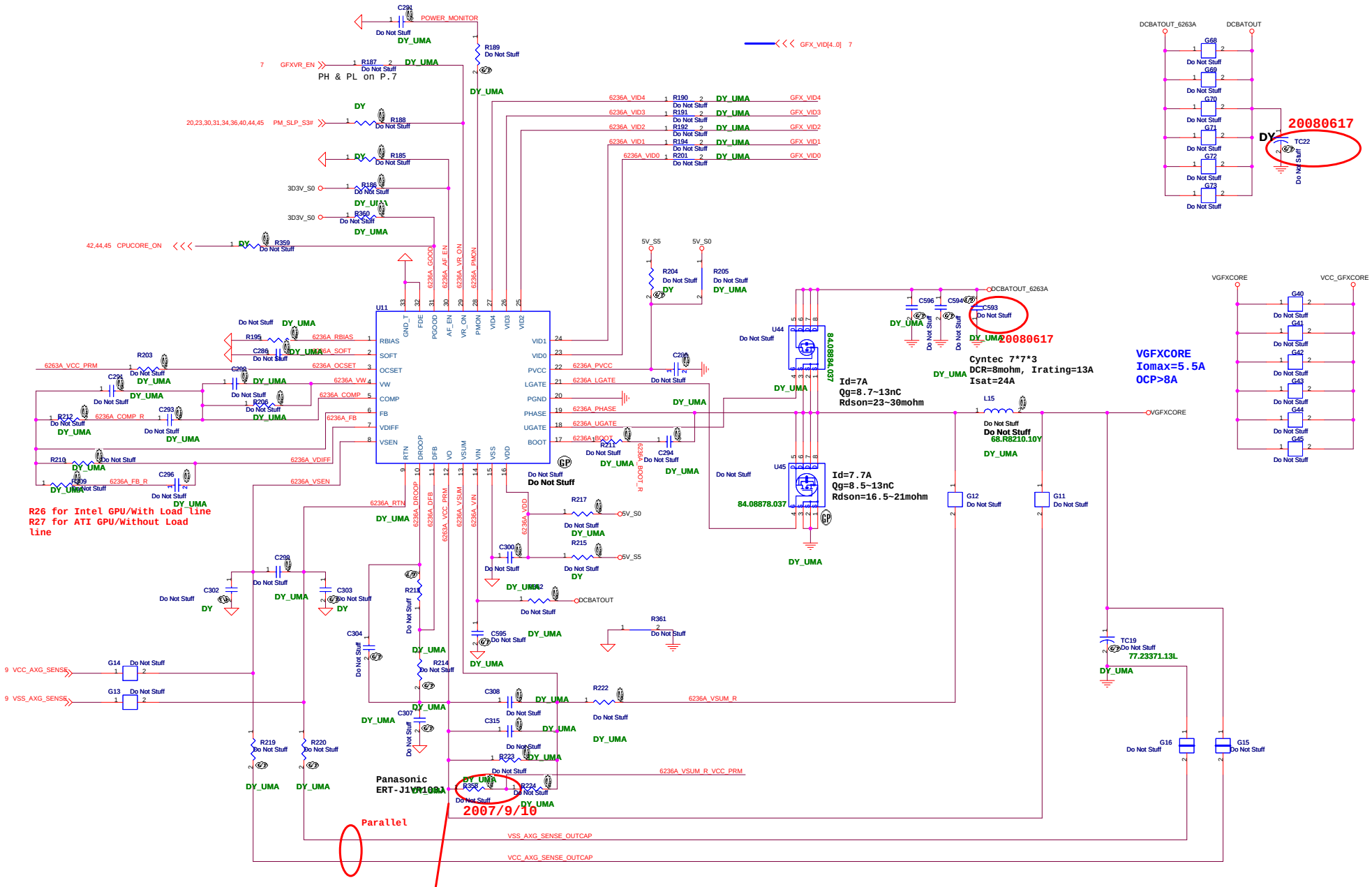


UMA

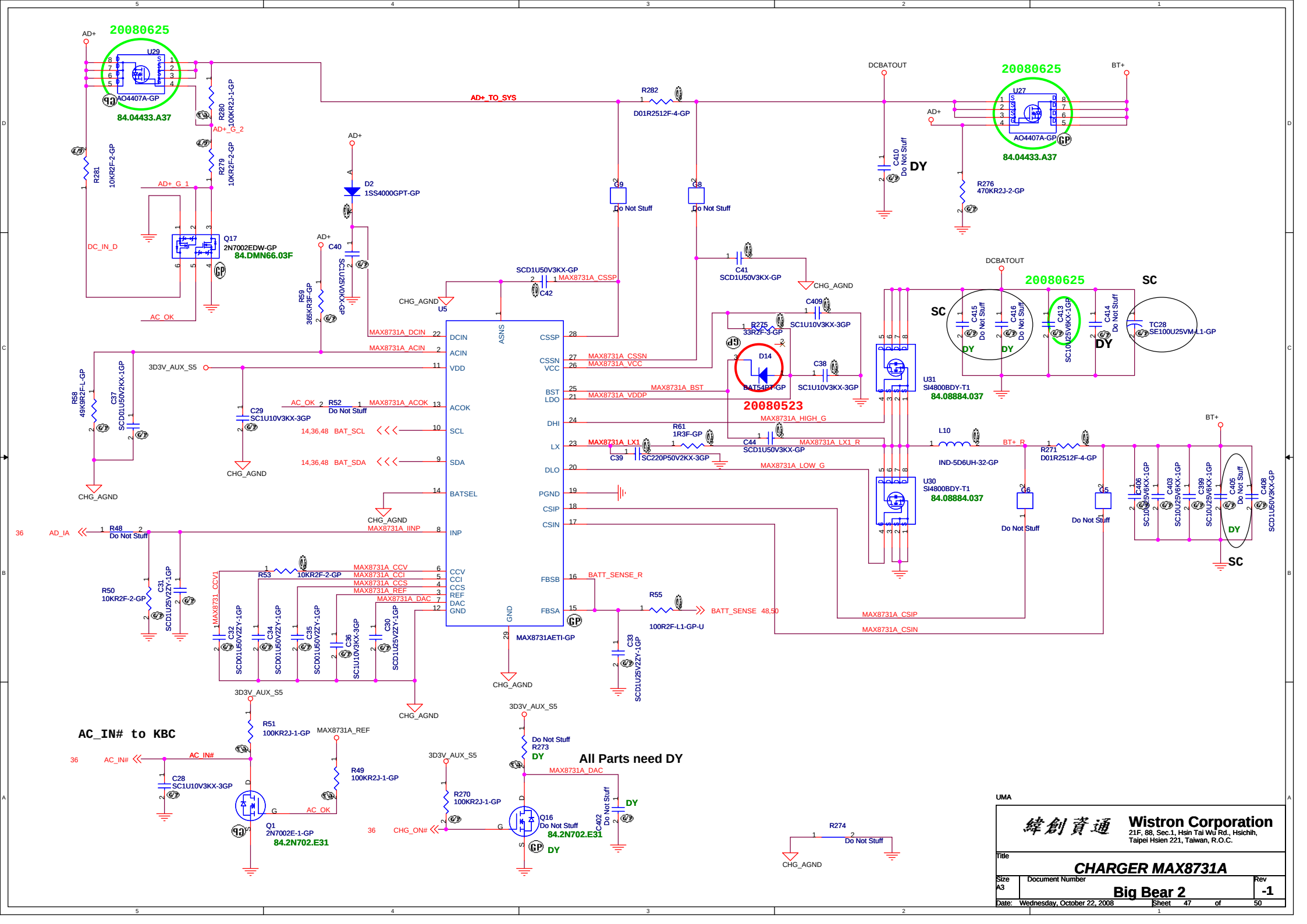
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *1D5V & 0D9V & 2D5V*		
Size: A3	Document Number: Big Bear 2	Rev: -1
Date: Wednesday, October 22, 2008	Sheet 44 of 50	



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL6236A_GFX CORE
Size: C	Document Number: Big Bear 2
Rev	-1
Date: Wednesday, October 22, 2008	Sheet 46 of 50


20080625
U29
AO4407A-GP
84.04433.A37
AD+
AD+_TO_SYS
R280 100KR2J-1-GP
AD+_G_2
R279 10KR2F-2-GP
R281 10KR2F-2-GP
AD+_G_1
Q17
2N7002EDW-GP
84.DMN66.03F
DC_IN_D
AC_OK
D2
1SS4000GPT-GP
C40
SCD1U25V6KX-GP
R59 365KR3F-GP
CHG_AGND
U5
SCD1U50V3KX-GP
C42
MAX8731A_CSSP
R282
D01R2512F-4-GP
DCBATOUT
BT+
C410 Do Not Stuff
DY
R276 470KR2J-2-GP
G9 Do Not Stuff
G8 Do Not Stuff
C41 SCD1U50V3KX-GP
C409
R275 33R2F-3-GP
SC1U10V3KX-3GP
D14
BAT54PT-GP
C38
SC1U10V3KX-3GP
20080523
U31
SI4800BDY-T1
84.08884.037
SC
C415 Do Not Stuff
C416 Do Not Stuff
C413 SC10U25V6KX-1GP
C414 Do Not Stuff
TC28 SE100U25VM-L1-GP
MAX8731A_DCIN
MAX8731A_ACIN
MAX8731A_ACOK
MAX8731A_CCV
MAX8731A_CCI
MAX8731A_CCS
MAX8731A_REF
MAX8731A_DAC
MAX8731A_IINP
MAX8731A_CSSN
MAX8731A_VCC
MAX8731A_BST
MAX8731A_VDDP
MAX8731A_HIGH_G
MAX8731A_LX1
MAX8731A_LX1_R
MAX8731A_LOW_G
MAX8731A_CSIP
MAX8731A_CSIN
BATT_SENSE_R
BATT_SENSE 48,50
DCIN
ACIN
VDD
ACOK
SCL
SDA
BATSEL
INP
CCV
CCI
CCS
REF
DAC
GND
ASNS
CSSP
CSSN
VCC
BST
LDO
DHI
LX
DLO
PGND
CSIP
CSIN
FBSB
FBSA
MAX8731AETI-GP
3D3V_AUX_S5
R58 49K9R2F-L-GP
C37 SCD01U50V2KX-1GP
C29 SC1U10V3KX-3GP
R52 Do Not Stuff
14,36,48 BAT_SCL
14,36,48 BAT_SDA
36 AD_IA
R48 Do Not Stuff
R50 10KR2F-2-GP
C31 SCD1U25V2ZY-1GP
R53 10KR2F-2-GP
C32 SCD01U50V2ZY-1GP
C34 SCD01U50V2ZY-1GP
C35 SCD01U50V2ZY-1GP
C36 SC1U10V3KX-3GP
C30 SCD1U25V2ZY-1GP
R55
100R2F-L1-GP-U
C33 SCD1U25V2ZY-1GP
L10
IND-5D6UH-32-GP
R271 D01R2512F-4-GP
U30
SI4800BDY-T1
84.08884.037
G6 Do Not Stuff
G5 Do Not Stuff
C406 SC10U25V6KX-1GP
C403 SC10U25V6KX-1GP
C399 SC10U25V6KX-1GP
C405 Do Not Stuff
C408 SCD1U50V3KX-GP
AC_IN# to KBC
36 AC_IN#
R51 100KR2J-1-GP
C28 SC1U10V3KX-3GP
R49 100KR2J-1-GP
Q1
2N7002E-1-GP
84.2N702.E31
R270 100KR2J-1-GP
36 CHG_ON#
Q16
Do Not Stuff
84.2N702.E31
C402 Do Not Stuff
R273 Do Not Stuff
All Parts need DY
R274 Do Not Stuff
UMA
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Title
CHARGER MAX8731A
Size A3
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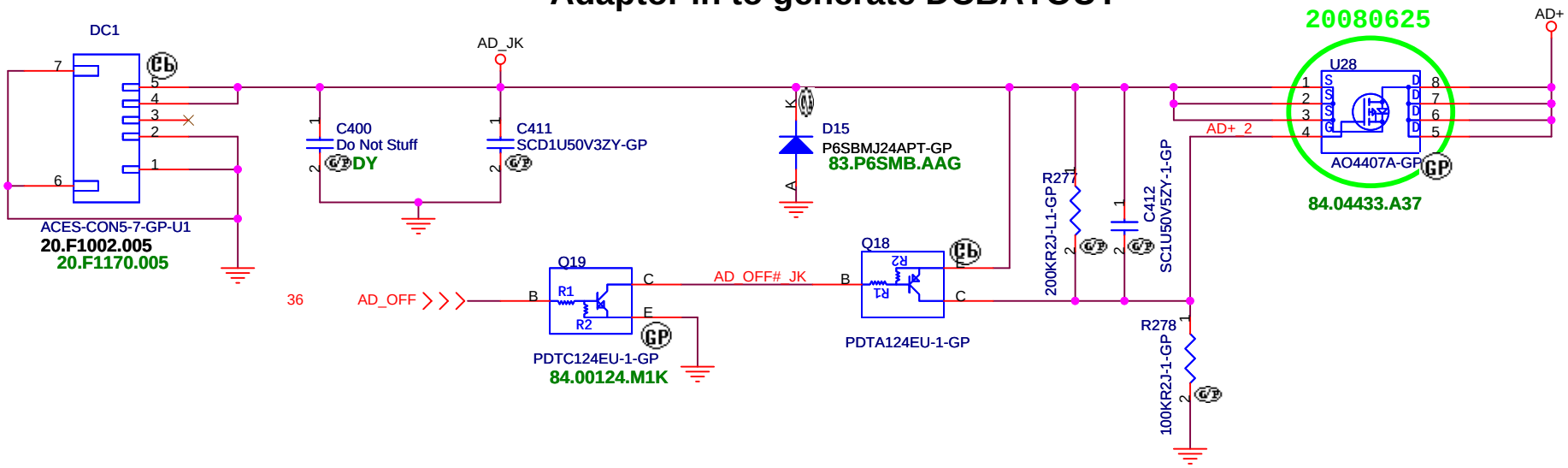
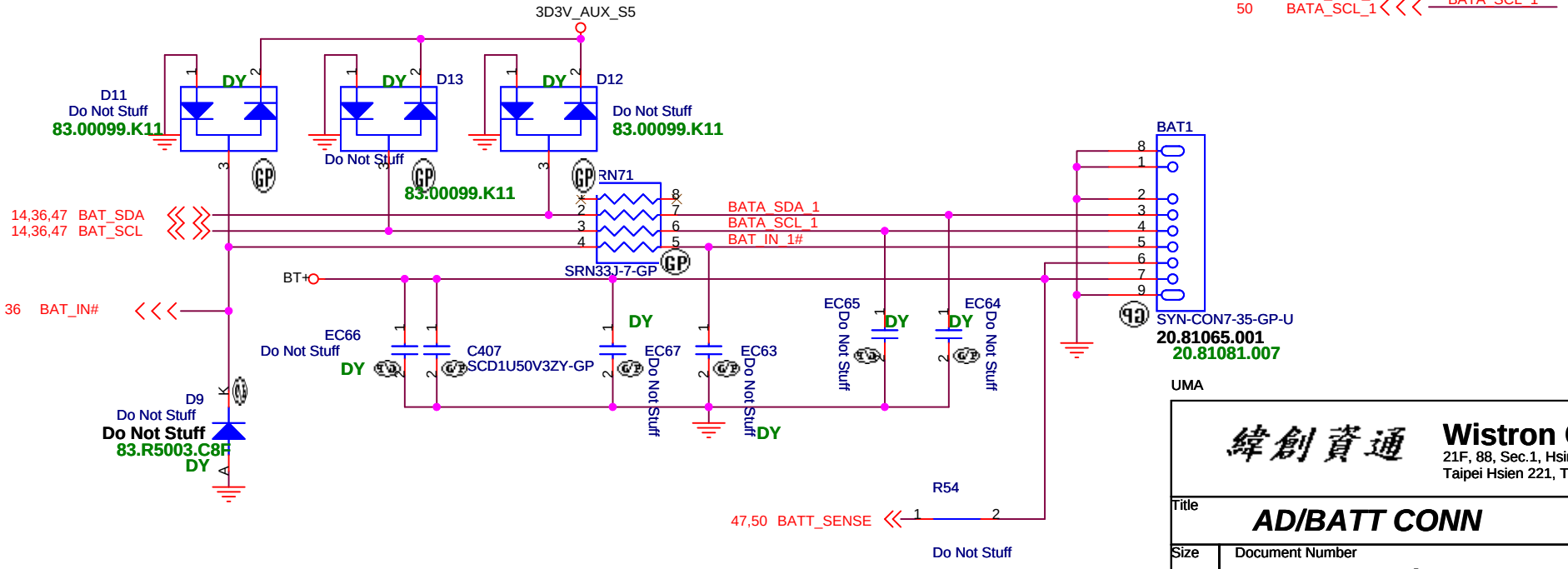
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



47,50 BATT_SENSE — BATT_SENSE
50 BAT_IN_1# — BAT_IN_1#
50 BATA_SDA_1 — BATA_SDA_1
50 BATA_SCL_1 — BATA_SCL_1

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STAND OFF

SPRING ON BOTTOM

CPU & NB

H31 HOLE — 34.42Y01.011
H32 HOLE — 34.42Y01.011
H33 HOLE — 34.42Y01.011
H34 HOLE — 34.42Y01.011

MDC

H21 HOLE — 34.42Y01.011
H22 HOLE — 34.42Y01.011

Mini Card

H35 HOLE — 34.4Z402.001
H36 HOLE — 34.4Z402.001
H37 HOLE — 34.4AJ01.001
H38 HOLE — 34.4AJ01.001

MXM

H14 Do Not Stuff — DIS_34.4Z401.001
H17 Do Not Stuff — DIS_34.4Z401.001

DIMM

GND1 Do Not Stuff Do Not Stuff DY

Touch Pad

SC

MXM SPRING

S1 Do Not Stuff DIS
S3 Do Not Stuff DIS
S2 Do Not Stuff DIS

H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H13 H18 PAD1 Do Not Stuff

GND2 Do Not Stuff Do Not Stuff DY
GND3 Do Not Stuff Do Not Stuff DY

H39 H40 Do Not Stuff

EMI

DCBATOUT
EC6 SCD1U50V3ZY-GP DY
EC15 Do Not Stuff DY
EC16 SCD1U50V3ZY-GP DY
EC50 Do Not Stuff DY
EC53 Do Not Stuff DY
EC41 Do Not Stuff DY
EC31 Do Not Stuff DY
EC12 Do Not Stuff DY
EC11 Do Not Stuff DY
EC10 SCD1U50V3ZY-GP DY
EC9 SCD1U50V3ZY-GP

DCBATOUT
EC7 Do Not Stuff DY
EC8 SCD1U50V3ZY-GP DY

5V_USB1_S0
EC29 Do Not Stuff DY

1D8V_S3
EC17 Do Not Stuff DY
EC77 Do Not Stuff DY
EC20 Do Not Stuff DY

3D3V_S0
EC38 Do Not Stuff DY
EC40 Do Not Stuff DY
EC45 Do Not Stuff DY
EC42 Do Not Stuff DY
EC47 SCD1U50V3ZY-GP DY
EC35 Do Not Stuff DY
EC62 Do Not Stuff DY

3D3V_S0
EC81 Do Not Stuff DY
EC79 Do Not Stuff DY
EC59 Do Not Stuff DY
EC21 Do Not Stuff DY
EC58 Do Not Stuff DY

1D05V_S0
EC27 Do Not Stuff DY

1D05V_S0
EC75 Do Not Stuff DY
EC39 Do Not Stuff DY

5V_S0
EC83 Do Not Stuff DY
EC84 Do Not Stuff DY

5V_S0
EC28 Do Not Stuff DY
EC26 Do Not Stuff DY
EC68 Do Not Stuff DY
EC4 Do Not Stuff DY
EC18 Do Not Stuff DY
EC82 Do Not Stuff DY
EC37 Do Not Stuff DY
EC80 Do Not Stuff DY

BT+
EC100 Do Not Stuff DY
EC99 Do Not Stuff DY

5V_S5
EC49 Do Not Stuff DY
EC57 Do Not Stuff DY

3D3V_S5
EC46 Do Not Stuff DY
EC56 Do Not Stuff DY
EC78 Do Not Stuff DY
EC48 Do Not Stuff DY
EC36 Do Not Stuff DY

1D8V_S3
EC86 Do Not Stuff DY
EC85 Do Not Stuff DY
EC87 Do Not Stuff DY
EC89 Do Not Stuff DY
EC88 Do Not Stuff DY
EC90 Do Not Stuff DY

AD_JK
EC101 Do Not Stuff DY

1D05V_S0
EC93 Do Not Stuff DY
EC92 Do Not Stuff DY
EC91 Do Not Stuff DY
EC95 Do Not Stuff DY
EC94 Do Not Stuff DY

5V_S0
EC97 Do Not Stuff DY
EC96 Do Not Stuff DY

DCBATOUT
EC98 Do Not Stuff DY

VCC_GFXCORE
EC106 Do Not Stuff DY
EC107 Do Not Stuff DY
EC108 Do Not Stuff DY

DCBATOUT
EC109 SCD1U50V3ZY-GP
EC110 Do Not Stuff DY

Near H38

S4 Do Not Stuff DY
S5 SPRING-7 DY

Near SB

S6 Do Not Stuff DY
S7 Do Not Stuff DY

Near CRT

S8 Do Not Stuff DY
S9 Do Not Stuff DY

USB port

S10 Do Not Stuff DY
S11 Do Not Stuff DY
S12 Do Not Stuff DY

HDMI

S13 Do Not Stuff DY

SC

UMA

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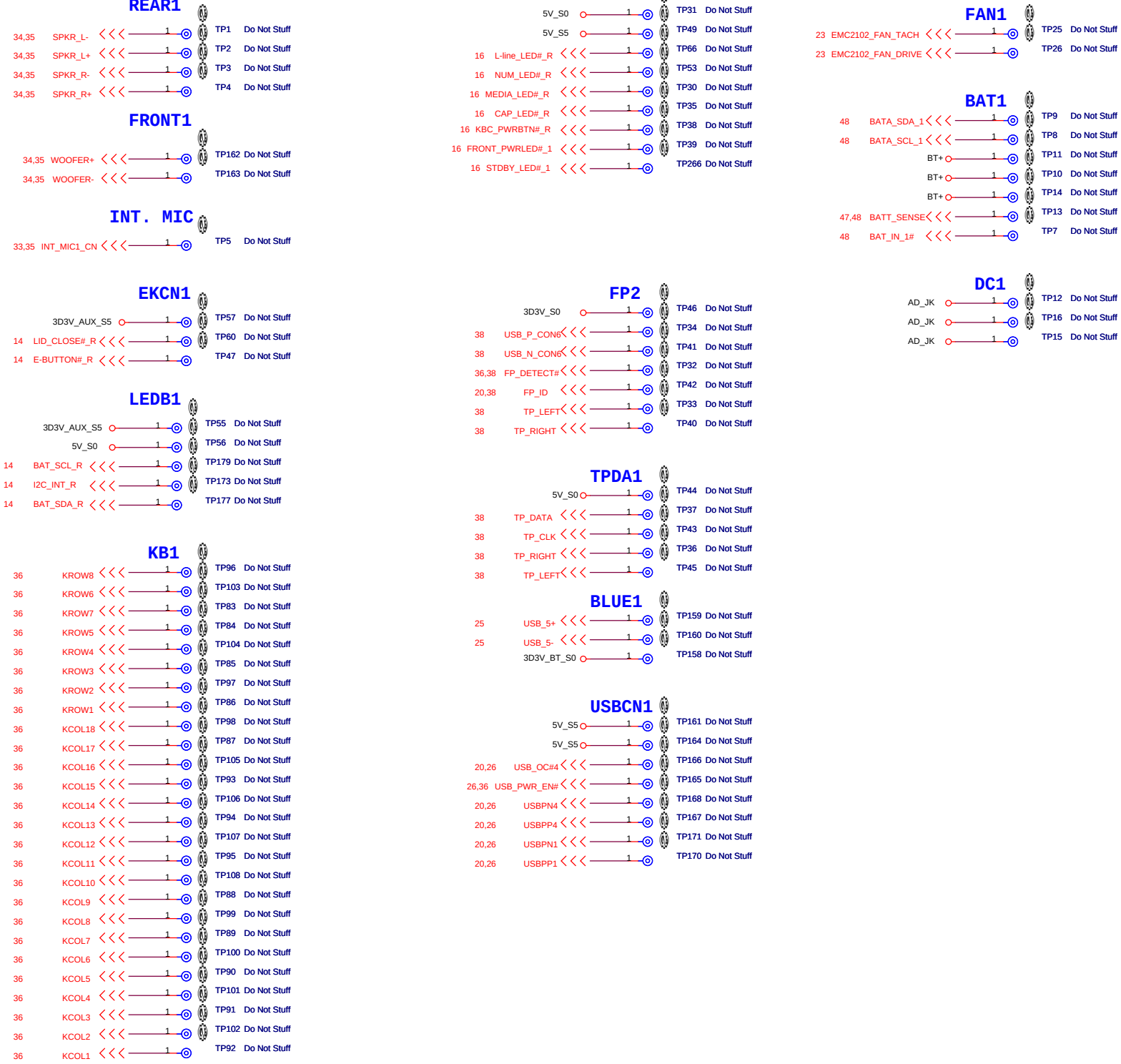

UMA

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Big Bear 2 Schematic EC Tracking Record LAB 0911 , 2008
EC #/ Page / Description / Part Affected

EC SC01/20/Change R316 to 20R2F(For USB eye diagram)

EC SC02/24/Swap net SATA_RXN5 SATA_RXP5

EC SC03/29/Add C679 C680 for XF1(For IEEE common voltage channel D fail)

EC SC04/33/Add RN95 RN104(vendor realtek request)

EC SC05/36/Swap KBI1 pin definition

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