See 'TEXT' in 0MEMO or 1MEMO property in component

Bolsena-E(AB2) Block Diagram

Project Code: 91.4G401.001
REVISION: 05236-SA

Dummy when use '10/100'
Dummy when use 'GIGA'
Dummy when use 'UMA'
Dummy when use 'DIS'
Dummy when use 'SATA'
Dummy when use 'IDE'

PCB Layer Stackup
L1: Signal 1
L2:VCC
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

Power Block Diag -> Page 40

AMD CPU 35W/25W 4,5,6,7
DDR 333/400
200-PIN DDR SODIMM
DDR x2 8,9,10
HyperTransport 6.4GB/S 16b/8b
CLK GEN IDT CV137 3
LEDs 16
RTC BAT. 17
BUTTONs 33
PWR SW CP2211 26
PCMCIA SLOT Support TypeII 26
PCMCIA I/F
ENE CB1410 1* Slot Cardbus 25
ATI RS482M AGTL+ CPU I/F + UMA 11,12,13,14
tv 16
LVDS
LCD 16
PCI Express x16
ATI M52P 49,50,51,52,53
RGB CRT
CRT 15
VRAM x4 54,55
PCI-Express x2
MS/MS Pro/xD/MMC/SD 5 in 1 28
1394 CONN 28
RICOH R5C832 1394 CardReader 27,28
Mini-PCI 802.11a/b/g 29
PCI Bus / 33MHz
ATI SB450
PCI
ACPI 2.0
6xUSB 2.0
AZALIA
LPC I/F
ATA 133 17,18,19,20,21
USB x 4 24
BlueTooth miniUSB 23
CODEC ALC883 32
Line In MIC In 3
Line Out 33
Int. SPKR 33
MODEM MDC Card 23
RJ11 CONN 31
OP AMP G1421 33
RJ45 31
TXFM 31
1000Mb
TXFM 31
10/100Mb
PCI LAN Realtek RTL8110SBL 1000/100/10 RTL8100C 100/10 30
LPC Bus / 33MHz
NS SIO PC87381 37
FIR TFDU6102 37
Thermal & Fan G792 23
KBC KB3910 34
XBUS
Touch Pad 35
Int. KB 35
ISA ROM 36
SATA 24
PIDE
HDD 24
SIDE
DVD/CD-RW 24

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BLOCK DIAGRAM		
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 1 of 58	

PCI Routing

	IDSEL	IRQ	REQ/GNT
MiniPCI	21	F	0
LAN	23	H	2
7411	22	E (CardBus)	1
7411	17	G (1394)	3
7411	17	E (FlashMedia)	3


```
Ref.  function    schematic         BOM
-------------------------
U81  cpu socket    62.10055.121  (DON'T CHANGE)  (3mm high)
U80  north bridge  71.RS482.M03  71.RS482.M03  (ver A12)
U43  south bridge  71.SB400.B0U  71.SB400.D0U  (ver A13)
U32  clock gen.    71.00137.C0W  71.00137.C0W

---
U70  VGA M52     71.0M52P.A0U
U64  VRAM FOR M52
U65  VRAM FOR M52
U69  VRAM FOR M52
U71  VRAM FOR M52




---
U66  BIOS SOCKET  72.39040.G03  62.10002.032   (NO NEED WHEN PD)
U66  BIOS IC      72.39040.G03  72.39040.H03  (DIP STAGE IN LAB, SMT IN PD)
---
U75 GIGA LAN    71.08110.00G 71.08110.A0G
U75 10/100 LAN  71.08110.00G 71.08100.C0G
```

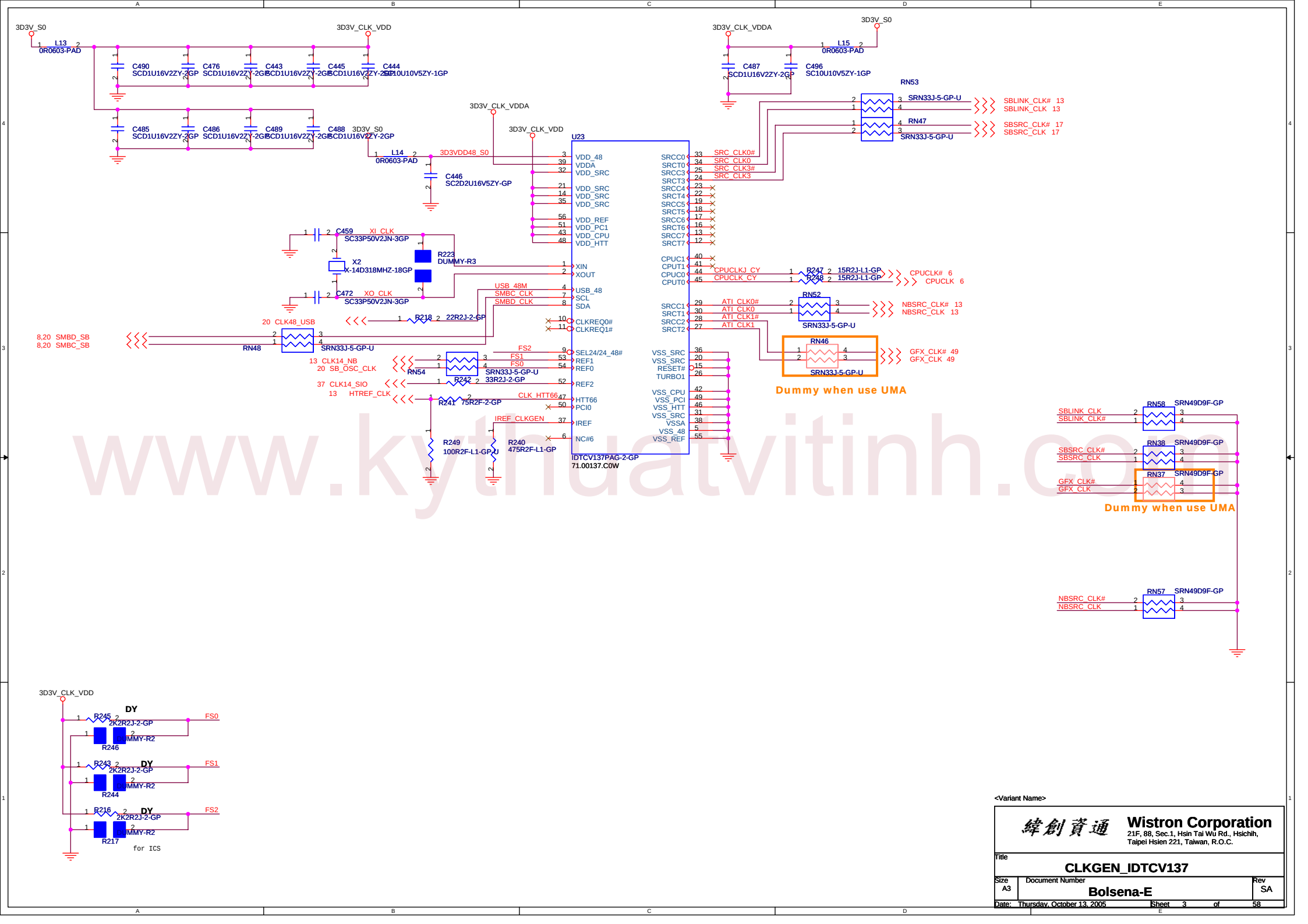
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HISTORY

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 2 of 58



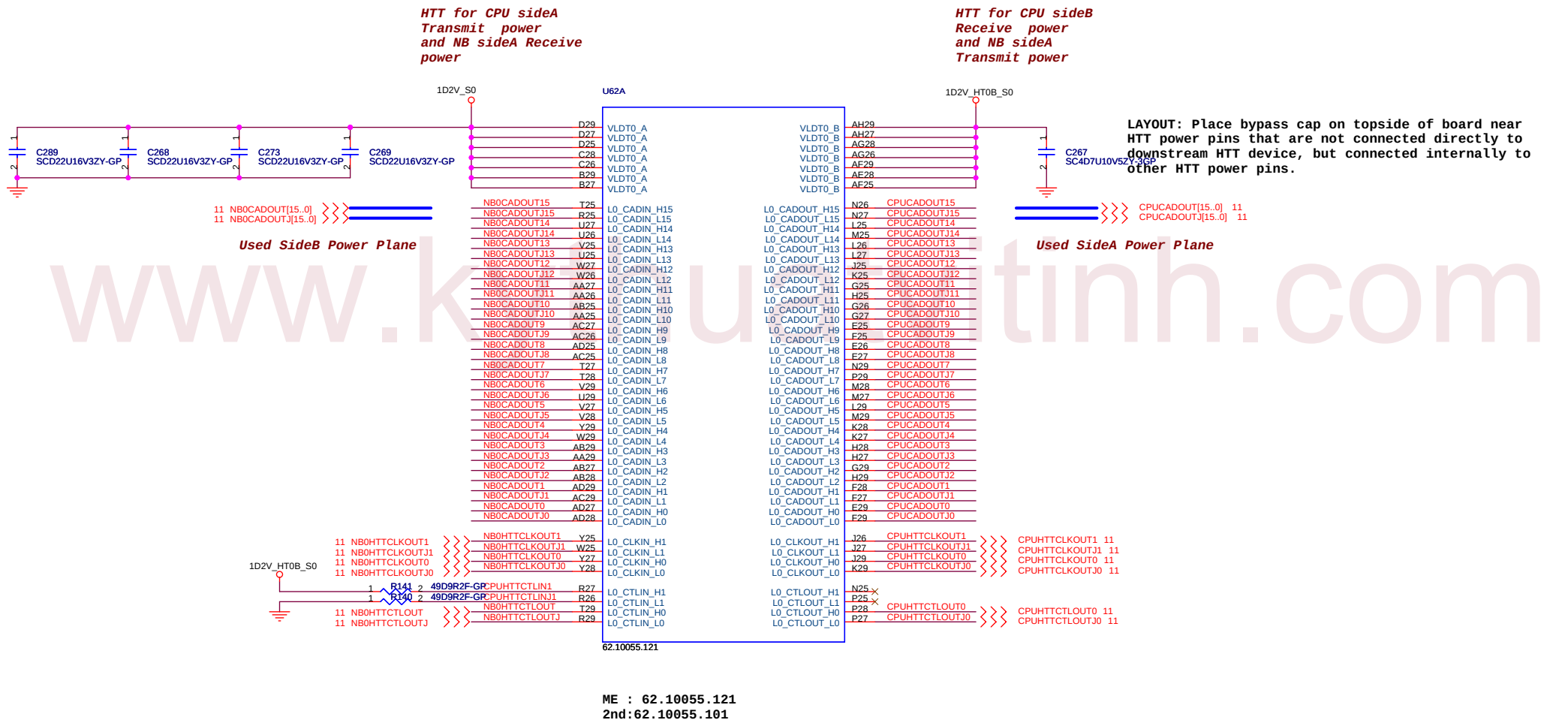
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_IDTCV137

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 3 of 58



ME : 62.10055.121
2nd:62.10055.101

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(1/4)_HyperTransport I/F**

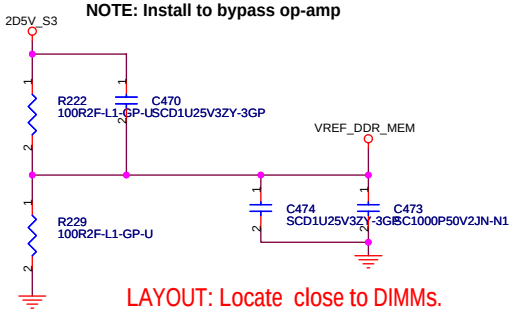
Size: A3 | Document Number: **Bolsena-E** | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 4 of 58

VREF_DDR_MEM

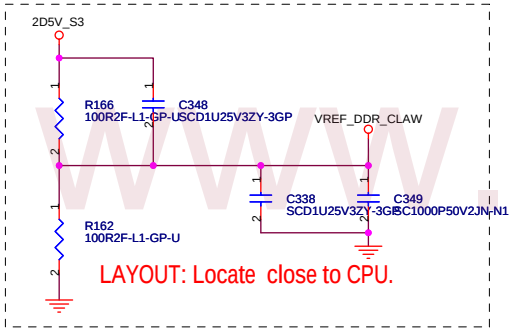
NOTE: Test with passive probes only.

NOTE: Install to bypass op-amp

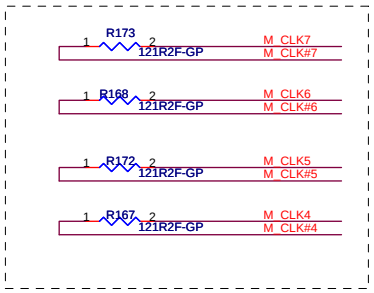


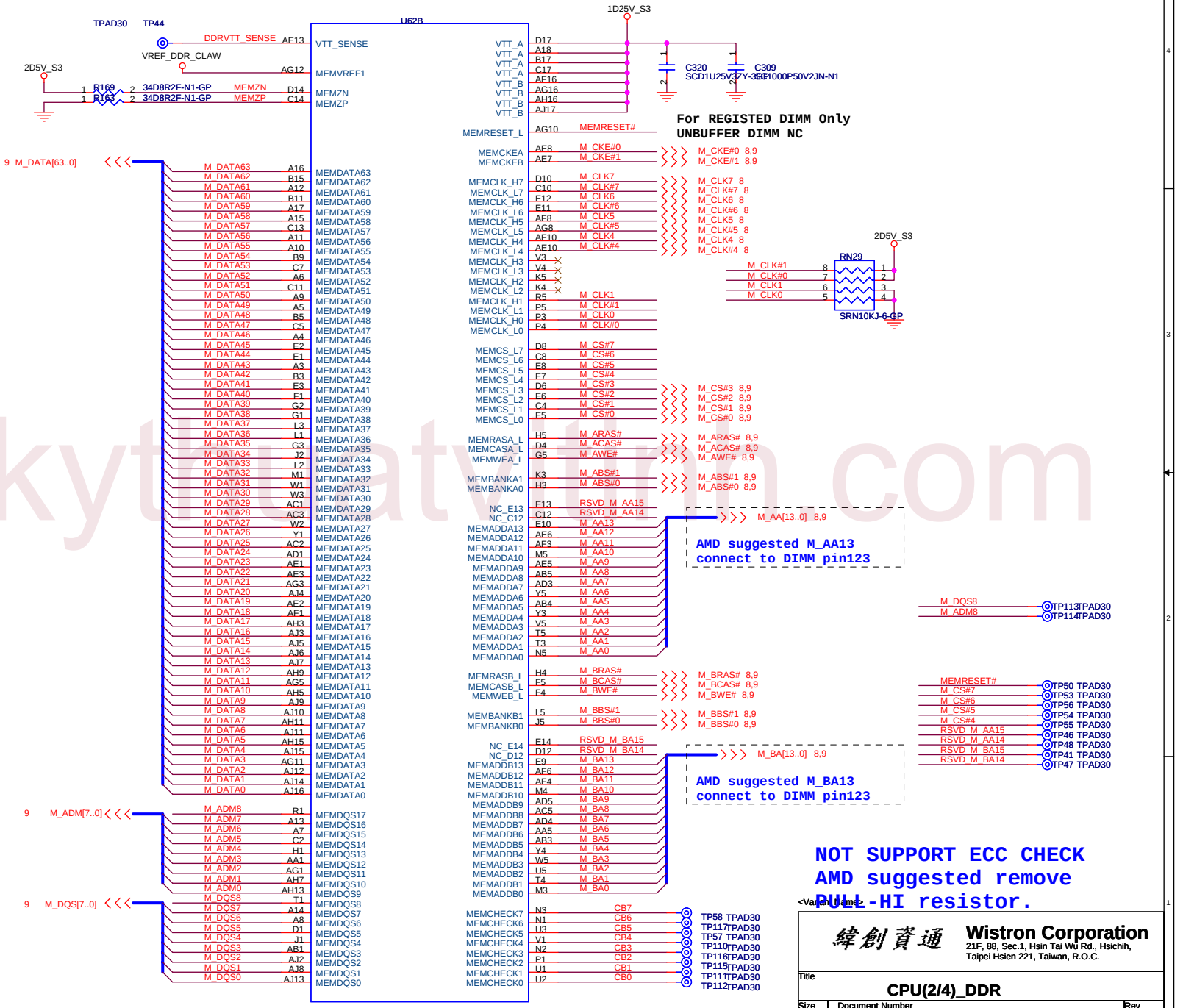
NOTE: Remove to bypass op-amp

VREF_DDR_CLAW



Place it near CPU





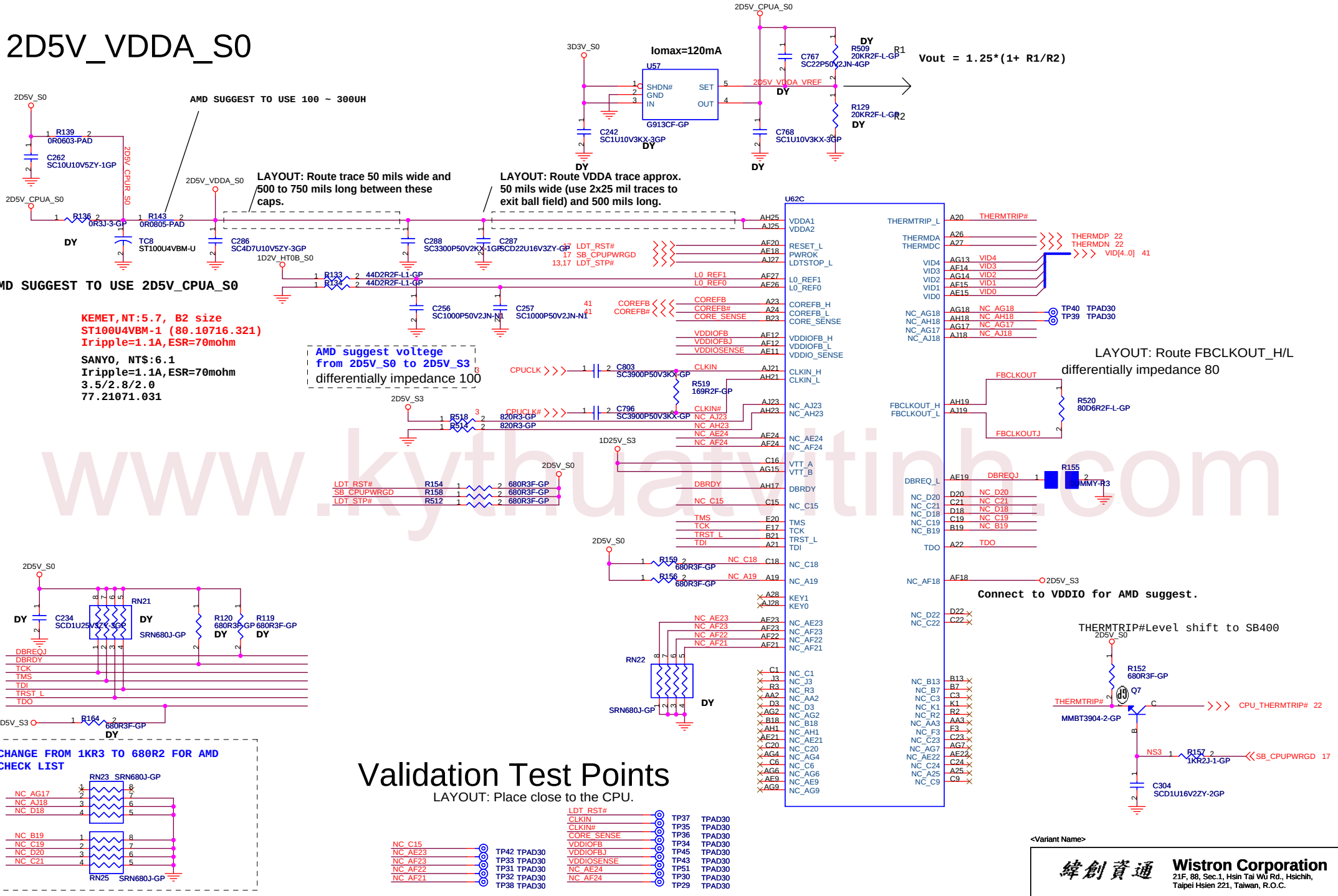
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(2/4)_DDR

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 5 of 58

2D5V_VDDA_S0



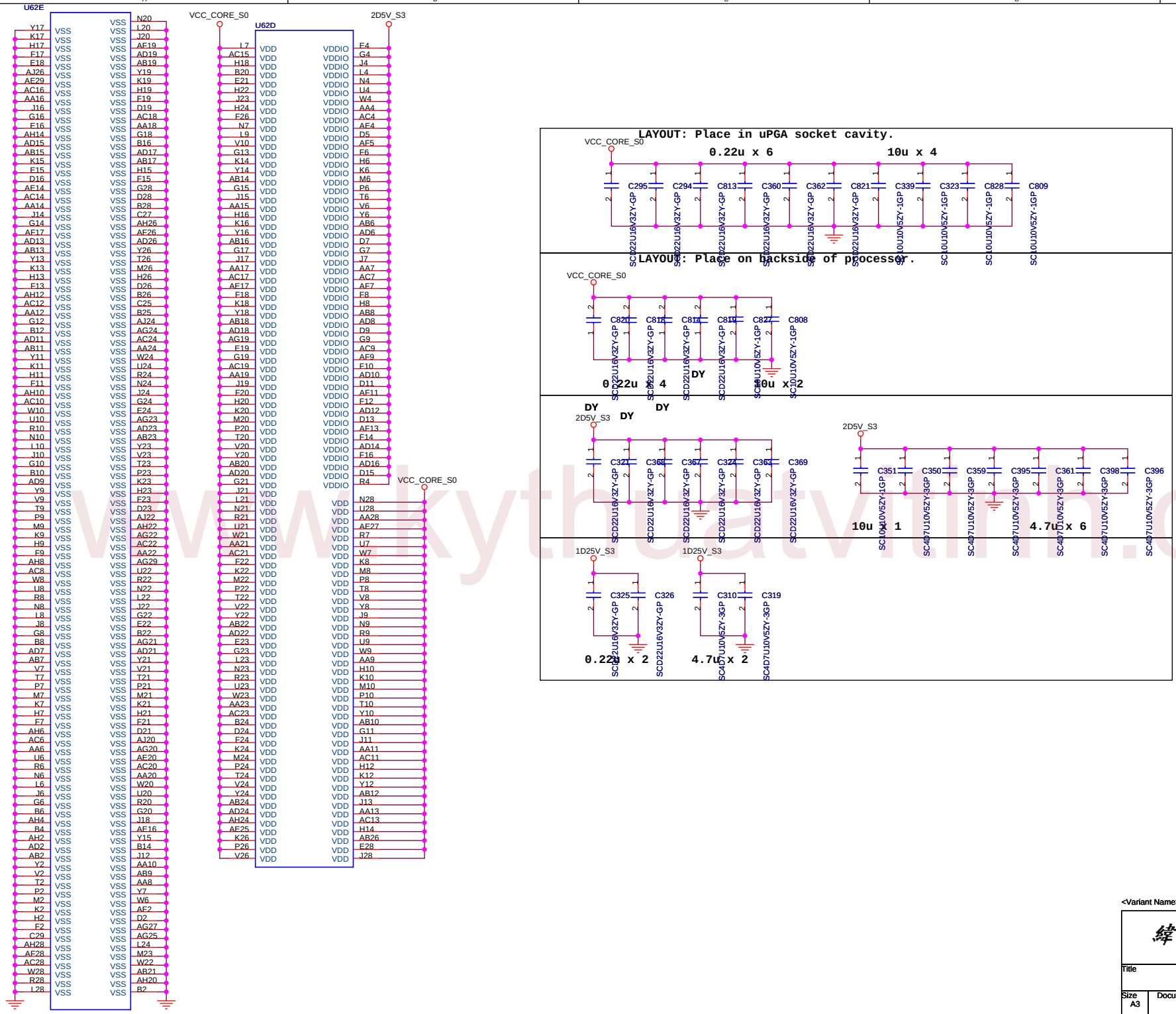
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(3/4)_Control & Debug

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 6 of 58



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(4/4)_Power

Size	Document Number	Rev
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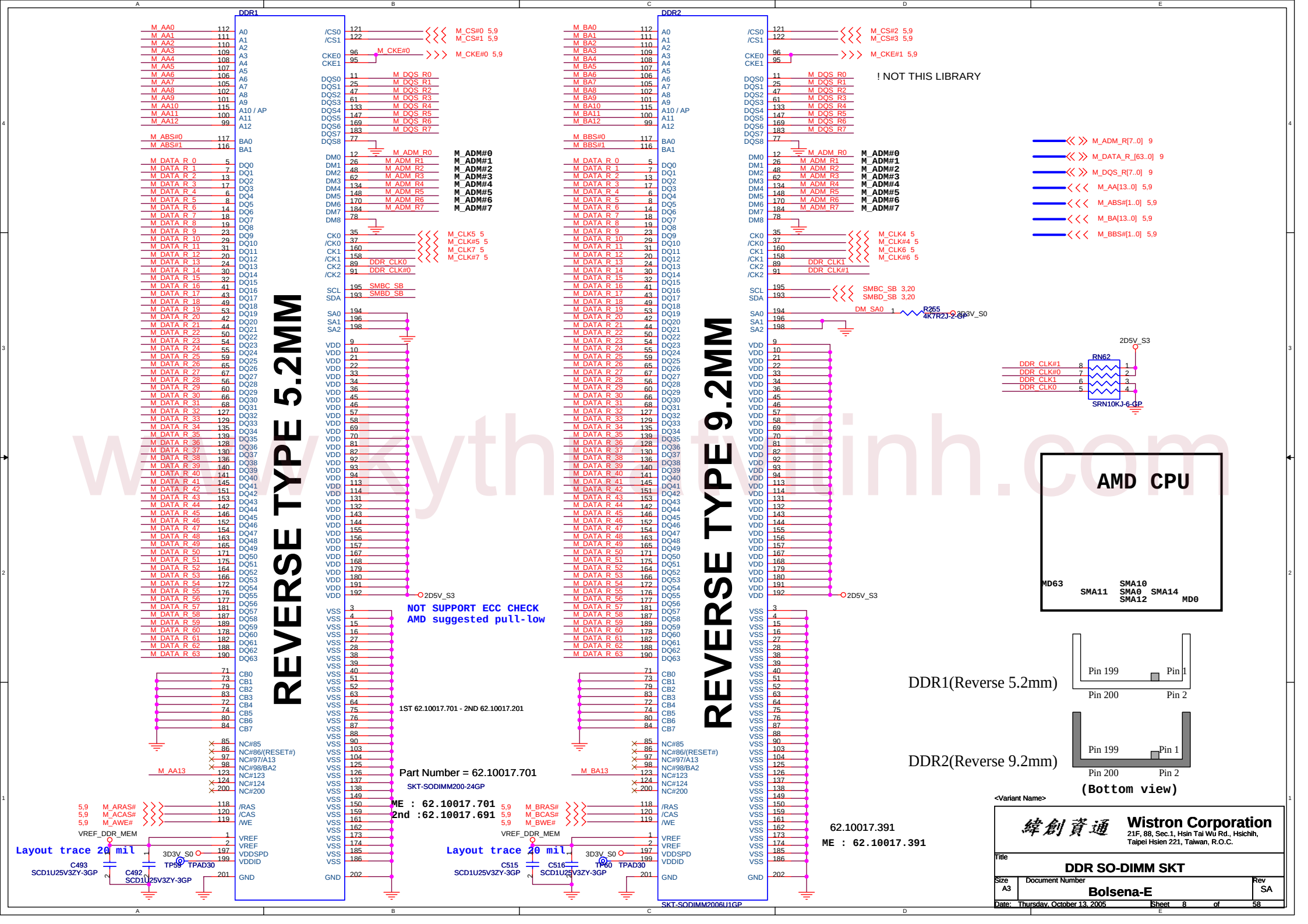
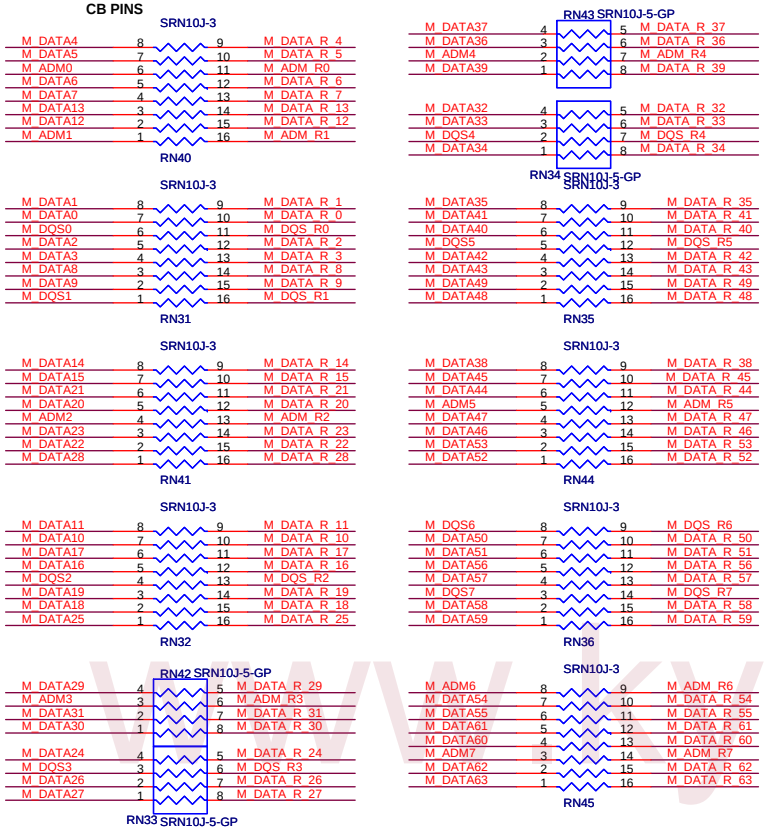

DDR1
REVERSE TYPE 5.2MM
DDR2
REVERSE TYPE 9.2MM
! NOT THIS LIBRARY
NOT SUPPORT ECC CHECK
AMD suggested pull-low
1ST 62.10017.701 - 2ND 62.10017.201
Part Number = 62.10017.701
SKT-SODIMM200-24GP
ME : 62.10017.701
2nd :62.10017.691
62.10017.391
ME : 62.10017.391
SKT-SODIMM2006U1GP
Layout trace 20 mil
AMD CPU
MD63
SMA10
SMA11
SMA0
SMA14
SMA12
MD0
RN62
SRN10KJ-6-GP
DDR1(Reverse 5.2mm)
DDR2(Reverse 9.2mm)
Pin 199
Pin 1
Pin 200
Pin 2
(Bottom view)
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR SO-DIMM SKT
Size
A3
Document Number
Bolsena-E
Rev
SA
Date: Thursday, October 13, 2005
Sheet 8 of 58

SERIES DAMPING

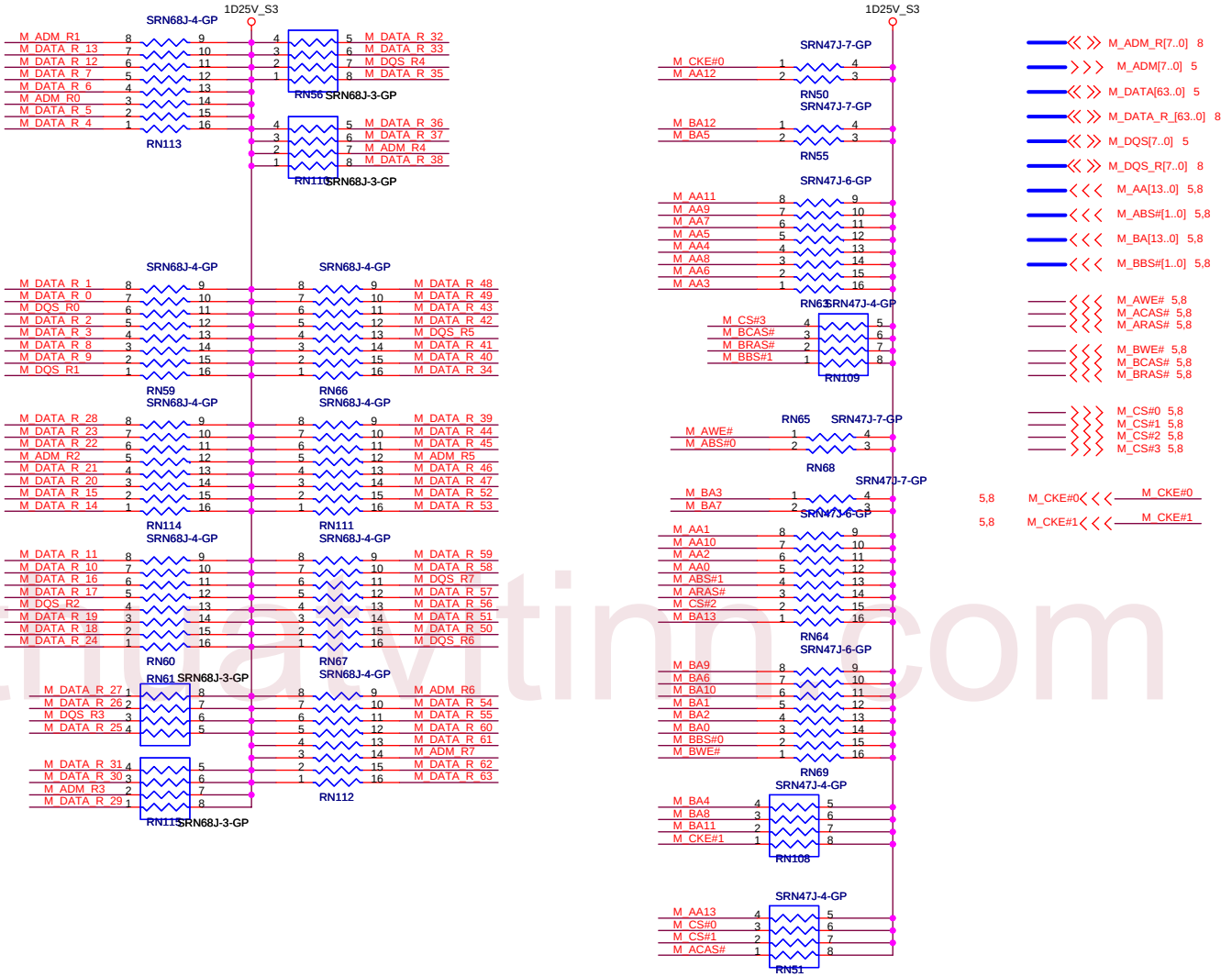
PLACE RNs CLOSE TO FIRST DIMM, < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS



05/10
Remove the damping resistor for AMD suggest.

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR DAMPING & TERMINATION**

Size	Document Number	Rev
A3	Bolsena-E	SA

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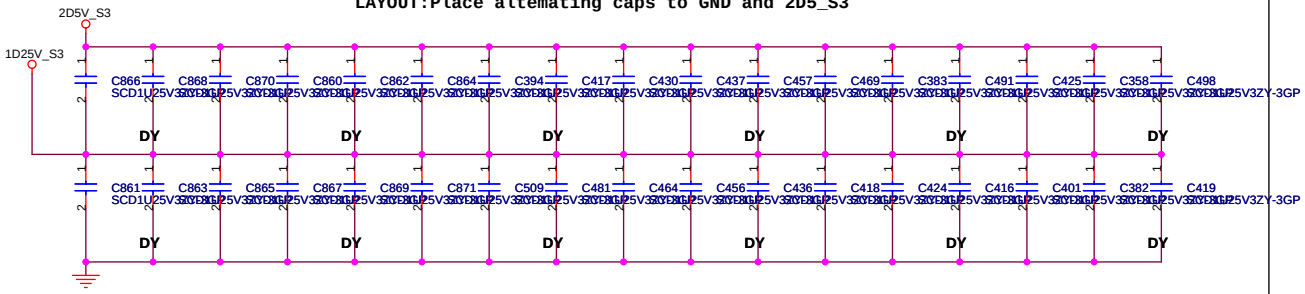
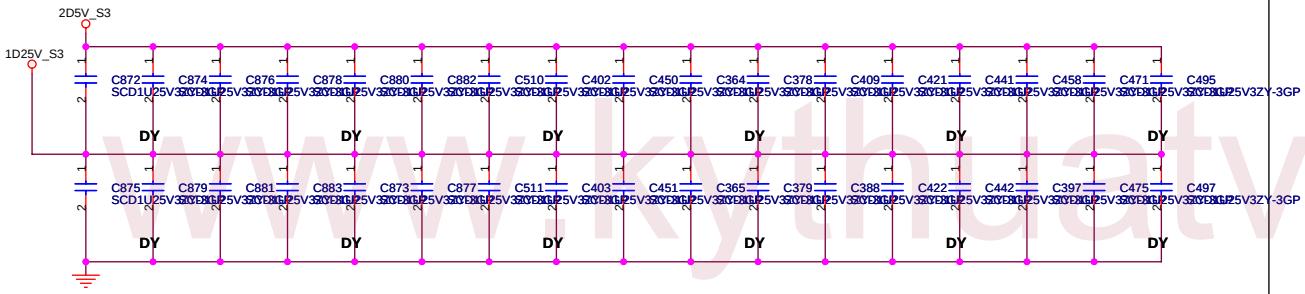
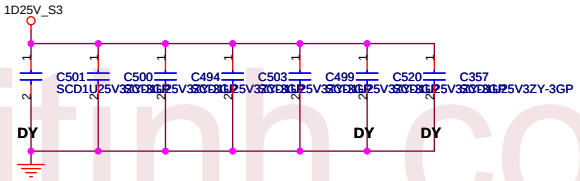
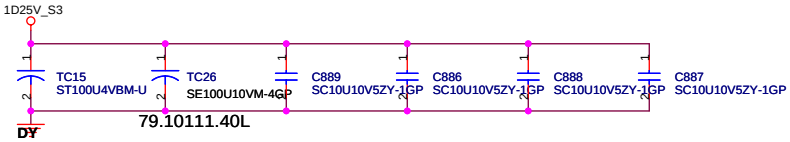
LAYOUT:Place altemating caps to GND and 2D5_S3



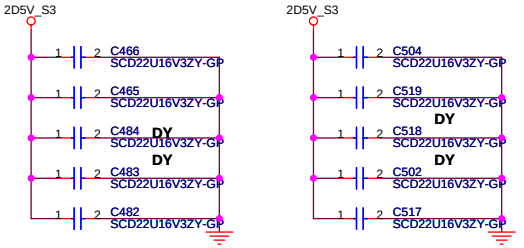




LAYOUT:Place at end of the DIMMs



LAYOUT:Place close to Power Pin of DDR socket.



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR DECOUPLING

Size: A3 | Document Number: Bolsena-E | Rev: SA

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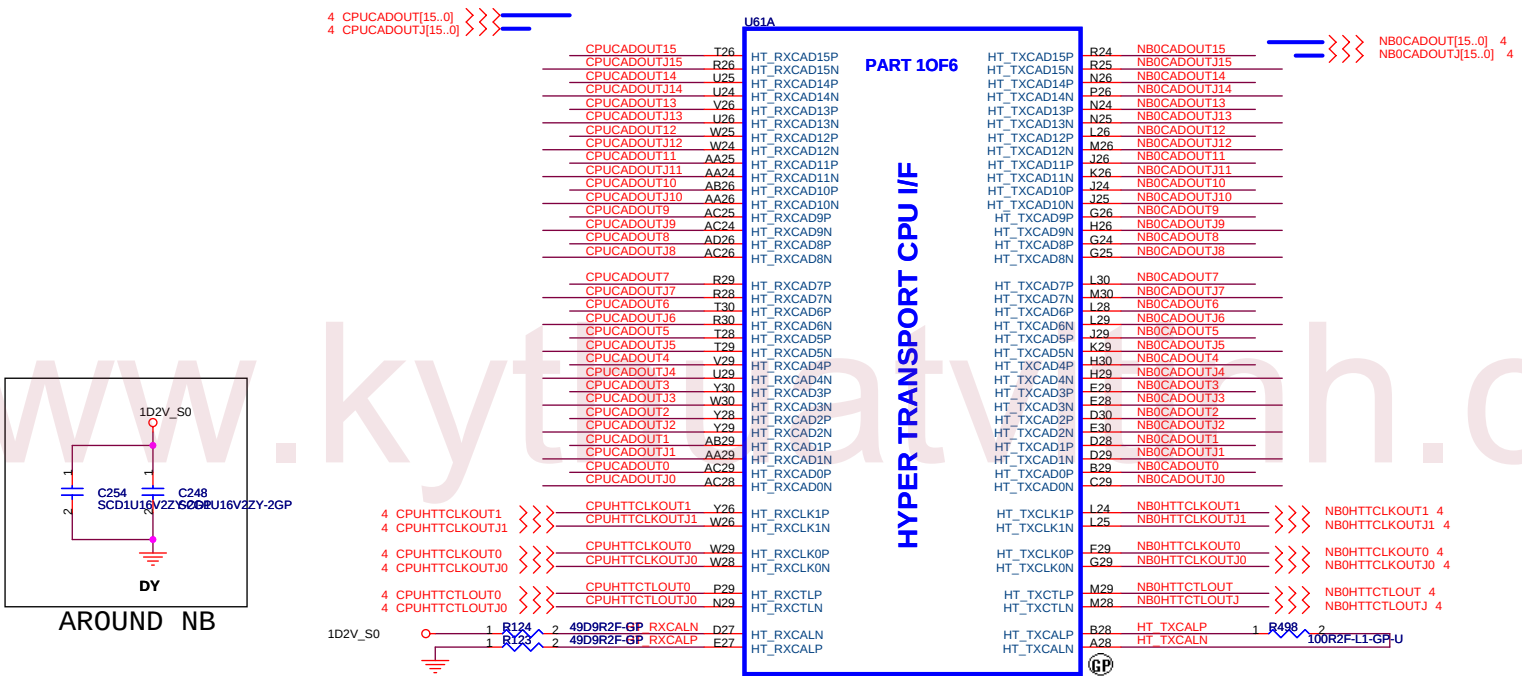
CLAW HAMMER TO NB

NB TO CLAW HAMMER



AROUND NB

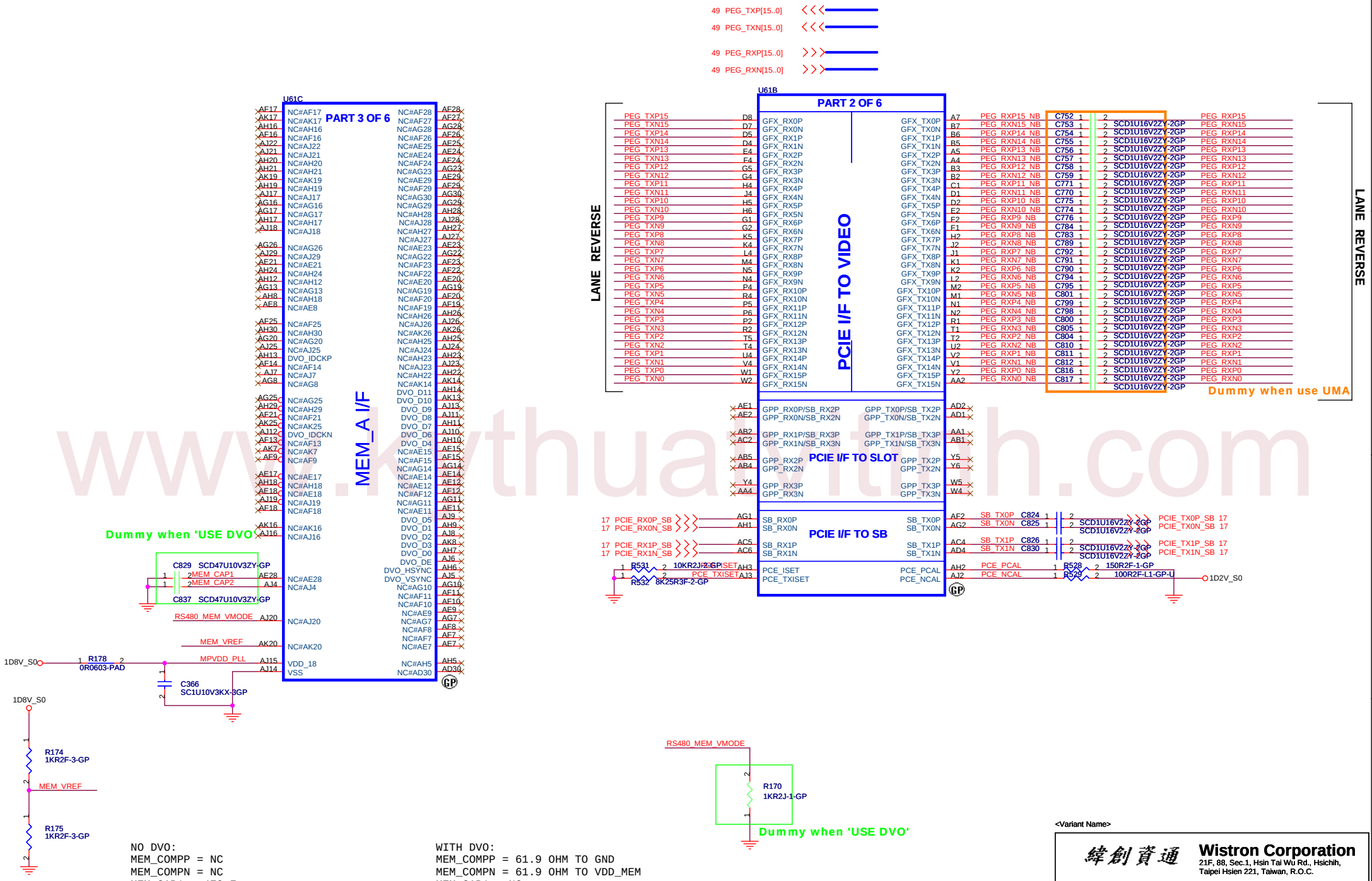
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-RS482M (1 of 4) HT

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 11 of 58



NO DVO:
MEM_COMPP = NC
MEM_COMPN = NC
MEM_CAP1 = 470nF
MEM_CAP2 = 470nF
MEM_VMODE = GND (IF VDD_MEM = 2.5V)
MEM_VREF = VDD_MEM / 2

WITH DVO:
MEM_COMPP = 61.9 OHM TO GND
MEM_COMPN = 61.9 OHM TO VDD_MEM
MEM_CAP1 = NC
MEM_CAP2 = NC
MEM_VMODE = 1.8V(IF VDD_MEM = 1.8V)
MEM_VREF = VDD_MEM / 2

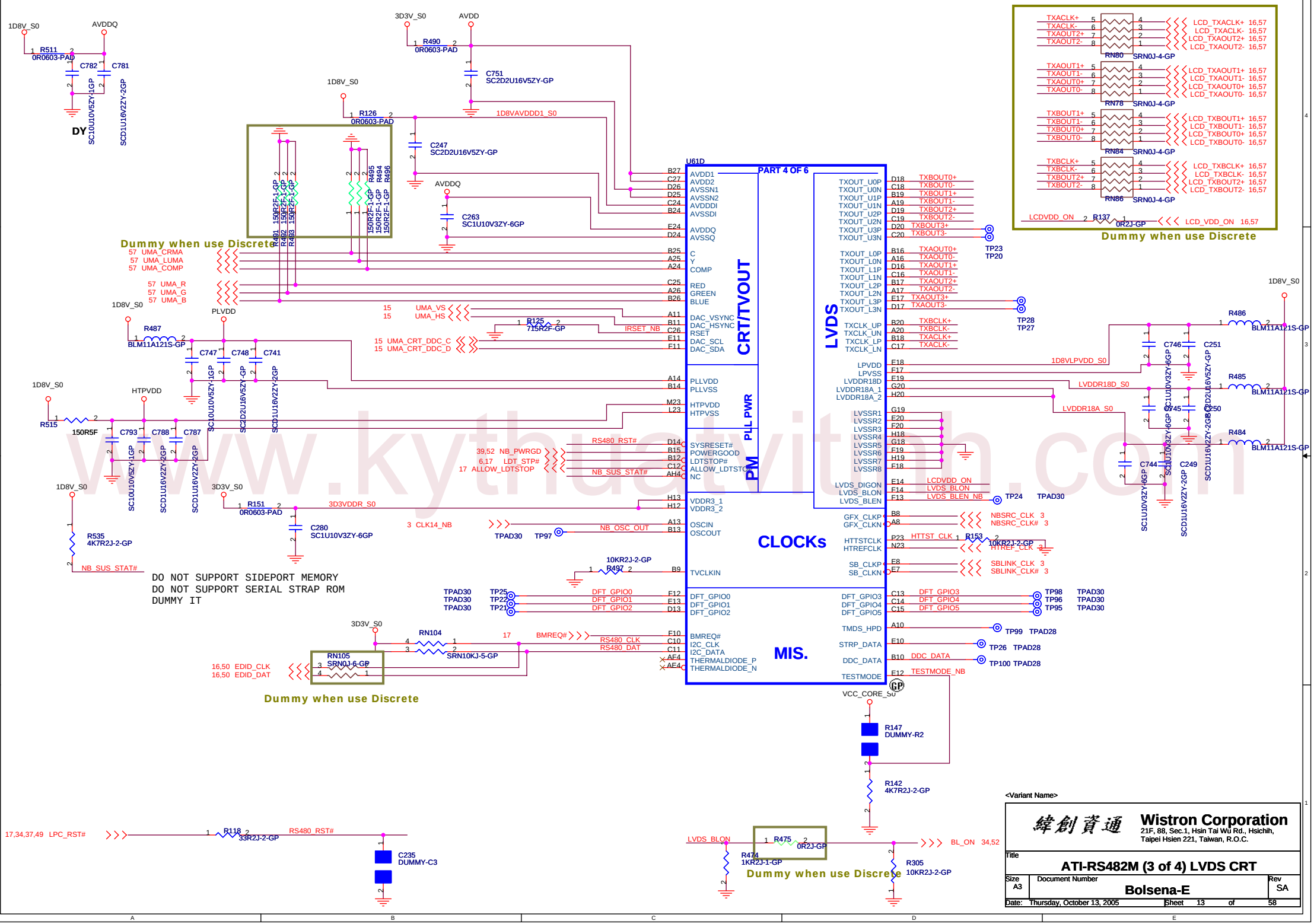
<Variant Name>

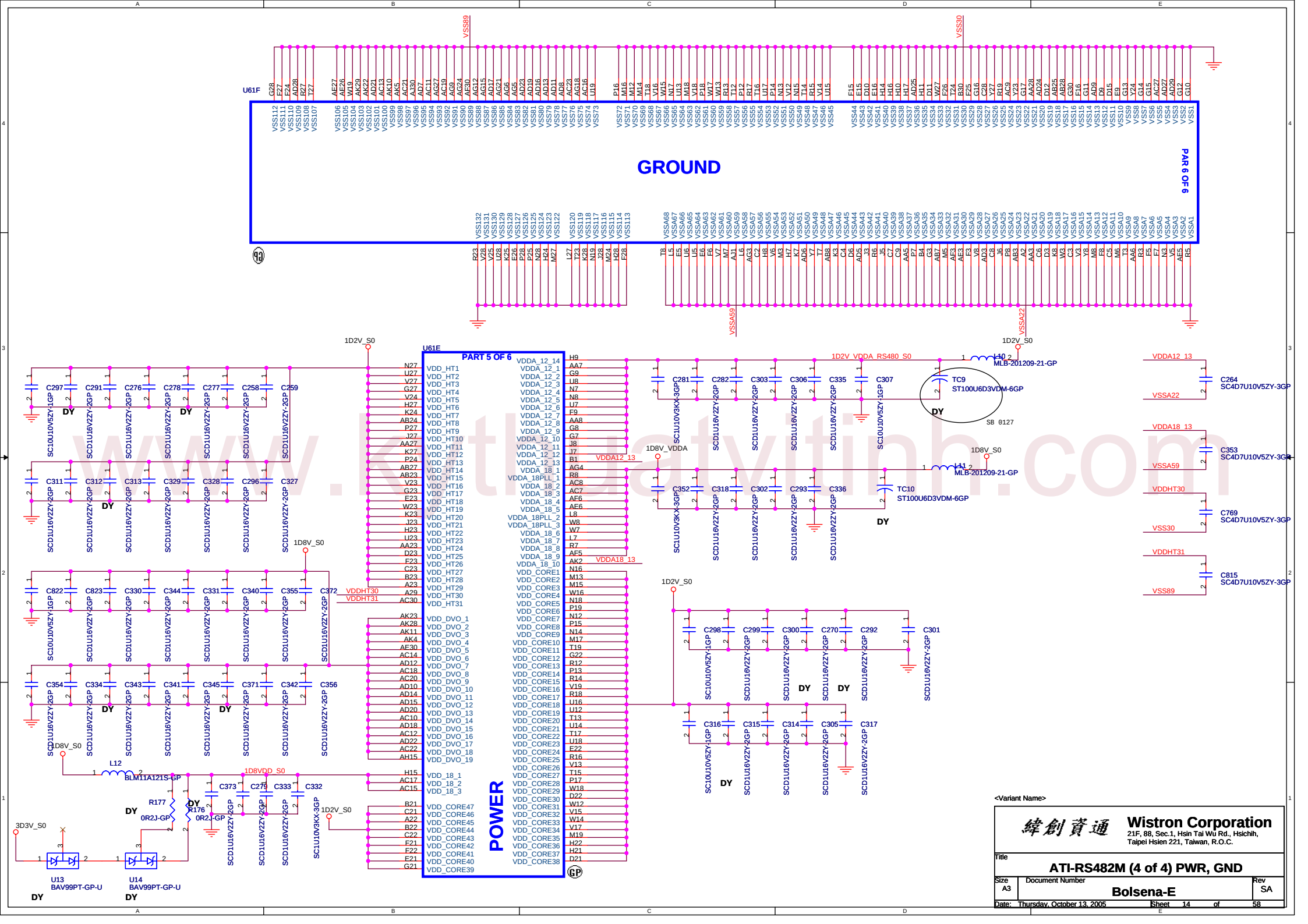
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-RS482M (2 of 4) PCIE

Size	Document Number	Rev
A3	Bolsena-E	SA

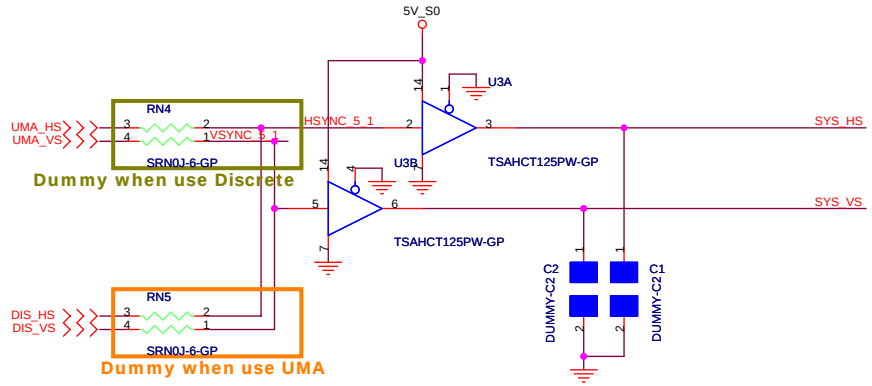
Date: Thursday, October 13, 2005 Sheet 12 of 58

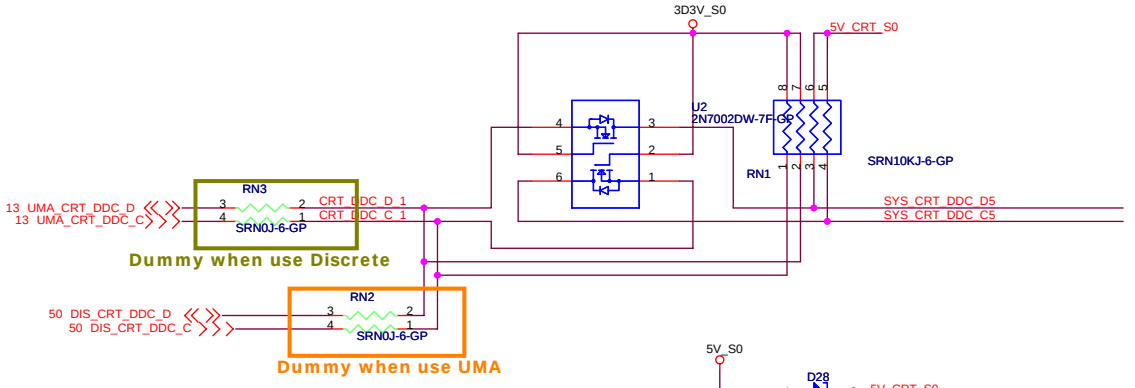


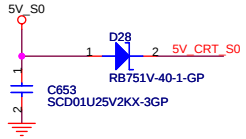

GROUND
PAR 6 OF 6
PART 5 OF 6
POWER
U61F
U61E
1D2V_S0
1D8V_S0
1D8V_VDDA
1D2V_VDDA_RS480_S0
1D8VDD_S0
3D3V_S0
VDDA12_13
VDDA18_13
VDDHT30
VDDHT31
DY
TC9 ST100U6D3VDM-6GP
TC10 ST100U6D3VDM-6GP
L10 MLB-201209-21-GP
L11 MLB-201209-21-GP
L12 BLM11A121S-GP
U13 BAV99PT-GP-U
U14 BAV99PT-GP-U
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-RS482M (4 of 4) PWR, GND
Size A3
Document Number
Bolsena-E
Rev SA
Date: Thursday, October 13, 2005
Sheet 14 of 58

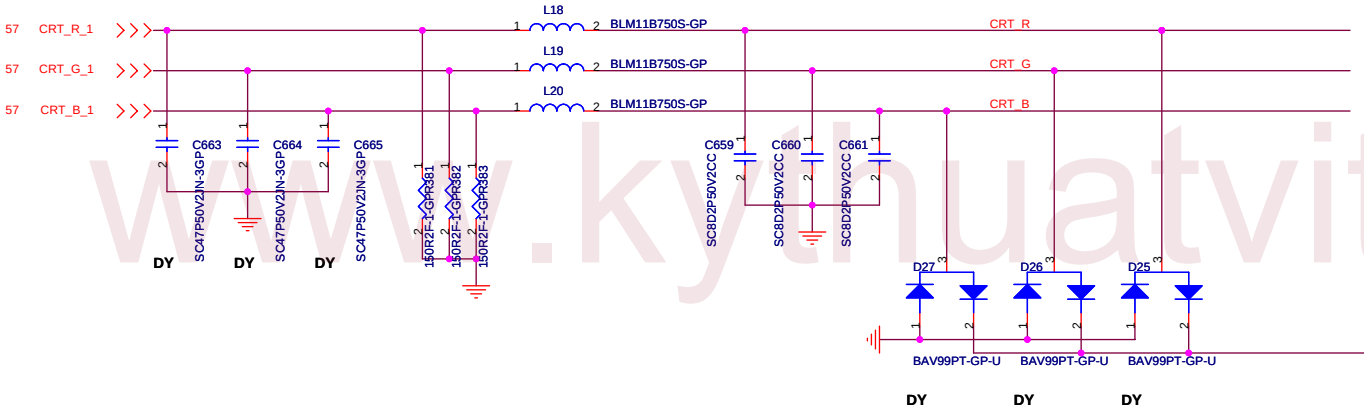
CRT CONN

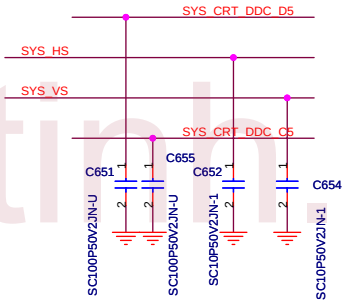
200mA Rating/Spec 500mA

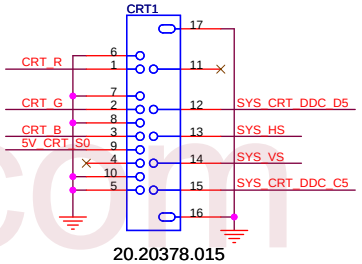


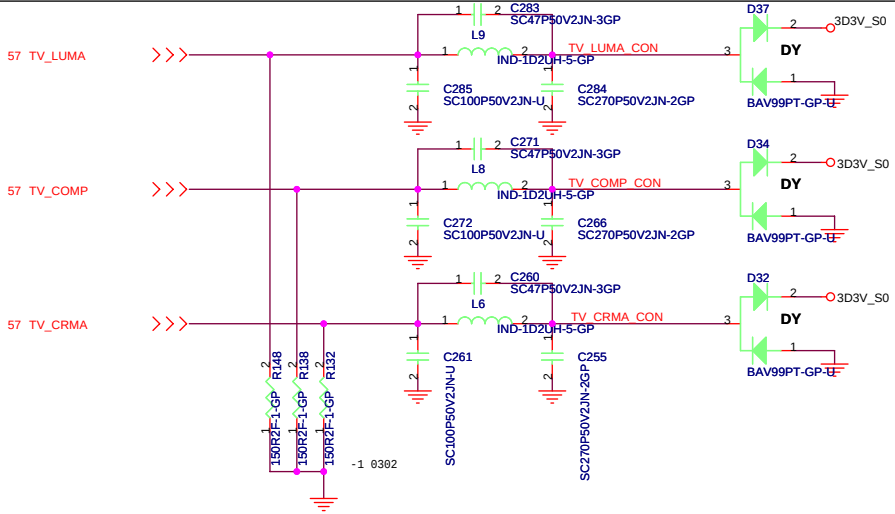


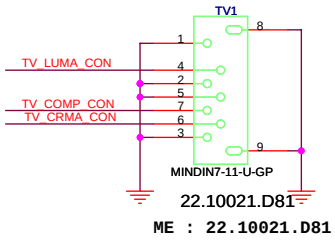




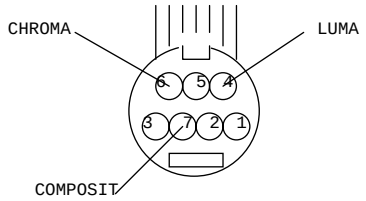








TV CONN



<Variant Name>

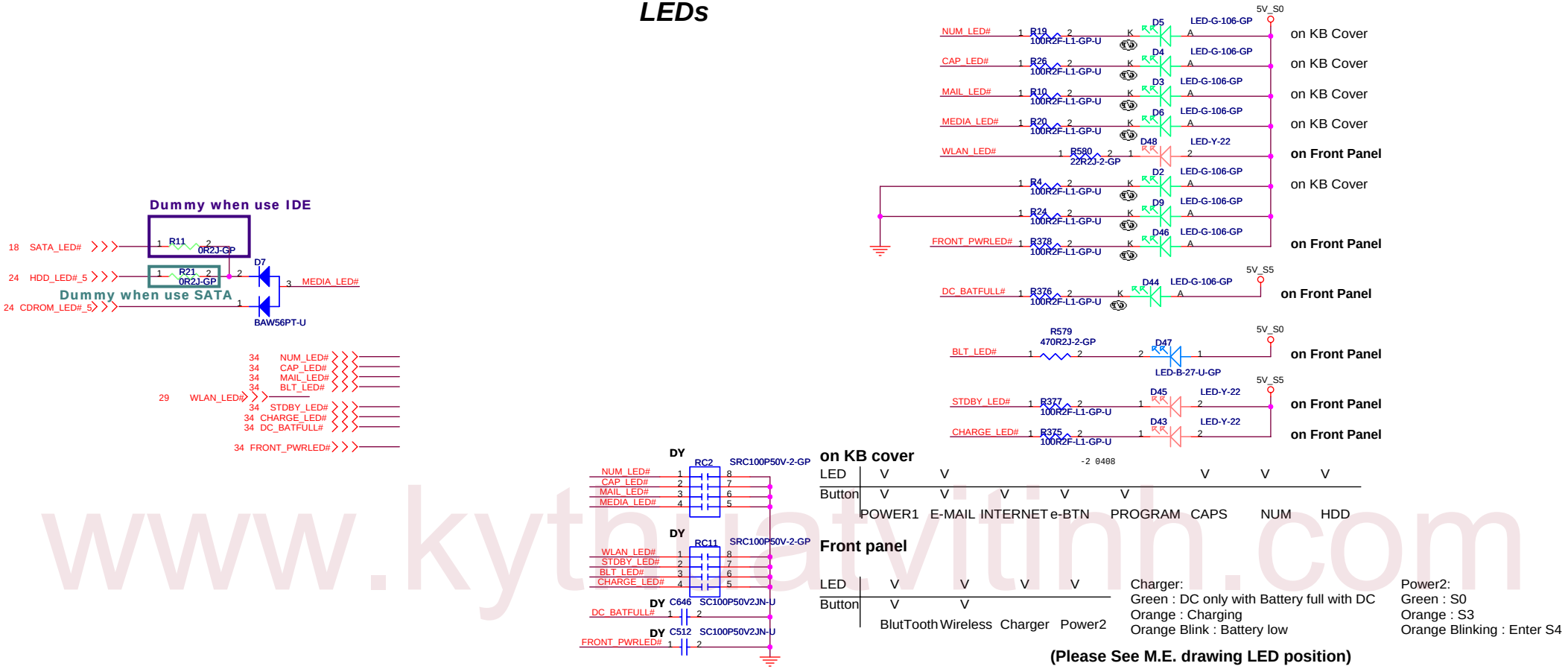
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT/TV**

Size	Document Number	Rev
A3	**Bolsena-E**	SA

Date: Thursday, October 13, 2005 Sheet 15 of 58

LEDs



on KB cover

LED	V	V				V	V	V
Button	V	V	V	V	V			
	POWER1	E-MAIL	INTERNET	e-BTN	PROGRAM	CAPS	NUM	HDD

Front panel

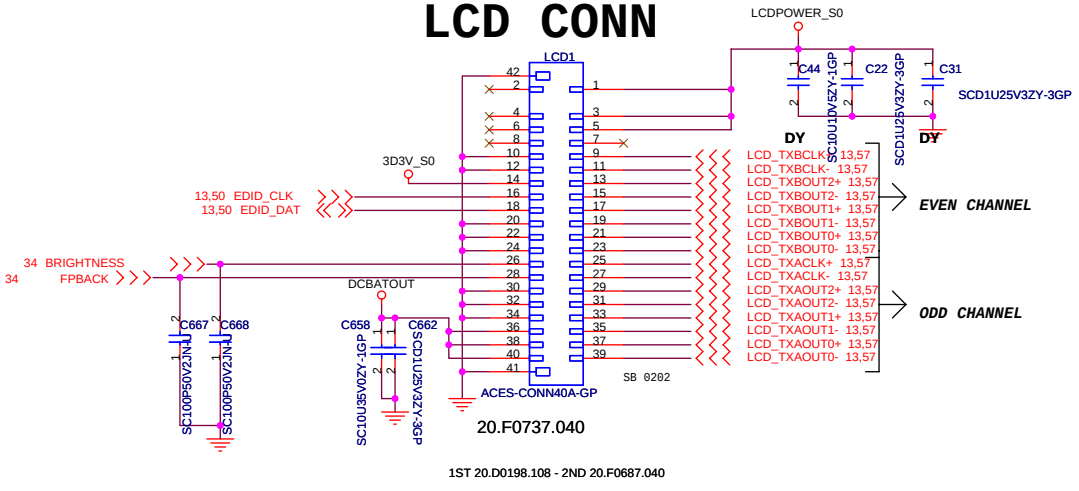
LED	V	V	V	V
Button	V	V		
	BlutTooth	Wireless	Charger	Power2

Charger:
Green : DC only with Battery full with DC
Orange : Charging
Orange Blink : Battery low

Power2:
Green : S0
Orange : S3
Orange Blinking : Enter S4

(Please See M.E. drawing LED position)

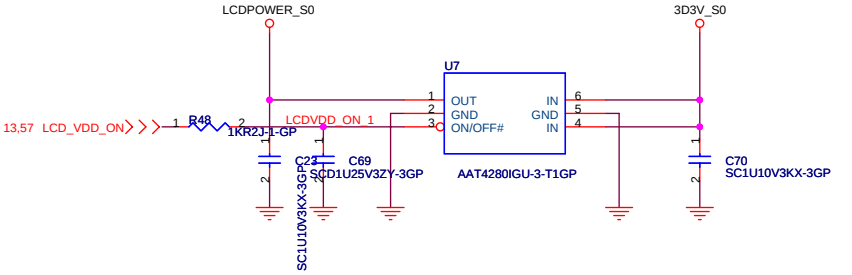
LCD CONN



1ST 20.D0198.108 - 2ND 20.F0687.040

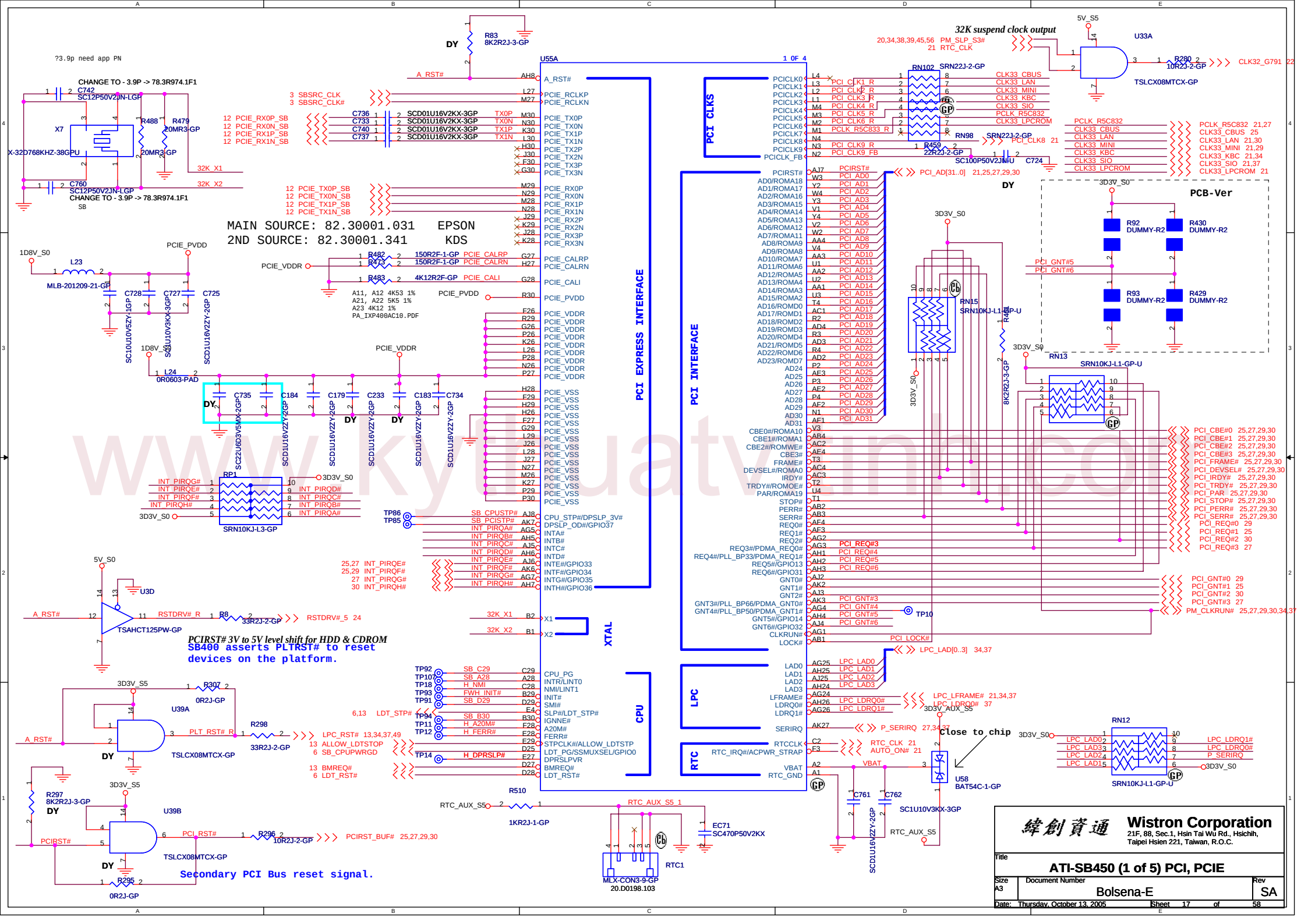
LCD POWER

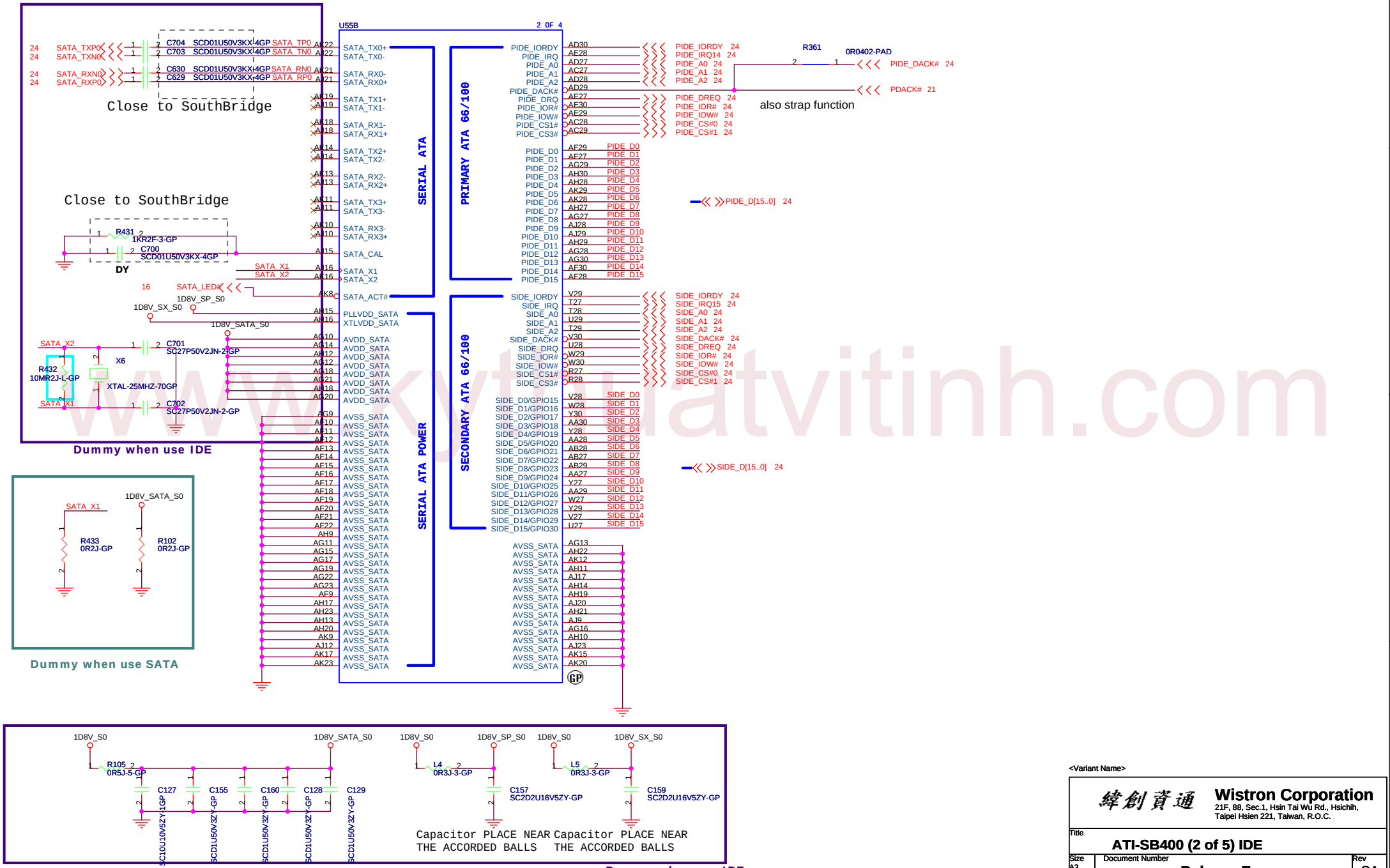
Layout 40 mil



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LCD / LEDs**	
Size A3	Document Number **Bolsena-E**	Rev SA
Date: Thursday, October 13, 2005	Sheet 16 of 58	


MAIN SOURCE: 82.30001.031 EPSON
2ND SOURCE: 82.30001.341 KDS
U55A
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
CPU
LPC
RTC
32K suspend clock output
PCIRST# 3V to 5V level shift for HDD & CDROM
SB400 asserts PLTRST# to reset devices on the platform.
Secondary PCI Bus reset signal.
Close to chip
PCB-Ver
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATI-SB450 (1 of 5) PCI, PCIE
Bolsena-E
SA
Date: Thursday, October 13, 2005
Sheet 17 of 58



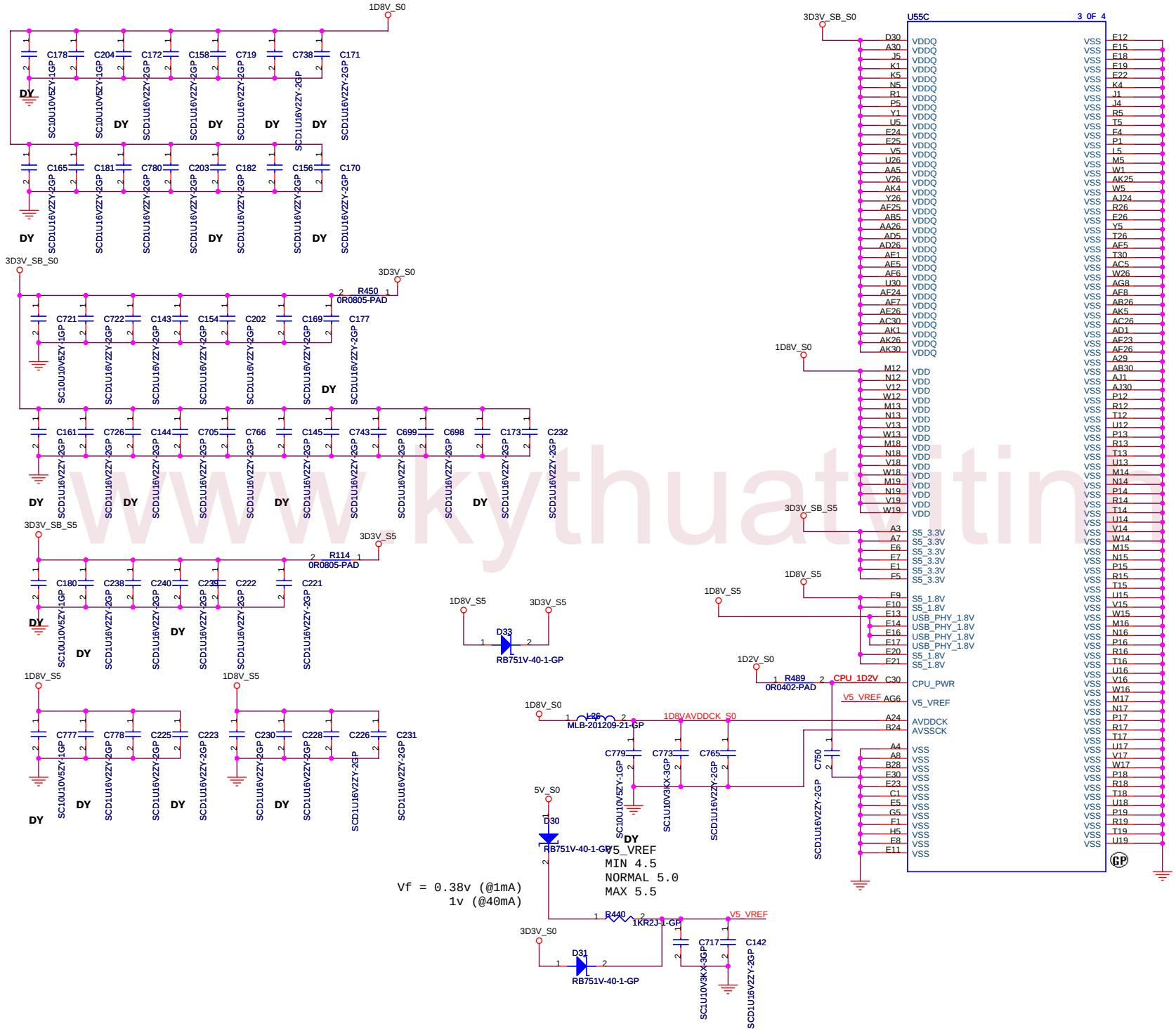
<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 (2 of 5) IDE

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 18 of 58



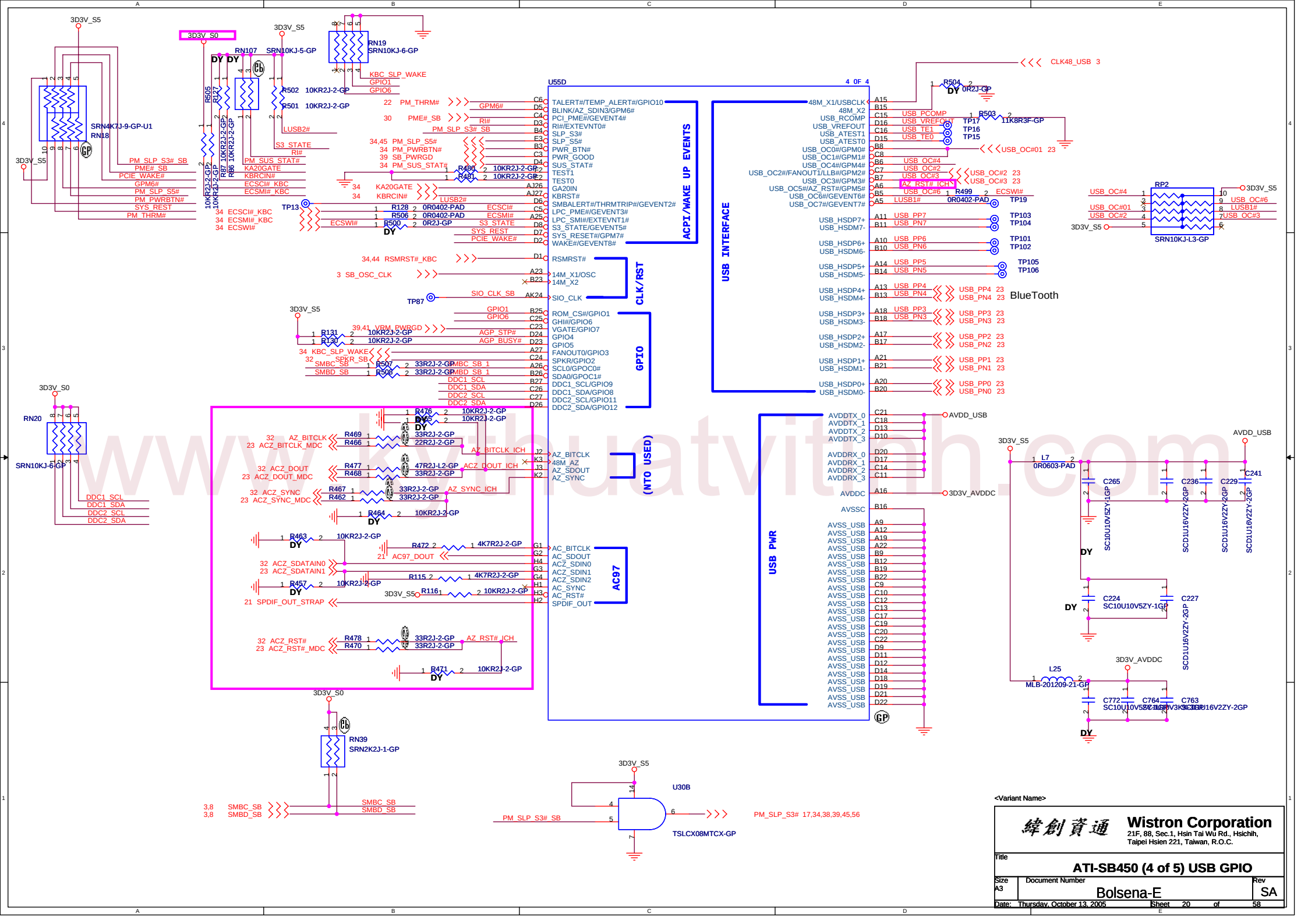
<Variant Name>

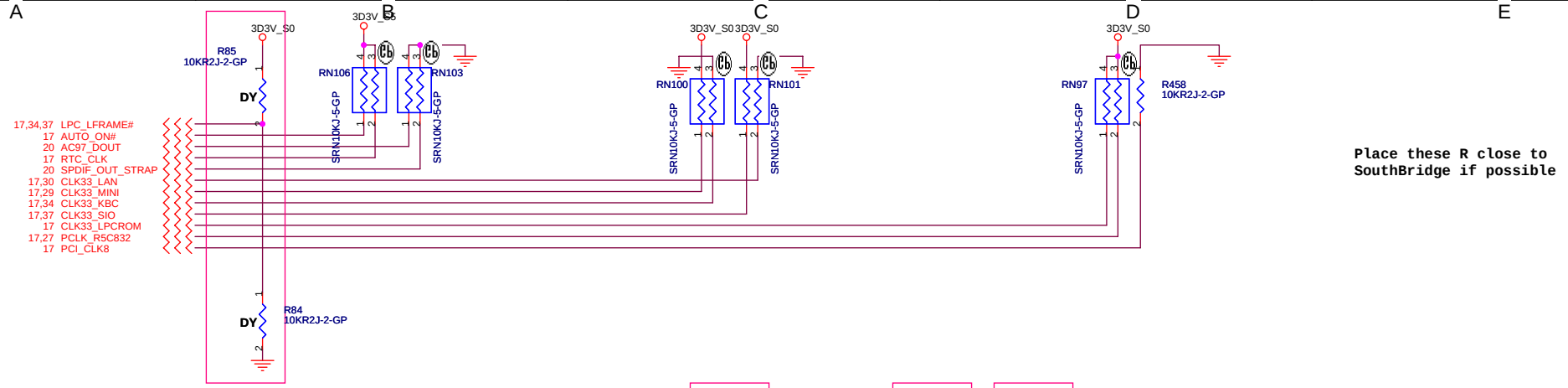
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 (3 of 5) POWER

Size: A3 | Document Number: Bolsena-E | Rev: SA

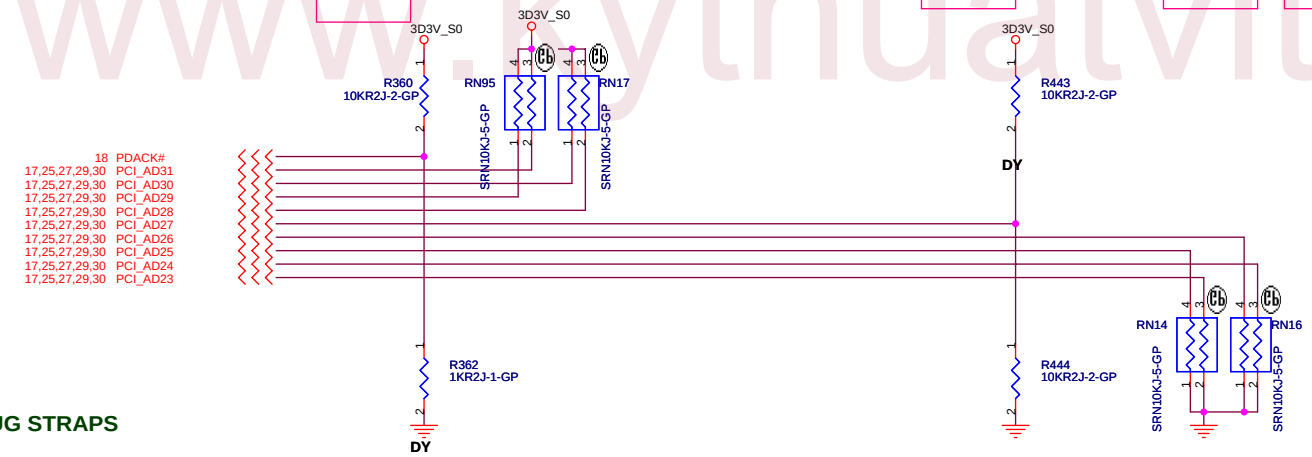
Date: Thursday, October 13, 2005 | Sheet 19 of 58


U55D
4 OF 4
ACPI/WAKE UP EVENTS
CLK/RST
GPIO
(NTO USED)
AC97
USB INTERFACE
USB PWR
BlueTooth
U30B
TSLCX08MTCX-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
Title
ATI-SB450 (4 of 5) USB GPIO
Size A3
Document Number
Bolsena-E
Rev SA
Date: Thursday, October 13, 2005
Sheet 20 of 58



REQUIRED SYSTEM STRAPS

	LFRAME#	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2 (CLK33_LAN)	PCI_CLK3 (CLK33_MINI)	PCI_CLK4 (CLK33_KBC)	PCI_CLK5 (CLK33_SIO)	PCI_CLK6 (CLK33_LPCROM)	PCI_CLK7 (PCLK_R5C832) PCI_CLK8
STRAP HIGH	Thermal Trip is not enable as default Optional	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHZ -Crytsal Pad	USB PHY PWRDOWN DISABLE DEFAULT	USB INT PLL48	PCIE_CM_SET HIGH DEFAULT	CPU I/F=K8 DEFAULT	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I
STRAP LOW	Thermal Trip is enable as default Optional	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTENNAL RTC (NOT SUPPORTED W/IT8712) DEFAULT	SIO 48MHz	48MHZ-Clock Input Buffer DEFAULT	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ Use External only	PCIE_CM_SET LOW	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

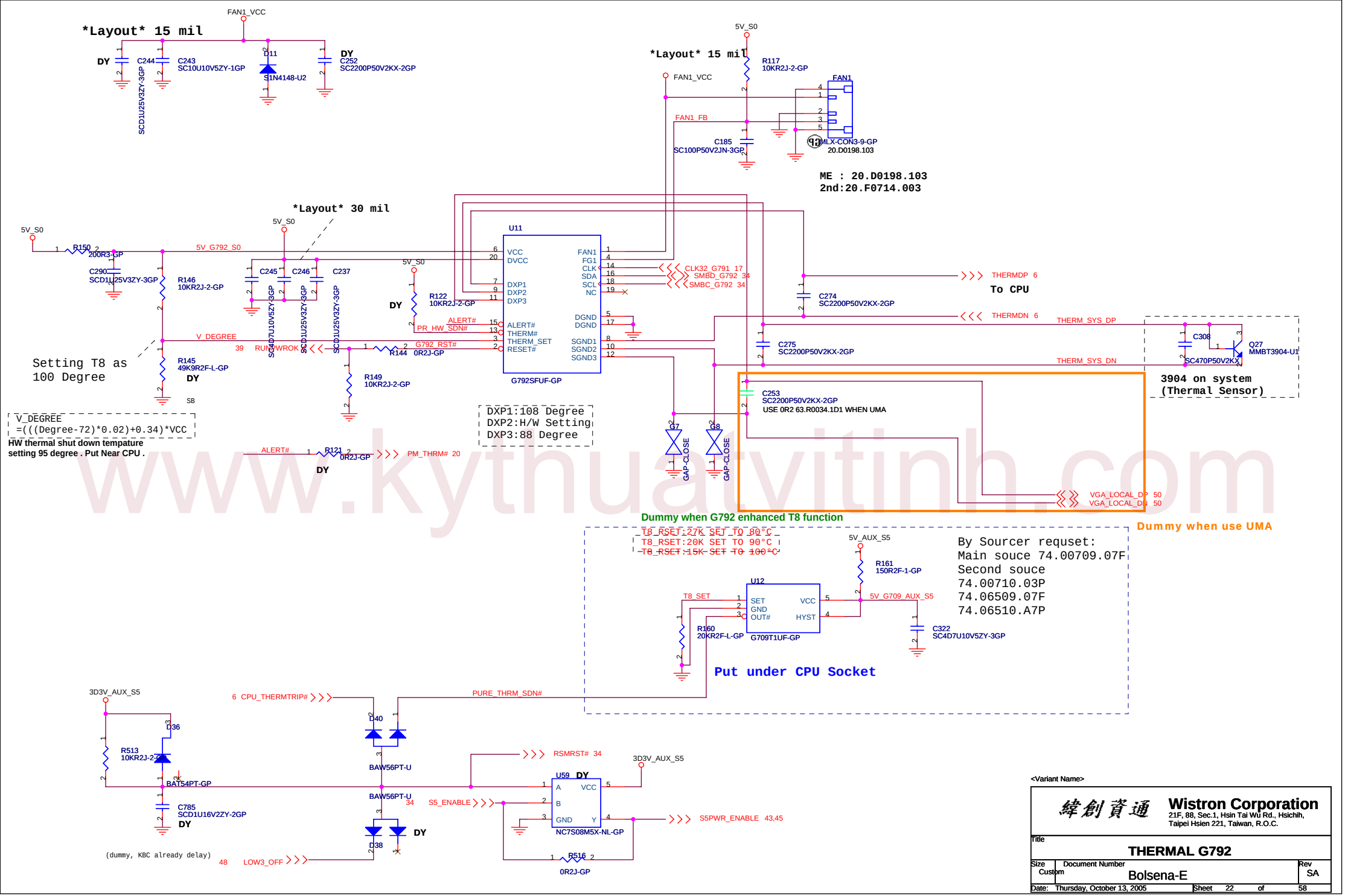
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 STRAPPING(5 of 5)

Size: A3 | Document Number: Bolsena-E | Rev: SA

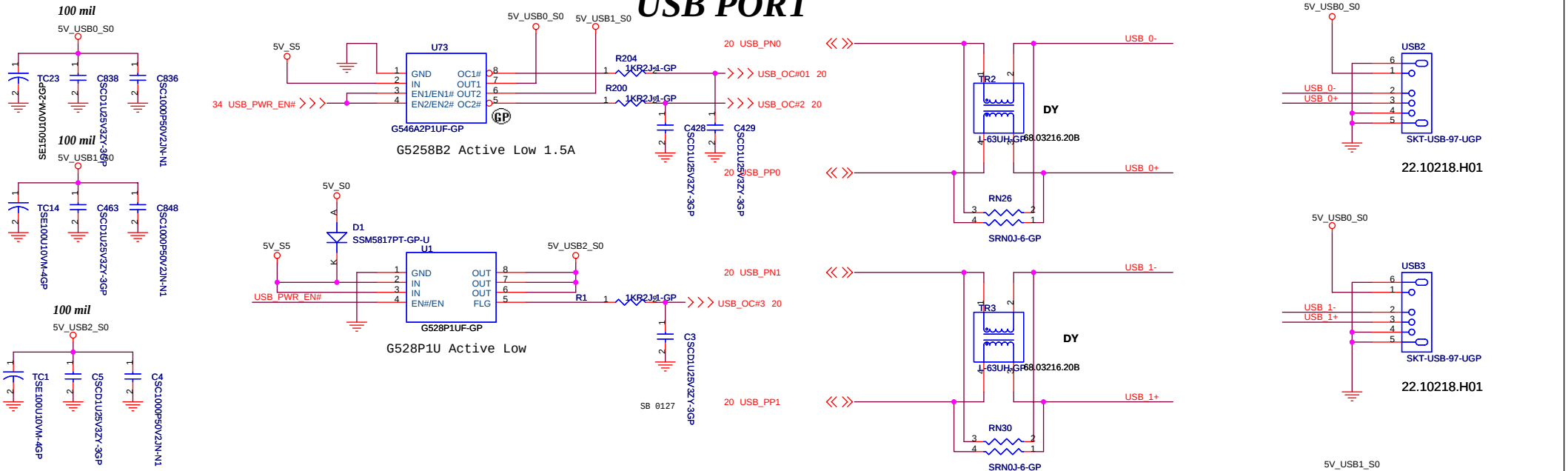
Date: Thursday, October 13, 2005 | Sheet 21 of 58



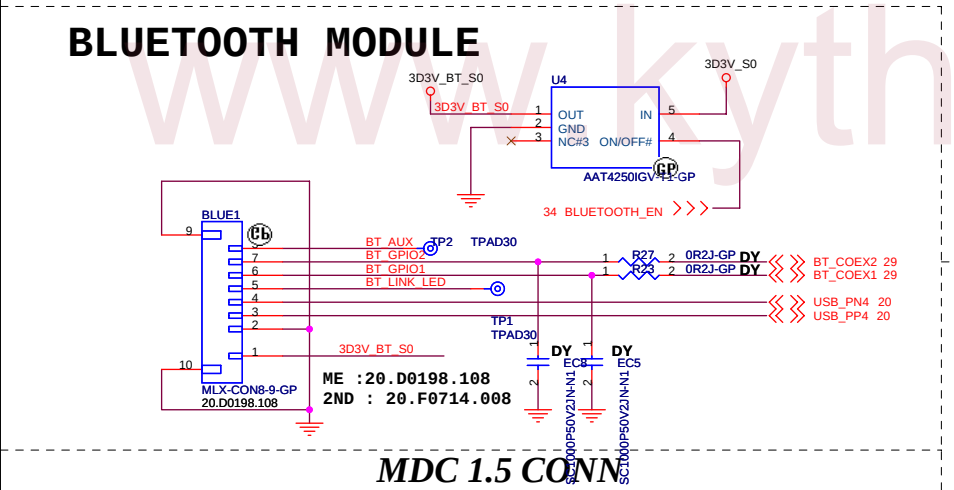
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**THERMAL G792**
Size: Custom	Document Number: Bolsena-E
Rev	SA
Date: Thursday, October 13, 2005	Sheet 22 of 58

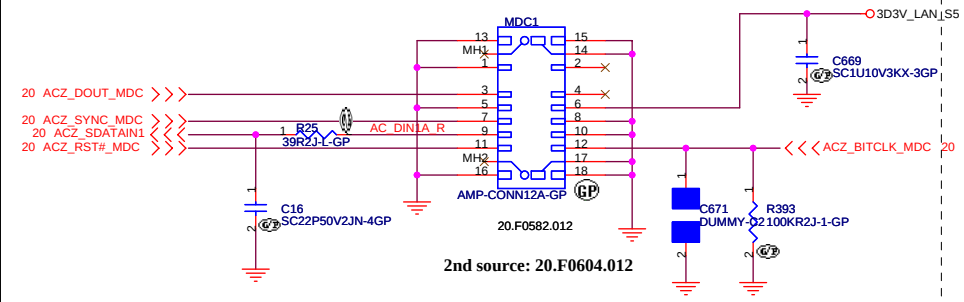
USB PORT



BLUETOOTH MODULE



MDC 1.5 CONN

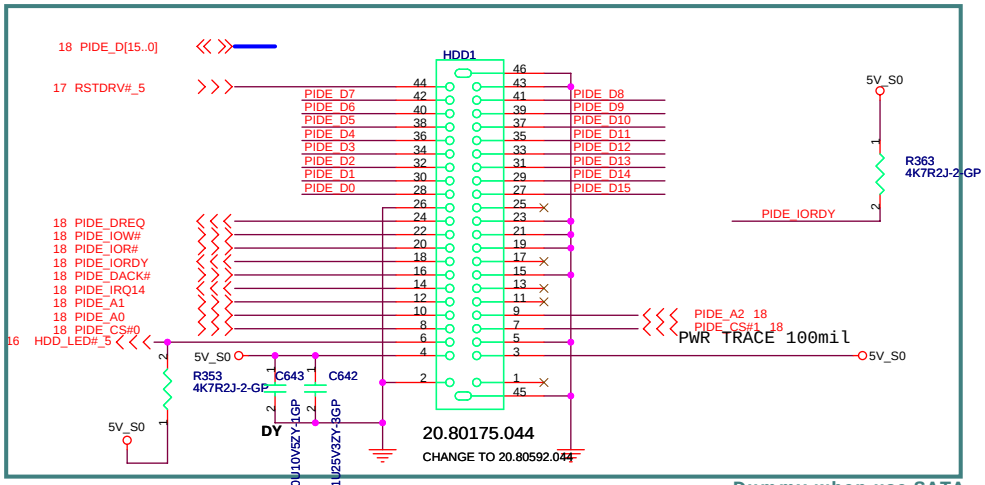


ME : 22.10218.H01
2ND : 22.10245.H11

<Variant Name>

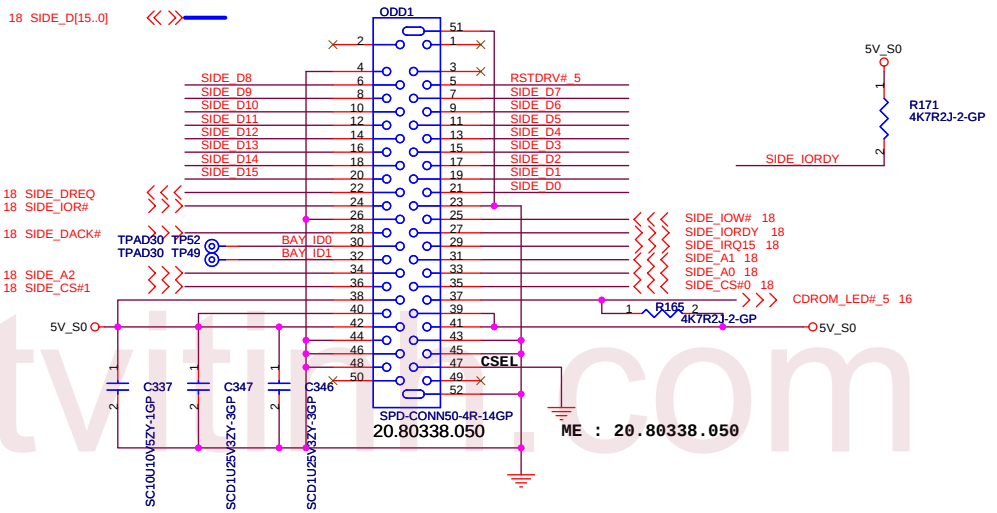
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB / MDC / BLUETOOTH		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 23 of 58	

HDD



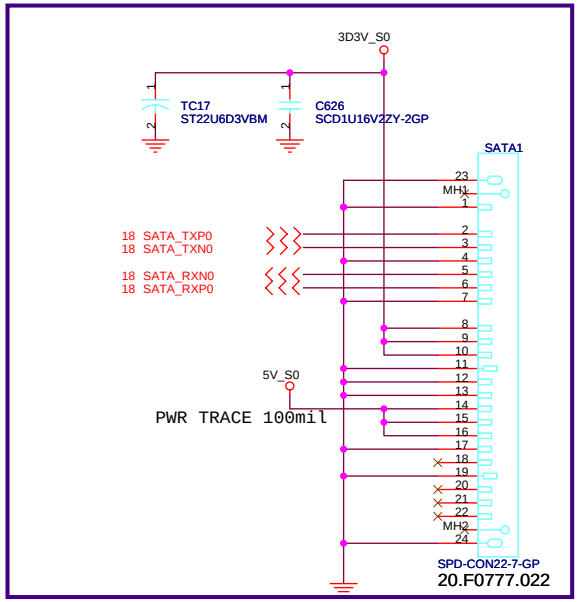
ME : 20.80592.044
(DIFFERENT FROM ORCAD P/N)

CDROM



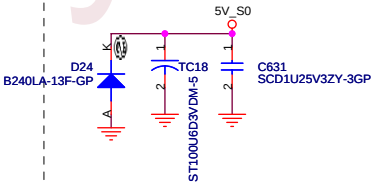
ME : 20.80338.050

SATA Connector



ME : 20.F0777.022

For HDD & SATA both



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD / CDROM / SATA

Size	Document Number	Rev
A3	Bolsena-E	SA

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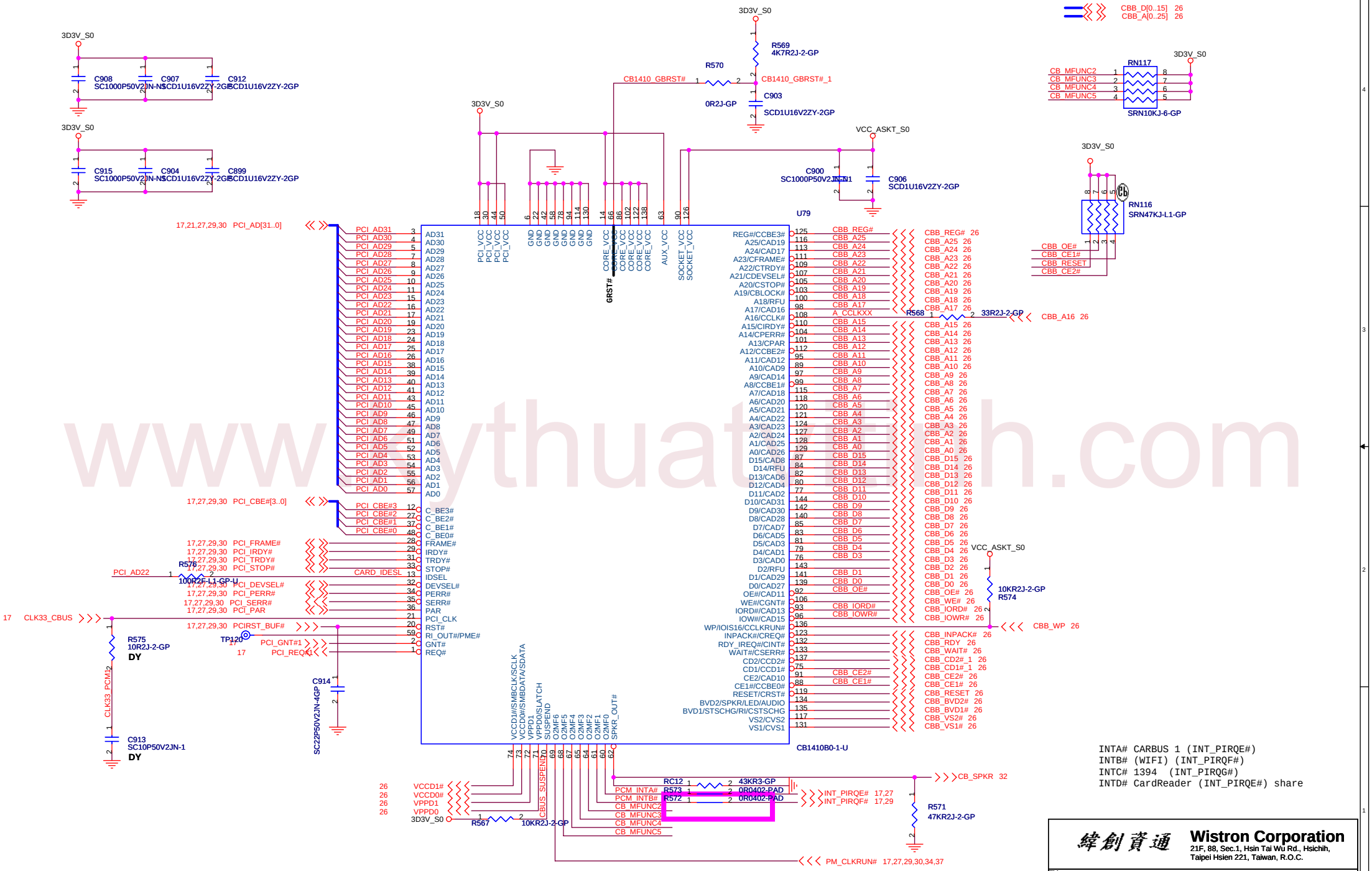
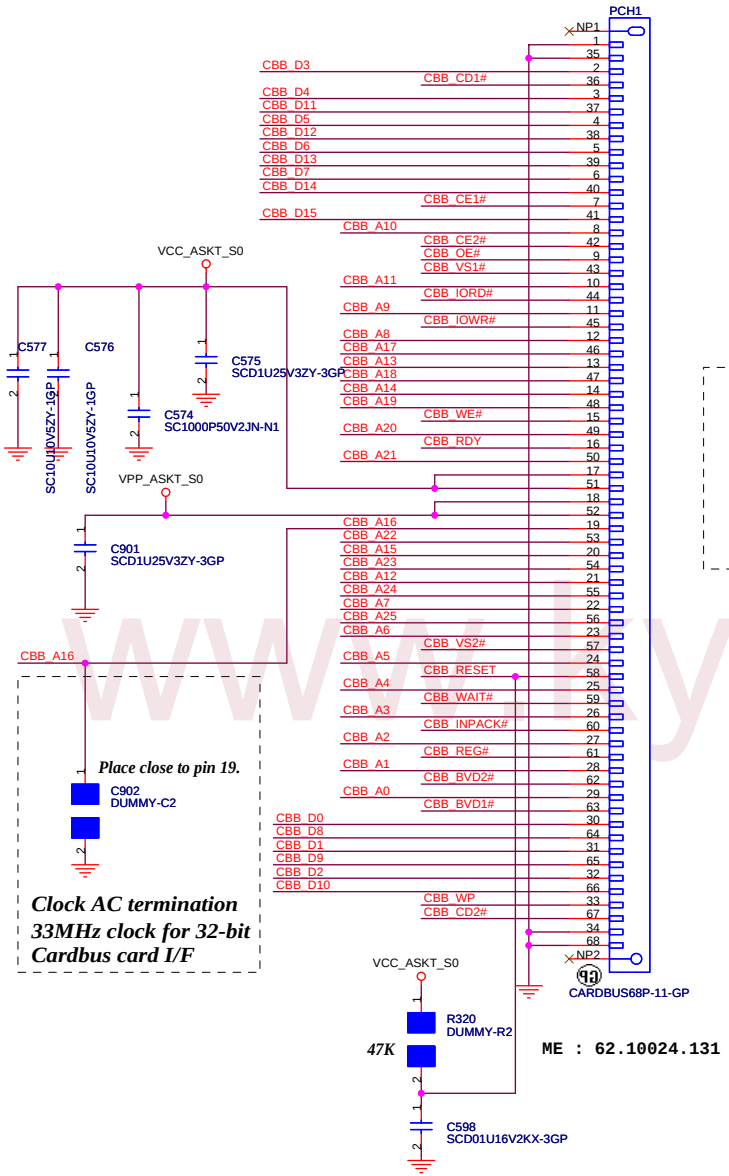


Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CardBus_ENE CB1410	
Size: A3	Document Number: Bolsena-E
Rev: SA	
Date: Thursday, October 13, 2005	Sheet 25 of 58

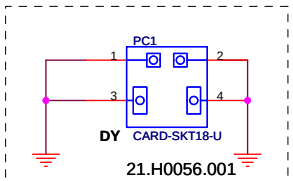
PCMCIA Socket



ME : 62.10024.131

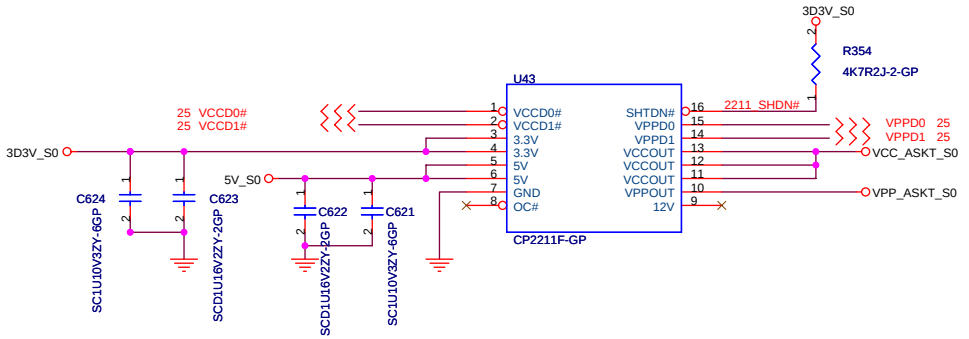
Cardbus I/F

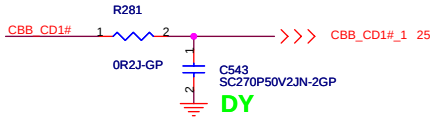
CBB_D[0..15] 25
CBB_A[0..25] 25
CBB_IORD# 25
CBB_IOWR# 25
CBB_OE# 25
CBB_WE# 25
CBB_REG# 25
CBB_RDY 25
CBB_WP 25
CBB_RESET 25
CBB_WAIT# 25
CBB_INPACK# 25
CBB_CE1# 25
CBB_CE2# 25
CBB_BVD1# 25
CBB_BVD2# 25
CBB_VS1# 25
CBB_VS2# 25

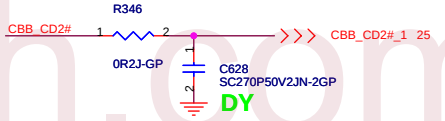


ME : 21.H0056.001

Power switch







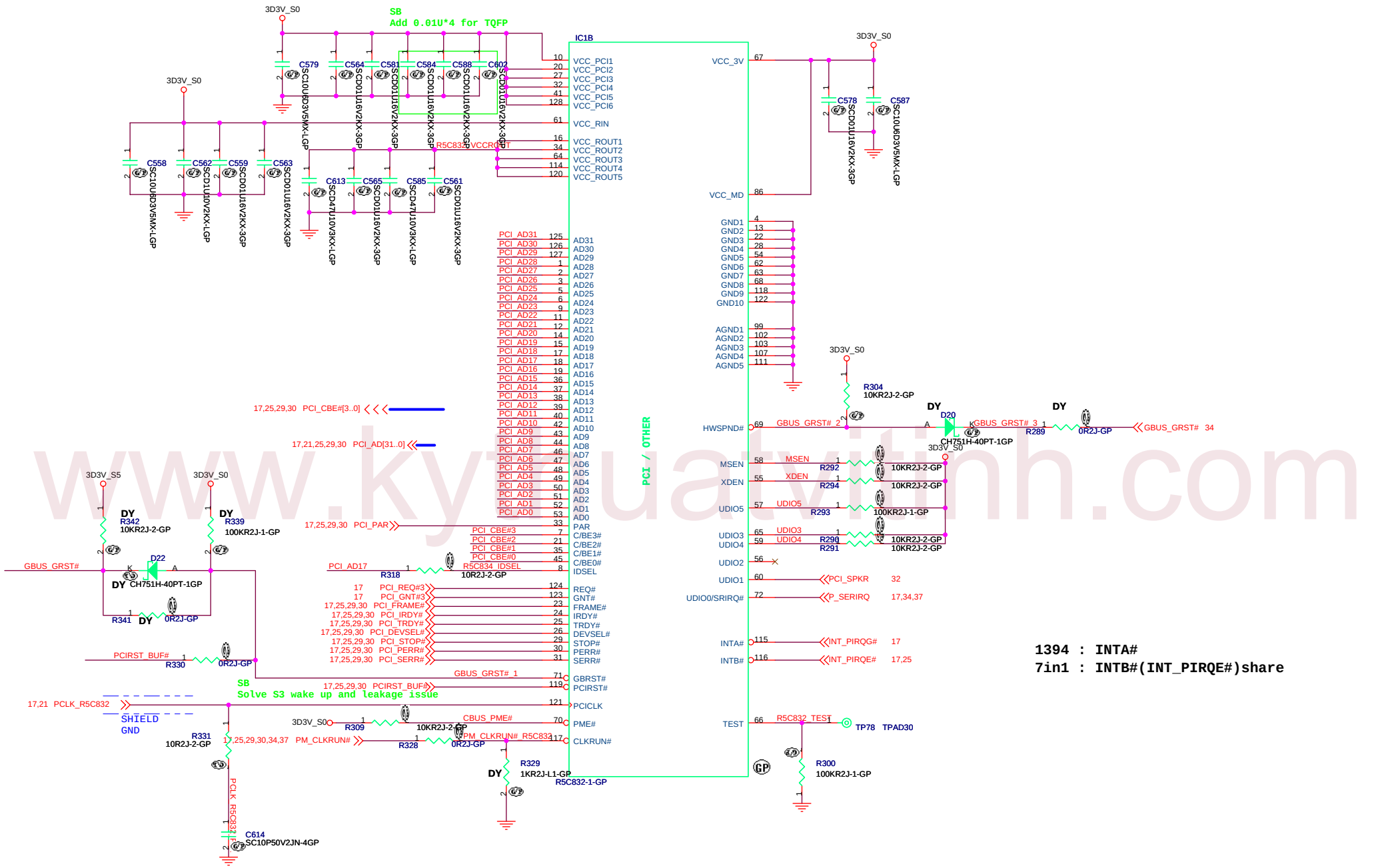
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

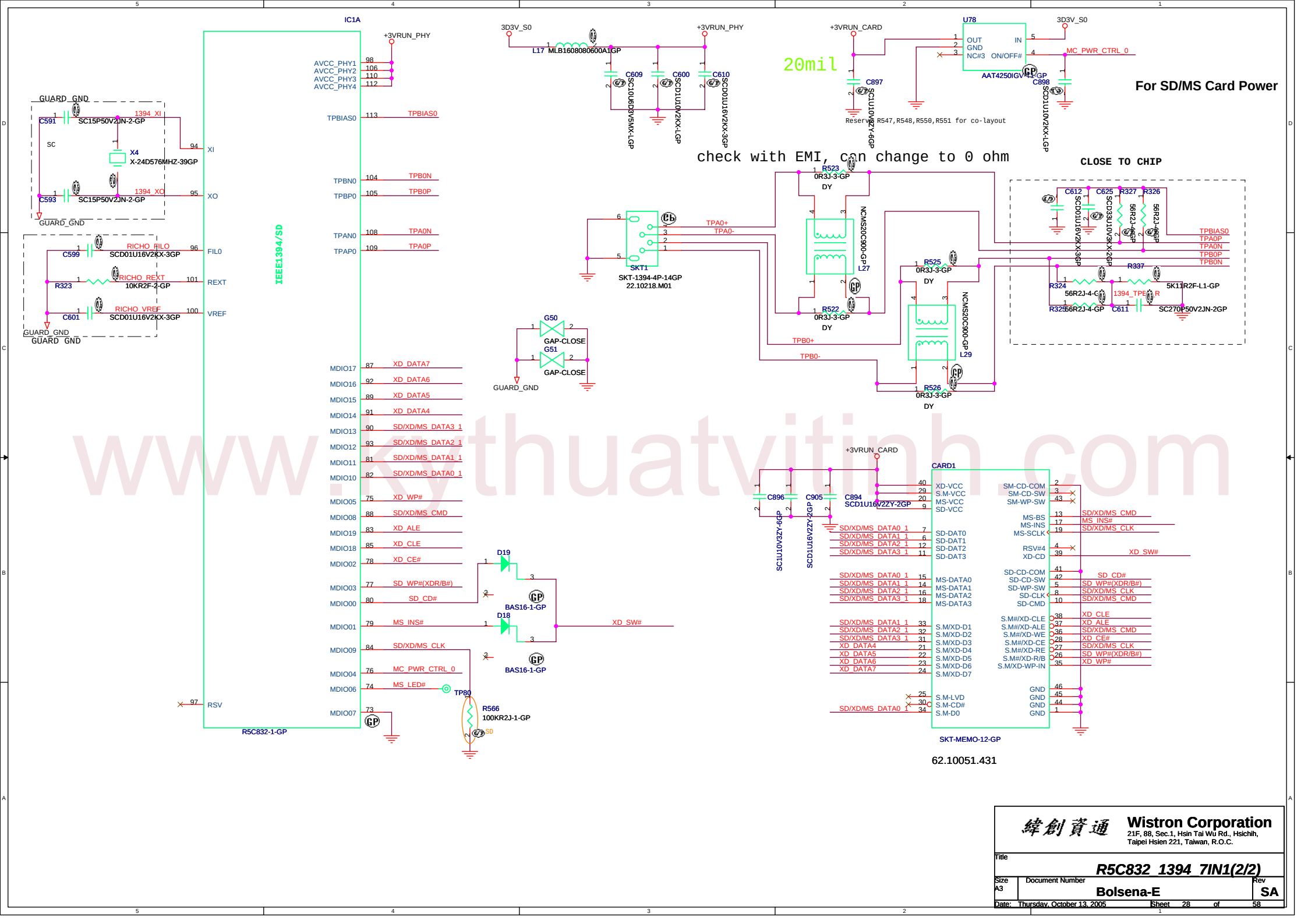
Title: **PCMCA / 1394 / CARD READER**

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 26 of 58



緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	R5C832_1394_7IN1(2/2)	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 27 of 58	


IC1A
IEEE1394/SD
R5C832-1-GP
+3VRUN_PHY
3D3V_S0
+3VRUN_CARD
20mil
For SD/MS Card Power
check with EMI, can change to 0 ohm
CLOSE TO CHIP
SKT-1394-4P-14GP
22.10218.M01
SKT-MEMO-12-GP
CARD1
62.10051.431
www.kythuatvitinh.com
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
R5C832_1394_7IN1(2/2)
Bolsena-E
SA
Thursday, October 13, 2005
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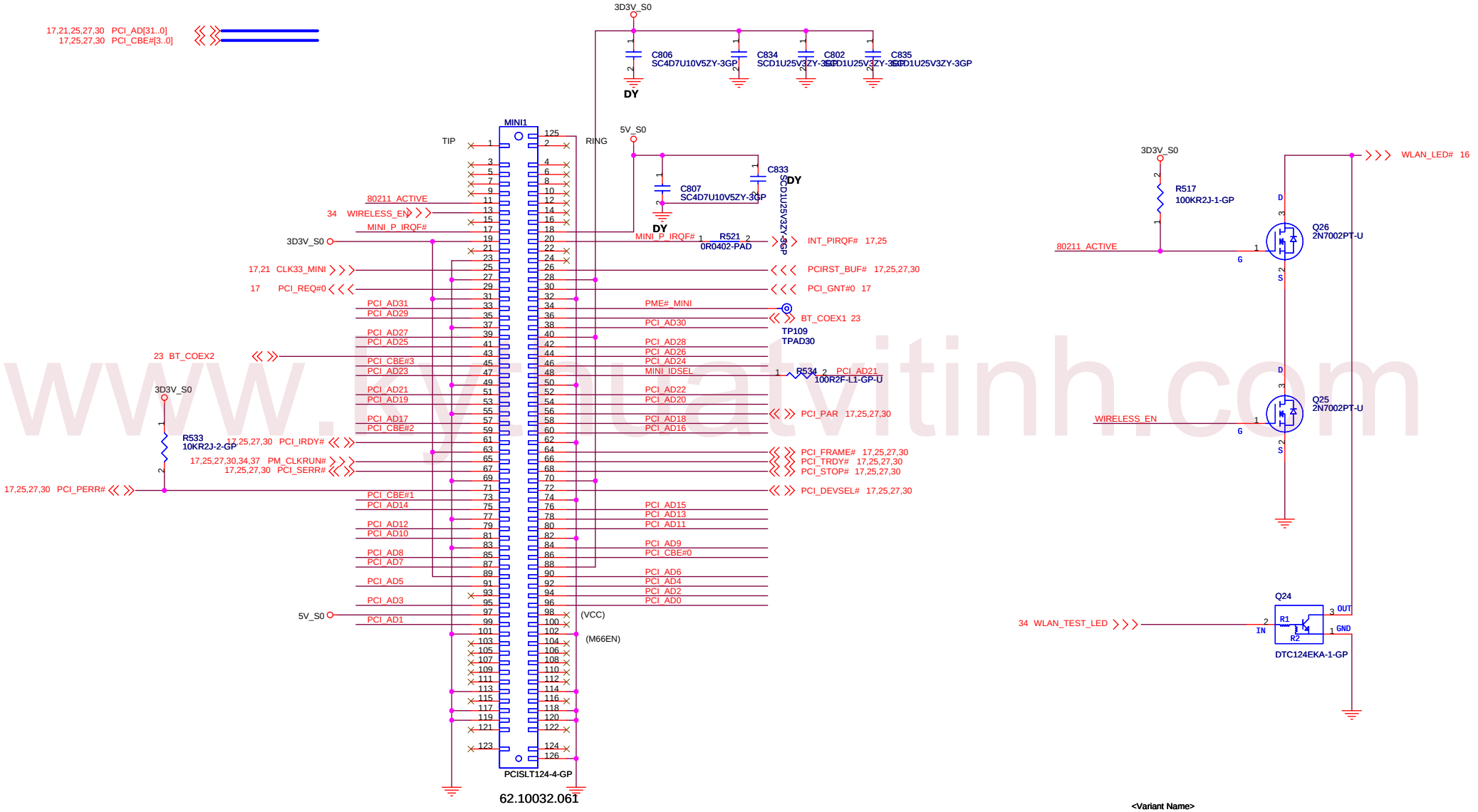
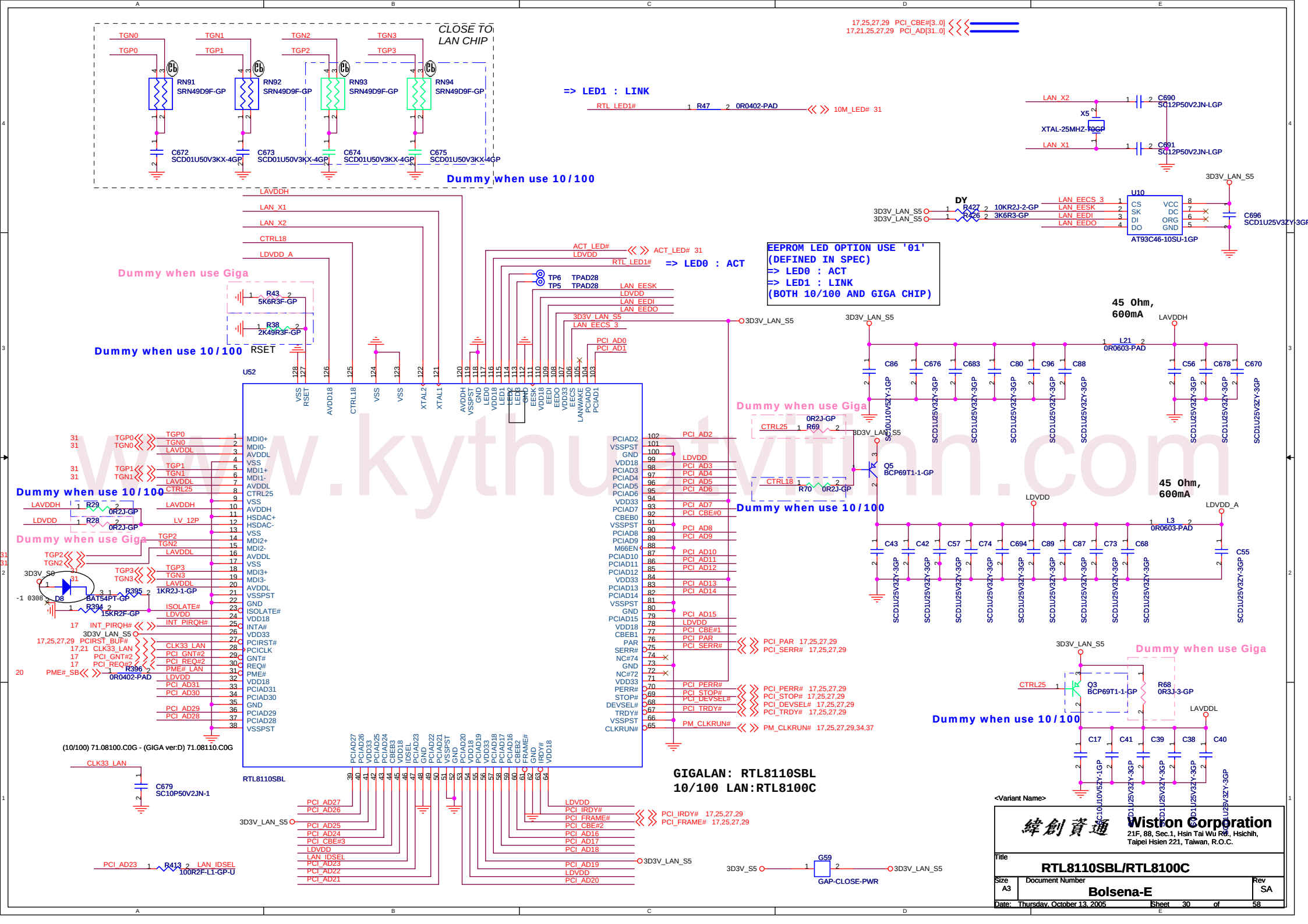
MINI-PCI



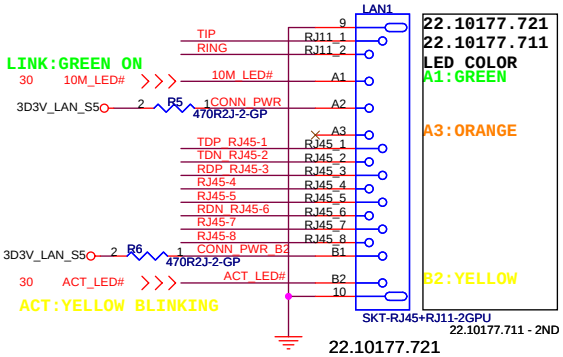
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

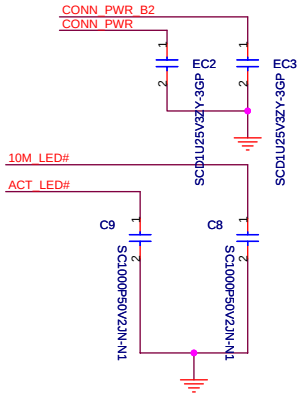
Title: MINI-PCI		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 29 of 58	

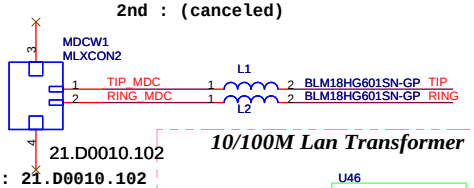


Link: Green - 10Mbps/802.11b Activity: Yellow
Orange - 100Mbps/802.11a
Yellow - 1Gbps



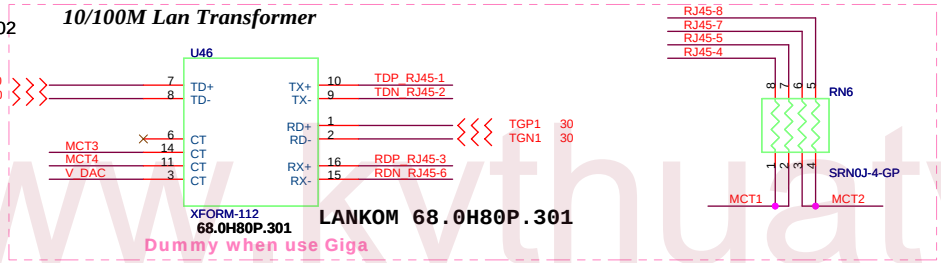
22.10177.721
ME : 22.10177.721
2nd : (canceled)





21.D0010.102
ME : 21.D0010.102

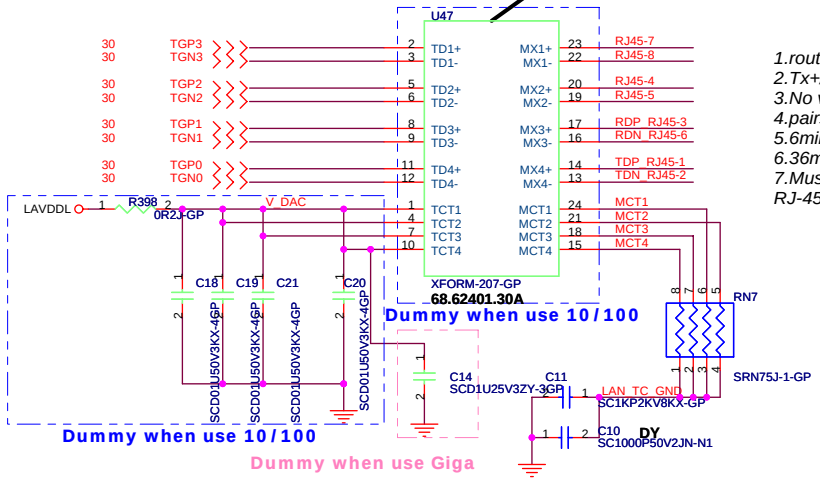
10/100M Lan Transformer



GIGA Lan Transformer

LANKOM 68.02402.30A
netSWAP 68.62401.301 (GIGA ,Thick)

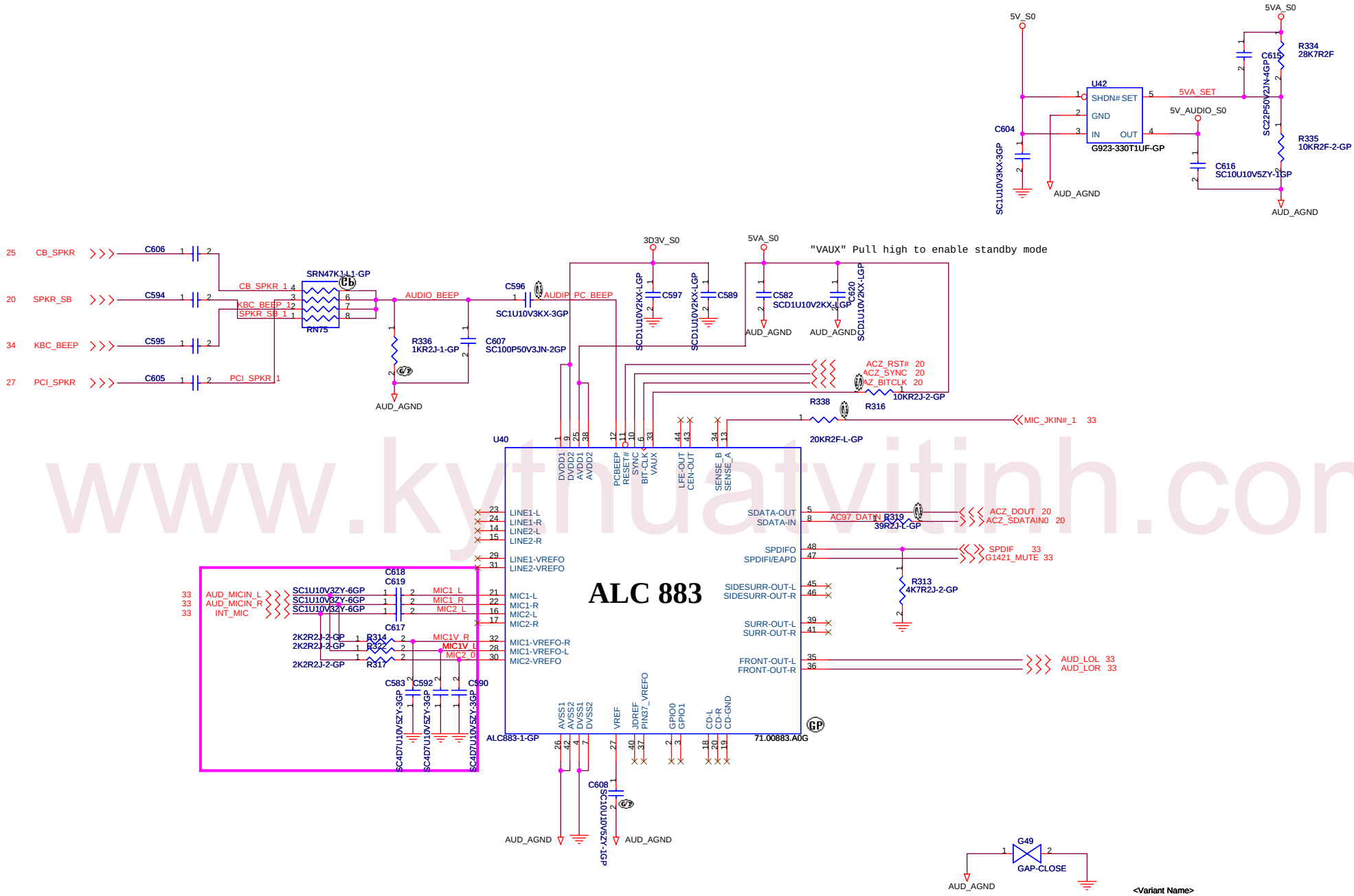
NETSWAP GIGA THICK PN IS 68.62401.301, DON'T USE NETSWAP THIN



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**
Size: A3 | Document Number: **Bolsena-E** | Rev: SA
Date: Thursday, October 13, 2005 | Sheet 31 of 58



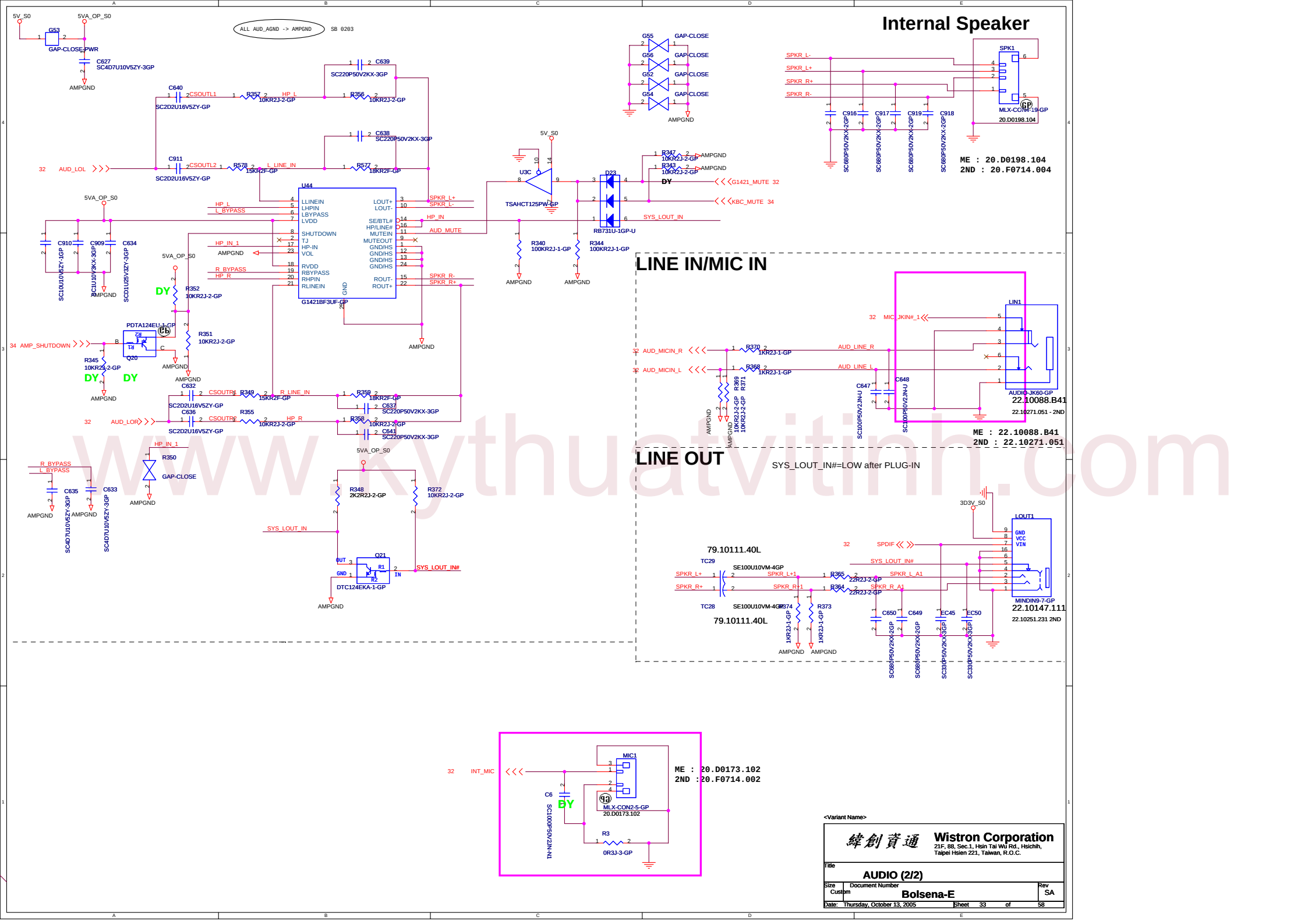
<Variant Name>

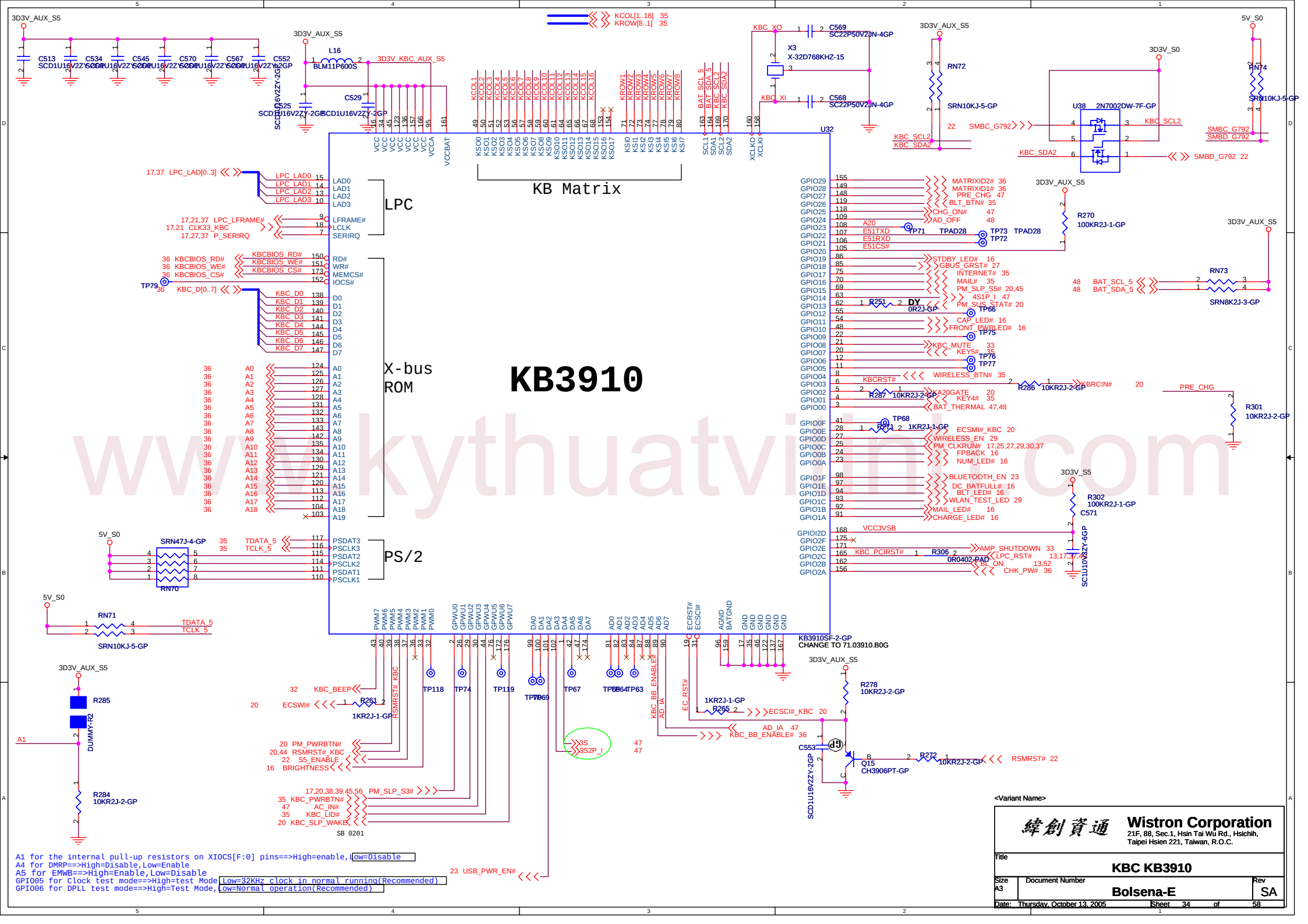
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO (1/2) -- CODEC ALC655**

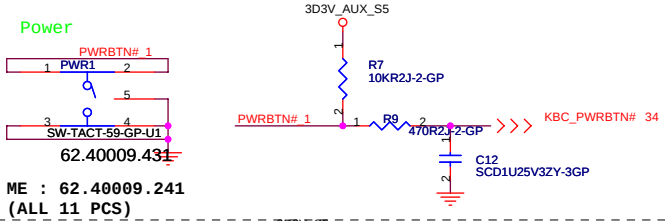
Size	Document Number	Rev
A3	**Bolsena-E**	SA

Date: Thursday, October 13, 2005 Sheet 32 of 58



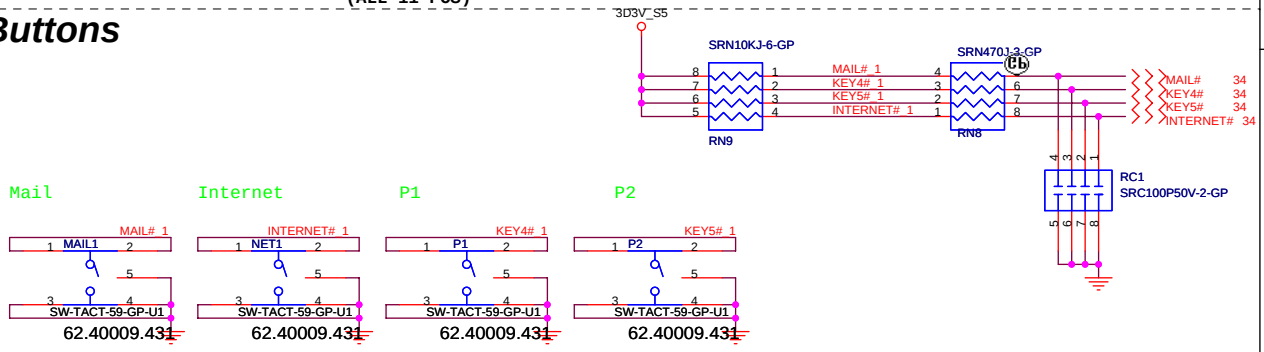

KB3910
KB Matrix
LPC
X-bus ROM
PS/2
U32
KB3910SF-2-GP
CHANGE TO 71.03910.B0G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC KB3910
Bolsena-E
Size A3
Rev SA
Date: Thursday, October 13, 2005
Sheet 34 of 58
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable, Low=Disable
A4 for DMRP==>High=Disable, Low=Enable
A5 for EMWB==>High=Enable, Low=Disable
GPIO05 for Clock test mode==>High=test Mode, Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode, Low=Normal operation(Recommended)

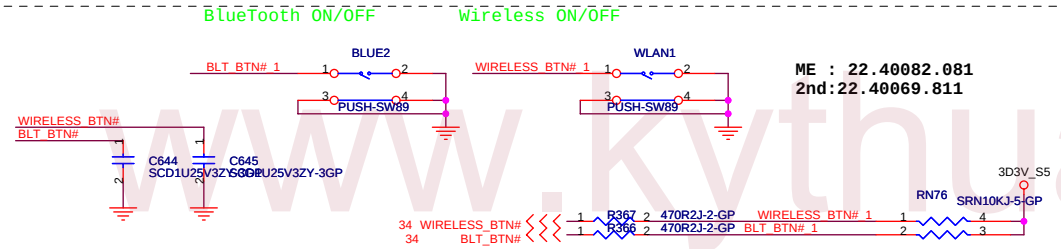
POWER BUTTON



ME : 62.40009.241
(ALL 11 PCS)

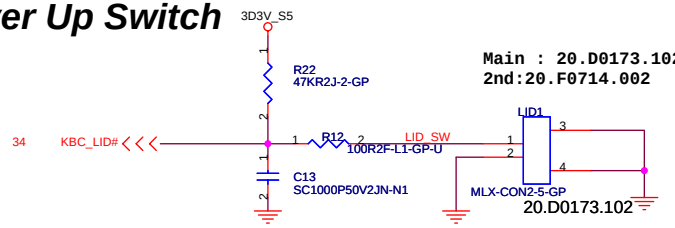
Buttons





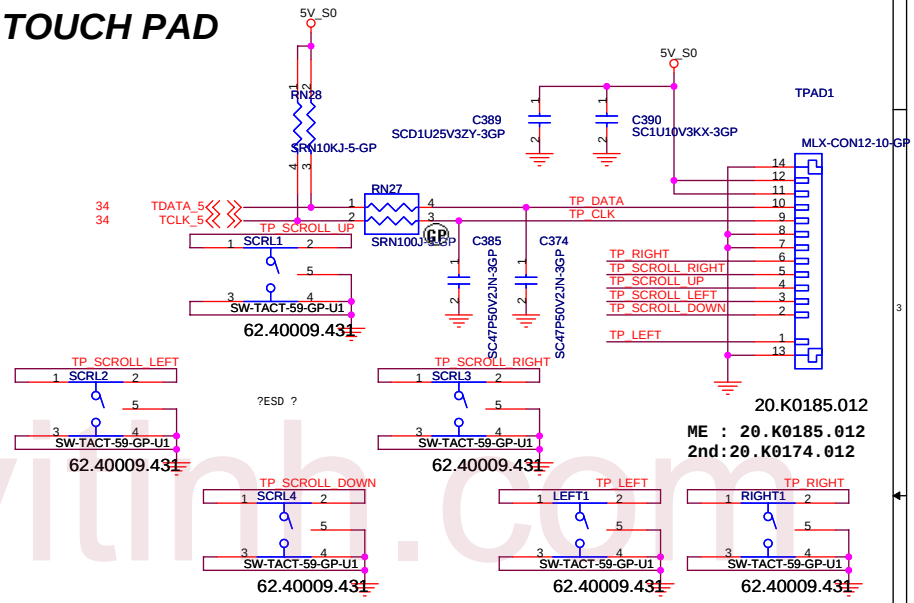
ME : 22.40082.081
2nd:22.40069.811

Cover Up Switch



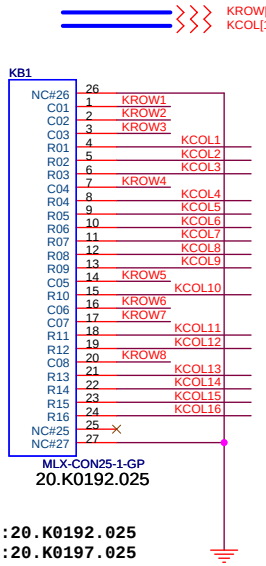
Main : 20.D0173.102
2nd:20.F0714.002

TOUCH PAD



20.K0185.012
ME : 20.K0185.012
2nd:20.K0174.012

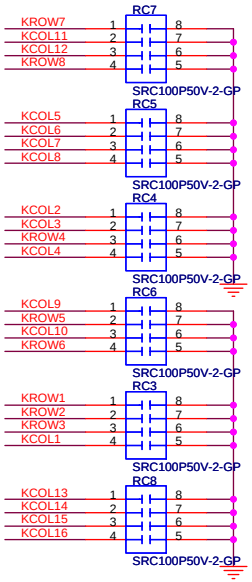
Internal KeyBoard CONN

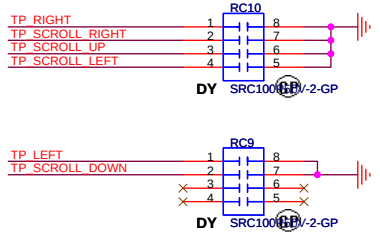


ME :20.K0192.025
2nd:20.K0197.025

```
Pin1 ==>*R01
Pin2 ==>*R02
Pin3 ==>*R03
Pin4 ==> C01
Pin5 ==> C02
Pin6 ==> C03
Pin7 ==>*R04
Pin8 ==> C04
Pin9 ==> C05
Pin10 ==> C06
Pin11 ==> C07
Pin12 ==> C08
Pin13 ==> C09
Pin14 ==>*R05
Pin15 ==> C10
Pin16 ==>*R06
Pin17 ==>*R07
Pin18 ==> C11
Pin19 ==> C12
Pin20 ==>*R08
Pin21 ==> C13
Pin22 ==> C14
Pin23 ==> C15
Pin24 ==> C16
Pin25 ==> NC
```

EMI Bypass cap.





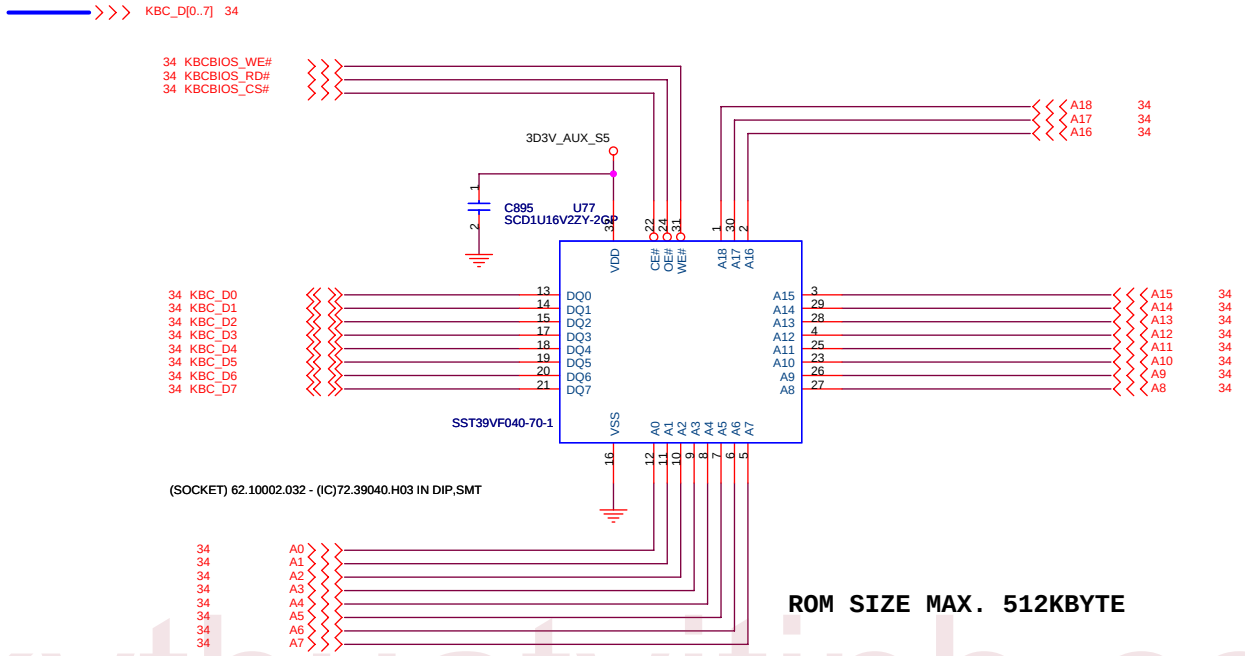
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BUTTONs / KB / TOUCHPAD

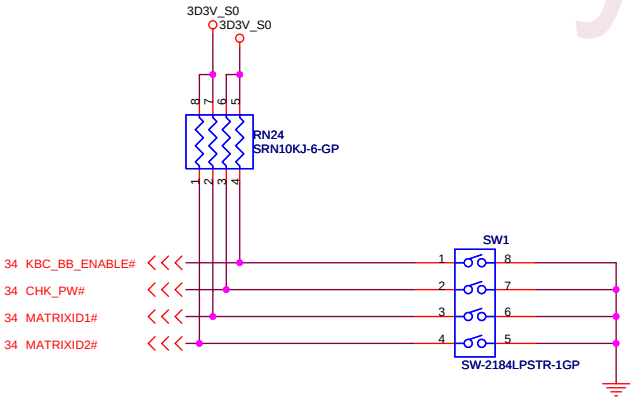
Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 35 of 58



ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

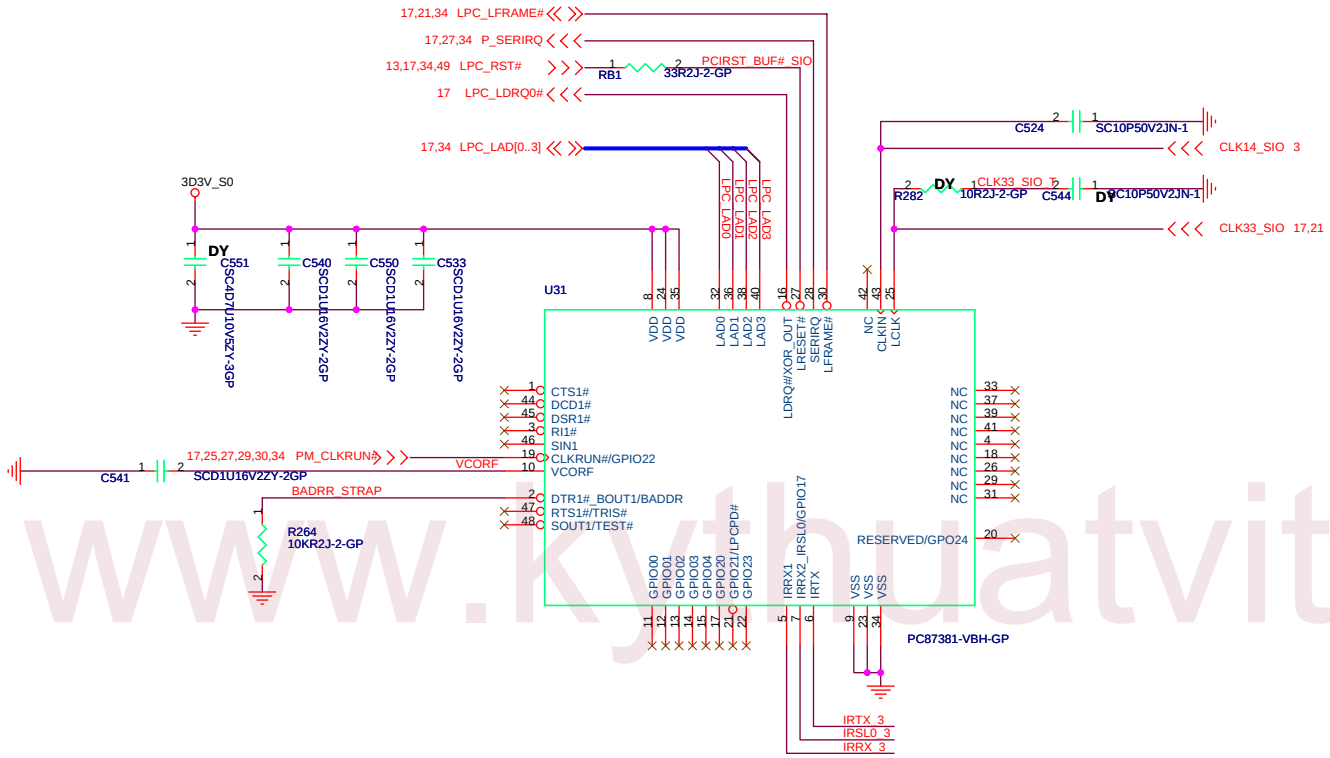
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

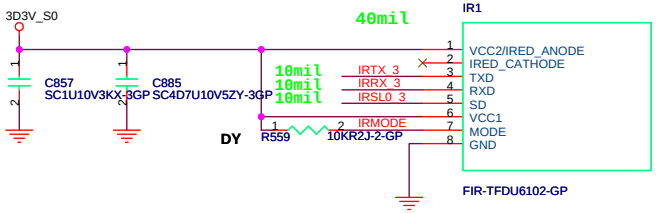
Title: **BIOS ROM**

Size: A3 | Document Number: **Bolsena-E** | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 36 of 58



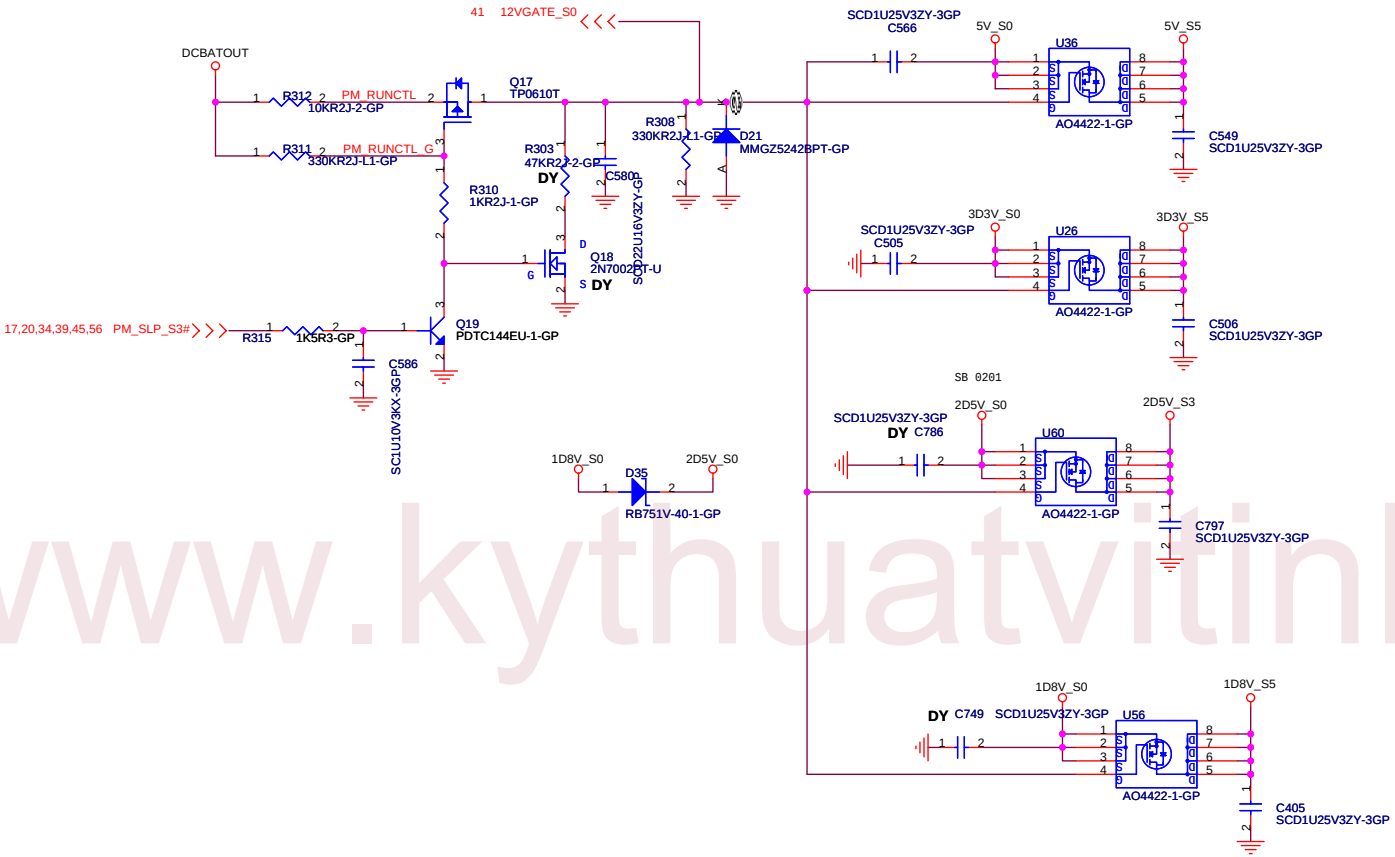
Infineon FIR Module



56.15001.051

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SUPER IO NC87381		
Size: A3	Document Number: SNIPE	Rev: -2
Date: Thursday, October 13, 2005	Sheet 37 of 58	

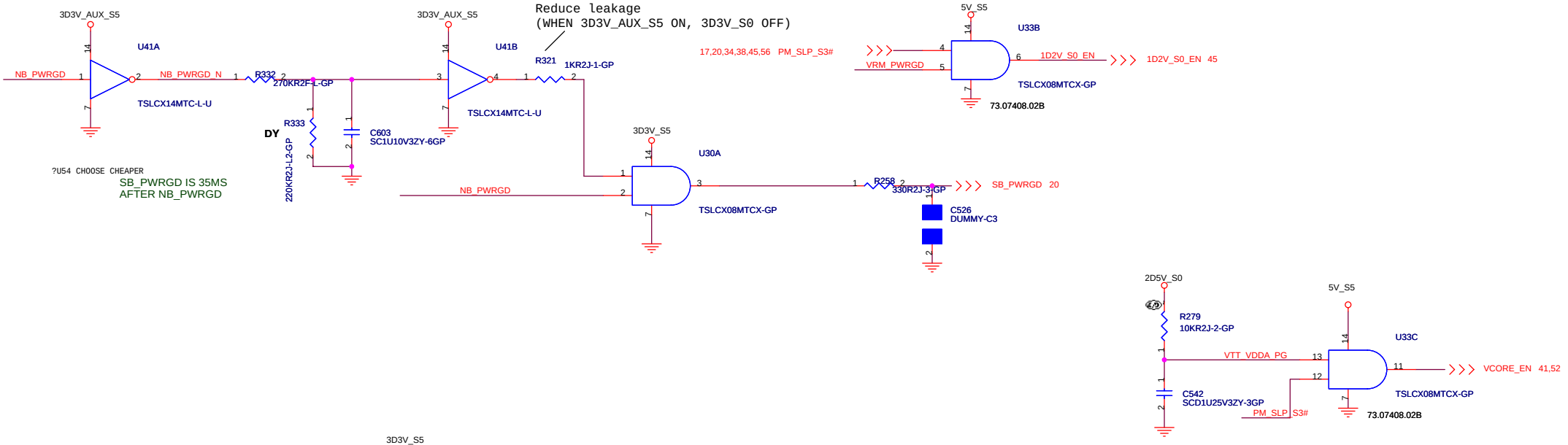
Run Power



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PWR CTL LOGIC / PWR PLANE	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 38 of 58	



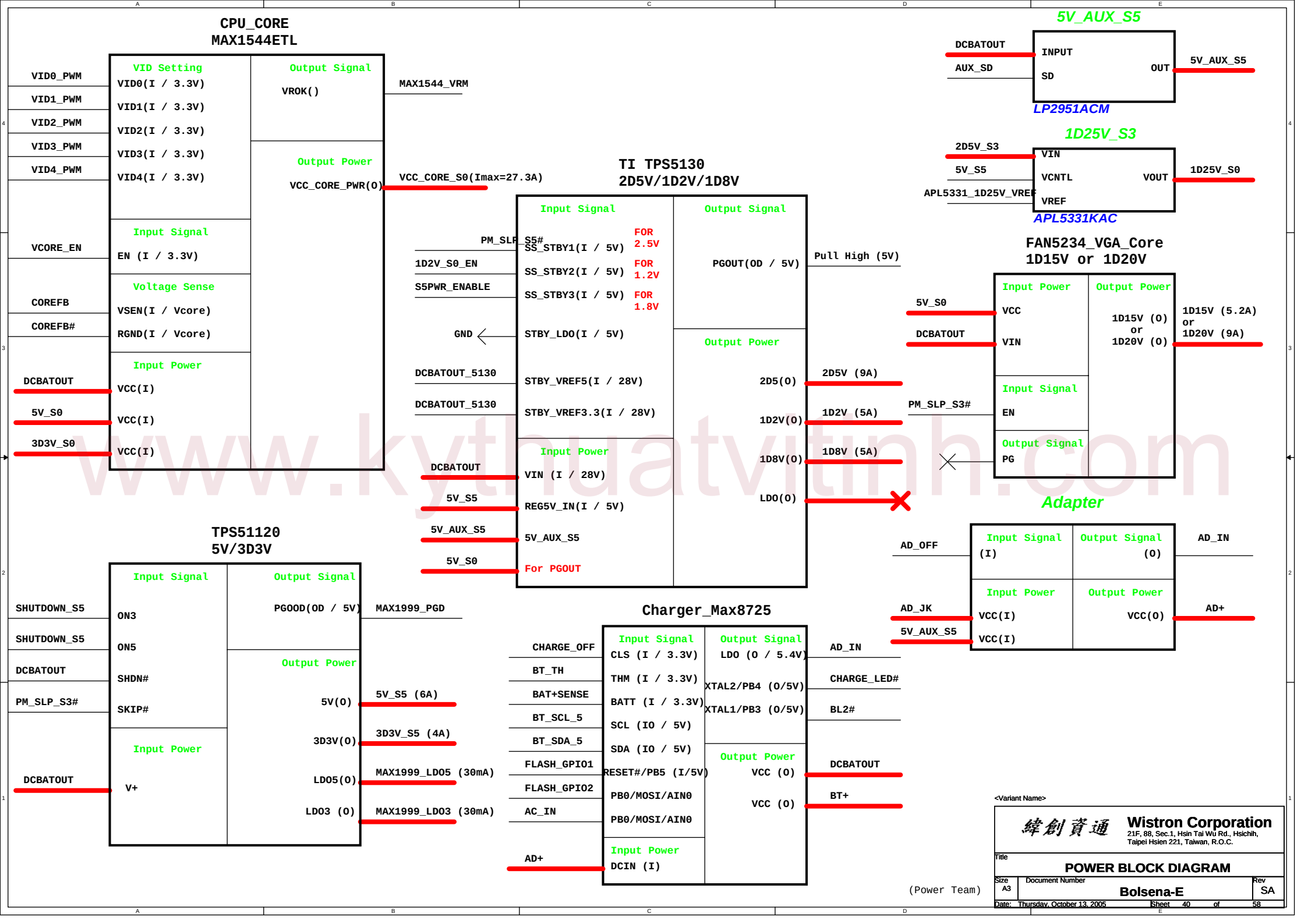
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWERGOOD&ENABLES

Size: Custom | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 39 of 58



CPU_VCORE
VID=1.20V
Iomax=27.3A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

TON:	Frequency:
GND	550KHz
REF	300KHz
OPEN	200KHz
VCC	100KHz

For Dummy Phase 2

For alone test==>short C395 pin1 and pin2

VCC_CORE_S0 feedback

From KBC

<Variant Name>

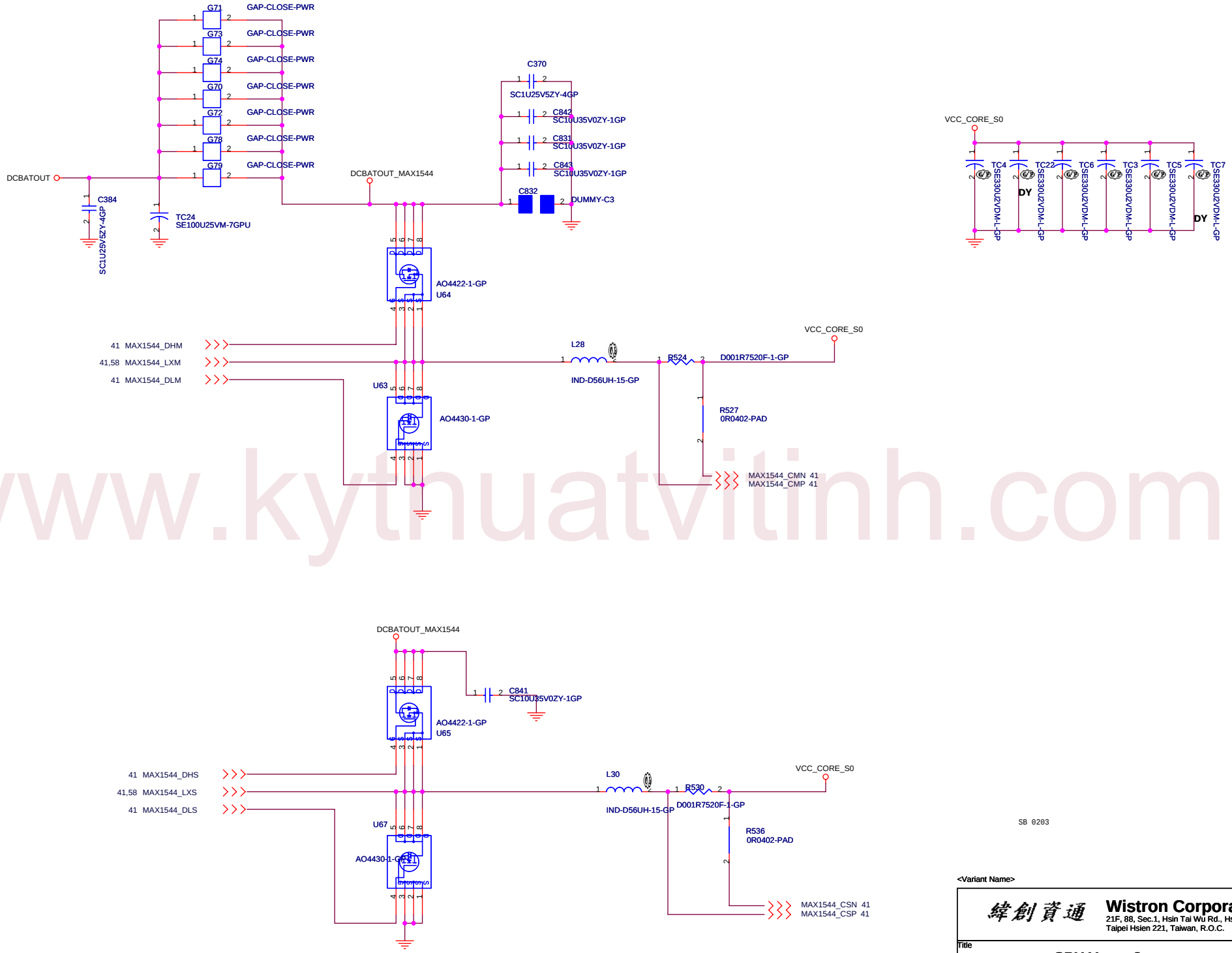
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore 1

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 41 of 58

(Power Team)



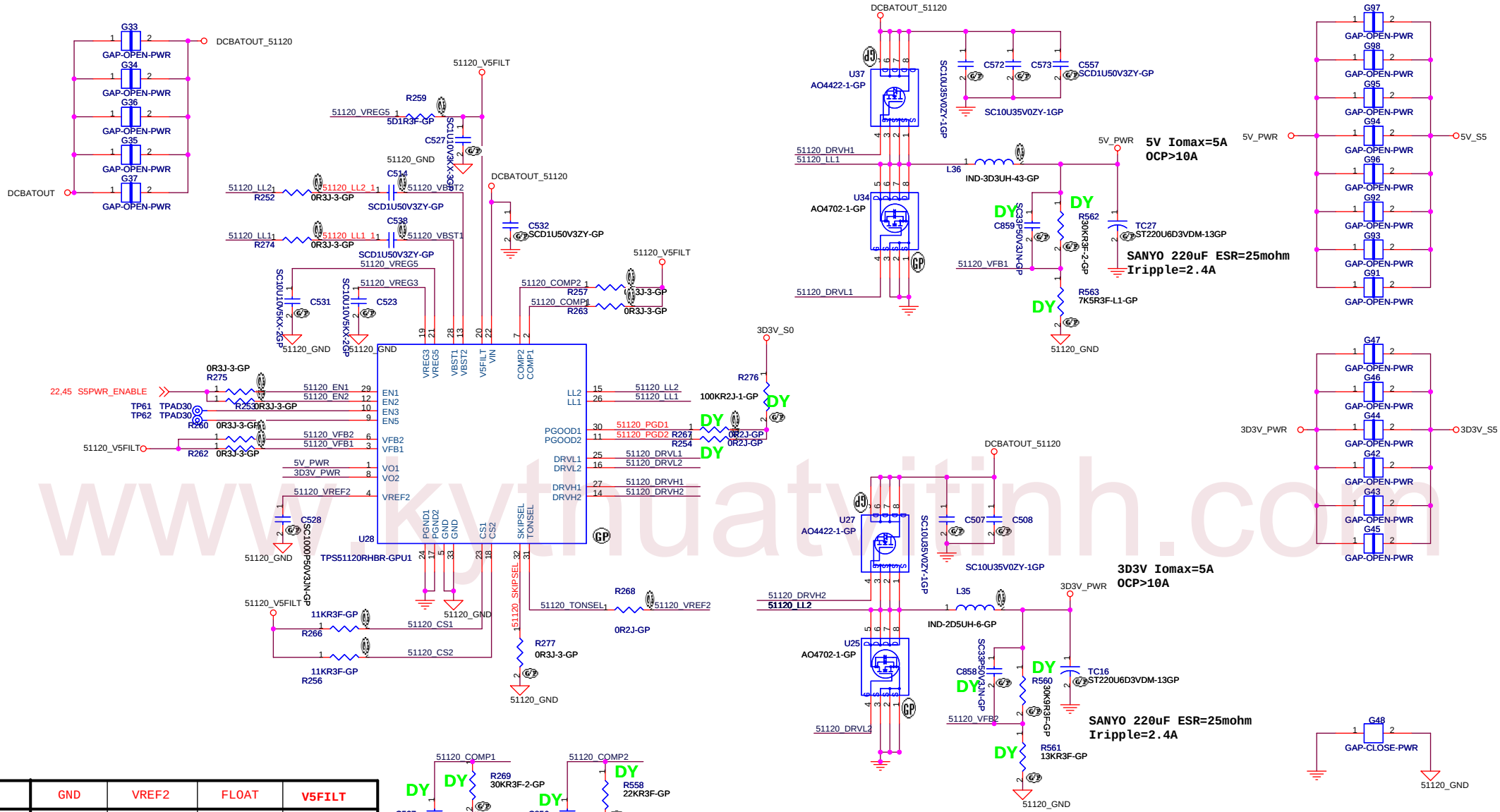
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore 2

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 42 of 58



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

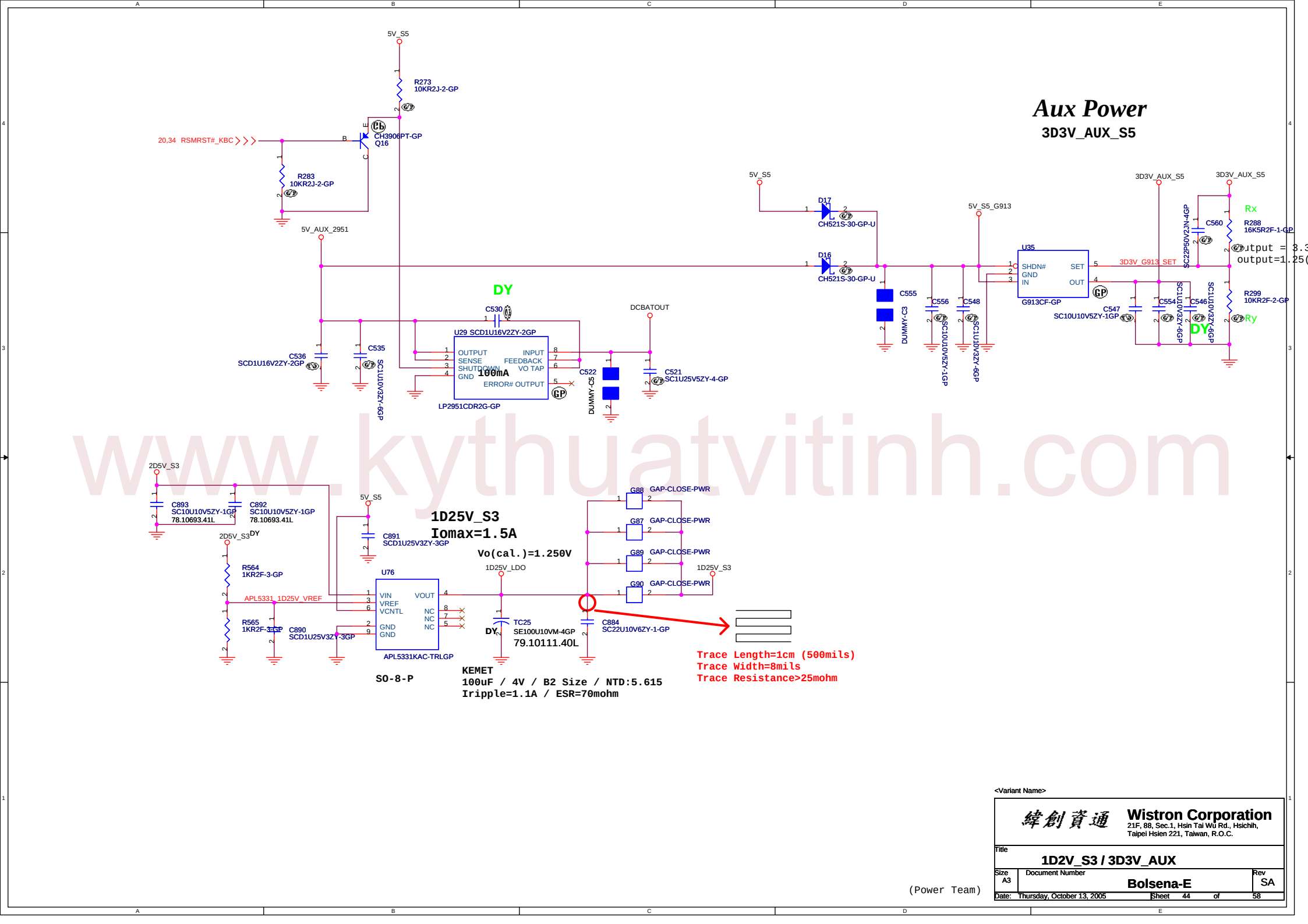
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51120 / 3D3V / 5V

Size: A3 | Document Number: Bolsena-E | Rev: -1

Date: Thursday, October 13, 2005 | Sheet 43 of 58



<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	1D2V_S3 / 3D3V_AUX
Size: A3	Document Number: Bolsena-E
Rev: SA	
Date: Thursday, October 13, 2005	Sheet 44 of 58

(Power Team)

TI TPS5130 for 2.5V, 1.2V, 1.8V

Vo=(R1*0.85)/R2+0.85

(1D2V=>CH1 , 1D8V=>CH2 , 2D5V =>CH3)

For 2.5V
SETTING=2.516V

For 1.8V
SETTING=1.8275V

For 1.2V
SETTING=1.2172V

close to IC

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

T(soft)=1.736ms

TPS5130

LDO SETTING

1D2V_OCP
OCP
8.4A=>R226=13K
10A=>R226=22K

1D8V_OCP
OCP
8.4A=>R229=12.65K
10A=>R229=22K

2D5V_OCP
OCP
12A=>R225=18K
18A=>R225=28K

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS5130 1D2V/1D8V2D5V/ (1/2)

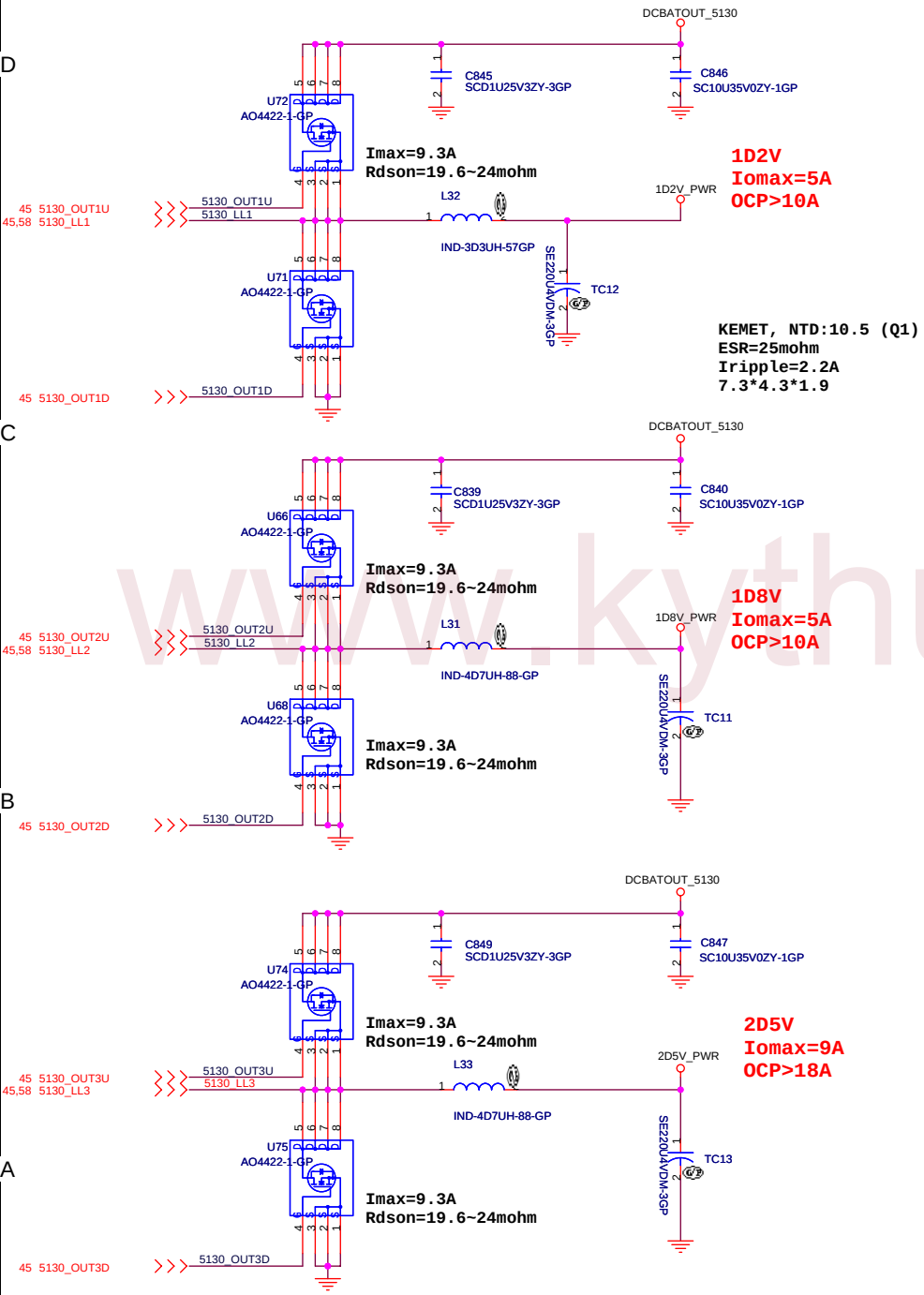
Size: A3 | Document Number: Bolsena-E | Rev: SA

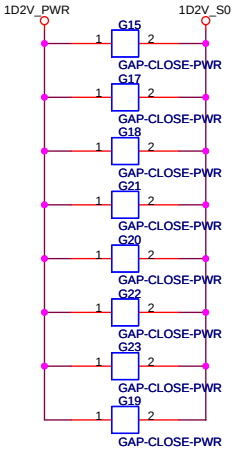
Date: Thursday, October 13, 2005 | Sheet 45 of 58

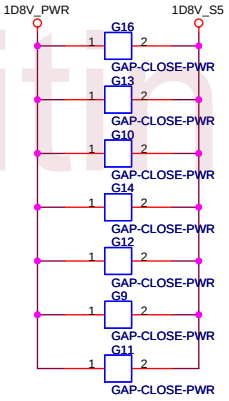
(Power Team)

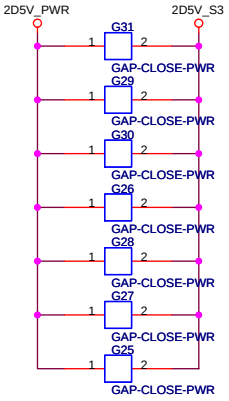
TI TPS5130 for 2D5V, 1D2V, 1D8V

(1D2V=>CH1 , 1D8V=>CH2 , 2D5V =>CH3)









(Power Team)

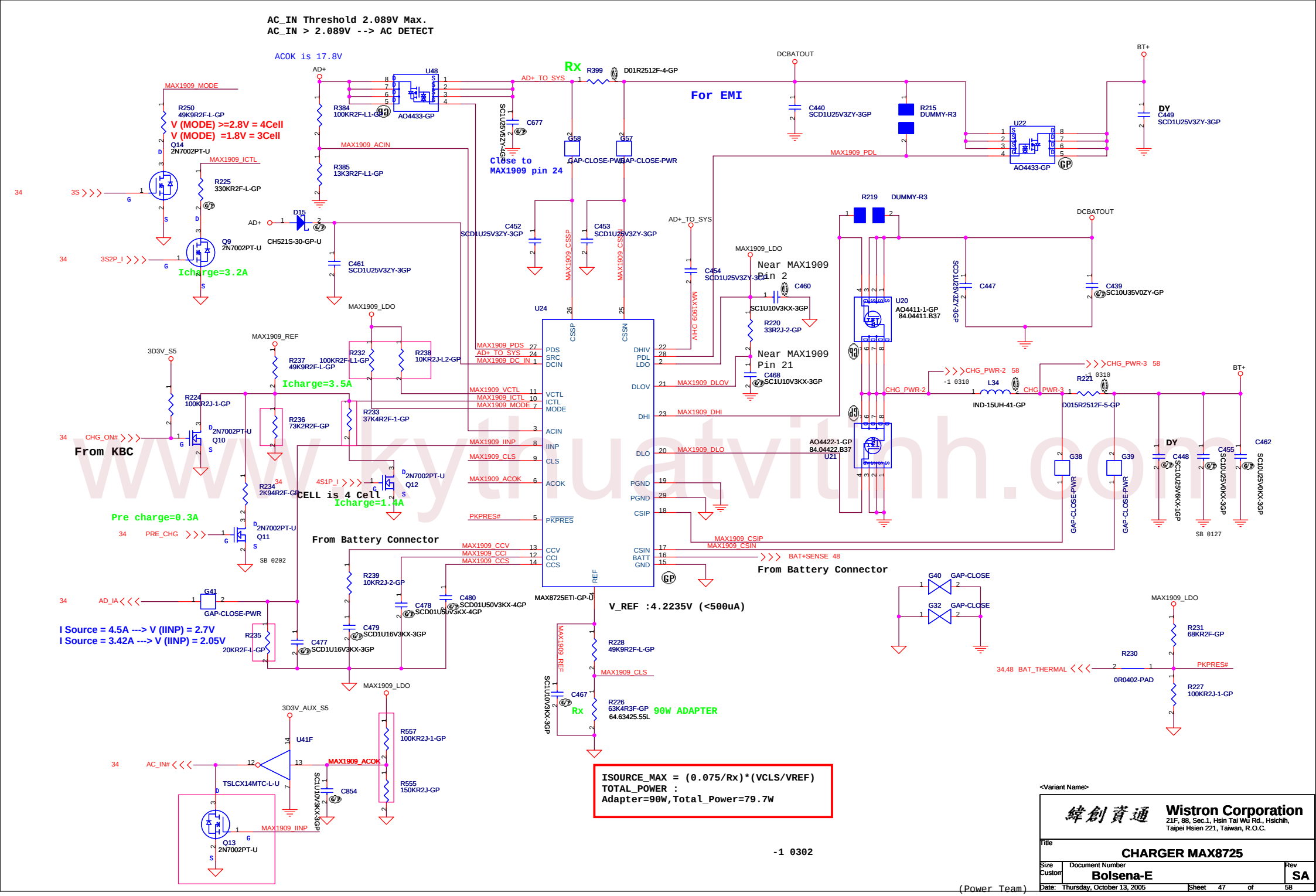
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

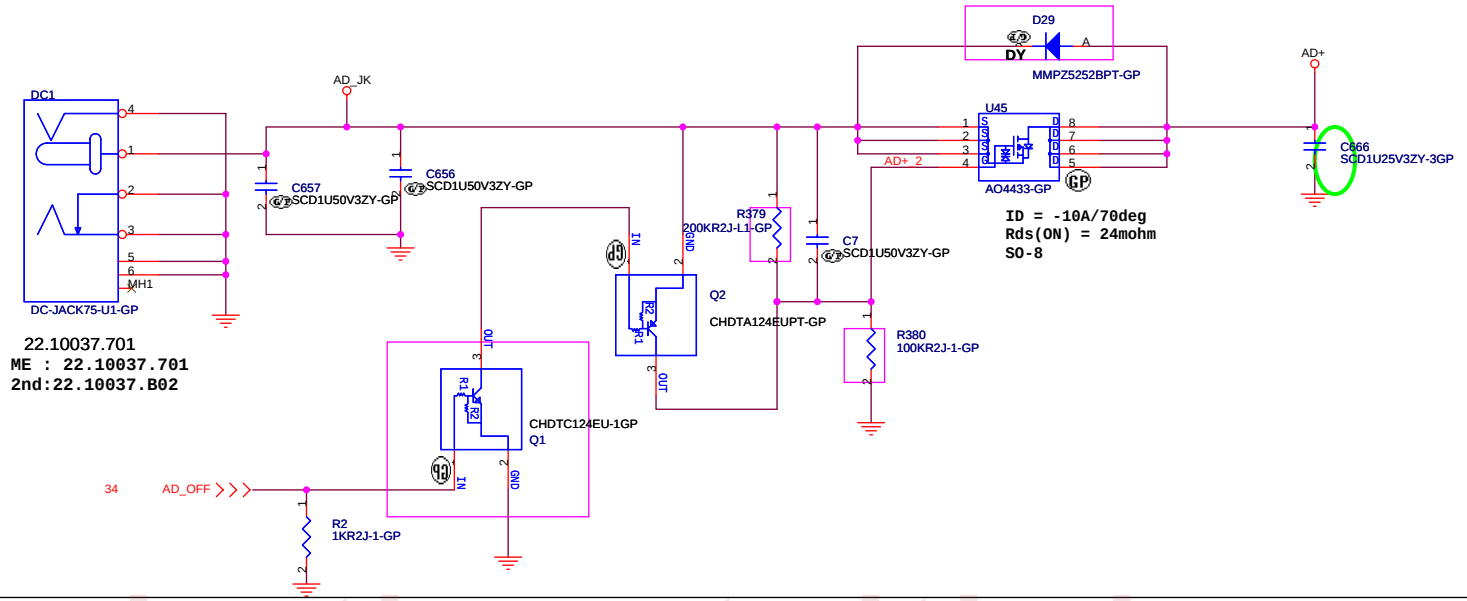
Title: TPS5130 1D2V/1D8V2D5V/ (2/2)

Size	Document Number	Rev
A3	Bolsena-E	SA

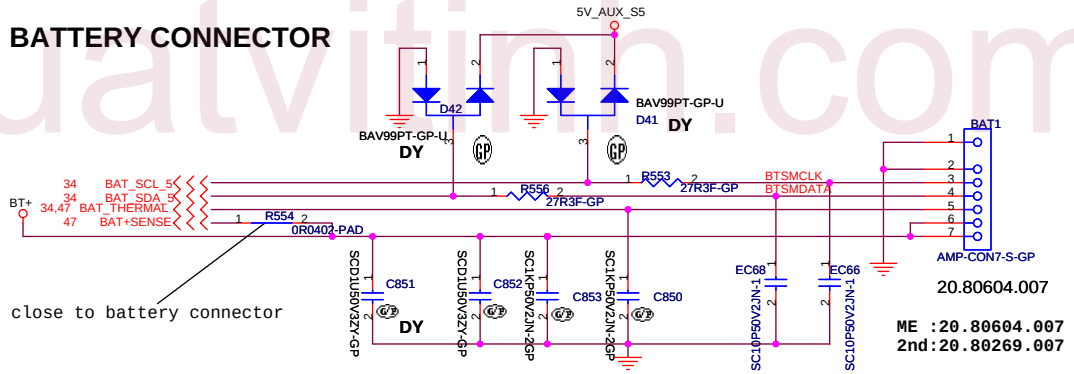
Date: Thursday, October 13, 2005 Sheet 46 of 58


AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
ACOK is 17.8V
V (MODE) >=2.8V = 4Cell
V (MODE) =1.8V = 3Cell
Icharge=3.2A
Icharge=3.5A
Pre charge=0.3A
CELL is 4 Cell
Icharge=1.4A
From KBC
From Battery Connector
From Battery Connector
Close to MAX1909 pin 24
Near MAX1909 Pin 2
Near MAX1909 Pin 21
For EMI
Rx
Rx
I Source = 4.5A ---> V (IINP) = 2.7V
I Source = 3.42A ---> V (IINP) = 2.05V
V_REF :4.2235V (<500uA)
90W ADAPTER
ISOURCE_MAX = (0.075/Rx)*(VCLS/VREF)
TOTAL_POWER :
Adapter=90W,Total_Power=79.7W
-1 0302
(Power Team)
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER MAX8725
Size Custom
Document Number
Bolsena-E
Rev
SA
Date: Thursday, October 13, 2005
Sheet 47 of 58

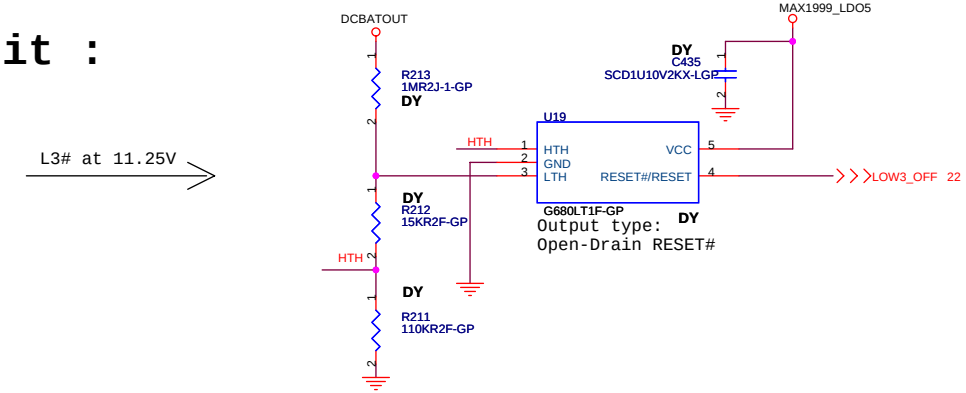
Adaptor in to generate DCBATOUT

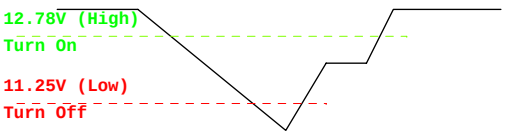


BATTERY CONNECTOR



Low3 Circuit :

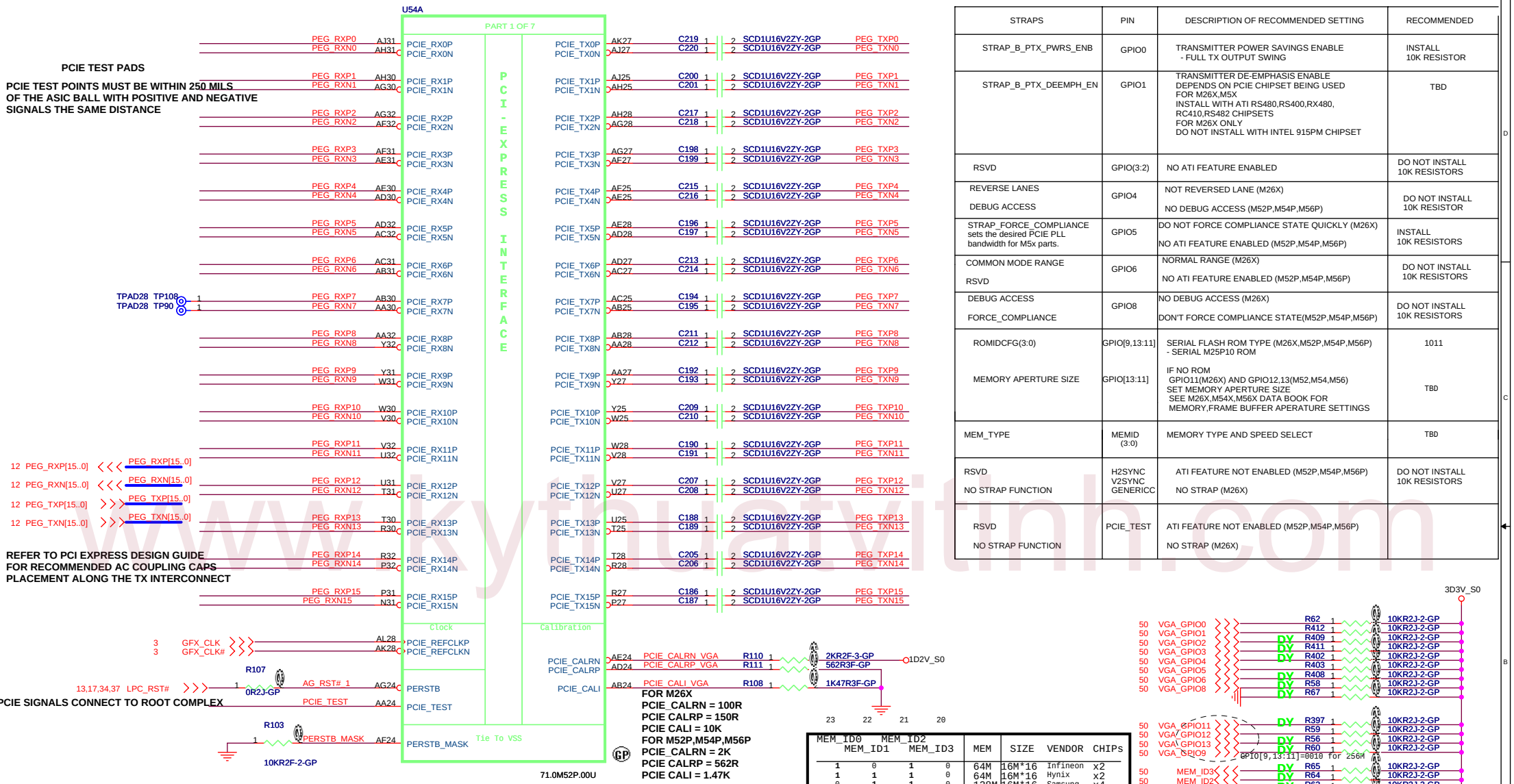




<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 48 of 58	



STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE DEPENDS ON PCIE CHIPSET BEING USED FOR M26X,M5X INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS FOR M26X ONLY DO NOT INSTALL WITH INTEL 915PM CHIPSET	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NOT REVERSED LANE (M26X) NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE sets the desired PCIE PLL bandwidth for M5x parts.	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	INSTALL 10K RESISTORS
COMMON MODE RANGE RSVD	GPIO6	NORMAL RANGE (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	NO DEBUG ACCESS (M26X) DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO[9,13:11] GPIO[13:11]	SERIAL FLASH ROM TYPE (M26X,M52P,M54P,M56P) - SERIAL M25P10 ROM IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE SEE M26X,M54X,M56X DATA BOOK FOR MEMORY,FRAME BUFFER APERATURE SETTINGS	1011 TBD
MEM_TYPE	MEMID (3:0)	MEMORY TYPE AND SPEED SELECT	TBD
RSVD NO STRAP FUNCTION	H2SYNC V2SYNC GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	DO NOT INSTALL 10K RESISTORS
RSVD NO STRAP FUNCTION	PCIE_TEST	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	

MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3	MEM	SIZE	VENDOR	CHIPs
1	0	1	0	64M	16M*16	Infineon	x2
1	1	1	0	64M	16M*16	Hynix	x2
0	1	1	0	128M	16M*16	Samsung	x4
0	0	1	0	256M	32M*16	Samsung	x4
0	1	0	0	128M	16M*16	Infineon	x4
1	1	0	0	256M	32M*16	Infineon	x4
1	0	0	0	128M	16M*16	Hynix	x4
0	0	0	0	256M	32M*16	Hynix	x4

When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the frame buffer aperture size.
GPIO[13:12] = 00: 128M frame buffer, same as ROM strap 00
GPIO[13:12] = 01: 256M frame buffer, same as ROM strap 01
GPIO[13:12] = 10: 64M frame buffer, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M5X-P PCIE 1/4
Size: A3 | Document Number: AG1 | Rev: SA
Date: Thursday, October 13, 2005 | Sheet 49 of 58

[USE ICS MK1726-08]

adjust SWING at 1.2v

Modulation Rate		
SEL1	SEL0	Center Spread
L	L	+-0.5%
L	H	+-1.0%
H	L	+-1.5%
H	H	No Spread

DVPCNTL,DVPDATA[23..0] ARE CONFIGURED FOR +3.3V SIGNALING MODE ON THIS DESIGN

FOR M26X
CONNECT TO +1.8V OR VSS
TO DEFINE DVO SIGNAL LEVEL
FOR M52P,M54P,M56P
NOT CONNECTED

ANY UNUSED GPIO CAN OPTIONALLY BE PANEL TYPE CONFIG STRAPS

ANY UNUSED GPIO CAN OPTIONALLY BE MEMORY TYPE CONFIG STRAPS

PLACE VREF DIVIDER AND CAP CLOSE TO ASIC

FOR M26X PVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

FOR M26X MPVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO VDDC

VOLTAGE DIVIDER 3.3V MEM SS MODOUT TO 1.2V XTALIN/OUT

adjust SWING at 1.2v

U54B PART 2 OF 7

VIDEO & MULTIMEDIA

Expand GPIO

VIP Host/External TMDS

Integrated TMDS

DAC / CRT

DAC2 (TV/CRT)

Monitor Interface

General Purpose I/O

Thermal Diode

PLL & XTAL

Test

ROM

External SSC

LVDS PLL and I/O GND

Placed close to ASIC end.

DUAL LINK IS ONLY SUPPORTED ON M56P
DO NOT CONNECT TXM,P[3:5] WITH M52P,M54P,M26X

FOR M26X TPVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

FOR M26X TXVDDR
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

FOR M26X AVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

FOR M26X VDD1DI
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

DAC2 CAN BE TV SIGNALS OR SECONDARY CRT SIGNALS AS CONTROLLED BY AN INTERNAL MUX

FOR M26X A2VDDQ
CONNECT TO +1.8V
FOR M52P,M54P,M56P
IT IS NO CONNECT

FOR M26X VDD2DI
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

For CRT

For DVI

For THERMAL SENSOR

FOR M26X GENERICC
NO CONNECT OR
EXT SPREAD SPECTRUM INPUT
FOR M52P,M54P,M56P
IT IS GPIO

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M5X-P IO 2/4

Size: A3 | Document Number: Bolsena-E | Rev: SA

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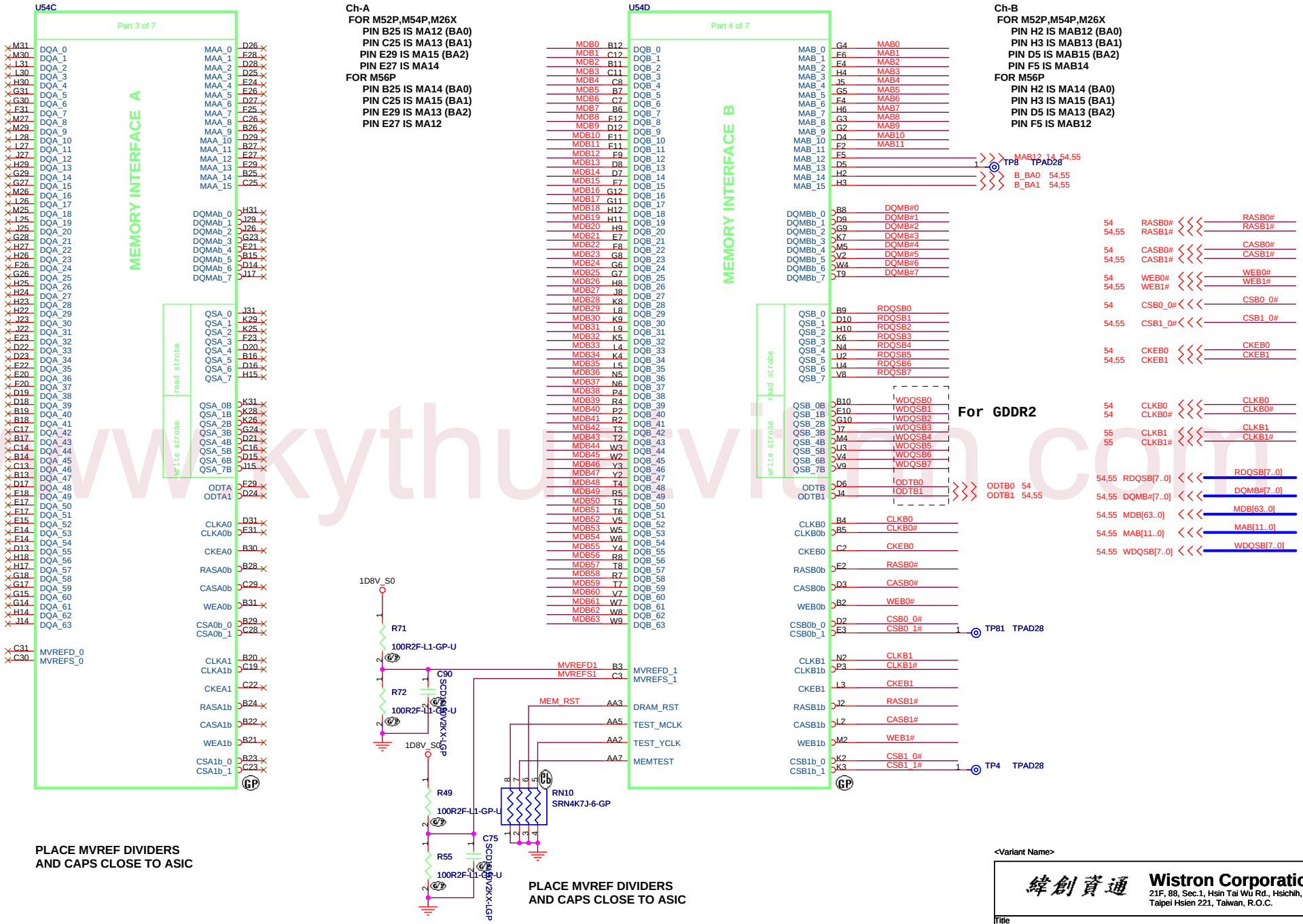
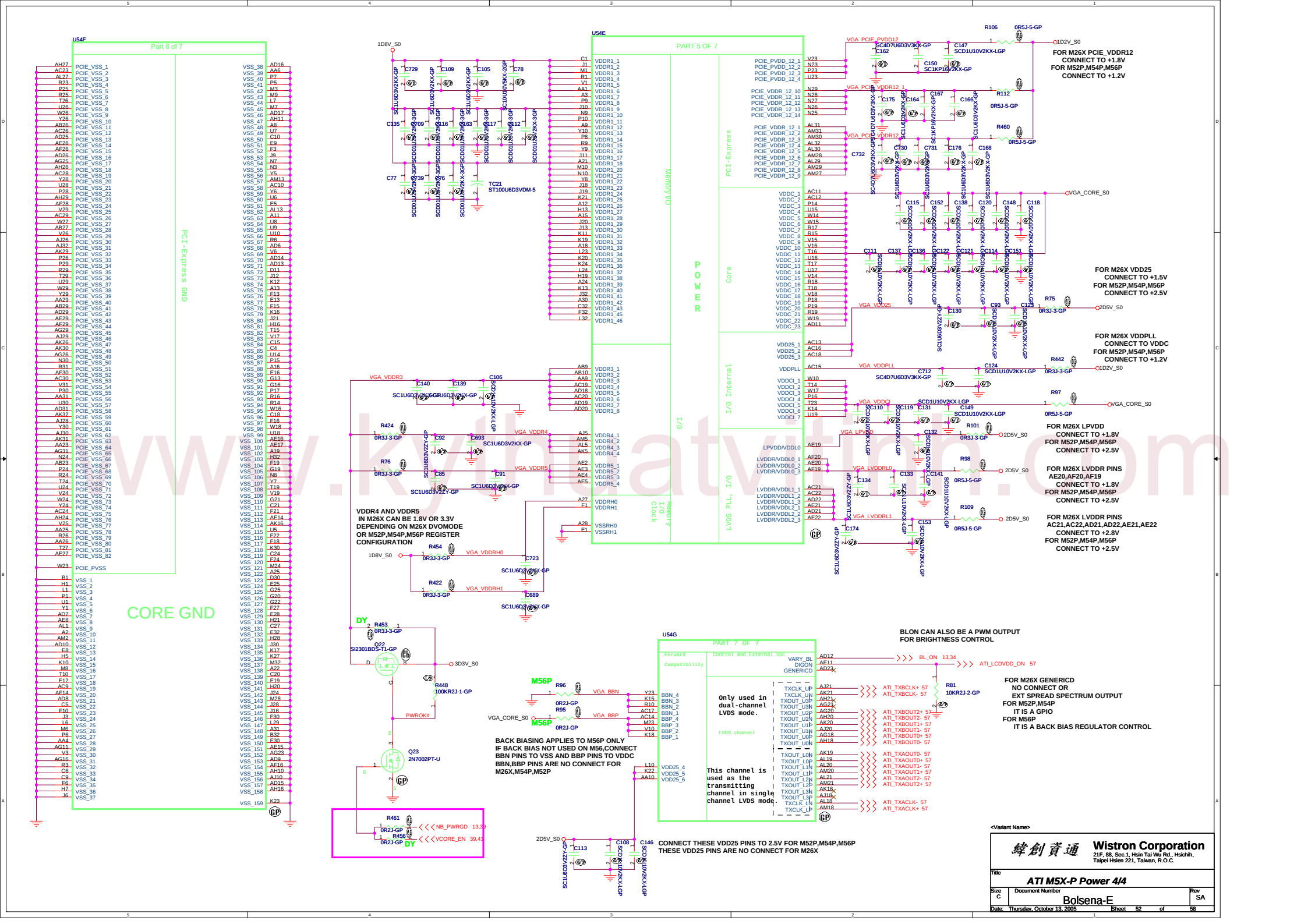
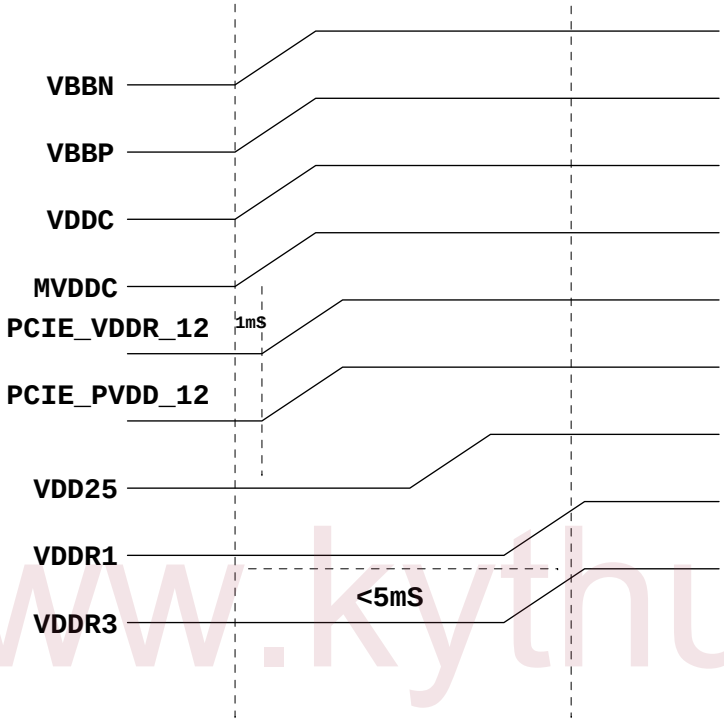
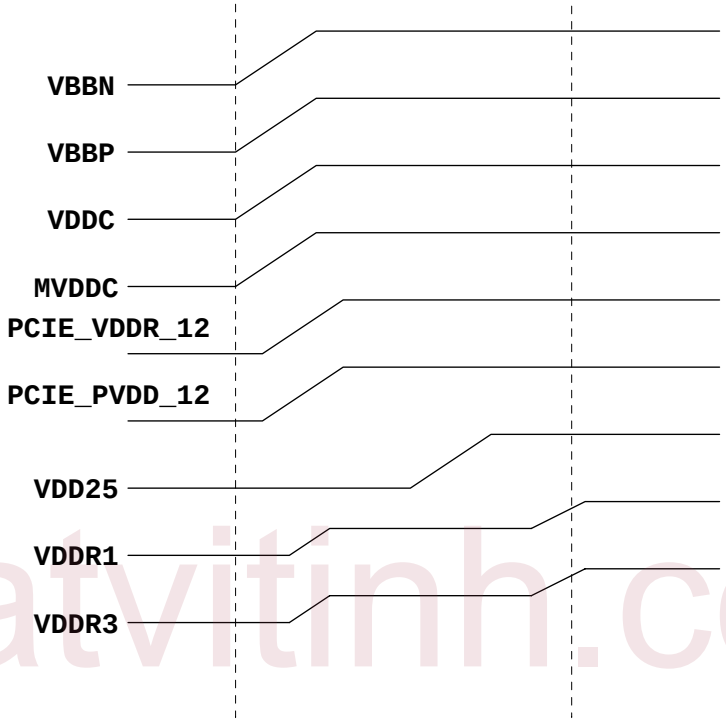




Ideal Power Up Sequence



Real Power Up Sequence



RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

General Guidelines:
- **BBN and BBP must ramp up before or at the same time as VDDC but not after.**
- **VDDC and MVDDC must be ramped up first, followed by PCIE_VDDR_12, PCIE_PVDD12, VDD25, VDDR1 and VDDR3 (and other I/O powers).**
- **All powers must be ramped up within 5ms of each other (from the ramp of VDDC to 90% of VDDR3).**
- **VDD25 can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.**
- **The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD25 ->VDDC/MVDDC/BBN/BBP.**

Due to the level shifter design in the memory I/Os, in order to avoid over-stressing the thin oxide transistors when VDDR1 is powered on but VDDC is not, VDDC must ramp up before VDDR1. Similarly, VDDC must ramp up before VDDR3. The level shifter design is a function of the transistor types used in 90nm technology and of the voltage level support. The drawback of ramping up VDDC before the I/O voltages (such as VDDR1 and VDDR3) is that parasitic P/N junctions are forward biased, thus creating a conduction path. These conduction paths will pump up VDDR1 (from the memory IOs) and VDDR3 (from the GPIOs).

The real power up sequence will appear as follows:

Figure 2-2. Real Power Up Sequence

As long as MVDDC ramps up with VDDC, the pump voltage on VDDR1 should be all right since the DRAM spec will not be violated.

CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M5X-P POWER SEQUENCE

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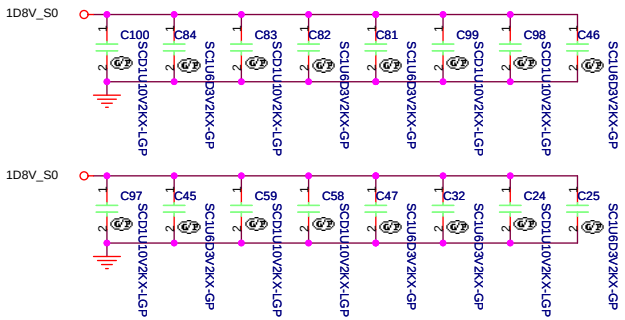
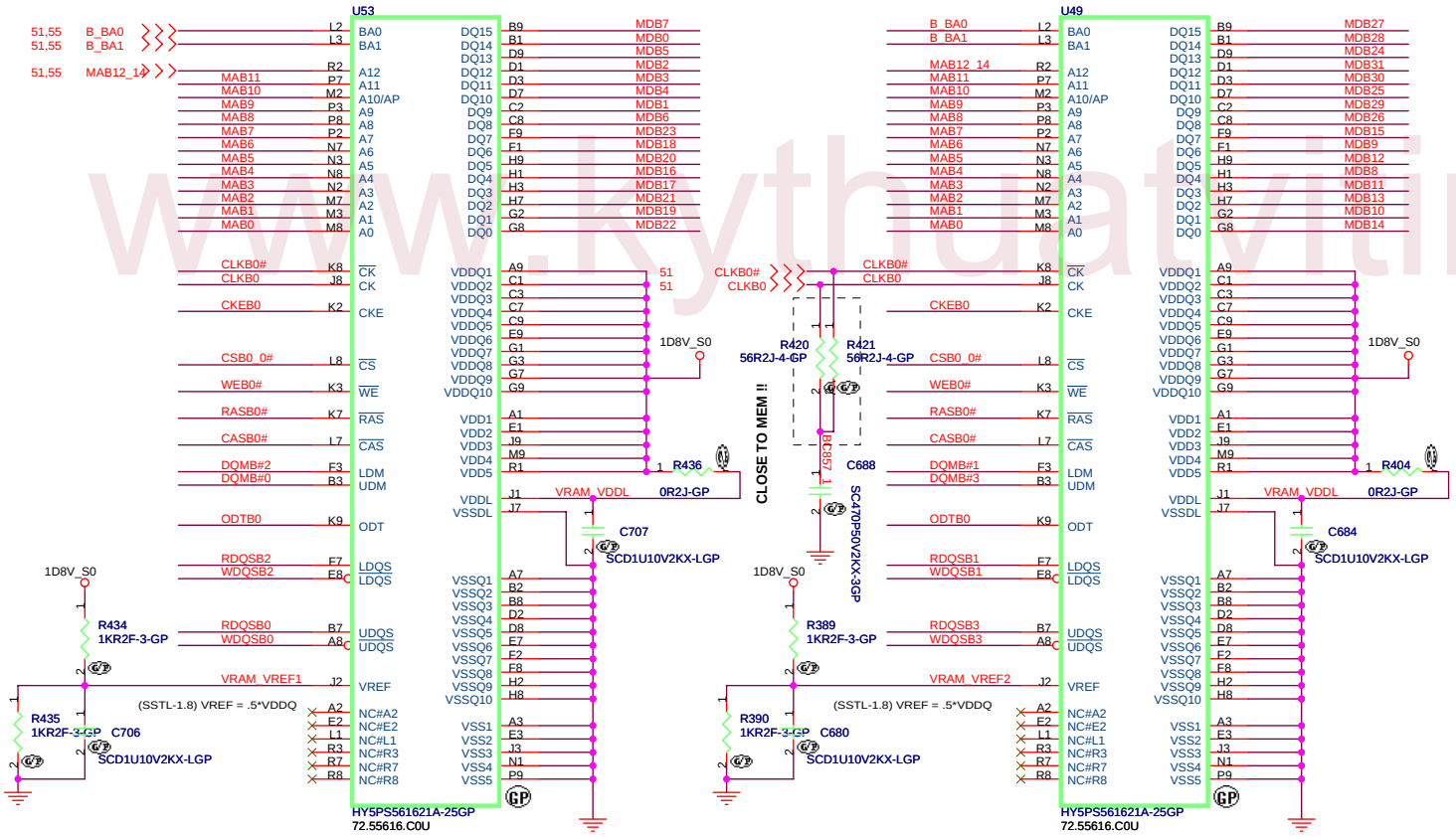
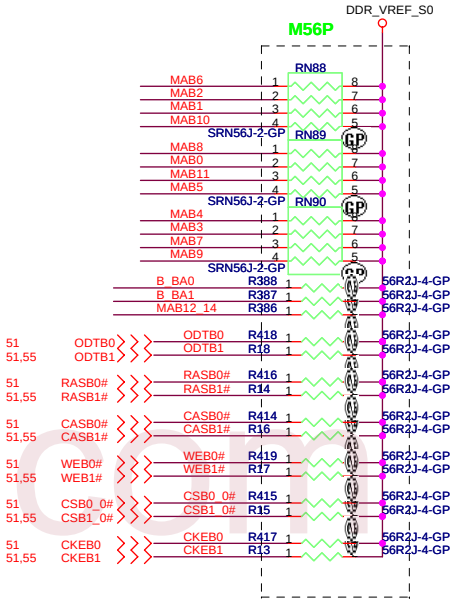
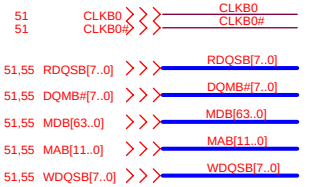
CHAN B DDR2 84BGA 32MX16 MEMORY







FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP TO A VTT RAIL (50% OF VDDQ)



72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGA(16M*16, 400Mhz)
72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M*16, 400Mhz)

<Variant Name>

緯創資通 **Wistron Corporation**
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Title: **VRAM 1/2**

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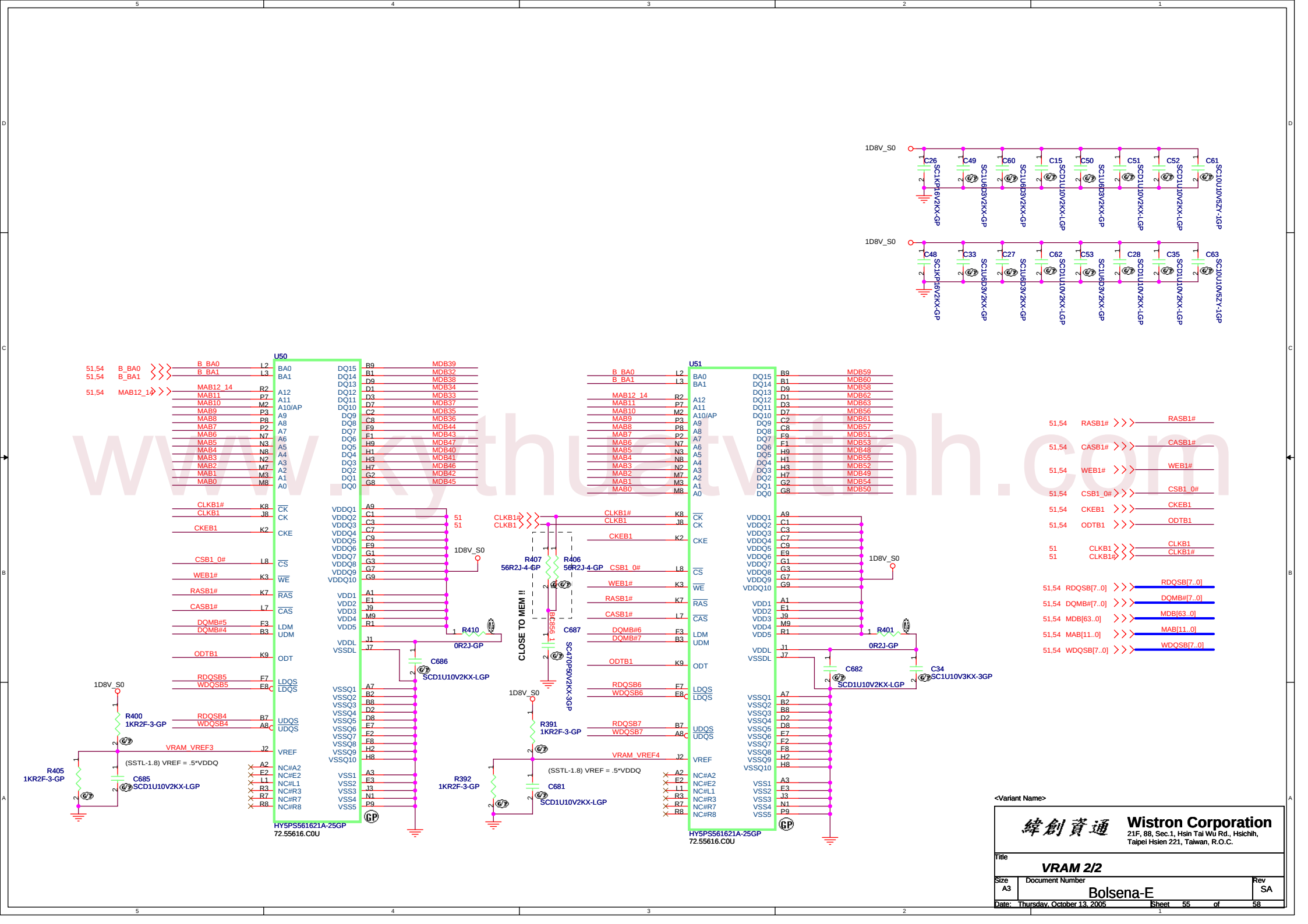

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM 2/2**

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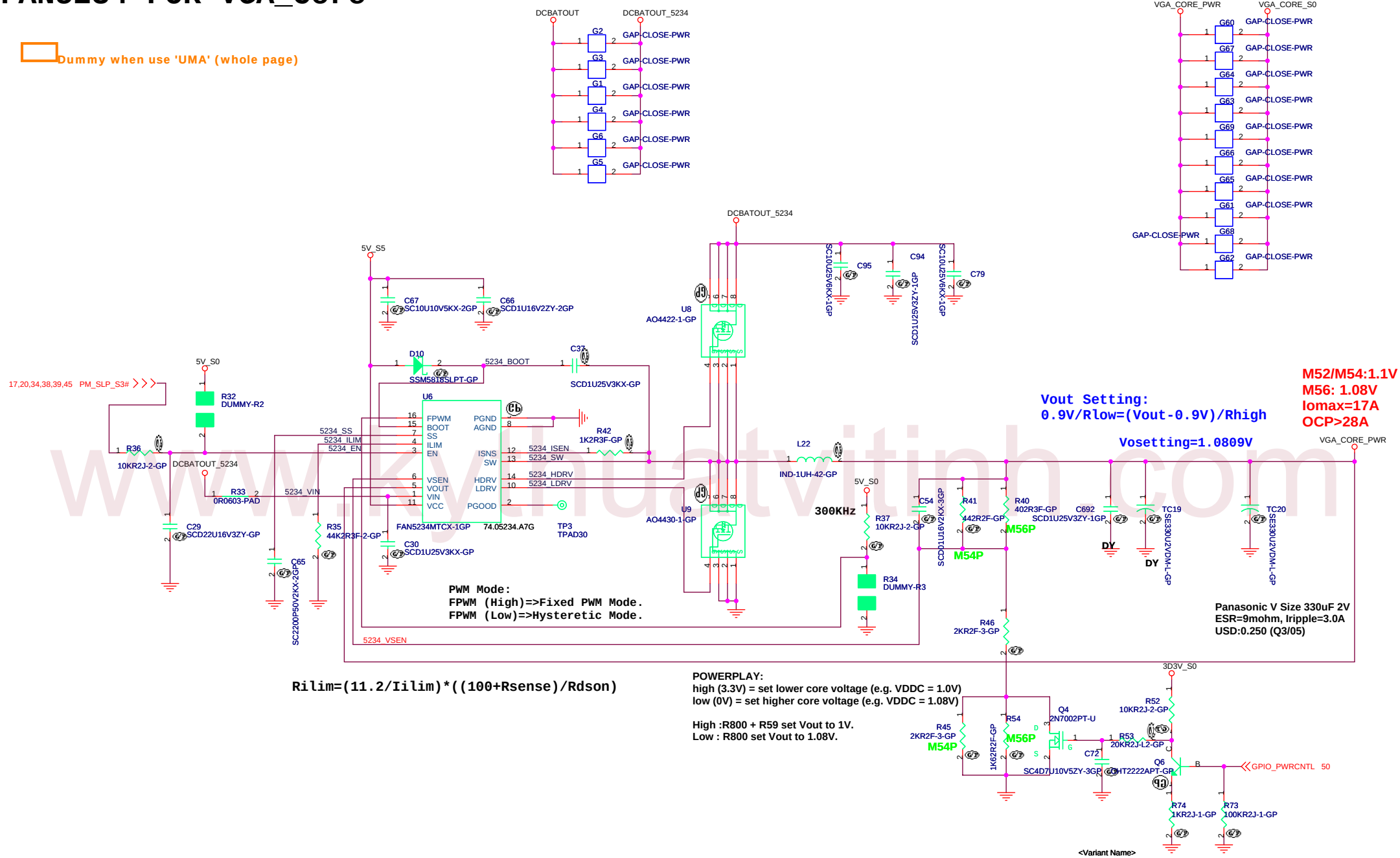
FAN5234 FOR VGA_Core

Dummy when use 'UMA' (whole page)



<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	VGA CORE 1D1V	
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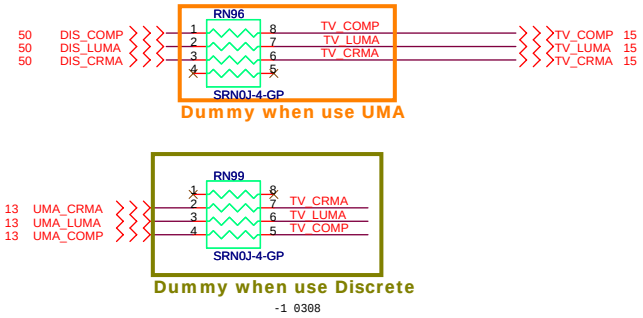
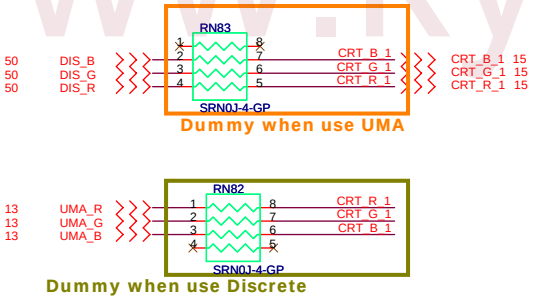
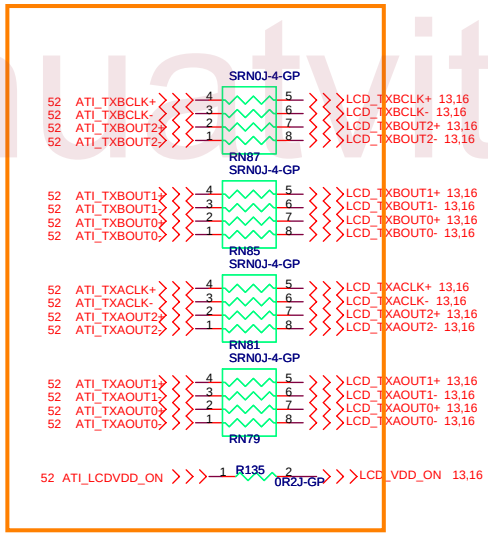
TV SWITCH

Function	S
A to B0	L
A to B1	H







<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA SELECTOR

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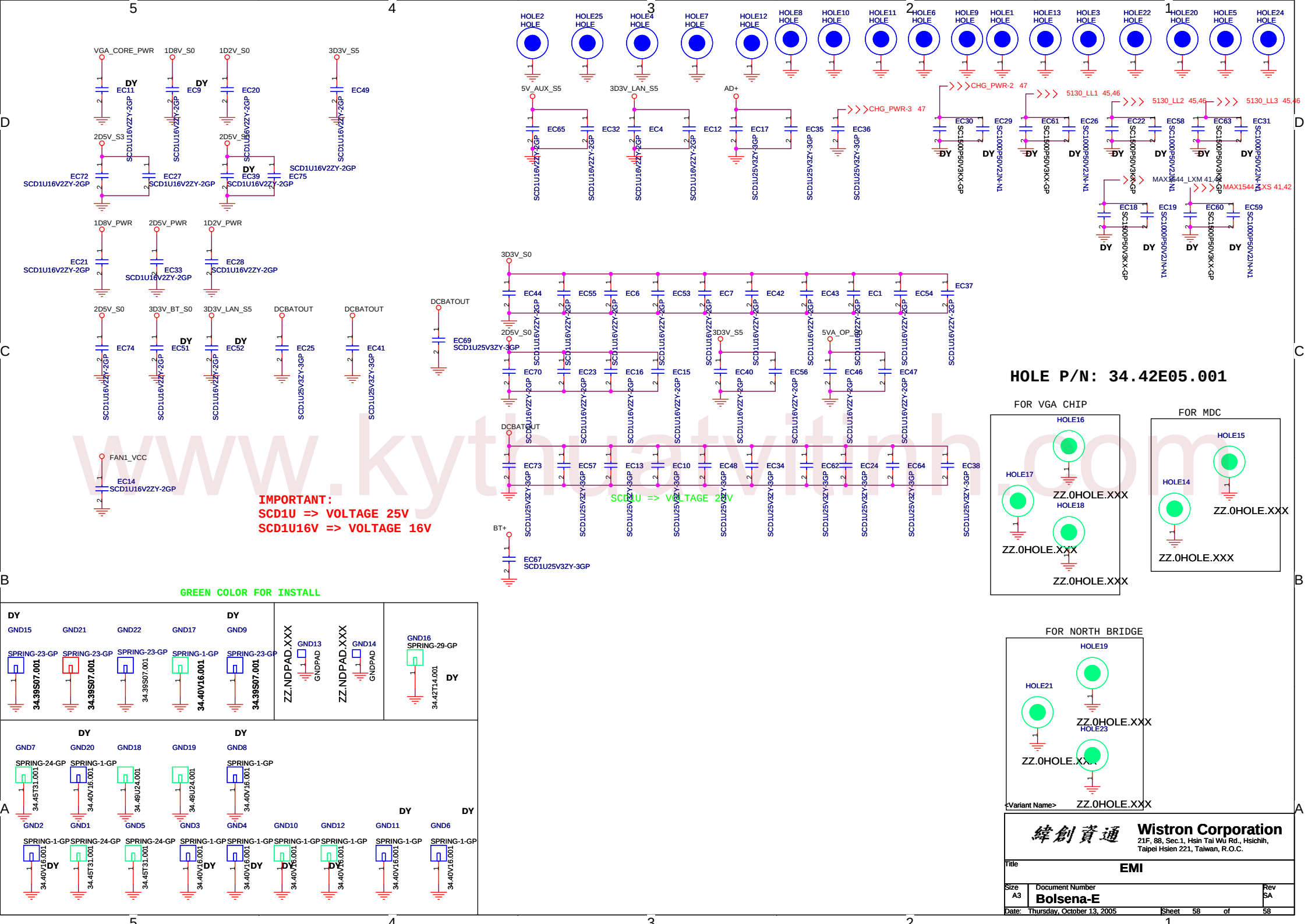
VGA_CORE_PWR
1D8V_S0
1D2V_S0
3D3V_S5
EC11
EC9
EC20
EC49
SCD1U16V2ZY-2GP
2D5V_S3
2D5V_S5
EC72
EC27
EC39
EC75
EC74
EC51
EC52
EC25
EC41
EC69
EC14
FAN1_VCC
DCBATOUT
3D3V_BT_S0
3D3V_LAN_S5
1D8V_PWR
2D5V_PWR
1D2V_PWR
EC21
EC33
EC28
HOLE2 HOLE
HOLE25 HOLE
HOLE4 HOLE
HOLE7 HOLE
HOLE12 HOLE
HOLE8 HOLE
HOLE10 HOLE
HOLE11 HOLE
HOLE6 HOLE
HOLE9 HOLE
HOLE1 HOLE
HOLE13 HOLE
HOLE3 HOLE
HOLE22 HOLE
HOLE20 HOLE
HOLE5 HOLE
HOLE24 HOLE
5V_AUX_S5
3D3V_LAN_S5
AD+
CHG_PWR-2 47
CHG_PWR-3 47
5130_LL1 45,46
5130_LL2 45,46
5130_LL3 45,46
MAX1544_LXM 41,42
MAX1544_LXS 41,42
EC65
EC32
EC4
EC12
EC17
EC35
EC36
EC30
EC29
EC61
EC26
EC22
EC58
EC63
EC31
EC18
EC19
EC60
EC59
3D3V_S0
2D5V_S0
3D3V_S5
5VA_OP
DCBATOUT
BT+
EC44
EC55
EC6
EC53
EC7
EC42
EC43
EC1
EC54
EC37
EC70
EC23
EC16
EC15
EC40
EC56
EC46
EC47
EC73
EC57
EC13
EC10
EC48
EC34
EC62
EC24
EC64
EC38
EC67
SCD1U25V3ZY-3GP
SCD1U25V2ZY-3GP
SCD1U16V2ZY-2GP
DY
IMPORTANT:
SCD1U => VOLTAGE 25V
SCD1U16V => VOLTAGE 16V
SCD1U => VOLTAGE 25V
HOLE P/N: 34.42E05.001
FOR VGA CHIP
FOR MDC
FOR NORTH BRIDGE
HOLE16
HOLE17
HOLE18
HOLE15
HOLE14
HOLE19
HOLE21
HOLE23
ZZ.0HOLE.XXX
<Variant Name>
GREEN COLOR FOR INSTALL
GND15
GND21
GND22
GND17
GND9
GND7
GND20
GND18
GND19
GND8
GND2
GND1
GND5
GND3
GND4
GND10
GND12
GND11
GND6
GND13
GND14
GND16
SPRING-23-GP
SPRING-1-GP
SPRING-24-GP
SPRING-29-GP
34.39S07.001
34.40V16.001
34.45T31.001
34.48U24.001
34.42T14.001
ZZ.NDPAD.XXX
GNDPAD
www.kythuatvitinh.com
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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