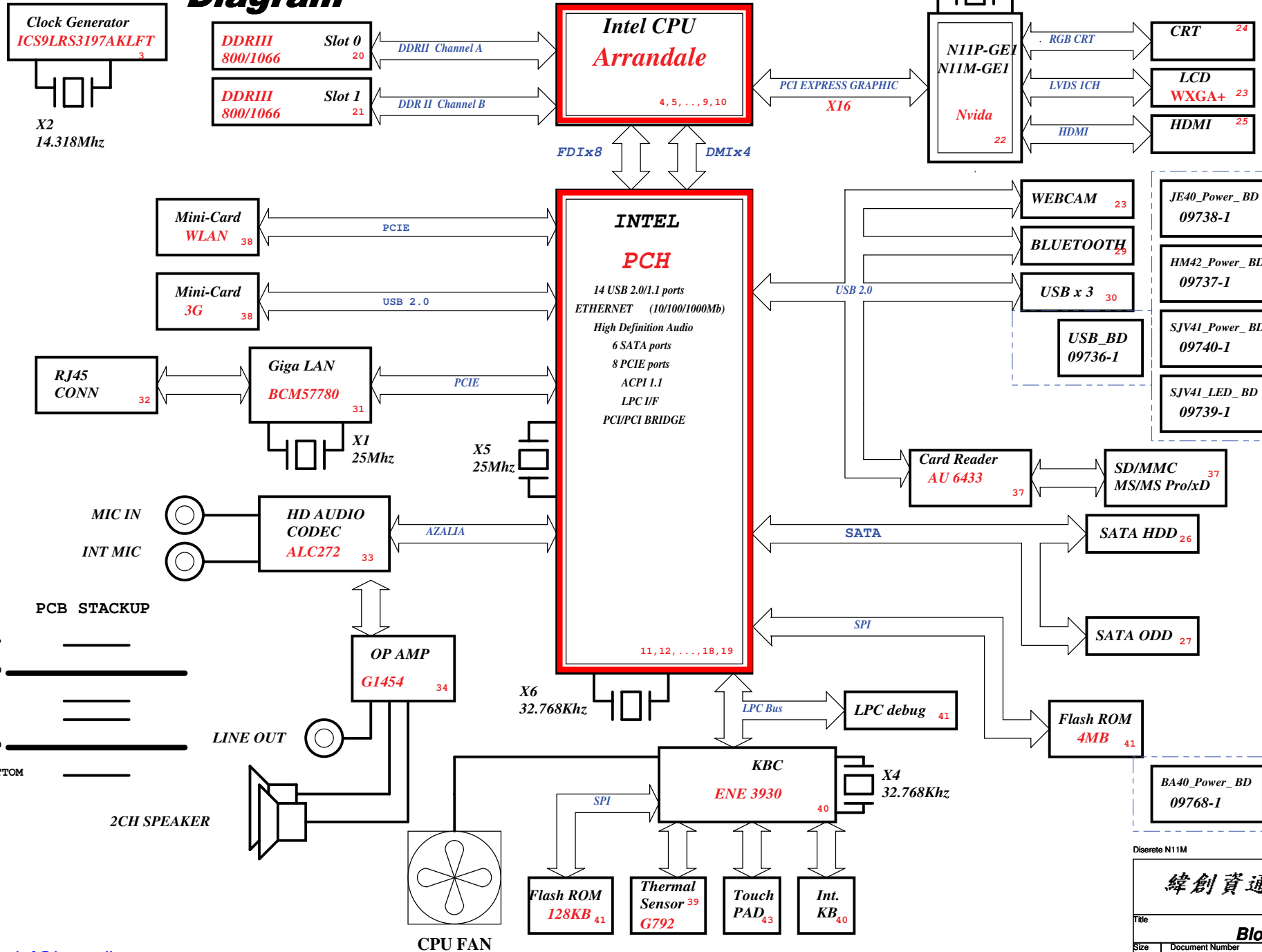


HM42-CP Block Diagram

PCB P/N : 48.4GW01.011
REVISION : -1 09920

Project code: 91.4GW01.001 (HM42-CP)
91.4GY01.001 (JE40-CP)
91.4GZ01.001 (SJV41-CP)
91.4JD01.001 (BA40-CP)



SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49
SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50
SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 1D05V_S0 51
SYSTEM DC/DC RT9025	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0 52
SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 55
SYSTEM DC/DC TPS5161	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 47, 48
CPU DC/DC ISL62882C	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47, 48
CHARGER ISL88731C	
INPUTS	OUTPUTS
DCBATOUT	BT+ 53

PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

USB Table

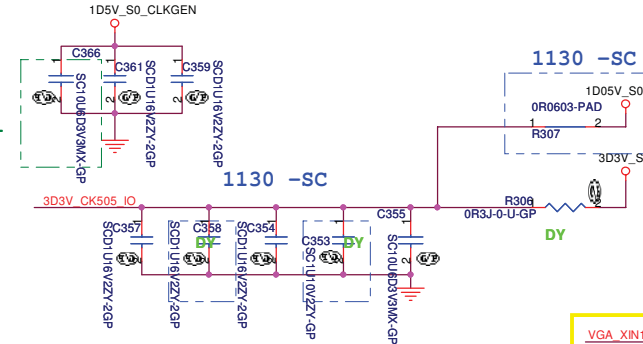
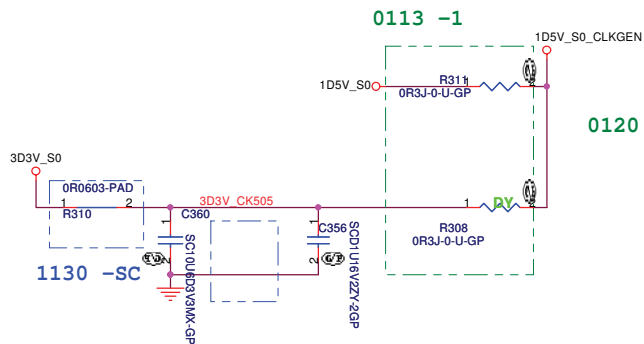
PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

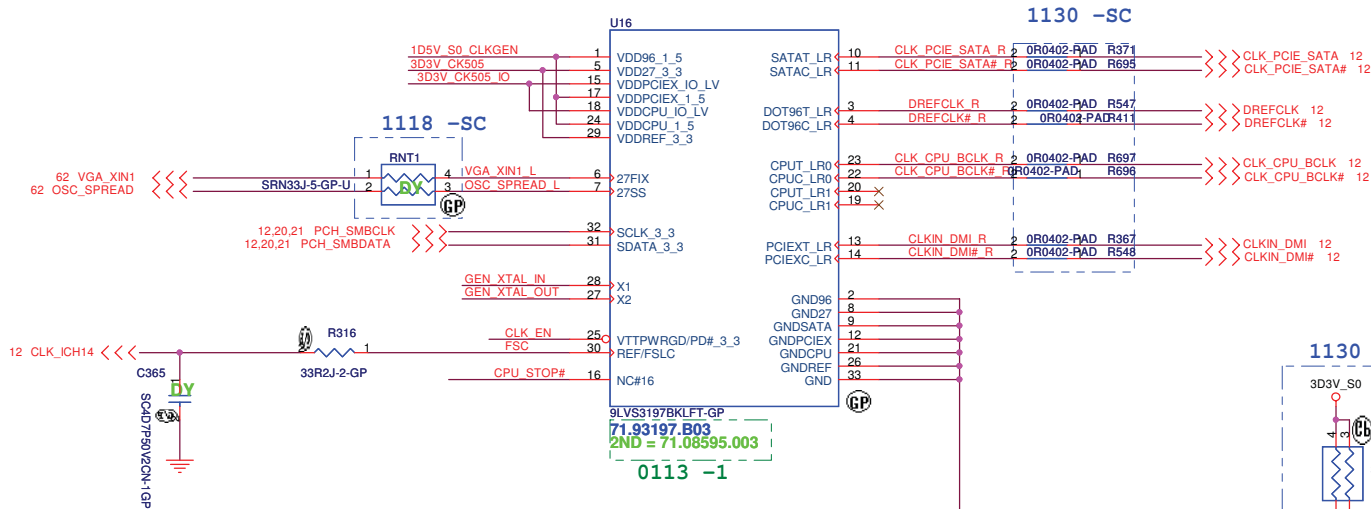
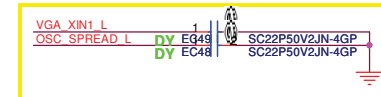
Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1 (HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

<Variant Name>

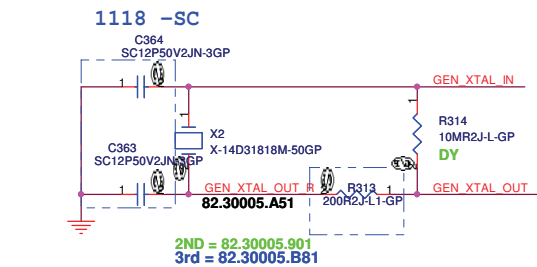
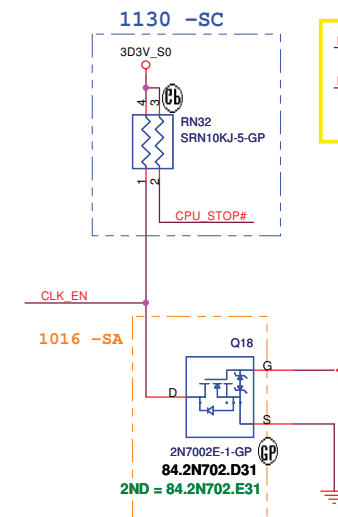
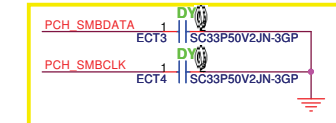
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Title			
Table of Content			
Size A3	Document Number HM42-CP	Rev SC	
Date: Friday, January 22, 2010	Sheet 2	of	72



SA 0622 EMI

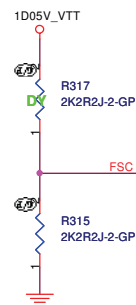


SA 0629 RF



SB 0813 $C_L = 10pF$
Freq tolerance: ± 30 ppm

FSC	0	1
SPEED	133MHz (Default)	100MHz



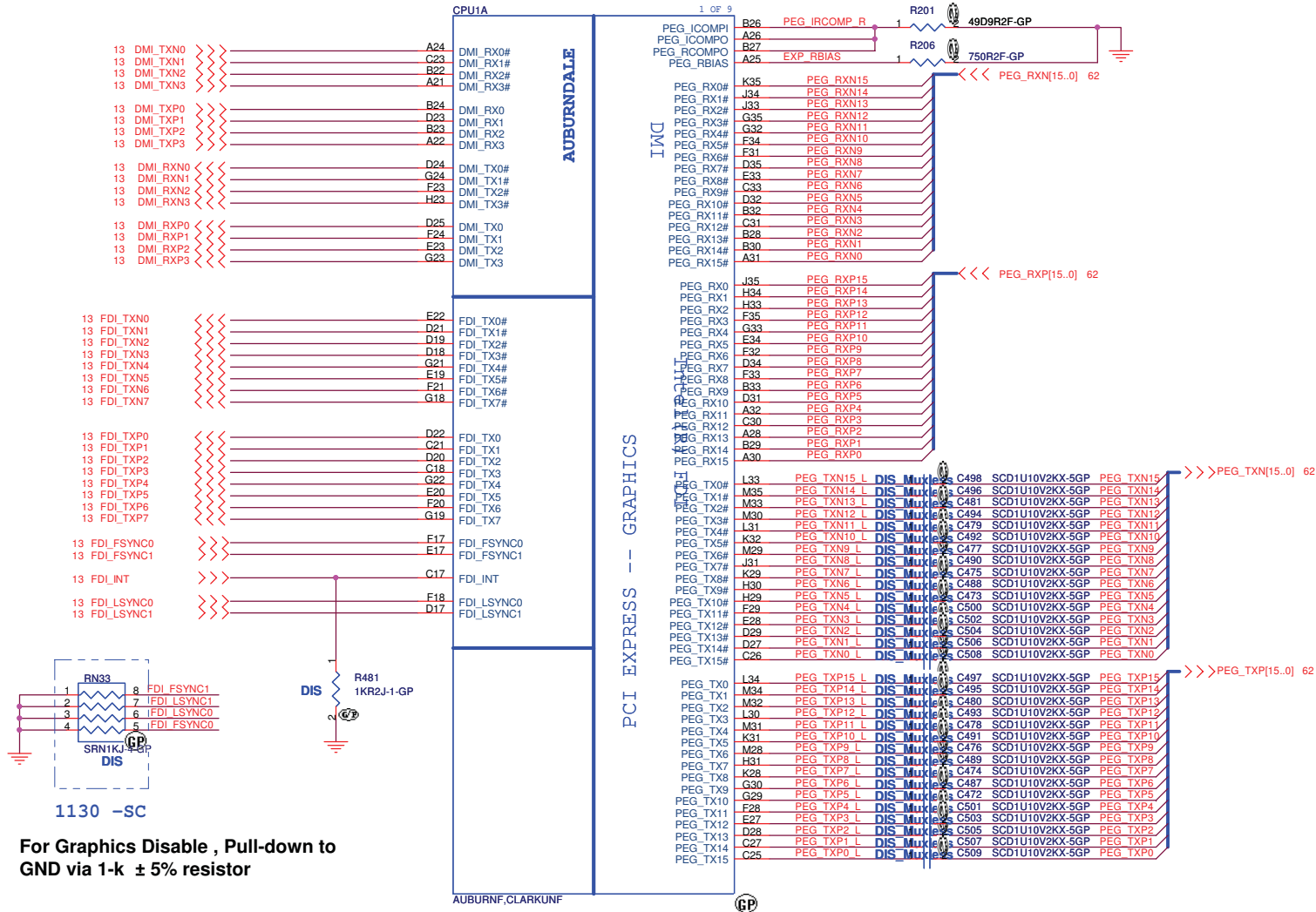
UMA

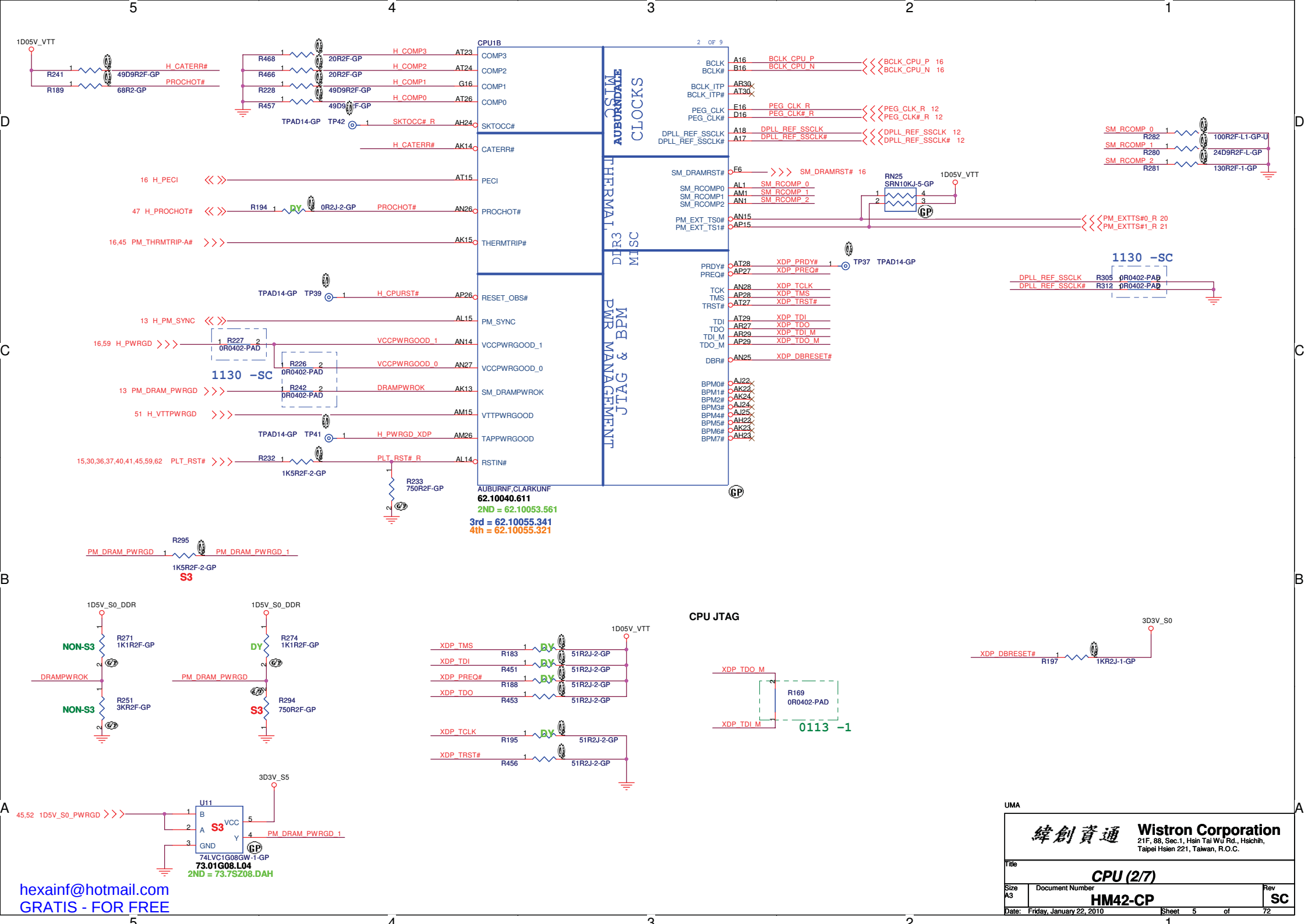
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator**

Size: A3 Document Number: **HM42-CP** Rev: **SC**

Date: Friday, January 22, 2010 Sheet 3 of 72





20 M_A_DQ[63..0] <<>>

20 M_A_BS0 <<>>
20 M_A_BS1 <<>>
20 M_A_BS2 <<>>

20 M_A_CAS# <<>>
20 M_A_RAS# <<>>
20 M_A_WE# <<>>

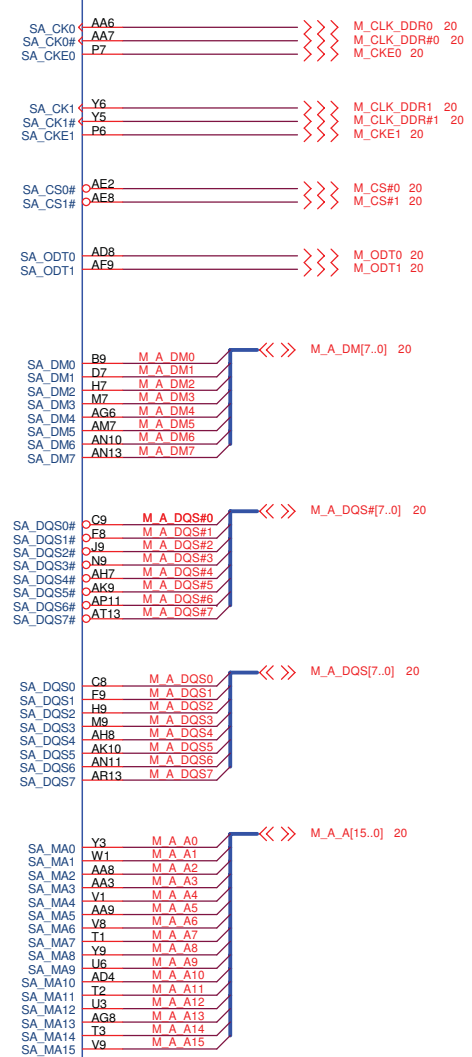
hexainf@hotmail.com
GRATIS - FOR FREE

CPU1C 3 OF 9

AUBURNDALE

DDR SYSTEM MEMORY A

3 OF 9



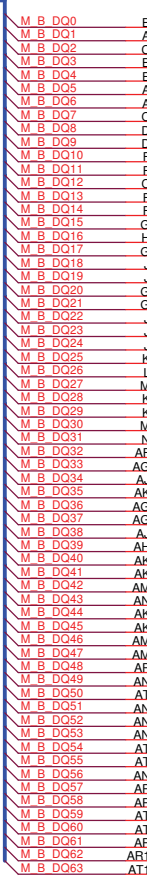
AUBURNF.CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321



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21 M_B_BS0 <<>>
21 M_B_BS1 <<>>
21 M_B_BS2 <<>>

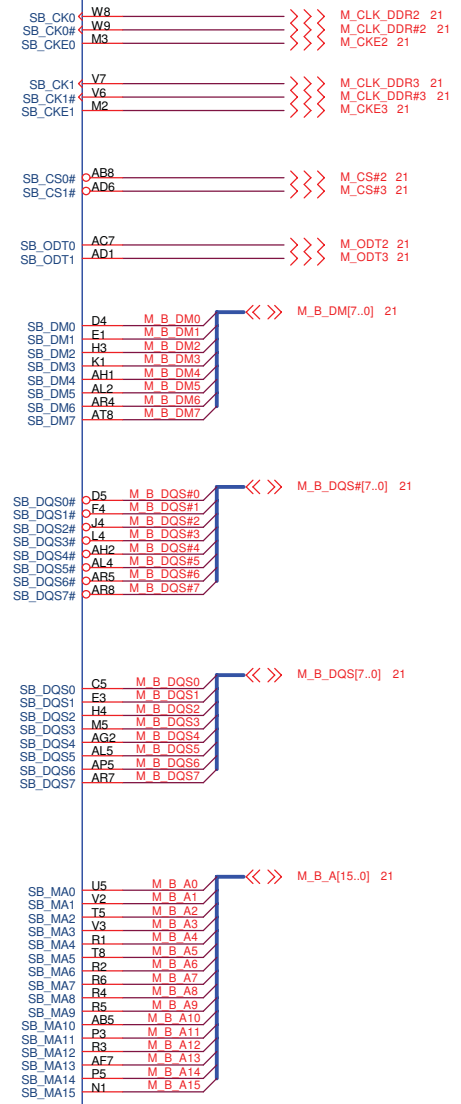
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21 M_B_RAS# <<>>
21 M_B_WE# <<>>



CPU1D 4 OF 9

AUBURNDALE

DDR SYSTEM MEMORY - B



AUBURNF.CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321

<Variant Name> GP

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (3/7)

Size

A3

Document Number

HM42-CP

Date

Friday, January 22, 2010

Rev

SC

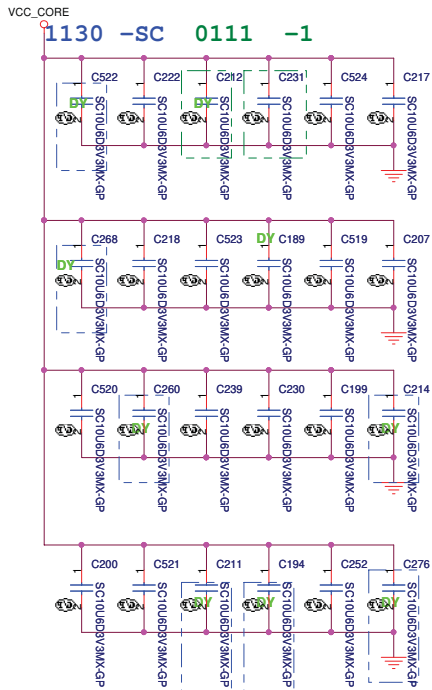
Sheet

6

of

72

PROCESSOR CORE POWER



VCC_CORE
48A

AG35
AG34
AG33
AG32
AG31
AG30
AG29
AG28
AG27
AG26
AF55
AF54
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R00

AUBURNDALE

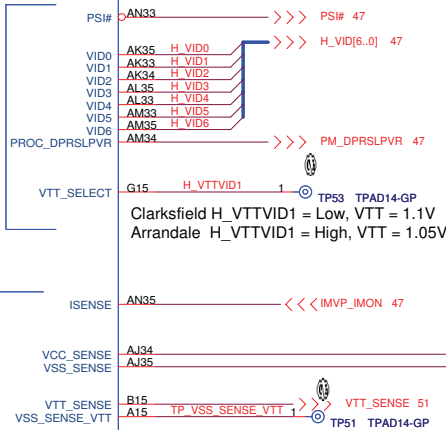
1.1V RAIL POWER

CPU CORE SUPPLY

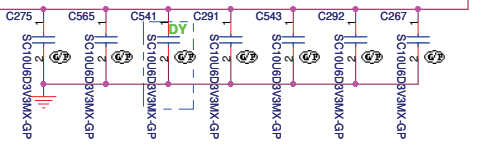
POWER

CPU VIDS

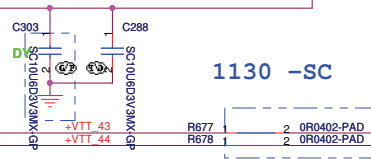
SENSE LINE



1130 -SC



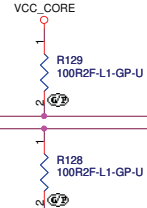
1130 -SC



1130 -SC

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

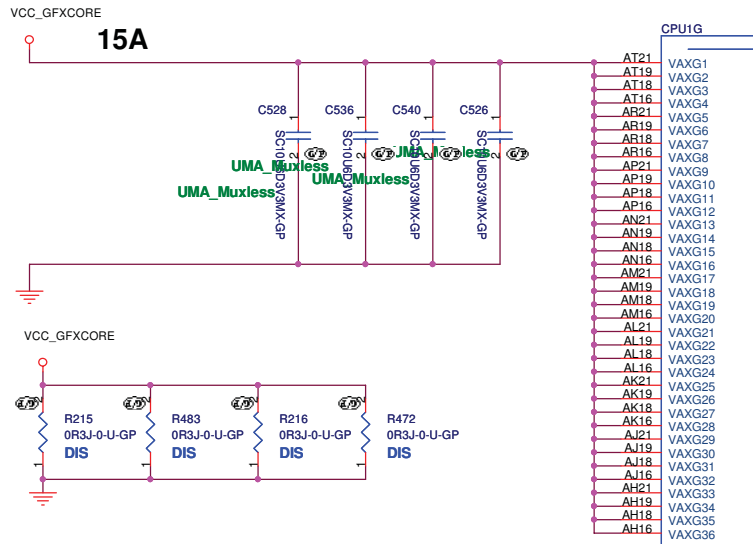
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



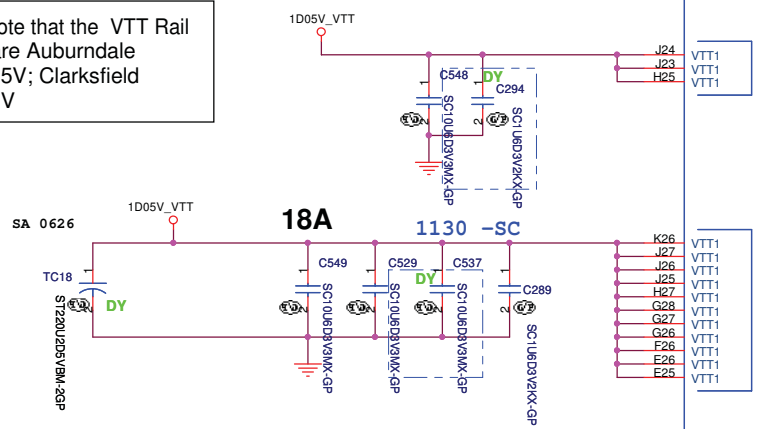
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title		CPU (4/7)	
Size	Document Number	Rev	SC
Custom	HM42-CP		
Date:	Friday, January 22, 2010	Sheet	7 of 72

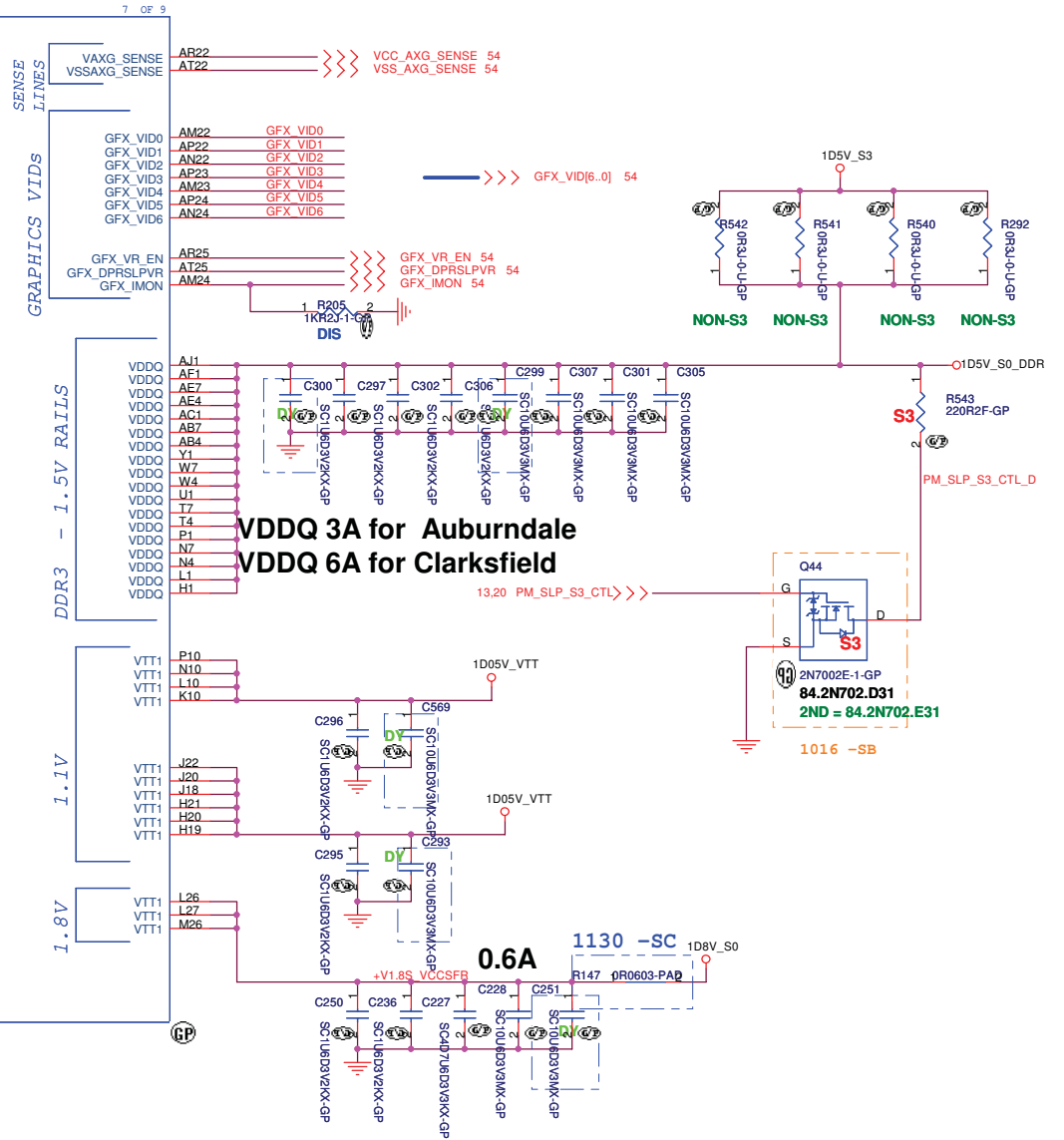


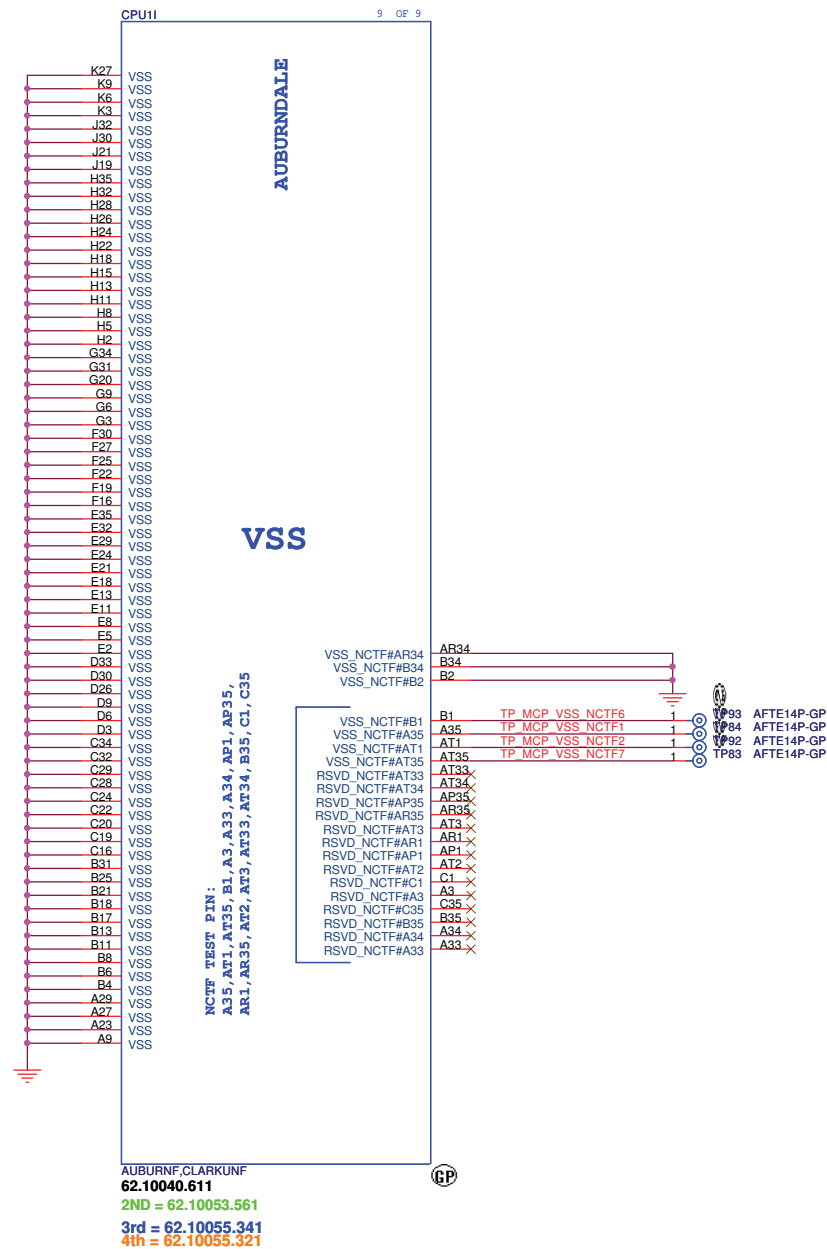
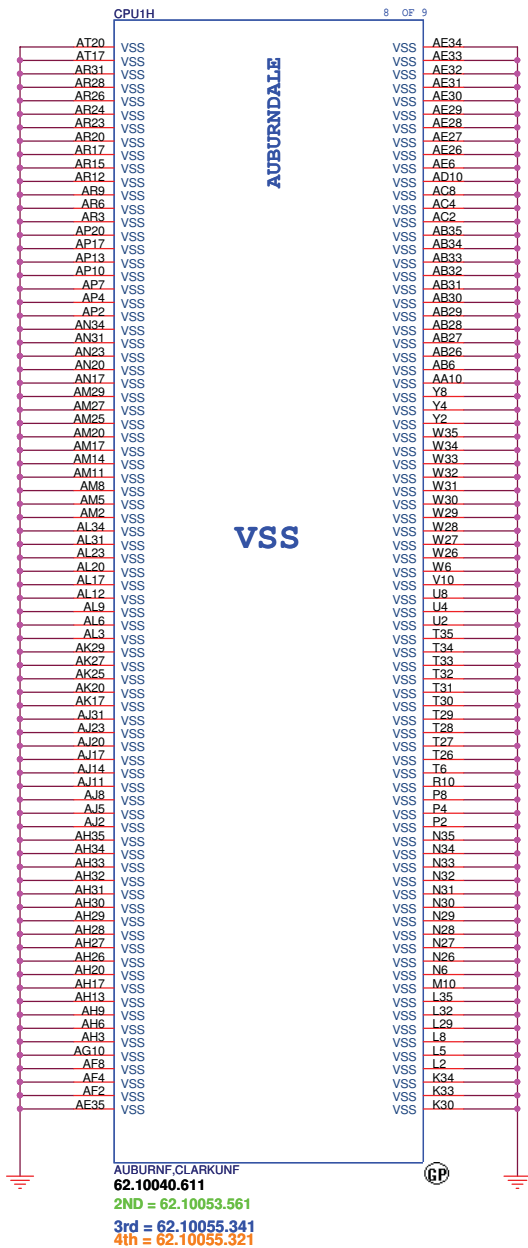
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V



AUBURN, CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321

AUBURNDALE **GRAPHICS** **POWER** **PEG & DMI**



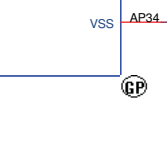
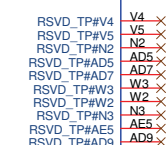
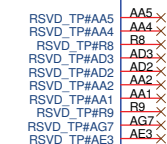
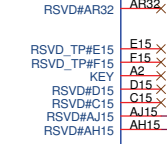
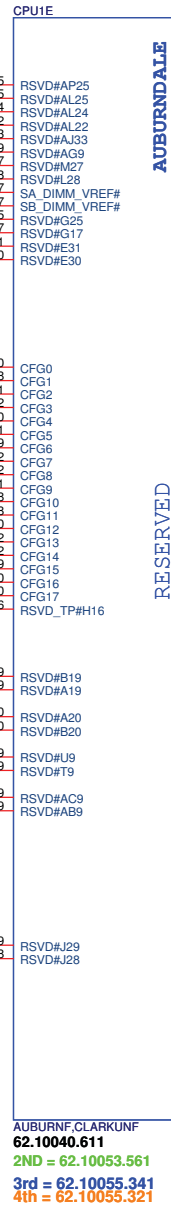
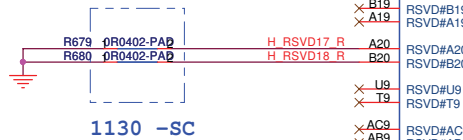
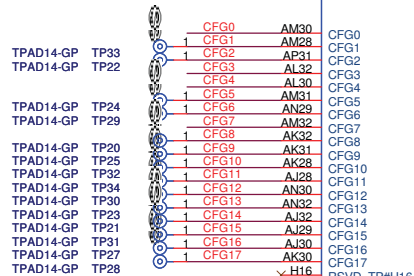
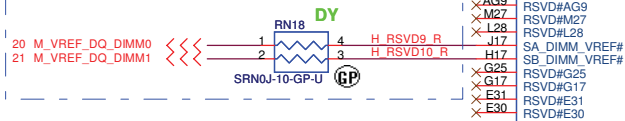


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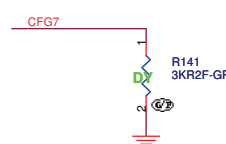
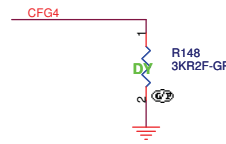
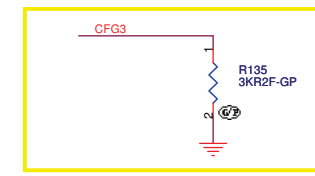
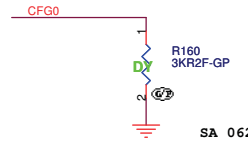
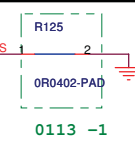
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU (6/7)		
Size	Document Number	Rev
A3	HM42-CP	SC
Date:	Friday, January 22, 2010	Sheet 9 of 72

SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



Processor Strapping

PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

<Variant Name>

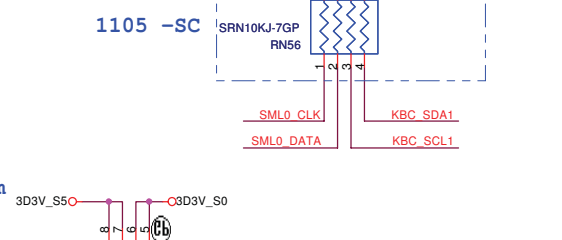
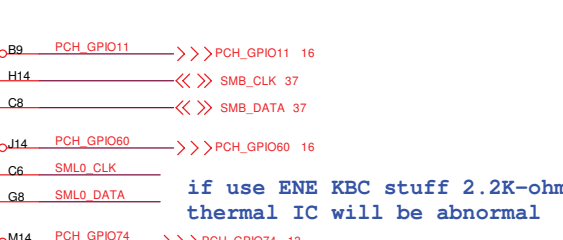
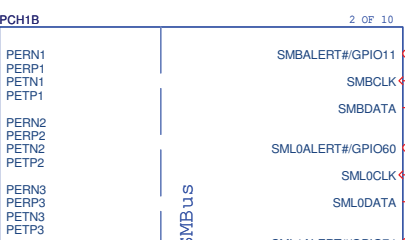
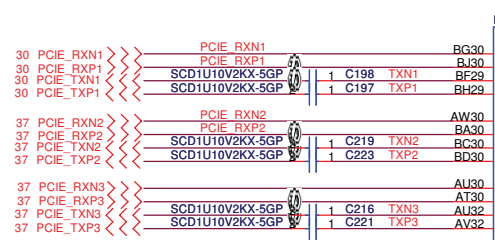
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (7/7)	
Size A3	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010	Sheet 10 of 72	

LAN

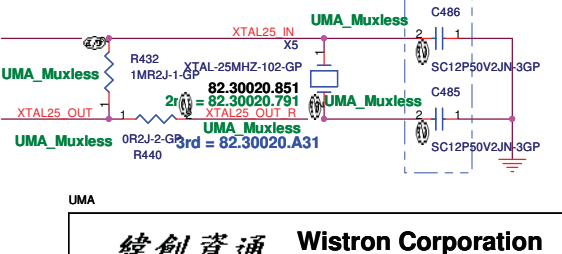
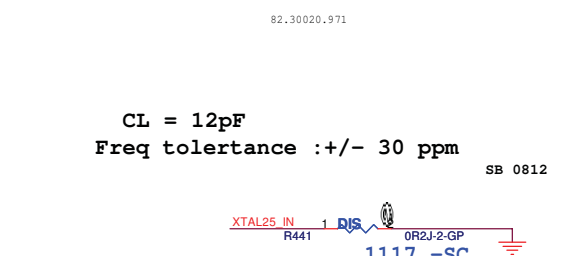
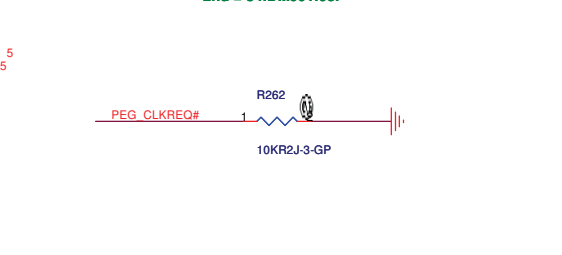
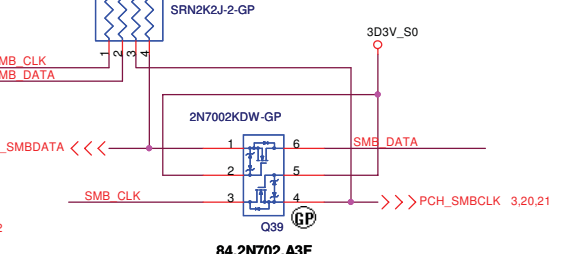
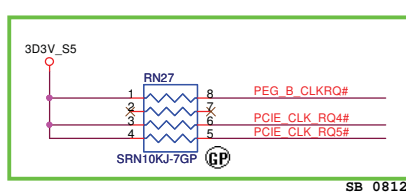
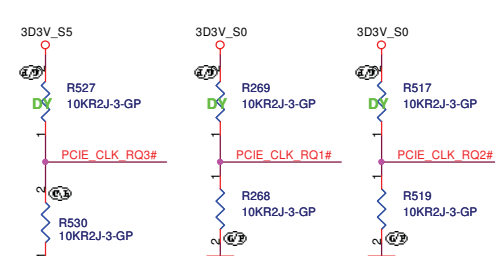
MINICARD1

MINICARD2



PCIECLKRQ[0,3,4,5,6,7] should have a 10K pull-up to +3VALW.

PCIECLKRQ[1,2] should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).



Wistron Corporation

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緯創資通

HM42-CP

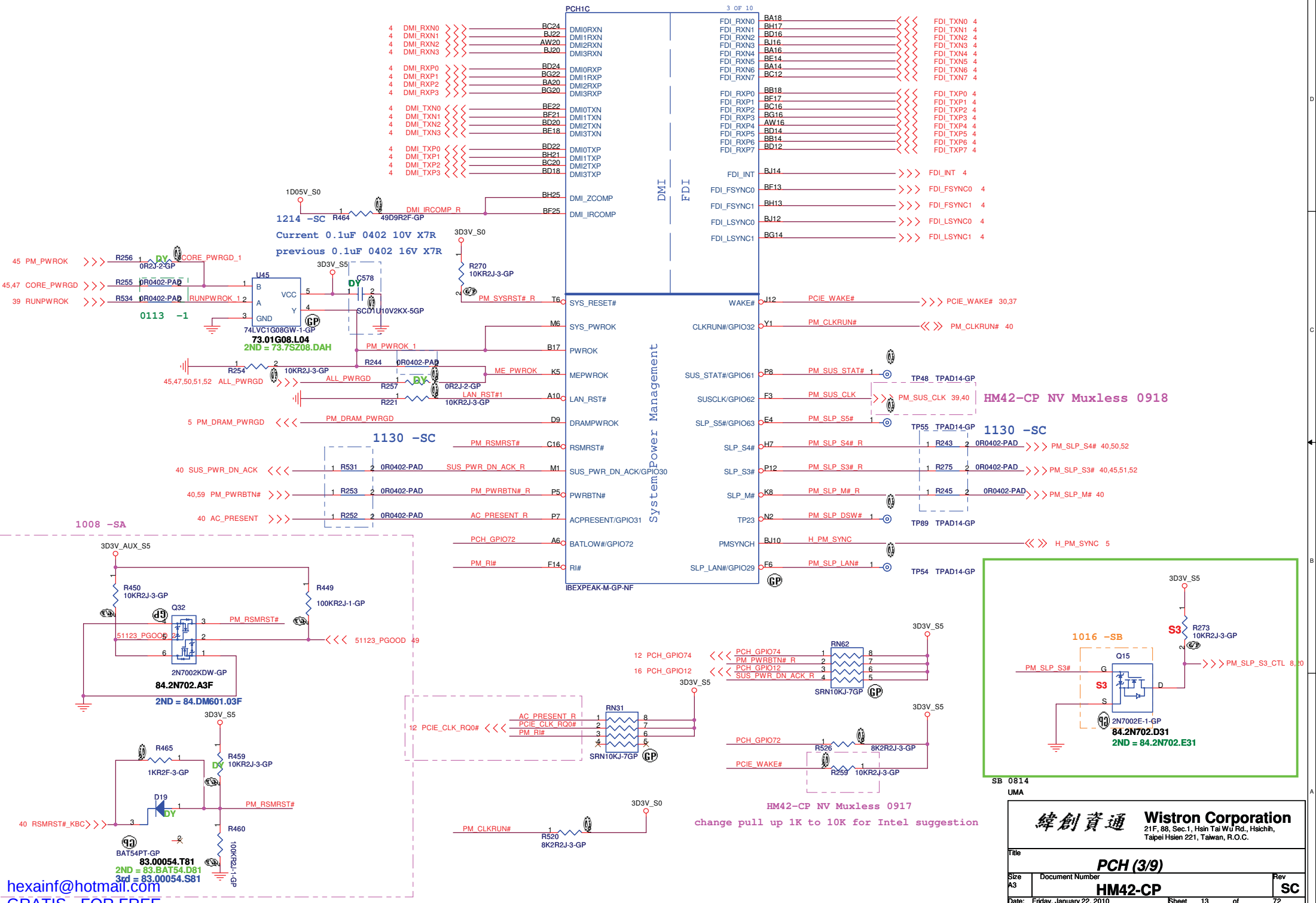
Rev SC

Date: Friday, January 22, 2010

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hexainf@hotmail.com

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Title			
PCH (4/9)			
Size A3	Document Number		Rev
	HM42-CP		SC
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GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

HM42-CP_NV_Muxless SA

62 DGPU_HOLD_RST# >>> DGPU_HOLD_RST#
55,61,62 DGPU_PWROK >>> DGPU_PWROK

TPAD14-GP TP36
TPAD14-GP TP46
TPAD14-GP TP45
TPAD14-GP TP56

12 PCH_GPIO11 <<< PCH_GPIO11
EC_SW# <<< EC_SW#
12 PCH_GPIO60 <<< PCH_GPIO60
PCH_GPIO28 <<< PCH_GPIO28

SRN10KJ-7GP
R30
3D3V_S5

PCH_GPIO45 <<< PCH_GPIO45
R508 8K2R2J-3-GP

SB 0819
PCH_GPIO15 <<< PCH_GPIO15
R266 1K2R2J-1-GP

PSW_CLR# <<< PSW_CLR#
GAP-OPEN
G111

11,44 SATA_LED# <<< SATA_LED#
PCH_GPIO39 <<< PCH_GPIO39
INT_SERIRQ <<< INT_SERIRQ
PSW_CLR# <<< PSW_CLR#

SRN10KJ-7GP
RN29
3D3V_S0

STP_PCI# <<< STP_PCI#
PCH_GPIO22 <<< PCH_GPIO22
PCH_GPIO0 <<< PCH_GPIO0
dGPU_EDID <<< dGPU_EDID

3D3V_S0 <<< 3D3V_S0
SRN10KJ-L3-GP

PCH_GPIO35 <<< PCH_GPIO35
10K2R2J-3-GP R265

SB 0722
AFTE14P-GP TP806
AFTE14P-GP TP88
AFTE14P-GP TP87
AFTE14P-GP TP82

1 PCH TP95
1 PCH TP96
1 PCH TP97
1 PCH TP98

10K2R2J-3-GP R265

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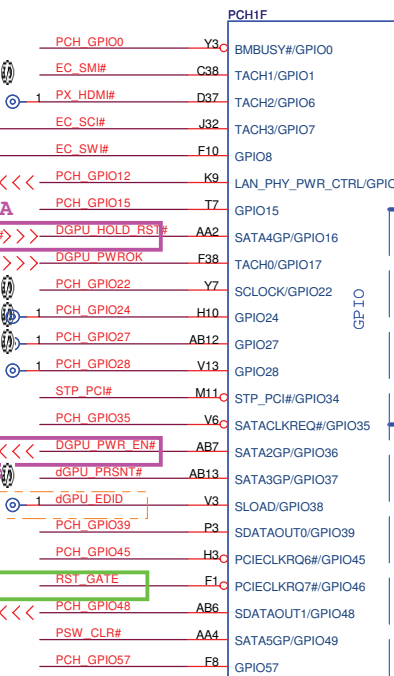
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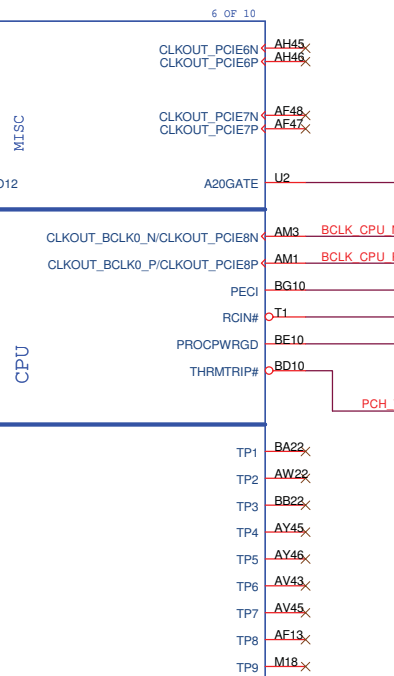
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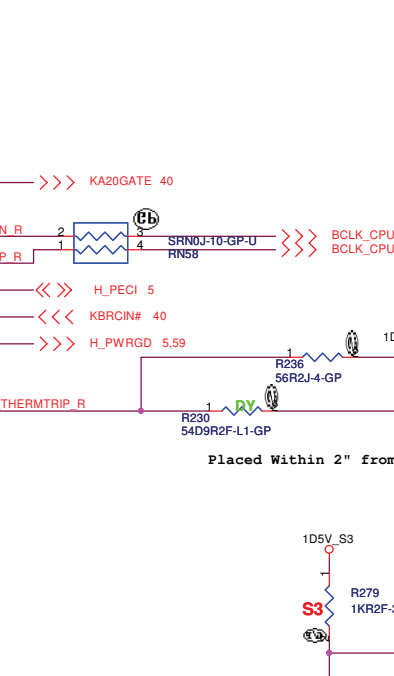
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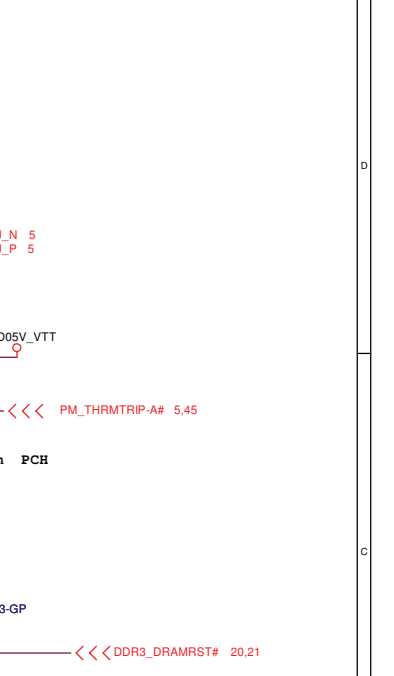
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hexainf@hotmail.com
GRATIS - FOR FREE

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size A3

Date: Friday, January 22, 2010

Document Number

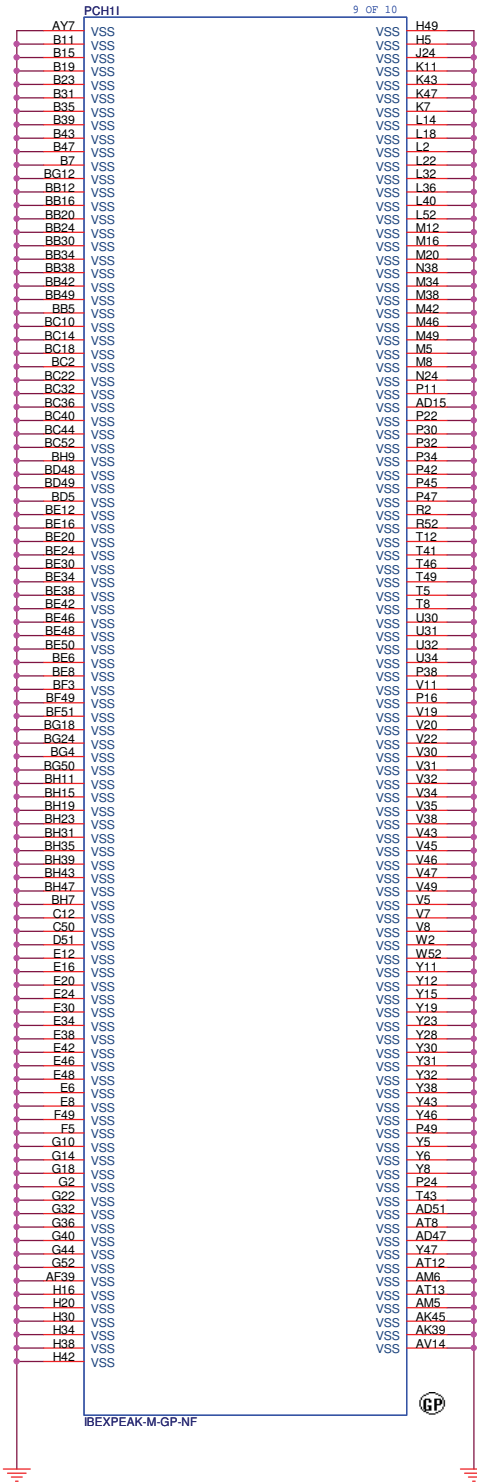
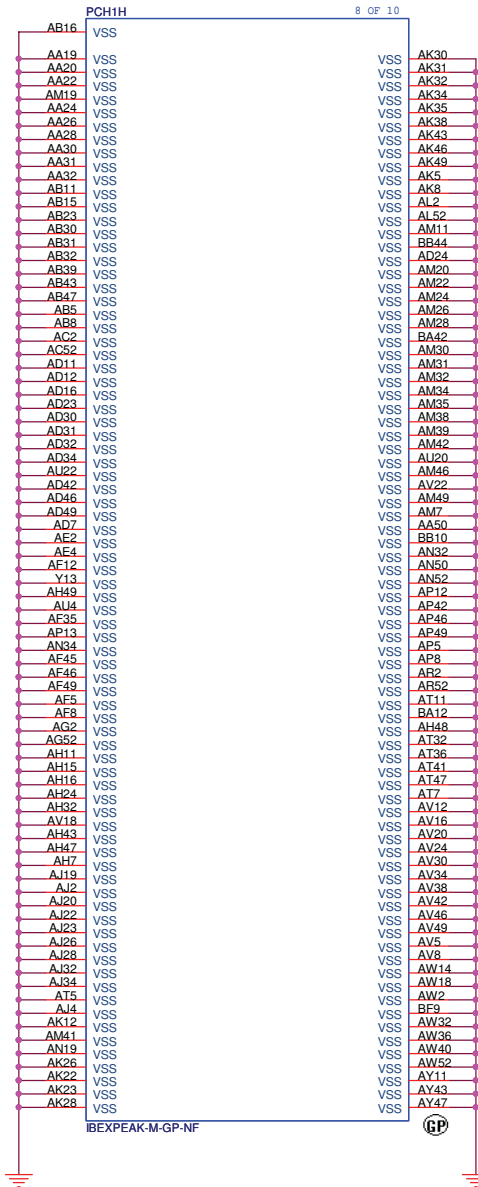
Sheet 16 of 72

Rev

SC

PCH (6/9)

HM42-CP



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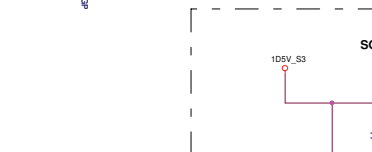
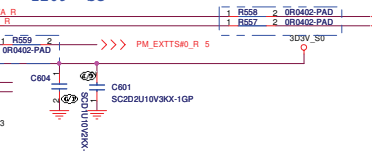
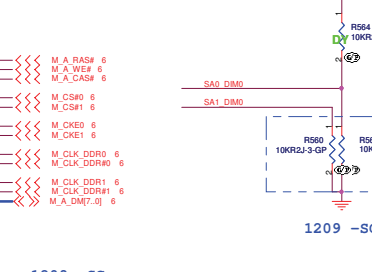
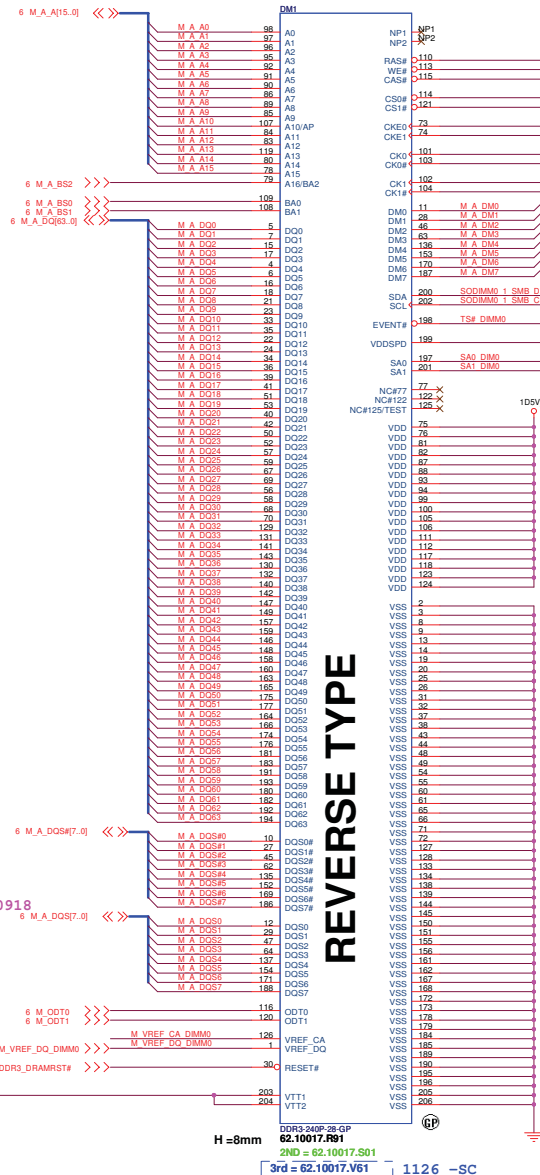
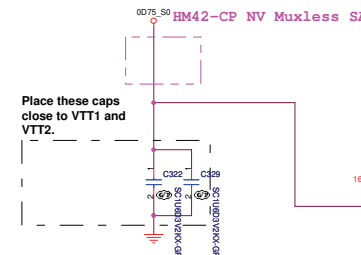
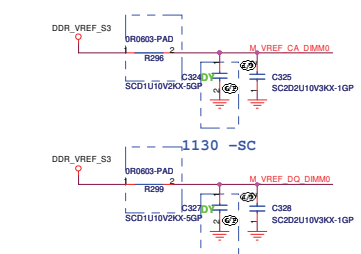
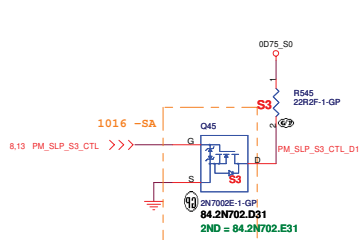
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH (9/9)

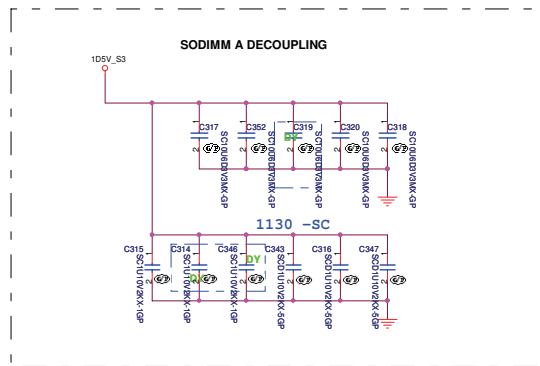
Size A3 Document Number Rev
HM42-CP **SC**

Date: Friday, January 22, 2010 Sheet 19 of 72



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

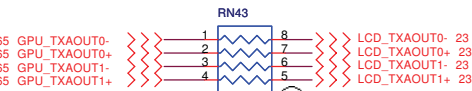
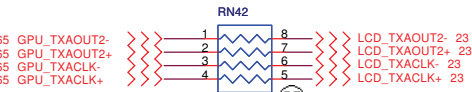
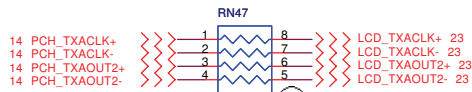
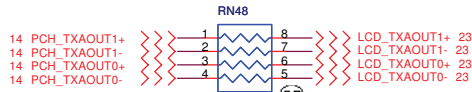
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SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



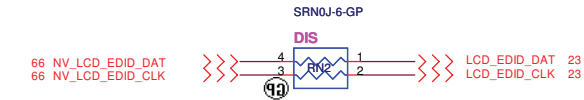
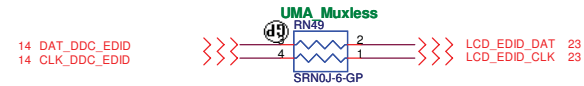
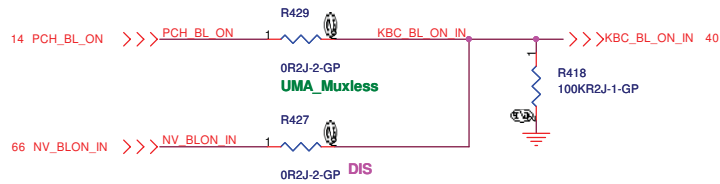
Layout Note:
Place these Caps near
SO-DIMMA.

REVERSE TYPE

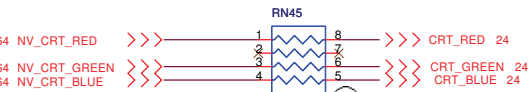
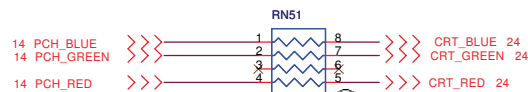
H=8mm
2ND = 62.10017.S01
3rd = 62.10017.V61



1016 -SB



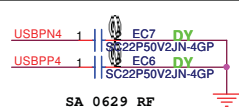
1016 -SB



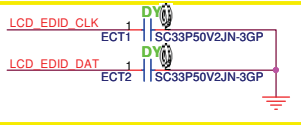
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LCD/INVERTER/CCD CONN

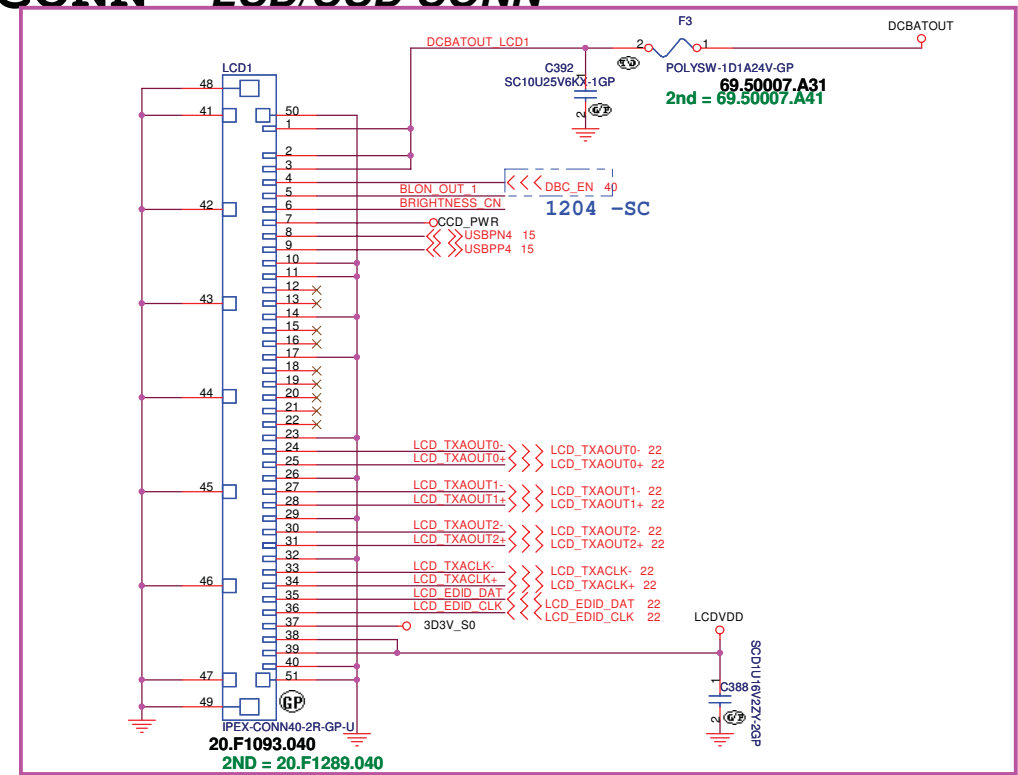
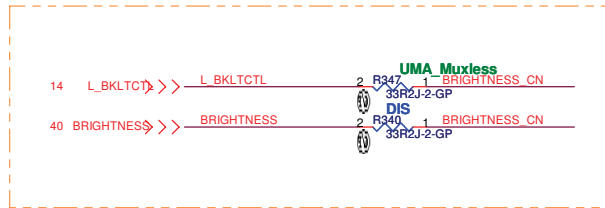
LCD/CCD CONN



SA 0629 RF

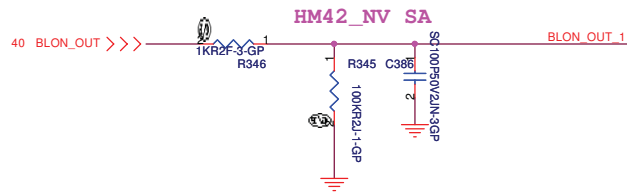


1016 -SB

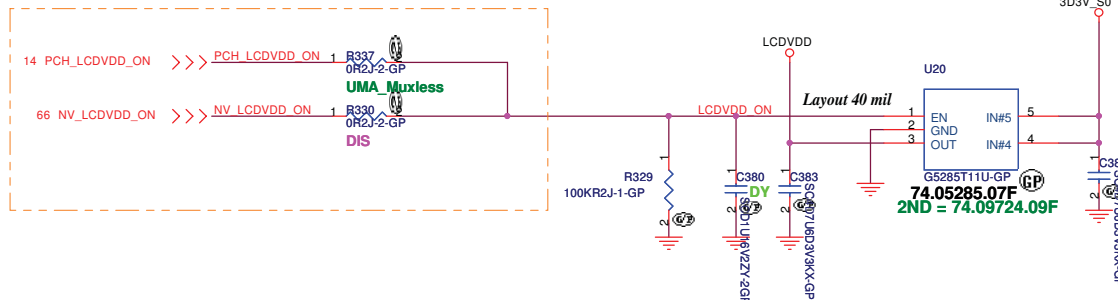


1005 -SA

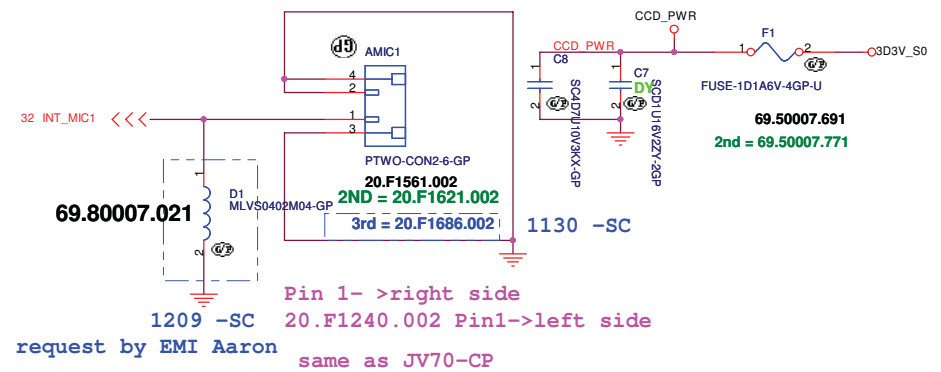
define same as SJM50-PU, can use SJM50 Cable



1016 -SB



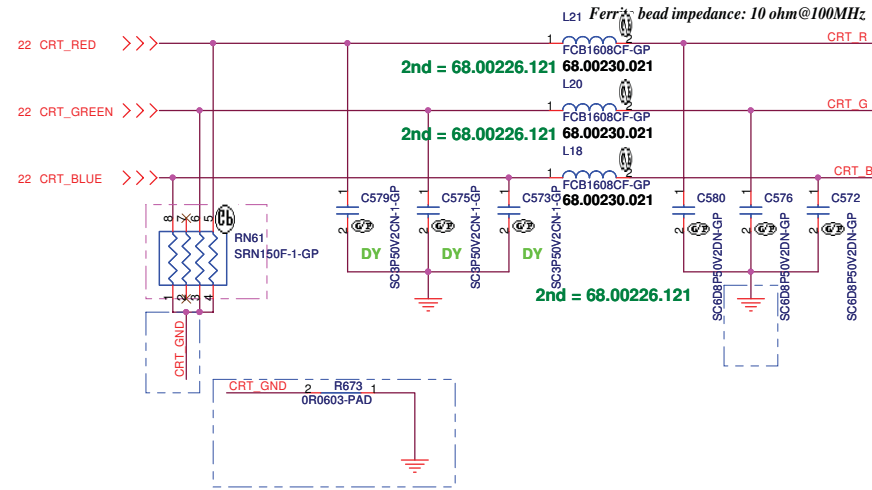
Internal Mic



Discrete N11M

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Size	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010	Sheet 23 of 72	

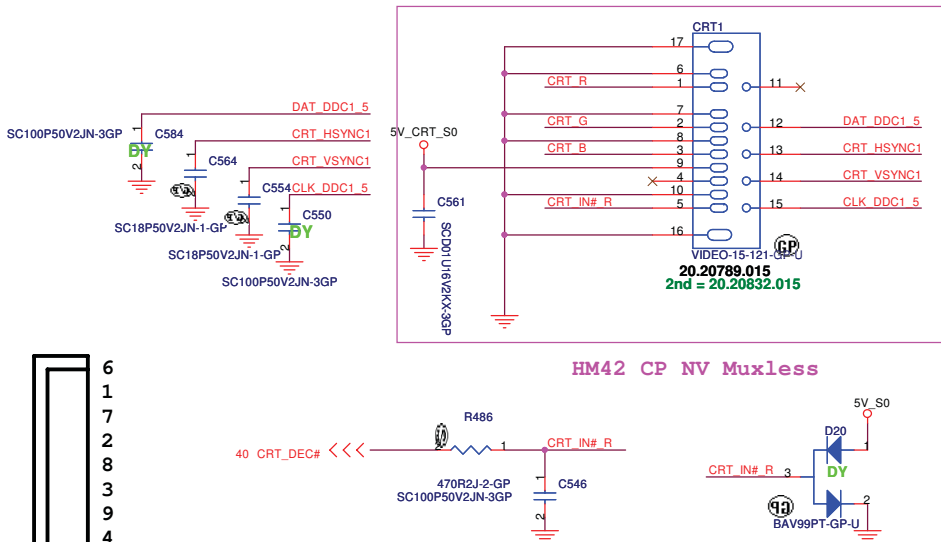
Layout Note:
Place these resistors
close to the CRT-out
connector



Layout Note:

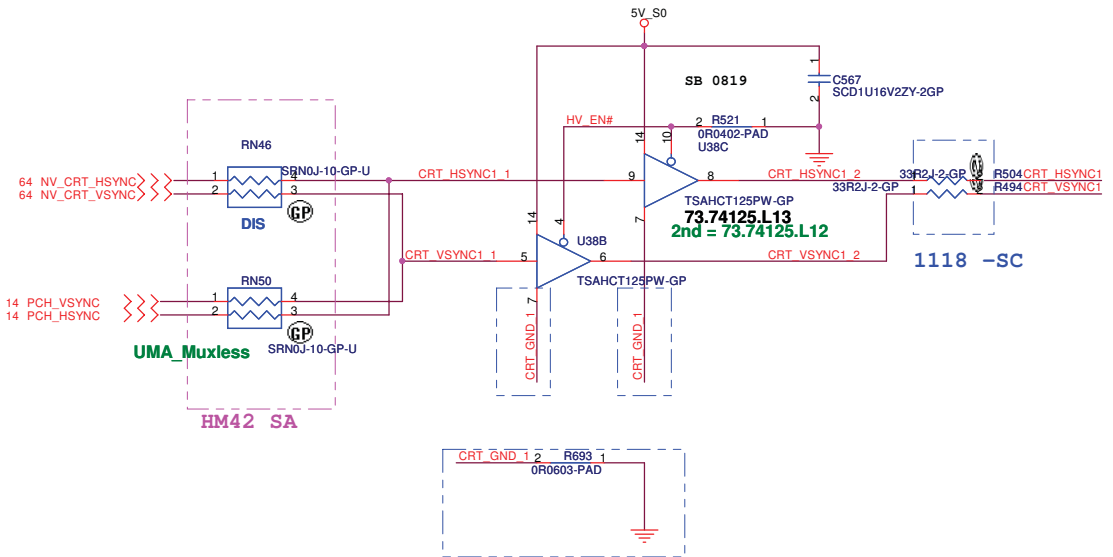
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

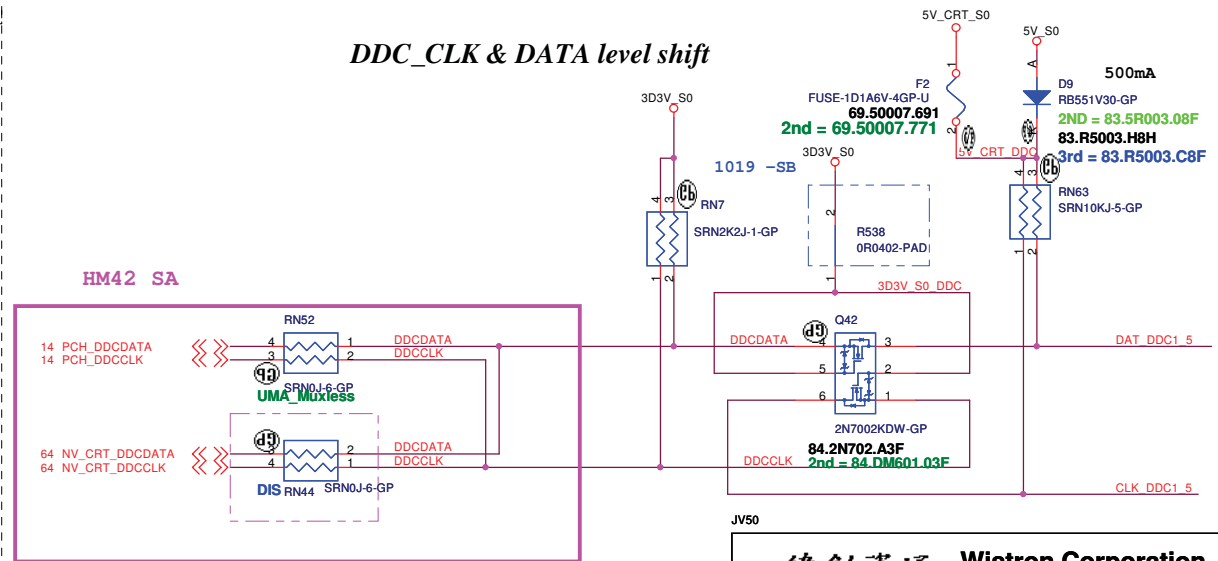


HM42 CP NV Muxless

Hsync & Vsync level shift



DDC_CLK & DATA level shift



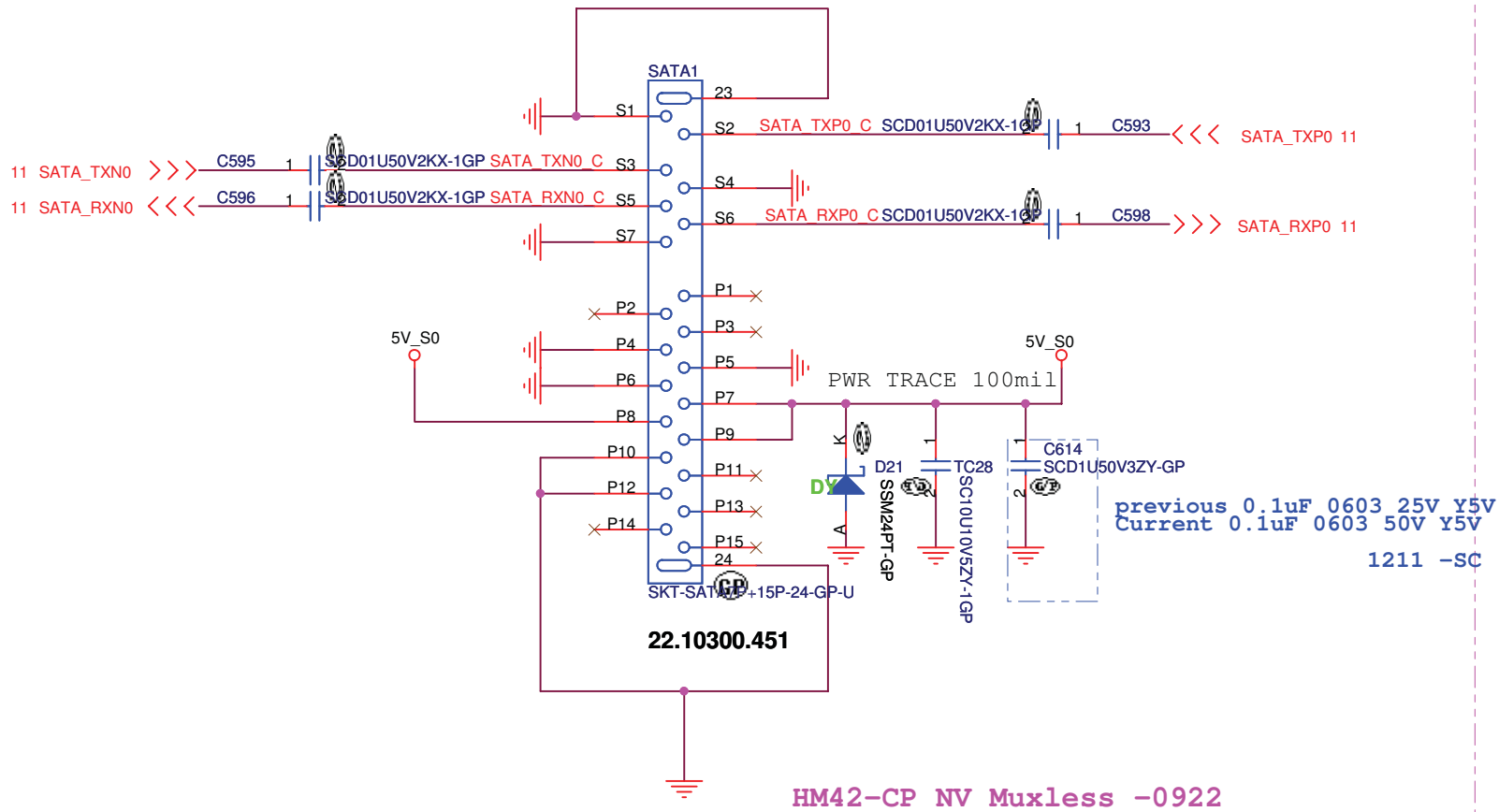
JV50

緯創資通

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		CRT CONN	
Size	Document Number	Rev	SC
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SATA Connector



UMA

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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HDD CONN

Size

Document Number

HM42-CP

Rev

SC

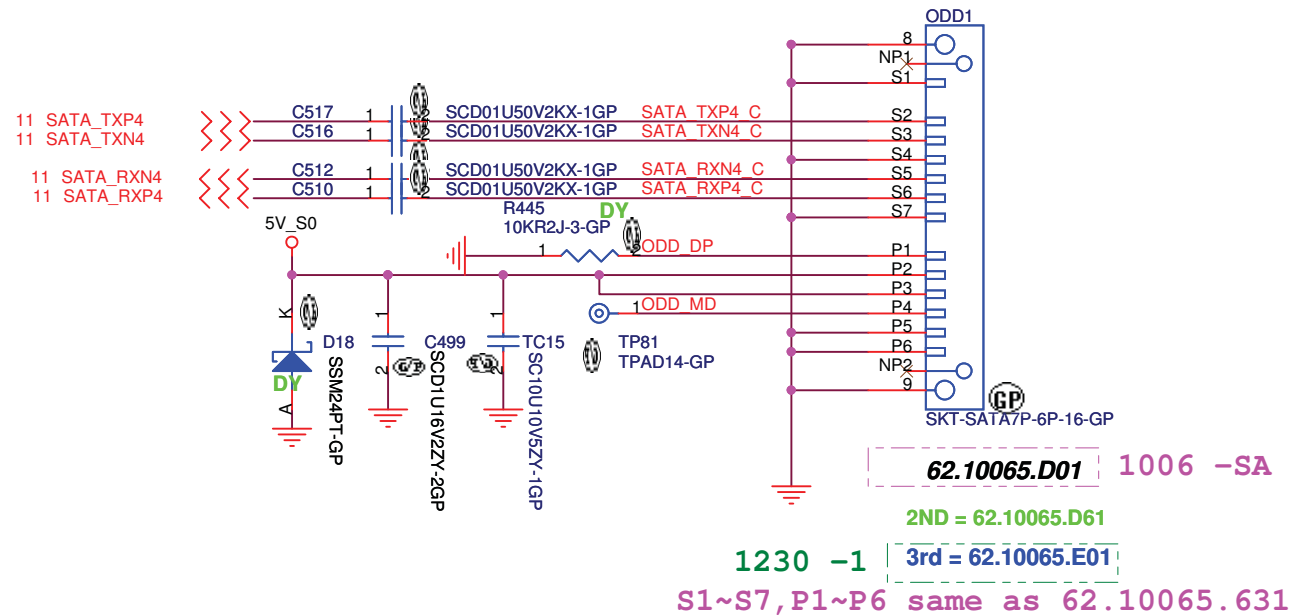
Date: Friday, January 22, 2010

Sheet 26

of

72

ODD Connector



UMA

緯創資通

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Title

ODD

Size

Document Number

HM42-CP

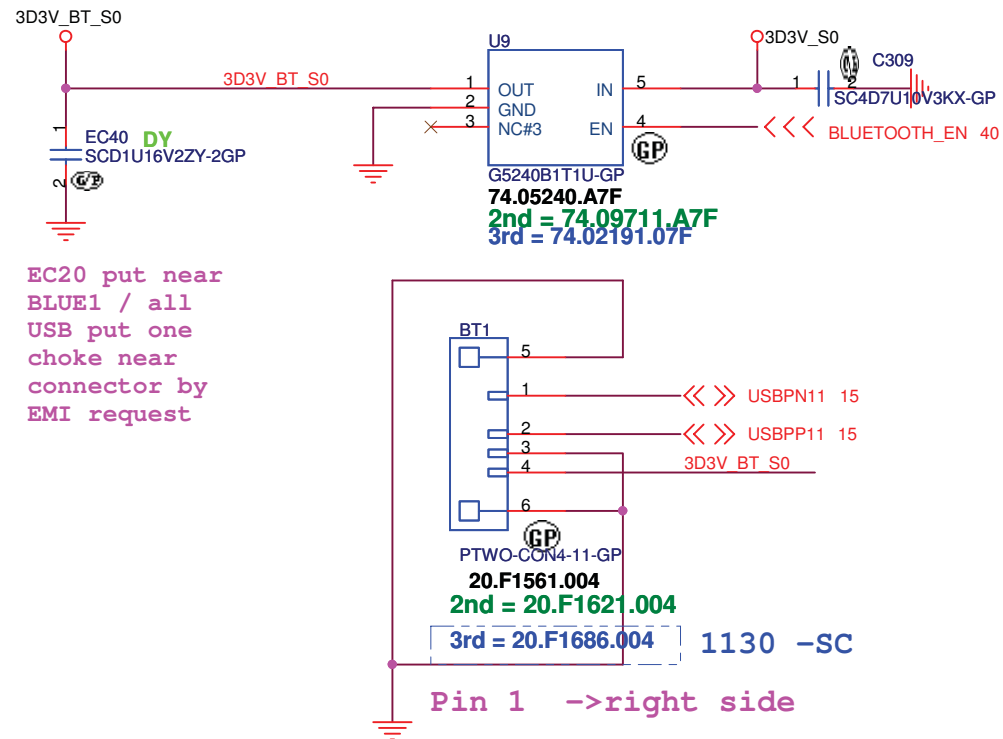
Rev

SC

Date: Friday, January 22, 2010

Sheet 27 of 72

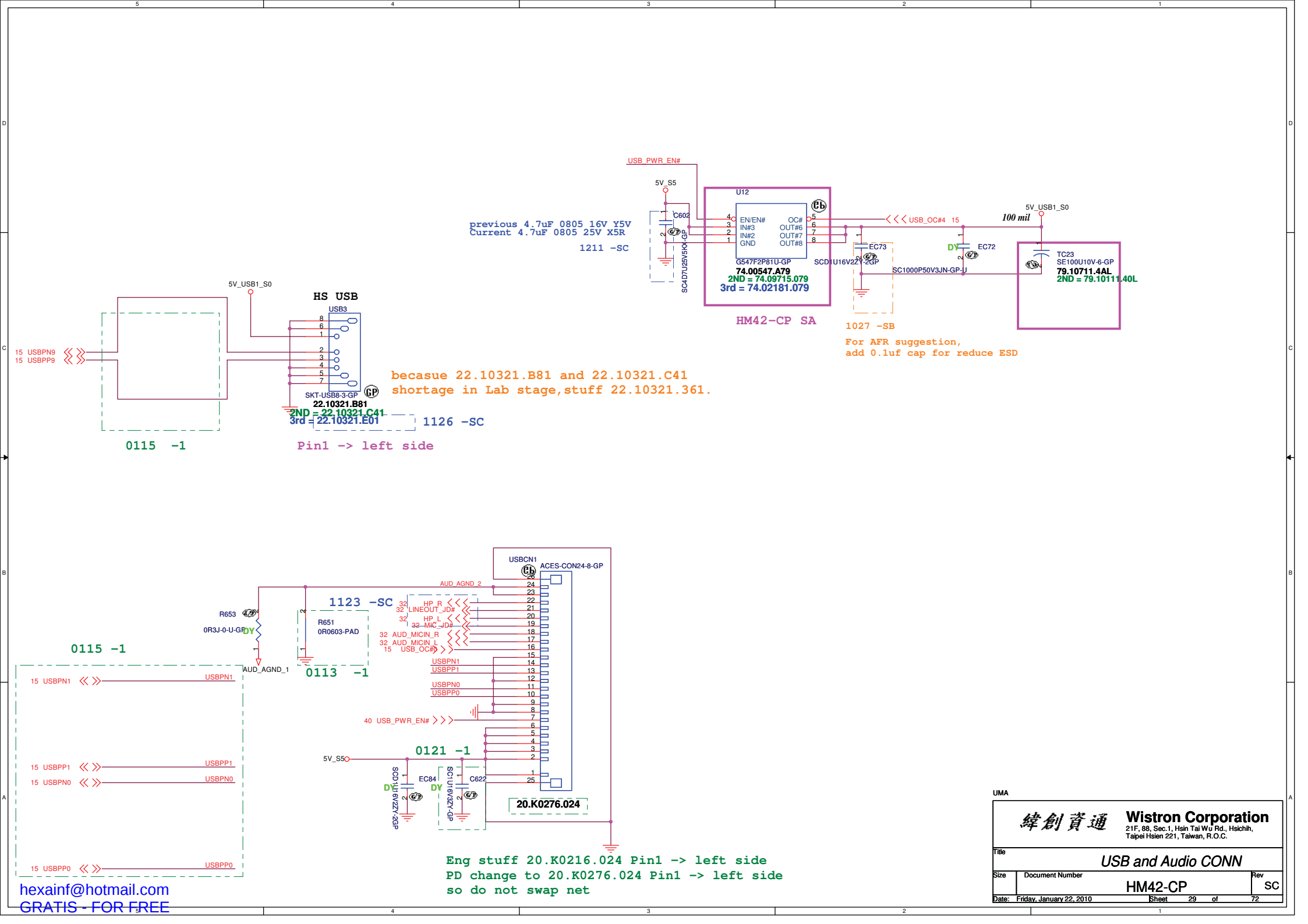
BLUETOOTH MODULE



JV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BLUETOOTH		
Size	Document Number	Rev
	HM42-CP	SC
Date:	Friday, January 22, 2010	Sheet 28 of 72



previous 4.7uF 0805 16V Y5V
Current 4.7uF 0805 25V X5R
1211 -SC

HM42-CP SA

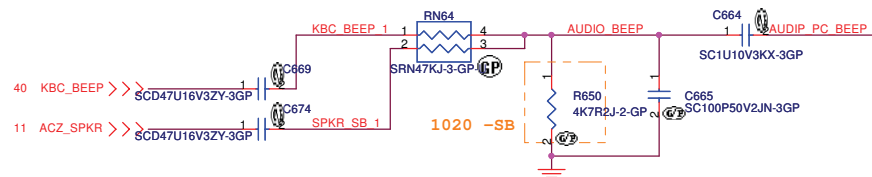
1027 -SB
For AFR suggestion,
add 0.1uf cap for reduce ESD

because 22.10321.B81 and 22.10321.C41
shortage in Lab stage,stuff 22.10321.361.

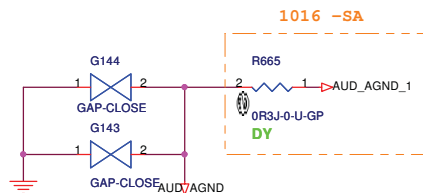
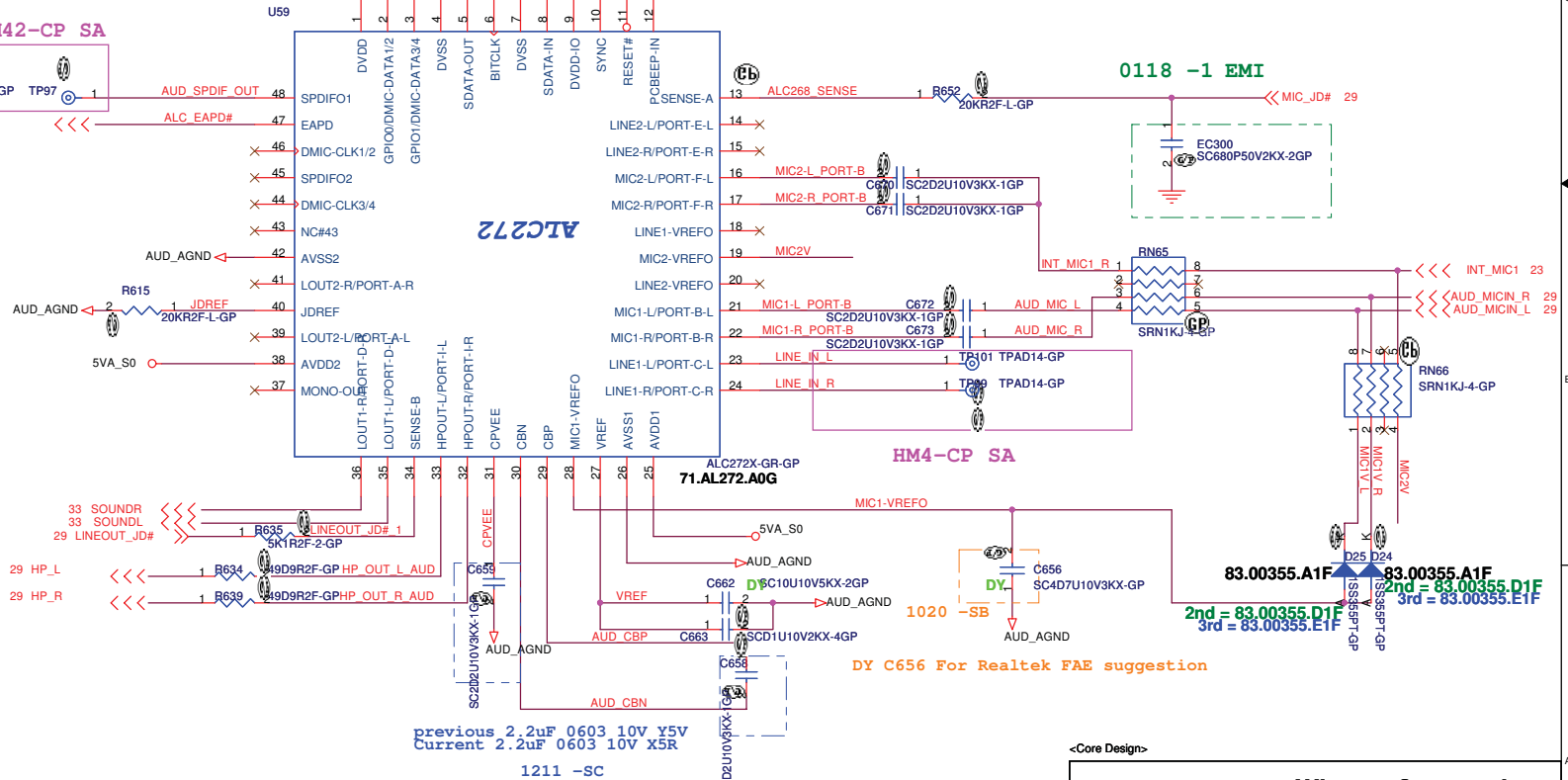
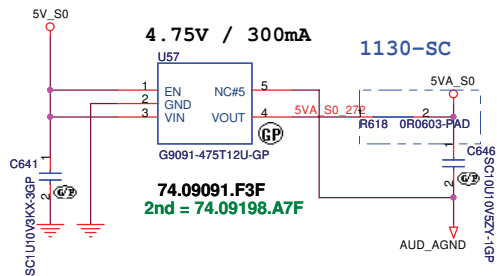
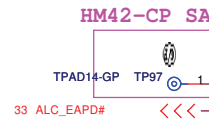
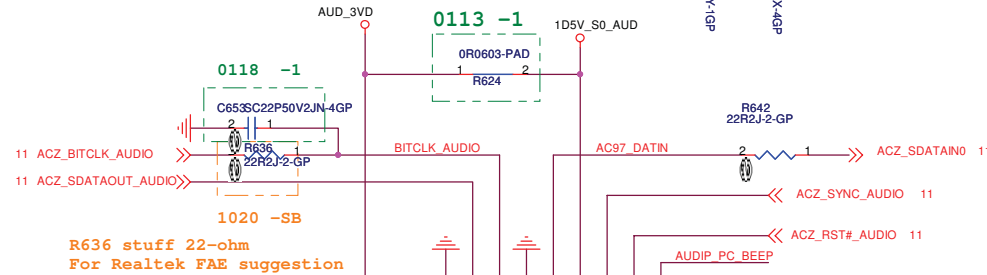
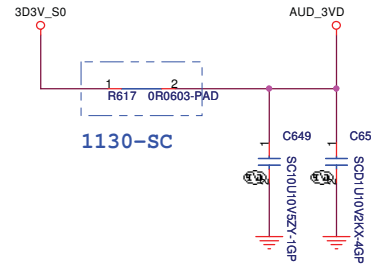
Pin1 -> left side

Eng stuff 20.K0216.024 Pin1 -> left side
PD change to 20.K0276.024 Pin1 -> left side
so do not swap net

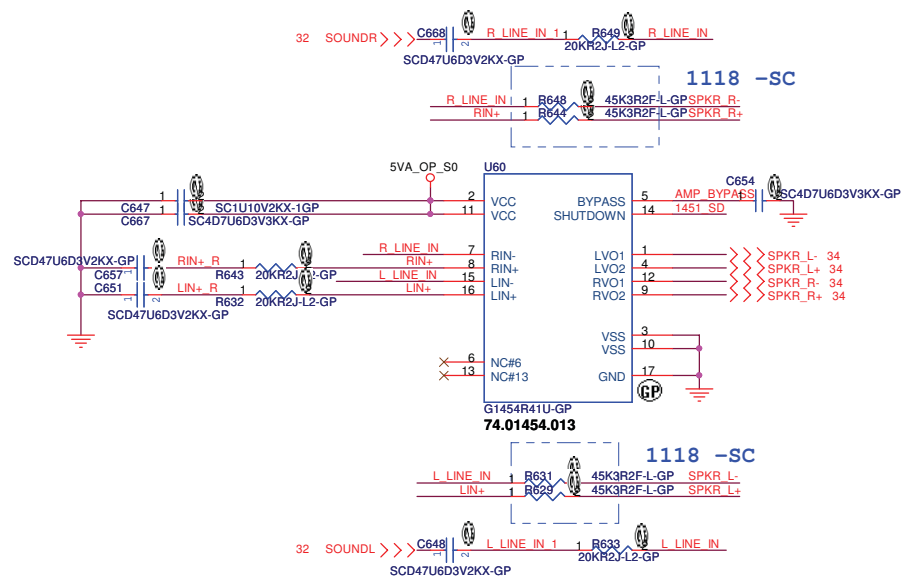
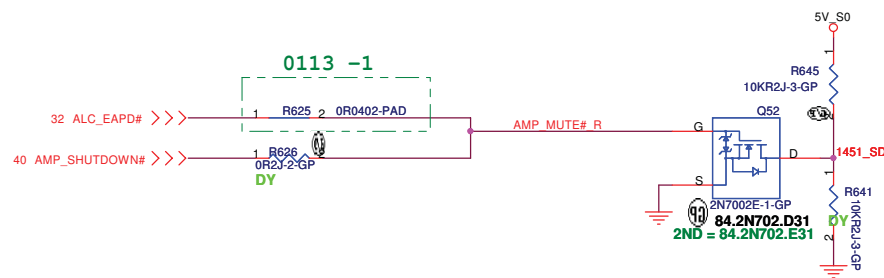
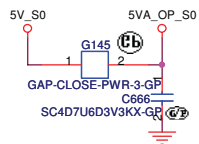
UMA			
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB and Audio CONN			
Size	Document Number		Rev
	HM42-CP		SC
Date:	Friday, January 22, 2010		Sheet 29 of 72



change R650 from 10K-ohm to 4.7K-ohm
For preventing the beep sound is too loudly
from Realtek FAE suggestion



緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title Azalia codec ALC272			
Size A3	Document Number	HM42-CP	Rev SC
Date: Friday, January 22, 2010	Sheet 32	of 72	



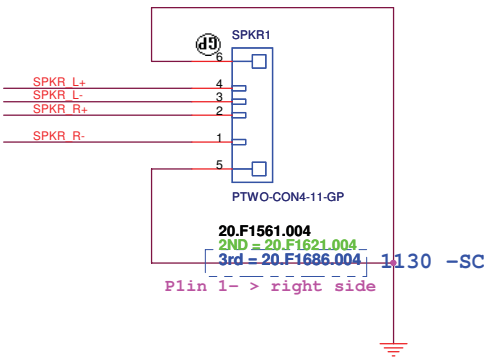
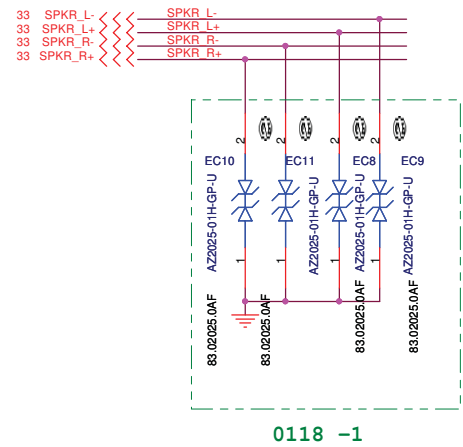
Gain= $R_f/R_i=52K/20K=2.6V/V$
 $f(HP)=1/(2 \pi * 20K * 0.47uF)=16.9Hz$
 If $V_{IN}=1.54V$ Gain=2.6V/V $R_L=4\Omega$ $V_O(peak)=4V$ $V(rms)=2.828V$
 Power= $2.446^2/4=1.5W$

UMA

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

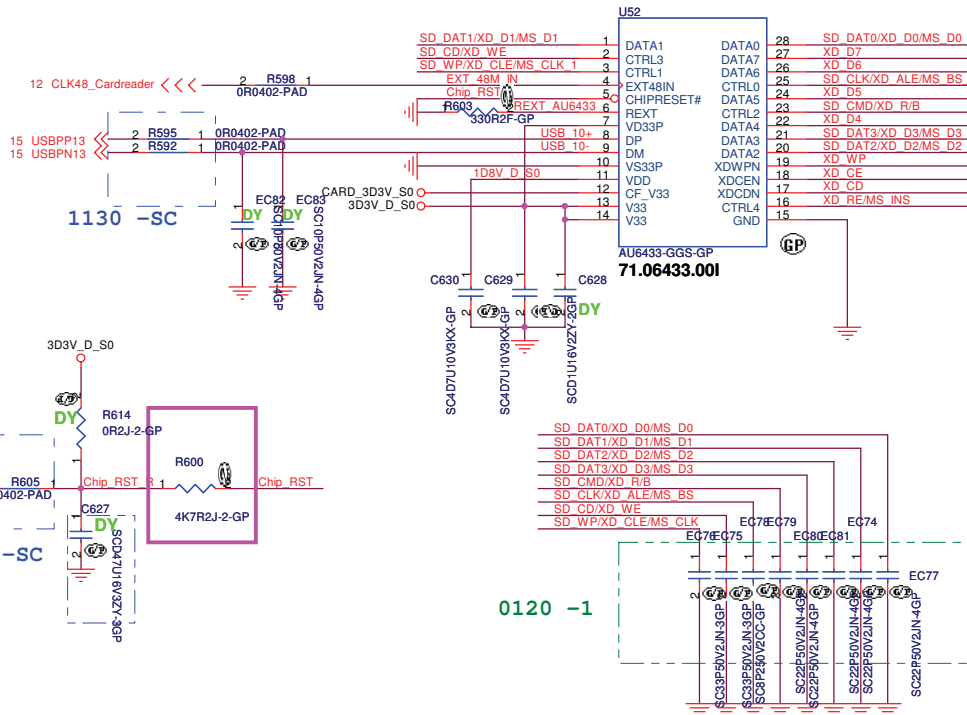
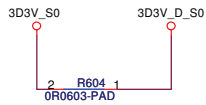
Title		AUDIO AMP	
Size	Document Number	HM42-CP	Rev SC
Date:	Friday, January 22, 2010	Sheet 33 of 72	

Internal Speaker



JV50

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Resrve MDC			
Size	Document Number		Rev
	HM42-CP		SC
Date: Friday, January 22, 2010		Sheet 35 of 72	

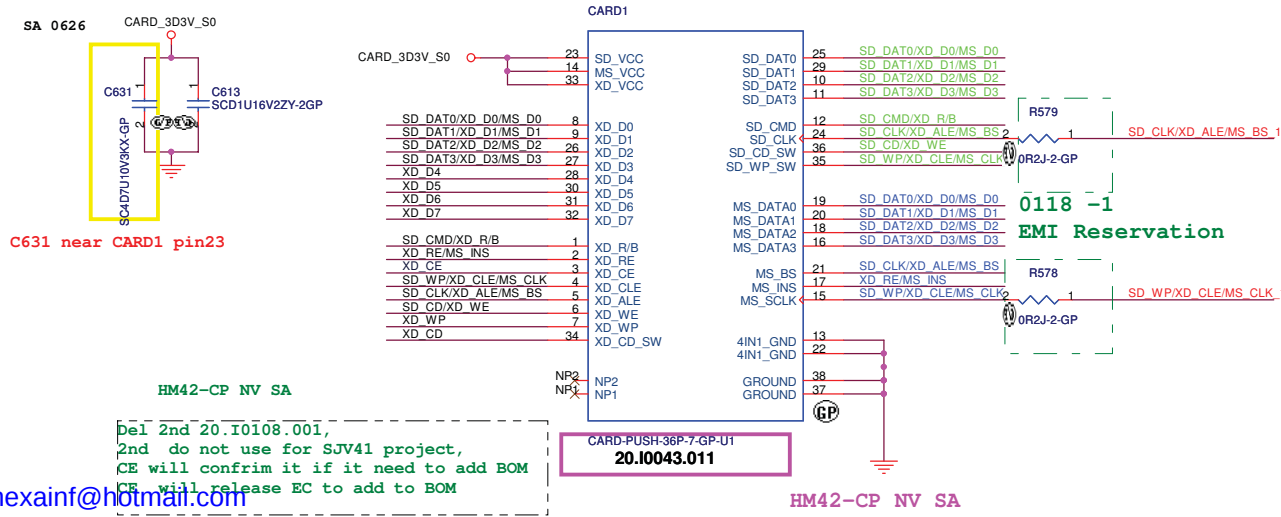


Pin	Name	SD Mode Description
1	CD/DAT3	Card detect/Data line[Bit 3]
2	CMD	Command/Response
3	VSS1	Supply voltage ground
4	VDD	Supply voltage
5	CLK	Clock
6	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]
8	DAT1	Data line[Bit 1]
9	DAT2	Data line[Bit 2]

Pin No.	SD/MMC	MS/MS PRO	xD
P1	xD-R/B		2P
P2	xD-RE		3P
P3	xD-CE		4P
P4	xD-CLE		5P
P5	xD-ALE		6P
P6	xD-WE		7P
P7	xD-WP		8P
P8	xD-D0		10P
P9	xD-D1		11P
P10	SD-DAT2	9P	
P11	SD-DAT3	1P	
P12	SD-CMD	2P	
P13	4in1-GND	3P/6P	1P/10P
P14	MS-VCC		8P
P15	MS-SCLK		8P
P16	MS-DATA3		7P
P17	MS-INS		6P
P18	MS-DATA2		5P
P19	MS-DATA0		4P

Pin No.	SD/MMC	MS/MS PRO	xD
P20	MS-DATA1		3P
P21	MS-BS		2P
P22	4in1-GND	3P/6P	1P/10P
P23	SD-VCC	4P	
P24	SD-CLK	5P	
P25	SD-DAT0	7P	
P26	xD-D2		12P
P27	xD-D3		13P
P28	xD-D4		14P
P29	SD-DAT1	8P	
P30	xD-D5		15P
P31	xD-D6		16P
P32	xD-D7		17P
P33	xD-VCC		18P
P34	XD-CD-SW		19P
P35	SD-WP-SW	SD-WP-SW	
P36	SD-CD-SW	SD-CD-SW	
P37	4 IN 1-GND	SD-WP/CD-SW-GND	
P38			

5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



Pin	Name	Dir	description
1	XD_CD#	-	presence detect
2	R/B#	OUT	Ready / Busy (open-drain)
3	RE#	IN	Read Enable
4	CE#	IN	Card Enable
5	CLE	IN	Command Latch Enable
6	ALE#	IN	Address Latch Enable
7	WE#	IN	Write Enable
8	WP#	IN	Write Protect
9	GND	-	Ground
10	SD0	IN/OUT	data bit 0
11	SD1	IN/OUT	data bit 1
12	SD2	IN/OUT	data bit 2
13	SD3	IN/OUT	data bit 3
14	SD4	IN/OUT	data bit 4
15	SD5	IN/OUT	data bit 5
16	SD6	IN/OUT	data bit 6
17	SD7	IN/OUT	data bit 7
18	VCC	-	3.3V power

Pin	Pin Name	Description
1	VSS	Vss
2	BS	Bus state signal
3	DATA1	Data1 Parallel / NC Serial
4	SDIO/DATA0	Data0 Parallel / Data Serial
5	DATA2	Data2 Parallel / NC Serial
6	INS	Stick detect (connected to VSS)
7	DATA3	Data3 Parallel / NC Serial
8	SCLK	Clock signal
9	VCC	Vcc (2.7V - 3.6V)
10	VSS	Vss

UMA

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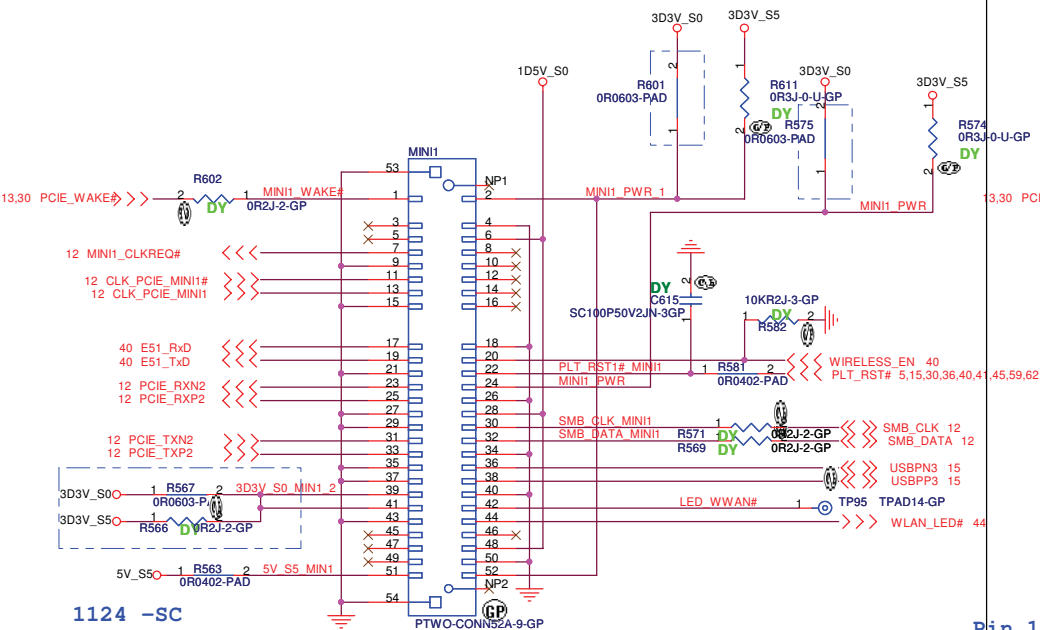
Title: **Cardreader**

Size: Document Number: **HM42-CP** Rev: **SC**

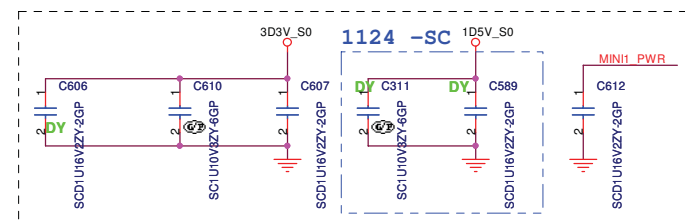
Date: Friday, January 22, 2010 Sheet: 36 of 72

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Mini Card Connector(WLAN) Support debug-card

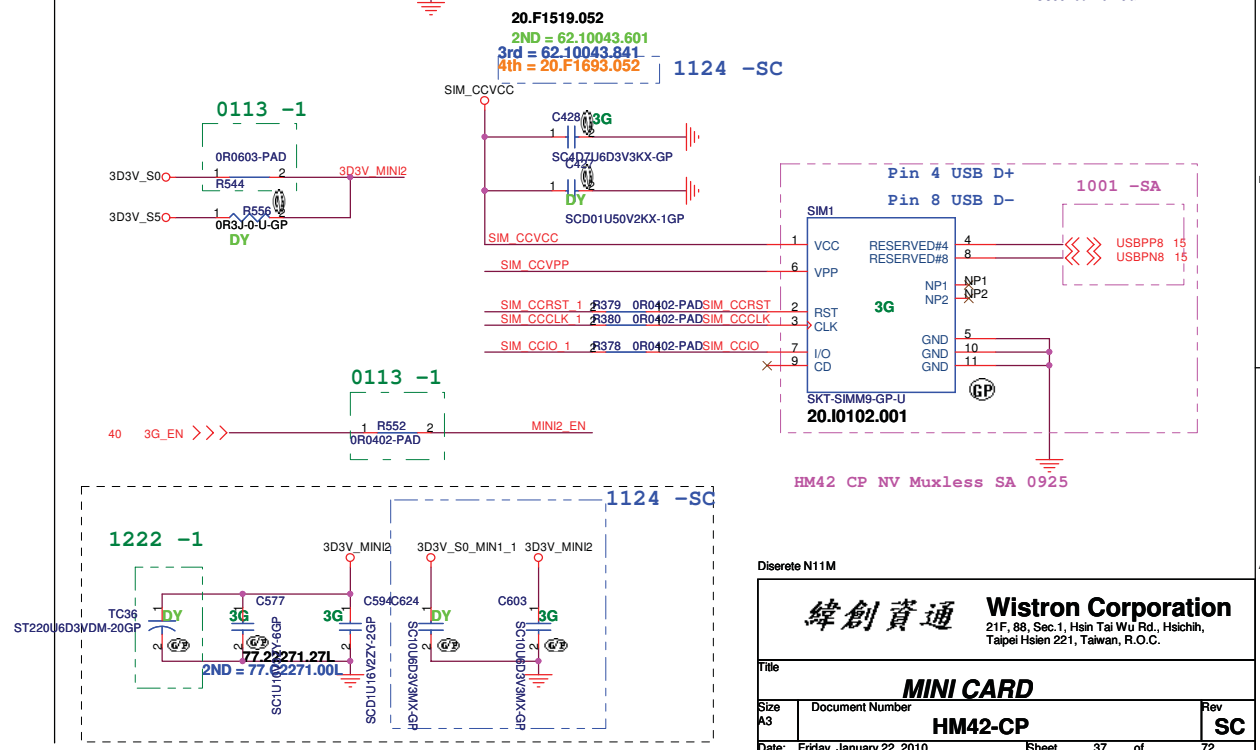
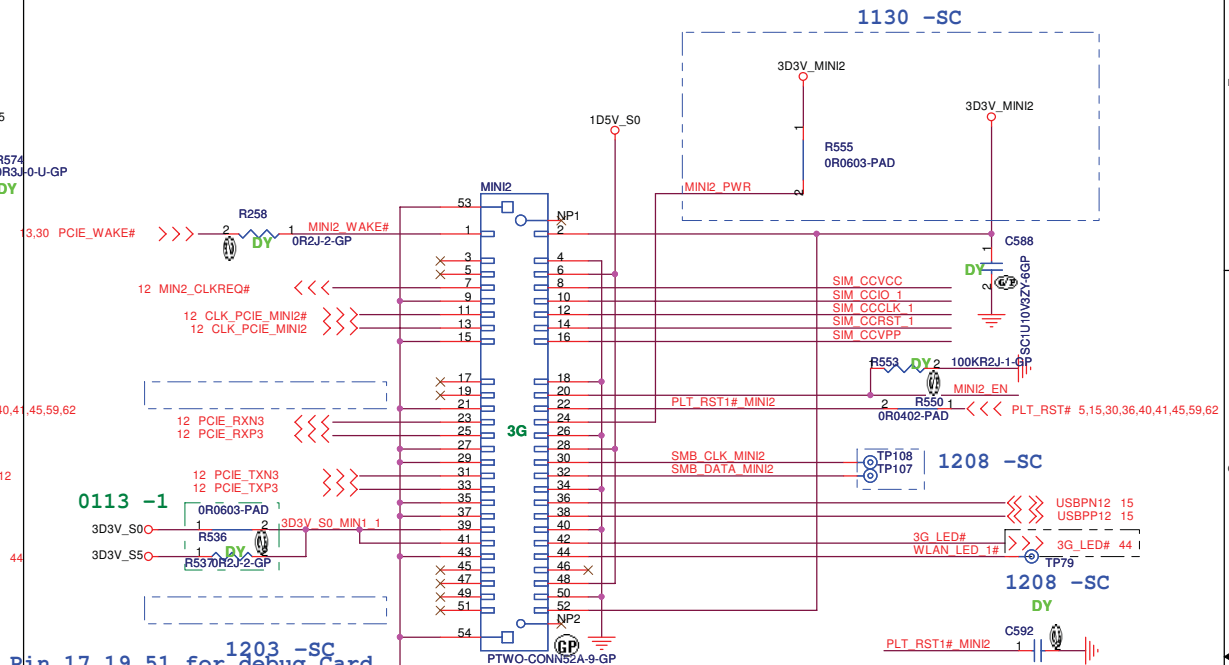


Place near MINI1



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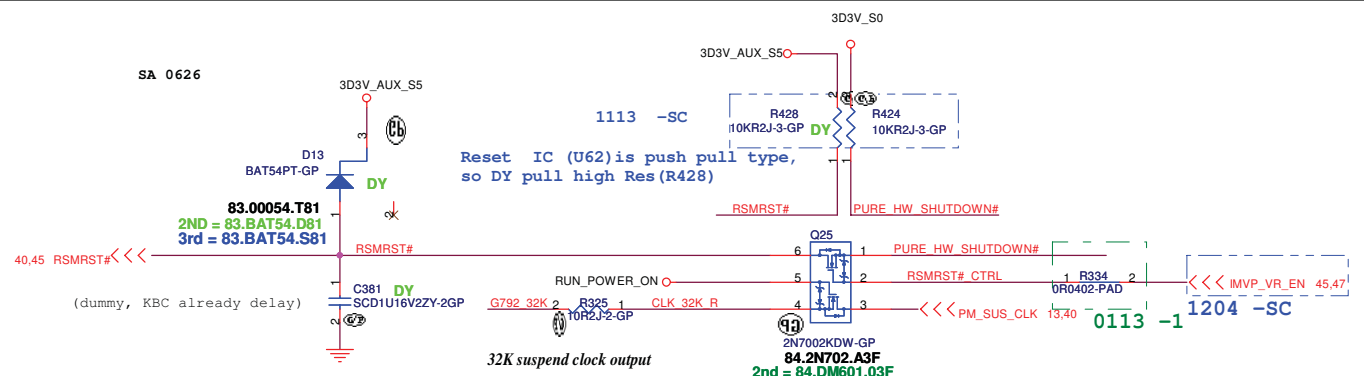
Mini Card Connector(Robson2 and 3G)



Discrete N11M

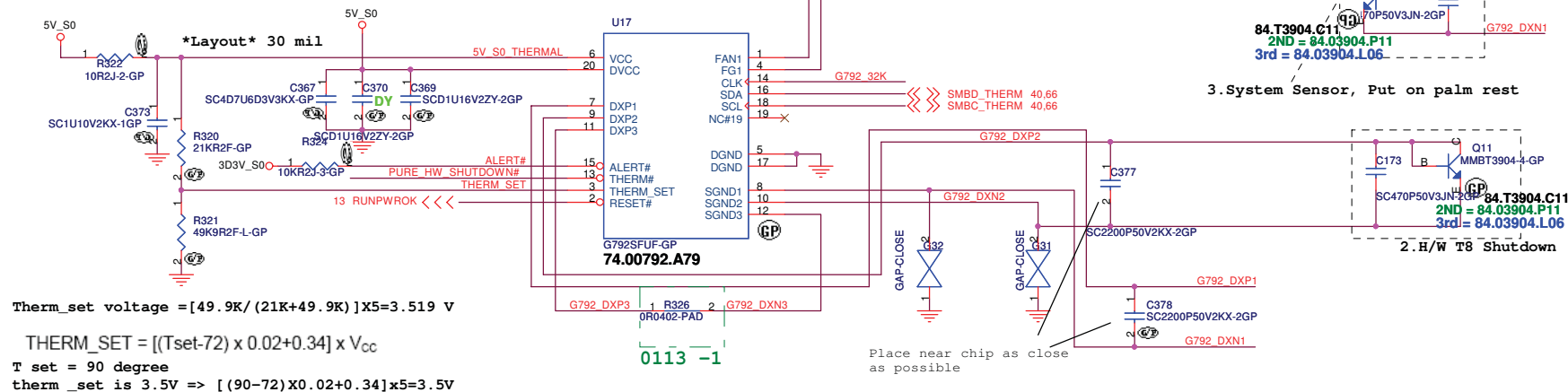
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			MINI CARD		
Size	Document Number	HM42-CP			Rev
A3					SC
Date:	Friday, January 22, 2010	Sheet	37	of	72



Thermal Get define

- Sensor0 => CPU
Sensor1=> system temp (thermal DPX1)
Sensor2=> HW T8 shut down(thermal DPX2)
Sensor3=> unused(thermal DPX3)
Sensor4=> MCH
Sensor5=> PCH
Sensor6=> Adpater Current
Sensor7=>dGPU
Sensor8=>Battery Thermal
Sensor9=>Battery Current



Therm_set voltage = $[49.9\text{K}/(21\text{K}+49.9\text{K})]\times 5=3.519\text{ V}$

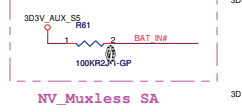
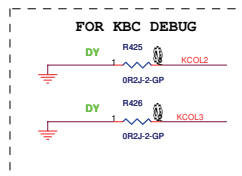
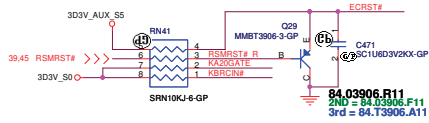
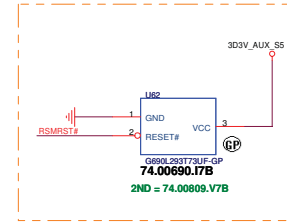
$$\text{THERM_SET} = [(T_{\text{set}} - 72) \times 0.02 + 0.34] \times V_{\text{CC}}$$

T set = 90 degree

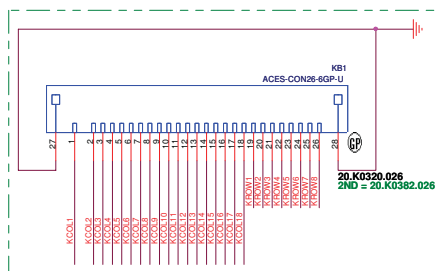
therm_set is 3.5V => $[(90-72) \times 0.02 + 0.34] \times 5 = 3.5V$

```
DXP1: System Sensor
DXP2: H/W Setting(T8)
DXP3: do not use
```

Prevent BIOS data loss solution
1019 -SB

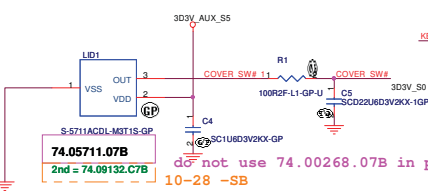


Internal Keyboard Connector



change connect to FPC (Same as Lab)
20.K0251.026 Pin 1 -> left side
20.K0320.026 Pin 1 -> right side (use in lab stage)
so swap net

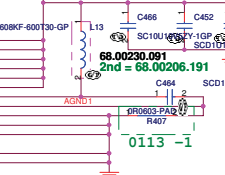
Cover Up Switch



do not use 74.00268.07B in project for Deark suggestion
10-28 -SB

L16 -> 68.00082.011 is a obsoleted part
0930 -SA

Impedance: 60-ohm
rated Current :3A



BATTERY
THERMAL

1016 -SB

SS_ENABLE KBC

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

SS_ENABLE

PCB Version AID (Pin8)	Pull-Down Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100K	10K	3.0V
SB	100K	20K	2.75V
SC	100K	30K	2.54V
-I	100K	47K	2.24V
Reserved	100K	68K	1.94V
Reserved	100K	82K	1.81V
Reserved	100K	100K	1.65V

Value PN

10K 63.10334.1DL

8.2K 63.82234.1DL

6.98K 64.69815.6DL

4.7K 63.47234.1DL

3K 64.30015.6DL

2K 64.20015.6DL

1K 63.10234.1DL

Model ID

14" PH 10K 3.3V_AUX_S5

17" PL 10K GND

1118 -SC

Model ID

PCB_VERR AD

0111 -1

UMA_65W

DIS_Muxless_90W

UMA

UMA

UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taiwan 305, R.O.C.

File

KBC KB3930

Size

Document Number

1

Rev

SC

Date

Friday, January 22, 2010

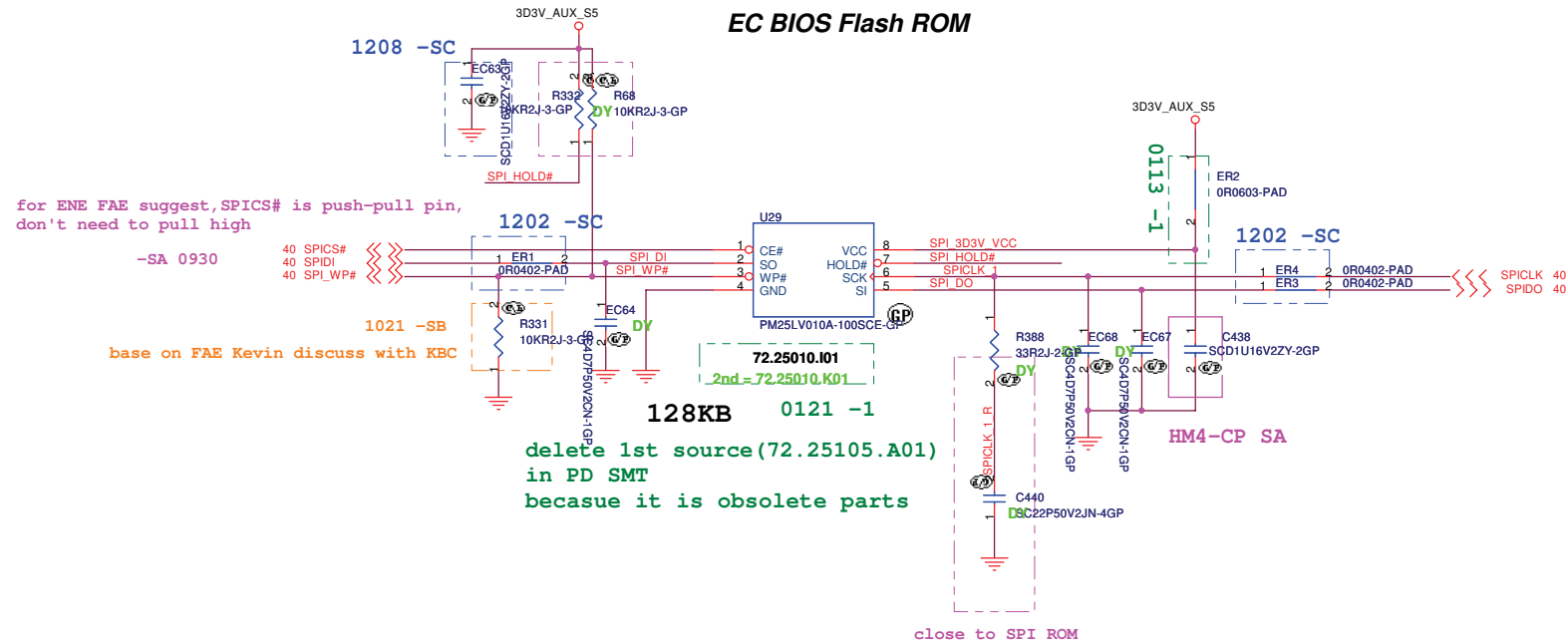
Sheet

40

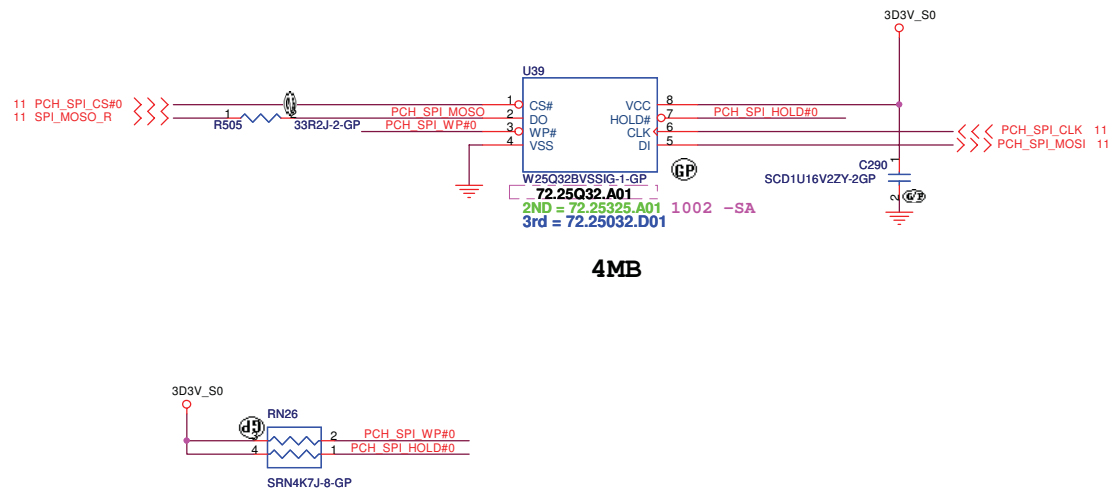
of

72

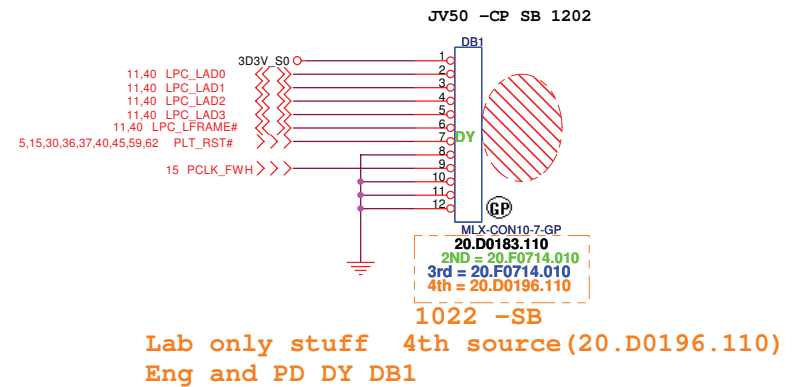
EC BIOS Flash ROM



System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD



Discrete N11M

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

[illegible]

BIOS

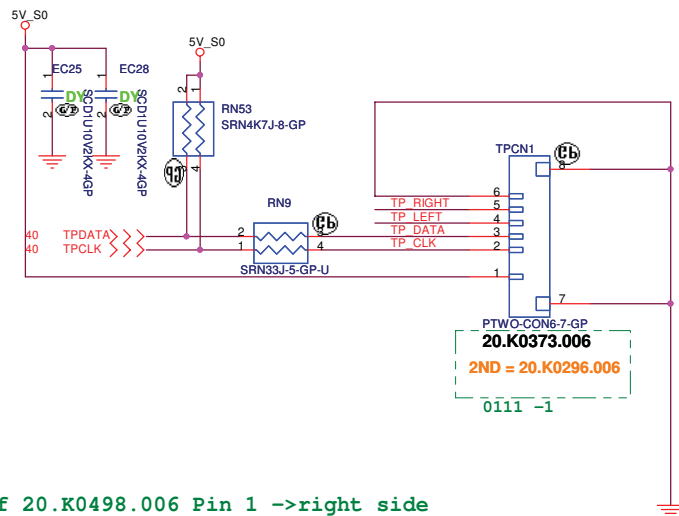
Size	Document Number
------	-----------------

HM42-CPRev
SC

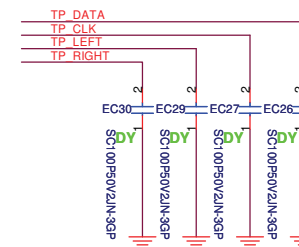
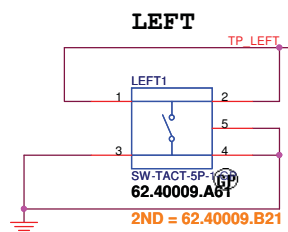
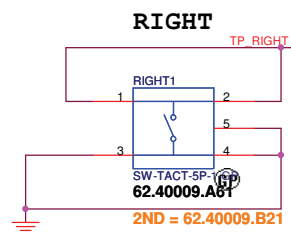
Date: Friday, January 22, 2010

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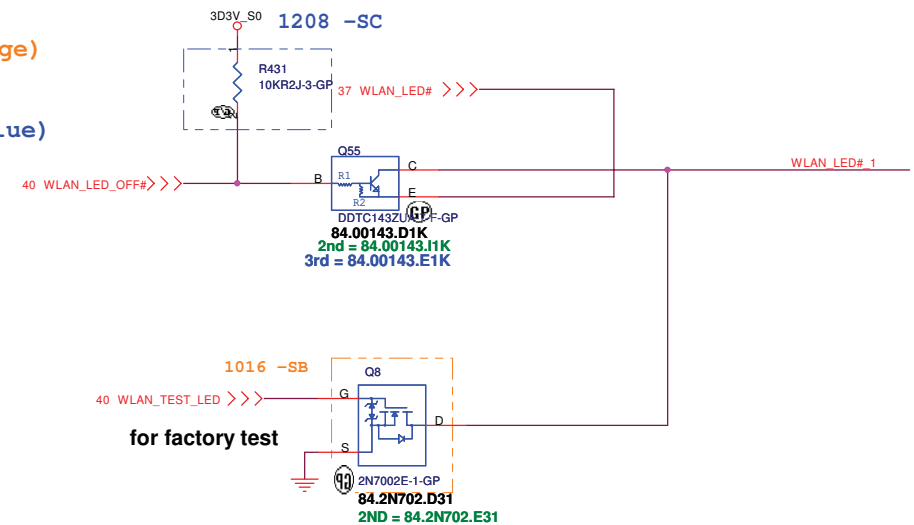
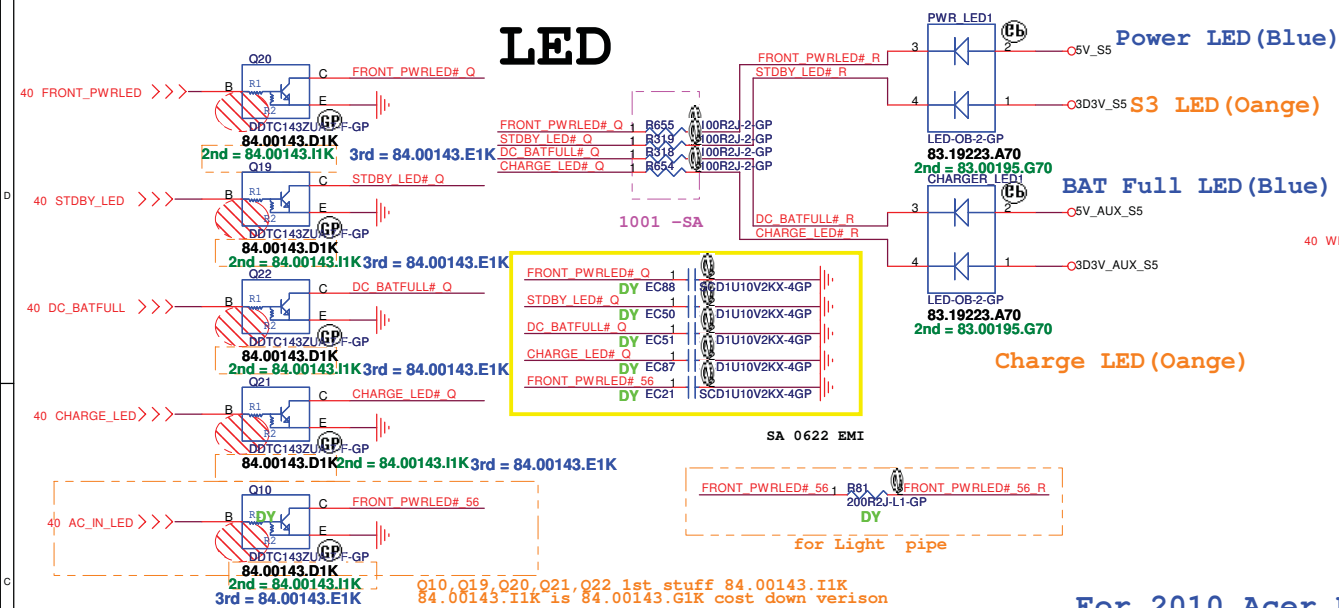
Eng stuff 20.K0498.006 Pin 1 ->right side
PD change to 20.K0373.006 pin 1 ->left side
so net mirror Vertically



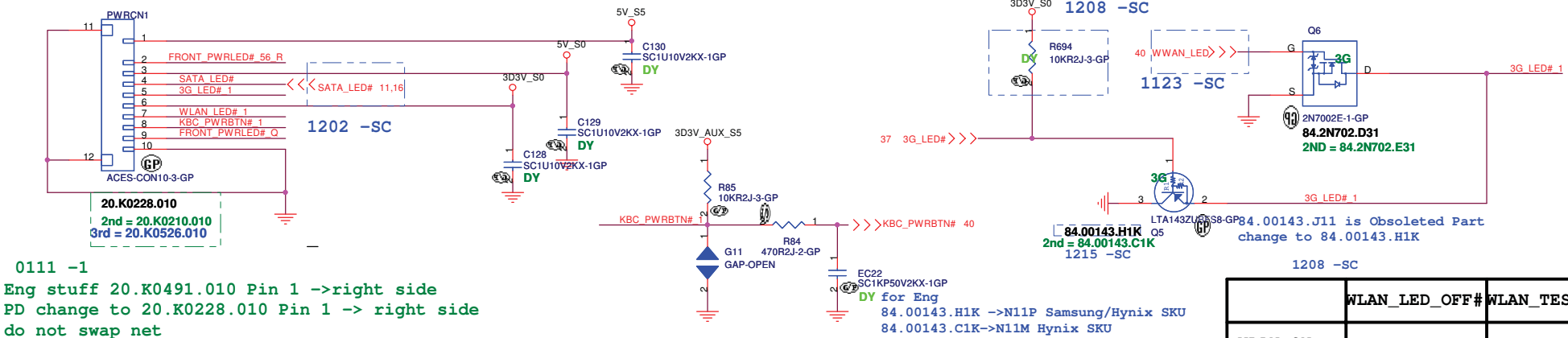
Discrete N11M

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title Touch PAD			
Size	Document Number	Rev	SC
Date: Friday, January 22, 2010	Sheet 43 of 72	HM42-CP	

LED



For 2010 Acer Project, WLAN and 3G LED control by KBC



Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

	WLAN_LED_OFF#	WLAN_TEST_LED	WWAN_LED
WLAN ON Always on	L	H	L
WLAN ON (flash)	H	L	L
WWAN_ON	L	L	H
WLAN ON WWAN_ON	L	L	H

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
LED&POWERBD CONN			
Size	Document Number		Rev
	HM42-CP		SC
Date:	Friday, January 22, 2010	Sheet 44 of 72	

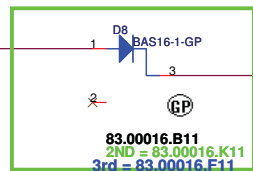
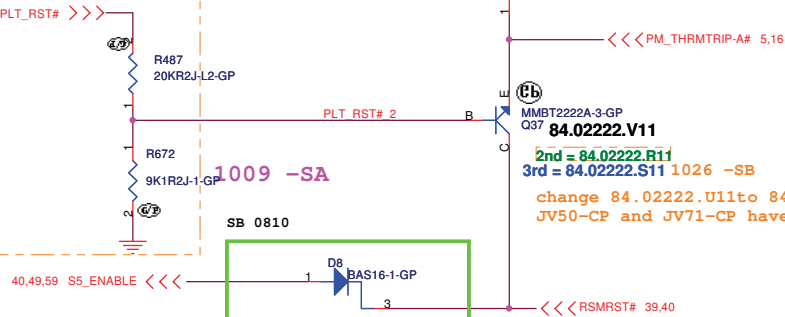
Run Power

3D3V_AUX_S5

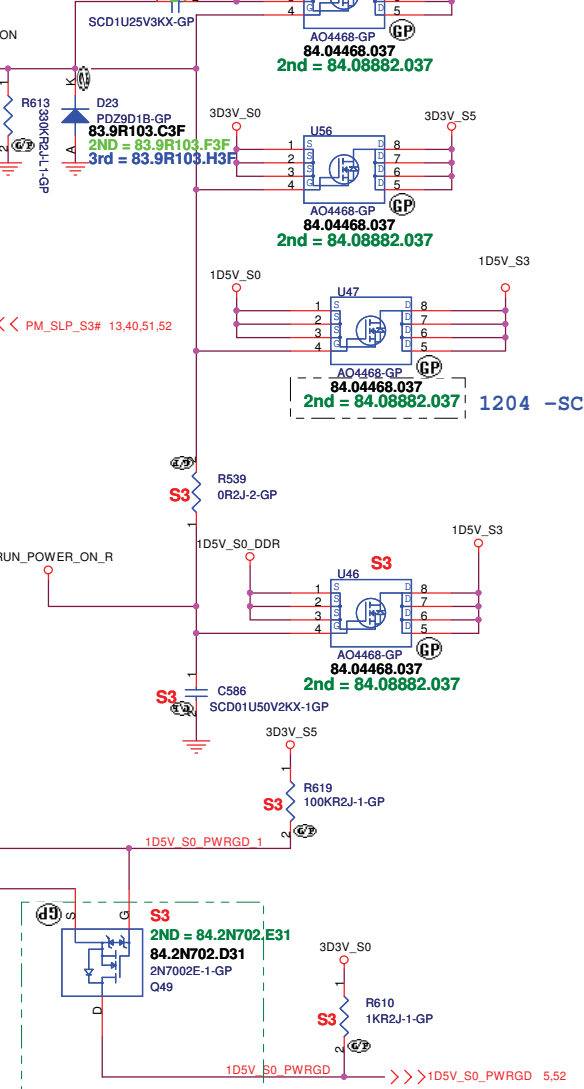
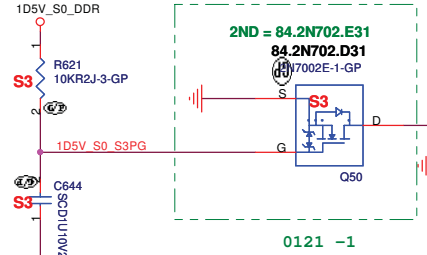
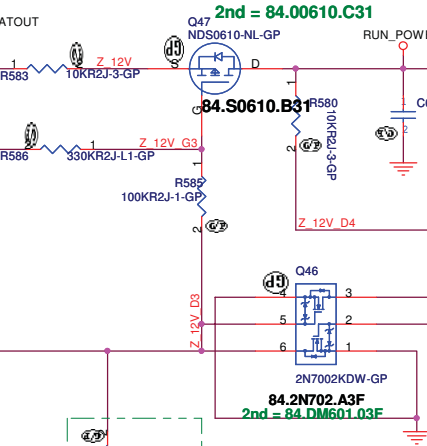
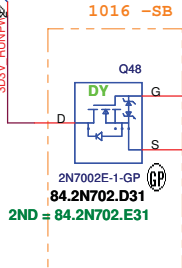
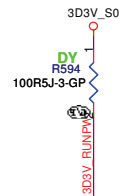
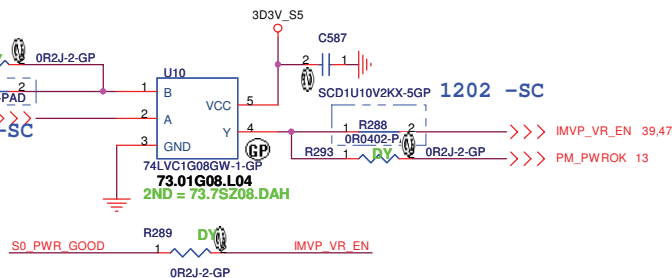
*Del Aux Power schematic,
it is not necessary for reservation*

1008 -SA

1014 -SA



1202 -SC



PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_S0
0	0	0	0
1	1	1	1

UMA

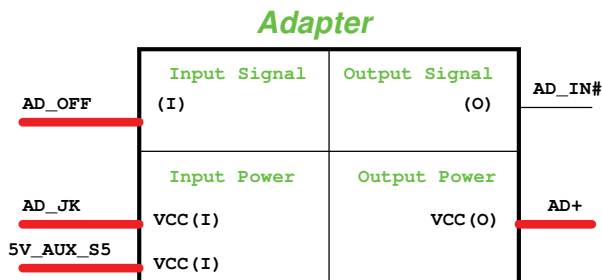
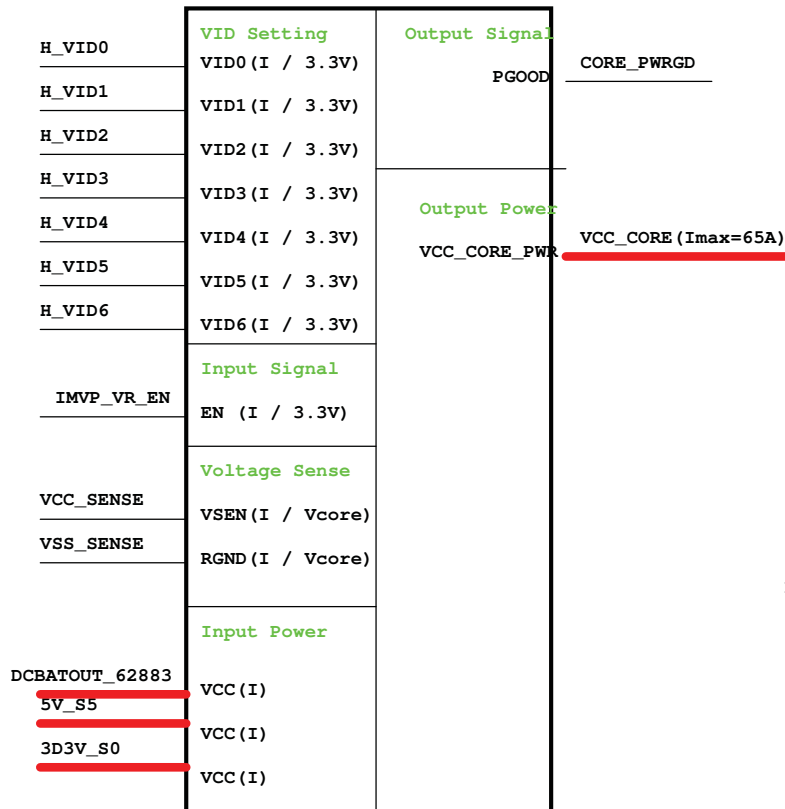
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and 3D3V AUX S5**

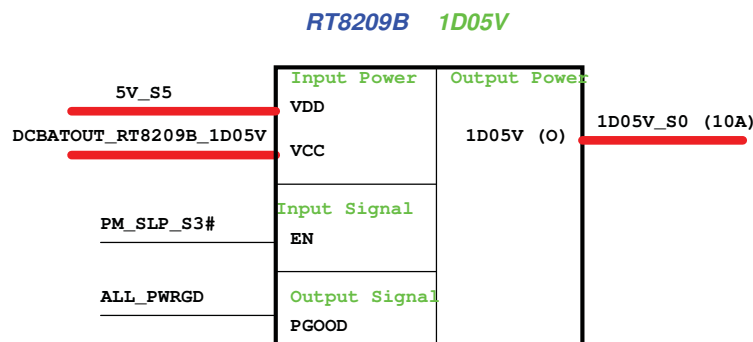
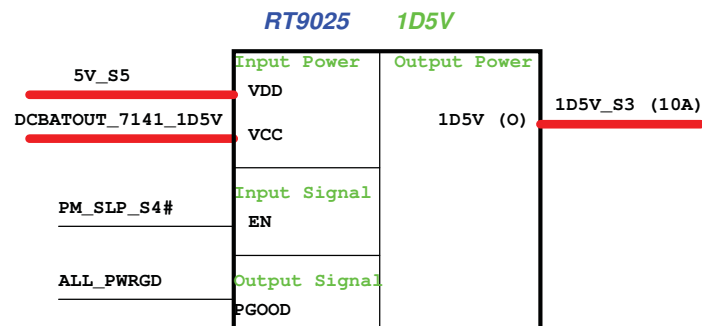
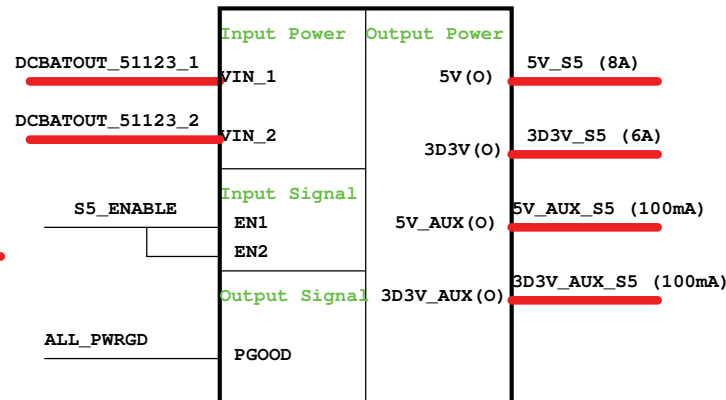
Size: Document Number **HM42-CP** Rev **SC**

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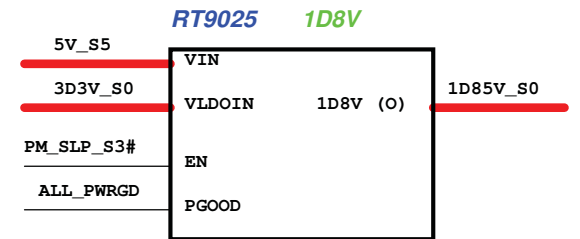
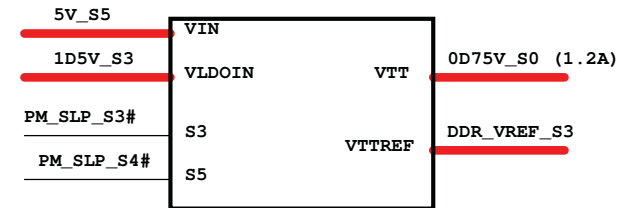
ISL62883 VCC_CORE



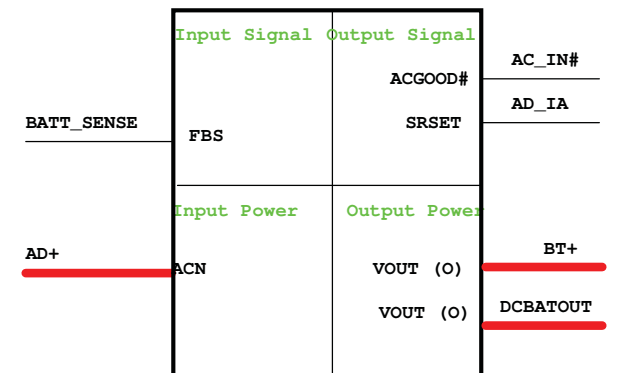
TPS51123 5V/3D3V



RT9026 0D75V_S0



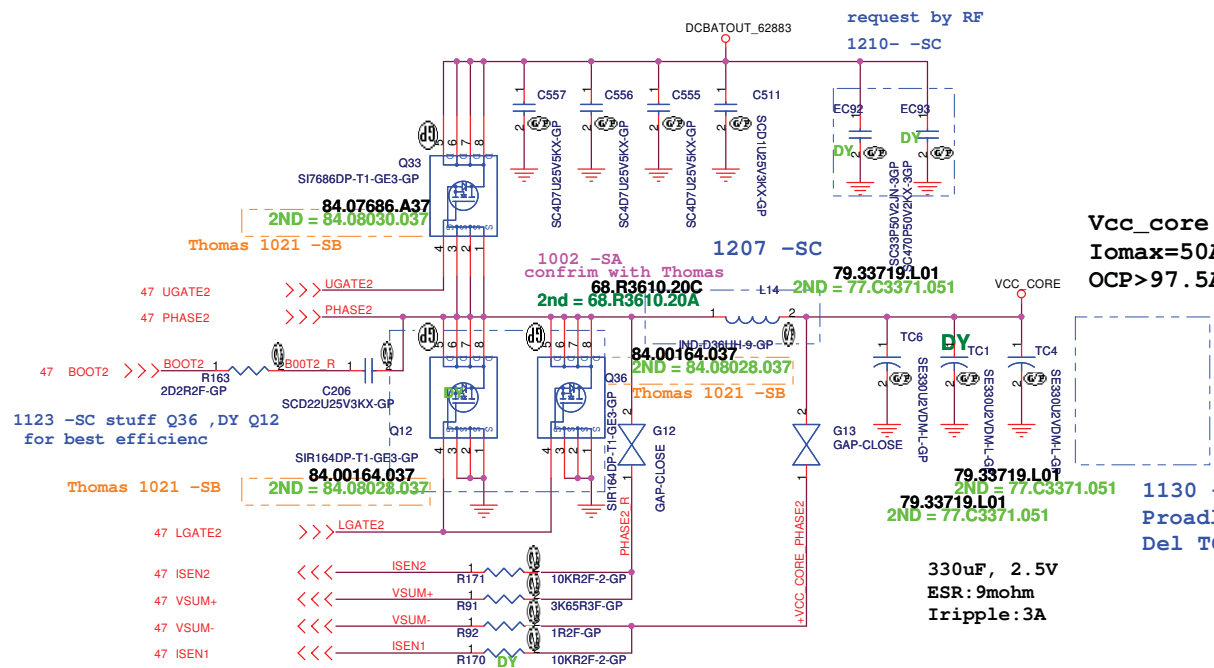
Charger BQ24745



Discrete N11M

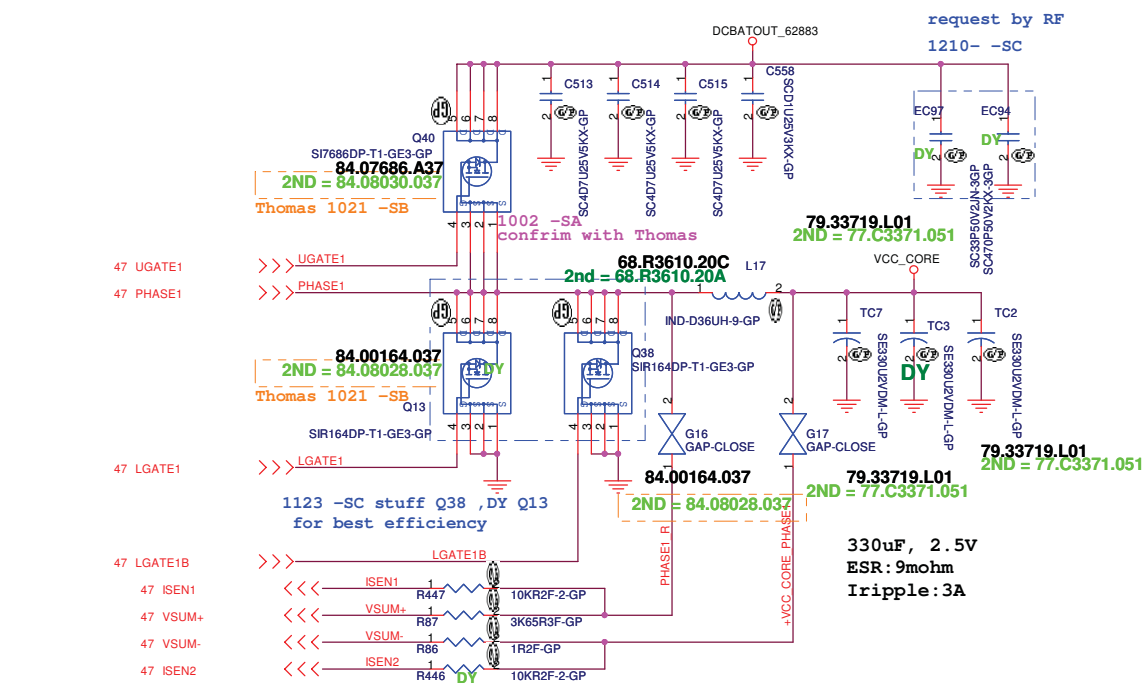
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Power Block Diagram		
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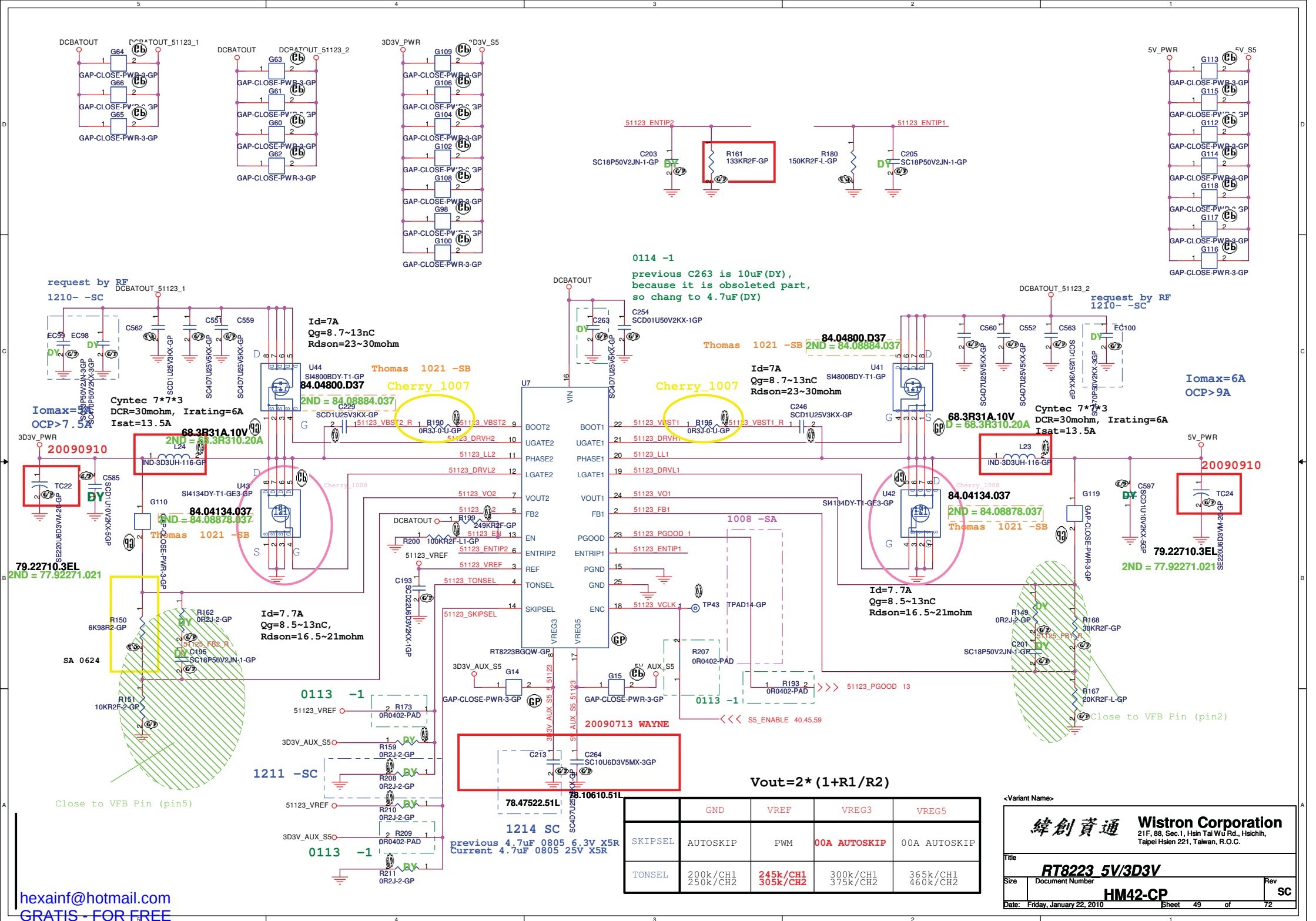


1130 -SC
Broadlizer Cap power team testing fail,
Del TC5 for co-layout

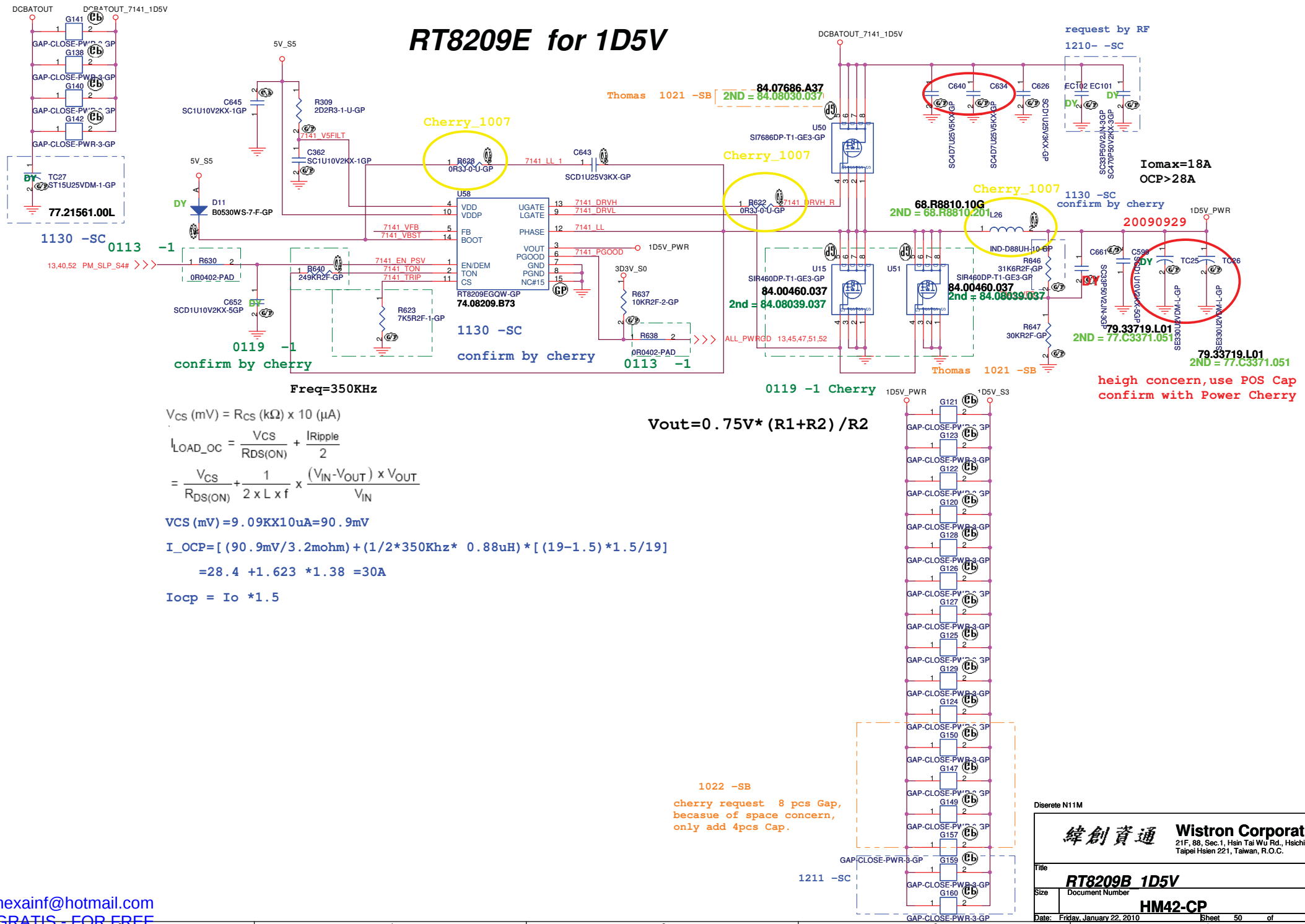
330uF, 2.5V
ESR: 9mohm
Irripple: 3A



330uF, 2.5V
ESR: 9mohm
Irripple: 3A



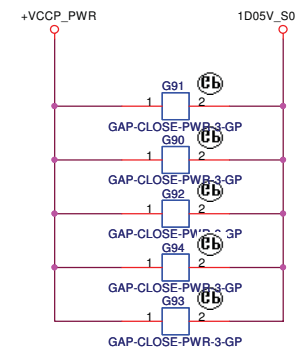
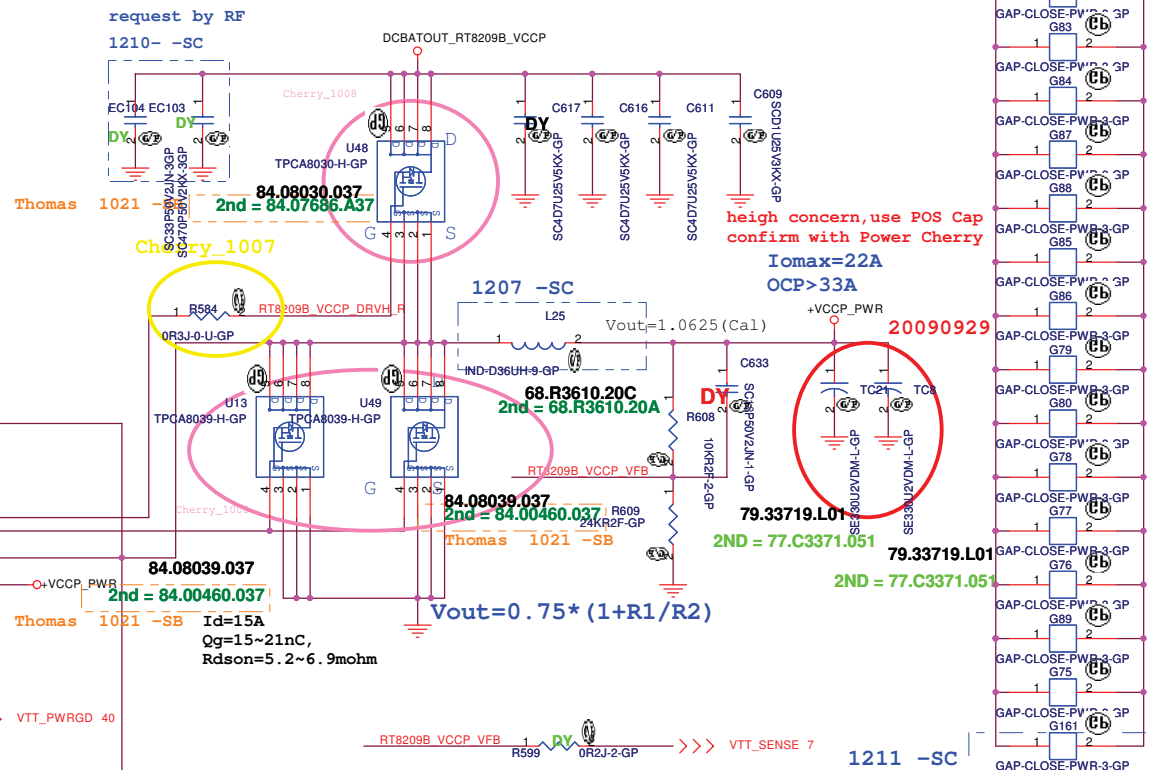
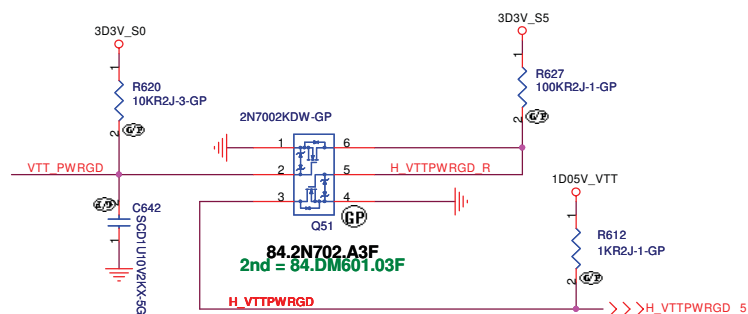
RT8209E for 1D5V



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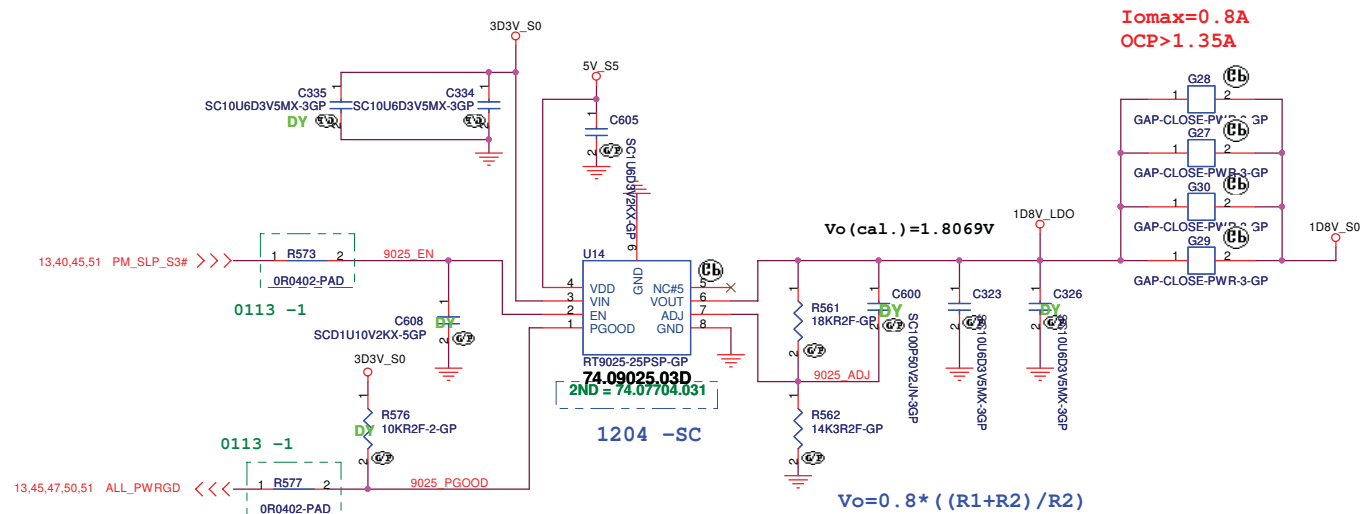


becasue of 1.05V_S0 and 1.05V_VTT combin together
use PM_SLP_S3# Enable 1.05V power

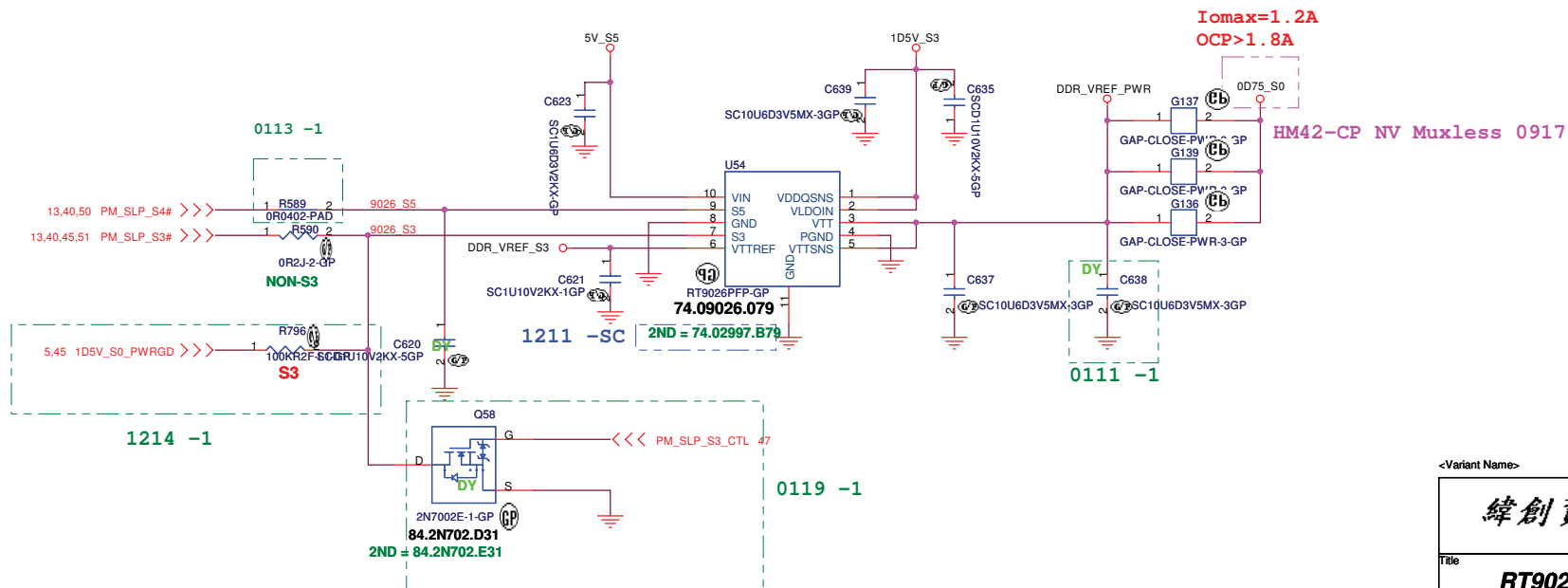


RT9025 for 1D8V_S0

20090915



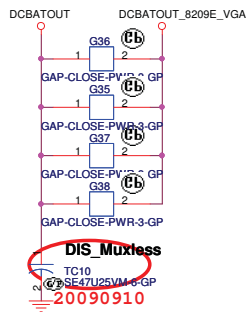
RT9026 for 0D75V_S0



<Variant Name>

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Title		RT9025 1D8V/RT9026 0D75	
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RT8208A for VGA

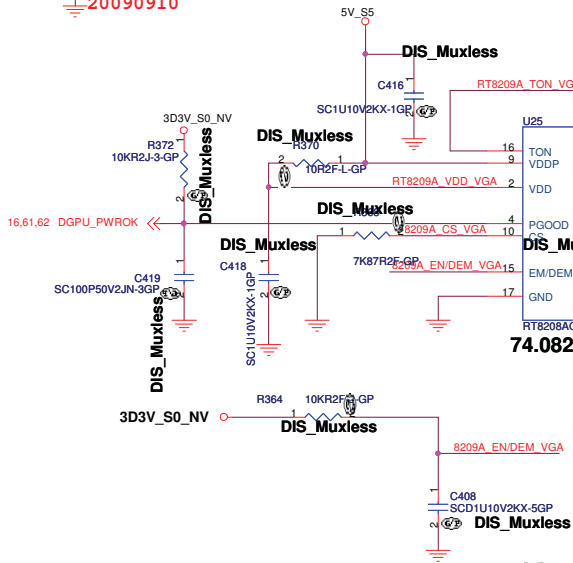


Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVDD
Performance (P0)	N11P-GE1	575	790	0.95 V
Performance (P0)	N11P-LP1	475	700	0.85 V
Balanced (P8)	N11P-GE1, N11P-LP1	405	324	0.85 V
Battery (P12)	N11P-GE1, N11P-LP1	135	135	0.80 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVDD
Performance (P0)	N11M-GE1	625	790	1.03 V
Performance (P0)	N11M-LP1	525	700	0.86 V
Balanced (P8)	N11M-GE1, N11M-LP1	405	405	0.85 V
Battery (P12)	N11M-GE1, N11M-LP1	135	135	0.85 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVDD
Performance (P0)	N11M-OP1	625	790	1.03 V
Performance (P0)	N11M-OP2	525	700	0.86 V
Balanced (P8)	N11M-OP1, N11M-OP2	405	405	0.85 V

N11P-GE1
For 40nm GPU the NVDD and GPIO5 (NVDD_ALTVO) /GPIO6 (NVDD_ALTIV1) relationship

GPIO6/NVDD_ALTIV1	GPIO5/NVDD_ALTVO	NVDD
0	0	0.8
0	1	0.85
1	0	0.95

N11M-GE1/N11M-OP1
For 40nm GPU the NVDD and GPIO5 (NVDD_ALTVO) /GPIO6 (NVDD_ALTIV1) relationship

GPIO6/NVDD_ALTIV1	GPIO5/NVDD_ALTVO	NVDD
0	1	0.85
1	0	1.03

RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2/R3)}{(R2/R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2/R4)}{(R2/R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2/R3/R4)}{(R2/R3/R4)} \times 0.75$

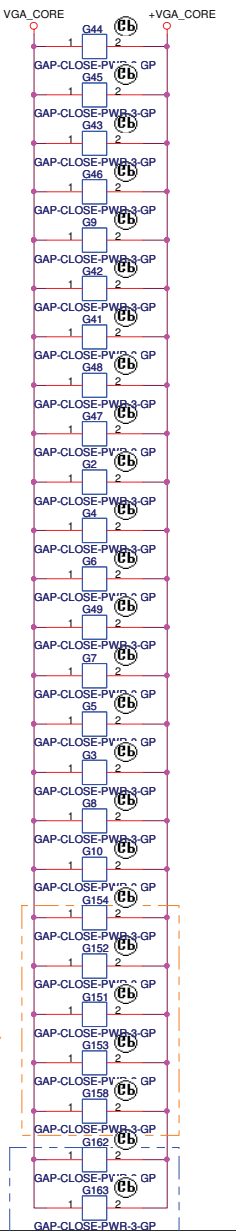
I_{max}=27A
OCP>40A

$$V_{out} = 0.75V * (R1+R2) / R2$$

68.3310.20C
2nd = 68.3310.20A

for 40nm GPU
32.4K of N11M
49.9K of N11P
11P-49.9K (64.49925.6DL)
11M-32.4K (64.32425.6DL)

cherry request 9 pcs Gap,
because of space concern,
only add 5pcs Cap.



UMA

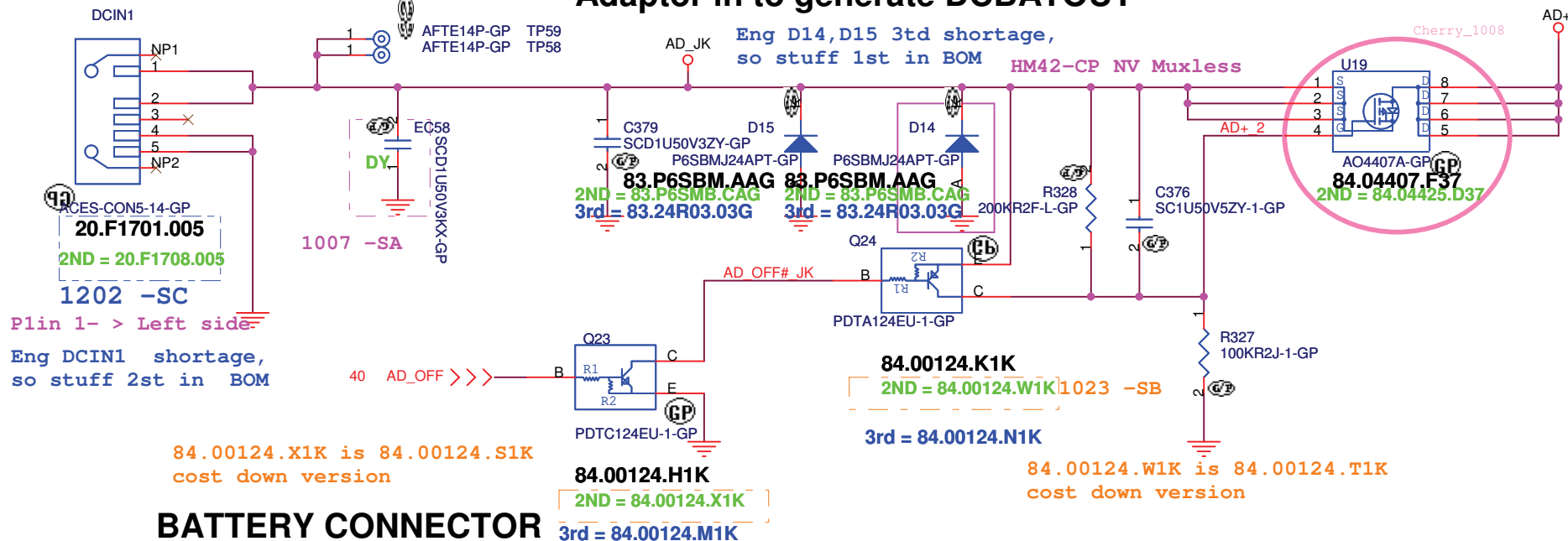
緯創資通 Wistron Corporation
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Title: **RT8209A VGA CORE**

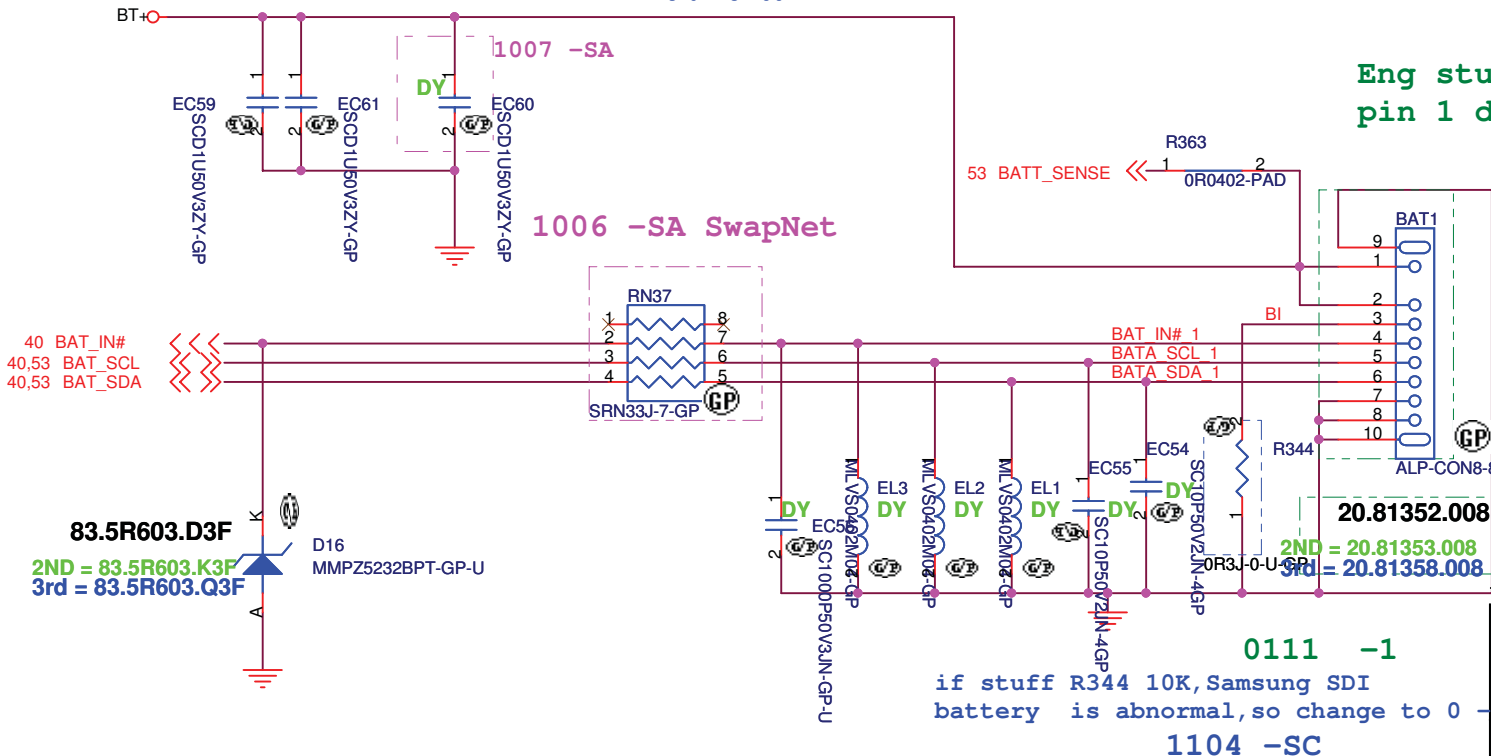
Size: Custom Document Number: **HM42-CP**

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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



Eng stuff 20.81340.008
pin 1 definition same,

• Pin Definition:

1	GND	Batt-, Battery Negative Terminal
2	GND	Batt-, Battery Negative Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	TH	Connect to Resistor to GND (10kΩ to GND)
6	BI	System present pin, low active
7	BATT+	Batt+, Battery Positive Terminal
8	BATT+	Batt+, Battery Positive Terminal

<Core Design>

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Title

AD/BATT CONN

Size

Document Number

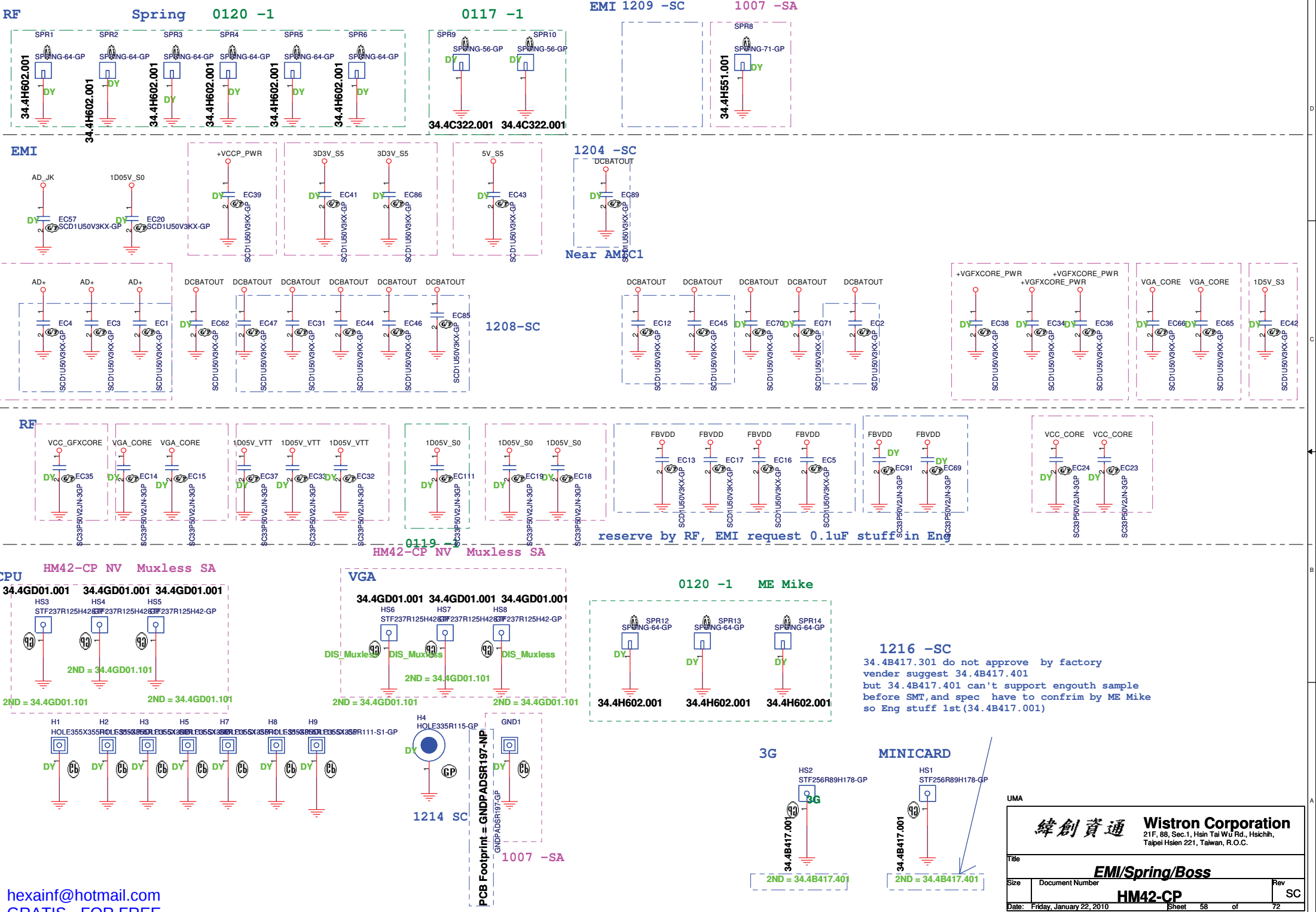
HM42-CP

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SC

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Check test point

~~delete 3D3V_S0 test point~~



Test Point放在Dimm Door打開可量測處

<Variant Name>

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Title

AFTE TP

Size

Document Number

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+3VS to 1.8V Transfer

+1.5V to FBVDD Transfer

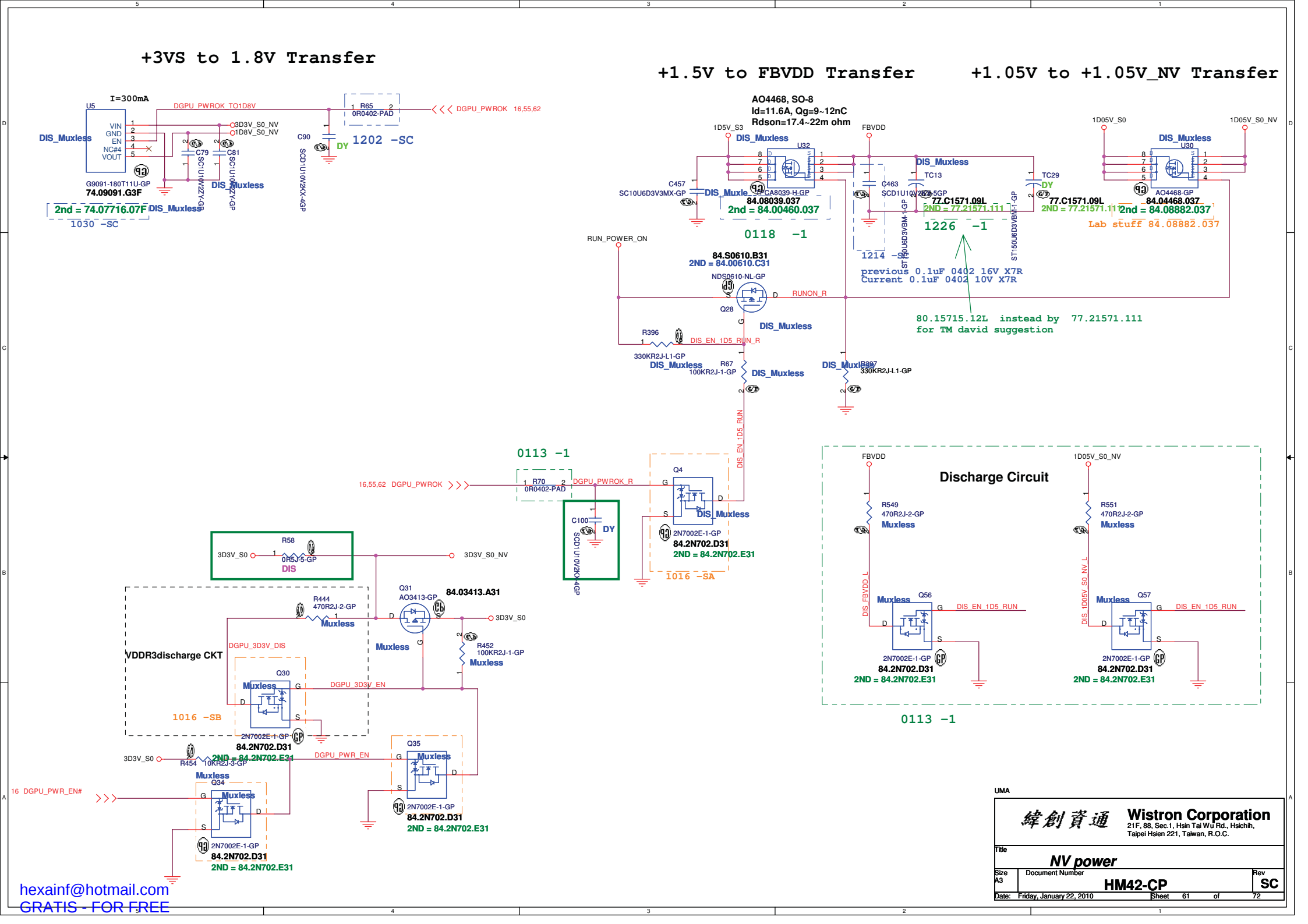
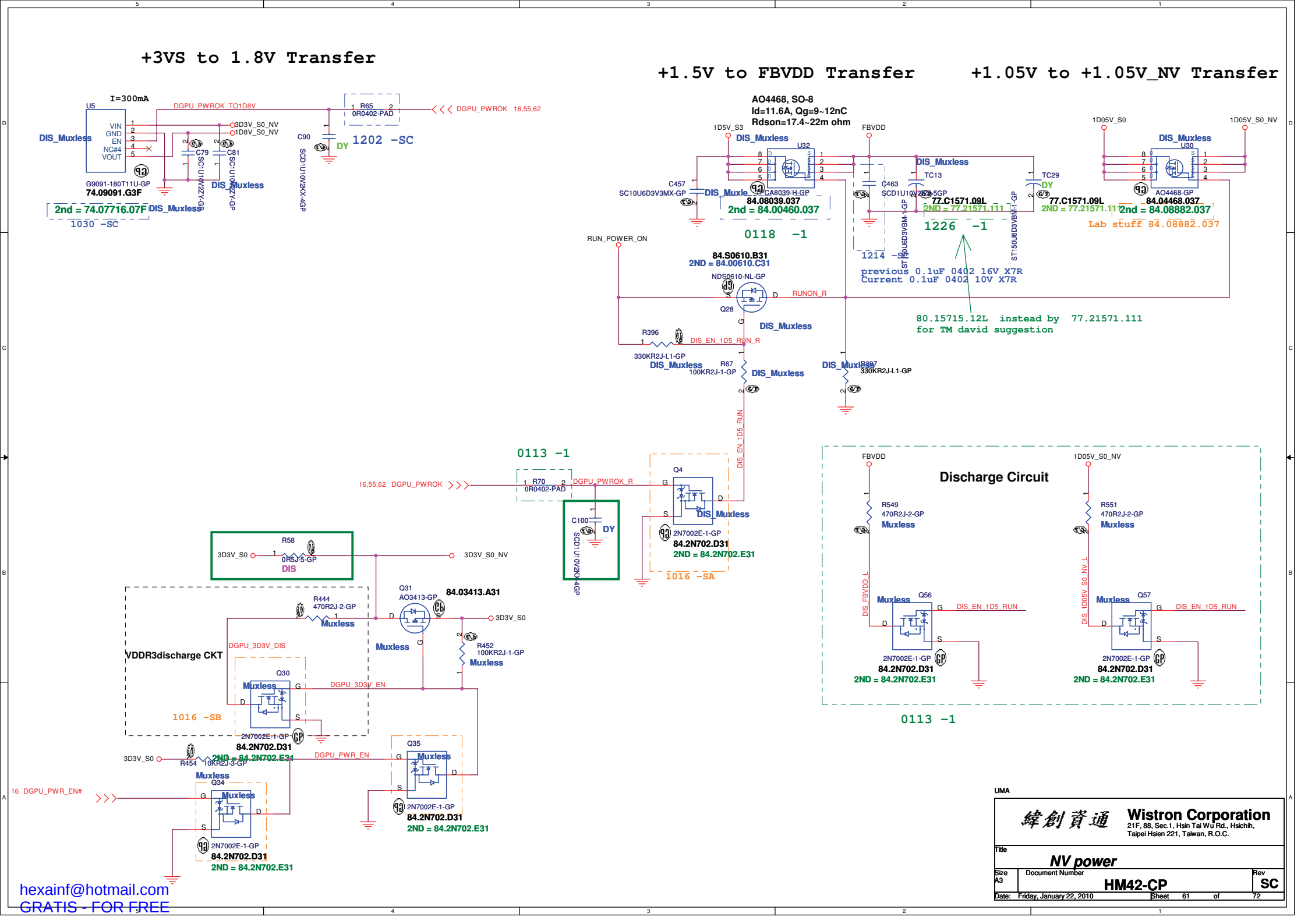
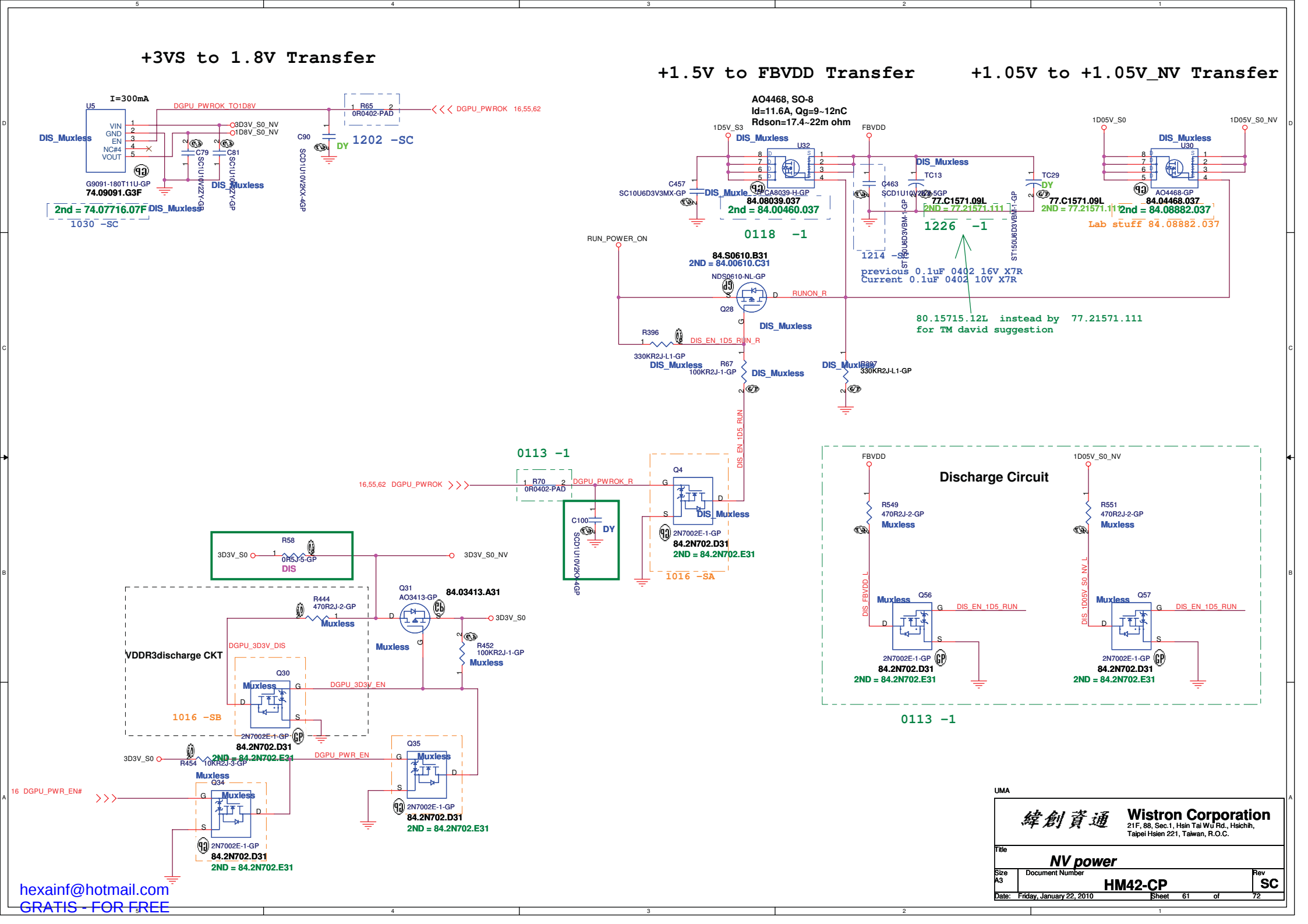
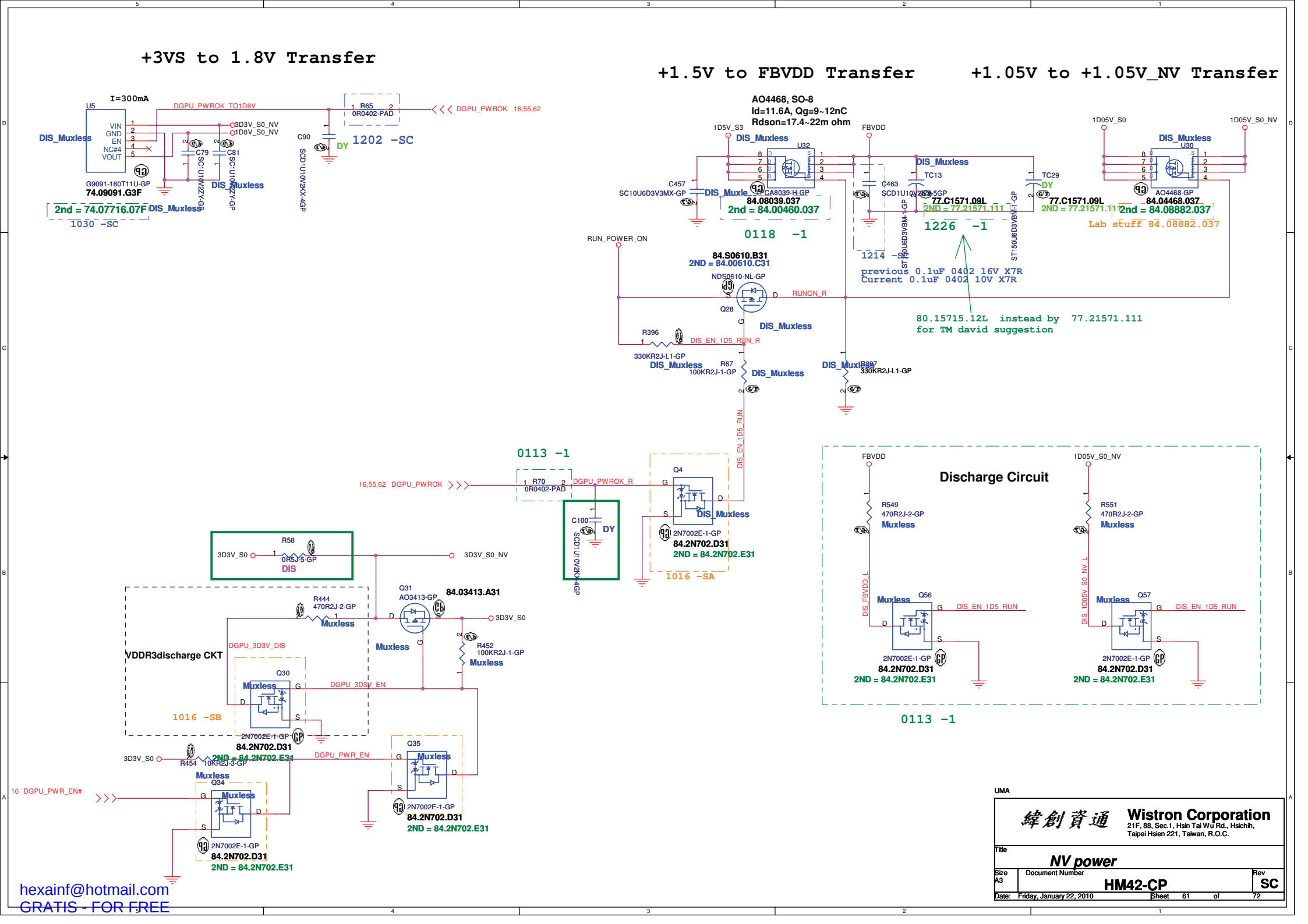
+1.05V to +1.05V_NV Transfer

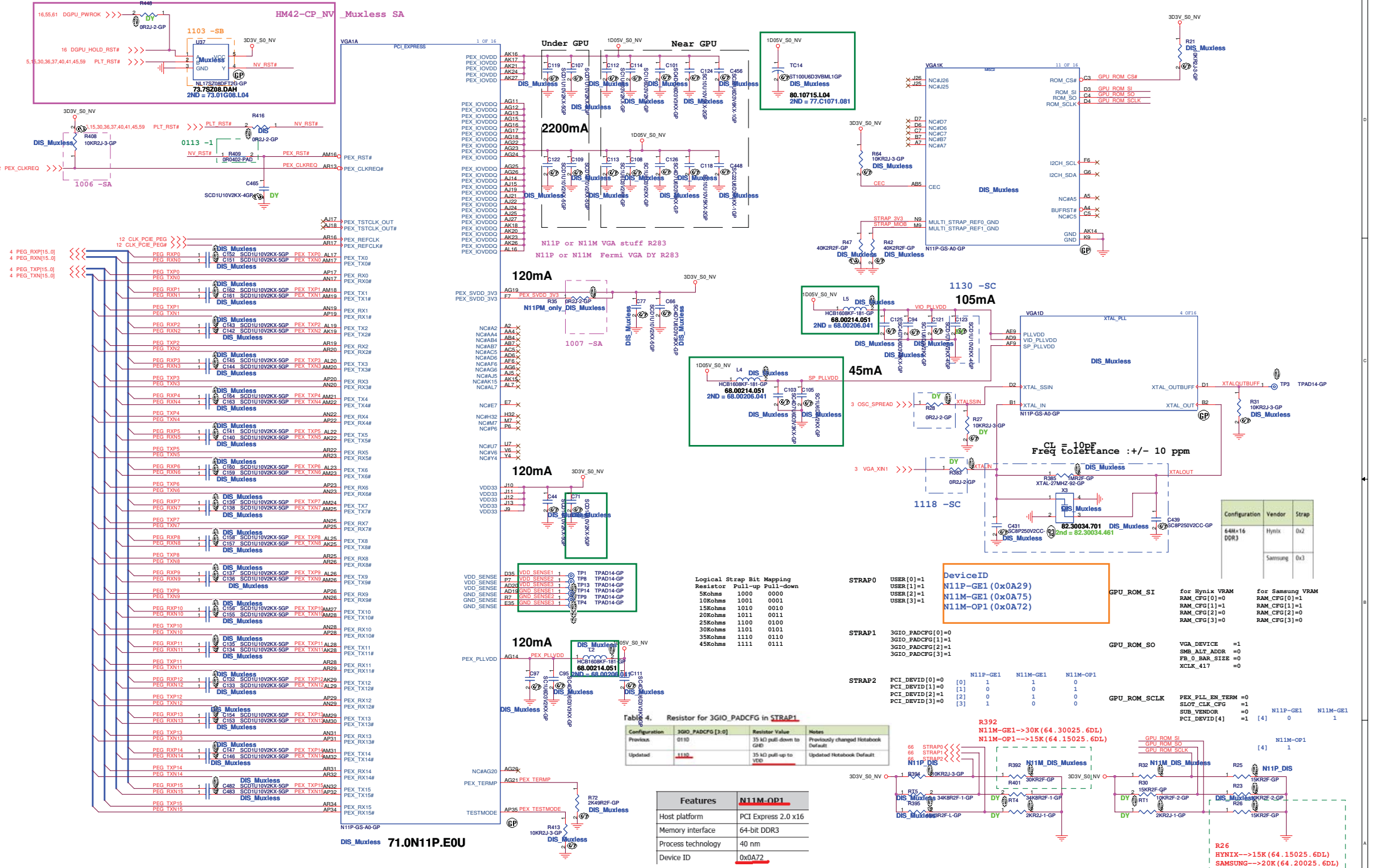
Discharge Circuit

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VGA 1 N11P-GE1 A3-->71.0N11P.GOU,
N11M-GE1-B -A3 -> 71.0N11M.EOU

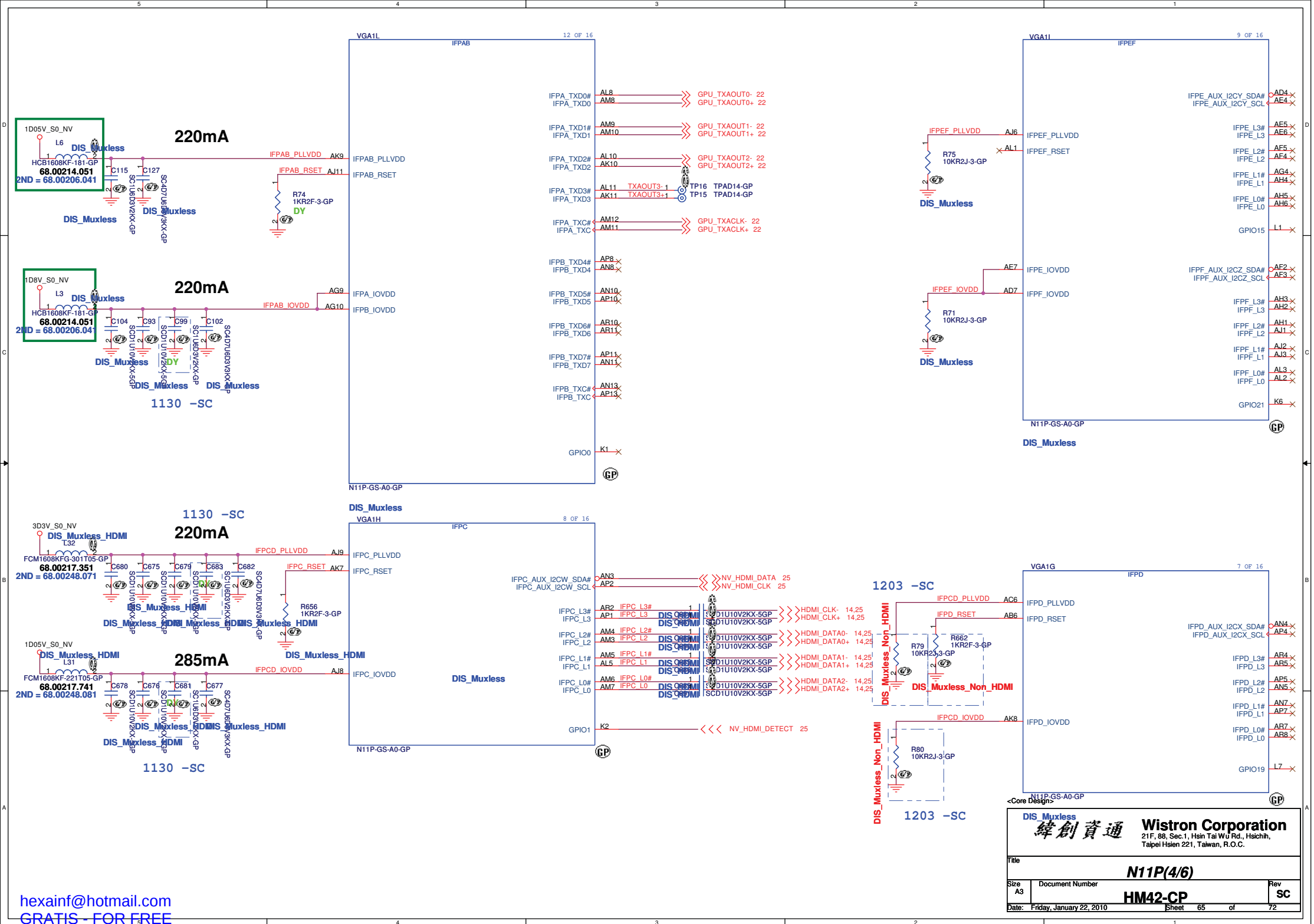
Chip	N11P-GS1-A2	N11P-GE1-A2	N11P-LP1-A2
Device ID	0x0A7A	0x0A29	0x0A28

Chip	N11M-GS1-B-A2	N11M-GE1-B-A2
Device ID	0x0A35	0x0A75

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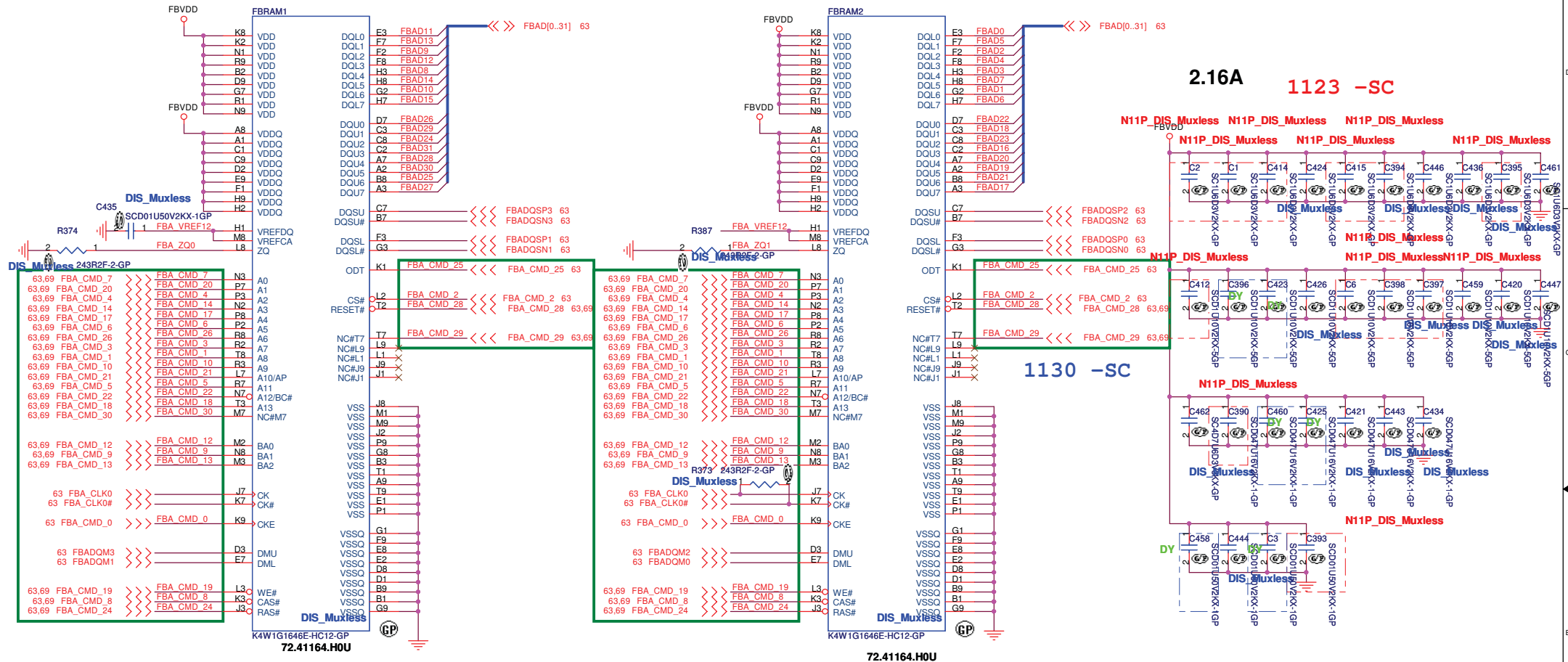
File: N11P(1/6) PEG
Size: A2
Date: Friday, January 22, 2010

Document Number: HM42-CP
Rev: SC

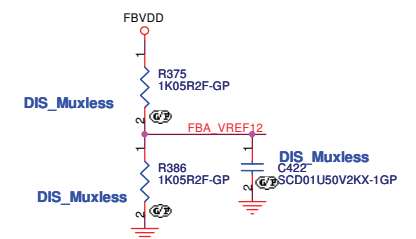




DDR3



SAMSUNG: 72.41164.H0U(Use OEM PN:VR.1GB0B.006)
HYNIX: 72.51G63.C0U(Use OEM PN: VR.1GB0G.004)

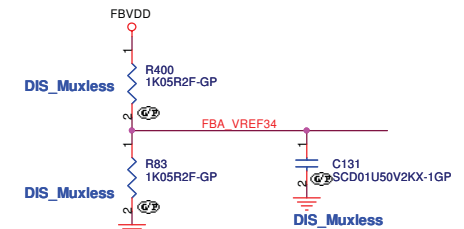
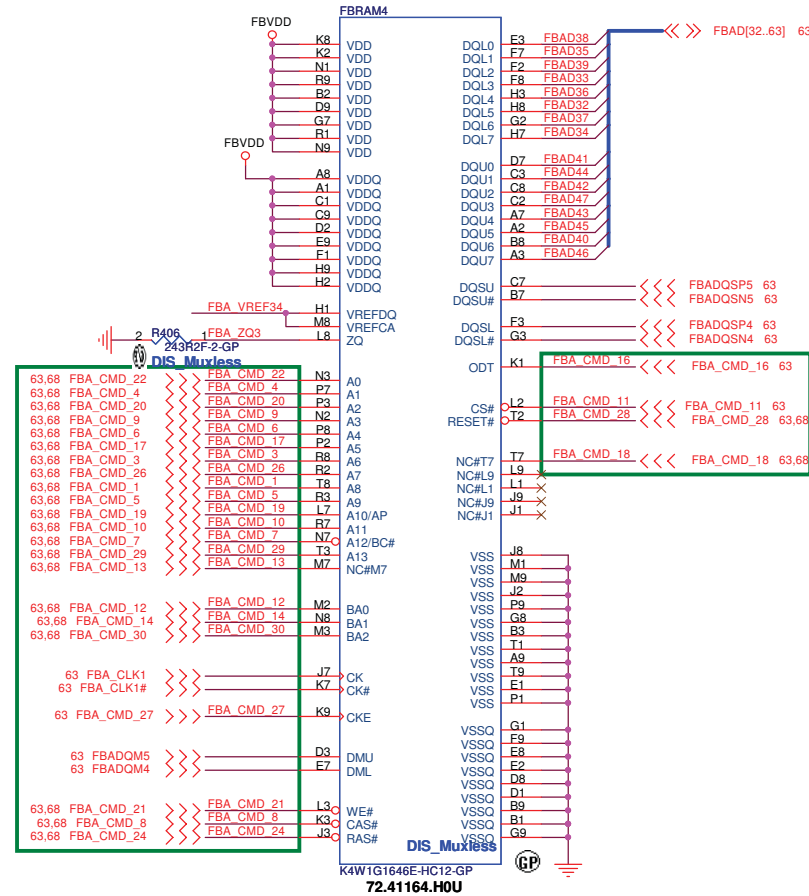
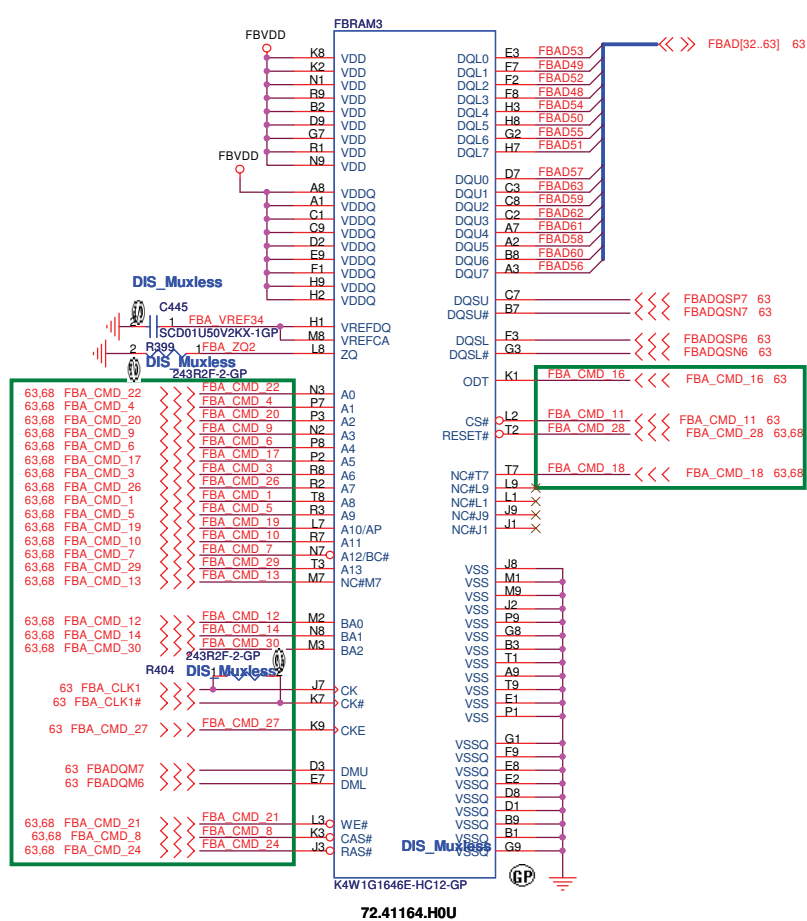


UMA

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Title			
VRAM(1/4)			
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DDR3



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

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Title

VRAM(2/4)

Size

	Document Number
--	-----------------

HM42-CP

Rev

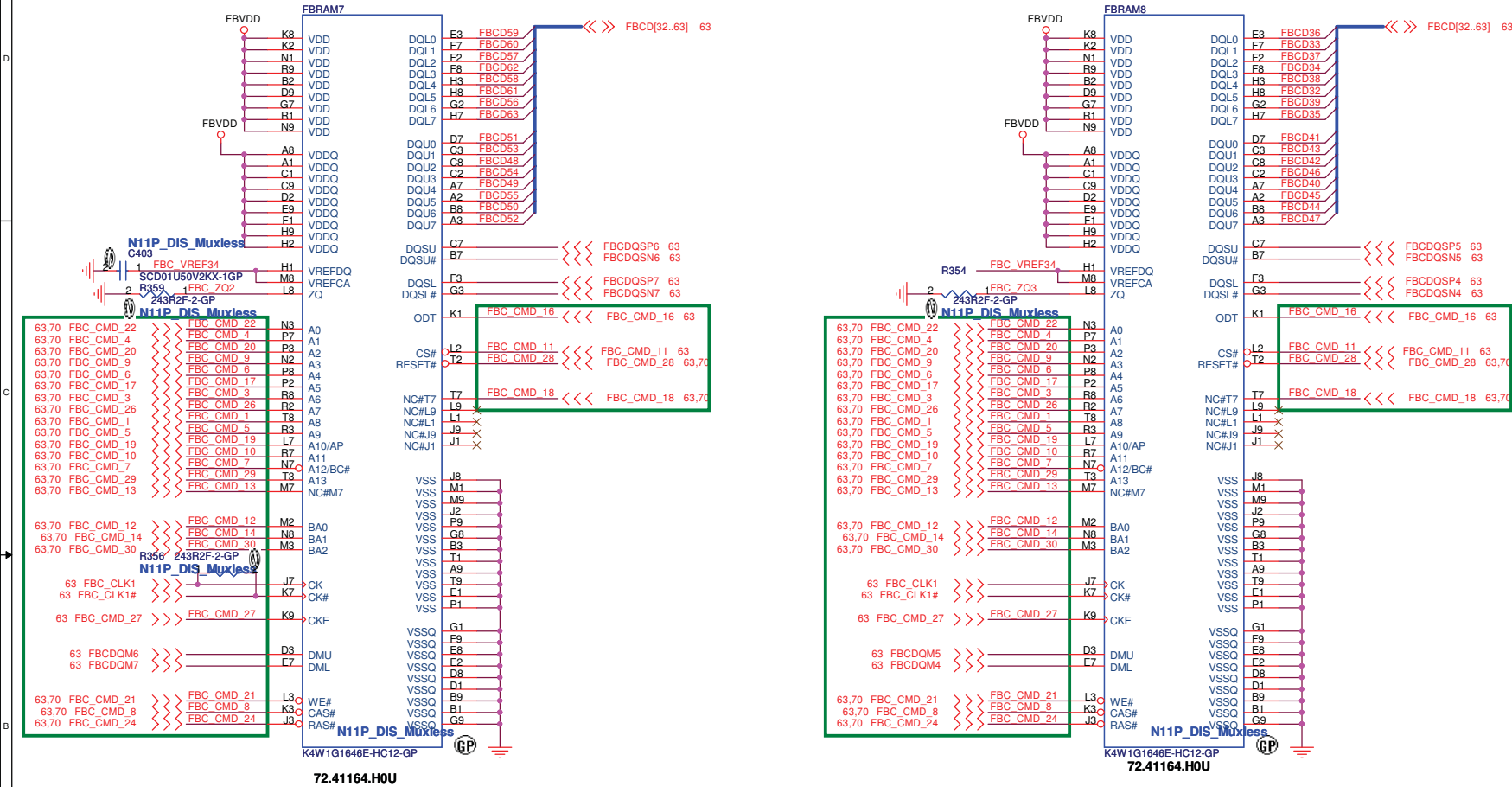
SC

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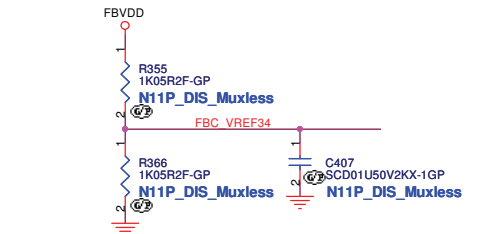
72

DDR3



SAMSUNG: 72.41164.H0U

HYNIX: 72.51G63.C0U



UMA

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Title			
VRAM(4/4)			
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3) Samsung VRAM FBRAM1~8 PN:VR.1GB0B.006

Hynix VRAM FBRAM1~8 PN:VR.1GB0G.004

4) VGA 1 N11P-GE1 A3->71.0N11P.G0U,
N11M-GE1-B -A3 -> 71.0N11M.E0U
N11M-OP1 ->

6) VGA 1 N11P-GE1-> R53 49.9K(64.49925.6DL)
N11M-GE1 -> R53 32.4K(64.32425.6DL)

7) R26 stuff Hynix VRAM : 15K(64.15025.6DL)
Samsung VRAM : 20K(64.20025.6DL)

8) R45 stuff N11M use 60.4 ohm (64.32425.6DL)
N11P use 40.2 ohm (64.40R25.6DL)

9) Muxless SKU stuff R181 2.37K (64.23715.6DL)
UMA SKU Stuff R181 2.4K (64.24015.6DL)

10) N11M OP1 ->R392 15K(64.15025.6DL)
N11M GE1 ->R392 30K(64.30025.6DL)

Mini Card 2nd and 3rd source PN confirm

Card Reader 2nd source confrim

[ECR]

Date	released by	ECR Number
11/22	Anita	R1001240

[Old]

PCH1 PN : 71.0IBEX.A0U

[New]

PCH1 PN : 71.0HM55.00U(KI.G5501.002)

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[lab -SB]

2nd -> UMA (S01G)

1st -> Diserete N11P Hynix(S02G)

1st +3rd -> Diserete N11M Hynix(S03G)

2nd +4th -> Diserete N11M Samsung(S04G)

1st -> Diserete N11P Samsung (S05G)

2nd -> N11M Hynix_support Optimus (S06G)

[Eng -SC]

2nd -> UMA Non 3G (55.4GY01.S07G)

1st -> Diserete N11P Hynix_3G(55.4GZ01.S03G)

1st +3rd -> Diserete N11M Hynix_3G(55.4GY01.S09G)

2nd +4th -> Diserete N11M Samsung_Non 3G(55.4GZ01.S02G)

1st + 5th -> Diserete N11P Samsung _3G(55.4GY01.S10G)

1st +3 rd -> UMA Non 3G Non HDMI (55.4GW01.S01G)

[PD -1]

UMA 3G (55.4GY01.M01G)

Diserete N11P Hynix_3G(55.4GY01.M02G) => 1st

Diserete N11P Hynix_Non 3G(55.4GY01.M03G) => 2nd

UMA Non 3G (55.4GY01.M04G)

Diserete N11M Hynix_3G(55.4GY01.M05G)

Diserete N11P Samsung _3G(55.4GY01.M06G) =>1 st

Diserete N11M Samsung_Non 3G(55.4GY01.M07G)

[PD action]

qual TPCN1 2nd source(20.K0296.006)

qual KB1 2nd source(20.K0382.026)

qual HDMI 2nd and 3rd

qual ODD1 3rd source(62.10065.E01)

qual PWRCN1 2nd and 3rd

qual RTC1 4th source

qual BT1 2nd and 3 source

qual U51 and U15 2nd source

qual TC13 2nd source(77.21571.111)

qual U32 2nd source

Qual HS1,HS2 2nd: 34.4B417.401

UMA

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Title

Modify History

Size

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