Tahoe Block Diagram

Project code: 91.4T901.001
PCB P/N : 48.4T901.0SA
REVISION : 06252-SA

CLK GEN.
ICS 9LPRS502
(RTM875T-605) 3
71.09502.00W

Mobile CPU
Merom 479
2G/2.33G
2.0G : 71.MEROM.A0U
2.33G : 71.MEROM.B0U
4, 5

G792 20

HOST BUS 667/800MHz@1.05V

DDR2 533/667 MHz 12,13
533/667MHz

DDR2 533/667 MHz 12,13
533/667MHz

Crestline
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CREST.00U
6,7,8,9,10,11

X4 DMI 400MHz
C-Link0

TV Out 15
CRT 15
LCD 14
VGA Borad 27

Line In
MIC In 30
INT.SPKR 30
Line Out (SPDIF)

Codec ALC268 29
AZALIA

OP AMP G1431Q 30
OP AMP G1412 30

MODEM MDC Card 22
RJ11

ICH8M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
3 SATA
1 PATA 66/100
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
71.0ICH8.A0U
16,17,18,19

PCI BUS
OZ129 1394 CardReader 25
1394 CONN 26
Cardreader
MS/MS Pro/xD/ MMC/SD 5 in 1 26

Giga LAN 23 BCM5787MKMLG
TXFM 24
RJ45 24

PCIex1
Mini Card Kedron a/b/g/n 28

LPC BUS
MINI USB BlueTooth 22
KBC Winbond WPC8768L 31
SPI I/F
BIOS W25X80-VSS 33
LPC DEBUG CONN. 33

New card 28
PCI Express
P2231NFC1 28
SATA
HDD 21
PATA
CDROM 21
USB
USB 4 Port 22
CAMERA 14
MEDIA BD 32
Touch Pad 32
INT. KB 32
CIR 31

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC MAX8744 38

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A)

SYSTEM DC/DC Max8717 39

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9.5A) 1D8V_S3(8.5A)

TPS51100 41

1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5915 41

1D8V_S3	1D25V_S0 (2A)

APL531230

3D3V_S0	2D5V_S0 (300mA)

APW5912 40

3D3V_S5	1D5V_S3 (7.5A)

CHARGER MAX8731 41

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC MAX8770 35,36

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

<Core Design>

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: Tahoe | Rev: -1
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ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	FT
4	USB3
5	BLUETOOTH
6	NC
7	MINICARD
8	WEBCAM
9	NEW1

UMA

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Title: Reference

Size A3 | Document Number: Tahoe | Rev: -1

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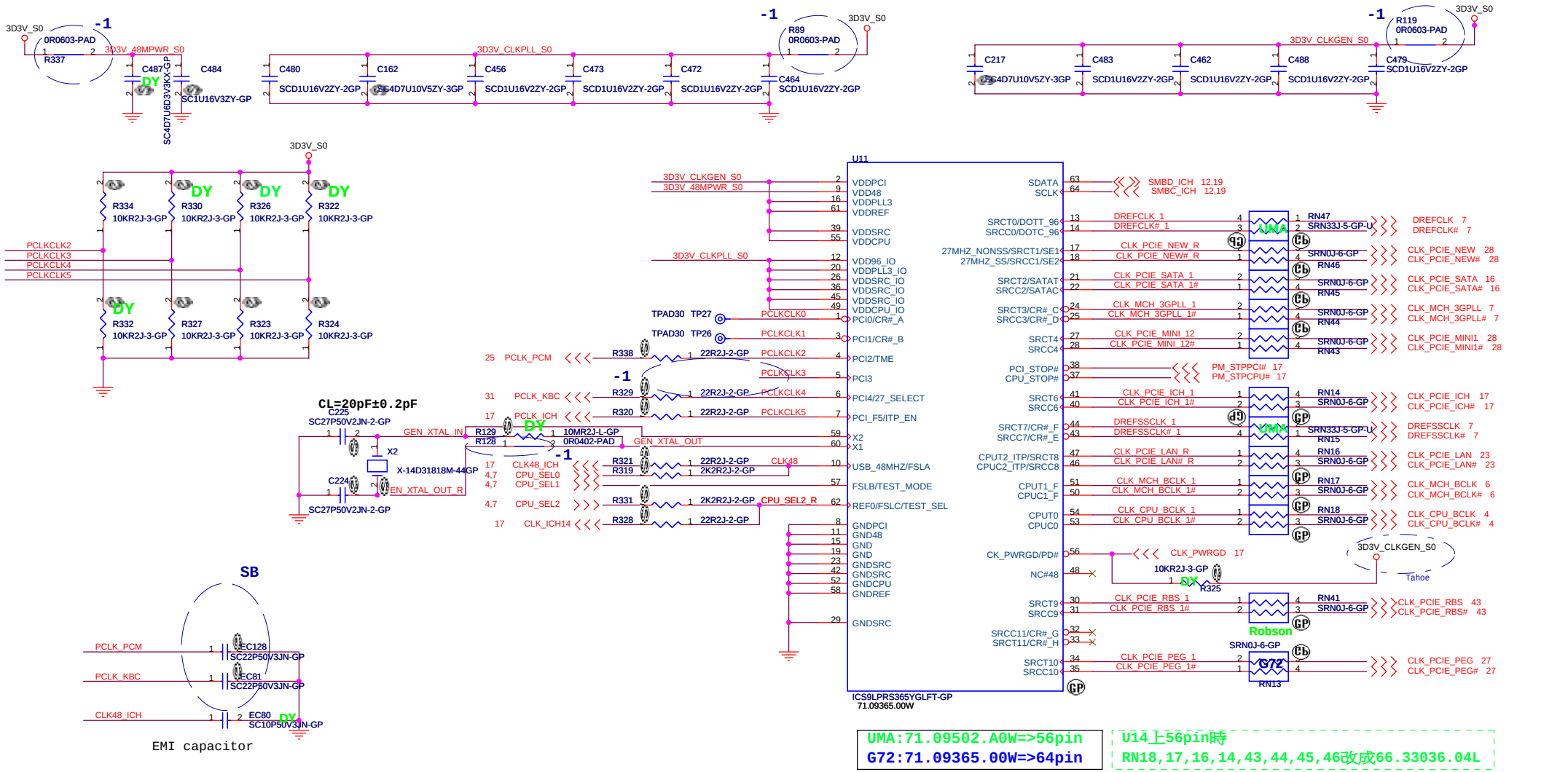

UMA:71.09502.A0W=>56pin
G72:71.09365.00W=>64pin

U14上56pin時
RN18,17,16,14,43,44,45,46改成66.33036.04L

ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

UMA

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Title: Clock Generator

Size	Document Number	Rev
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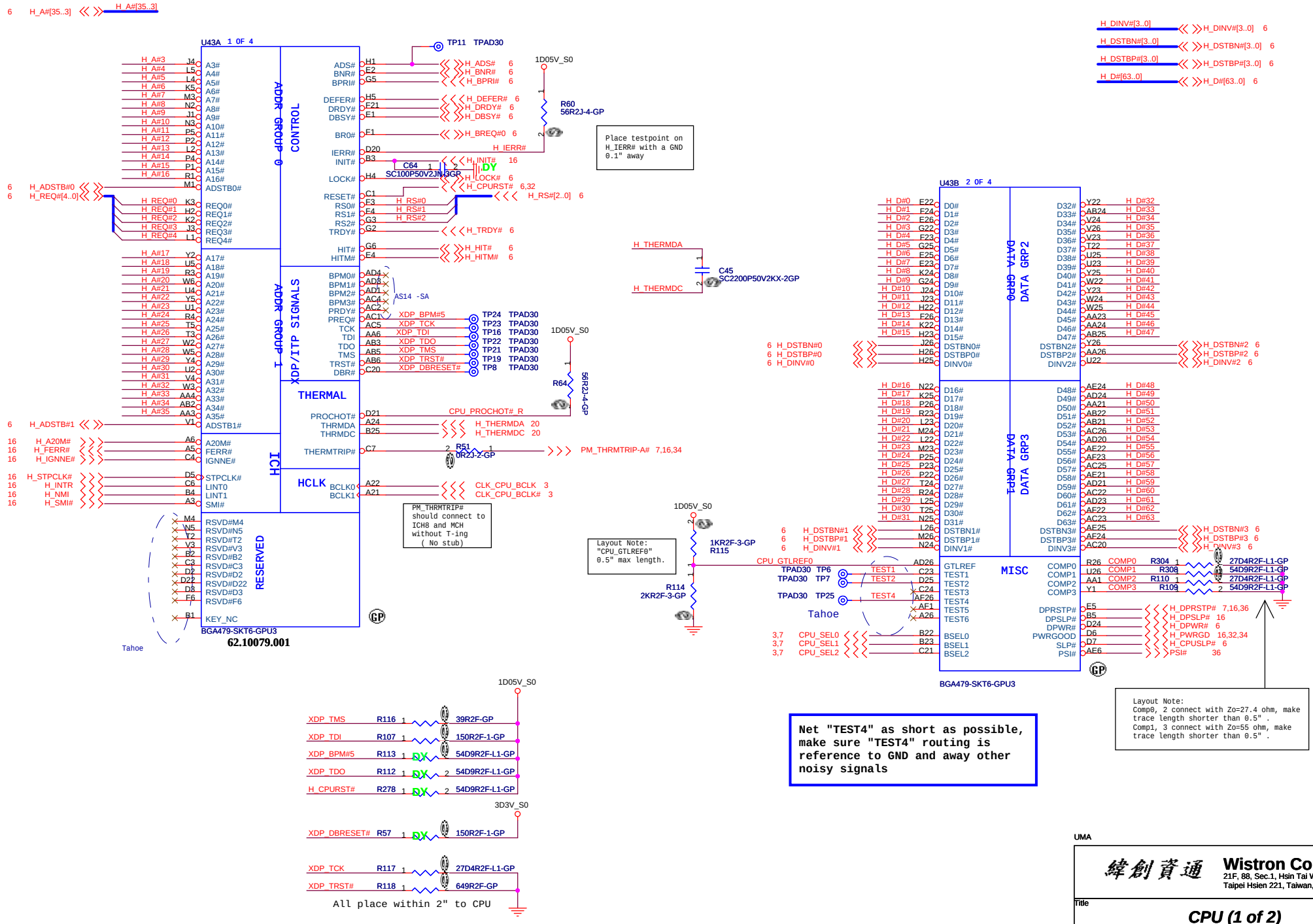

UMA

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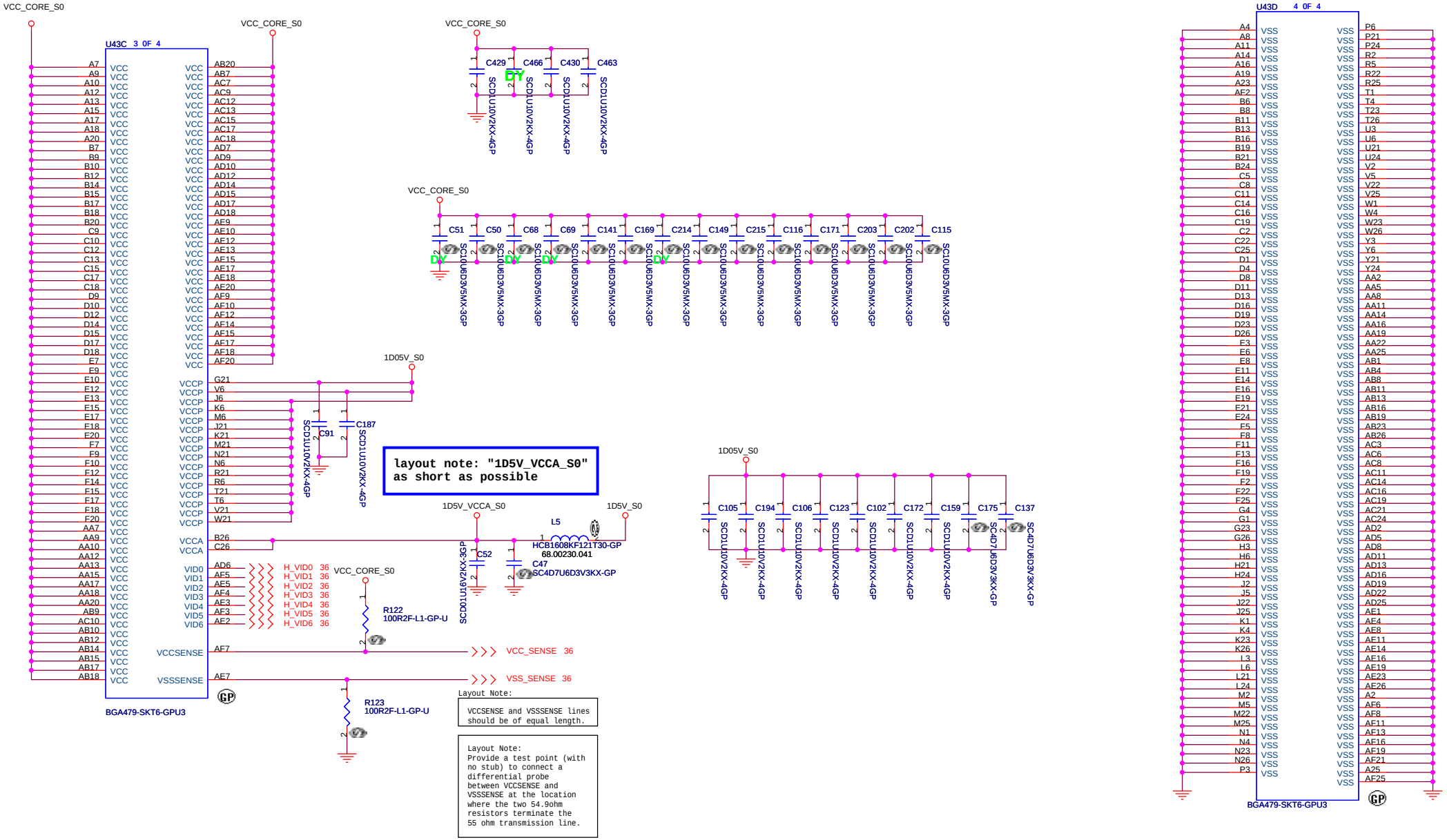
Title: **CPU (1 of 2)**

Size	Document Number	Rev
	Tahoe	-1

Date: Friday, April 27, 2007 Sheet 4 of 44



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Title	CPU (2 of 2)	
Size	Document Number: Tahoe	Rev: -1
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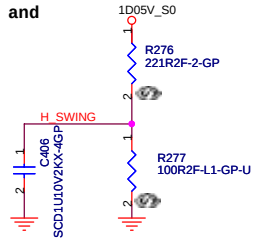
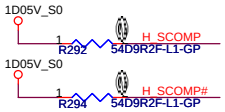
H_SWING routing Trace width and Spacing use 10 / 20 mil

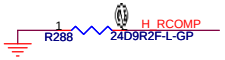
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

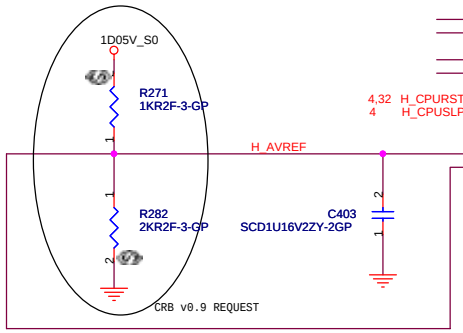


H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil



UMA

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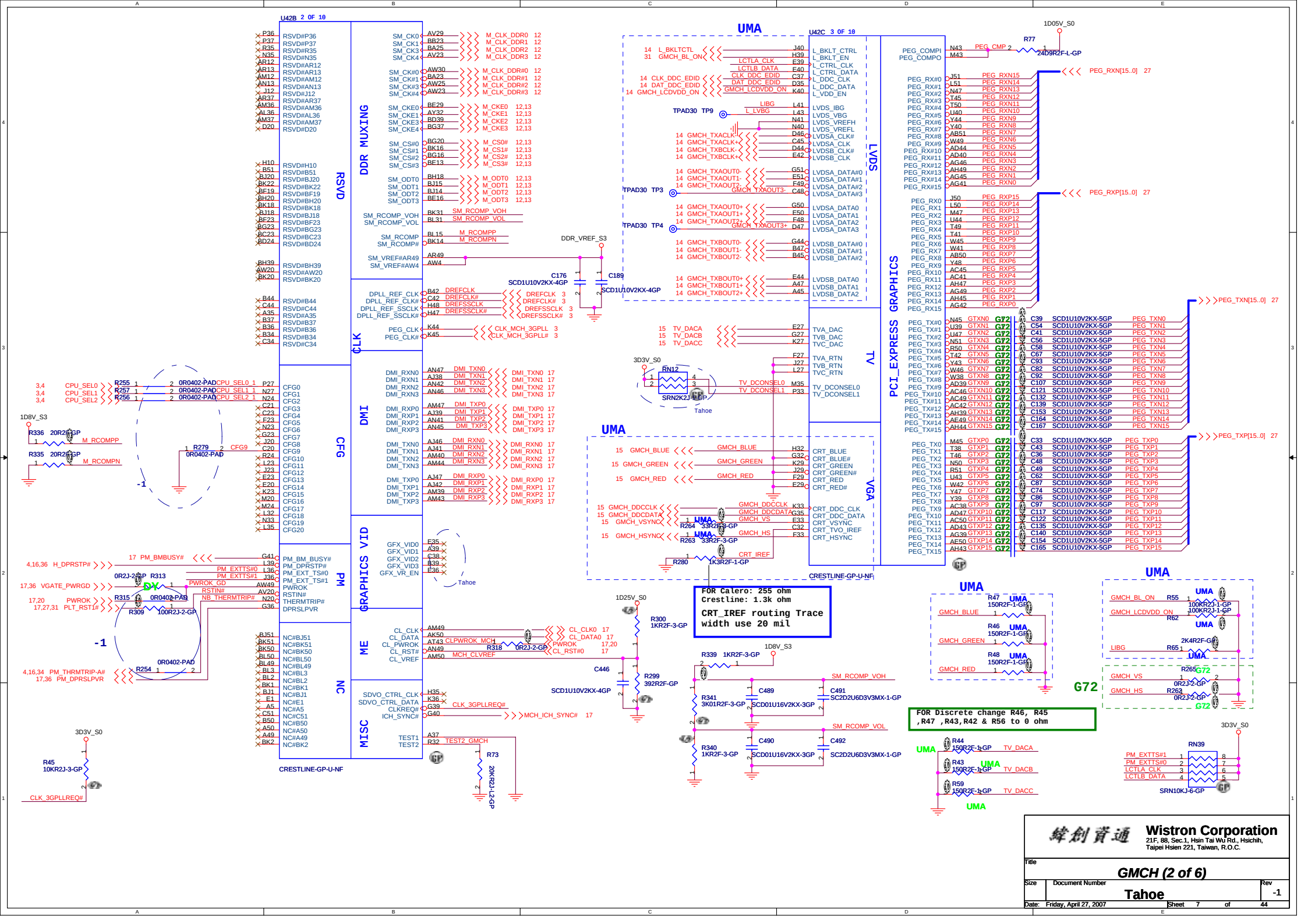
Title: GMCH (1 of 6)

Size | Document Number: Tahoe | Rev: -1

Date: Friday, April 27, 2007 | Sheet 6 of 44


U42B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
CRESTLINE-GP-U-NF
UMA
U42C 3 OF 10
LVDS
PCI_EXPRESS GRAPHICS
TV
VGA
CRESTLINE-GP-U-NF
Tahoe
FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
FOR Discrete change R46, R45 ,R47 ,R43,R42 & R56 to 0 ohm
Wistron Corporation
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GMCH (2 of 6)
Tahoe
-1
Friday, April 27, 2007
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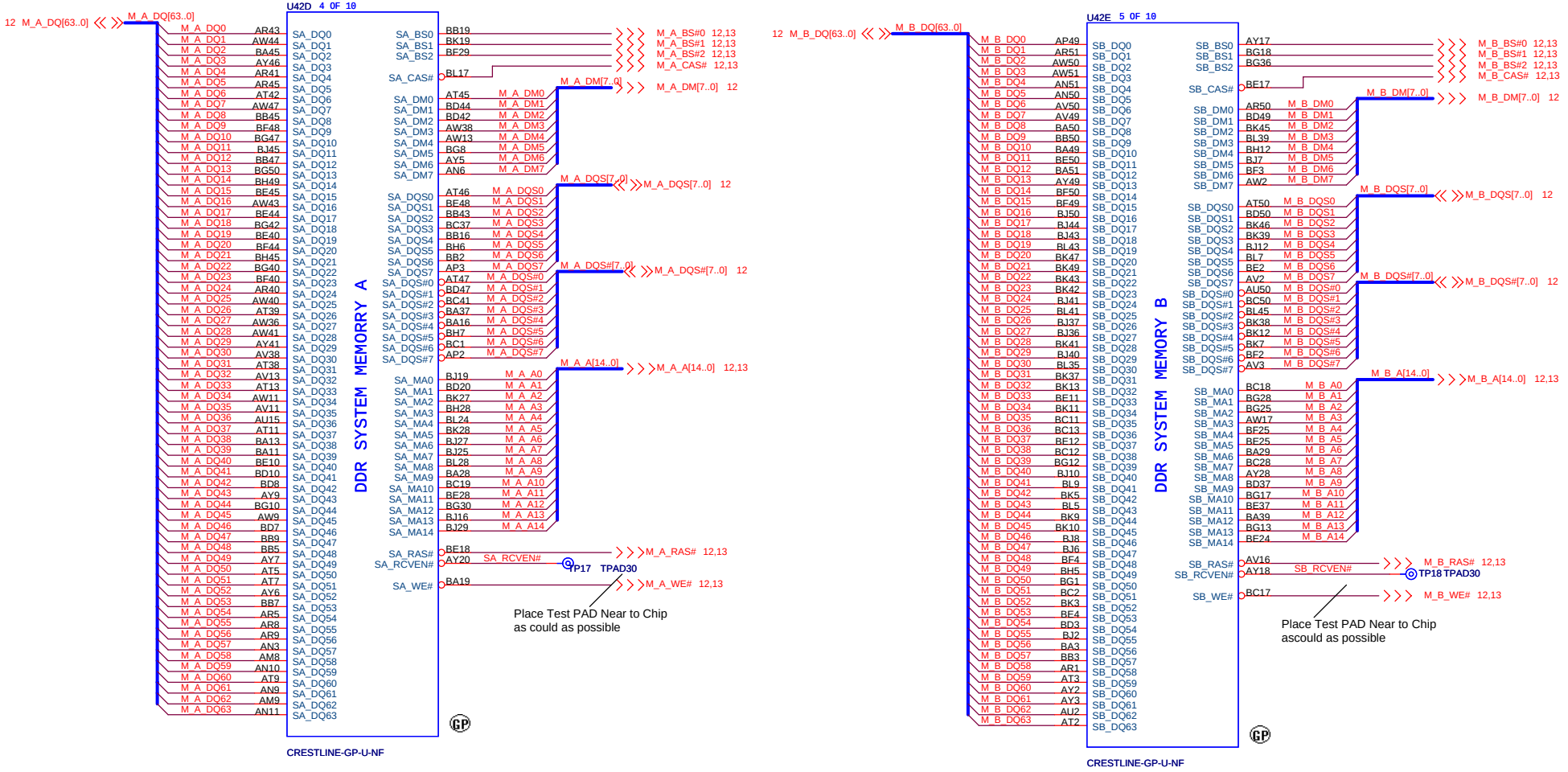

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Title: ***GMCH (3 of 6)***

Size	Document Number	Rev
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VCC_NCTF + VCC=1573mA

1573mA

U42F 6 OF 10

VCC CORE

POWER

VCC_AXG_NCTF + VCC_AXG=7700mA

3138mA

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF

CRESTLINE-GP-U-NF

FOR VCC CORE AND VCC NCTF

U42G 7 OF 10

308 mils from the Edge

Coupling CAP

FOR VCC CORE

Coupling CAP 370 mils from the Edge

VCC NCTF

VSS NCTF

VSS SCB

VSS AXM

VSS AXM NCTF

FOR VCC AXM NCTF AND VCC AXM

Place on the Edge

VCC_AXM_NCTF + VCC_AXM=540mA

CRESTLINE-GP-U-NF

Place CAP where LVDS and DDR2 taps

FOR VCC SM

Place on the Edge

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Title: GMCH (4 of 6)

Size | Document Number: Tahoe | Rev: -1

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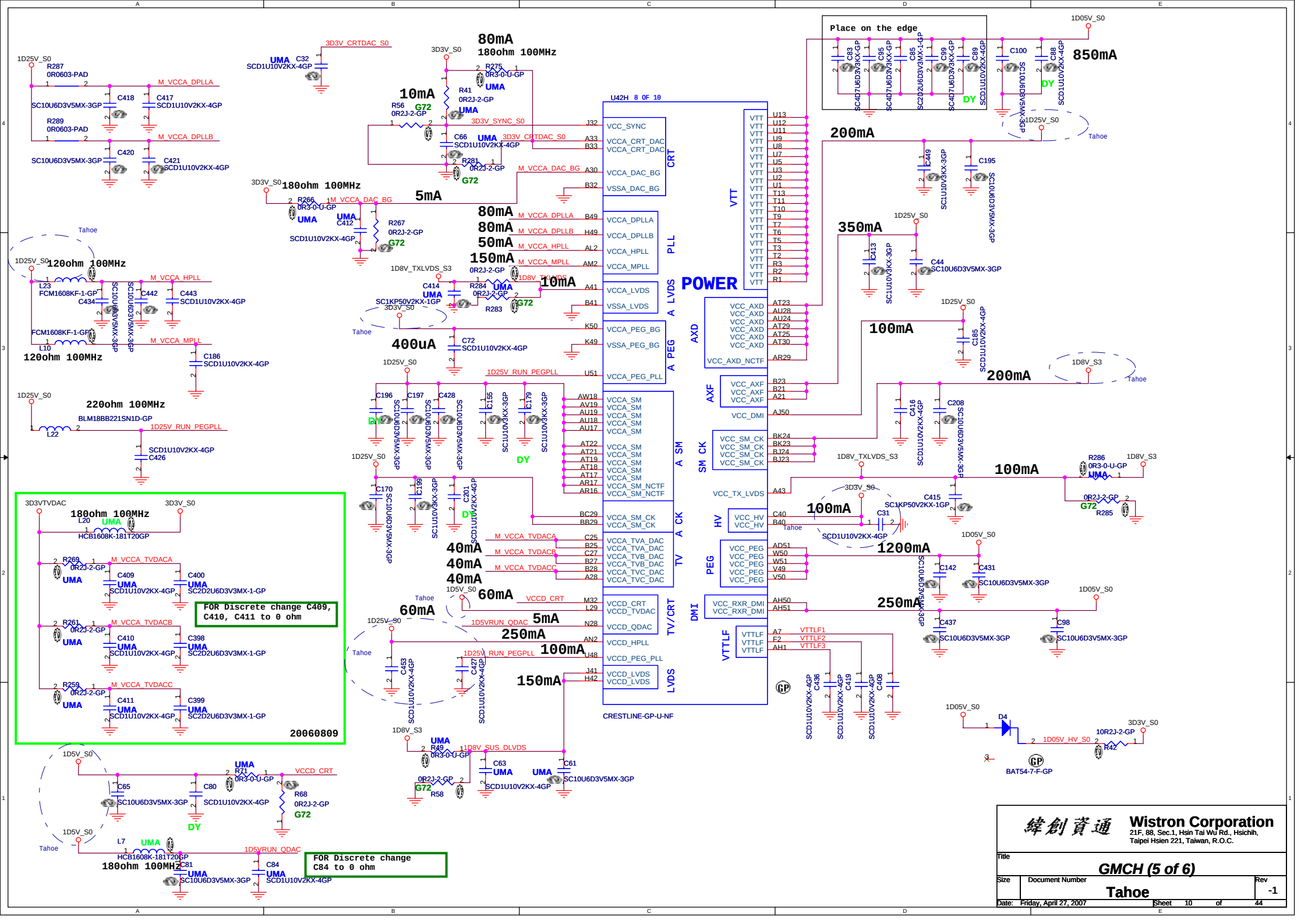
POWER
U42H 8 OF 10
CRESTLINE-GP-U-NF
Tahoe
Place on the edge
180ohm 100MHz
120ohm 100MHz
220ohm 100MHz
80mA
10mA
5mA
400uA
60mA
40mA
250mA
100mA
150mA
200mA
350mA
850mA
1200mA
FOR Discrete change C409, C410, C411 to 0 ohm
FOR Discrete change C84 to 0 ohm
20060809
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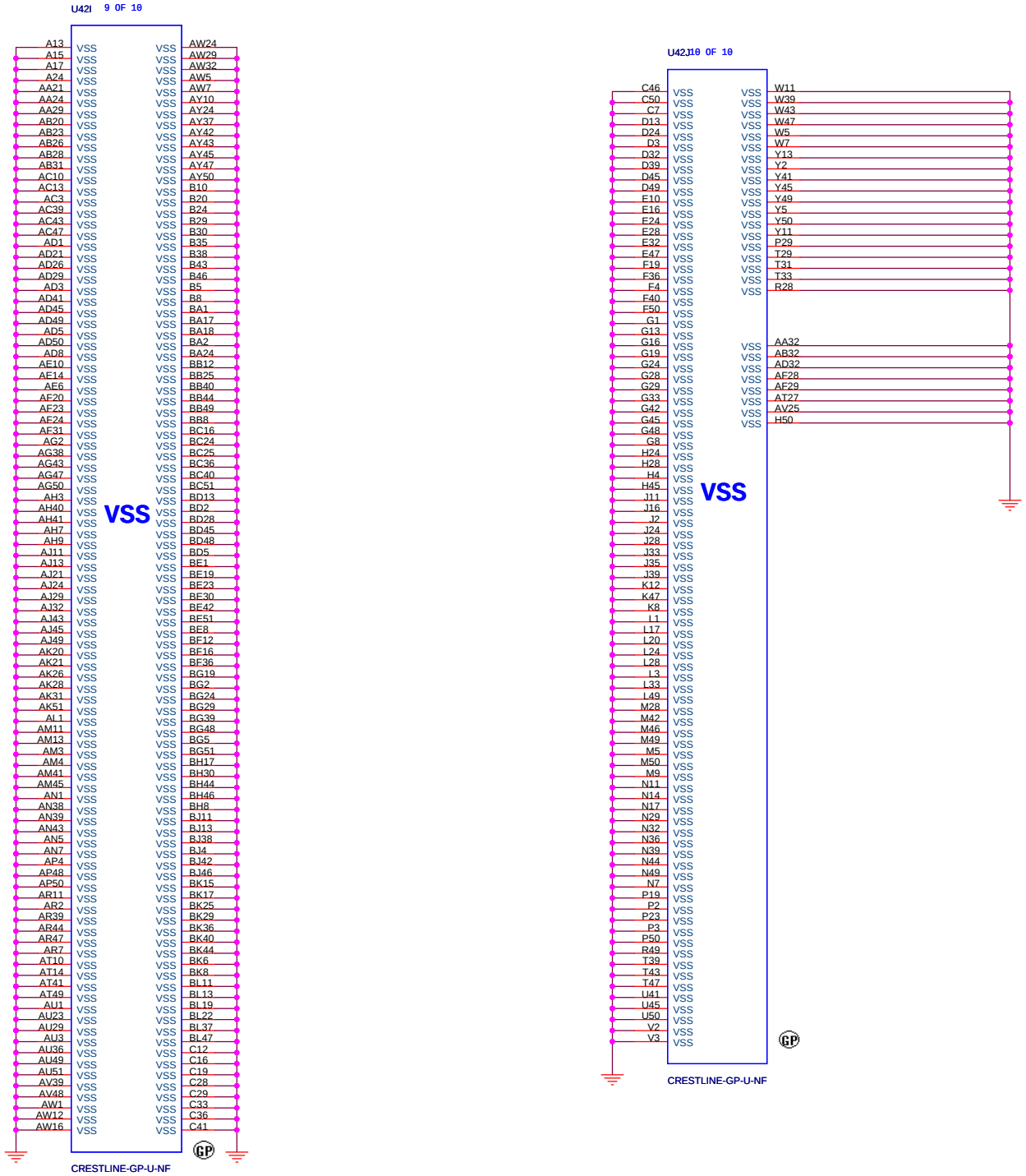
GMCH (5 of 6)
Tahoe
Date: Friday, April 27, 2007
Sheet 10 of 44



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Title	***GMCH (6 of 6)***	
Size	Document Number **Tahoe**	Rev -1
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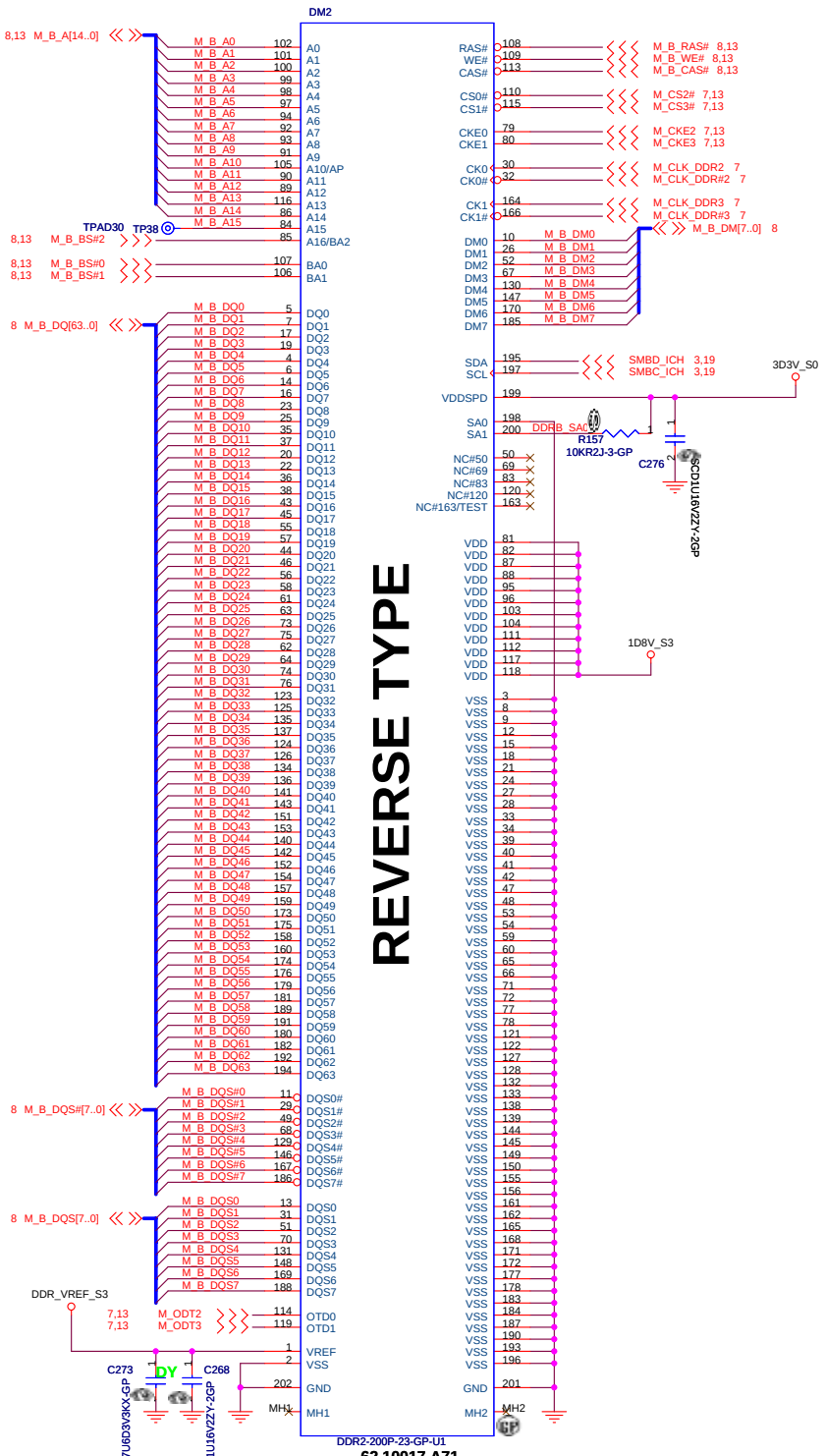

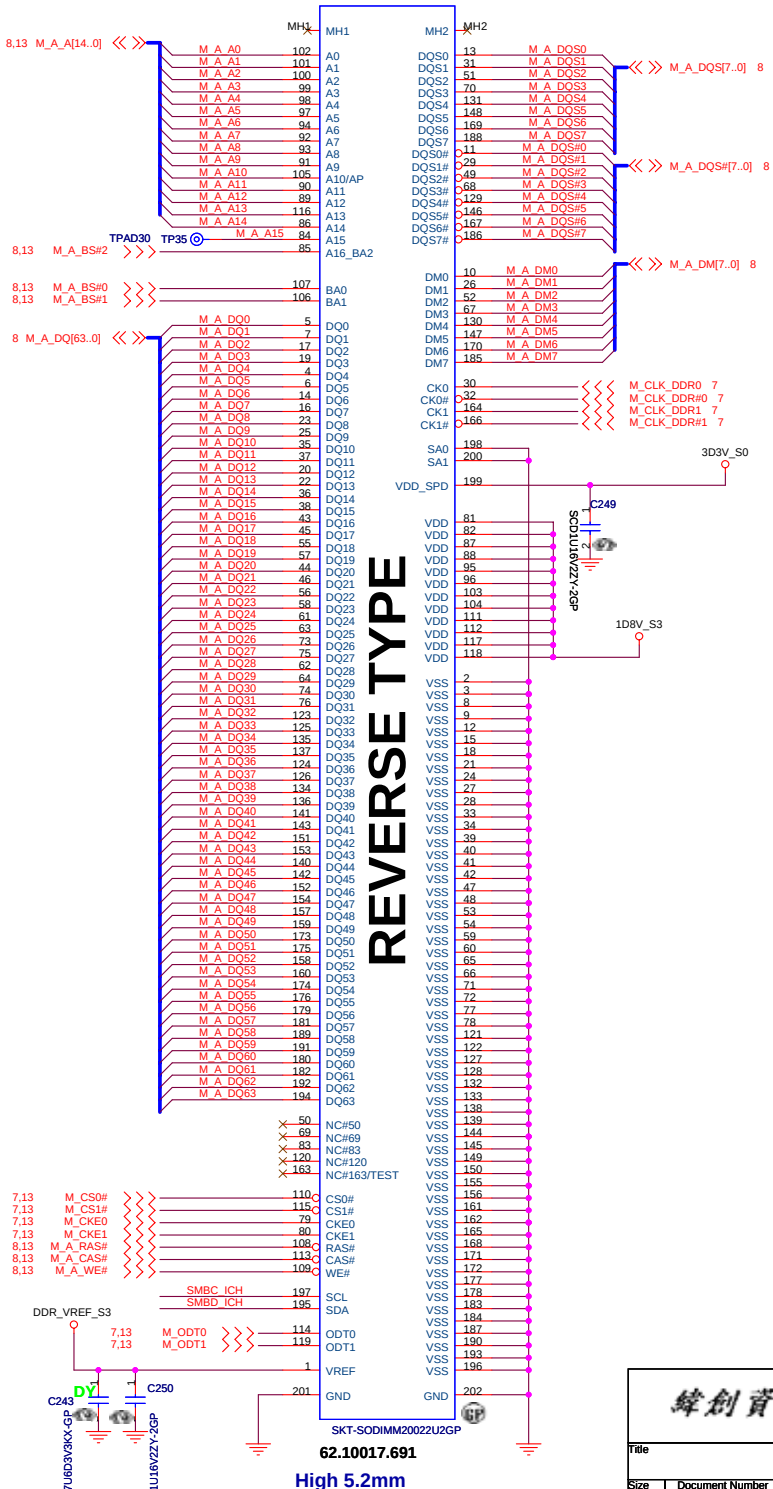

Company	Wistron Corporation
Address	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DDR2 Socket
Size	
Document Number	Tahoe
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PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

RN22: M_CKE0 7,12; M_CKE1 7,12; M_A_BS#2 8,12; M_A_A12
RN31: M_B_A8; M_B_A9; M_B_A5
RN30: M_CKE2 7,12; M_CKE3 7,12; M_B_BS#2 8,12; M_B_A12
RN32: M_B_A3; M_B_A1; M_B_A10; M_B_WE# 8,12
RN36: M_B_A13; M_ODT2 7,12; M_ODT3 7,12; M_B_RAS# 8,12
RN35: M_B_BS#1 8,12; M_B_A2; M_B_A0; M_B_A4
RN34: M_B_A14; M_B_A6; M_B_A7; M_B_A11
RN33: M_B_BS#0 8,12; M_B_CAS# 8,12; M_CS3# 7,12; M_CS2# 7,12
RN29: M_A_A13; M_ODT0 7,12; M_CS0# 7,12; M_A_RAS# 8,12
RN28: M_A_BS#1 8,12; M_A_A0; M_A_A2; M_A_A4
RN25: M_A_CAS# 8,12; M_CS1# 7,12; M_ODT1 7,12
RN23: M_A_A9; M_A_A8; M_A_A5; M_A_A3
RN27: M_A_A6; M_A_A7; M_A_A11; M_A_A14
RN24: M_A_A1; M_A_A10; M_A_BS#0 8,12; M_A_WE# 8,12

All: SRN56J-5-GP

M_A_A[14..0] <<>> M_A_A[14..0] 8,12
M_B_A[14..0] <<>> M_B_A[14..0] 8,12

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S0

C235 C286 C274 C247 C261 C266 C264 C248 C281 C263 C275 — SCD1U16V2ZY-2GP — DY DY DY DY DY DY DY DY DY DY

C238 C262 C288 C252 C280 C253 C265 C236 C289 C287 C237 — SCD1U16V2ZY-2GP — DY DY DY DY DY DY DY DY DY DY

Place these Caps near DM1

1D8V_S3

C514 C255 C515 C256 C513 — SC2D2U6D3V3MX-1-GP

C234 C246 C251 C254 — SCD1U16V2ZY-2GP — DY DY DY DY

Place these Caps near DM2

1D8V_S3

C270 C290 C271 C282 C291 — SC2D2U6D3V3MX-1-GP

C284 C269 C285 C267 — SCD1U16V2ZY-2GP — DY DY DY DY

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Title: ***DDR2 Termination Resistor***

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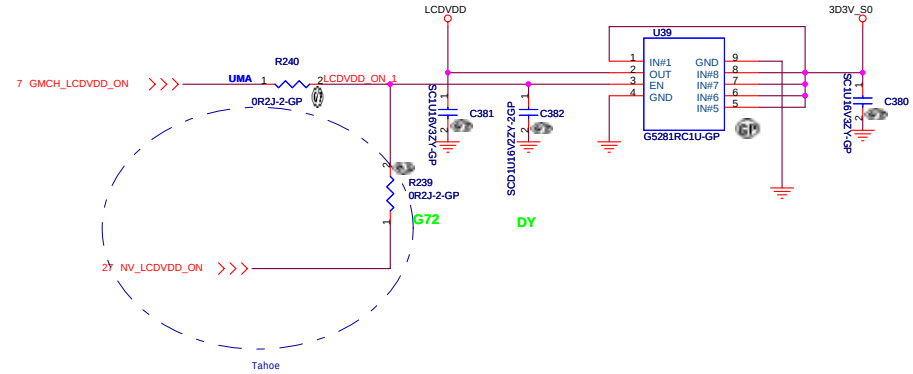
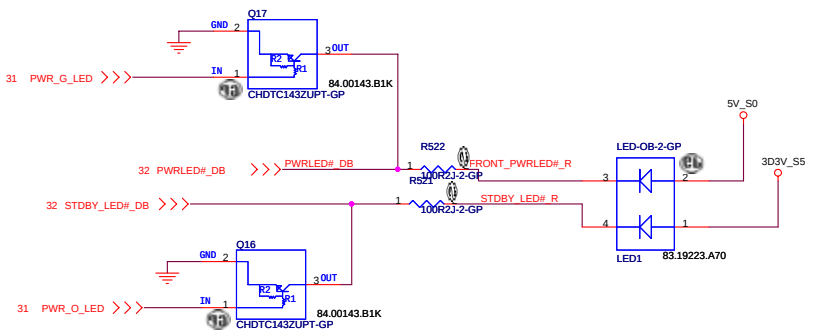
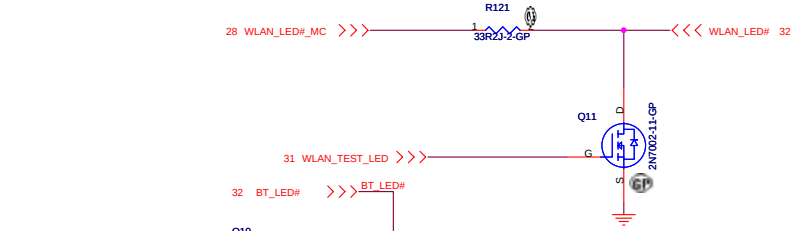
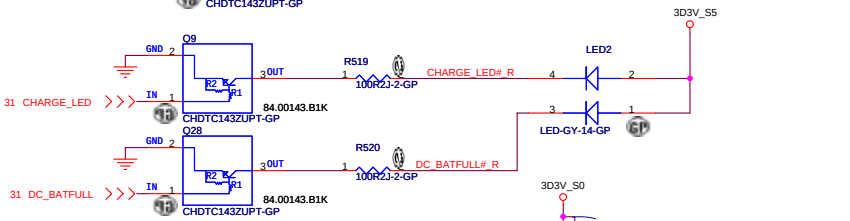
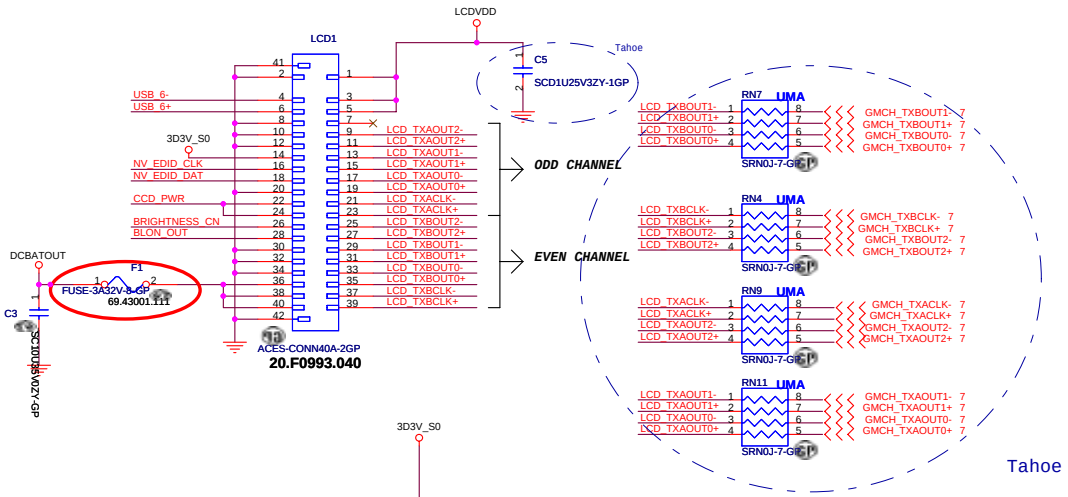
LCD/INVERTER CONN

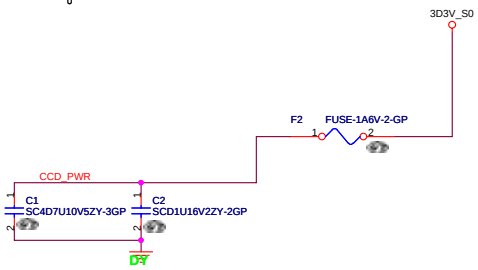


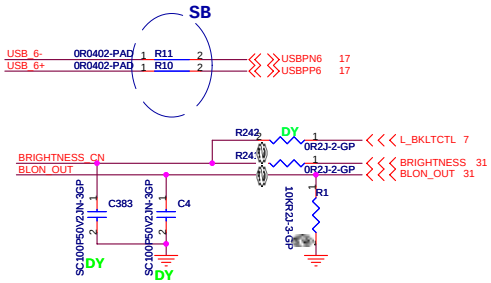


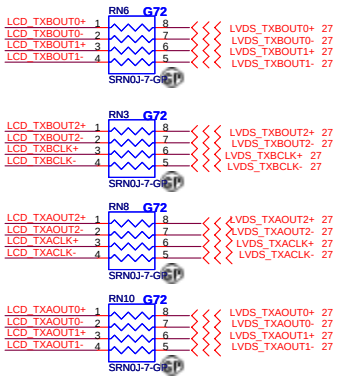




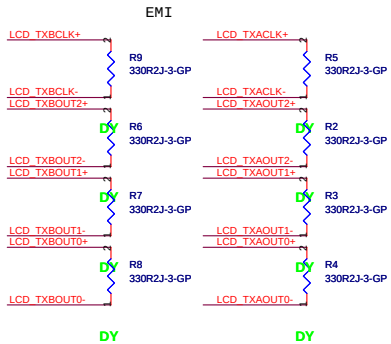


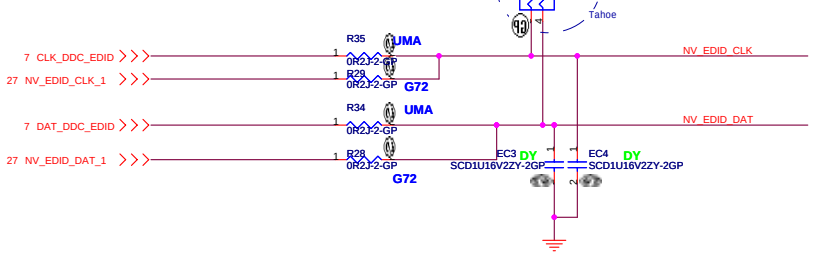






Tahoe





<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & LED

Size | Document Number: Tahoe | Rev: -1

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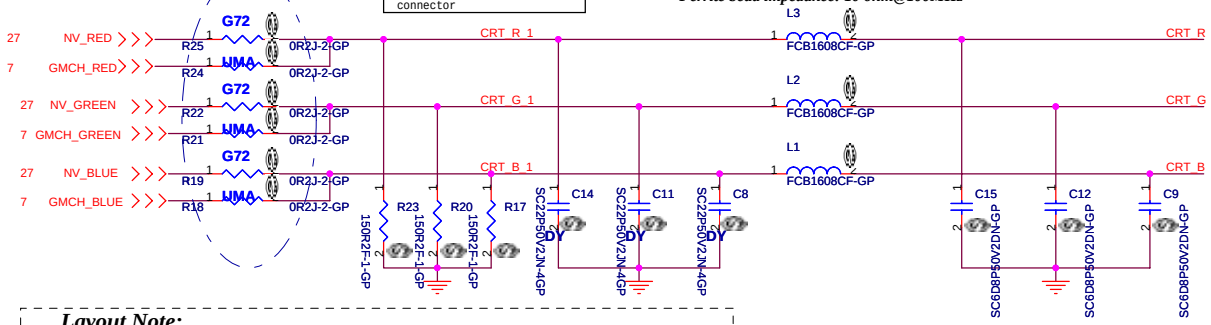
CRT I/F & CONNECTOR

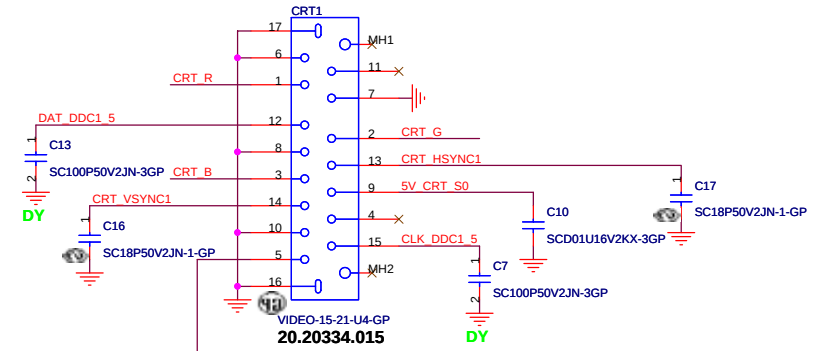
Layout Note:
Place these resistors close to the CRT-out connector

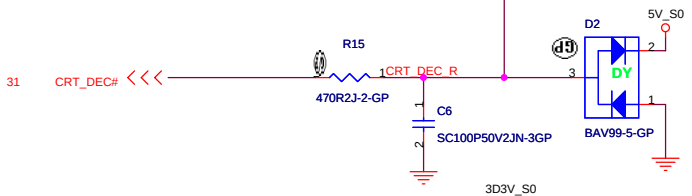
Ferrite bead impedance: 10 ohm@100MHz



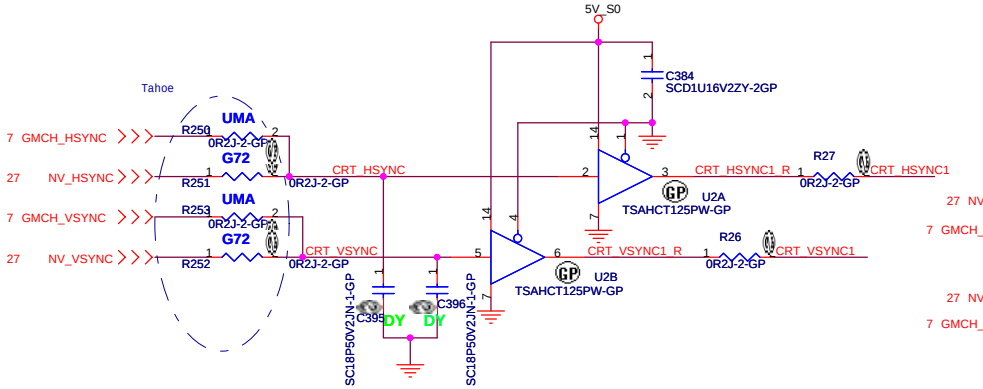
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

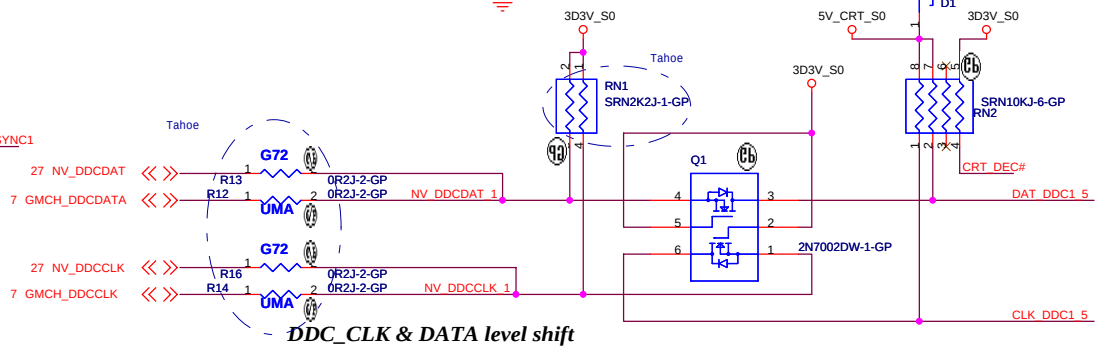
For DIS
C15--->78.15034.1FL
C12,C9--->78.18034.1FL





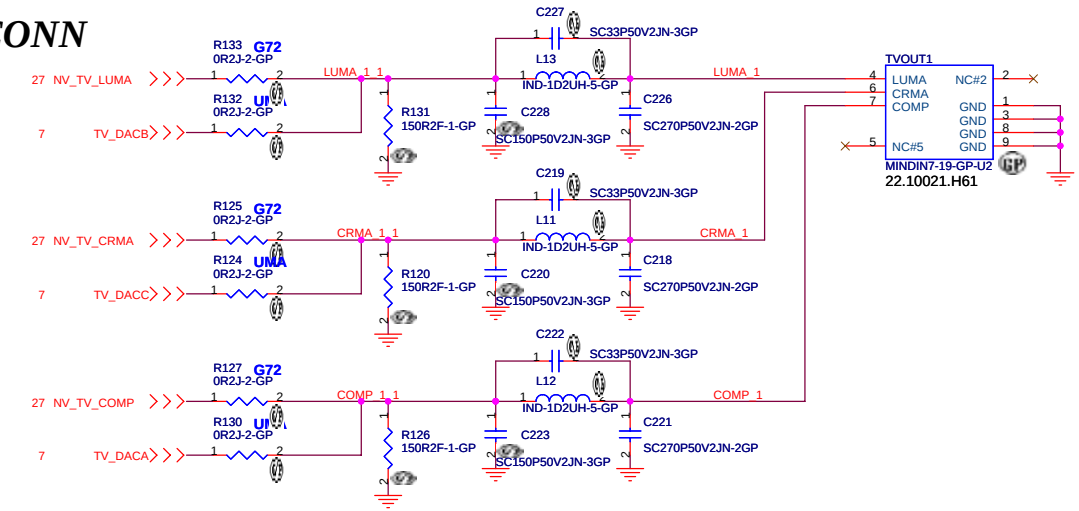
Hsync & Vsync level shift

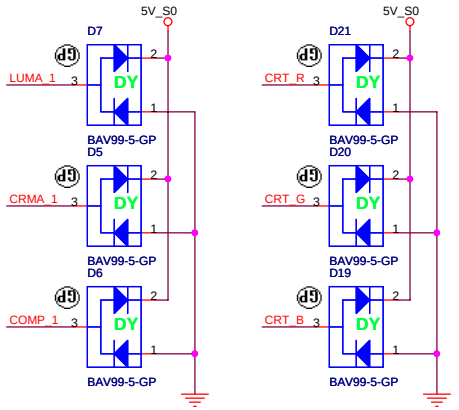




DDC_CLK & DATA level shift

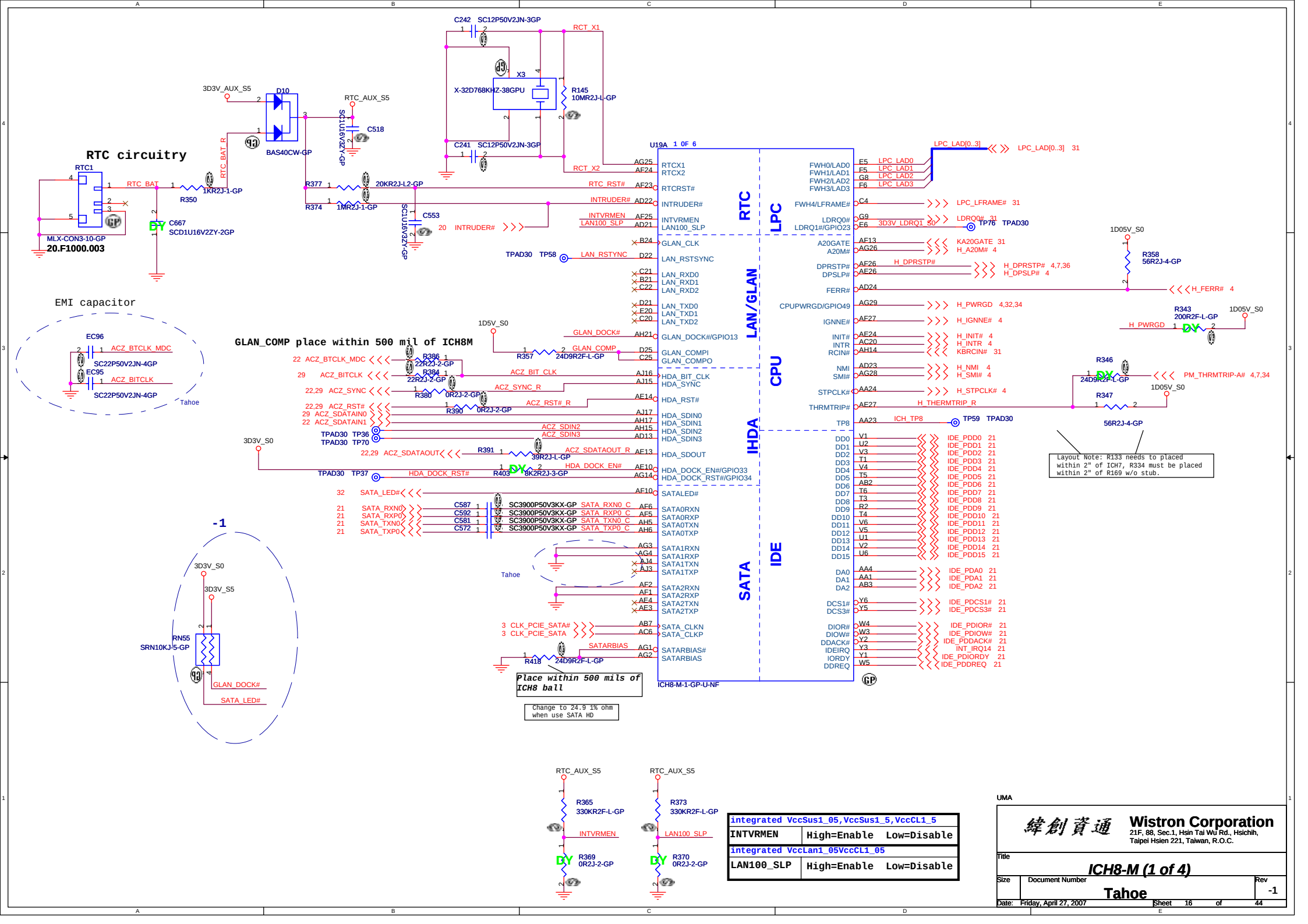
TV CONN

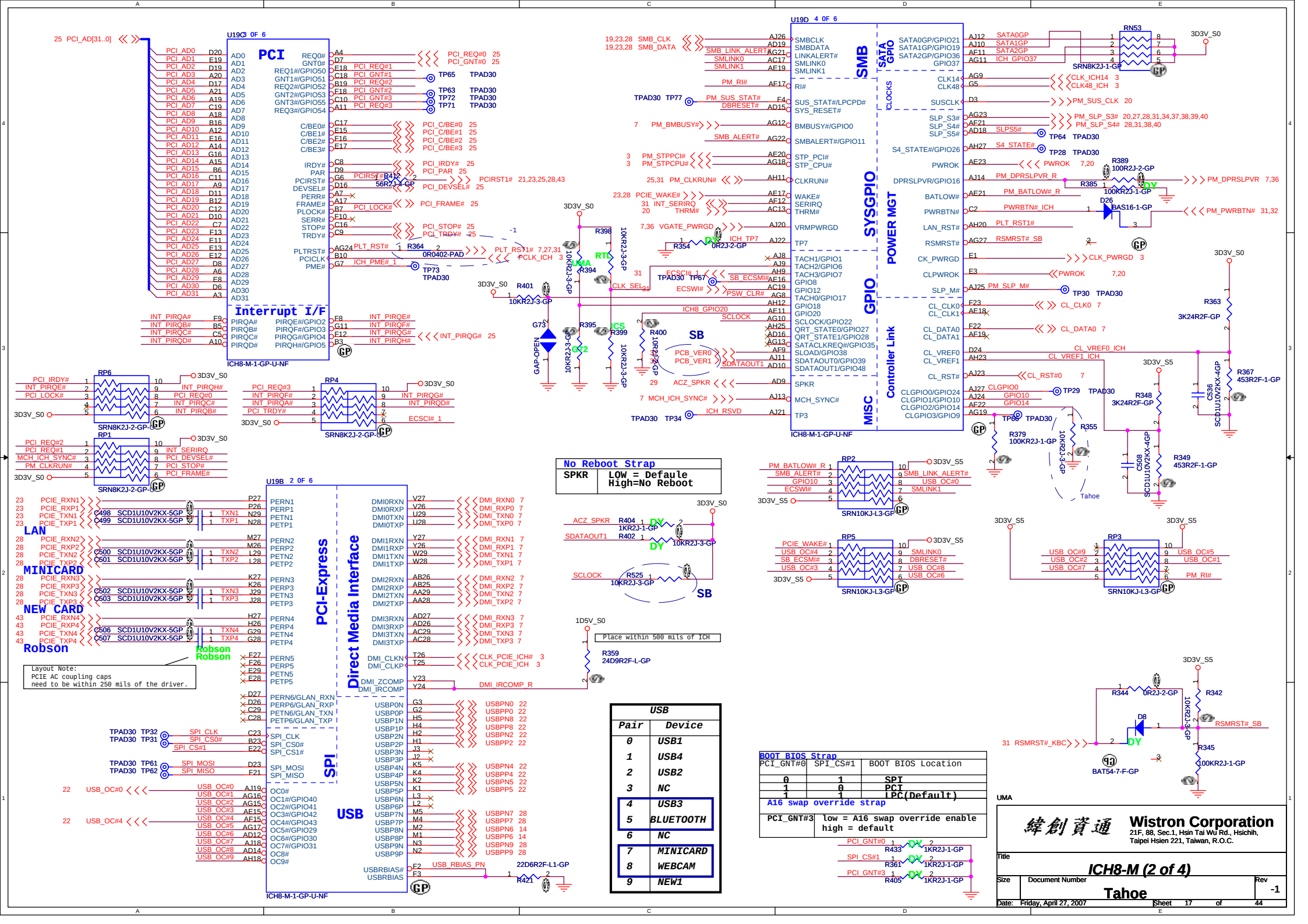




緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT/TV Connector	
Size	Document Number: Tahoe	Rev: -1
Date: Friday, April 27, 2007	Sheet 15 of 44	


RTC circuitry
EMI capacitor
GLAN_COMP place within 500 mil of ICH8M
-1
U19A 1 OF 6
ICH8-M-1-GP-U-NF
RTC
LPC
LAN/GLAN
CPU
IHDA
IDE
SATA
Tahoe
Place within 500 mils of ICH8 ball
Change to 24.9 1% ohm when use SATA HD
Layout Note: R133 needs to placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (1 of 4)
Size
Document Number
Tahoe
Rev
-1
Date: Friday, April 27, 2007
Sheet 16 of 44


U19C 3 OF 6
PCI
Interrupt I/F
ICH8-M-1-GP-U-NF
U19D 4 OF 6
SMB
SYSGPIO
GPIO
Controller Link
MISC
ICH8-M-1-GP-U-NF
U19B 2 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH8-M-1-GP-U-NF
No Reboot Strap
SPKR LOW = Defaule High=No Reboot
USB
Pair Device
0 USB1
1 USB4
2 USB2
3 NC
4 USB3
5 BLUETOOTH
6 NC
7 MINICARD
8 WEBCAM
9 NEW1
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable high = default
Layout Note:
PCIE AC coupling caps need to be within 250 mils of the driver.
Place within 500 mils of ICH
LAN
MINICARD
NEW CARD
Robson
Tahoe
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (2 of 4)
Size
Document Number
Tahoe
Rev
-1
Date: Friday, April 27, 2007
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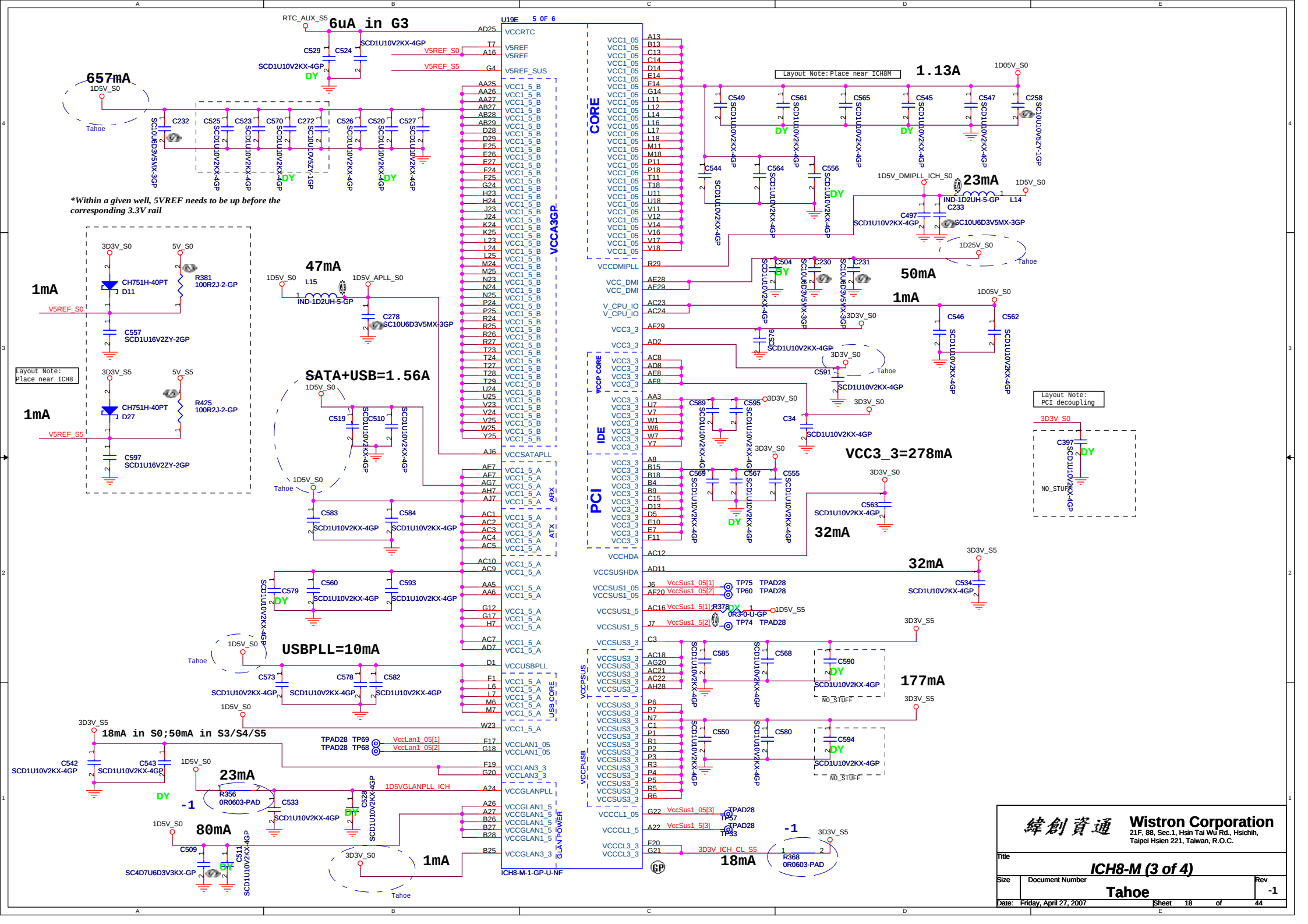
6uA in G3
657mA
1D5V_S0
Tahoe
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
1mA
CH751H-40PT
D11
R381
100R2J-2-GP
V5REF_S0
C557
SCD1U16V2ZY-2GP
Layout Note: Place near ICH8
3D3V_S5
5V_S5
CH751H-40PT
D27
R425
100R2J-2-GP
V5REF_S5
C597
SCD1U16V2ZY-2GP
47mA
1D5V_APLL_S0
L15
IND-1D2UH-5-GP
C278
SC10U6D3V5MX-3GP
SATA+USB=1.56A
C519
C510
C583
C584
USBPLL=10mA
C573
C578
C582
18mA in S0;50mA in S3/S4/S5
C542
C543
23mA
R356
0R0603-PAD
C533
80mA
C509
C511
SC4D7U6D3V3KX-GP
1mA
U19E
5 OF 6
CORE
VCCA3GP
IDE
PCI
USB CORE
GLAN POWER
VCCP CORE
VCCPSUS
VCCPUSB
ICH8-M-1-GP-U-NF
Layout Note:Place near ICH8M
1.13A
C549
C561
C565
C545
C547
C258
C544
C564
C556
1D5V_DMIPLL_ICH_S0
23mA
IND-1D2UH-5-GP
L14
C233
C497
SC10U6D3V5MX-3GP
1D25V_S0
50mA
C504
C230
C231
1mA
C546
C562
C591
C34
VCC3_3=278mA
C589
C595
C569
C567
C555
C563
32mA
C534
C590
C585
C568
177mA
C550
C580
C594
NO_STUFF
-1
R368
0R0603-PAD
18mA
Layout Note: PCI decoupling
C397
NO_STUFF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8-M (3 of 4)
Size
Document Number
Tahoe
Rev
-1
Date: Friday, April 27, 2007
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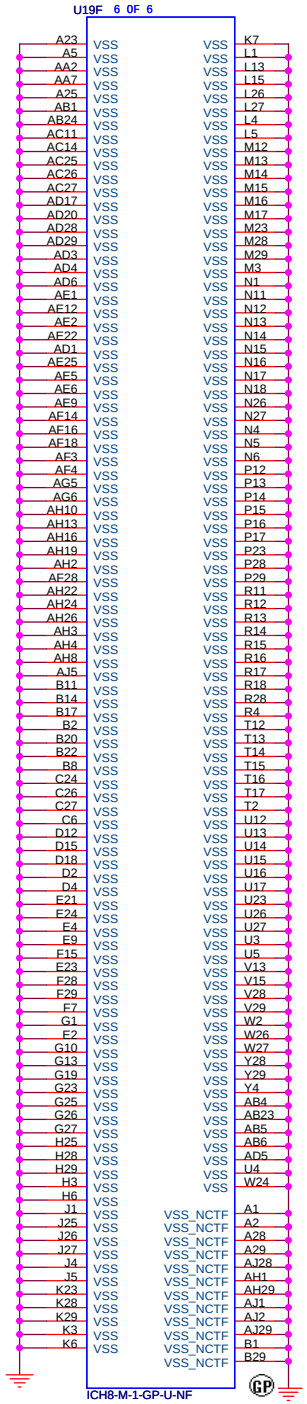

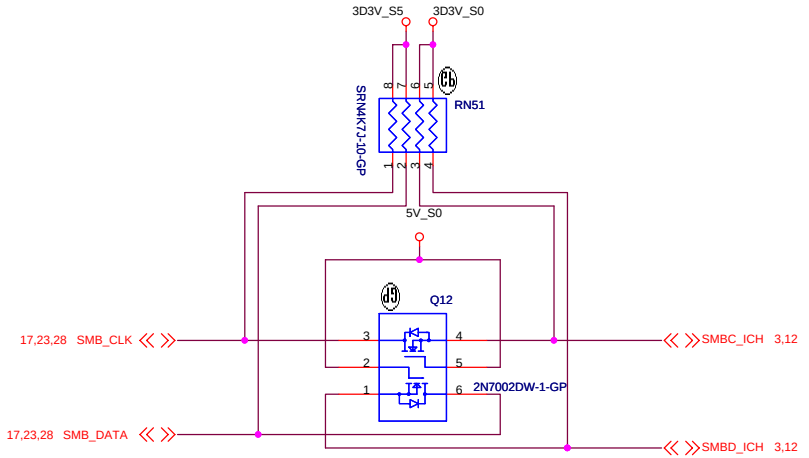

Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

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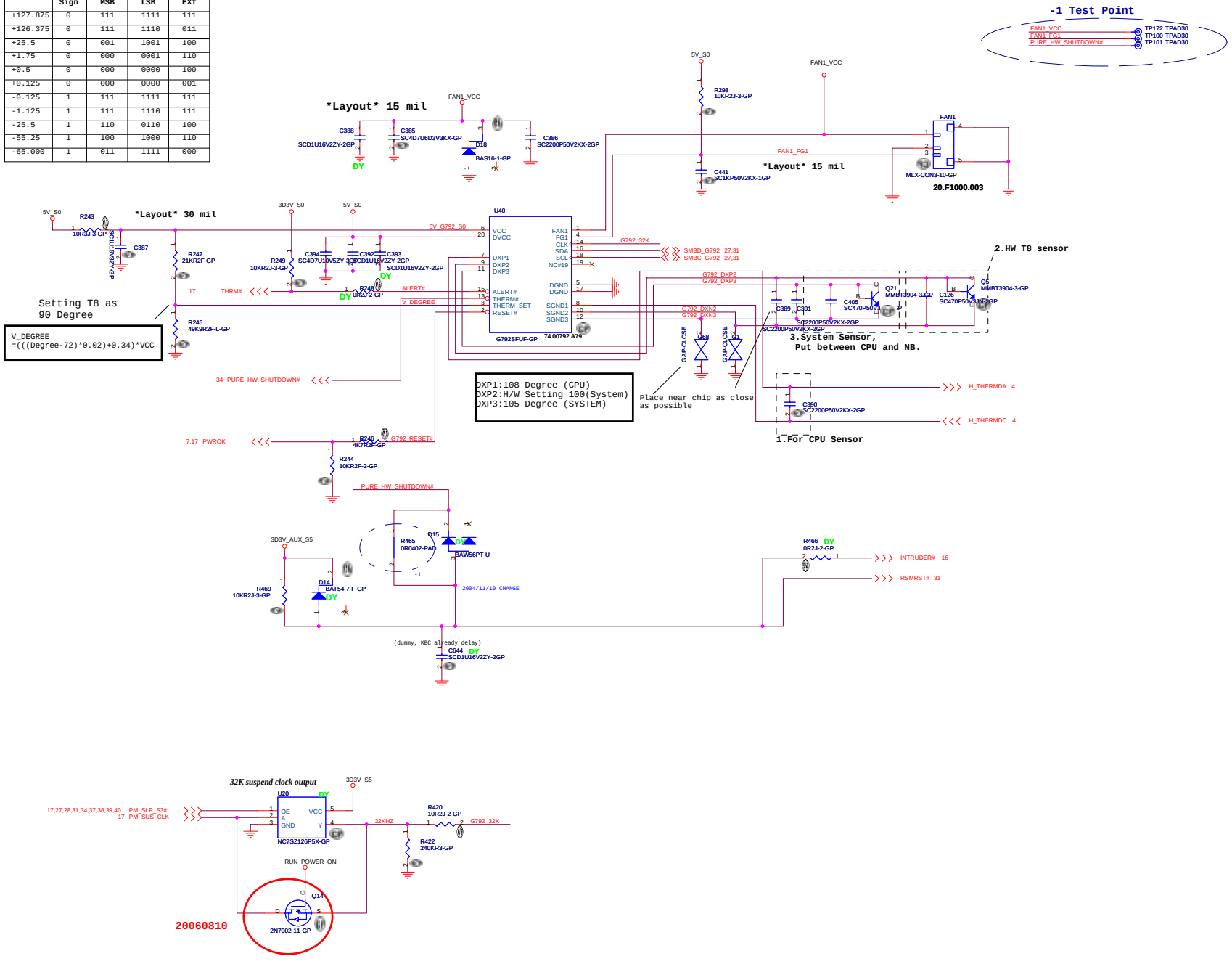
Title	*ICH8-M (4 of 4)*	
Size	Document Number: **Tahoe**	Rev: -1
Date: Friday, April 27, 2007	Sheet 19 of 44	

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



鋒創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Thermal/Fan Controllor		
Size	Document Number: Tahoe	Rev: -1
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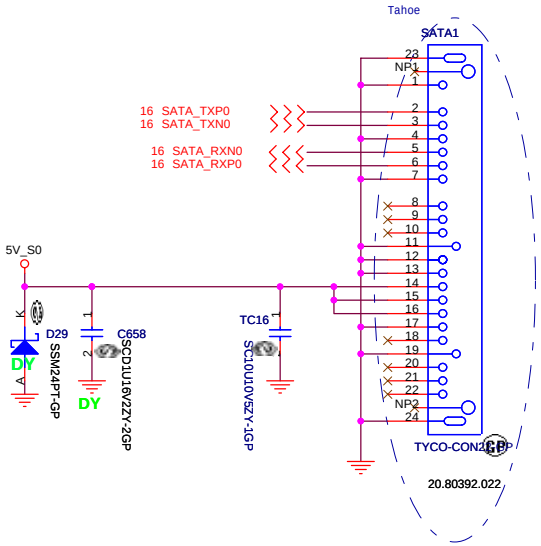
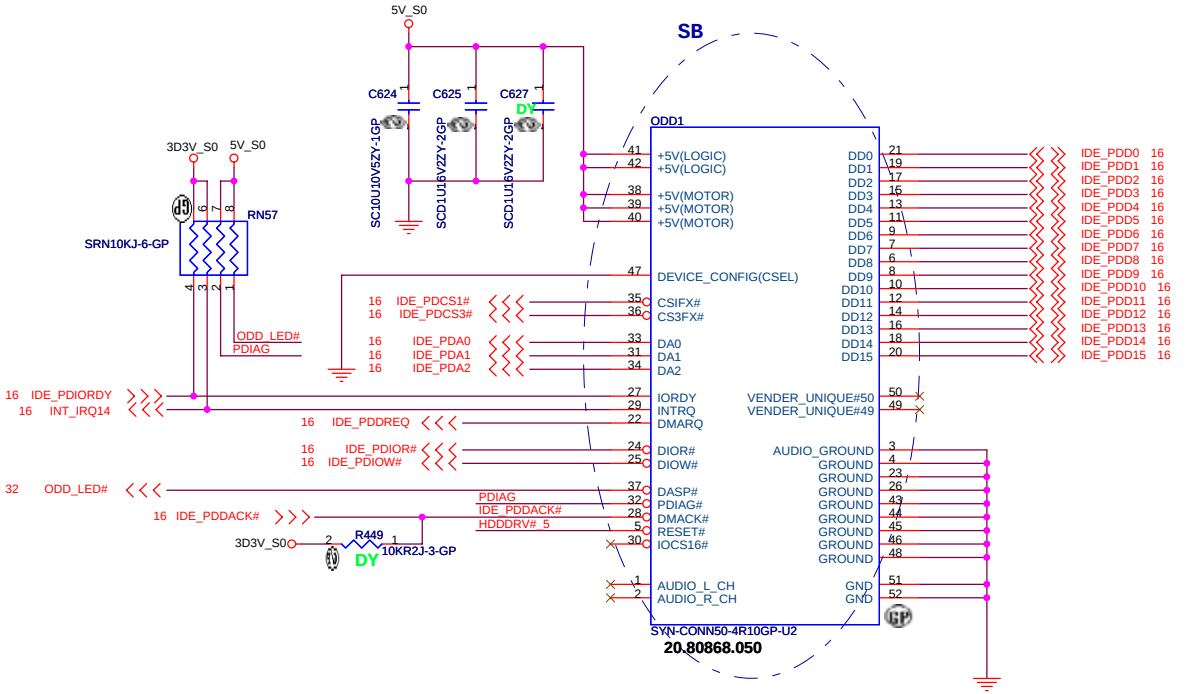
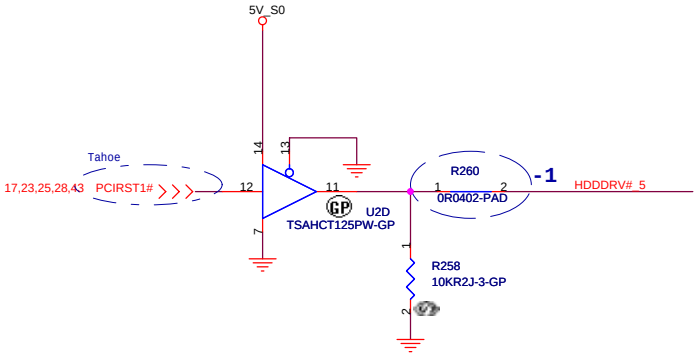
SATA HD Connector



ODD Connector





bom1

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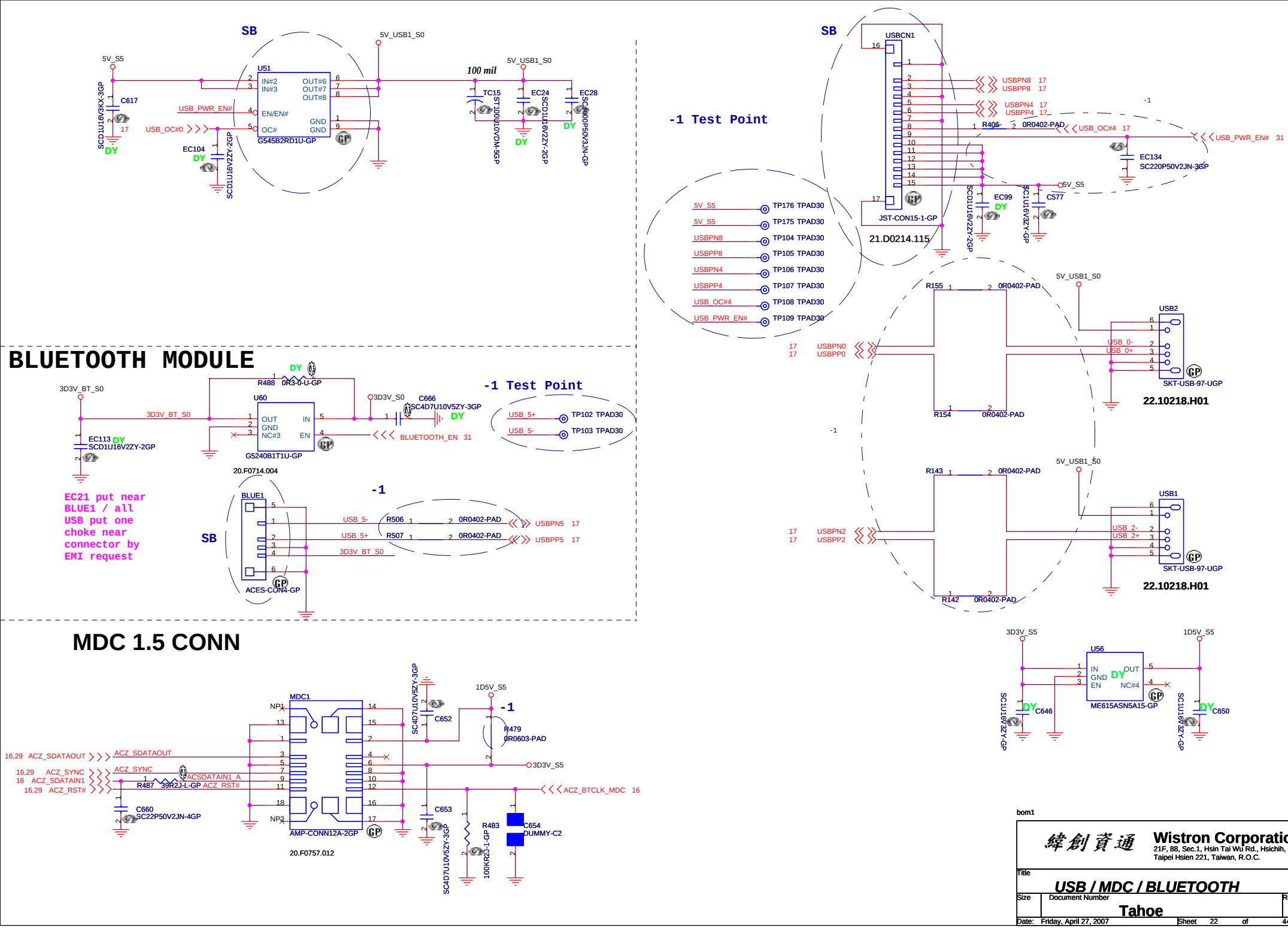
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD and CDROM***

Size	Document Number	Rev
	Tahoe	-1

Date: Friday, April 27, 2007 Sheet 21 of 44



bom1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB / MDC / BLUETOOTH***	
Size	Document Number: **Tahoe**	Rev: -1
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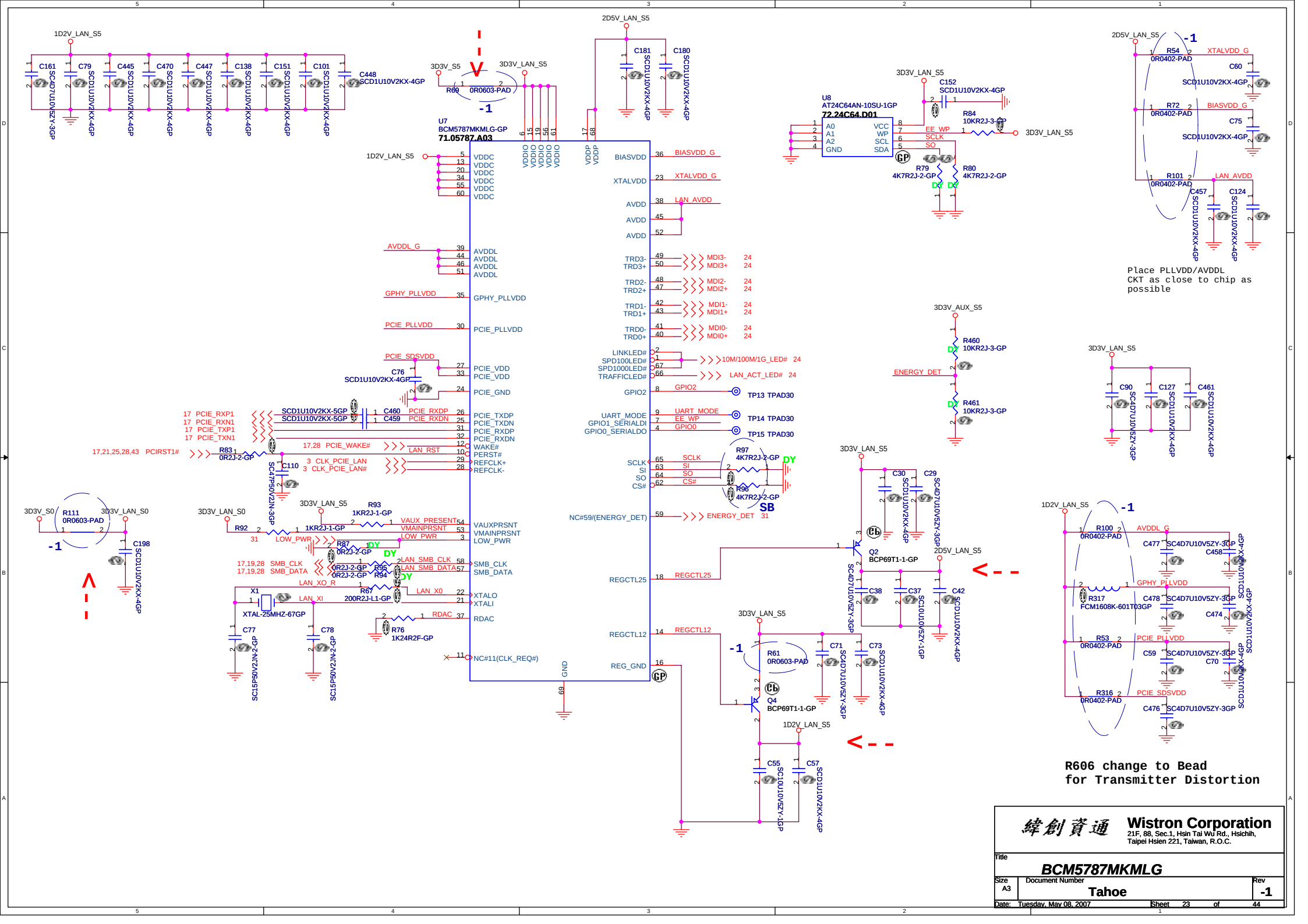
1D2V_LAN_S5
2D5V_LAN_S5
3D3V_LAN_S5
3D3V_S5
3D3V_AUX_S5
3D3V_LAN_S0
U7
BCM5787MKMLG-GP
71.05787.A03
U8
AT24C64AN-10SU-1GP
72.24C64.D01
XTAL-25MHZ-67GP
Q2
BCP69T1-1-GP
Q4
BCP69T1-1-GP
R606 change to Bead
for Transmitter Distortion
Place PLLVDD/AVDDL
CKT as close to chip as
possible
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BCM5787MKMLG
Tahoe
Size A3
Rev -1
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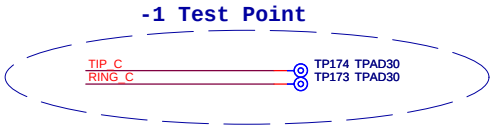
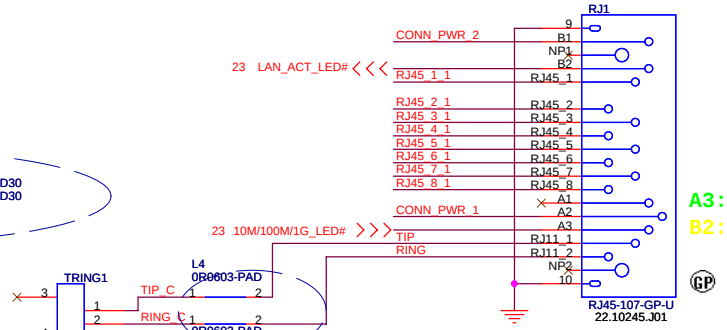
LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

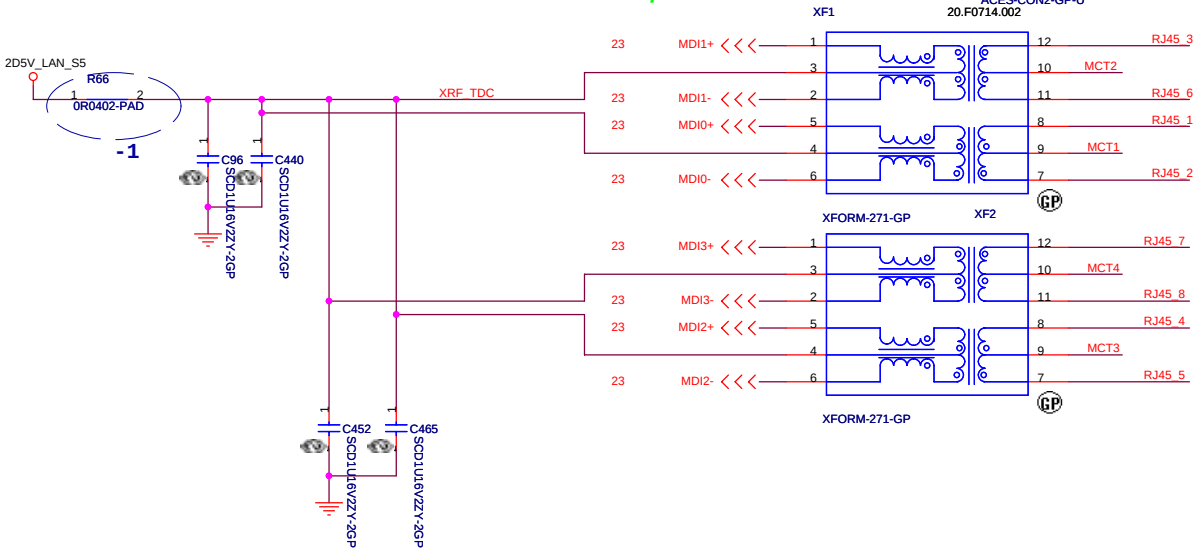




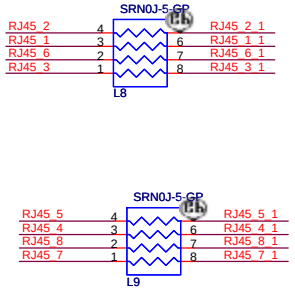
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

GIGA Lan Transformer



For EMI



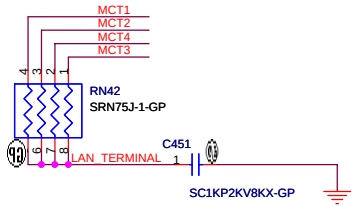
Tahoe

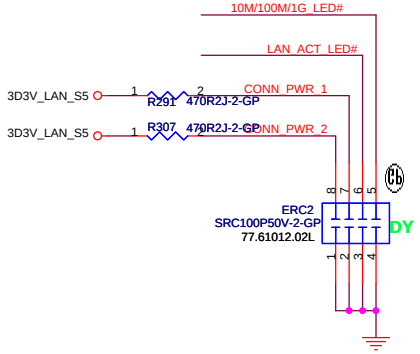
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size: A3 | Document Number: Tahoe | Rev: -1

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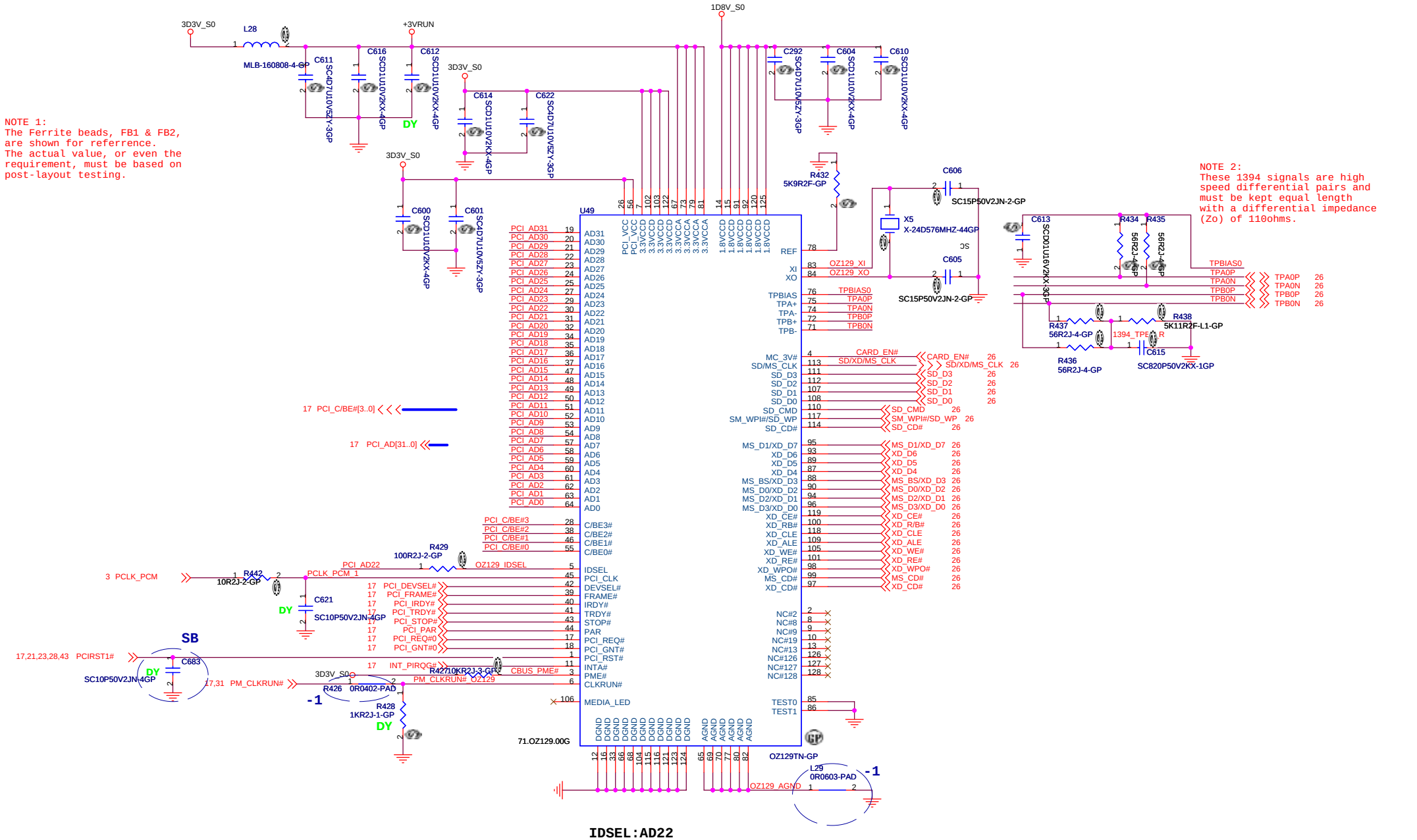
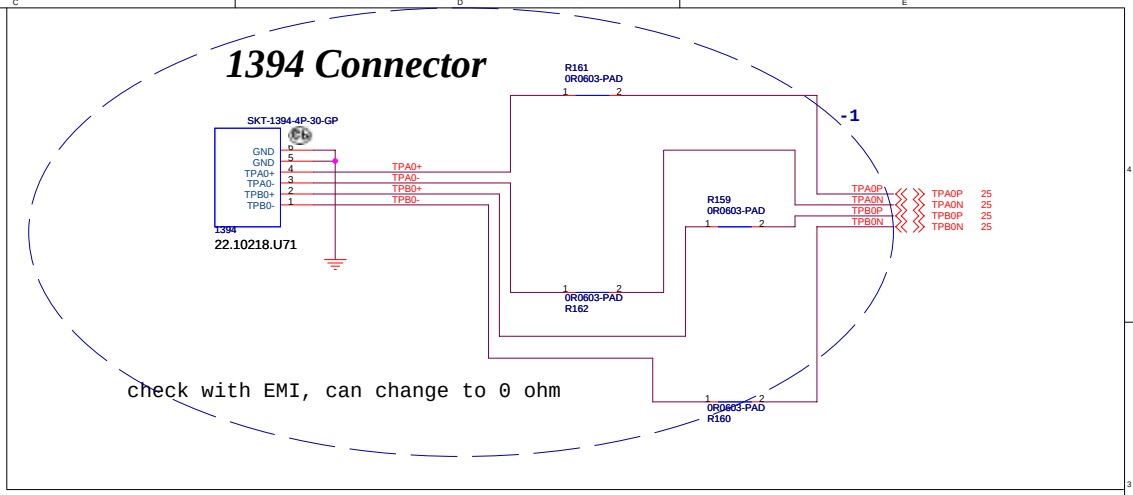


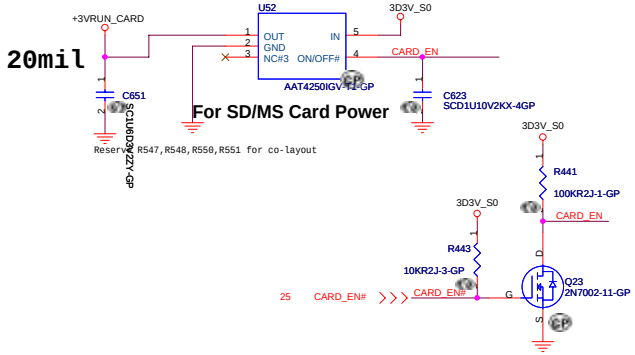
<variant_name="<Variant Name>">
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

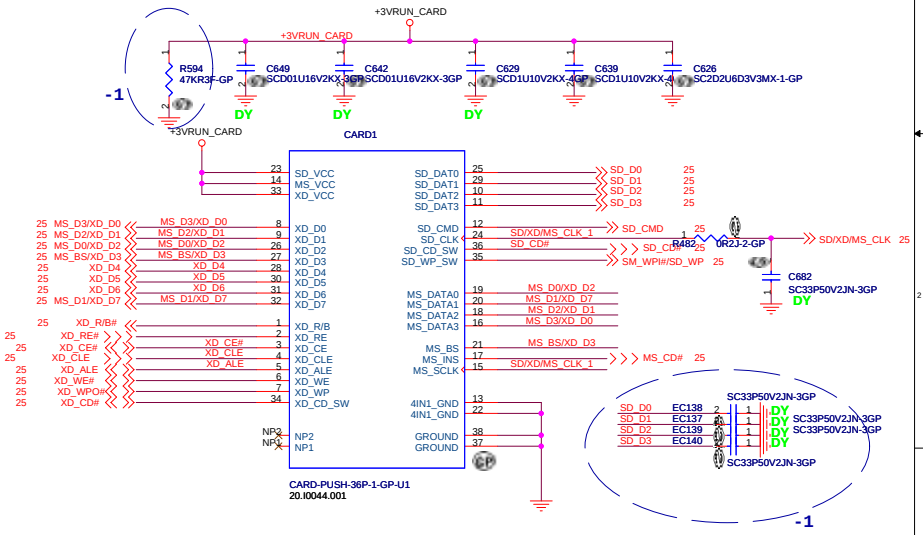
Title: OZ129T

Size | Document Number: Tahoe | Rev: -1

Date: Friday, April 27, 2007 | Sheet 25 of 44







<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*1394 / CARD READER*	
Size	Document Number: Tahoe	Rev: -1
Date: Friday, April 27, 2007	Sheet 26 of 44	

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

7 PEG_TXP[15..0]
7 PEG_TXN[15..0]
7 PEG_RXP[15..0]
7 PEG_RXN[15..0]

14 LVDS_TXBOUT0+
14 LVDS_TXBOUT0-
14 LVDS_TXBOUT1+
14 LVDS_TXBOUT1-
14 LVDS_TXBOUT2+
14 LVDS_TXBOUT2-
14 LVDS_TXBCLK+
14 LVDS_TXBCLK-
15 NV_BLUE
15 NV_GREEN
15 NV_RED

LVDS_TXACLK- 14
LVDS_TXACLK+ 14
LVDS_TXAOUT2- 14
LVDS_TXAOUT2+ 14
LVDS_TXAOUT1- 14
LVDS_TXAOUT1+ 14
LVDS_TXAOUT0- 14
LVDS_TXAOUT0+ 14
NV_EDID_DAT_1 14
NV_EDID_CLK_1 14
NV_LCDVDD_ON 14
NV_BLON 31

-2
36,37,38,39,40 CPUCORE_ON
17,20,28,31,34,37,38,39,40 PM_SLP_S3#
DY
R314 0R2J-2-GP
R312 0R2J-2-GP
G72
5V_S0
15 NV_TV_COMP
15 NV_TV_LUMA
15 NV_TV_CRMA
C482 SCD1U25V3KX-GP
TPAD30TP55
1D8V_S0
C475 SCD1U25V3KX-GP
C481 SCD1U25V3KX-GP
G72
20.F0623.230
DCBATOUT
C485 SCD1U25V3KX-GP
C486 SCD1U25V3KX-GP
C209 SC4D7U25V6KX-1GP
C210 SC4D7U25V6KX-1GP
C211 SC4D7U25V6KX-1GP
3 CLK_PCIE_PEG#
3 CLK_PCIE_PEG
7,17,31 PLT_RST1#
R360 0R2J-2-GP
G72
C530 SC100P50V2JN-3GP
20,31 SMBD_G792
20,31 SMBC_G792
PLT_RST1# MXM
R362 0R0402-PAD
R366 0R0402-PAD
-1
34 MXM_THER
15 NV_HSYNC
15 NV_VSYNC
15 NV_DDCCLK
15 NV_DDCDAT

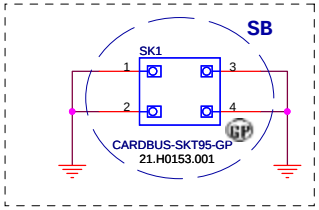
2D5V_S0
C283 SCD1U25V3KX-GP
NV
R158 0R3-0-U-GP
3D3V_S0
C607 SC10U10V5ZY-1GP
MXM1
AMP-CONN230A-GP-U2
Tahoe

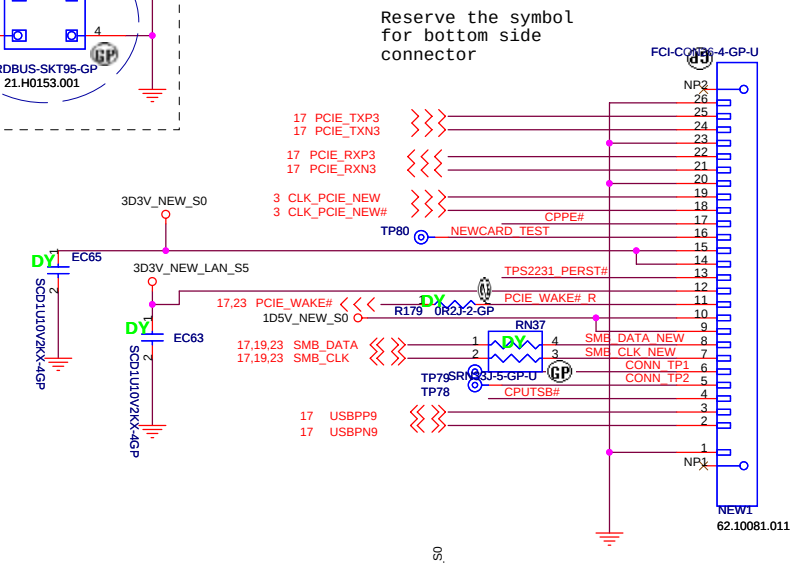
<Core Design>

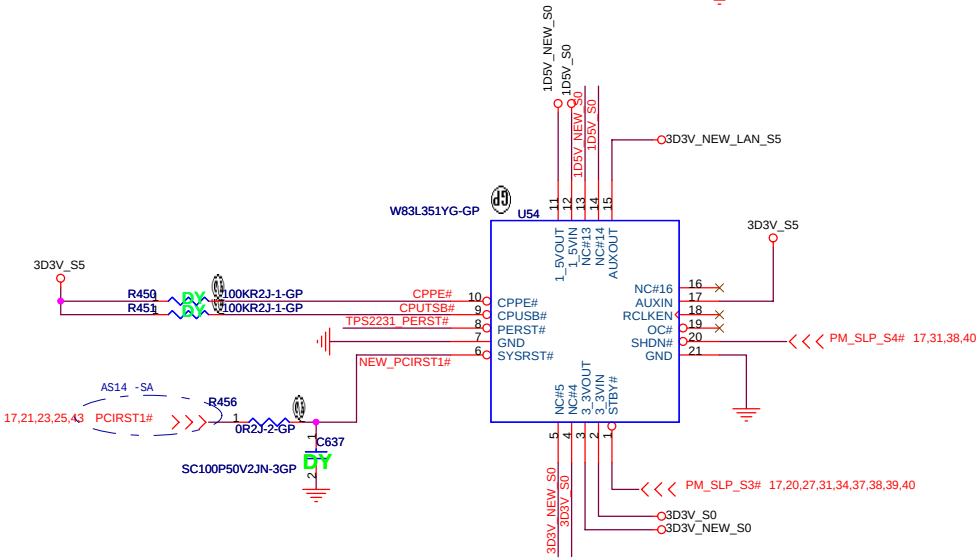
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Graphic MXM CONN	
Size A3	Document Number Tahoe	Rev -1
Date: Friday, April 27, 2007	Sheet 27 of 44	

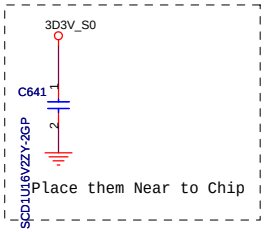
Mini Card Connector

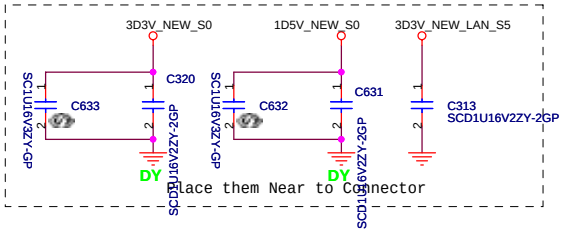
NEWCARD Connector

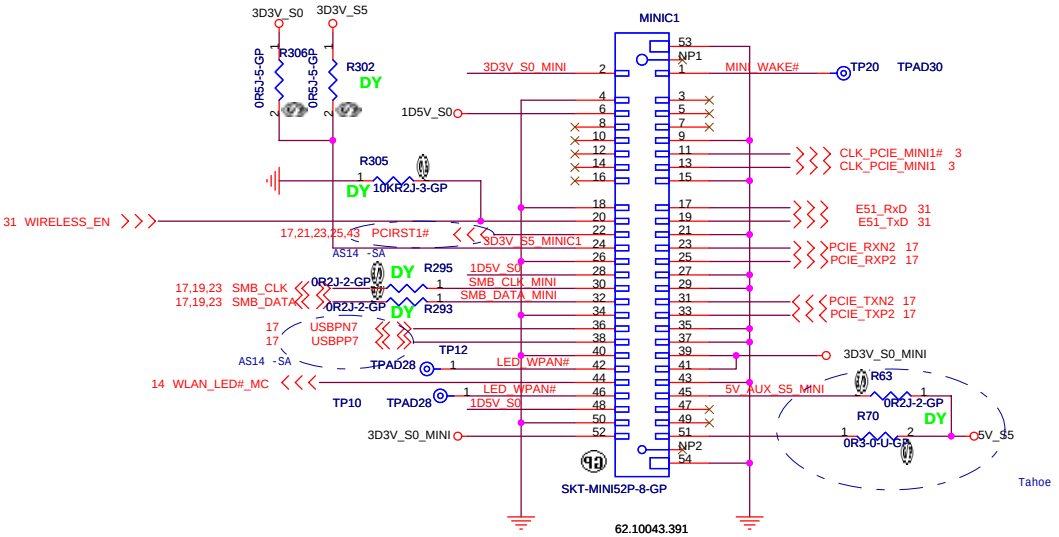


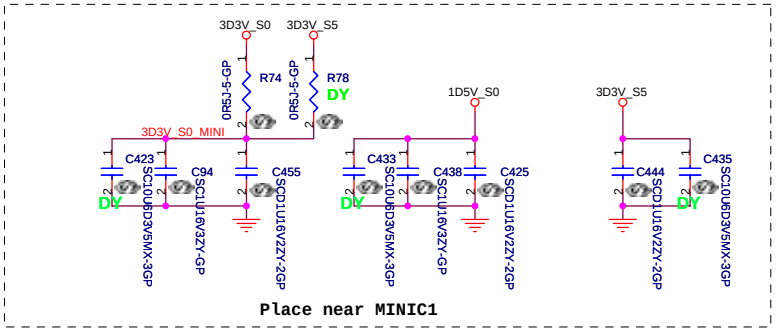






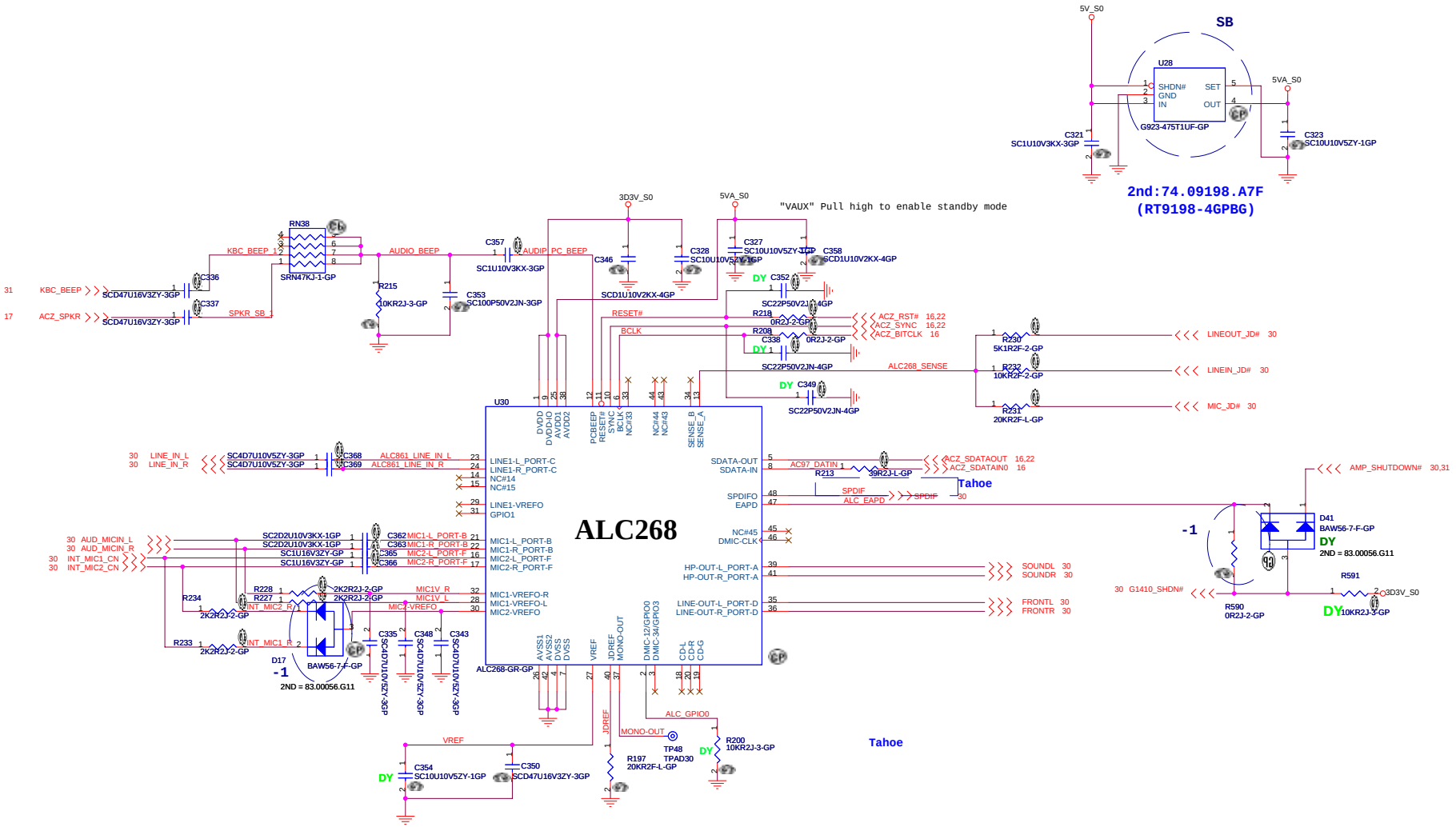






bom1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD / NEW CARD		
Size	Document Number: Tahoe	Rev: -1
Date: Friday, April 27, 2007	Sheet 28 of 44	



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AZALIA CODEC - ALC268

Size	Document Number	Rev
	Tahoe	-1

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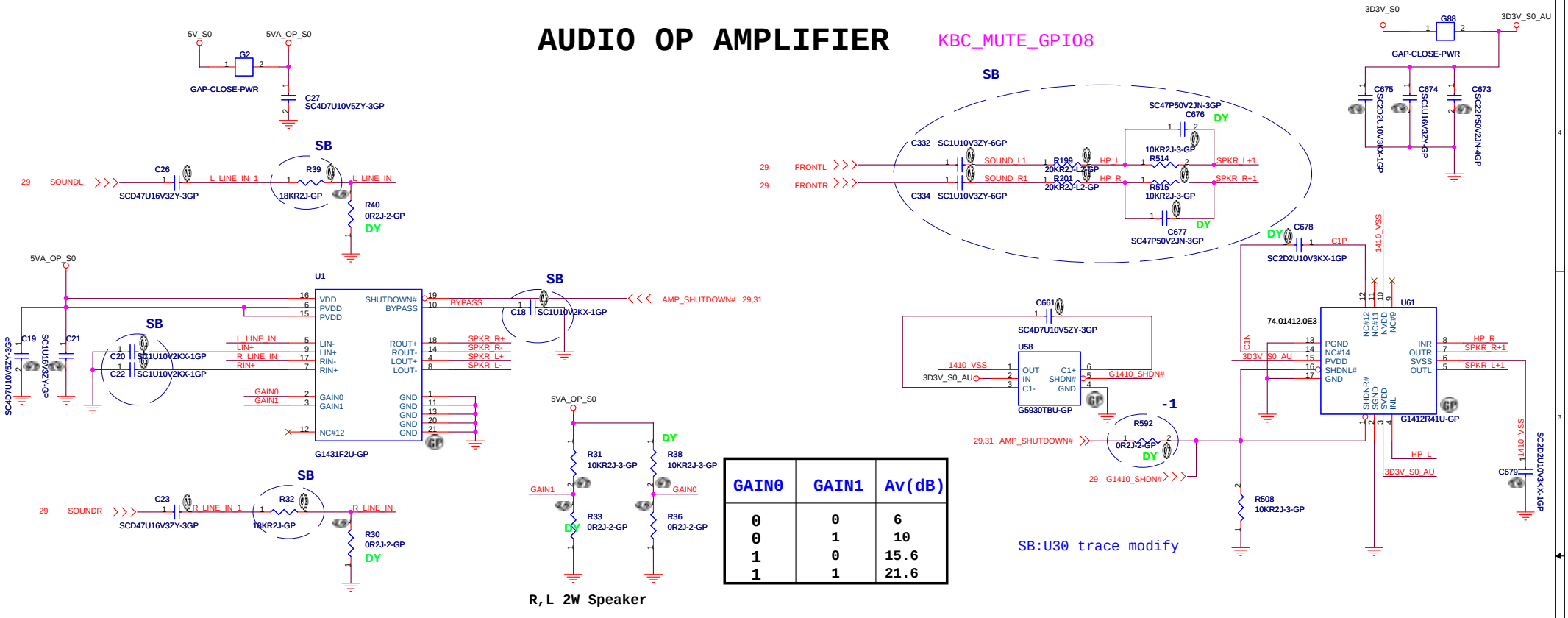
AUDIO OP AMPLIFIER

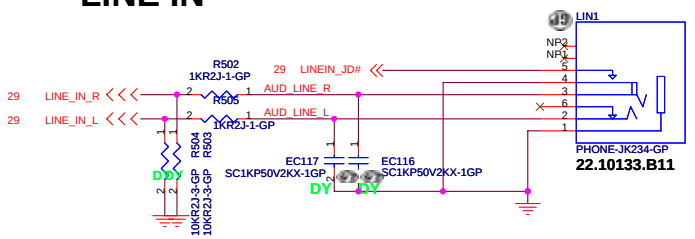
KBC_MUTE_GPIO8



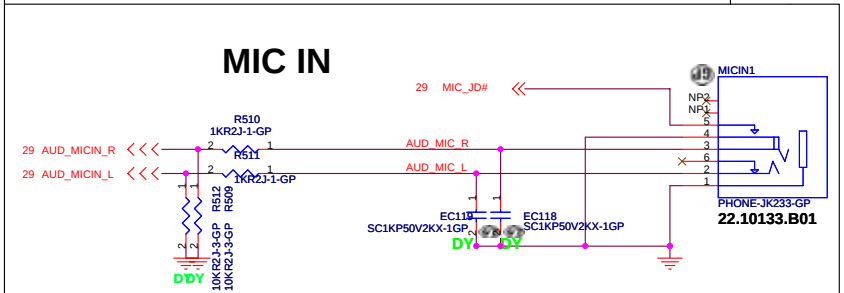
GAIN0	GAIN1	Av(dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

SB:U30 trace modify

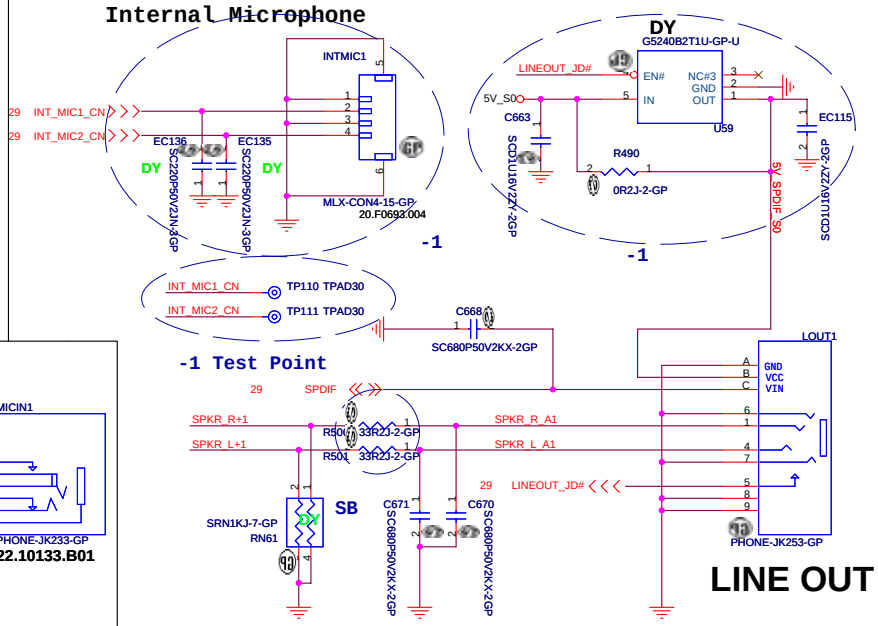
LINE IN



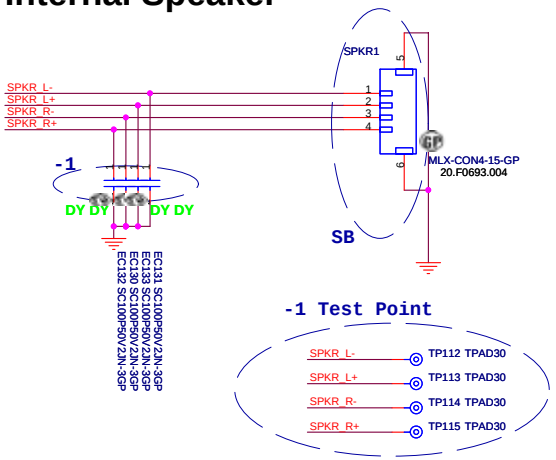
MIC IN



Internal Microphone

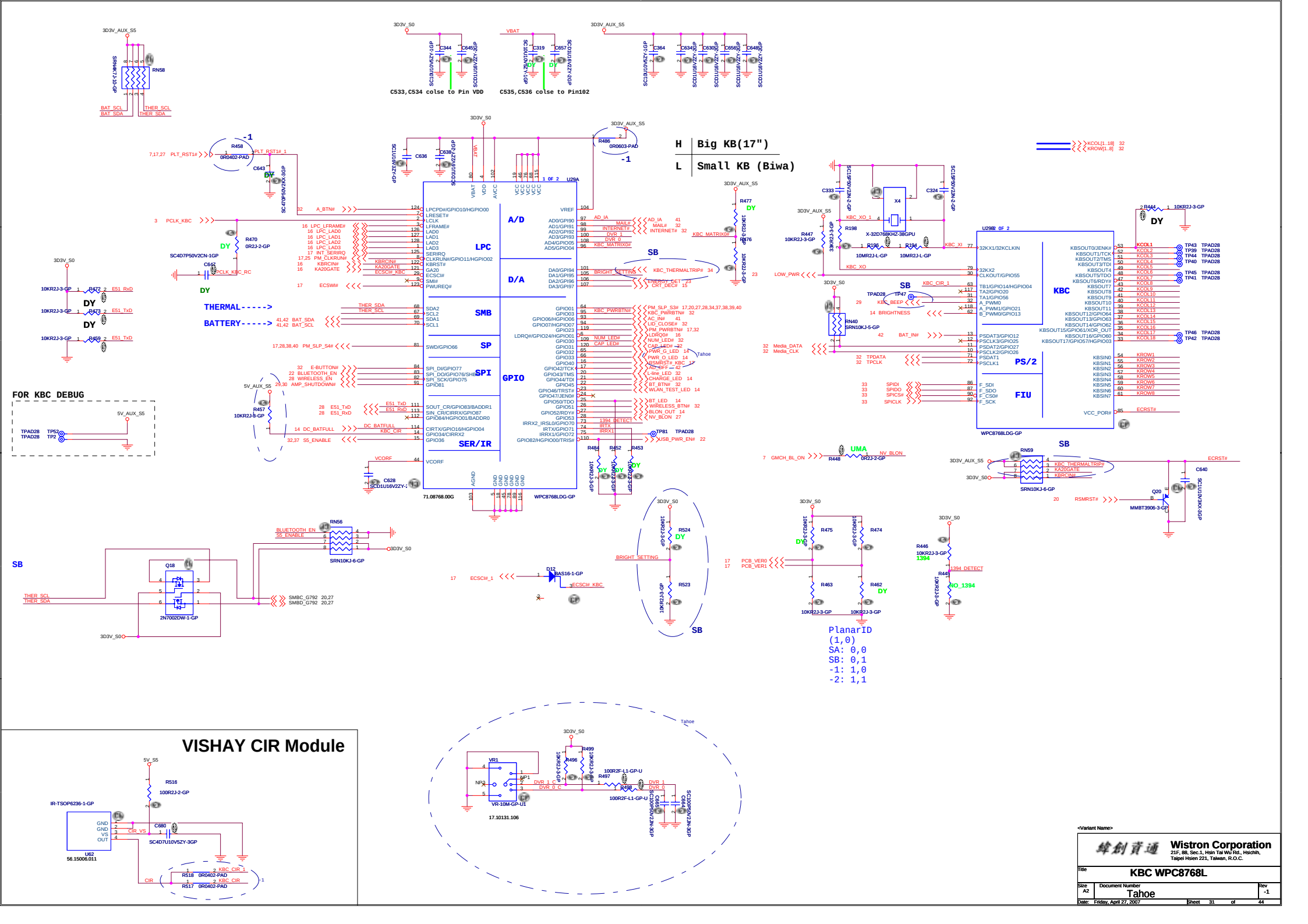


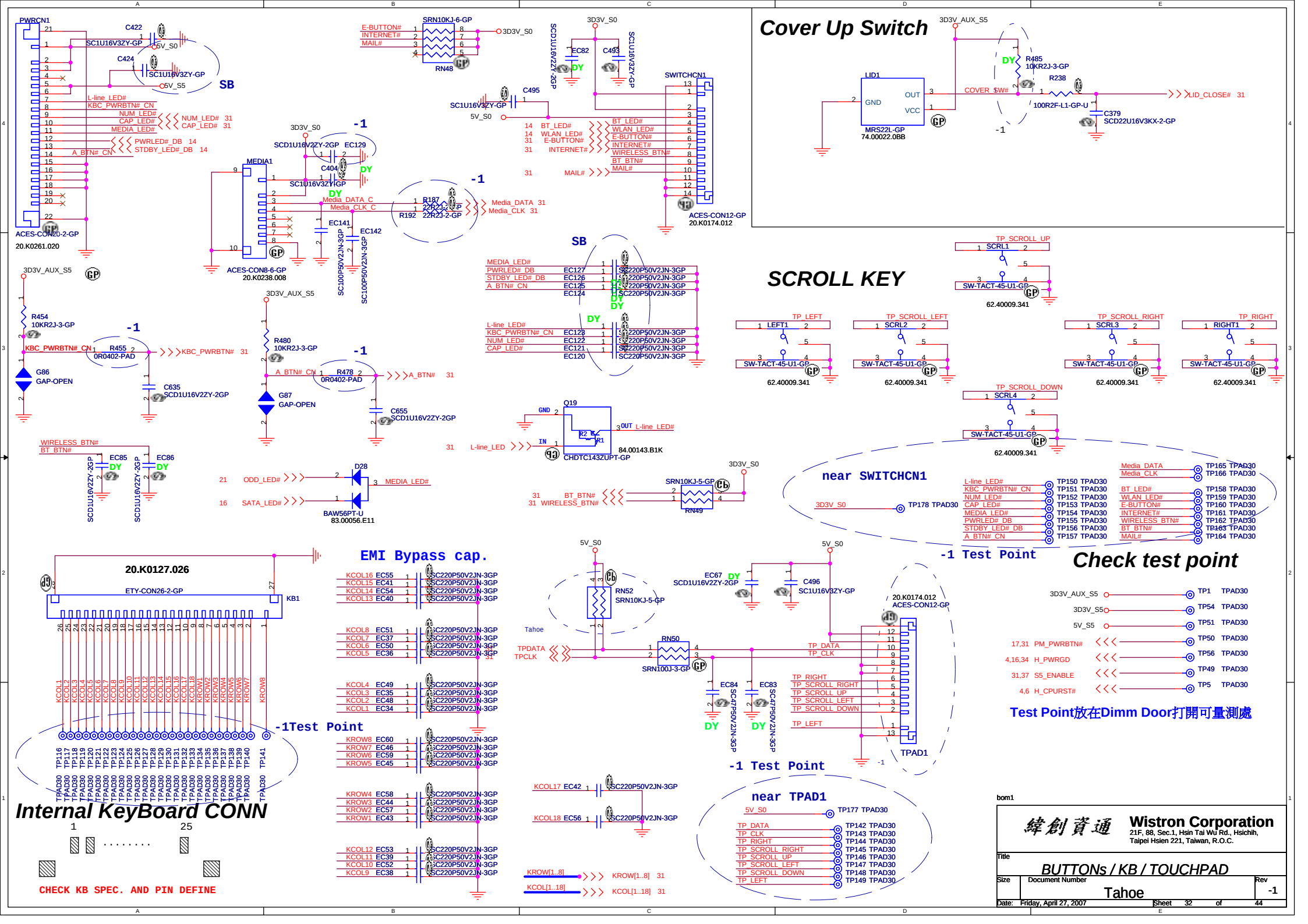
Internal Speaker

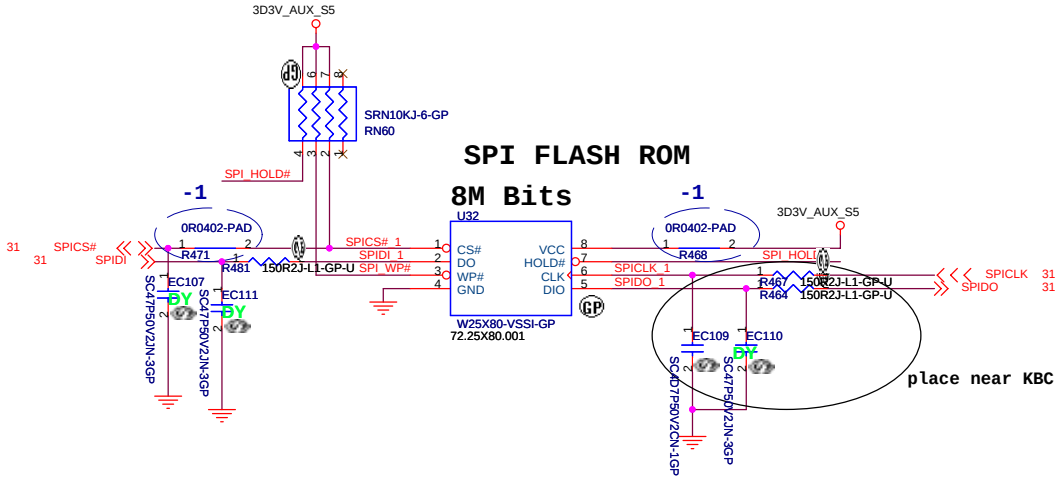


<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO AMP AND JACK	
Size	Document Number: Tahoe	Rev: -1
Date: Friday, April 27, 2007	Sheet 30 of 44	


H | Big KB(17")
L | Small KB (Biwa)
C533,C534 colse to Pin VDD
C535,C536 colse to Pin102
FOR KBC DEBUG
SB
DY
THERMAL----->
BATTERY----->
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
SB
PS/2
FIU
KBC
UMA
VISHAY CIR Module
PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
-2: 1,1
Tahoe
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
Size A2
Document Number Tahoe
Rev -1
Date: Friday, April 27, 2007
Sheet 31 of 44


Cover Up Switch
SCROLL KEY
Internal KeyBoard CONN
EMI Bypass cap.
Check test point
near SWITCHCN1
near TPAD1
-1 Test Point
-1Test Point
SB
CHECK KB SPEC. AND PIN DEFINE
Test Point放在Dimm Door打開可量測處
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BUTTONs / KB / TOUCHPAD
Tahoe
Date: Friday, April 27, 2007
Sheet 32 of 44



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BIOS	
Size: A3	Document Number: Tahoe	Rev: -1
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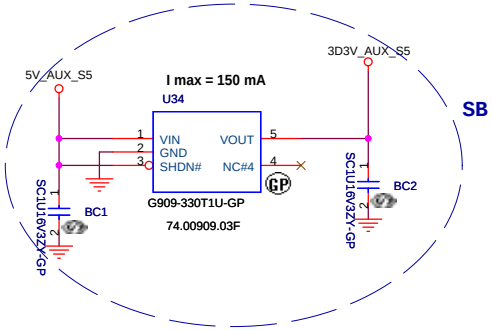
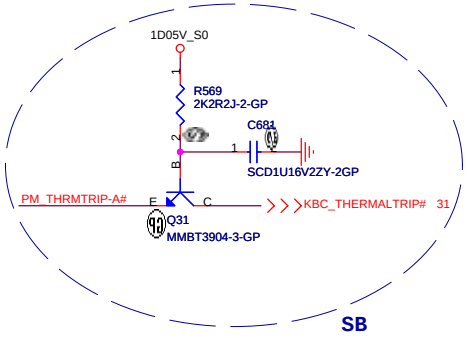
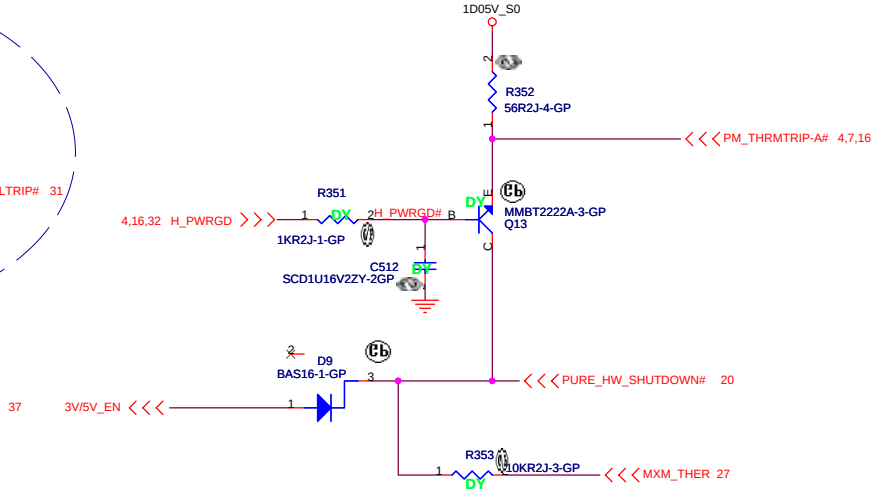
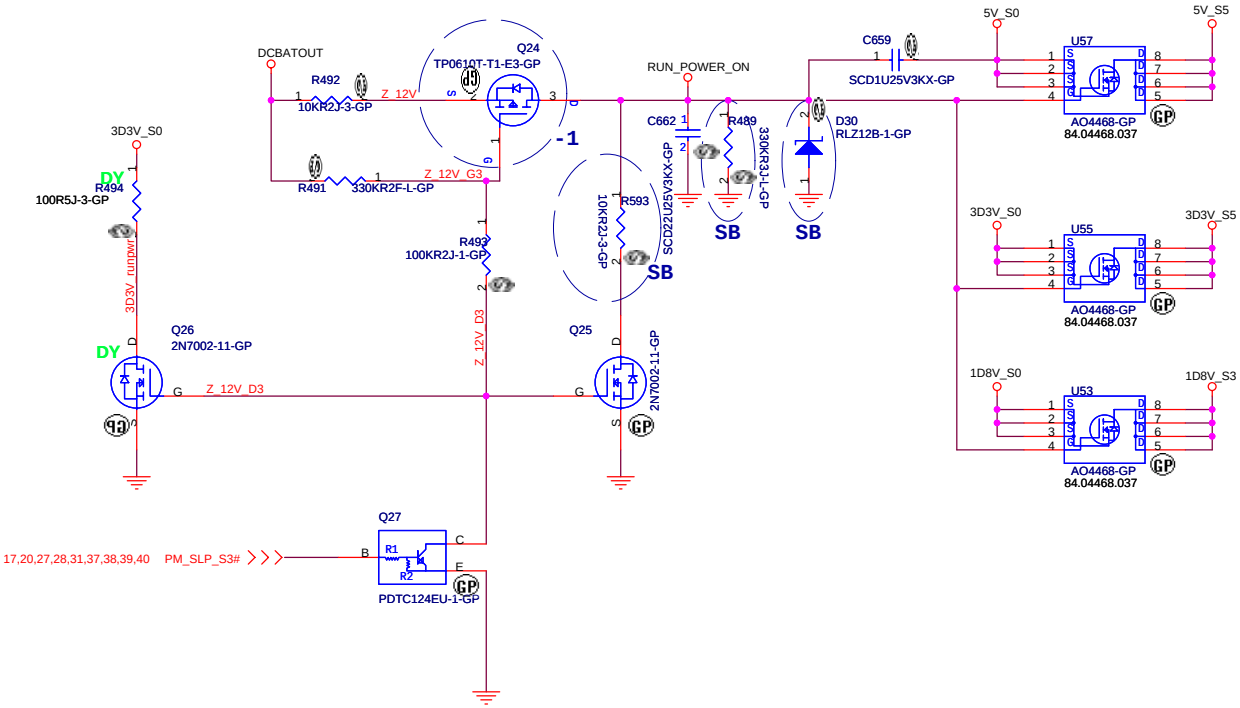
Aux Power 3D3V_AUX_S5







Run Power

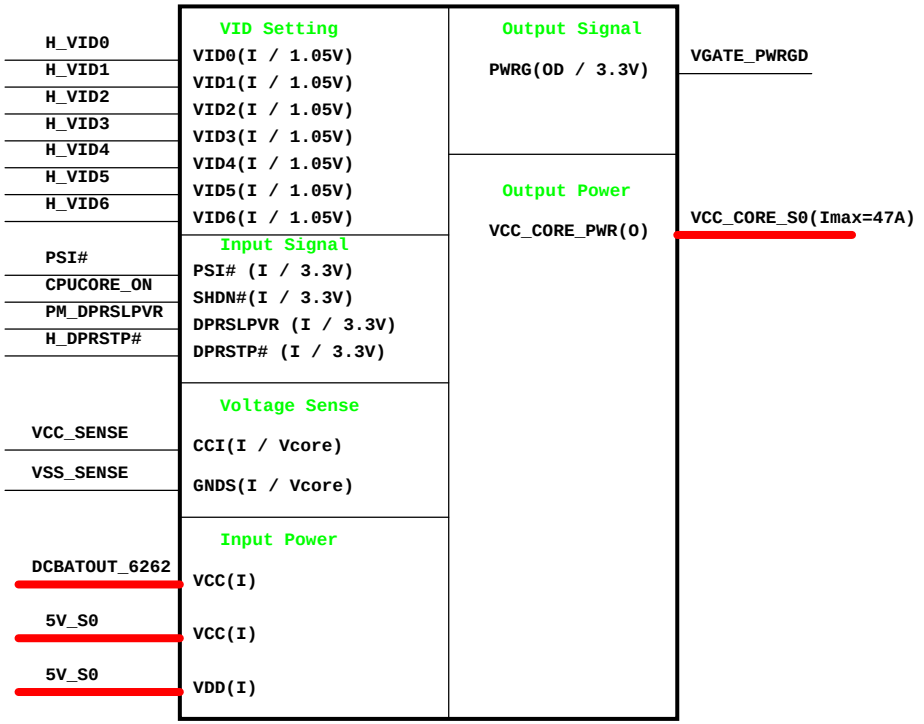


UMA

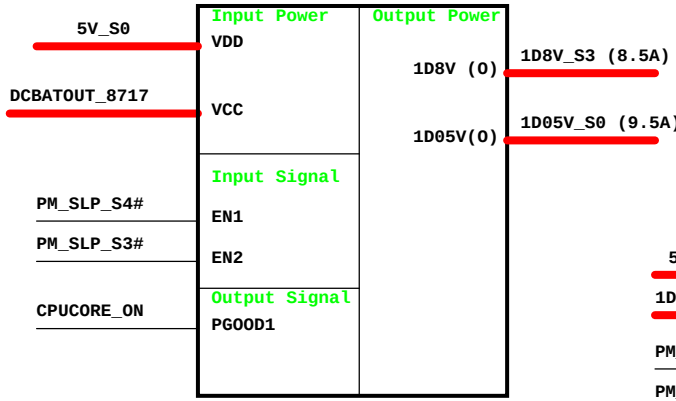
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER and 3D3V_AUX_S5	
Size	Document Number: Tahoe	Rev: -1
Date: Friday, April 27, 2007	Sheet 34 of 44	

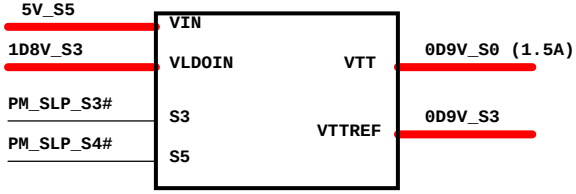
CPU_CORE
MAX8770



MAX8717
1D8V/1D05V

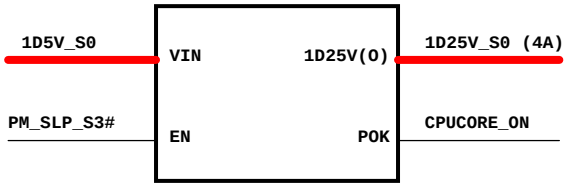


0D9V_S0



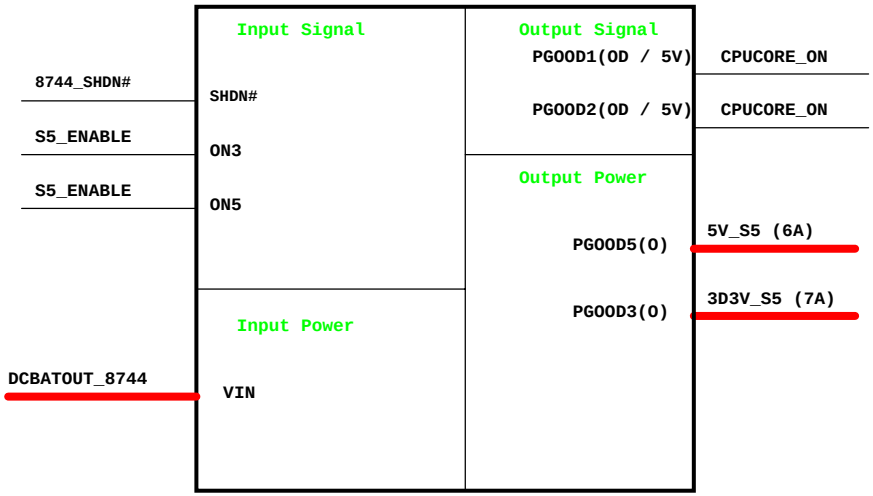
TPS51100

1D25V_S0

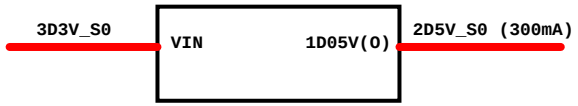


APL5915

MAX8744
5V/3D3V

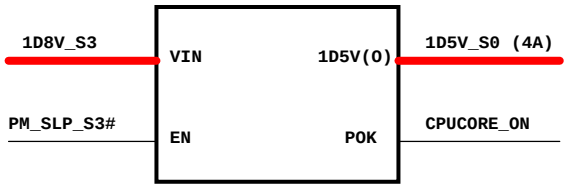


2D5V_S0



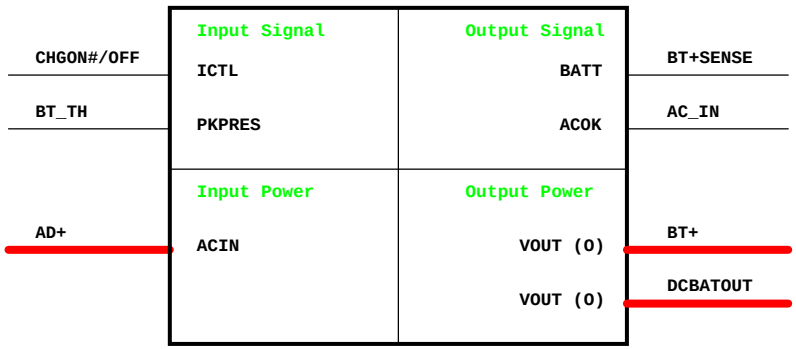
APL5308

1D5V_S0



APL5912

Charger ISL6255



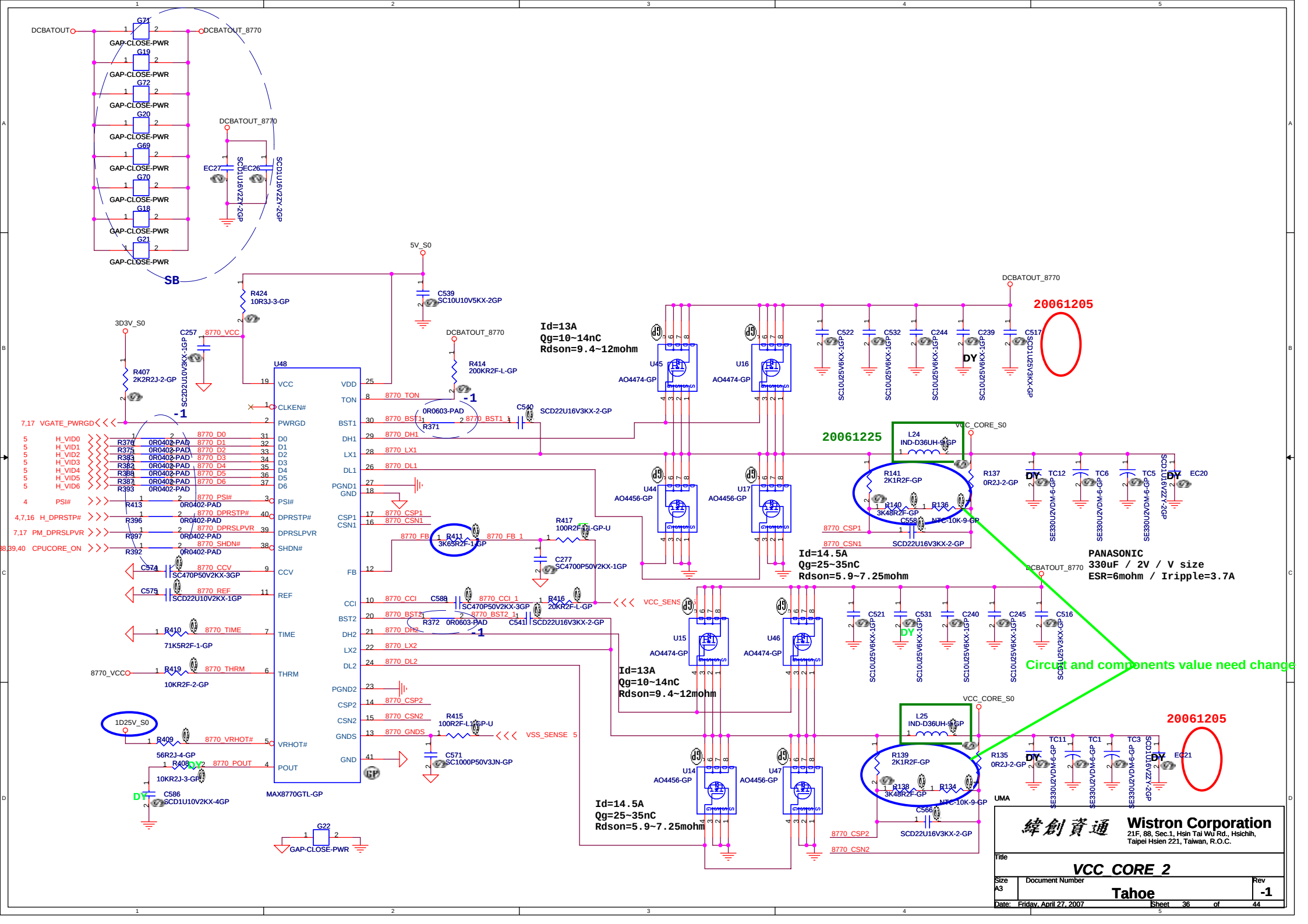
<Variant Name>

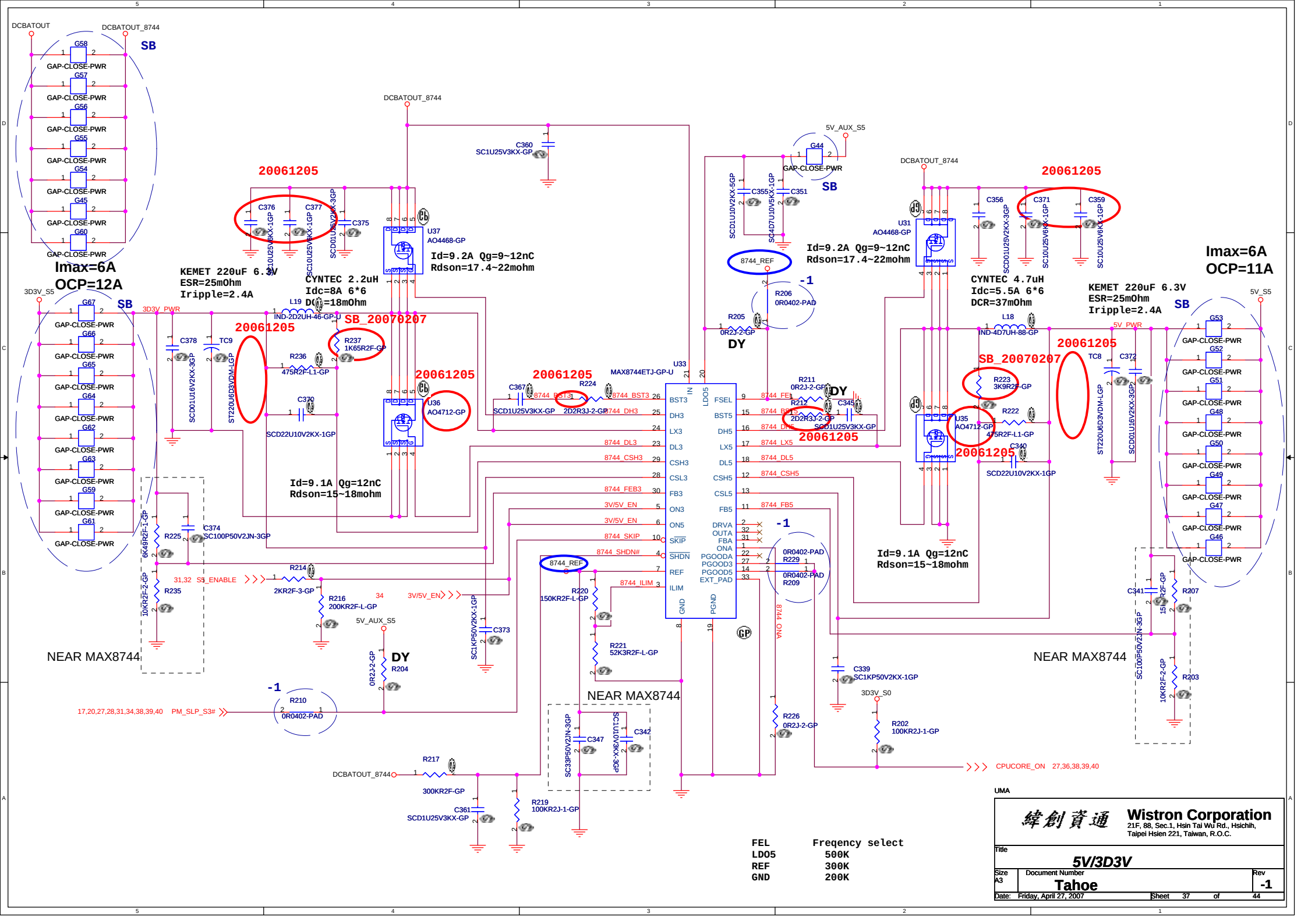
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
A3	Tahoe	-1

Date: Friday, April 27, 2007 Sheet 35 of 44


DCBATOUT
DCBATOUT_8770
GAP-CLOSE-PWR
SB
5V_S0
3D3V_S0
MAX8770GTL-GP
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
20061205
20061225
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
Circuit and components value need change
VCC_CORE_S0
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VCC_CORE_2
Tahoe
Friday, April 27, 2007



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V/3D3V

Size: A3 | Document Number: Tahoe | Rev: -1

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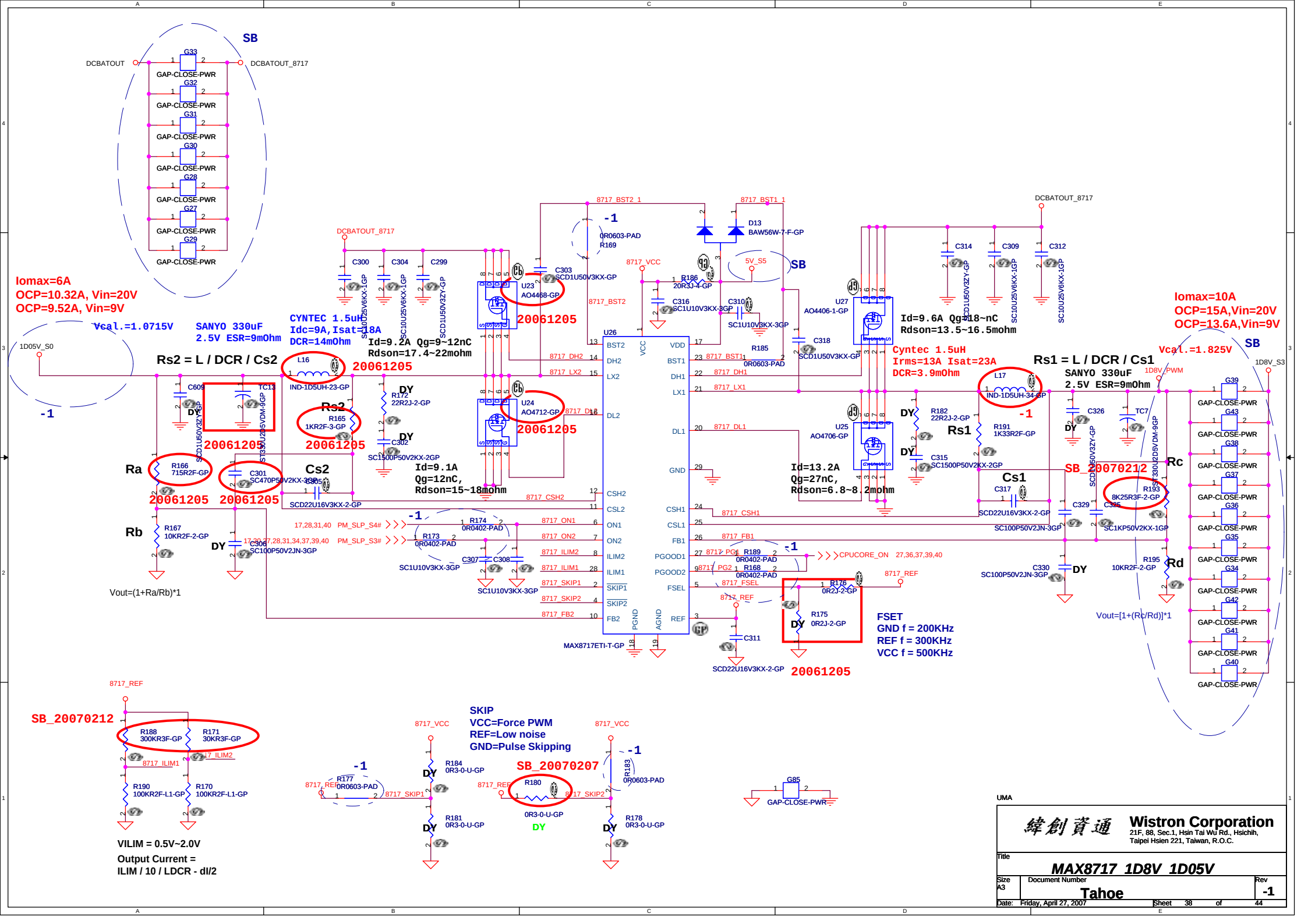
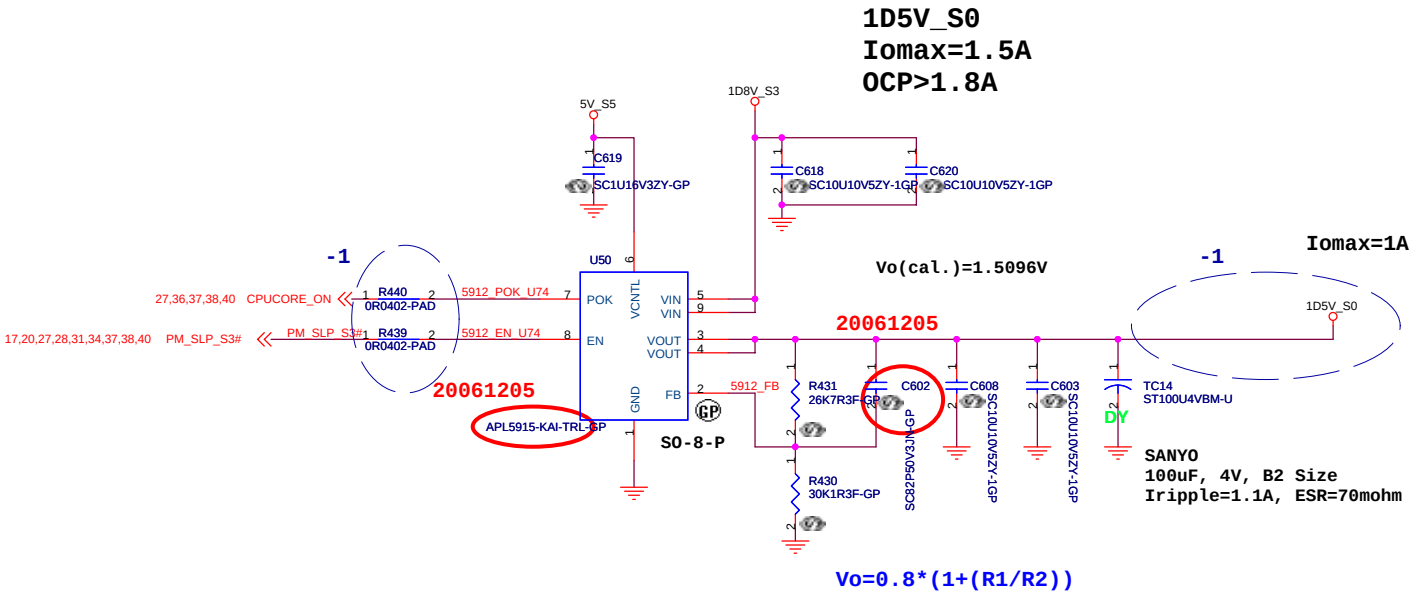

SB
DCBATOUT
DCBATOUT_8717
G33
G32
G31
G30
G28
G27
G29
GAP-CLOSE-PWR
Iomax=6A
OCP=10.32A, Vin=20V
OCP=9.52A, Vin=9V
Vcal.=1.0715V
SANYO 330uF
2.5V ESR=9mOhm
CYNTEC 1.5uH
Idc=9A,Isat=18A
DCR=14mOhm
Id=9.2A Qg=9~12nC
Rdson=17.4~22mohm
1D05V_S0
Rs2 = L / DCR / Cs2
L16
IND-1D5UH-23-GP
20061205
C609
TC13
DY
Rs2
R165
1KR2F-3-GP
R172
22R2J-2-GP
C302
SC1500P50V2KX-2GP
Ra
R166
715R2F-GP
C301
SC470P50V2KX-3GP
C305
SCD22U16V3KX-2-GP
Cs2
Id=9.1A
Qg=12nC,
Rdson=15~18mohm
Rb
R167
10KR2F-2-GP
C306
SC100P50V2JN-3GP
Vout=(1+Ra/Rb)*1
U23
AO4468-GP
U24
AO4712-GP
U26
MAX8717ETI-T-GP
BST2
DH2
LX2
DL2
DL1
GND
CSH2
CSL2
ON1
ON2
ILIM2
ILIM1
SKIP1
SKIP2
FB2
VDD
BST1
DH1
LX1
CSH1
CSL1
FB1
PGOOD1
PGOOD2
FSEL
REF
PGND
AGND
VCC
8717_BST2_1
8717_BST1_1
8717_VCC
8717_BST2
8717_DH2
8717_LX2
8717_DH1
8717_LX1
8717_CSH2
8717_ON1
8717_ON2
8717_ILIM2
8717_ILIM1
8717_SKIP1
8717_SKIP2
8717_FB2
8717_CSH1
8717_FB1
8717_PG1
8717_PG2
8717_FSEL
8717_REF
R169
0R0603-PAD
R186
20R3J-4-GP
C316
SC1U10V3KX-3GP
C310
SC1U10V3KX-3GP
C303
SCD1U50V3KX-GP
R185
0R0603-PAD
D13
BAW56W-7-F-GP
5V_S5
SB
U27
AO4406-1-GP
U25
AO4706-GP
Id=9.6A Qg=18~nC
Rdson=13.5~16.5mohm
Cyntec 1.5uH
Irms=13A Isat=23A
DCR=3.9mOhm
Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm
C318
SCD1U50V3KX-GP
R182
22R2J-2-GP
C315
SC1500P50V2KX-2GP
Rs1
R191
1K33R2F-GP
L17
IND-1D5UH-34-GP
Cs1
C317
SCD22U16V3KX-2-GP
SC100P50V2JN-3GP
C330
SC100P50V2JN-3GP
Rs1 = L / DCR / Cs1
SANYO 330uF
2.5V ESR=9mOhm
Iomax=10A
OCP=15A,Vin=20V
OCP=13.6A,Vin=9V
Vcal.=1.825V
1D8V_S3
1D8V_PWM
SB_20070212
R193
8K25R3F-2-GP
SC1KP50V2KX-1GP
Rc
R195
10KR2F-2-GP
Rd
Vout=[1+(Rc/Rd)]*1
C314
C309
C312
SC10U25V6KX-1GP
SCD1U50V3ZY-GP
C326
C329
C325
C307
C308
SC1U10V3KX-3GP
R174
0R0402-PAD
R173
0R0402-PAD
R189
0R0402-PAD
R168
0R0402-PAD
R176
0R2J-2-GP
R175
0R2J-2-GP
C311
SCD22U16V3KX-2-GP
20061205
FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz
17,28,31,40 PM_SLP_S4#
17,28,31,34,37,39,40 PM_SLP_S3#
CPUCORE_ON 27,36,37,39,40
8717_REF
SB_20070212
R188
300KR3F-GP
R171
30KR3F-GP
R190
100KR2F-L1-GP
R170
100KR2F-L1-GP
VILIM = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - dI/2
SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping
SB_20070207
R177
0R0603-PAD
R180
0R3-0-U-GP
R184
0R3-0-U-GP
R181
0R3-0-U-GP
R183
0R0603-PAD
R178
0R3-0-U-GP
G85
GAP-CLOSE-PWR
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MAX8717 1D8V 1D05V
Size
A3
Document Number
Tahoe
Rev
-1
Date: Friday, April 27, 2007
Sheet 38 of 44



UMA

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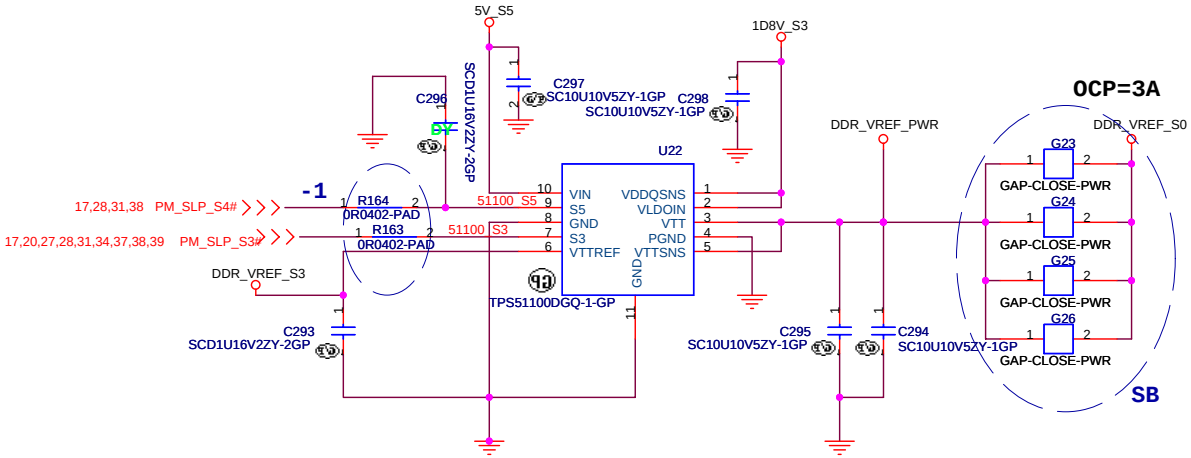
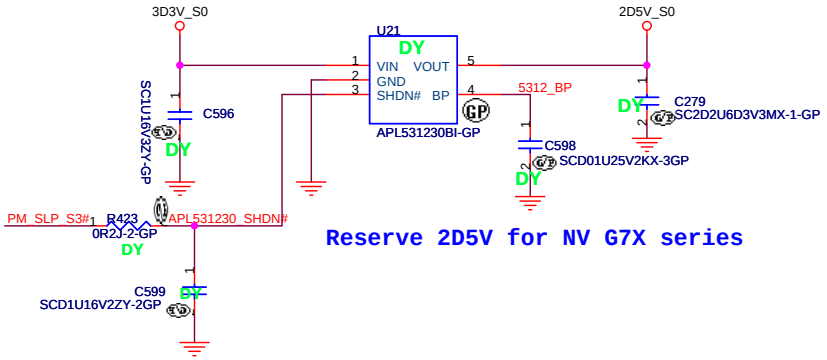
Title	***APW5912_1D5V***	
Size	Document Number: **Tahoe**	Rev: -1
Date: Friday, April 27, 2007	Sheet 39 of 44	

0D9V_S3
Iomax=0.5A

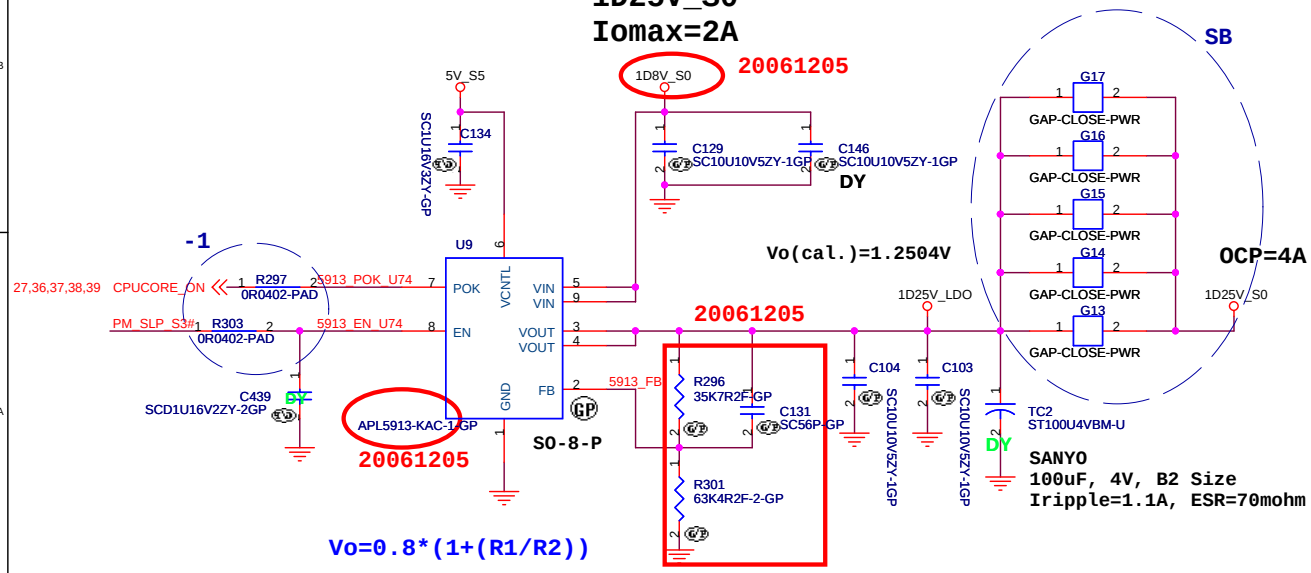


2D5V
Iomax=130mA



Reserve 2D5V for NV G7X series

1D25V_S0
Iomax=2A



Vo=0.8*(1+(R1/R2))

UMA

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Title	1D25V/2D5V//1D05V/0D9V	
Size B	Document Number: Tahoe	Rev: -1
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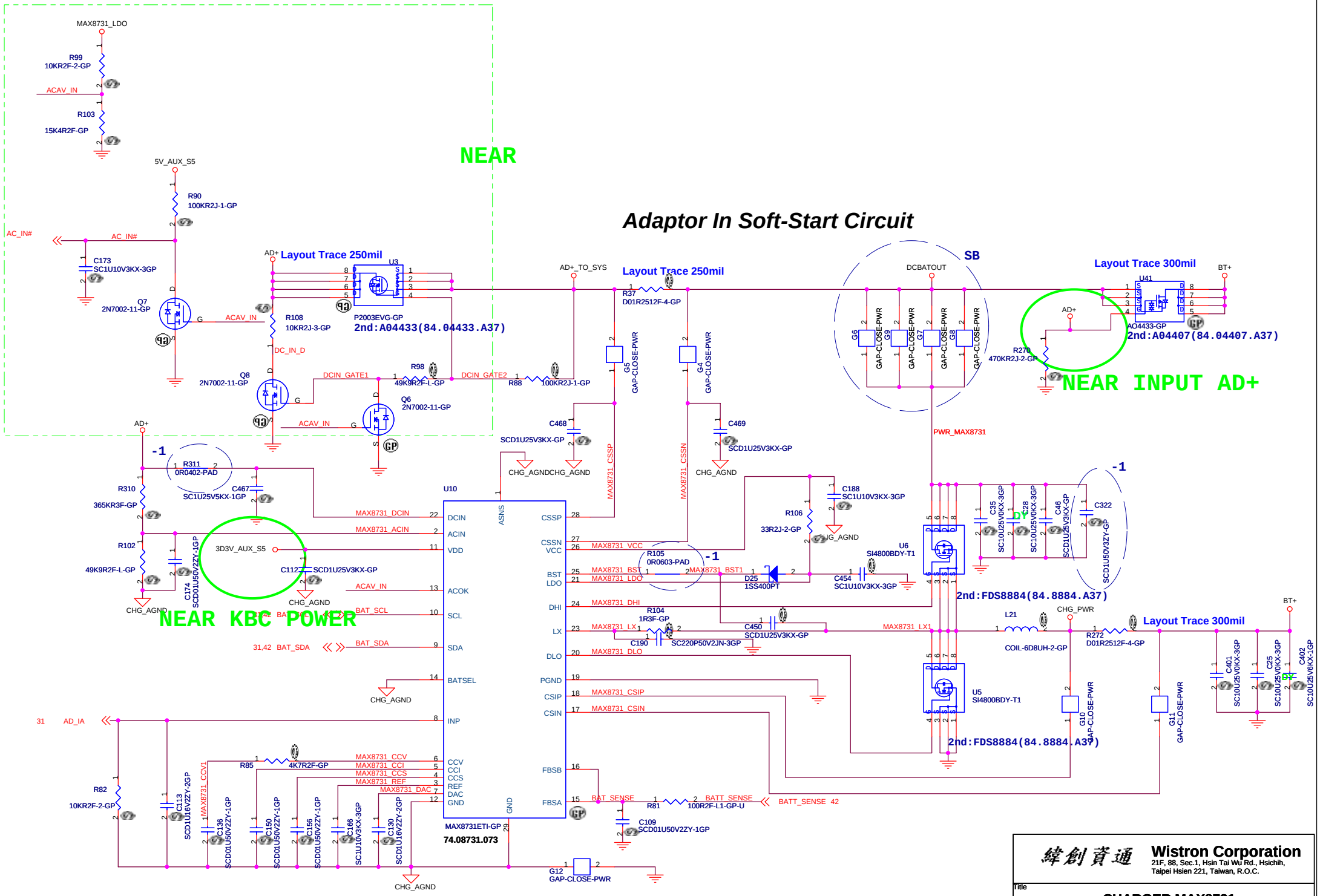

Need Check MAXIM Sming Use MAX8731 or MAX8731A

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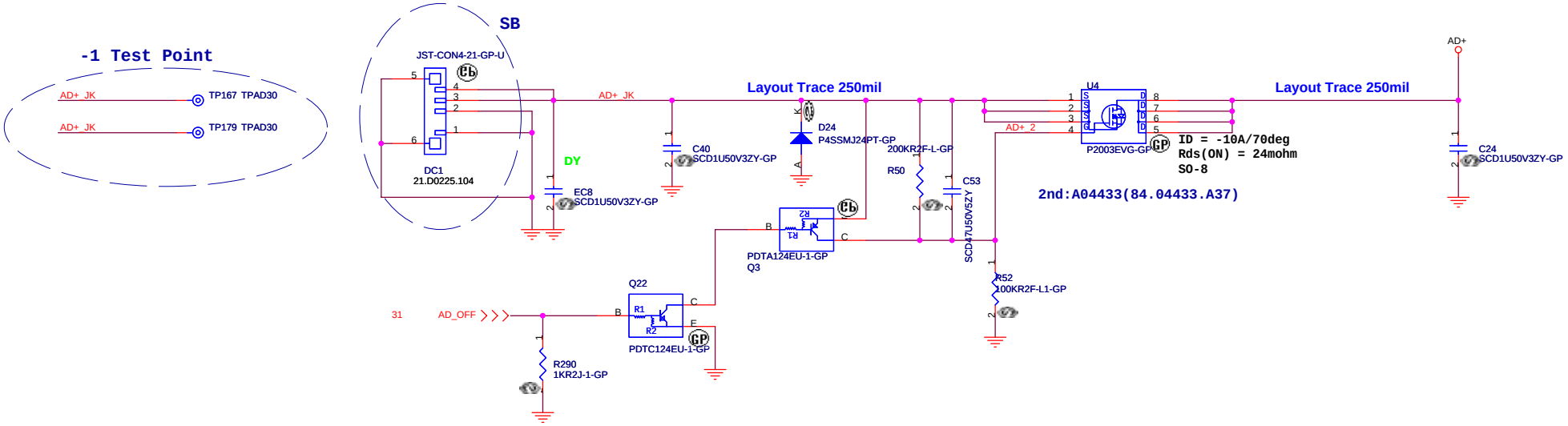
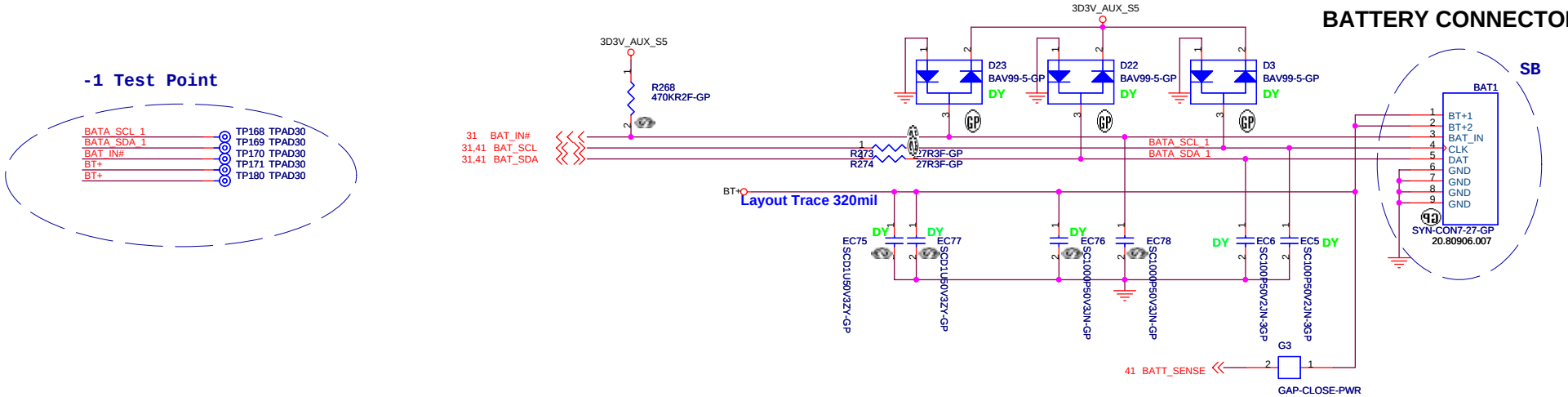
Title	**CHARGER MAX8731**
Size A3	Document Number **Tahoe** Rev **-1**
Date: Friday, April 27, 2007	Sheet 41 of 44

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title	AD/BATT CONN	
Size A3	Document Number: Tahoe	Rev: -1
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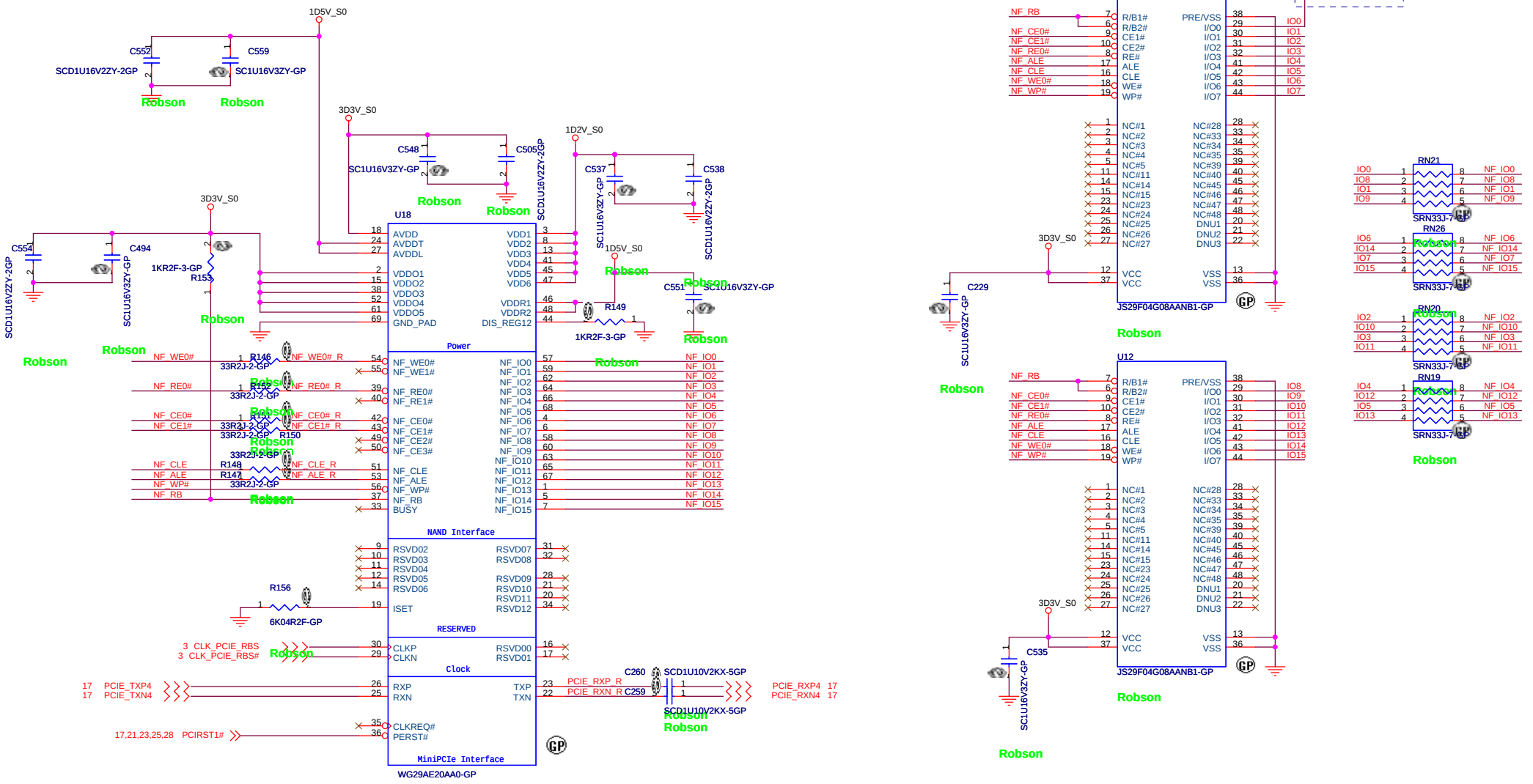
R632
STUFF: INDICATES A 2KB VIRTUAL PAGE
DESTUFF: INDICATES A 4KB VIRTUAL PAGE
R144 DY
10KR2J-3-GP
U13
U12
U18
JS29F04G08AANB1-GP
WG29AE20AA0-GP
Power
NAND Interface
RESERVED
Clock
MiniPCIe Interface
1D5V_S0
3D3V_S0
1D2V_S0
Robson
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
Title
Robson
Size A3
Document Number Tahoe
Rev -1
Date: Thursday, May 17, 2007
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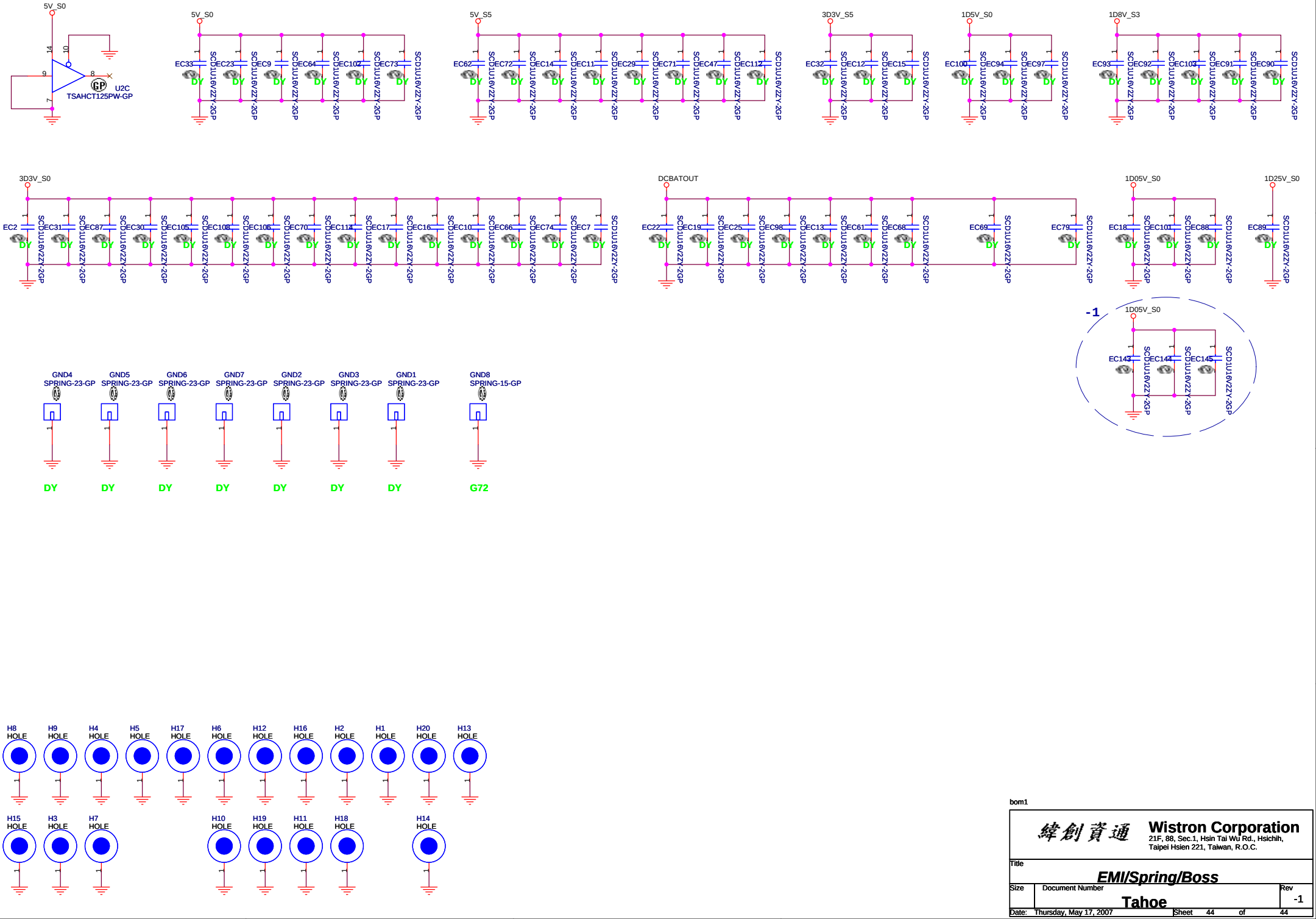

bom1

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Title: ***EMI/Spring/Boss***

Size | Document Number: **Tahoe** | Rev: -1

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