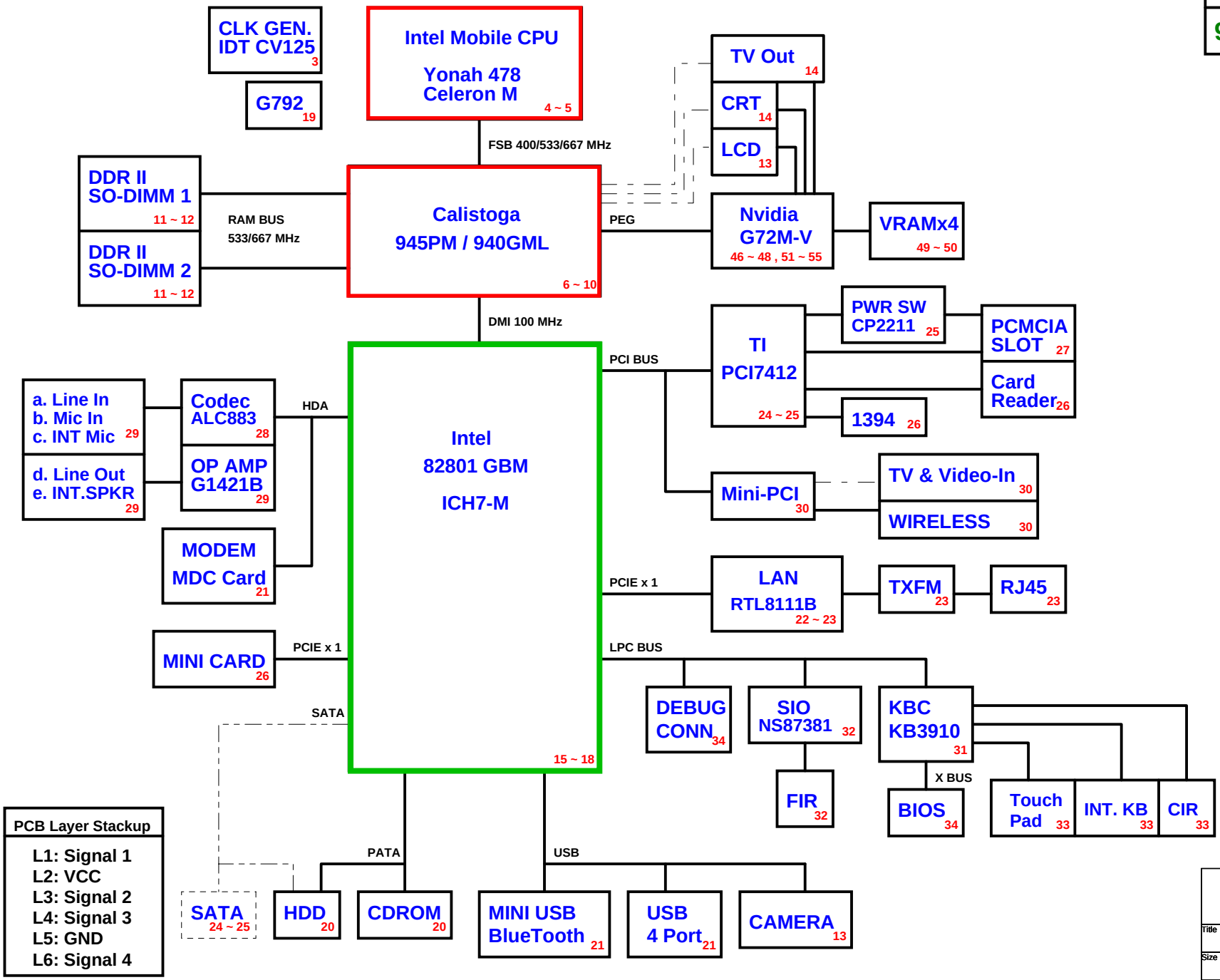
MYALL2 Block Diagram

Project Code	PCB
91.4G901.001	06203-MP



CPU DC/DC
ISL6262 37 ~ 38

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

SYSTEM DC/DC
MAX8744 35

INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

APL5331-KAC
APL5912-KAC
APL5308-25AC 40

INPUTS	OUTPUTS
1D5V_S5	1D05V_S0
1D8V_S3	1D5V_S0
3D3V_S5	1D5V_S5
3D3V_S0	2D5V_S0

APW7057-KC
TPS51100DGQ
APL5331-KAC 41

INPUTS	OUTPUTS
5V_S5	3D3V_S5
5V_S5	1D8V_S3
5V_S5	0D9V
1D8V_S0	1D2V_S0

CHARGER
ISL6255 42

INPUTS	OUTPUTS
DCBATOUT	BT+ 16.8V 3A

PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Signal 2
L4: Signal 4
L5: GND
L6: Signal 4

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Title: BLOCK DIAGRAM

Size | Document Number: MYALL2 | Rev: MP

Date: Tuesday, April 11, 2006 | Sheet 1 of 57

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+-0.25 Center
1	0	0	1	+-0.5 Center
1	0	1	0	+-0.75 Center
1	0	1	1	+-1.0 Center
1	1	0	0	+-0.25 Center
1	1	0	1	+-0.5 Center
1	1	1	0	+-0.75 Center
1	1	1	1	+-1.0 Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
7412	22	A->G, B->B, C->F, D->G	0
MiniPCI	21	A/C -> E B/D -> E	1

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

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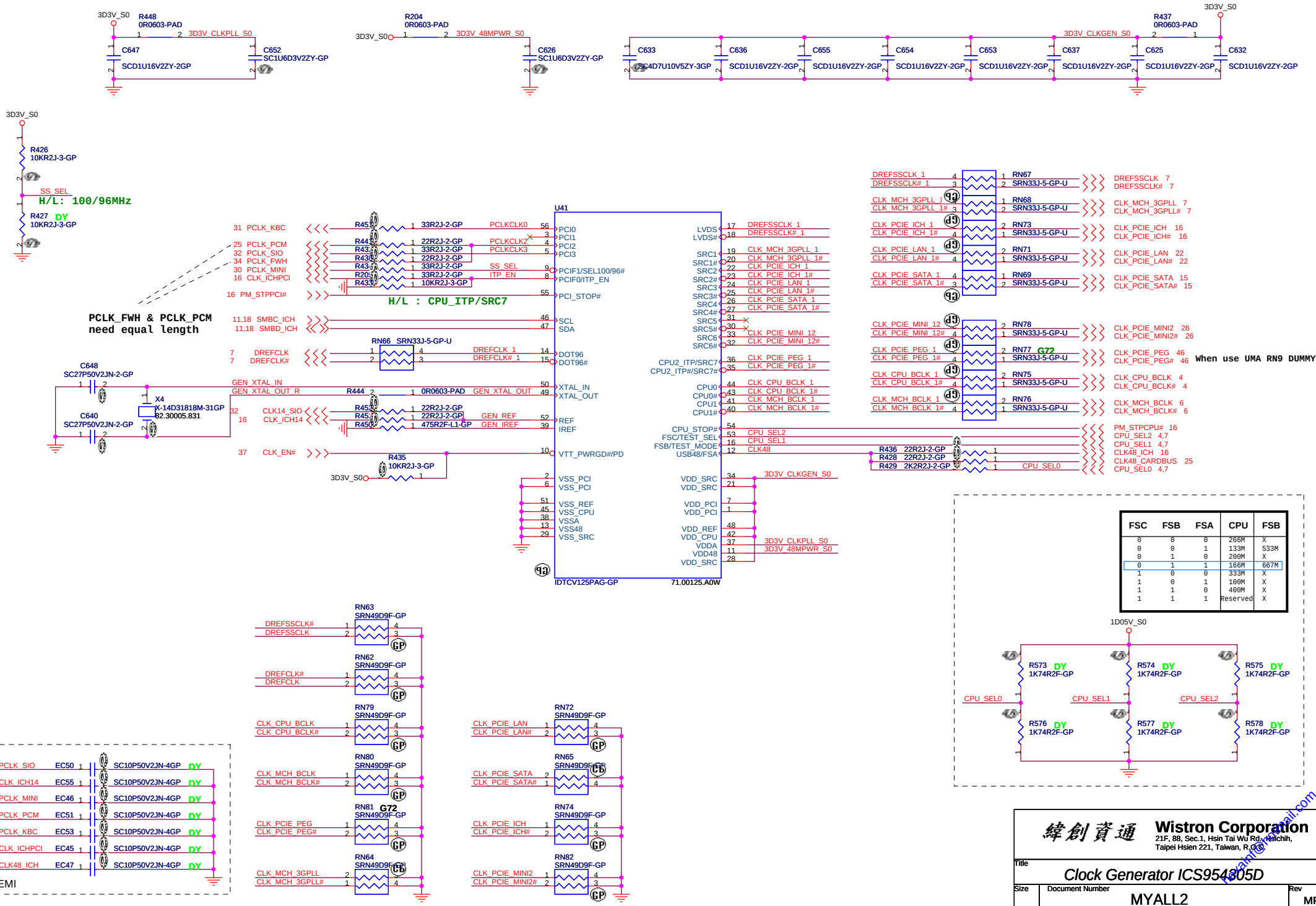
Title: Reference

Size | Document Number: MYALL2 | Rev: MP

Date: Friday, March 24, 2006 | Sheet 2 of 57


3D3V_S0
R448 0R0603-PAD
3D3V_CLKPLL_S0
C647 SCD1U16V2ZY-2GP
C652 SC1U6D3V2ZY-GP
R204 0R0603-PAD
3D3V_48MPWR_S0
C626 SC1U6D3V2ZY-GP
C633 SC4D7U10V5ZY-3GP
C636 SCD1U16V2ZY-2GP
C655 SCD1U16V2ZY-2GP
C654 SCD1U16V2ZY-2GP
C653 SCD1U16V2ZY-2GP
C637 SCD1U16V2ZY-2GP
C625 SCD1U16V2ZY-2GP
C632 SCD1U16V2ZY-2GP
3D3V_CLKGEN_S0
R437 0R0603-PAD
R426 10KR2J-3-GP
SS_SEL
H/L: 100/96MHz
R427 10KR2J-3-GP DY
PCLK_FWH & PCLK_PCM
need equal length
31 PCLK_KBC
25 PCLK_PCM
32 PCLK_SIO
34 PCLK_FWH
30 PCLK_MINI
16 CLK_ICHPCI
16 PM_STPPCI#
R451 33R2J-2-GP PCLKCLK0
R441 22R2J-2-GP
R443 33R2J-2-GP PCLKCLK2
R439 22R2J-2-GP
R438 33R2J-2-GP PCLKCLK3
R420 33R2J-2-GP SS_SEL
R433 10KR2J-3-GP ITP_EN
H/L : CPU_ITP/SRC7
11,18 SMBC_ICH
11,18 SMBD_ICH
RN66 SRN33J-5-GP-U
7 DREFCLK
7 DREFCLK#
DREFCLK_1
DREFCLK# 1
C648 SC27P50V2JN-2GP
C640 SC27P50V2JN-2GP
X4 X-14D31818M-31GP 82.30005.831
GEN_XTAL_IN
GEN_XTAL_OUT_R
R444 0R0603-PAD
GEN_XTAL_OUT
32 CLK14_SIO
16 CLK_ICH14
R452 22R2J-2-GP
R453 22R2J-2-GP
GEN_REF
R450 475R2F-L1-GP
GEN_IREF
37 CLK_EN#
R435 10KR2J-3-GP
3D3V_S0
U41
PCI0
PCI1
PCI2
PCI3
PCIF1/SEL100/96#
PCIF0/ITP_EN
PCI_STOP#
SCL
SDA
DOT96
DOT96#
XTAL_IN
XTAL_OUT
REF
IREF
VTT_PWRGD#/PD
VSS_PCI
VSS_PCI
VSS_REF
VSS_CPU
VSSA
VSS48
VSS_SRC
LVDS
LVDS#
SRC1
SRC1#
SRC2
SRC2#
SRC3
SRC3#
SRC4
SRC4#
SRC5
SRC5#
SRC6
SRC6#
CPU2_ITP/SRC7
CPU2_ITP#/SRC7#
CPU0
CPU0#
CPU1
CPU1#
CPU_STOP#
FSC/TEST_SEL
FSB/TEST_MODE
USB48/FSA
VDD_SRC
VDD_SRC
VDD_PCI
VDD_PCI
VDD_REF
VDD_CPU
VDDA
VDD48
VDD_SRC
IDTCV125PAG-GP
71.00125.A0W
DREFSSCLK_1
DREFSSCLK# 1
CLK_MCH_3GPLL_1
CLK_MCH_3GPLL_1#
CLK_PCIE_ICH_1
CLK_PCIE_ICH_1#
CLK_PCIE_LAN_1
CLK_PCIE_LAN_1#
CLK_PCIE_SATA_1
CLK_PCIE_SATA_1#
CLK_PCIE_MINI_12
CLK_PCIE_MINI_12#
CLK_PCIE_PEG_1
CLK_PCIE_PEG_1#
CLK_CPU_BCLK_1
CLK_CPU_BCLK_1#
CLK_MCH_BCLK_1
CLK_MCH_BCLK_1#
CPU_SEL2
CPU_SEL1
CLK48
3D3V_CLKGEN_S0
3D3V_CLKPLL_S0
3D3V_48MPWR_S0
R436 22R2J-2-GP
R428 22R2J-2-GP
R429 2K2R2J-2-GP
CPU_SEL0
RN67 SRN33J-5-GP-U
DREFSSCLK_1
DREFSSCLK# 1
DREFSSCLK_7
DREFSSCLK#_7
RN68 SRN33J-5-GP-U
CLK_MCH_3GPLL_1
CLK_MCH_3GPLL_1#
CLK_MCH_3GPLL_7
CLK_MCH_3GPLL#_7
RN73 SRN33J-5-GP-U
CLK_PCIE_ICH_1
CLK_PCIE_ICH_1#
CLK_PCIE_ICH_16
CLK_PCIE_ICH#_16
RN71 SRN33J-5-GP-U
CLK_PCIE_LAN_1
CLK_PCIE_LAN_1#
CLK_PCIE_LAN_22
CLK_PCIE_LAN#_22
RN69 SRN33J-5-GP-U
CLK_PCIE_SATA_1
CLK_PCIE_SATA_1#
CLK_PCIE_SATA_15
CLK_PCIE_SATA#_15
RN78 SRN33J-5-GP-U
CLK_PCIE_MINI_12
CLK_PCIE_MINI_12#
CLK_PCIE_MINI2_26
CLK_PCIE_MINI2#_26
RN77 G72 SRN33J-5-GP-U
CLK_PCIE_PEG_1
CLK_PCIE_PEG_1#
CLK_PCIE_PEG_46
CLK_PCIE_PEG#_46
When use UMA RN9 DUMMY
RN75 SRN33J-5-GP-U
CLK_CPU_BCLK_1
CLK_CPU_BCLK_1#
CLK_CPU_BCLK_4
CLK_CPU_BCLK#_4
RN76 SRN33J-5-GP-U
CLK_MCH_BCLK_1
CLK_MCH_BCLK_1#
CLK_MCH_BCLK_6
CLK_MCH_BCLK#_6
PM_STPCPU#_16
CPU_SEL2_4,7
CPU_SEL1_4,7
CLK48_ICH_16
CLK48_CARDBUS_25
CPU_SEL0_4,7
FSC FSB FSA CPU FSB
0 0 0 266M X
0 0 1 133M 533M
0 1 0 200M X
0 1 1 166M 667M
1 0 0 333M X
1 0 1 100M X
1 1 0 400M X
1 1 1 Reserved X
1D05V_S0
R573 DY 1K74R2F-GP
R574 DY 1K74R2F-GP
R575 DY 1K74R2F-GP
R576 DY 1K74R2F-GP
R577 DY 1K74R2F-GP
R578 DY 1K74R2F-GP
CPU_SEL0
CPU_SEL1
CPU_SEL2
RN63 SRN49D9F-GP
DREFSSCLK#
DREFSSCLK
RN62 SRN49D9F-GP
DREFCLK#
DREFCLK
RN79 SRN49D9F-GP
CLK_CPU_BCLK
CLK_CPU_BCLK#
RN80 SRN49D9F-GP
CLK_MCH_BCLK
CLK_MCH_BCLK#
RN81 G72 SRN49D9F-GP
CLK_PCIE_PEG
CLK_PCIE_PEG#
RN64 SRN49D9F-GP
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
RN72 SRN49D9F-GP
CLK_PCIE_LAN
CLK_PCIE_LAN#
RN65 SRN49D9F-GP
CLK_PCIE_SATA
CLK_PCIE_SATA#
RN74 SRN49D9F-GP
CLK_PCIE_ICH
CLK_PCIE_ICH#
RN82 SRN49D9F-GP
CLK_PCIE_MINI2
CLK_PCIE_MINI2#
PCLK_SIO EC50 SC10P50V2JN-4GP DY
CLK_ICH14 EC55 SC10P50V2JN-4GP DY
PCLK_MINI EC46 SC10P50V2JN-4GP DY
PCLK_PCM EC51 SC10P50V2JN-4GP DY
PCLK_KBC EC53 SC10P50V2JN-4GP DY
CLK_ICHPCI EC45 SC10P50V2JN-4GP DY
CLK48_ICH EC47 SC10P50V2JN-4GP DY
EMI
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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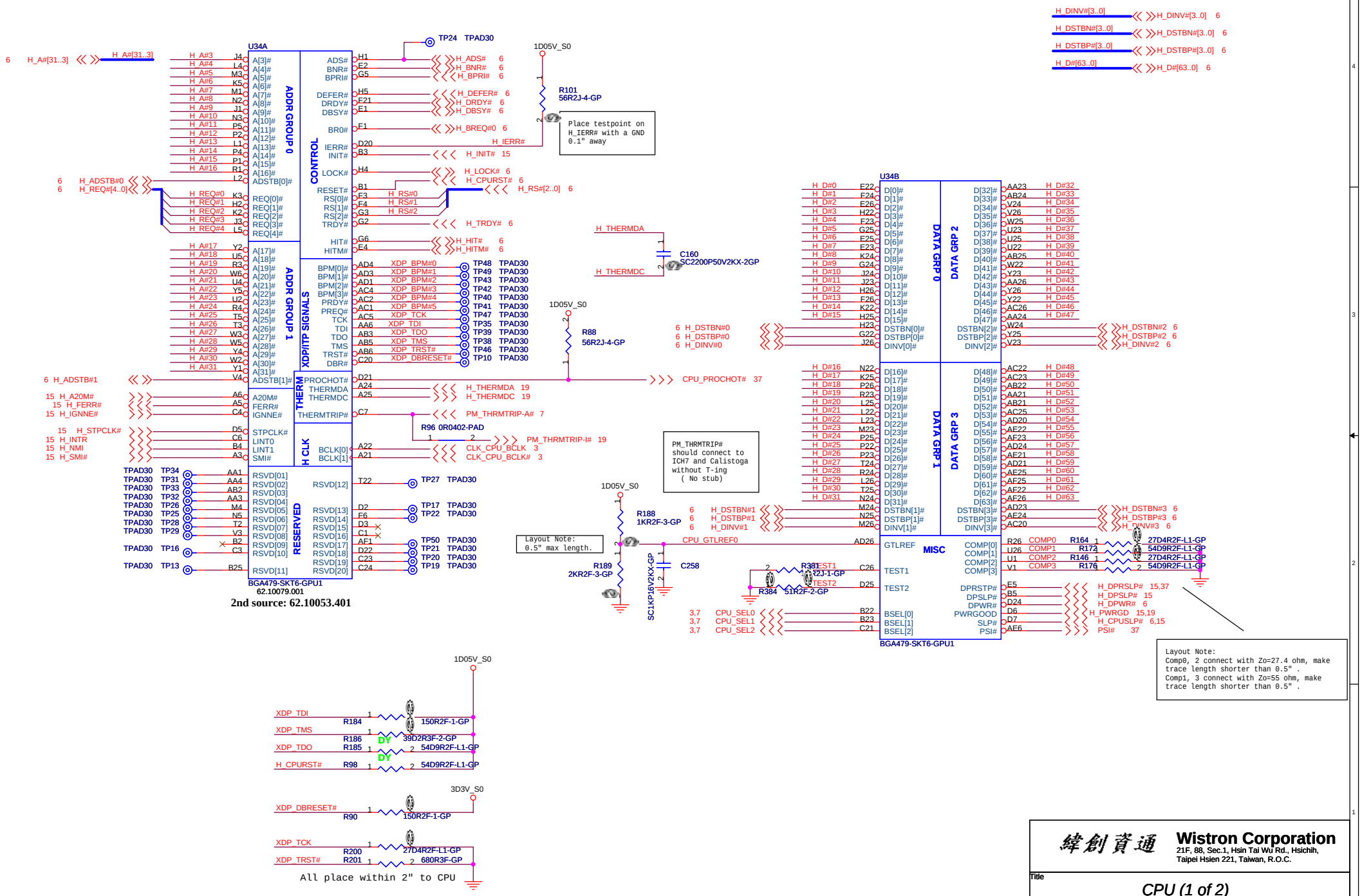
Title
Clock Generator ICS954305D
Size
Document Number
MYALL2
Rev
MP
Date: Thursday, March 30, 2006
Sheet 3 of 57



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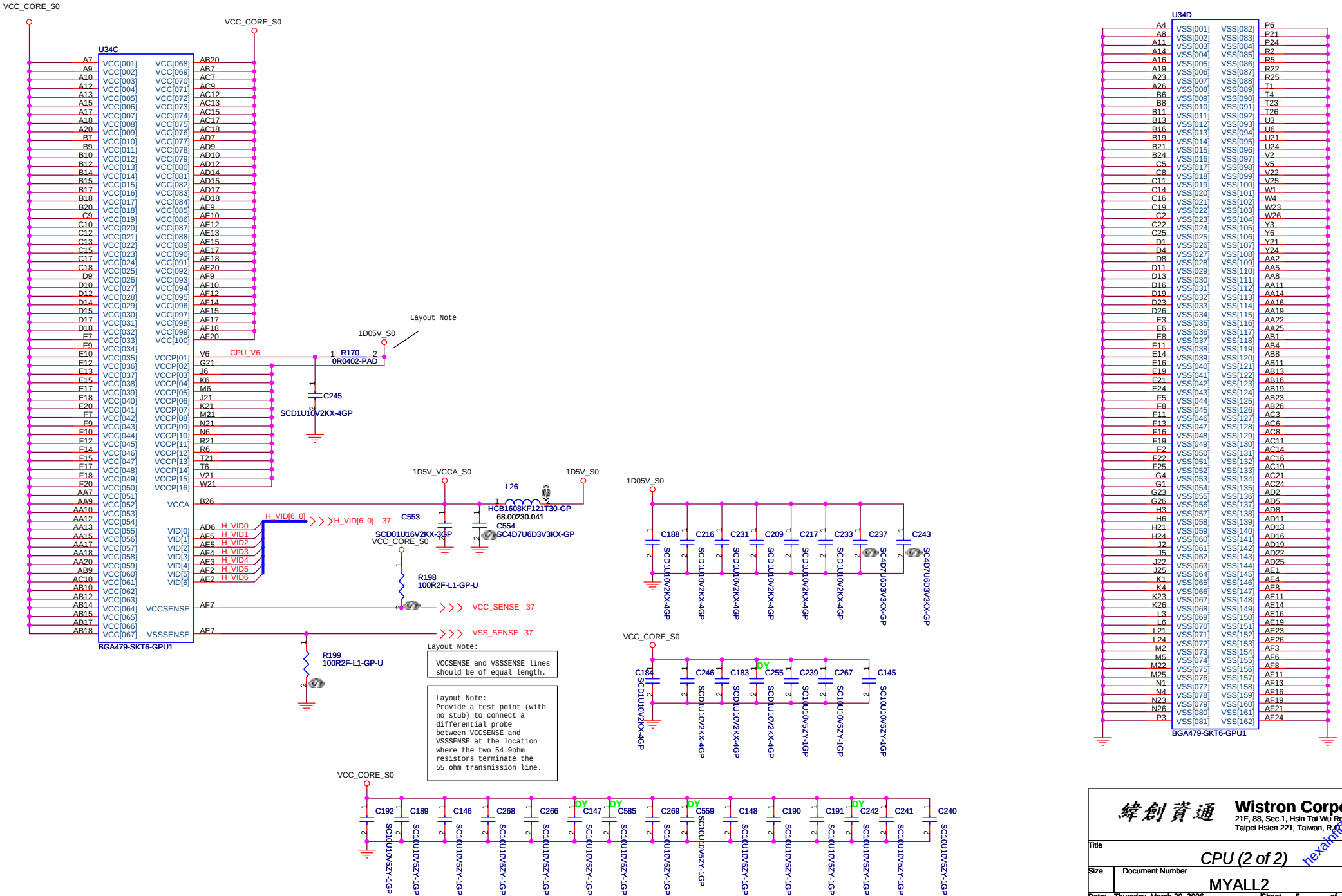

Company	Wistron Corporation
Address	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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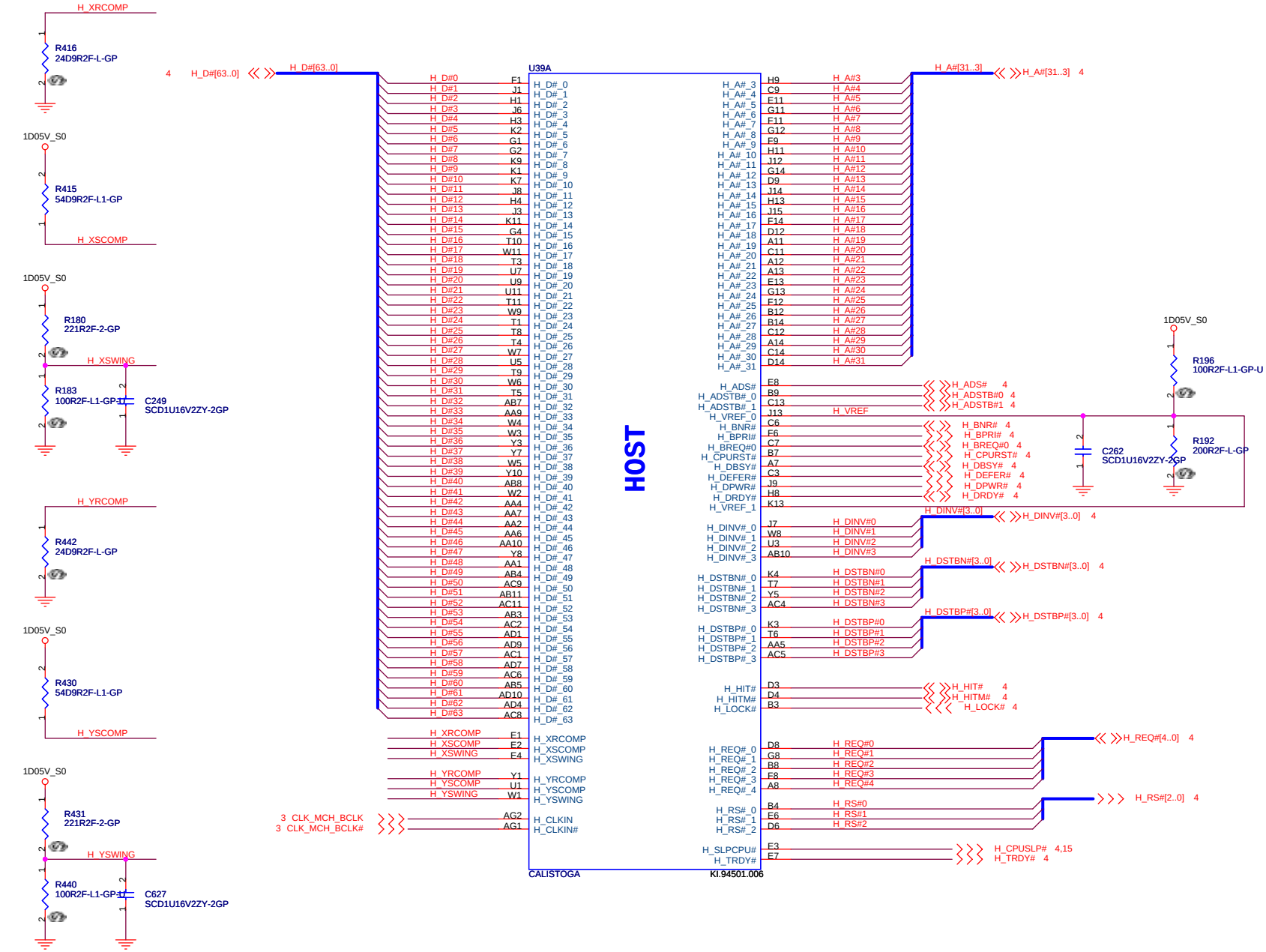
Size	
Document Number	MYALL2
Rev	MP
Date	Thursday, March 30, 2006
Sheet	5 of 57



Place them near to the chip (< 0.5")

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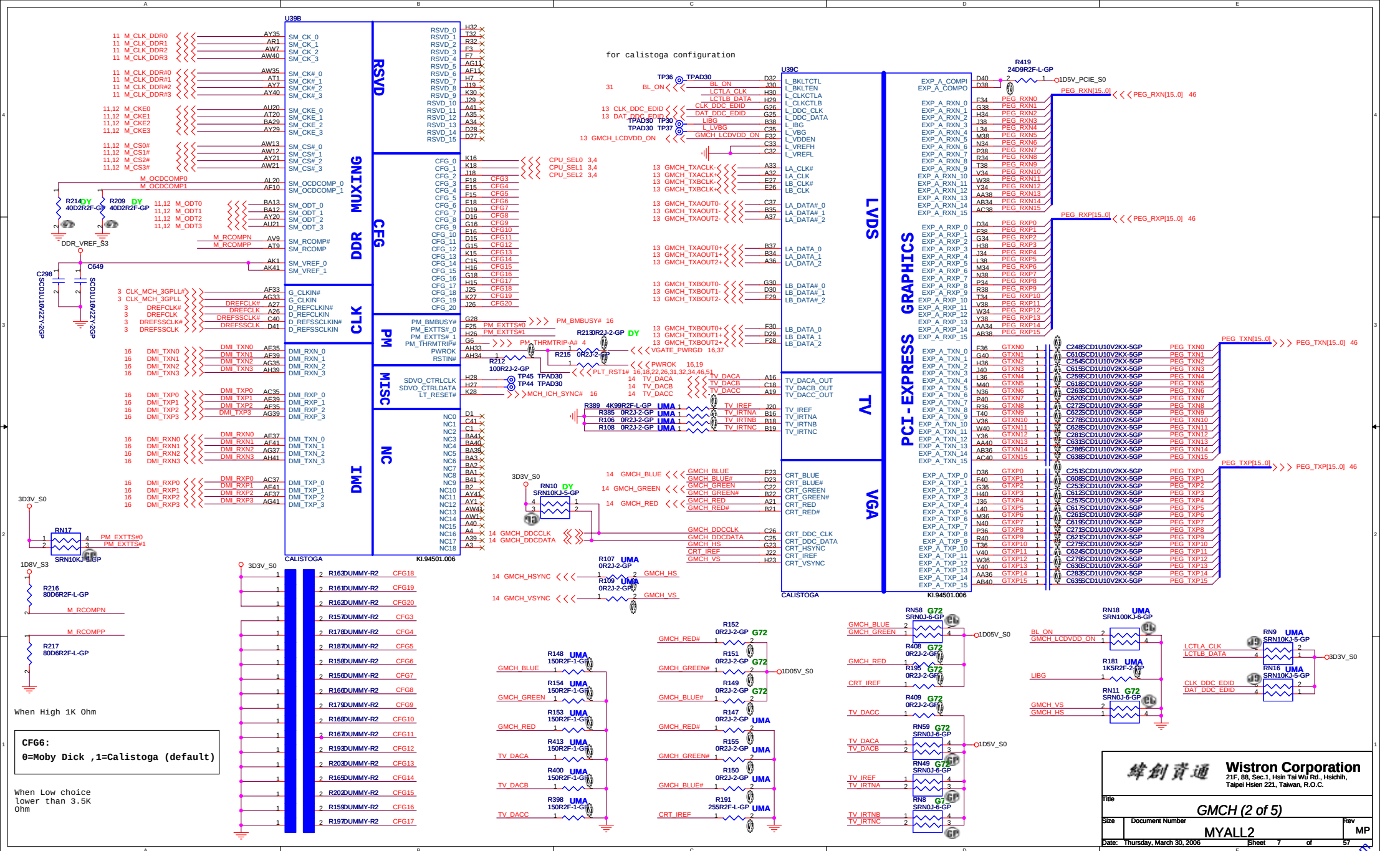
U39B
RSVD
CFG
MUXING
DDR
CLK
PM
MISC
NC
DMI
CALISTOGA
KI.94501.006
for calistoga configuration
U39C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA
KI.94501.006
When High 1K Ohm
CFG6:
0=Moby Dick ,1=Calistoga (default)
When Low choice
lower than 3.5K
Ohm
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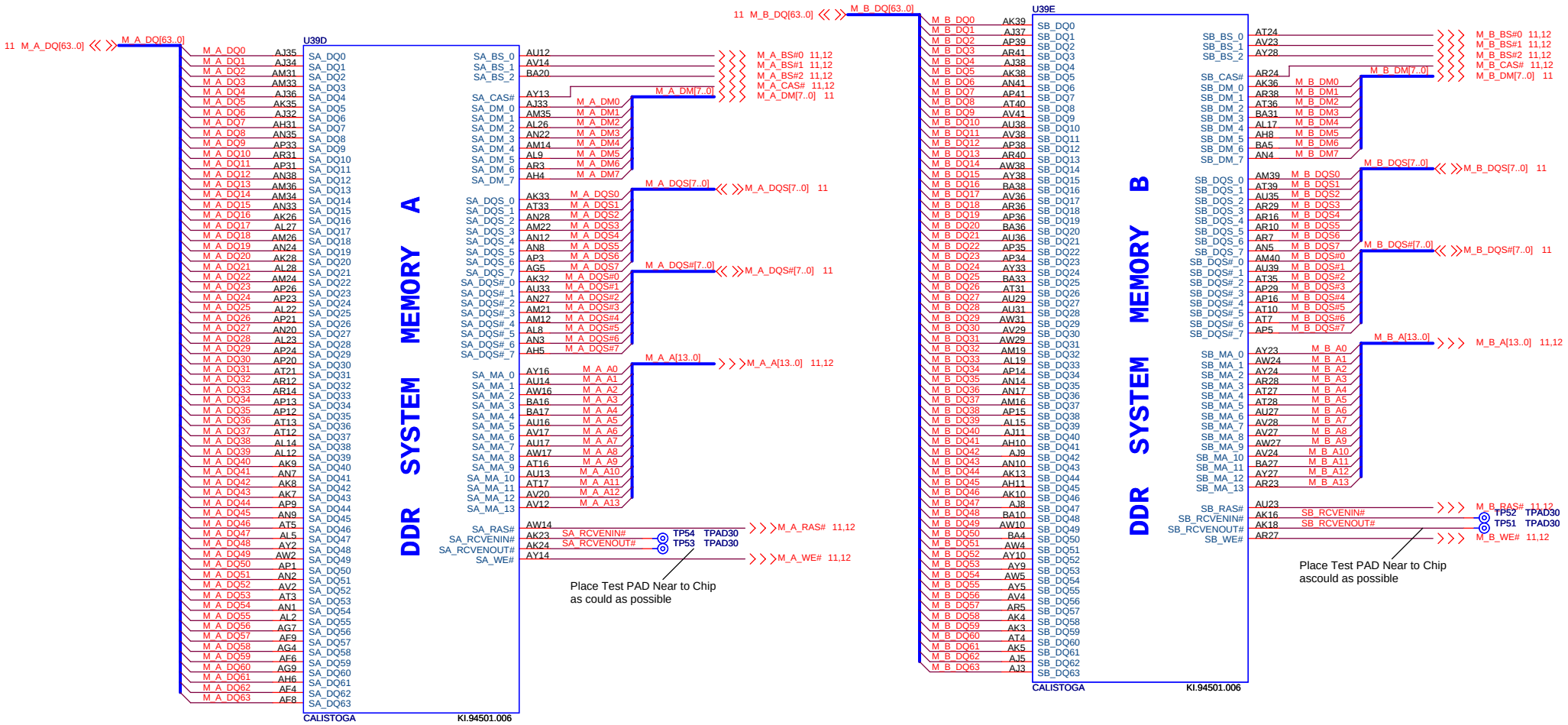
hexainf@hotmail.com



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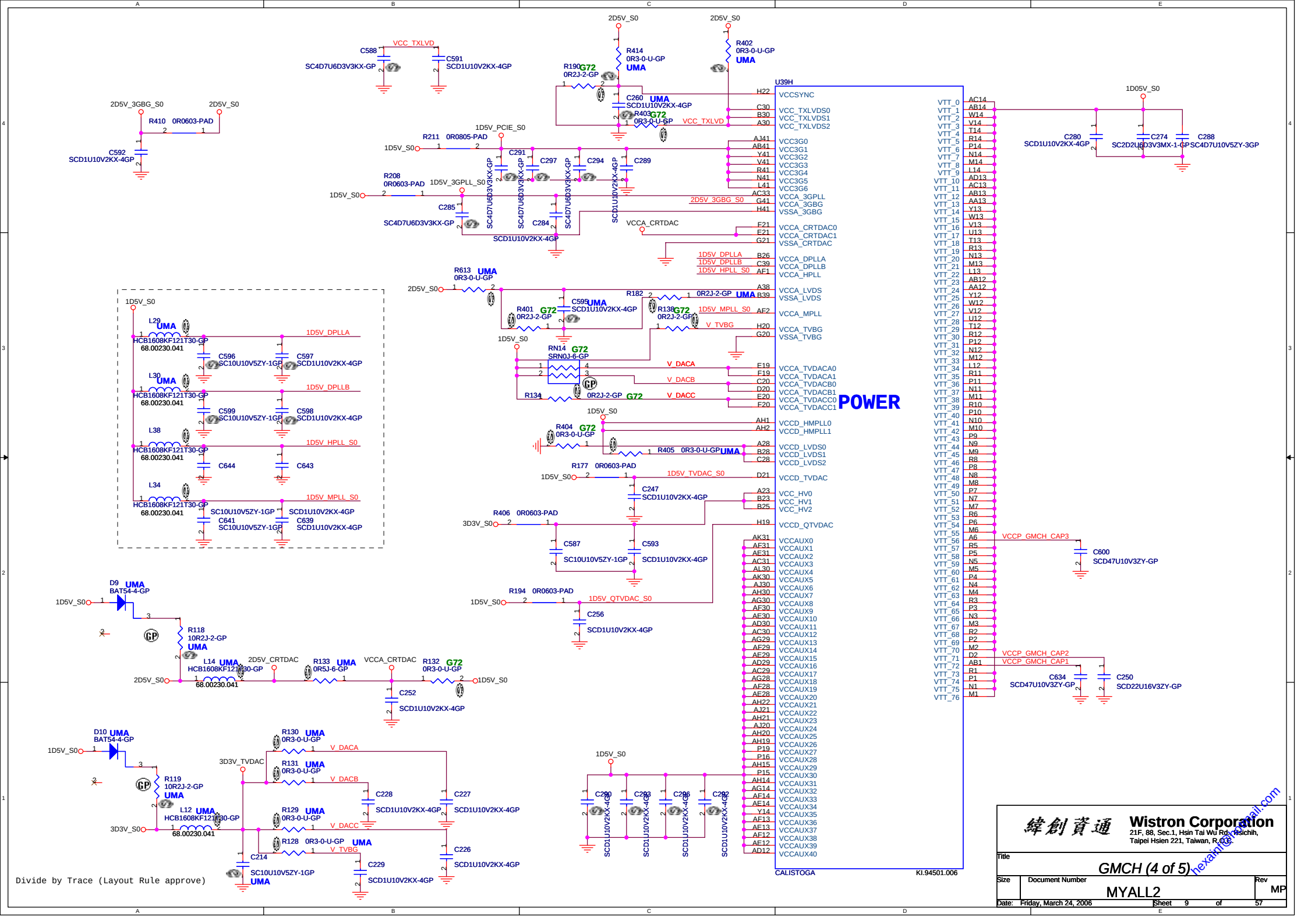
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U39H
CALISTOGA
KI.94501.006
Divide by Trace (Layout Rule approve)
Wistron Corporation
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Title
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Size
Document Number
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Rev
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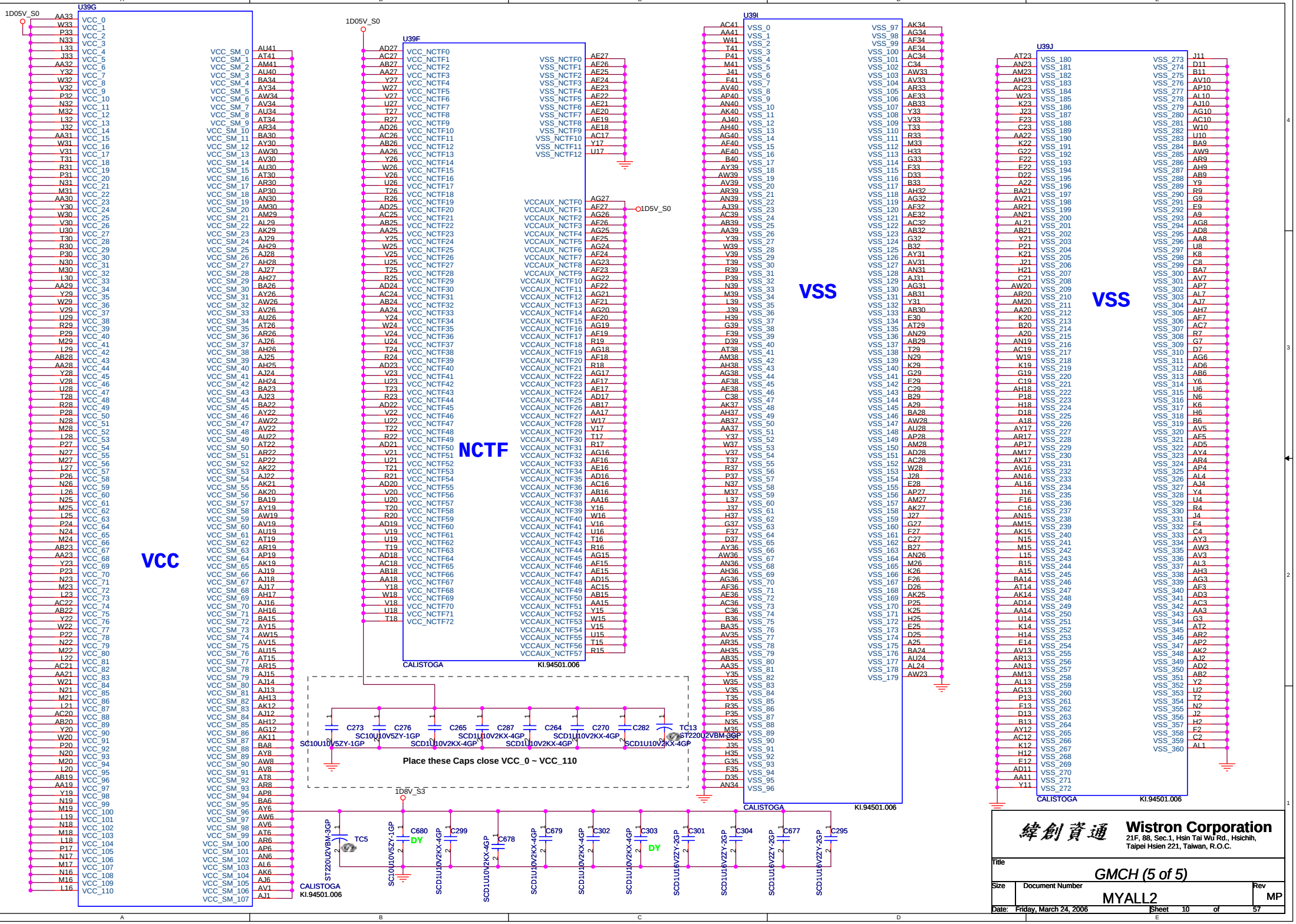
Date: Friday, March 24, 2006
Sheet 9 of 57



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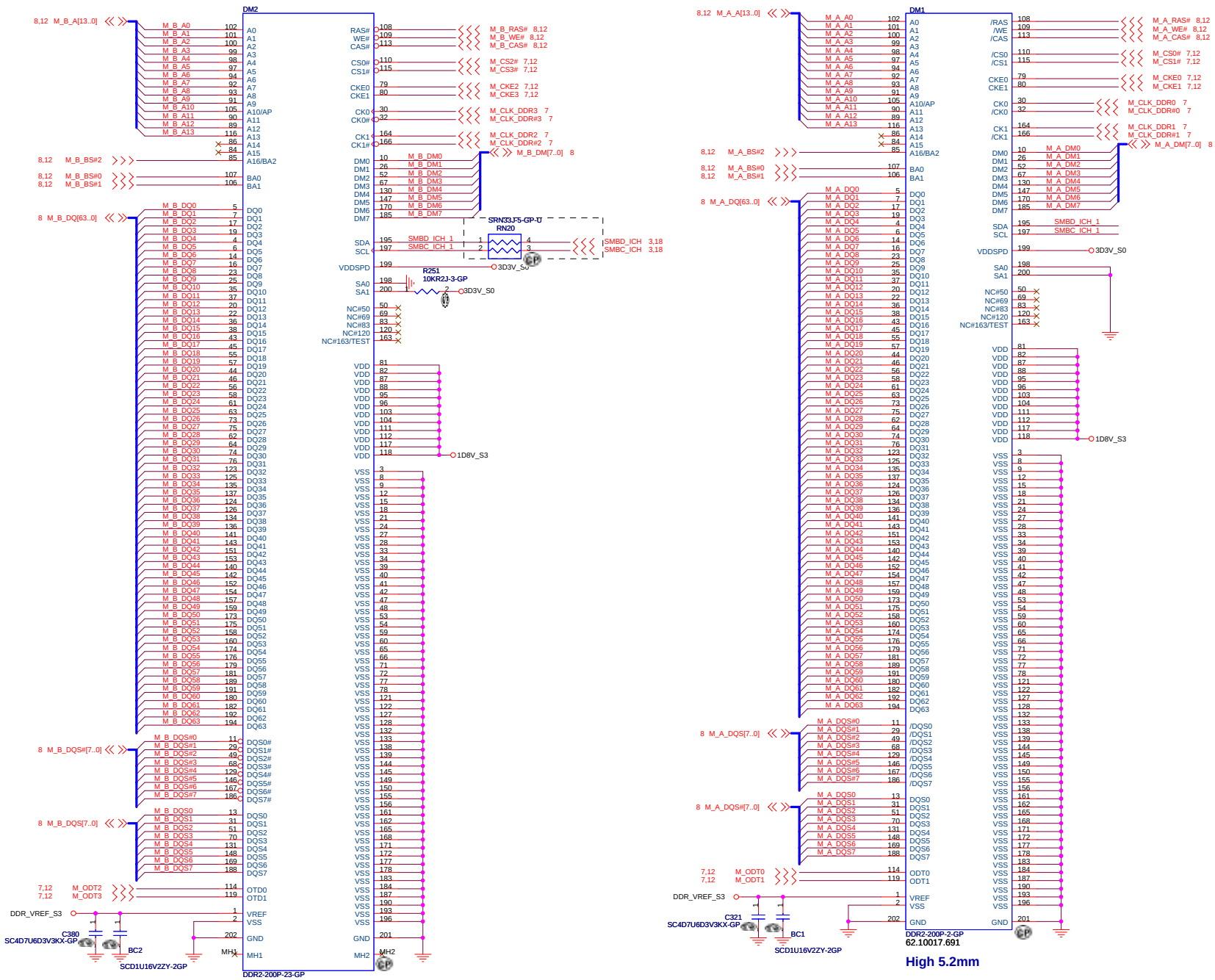
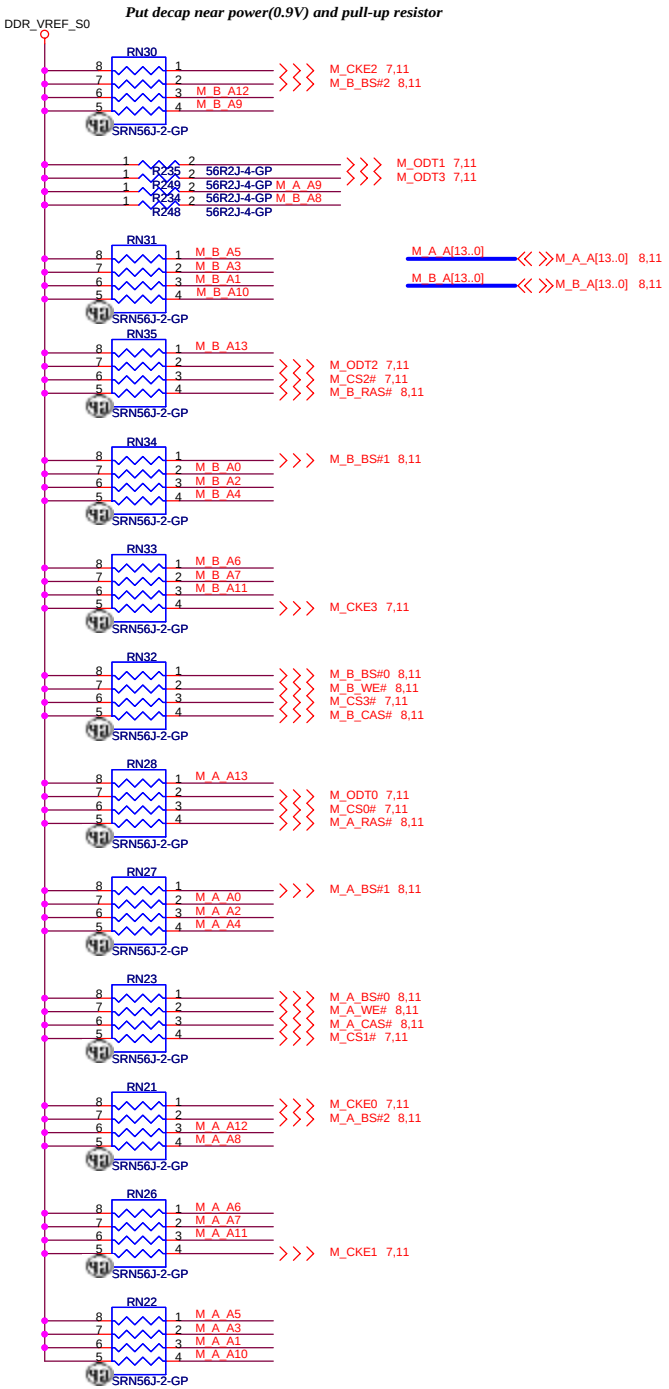
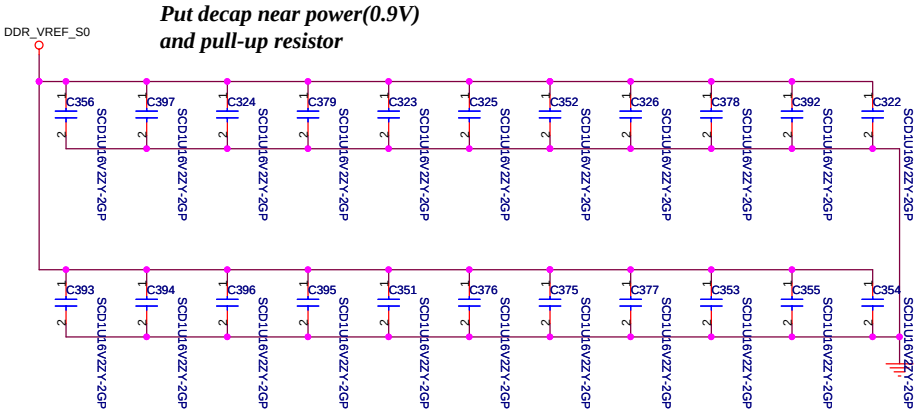


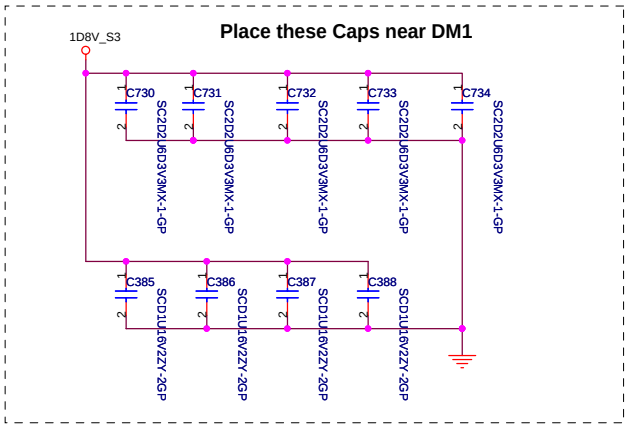
Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DDR2 Socket	
Size	Document Number MYALL2	Rev MP
Date: Thursday, March 30, 2006	Sheet 11 of 57	

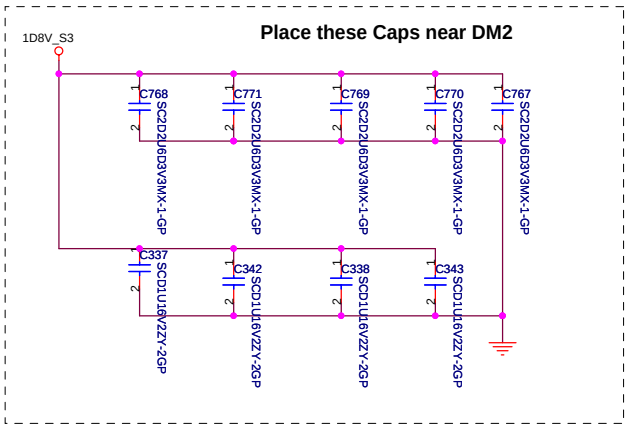
PARALLEL TERMINATION



Decoupling Capacitor







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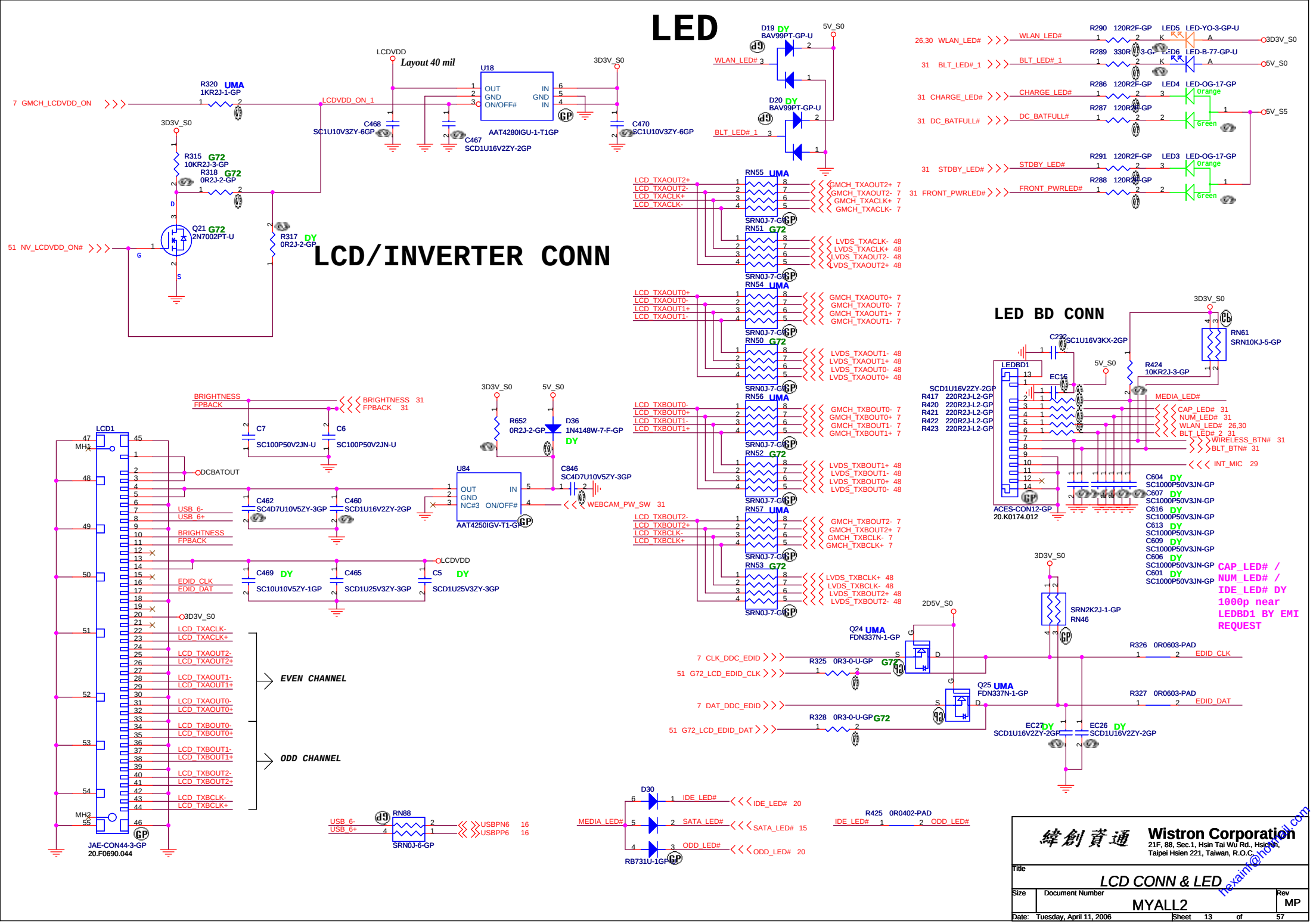
Title	*DDR2 Termination Resistor*	
Size	Document Number: MYALL2	Rev: MP
Date: Thursday, March 30, 2006	Sheet 12 of 57	

LED

LCD/INVERTER CONN

LED BD CONN



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD CONN & LED	
Size	Document Number	Rev
	MYALL2	MP
Date: Tuesday, April 11, 2006	Sheet 13 of 57	

CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

47 CRT_RED — R375 G72 0R2J-2-GP
7 GMCH_RED — R376 UMA 0R2J-2-GP
47 CRT_GREEN — R373 G72 0R2J-2-GP
7 GMCH_GREEN — R374 UMA 0R2J-2-GP
47 CRT_BLUE — R371 G72 0R2J-2-GP
7 GMCH_BLUE — R372 UMA 0R2J-2-GP

RED — L22 FCB1608CF-GP — CRT_R
GREEN — L23 FCB1608CF-GP — CRT_G
BLUE — L24 FCB1608CF-GP — CRT_B

R294 150R2F-1-GP R295 150R2F-1-GP R296 150R2F-1-GP
C457 C452 C453 SC8P50V2CN-1-GP DY
C446 C447 C448 SC3P50V2CN-1-GP

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT1 VIDEO-15-21-U3-GP 20.20334.015
MH1 MH2
CRT_R CRT_G CRT_B
DAT_DDC1_5 CRT_HSYNC1 CRT_VSYNC1 CLK_DDC1_5 5V_CRT_S0
C441 SC100P50V2JN-3GP
C439 SC18P50V2JN-1-GP
C440 SCD01U16V2KX-3GP
C442 SC100P50V2JN-3GP
C438 SC18P50V2JN-1-GP

5V_S0
R646 10KR2J-3-GP
R648 0R2J-GP
31 CRT_DEC
R647 0R2J-GP DY

Hsync & Vsync level shift

5V_S0
C459 SCD1U16V2ZY-2GP
7 GMCH_HSYNC — R306 UMA 0R2J-2-GP
R308 G72 0R2J-2-GP
47 HSYNC — R313 UMA 0R2J-2-GP — HSYNC_4
7 GMCH_VSYNC — R311 G72 0R2J-2-GP
47 VSYNC — VSYNC_4
U16A TSAHCT125PW-GP → CRT_HSYNC1
U16B TSAHCT125PW-GP → CRT_VSYNC1

DDC_CLK & DATA level shift

2D5V_S0 3D3V_S0
RN43 UMA SRN2K2J-1-GP
SRN2K2J-1-GP RN44 G72
R298 0R2J-2-GP UMA
R299 0R2J-2-GP G72
D24 CH751H-40PT
RN41 SRN10KJ-5-GP
7 GMCH_DDCDATA — R305 0R2J-2-GP UMA
47 G72_CRT_EDID_DAT — R297 0R2J-2-GP G72
47 G72_CRT_EDID_CLK — R303 0R2J-2-GP G72
7 GMCH_DDCCLK — R304 0R2J-2-GP UMA
Q19 FDN337N-1-GP
Q20 FDN337N-1-GP
DAT_DDC1_5
CLK_DDC1_5

TV CONN

47 G72_TV_LUMA — R379 G72 0R2J-2-GP
7 TV_DACB — R380 UMA 0R2J-2-GP
DACB — R300 150R2F-1-GP TVOUT
C449 SC33P50V3JN-GP TVOUT
L19 IND-1D2UH-5-GP TVOUT
C454 SC150P-GP TVOUT
C443 SC270P50V2JN-2GP TVOUT
LUMA_1

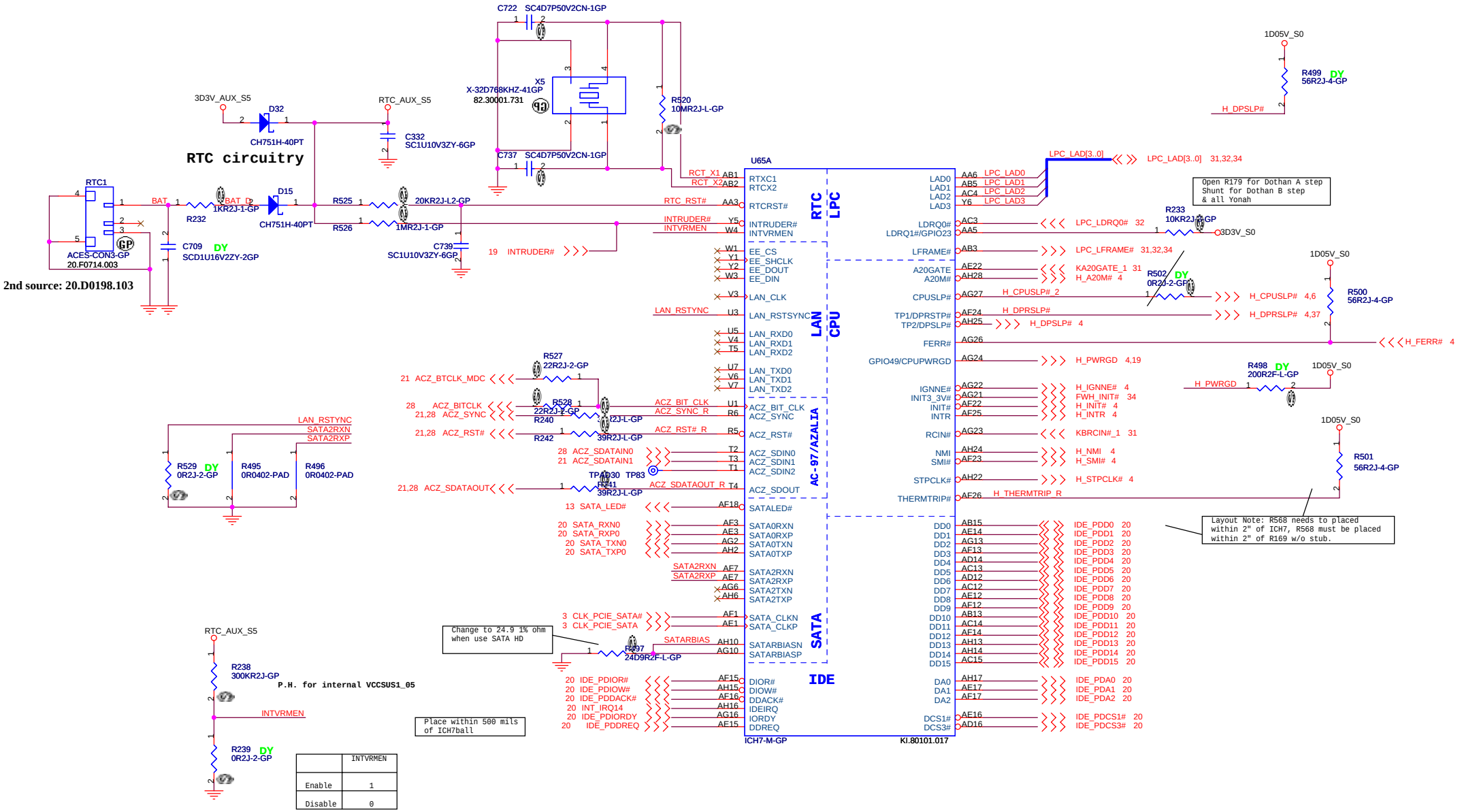
47 G72_TV_CRMA — R382 G72 0R2J-2-GP
7 TV_DACC — R383 UMA 0R2J-2-GP
DACC — R302 150R2F-1-GP TVOUT
C451 SC33P50V3JN-GP TVOUT
L21 IND-1D2UH-5-GP TVOUT
C456 SC150P-GP TVOUT
C445 SC270P50V2JN-2GP TVOUT
CRMA_1

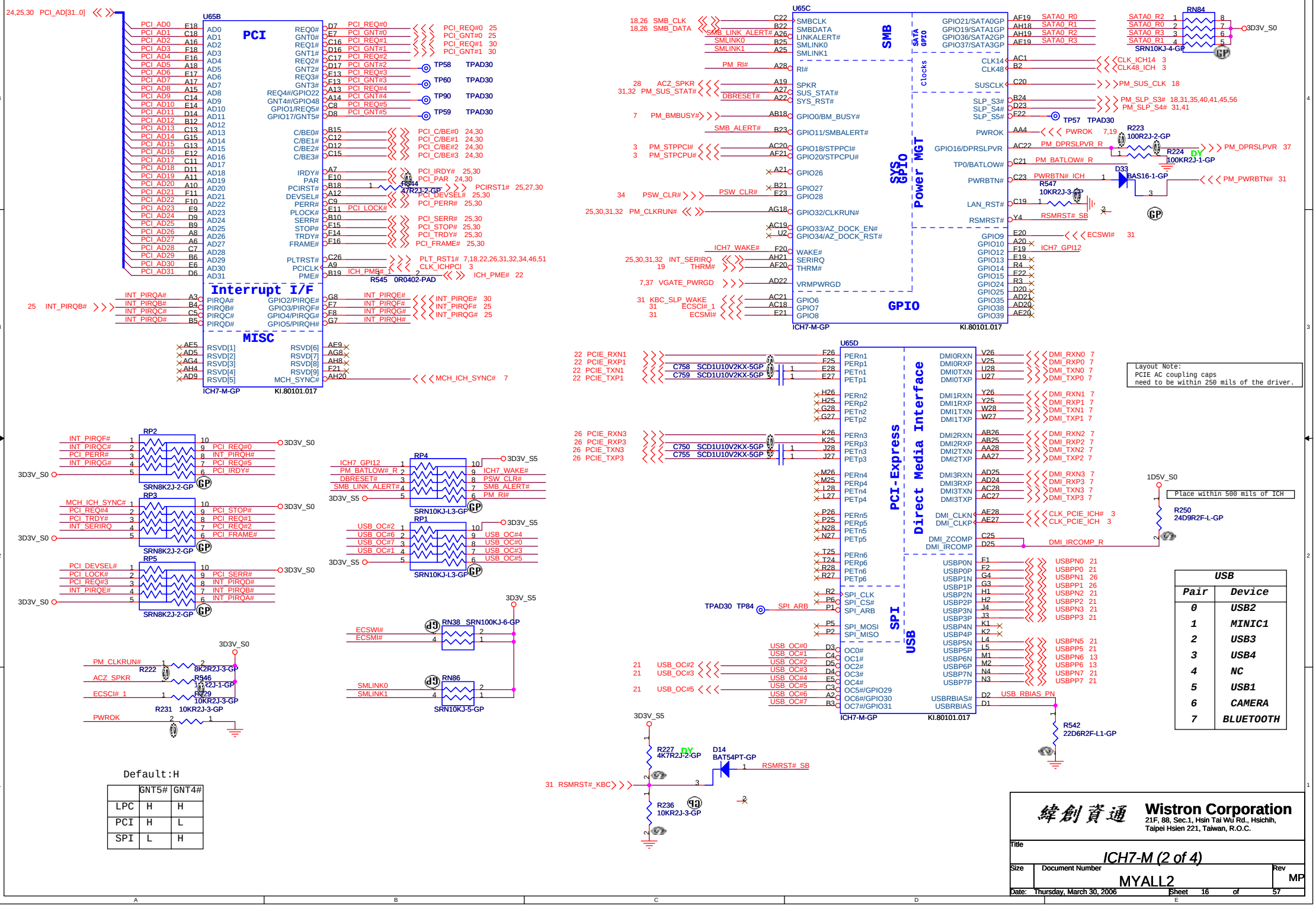
47 G72_TV_COMP — R377 G72 0R2J-2-GP
7 TV_DACA — R378 UMA 0R2J-2-GP
DACA — R301 150R2F-1-GP TVOUT
C450 SC33P50V3JN-GP TVOUT
L20 IND-1D2UH-5-GP TVOUT
C455 SC150P-GP TVOUT
C444 SC270P50V2JN-2GP TVOUT
COMP_1

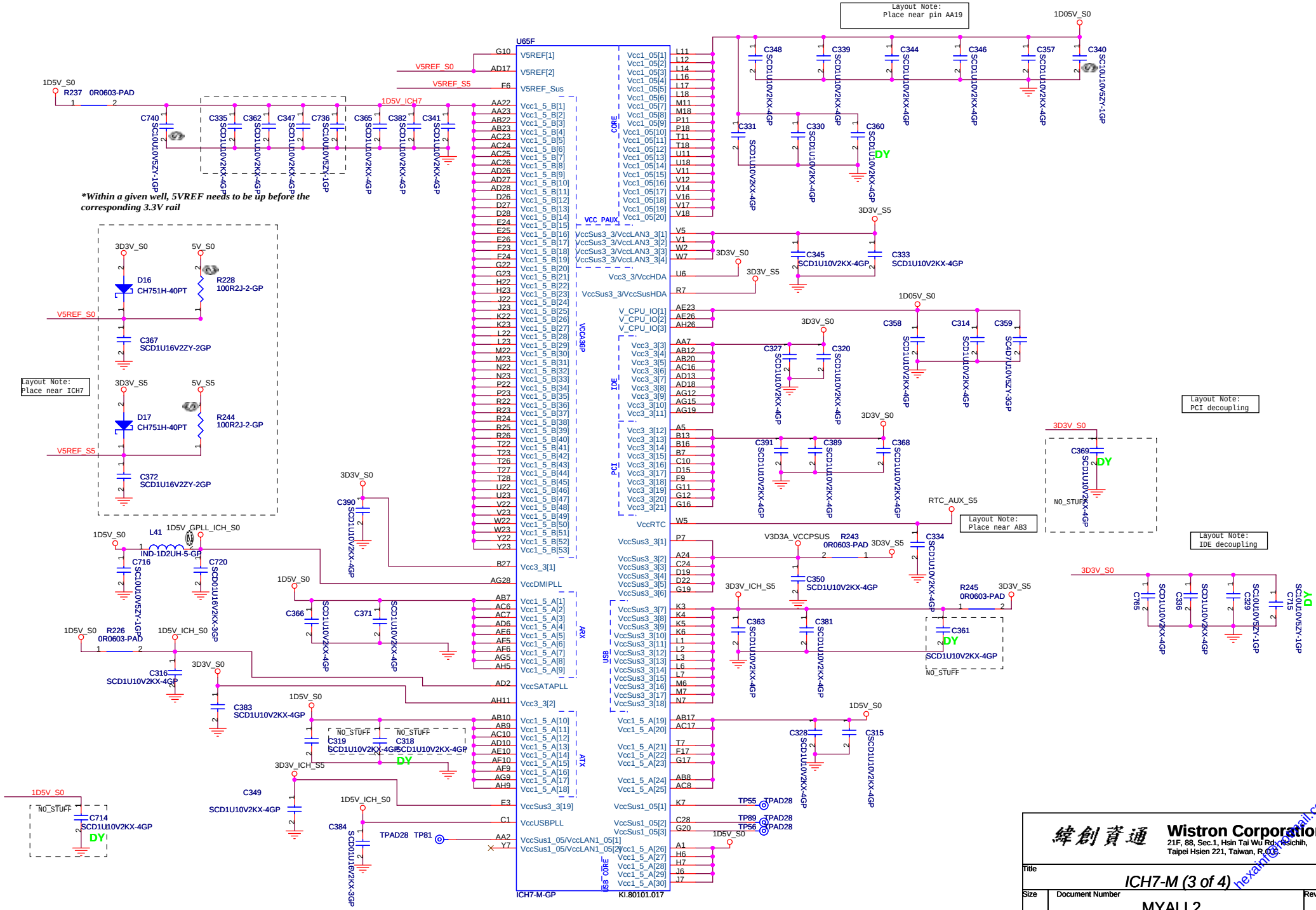
TVOUT1 MINDIN7-19-GP-U2 22.10021.H61 TVOUT
LUMA CRMA COMP NC#2 NC#5 GND GND GND GND

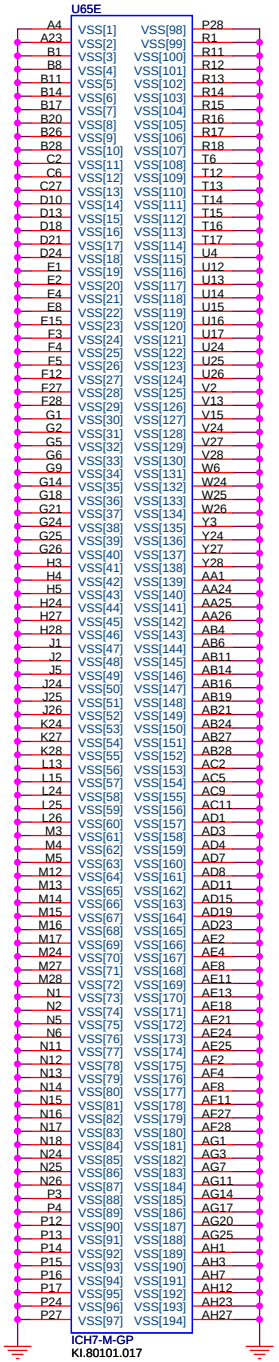
5V_S0
D1 BAV99PT-GP-U TVOUT — DACB
D3 BAV99PT-GP-U TVOUT — DACC
D2 BAV99PT-GP-U TVOUT — DACA
D21 BAV99PT-GP-U — CRT_R
D22 BAV99PT-GP-U — CRT_G
D23 BAV99PT-GP-U — CRT_B

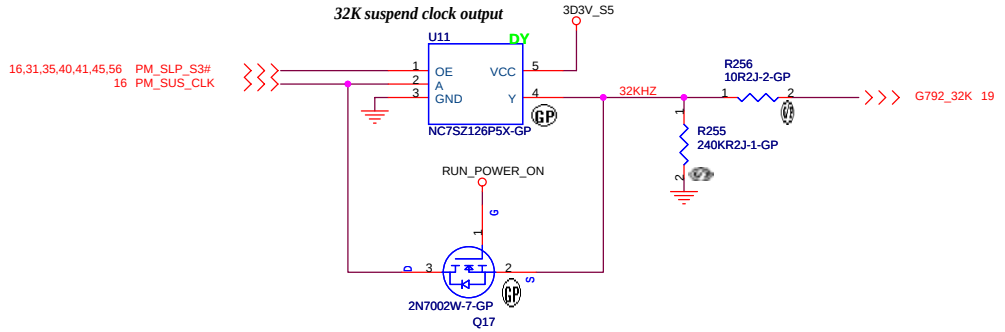
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CRT/TV Connector	
Size	Document Number MYALL2	Rev MP
Date: Thursday, March 30, 2006	Sheet 14 of 57	

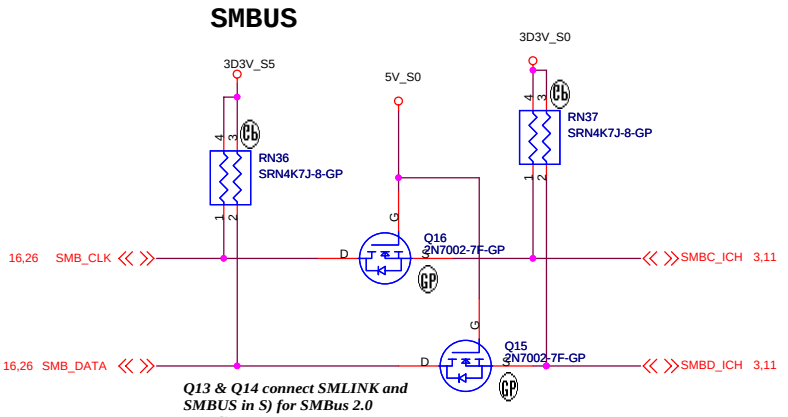

RTC circuitry
2nd source: 20.D0198.103
U65A
ICH7-M-GP
KI.80101.017
RTC
LPC
CPU
LAN
AC-97/AZALIA
SATA
IDE
Change to 24.9 1% ohm when use SATA HD
Place within 500 mils of ICH7ball
P.H. for internal VCCSUS1_05
Layout Note: R568 needs to placed within 2" of ICH7, R568 must be placed within 2" of R169 w/o stub.
Open R179 for Dothan A step Shunt for Dothan B step & all Yonah
Placement Note:
Diatance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.
INTVRMEN
Enable 1
Disable 0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (1 of 4)
Size
Document Number
MYALL2
Rev
MP
Date: Thursday, March 30, 2006
Sheet 15 of 57

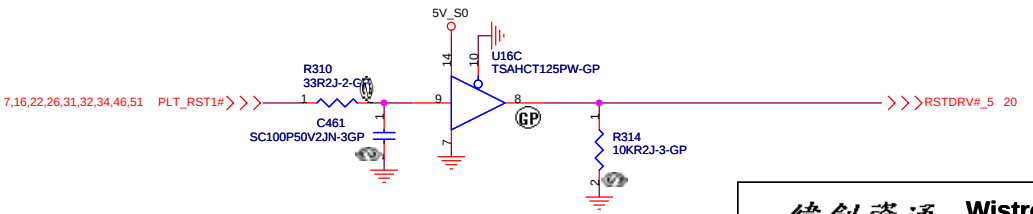

U65B
PCI
Interrupt I/F
MISC
ICH7-M-GP
KI.80101.017
U65C
SMB
GPIO
Power MGT
SYS
Clocks
SATA GPIO
U65D
PCI-Express
Direct Media Interface
SPI
USB
Default:H
GNT5#
GNT4#
LPC
PCI
SPI
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
USB
Pair
Device
0 USB2
1 MINIC1
2 USB3
3 USB4
4 NC
5 USB1
6 CAMERA
7 BLUETOOTH
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (2 of 4)
Size
Document Number
MYALL2
Rev
MP
Date: Thursday, March 30, 2006
Sheet 16 of 57


U65F
ICH7-M-GP
KI.80101.017
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near pin AA19
Layout Note: Place near ICH7
Layout Note: Place near AB3
Layout Note: PCI decoupling
Layout Note: IDE decoupling
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size
Document Number
MYALL2
Rev
MP
Date: Friday, March 24, 2006
Sheet 17 of 57



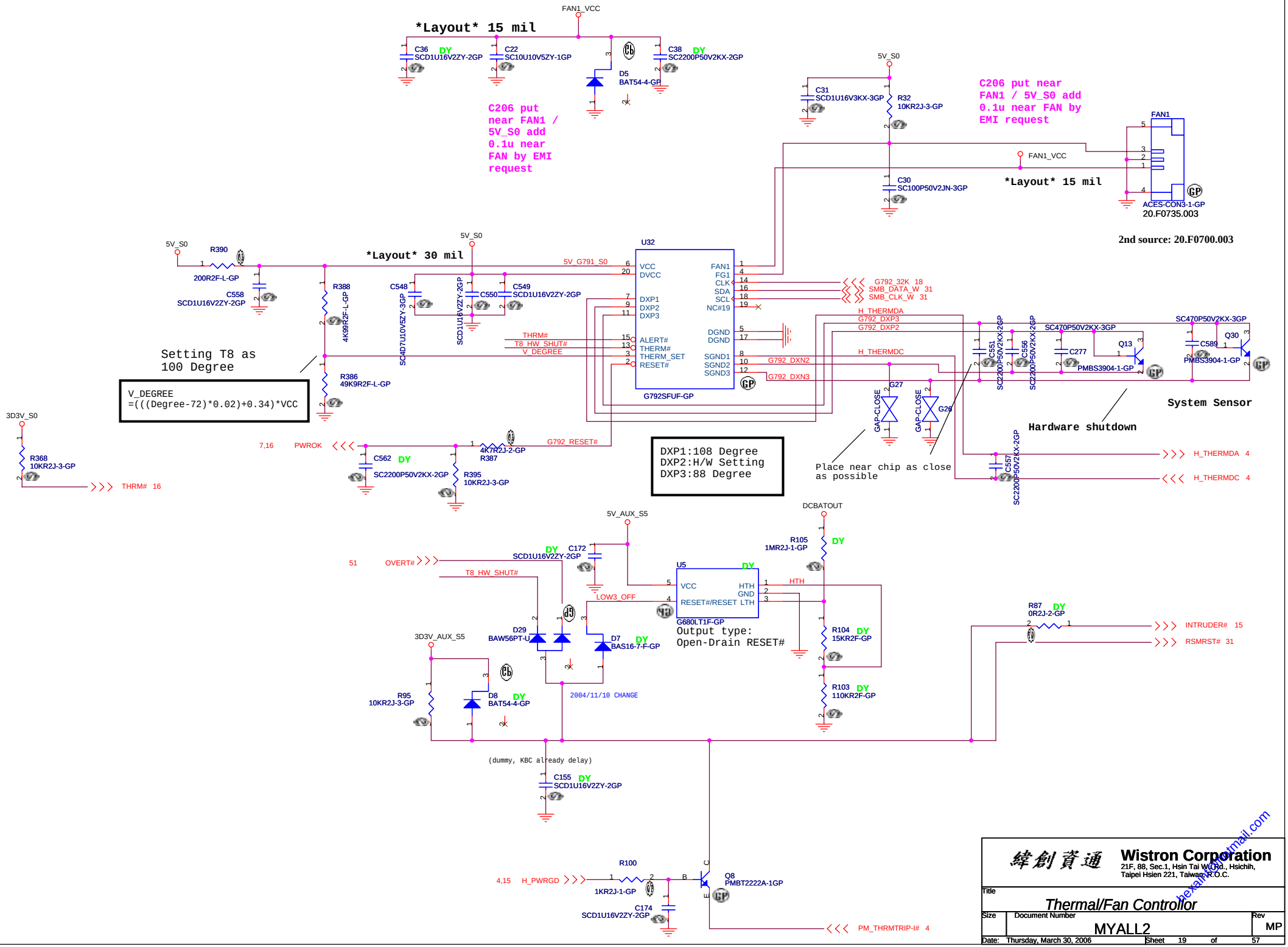




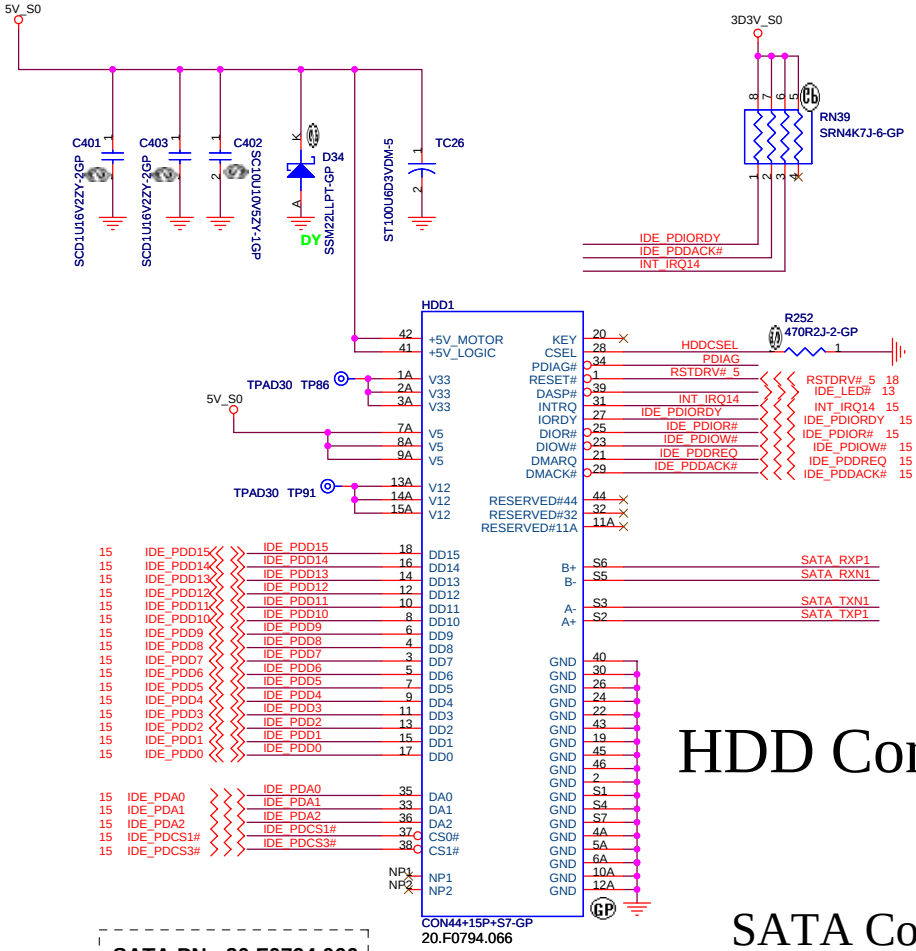


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*ICH7-M (4 of 4)*	
Size	Document Number: MYALL2	Rev: MP
Date: Thursday, March 30, 2006	Sheet 18 of 57	

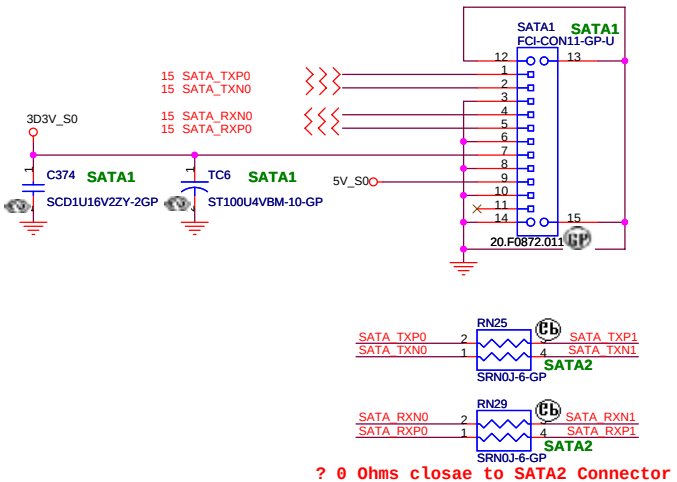

Layout 15 mil
FAN1_VCC
C36 DY SCD1U16V2ZY-2GP
C22 SC10U10V5ZY-1GP
C38 DY SC2200P50V2KX-2GP
D5 BAT54-4-GP
C206 put near FAN1 / 5V_S0 add 0.1u near FAN by EMI request
5V_S0
C31 SCD1U16V3KX-3GP
R32 10KR2J-3-GP
C206 put near FAN1 / 5V_S0 add 0.1u near FAN by EMI request
FAN1
FAN1_VCC
Layout 15 mil
C30 SC100P50V2JN-3GP
ACES-CON3-1-GP
20.F0735.003
2nd source: 20.F0700.003
5V_S0
R390 200R2F-L-GP
C558 SCD1U16V2ZY-2GP
Layout 30 mil
5V_S0
5V_G791_S0
R388 4K99R2F-L-GP
C548 SC4D7U10V5ZY-3GP
C550 SCD1U16V2ZY-2GP
C549 SCD1U16V2ZY-2GP
U32
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792SFUF-GP
G792_32K 18
SMB_DATA_W 31
SMB_CLK_W 31
H_THERMDA
G792_DXP3
G792_DXP2
H_THERMDC
G792_DXN2
G792_DXN3
THRM#
T8_HW_SHUT#
V_DEGREE
Setting T8 as 100 Degree
V_DEGREE =(((Degree-72)*0.02)+0.34)*VCC
R386 49K9R2F-L-GP
3D3V_S0
R368 10KR2J-3-GP
THRM# 16
7,16 PWROK
C562 DY SC2200P50V2KX-2GP
4K7R2J-2-GP R387
R395 10KR2J-3-GP
G792_RESET#
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
G27
G26
GAP-CLOSE
GAP-CLOSE
C551 SC2200P50V2KX-2GP
C556 SC2200P50V2KX-2GP
C557 SC2200P50V2KX-2GP
SC470P50V2KX-3GP
C277
PMBS3904-1-GP
Q13
SC470P50V2KX-3GP
C589
PMBS3904-1-GP
Q30
System Sensor
Hardware shutdown
H_THERMDA 4
H_THERMDC 4
5V_AUX_S5
DCBATOUT
C172 DY SCD1U16V2ZY-2GP
51 OVERT#
T8_HW_SHUT#
LOW3_OFF
U5 DY
VCC
RESET#/RESET
HTH
GND
LTH
G680LT1F-GP
Output type:
Open-Drain RESET#
R105 1MR2J-1-GP DY
HTH
R104 DY 15KR2F-GP
R103 DY 110KR2F-GP
D29 BAW56PT-U
D7 DY BAS16-7-F-GP
3D3V_AUX_S5
R95 10KR2J-3-GP
D8 DY BAT54-4-GP
2004/11/10 CHANGE
R87 DY 0R2J-2-GP
INTRUDER# 15
RSMRST# 31
(dummy, KBC already delay)
C155 DY SCD1U16V2ZY-2GP
R100
4,15 H_PWRGD
1KR2J-1-GP
Q8 PMBT2222A-1GP
C174 SCD1U16V2ZY-2GP
PM_THRMTRIP-I# 4
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Document Number
MYALL2
Rev
MP
Date: Thursday, March 30, 2006
Sheet 19 of 57

HDD Connector



SATA PN : 20.F0794.066
PATA PN : 20.E0021.222

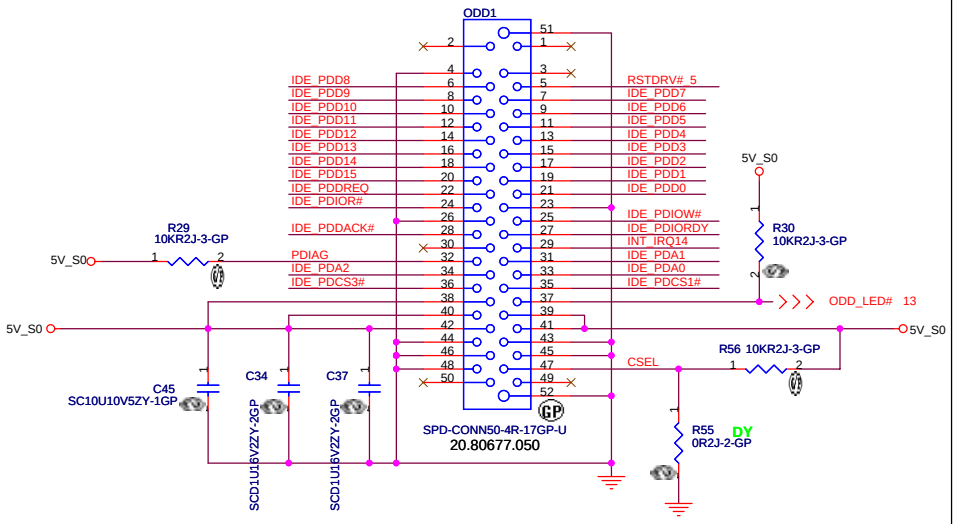
SATA Connector



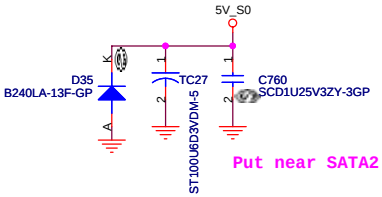
? 0 Ohms closae to SATA2 Connector

Dummy when use IDE

CD-ROM Connector



For HDD & SATA both

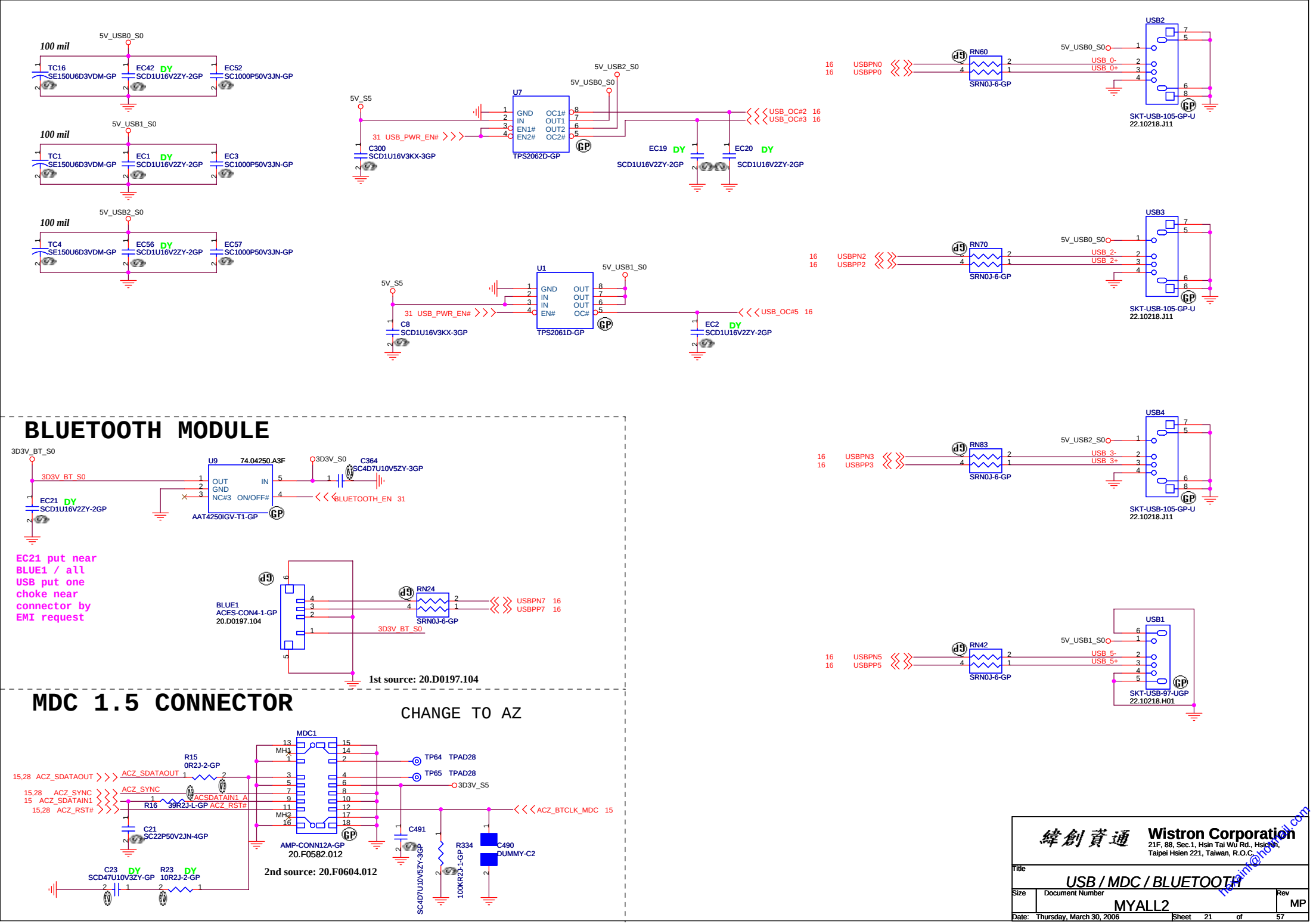


Put near SATA2 Connector

ME : 20.F0777.022

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
HDD and CDROM			
Size	Document Number		Rev
	MYALL2		MP
Date: Thursday, March 30, 2006	Sheet 20 of 57		



BLUETOOTH MODULE

EC21 put near BLUE1 / all USB put one choke near connector by EMI request

1st source: 20.D0197.104

MDC 1.5 CONNECTOR

CHANGE TO AZ

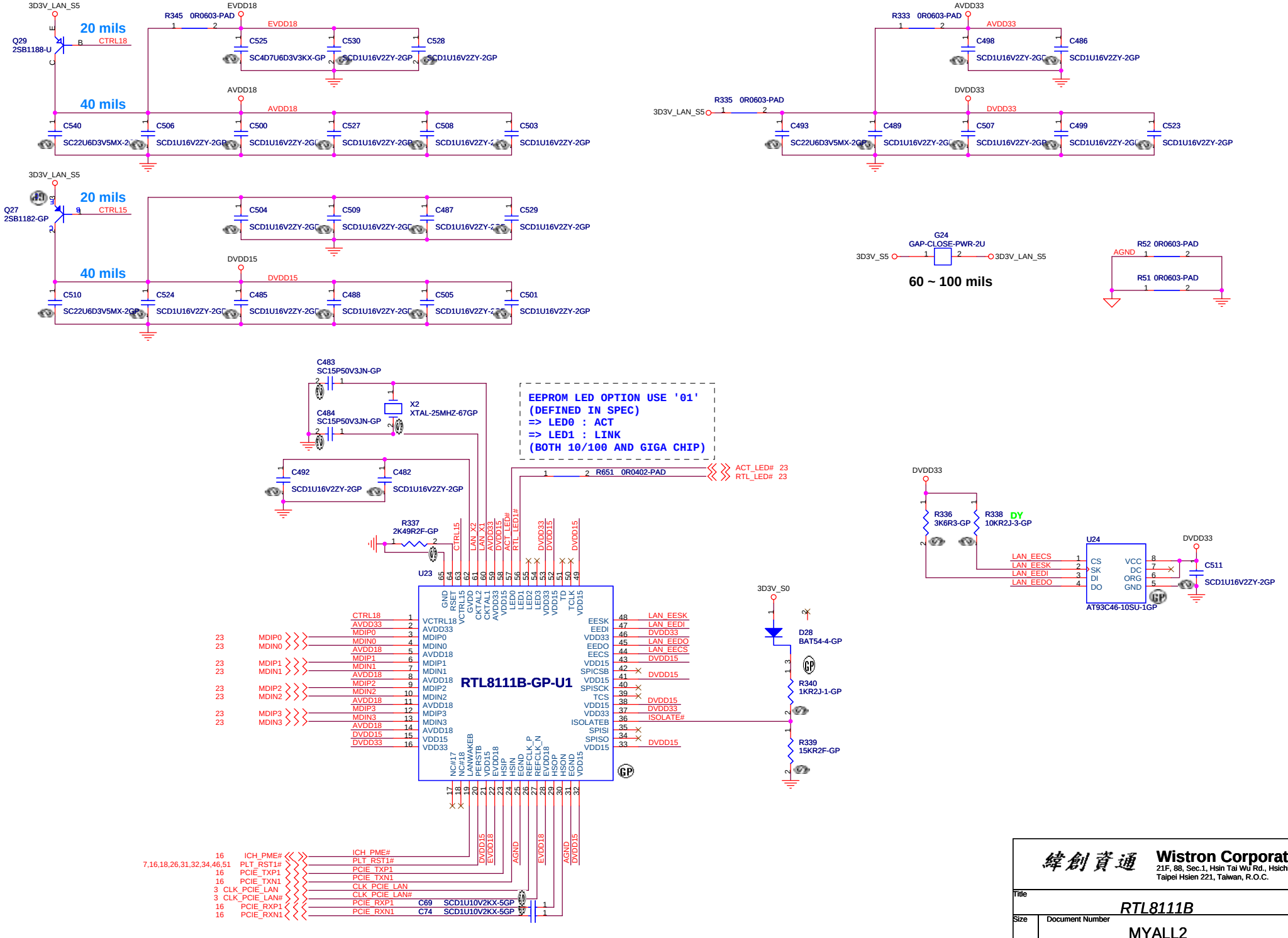
2nd source: 20.F0604.012

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
mainin@hotmail.com

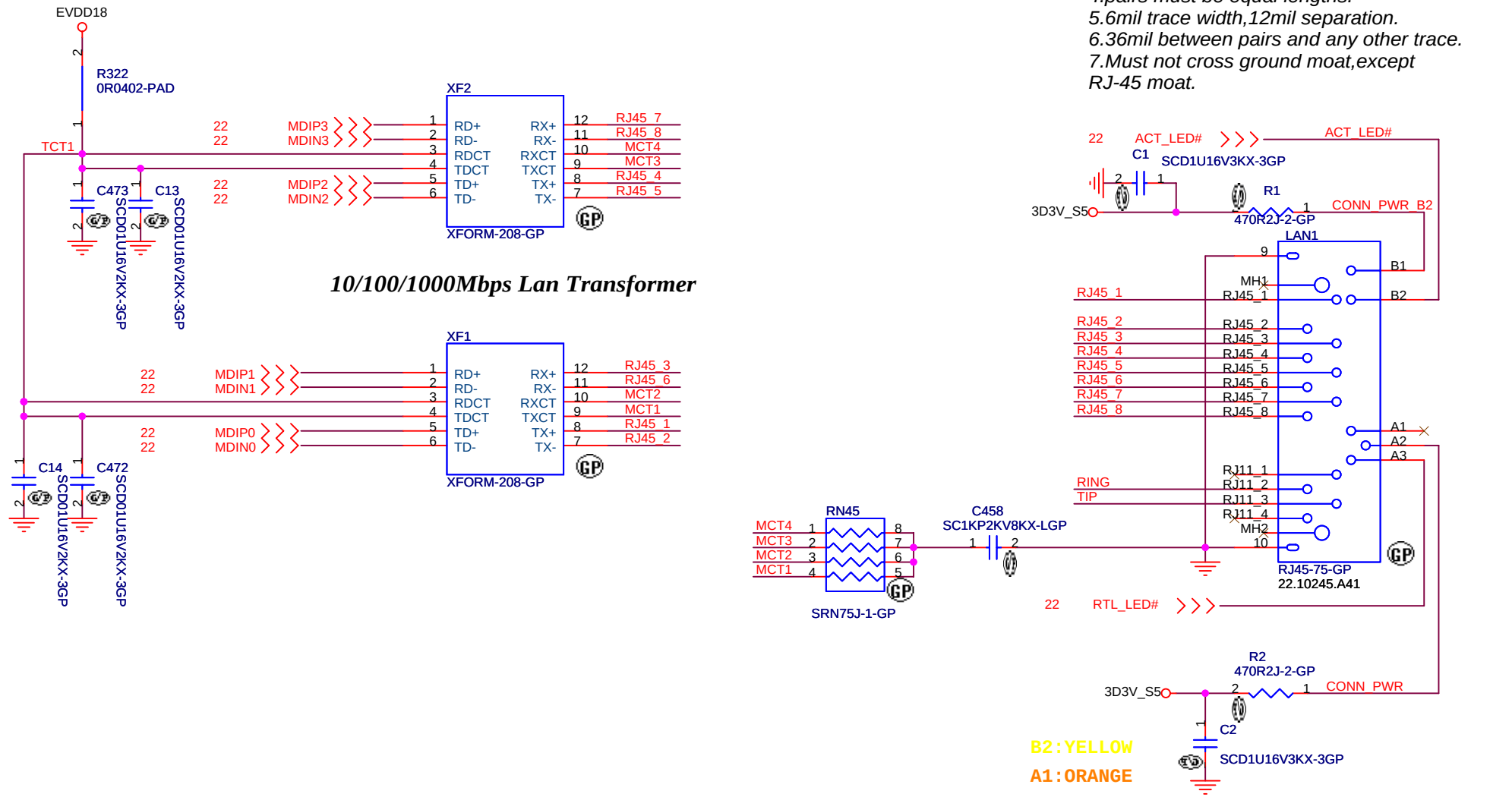
Title: USB / MDC / BLUETOOTH

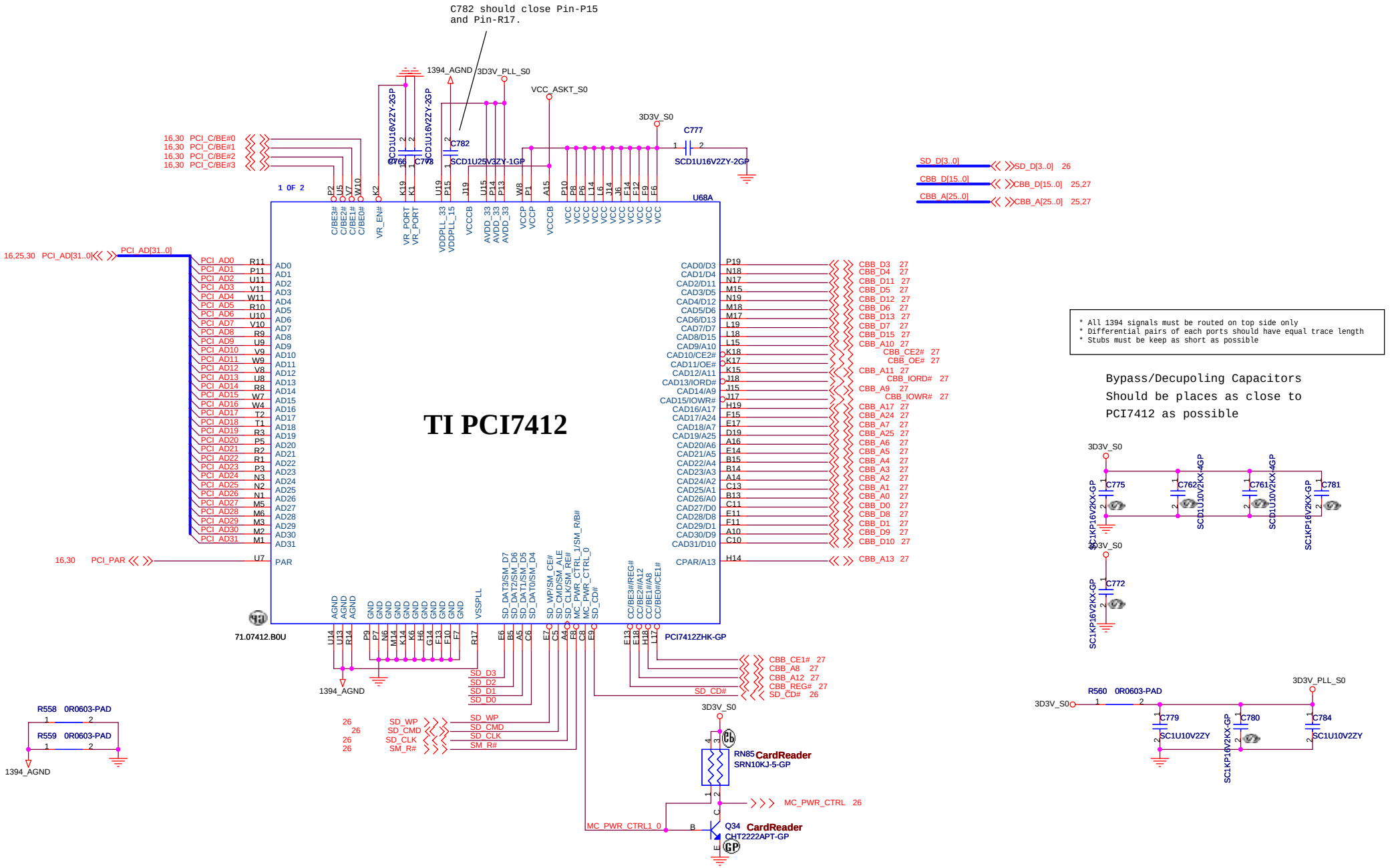
Size	Document Number	Rev
	MYALL2	MP

Date: Thursday, March 30, 2006 Sheet 21 of 57



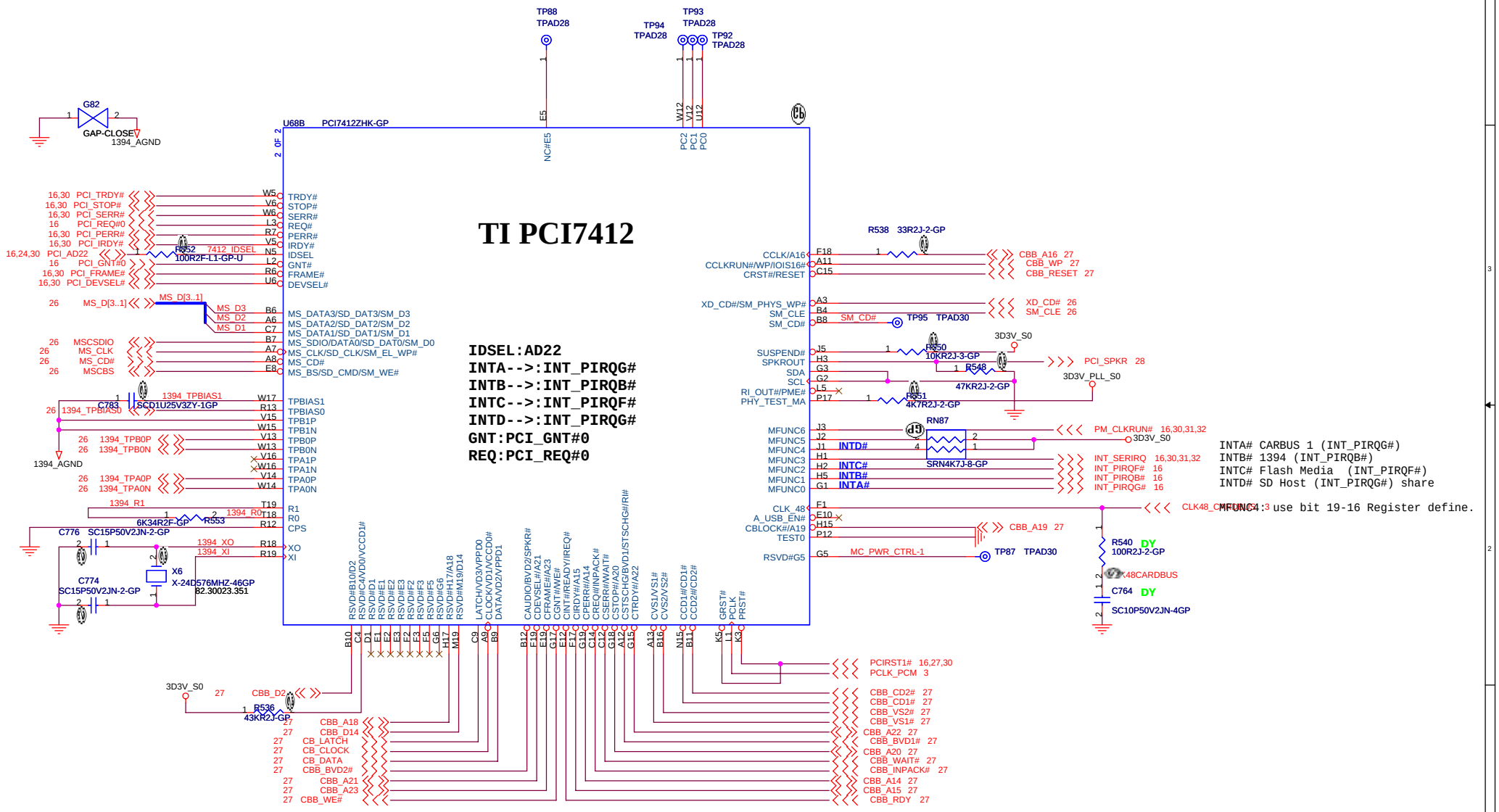
緯創資通	**Wistron Corporation**	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*RTL8111B*	
Size	Document Number: MYALL2	Rev: MP
Date: Thursday, March 30, 2006	Sheet 22 of 57	


1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.
EVDD18
R322
0R0402-PAD
TCT1
C473
SCD01U16V2KX-3GP
C13
SCD01U16V2KX-3GP
XF2
MDIP3
MDIN3
MDIP2
MDIN2
RD+
RD-
RDCT
TDCT
TD+
TD-
RX+
RX-
RXCT
TXCT
TX+
TX-
RJ45_7
RJ45_8
MCT4
MCT3
RJ45_4
RJ45_5
XFORM-208-GP
10/100/1000Mbps Lan Transformer
XF1
MDIP1
MDIN1
MDIP0
MDIN0
RJ45_3
RJ45_6
MCT2
MCT1
RJ45_1
RJ45_2
XFORM-208-GP
C14
SCD01U16V2KX-3GP
C472
SCD01U16V2KX-3GP
ACT_LED#
C1
SCD1U16V3KX-3GP
3D3V_S5
R1
470R2J-2-GP
CONN_PWR_B2
LAN1
RJ45_1
RJ45_2
RJ45_3
RJ45_4
RJ45_5
RJ45_6
RJ45_7
RJ45_8
MH1
MH2
B1
B2
A1
A2
A3
RING
TIP
RJ11_1
RJ11_2
RJ11_3
RJ11_4
RJ45-75-GP
22.10245.A41
RN45
MCT4
MCT3
MCT2
MCT1
SRN75J-1-GP
C458
SC1KP2KV8KX-LGP
RTL_LED#
R2
470R2J-2-GP
CONN_PWR
C2
SCD1U16V3KX-3GP
B2:YELLOW
A1:ORANGE
A3:GREEN
3D3V_S5 add 0.1u near LAN1 by EMI request
TIP1
TIP_MDC
RING_MDC
L1
L2
0R0603-PAD
TIP
RING
ACES-CON2-1-GP
20.D0197.102
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN CONN
Size
Document Number
MYALL2
Rev
MP
Date: Thursday, March 30, 2006
Sheet 23 of 57
hexainf@hotmail.com



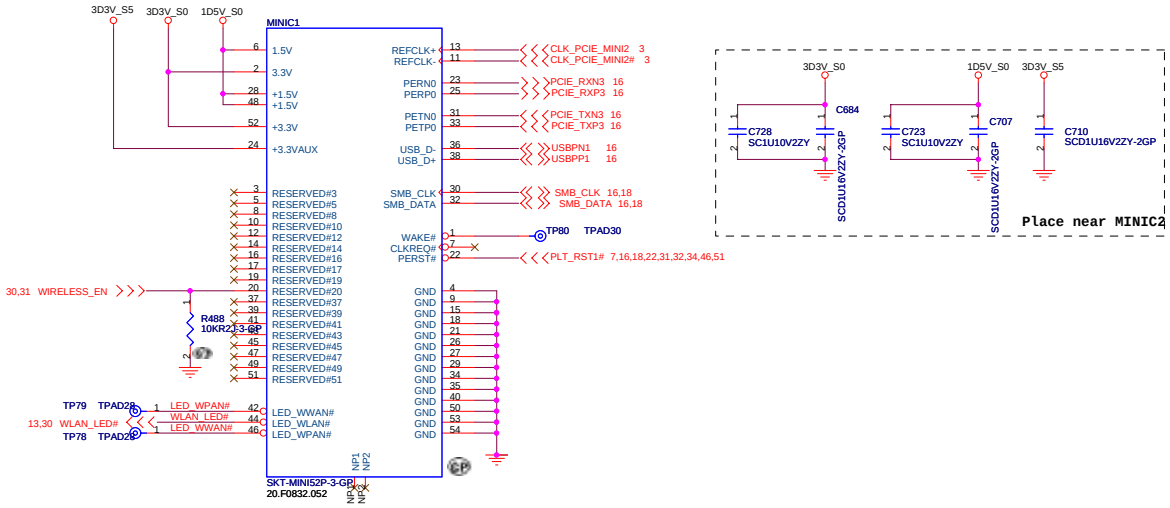
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*TI PCI7412 (1 of 2)*	
Size	Document Number: MYALL2	Rev: MP
Date: Thursday, March 30, 2006	Sheet 24 of 57	

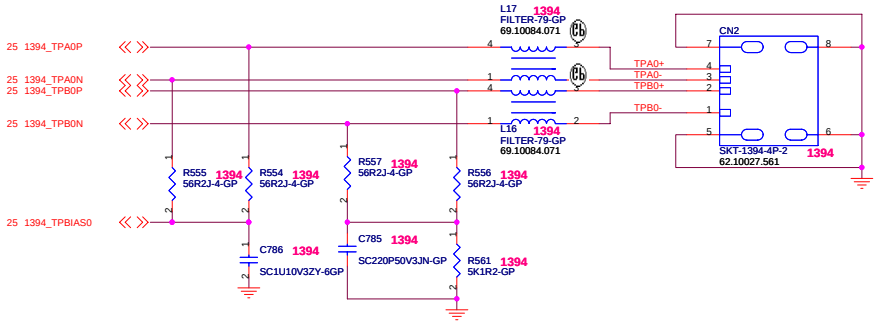


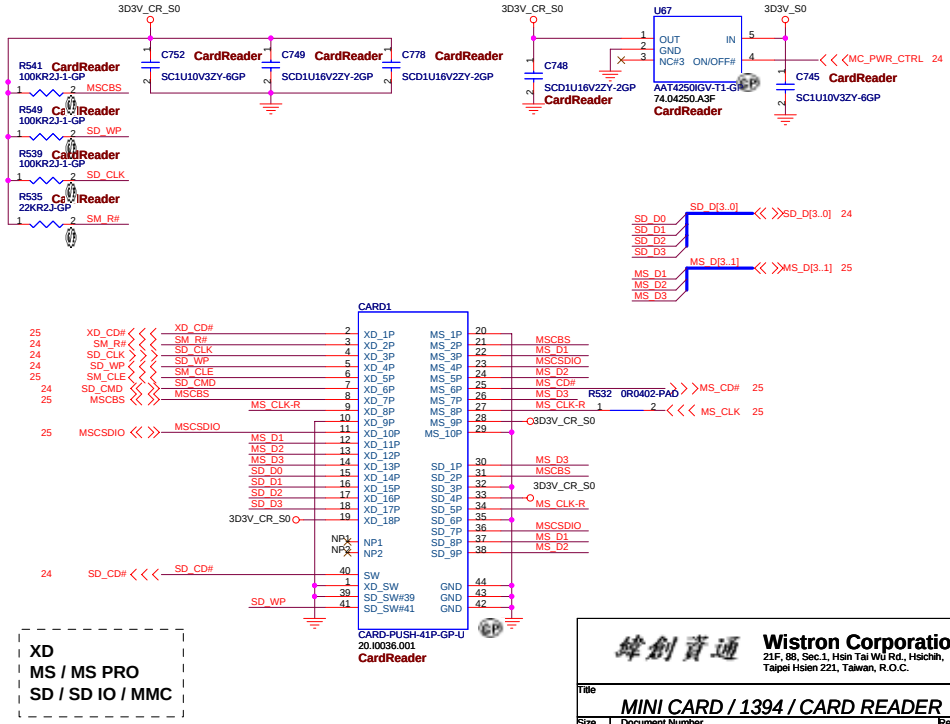
緯創資通	**Wistron Corporation**	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*TI PCI7412 (2 of 2)*	
Size	Document Number: MYALL2	Rev: MP
Date: Thursday, March 30, 2006	Sheet 25 of 57	

Mini Card Connector



1394 Connector

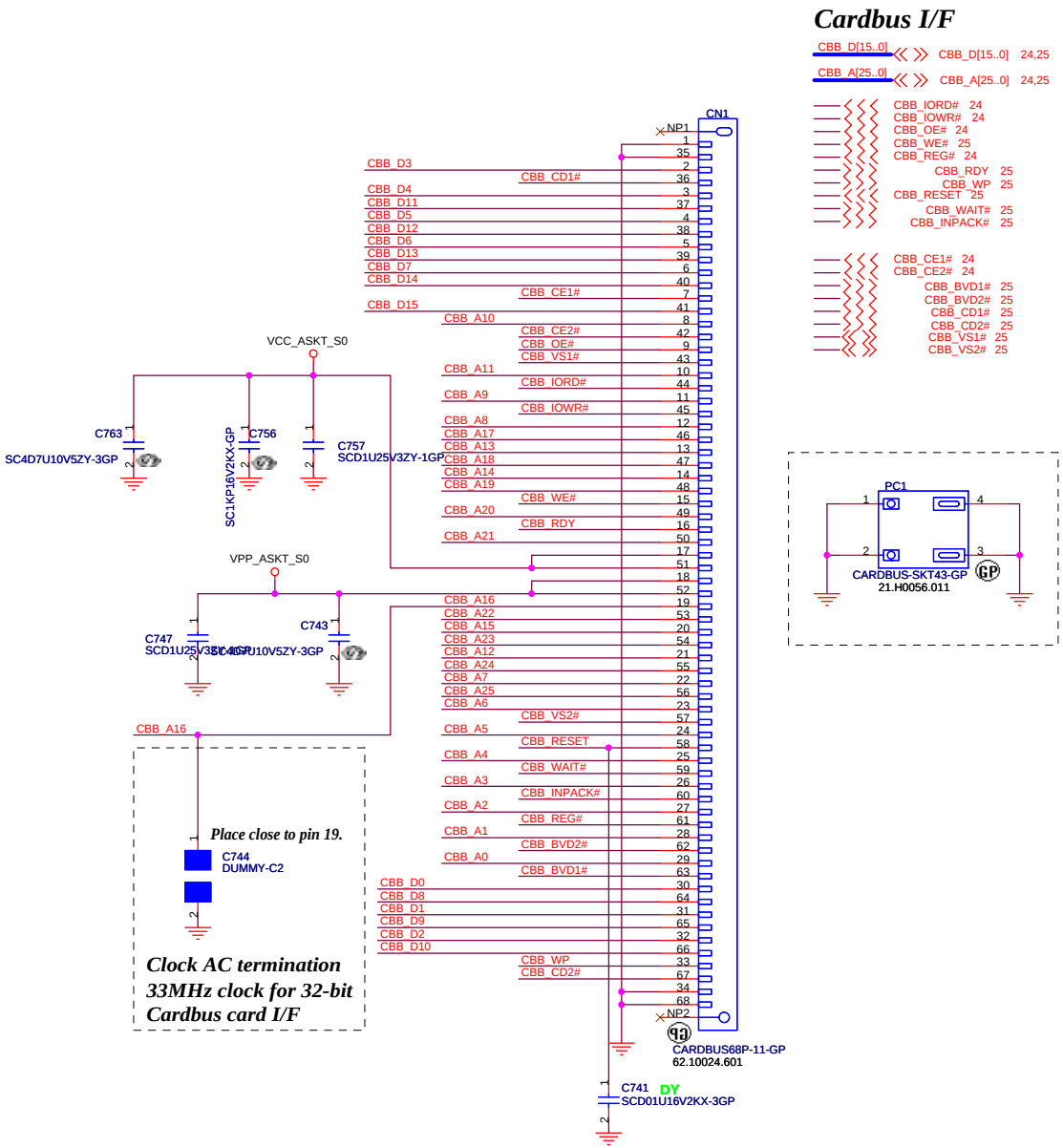




XD
MS / MS PRO
SD / SD IO / MMC

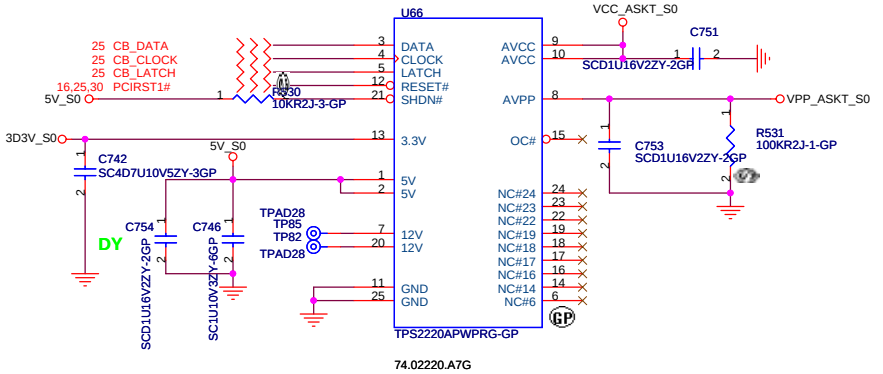
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD / 1394 / CARD READER		
Size	Document Number: MYALL2	Rev: MP
Date: Friday, March 31, 2006	Sheet 26 of 57	

PCMCIA Socket



Cardbus I/F

Power switch



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCMCIA	
Size	Document Number MYALL2	Rev MP
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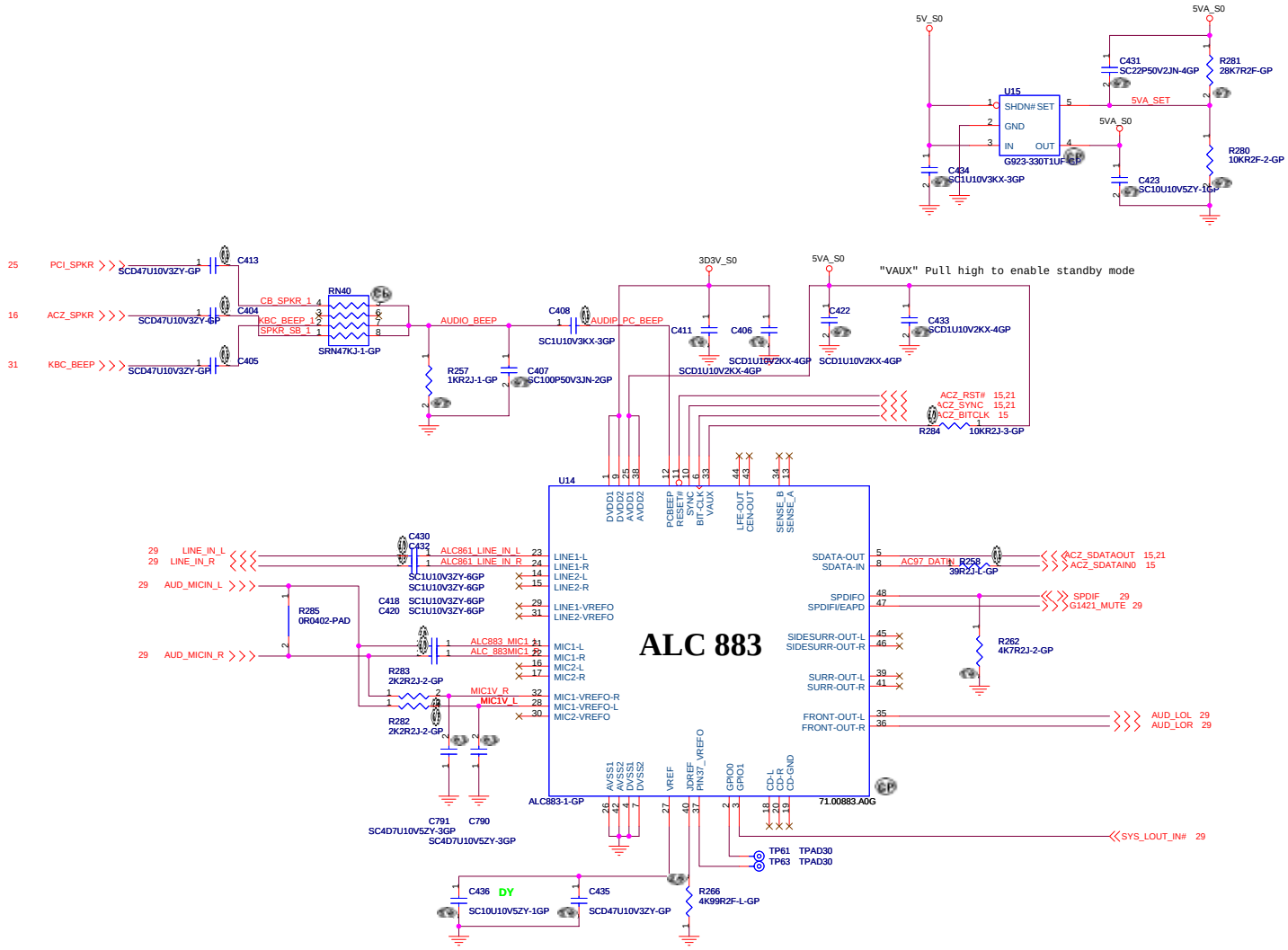

蜂創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	*AZALIA CODEC - ALC883*		
Size	Document Number MYALL2		Rev MP
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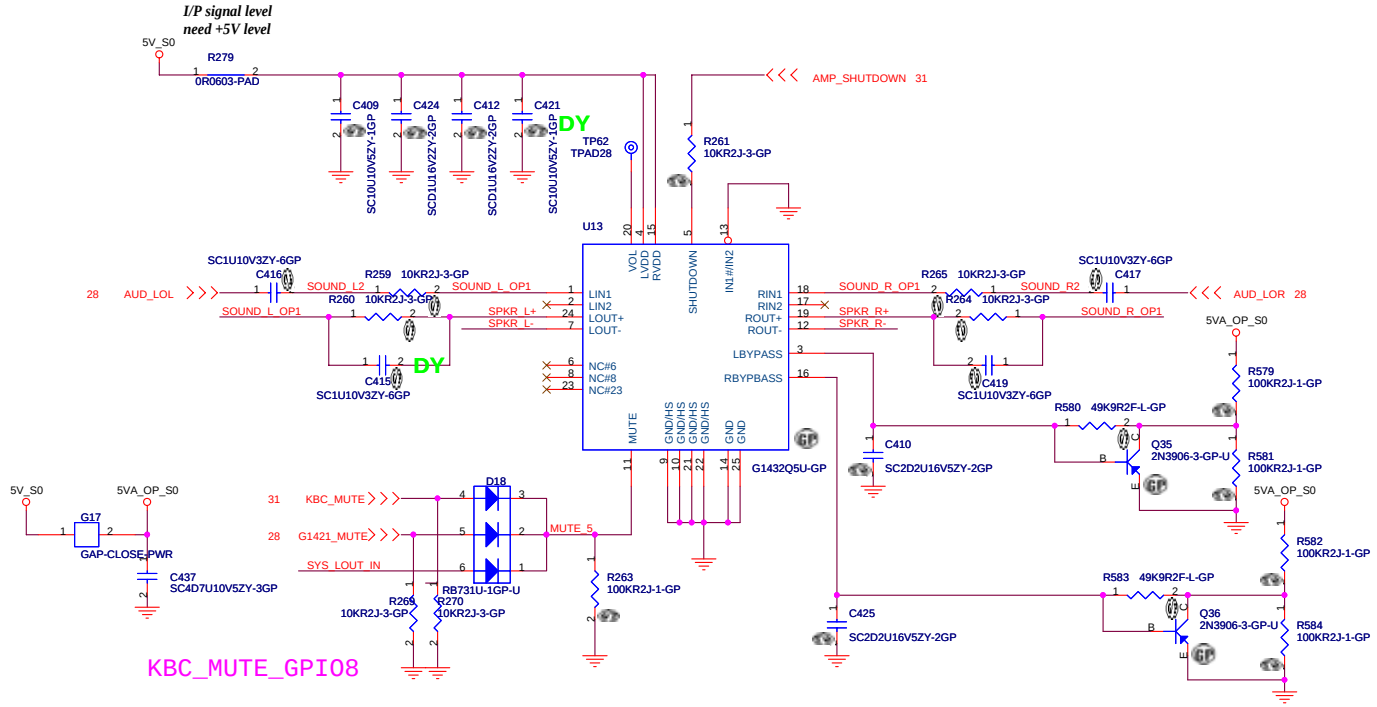
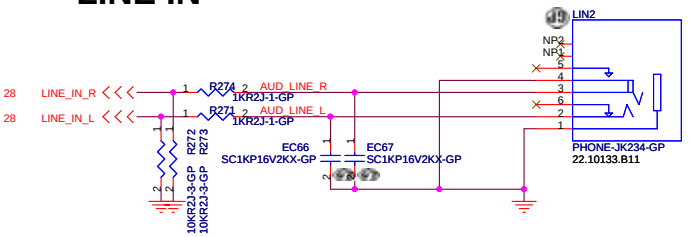
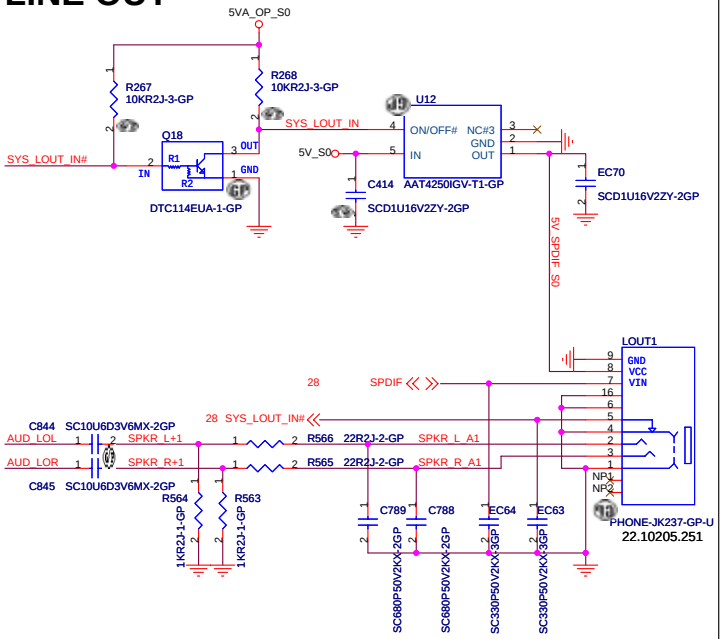
AUDIO OP AMPLIFIER



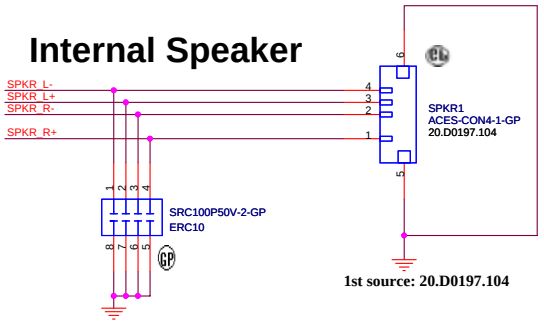
LINE IN



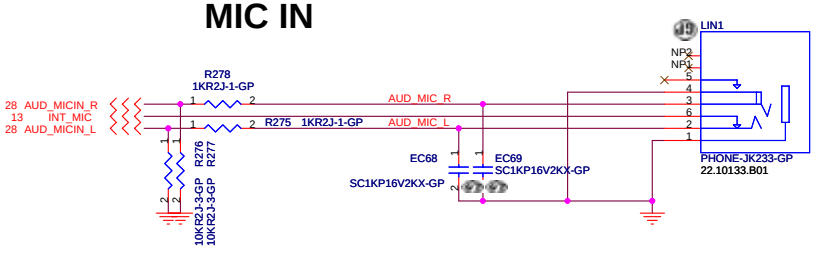
LINE OUT



Internal Speaker



MIC IN



蜂創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP AND JACK

Size: | Document Number: MYALL2 | Rev: MP

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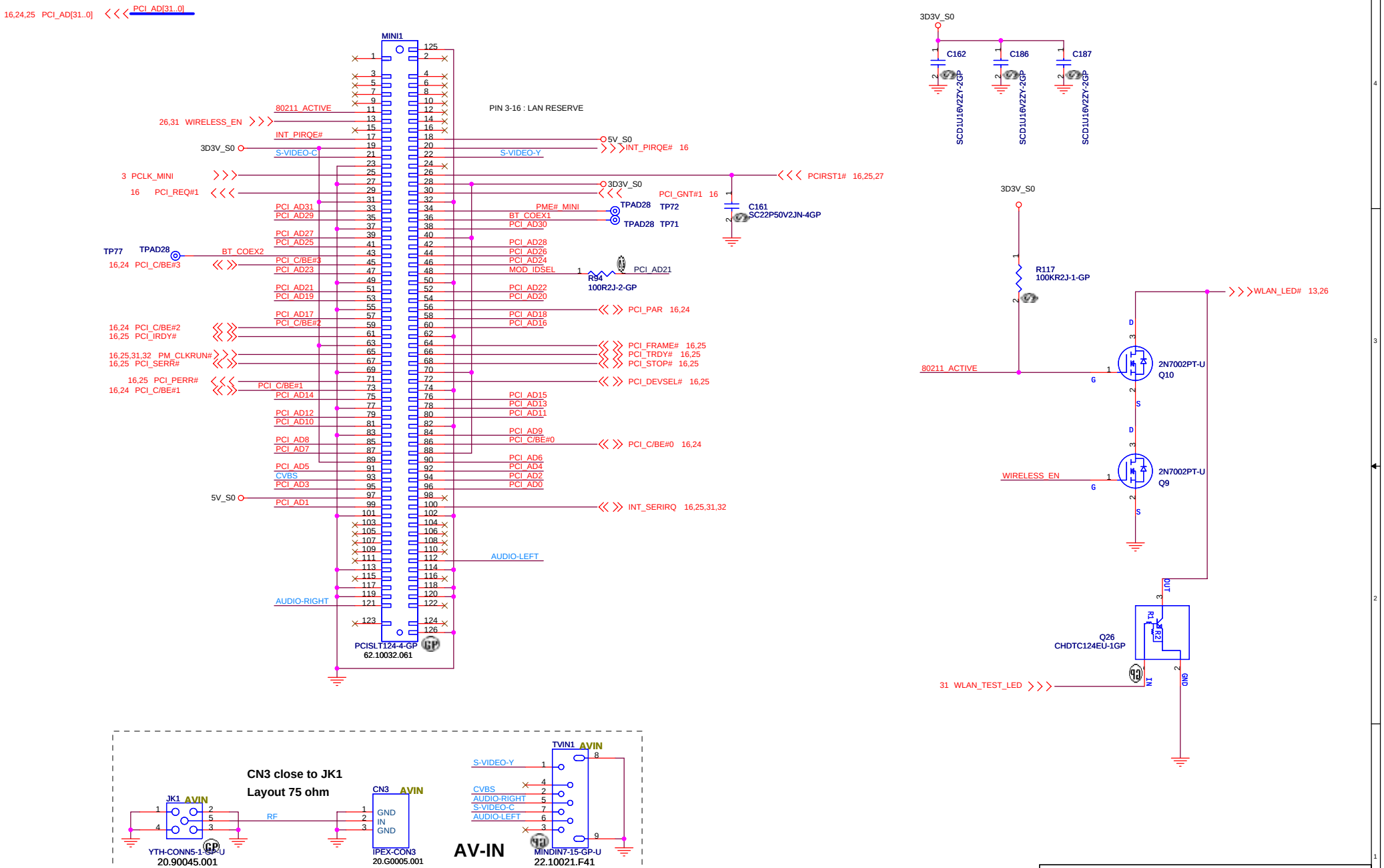

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*MINI-PCI / AV-IN*	
Size	Document Number MYALL2	Rev MP
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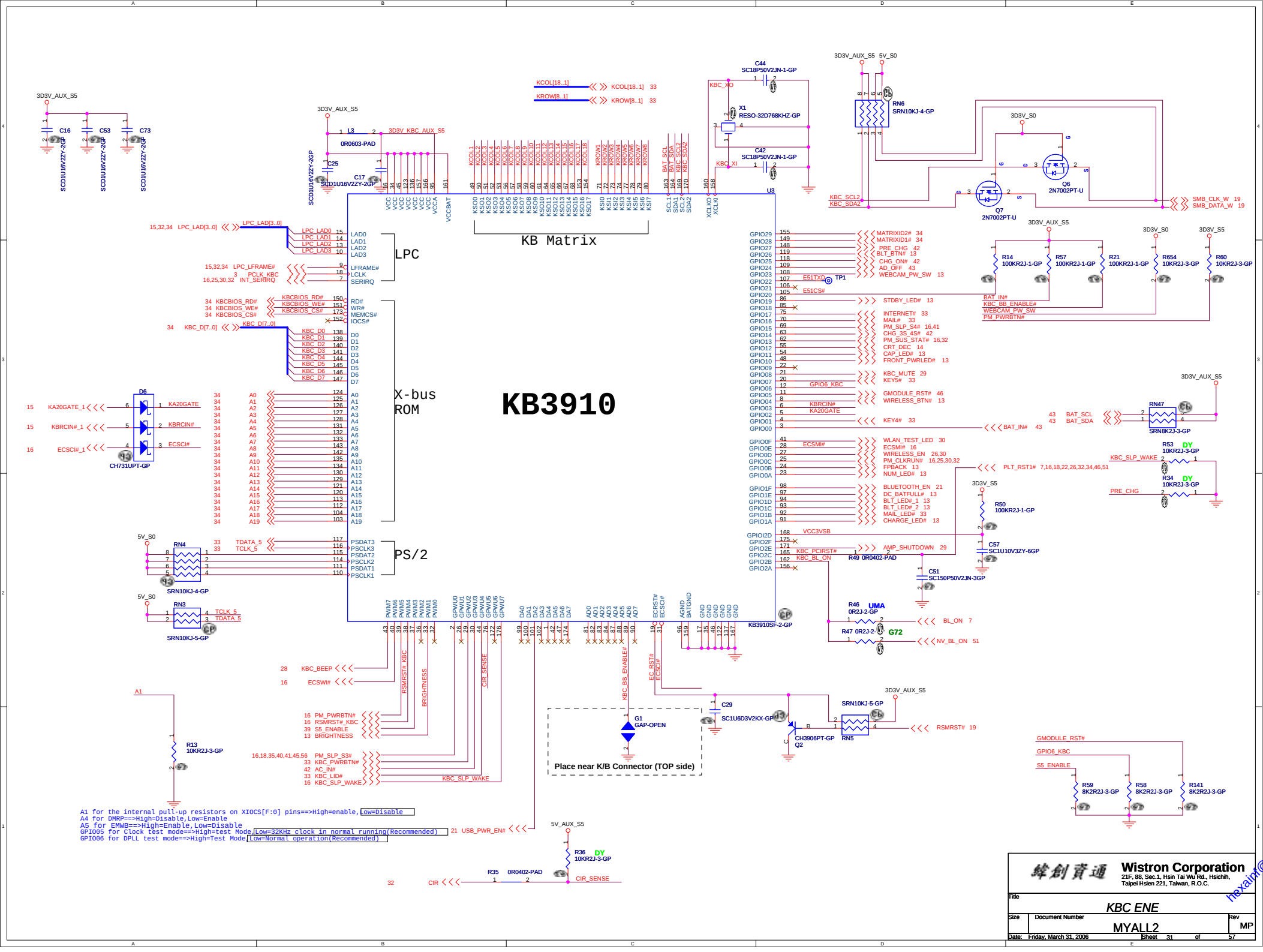
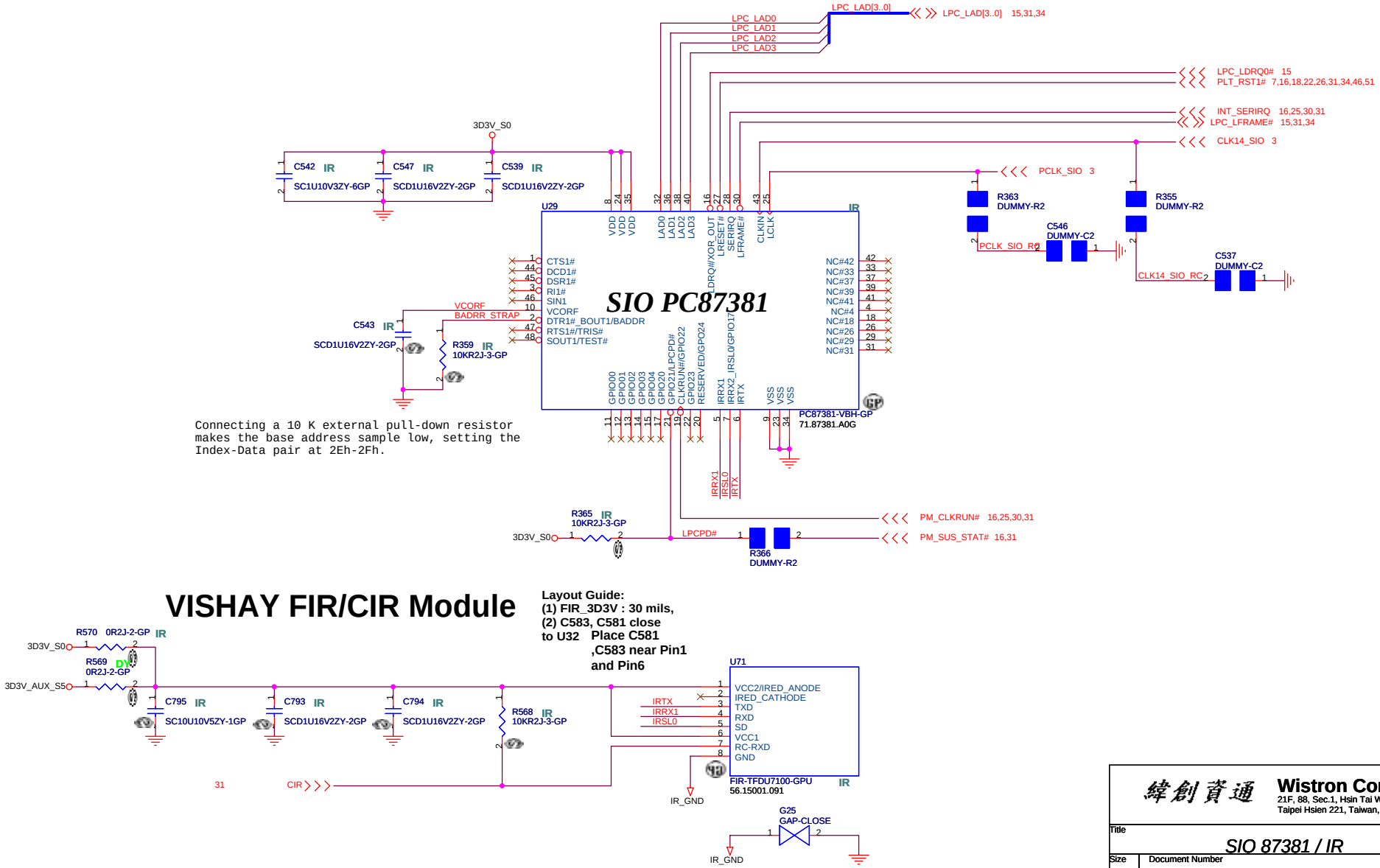

KB3910
KB Matrix
LPC
X-bus ROM
PS/2
Place near K/B Connector (TOP side)
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable, Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC ENE
MYALL2
MP
Friday, March 31, 2006
31
57
hexainf@hotmail.com



VISHAY FIR/CIR Module

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32 Place C581 ,C583 near Pin1 and Pin6

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*SIO 87381 / IR*	
Size	Document Number: MYALL2	Rev: MP
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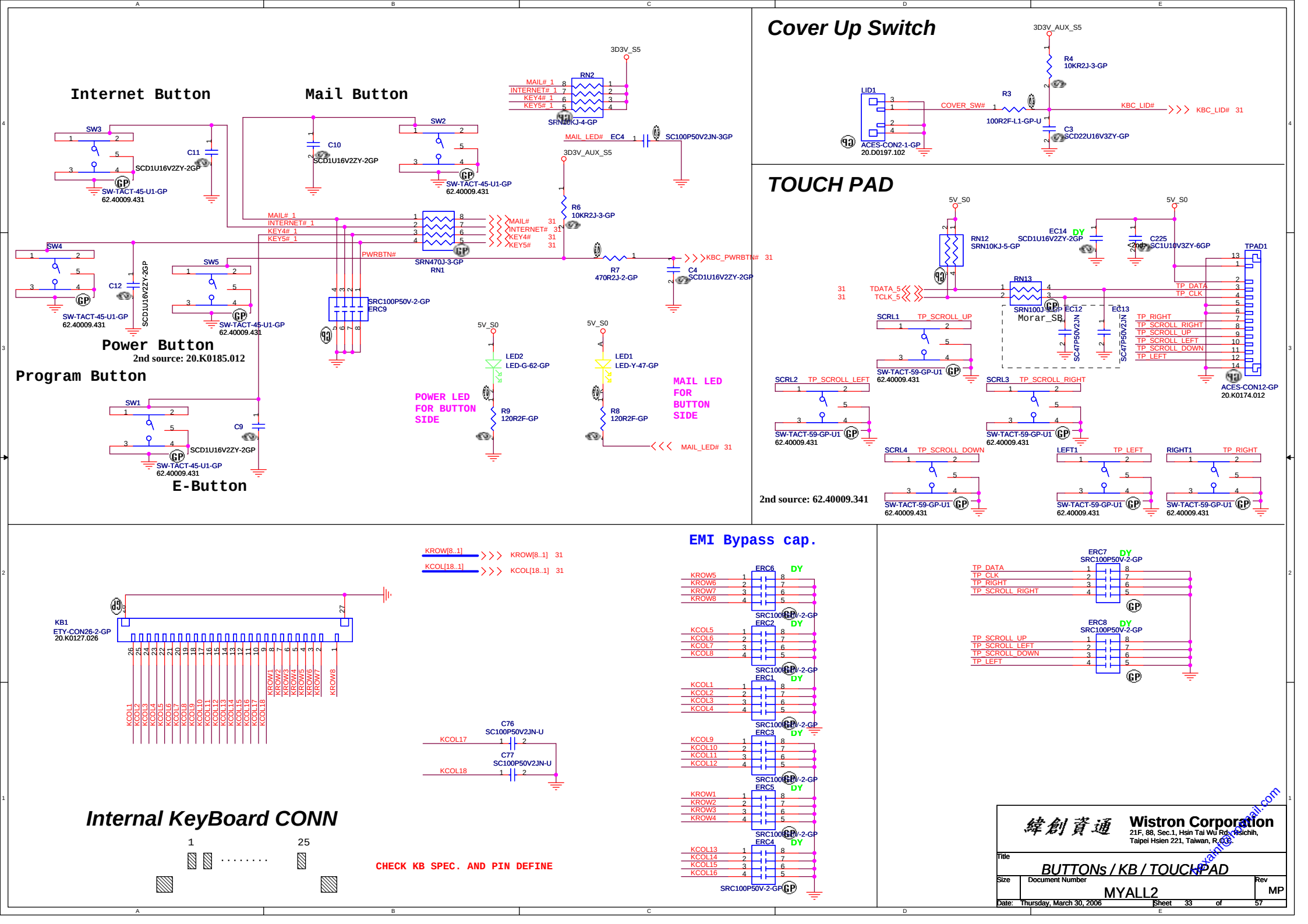
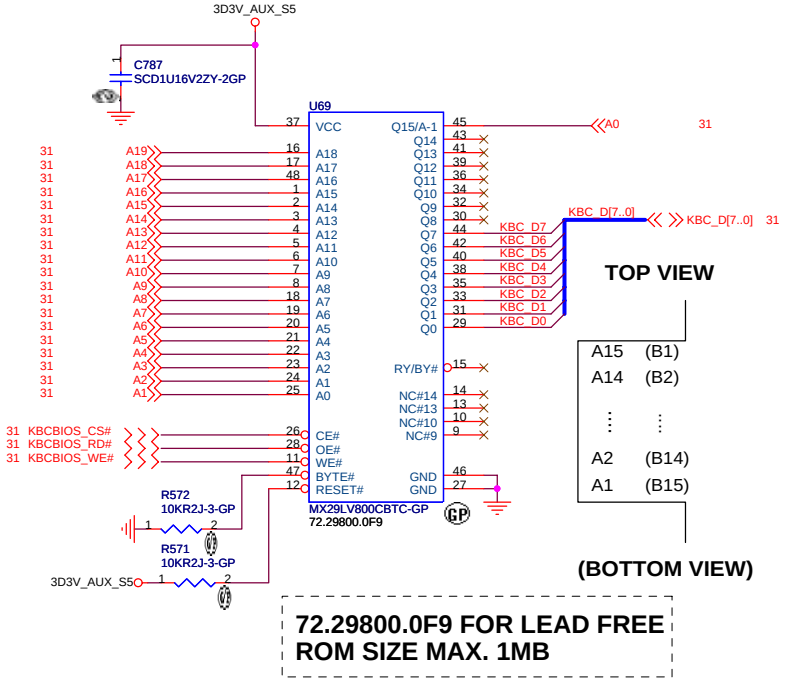
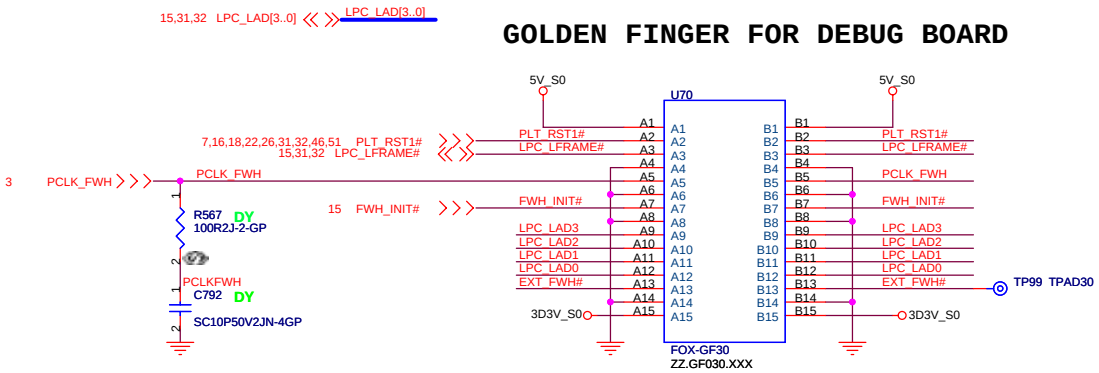
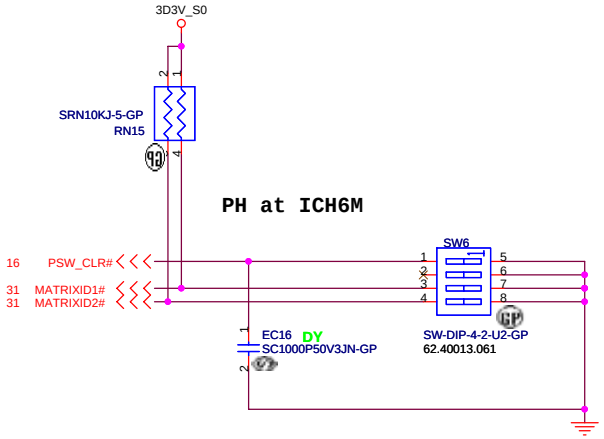

Internet Button
Mail Button
Power Button
2nd source: 20.K0185.012
Program Button
E-Button
POWER LED FOR BUTTON SIDE
MAIL LED FOR BUTTON SIDE
Cover Up Switch
TOUCH PAD
2nd source: 62.40009.341
EMI Bypass cap.
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BUTTONs / KB / TOUCHPAD
Size
Document Number
MYALL2
Rev
MP
Date: Thursday, March 30, 2006
Sheet 33 of 57







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Title	*BIOS*	
Size	Document Number: MYALL2	Rev: MP
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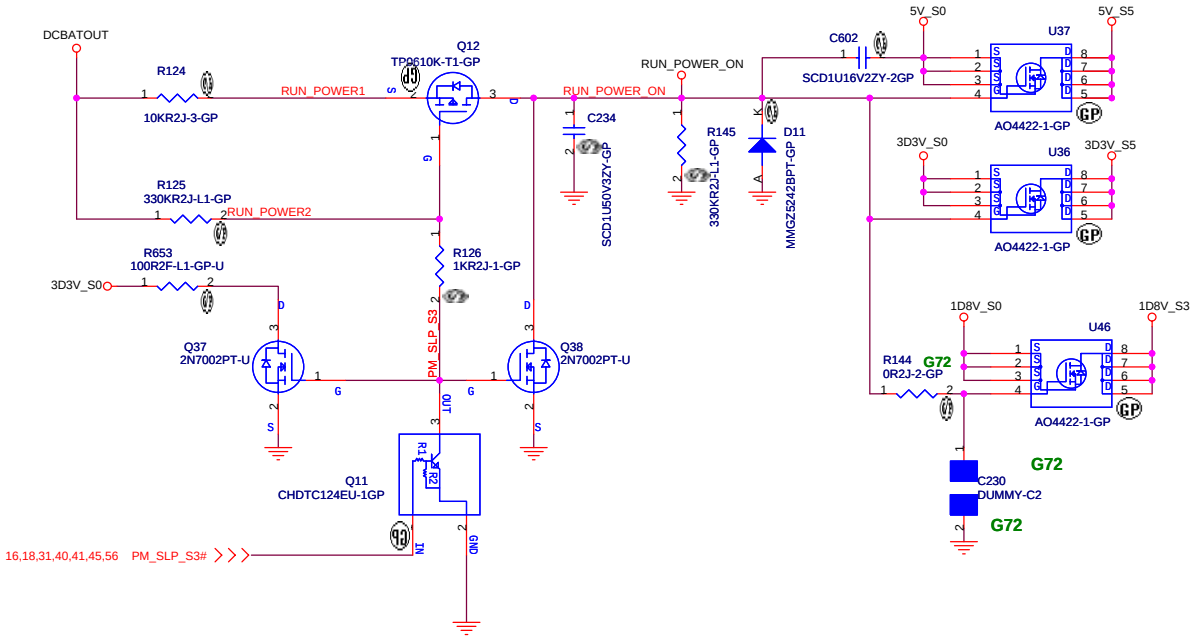
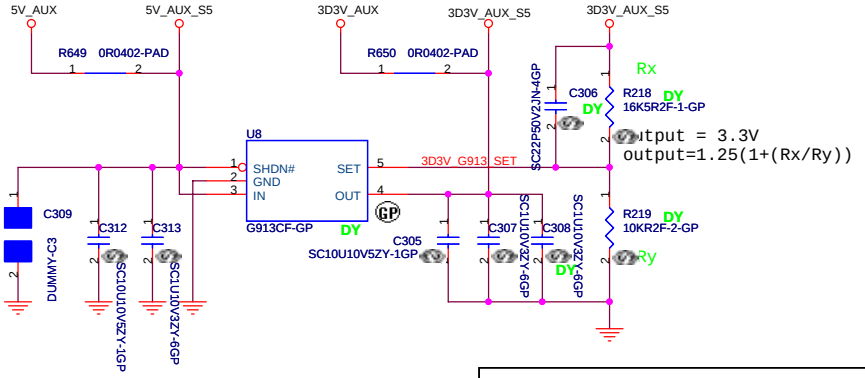
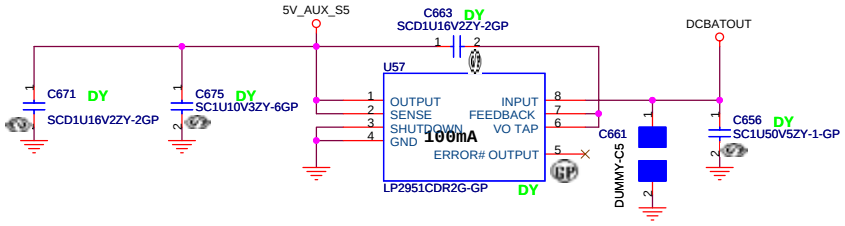
Run Power



Aux Power

3D3V_AUX_S5

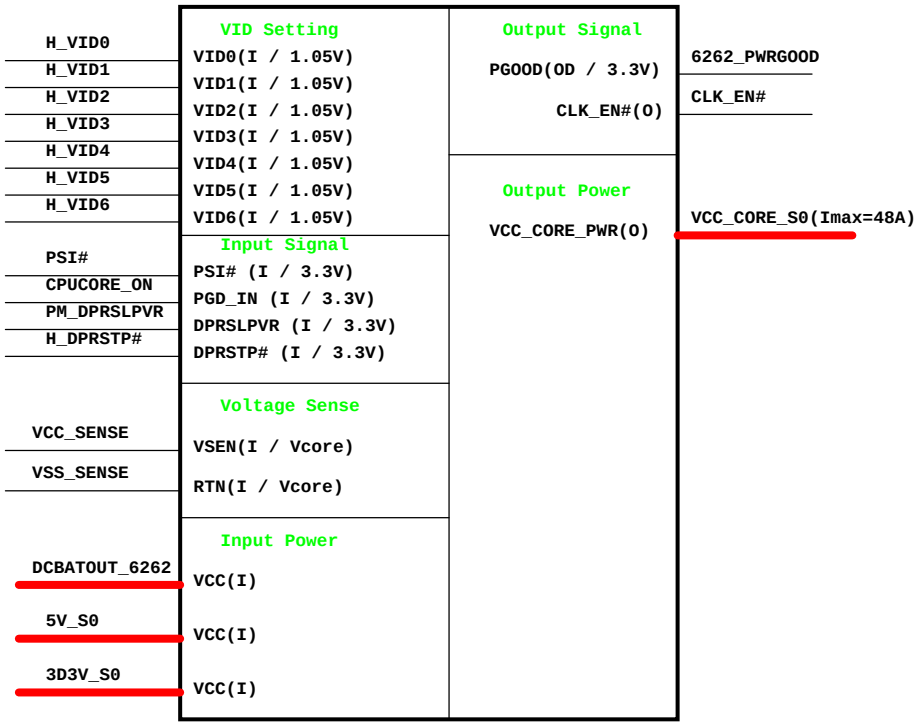




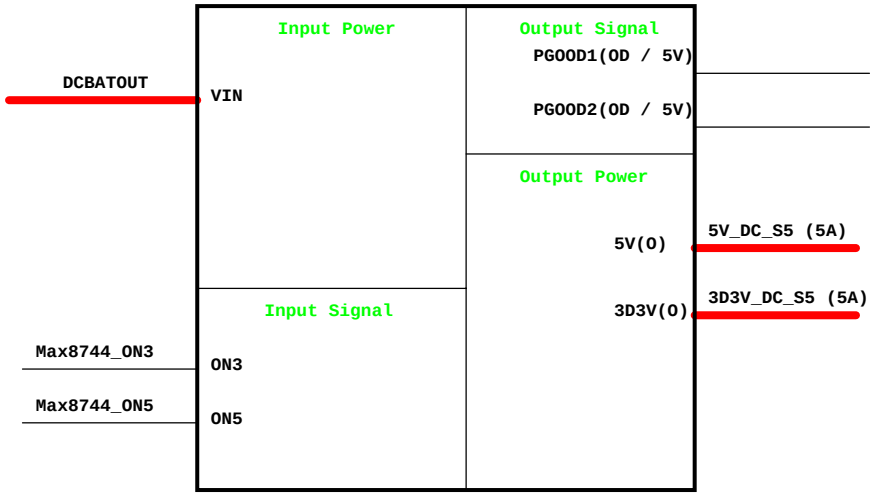
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER and 3D3V_AUX_S5	
Size	Document Number: MYALL2	Rev: MP
Date: Thursday, March 30, 2006	Sheet 35 of 57	

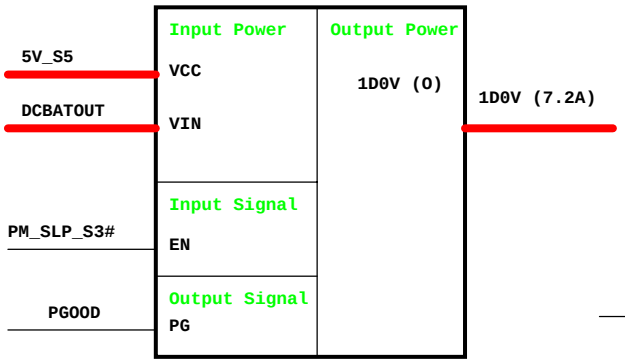
CPU_CORE
Intersil ISL6262



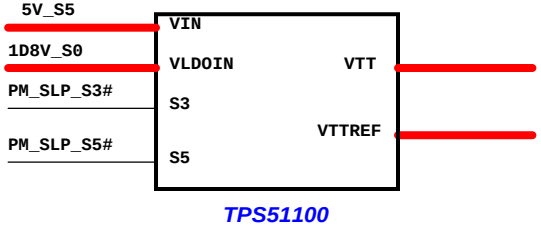
Max8744 3D3V/5V



ISL6269_VGA_Core 1D0V

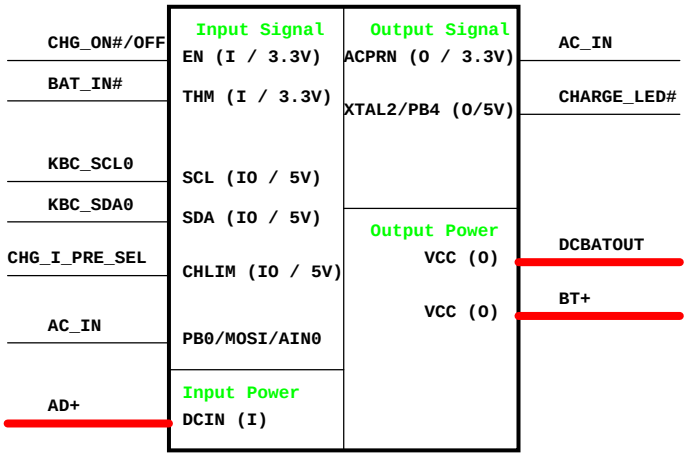


0D9V_S3

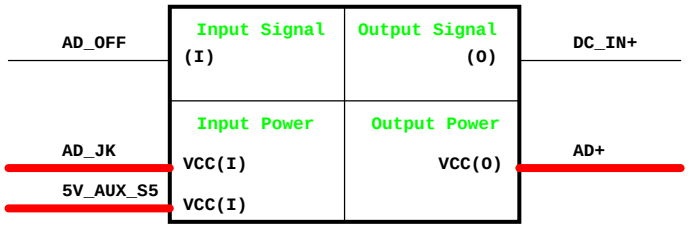


TPS51100

Charger_ISL6255



Adapter



緯創資通 **Wistron Corporation**
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Title	*Power Block Diagram*	
Size	Document Number: MYALL2	Rev: MP
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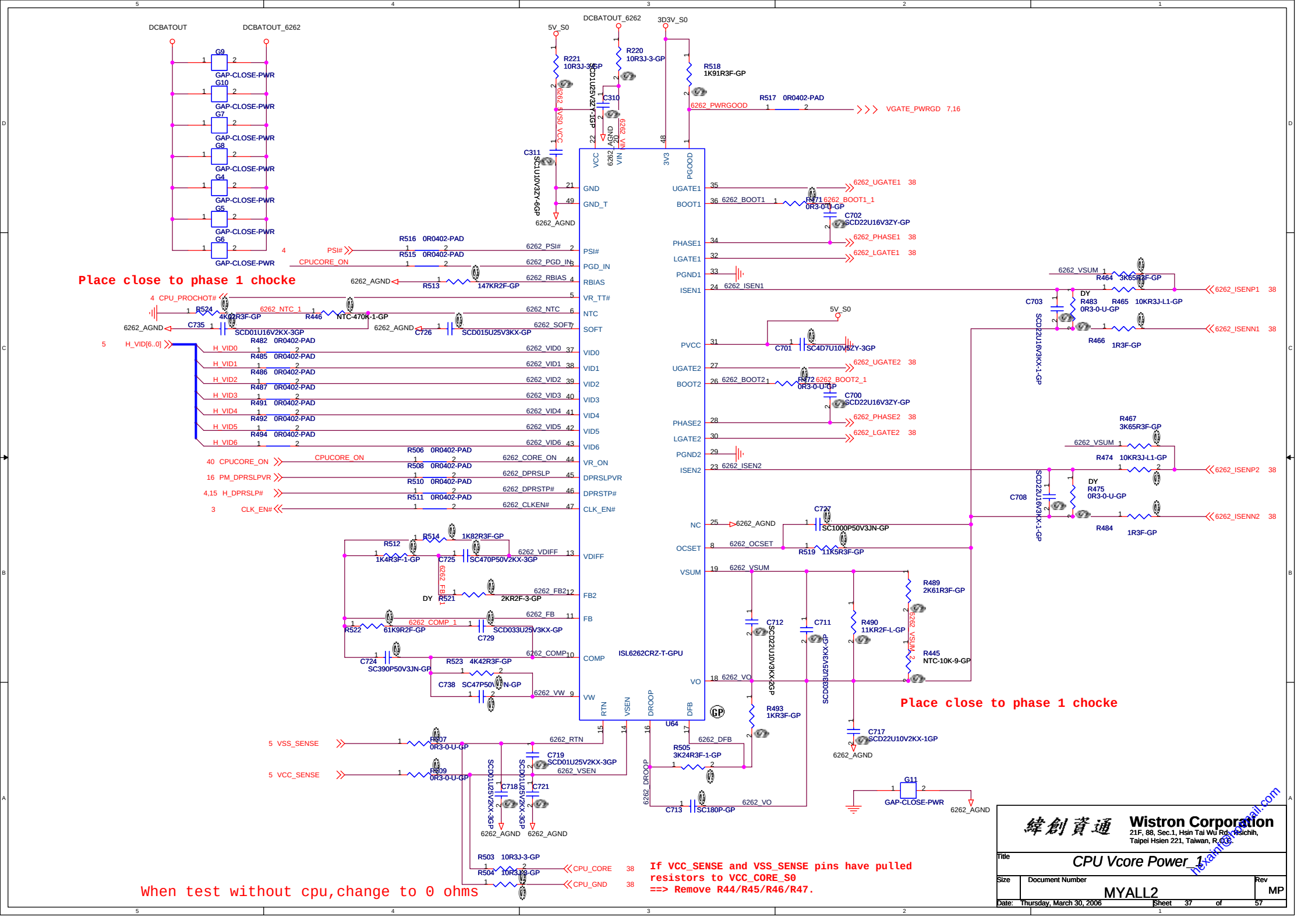
DCBATOUT
DCBATOUT_6262
5V_S0
3D3V_S0
ISL6262CRZ-T-GPU
Place close to phase 1 chocke
Place close to phase 1 chocke
When test without cpu,change to 0 ohms
If VCC_SENSE and VSS_SENSE pins have pulled resistors to VCC_CORE_S0
==> Remove R44/R45/R46/R47.
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Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore Power_1
MYALL2
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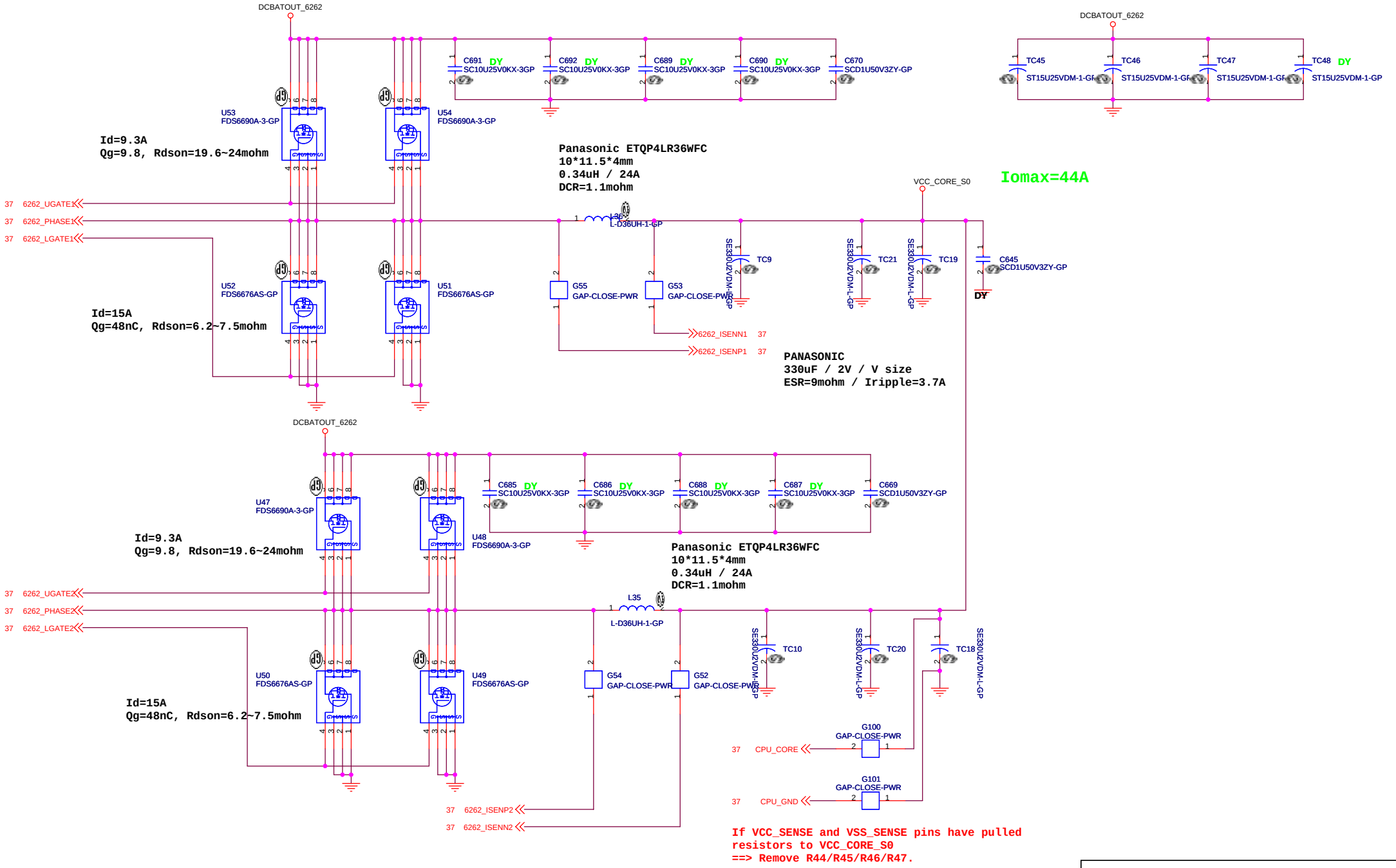

緯創資通 **Wistron Corporation**
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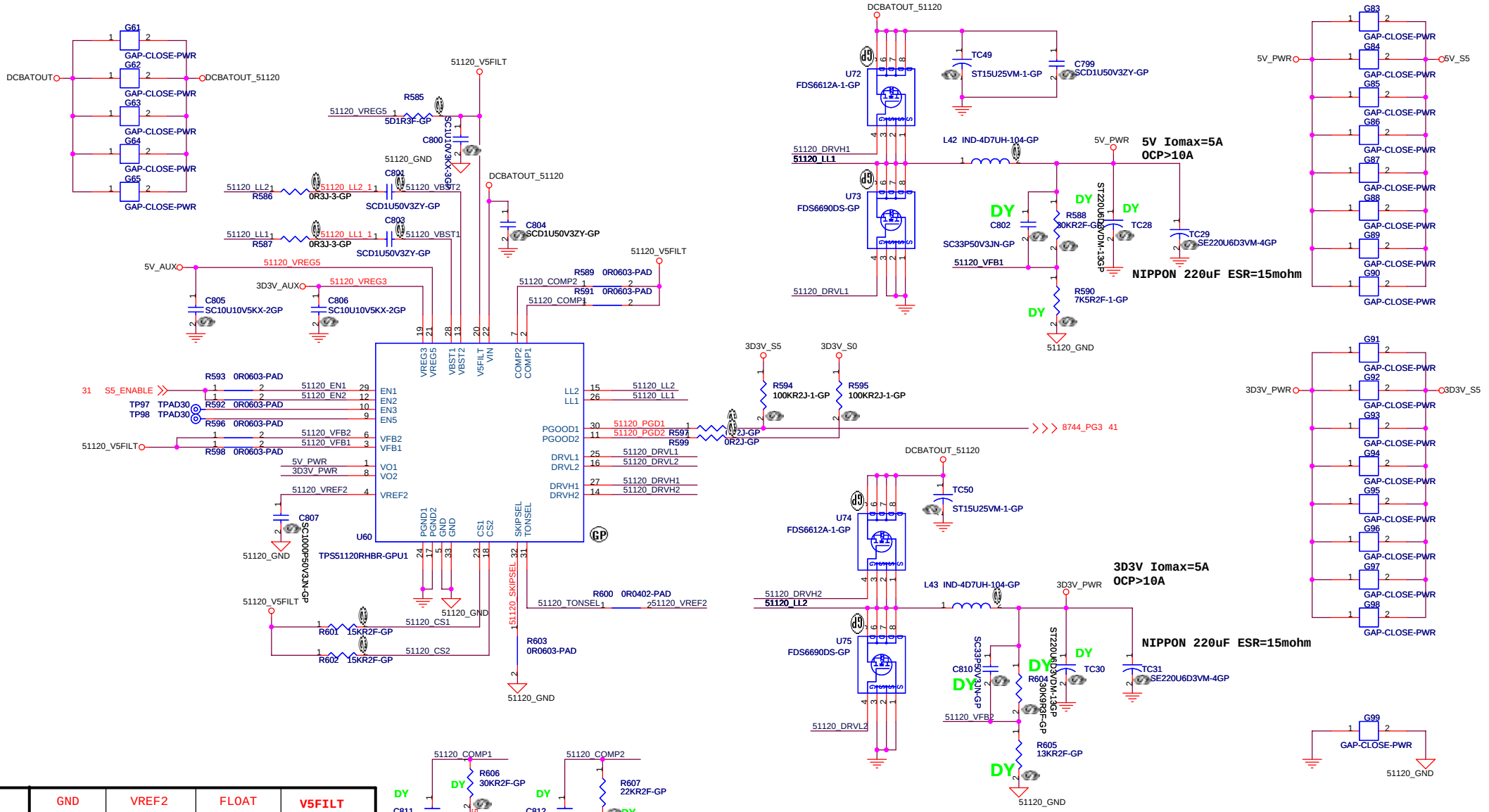
Taipei Hsien 221, Taiwan, R.O.C.

Title	*CPU Vcore Power_2*	
Size	Document Number: MYALL2	Rev: MP
Date: Thursday, March 30, 2006	Sheet 38 of 57	



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	**280k/CH1 430k/CH2**	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

緯創資通 Wistron Corporation
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Title: 3D3V_S5 & 5V_S5
Size: Document Number: MYALL2 Rev: MP
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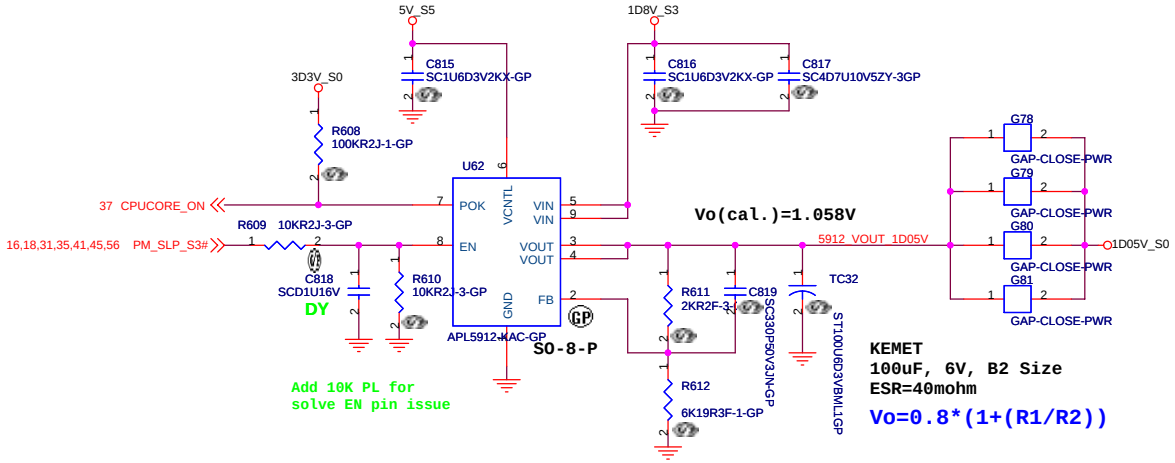

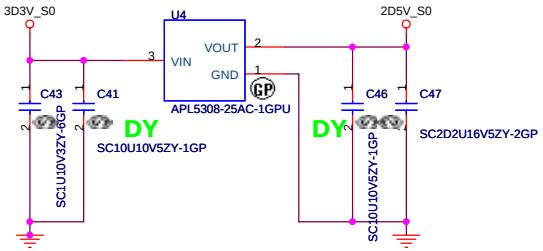

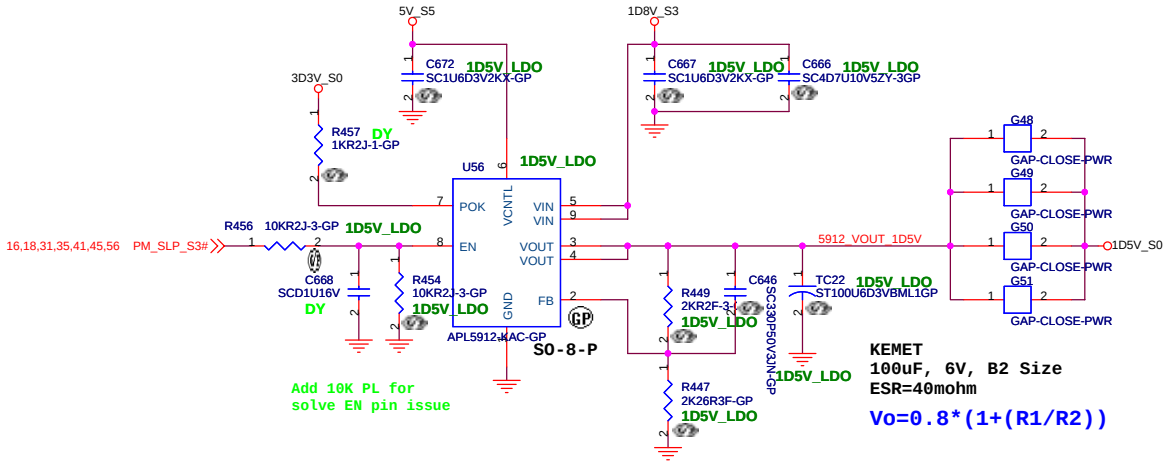

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*1D05V / 1D5V/2D5V*	
Size	Document Number: MYALL2	Rev: MP
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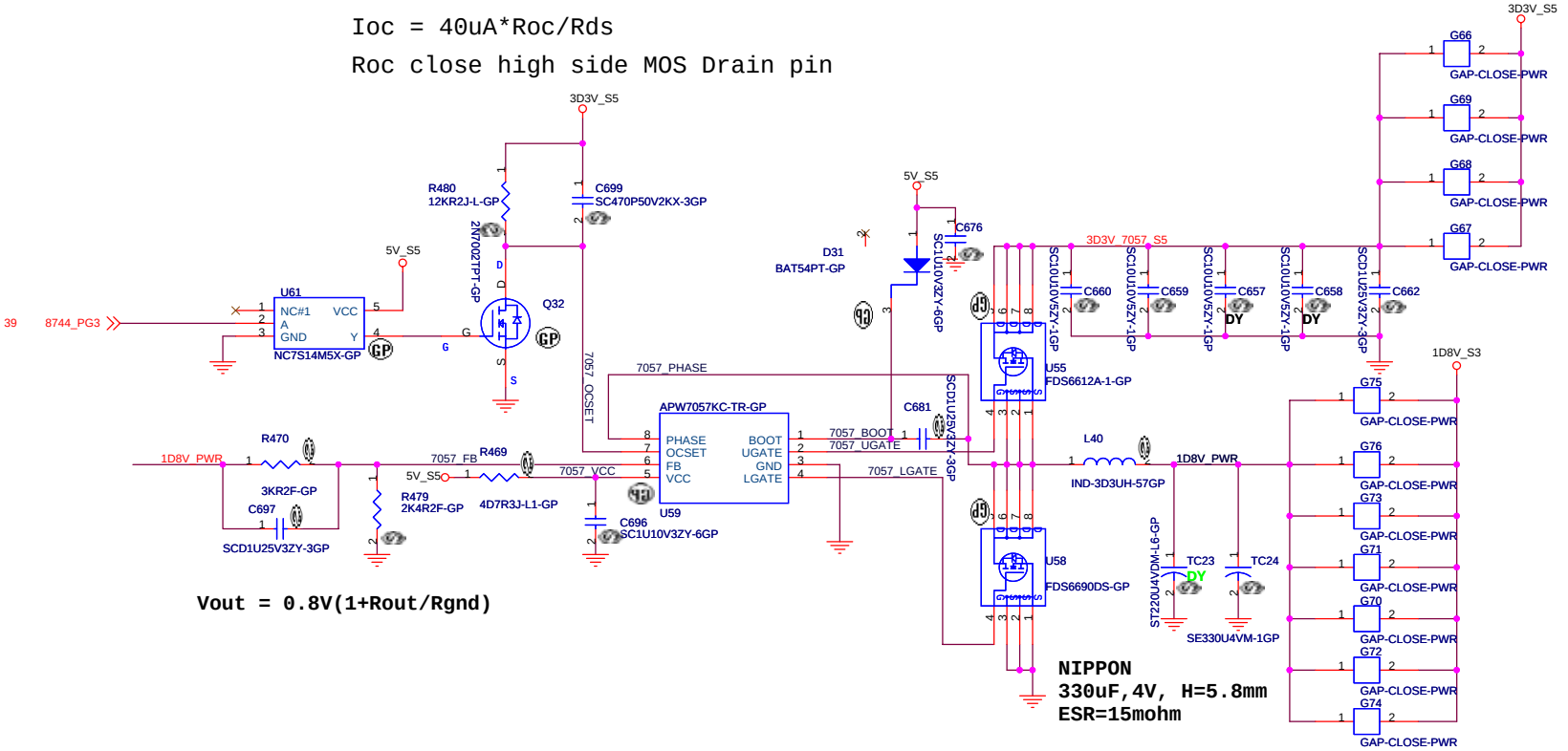
Ioc = 40uA*Roc/Rds

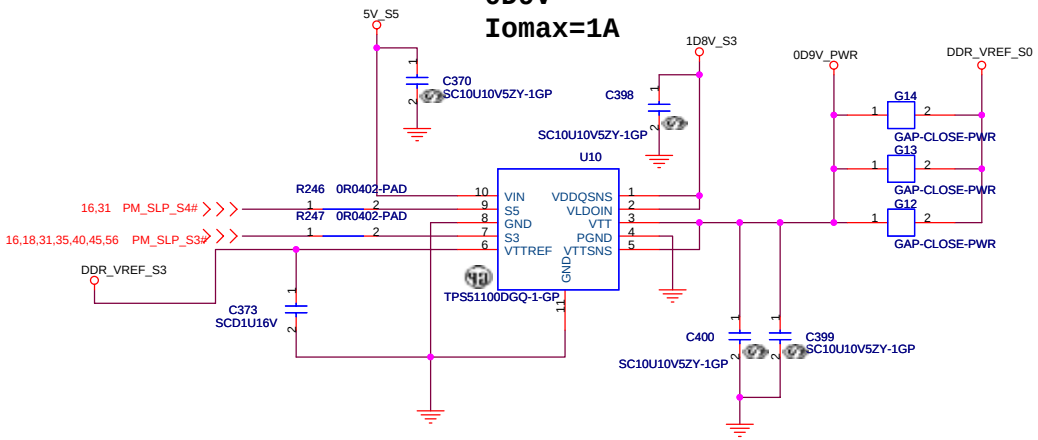
Roc close high side MOS Drain pin



Vout = 0.8V(1+Rout/Rgnd)

NIPPON
330uF,4V, H=5.8mm
ESR=15mohm

0D9V
Iomax=1A



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: APW7057 / 1D8V/0D9V

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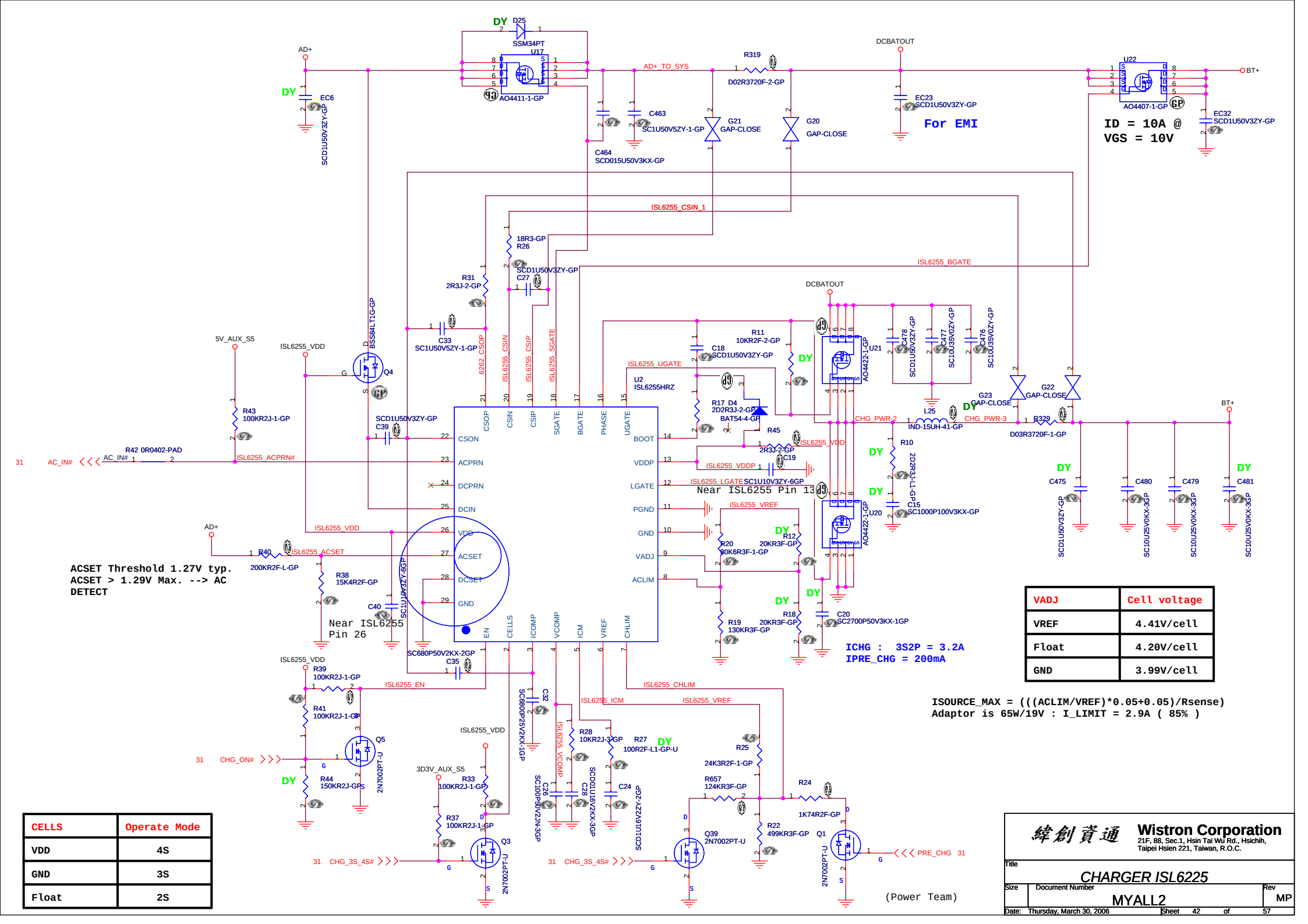

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL6225

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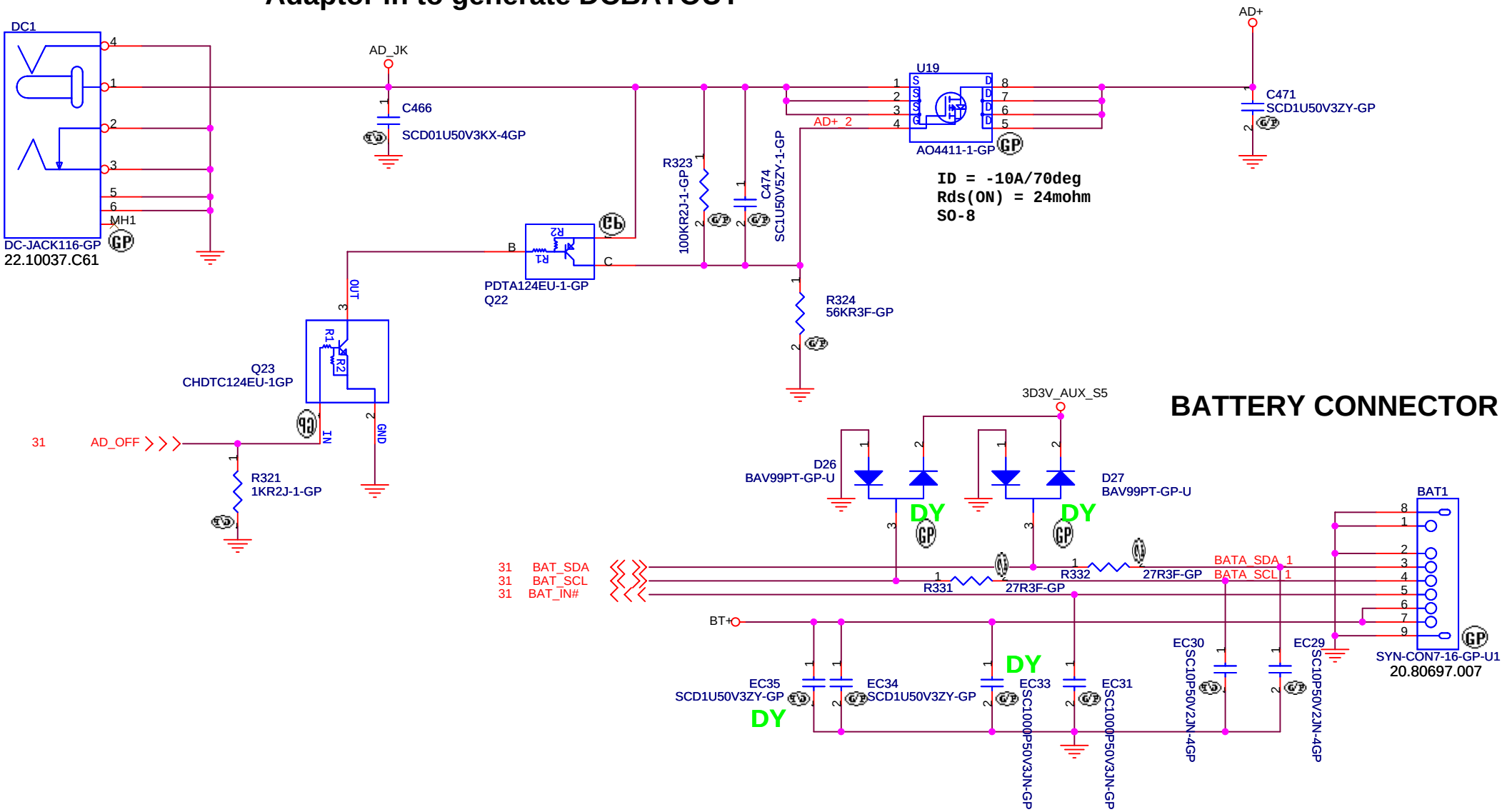
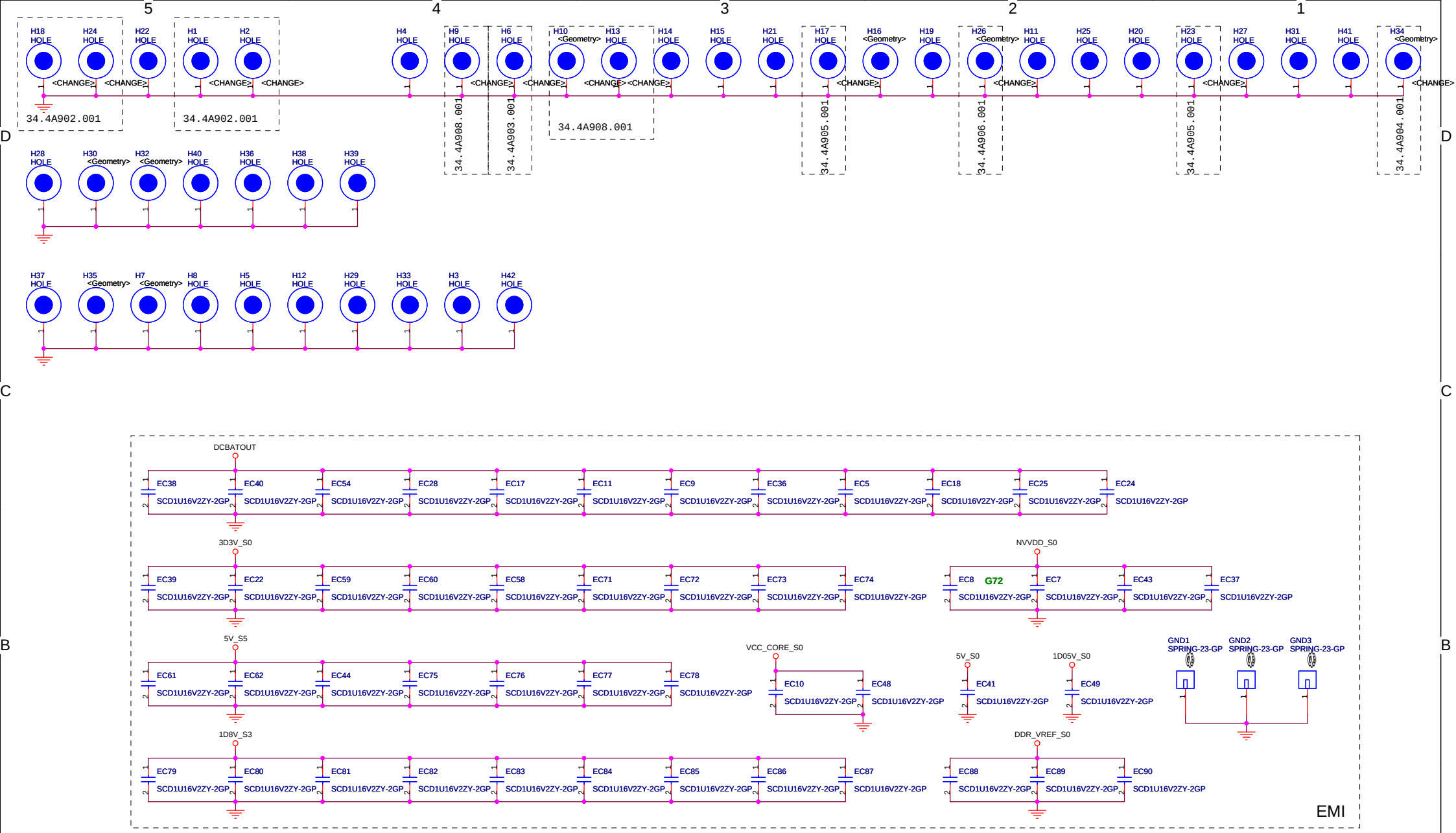
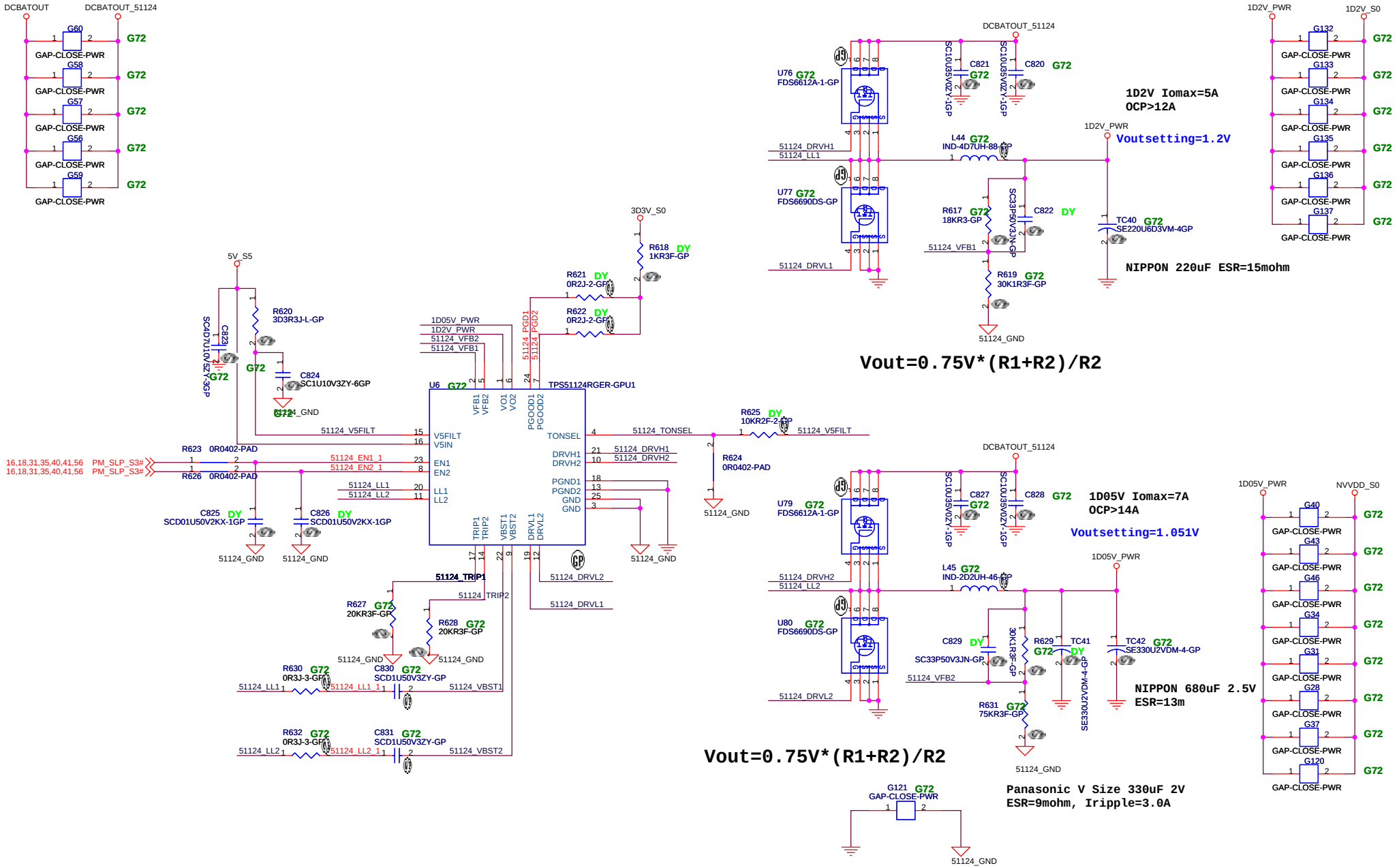
Adaptor in to generate DCBATOUT



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AD/BATT CONN*	
Size	Document Number: MYALL2	Rev: MP
Date: Thursday, March 30, 2006	Sheet 43 of 57	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*EMI*	
Size	Document Number: MYALL2	Rev: MP
Date: Friday, March 24, 2006	Sheet 44 of 57	



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 / NVDD/1D2V

Size	Document Number	Rev
	MYALL2	MP

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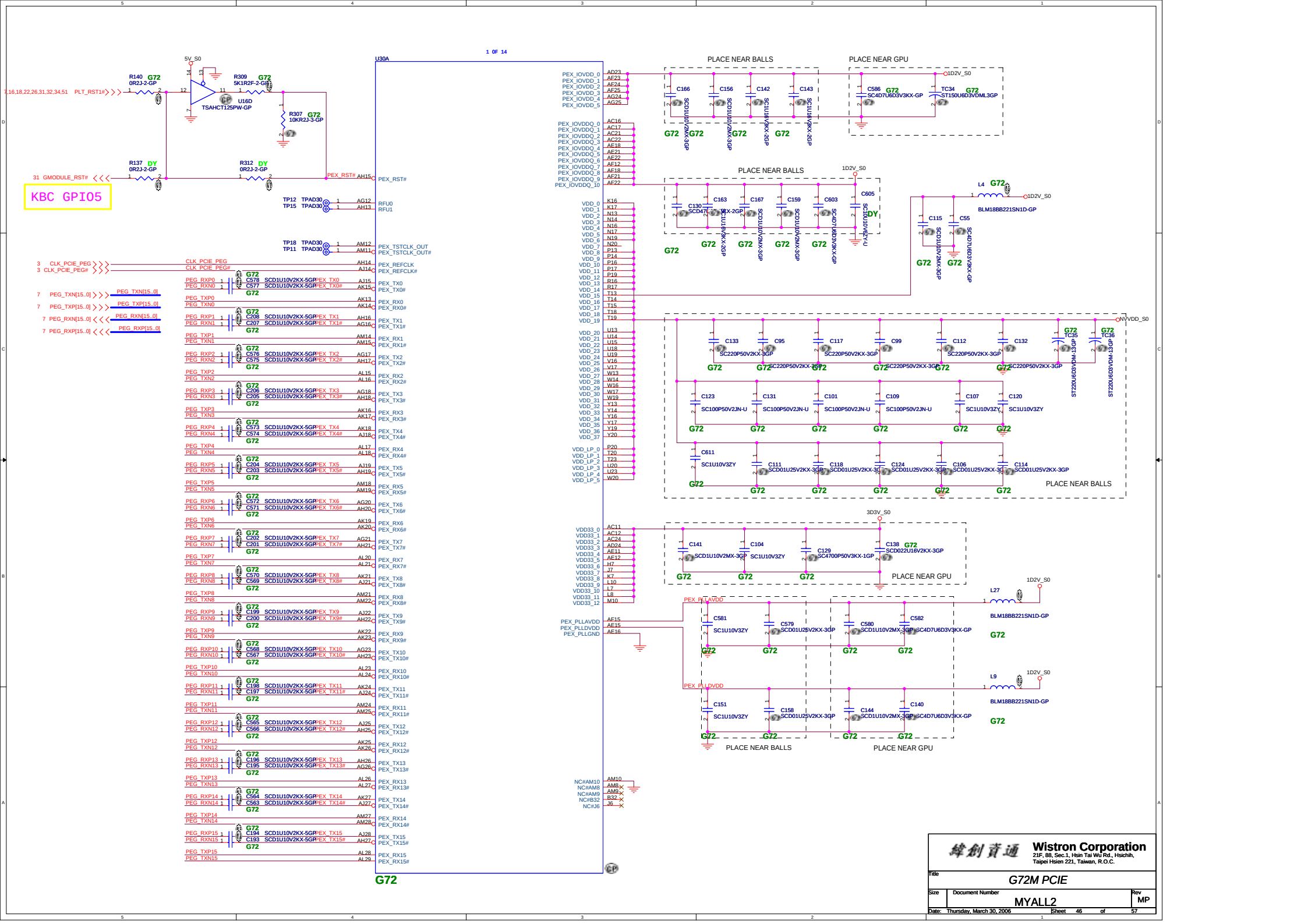
U30A
1 OF 14
G72
5V_S0
U16D
TSAHCT125PW-GP
R140 G72 0R2J-2-GP
R309 G72 5K1R2F-2-GP
R307 G72 10KR2J-3-GP
R137 DY 0R2J-2-GP
R312 DY 0R2J-2-GP
PLT_RST1#
GMODULE_RST#
PEX_RST#
KBC GPIO5
TP12 TPAD30
TP15 TPAD30
TP18 TPAD30
TP11 TPAD30
RFU0
RFU1
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
CLK_PCIE_PEG
CLK_PCIE_PEG#
PEX_REFCLK
PEX_REFCLK#
PEG_TXN[15..0]
PEG_TXP[15..0]
PEG_RXN[15..0]
PEG_RXP[15..0]
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
PEX_RX4#
PEX_TX5
PEX_TX5#
PEX_RX5
PEX_RX5#
PEX_TX6
PEX_TX6#
PEX_RX6
PEX_RX6#
PEX_TX7
PEX_TX7#
PEX_RX7
PEX_RX7#
PEX_TX8
PEX_TX8#
PEX_RX8
PEX_RX8#
PEX_TX9
PEX_TX9#
PEX_RX9
PEX_RX9#
PEX_TX10
PEX_TX10#
PEX_RX10
PEX_RX10#
PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
PEX_RX12#
PEX_TX13
PEX_TX13#
PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#
PEX_IOVDD
PEX_IOVDDQ
PEX_PLLAVDD
PEX_PLLDVDD
PEX_PLLGND
VDD
VDD_LP
VDD33
NC#AM10
NC#AM8
NC#AM9
NC#B32
NC#J6
PLACE NEAR BALLS
PLACE NEAR GPU
1D2V_S0
NVVDD_S0
3D3V_S0
L4 G72 BLM18BB221SN1D-GP
L27 G72 BLM18BB221SN1D-GP
L9 G72 BLM18BB221SN1D-GP
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G72M PCIE
Size
Document Number
MYALL2
Rev
MP
Date: Thursday, March 30, 2006
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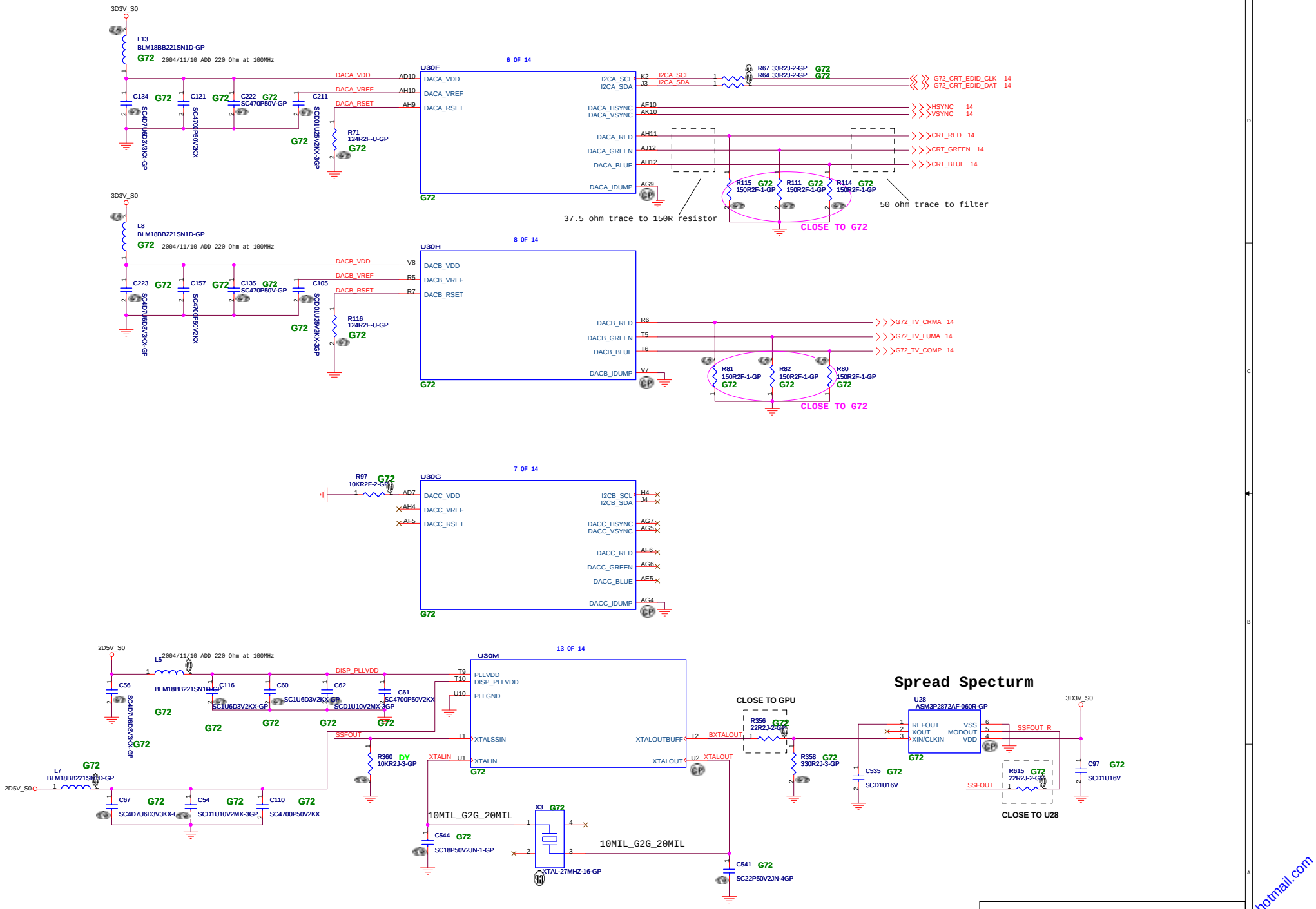
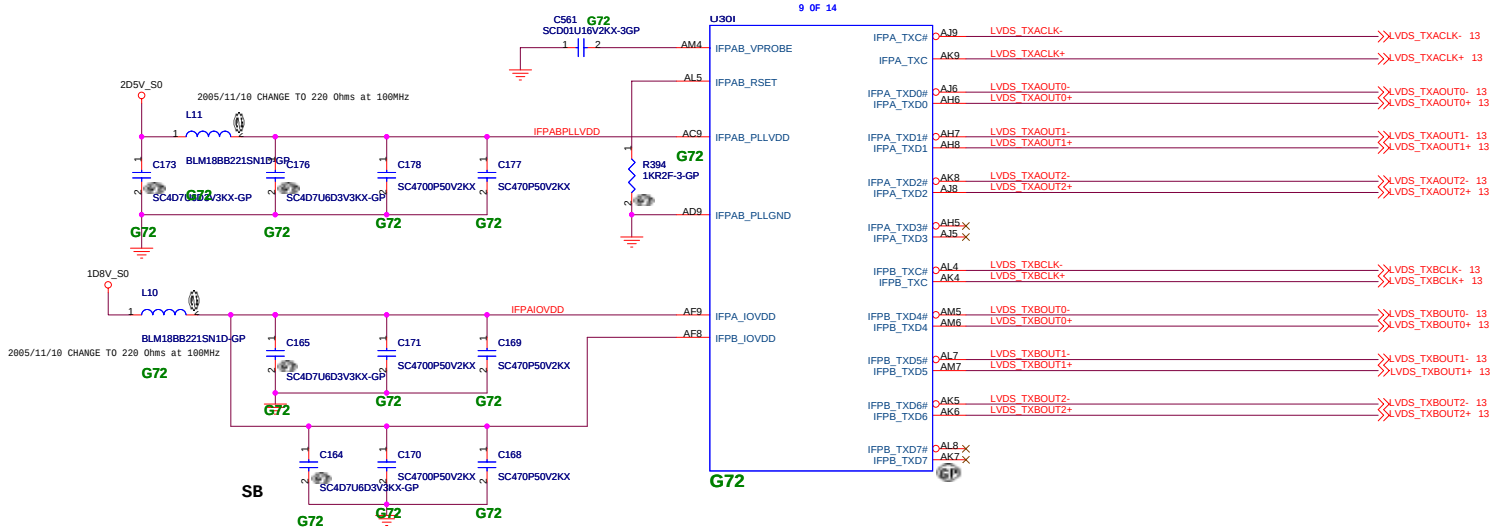
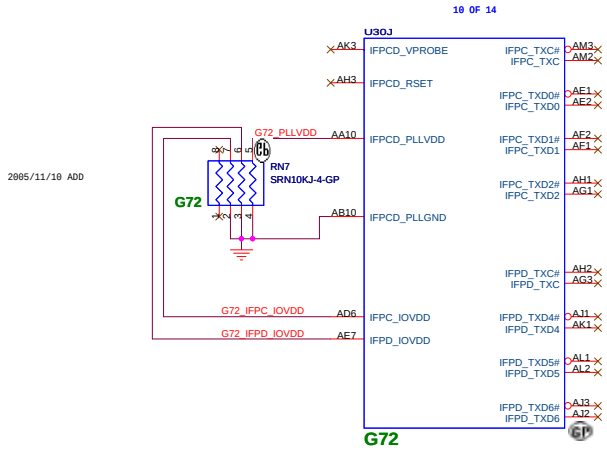
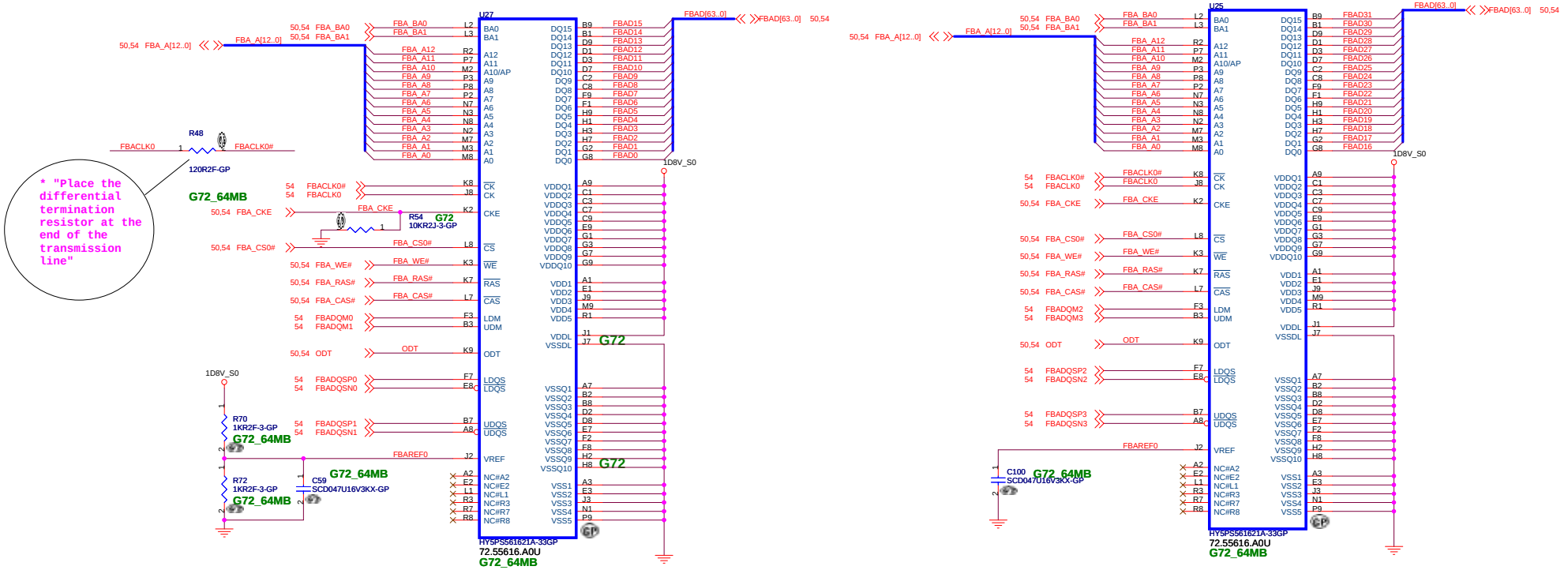


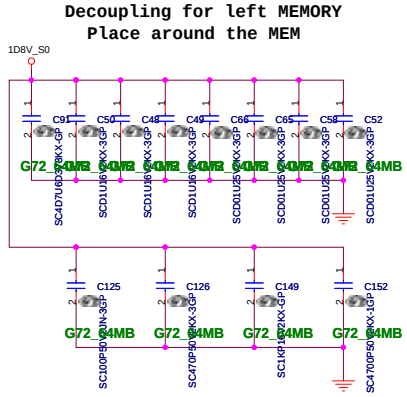
Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	G72M CRT & TV OUT		
Size	Document Number	MYALL2	Rev MP
Date: Thursday, March 30, 2006	Sheet 47 of 57		

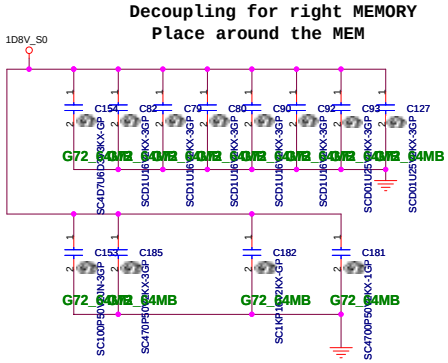




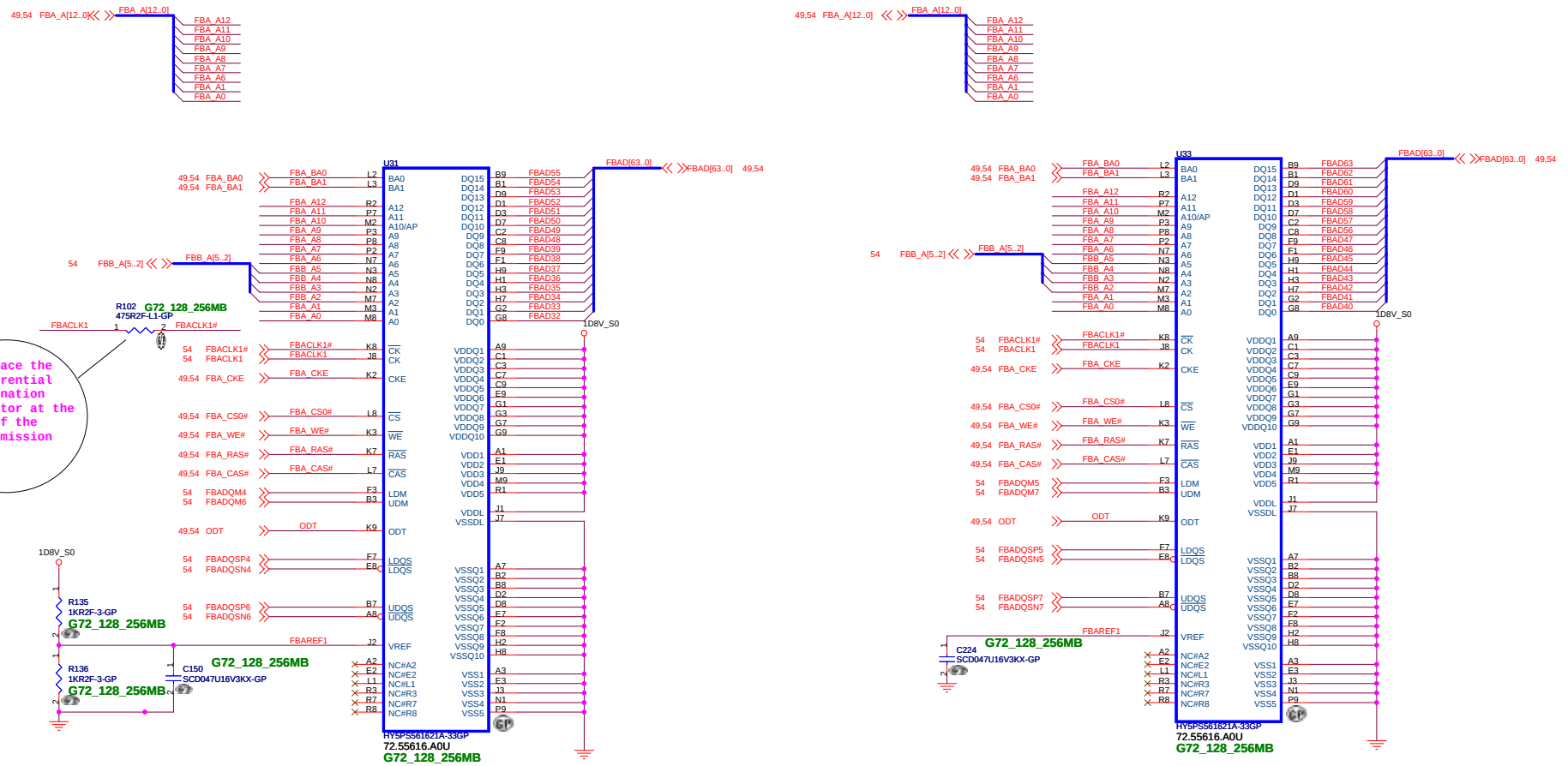
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: G72M LVDS & TMDS		
Size	Document Number: MYALL2	Rev: MP
Date: Thursday, March 30, 2006	Sheet 48 of 57	



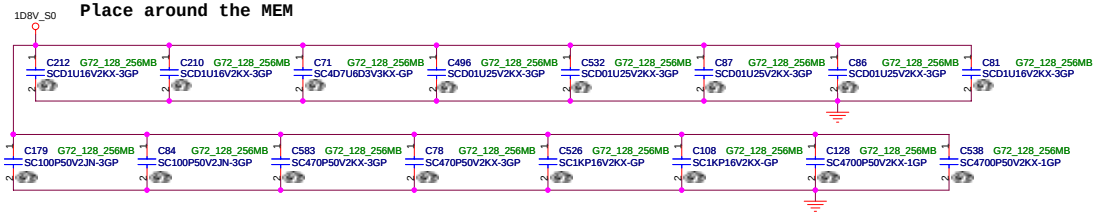




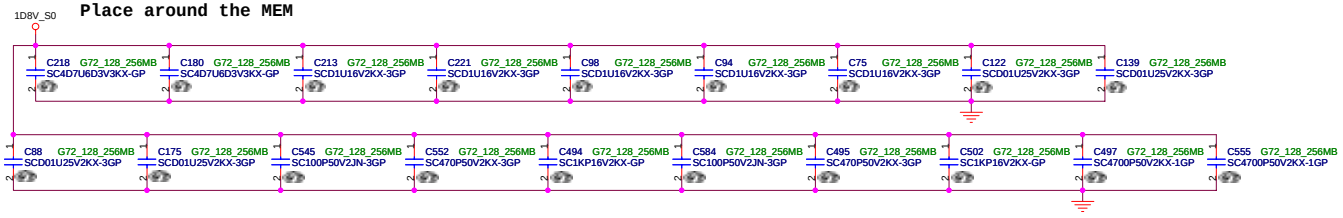
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	G72M VRAM (1ST 1/2)	
Size	Document Number: MYALL2	Rev: MP
Date: Thursday, March 30, 2006	Sheet 49 of 57	



Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



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Title: G72M VRAM (1ST 2/2)

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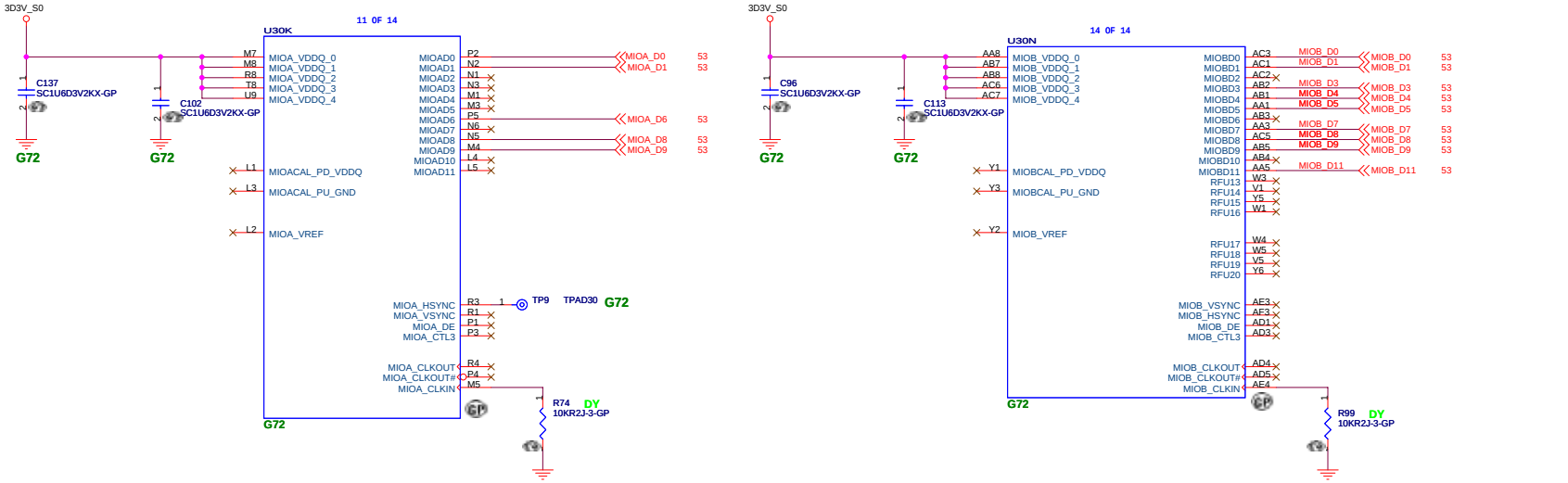
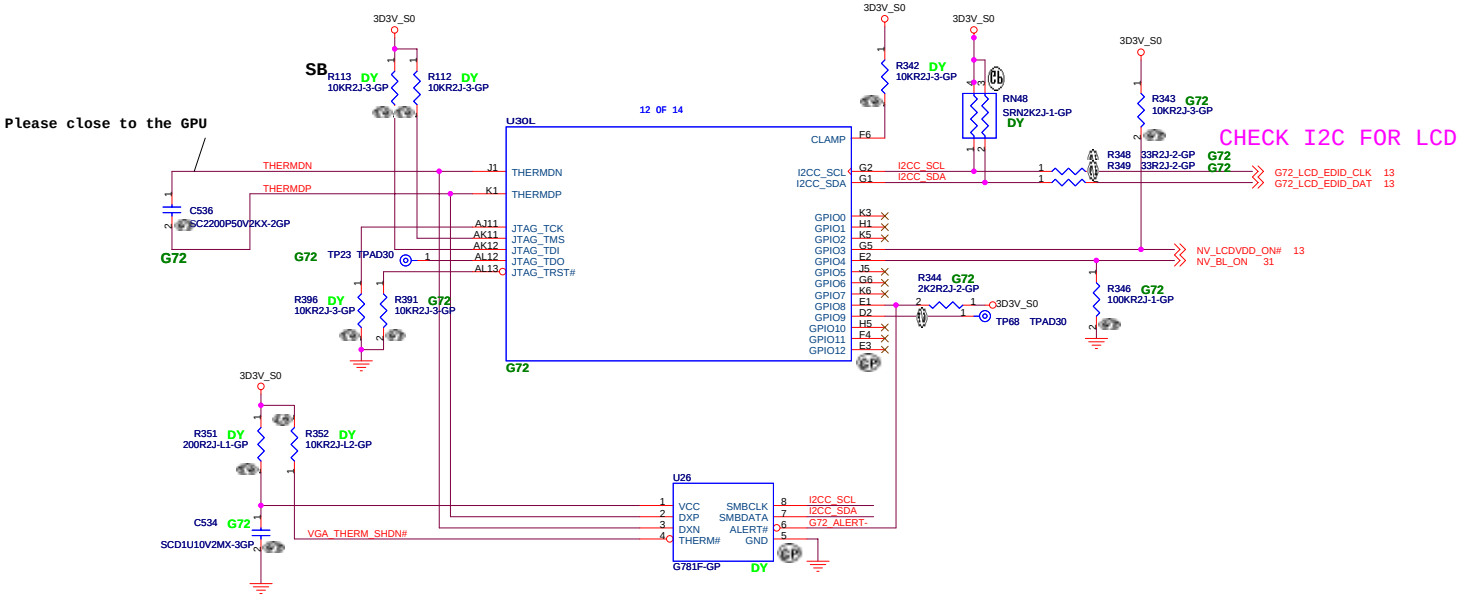
Date: Thursday, March 30, 2006 | Sheet 50 of 57





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Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M THERMAL

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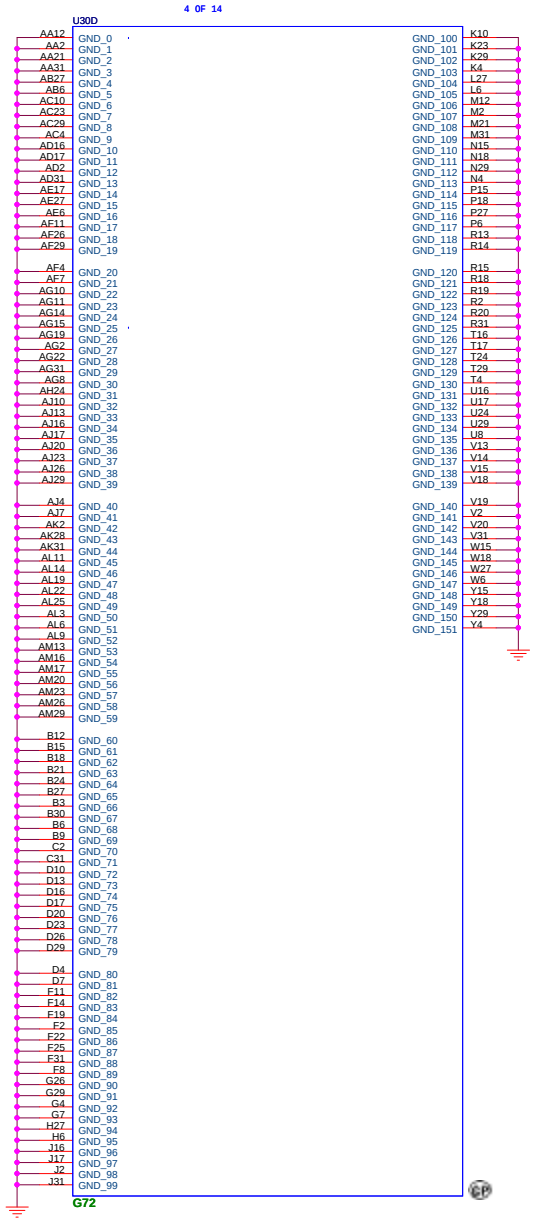

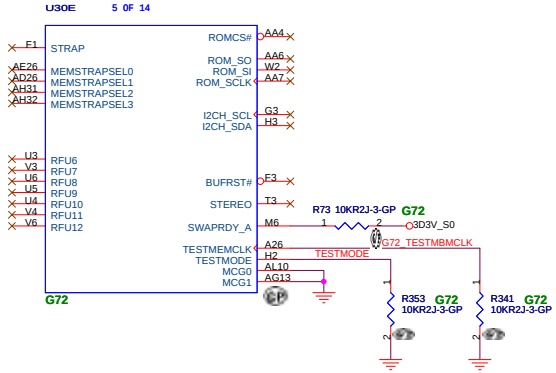

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*G72M ROM & Spread Specturm*	
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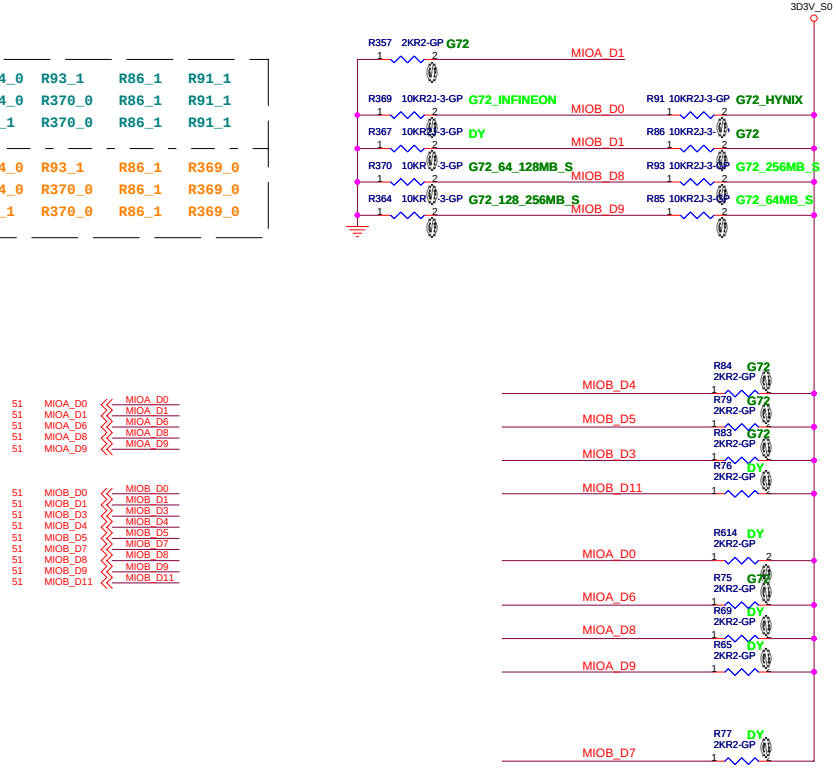
STRAPS, Mechanical Parts

Hynix256MB :	R364_0	R93_1	R86_1	R91_1
Hynix128MB :	R364_0	R370_0	R86_1	R91_1
Hynix64MB :	R85_1	R370_0	R86_1	R91_1
Infineon256MB :	R364_0	R93_1	R86_1	R369_0
Infineon128MB :	R364_0	R370_0	R86_1	R369_0
Infineon64MB :	R85_1	R370_0	R86_1	R369_0



Bit	Signal	Values	
MIOA_D1:	SUB_VENDOR	0 NO_BIOS 1 READ FROM BIOS	
MIOB_D0: MIOB_D1: MIOB_D8: MIOB_D9:	RAM_CFG_0 RAM_CFG_1 RAM_CFG_2 RAM_CFG_3	0000 RFU 0001 8Mx32 BGA 1.8V 0010 RFU 0011 RFU 0100 4Mx32 BGA 1.8V 0101 RFU 0110 RFU 0111 RFU 0011 16MX16	1000 RFU 1001 RFU 1010 RFU 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 RFU
MIOB_D2: MIOB_D6:	CRYSTAL_0 CRYSTAL_1	00 13.500 MHz 01 14.31818 MHz 10 27.000 MHz 11 UNKNOWN	
MIOA_D7: MIOA_D10:	TV_MODE_0 TV_MODE_1	00 SECAM 01 NTSC 10 PAL 11 CRT	
MIOB_D4: MIOB_D5: MIOB_D3: MIOB_D11:	PCI_DEVID_0 PCI_DEVID_1 PCI_DEVID_2 PCI_DEVID_3	1000 (default 0x00FC) 0111 G72MV	
MIOA_D0:	PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED	
MIOA_D6: MIOA_D8: MIOA_D9:	3GIO_PADCFG_LUT_ADDR[0] 3GIO_PADCFG_LUT_ADDR[1] 3GIO_PADCFG_LUT_ADDR[2]	0 DESKTOP 1 MOBILE 010 DEFAULT	
MIOB_D7:	MOBILE_GPIO	0 GPIO_PULLDN 1 GPIO_FLOAT	

For MEM strapping, Please use below table:

RAM_CFG[3:0]	Config	FB Bus Width	Definitions
0000	16Mx16 DDR2	64-bit	Elpida
0001	16Mx16 DDR2	64-bit	Samsung
0010	16Mx16 DDR2	64-bit	Infineon
0011	16Mx16 DDR2	64-bit	Hynix
0100	32Mx16 DDR2	64-bit	Elpida
0101	32Mx16 DDR2	64-bit	Samsung
0110	32Mx16 DDR2	64-bit	Infineon
0111	32Mx16 DDR2	64-bit	Hynix

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Title: G72M STRAPPING

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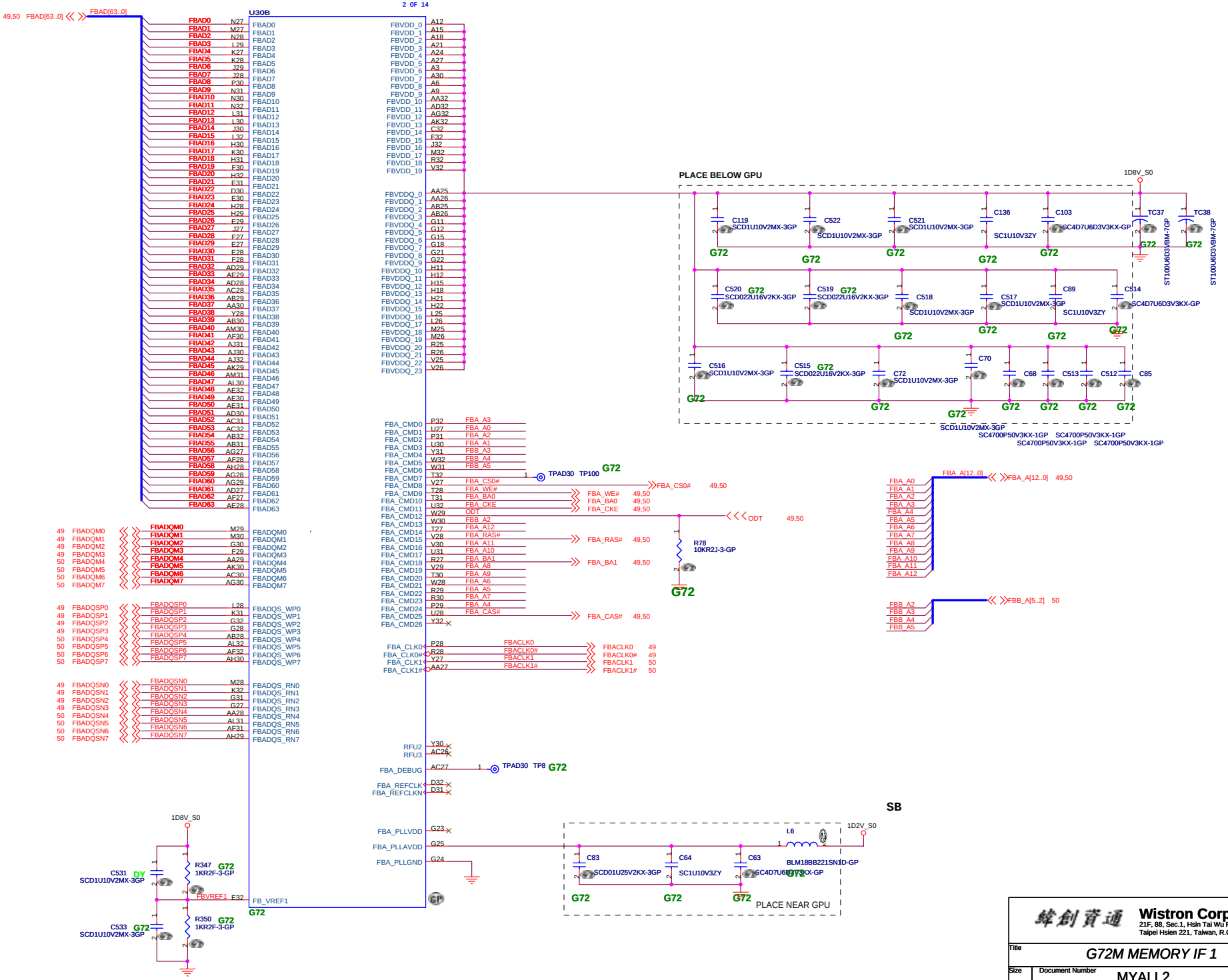
Date: Thursday, March 30, 2006 | Sheet 53 of 57



Company	Wistron Corporation
Address	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	G72M MEMORY IF 1
Size	
Document Number	MYALL2
Rev	MP
Date	Thursday, March 30, 2006
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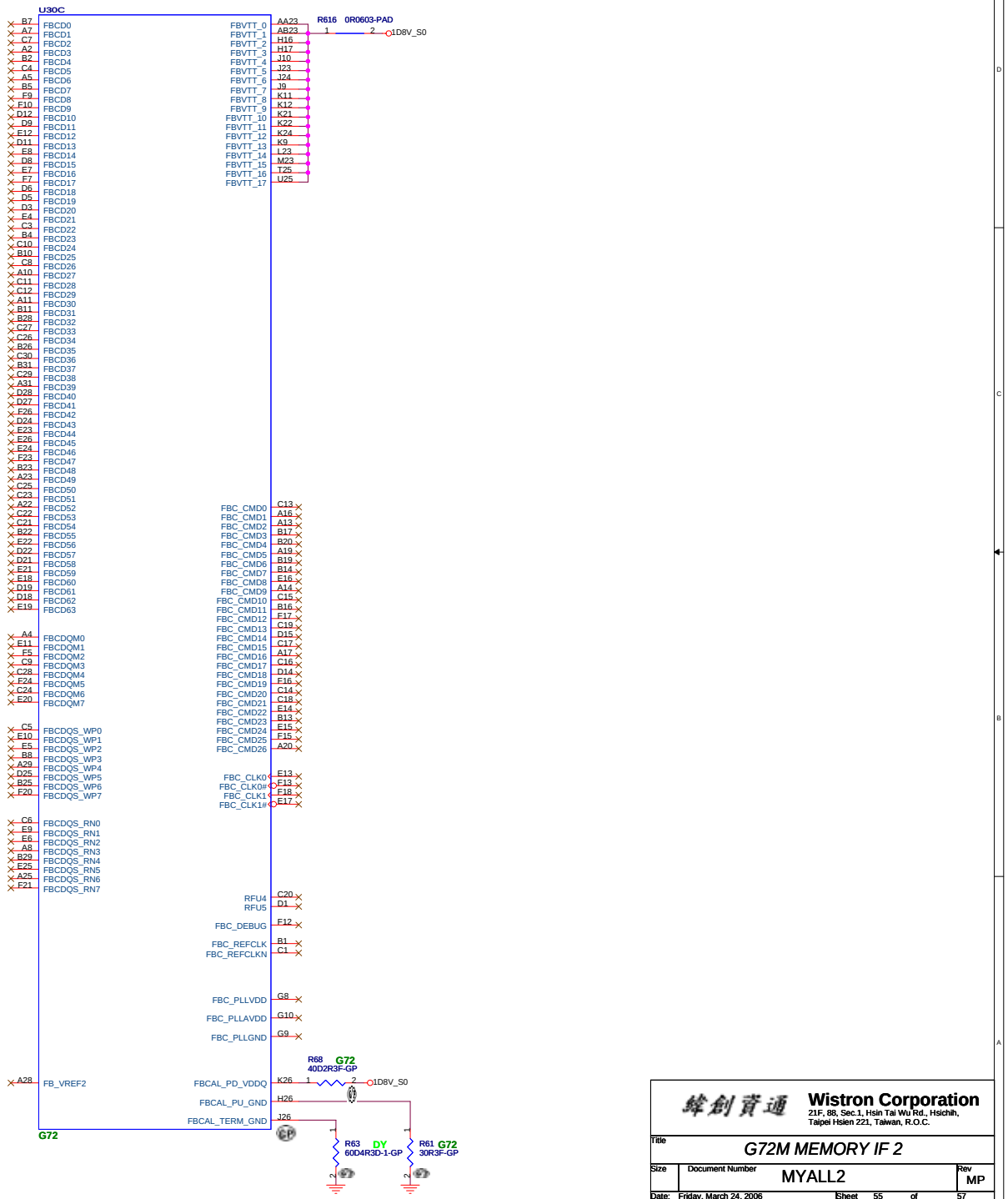

蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G72M MEMORY IF 2

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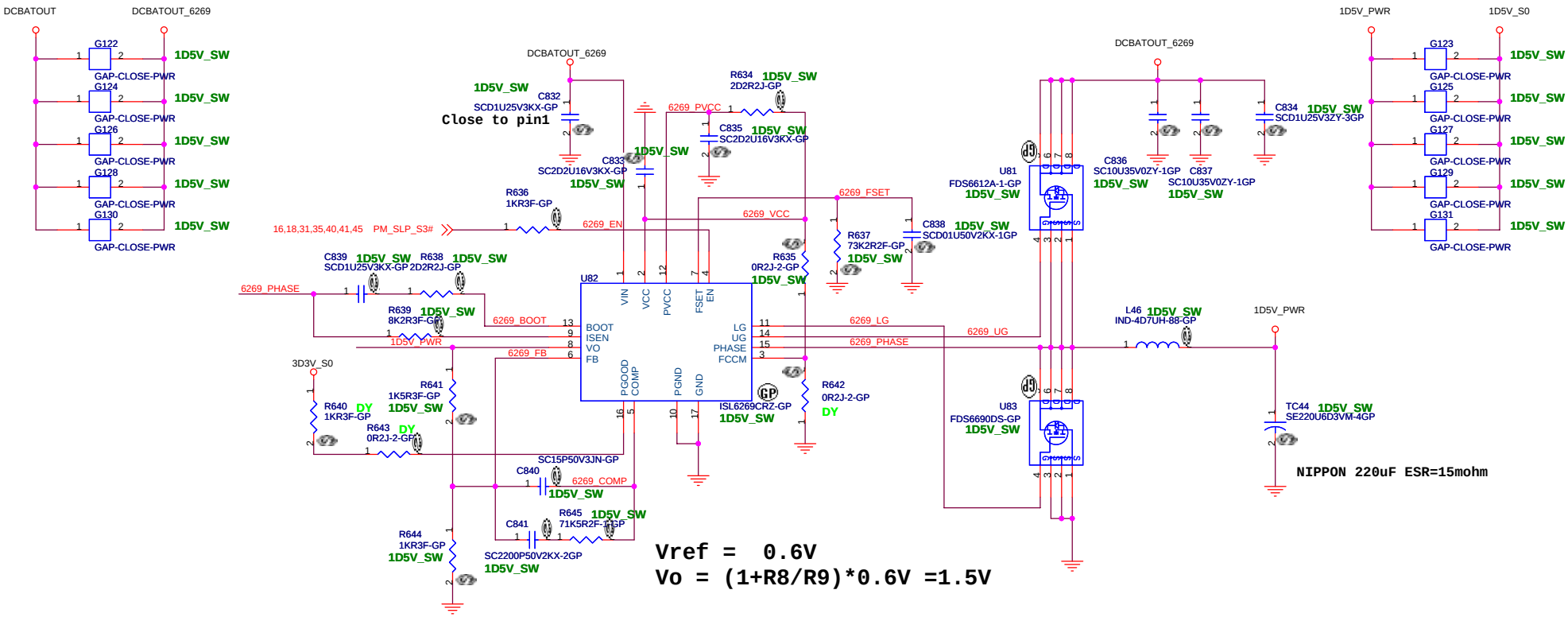

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*ISL6269/1D5V*	
Size: A3	Document Number: MYALL2	Rev: MP
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1. 5V_S5_G913 chnge to 5V_AUX_S5 ====> 1229
2. Bluetooth USB change to port 7 ====> 1229
3. Add CPU frequency selection resistor ====> 1229
4. Change LVDS connector ====> 1229
5. Change C435 from 1uF to 0.47uF and for pop noise ====> 1230
6. Change T7 and T8 from 68uF to 22uF for pop noise ====> 1230
7. Add 579 ~ R584 / Q35 and Q36 for pop noise ====> 1230
8. Power change 1D05V_S0 and 1D5V_S0 power source ====> 0102
9. Power change 5D_PWR and 3D3V_PWR power source ====> 0107
10. R427 DY for PCIE bus clock ====> 0107
11. Delete Q14 / R543 / R254 for boot up ====> 0107
12. Power change R505 from 3.01K to 3.24K ====> 0107
13. Power change R142 from 2.21K to 8.2K ====> 0107
14. Power change R122 from 56.2K to 73.2K ====> 0107
15. Change R68 from 37ohm to 40.2ohm and R61 from 37ohm to 30ohm ====> 0107
16. Delete R401 for UMA boot up short ====> 0107
17. ME change TVOUT1 material from 22.10021.F41 to 22.10021.H61 ====> 0107
18. R568 DY for CIR working ====> 0109
19. Swap CARD1 pin18 and pin19 ====> 0110
20. Power change C699 from 510P/50V to 470P/50V ====> 0111
21. Power change R397 and R399 from resister to gap-close ====> 0111
22. Remove R392 / R393 / C560 / R62 / R92 / R123 ====> 0111
23. Add R615 for G72 SS ====> 0111
24. Dummy G72 external thermal sensor U26 / R351 / R352 / C534 ====> 0111
25. Add G72 strapping MIOA_D0 R614 with dummy ====> 0111
26. EMI add capacitor EC66 ~ EC69 for 1000P/16V and EC70 ~ EC78 for 0.1U/16V ====> 0111
27. Power change R480 from 6.2K to 8.2K ====> 0112
28. Delete R533 and R534 for cardreader detect ====> 0112
29. Delete R210 for 1D5V_S0 power rail ====> 0112
30. Power delete R407 0 ohm ====> 0112
31. Add TC34 ~ TC38 for U39_G72 ====> 0112
32. Remove R362 ====> 0112
33. Change R282 and R283 from 22 ohm to 2.2K for internal mic record function failure ====> 0112
34. Change R306 / R308 / R313 / R311 from 47 ohm to 0 ohm for Hsync and Vsync input ====> 0112
35. Change R379 / R380 / R377 / R378 / R382 / R383 from 47 ohm to 0 ohm for TV input ====> 0112
36. Change CIR pull hi voltage from 5V to 3D3V ====> 0113
37. Delete G2 pad ====> 0113
38. Add GIGA LAN reset trace ====> 0113
39. Power change 1D5V power source ====> 0117
40. Power change NVVDD power source ====> 0117
41. Power add 1D5V power switching ====> 0117
42. Change C774 and C776 from 12pF to 15pF ====> 0119
43. Change C640 and C648 from 20pF to 27pF ====> 0119
44. Change C722 and C737 from 4.7pF to 2.7pF ====> 0119
45. Change C42 and C44 from 22pF to 18pF ====> 0119
46. Power delete R633 and pull hi voltage ====> 0119
47. Power delete TC39, TC43 and change TC41, TC42 to 79.33719.20C ====> 0120
48. Add CRT detect circuit ====> 0119
49. Change R594 pull hi voltage from 3D3V_S0 to 3D3V_S5 for S3 wake up issue ====> 0123
50. Power change material L44 and L46 from 68.3R310.20A to 68.4R710.20D
    L45 from 68.3R310.20A to 68.2R210.20B ====> 0123
51. Power change R480 from 8.2K to 12K ====> 0124
52. Power change capacitor material from 78.10699.42L to 78.10622.53L as C685 ~ C692 ====> 0125
53. Delete U57 / C671 /C675 / C656 / C663 / U8 / D12 / D13 / C306 / R218 / R219 for don't boot up with battery only ====> 0205
54. Change R59 from 100K to 8.2K and add R649 / R650 for don't boot up with battery only ====> 0205
55. Change TC7 / TC8 to C844 / C845 from 22U/6.3V to 10U/6.3V for headphone system resume have "BO" sound ====> 0208-PD
56. EMC change U1 and U7 materials from G528 / G546 to TPS2061 / TPS2062 ====> 0208-PD
57. Add R651 0 ohm for vendor test ====> 0208-PD
58. Add R652 0 ohm for camera voltage ====> 0209-PD
59. Add R653 / Q37 / Q38 for quick discharge of 5V_S0 / 3D3V_S0 / 1D8V_S0 ====> 0209-PD
60. Change DIMM connector from 62.10017.741(DM1)/62.10017.751(DM2) to 62.10017.691(DM1)/62.10017.A71(DM2) ====> 0209-PD
61. Change G72 DACB net of DACA_VDD / DACA_VREF / DACA_RSET to DACB_VDD / DACB_VREF / DACB_RSET ====> 0209-PD
62. Delete R230 and C317 for non-delay RSMRST# ====> 0210-PD
63. Stuff R285 for internal mic record issue ====> 0210-PD
64. Change C541 and C544 from 27pF to 22pF with 18pF ====> 0210-PD
65. Change HDD1/ODD1/TVOUT1/TVIN1/LOUT1 symbol ====> 0210-PD
66. Delete R330 for BAT_IN# double pull hi issue ====> 0213-PD
67. EMI add EC79 ~ EC87 for 1D8V_S3 and EC88 ~ EC90 for DDR_VREF_S0 ====> 0213-PD
68. Add U84/C846/R654/R655/R656/L47 for camera function ====> 0213-PD
69. EMI add spring GND1 ~ GND3 ====> 0213-PD
70. Change TVOUT1 symbol for don't display TV issue ====> 0214-PD
71. Power change C805 and C806 from 51120_GND to GND ====> 0220-PD
72. Change DC1material from 22.10037.C51(yellow power jack) to 22.10037.C61(blue power jack) ====> 0223-PD
73. Power change C466 from 0.1uF to 0.01uF for U19 burned issue ====> 0303-PD
74. Power change material U47 / U48 / U53 / U54 from 84.07807.F37 to 84.06690.F37
    U49 / U50 / U51 / U52 from 84.07805.A37 to 84.06676.A37 for burned issue ====> 0306-PD
75. Power change R523 / C738 from 3.57K / 5600pF to 4.42K / 47pF ====> 0306-MP
76. Charger change R19 from 15.8K to 130K ====> 0307-MP
77. Charger change R22 from 100K to 499K and add R657 124K / Q39 2N7002 for 6 cell 3.2A with 8 cell 3.8A issue ====> 0309-MP
78. Acer suggestion change JK1 AV-IN connector from 62.10059.011 to 20.90045.001 and delete R292 / R293 ====> 0315-MP
79. Change CRT1 / Q35 / Q36 footprint for SMT issue ====> 0317-MP
80. Change LED5 driver voltage from 5V_S0 to 3D3V_S0 for light leak issue ====> 0317-MP
81. Delete dual layout of dummy of of L47 / L28 / L33 / L39 / L15 / L18 ====> 0317-MP
82. Short 0 ohm with pad ====> 0320-MP
    S : R89 / R418 / R225 / R537 / R316 / R5 / R52 / R51 / R333 / R345 / R335 / R651 / R558 / R559 / R532 / R285 / R649 / R650 / R49 / R448 / R204 / R437 / R96 / R562 / R410 / R211 / R208 / R177 / R406 / R194 / R237 / R226 / R245 / R243 / R322 / R326 / R327 / R425 / R444 / R495 / R496 / R560 / R616
    P : R515 / R516 / R491 / R492 / R494 / R482 / R485 / R486 / R487 / R517 / R506 / R508 / R510 / R511 / R591 / R589 / R592 / R593 / R596 / R598 / R603 / R600 / R246 / R247 / R623 / R626 / R624 / R42
83. Power change materials for high frequency noise issue ====> 0324-MP
    A. add TC45 ~ TC50
    B. dummy C691 / C692 / C689 /C685 / C686 / C688
    C. delete C797 / C798 / C808 / C809
84. Power change material TC23 from 79.3371T.30L to 80.22716.L08 and L42 / L43 from 68.4R750.10Z to 68.4R71A.10P ====> 0324-MP
85. Change C29 material from 78.10491.4FL to 78.10520.5FL for hot plug don't boot up issue ====> 0328-MP
86. Change BOM level that add 1394 / TVIN / TVOUT / IR function ====> 0331-MP
87. ME change 1394 connector material from 62.10027.121 to 62.10027.561 for RoSH issue ====> 0331-MP

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *HISTORY*

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	MYALL2	MP

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