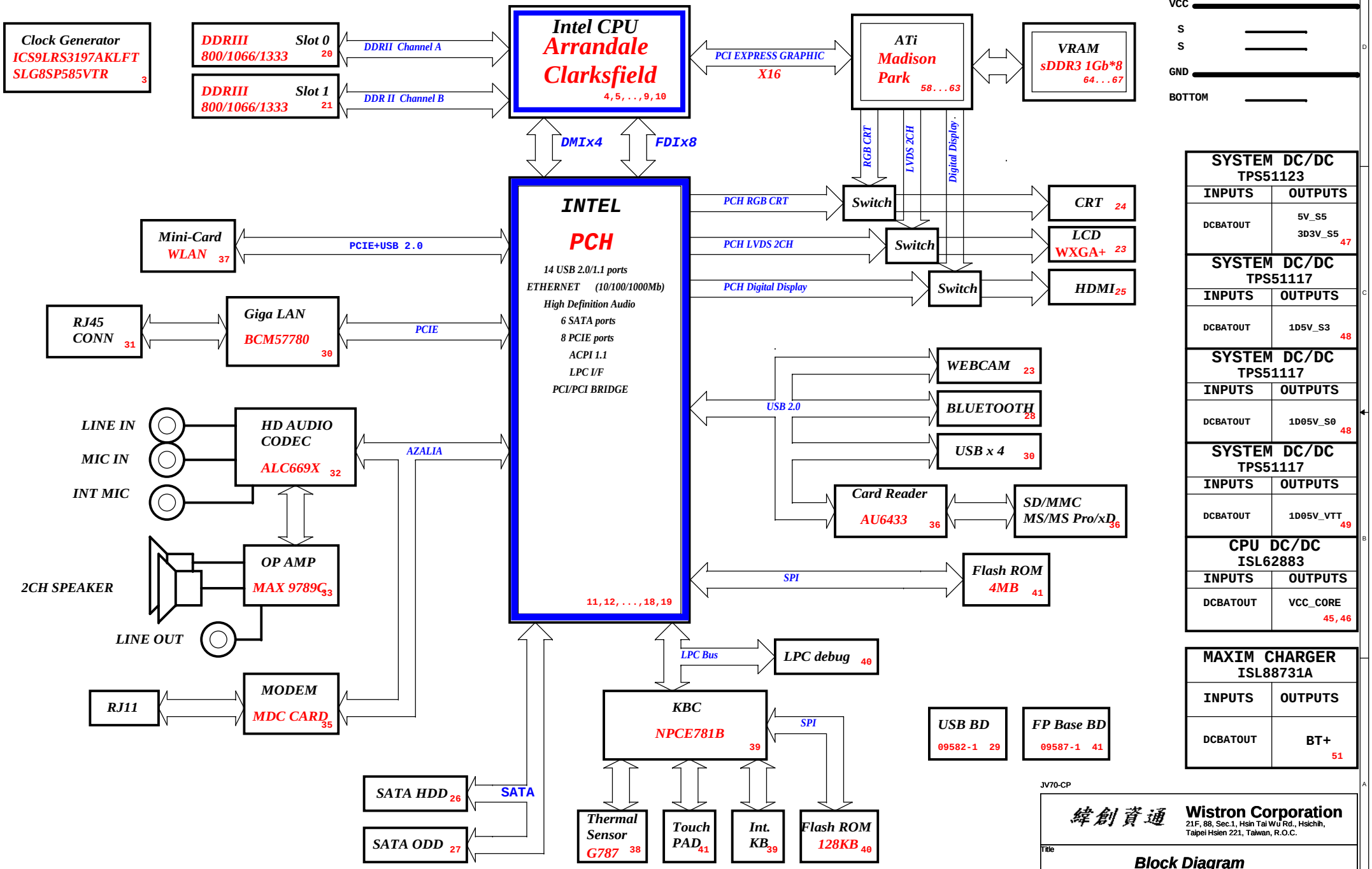
JV70-CP Block Diagram

Project code: 91.4GC01.001
PCB P/N : 48.4GC01.011
REVISION : 09293--1



PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC
TPS51123

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 47

SYSTEM DC/DC
TPS51117

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 48

SYSTEM DC/DC
TPS51117

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 48

SYSTEM DC/DC
TPS51117

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 49

CPU DC/DC
ISL62883

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 45,46

MAXIM CHARGER
ISL88731A

INPUTS	OUTPUTS
DCBATOUT	BT+ 51

JV70-CP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	**LAN**
LANE2	**MiniCard WLAN**

USB

Pair	*Device*
0	*USB1*
1	*USB2*
2	*USB4*
3	*MINICARD1*
4	*WECAM*
5	*NC*
6	*NC*
7	*NC*
8	*NC*
9	*USB3(HS)*
10	*Finger Print*
11	*Blue Tooth*
12	*NC*
13	*Cardreader*

JV70-CP

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Title: *Table of Content*

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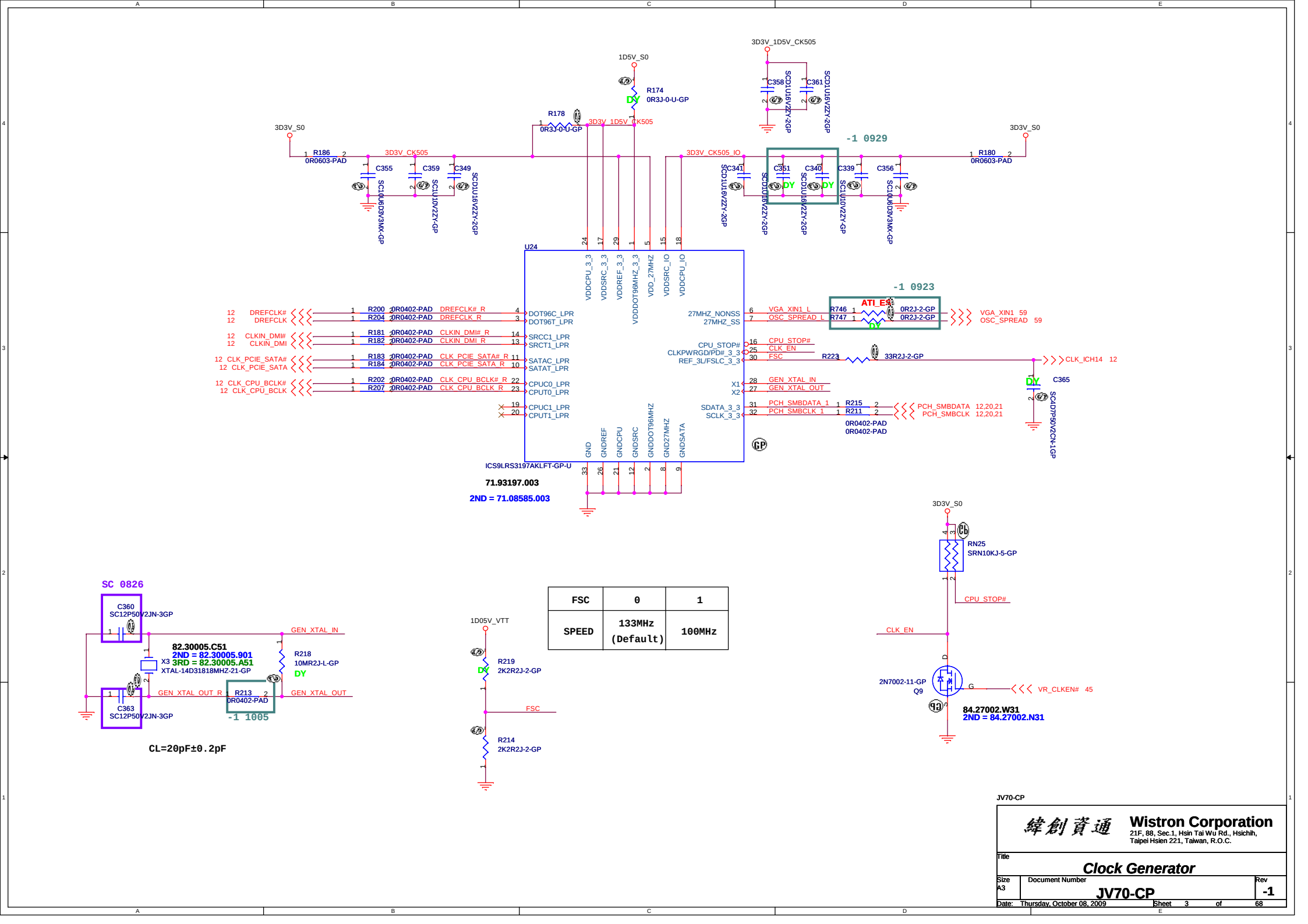

JV70-CP

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Title: Clock Generator

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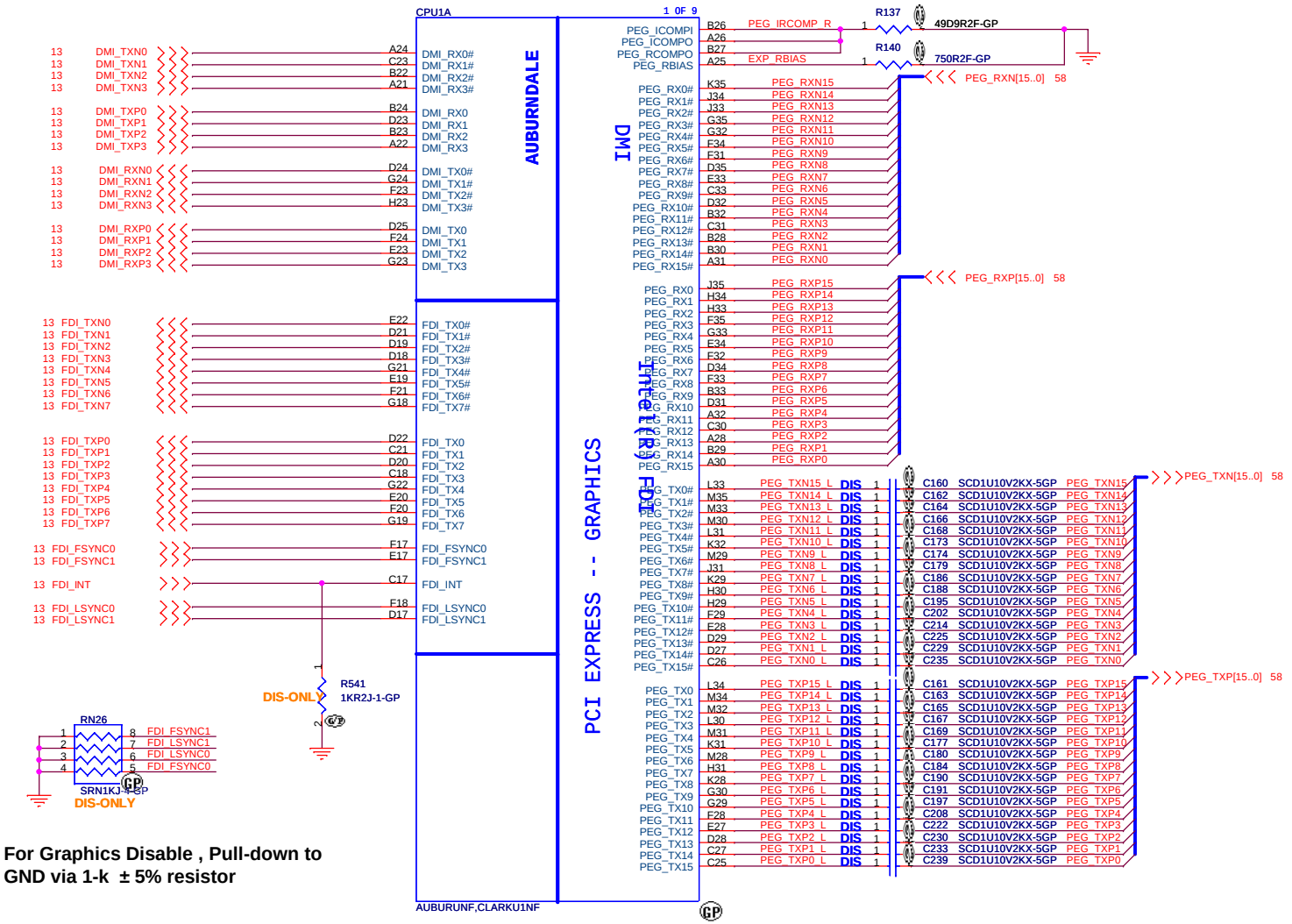

JV70-CP

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU (1/7)		
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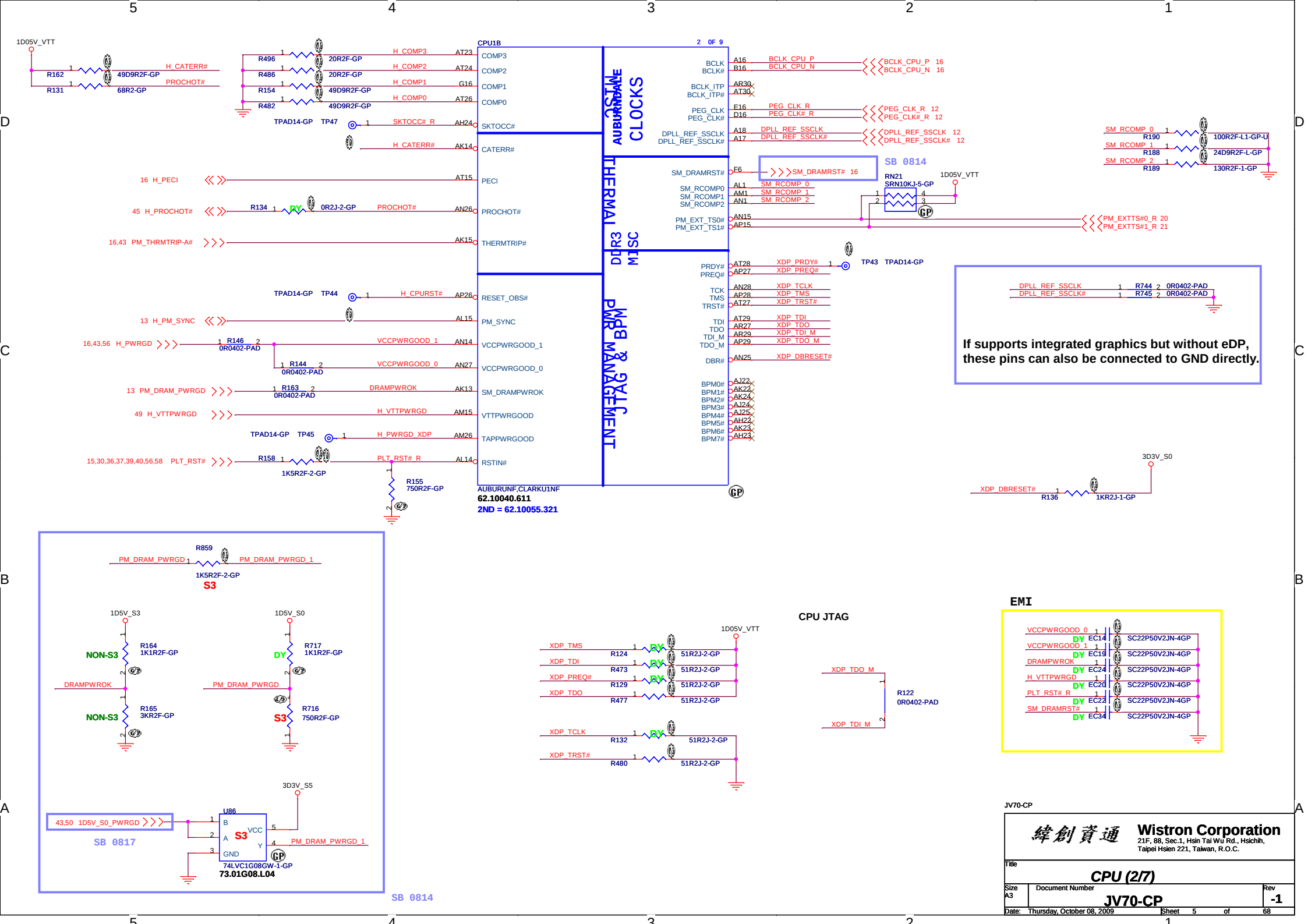
CPU1B
2 OF 9
AUBURNDALE
CLOCKS
THERMAL
DDR3
MISC
PWR MANAGEMENT
JTAG & BPM
COMP3
COMP2
COMP1
COMP0
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
RESET_OBS#
PM_SYNC
VCCPWRGOOD_1
VCCPWRGOOD_0
SM_DRAMPWROK
VTTPWRGOOD
TAPPWRGOOD
RSTIN#
BCLK
BCLK#
BCLK_ITP
BCLK_ITP#
PEG_CLK
PEG_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
SM_DRAMRST#
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
PM_EXT_TS0#
PM_EXT_TS1#
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
TDI_M
TDO_M
DBR#
BPM0#
BPM1#
BPM2#
BPM3#
BPM4#
BPM5#
BPM6#
BPM7#
AUBURUNF,CLARKU1NF
62.10040.611
2ND = 62.10055.321
1D05V_VTT
H_CATERR#
PROCHOT#
H_COMP3
H_COMP2
H_COMP1
H_COMP0
SKTOCC# R
16 H_PECI
45 H_PROCHOT#
16,43 PM_THRMTRIP-A#
TPAD14-GP TP47
TPAD14-GP TP44
TPAD14-GP TP45
13 H_PM_SYNC
16,43,56 H_PWRGD
13 PM_DRAM_PWRGD
49 H_VTTPWRGD
15,30,36,37,39,40,56,58 PLT_RST#
H_CPURST#
VCCPWRGOOD_1
VCCPWRGOOD_0
DRAMPWROK
H_VTTPWRGD
H_PWRGD_XDP
PLT_RST# R
SM_DRAMRST# 16
SB 0814
RN21
SRN10KJ-5-GP
PM_EXTTS#0_R 20
PM_EXTTS#1_R 21
TP43 TPAD14-GP
XDP_PRDY#
XDP_PREQ#
XDP_TCLK
XDP_TMS
XDP_TRST#
XDP_TDI
XDP_TDO
XDP_TDI_M
XDP_TDO_M
XDP_DBRESET#
SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
If supports integrated graphics but without eDP, these pins can also be connected to GND directly.
3D3V_S0
PM_DRAM_PWRGD
PM_DRAM_PWRGD_1
S3
1D5V_S3
1D5V_S0
NON-S3
DY
3D3V_S5
43,50 1D5V_S0_PWRGD
SB 0817
74LVC1G08GW-1-GP
73.01G08.L04
SB 0814
CPU JTAG
EMI
VCCPWRGOOD_0
VCCPWRGOOD_1
DRAMPWROK
H_VTTPWRGD
PLT_RST# R
SM_DRAMRST#
SC22P50V2JN-4GP
JV70-CP
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CPU (2/7)
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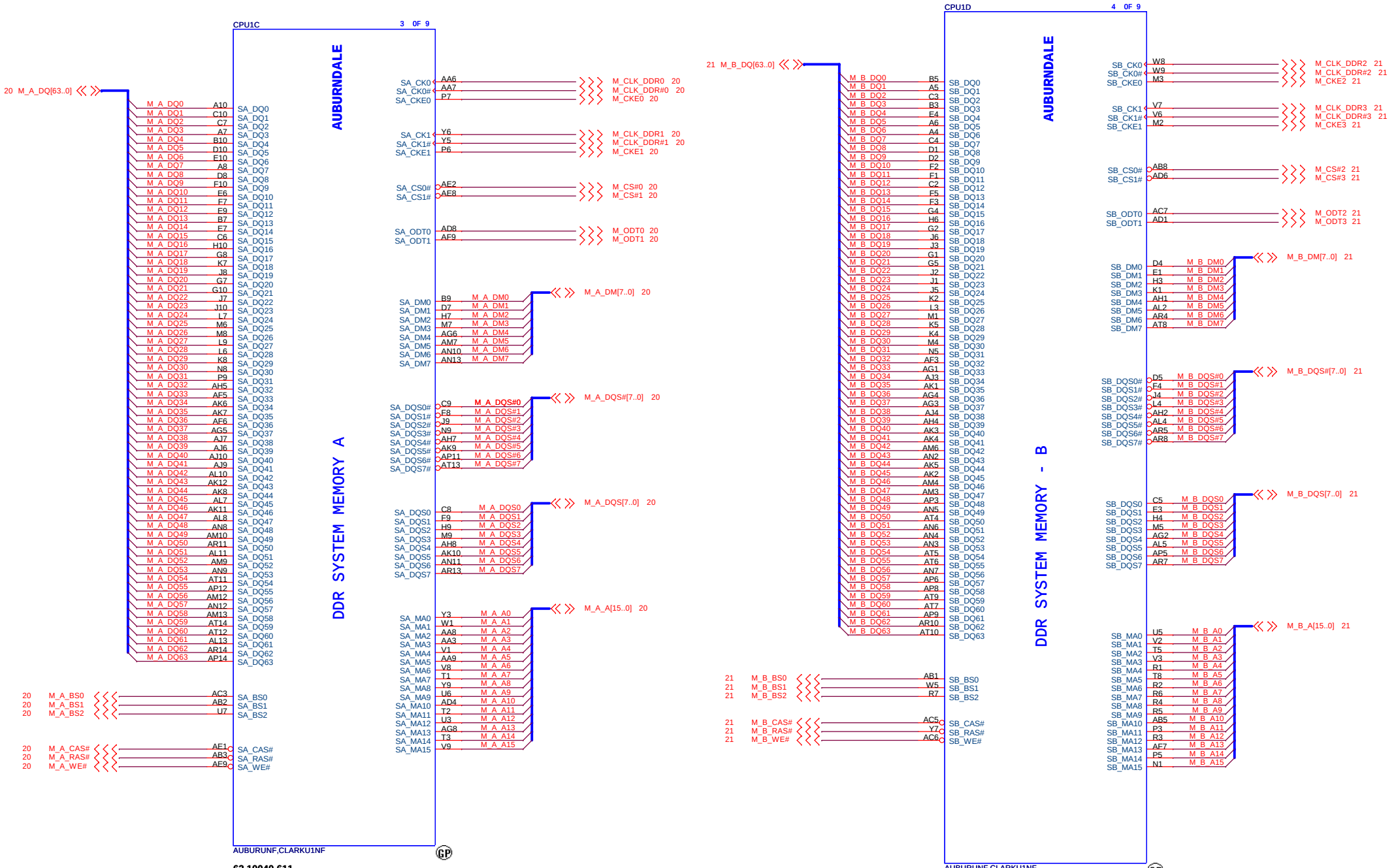
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3 0F 9
AUBURNDALE
DDR SYSTEM MEMORY A
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M_A_DQ0 A10 SA_DQ0
M_A_DQ1 C10 SA_DQ1
M_A_DQ2 C7 SA_DQ2
M_A_DQ3 A7 SA_DQ3
M_A_DQ4 B10 SA_DQ4
M_A_DQ5 D10 SA_DQ5
M_A_DQ6 E10 SA_DQ6
M_A_DQ7 A8 SA_DQ7
M_A_DQ8 D8 SA_DQ8
M_A_DQ9 F10 SA_DQ9
M_A_DQ10 E6 SA_DQ10
M_A_DQ11 F7 SA_DQ11
M_A_DQ12 E9 SA_DQ12
M_A_DQ13 B7 SA_DQ13
M_A_DQ14 E7 SA_DQ14
M_A_DQ15 C6 SA_DQ15
M_A_DQ16 H10 SA_DQ16
M_A_DQ17 G8 SA_DQ17
M_A_DQ18 K7 SA_DQ18
M_A_DQ19 J8 SA_DQ19
M_A_DQ20 G7 SA_DQ20
M_A_DQ21 G10 SA_DQ21
M_A_DQ22 J7 SA_DQ22
M_A_DQ23 J10 SA_DQ23
M_A_DQ24 L7 SA_DQ24
M_A_DQ25 M6 SA_DQ25
M_A_DQ26 M8 SA_DQ26
M_A_DQ27 L9 SA_DQ27
M_A_DQ28 L6 SA_DQ28
M_A_DQ29 K8 SA_DQ29
M_A_DQ30 N8 SA_DQ30
M_A_DQ31 P9 SA_DQ31
M_A_DQ32 AH5 SA_DQ32
M_A_DQ33 AF5 SA_DQ33
M_A_DQ34 AK6 SA_DQ34
M_A_DQ35 AK7 SA_DQ35
M_A_DQ36 AF6 SA_DQ36
M_A_DQ37 AG5 SA_DQ37
M_A_DQ38 AJ7 SA_DQ38
M_A_DQ39 AJ6 SA_DQ39
M_A_DQ40 AJ10 SA_DQ40
M_A_DQ41 AJ9 SA_DQ41
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M_A_DQ47 AL8 SA_DQ47
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M_A_DQ49 AM10 SA_DQ49
M_A_DQ50 AR11 SA_DQ50
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M_A_DQ52 AM9 SA_DQ52
M_A_DQ53 AN9 SA_DQ53
M_A_DQ54 AT11 SA_DQ54
M_A_DQ55 AP12 SA_DQ55
M_A_DQ56 AM12 SA_DQ56
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M_A_DQ59 AT14 SA_DQ59
M_A_DQ60 AT12 SA_DQ60
M_A_DQ61 AL13 SA_DQ61
M_A_DQ62 AR14 SA_DQ62
M_A_DQ63 AP14 SA_DQ63
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20 M_A_BS1 AB2 SA_BS1
20 M_A_BS2 U7 SA_BS2
20 M_A_CAS# AE1 SA_CAS#
20 M_A_RAS# AB3 SA_RAS#
20 M_A_WE# AE9 SA_WE#
SA_CK0 AA6 M_CLK_DDR0 20
SA_CK0# AA7 M_CLK_DDR#0 20
SA_CKE0 P7 M_CKE0 20
SA_CK1 Y6 M_CLK_DDR1 20
SA_CK1# Y5 M_CLK_DDR#1 20
SA_CKE1 P6 M_CKE1 20
SA_CS0# AE2 M_CS#0 20
SA_CS1# AE8 M_CS#1 20
SA_ODT0 AD8 M_ODT0 20
SA_ODT1 AF9 M_ODT1 20
SA_DM0 B9 M_A_DM0
SA_DM1 D7 M_A_DM1
SA_DM2 H7 M_A_DM2
SA_DM3 M7 M_A_DM3
SA_DM4 AG6 M_A_DM4
SA_DM5 AM7 M_A_DM5
SA_DM6 AN10 M_A_DM6
SA_DM7 AN13 M_A_DM7
M_A_DM[7..0] 20
SA_DQS0# C9 M_A_DQS#0
SA_DQS1# F8 M_A_DQS#1
SA_DQS2# J9 M_A_DQS#2
SA_DQS3# N9 M_A_DQS#3
SA_DQS4# AH7 M_A_DQS#4
SA_DQS5# AK9 M_A_DQS#5
SA_DQS6# AP11 M_A_DQS#6
SA_DQS7# AT13 M_A_DQS#7
M_A_DQS#[7..0] 20
SA_DQS0 C8 M_A_DQS0
SA_DQS1 F9 M_A_DQS1
SA_DQS2 H9 M_A_DQS2
SA_DQS3 M9 M_A_DQS3
SA_DQS4 AH8 M_A_DQS4
SA_DQS5 AK10 M_A_DQS5
SA_DQS6 AN11 M_A_DQS6
SA_DQS7 AR13 M_A_DQS7
M_A_DQS[7..0] 20
SA_MA0 Y3 M_A_A0
SA_MA1 W1 M_A_A1
SA_MA2 AA8 M_A_A2
SA_MA3 AA3 M_A_A3
SA_MA4 V1 M_A_A4
SA_MA5 AA9 M_A_A5
SA_MA6 V8 M_A_A6
SA_MA7 T1 M_A_A7
SA_MA8 Y9 M_A_A8
SA_MA9 U6 M_A_A9
SA_MA10 AD4 M_A_A10
SA_MA11 T2 M_A_A11
SA_MA12 U3 M_A_A12
SA_MA13 AG8 M_A_A13
SA_MA14 T3 M_A_A14
SA_MA15 V9 M_A_A15
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AUBURNDALE
DDR SYSTEM MEMORY - B
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M_B_DQ0 B5 SB_DQ0
M_B_DQ1 A5 SB_DQ1
M_B_DQ2 C3 SB_DQ2
M_B_DQ3 B3 SB_DQ3
M_B_DQ4 E4 SB_DQ4
M_B_DQ5 A6 SB_DQ5
M_B_DQ6 A4 SB_DQ6
M_B_DQ7 C4 SB_DQ7
M_B_DQ8 D1 SB_DQ8
M_B_DQ9 D2 SB_DQ9
M_B_DQ10 F2 SB_DQ10
M_B_DQ11 F1 SB_DQ11
M_B_DQ12 C2 SB_DQ12
M_B_DQ13 E5 SB_DQ13
M_B_DQ14 F3 SB_DQ14
M_B_DQ15 G4 SB_DQ15
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M_B_DQ18 J6 SB_DQ18
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M_B_DQ21 G5 SB_DQ21
M_B_DQ22 J2 SB_DQ22
M_B_DQ23 J1 SB_DQ23
M_B_DQ24 J5 SB_DQ24
M_B_DQ25 K2 SB_DQ25
M_B_DQ26 L3 SB_DQ26
M_B_DQ27 M1 SB_DQ27
M_B_DQ28 K5 SB_DQ28
M_B_DQ29 K4 SB_DQ29
M_B_DQ30 M4 SB_DQ30
M_B_DQ31 N5 SB_DQ31
M_B_DQ32 AF3 SB_DQ32
M_B_DQ33 AG1 SB_DQ33
M_B_DQ34 AJ3 SB_DQ34
M_B_DQ35 AK1 SB_DQ35
M_B_DQ36 AG4 SB_DQ36
M_B_DQ37 AG3 SB_DQ37
M_B_DQ38 AJ4 SB_DQ38
M_B_DQ39 AH4 SB_DQ39
M_B_DQ40 AK3 SB_DQ40
M_B_DQ41 AK4 SB_DQ41
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M_B_DQ46 AM4 SB_DQ46
M_B_DQ47 AM3 SB_DQ47
M_B_DQ48 AP3 SB_DQ48
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M_B_DQ56 AN7 SB_DQ56
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M_B_DQ61 AP9 SB_DQ61
M_B_DQ62 AR10 SB_DQ62
M_B_DQ63 AT10 SB_DQ63
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21 M_B_BS1 W5 SB_BS1
21 M_B_BS2 R7 SB_BS2
21 M_B_CAS# AC5 SB_CAS#
21 M_B_RAS# Y7 SB_RAS#
21 M_B_WE# AC6 SB_WE#
SB_CK0 W8 M_CLK_DDR2 21
SB_CK0# W9 M_CLK_DDR#2 21
SB_CKE0 M3 M_CKE2 21
SB_CK1 V7 M_CLK_DDR3 21
SB_CK1# V6 M_CLK_DDR#3 21
SB_CKE1 M2 M_CKE3 21
SB_CS0# AB8 M_CS#2 21
SB_CS1# AD6 M_CS#3 21
SB_ODT0 AC7 M_ODT2 21
SB_ODT1 AD1 M_ODT3 21
SB_DM0 D4 M_B_DM0
SB_DM1 E1 M_B_DM1
SB_DM2 H3 M_B_DM2
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SB_DM7 AT8 M_B_DM7
M_B_DM[7..0] 21
SB_DQS0# D5 M_B_DQS#0
SB_DQS1# F4 M_B_DQS#1
SB_DQS2# J4 M_B_DQS#2
SB_DQS3# L4 M_B_DQS#3
SB_DQS4# AH2 M_B_DQS#4
SB_DQS5# AL4 M_B_DQS#5
SB_DQS6# AR5 M_B_DQS#6
SB_DQS7# AR8 M_B_DQS#7
M_B_DQS#[7..0] 21
SB_DQS0 C5 M_B_DQS0
SB_DQS1 E3 M_B_DQS1
SB_DQS2 H4 M_B_DQS2
SB_DQS3 M5 M_B_DQS3
SB_DQS4 AG2 M_B_DQS4
SB_DQS5 AL5 M_B_DQS5
SB_DQS6 AP5 M_B_DQS6
SB_DQS7 AR7 M_B_DQS7
M_B_DQS[7..0] 21
SB_MA0 U5 M_B_A0
SB_MA1 V2 M_B_A1
SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
SB_MA4 R1 M_B_A4
SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
SB_MA7 R6 M_B_A7
SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AE7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15
M_B_A[15..0] 21
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62.10040.611
2ND = 62.10055.321
JV70-CP
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (3/7)
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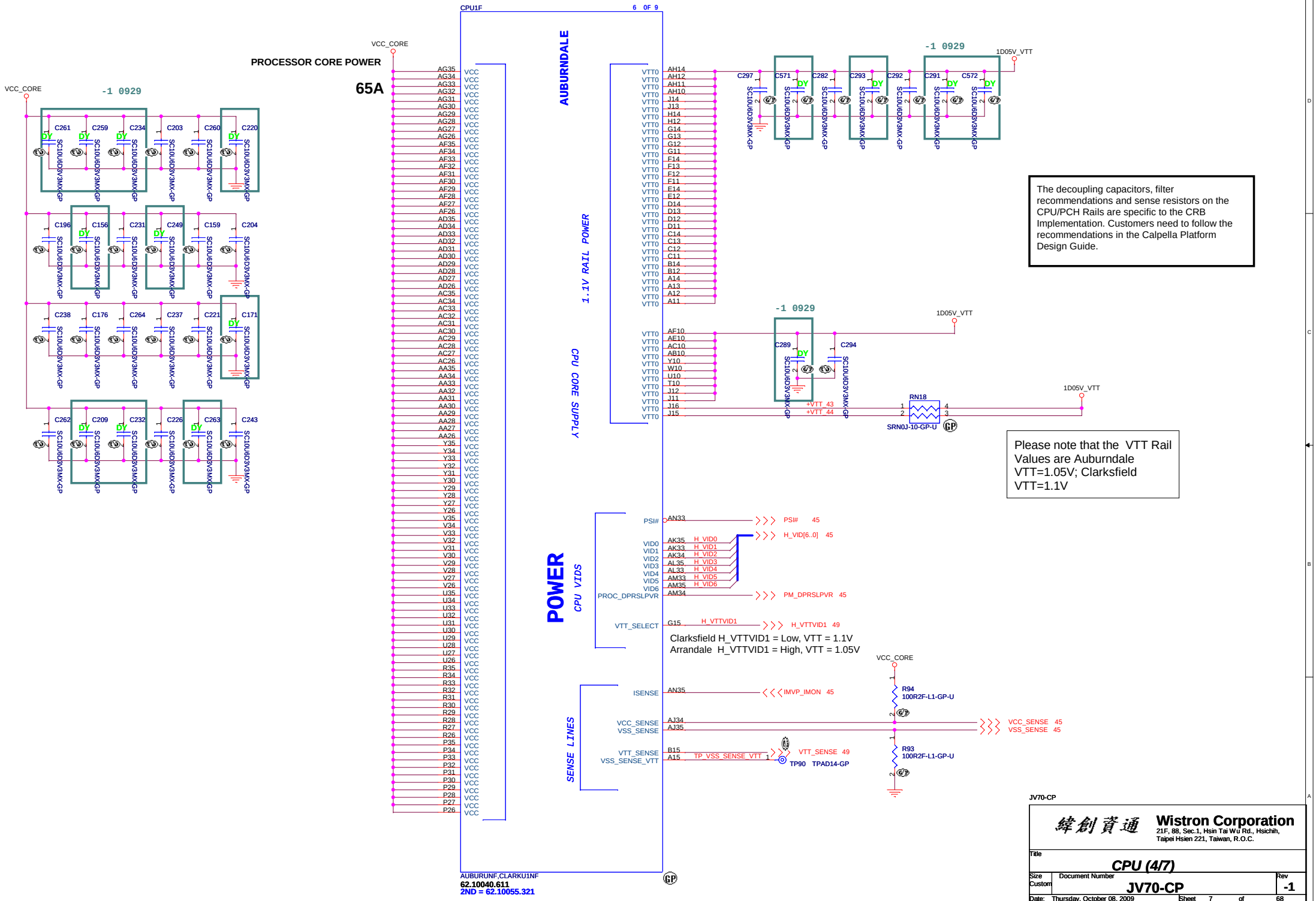
PROCESSOR CORE POWER
65A
VCC_CORE
-1 0929
CPU1F
6 0F 9
AUBURNDALE
1.1V RAIL POWER
CPU CORE SUPPLY
1D05V_VTT
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
POWER
CPU VIDS
SENSE LINES
PSI#
VID0
VID1
VID2
VID3
VID4
VID5
VID6
PROC_DPRSLPVR
VTT_SELECT
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
ISENSE
VCC_SENSE
VSS_SENSE
VTT_SENSE
VSS_SENSE_VTT
SRN0J-10-GP-U
TP90 TPAD14-GP
AUBURUNF,CLARKU1NF
62.10040.611
2ND = 62.10055.321
JV70-CP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (4/7)
Size Custom
Document Number
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Rev
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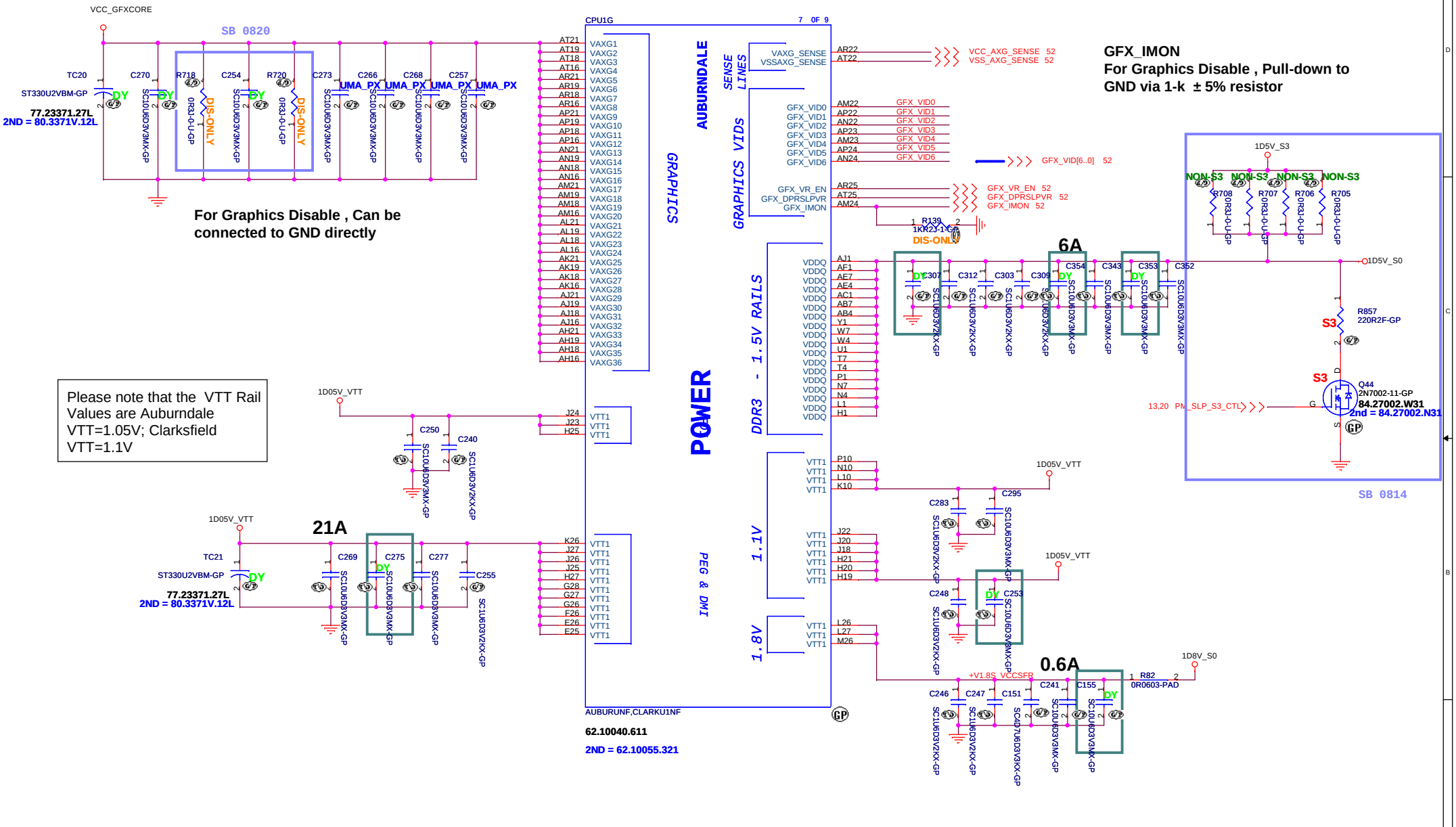

JV70-CP

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Title: **CPU (5/7)**

Size	Document Number	Rev
A3	JV70-CP	-1

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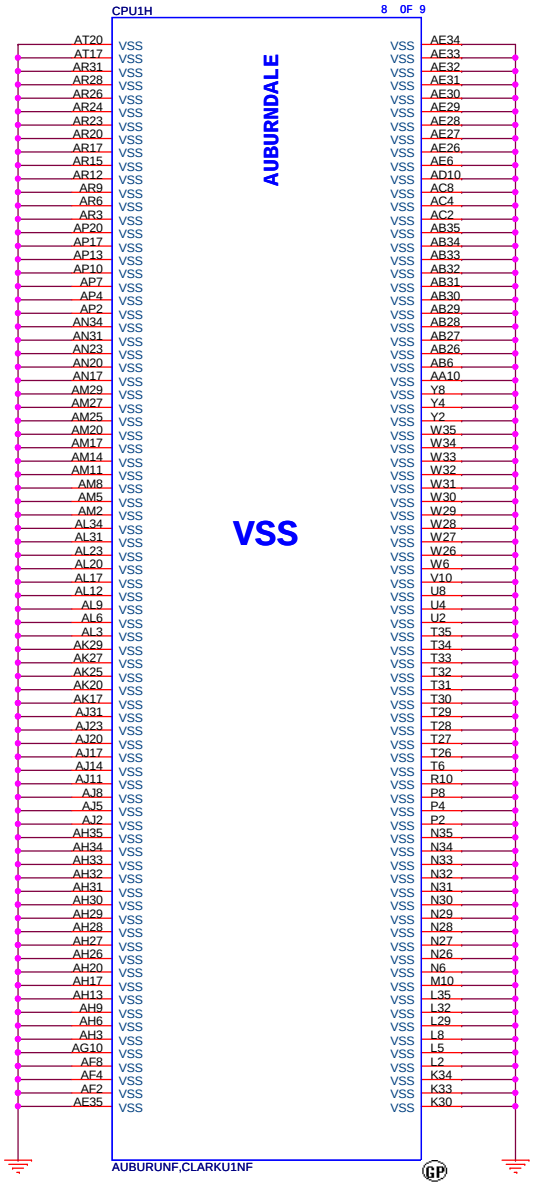
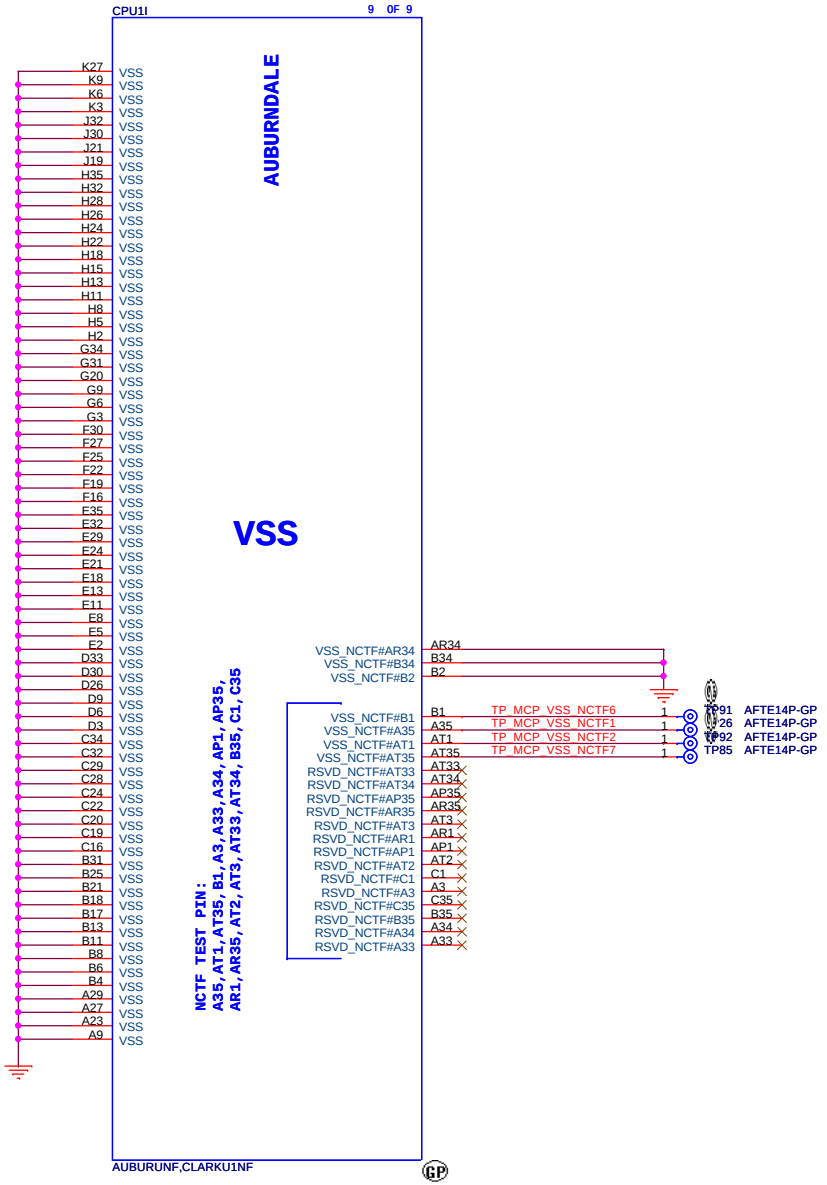


62.10040.611

2ND = 62.10055.321



62.10040.611

2ND = 62.10055.321

JV70-CP

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Title: CPU (6/7)

Size: A3 | Document Number: JV70-CP | Rev: -1

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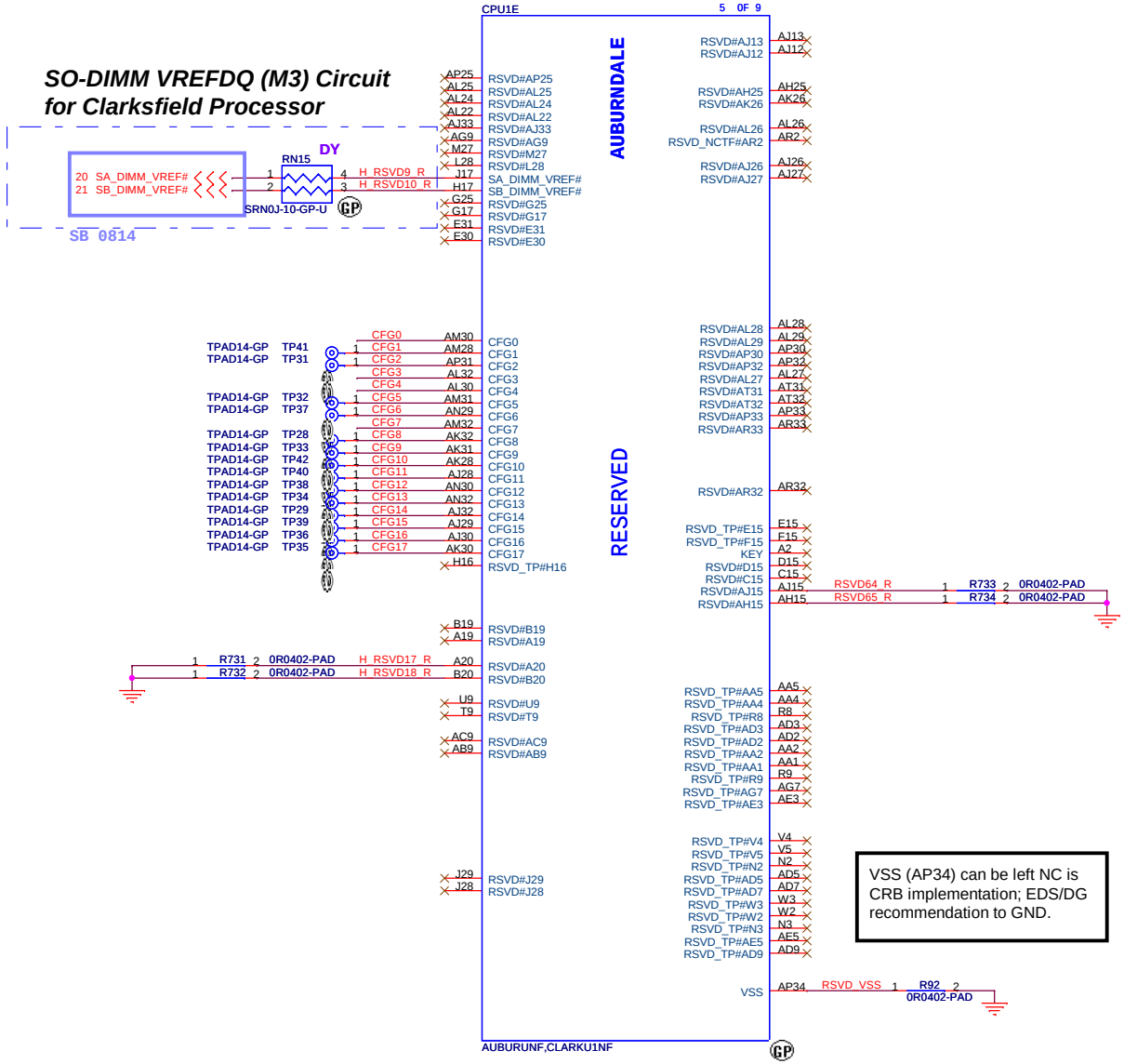
SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



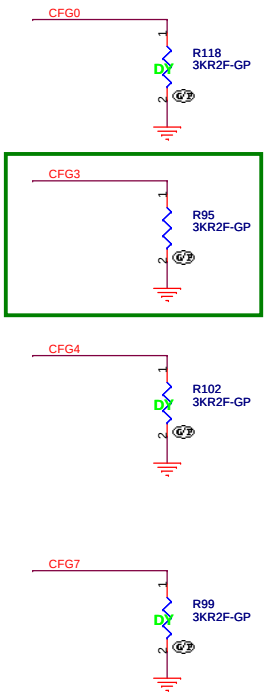
VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

62.10040.611

BOM change to 62.10055.321

2ND = 62.10053.561

3RD = 62.10055.341



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

JV70-CP

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Title: **CPU (7/7)**

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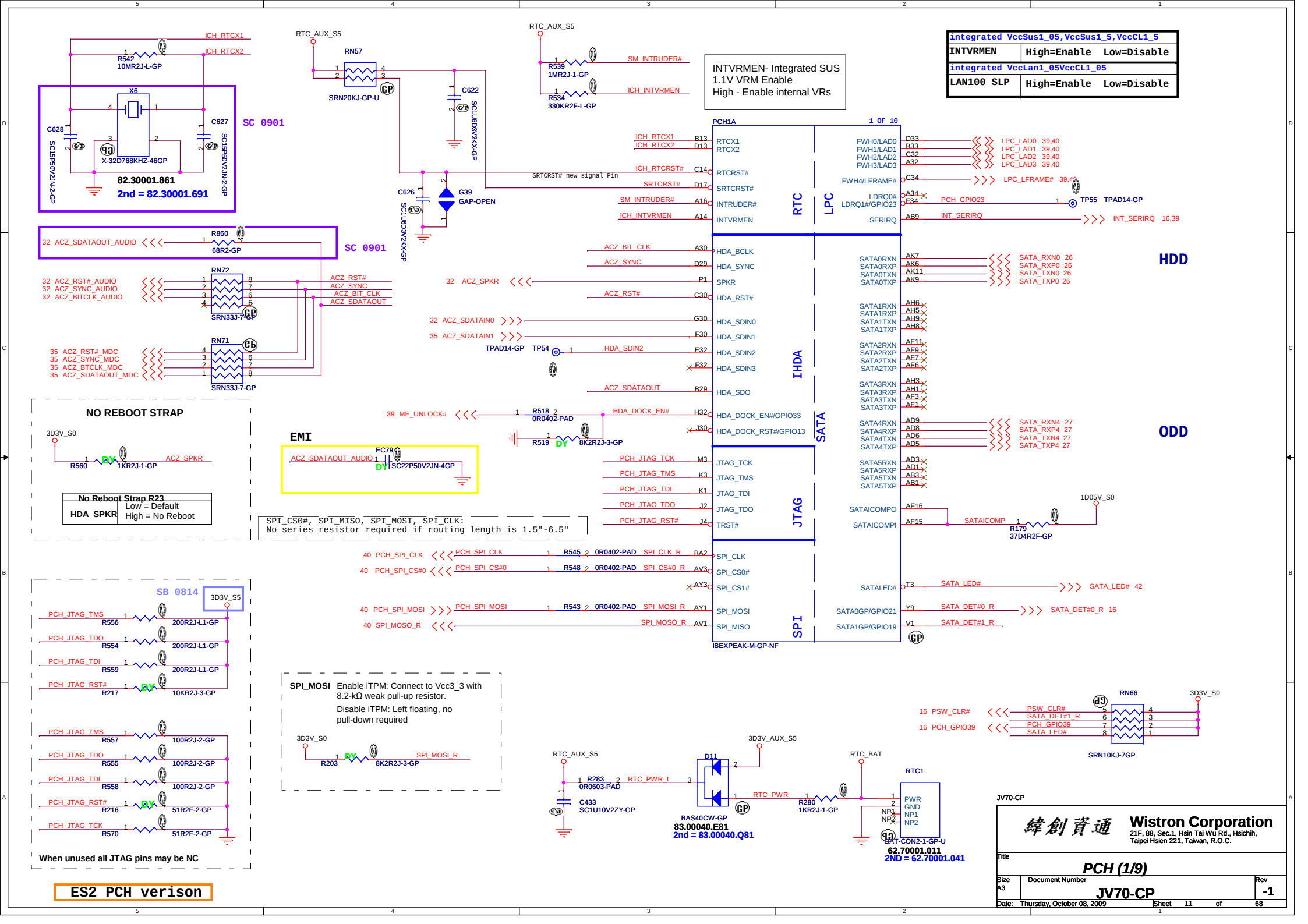
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
PCH1A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
HDD
ODD
SC 0901
82.30001.861
2nd = 82.30001.691
NO REBOOT STRAP
No Reboot Strap R23
HDA_SPKR Low = Default High = No Reboot
EMI
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"
SB 0814
When unused all JTAG pins may be NC
SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
IBEXPEAK-M-GP-NF
83.00040.E81
2nd = 83.00040.Q81
62.70001.011
2ND = 62.70001.041
ES2 PCH verison
JV70-CP
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Title
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LAN

MINICARD1

PCH1B

2 OF 10

PCI-E*

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

SB 0813

DIS-ONLY

SC 0915

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Title: PCH (2/9)

Size: A3 | Document Number: JV70-CP | Rev: -1

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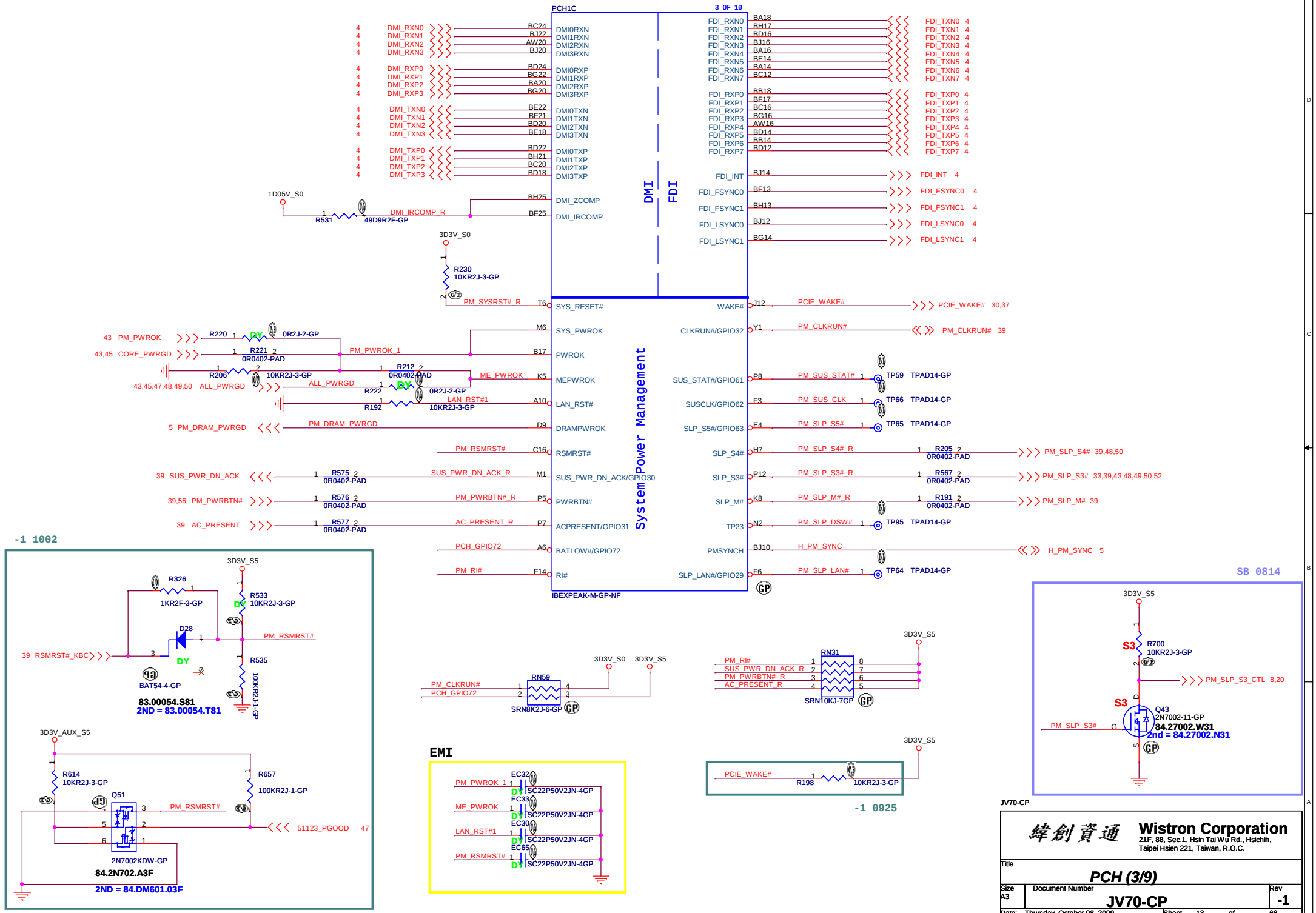

JV70-CP

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Title	PCH (3/9)
Size A3	Document Number JV70-CP
Rev	-1
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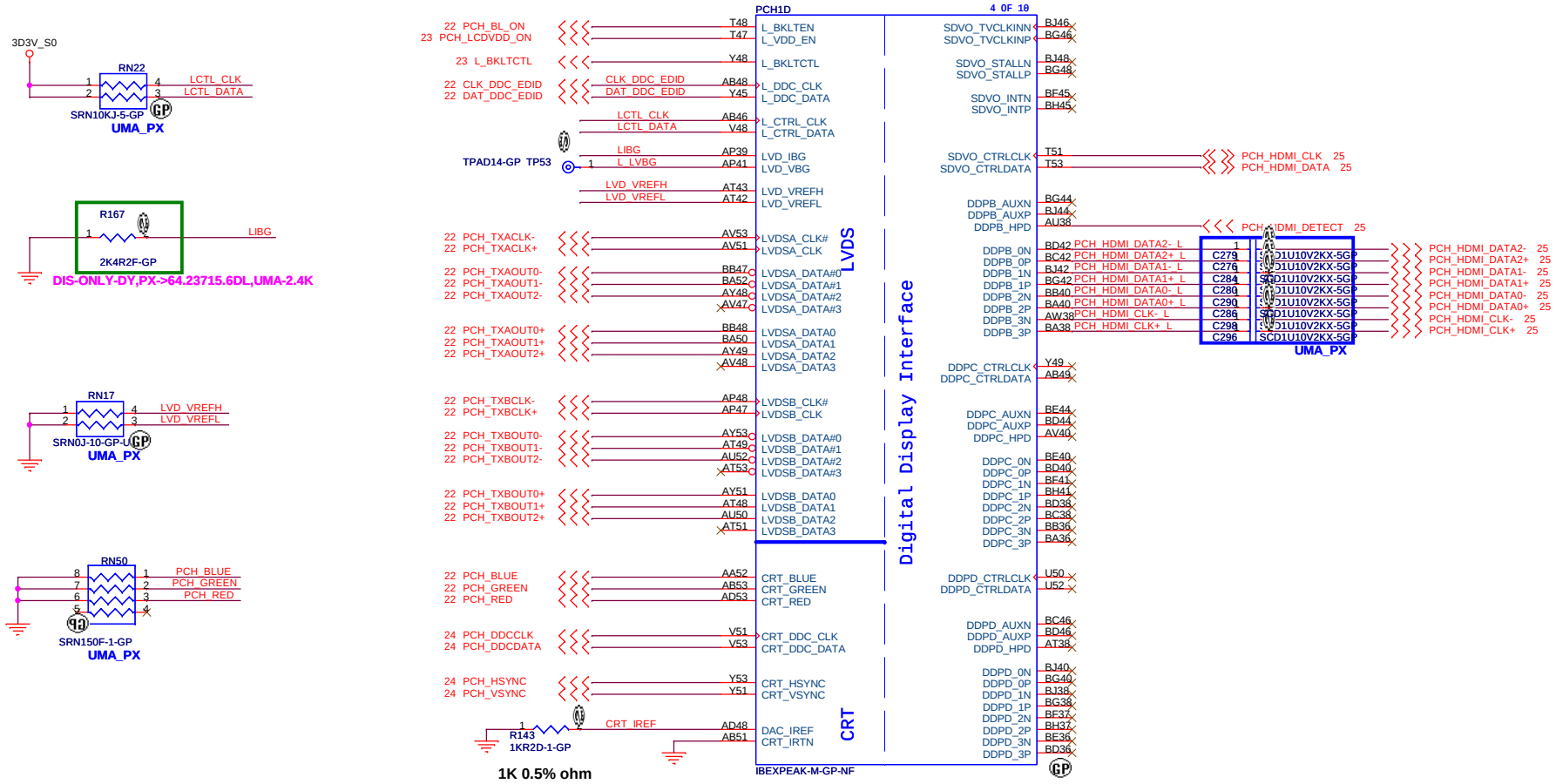

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Title: PCH (4/9)

Size	Document Number	Rev
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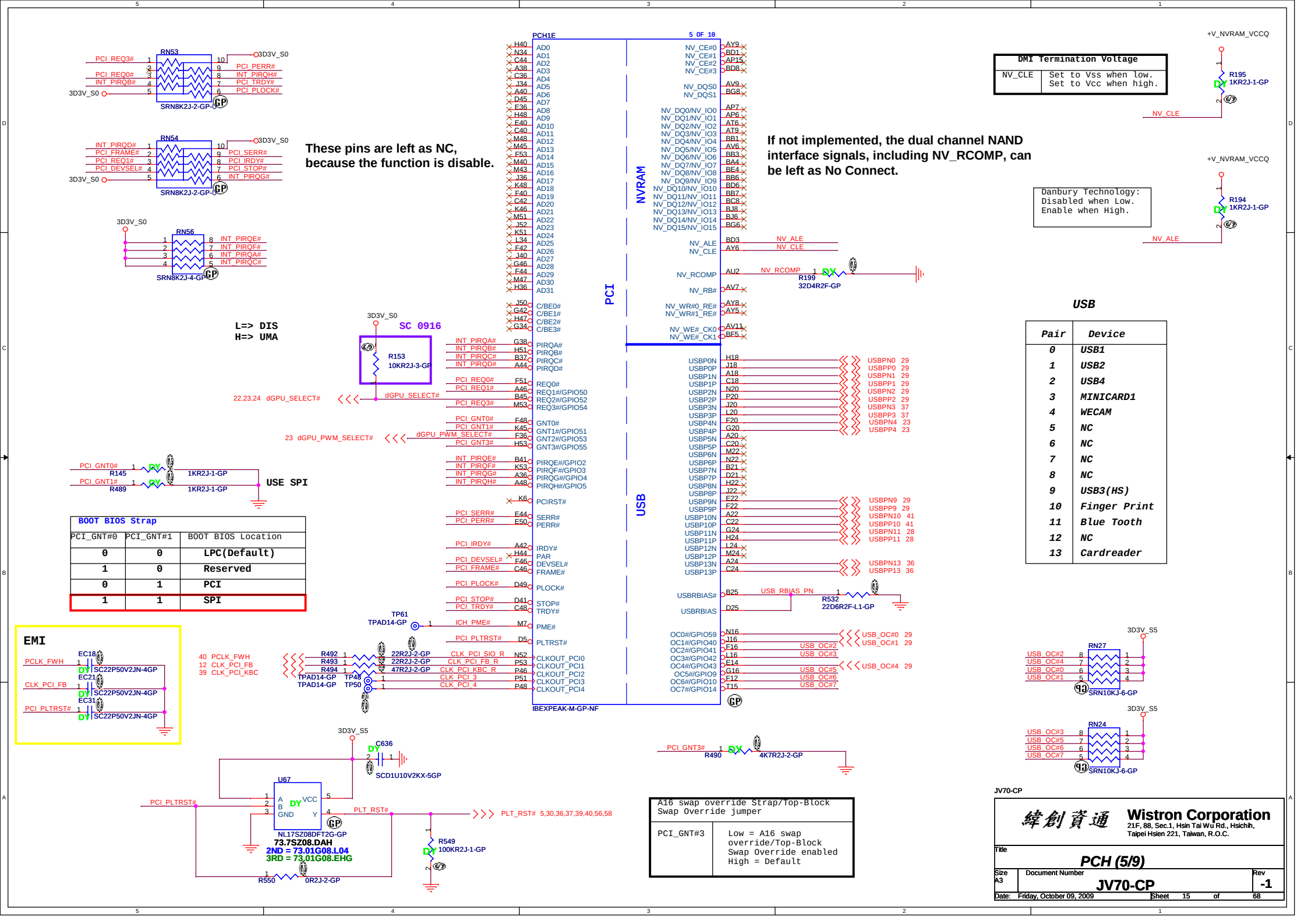
RN53
PCI_REQ3#
PCI_REQ0#
INT_PIRQB#
3D3V_S0
PCI_PERR#
INT_PIRQH#
PCI_TRDY#
PCI_PLOCK#
SRN8K2J-2-GP-U
RN54
INT_PIRQD#
PCI_FRAME#
PCI_REQ1#
PCI_DEVSEL#
PCI_SERR#
PCI_IRDY#
PCI_STOP#
INT_PIRQG#
SRN8K2J-2-GP-U
RN56
INT_PIRQE#
INT_PIRQF#
INT_PIRQA#
INT_PIRQC#
SRN8K2J-4-GP
These pins are left as NC, because the function is disable.
L=> DIS
H=> UMA
SC 0916
R153
10KR2J-3-GP
22,23,24 dGPU_SELECT#
dGPU_SELECT#
23 dGPU_PWM_SELECT#
dGPU_PWM_SELECT#
PCI_GNT0#
PCI_GNT1#
R145
R489
1KR2J-1-GP
USE SPI
BOOT BIOS Strap
PCI_GNT#0 | PCI_GNT#1 | BOOT BIOS Location
0 | 0 | LPC(Default)
1 | 0 | Reserved
0 | 1 | PCI
1 | 1 | SPI
EMI
EC18
EC21
EC31
SC22P50V2JN-4GP
PCLK_FWH
CLK_PCI_FB
PCI_PLTRST#
40 PCLK_FWH
12 CLK_PCI_FB
39 CLK_PCI_KBC
TP61
TPAD14-GP
ICH_PME#
R492
R493
R494
22R2J-2-GP
47R2J-2-GP
TP48
TP50
CLK_PCI_SIO_R
CLK_PCI_FB_R
CLK_PCI_KBC_R
CLK_PCI_3
CLK_PCI_4
PCH1E
PCI
NVRAM
USB
IBEXPEAK-M-GP-NF
5 OF 10
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
C/BE0#
C/BE1#
C/BE2#
C/BE3#
PIRQA#
PIRQB#
PIRQC#
PIRQD#
REQ0#
REQ1#/GPIO50
REQ2#/GPIO52
REQ3#/GPIO54
GNT0#
GNT1#/GPIO51
GNT2#/GPIO53
GNT3#/GPIO55
PIRQE#/GPIO2
PIRQF#/GPIO3
PIRQG#/GPIO4
PIRQH#/GPIO5
PCIRST#
SERR#
PERR#
IRDY#
PAR
DEVSEL#
FRAME#
PLOCK#
STOP#
TRDY#
PME#
PLTRST#
CLKOUT_PCI0
CLKOUT_PCI1
CLKOUT_PCI2
CLKOUT_PCI3
CLKOUT_PCI4
NV_CE#0
NV_CE#1
NV_CE#2
NV_CE#3
NV_DQS0
NV_DQS1
NV_DQ0/NV_IO0
NV_DQ1/NV_IO1
NV_DQ2/NV_IO2
NV_DQ3/NV_IO3
NV_DQ4/NV_IO4
NV_DQ5/NV_IO5
NV_DQ6/NV_IO6
NV_DQ7/NV_IO7
NV_DQ8/NV_IO8
NV_DQ9/NV_IO9
NV_DQ10/NV_IO10
NV_DQ11/NV_IO11
NV_DQ12/NV_IO12
NV_DQ13/NV_IO13
NV_DQ14/NV_IO14
NV_DQ15/NV_IO15
NV_ALE
NV_CLE
NV_RCOMP
NV_RB#
NV_WR#0_RE#
NV_WR#1_RE#
NV_WE#_CK0
NV_WE#_CK1
If not implemented, the dual channel NAND interface signals, including NV_RCOMP, can be left as No Connect.
R199
32D4R2F-GP
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P
USBP12N
USBP12P
USBP13N
USBP13P
USBRBIAS#
USBRBIAS
USB_RBIAS_PN
R532
22D6R2F-L1-GP
OC0#/GPIO59
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO9
OC6#/GPIO10
OC7#/GPIO14
USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
USB
Pair | Device
0 | USB1
1 | USB2
2 | USB4
3 | MINICARD1
4 | WECAM
5 | NC
6 | NC
7 | NC
8 | NC
9 | USB3(HS)
10 | Finger Print
11 | Blue Tooth
12 | NC
13 | Cardreader
DMI Termination Voltage
NV_CLE | Set to Vss when low. Set to Vcc when high.
+V_NVRAM_VCCQ
R195
1KR2J-1-GP
R194
1KR2J-1-GP
Danbury Technology:
Disabled when Low.
Enable when High.
RN27
RN24
SRN10KJ-6-GP
PCI_GNT3#
R490
4K7R2J-2-GP
C636
SCD1U10V2KX-5GP
U67
NL17SZ08DFT2G-GP
73.7SZ08.DAH
2ND = 73.01G08.L04
3RD = 73.01G08.EHG
PCI_PLTRST#
PLT_RST#
PLT_RST# 5,30,36,37,39,40,56,58
R549
100KR2J-1-GP
R550
0R2J-2-GP
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3
Low = A16 swap override/Top-Block Swap Override enabled
High = Default
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Wistron Corporation
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Title
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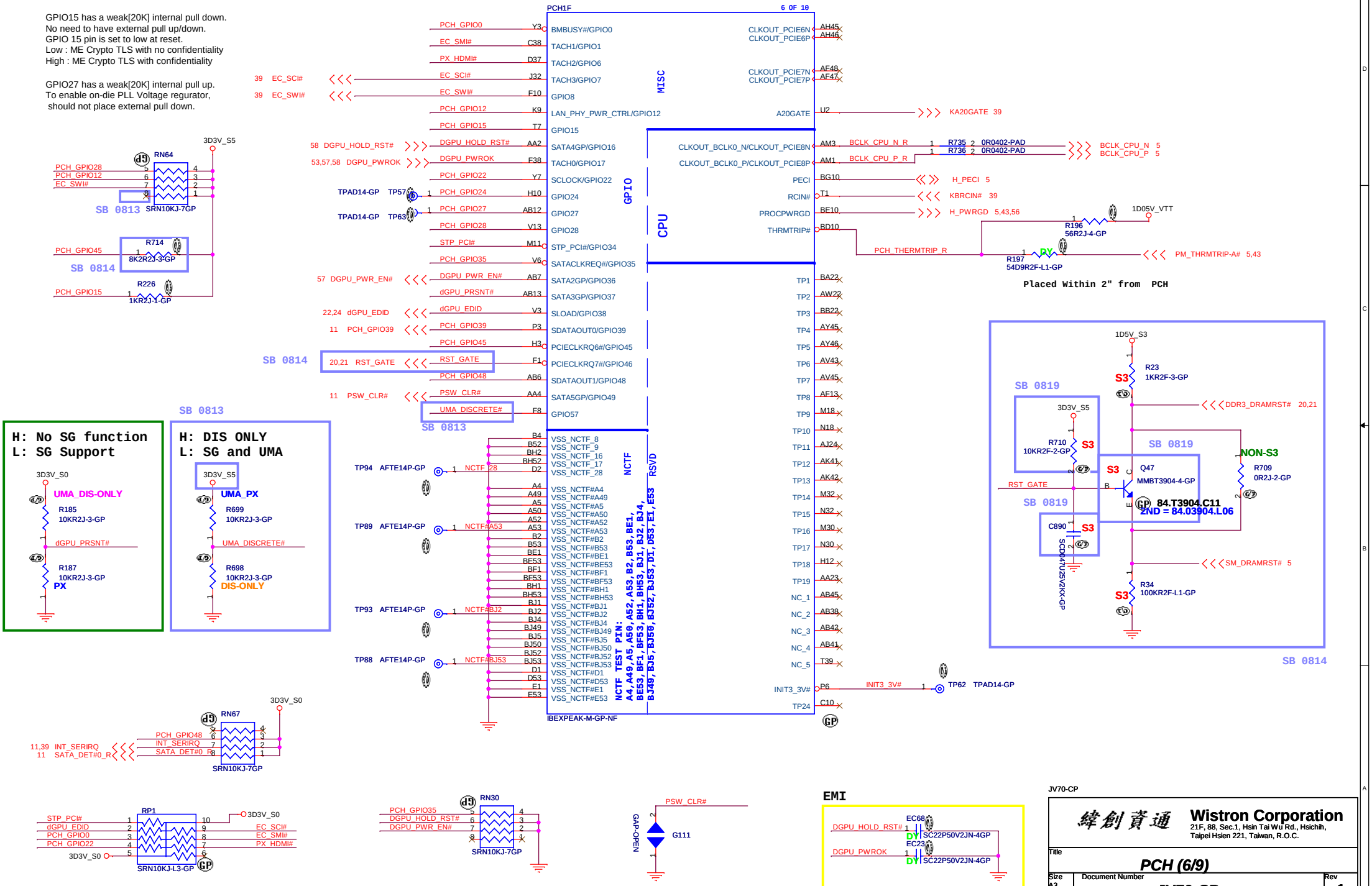
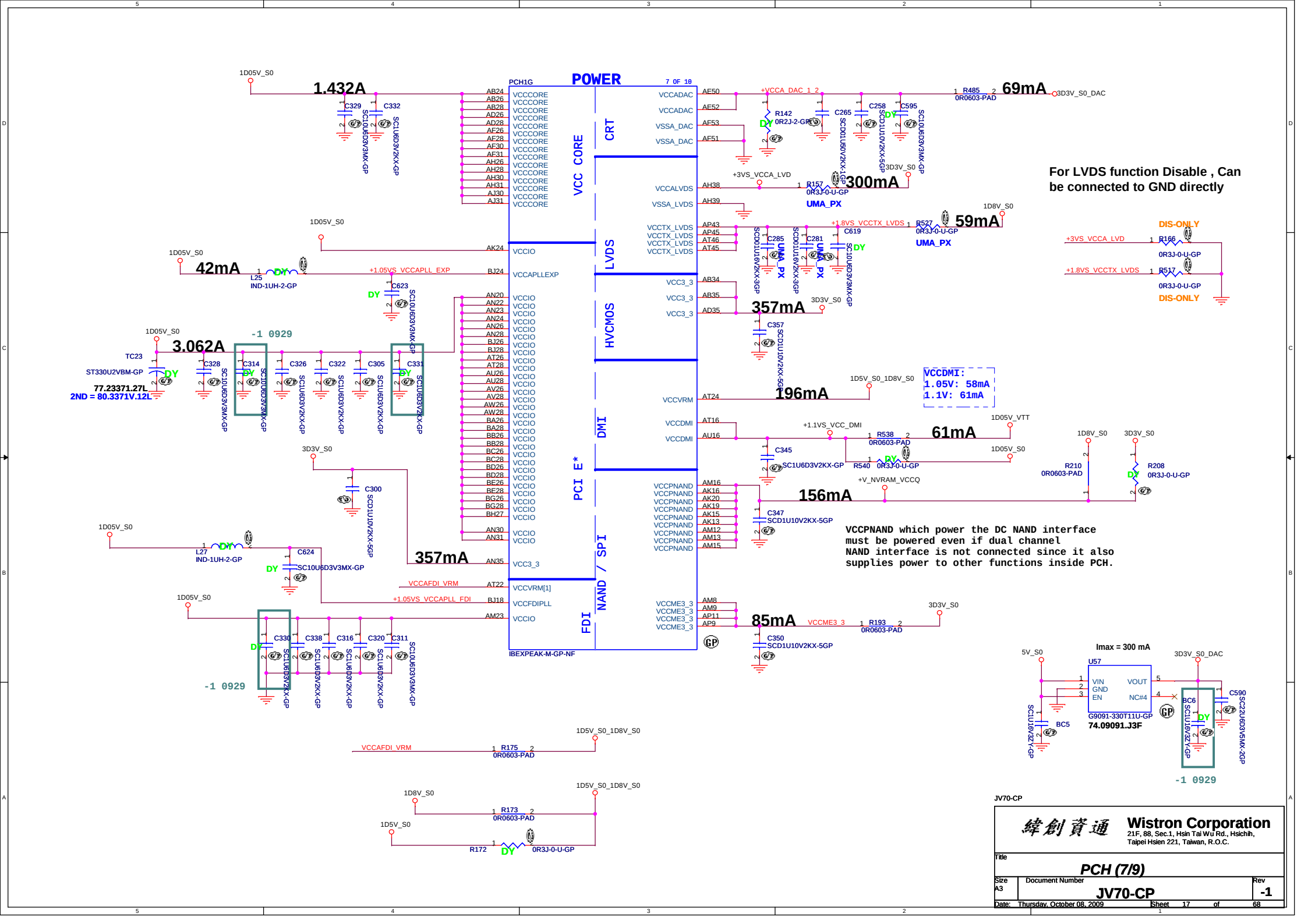
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.




POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
42mA
3.062A
357mA
300mA
59mA
357mA
196mA
61mA
156mA
85mA
69mA
For LVDS function Disable , Can be connected to GND directly
VCCDMI:
1.05V: 58mA
1.1V: 61mA
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
Imax = 300 mA
-1 0929
JV70-CP
Wistron Corporation
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PCH (7/9)
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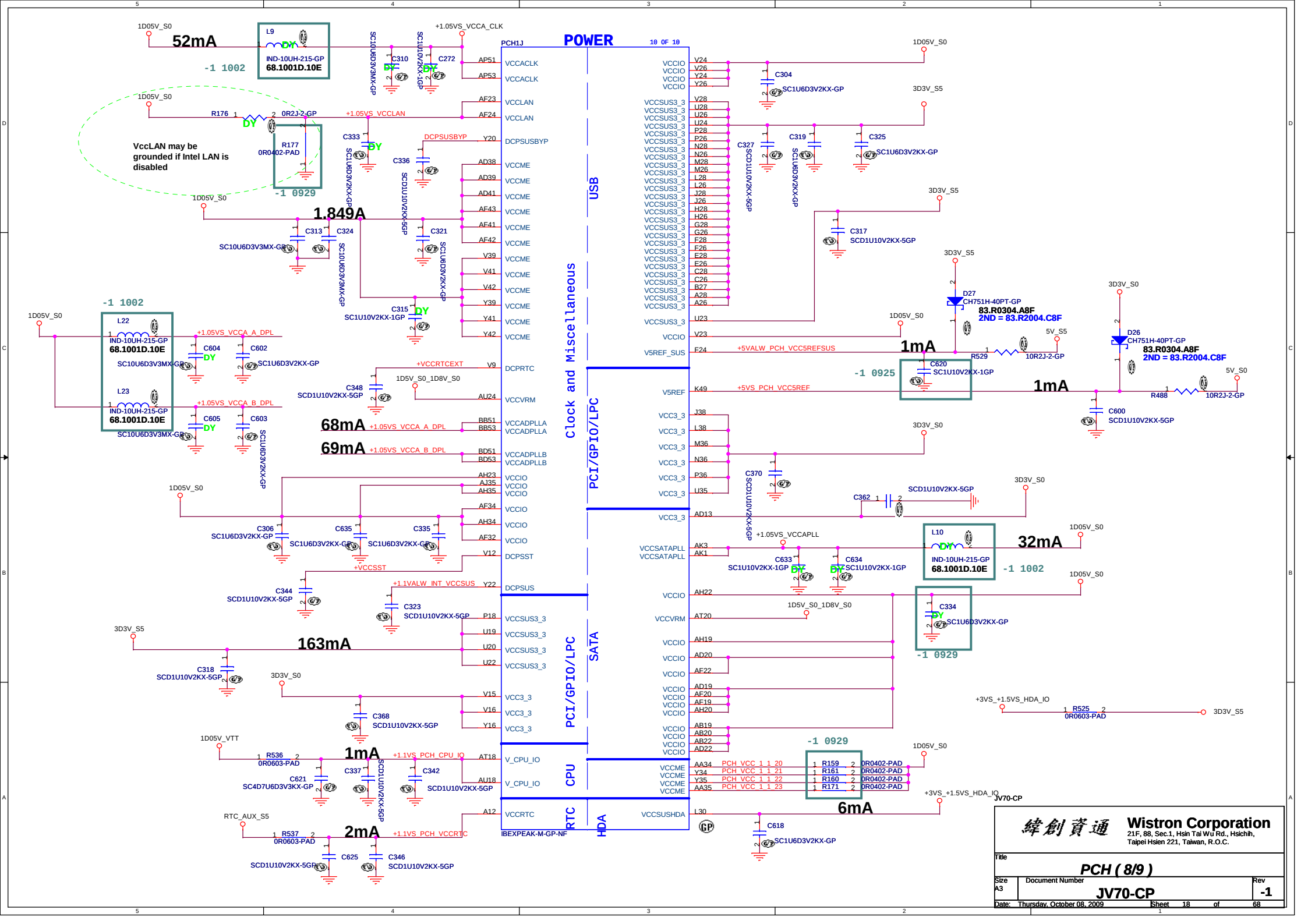
POWER
10 OF 10
PCH1J
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M-GP-NF
52mA
1.849A
163mA
68mA
69mA
1mA
32mA
6mA
2mA
-1 1002
-1 0929
-1 0925
VccLAN may be grounded if Intel LAN is disabled
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Title
PCH (8/9)
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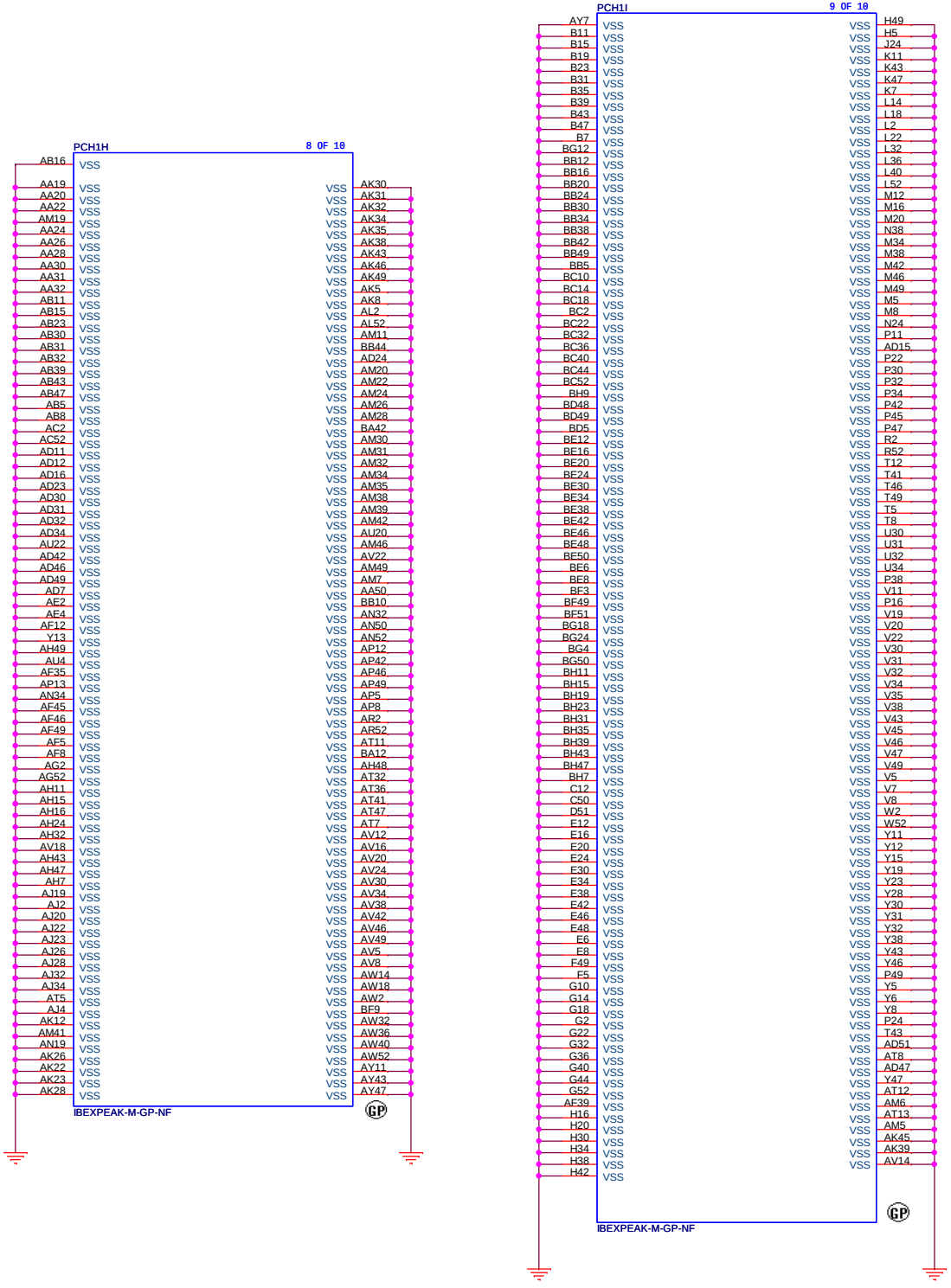

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Title: ***PCH (9/9)***

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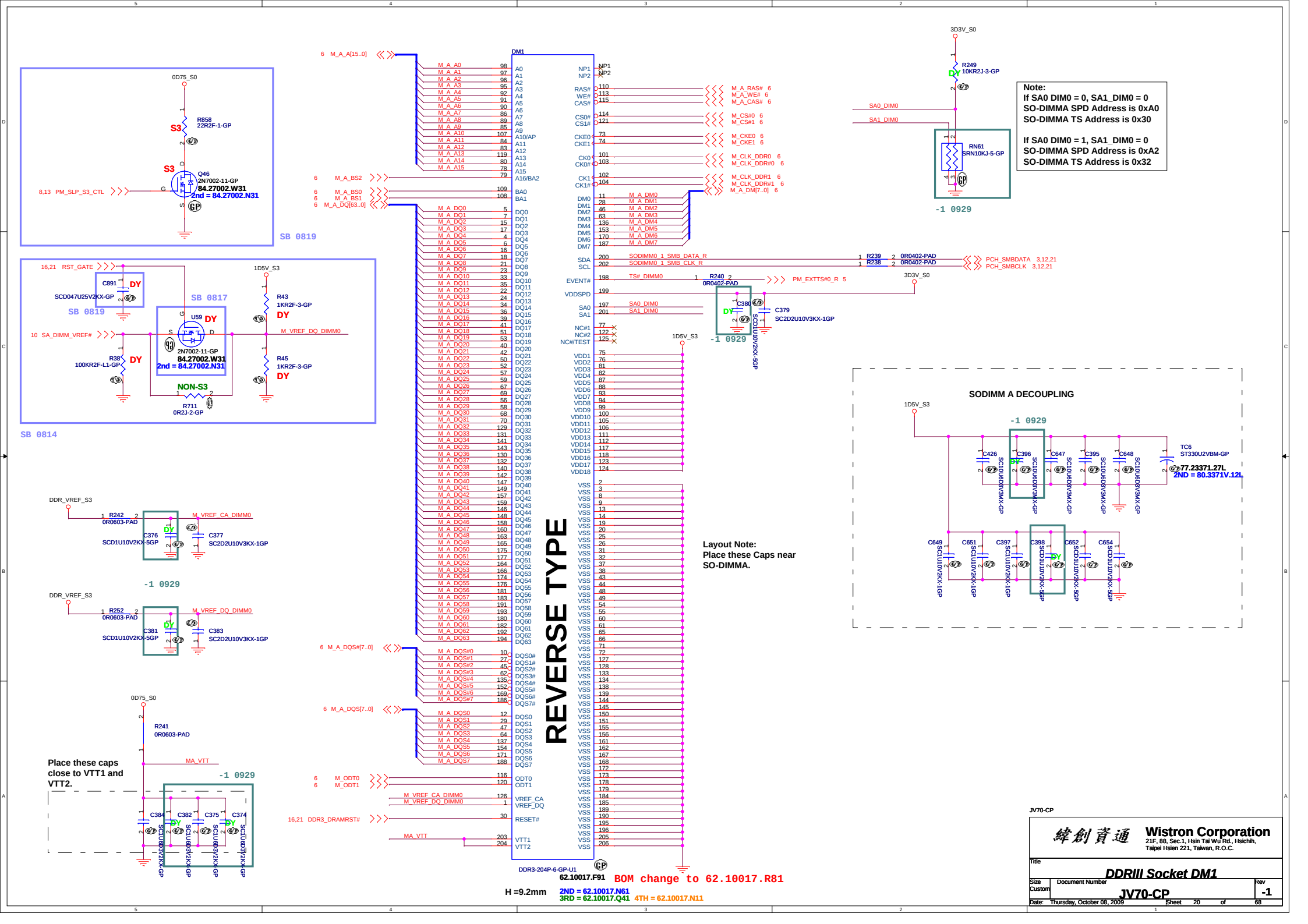
DM1
REVERSE TYPE
DDR3-204P-6-GP-U1
62.10017.F91
BOM change to 62.10017.R81
H =9.2mm
2ND = 62.10017.N61
3RD = 62.10017.Q41
4TH = 62.10017.N11
SB 0819
SB 0817
SB 0814
-1 0929
NON-S3
Q46
2N7002-11-GP
84.27002.W31
2nd = 84.27002.N31
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
SODIMM A DECOUPLING
Layout Note:
Place these Caps near
SO-DIMMA.
Place these caps
close to VTT1 and
VTT2.
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DDRIII Socket DM1
JV70-CP
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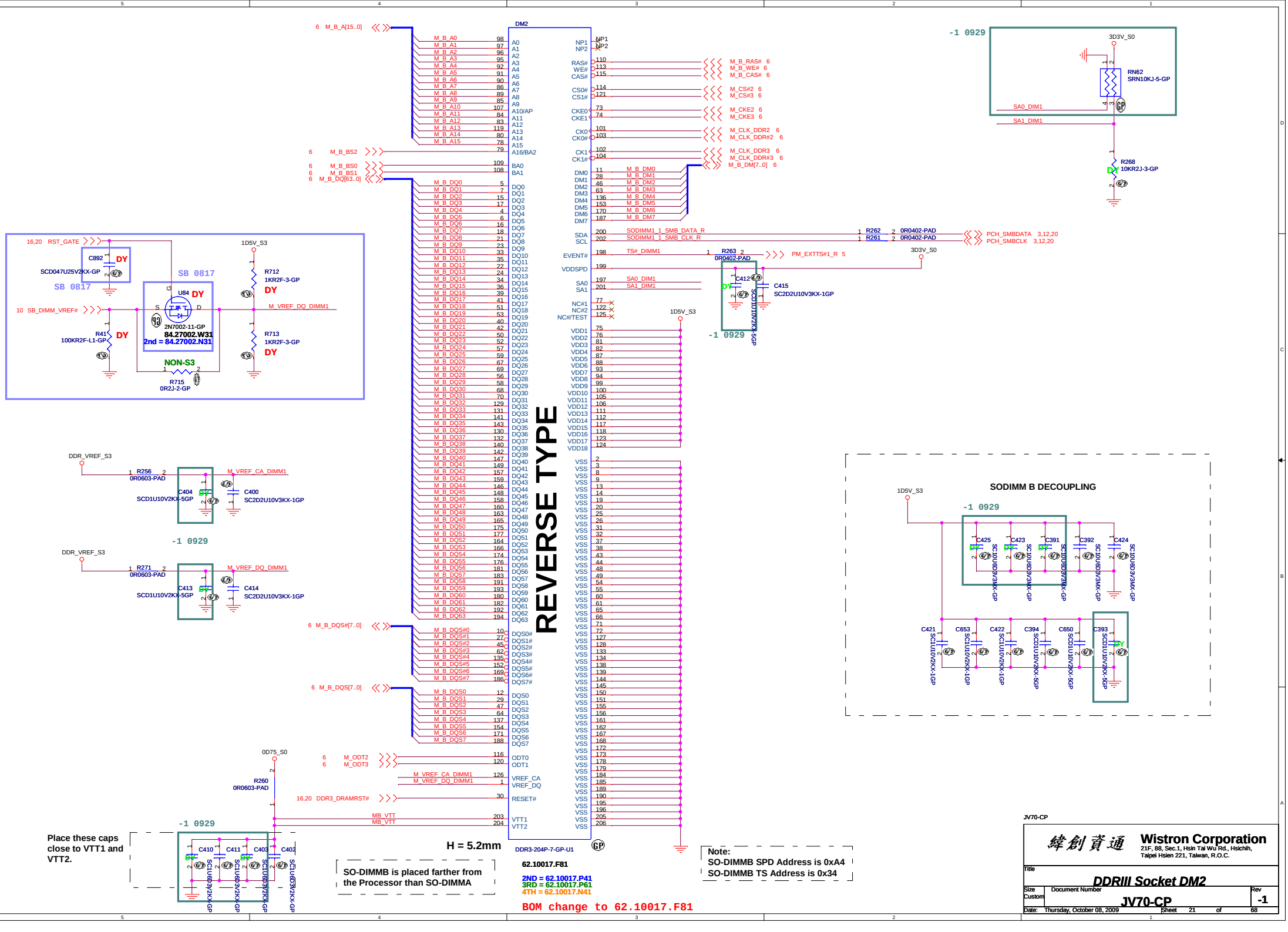
DM2
REVERSE TYPE
DDR3-204P-7-GP-U1
H = 5.2mm
SB 0817
SB 0817
NON-S3
-1 0929
-1 0929
-1 0929
-1 0929
SODIMM B DECOUPLING
Place these caps close to VTT1 and VTT2.
SO-DIMMB is placed farther from the Processor than SO-DIMMA
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
62.10017.F81
2ND = 62.10017.P41
3RD = 62.10017.P61
4TH = 62.10017.N41
BOM change to 62.10017.F81
JV70-CP
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DDRIII Socket DM2
JV70-CP
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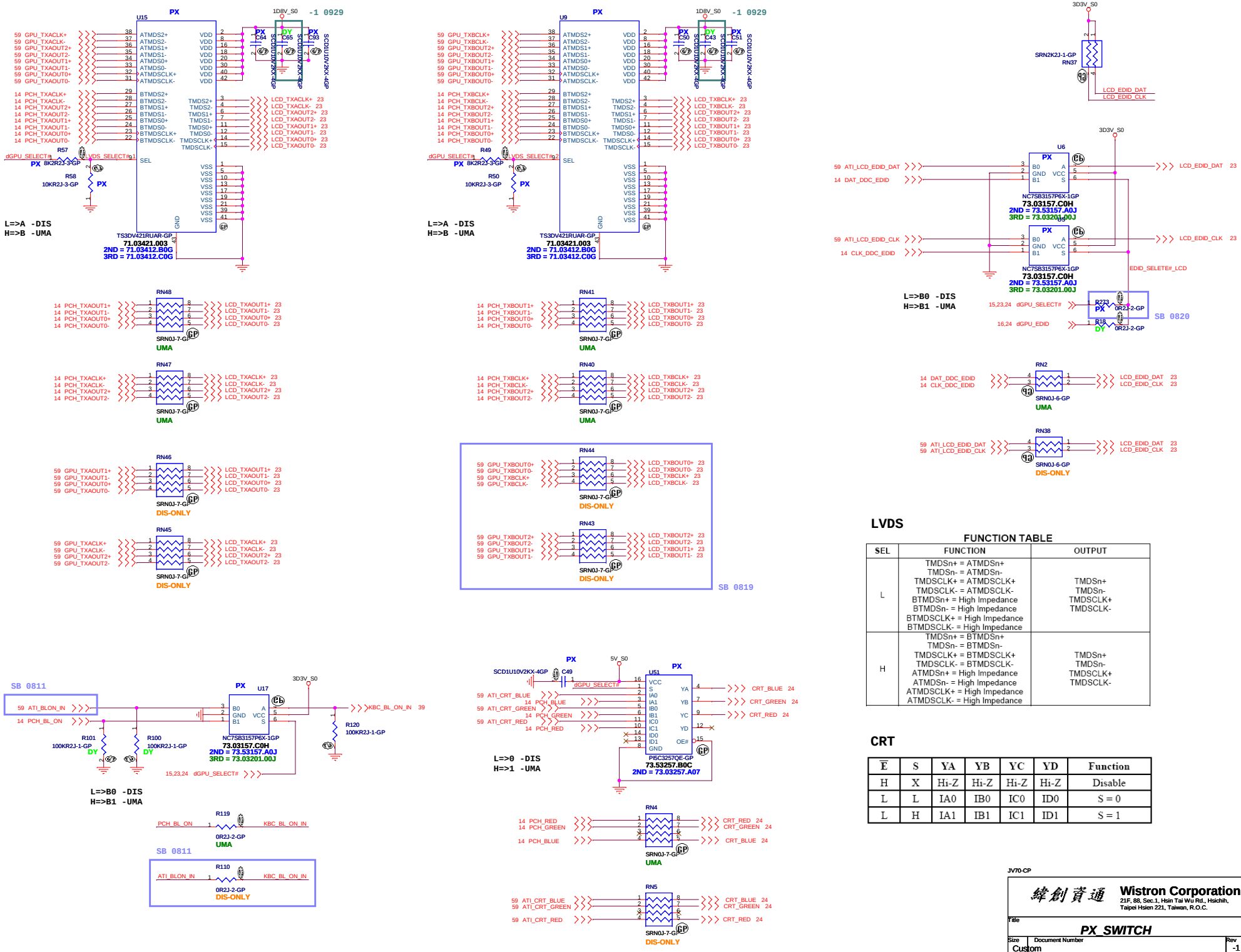

LVDS

FUNCTION TABLE

$EL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

CRT

$E	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

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Title: PX_SWITCH

Size	Document Number	Rev
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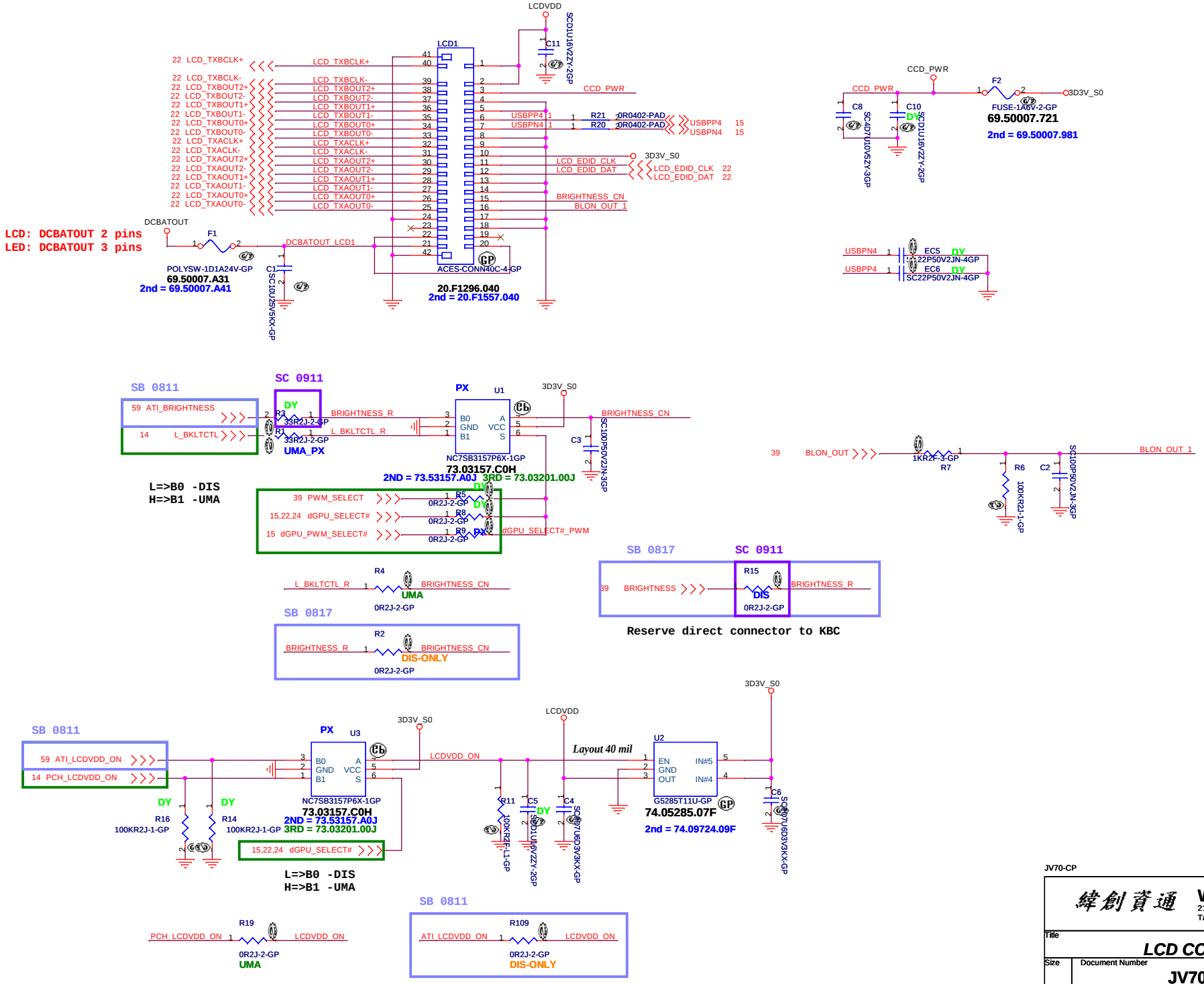
LCD/INVERTER/CCD CONN



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Title			
LCD CONN			
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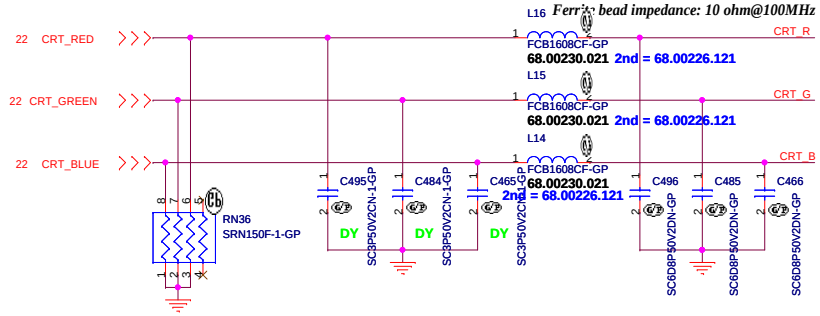
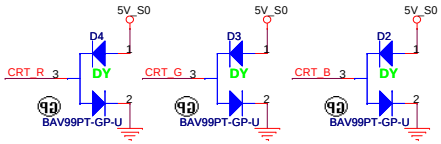
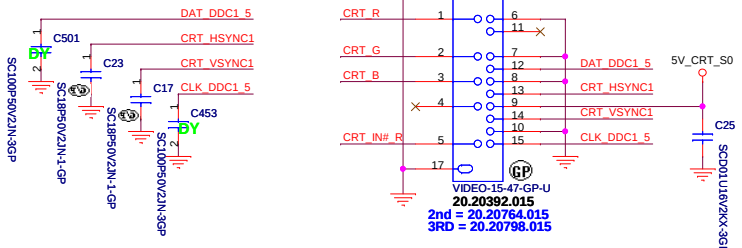
Layout Note:
Place these resistors close to the CRT-out connector

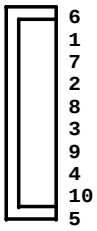


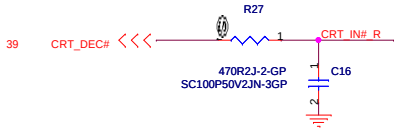
Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

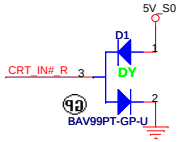


CRT I/F & CONNECTOR



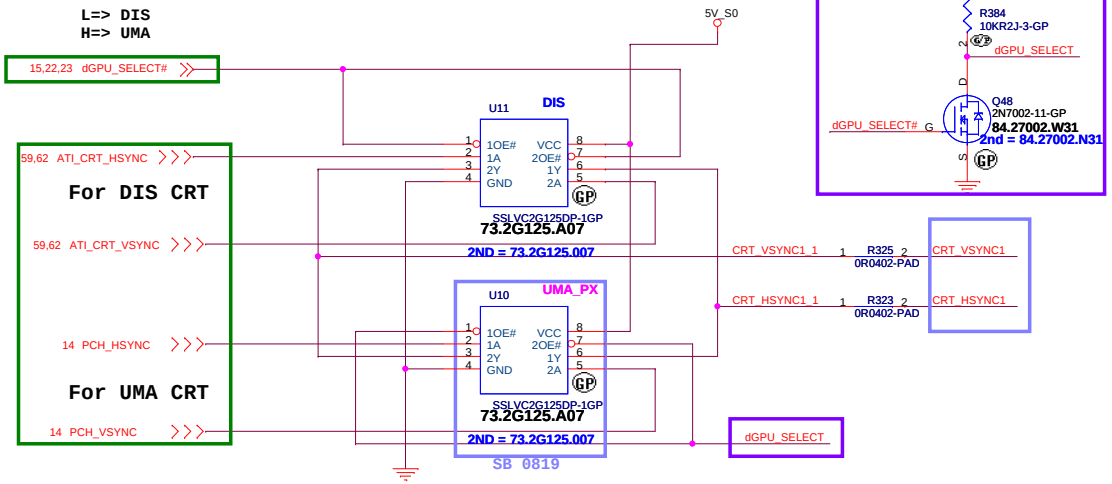




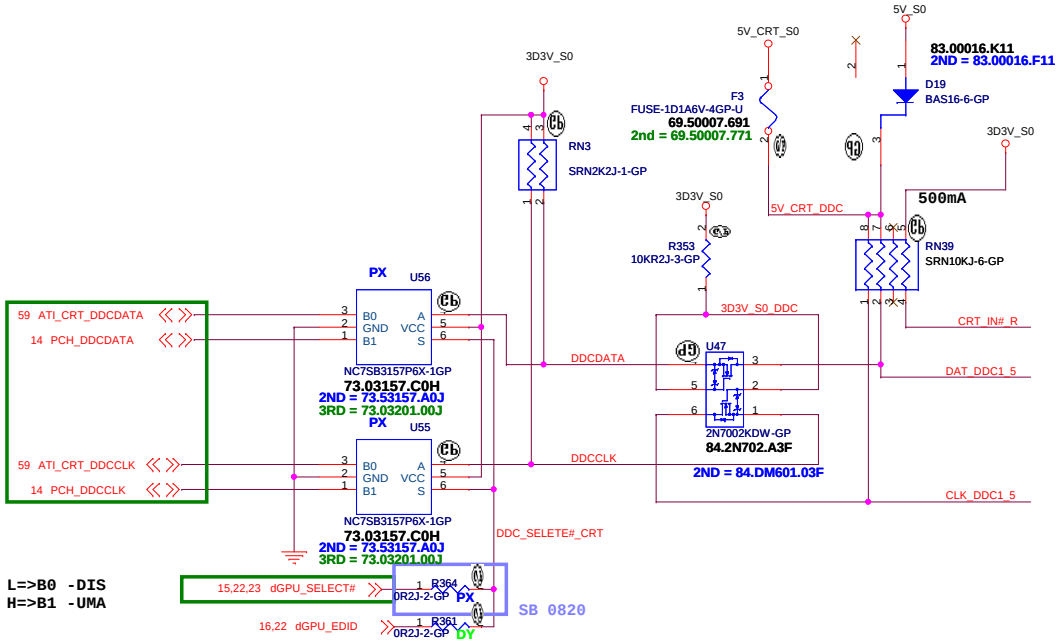


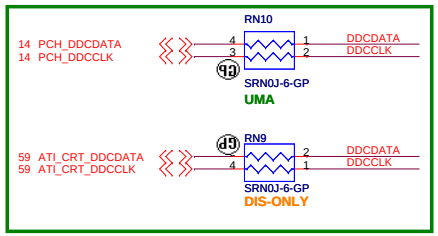
Hsync & Vsync level shift

L=> DIS
H=> UMA



DDC_CLK & DATA level shift





JV70-CP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT CONN	
Size	Document Number JV70-CP	Rev -1
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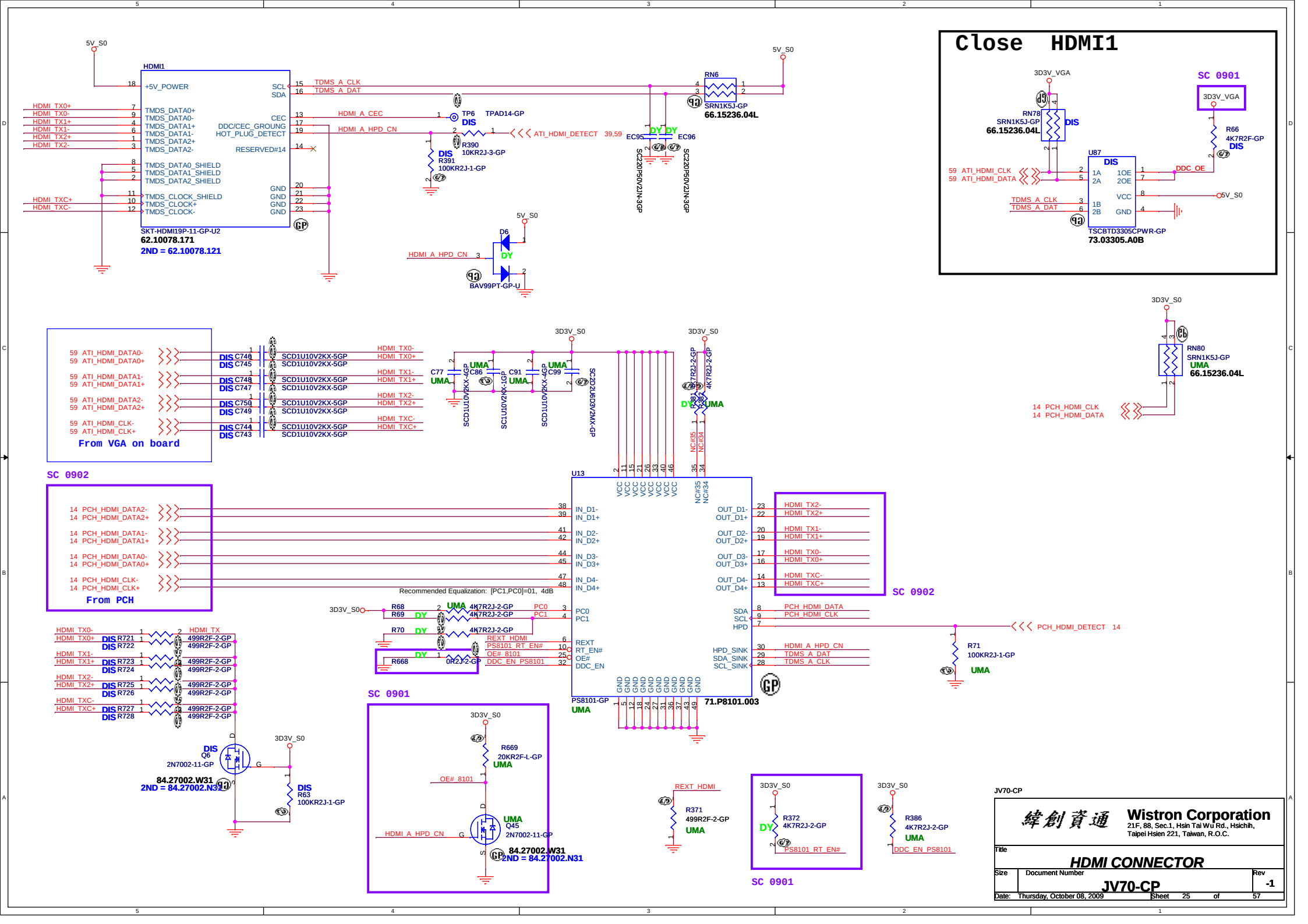
Close HDMI1
HDMI1
SKT-HDMI19P-11-GP-U2
62.10078.171
2ND = 62.10078.121
SC 0901
SC 0902
From VGA on board
From PCH
U13
PS8101-GP
71.P8101.003
TSCBTD3305CPWR-GP
73.03305.A0B
84.27002.W31
2ND = 84.27002.N31
JV70-CP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
HDMI CONNECTOR
JV70-CP
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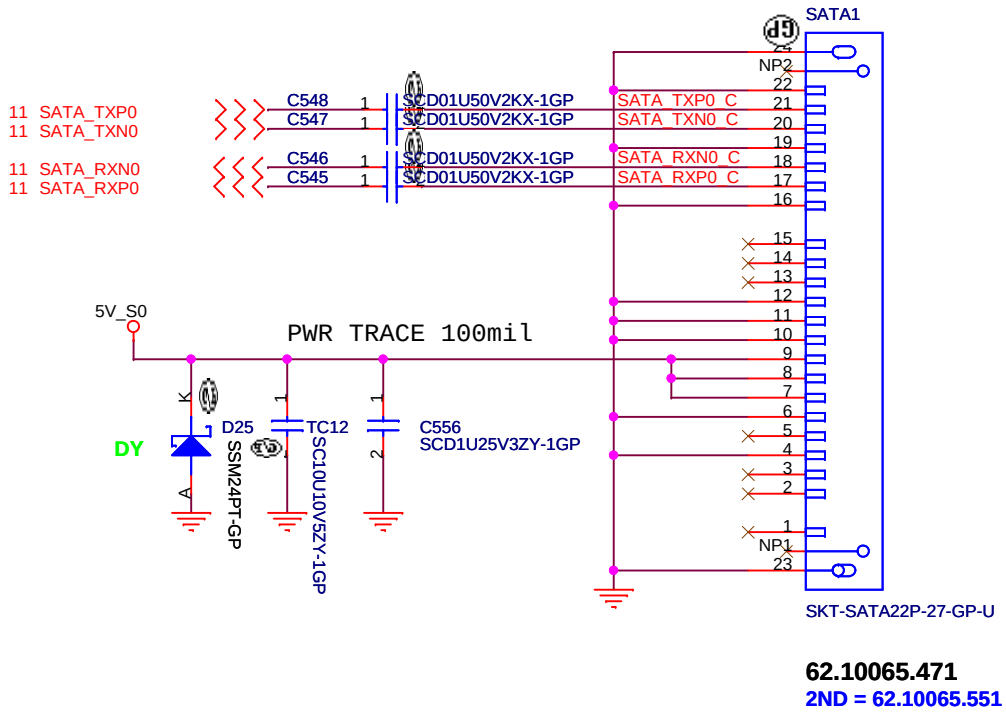
SATA Connector



62.10065.471

2ND = 62.10065.551

JV70-CP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD CONN***	
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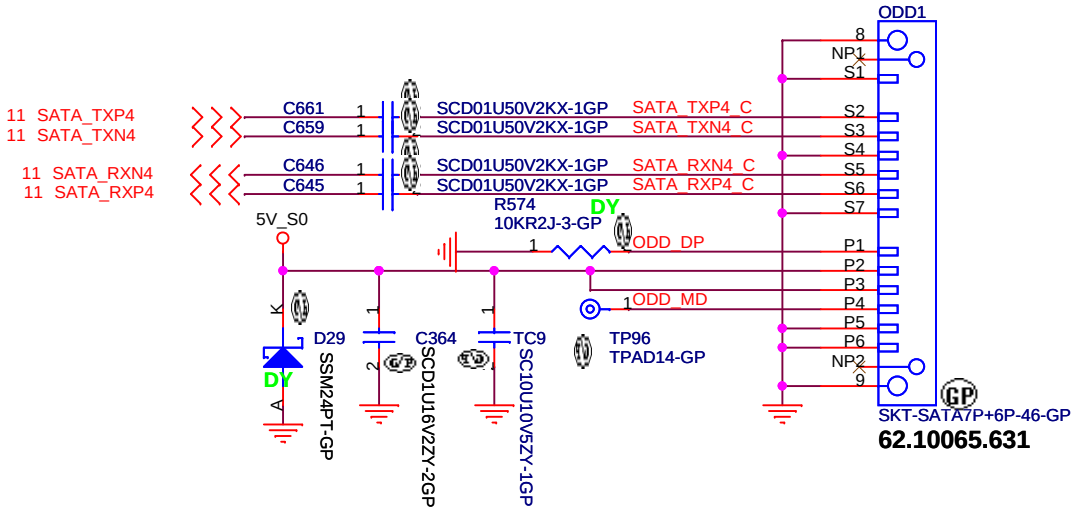
ODD Connector



JV70-CP

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Taipei Hsien 221, Taiwan, R.O.C.

Title	***ODD***	
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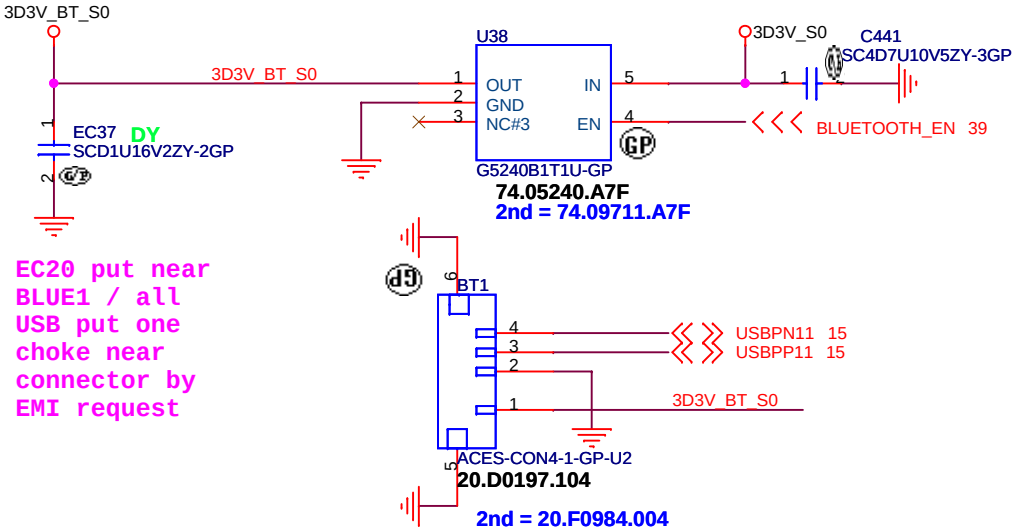
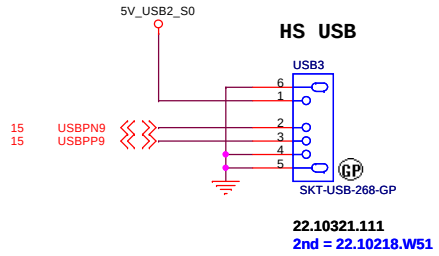
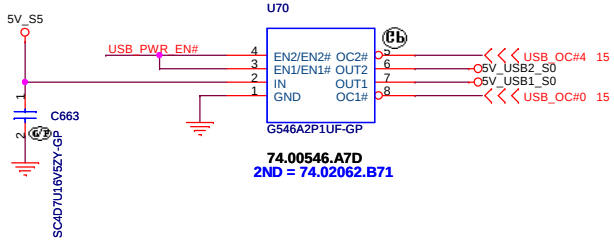
BLUETOOTH MODULE

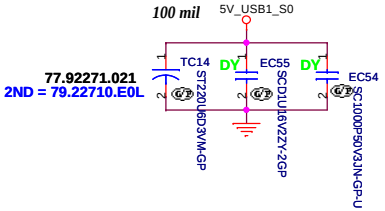


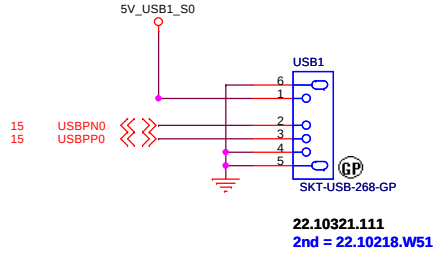
JV70-CP

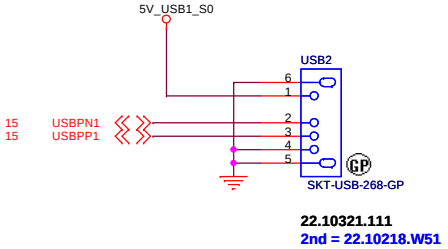
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
Size	Document Number: JV70-CP	Rev: -1
Date: Thursday, October 08, 2009	Sheet 28 of 68	

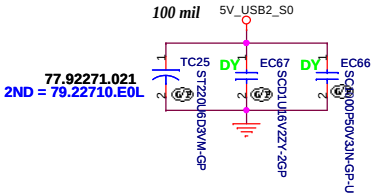


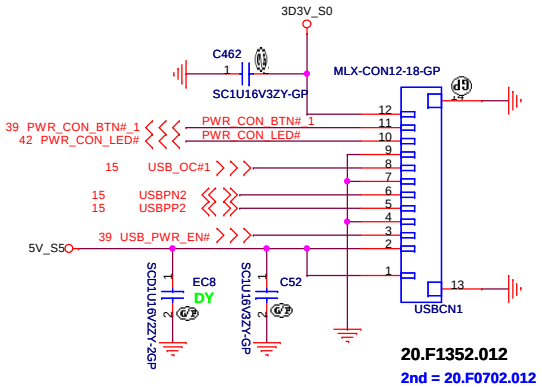


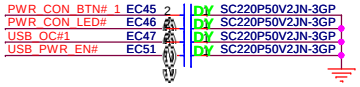












JV70-CP

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **USB CONN**		
Size	Document Number: JV70-CP	Rev: -1
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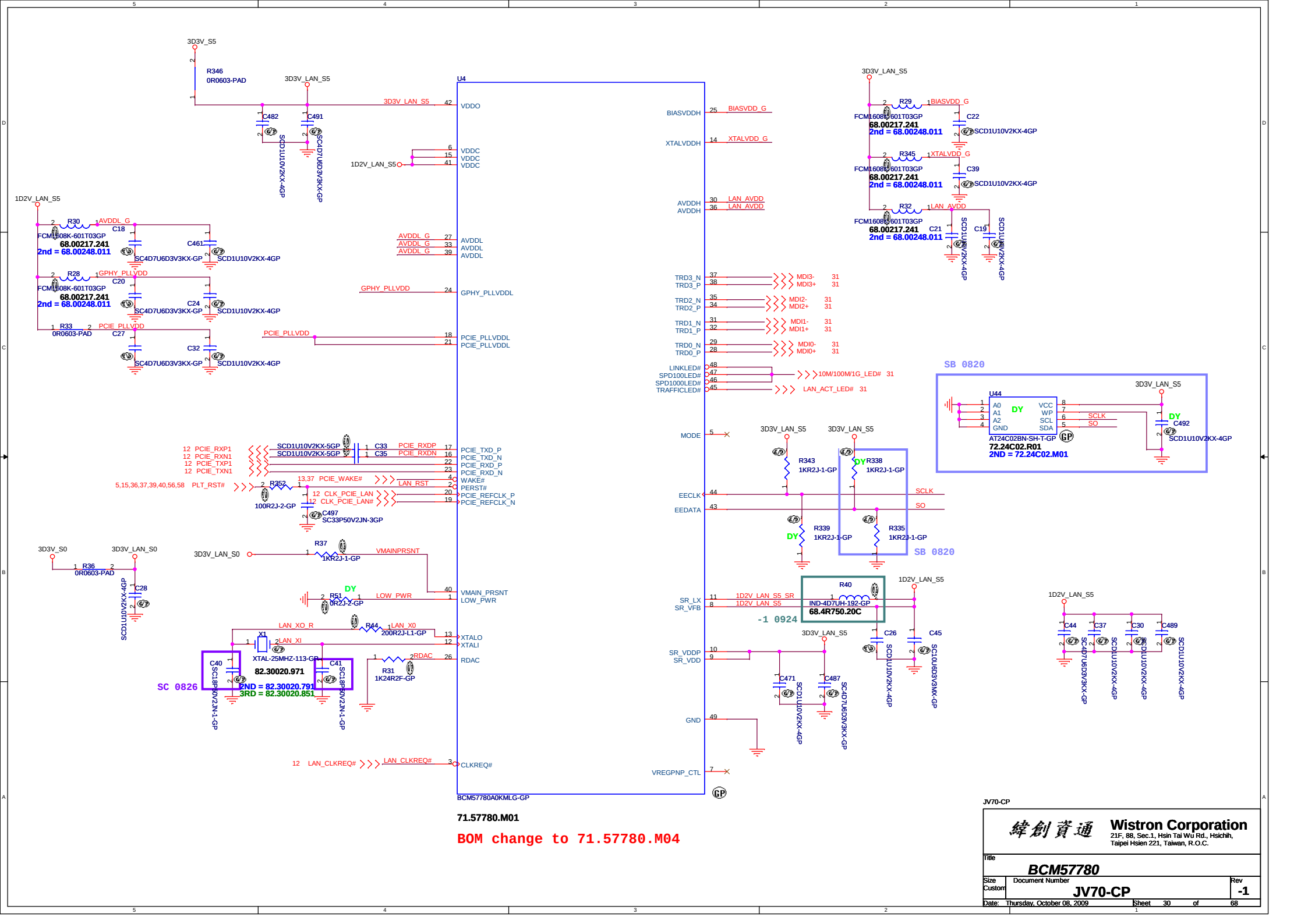
3D3V_S5
R346
0R0603-PAD
3D3V_LAN_S5
U4
VDDO
VDDC
VDDC
VDDC
1D2V_LAN_S5
C482
C491
SCD1U10V2KX-4GP
SC4D7U6D3V3KX-GP
BIASVDDH
XTALVDDH
AVDDH
AVDDH
BIASVDD_G
XTALVDD_G
LAN_AVDD
LAN_AVDD
R29
R345
R32
FCM1608K-601T03GP
68.00217.241
2nd = 68.00248.011
C22
C39
C21
C19
AVDDL_G
GPHY_PLLVDD
PCIE_PLLVDD
AVDDL
GPHY_PLLVDDL
PCIE_PLLVDDL
R30
R28
R33
C18
C20
C27
C461
C24
C32
SC4D7U6D3V3KX-GP
SCD1U10V2KX-4GP
TRD3_N
TRD3_P
TRD2_N
TRD2_P
TRD1_N
TRD1_P
TRD0_N
TRD0_P
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
10M/100M/1G_LED#
LAN_ACT_LED#
SB 0820
U44
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01
DY
C492
SCLK
SO
MODE
EECLK
EEDATA
R343
R338
R339
R335
1KR2J-1-GP
SR_LX
SR_VFB
SR_VDDP
SR_VDD
GND
VREGPNP_CTL
R40
IND-4D7UH-192-GP
68.4R750.20C
-1 0924
C26
C45
C471
C487
SC10U6D3V3MX-GP
SC4D7U6D3V3KX-GP
12 PCIE_RXP1
12 PCIE_RXN1
12 PCIE_TXP1
12 PCIE_TXN1
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
5,15,36,37,39,40,56,58 PLT_RST#
13,37 PCIE_WAKE#
WAKE#
PERST#
12 CLK_PCIE_LAN
12 CLK_PCIE_LAN#
PCIE_REFCLK_P
PCIE_REFCLK_N
R352
100R2J-2-GP
C497
SC33P50V2JN-3GP
3D3V_S0
3D3V_LAN_S0
R36
R37
VMAINPRSNT
VMAIN_PRSNT
R51
LOW_PWR
LOW_PWR
0R2J-2-GP
SC1U10V2KX-4GP
LAN_XO_R
LAN_XO
LAN_XI
R44
200R2J-L1-GP
X1
XTAL-25MHZ-113-GP
XTALO
XTALI
RDAC
C40
C41
82.30020.971
2ND = 82.30020.791
3RD = 82.30020.851
SC 0826
SC18P50V2JN-1-GP
R31
1K24R2F-GP
12 LAN_CLKREQ#
LAN_CLKREQ#
CLKREQ#
BCM57780A0KMLG-GP
71.57780.M01
BOM change to 71.57780.M04
JV70-CP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM57780
Size
Custom
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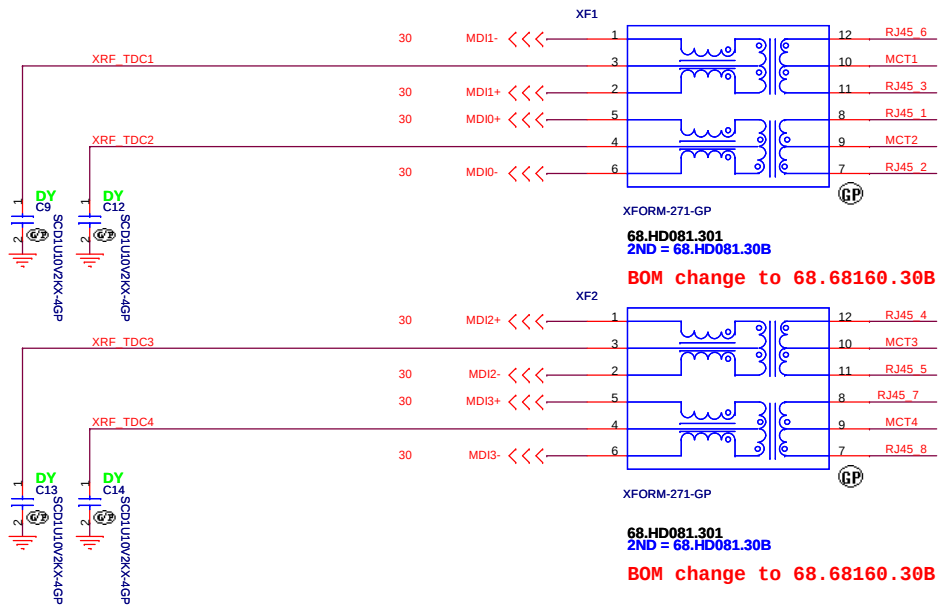
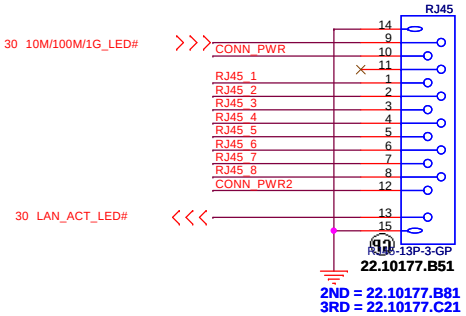
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

GIGA Lan Transformer





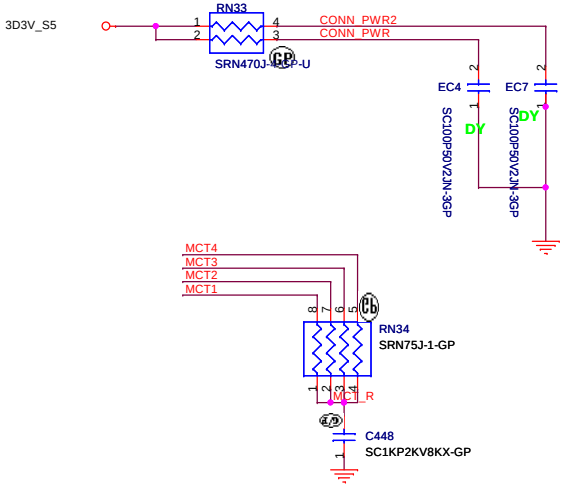
LED COLOR

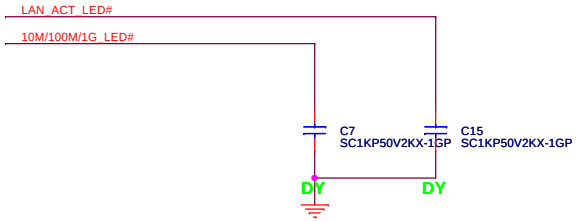
A2(+) A1(-)::GREEN
A2(+) A3(-):ORANGE

B1(+) B2(-):YELLOW

Green(A3), behavior is the same for 10/100/1000 bits

Yellow(B2), when LAN is transfering data.

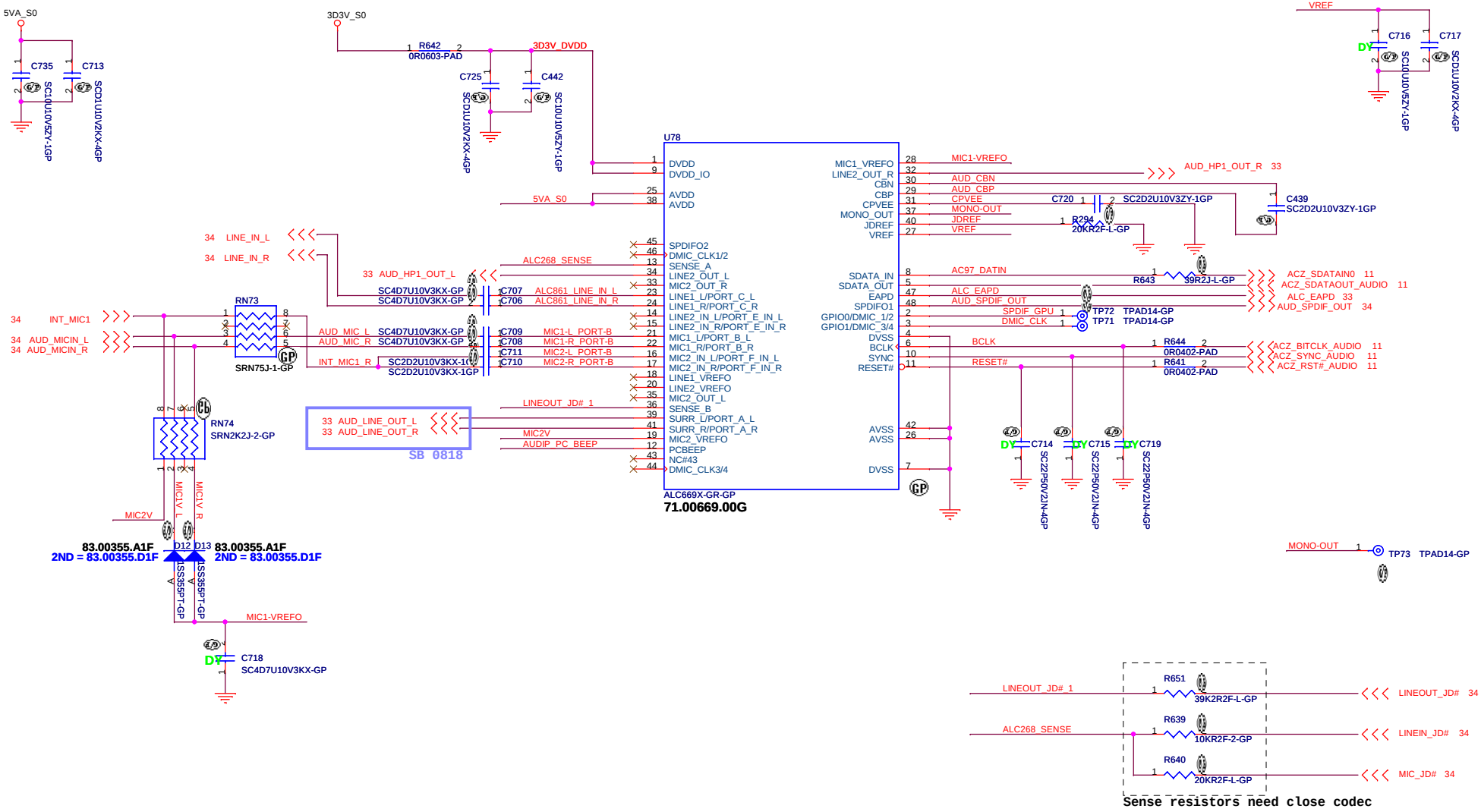




JV70-CP

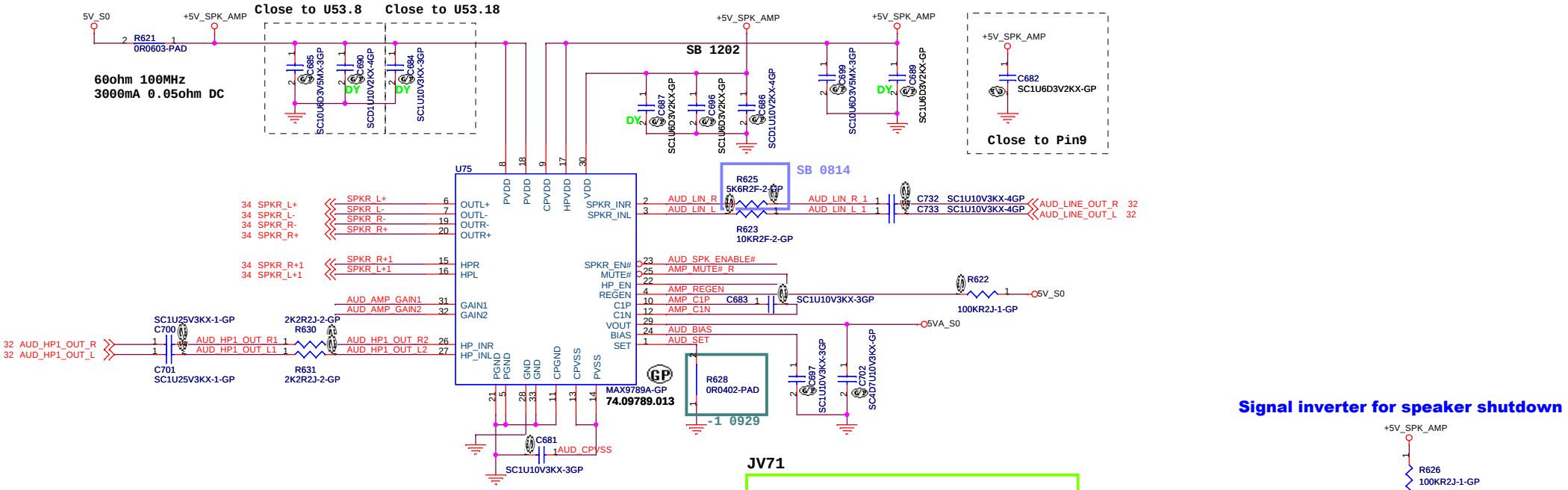
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

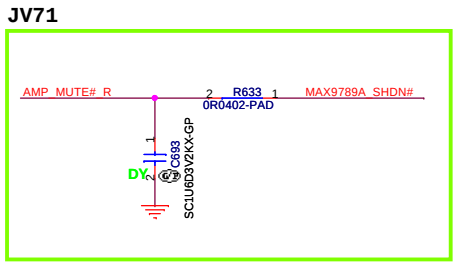
Title		
LAN CONN		
Size: A3	Document Number: JV70-CP	Rev: -1
Date: Thursday, October 08, 2009	Sheet 31 of 68	

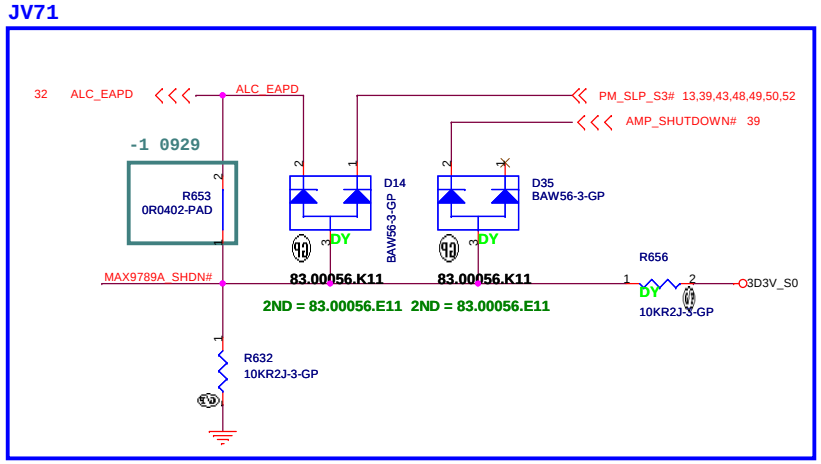


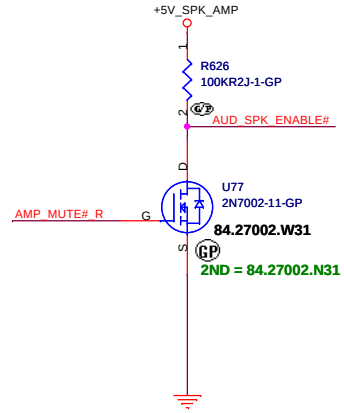
JV70-CP

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Azalia codec ALC669X*		
Size: A3	Document Number: JV70-CP	Rev: -1
Date: Friday, October 09, 2009	Sheet 32 of 68	

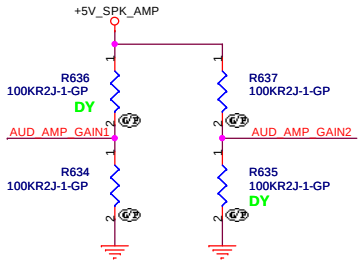








GAIN SETTING



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

JV70-CP

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AUDIO AMP MAX9789C
Size	Document Number: JV70-CP; Rev: -1
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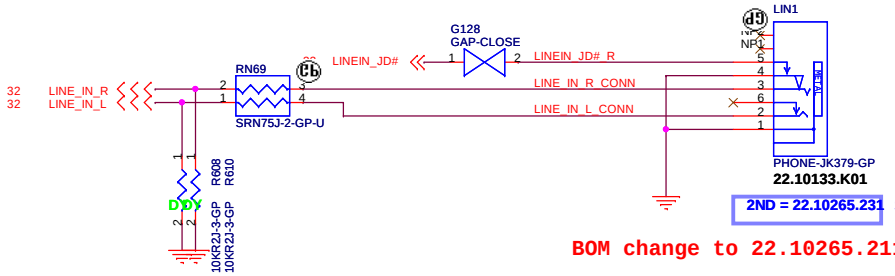
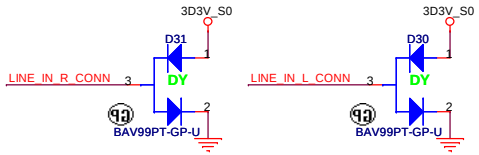
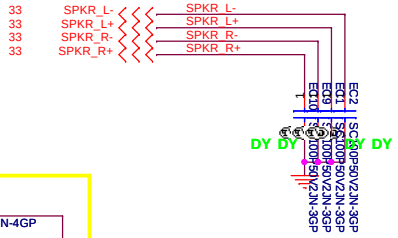
LINE IN

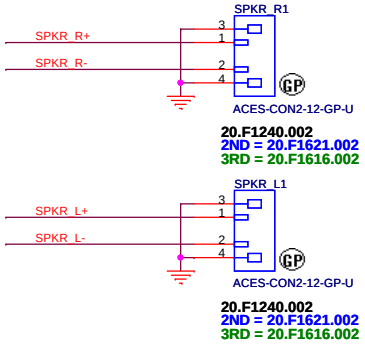


BOM change to 22.10265.211



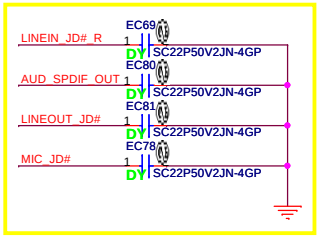
Internal Speaker

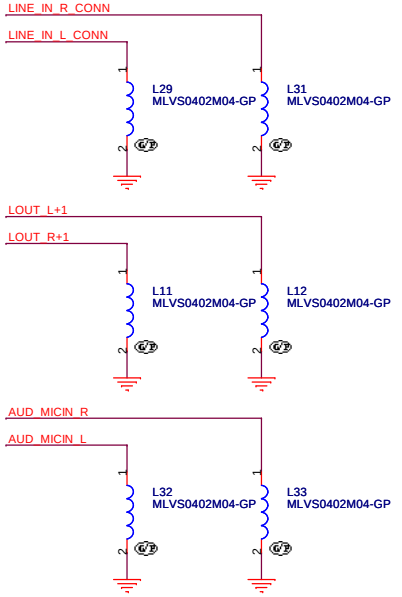




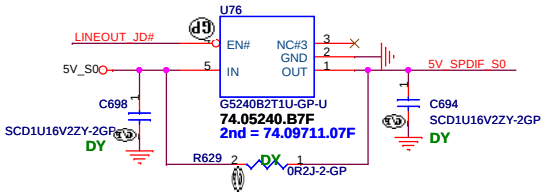
BOM change to 20.F1561.002

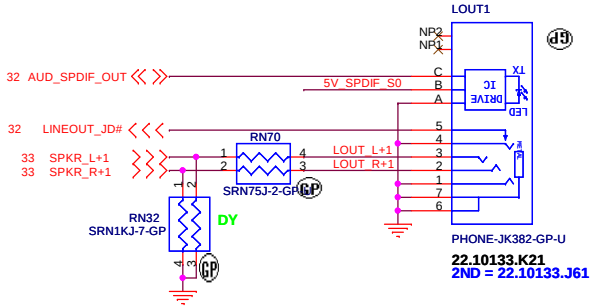
EMI



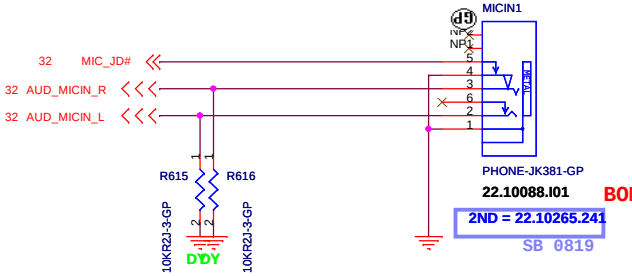


LINE OUT

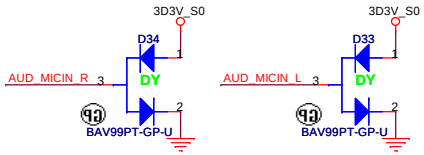




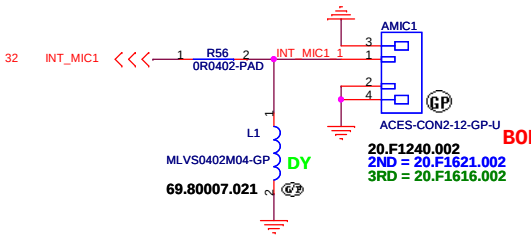
MIC IN



BOM change to 22.10265.201



Internal Mic



BOM change to 20.F1561.002

JV70-CP

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO Jack*		
Size	Document Number: JV70-CP	Rev: -1
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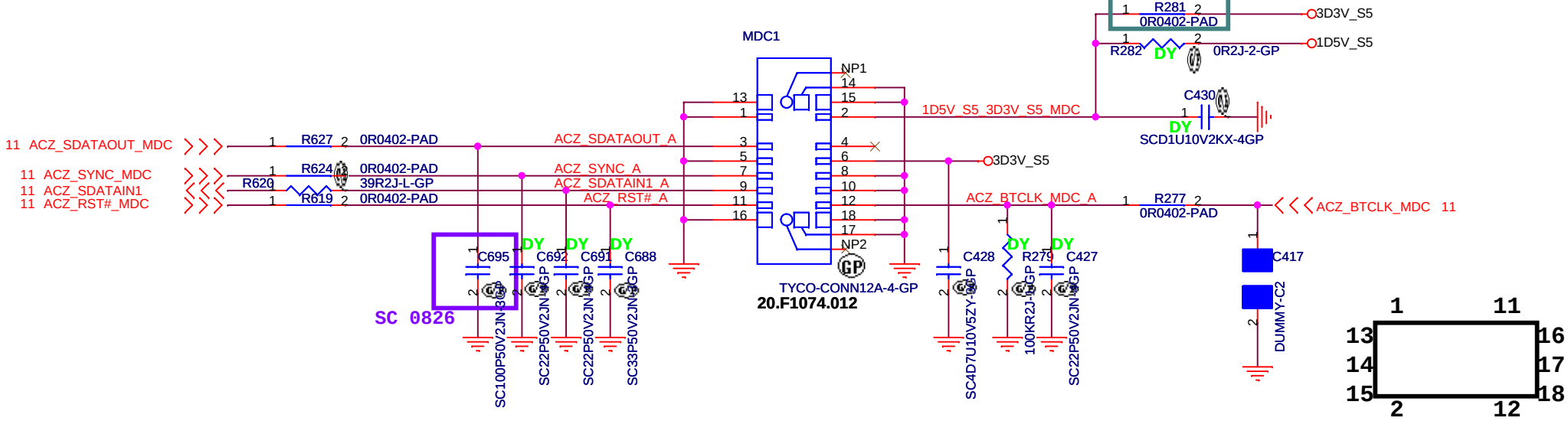
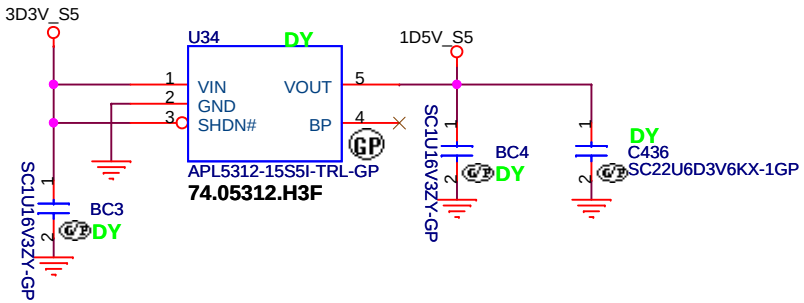
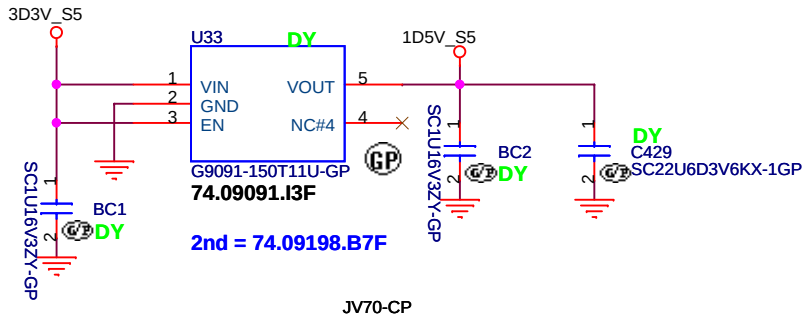
MDC 1.5 CONN

-1 0929







JV70-CP

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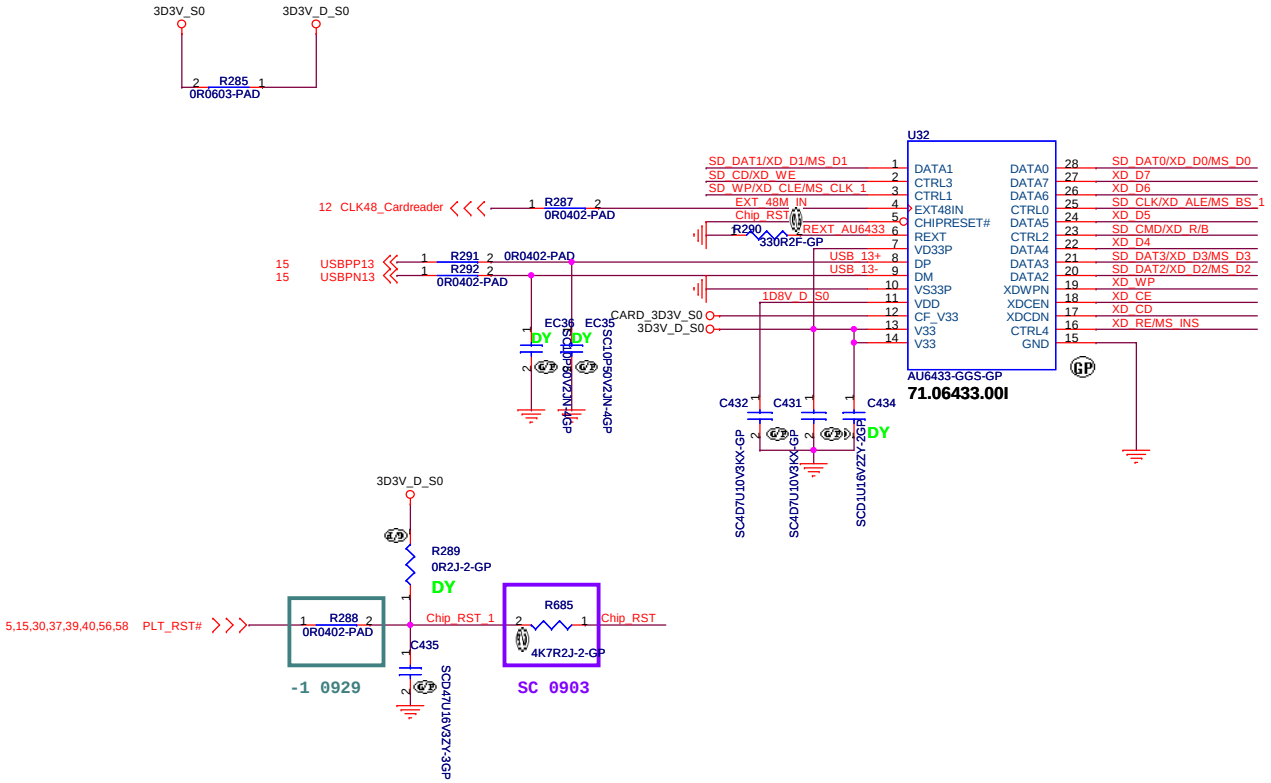
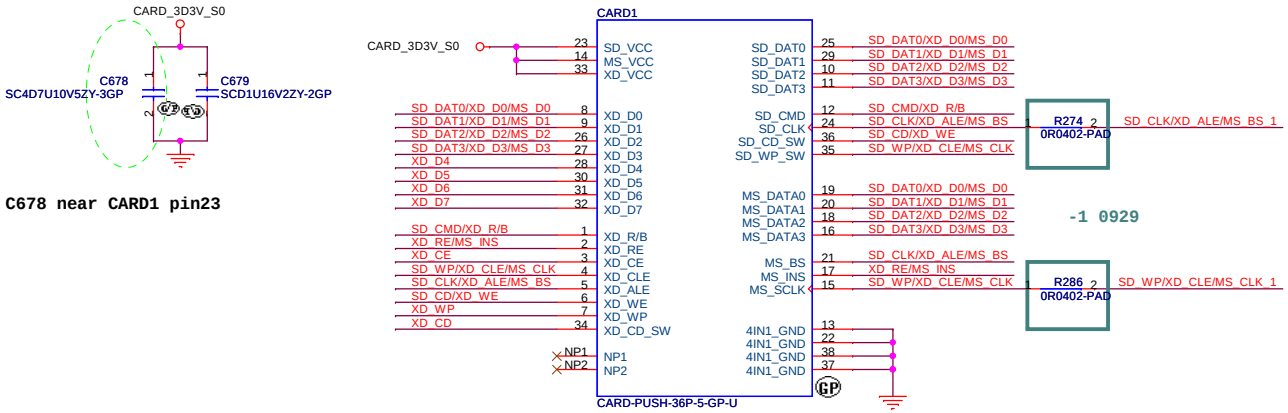
Taipei Hsien 221, Taiwan, R.O.C.

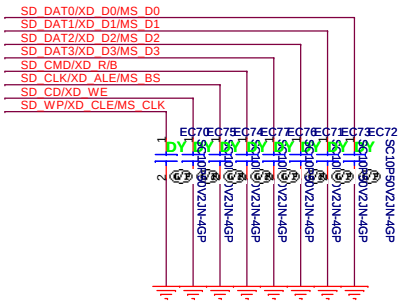
Title	MDC	
Size	Document Number JV70-CP	Rev -1
Date: Thursday, October 08, 2009	Sheet 35 of 68	



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



EMI capacitor



JV70-CP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*Cardreader AU6433*	
Size	Document Number JV70-CP	Rev -1
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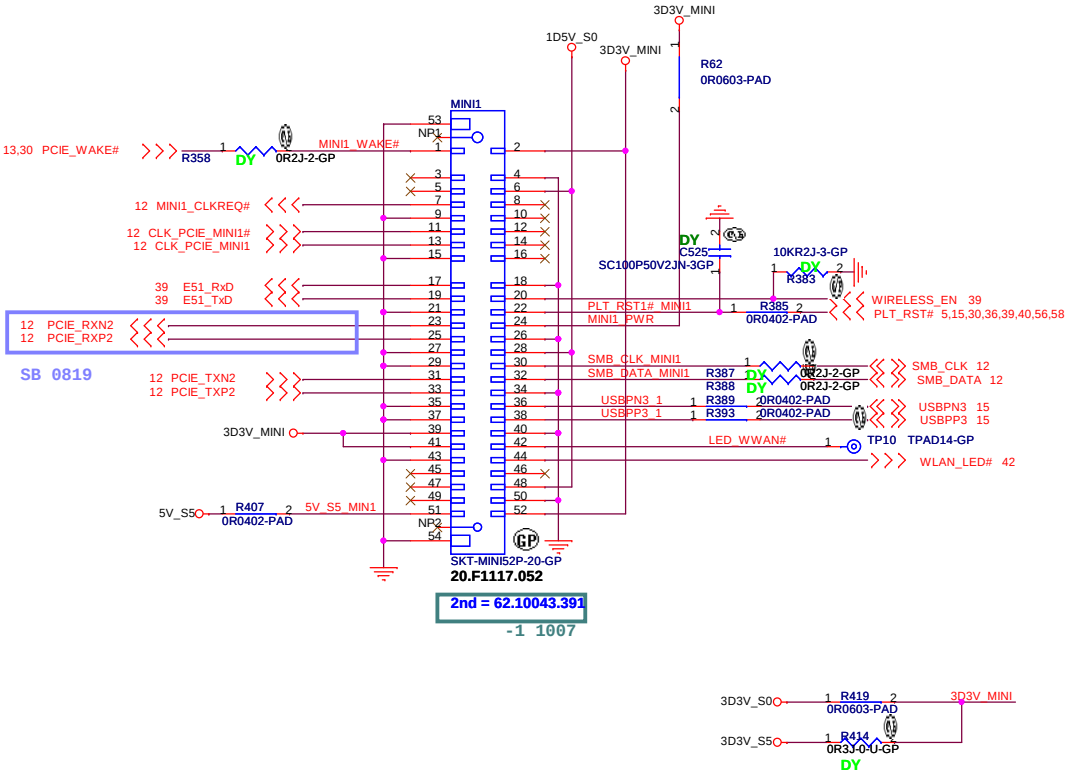
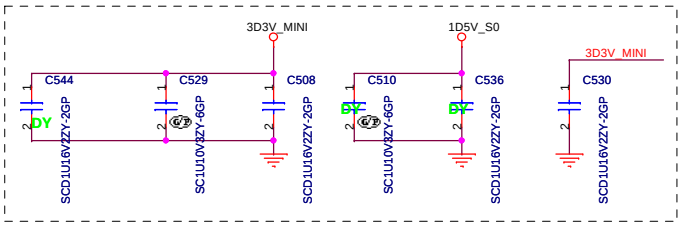
Mini Card Connector(WLAN)
Support debug-card



Place near MINI1



Mini Card Connector

JV70-CP

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD		
Size: A3	Document Number: JV70-CP	Rev: -1
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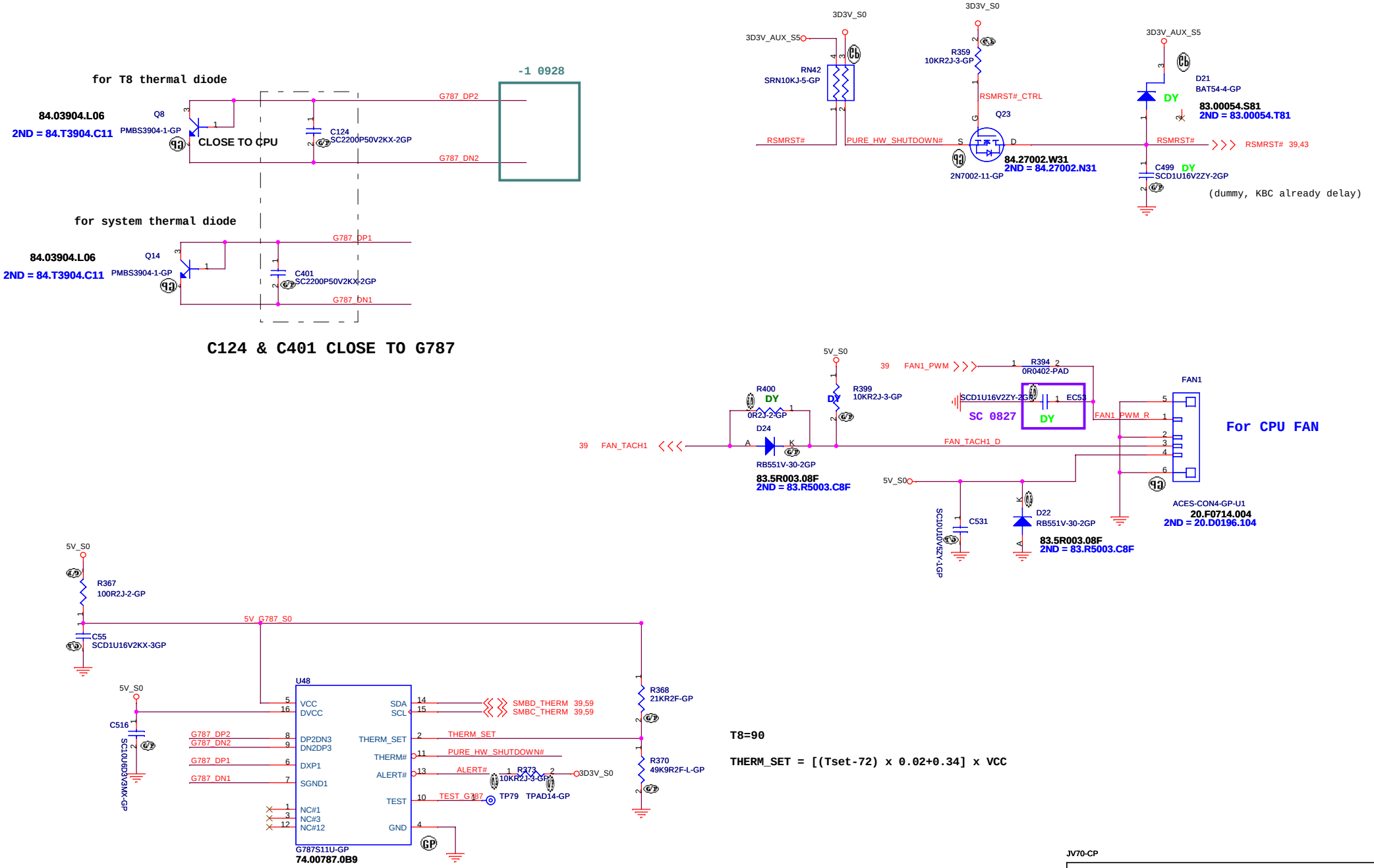

JV70-CP

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Connector***

Size	Document Number	Rev
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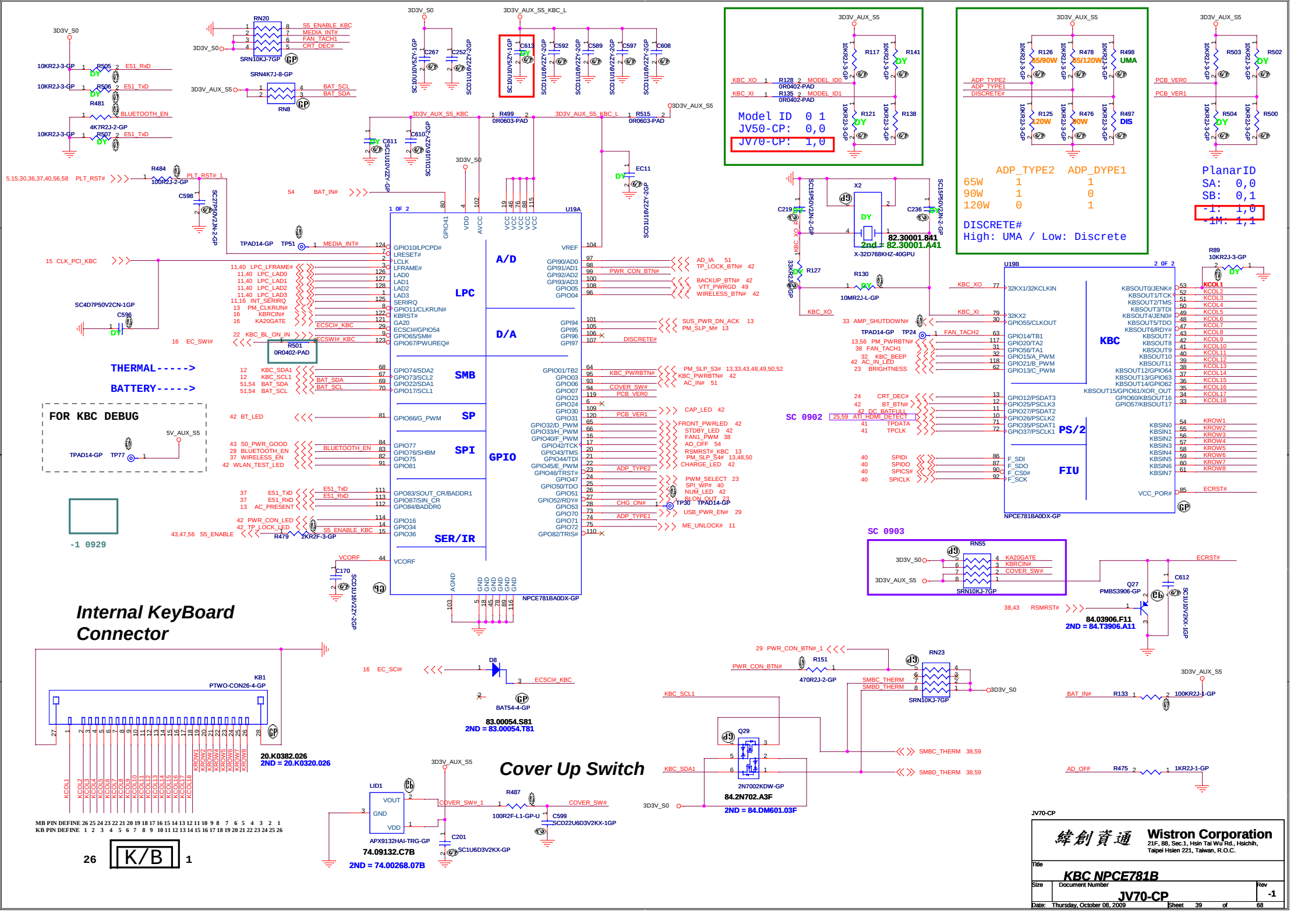
Model ID 0 1
JV50-CP: 0,0
JV70-CP: 1,0
ADP_TYPE2 ADP_DYPE1
65W 1 1
90W 1 0
120W 0 1
DISCRETE#
High: UMA / Low: Discrete
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
THERMAL----->
BATTERY----->
FOR KBC DEBUG
Internal KeyBoard Connector
Cover Up Switch
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
SC 0902
SC 0903
U19A
U19B
NPCE781BA0DX-GP
X-32D768KHZ-40GPU
82.30001.841
2nd = 82.30001.A41
83.00054.S81
2ND = 83.00054.T81
20.K0382.026
2ND = 20.K0320.026
74.09132.C7B
2ND = 74.00268.07B
84.03906.F11
2ND = 84.T3906.A11
84.2N702.A3F
2ND = 84.DM601.03F
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
JV70-CP
KBC NPCE781B
Document Number
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Rev
-1
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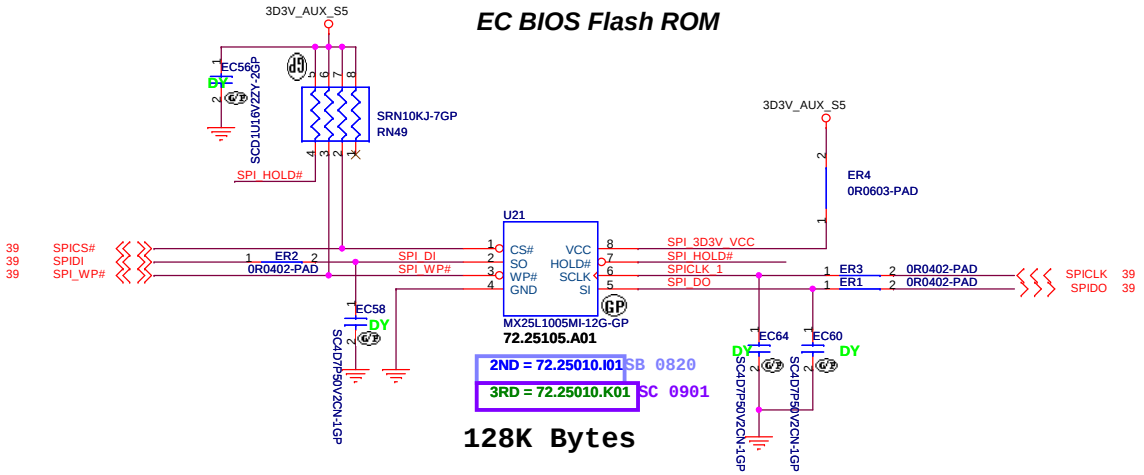
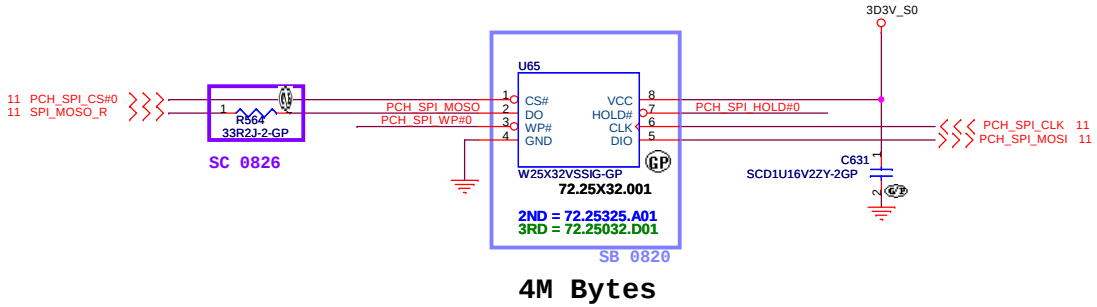
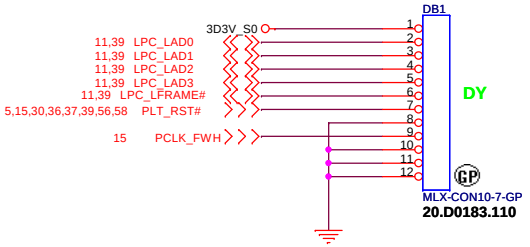
EC BIOS Flash ROM

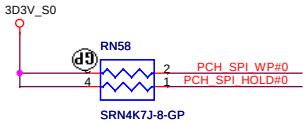


System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD





JV70-CP

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Title: **BIOS**

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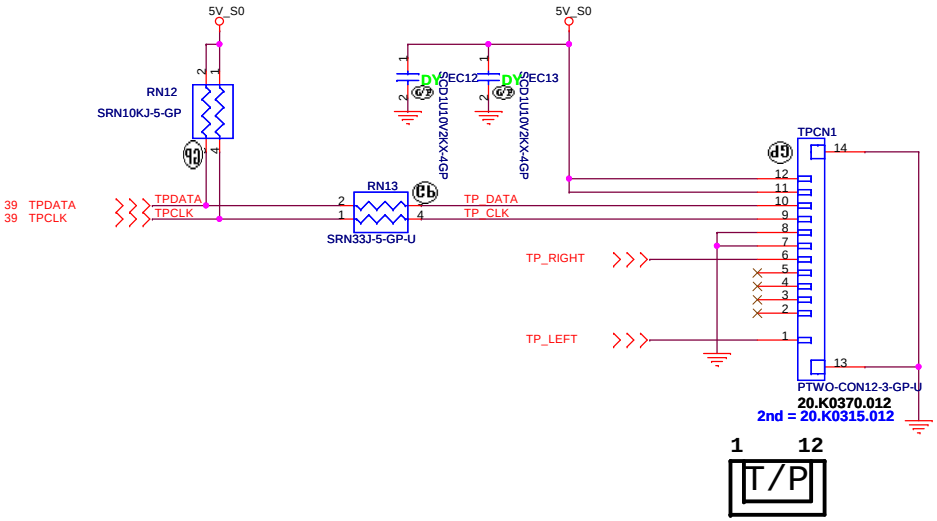
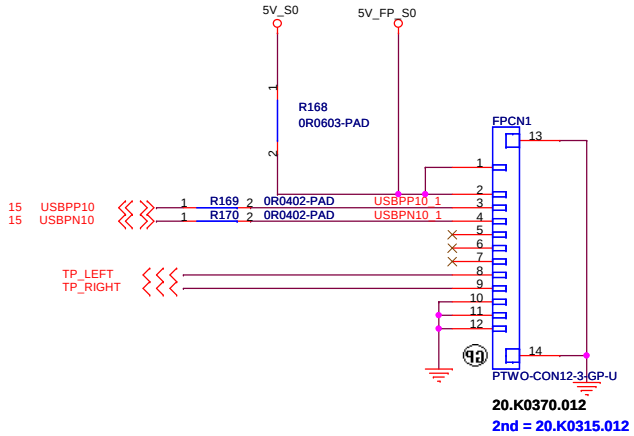
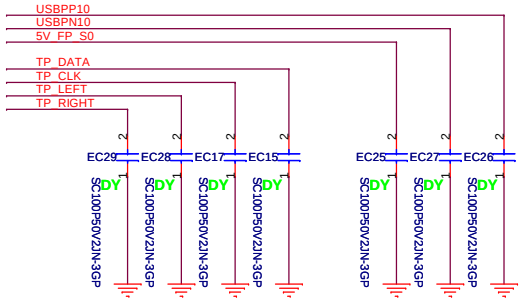
TOUCH PAD



Finger printer





JV70-CP

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Title: *Touch PAD and FP*

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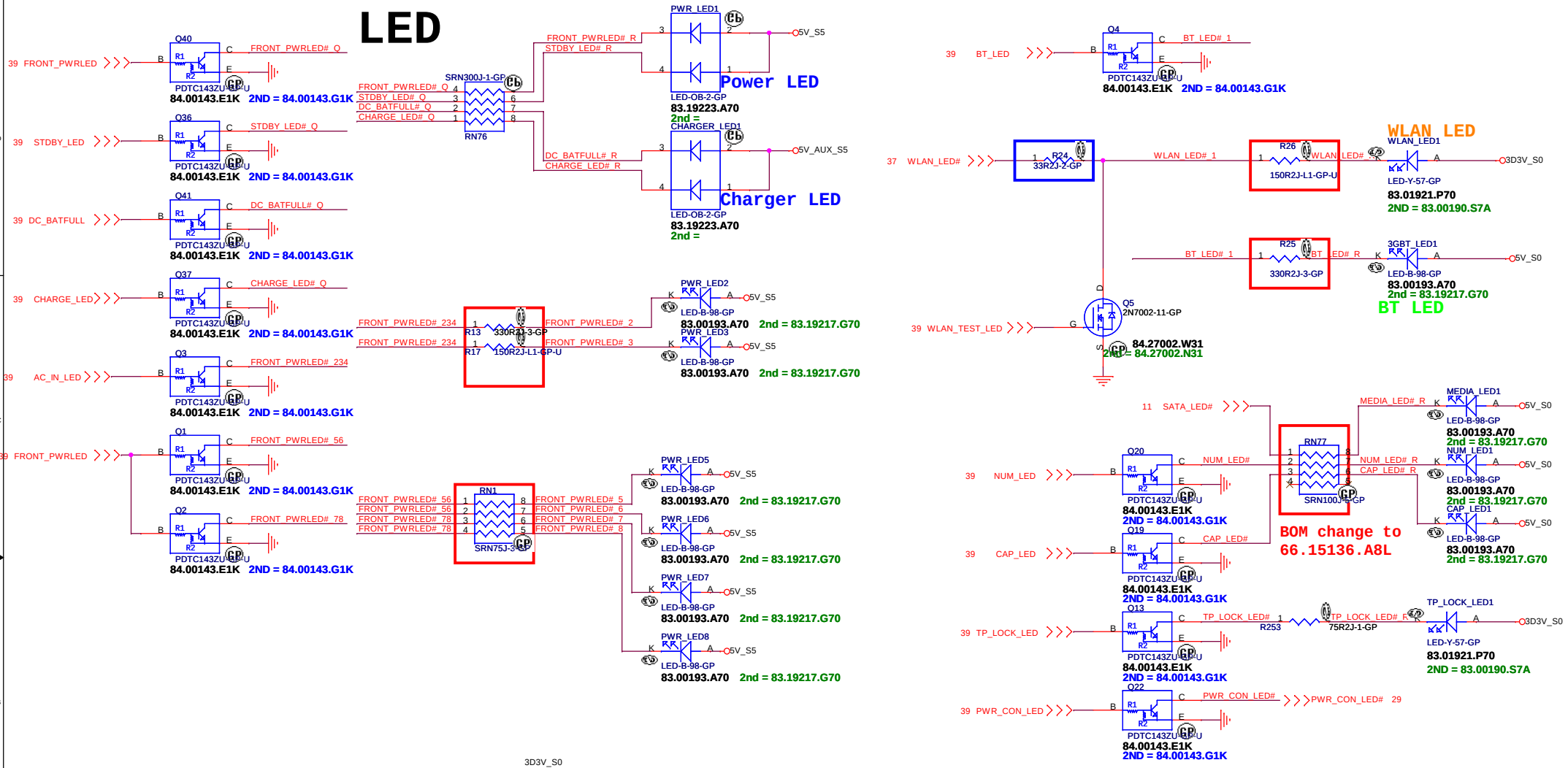
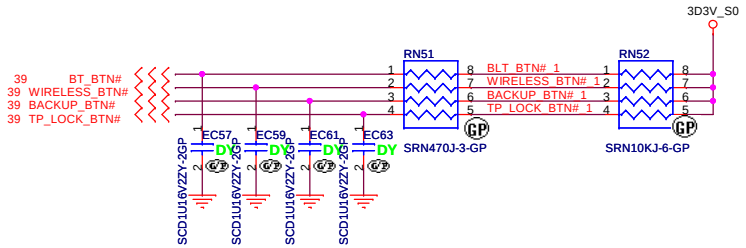
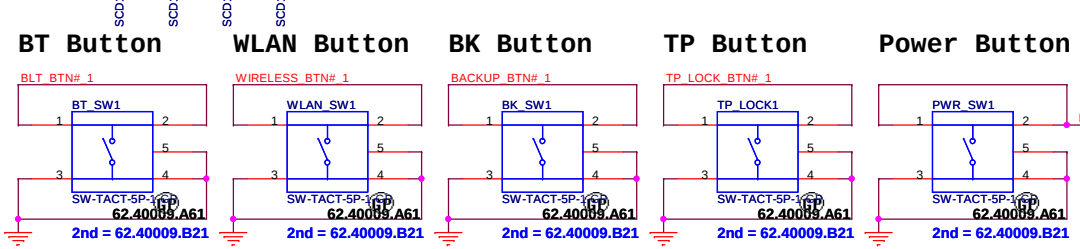
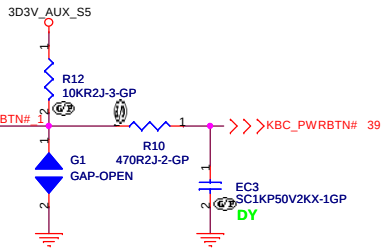
LED









JV70-CP

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Title: **LED&POWERBD CONN**

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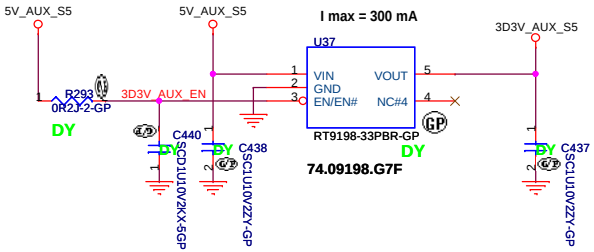
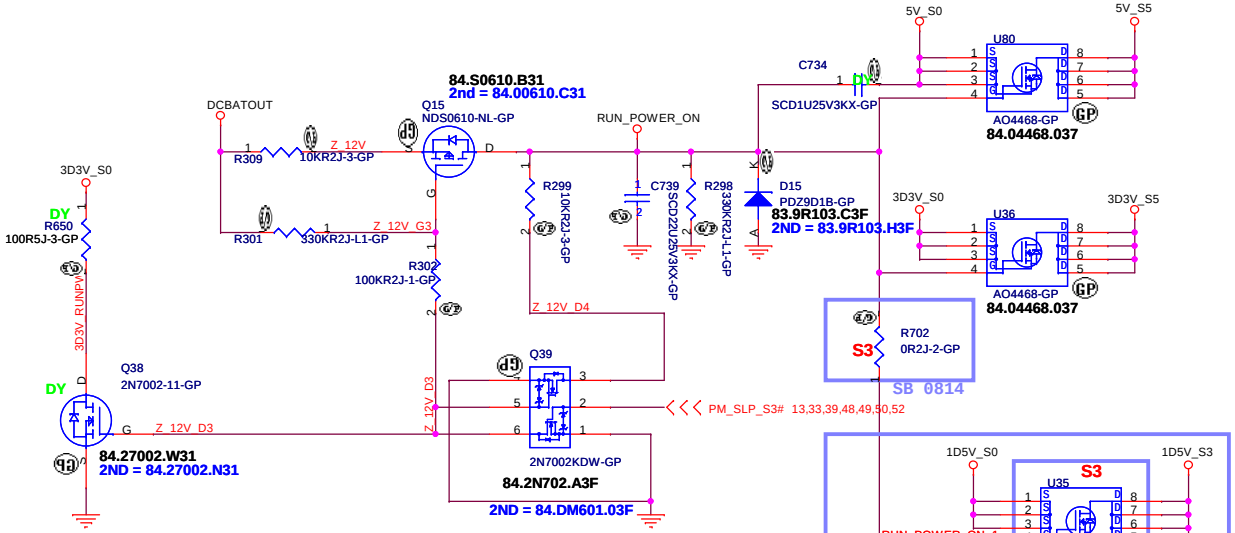
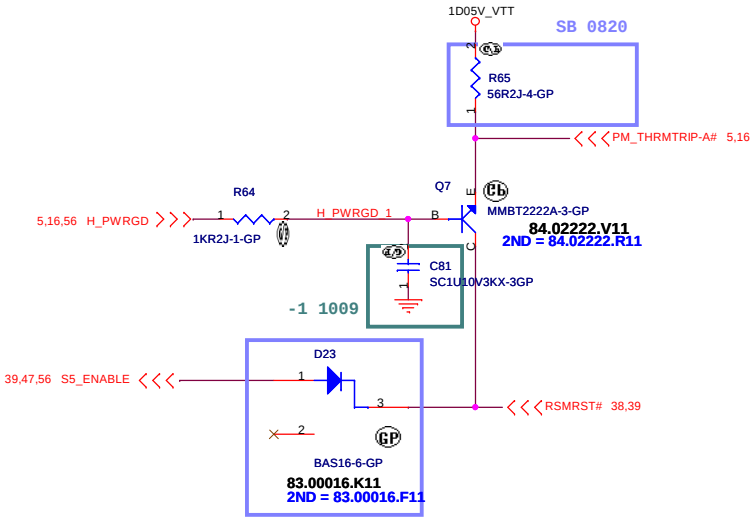
Aux Power

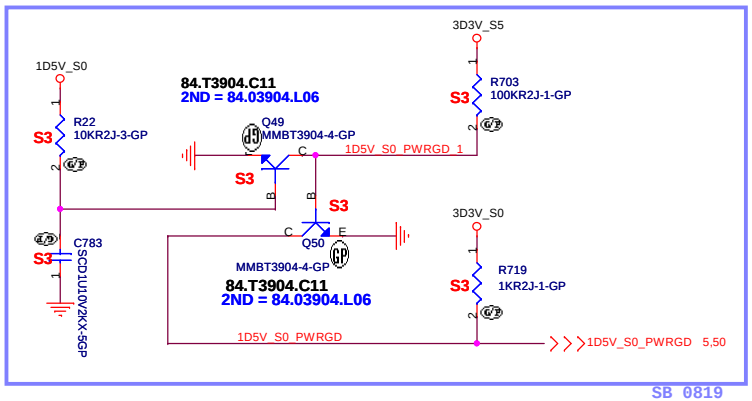
3D3V_AUX_S5

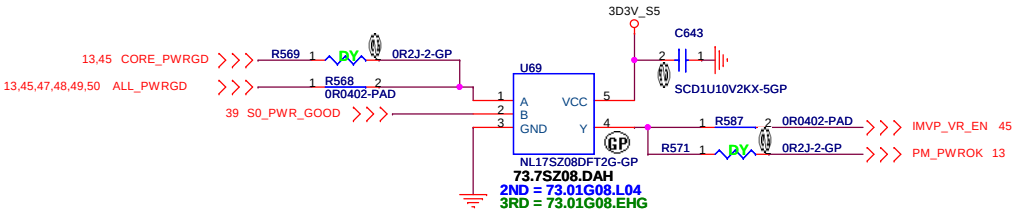


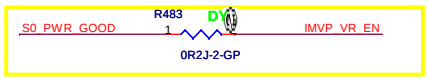
Run Power











JV70-CP

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Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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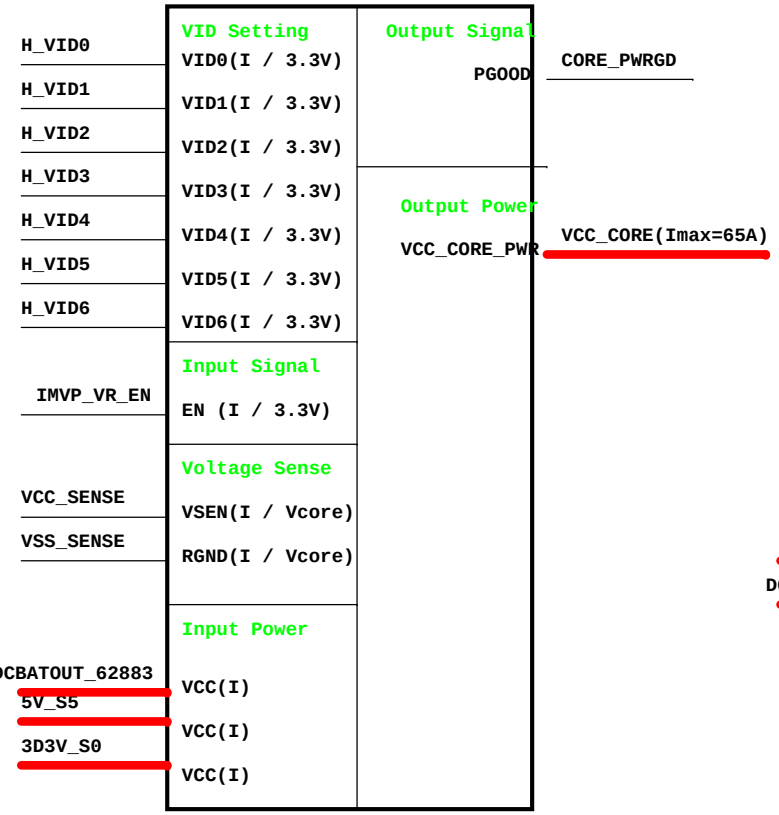
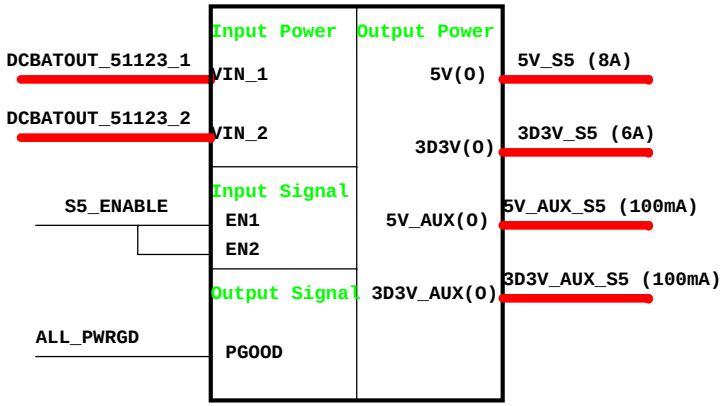
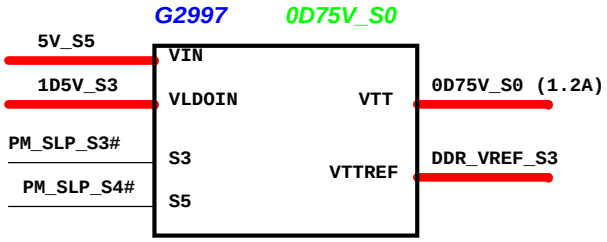
ISL62883 VCC_CORE



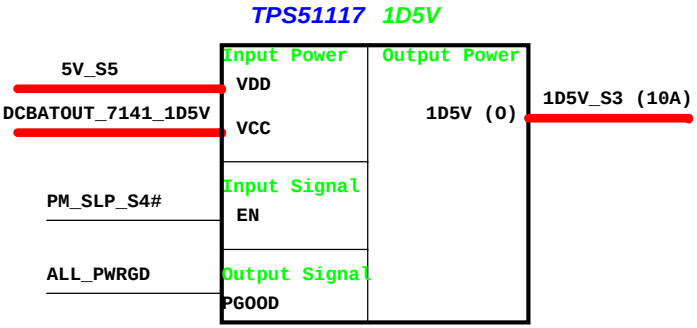
TPS51123 5V/3D3V



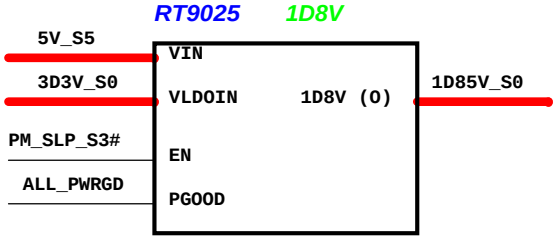
G2997 0D75V_S0



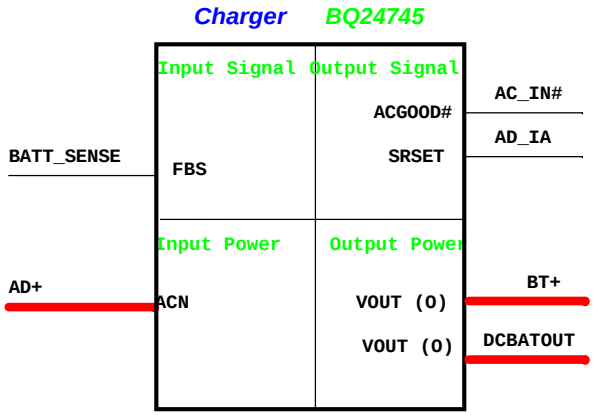
TPS51117 1D5V



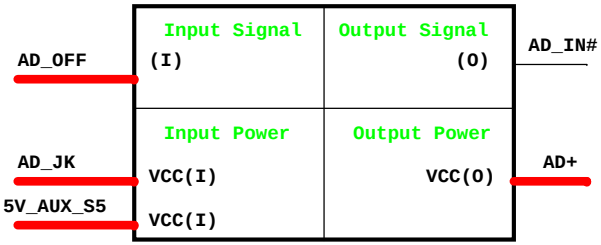
RT9025 1D8V



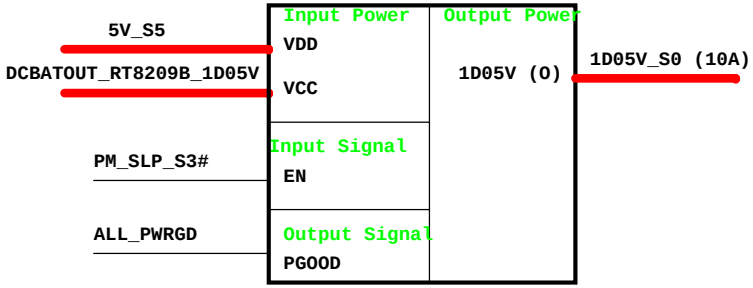
Charger BQ24745



Adapter



TPS51117 1D05V



JV70-CP

緯創資通 **Wistron Corporation**
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Title: **Power Block Diagram**

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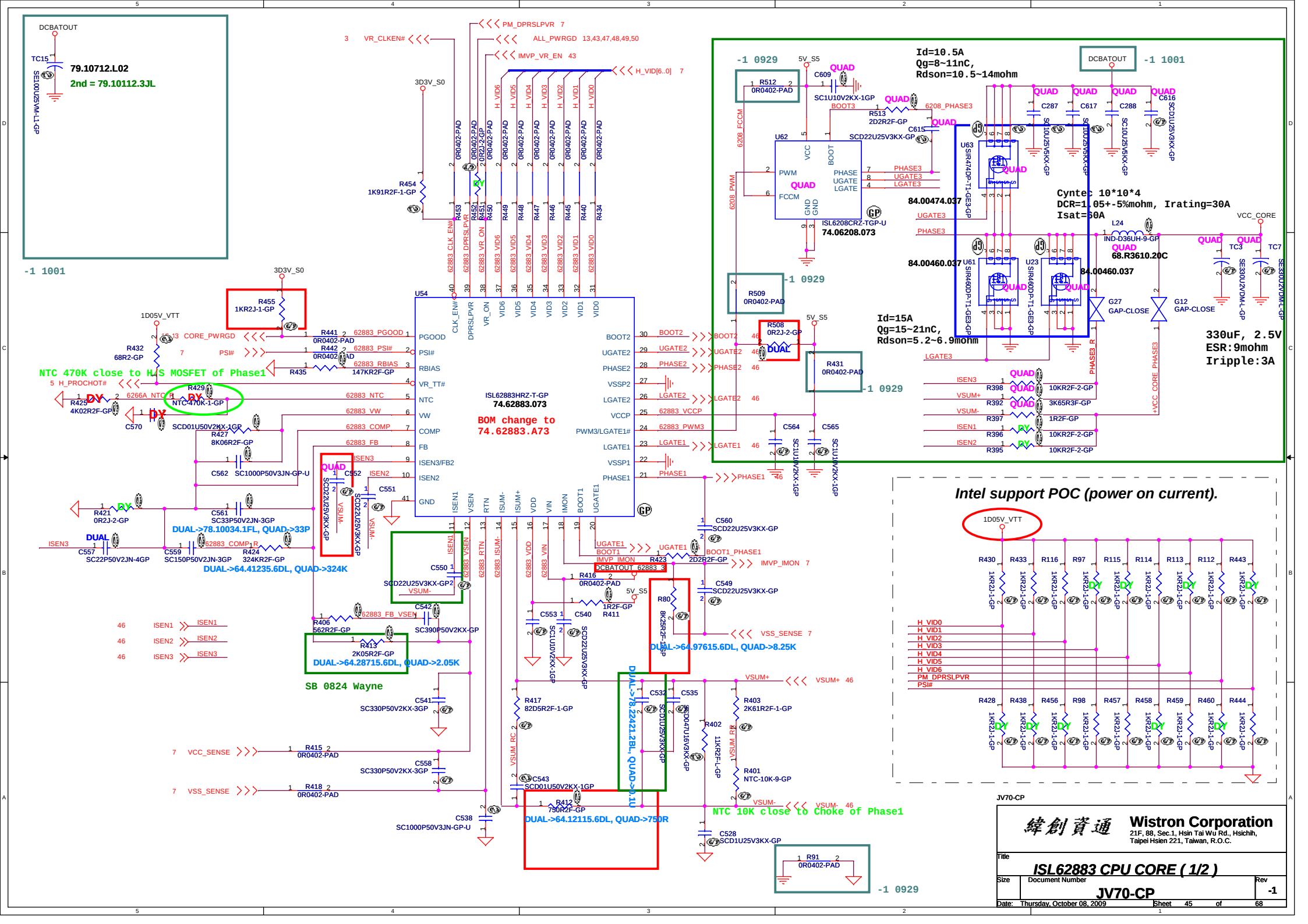
DCBATOUT
TC15
SE100U25VM-L1-GP
79.10712.L02
2nd = 79.10112.3JL
-1 1001
3D3V_S0
1D05V_VTT
VR_CLKEN# 3
PM_DPRSLPVR 7
ALL_PWRGD 13,43,47,48,49,50
IMVP_VR_EN 43
H_VID[6..0] 7
U54
ISL62883HRZ-T-GP
74.62883.073
BOM change to
74.62883.A73
NTC 470K close to H/S MOSFET of Phase1
DUAL->78.10034.1FL, QUAD->33P
DUAL->64.41235.6DL, QUAD->324K
DUAL->64.28715.6DL, QUAD->2.05K
SB 0824 Wayne
DUAL->64.97615.6DL, QUAD->8.25K
DUAL->78.22421.2BL, QUAD->0.1U
DUAL->64.12115.6DL, QUAD->750R
NTC 10K close to Choke of Phase1
-1 0929
5V_S5
Id=10.5A
Qg=8~11nC,
Rdson=10.5~14mohm
ISL6208CRZ-TGP-U
74.06208.073
84.00474.037
84.00460.037
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=50A
VCC_CORE
L24
IND-D36UH-9-GP
68.R3610.20C
330uF, 2.5V
ESR:9mohm
Iripple:3A
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
Intel support POC (power on current).
JV70-CP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62883 CPU CORE (1/2)
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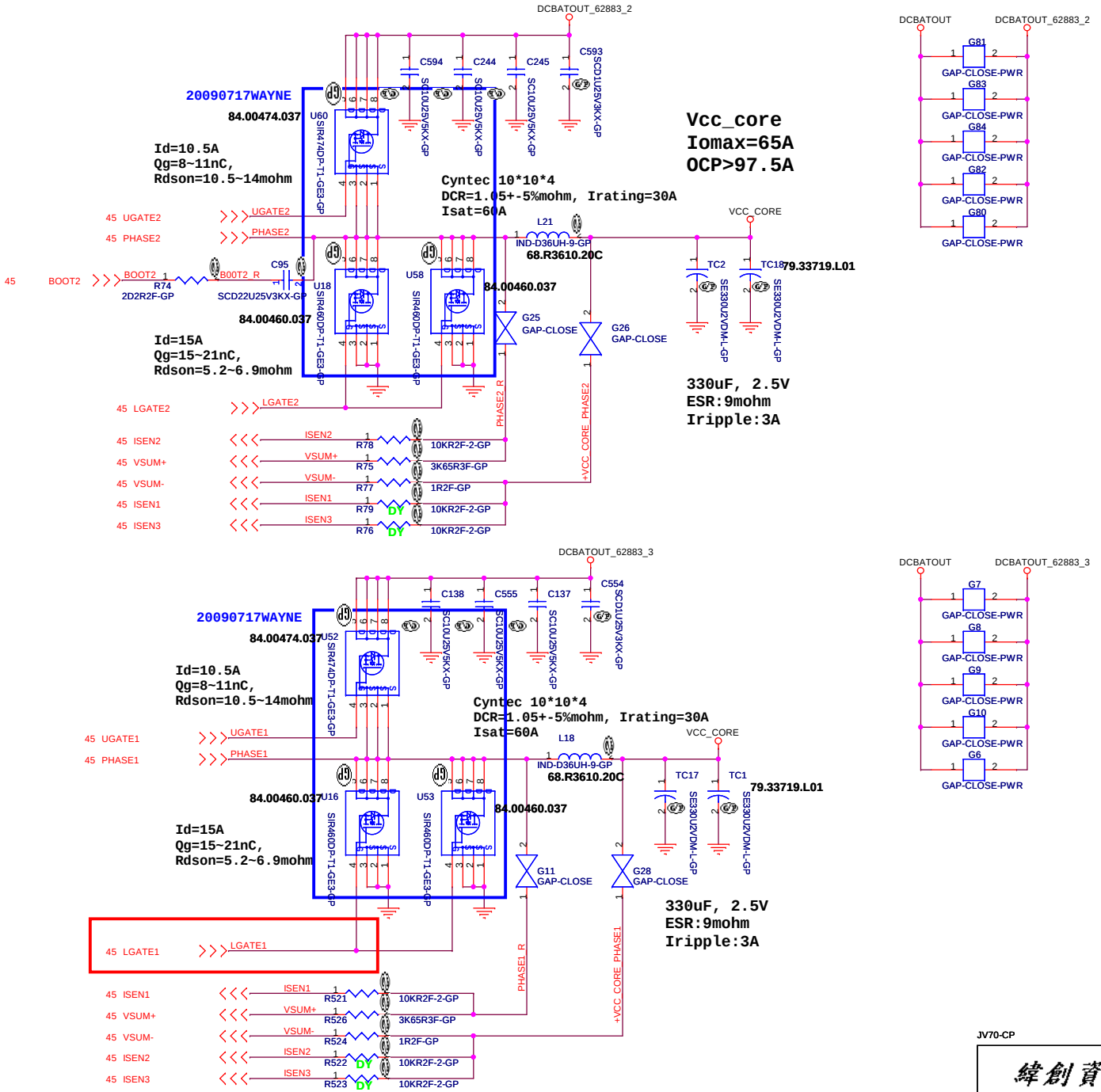

JV70-CP

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ISL62883 CPU CORE (1/2)***

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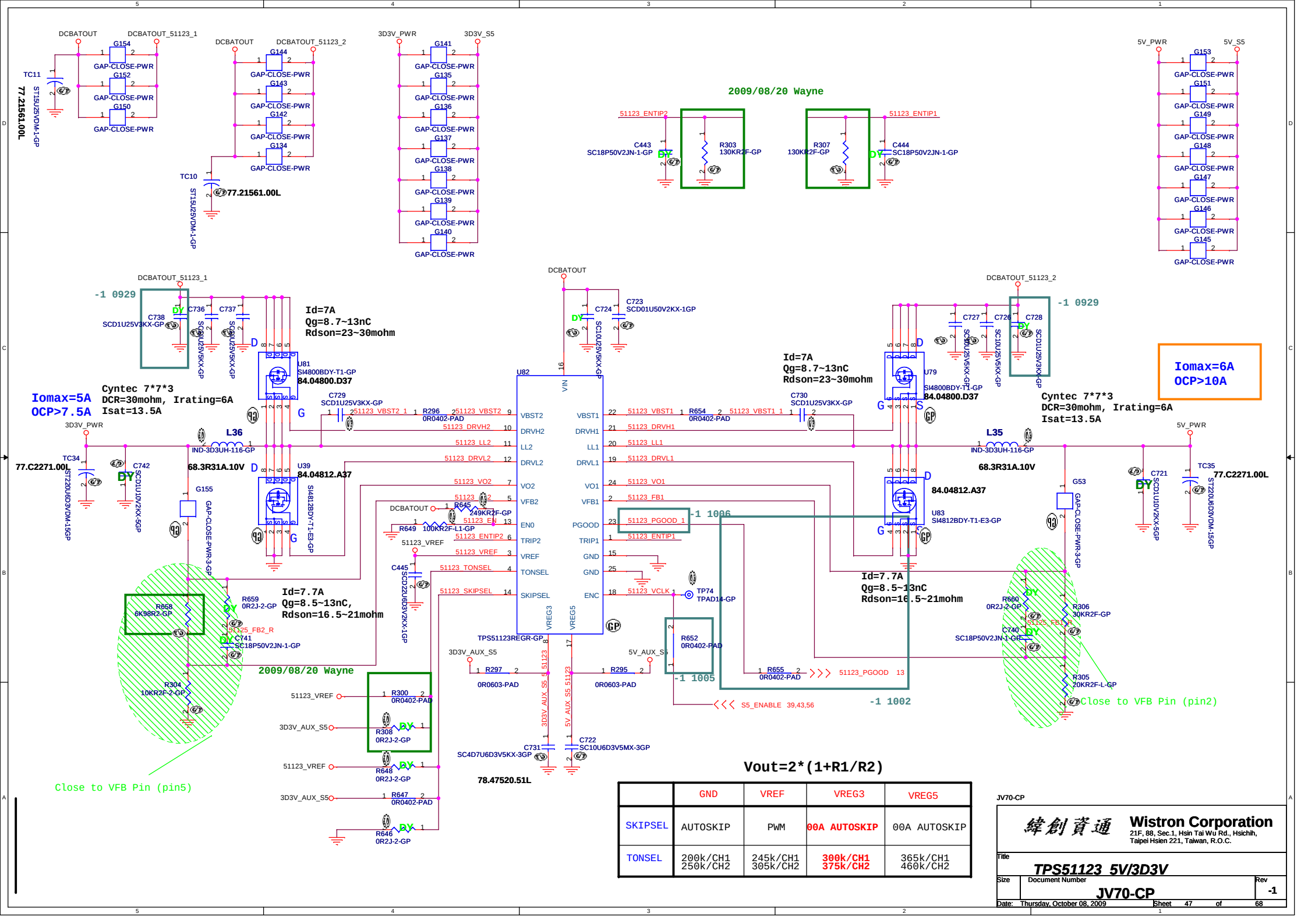

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

JV70-CP

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51123 5V/3D3V

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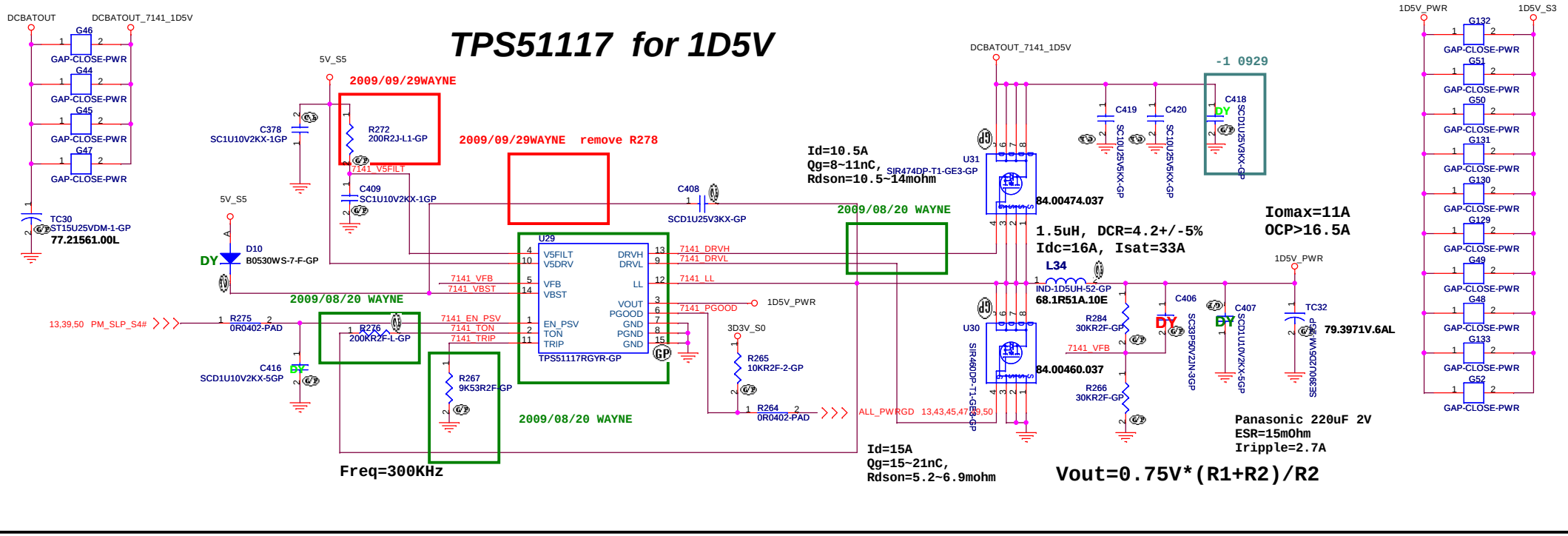
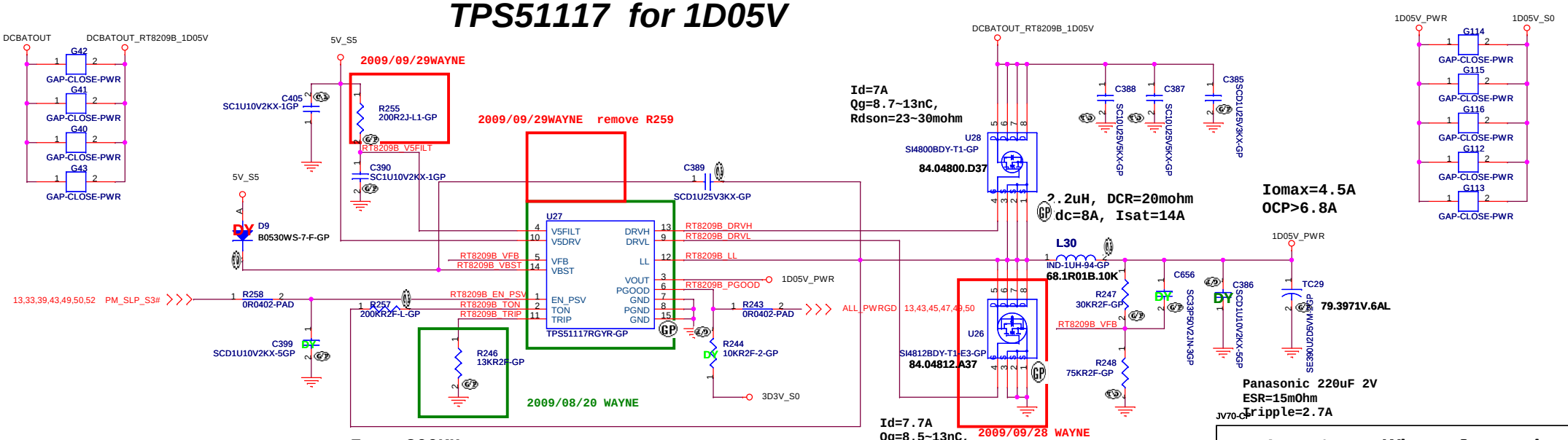
TPS51117 for 1D5V



TPS51117 for 1D05V



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51117 1D5V / TPS51117 1D05V

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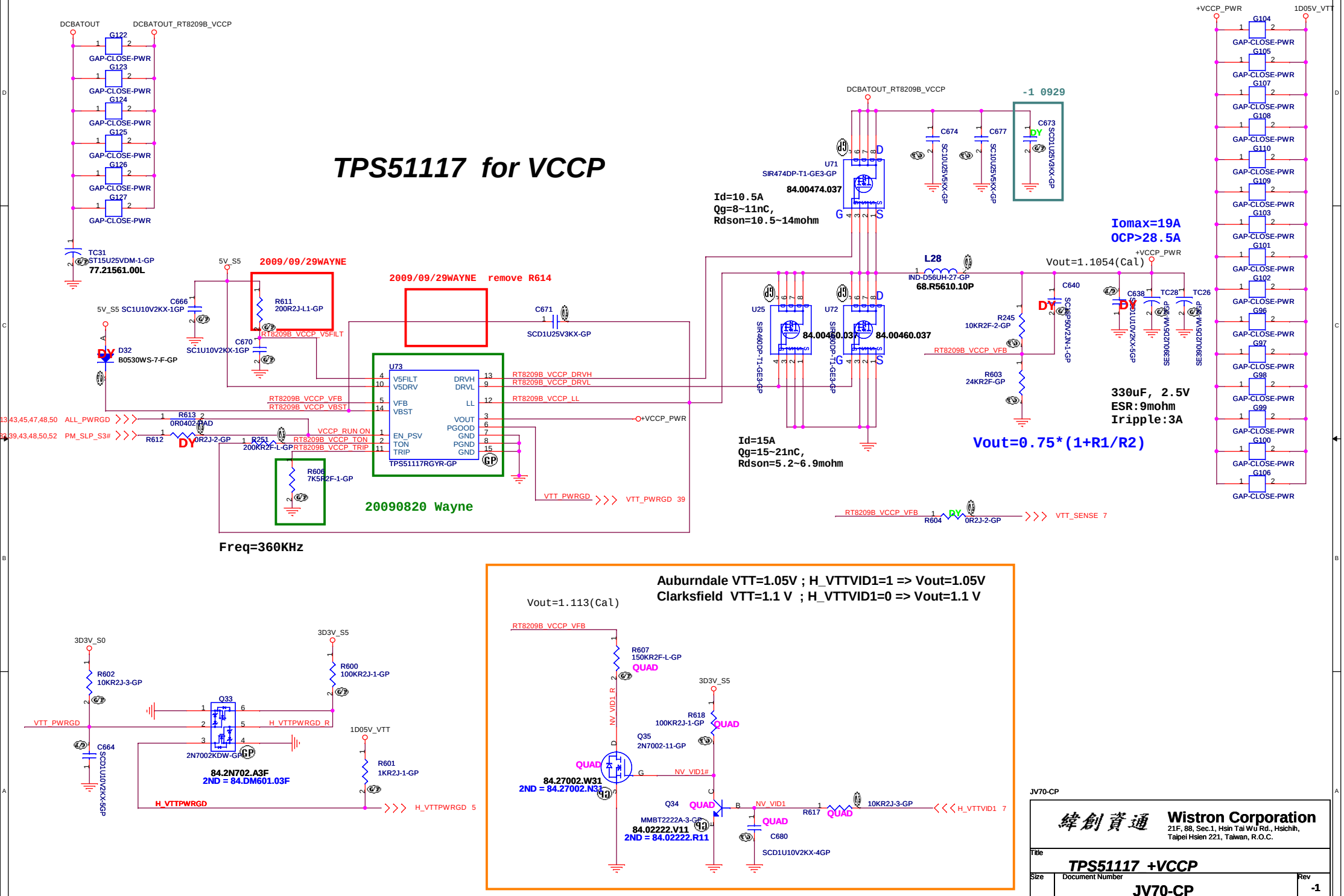
TPS51117 for VCCP
DCBATOUT
DCBATOUT_RT8209B_VCCP
G122
G123
G124
G125
G126
G127
GAP-CLOSE-PWR
TC31
ST15U25VDM-1-GP
77.21561.00L
5V_S5
2009/09/29WAYNE
R611
200R2J-L1-GP
C666
SC1U10V2KX-1GP
C670
D32
B0530WS-7-F-GP
DY
RT8209B_VCCP_V5FILT
2009/09/29WAYNE remove R614
C671
SCD1U25V3KX-GP
U73
V5FILT
V5DRV
VFB
VBST
EN_PSV
TON
TRIP
DRVH
DRVL
LL
VOUT
PGOOD
GND
PGND
TPS51117RGYR-GP
RT8209B_VCCP_DRVH
RT8209B_VCCP_DRVL
RT8209B_VCCP_LL
RT8209B_VCCP_VFB
RT8209B_VCCP_VBST
RT8209B_VCCP_TON
RT8209B_VCCP_TRIP
VCCP_RUN ON
ALL_PWRGD
PM_SLP_S3#
R613
0R0402-PAD
R612
0R2J-2-GP
R251
200KR2F-L-GP
R606
7K5R2F-1-GP
20090820 Wayne
+VCCP_PWR
VTT_PWRGD
VTT_PWRGD 39
Freq=360KHz
DCBATOUT_RT8209B_VCCP
-1 0929
C674
C677
C673
SC10U25V5KX-GP
SCD1U25V3KX-GP
U71
SIR474DP-T1-GE3-GP
84.00474.037
Id=10.5A
Qg=8~11nC,
Rdson=10.5~14mohm
U25
U72
SIR460DP-T1-GE3-GP
84.00460.037
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
L28
IND-D56UH-27-GP
68.R5610.10P
Vout=1.1054(Cal)
Iomax=19A
OCP>28.5A
R245
10KR2F-2-GP
R603
24KR2F-GP
C640
SCD1U50V2JN-1-GP
C638
SCD1U10V2KX-5GP
TC28
SCD47U6V3M-GP
TC26
SE390U2D5VM-GP
330uF, 2.5V
ESR:9mohm
Iripple:3A
Vout=0.75*(1+R1/R2)
R604
0R2J-2-GP
VTT_SENSE 7
+VCCP_PWR
1D05V_VTT
G104
G105
G107
G108
G110
G109
G103
G101
G102
G96
G97
G98
G99
G100
G106
3D3V_S0
3D3V_S5
R602
10KR2J-3-GP
R600
100KR2J-1-GP
Q33
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
C664
SCD1U10V2KX-5GP
R601
1KR2J-1-GP
H_VTTPWRGD_R
H_VTTPWRGD
H_VTTPWRGD 5
Auburndale VTT=1.05V ; H_VTTVID1=1 => Vout=1.05V
Clarksfield VTT=1.1 V ; H_VTTVID1=0 => Vout=1.1 V
Vout=1.113(Cal)
R607
150KR2F-L-GP
QUAD
NV_VID1_R
R618
100KR2J-1-GP
Q35
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N33
NV_VID1#
Q34
MMBT2222A-3-GP
84.02222.V11
2ND = 84.02222.R11
NV_VID1
R617
10KR2J-3-GP
H_VTTVID1 7
C680
SCD1U10V2KX-4GP
JV70-CP
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51117 +VCCP
Size
Document Number
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-1
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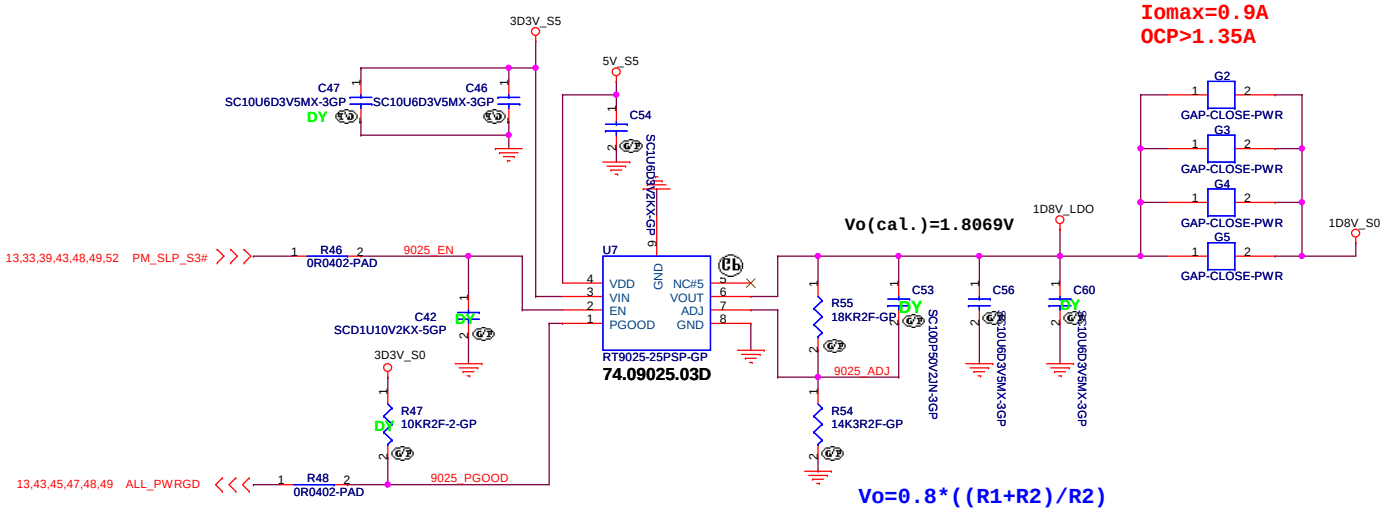
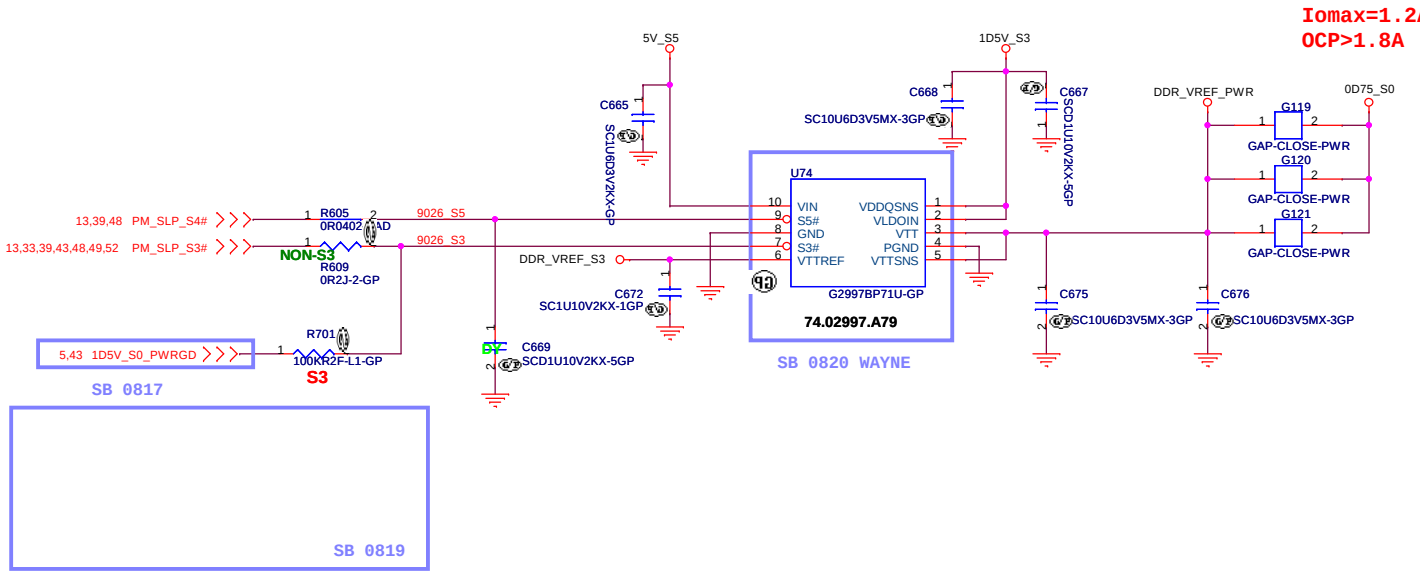
RT9025 for 1D8V_S0



G2997 for 0D75V_S3



JV70-CP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***RT9025_1D8V/G2997_0D75***
Size	Document Number: **JV70-CP** — Rev: **-1**
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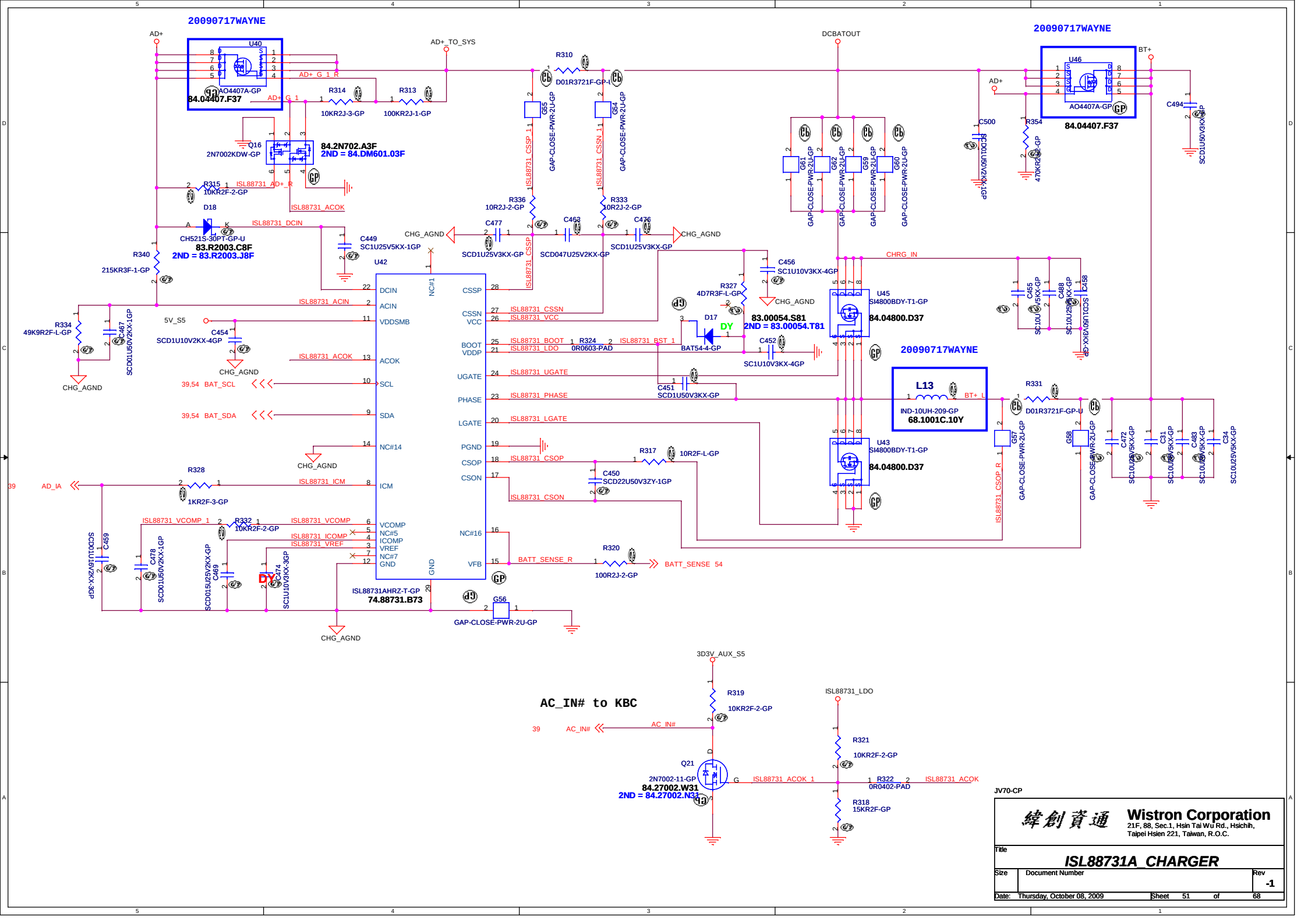
20090717WAYNE
AD+
U40
AO4407A-GP
84.04407.F37
AD+_TO_SYS
R310
D01R3721F-GP-U
R314
10KR2J-3-GP
R313
100KR2J-1-GP
Q16
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
R315
10KR2F-2-GP
ISL88731_AD+_R
D18
ISL88731_ACOK
ISL88731_DCIN
CH521S-30PT-GP-U
83.R2003.C8F
2ND = 83.R2003.J8F
C449
SC1U25V5KX-1GP
R340
215KR3F-1-GP
U42
CHG_AGND
C477
SCD1U25V3KX-GP
C463
SCD047U25V2KX-GP
C476
SCD1U25V3KX-GP
R336
10R2J-2-GP
R333
10R2J-2-GP
ISL88731_CSSP_1
ISL88731_CSSN_1
GAP-CLOSE-PWR-2U-GP
G55
G54
DCBATOUT
G61
G62
G59
G60
C500
SCD01U50V2KX-1GP
R354
470KR2J-GP
U46
AO4407A-GP
84.04407.F37
BT+
C494
SCD1U50V3KX-GP
CHRG_IN
C456
SC1U10V3KX-4GP
R327
4D7R3F-L-GP
83.00054.S81
2ND = 83.00054.T81
U45
SI4800BDY-T1-GP
84.04800.D37
C455
SC10U25V5KX-GP
C488
SC10U25V5KX-GP
C458
SCD1U50V3KX-GP
D17
DY
BAT54-4-GP
C452
SC1U10V3KX-4GP
R324
0R0603-PAD
ISL88731_BST_1
ISL88731_BOOT
ISL88731_LDO
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
C451
SCD1U50V3KX-GP
L13
IND-10UH-209-GP
68.1001C.10Y
BT+_L
R331
D01R3721F-GP-U
U43
SI4800BDY-T1-GP
84.04800.D37
ISL88731_CSOP_R
G57
G58
GAP-CLOSE-PWR-2U-GP
C472
C31
C483
C34
SC10U25V5KX-GP
R317
10R2F-L-GP
C450
SCD22U50V3ZY-1GP
ISL88731_CSOP
ISL88731_CSON
R328
1KR2F-3-GP
AD_IA
ISL88731_ICM
ISL88731_VCOMP_1
R332
10KR2F-2-GP
ISL88731_VCOMP
ISL88731_ICOMP
ISL88731_VREF
C459
SCD01U16V2KX-3GP
C478
SCD01U50V2KX-1GP
C469
SCD015U25V2KX-GP
C474
SC1U10V3KX-3GP
DY
ISL88731AHRZ-T-GP
74.88731.B73
R320
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE
G56
GAP-CLOSE-PWR-2U-GP
AC_IN# to KBC
3D3V_AUX_S5
R319
10KR2F-2-GP
AC_IN#
Q21
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N33
ISL88731_ACOK_1
R322
0R0402-PAD
R321
10KR2F-2-GP
R318
15KR2F-GP
JV70-CP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A_CHARGER
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Date: Thursday, October 08, 2009
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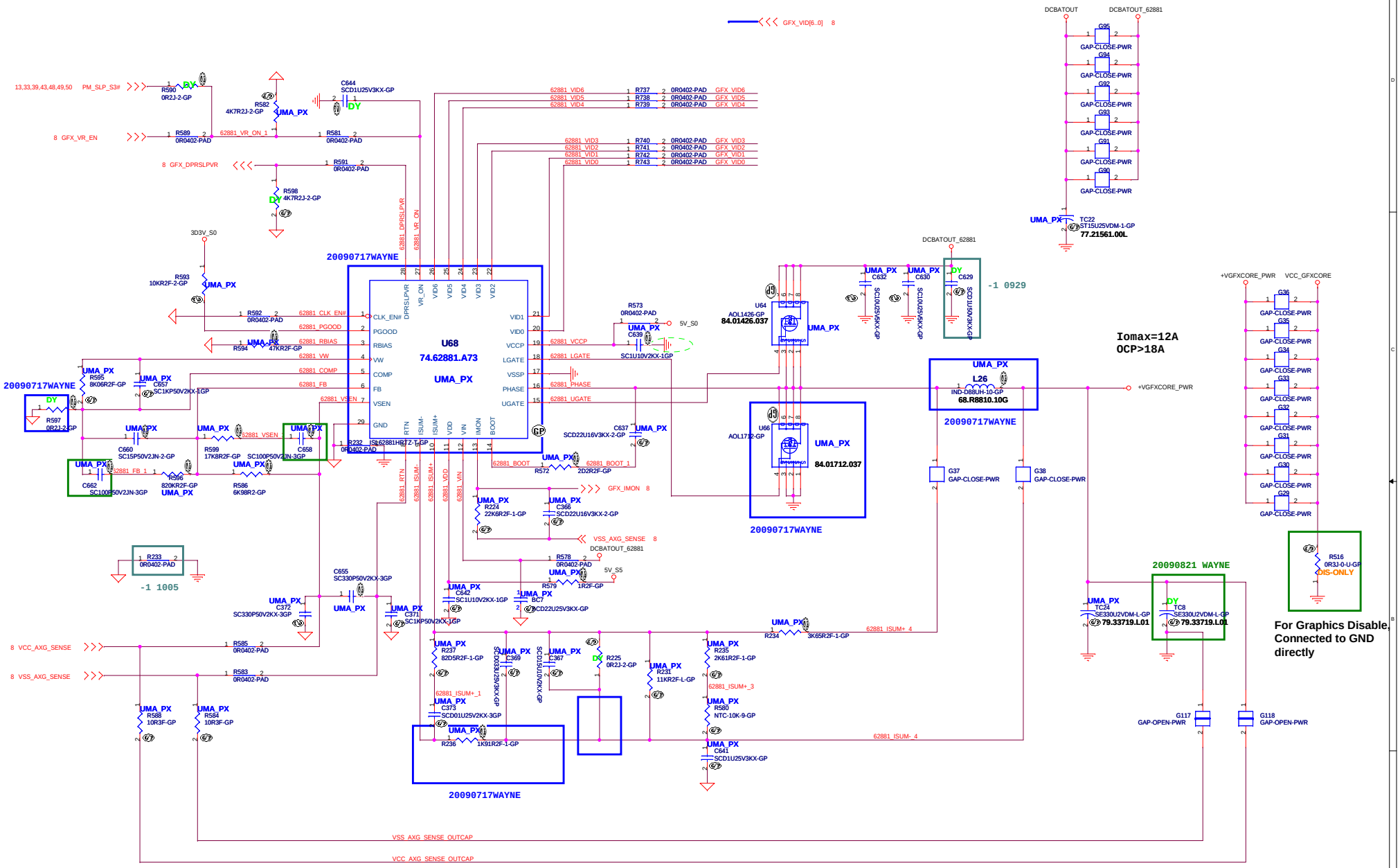
U68
74.62881.A73
UMA_PX
20090717WAYNE
ISL62881HRTZ-T-GP
CLK_EN#
PGOOD
RBIAS
VW
COMP
FB
VSEN
GND
VID1
VID0
VCCP
LGATE
VSSP
PHASE
UGATE
RTN
ISUM-
ISUM+
VDD
VIN
IMON
BOOT
DPRSLPVR
VR_ON
VID6
VID5
VID4
VID3
VID2
62881_VR_ON_1
62881_DPRSLPVR
62881_CLK_EN#
62881_PGOOD
62881_RBIAS
62881_VW
62881_COMP
62881_FB
62881_VSEN
62881_VCCP
62881_LGATE
62881_PHASE
62881_UGATE
62881_BOOT
62881_BOOT_1
62881_RTN
62881_ISUM-
62881_ISUM+
62881_VDD
62881_VIN
62881_FB_1
62881_ISUM+_1
62881_ISUM+_3
62881_ISUM+_4
62881_ISUM-_4
GFX_VID[6..0]
GFX_IMON
VSS_AXG_SENSE
VCC_AXG_SENSE
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
PM_SLP_S3#
GFX_VR_EN
GFX_DPRSLPVR
3D3V_S0
5V_S0
5V_S5
DCBATOUT
DCBATOUT_62881
+VGFXCORE_PWR
VCC_GFXCORE
Iomax=12A
OCP>18A
-1 0929
-1 1005
20090821 WAYNE
For Graphics Disable, Connected to GND directly
DIS-ONLY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL62881_+VCC_GFXCORE
JV70-CP
Rev -1
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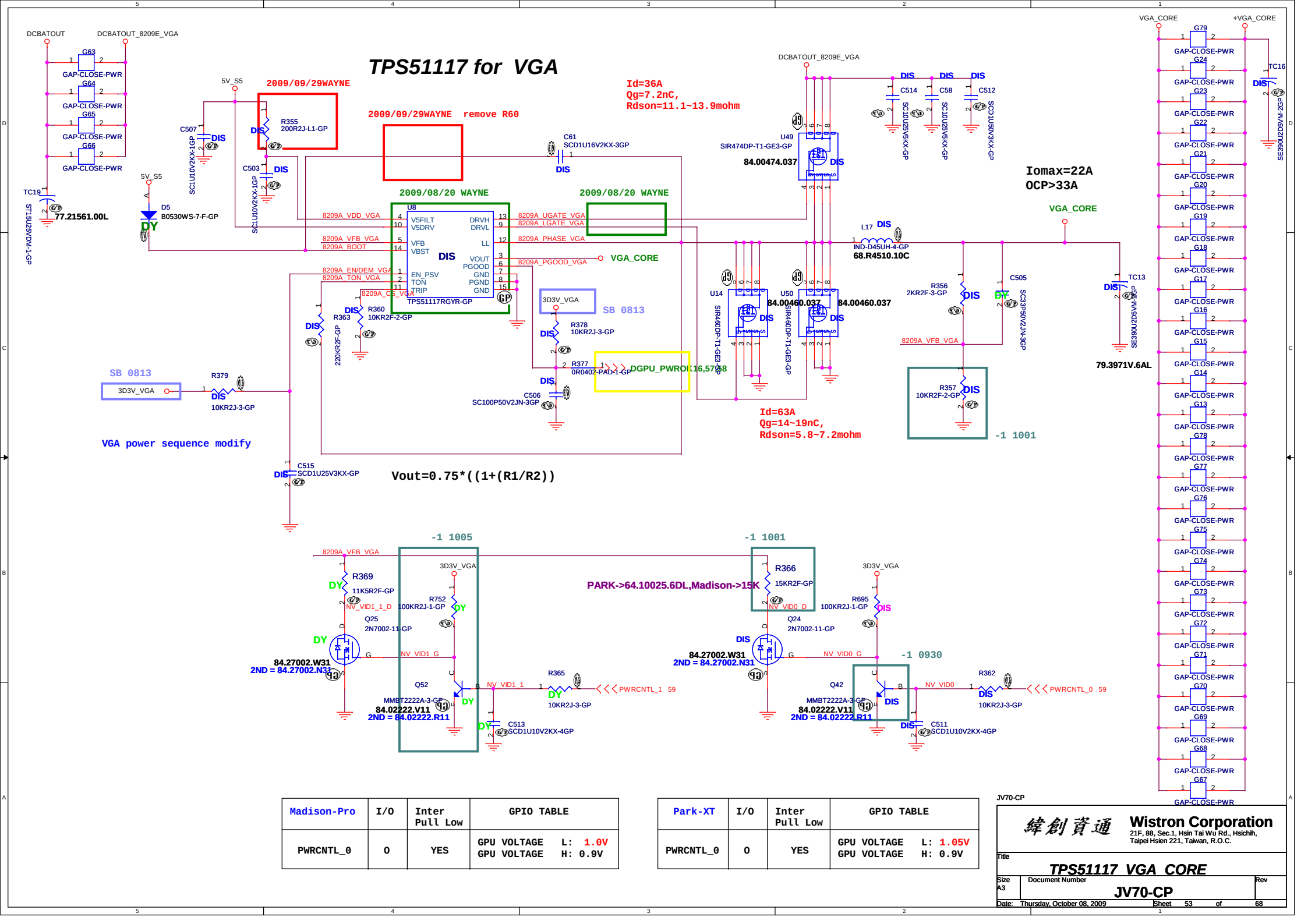
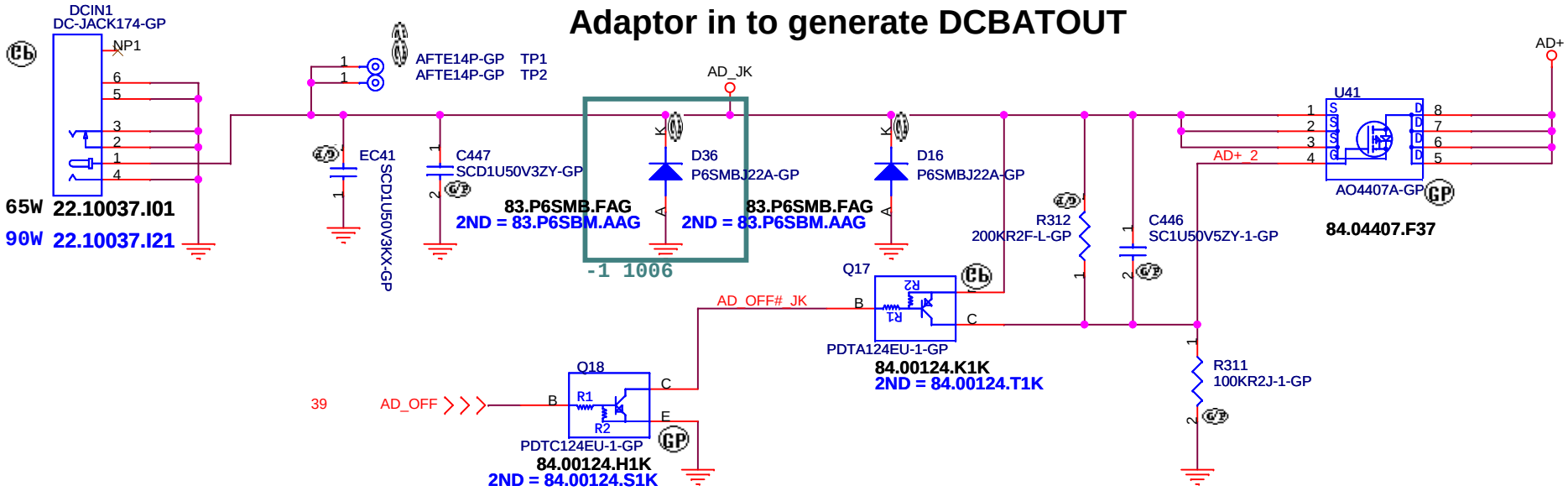


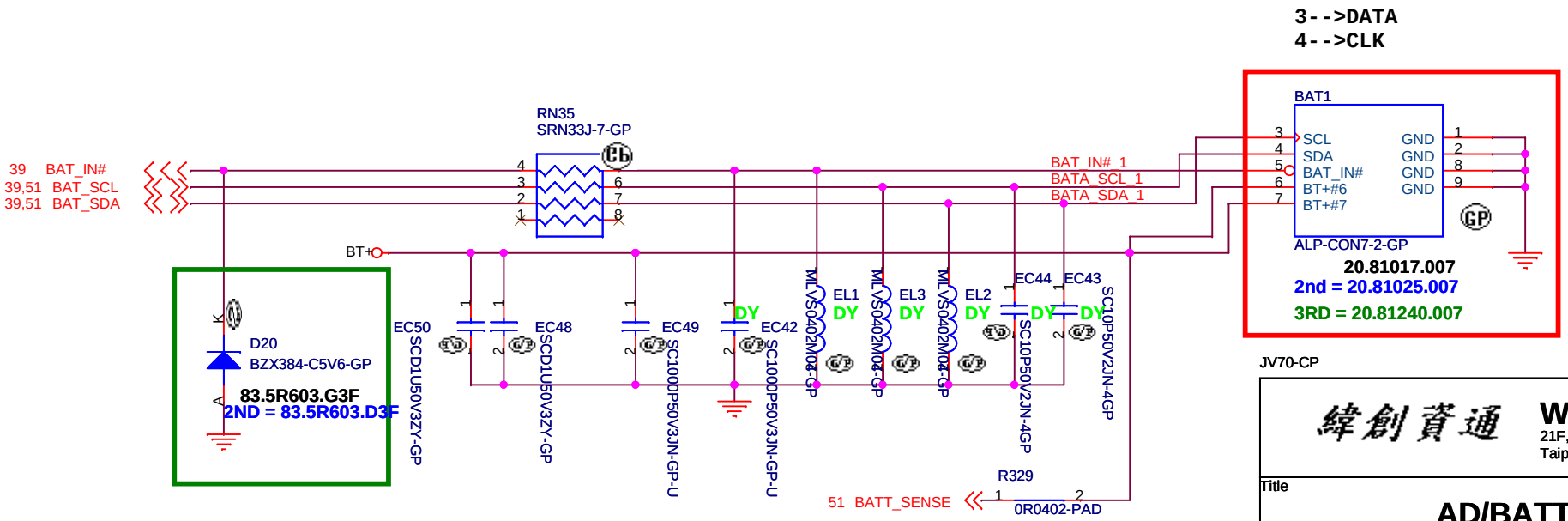
Madison-Pro	I/O	Inter Pull Low	GPIO TABLE
PWRCNTL_0	O	YES	GPU VOLTAGE L: 1.0V GPU VOLTAGE H: 0.9V

Park-XT	I/O	Inter Pull Low	GPIO TABLE
PWRCNTL_0	O	YES	GPU VOLTAGE L: 1.05V GPU VOLTAGE H: 0.9V

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



JV70-CP

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size	Document Number: JV70-CP	Rev: -1
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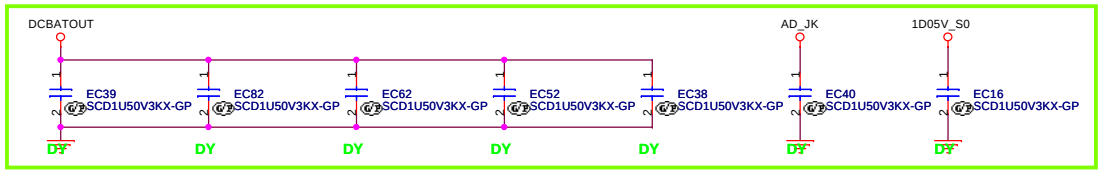
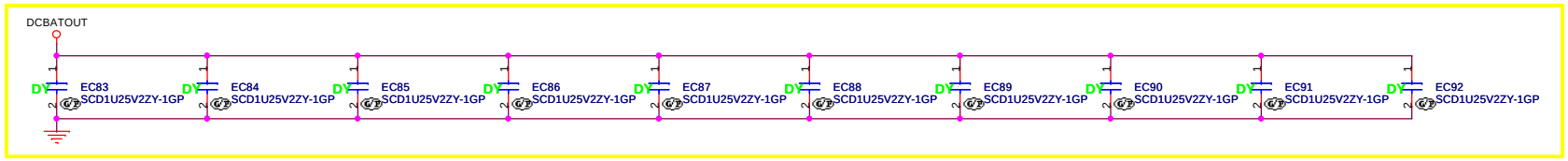
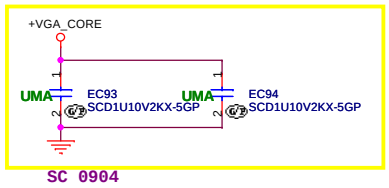
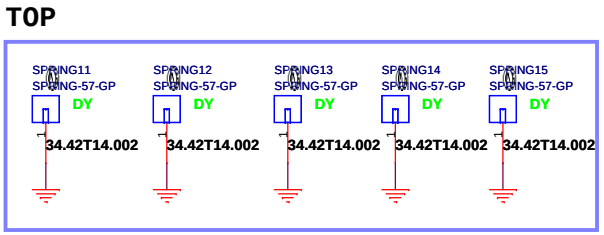
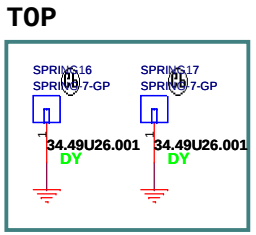


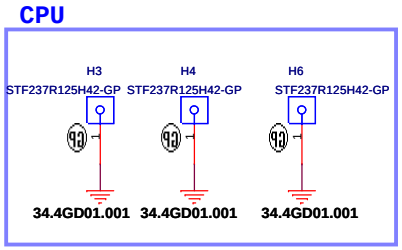


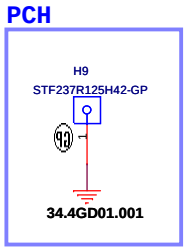


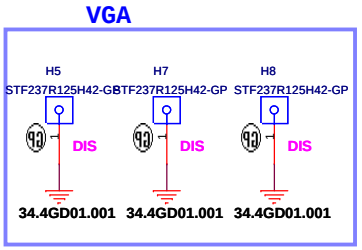


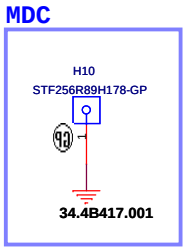


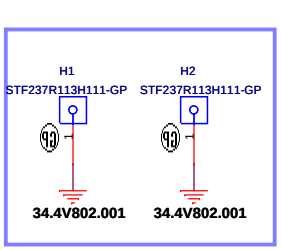
H1~H10 ALL IN TOP SIDE

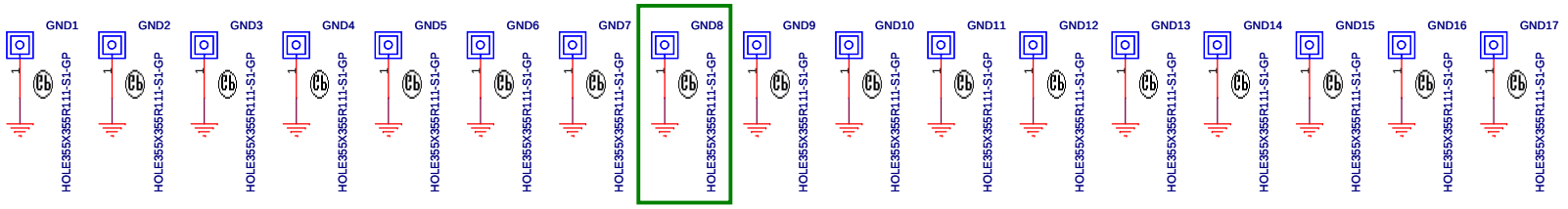


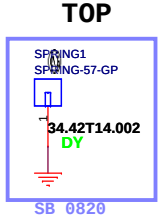


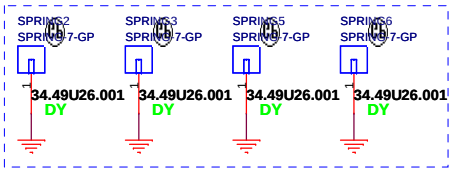


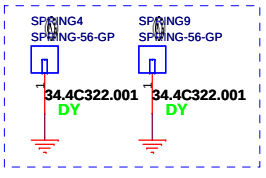


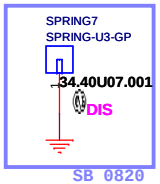


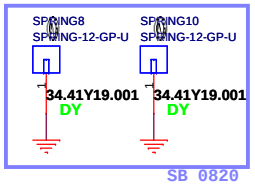








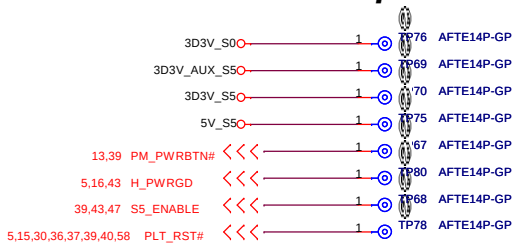




JV70-CP

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *EMI/Spring/Boss*		
Size	Document Number: JV70-CP	Rev: -1
Date: Tuesday, October 13, 2009	Sheet 55 of 68	

Check test point



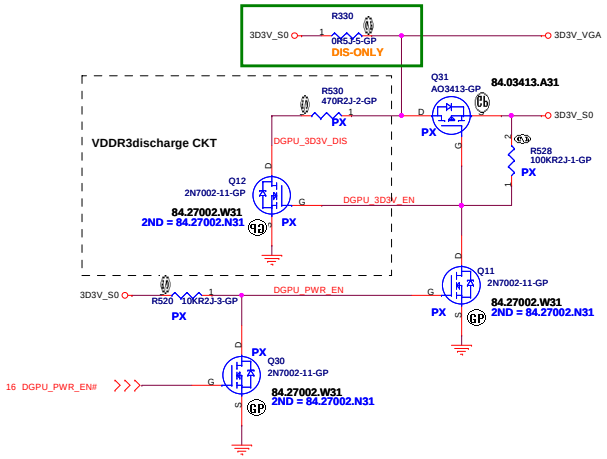
Test Point放在Dimm Door打開可量測處

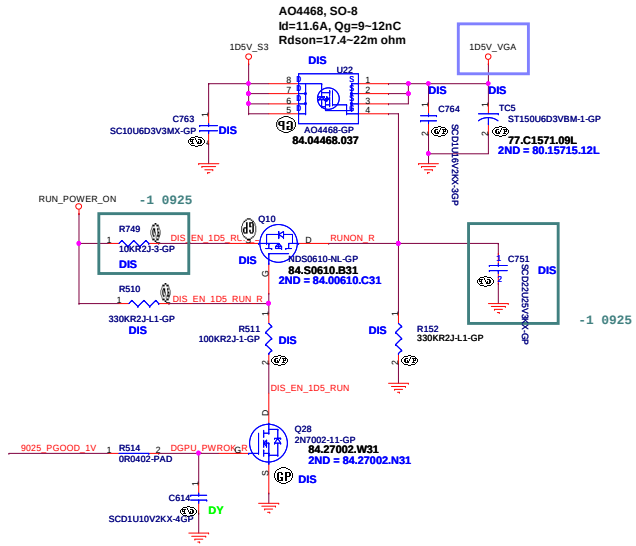
JV70-CP

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

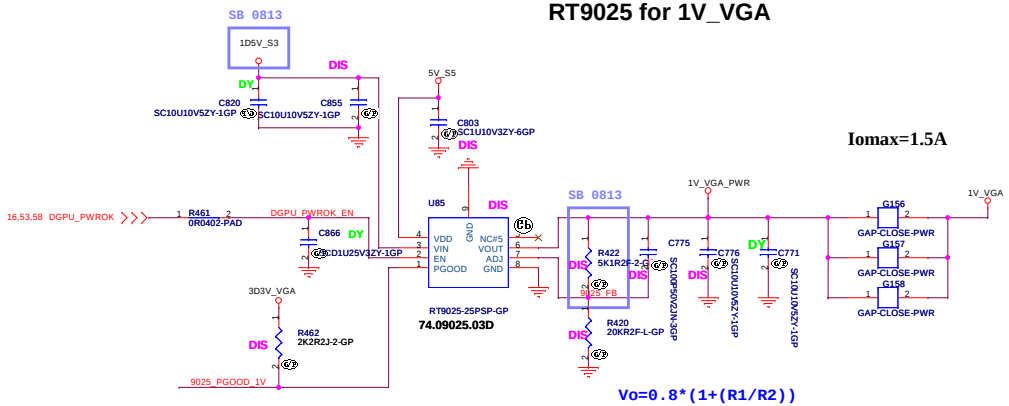
Title	***AFTE_TP***	
Size	Document Number **JV70-CP**	Rev **-1**
Date: Thursday, October 08, 2009	Sheet 56 of 68	

+3VS to 3.3V_DELAY Transfer

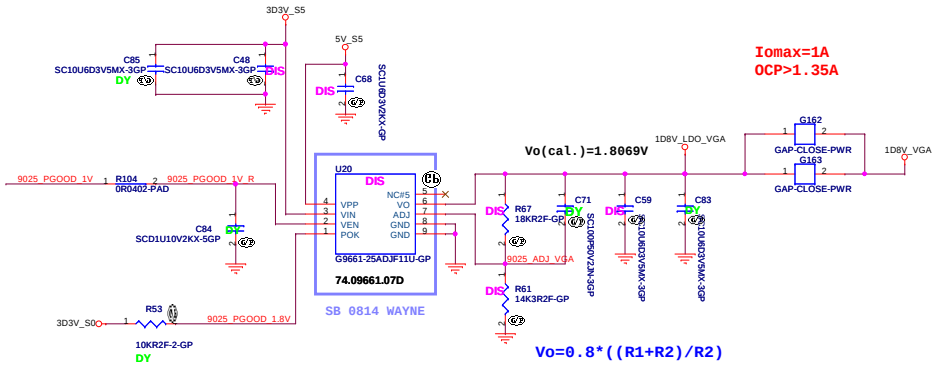




RT9025 for 1V_VGA



G9661 for 1D8V_VGA



JV70-CP

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI POWER

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Custom	JV70-CP	-1

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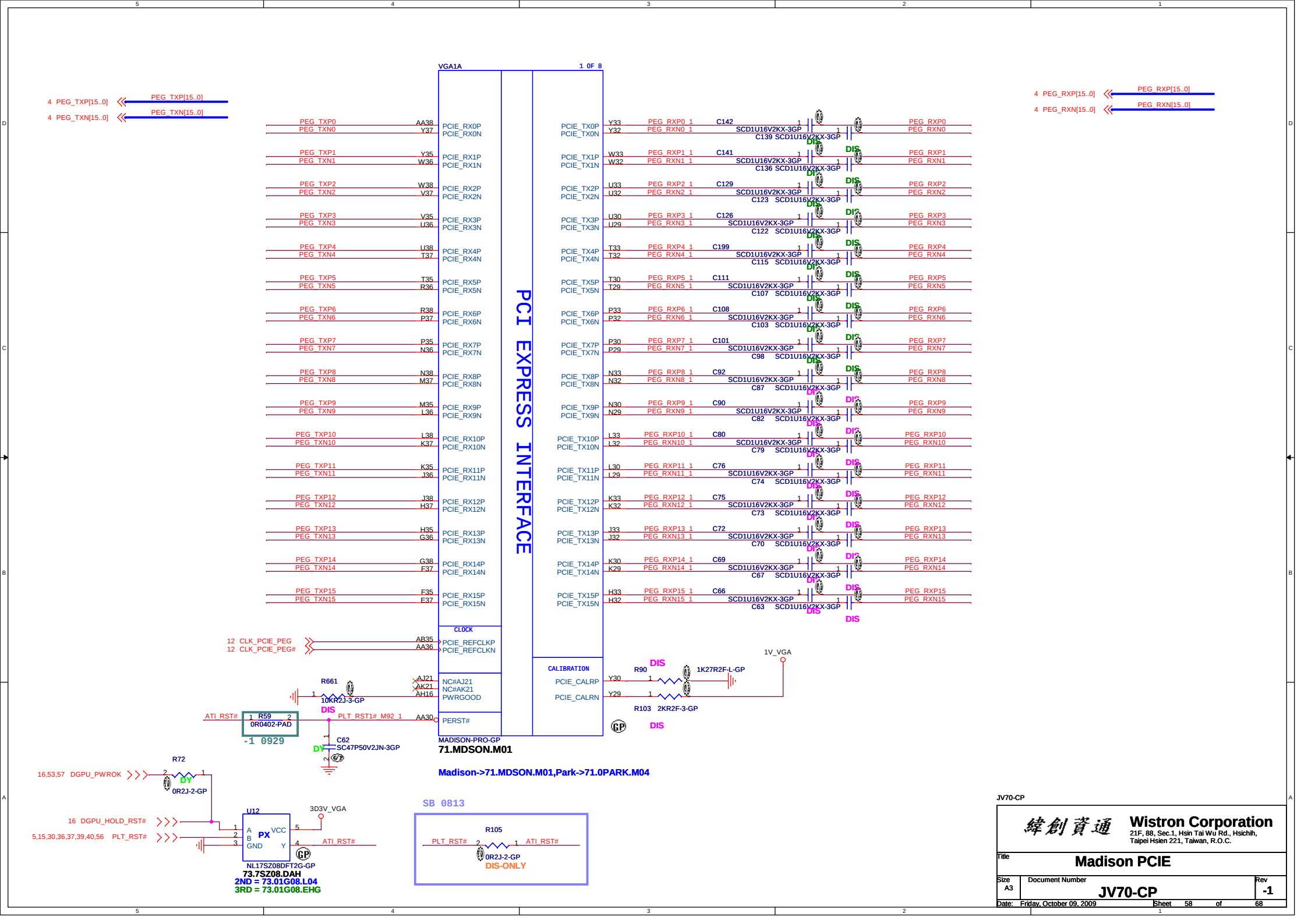

JV70-CP

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Madison PCIE**	
Size A3	Document Number **JV70-CP**	Rev -1
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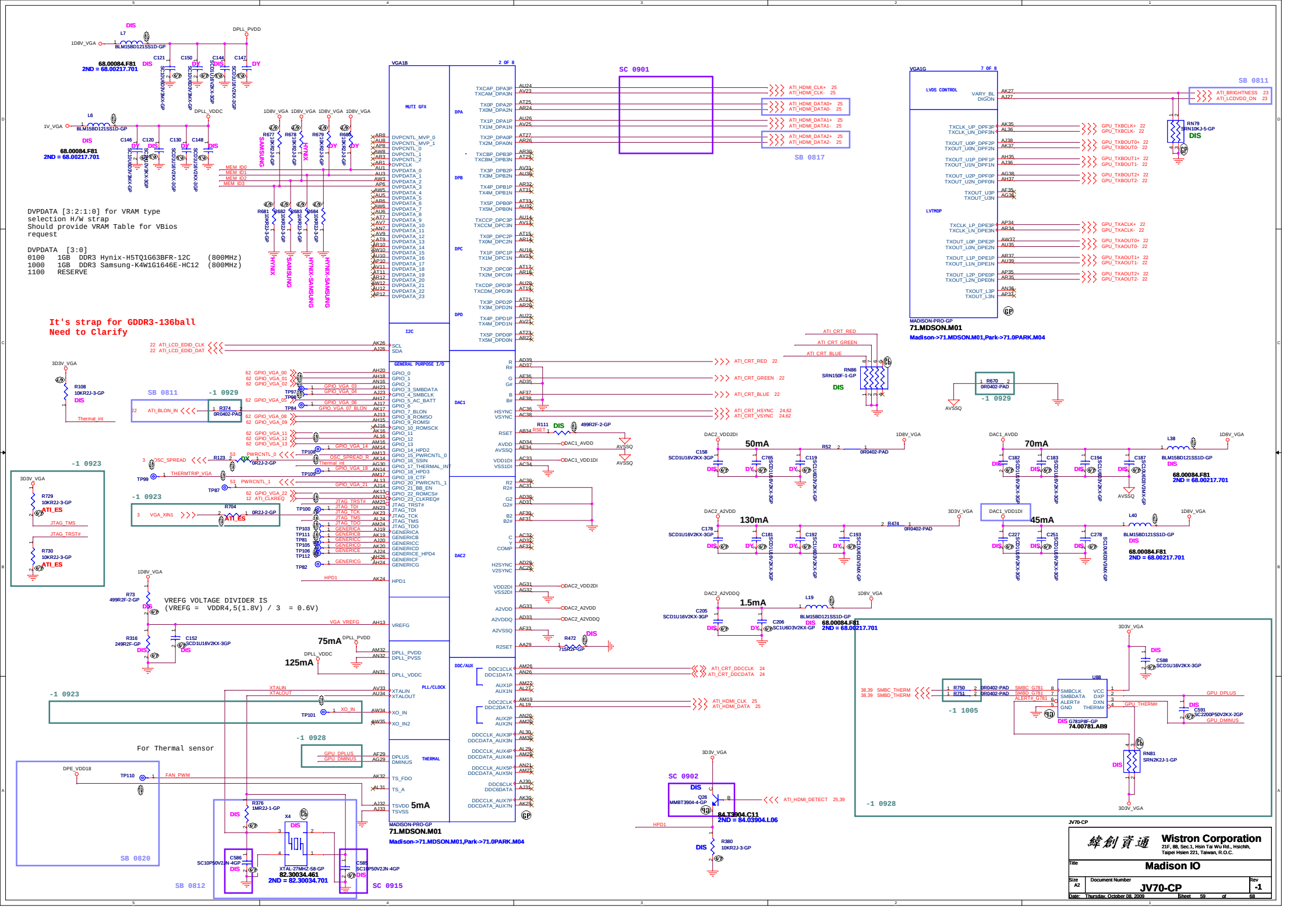
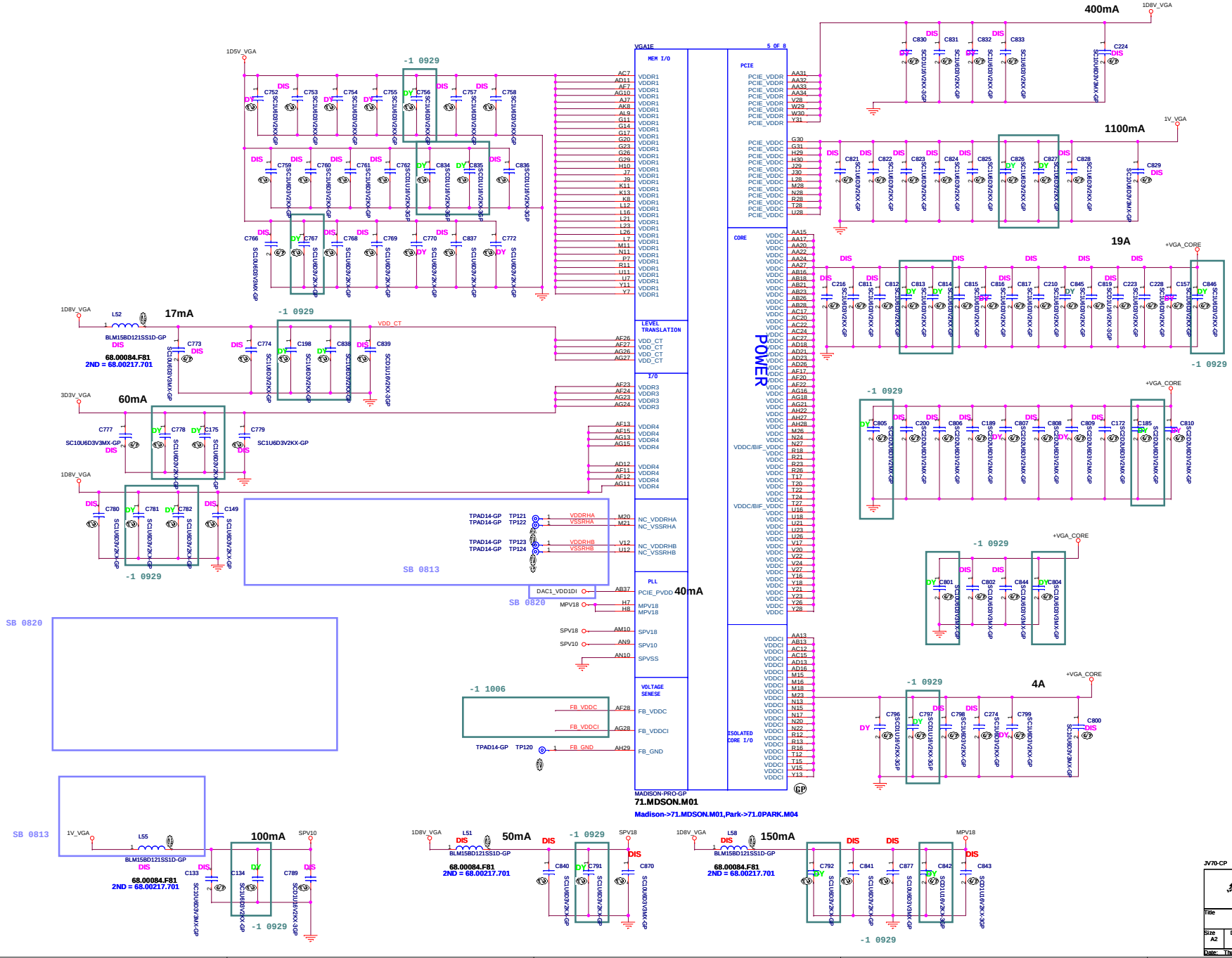

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
DVPDATA [3:0]
0100 1GB DDR3 Hynix-H5TQ1G63BFR-12C (800MHz)
1000 1GB DDR3 Samsung-K4W1G1646E-HC12 (800MHz)
1100 RESERVE
It's strap for GDDR3-136ball
Need to Clarify
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
For Thermal sensor
SC 0901
SB 0817
SB 0811
SB 0820
SB 0812
SC 0915
SC 0902
VGA1B
VGA1G
MADISON-PRO-GP
71.MDSON.M01
Madison->71.MDSON.M01,Park->71.0PARK.M04
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison IO
JV70-CP
Thursday, October 08, 2009


400mA
1100mA
19A
17mA
60mA
40mA
4A
100mA
50mA
150mA
-1 0929
-1 1006
SB 0813
SB 0820
VGA1E
MEM I/O
PCIE
CORE
POWER
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
ISOLATED CORE I/O
MADISON-PRO-GP
71.MDSON.M01
Madison->71.MDSON.M01,Park->71.0PARK.M04
68.00084.F81
2ND = 68.00217.701
BLM15BD121SS1D-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
JV70-CP
Madison POWER
Size A2
Document Number
JV70-CP
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Date: Thursday, October 08, 2009
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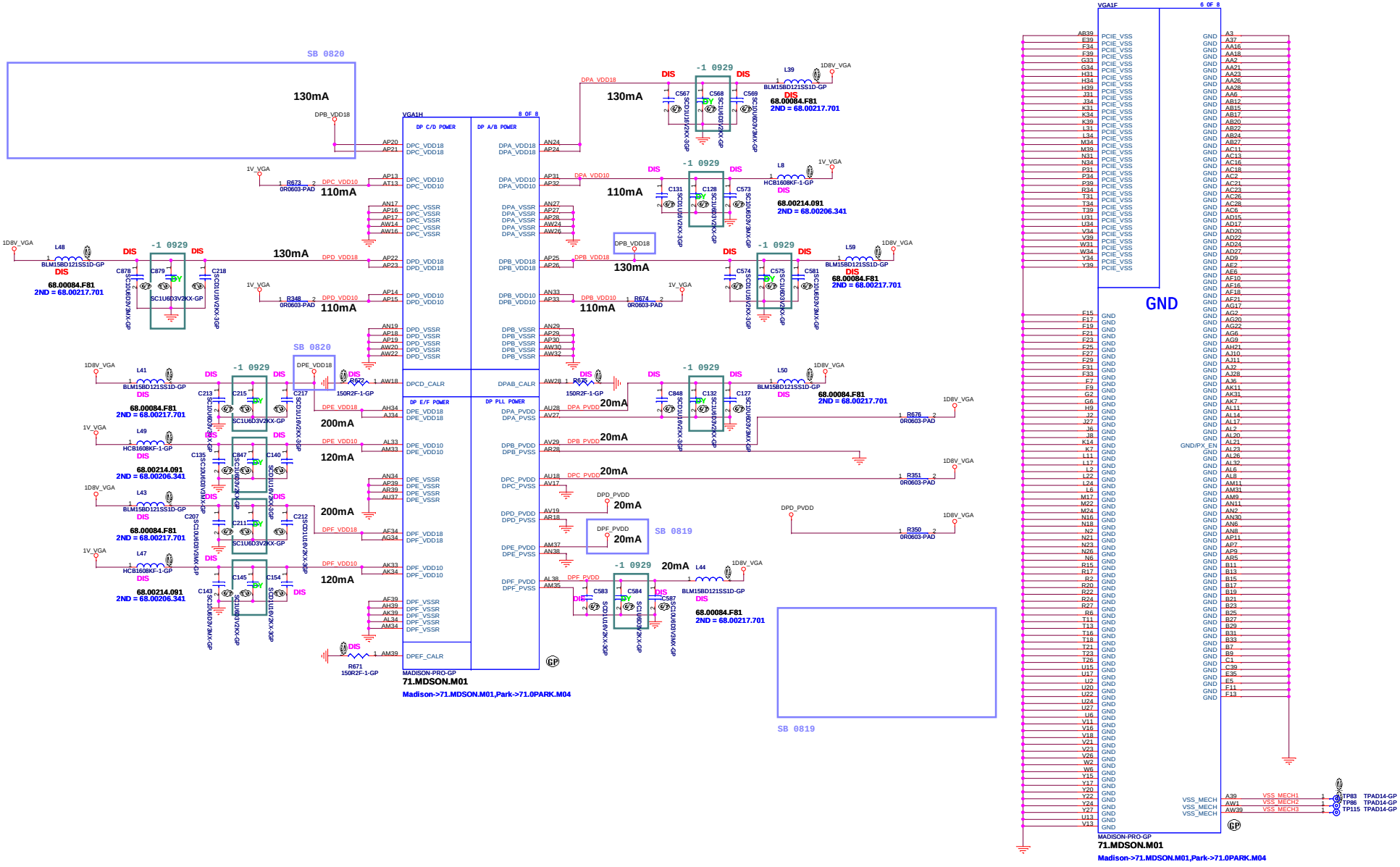

JV70-CP

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DP POWER_GND	
Size A2	Document Number JV70-CP	Rev -1
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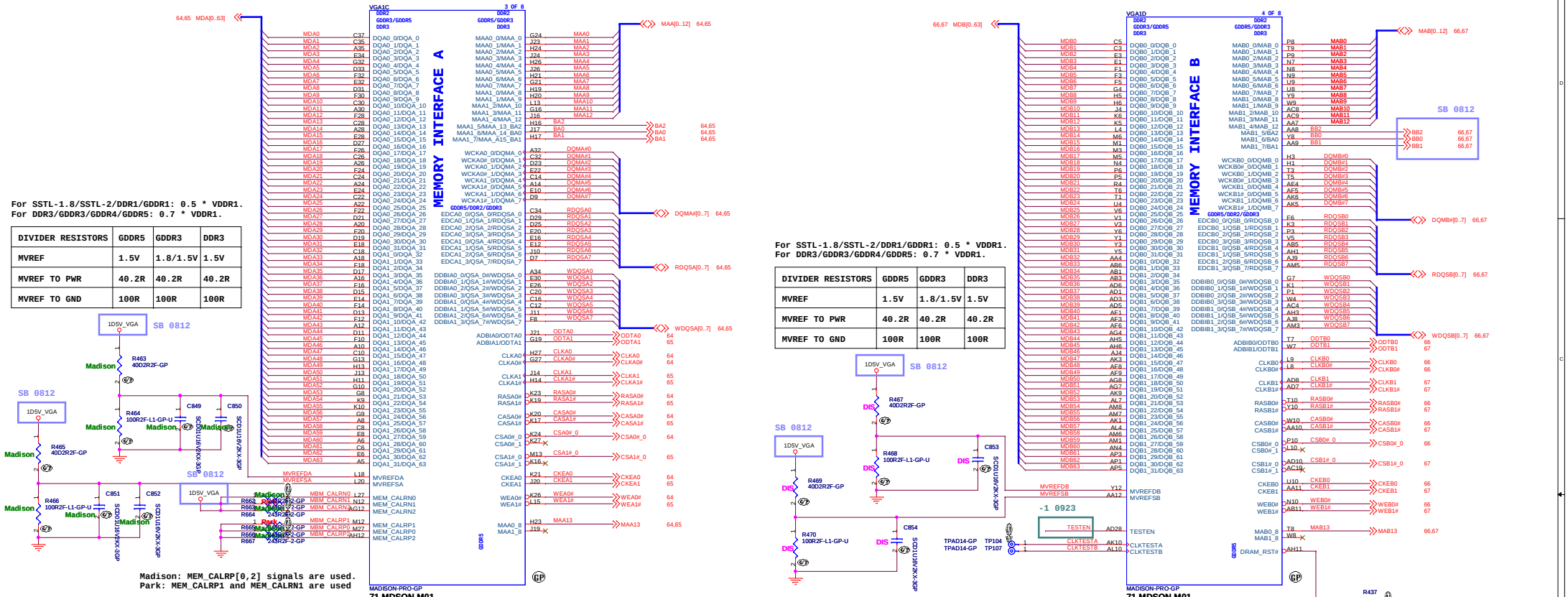


For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

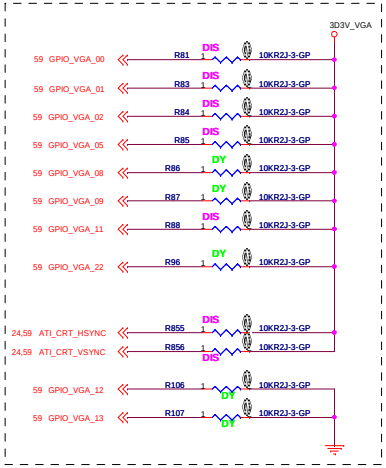
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

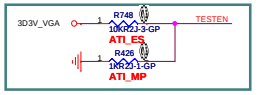
If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

HW STRAP PIN



Designator		For M97-M2	For Mannhatton
R_MEM_1	R471	10K	10K
R_MEM_2	R437	0R/Short	680R
R_MEM_3		DY	DY
C_MEM	C889	2.2nF	68pF

-1 0923



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Title: Madison Memory / Straps

Size	Document Number	Rev
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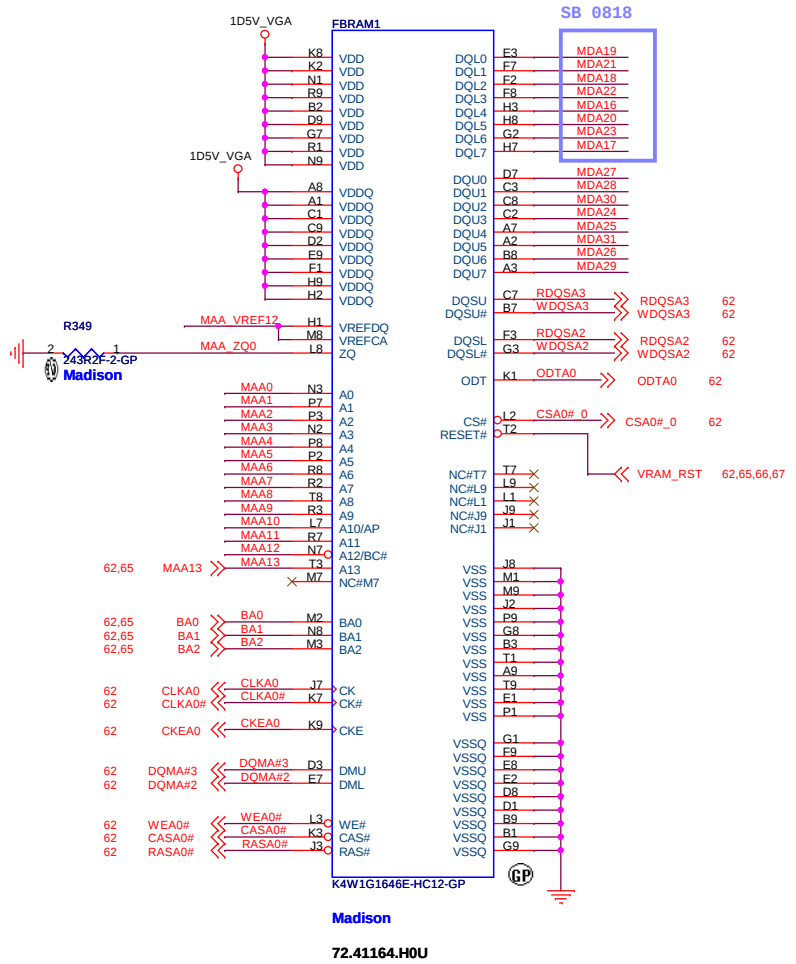
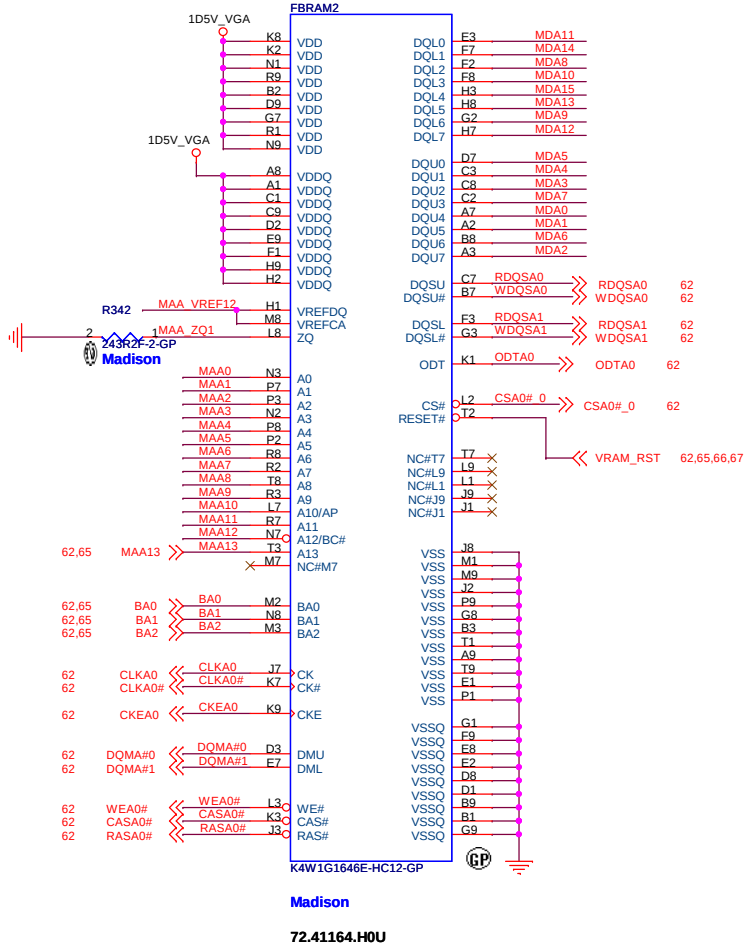
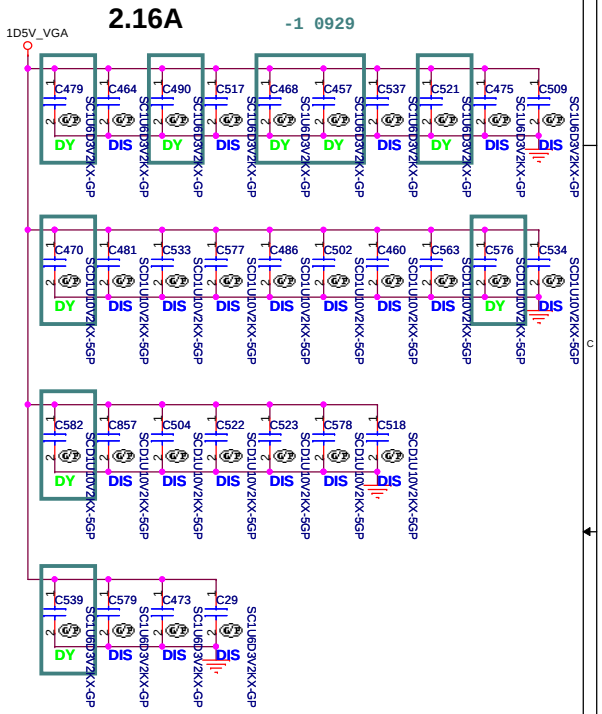
DDR3







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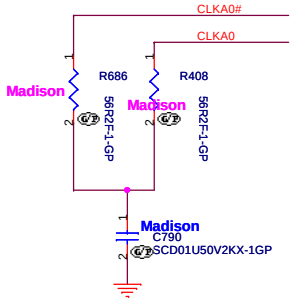
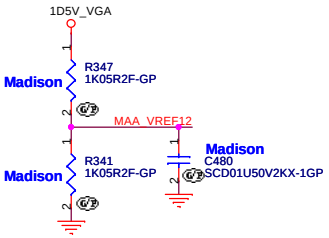
HYNIX: 72.51G63.C0U





62,65 DQMA#[0..7]

62,65 RDQSA[0..7]

62,65 WDQSA[0..7]

62,65 MAA[0..12] MAA[0..12]

62,65 MDA[0..63] MDA[0..63]

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***VRAM(1/4)***		
Size A3	Document Number **JV70-CP**	Rev **-1**	
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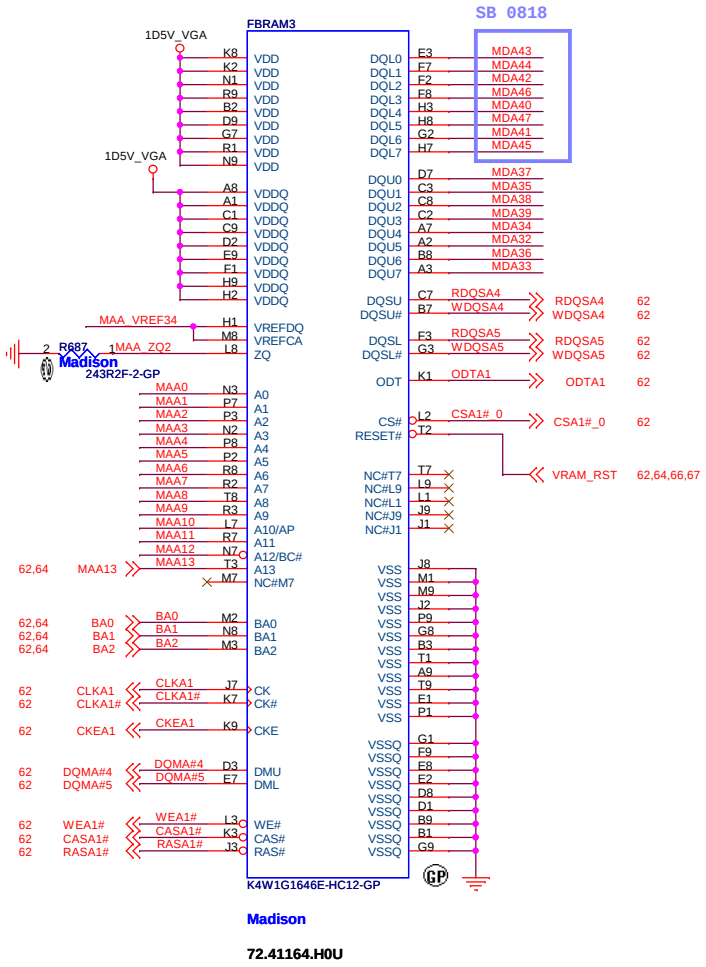
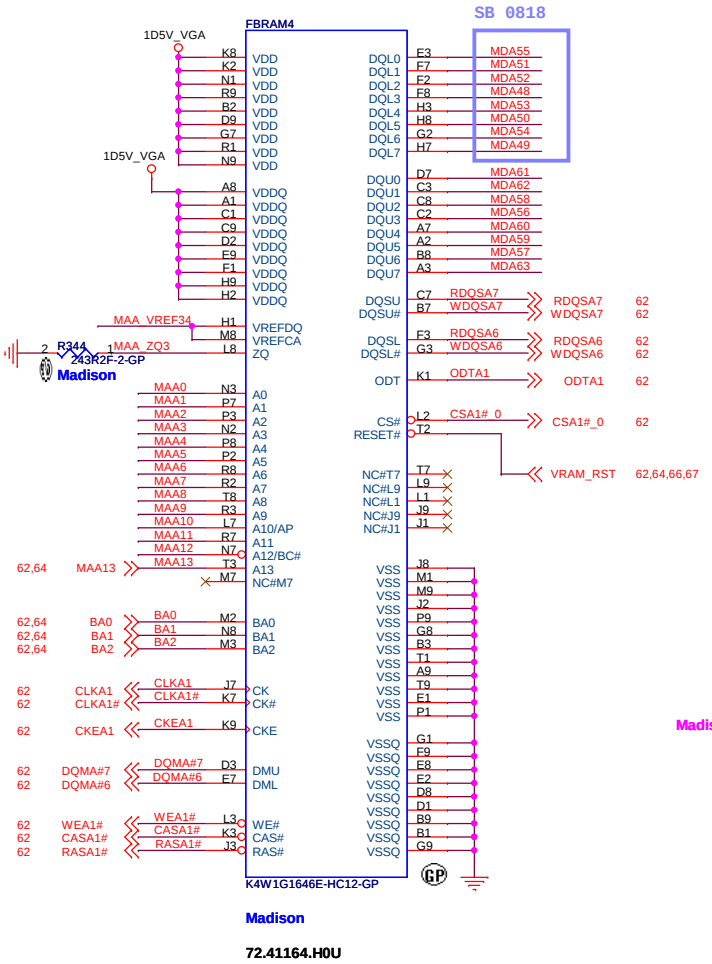
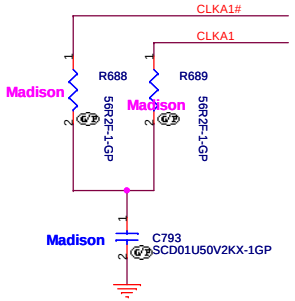
DDR3

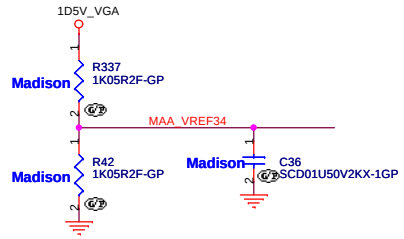




SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

62,64 DQMA#[0..7]
62,64 RDQSA[0..7]
62,64 WDQSA[0..7]
62,64 MAA[0..12] MAA[0..12]
62,64 MDA[0..63] MDA[0..63]





JV70-CP

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Title	*VRAM(2/4)*	
Size A3	Document Number JV70-CP	Rev -1
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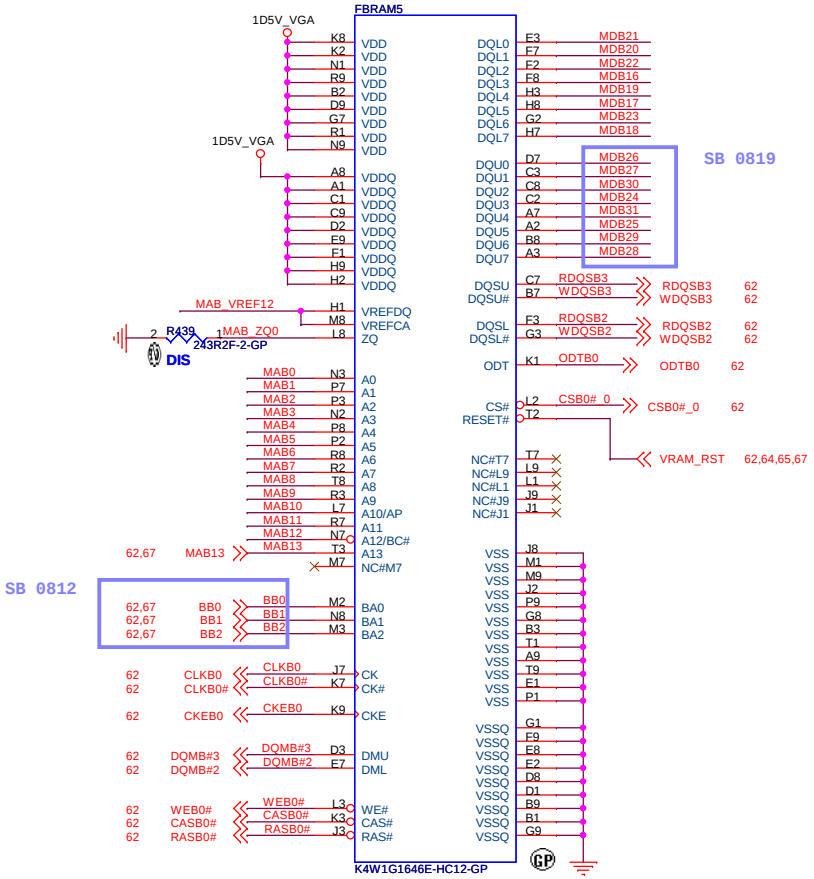
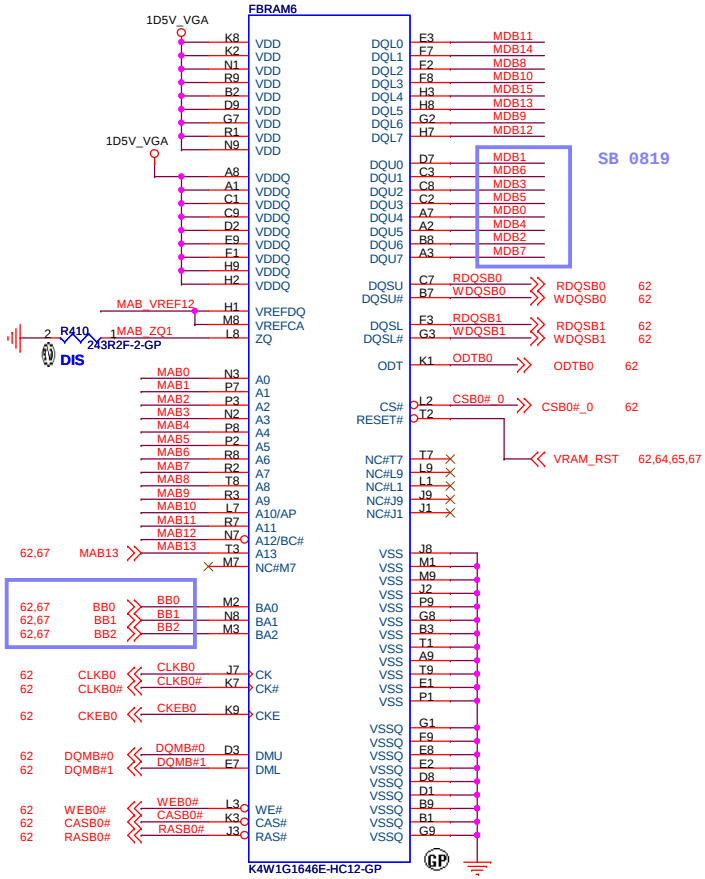
DDR3





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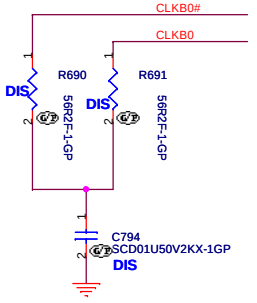

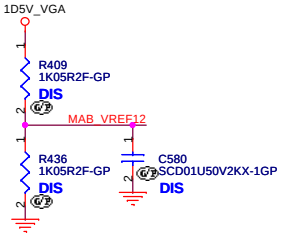

62,67 DQMB#[0..7]
62,67 RDQSB[0..7]
62,67 WDQSB[0..7]
62,67 MAB[0..12] MAB[0..12]
62,67 MDB[0..63] MDB[0..63]

JV70-CP

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Title	*VRAM(3/4)*	
Size A3	Document Number JV70-CP	Rev -1
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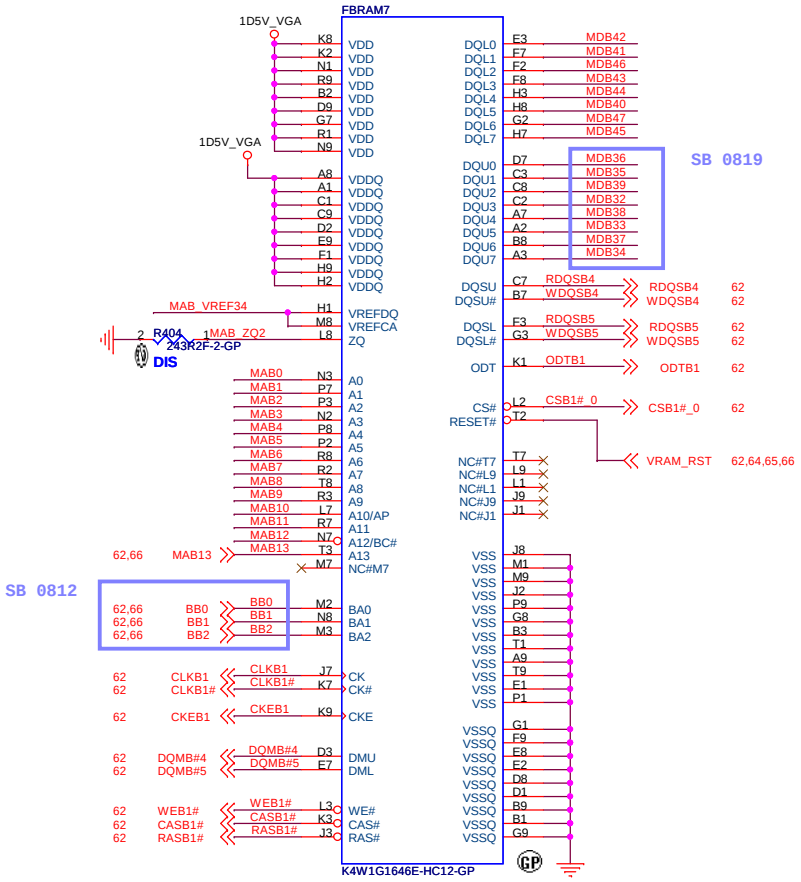
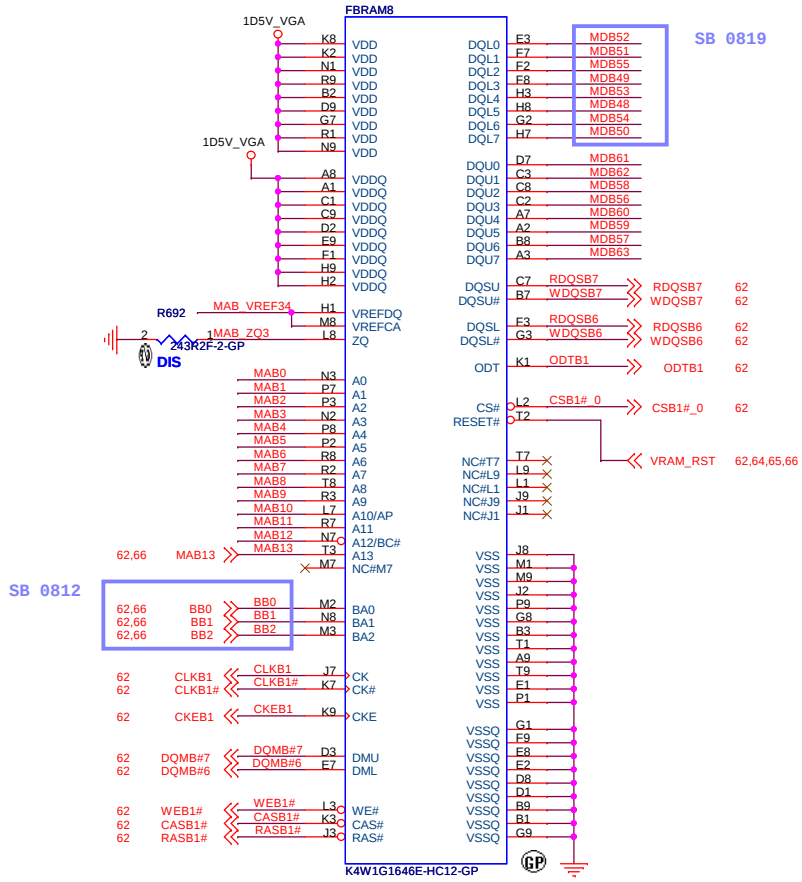
DDR3





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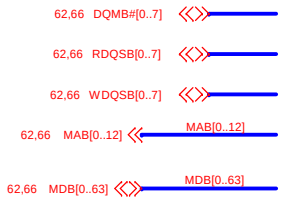

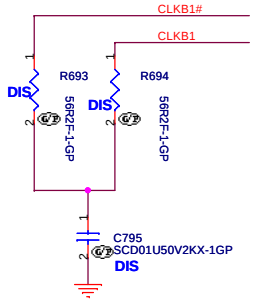

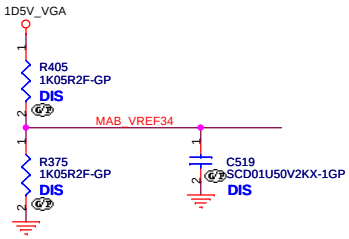

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Title: *VRAM(4/4)*		
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Modify History***

Size | Document Number: **JV70-CP** | Rev: **-1**

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