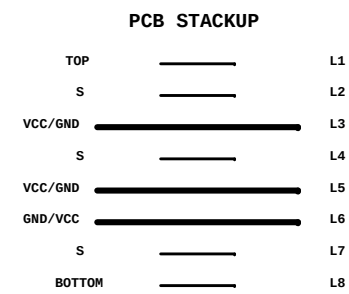


Project code: 91.4CQ01.001
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REVISION : 08274-SA



		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichai, Taipei Hsin 221, Taiwan, R.O.C.	
Title			
BLOCK DIAGRAM			
Size	Document Number		Rev
Custom		JM41 Discrete	SB
Date:	Monday, March 02, 2009	Sheet 1 of	48

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPI053	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPI020	Reserved	This signal should not be pulled high.
GNT1#/GPI051	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPI055	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/GPI058	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPI049	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPI033/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN controller functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPI0[20]	PULL-DOWN 20K
GPI0[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPI023	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPI06	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

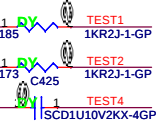
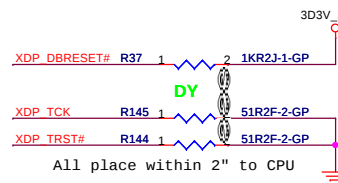
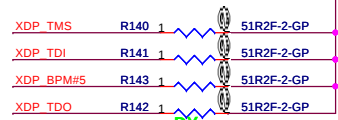
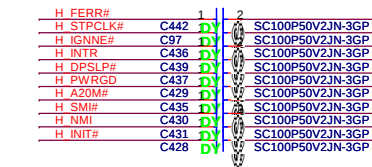
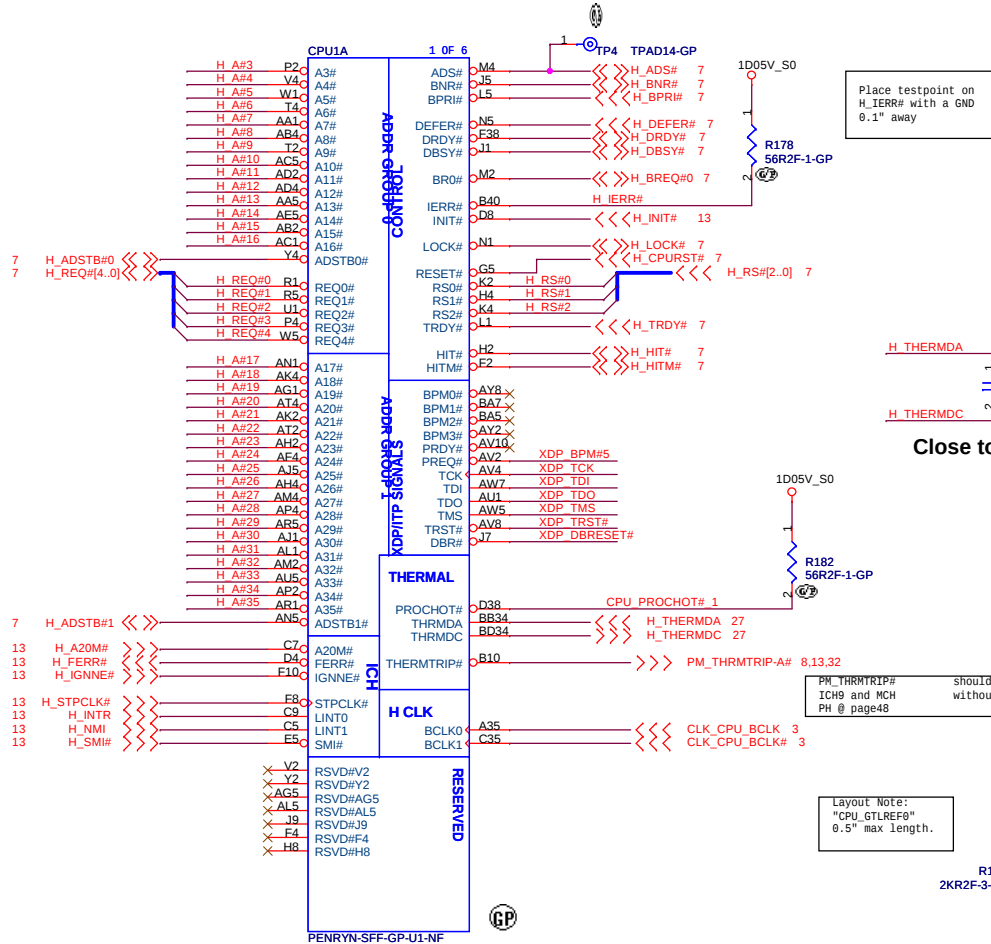
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display port and PCie are operating simulatanuously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

7 H_A#(35..3) <<< H_A#(35..3)



Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

Place these TP on button-side, easy to measure.

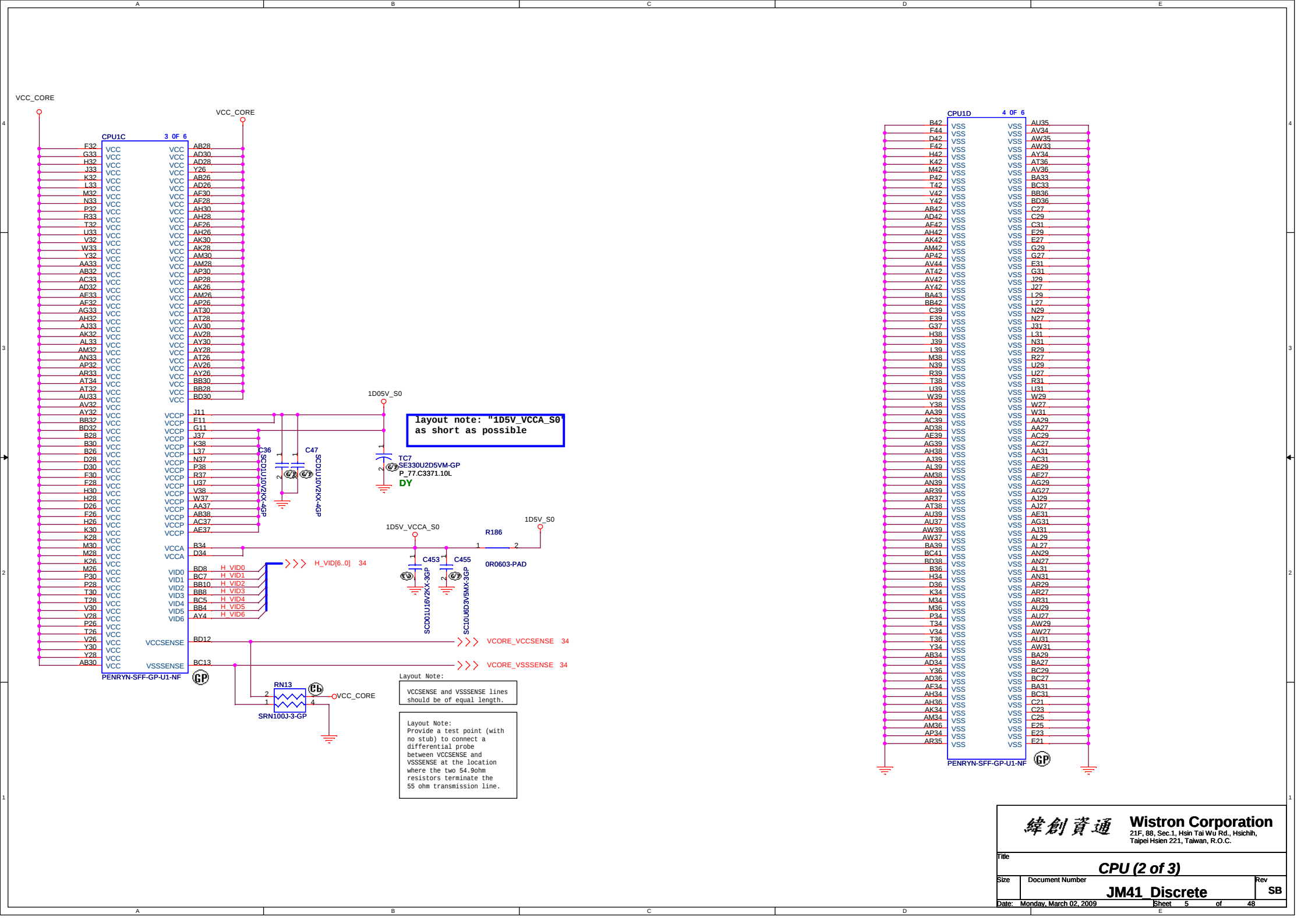
H_DINV#(3..0) <<>> H_DINV#(3..0) 7
H_DSTBN#(3..0) <<>> H_DSTBN#(3..0) 7
H_DSTBP#(3..0) <<>> H_DSTBP#(3..0) 7
H_DM#(63..0) <<>> H_DM#(63..0) 7

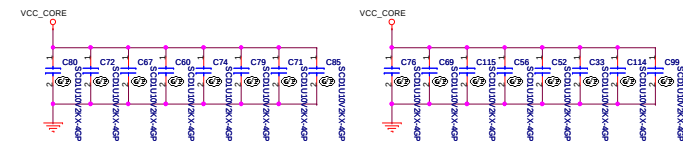
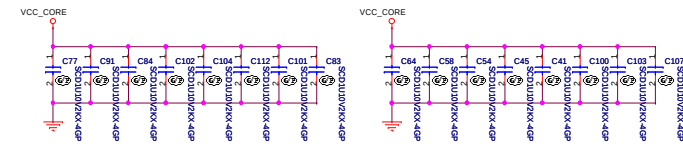
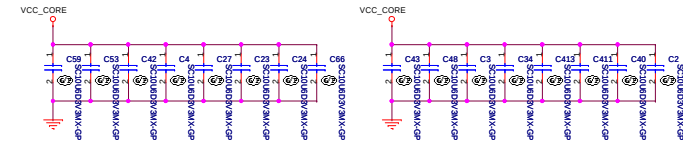
H_D#0 F40, H_D#1 G43, H_D#2 E43, H_D#3 J43, H_D#4 H40, H_D#5 H44, H_D#6 G39, H_D#7 E41, H_D#8 L41, H_D#9 K44, H_D#10 M41, H_D#11 T40, H_D#12 M40, H_D#13 G41, H_D#14 M44, H_D#15 L43, H_D#16 P44, H_D#17 V40, H_D#18 V44, H_D#19 AB44, H_D#20 R41, H_D#21 V44, H_D#22 N43, H_D#23 U41, H_D#24 A41, H_D#25 AB40, H_D#26 AD40, H_D#27 AC41, H_D#28 AA43, H_D#29 Y40, H_D#30 Y44, H_D#31 T44, H_D#32 D32, H_D#33 D33, H_D#34 D34, H_D#35 D35, H_D#36 D36, H_D#37 D37, H_D#38 D38, H_D#39 D39, H_D#40 D40, H_D#41 D41, H_D#42 D42, H_D#43 D43, H_D#44 D44, H_D#45 D45, H_D#46 D46, H_D#47 D47, H_D#48 D48, H_D#49 D49, H_D#50 D50, H_D#51 D51, H_D#52 D52, H_D#53 D53, H_D#54 D54, H_D#55 D55, H_D#56 D56, H_D#57 D57, H_D#58 D58, H_D#59 D59, H_D#60 D60, H_D#61 D61, H_D#62 D62, H_D#63 D63, H_D#64 D64, H_D#65 D65, H_D#66 D66, H_D#67 D67, H_D#68 D68, H_D#69 D69, H_D#70 D70, H_D#71 D71, H_D#72 D72, H_D#73 D73, H_D#74 D74, H_D#75 D75, H_D#76 D76, H_D#77 D77, H_D#78 D78, H_D#79 D79, H_D#80 D80, H_D#81 D81, H_D#82 D82, H_D#83 D83, H_D#84 D84, H_D#85 D85, H_D#86 D86, H_D#87 D87, H_D#88 D88, H_D#89 D89, H_D#90 D90, H_D#91 D91, H_D#92 D92, H_D#93 D93, H_D#94 D94, H_D#95 D95, H_D#96 D96, H_D#97 D97, H_D#98 D98, H_D#99 D99, H_D#100 D100.

H_DSTBN#0, H_DSTBP#0, H_DINV#0, H_DSTBN#1, H_DSTBP#1, H_DINV#1, H_DSTBN#2, H_DSTBP#2, H_DINV#2, H_DSTBN#3, H_DSTBP#3, H_DINV#3, H_DSTBN#4, H_DSTBP#4, H_DINV#4, H_DSTBN#5, H_DSTBP#5, H_DINV#5, H_DSTBN#6, H_DSTBP#6, H_DINV#6, H_DSTBN#7, H_DSTBP#7, H_DINV#7, H_DSTBN#8, H_DSTBP#8, H_DINV#8, H_DSTBN#9, H_DSTBP#9, H_DINV#9, H_DSTBN#10, H_DSTBP#10, H_DINV#10, H_DSTBN#11, H_DSTBP#11, H_DINV#11, H_DSTBN#12, H_DSTBP#12, H_DINV#12, H_DSTBN#13, H_DSTBP#13, H_DINV#13, H_DSTBN#14, H_DSTBP#14, H_DINV#14, H_DSTBN#15, H_DSTBP#15, H_DINV#15, H_DSTBN#16, H_DSTBP#16, H_DINV#16, H_DSTBN#17, H_DSTBP#17, H_DINV#17, H_DSTBN#18, H_DSTBP#18, H_DINV#18, H_DSTBN#19, H_DSTBP#19, H_DINV#19, H_DSTBN#20, H_DSTBP#20, H_DINV#20, H_DSTBN#21, H_DSTBP#21, H_DINV#21, H_DSTBN#22, H_DSTBP#22, H_DINV#22, H_DSTBN#23, H_DSTBP#23, H_DINV#23, H_DSTBN#24, H_DSTBP#24, H_DINV#24, H_DSTBN#25, H_DSTBP#25, H_DINV#25, H_DSTBN#26, H_DSTBP#26, H_DINV#26, H_DSTBN#27, H_DSTBP#27, H_DINV#27, H_DSTBN#28, H_DSTBP#28, H_DINV#28, H_DSTBN#29, H_DSTBP#29, H_DINV#29, H_DSTBN#30, H_DSTBP#30, H_DINV#30, H_DSTBN#31, H_DSTBP#31, H_DINV#31, H_DSTBN#32, H_DSTBP#32, H_DINV#32, H_DSTBN#33, H_DSTBP#33, H_DINV#33, H_DSTBN#34, H_DSTBP#34, H_DINV#34, H_DSTBN#35, H_DSTBP#35, H_DINV#35, H_DSTBN#36, H_DSTBP#36, H_DINV#36, H_DSTBN#37, H_DSTBP#37, H_DINV#37, H_DSTBN#38, H_DSTBP#38, H_DINV#38, H_DSTBN#39, H_DSTBP#39, H_DINV#39, H_DSTBN#40, H_DSTBP#40, H_DINV#40, H_DSTBN#41, H_DSTBP#41, H_DINV#41, H_DSTBN#42, H_DSTBP#42, H_DINV#42, H_DSTBN#43, H_DSTBP#43, H_DINV#43, H_DSTBN#44, H_DSTBP#44, H_DINV#44, H_DSTBN#45, H_DSTBP#45, H_DINV#45, H_DSTBN#46, H_DSTBP#46, H_DINV#46, H_DSTBN#47, H_DSTBP#47, H_DINV#47, H_DSTBN#48, H_DSTBP#48, H_DINV#48, H_DSTBN#49, H_DSTBP#49, H_DINV#49, H_DSTBN#50, H_DSTBP#50, H_DINV#50, H_DSTBN#51, H_DSTBP#51, H_DINV#51, H_DSTBN#52, H_DSTBP#52, H_DINV#52, H_DSTBN#53, H_DSTBP#53, H_DINV#53, H_DSTBN#54, H_DSTBP#54, H_DINV#54, H_DSTBN#55, H_DSTBP#55, H_DINV#55, H_DSTBN#56, H_DSTBP#56, H_DINV#56, H_DSTBN#57, H_DSTBP#57, H_DINV#57, H_DSTBN#58, H_DSTBP#58, H_DINV#58, H_DSTBN#59, H_DSTBP#59, H_DINV#59, H_DSTBN#60, H_DSTBP#60, H_DINV#60, H_DSTBN#61, H_DSTBP#61, H_DINV#61, H_DSTBN#62, H_DSTBP#62, H_DINV#62, H_DSTBN#63, H_DSTBP#63, H_DINV#63, H_DSTBN#64, H_DSTBP#64, H_DINV#64, H_DSTBN#65, H_DSTBP#65, H_DINV#65, H_DSTBN#66, H_DSTBP#66, H_DINV#66, H_DSTBN#67, H_DSTBP#67, H_DINV#67, H_DSTBN#68, H_DSTBP#68, H_DINV#68, H_DSTBN#69, H_DSTBP#69, H_DINV#69, H_DSTBN#70, H_DSTBP#70, H_DINV#70, H_DSTBN#71, H_DSTBP#71, H_DINV#71, H_DSTBN#72, H_DSTBP#72, H_DINV#72, H_DSTBN#73, H_DSTBP#73, H_DINV#73, H_DSTBN#74, H_DSTBP#74, H_DINV#74, H_DSTBN#75, H_DSTBP#75, H_DINV#75, H_DSTBN#76, H_DSTBP#76, H_DINV#76, H_DSTBN#77, H_DSTBP#77, H_DINV#77, H_DSTBN#78, H_DSTBP#78, H_DINV#78, H_DSTBN#79, H_DSTBP#79, H_DINV#79, H_DSTBN#80, H_DSTBP#80, H_DINV#80, H_DSTBN#81, H_DSTBP#81, H_DINV#81, H_DSTBN#82, H_DSTBP#82, H_DINV#82, H_DSTBN#83, H_DSTBP#83, H_DINV#83, H_DSTBN#84, H_DSTBP#84, H_DINV#84, H_DSTBN#85, H_DSTBP#85, H_DINV#85, H_DSTBN#86, H_DSTBP#86, H_DINV#86, H_DSTBN#87, H_DSTBP#87, H_DINV#87, H_DSTBN#88, H_DSTBP#88, H_DINV#88, H_DSTBN#89, H_DSTBP#89, H_DINV#89, H_DSTBN#90, H_DSTBP#90, H_DINV#90, H_DSTBN#91, H_DSTBP#91, H_DINV#91, H_DSTBN#92, H_DSTBP#92, H_DINV#92, H_DSTBN#93, H_DSTBP#93, H_DINV#93, H_DSTBN#94, H_DSTBP#94, H_DINV#94, H_DSTBN#95, H_DSTBP#95, H_DINV#95, H_DSTBN#96, H_DSTBP#96, H_DINV#96, H_DSTBN#97, H_DSTBP#97, H_DINV#97, H_DSTBN#98, H_DSTBP#98, H_DINV#98, H_DSTBN#99, H_DSTBP#99, H_DINV#99, H_DSTBN#100, H_DSTBP#100, H_DINV#100.

Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5"

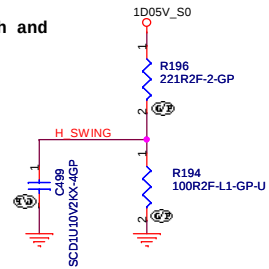
緯創資通 Wistron Corporation
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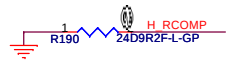


H_SWING routing Trace width and Spacing use 10 / 20 mil

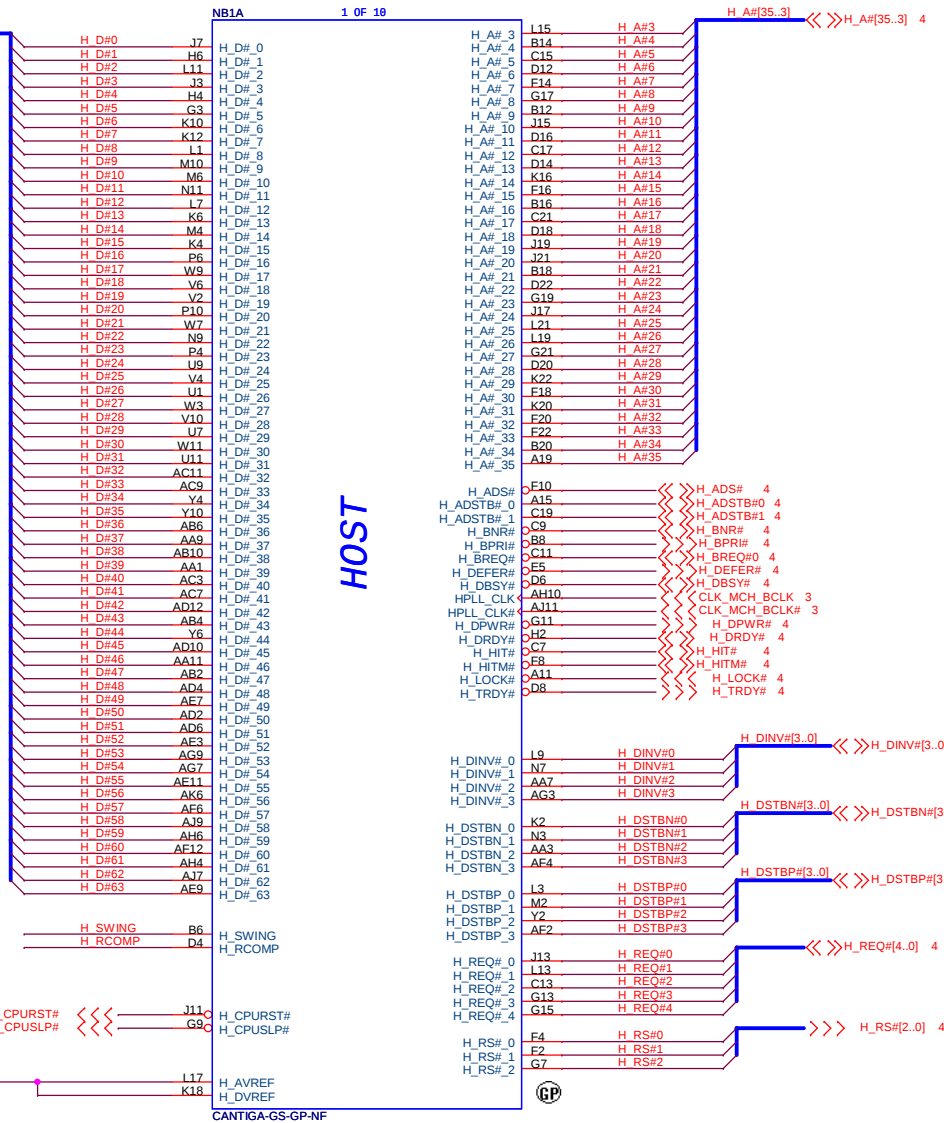
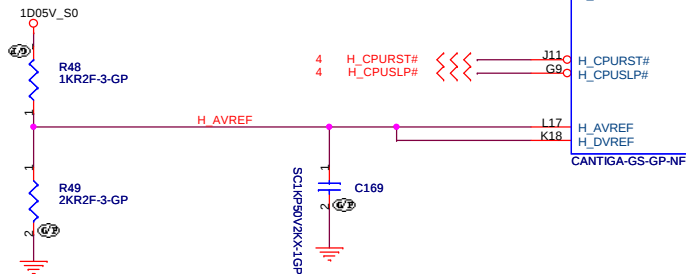
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



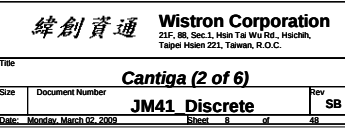
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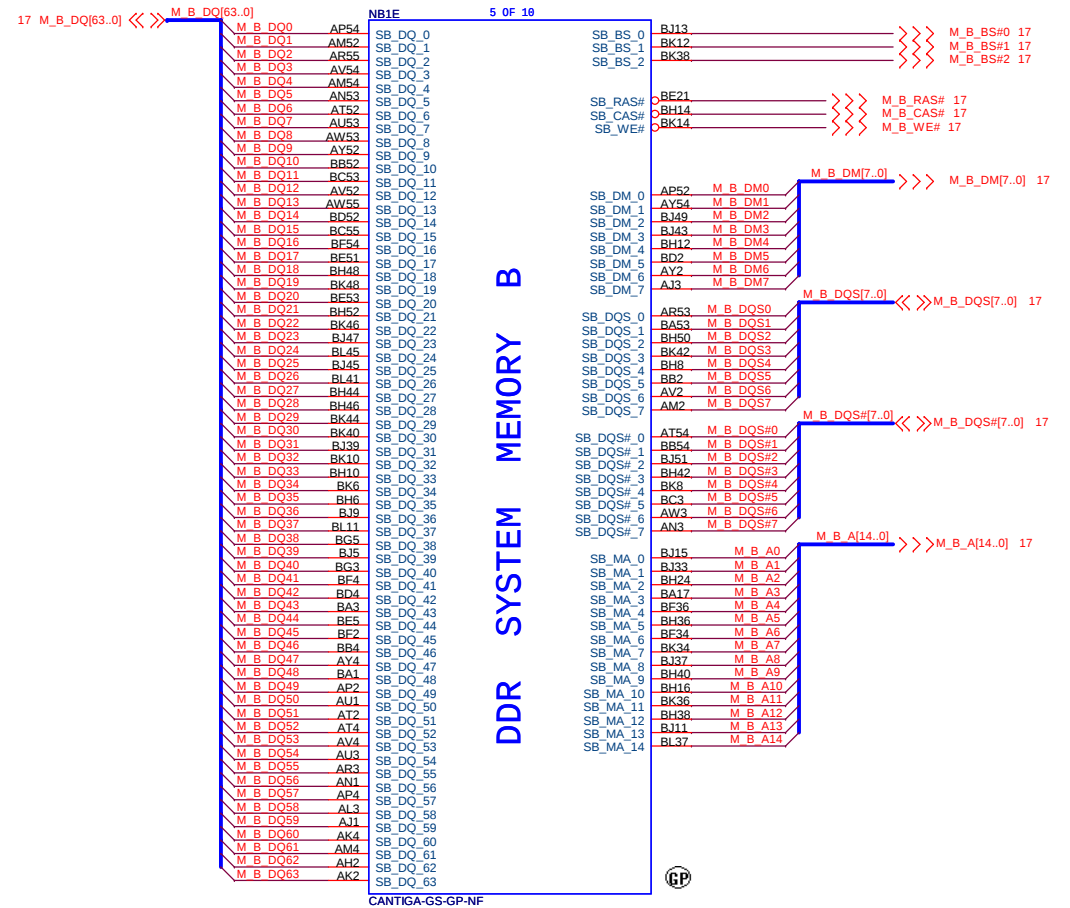
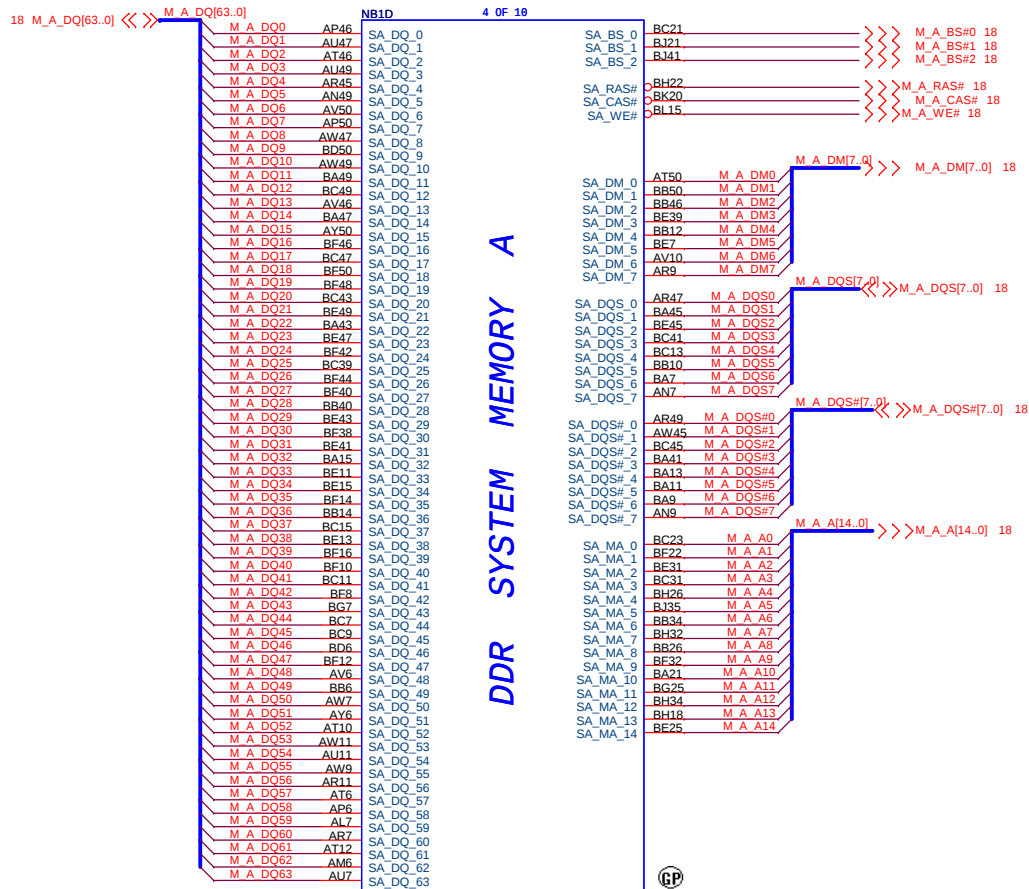


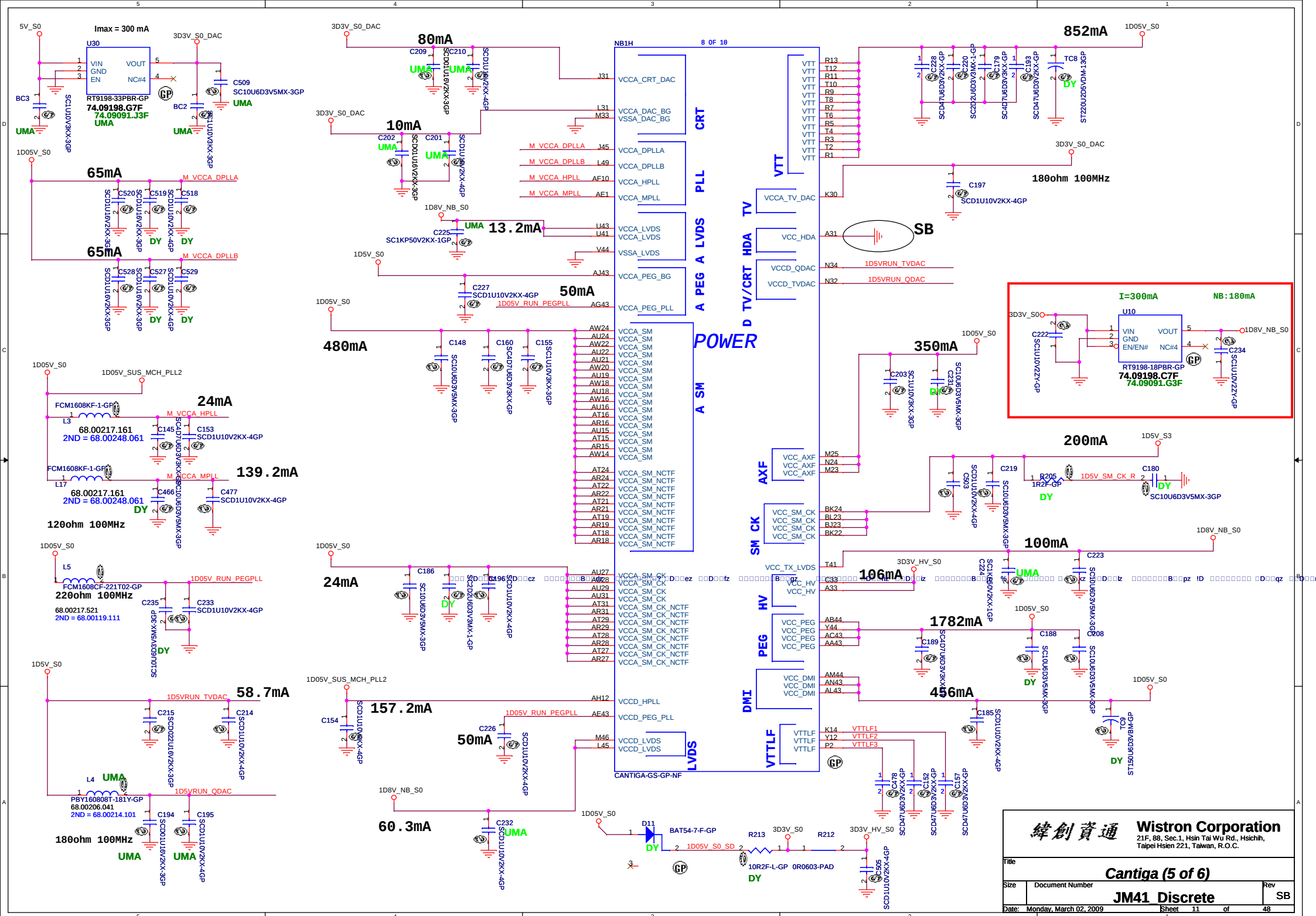
Place them near to the chip (< 0.5")

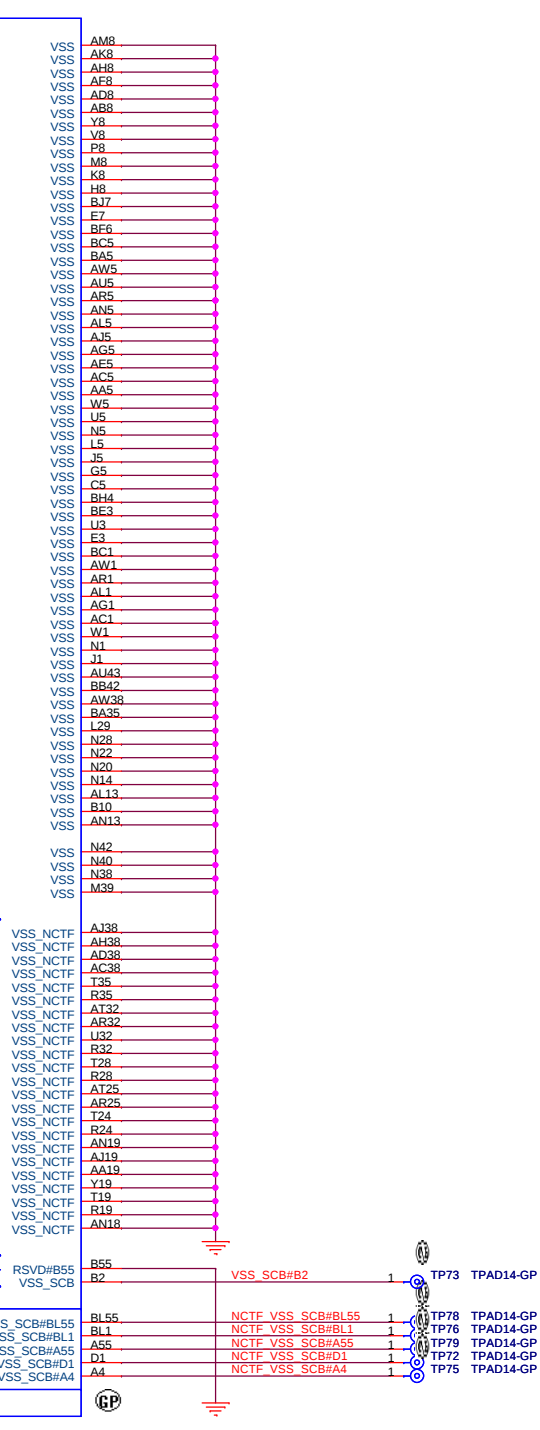
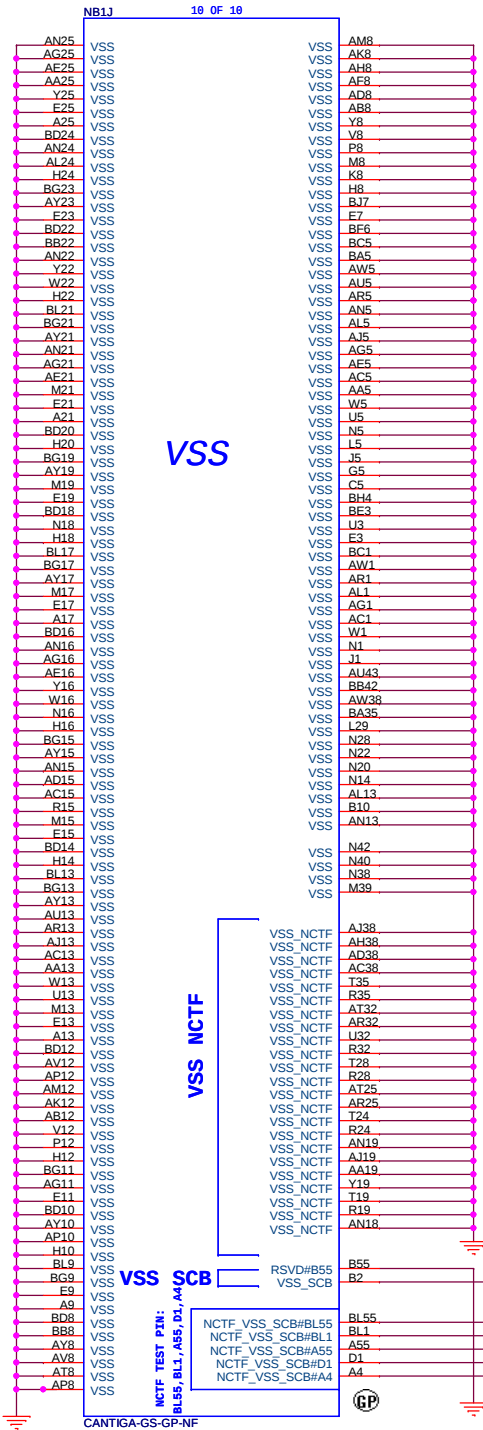
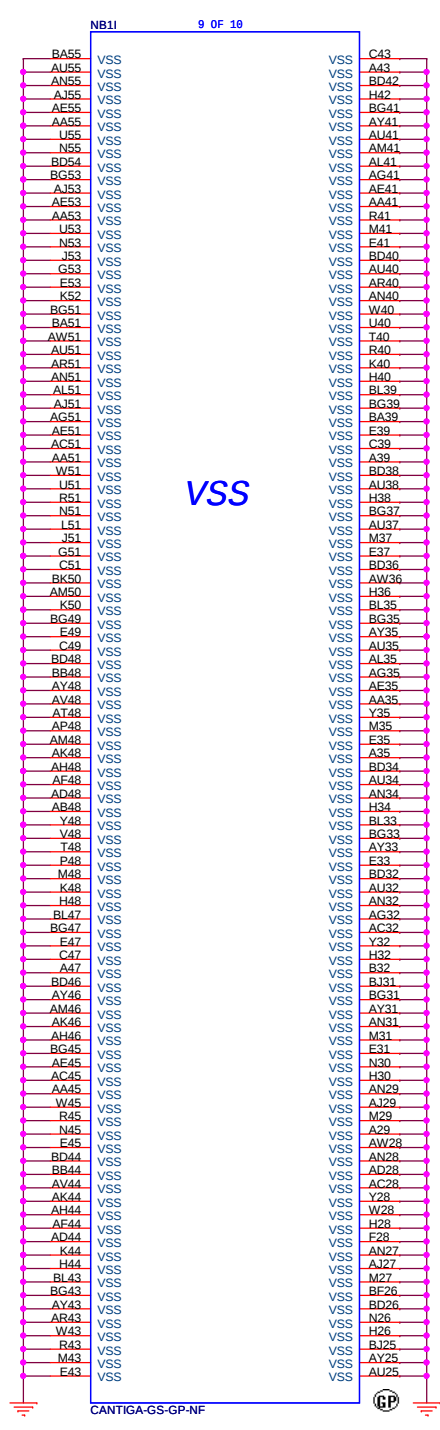


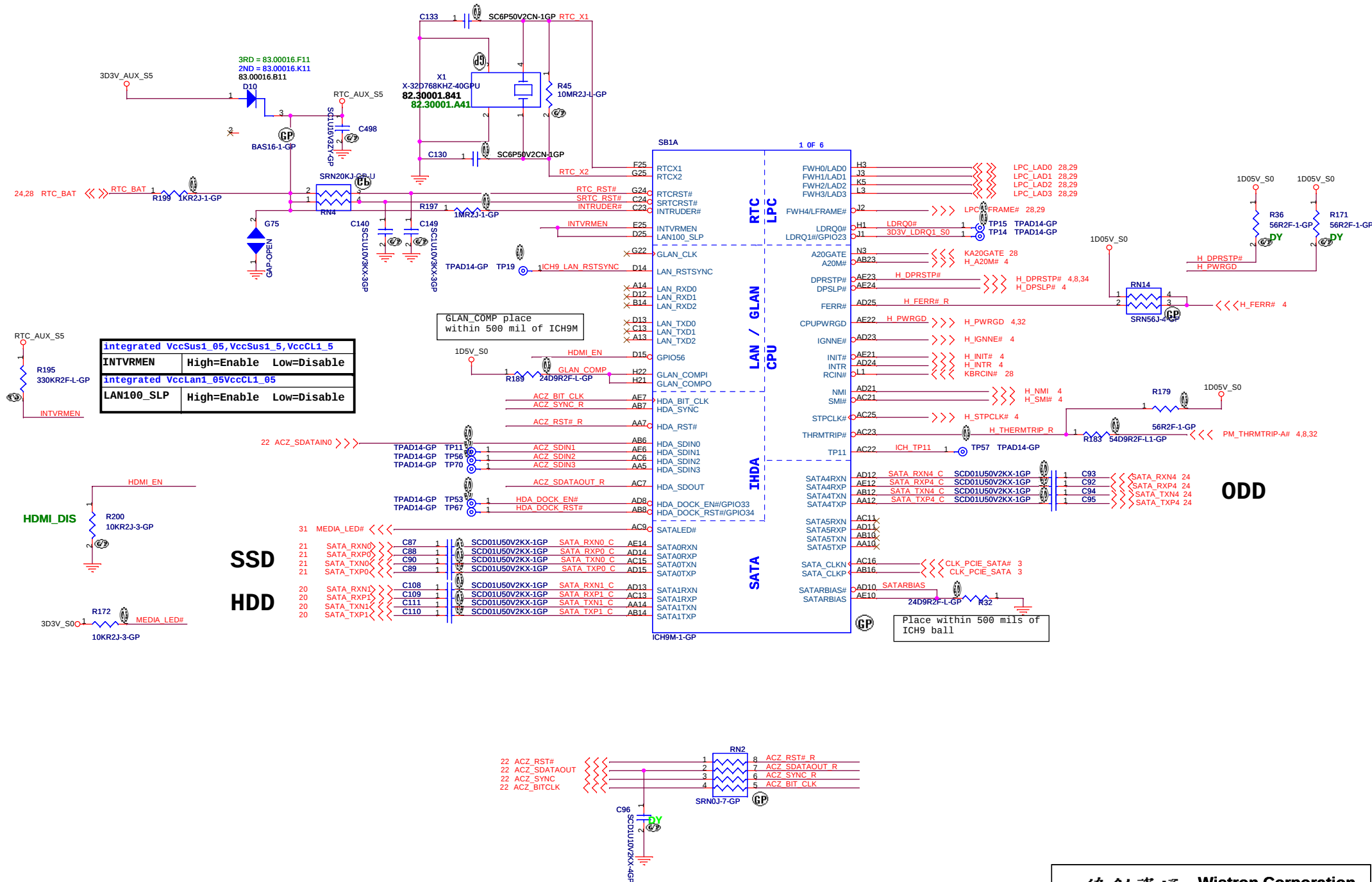
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Taipei Hsien 221, Taiwan, R.O.C.



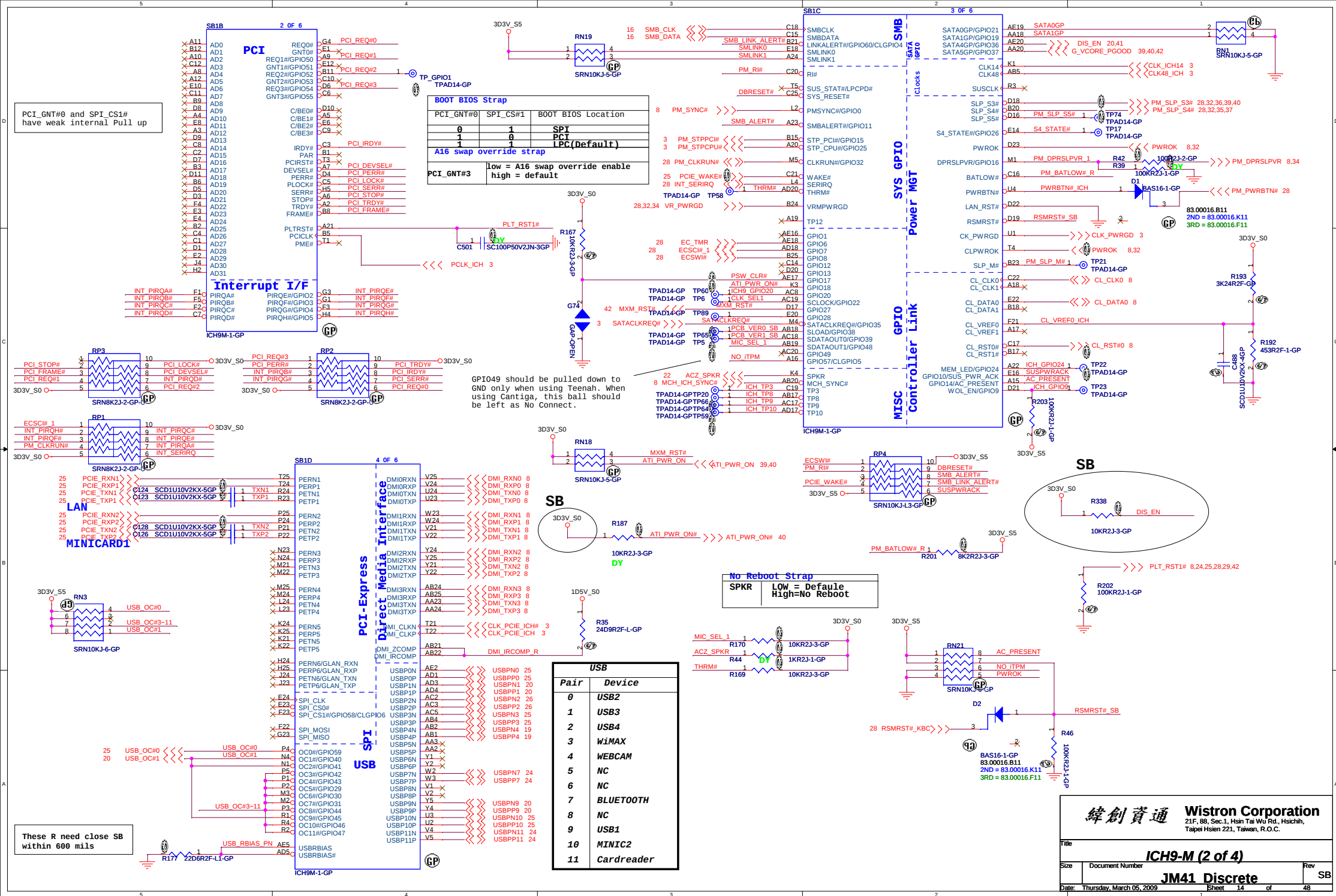








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Taipei Hsien 221, Taiwan, R.O.C.



657mA

6uA in G3

1.13A

23mA

50mA

1mA

VCC3_3=278mA

32mA

32mA

177mA

18mA

47mA

SATA+USB=1.56A

USBPLL=10mA

23mA

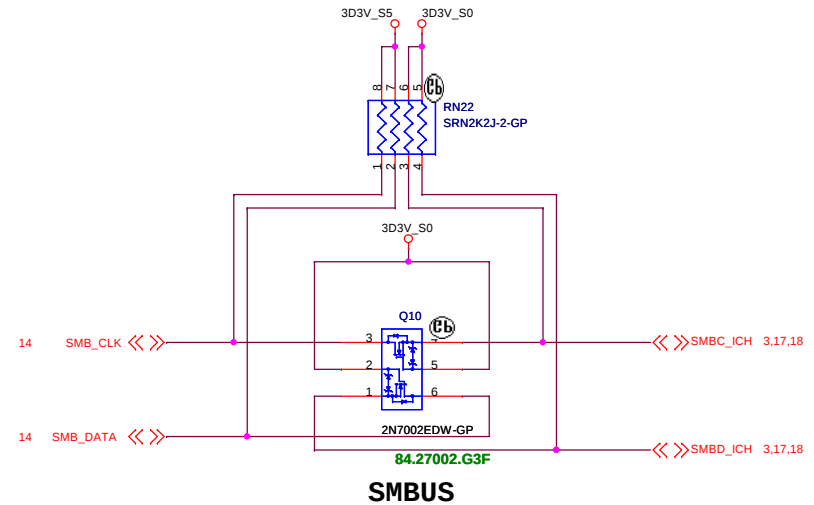
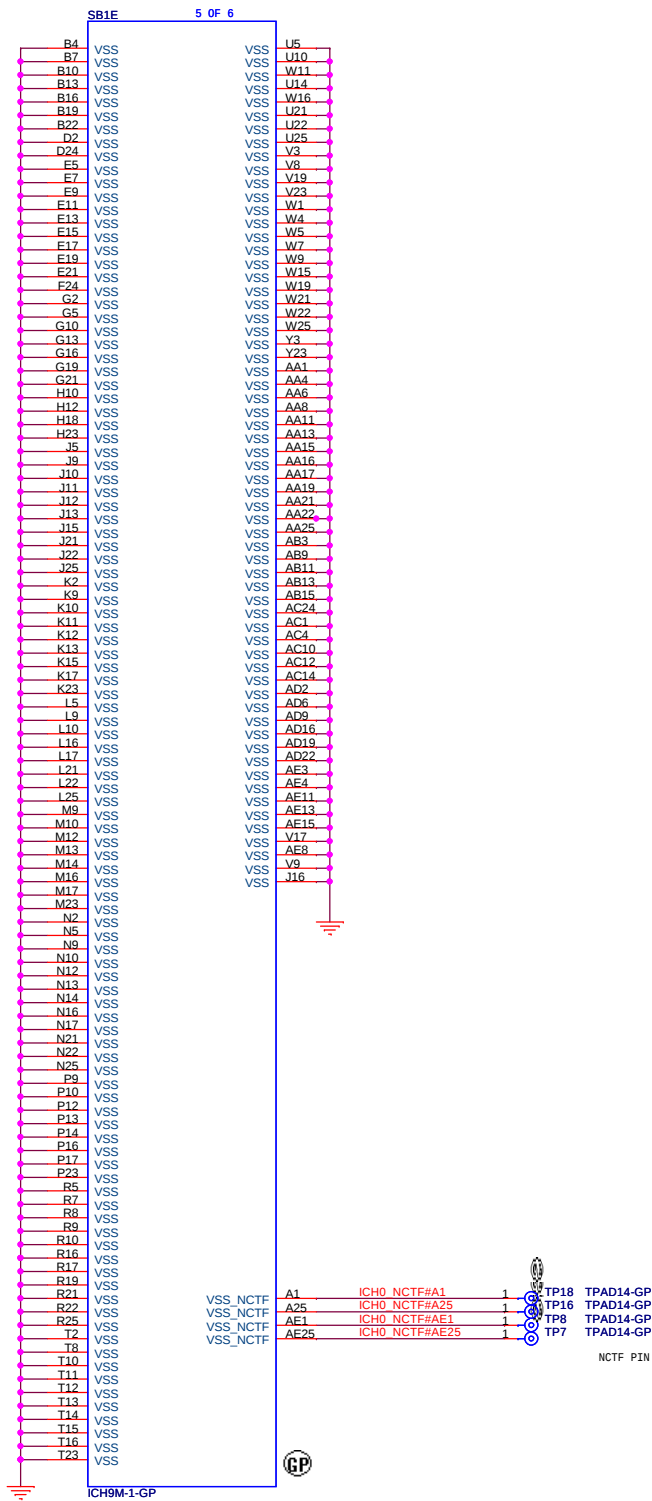
80mA

1mA

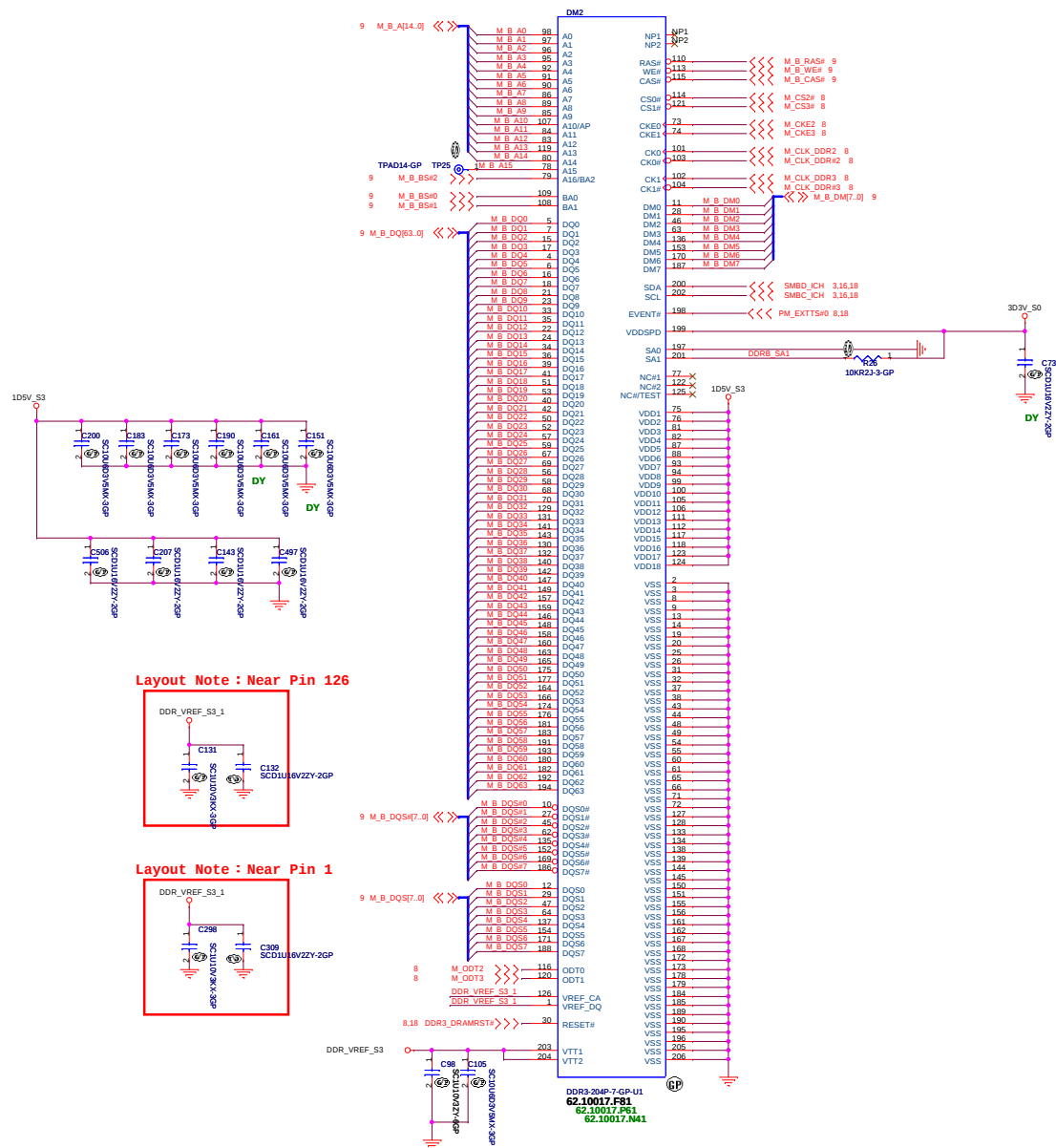
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

2mA

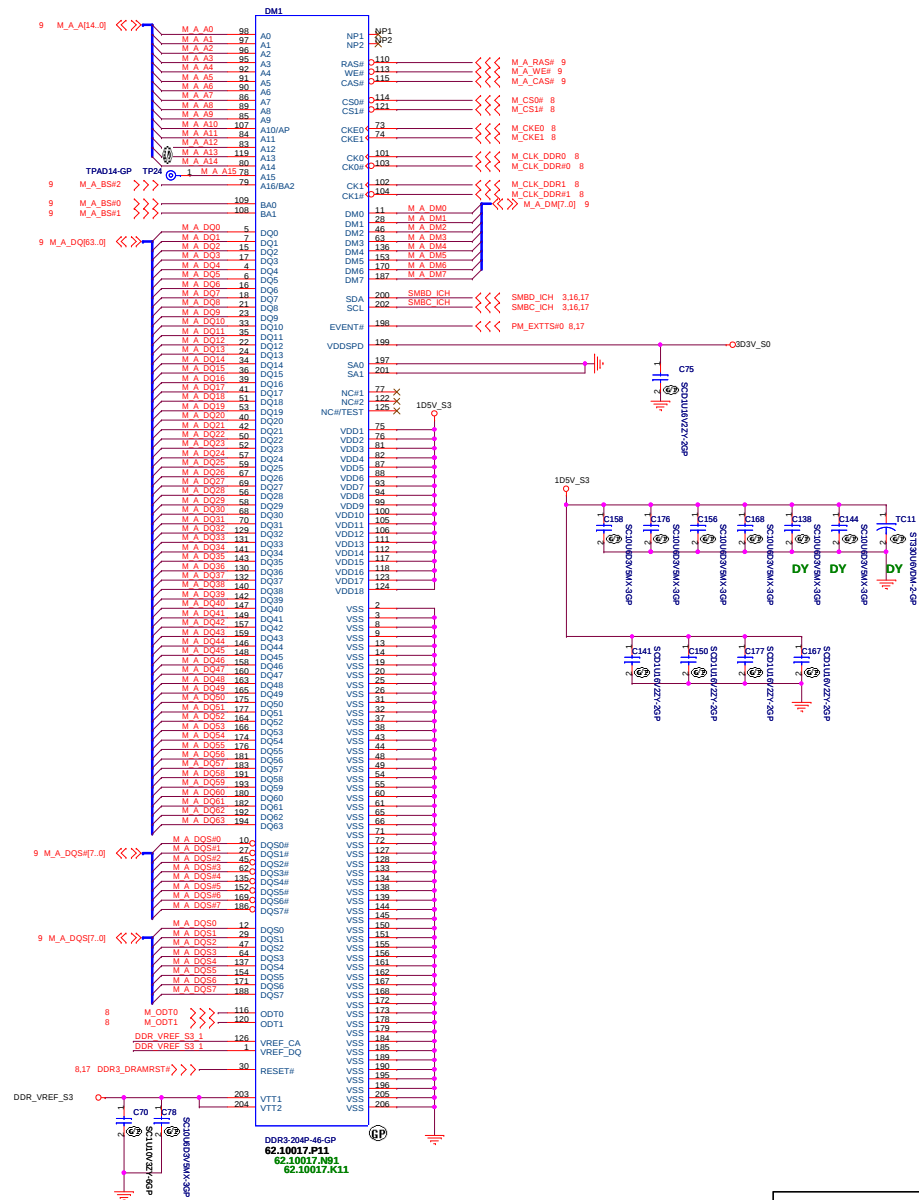
2mA



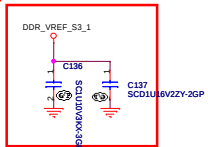
DDR3 SOCKET_1



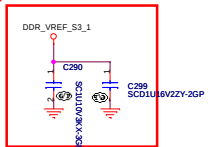
DDR3 SOCKET_2



Layout Note : Near Pin 126

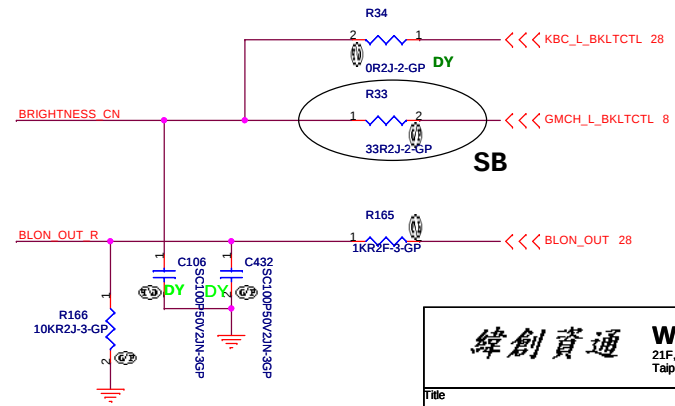
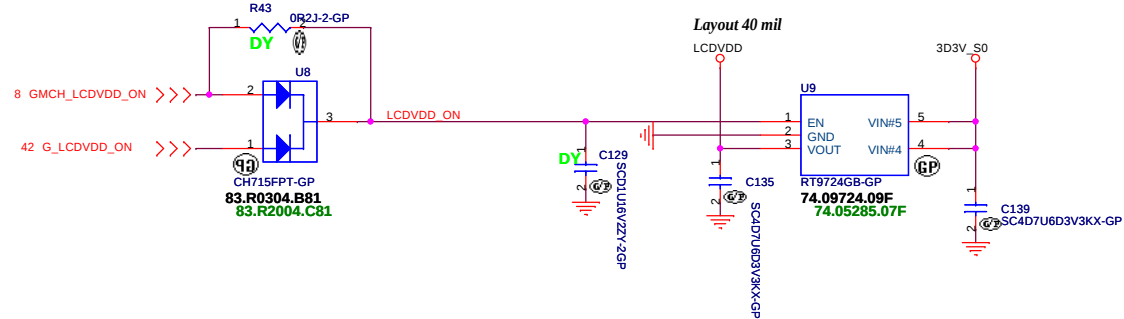
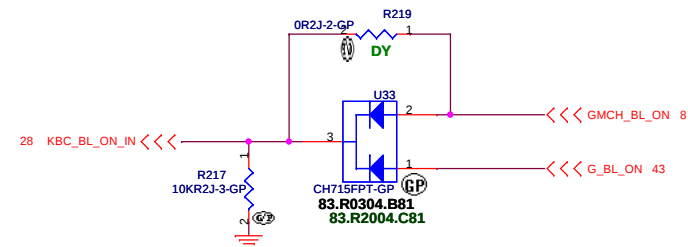
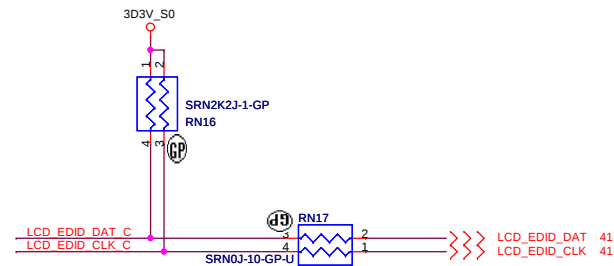
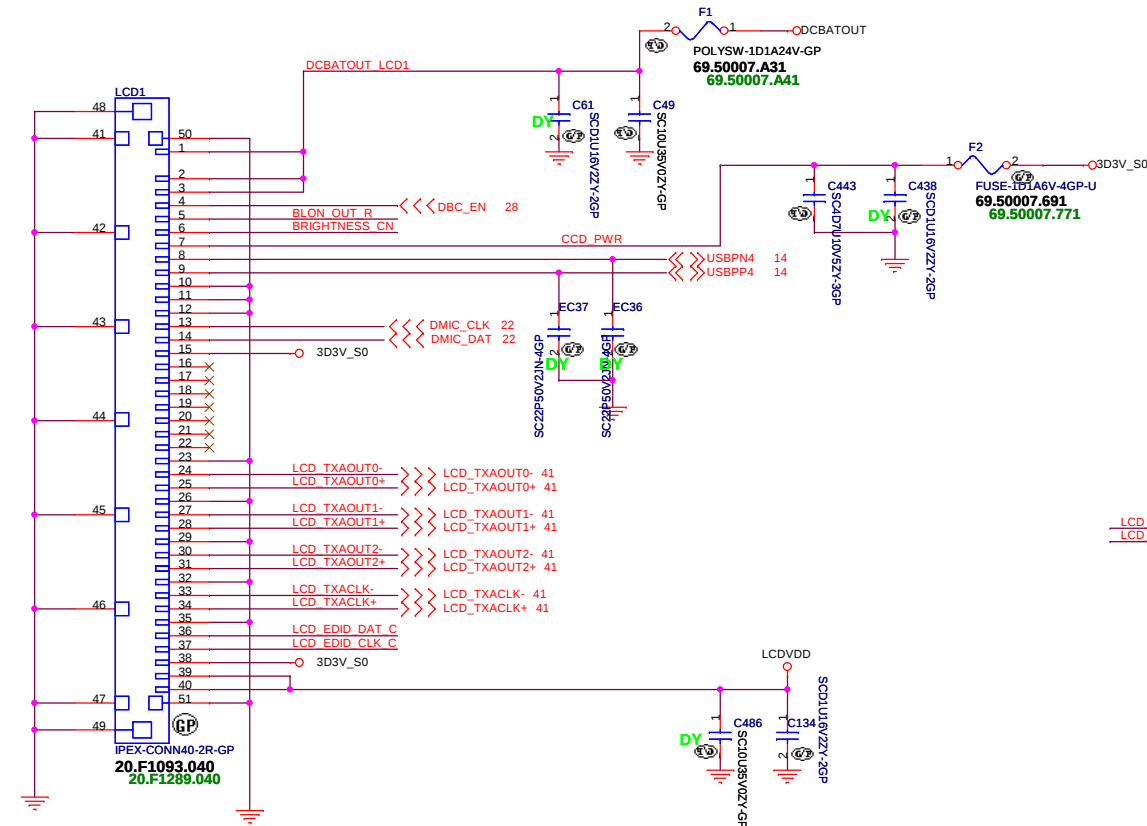


Layout Note : Near Pin 1

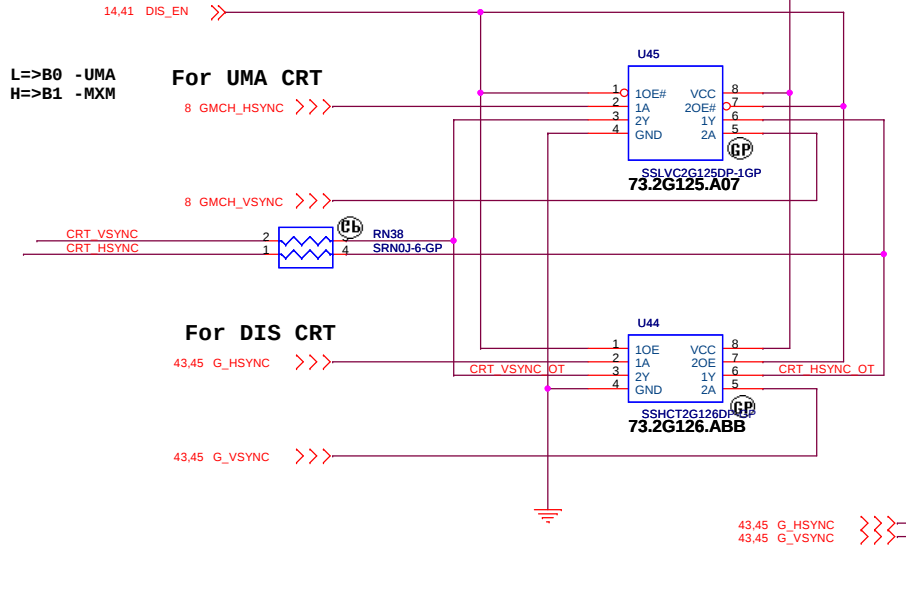


LCD/CCD CONN

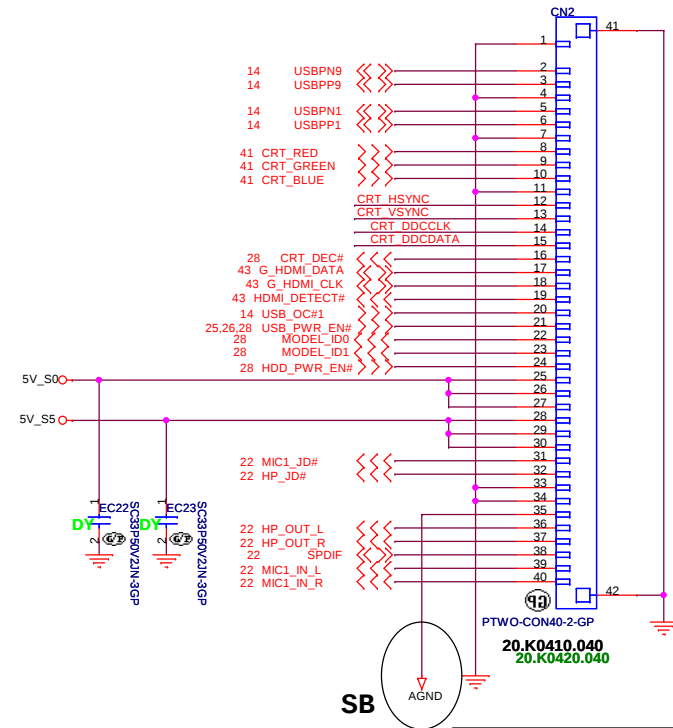
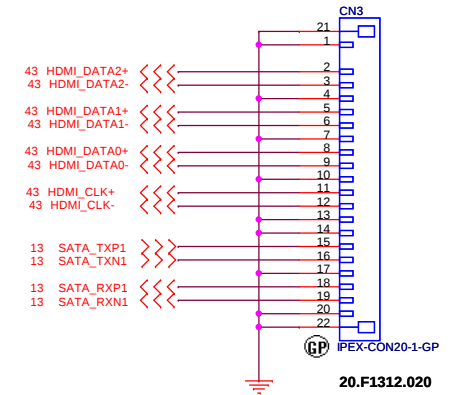
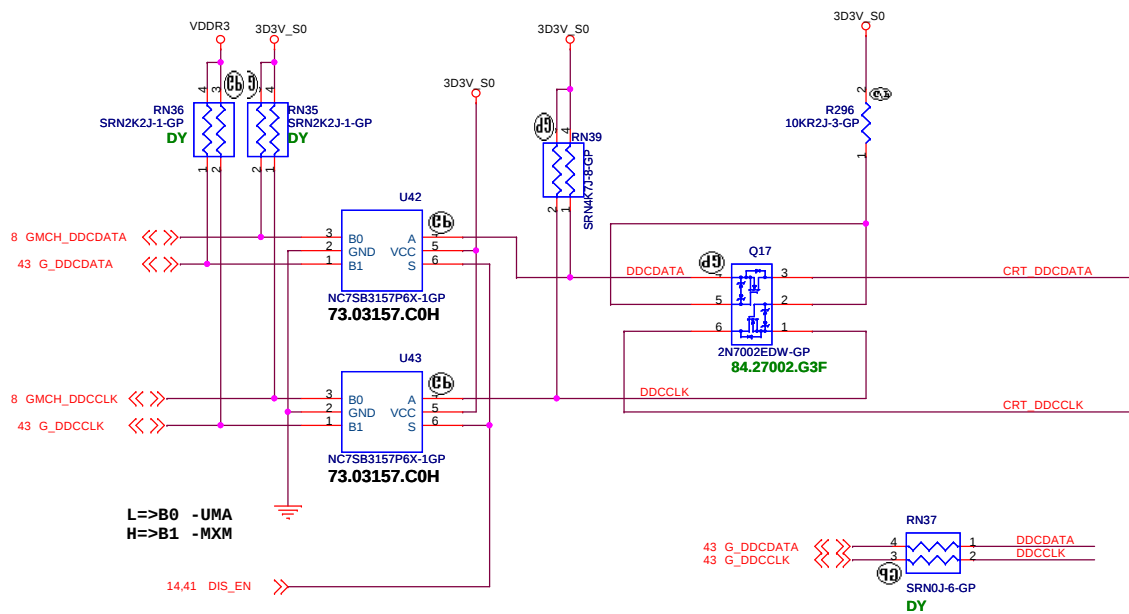
Internal MIC



Hsync & Vsync level shift



DDC_CLK & DATA level shift

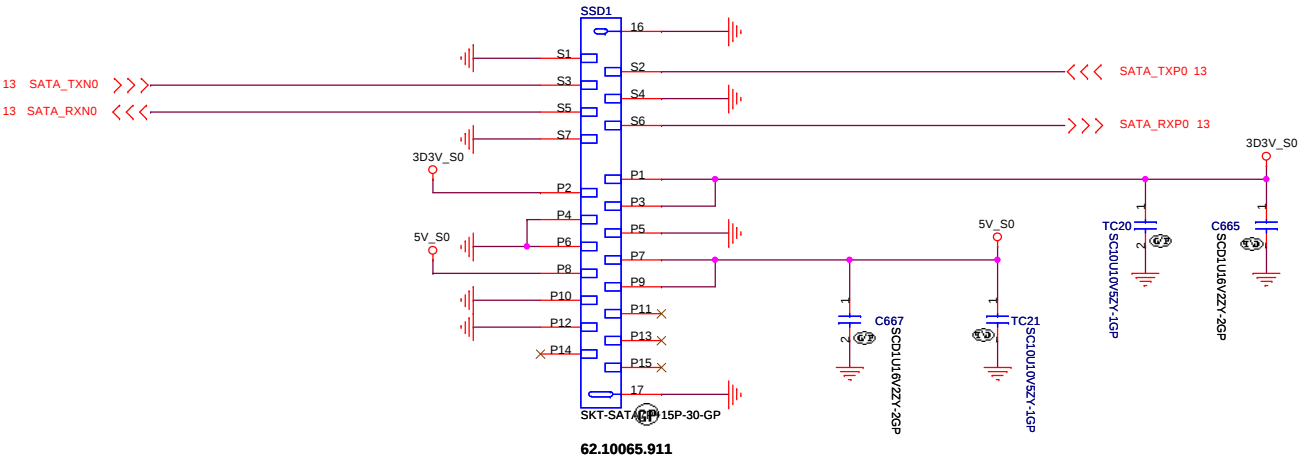


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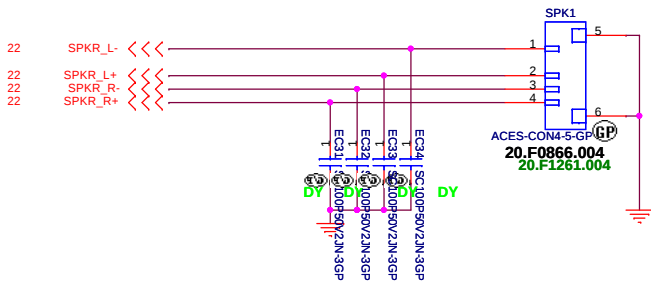
Title			CRT BD CONN
Size	Document Number	Rev	
		JM41 Discrete	
Date: Monday, March 02, 2009	Sheet 20	of	48

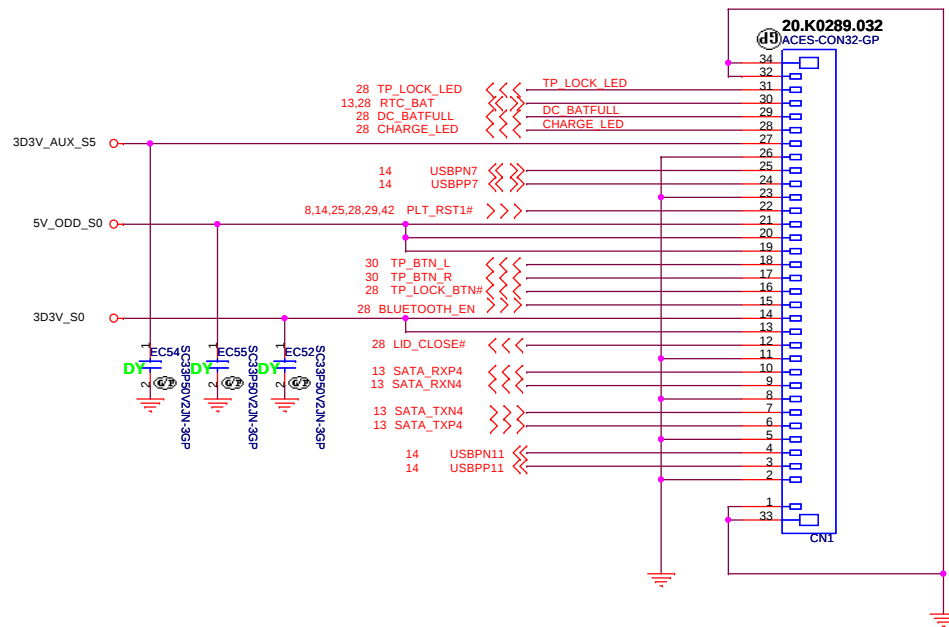
SB

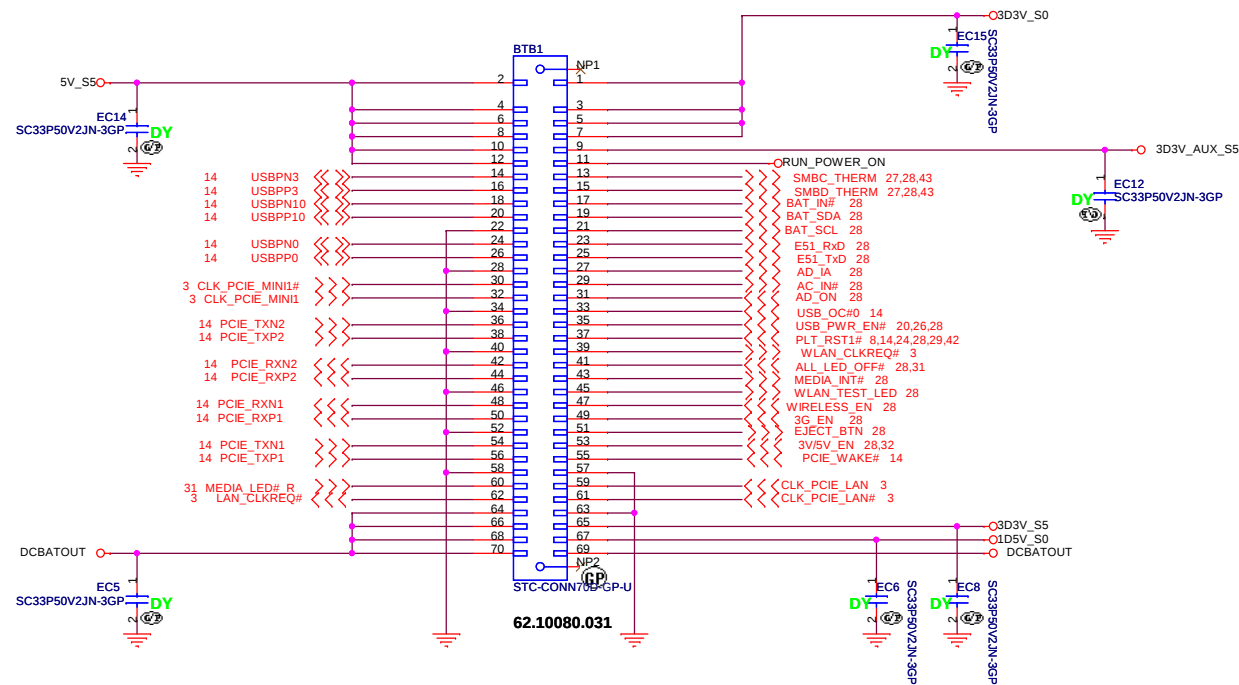
SSD SATA Connector



Internal Speaker

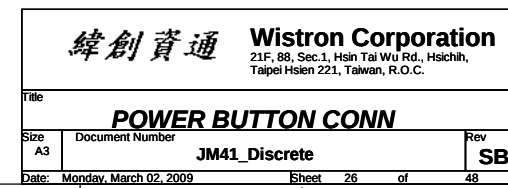


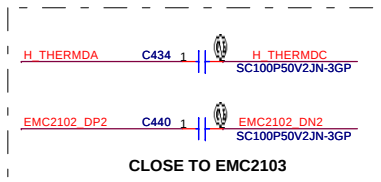




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Title		
MINI BD CONN		
Size	Document Number	Rev
A3	JM41_Discrete	SB
Date:	Tuesday, March 03, 2009	Sheet 25 of 48



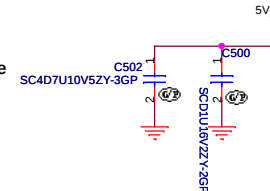


CPU TEMP:

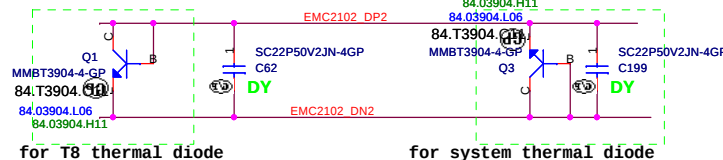
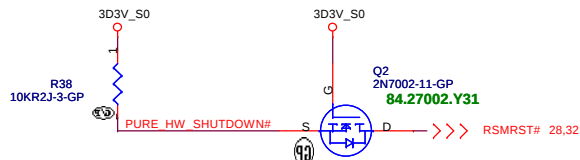
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near thermal diode



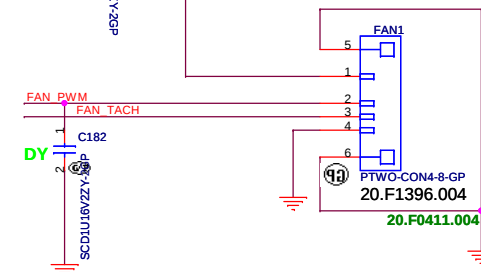
for CPU thermal diode



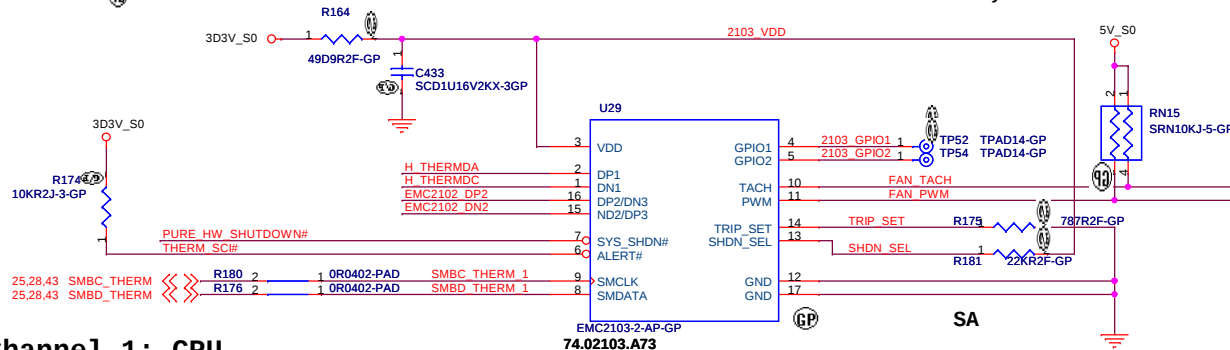
C587 for EMI and solve acoustic noise



for system thermal diode



ps. FAN1 POWER TRACE WIDTH MAY BE IN 25 MIL



Channel 1: CPU
Channel 2: Palmrest
Channel 3: T8

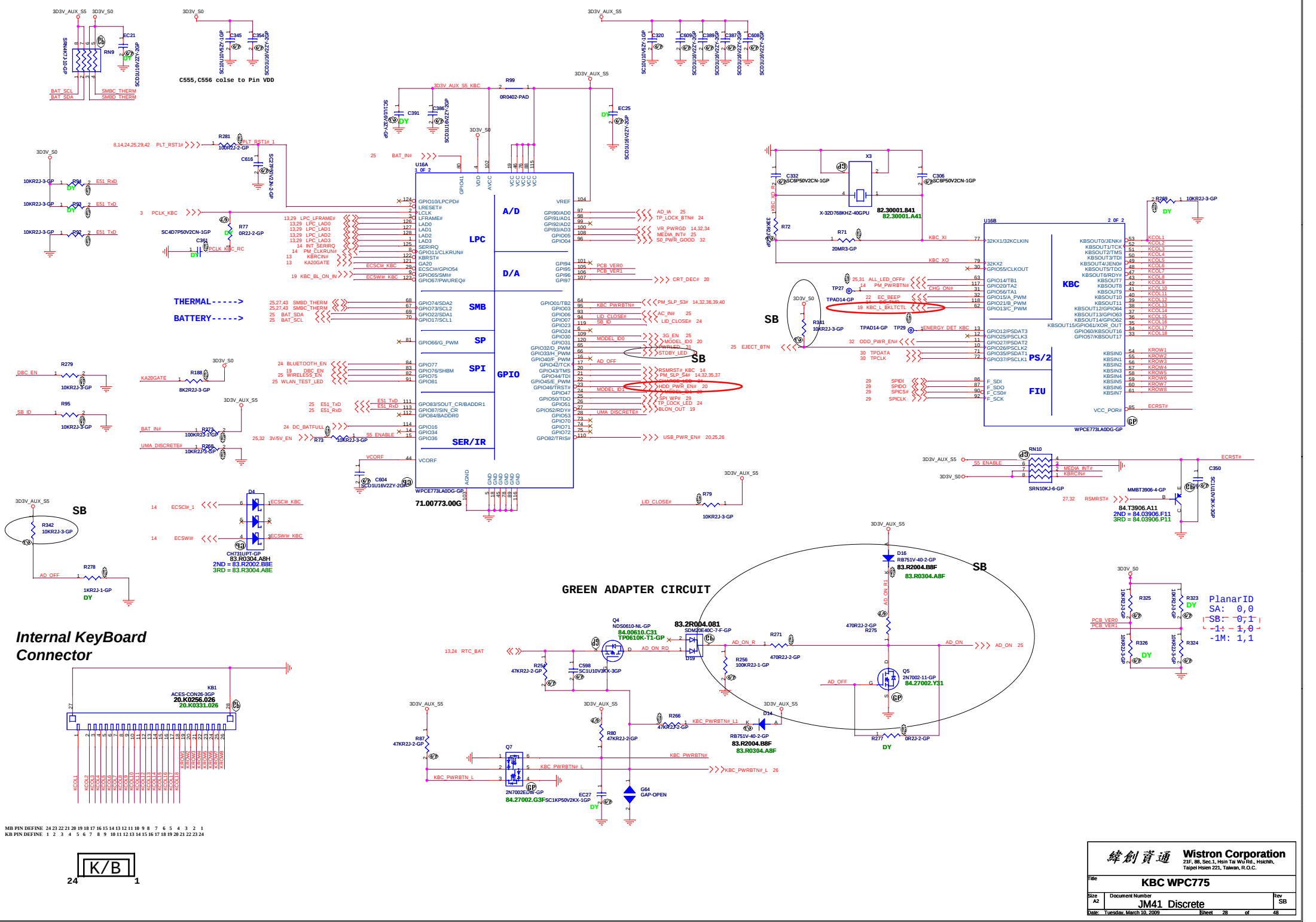
SHDN SEL

PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED, REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED, REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED

TRIP SET

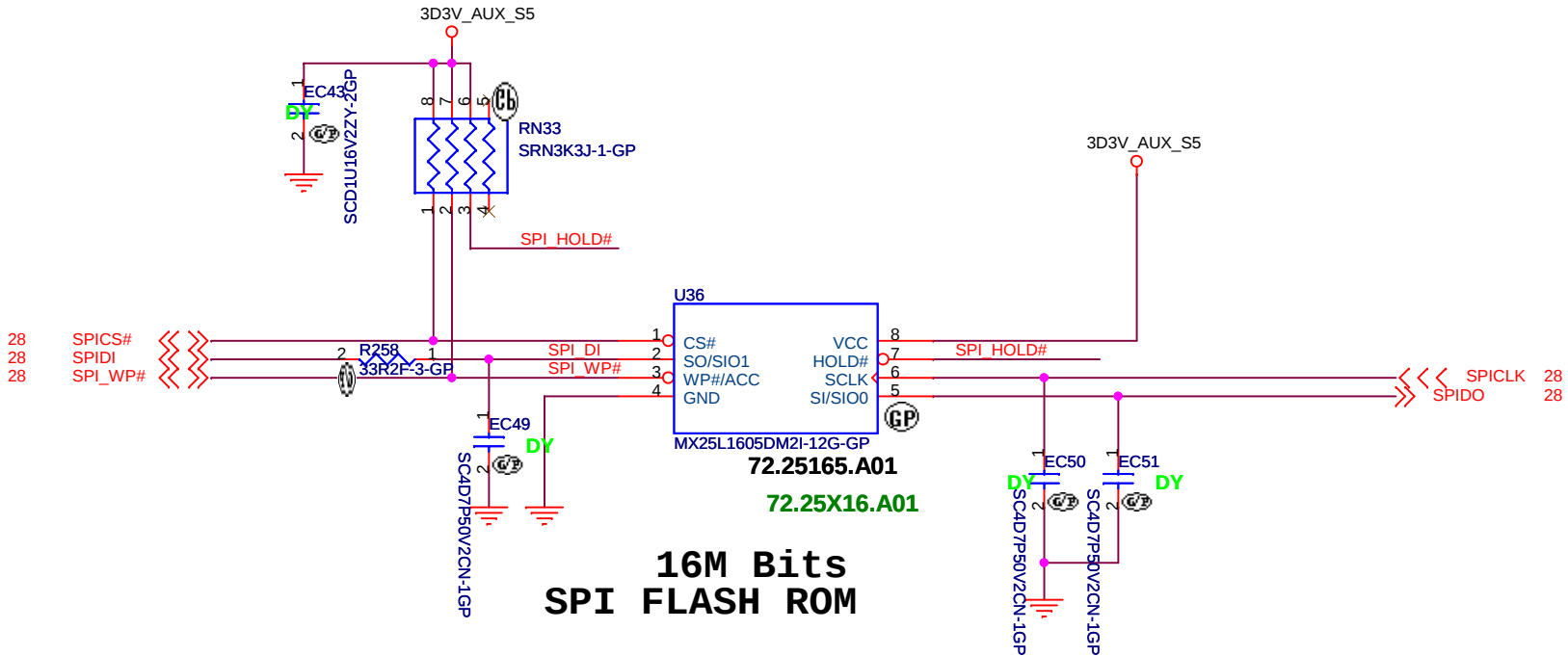
Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100

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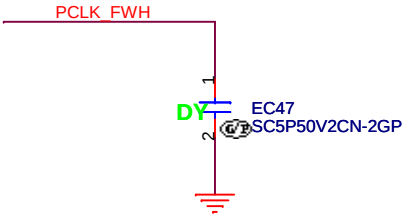
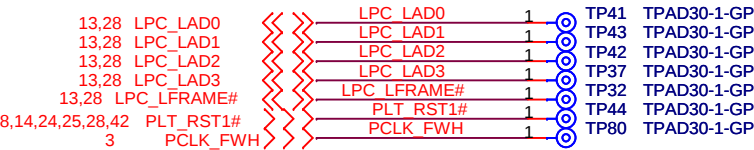


MB PIN DEFINE: 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24

24 **K/B** 1



GOLDEN FINGER FOR DEBUG BOARD



緯創資通

Wistron Corporation

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Title

BIOS

Size

Document Number

Rev

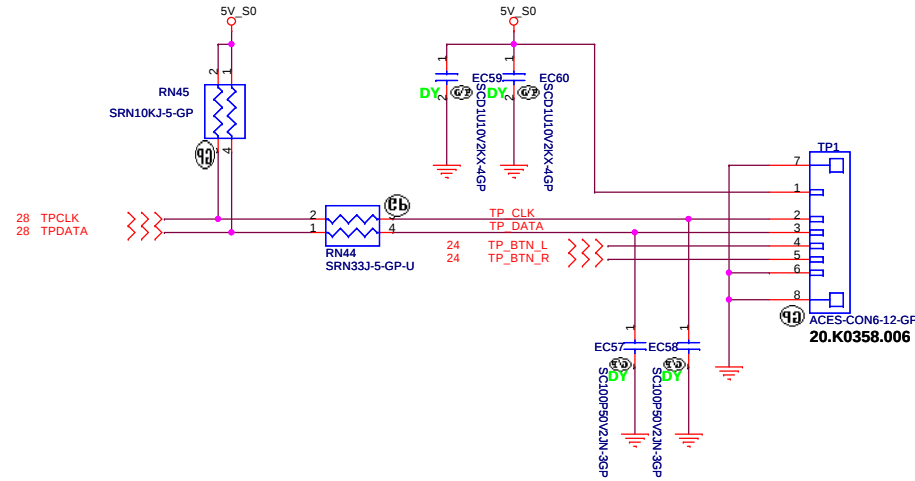
Monday, March 02, 2009

Sheet 29 of 48

SB

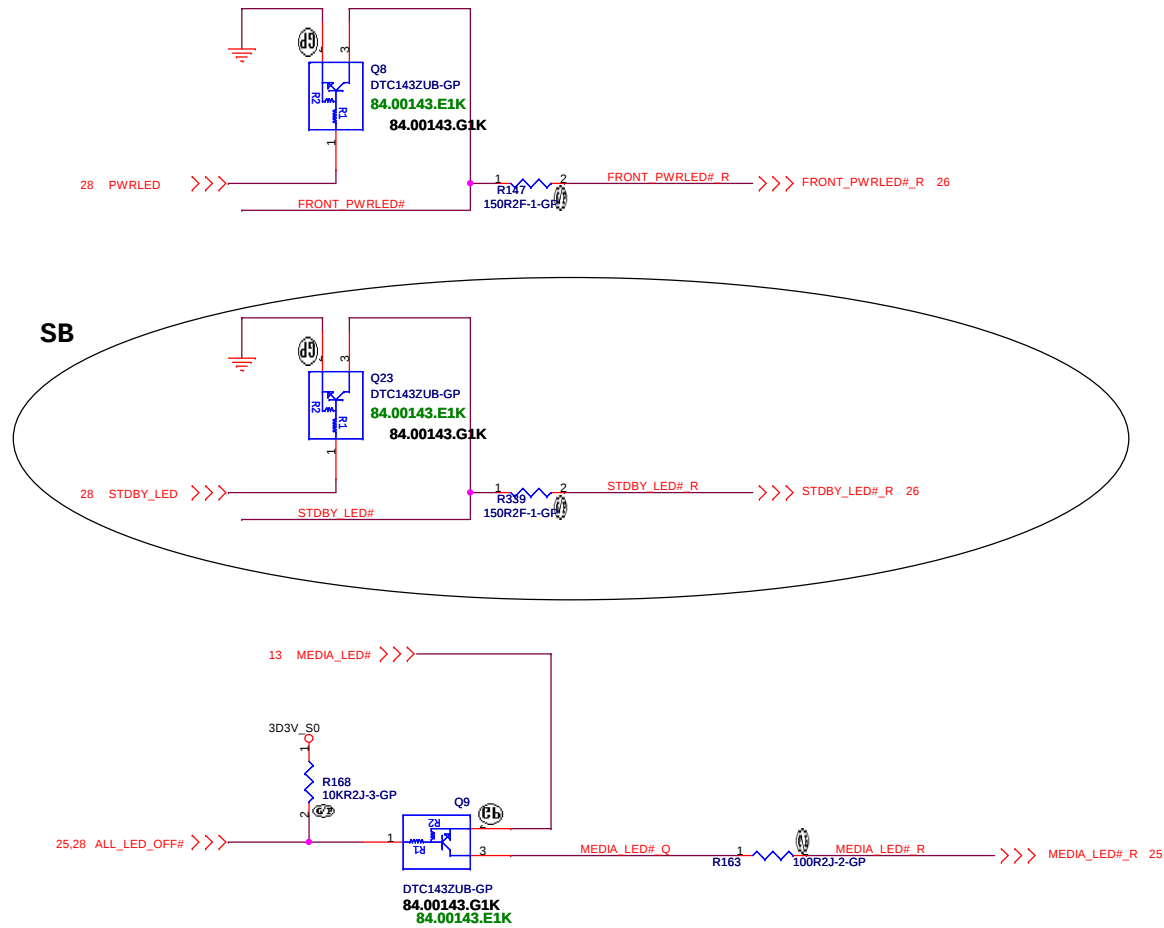
JM41 Discrete

TOUCH PAD

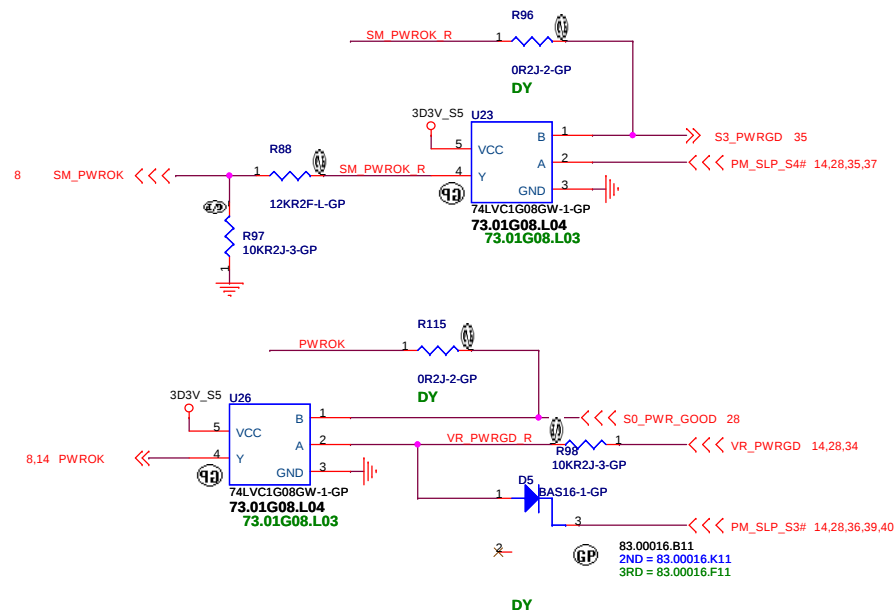
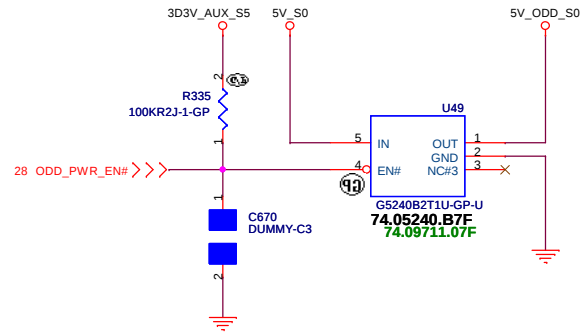


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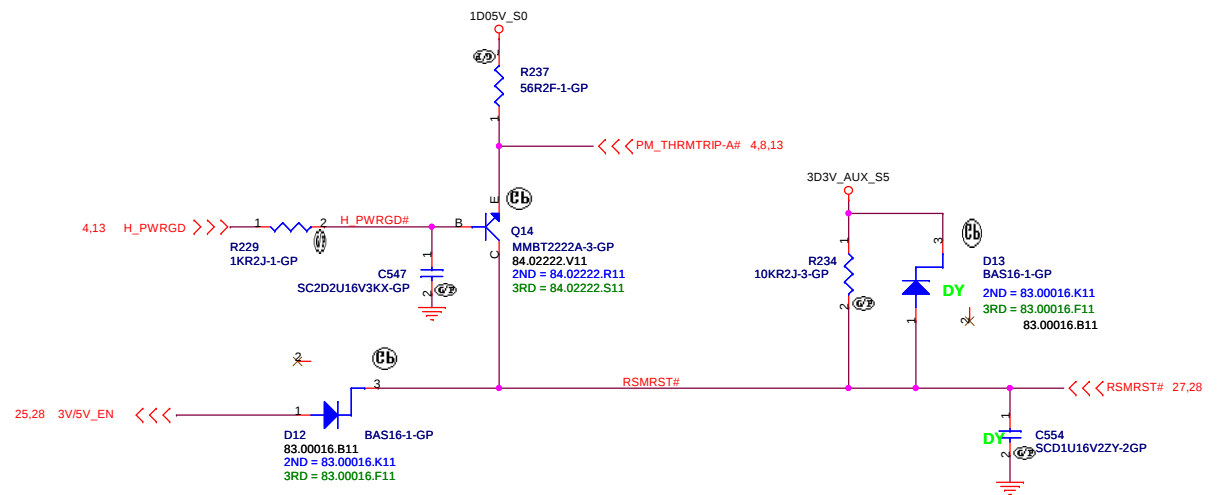
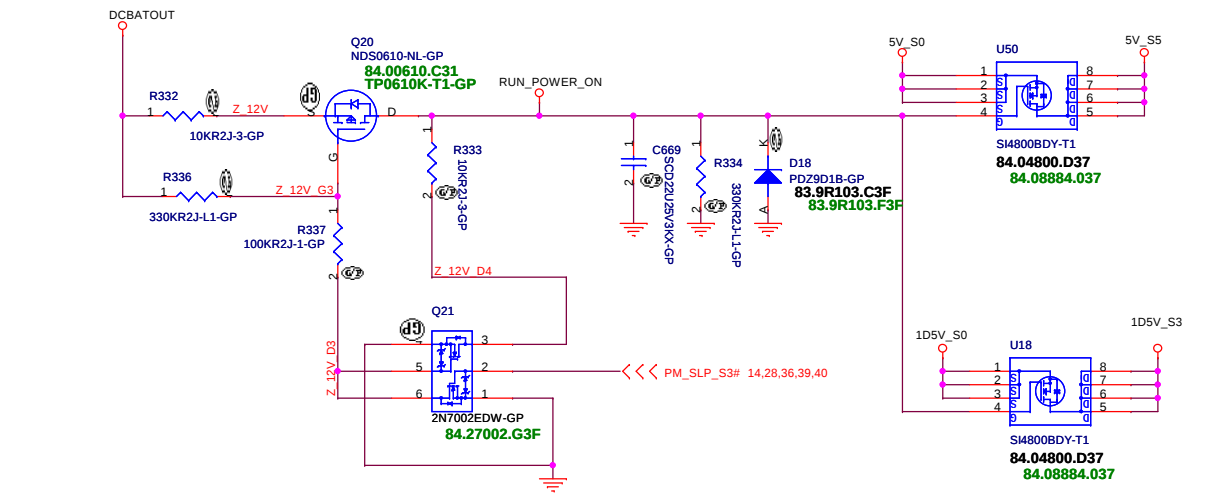
Title				
Touch PAD				
Size	Document Number			Rev
	JM41 Discrete			SB
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ODD Power



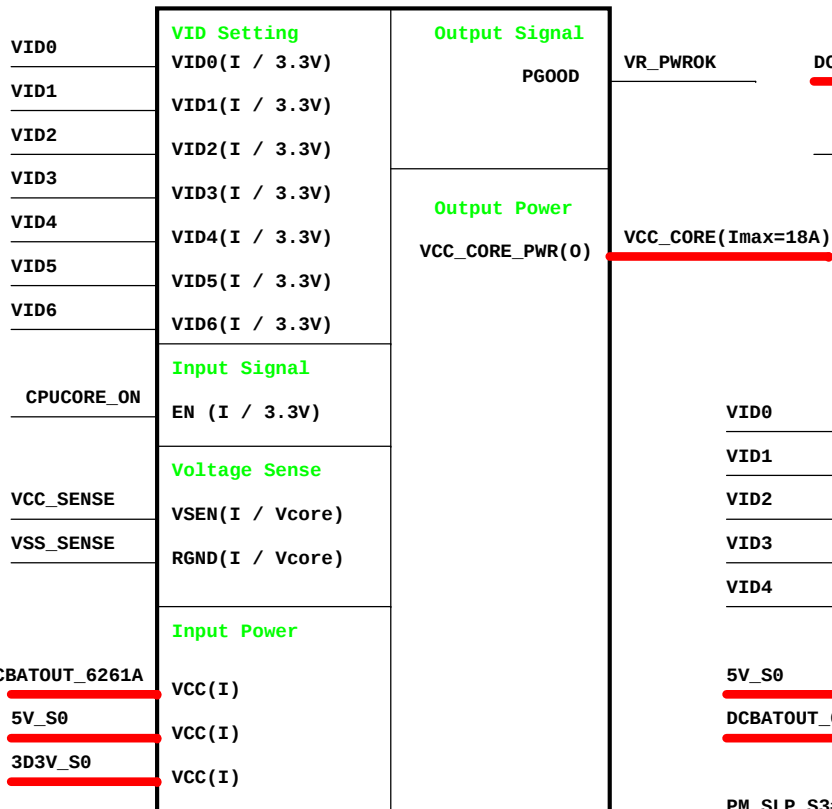
Run Power



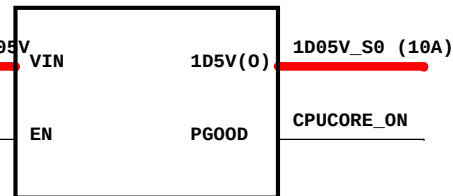
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
RUN & ODD POWER			
Size	Document Number	Rev	
	JM41_Discrete	SB	
Date: Monday, March 09, 2009		Sheet 32	of 48

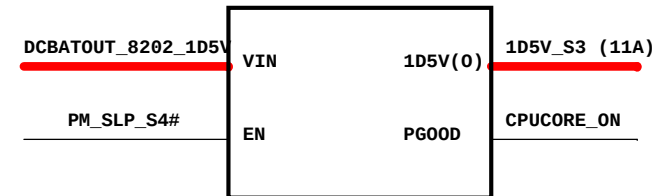
CPU_CORE
ISL6261A



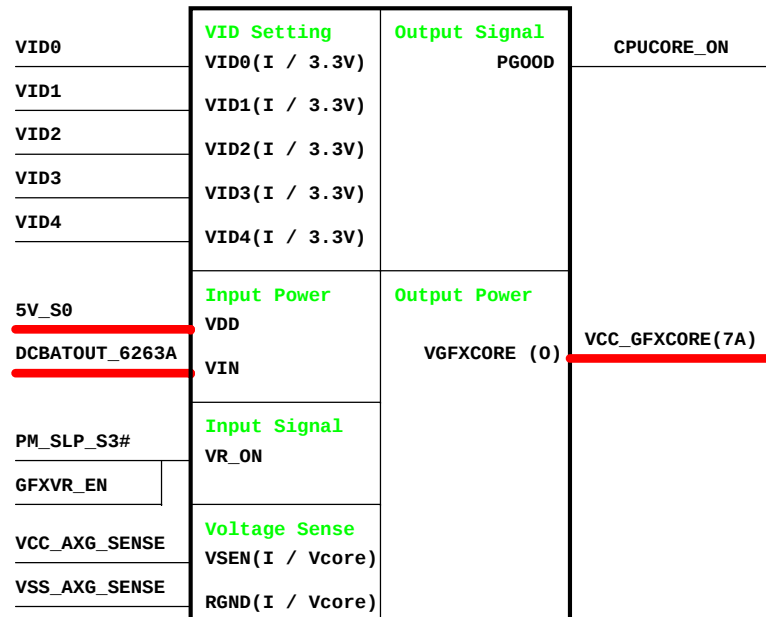
RT8202 1D05V_S0



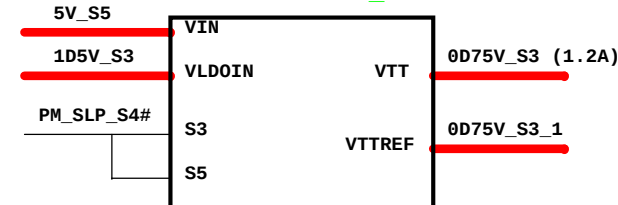
RT8202 1D5V_S3



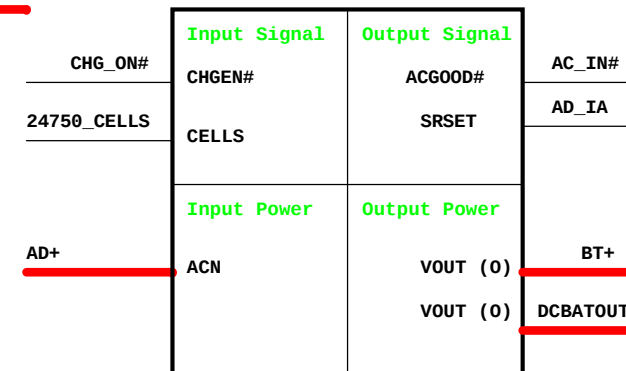
GFX_CORE
ISL6263A



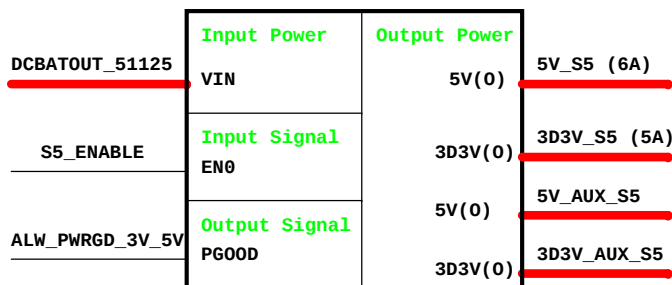
RT9026 0D9V_S0



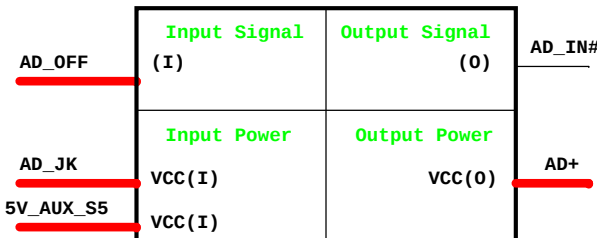
Charger MAX8731A



TPS51125
5V/3D3V

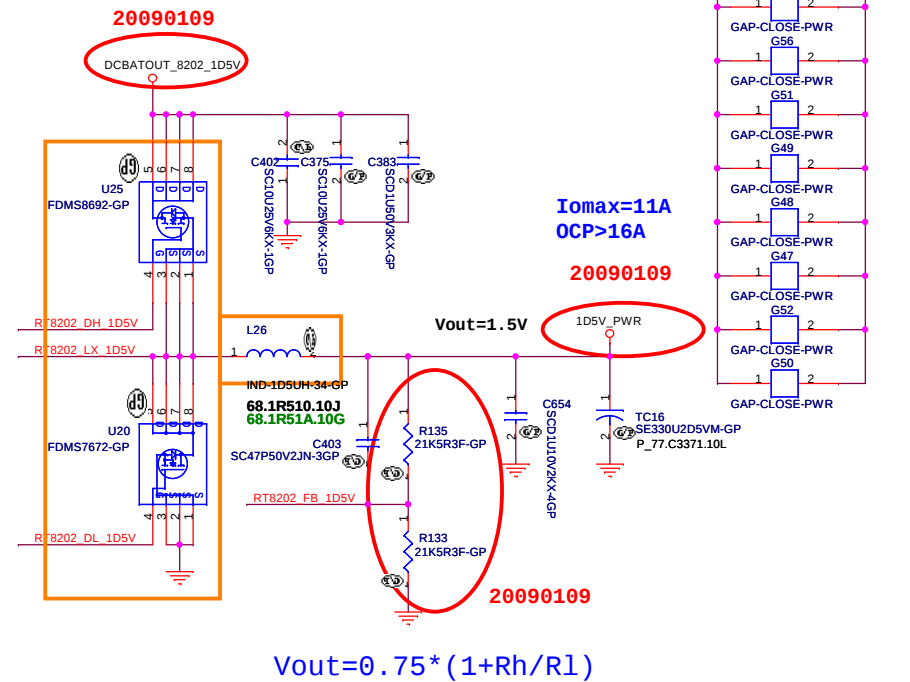
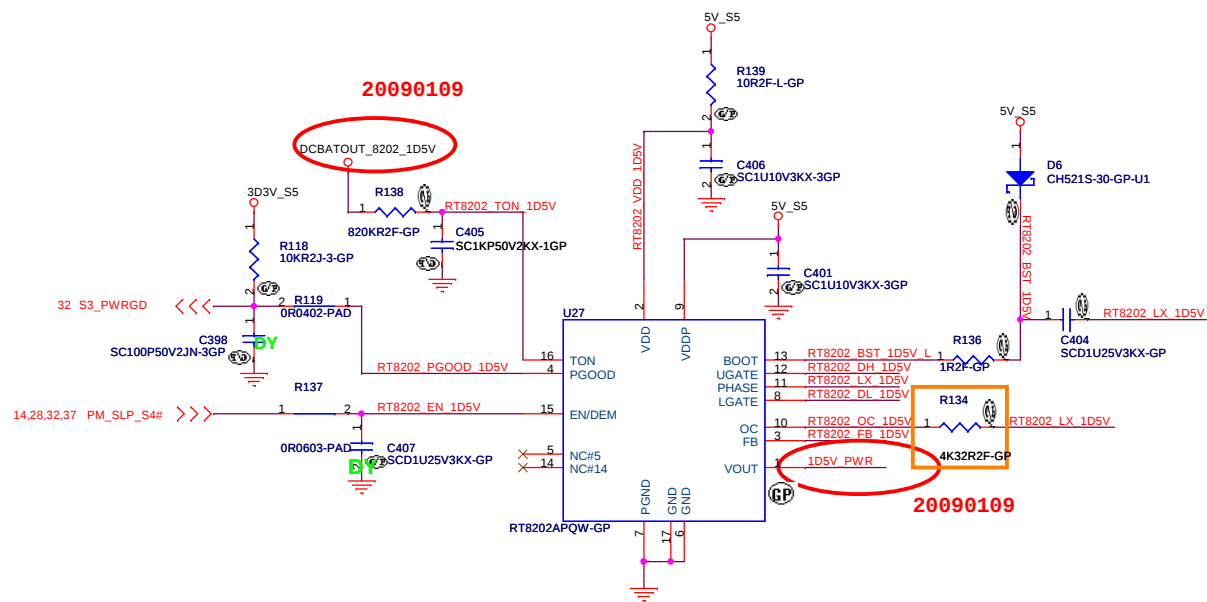
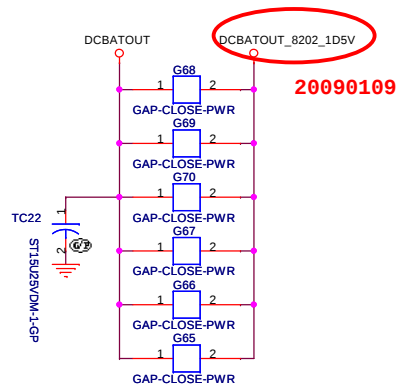


Adapter



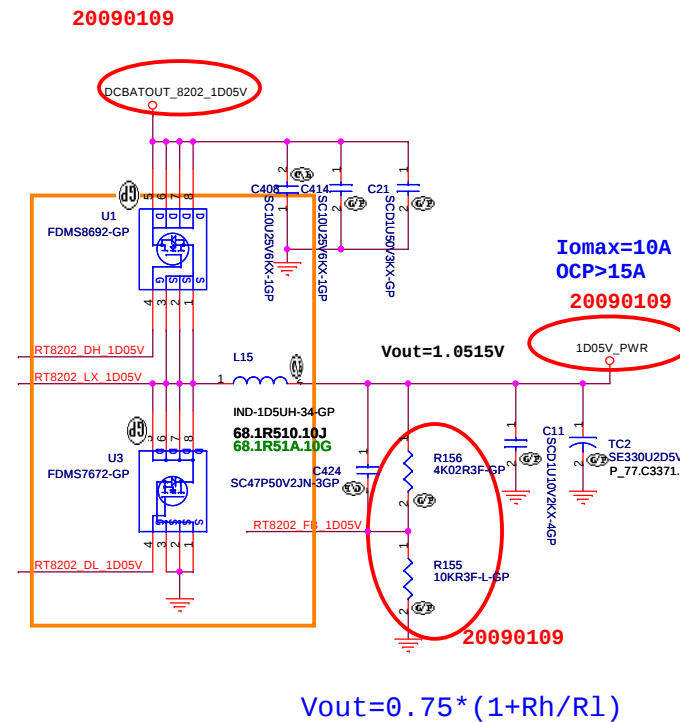
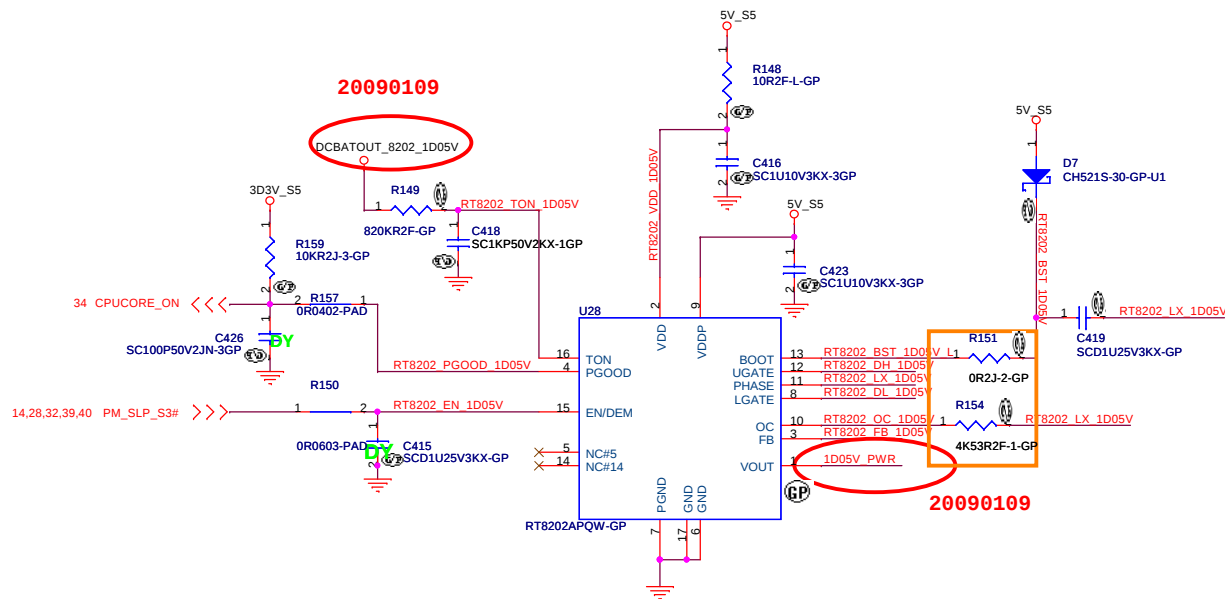
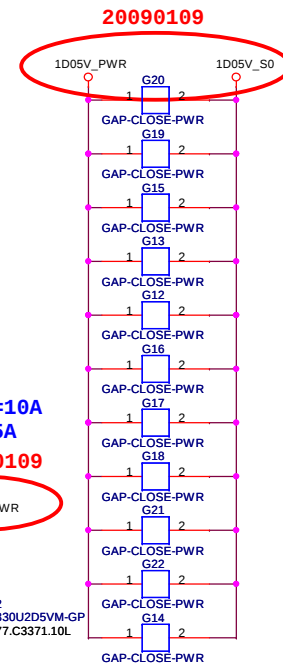
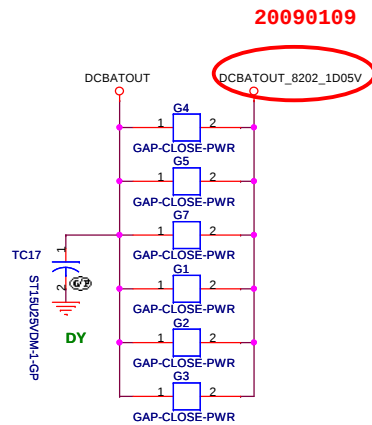
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Taipei Hsien 221, Taiwan, R.O.C.

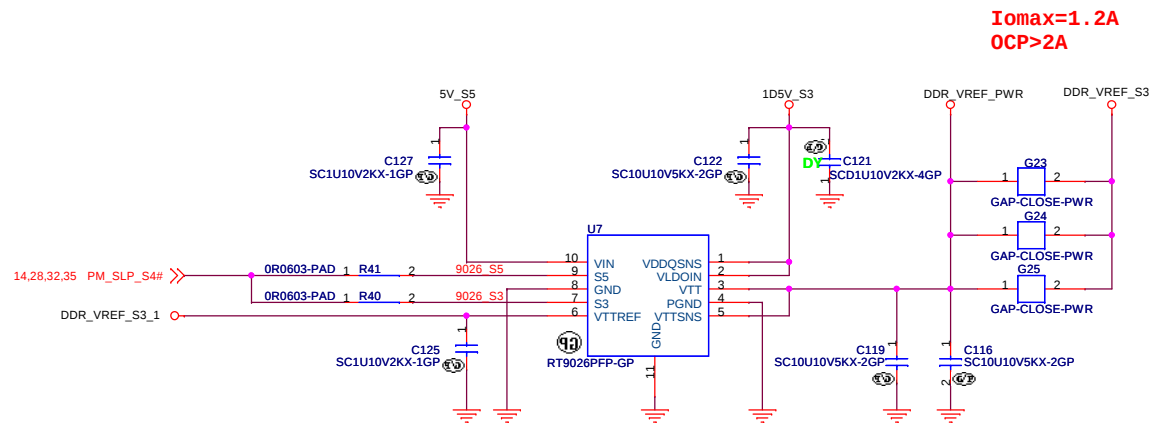
Title		
Power Sequence Logic		
Size B	Document Number	Rev
	JM41 Discrete	SB
Date: Monday, March 02, 2009	Sheet 33 of 48	



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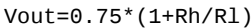
Title			RT8202 1D5V	
Size	Document Number	JM41 Discrete		Rev
A3				SB
Date:	Thursday, March 05, 2009	Sheet	35	of 48



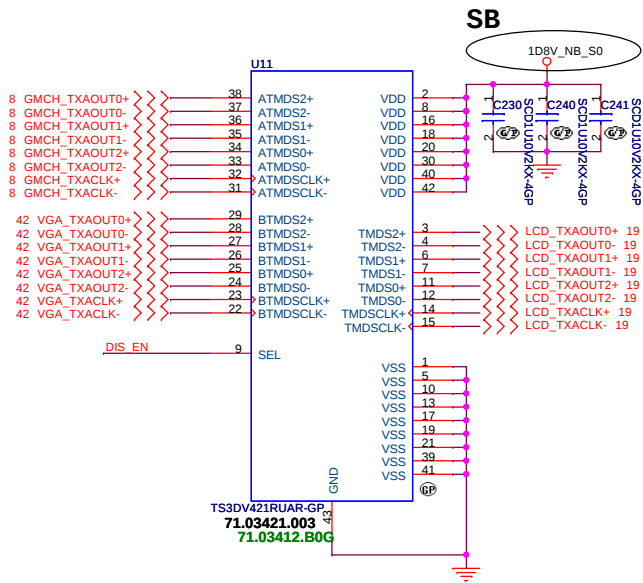


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Title			RT9026 0D75V	
Size	Document Number	JM41 Discrete		Rev
A3		SB		
Date:	Monday, March 02, 2009	Sheet	37	of 48

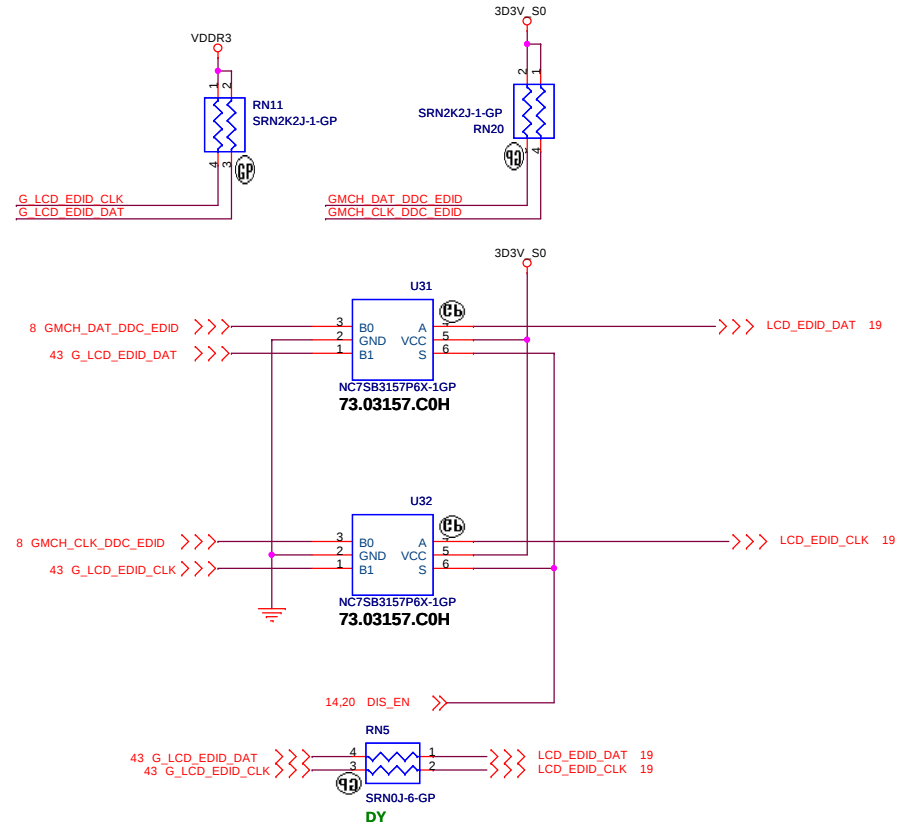


M92_XT	core power	
ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	1.2V

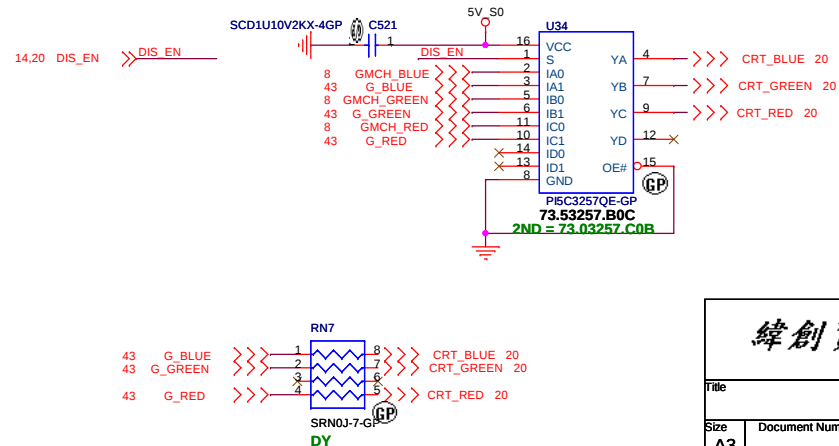
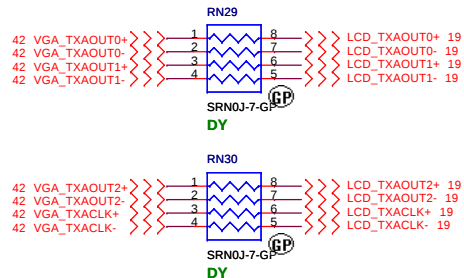


FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-



$\bar{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



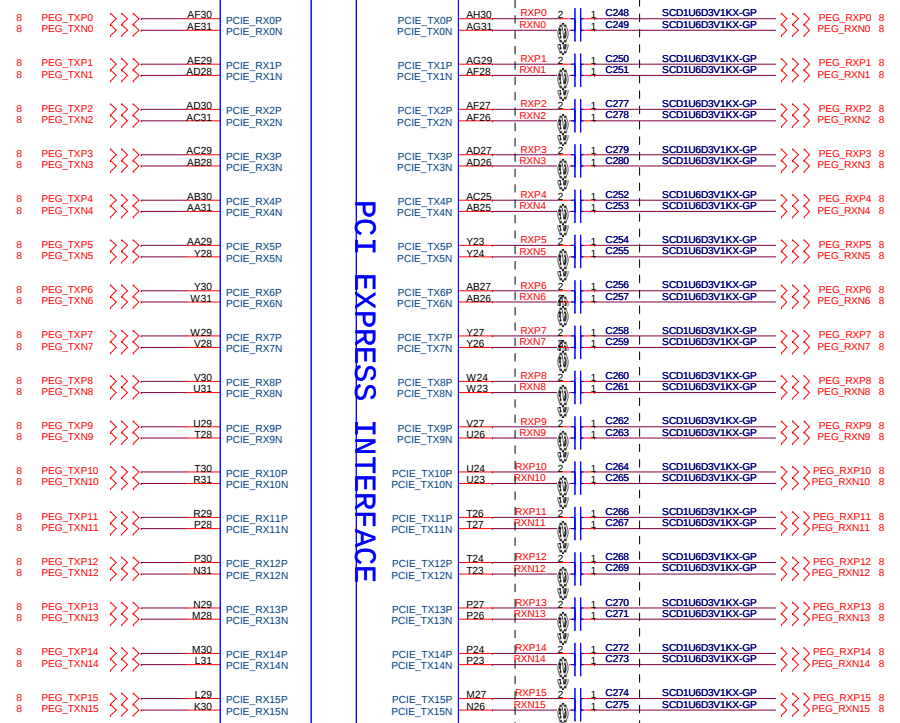
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Title: **PX SWITCH**

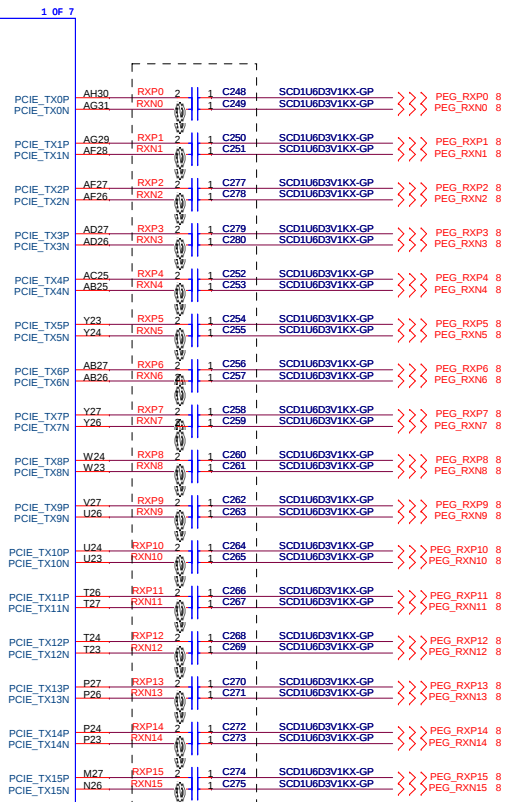
Size: A3 Document Number: Rev: SB

Date: Monday, March 02, 2009 Sheet 41 of 48

SSID = VIDEO

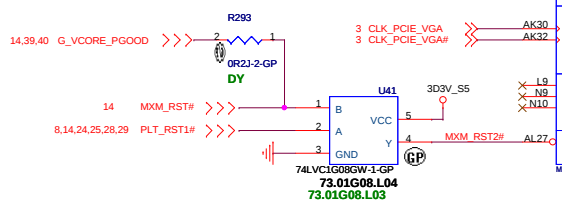
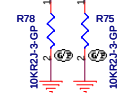
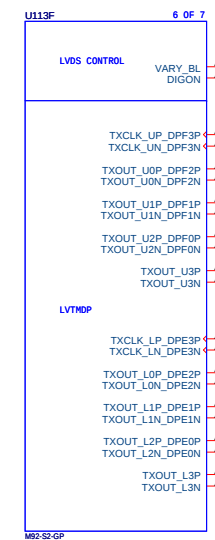


PCI EXPRESS INTERFACE



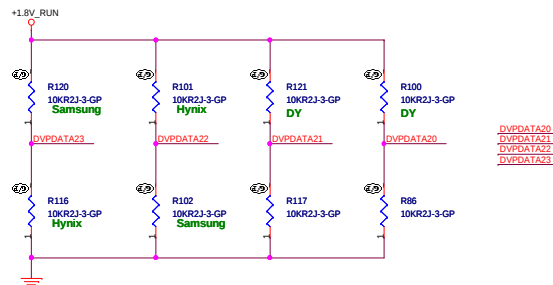
0201 CAPs

CALIBRATION

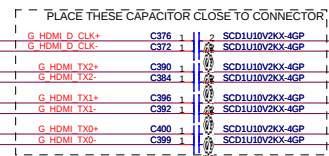
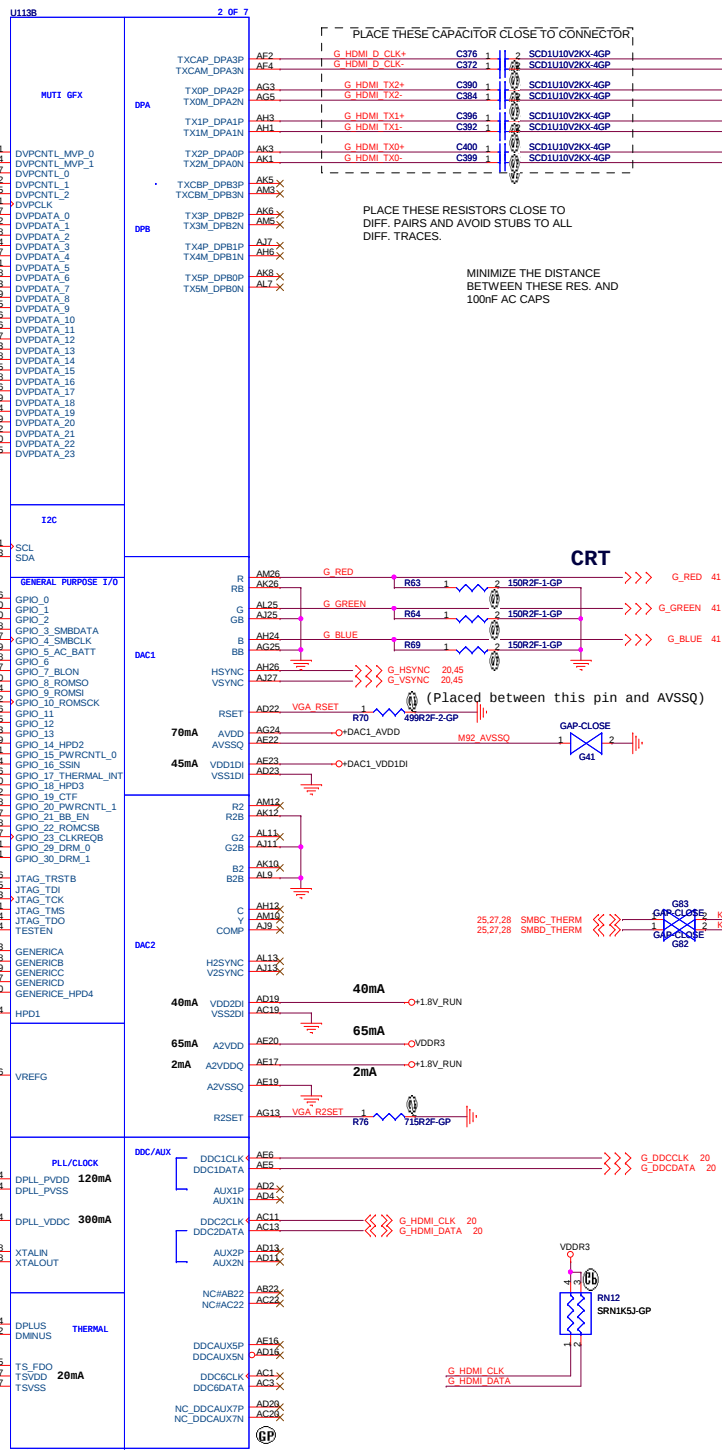
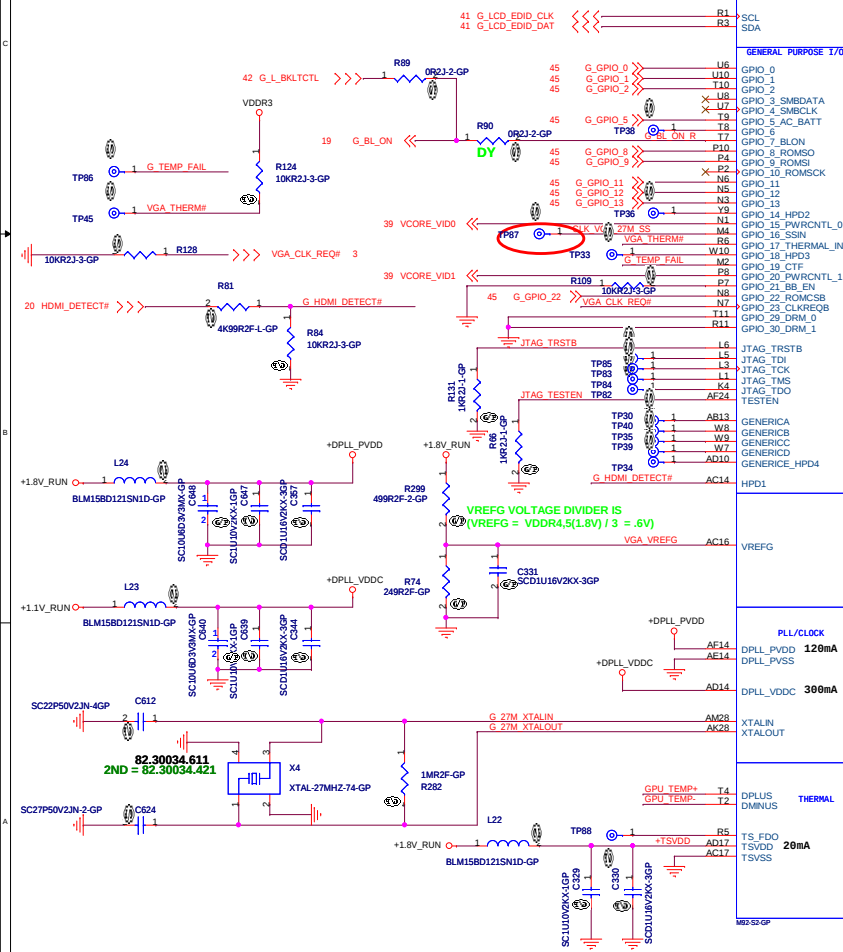


SSID = VIDEO

```
DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung
```

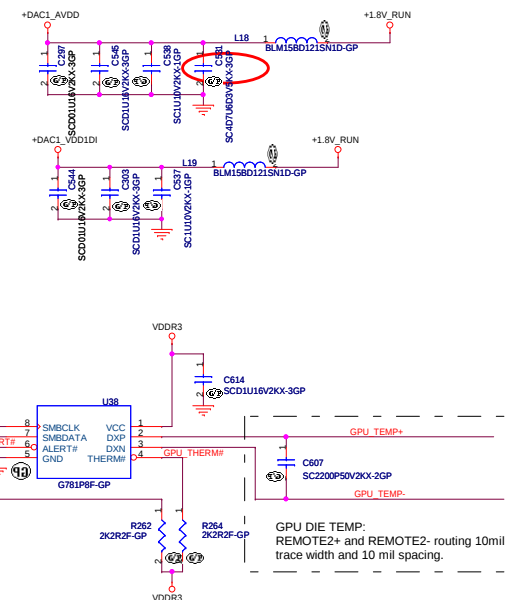
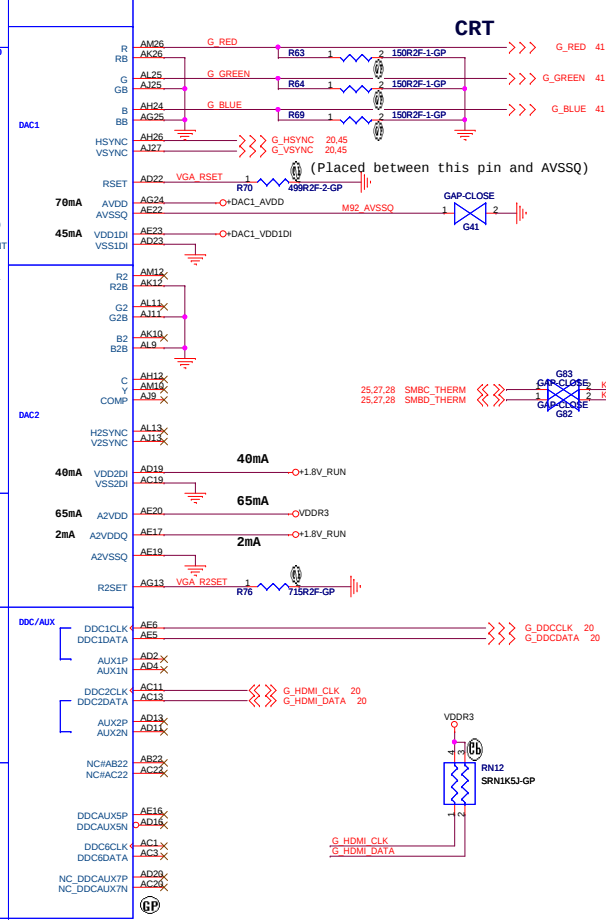


STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(23:20) (Internal PD)	MEMORY TYPE, MAKE AND SIZE INFO 0000 - GDDR3 16Mx32 Qimonda 0001 - GDDR3 32Mx32 Hynix 0010 - GDDR3 32Mx32 Qimonda 0011 - GDDR3 32Mx32 Samsung



PLACE THESE RESISTORS CLOSE TO
DIFF. PAIRS AND AVOID STUBS TO ALL
DIFF. TRACES.

MINIMIZE THE DISTANCE
BETWEEN THESE RES. AND
100nF AC CAPS

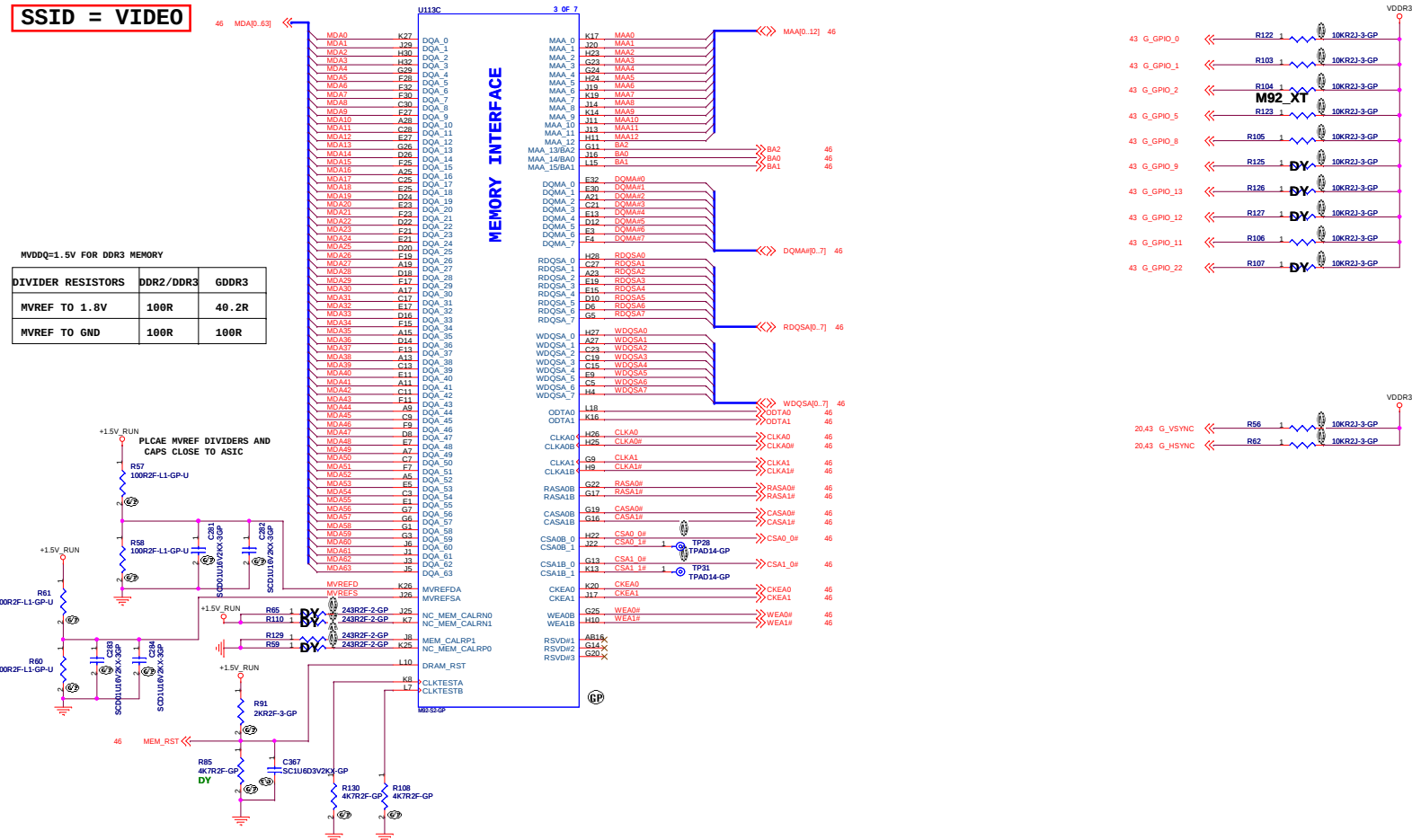


U113E



Title			
VGA-POWER/GND(3/4)			
Size A2	Document Number		Rev S
JM41 Discrete			
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SSID = VIDEO



FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED
THEY MUST NOT CONFLICT DURING RESE

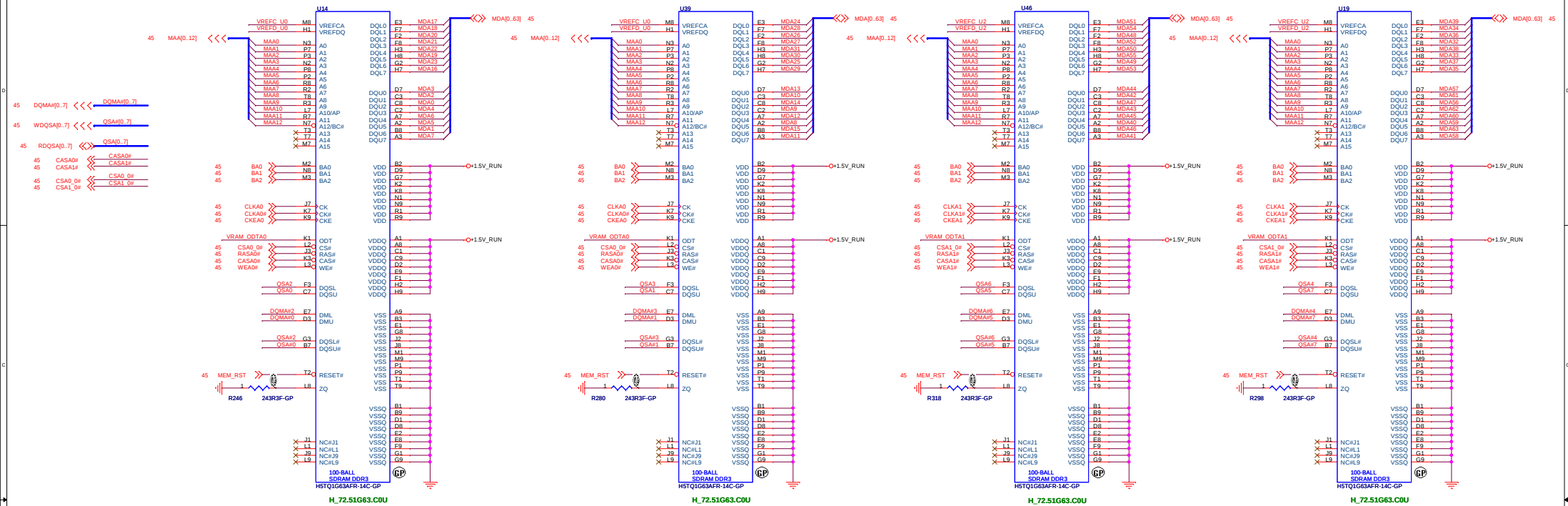
GPI03 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED,
THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1			
Size of the primary memory apertures	GPIO[9,13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]	
V	128MB	x000	ST Microelectronics	M25P05A	0100
	256MB	x001		M25P10A	0101
	64MB	x010		M25P20	0101
	32MB	x		M25P40	0101
	512MB	x		M25P80	0101
	1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
	2GB	x		Pm25LV810A	0101
4GB	x				

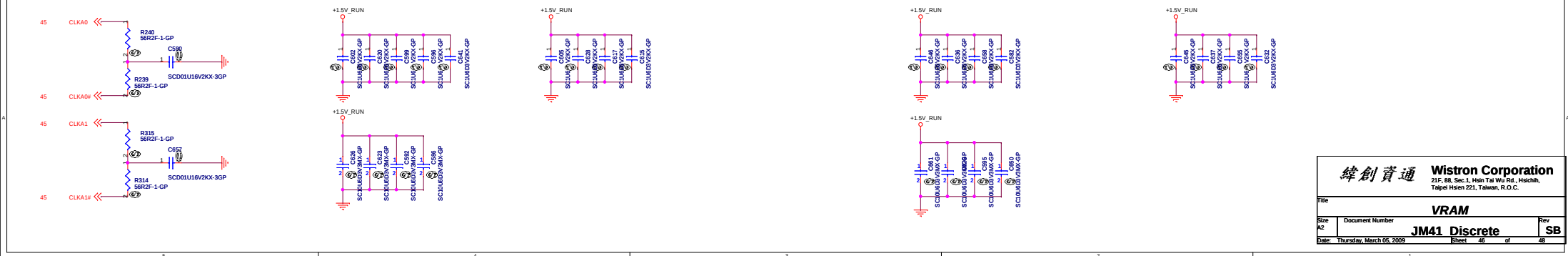
STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPI08	Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing ✓
TX_DEEMPH_EN (Internal PD)	GPI01	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled ✓
BIF_GEN2_EN_A	GPI02	✓ 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPI08	0= Disable CLKREQ# power management capability 1= Enable CLKREQ# power management capability ✓
ROMIDCFG[3:0] (Internal PD)	GPI0[13,12,11]	if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN (Internal PD)	GPI0_22_ROMCSB	✓ Enable external BIOS ROM device 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00=No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI ✓

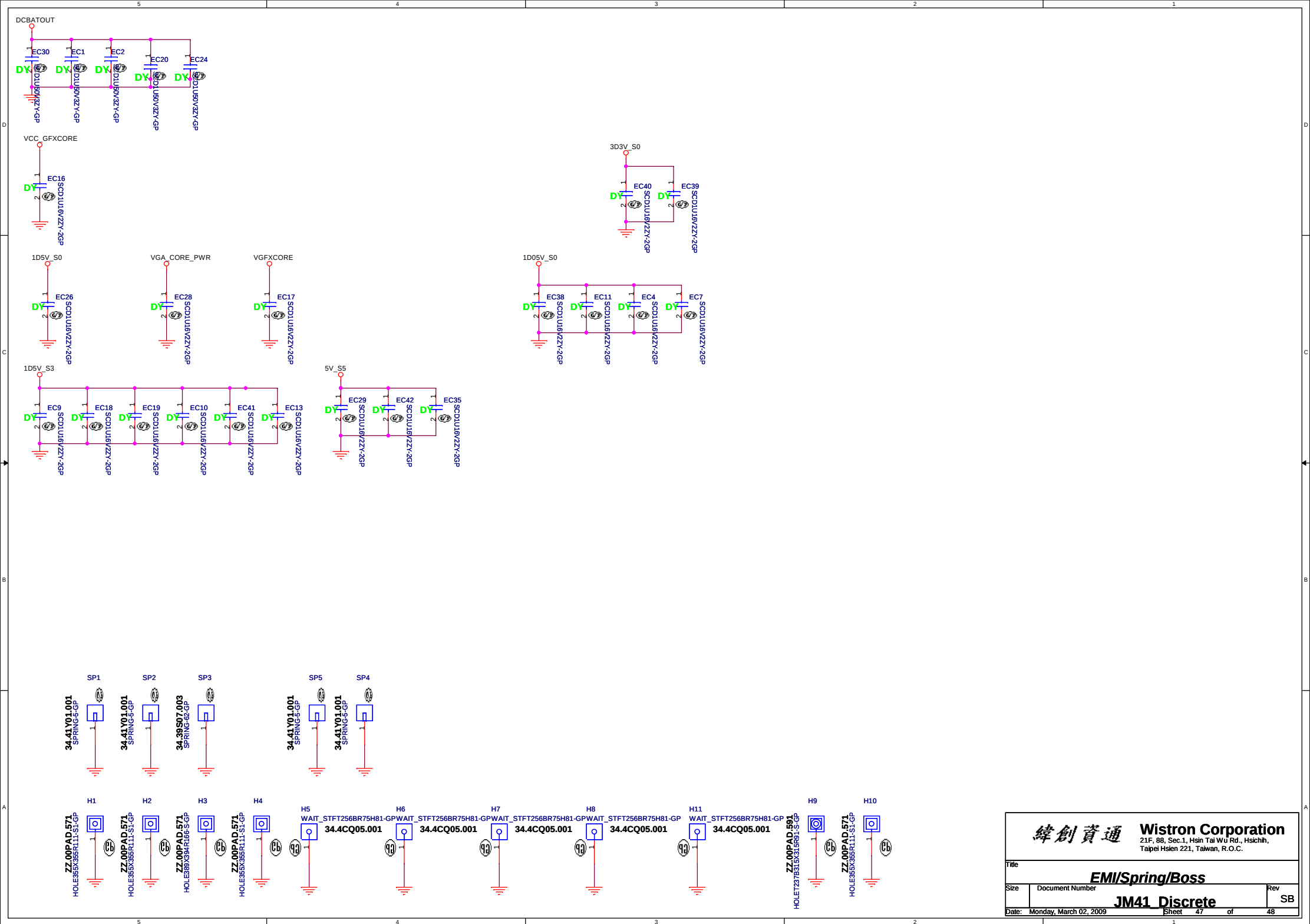
512MB DDR3

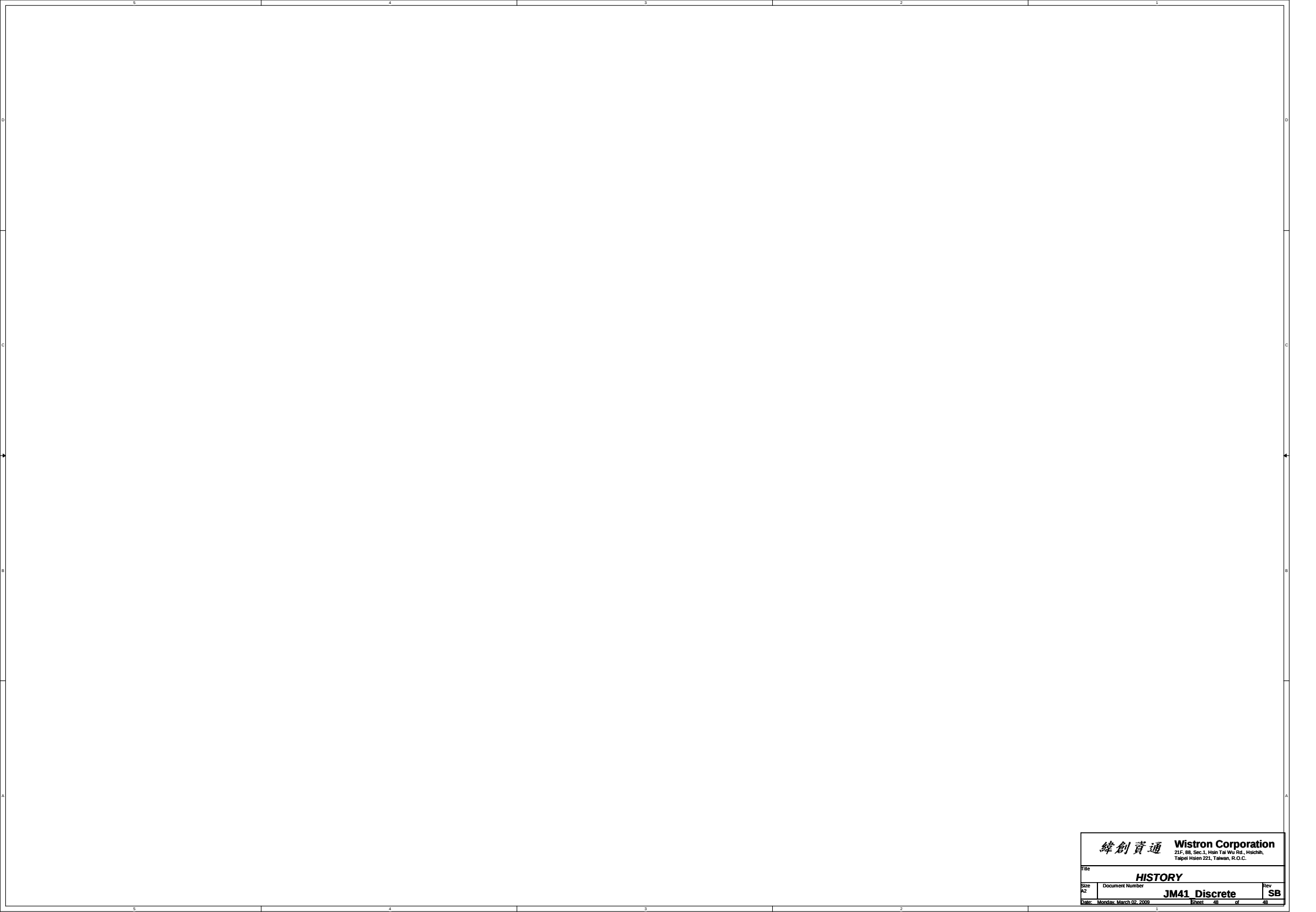


Samsung : K4W1G1646E-EC12

Hynix : H5TQ1G63BFR-12C







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Title

HISTORY

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