

Project code: 91.4H001.001
PCB P/N : 55.4H001.XXX
REVISION : 06237-2(GCE, Hannstar)



ICH8M Functional Strap Definitions

ICH8-M EDS 21762 2.0V1 page 16

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPI020	Reserved	This signal should not be pulled high.
GNT1#/ GPI051	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSusi_05, VccSusi_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSusi_05, VccSusi_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPI033/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOw#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	6:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIe Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	USB4
4	MINIC1
5	BT
6	CCD
7	Finger
8	NEW
9	NC

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K (?)
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPI023	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K (?)
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

2007/02/16
1. Page 33: Add SIO 87381 for FIR Issue.
2. Page 31, change KBC from 8768L to 8763L.
3. Page 33, del U33(LPC golden Finger).
4. Page 24/32, change ERC1/ERC2 due to 77.61021.02L is Obsoleted Part !
5. Page 37, del TC22/TC19.
6. Page 38, del TC1/TC4.

2007/02/09
1. Page 14:Modify "Q14" "BTBTN1" "WLBTN1" symbol.
2. Page 36, 37, 38: Replace 0ohm with 0ohm pad.

2007/02/08a
1. Page 14:Modify R428 to"FRONT_PWRLED#_1"and RN58 pin7 to"STBY_LED#_2"due to LED brightness issue.
2. Page 38:Replace "TC26" with "77.C1561.01L".

2007/02/08
1. Page 10:Replace "R244" with "0603-PAD".
2. Page 36:Replace open power gap with close power gap.
3. Page 38:Add capacitor "TC26" for acoustic noise

Crestline Strapping Signals and Configuration

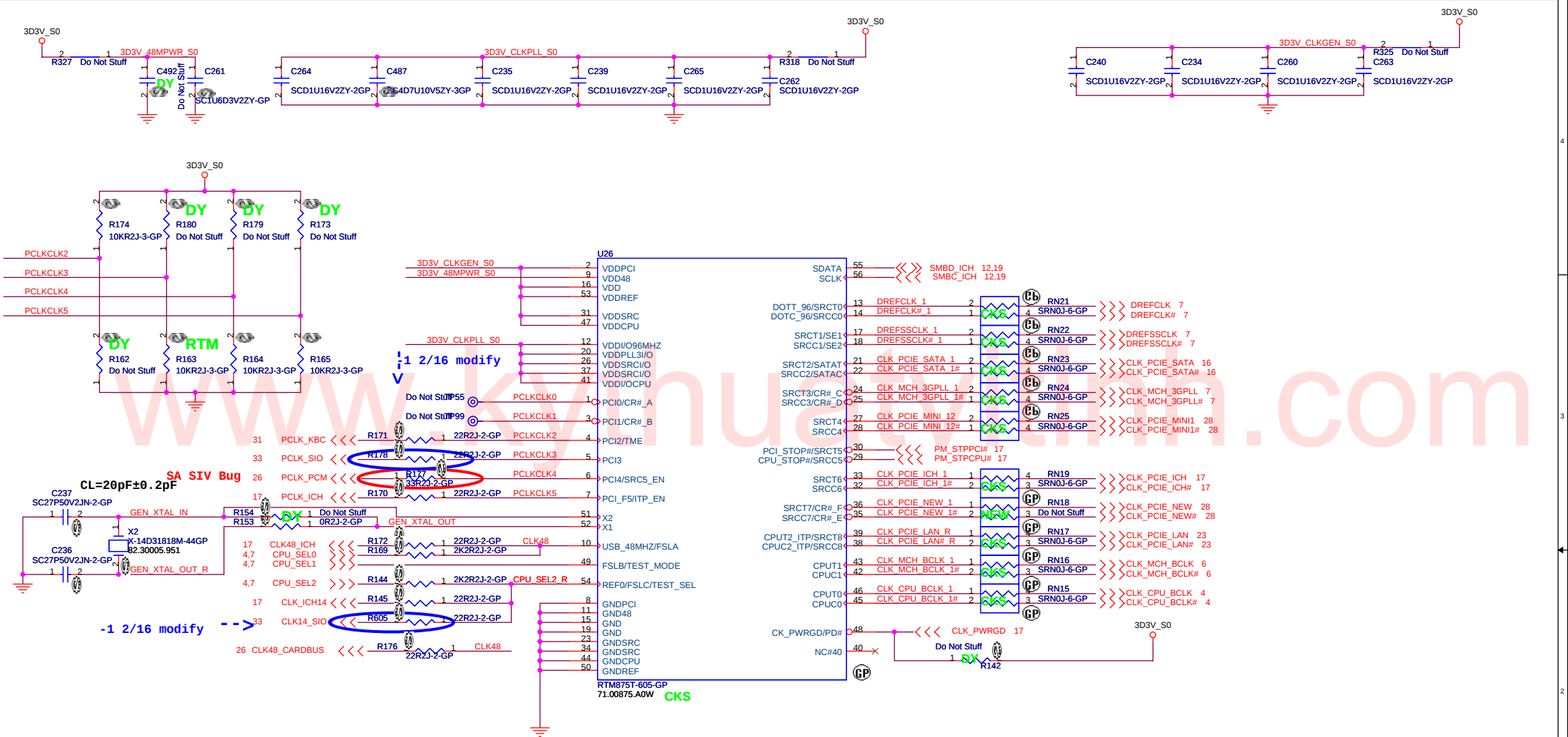
Crestline EDS 20954 1.0 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

55.4H001.S03G

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Title			
Reference			
Size A3	Document Number	Biwa	Rev -2
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ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP#, pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP#, pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

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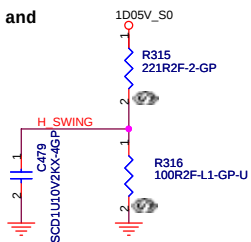
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator**

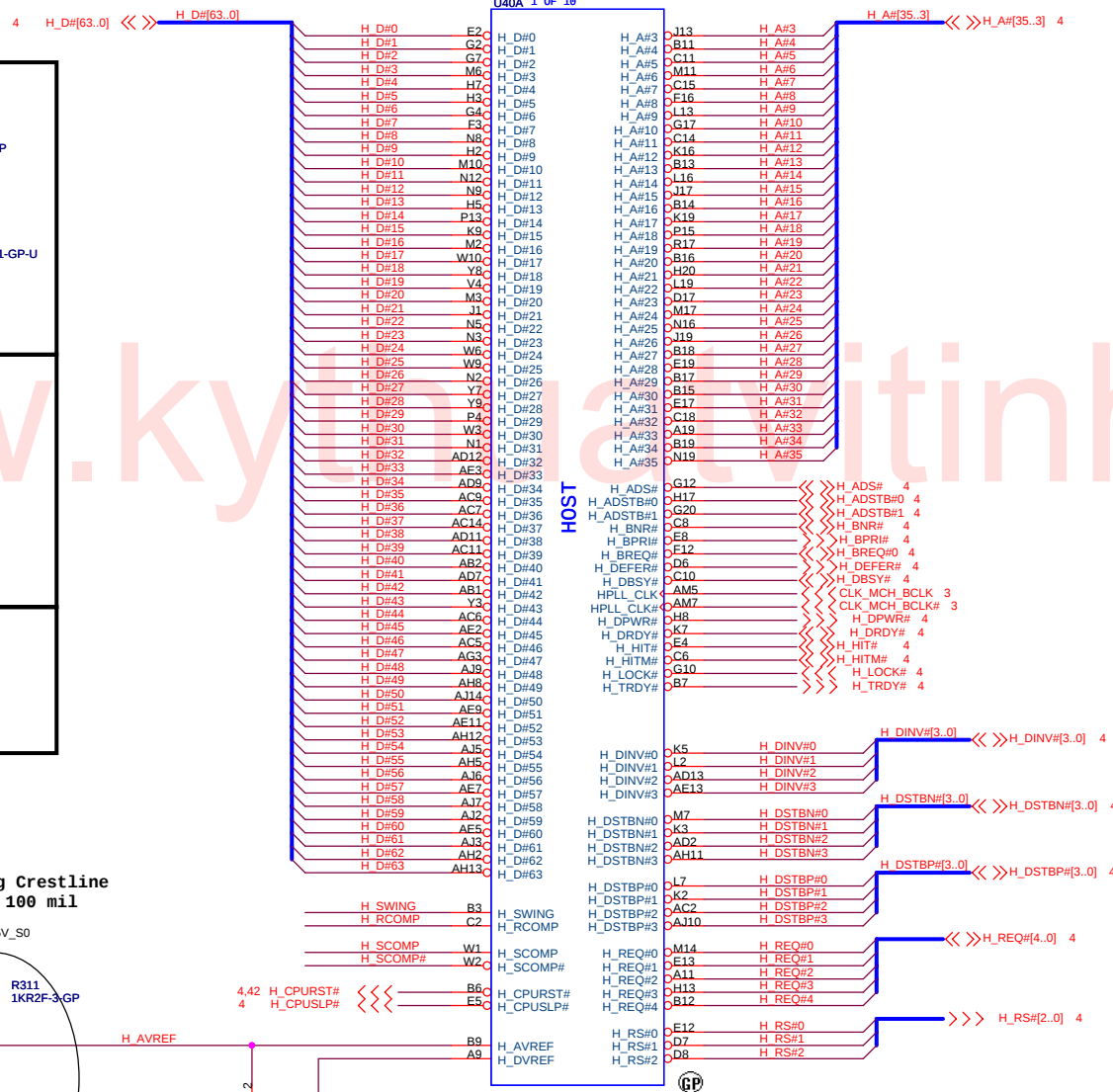
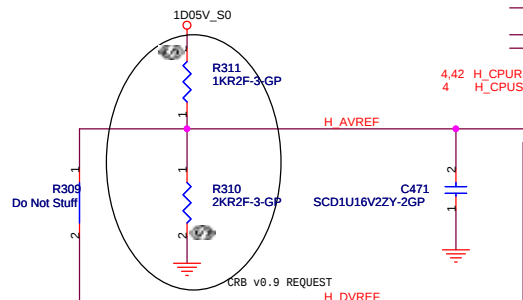
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H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)



H_REF Decoupling Crestline
close Crestline 100 mil



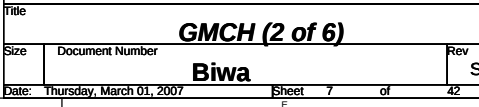
緯創資通 **Wistron Corporation**
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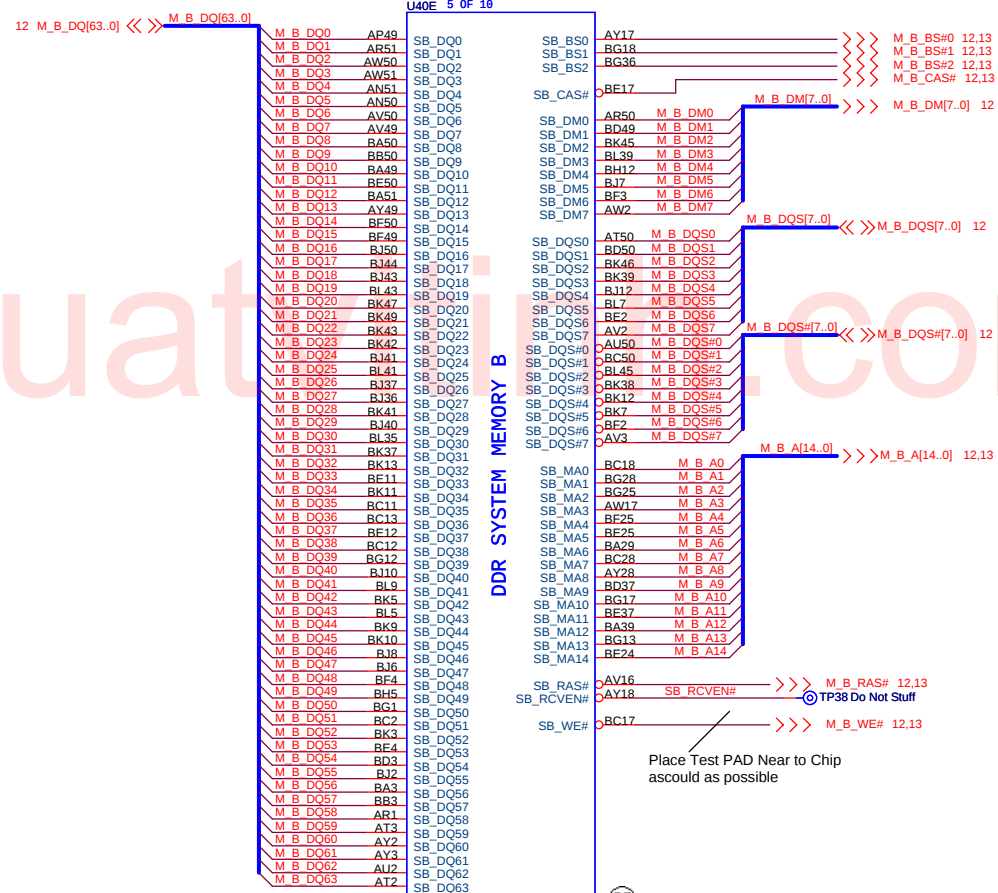
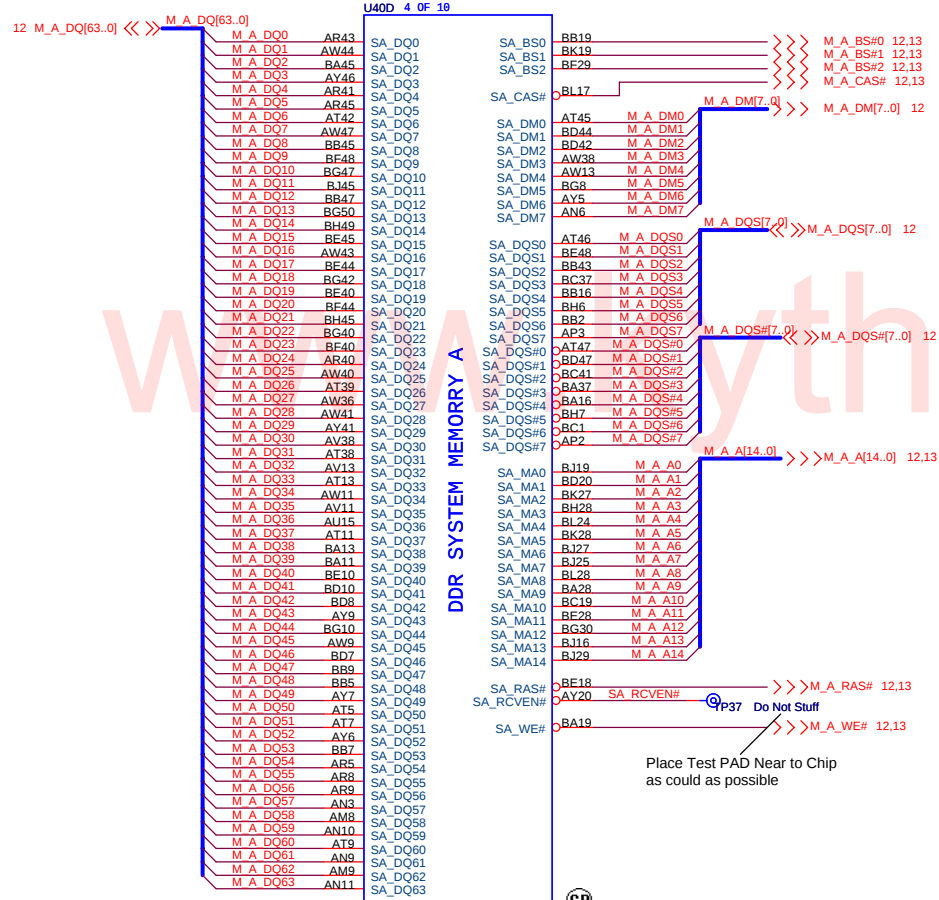
GMCH (1 of 6)

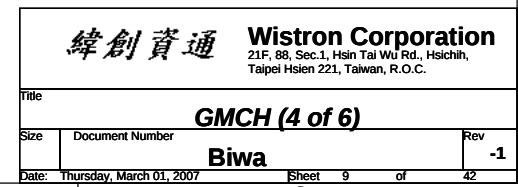
Rev

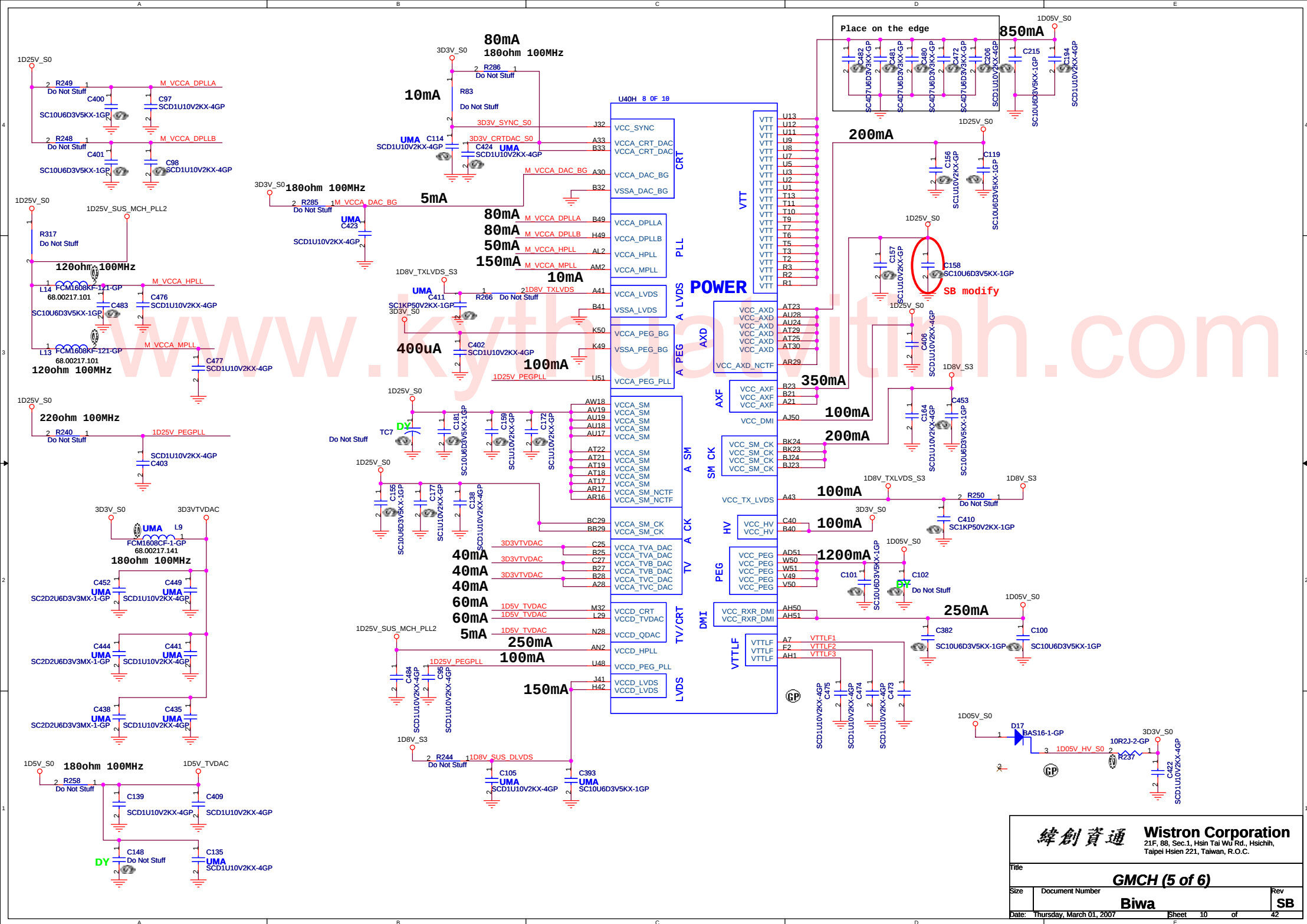
Biwa

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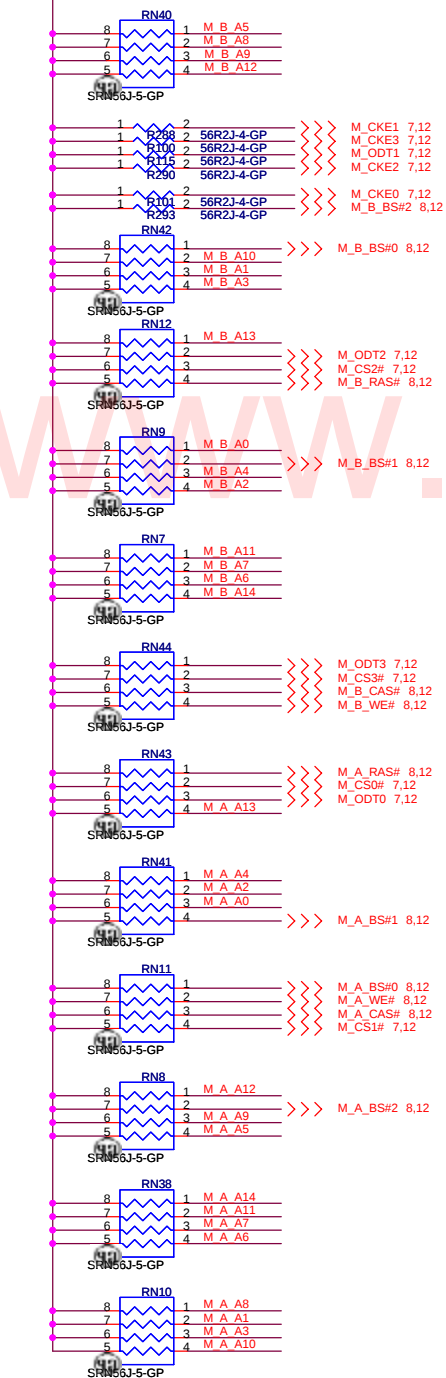






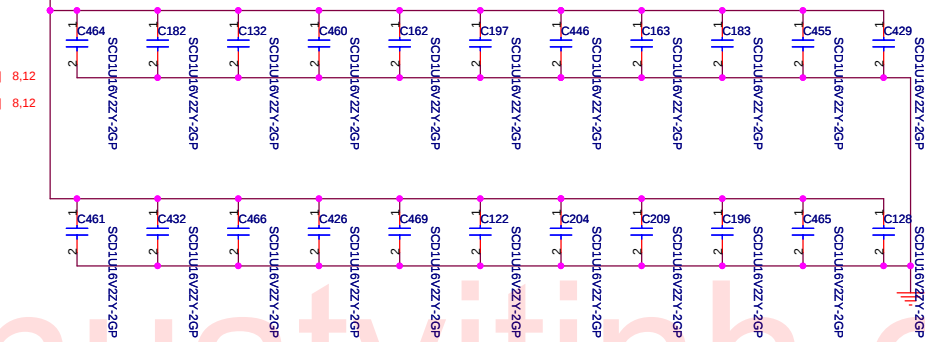
PARALLEL TERMINATION

DDR_VREF_S0 Put decap near power(0.9V) and pull-up resistor

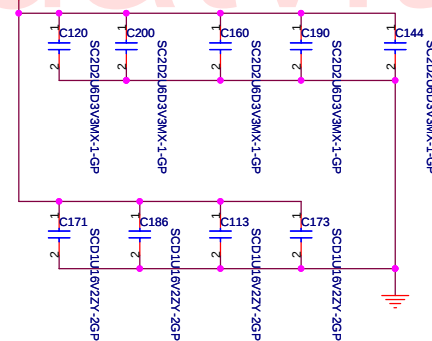


Decoupling Capacitor

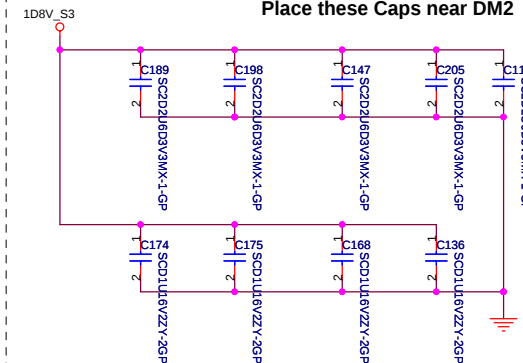
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



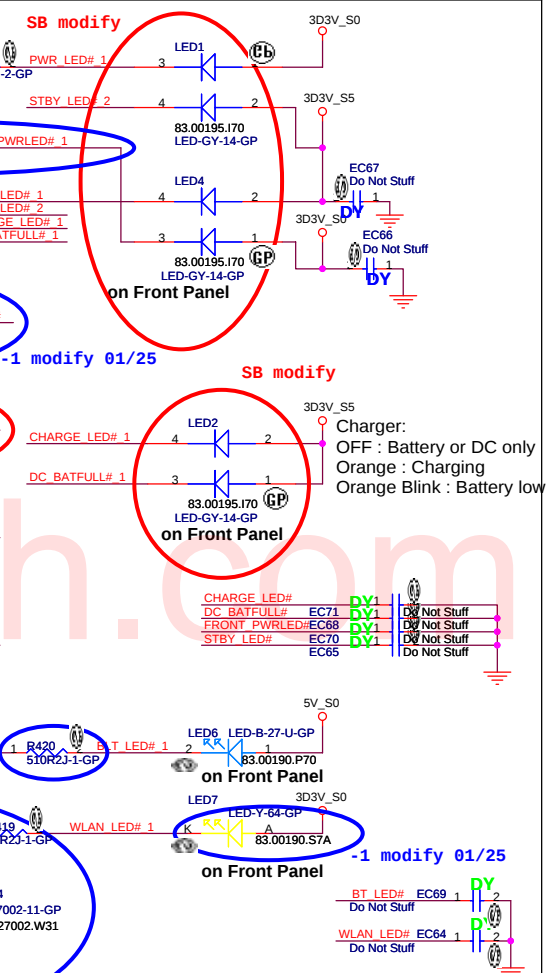
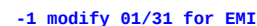
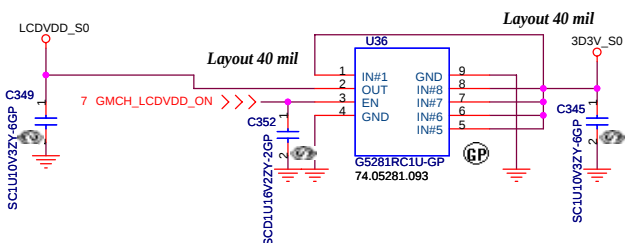
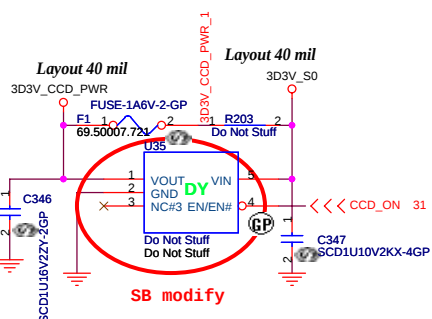
Place these Caps near DM2



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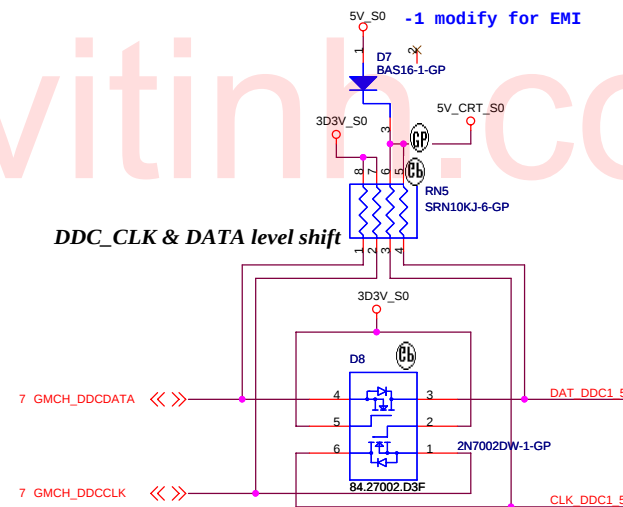
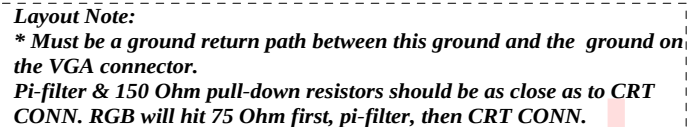
TOP VIEW

2 40
LCD
1 39

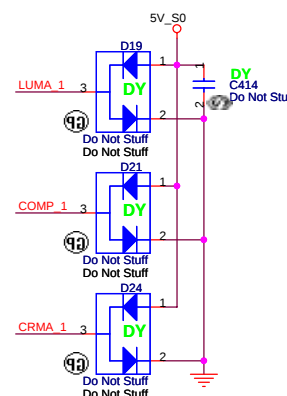
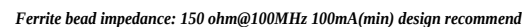
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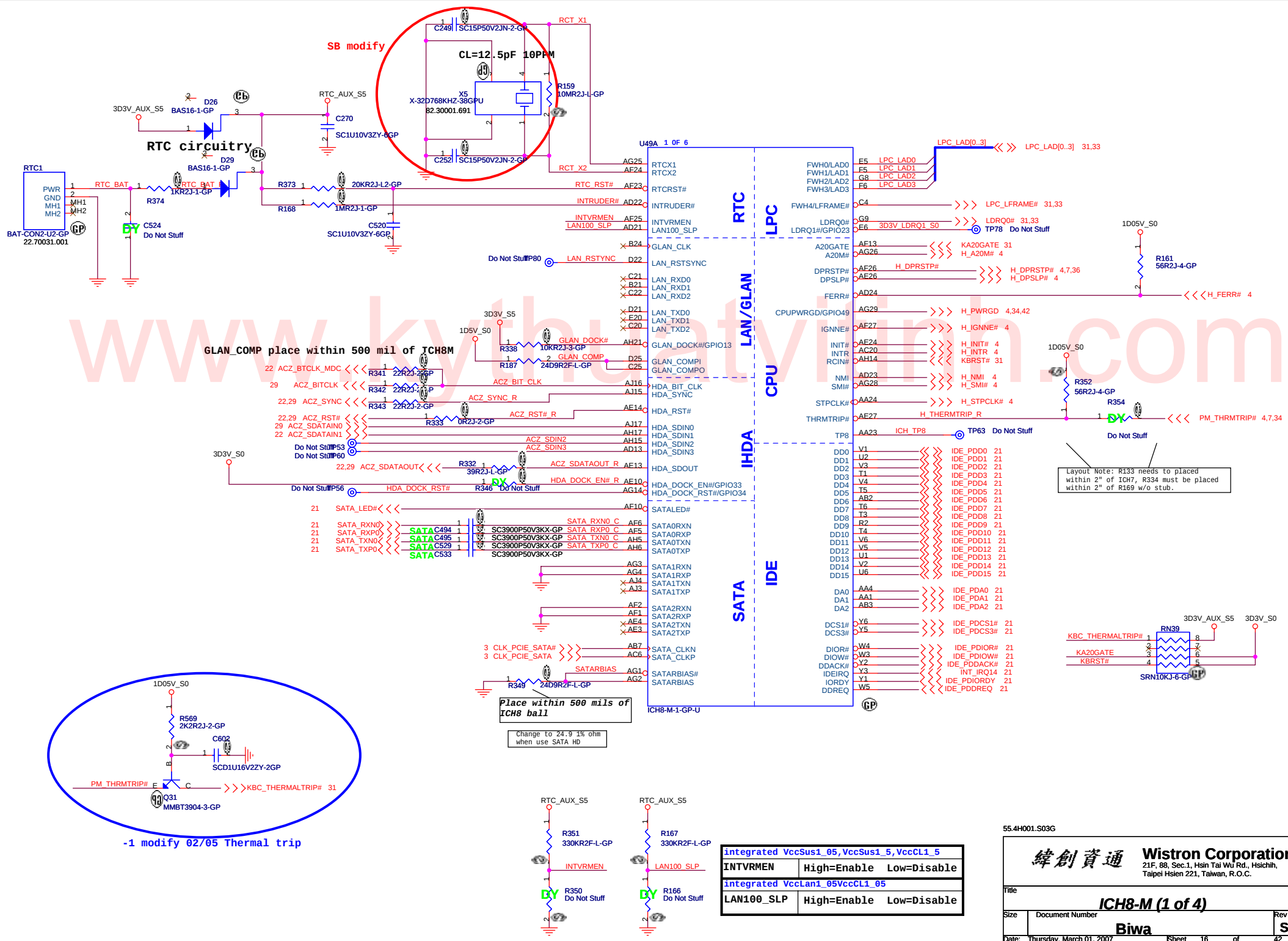
Title			
LCD CONN & LED			
Size	Document Number		Rev
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Diagram illustrating a vertical rectangle with numbers 11 through 15 on the left side and numbers 6 through 10 on the right side. The rectangle is outlined in black.

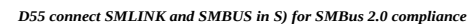


SB modify for SIV

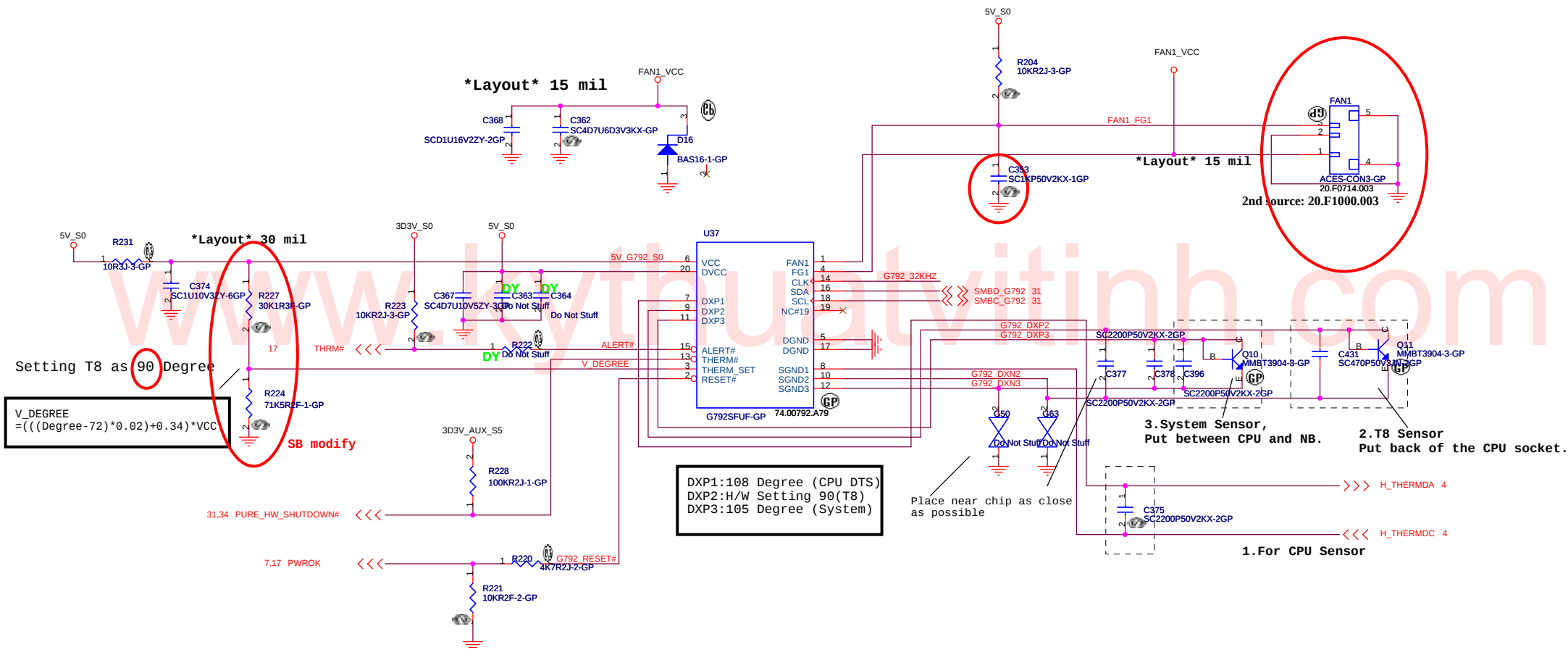




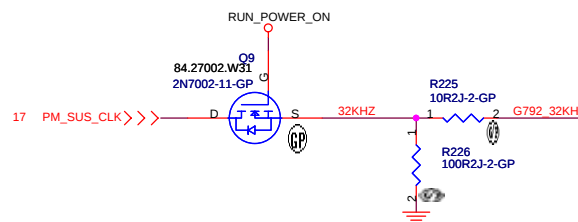




SMBUS



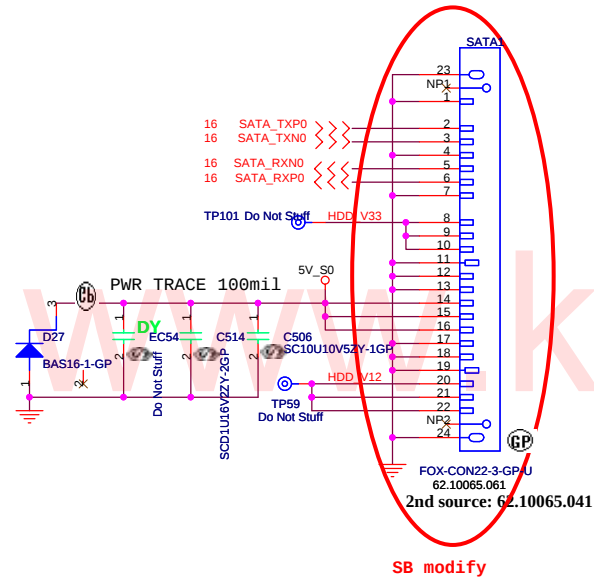
TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



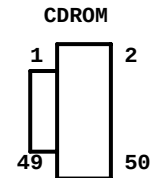
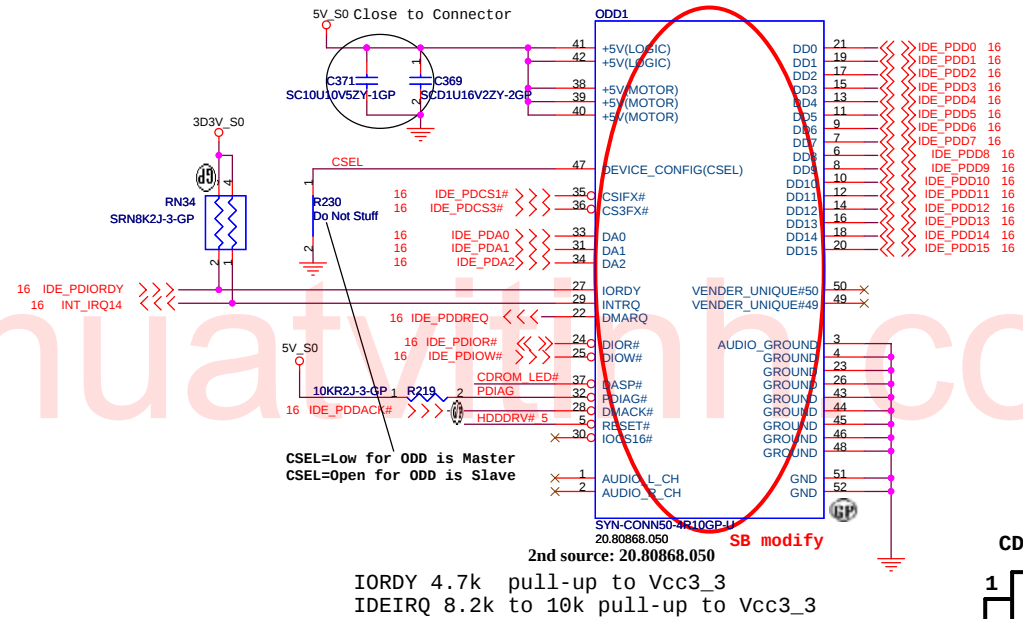
Biwa Thermal Table 1106

		T6	T7
Sensor 0	CPU DTS	100	102
Sensor 1	CPU G792 Analog	110	113
Sensor 2	System G792	85	87
Sensor 3	T8		
Sensor 4	ADIA status		

SATA Connector

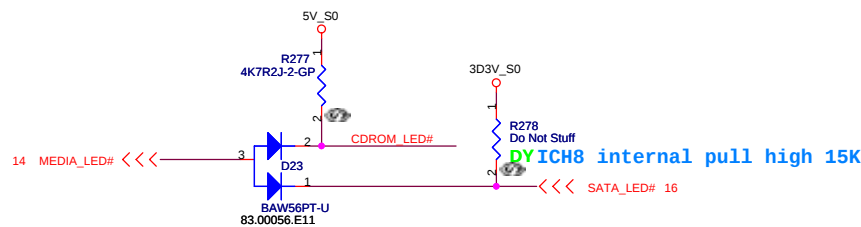
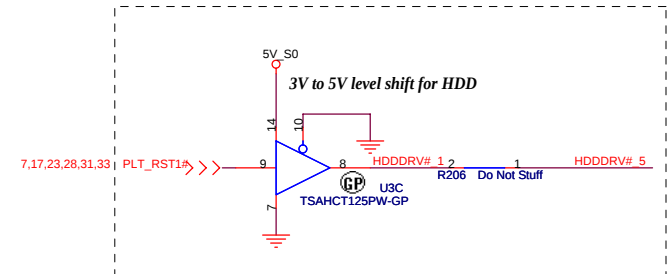


ODD Connector



2nd source: 20.80868.050

IORDY 4.7k pull-up to Vcc3_3
IDEIRQ 8.2k to 10k pull-up to Vcc3_3



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Title: **HDD and CDROM**
Size: Document Number: **Biwa** Rev: **SB**
Date: Thursday, March 01, 2007 Sheet 21 of 42

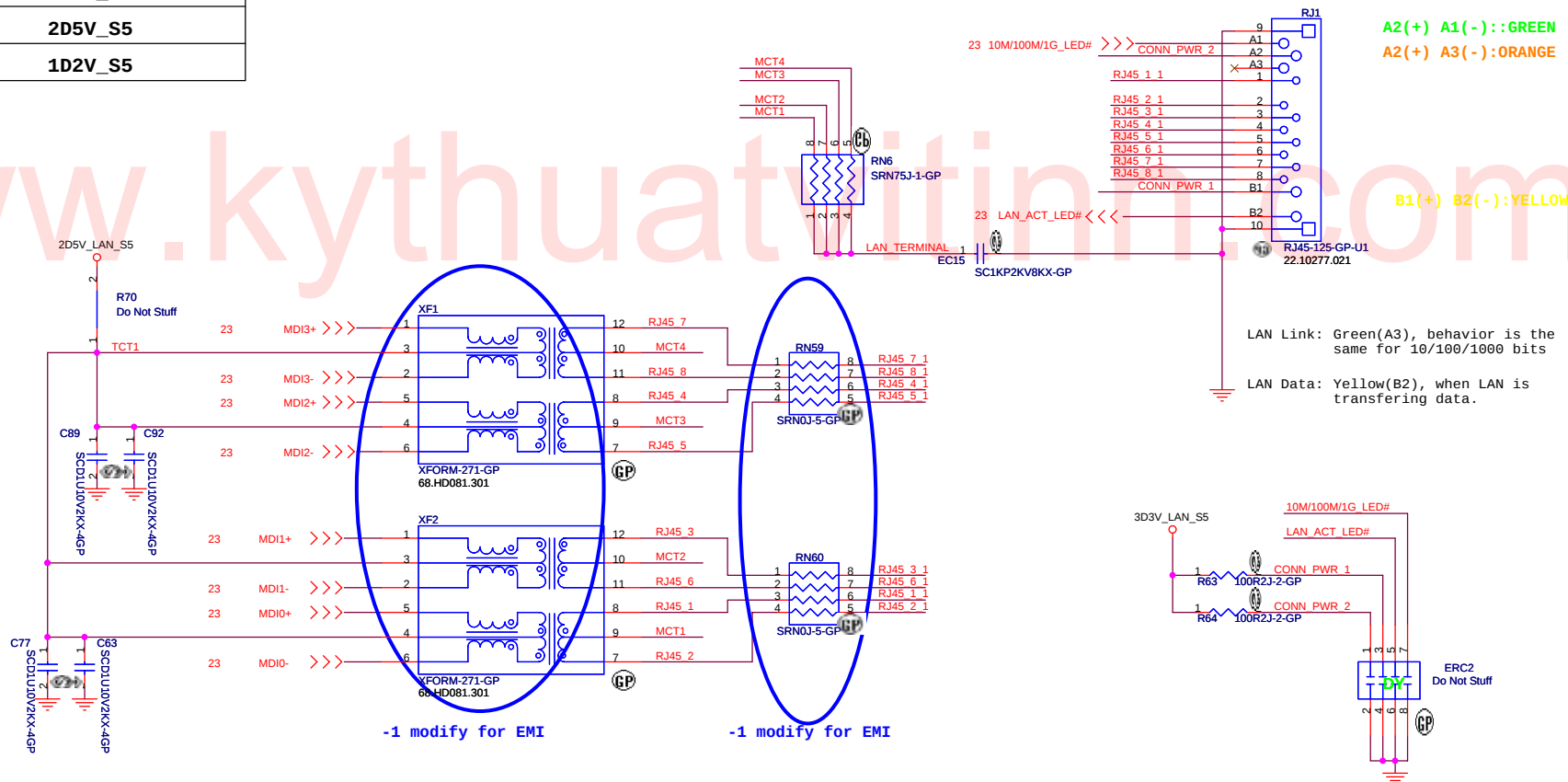
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector

LED COLOR

A2(+) A1(-)::GREEN
A2(+) A3(-):ORANGE

B1(+) B2(-):YELLOW



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

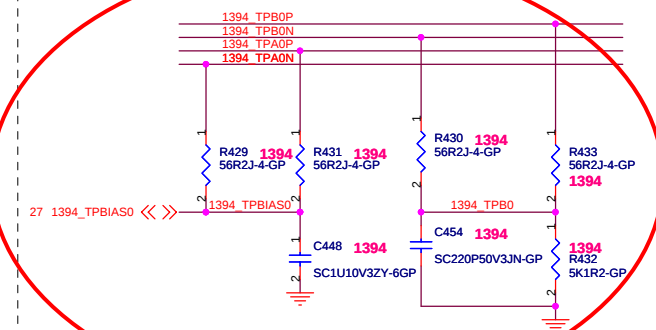
10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

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Title			
LAN Connector			
Size	Document Number		Rev
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CLOSE TO CHIP



TI PCI7412

IDSEL: AD22
INTA-->: INT_PIRQG#
INTB-->: INT_PIRQB#
INTC-->: INT_PIRQF#
INTD-->: INT_PIRQG#
GNT: PCI_GNT#0
REQ: PCI_REQ#0

INTA# CARBUS 1 (INT_PIRQG#)
INTB# 1394 (INT_PIRQB#)
INTC# Flash Media (INT_PIRQF#)
INTD# SD Host (INT_PIRQG#) share

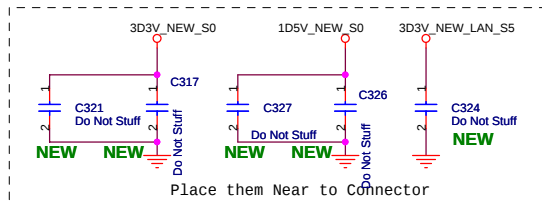
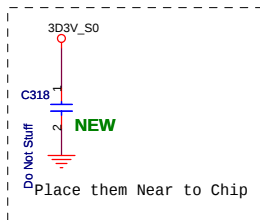
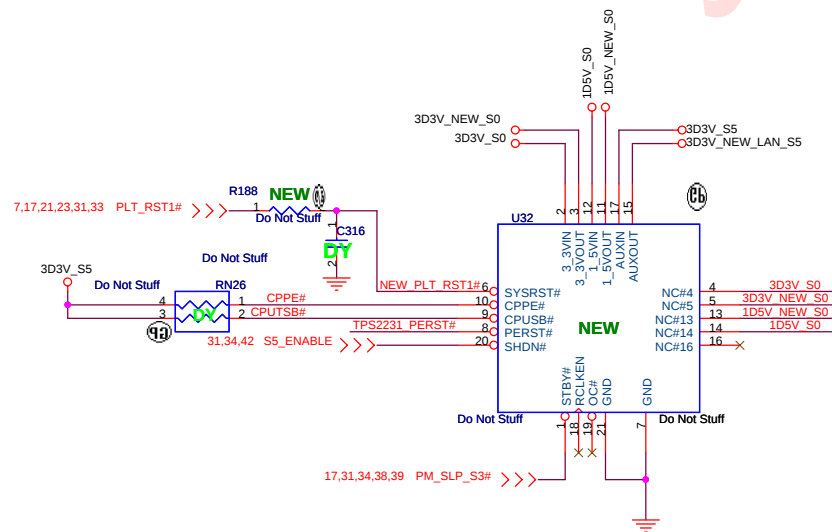
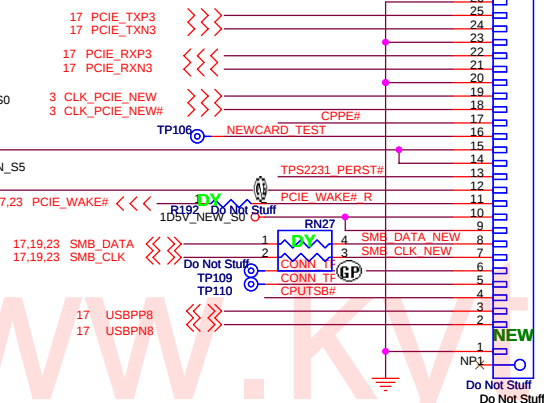
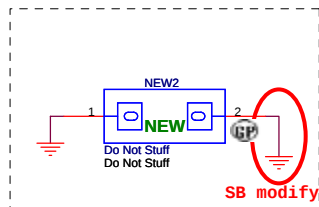
MFUNC4: use bit 19-16 Register define.

55.4H001.S03G

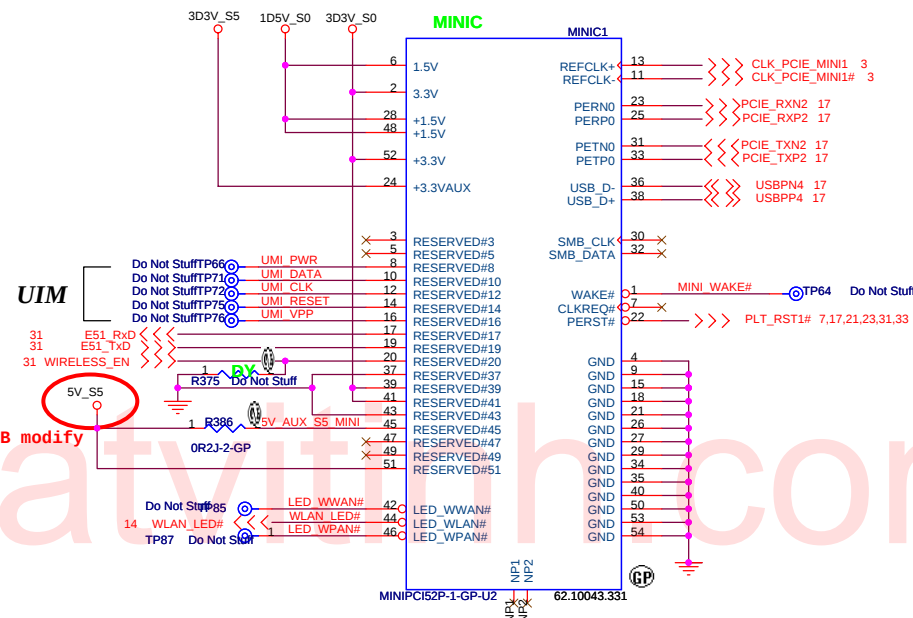
緯創資通 Wistron Corporation
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NEWCARD Connector

Reserve the symbol
for bottom side
connector

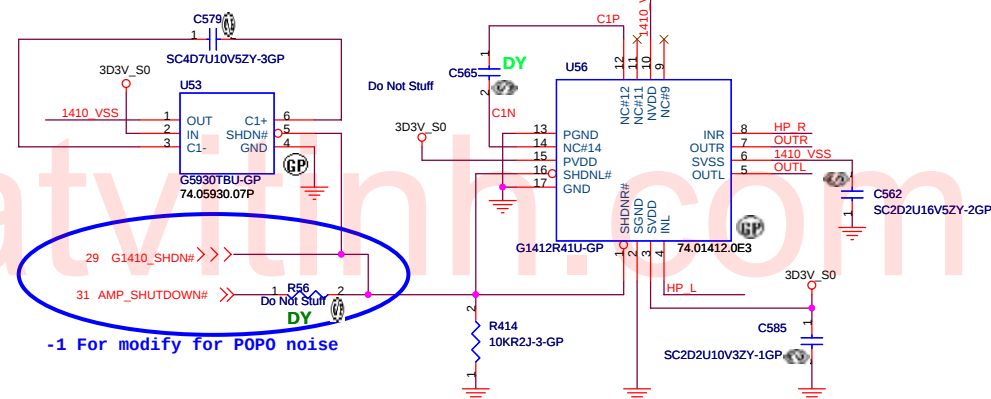
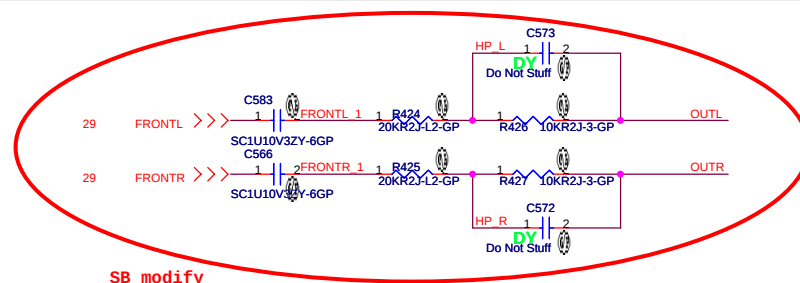
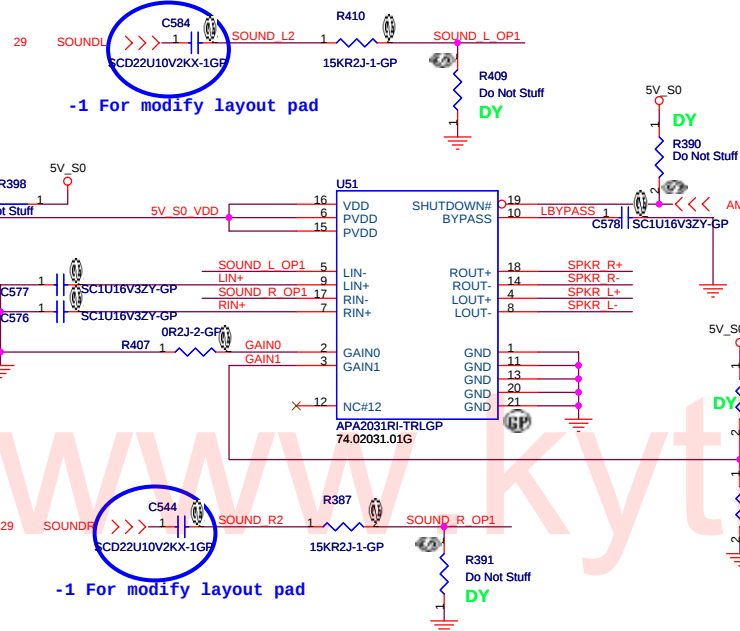


Mini Card Connector

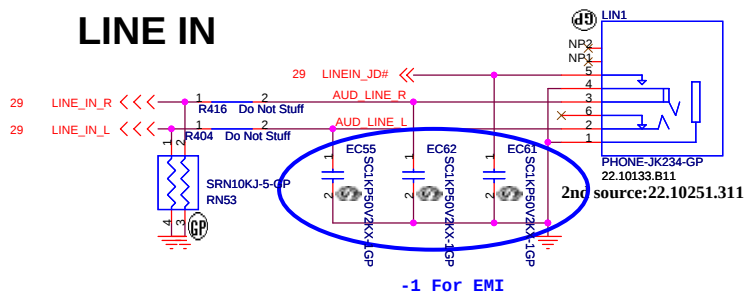


AUDIO OP AMPLIFIER

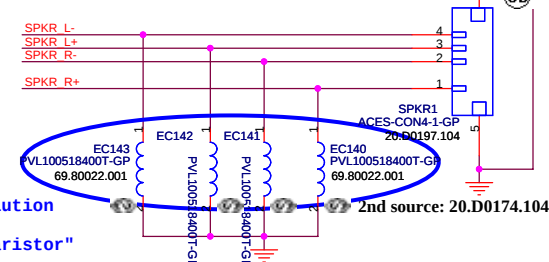
I/P signal level
need +5V level



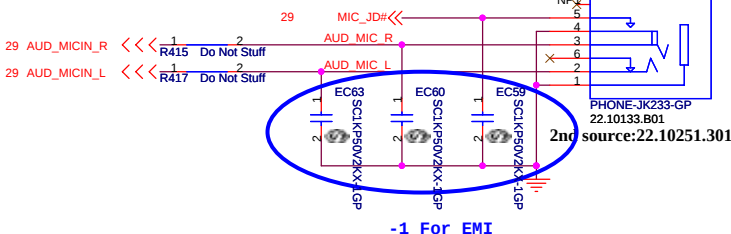
LINE IN



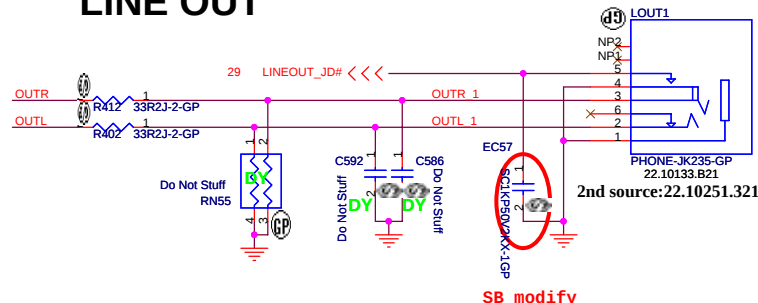
Internal Speaker



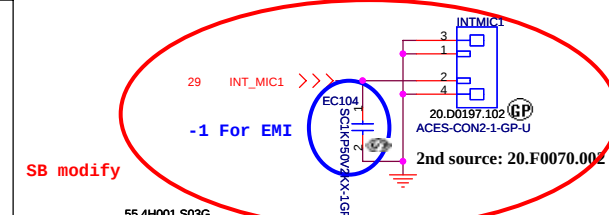
MIC IN



LINE OUT



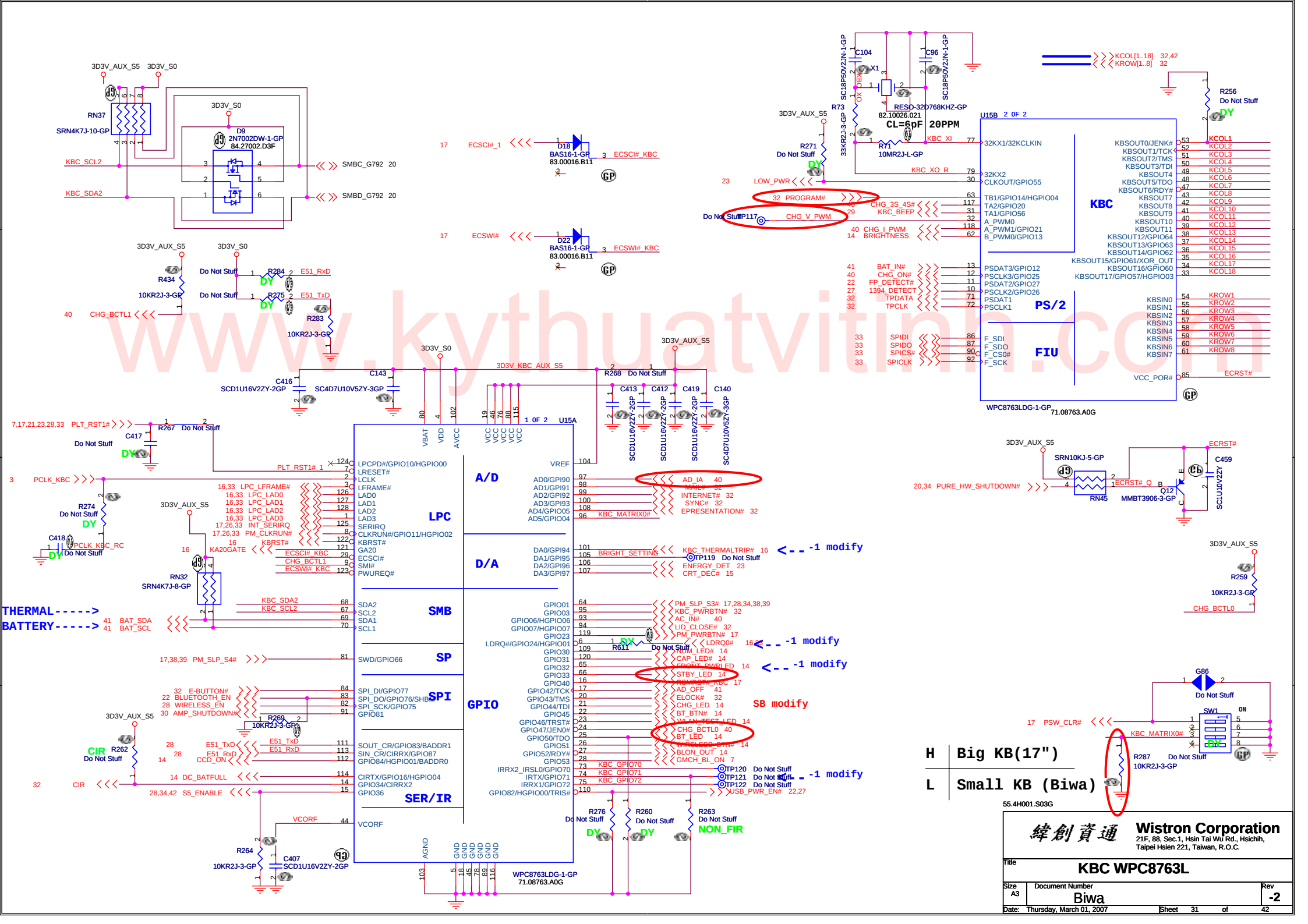
Internal Microphone



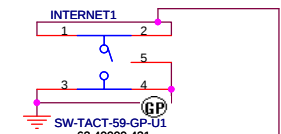
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Taipei Hsien 221, Taiwan, R.O.C.

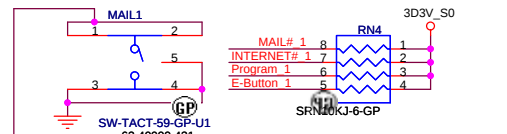
Title			AUDIO AMP AND JACK	
Size	A3	Document Number	Biwa	
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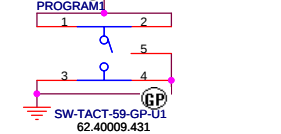
Internet Button



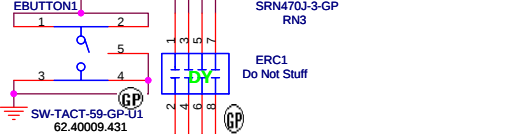
Mail Button



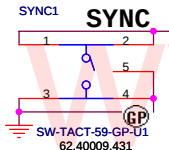
Program Button



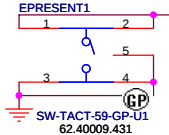
E-Button



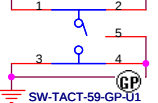
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EPRESENTATION

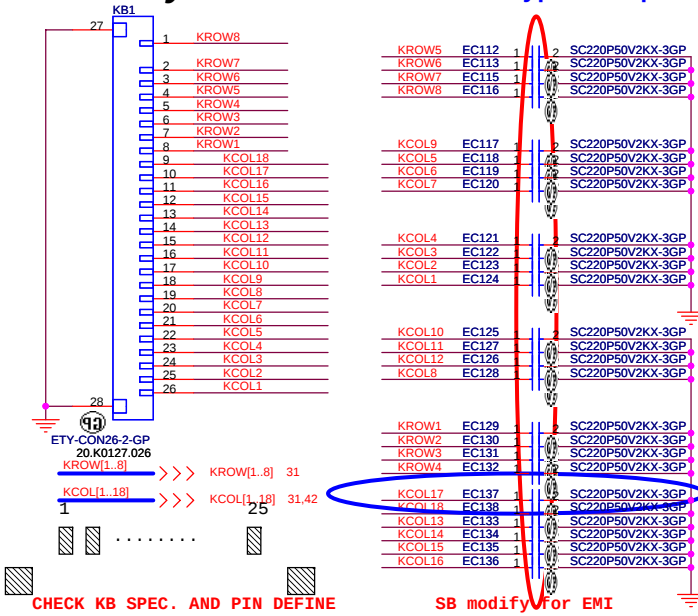


ELOCK



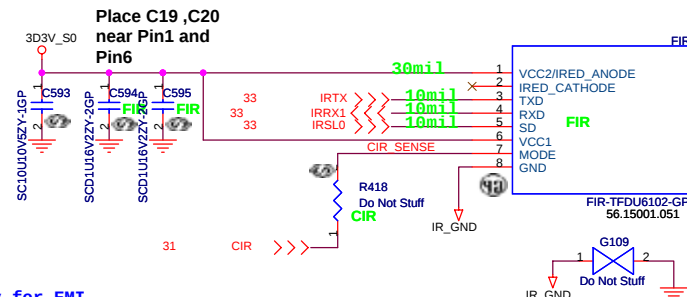
Internal KeyBoard CONN

EMI Bypass cap.



VISHAY FIR Module

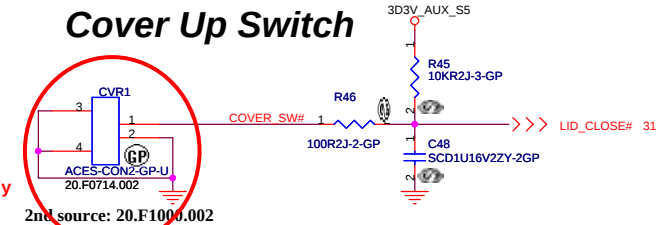
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close
to U32



Cover Up Switch

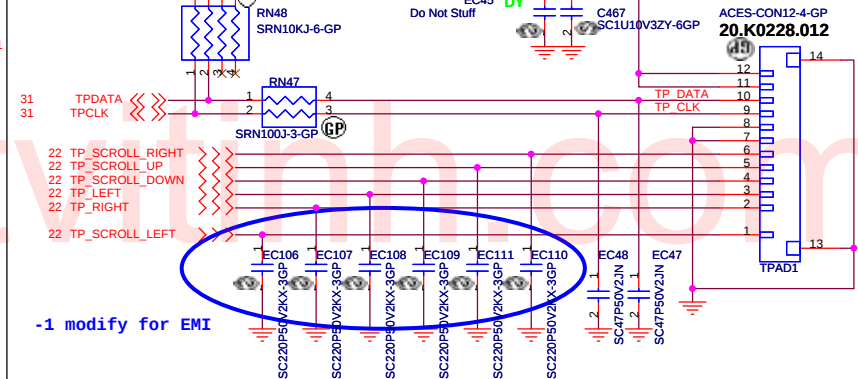
SB modify

2nd source: 20.F1000.002



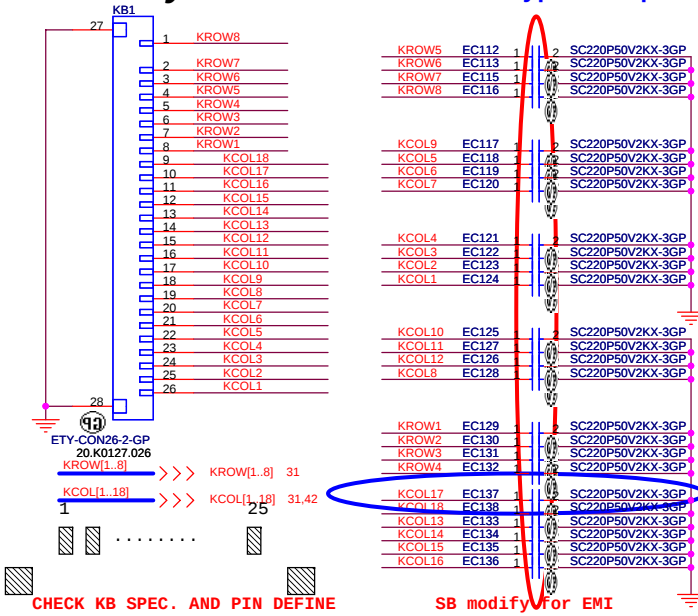
TOUCH PAD

2nd source: 20.K0227.012



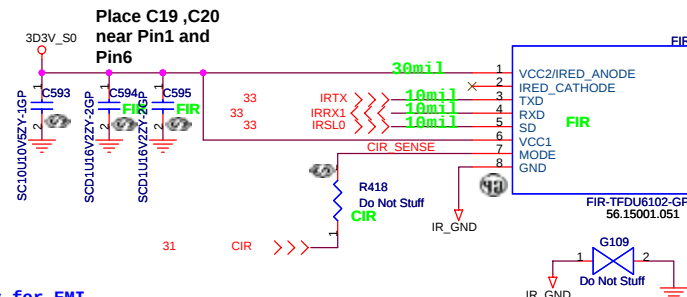
Internal KeyBoard CONN

EMI Bypass cap.



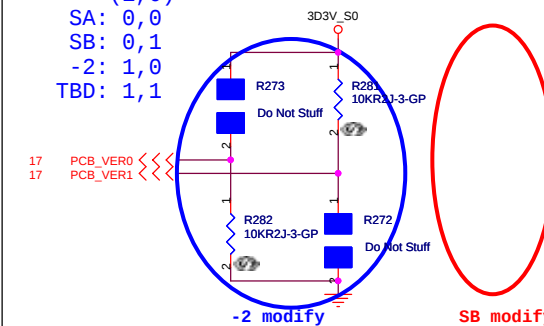
VISHAY FIR Module

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close
to U32



PlanarID

(1,0)
SA: 0,0
SB: 0,1
-2: 1,0
TBD: 1,1

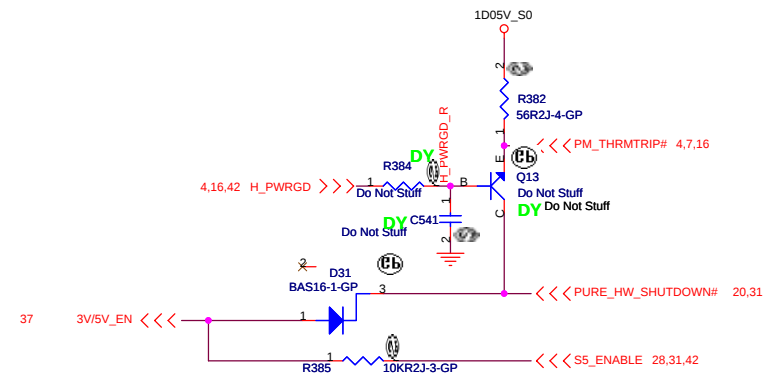


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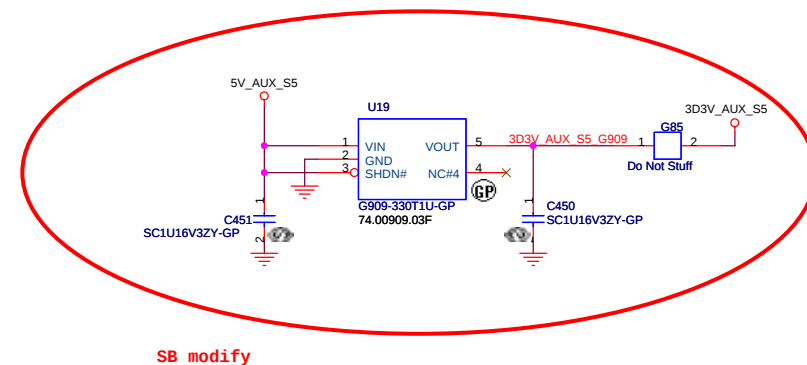
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **BUTTONS / KB / TOUCHPAD / FIR**
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Aux Power 3D3V_AUX_S5



SB modify

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Taipei Hsien 221, Taiwan, R.O.C.

Title	<i>RUN POWER and 3D3V AUX S5</i>
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Size	Document Number
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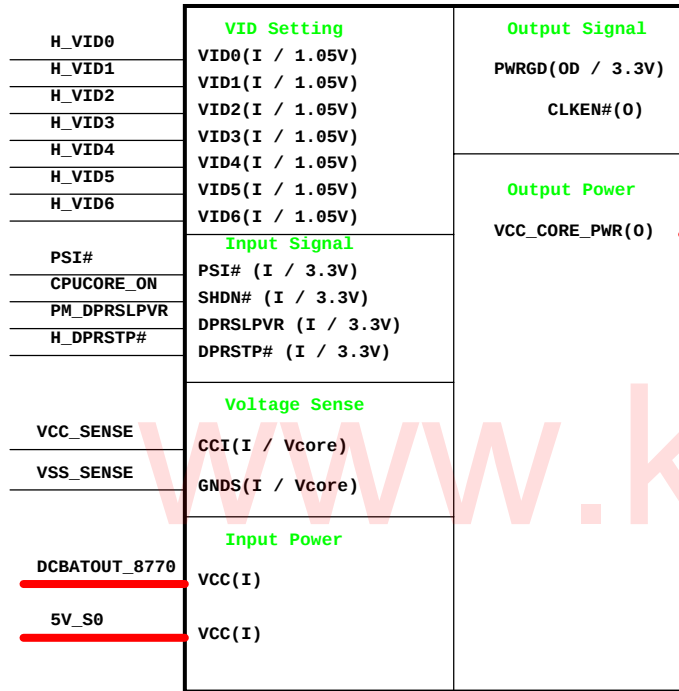
Biwa

Date: Thursday, March 01, 2007

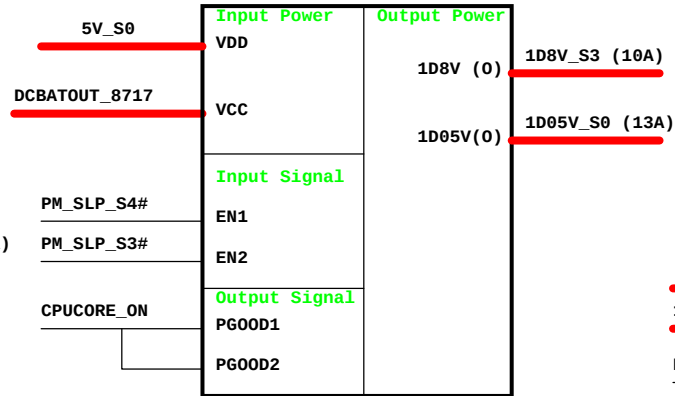
Sheet 34 of 42

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CPU_CORE
MAXIM MAX8770



MAX8717
1D8V/1D05V

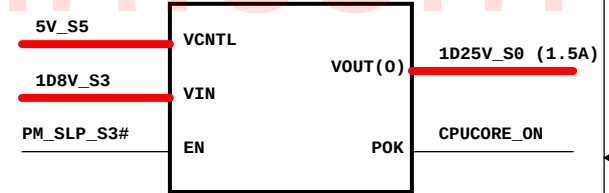


0D9V_S0



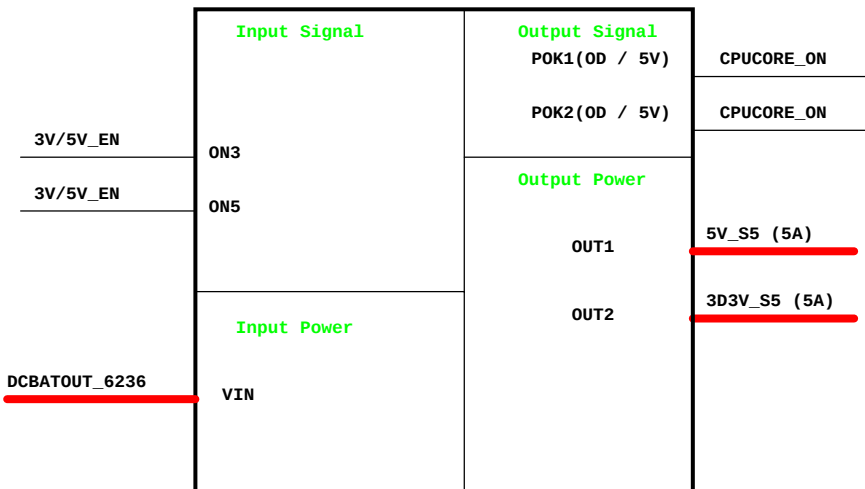
TPS51100

1D25V_S0

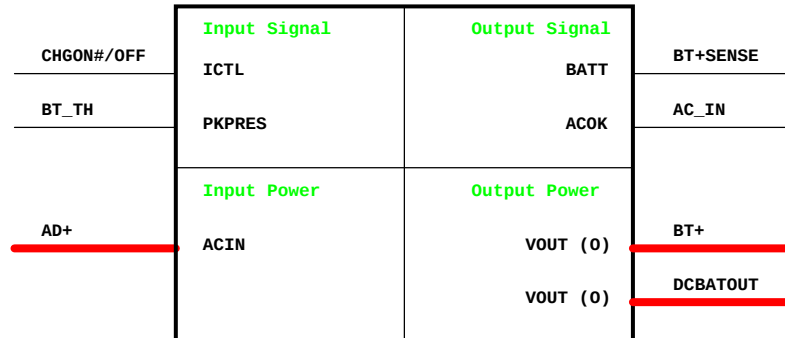


APL5915

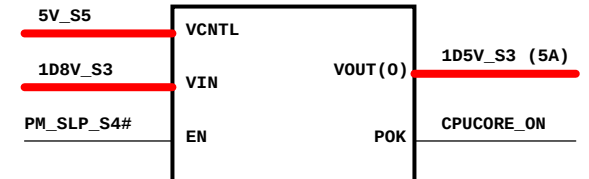
ISL6236
5V/3D3V



Charger ISL6255

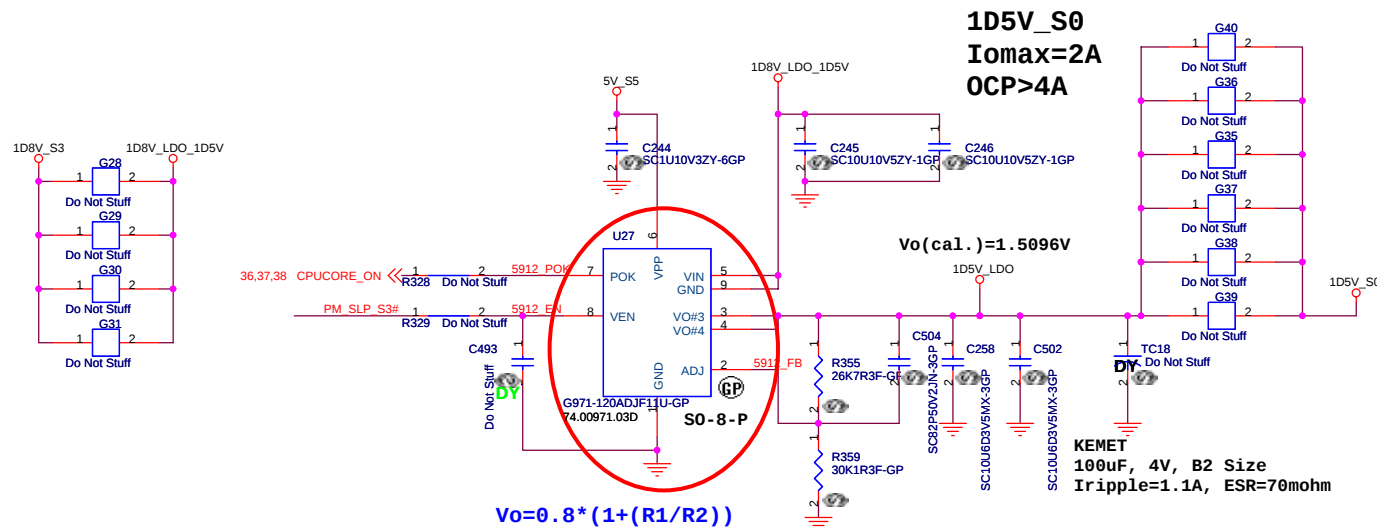
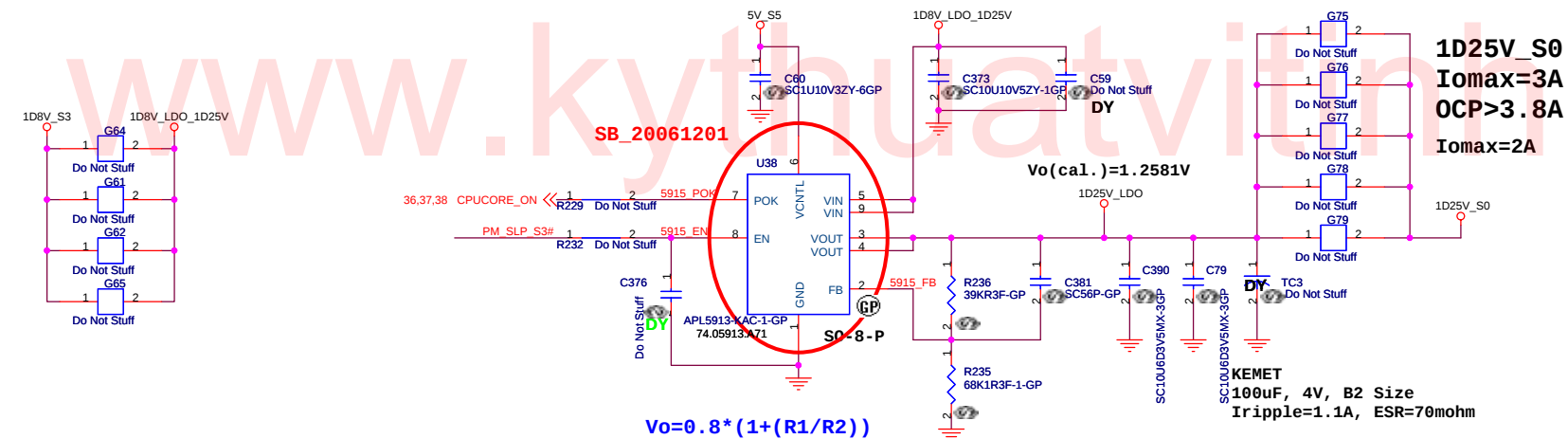
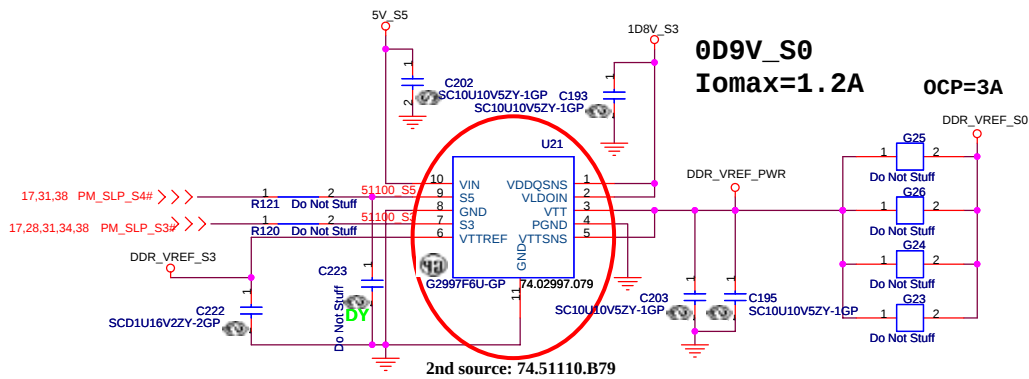


1D5V_S3



APL5912

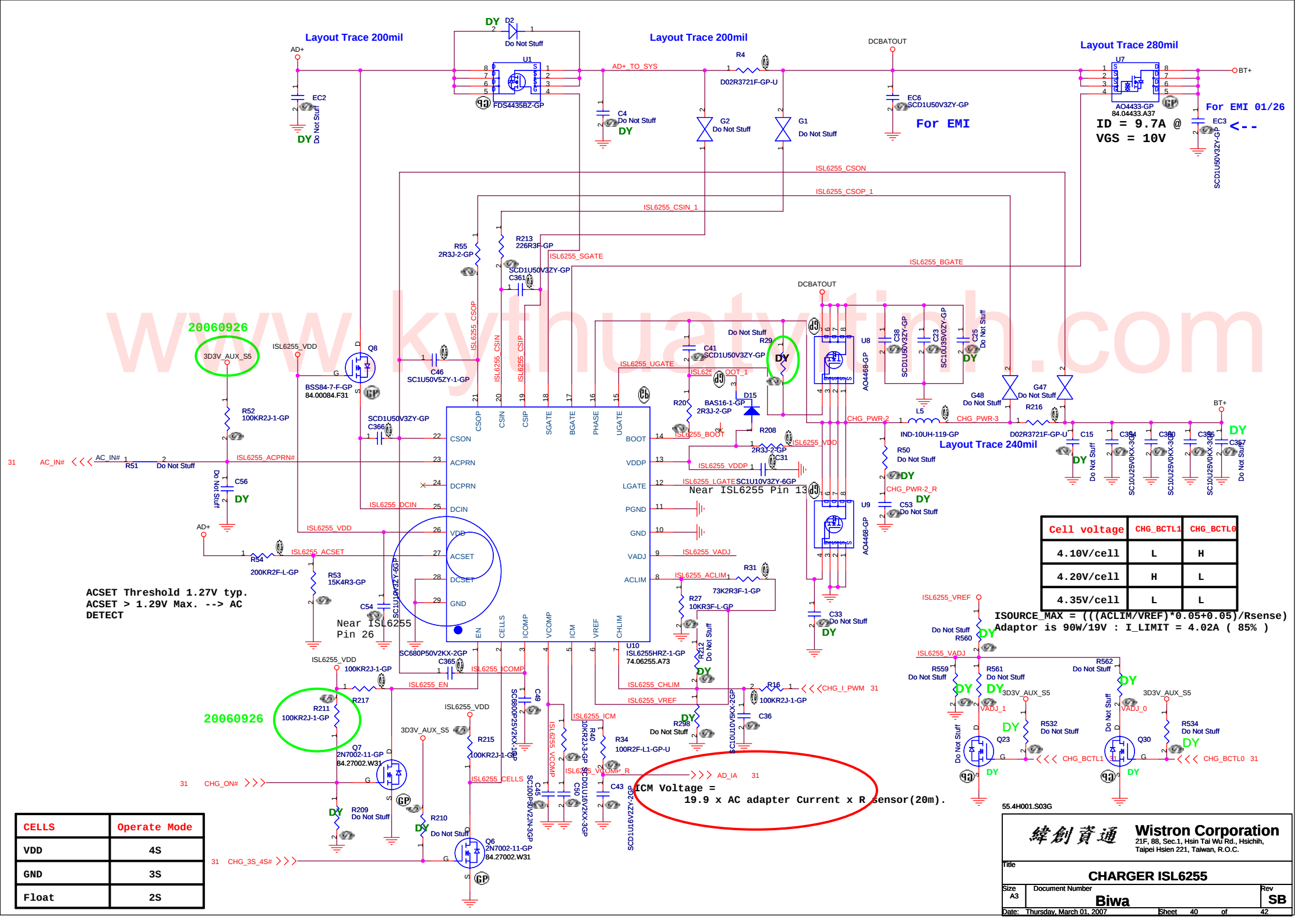
55.4H001.S03G



55.4H001.S03G

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1D25V/1D5V/0D9V		
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20060926

20060926

ACSET Threshold 1.27V typ.
ACSET > 1.29V Max. --> AC
DETECT

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Cell voltage	CHG_BCTL1	CHG_BCTL0
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 90W/19V : I_LIMIT = 4.02A (85%)

ICM Voltage =
19.9 x AC adapter Current x R sensor (20m).

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Title

CHARGER ISL6255

Size

A3

Document Number

Biwa

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Sheet

40

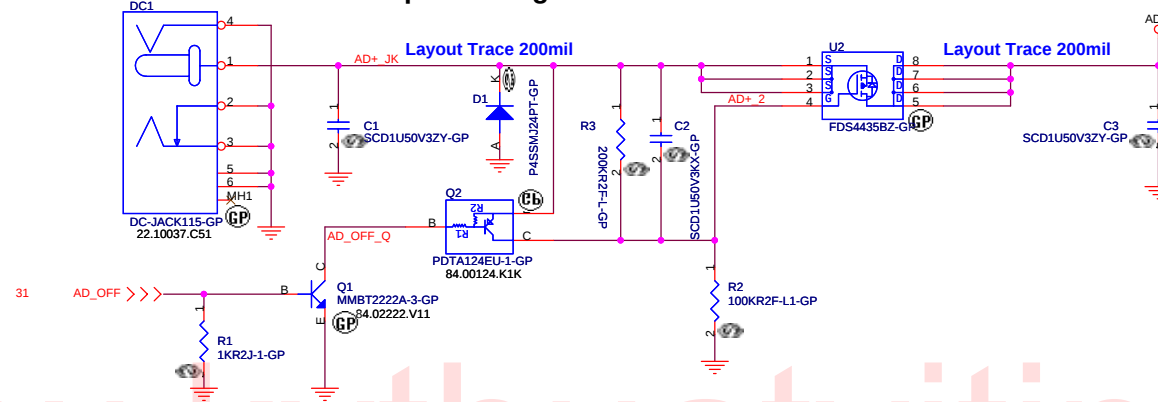
of

42

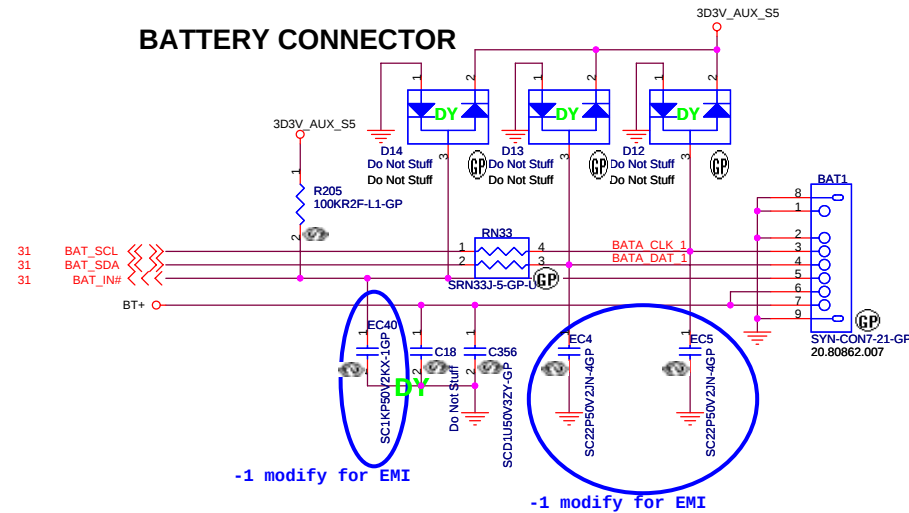
Rev

SB

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

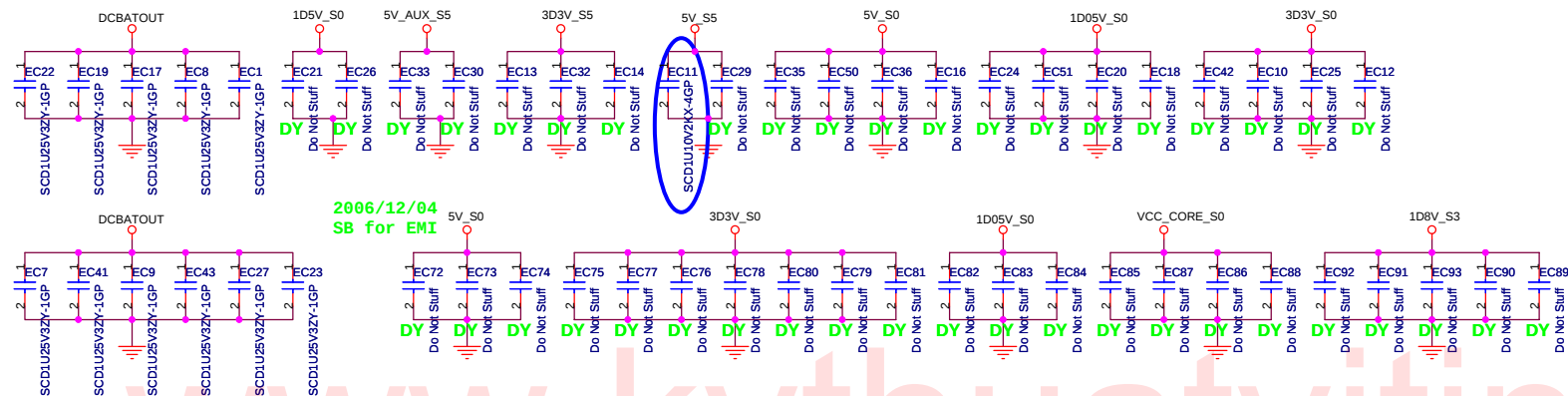


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Title		
AD/BATT CONN		
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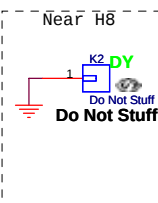
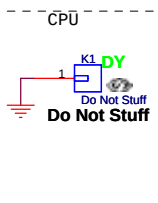
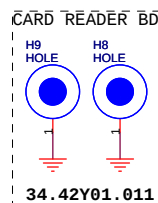
EMI Capacitor



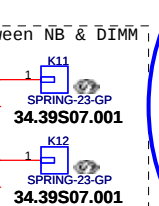
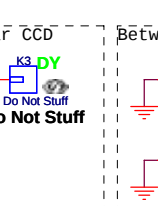
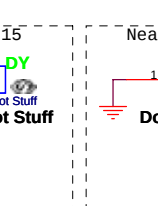
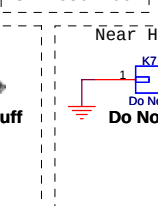
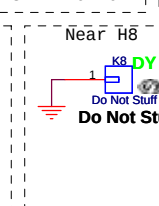
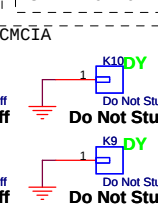
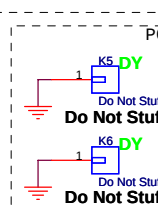
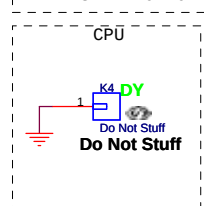
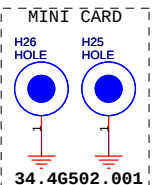
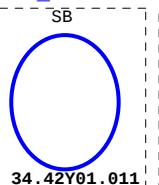
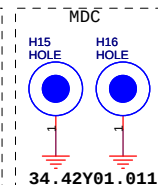
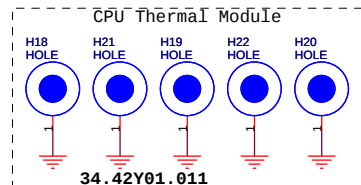
2006/12/04
SB for EMI

TOP

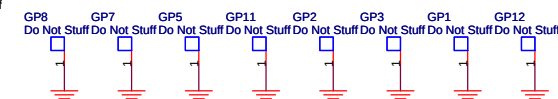
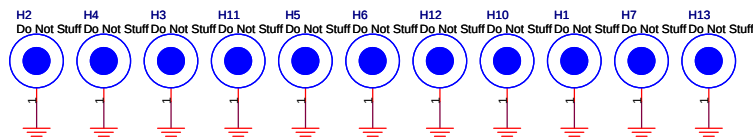
BOTTOM



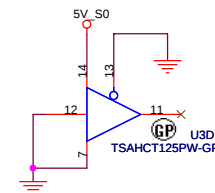
-1_0131 for thermal



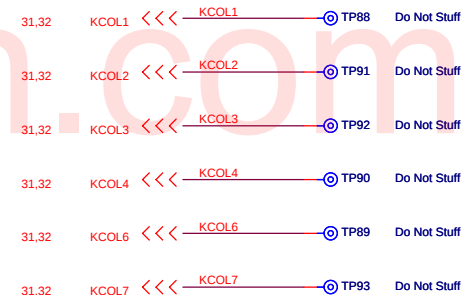
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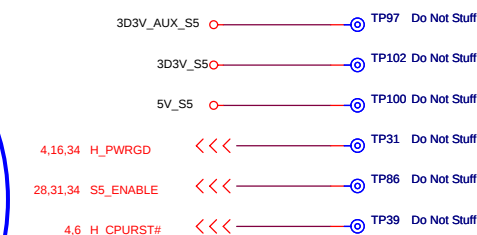
Unused gate



KBC JTAG Test Pad



DFX Test Point



Test Point 放在 Dimm Door 打開可量測處

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Title			EMI/Spring/Boss
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