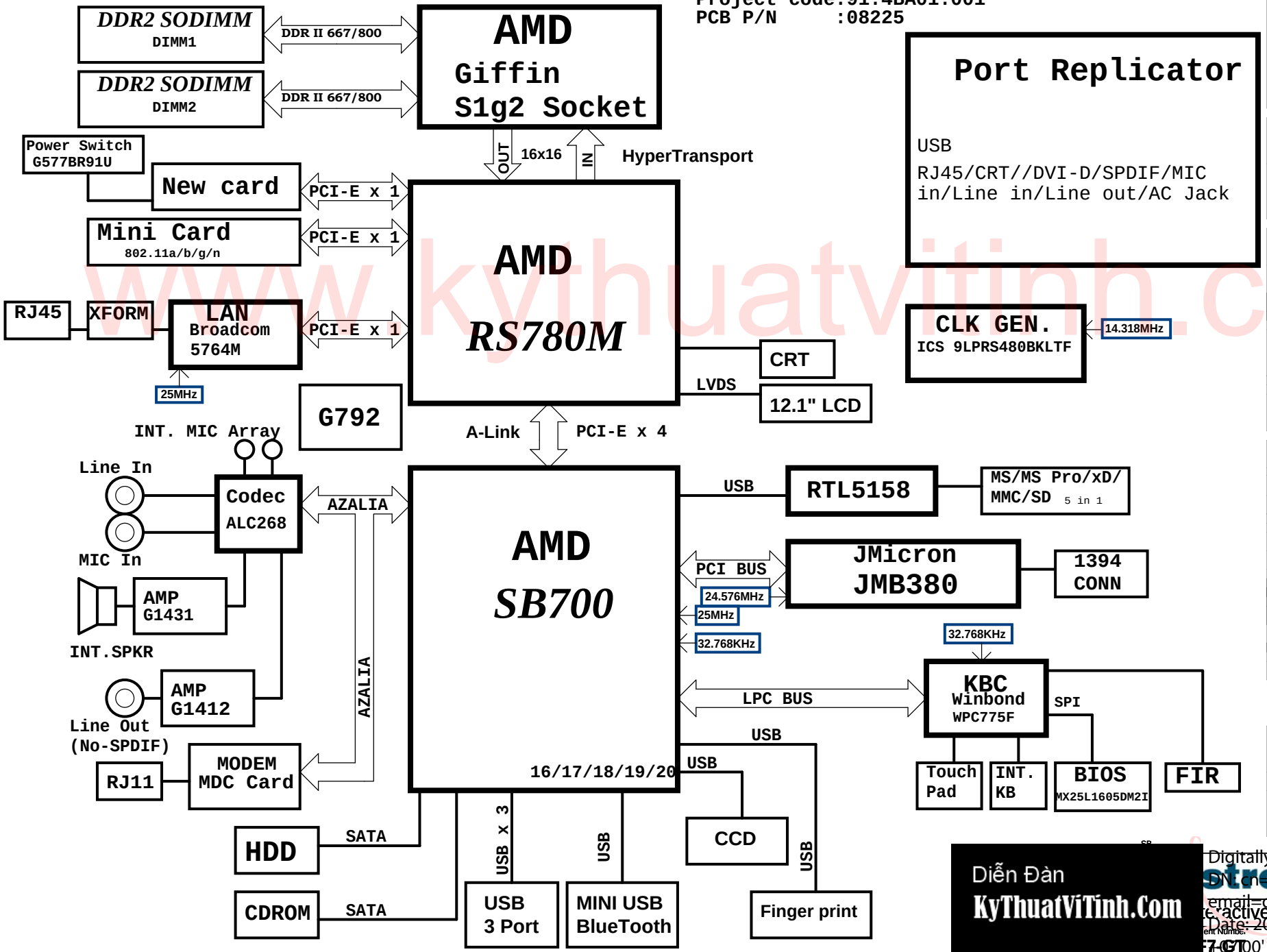
Ferrari 7 GT Block Diagram

2008/09/01

Project code:91.4BA01.001
PCB P/N :08225



PCB Layer Stackup

- L1: Component
- L2: GND
- L3: Signal
- L4: VCC
- L5: GND
- L6: Signal
- L7: GND
- L8: Component

CPU V_CORE — ISL6265HR — 37

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC — TPS51124 — 38

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D1V_S0

TPS51120 — 40

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

TPS51117 — 39

INPUT	OUTPUT
DCBATOUT	1D8V_S3

SYSTEM LDO — G2997 — 41

INPUT	OUTPUT
1D8V_S3	0D9V_S3

G9161

INPUT	OUTPUT
3D3V_S5	1D2V_S5

G9166

INPUT	OUTPUT
3D3V_S0	2D5V_S0

G957

INPUT	OUTPUT
3D3V_S0	1D5V_S0

Battery Charger — MAX8371 — 43

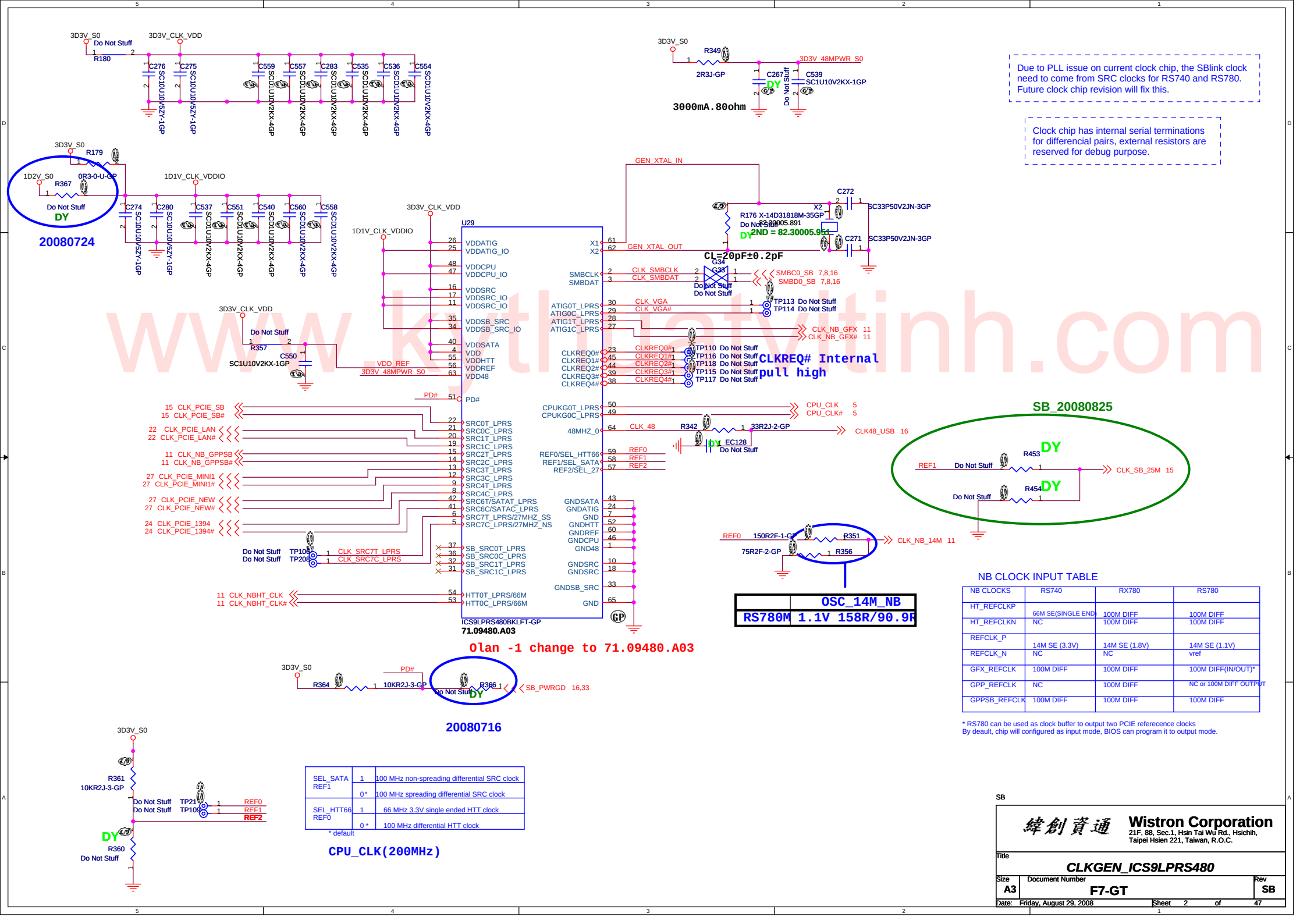
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Interactive Circuit Map

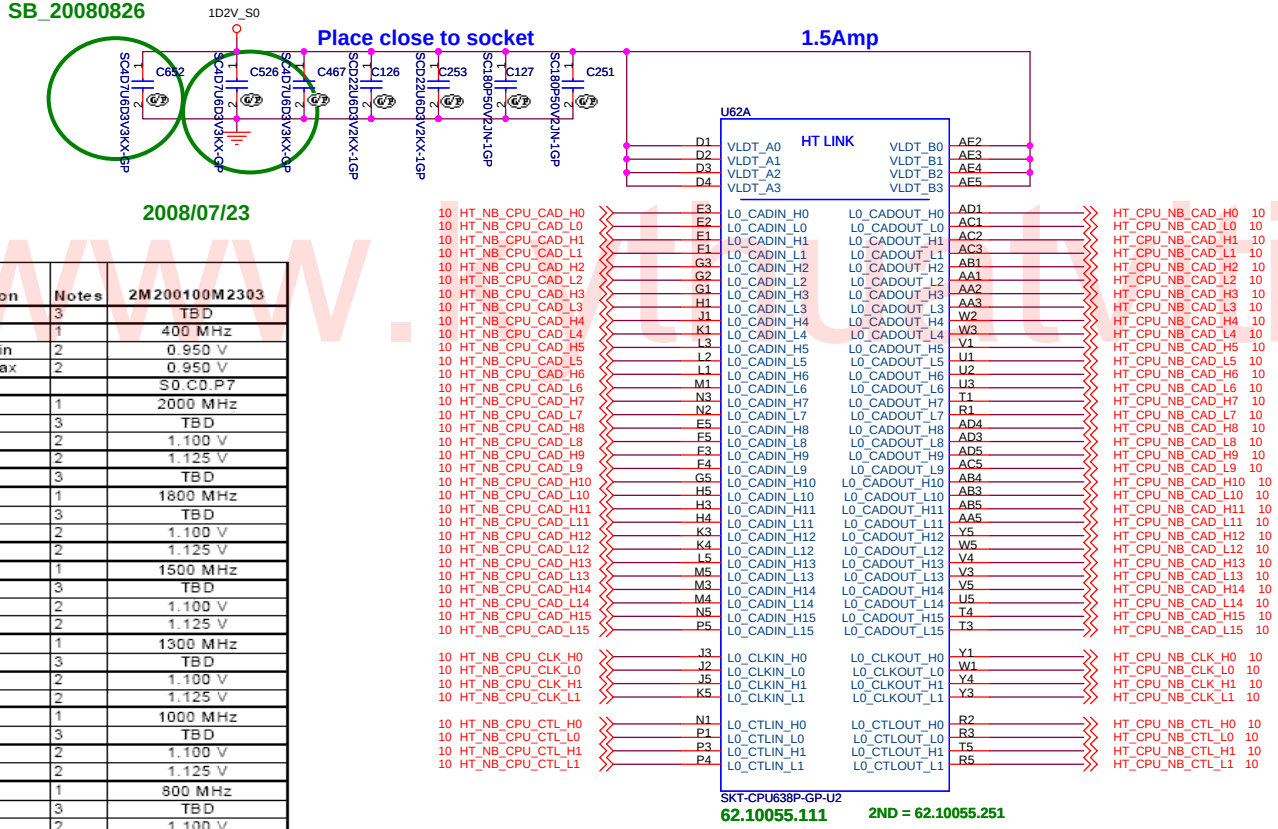
Size: C — Document Number: 7-GT00' — Rev: SB

Monday, September 01, 2008 — Sheet 1 of 47


Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
3000mA.80ohm
CL=20pF±0.2pF
2ND = 82.30005.951
82.30005.891
20080724
20080716
SB_20080825
CLKREQ# Internal pull high
ICS9LPRS480BKLFT-GP
71.09480.A03
Olan -1 change to 71.09480.A03
OSC_14M_NB
RS780M 1.1V 158R/90.9R
CPU_CLK(200MHz)
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
SEL_SATA REFI1 | 1 | 100 MHz non-spreading differential SRC clock
0* | 100 MHz spreading differential SRC clock
SEL_HTT66 REF0 | 1 | 66 MHz 3.3V single ended HTT clock
0 * | 100 MHz differential HTT clock
* default
SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CLKGEN_ICS9LPRS480
Size A3
Document Number F7-GT
Rev SB
Date: Friday, August 29, 2008
Sheet 2 of 47

SB_20080826

2008/07/23



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

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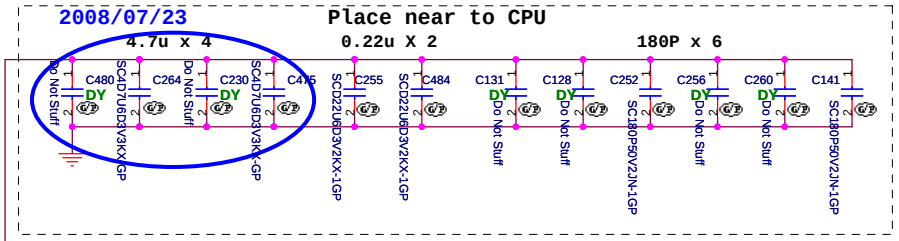
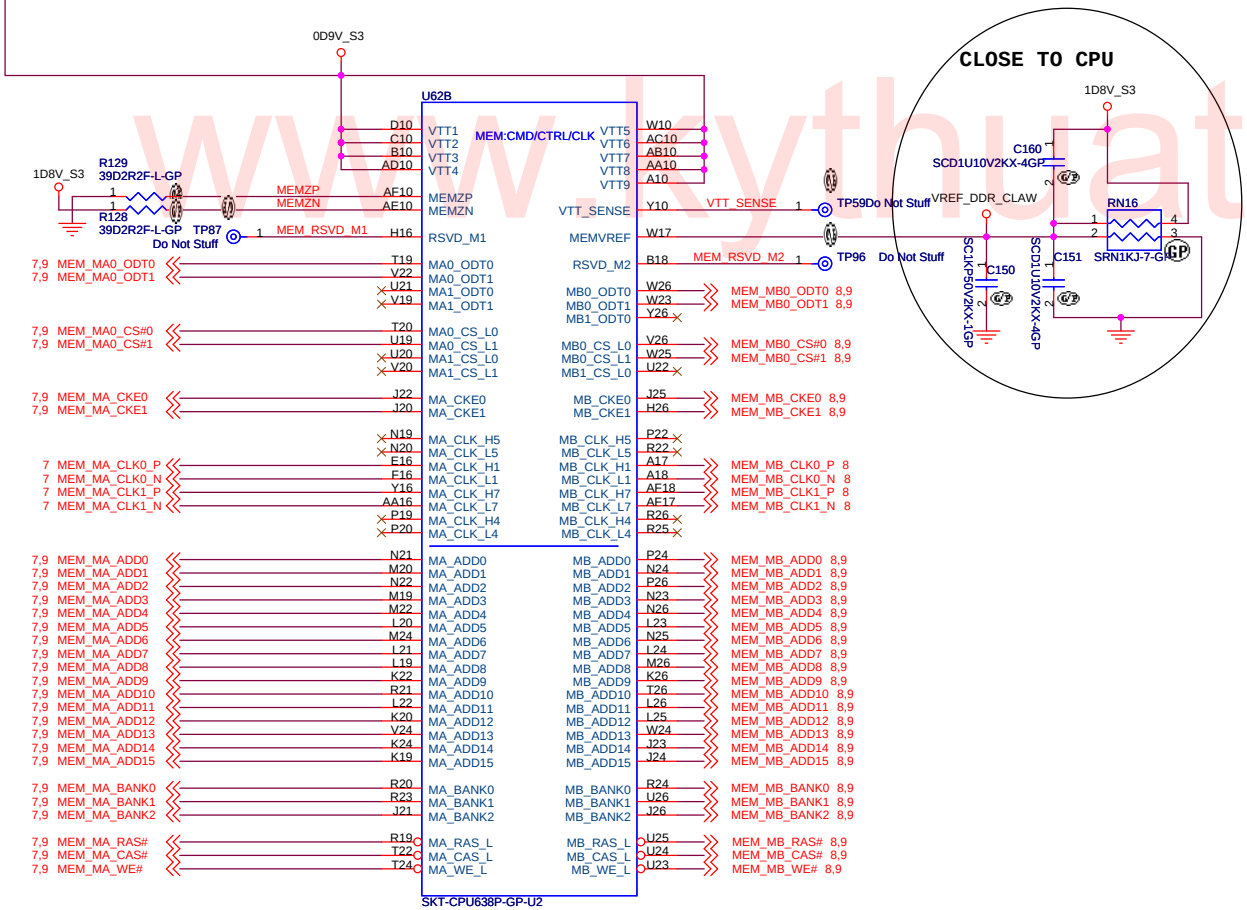
Taipei Hsien 221, Taiwan, R.O.C.

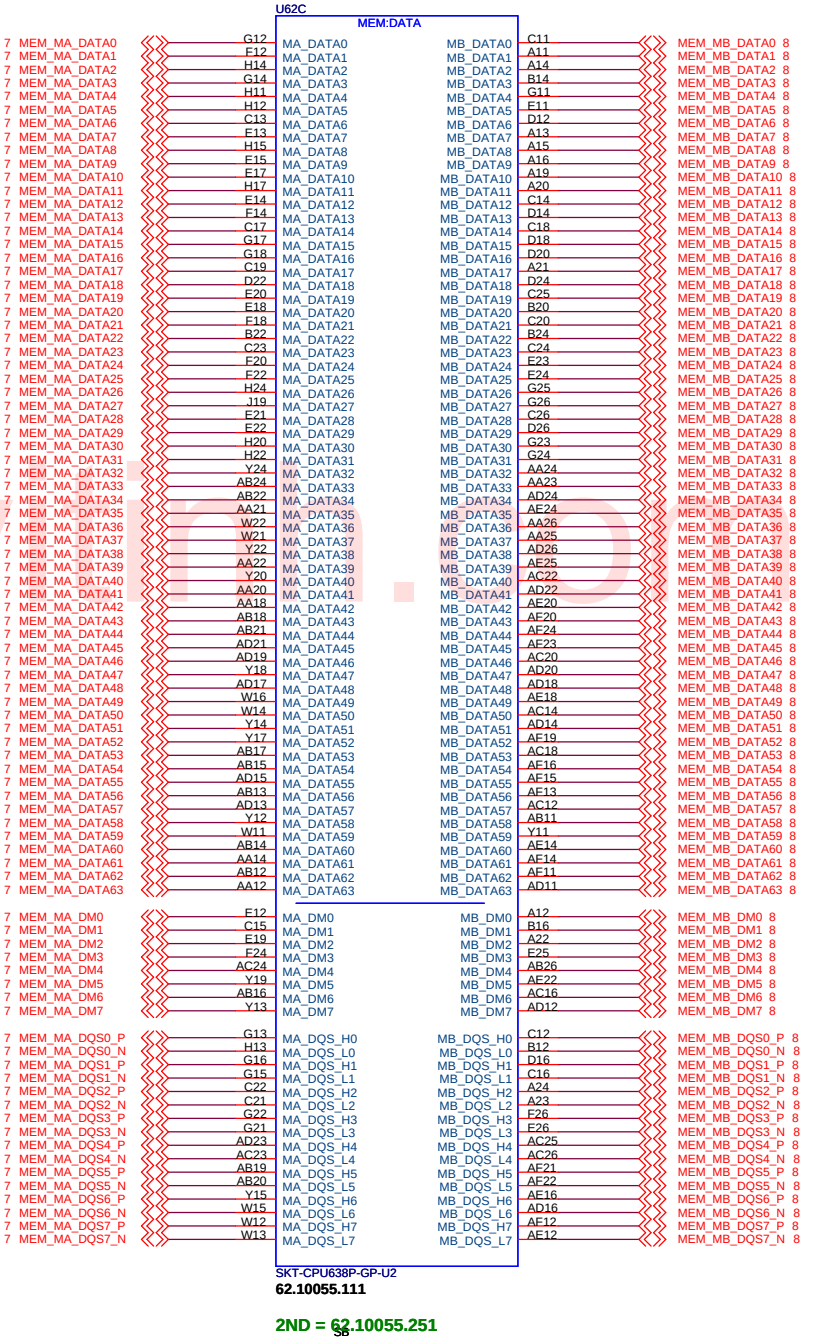
Title: CPU_HT_LINK I/F_(1/4)

Size: A3 | Document Number: F7-GT | Rev: SB

Date: Friday, August 29, 2008 | Sheet 3 of 47







緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU_DDR_(2/4)	
Size: A3	Document Number: F7-GT	Rev: SB
Date: Friday, August 29, 2008	Sheet 4 of 47	

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

For HDT DBG

20080721

20080723

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

Near CPU PIN

CPU exceeds to 125℃

HDT Connectors

CPU_DBREQ#	7	8	
CPU_DBRDY	9	10	
CPU_TCK	11	12	
CPU_TMS	13	14	
CPU_TDI	15	16	
CPU_TRST#	17	18	
CPU_TDO	19	20	
	21	22	
1D8V_S3	23	24	
		26	

HDT_RST#

Do Not Stuff

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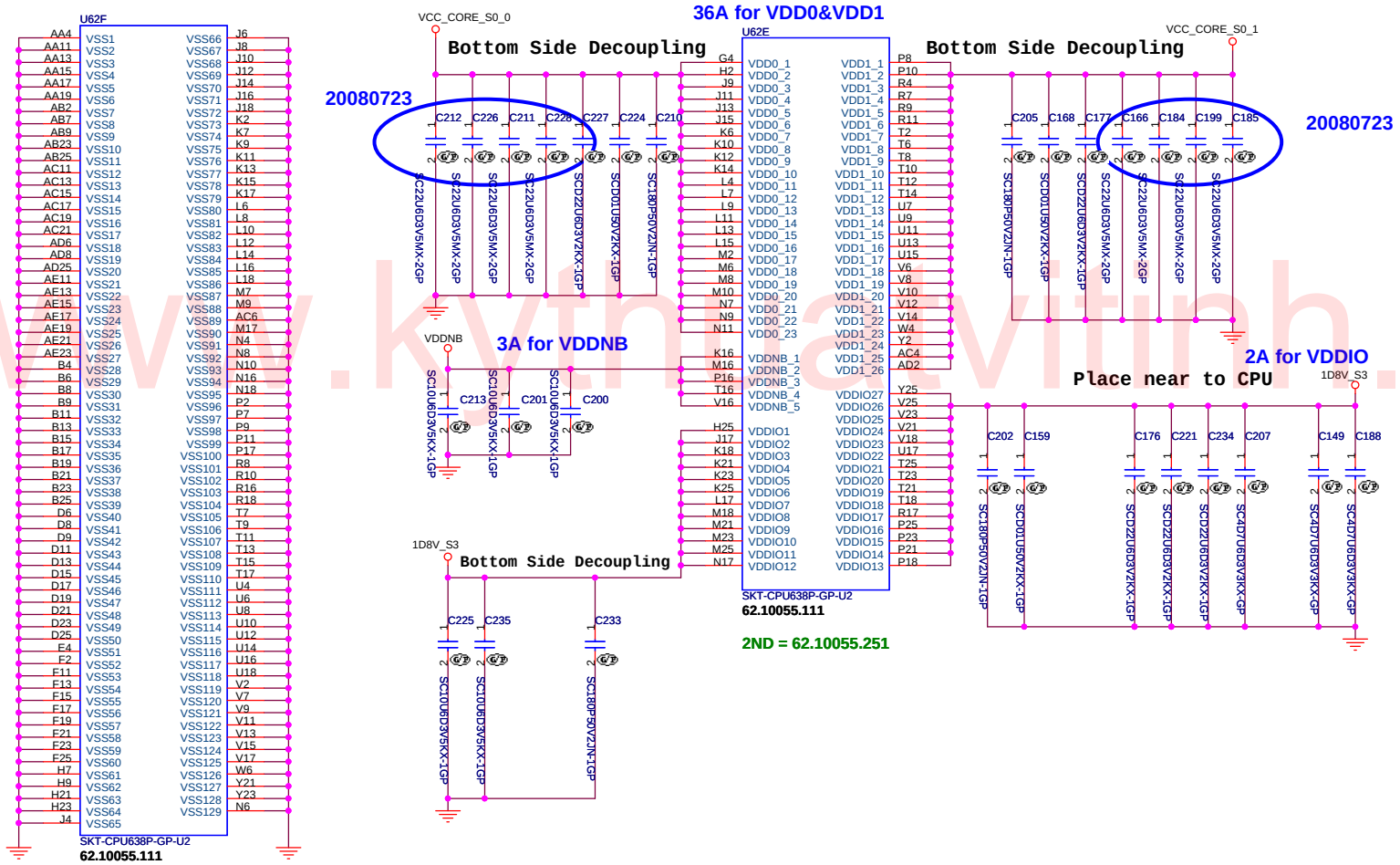
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_Control&Debug_(3/4)**

Size	Document Number	Rev
A3	F7-GT	SB

Date: Friday, August 29, 2008 Sheet 5 of 47



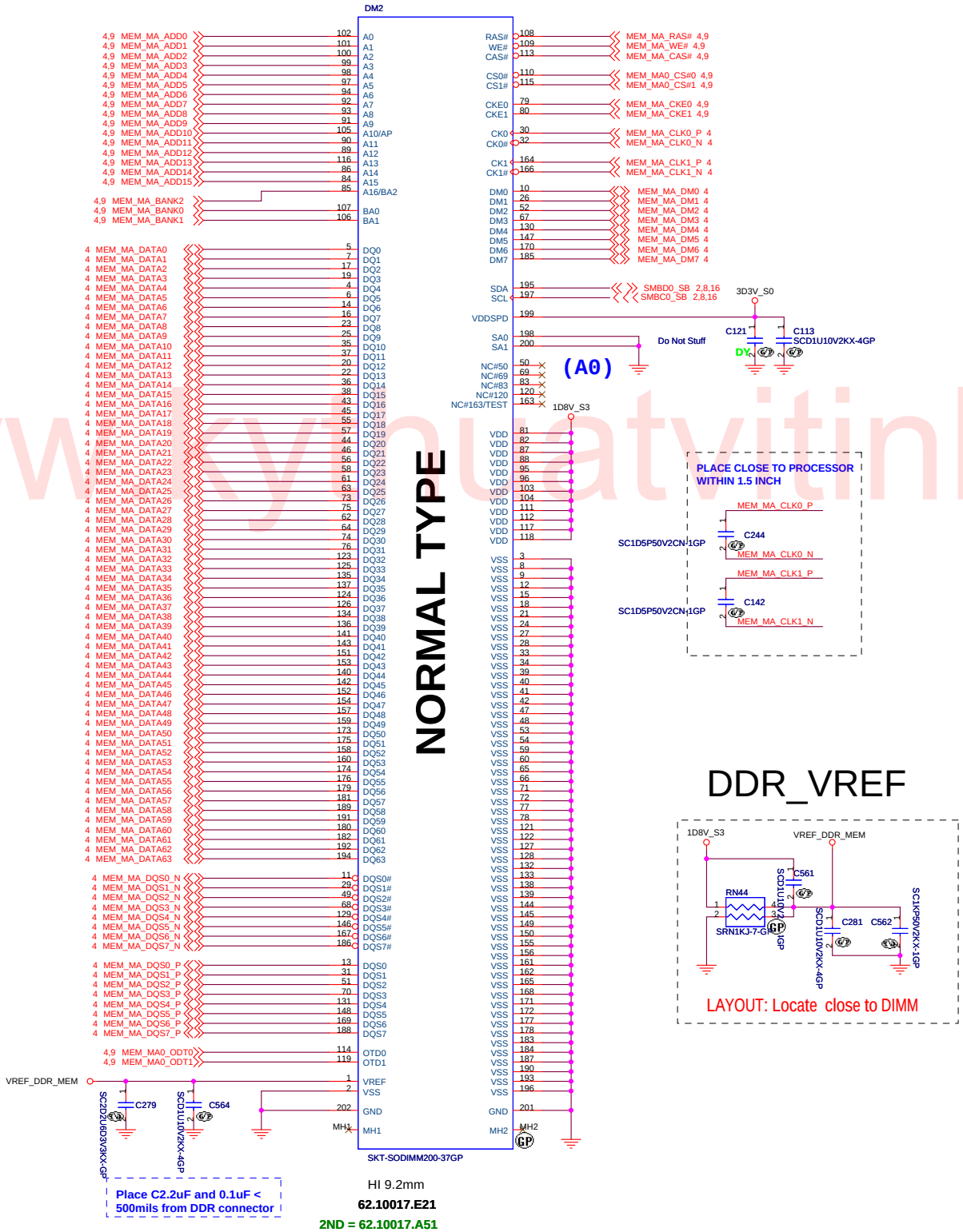
SB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Power_(4/4)

Size	Document Number	Rev
A3	F7-GT	SB

Date: Wednesday, August 20, 2008 Sheet 6 of 47



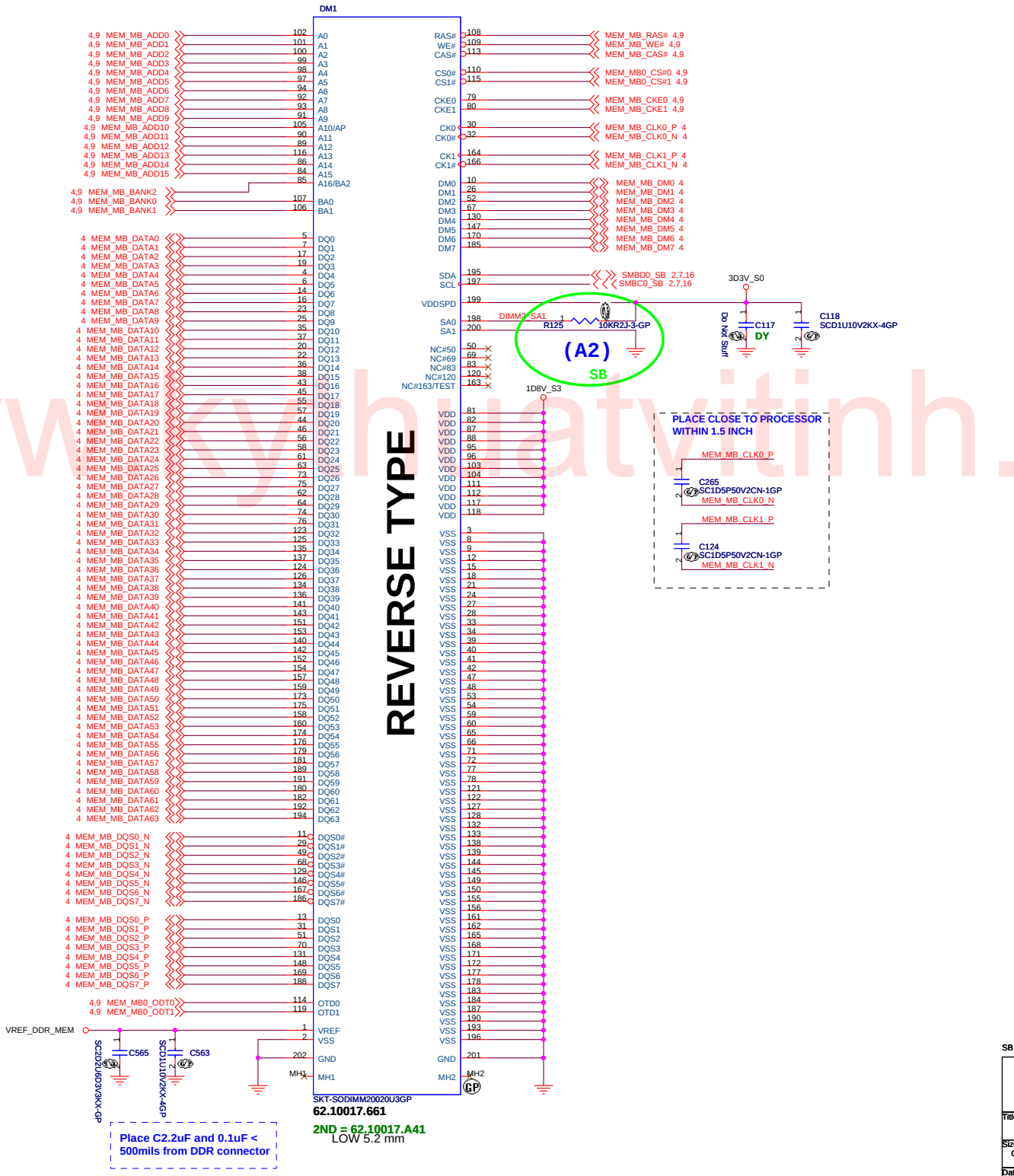
SB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	F7-GT	SB

Date: Wednesday, September 03, 2008 Sheet 7 of 47



SB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

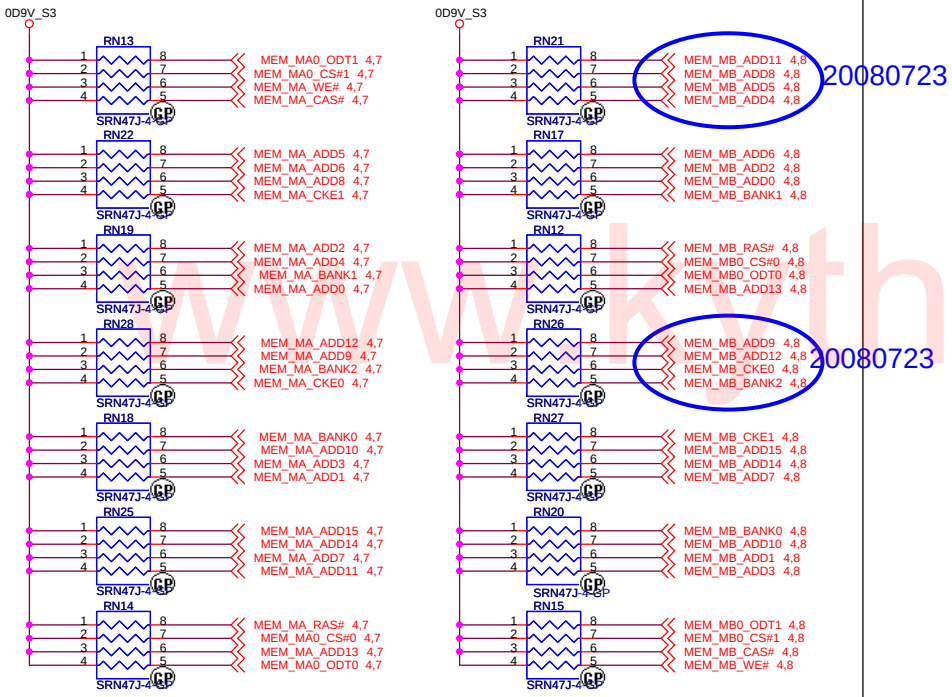
Title: DDR_SO-DIMM SKT_2

Size: Custom | Document Number: F7-GT | Rev: SB

Date: Friday, August 29, 2008 | Sheet 8 of 47

PARALLEL TERMINATION

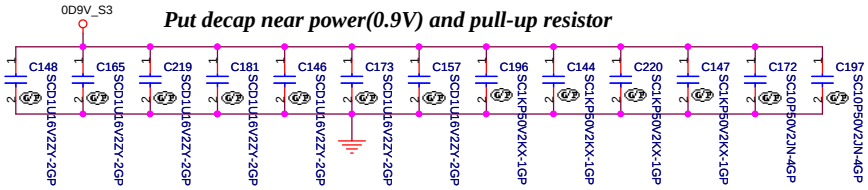
Put decap near power(0.9V) and pull-up resistor



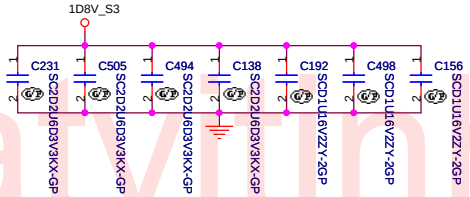
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

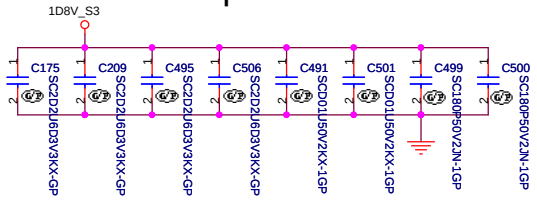


Place these Caps near DM1



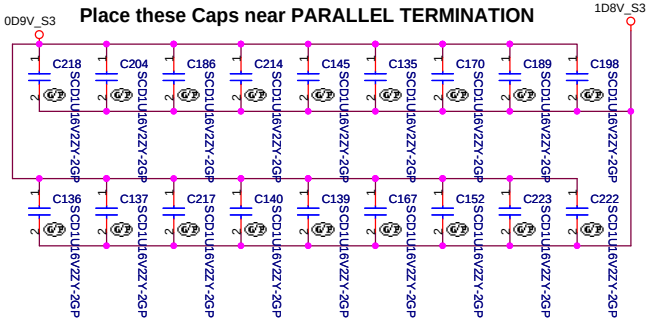
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



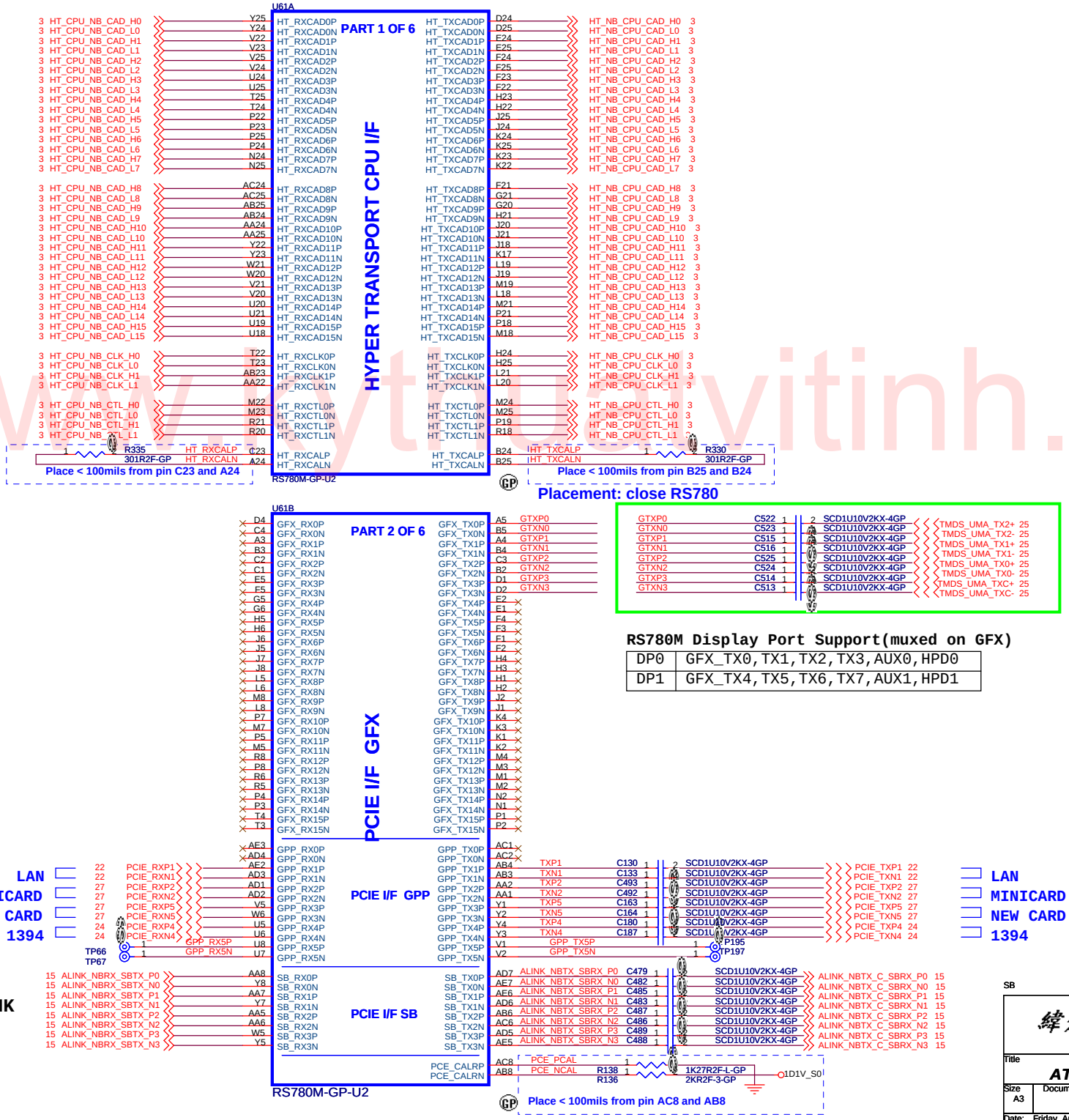
SB

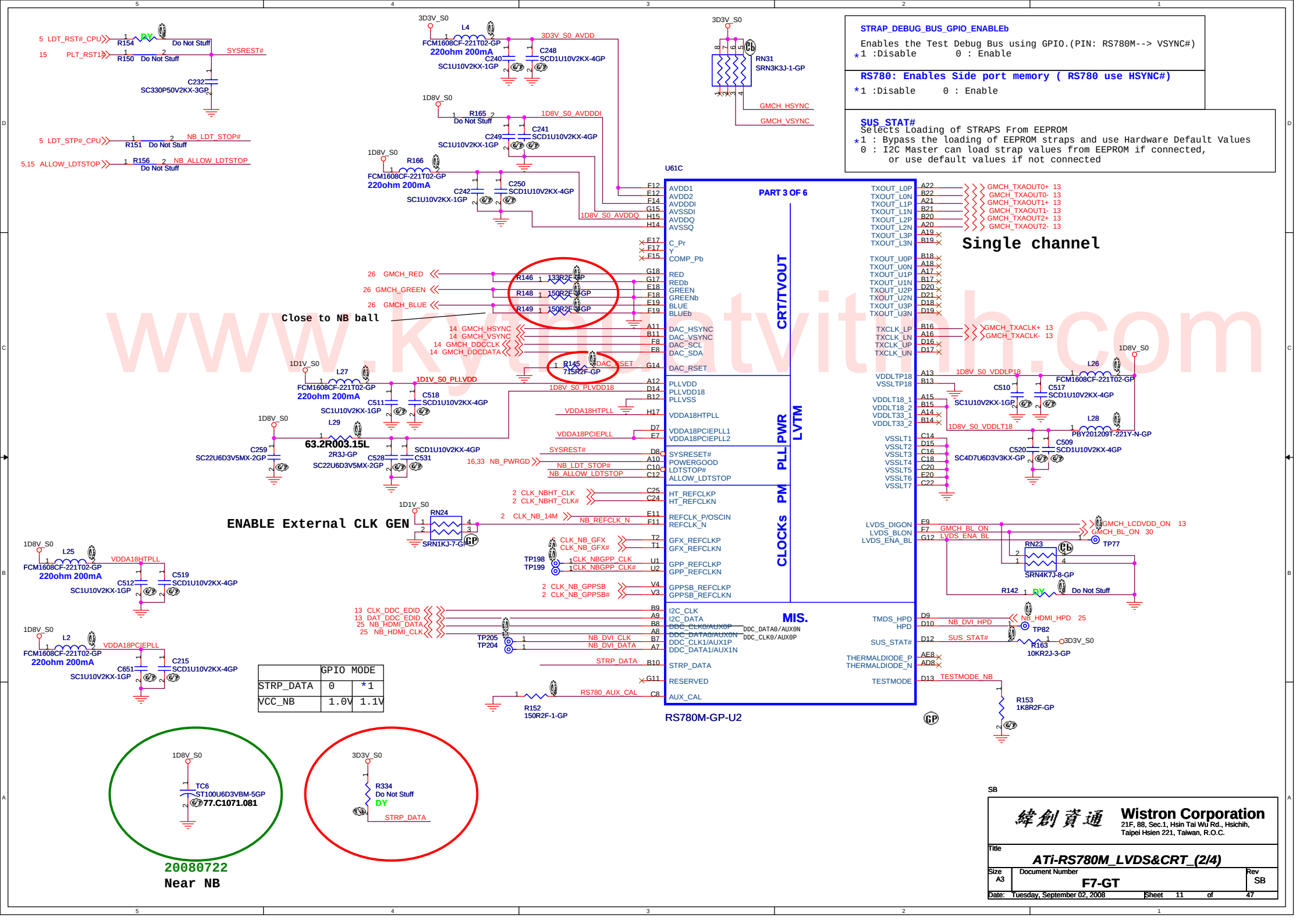
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

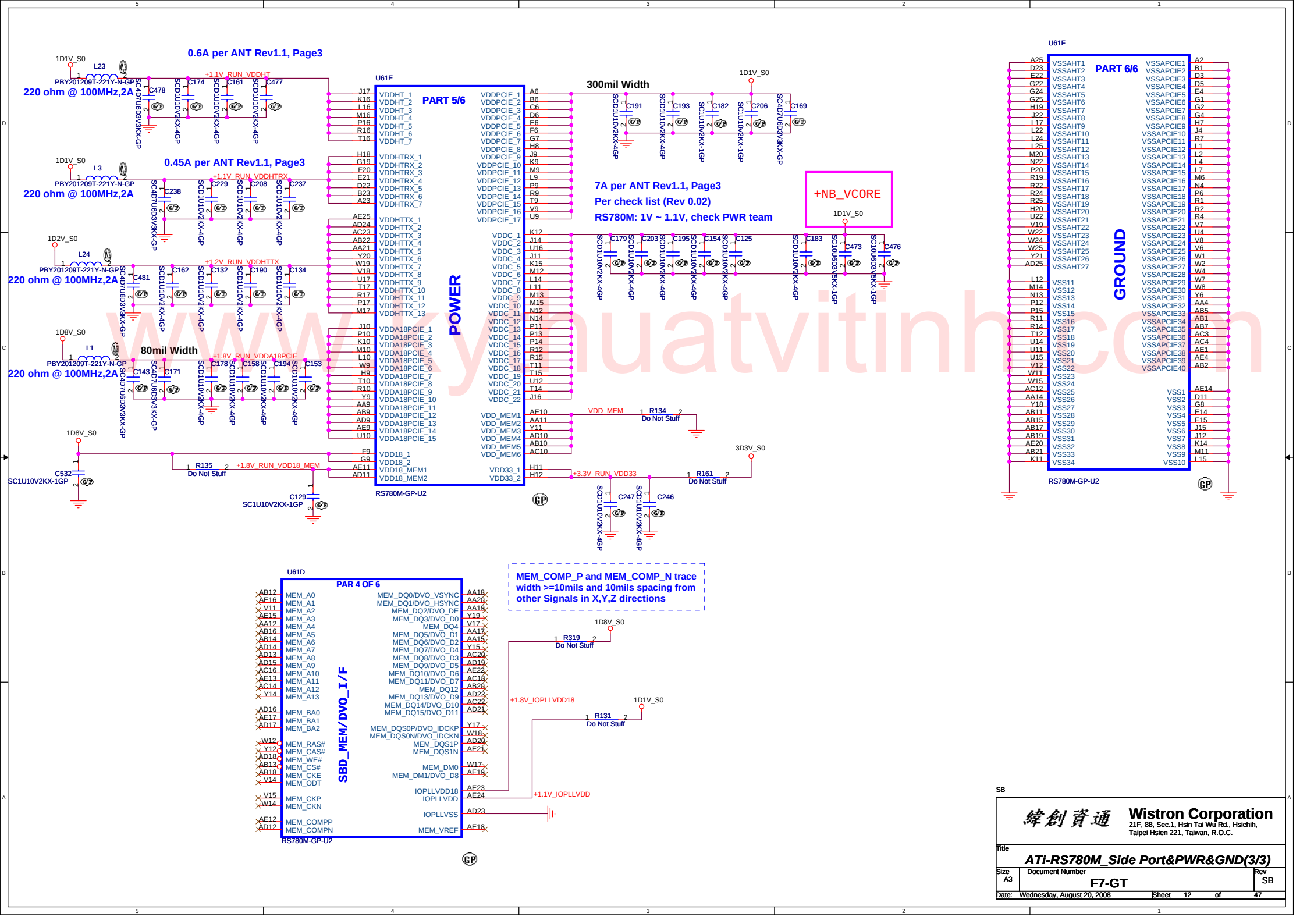
Title: ***DDR_DAMPING & TERMINATION***

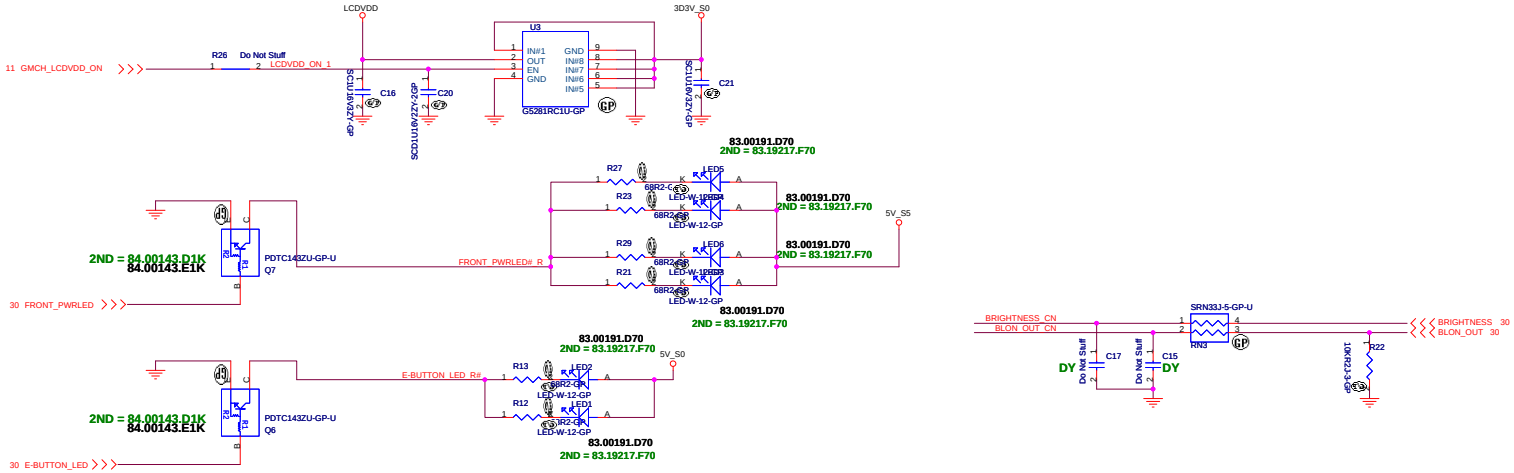
Size	Document Number	Rev
A3	F7-GT	SB

Date: Friday, August 29, 2008 Sheet 9 of 47

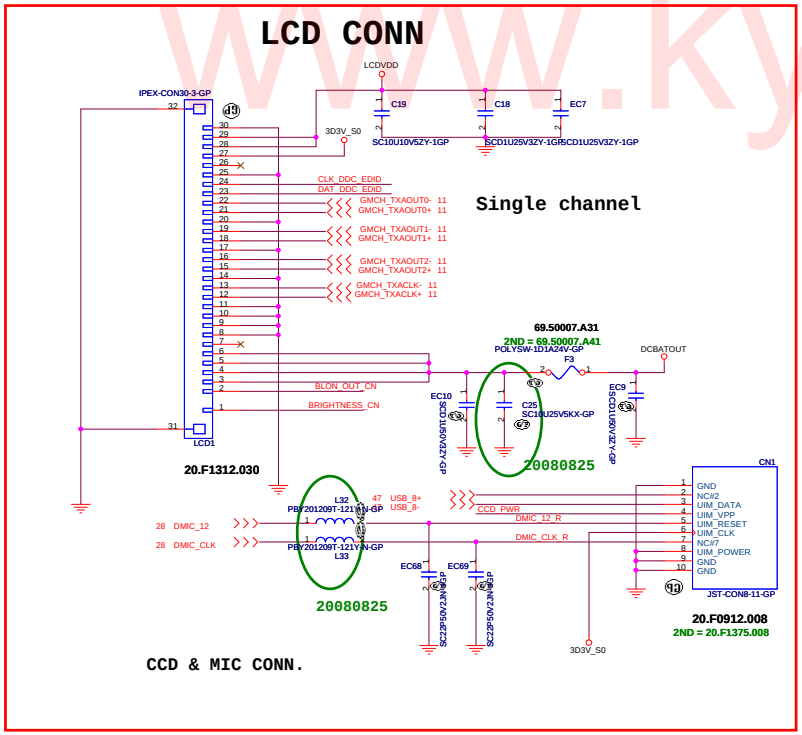

U61A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
Placement: close RS780
U61B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
Place < 100mils from pin AC8 and AB8
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
LAN
MINICARD
NEW CARD
1394
A-LINK
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M_HT LINK&PCIe(1/3)
F7-GT
SB
Friday, August 29, 2008
Sheet 10 of 47

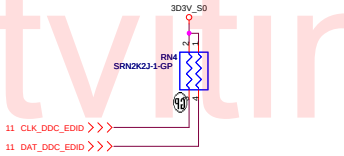


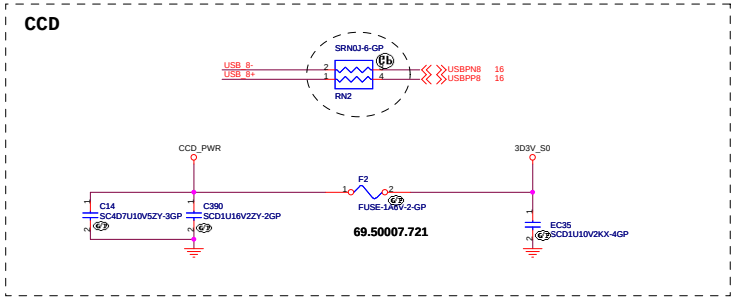

0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
7A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
220 ohm @ 100MHz,2A
PART 5/6
POWER
PART 6/6
GROUND
PAR 4 OF 6
SBD_MEM/DVO_I/F
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
Do Not Stuff
RS780M-GP-U2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M_Side Port&PWR&GND(3/3)
F7-GT
Wednesday, August 20, 2008
Sheet 12 of 47



20080731 change connect

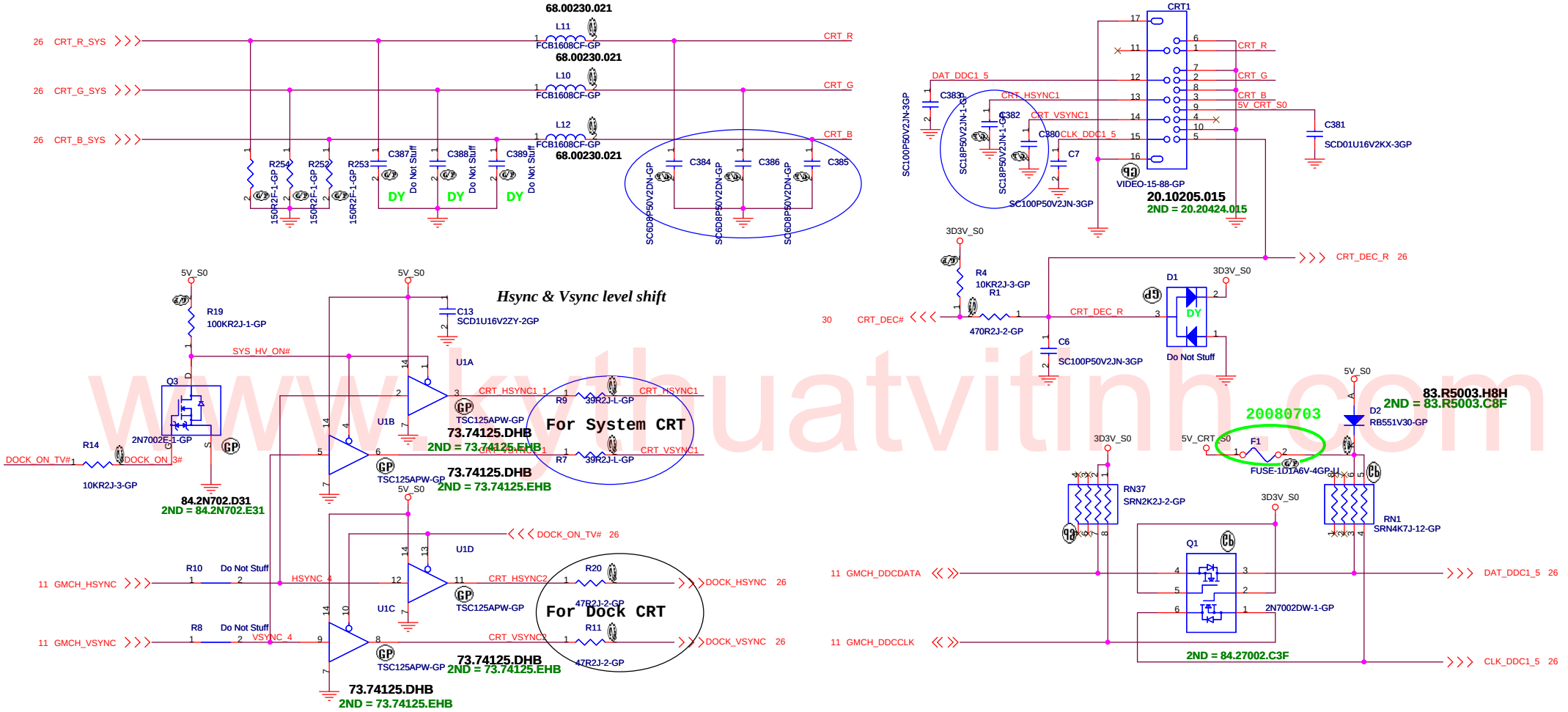




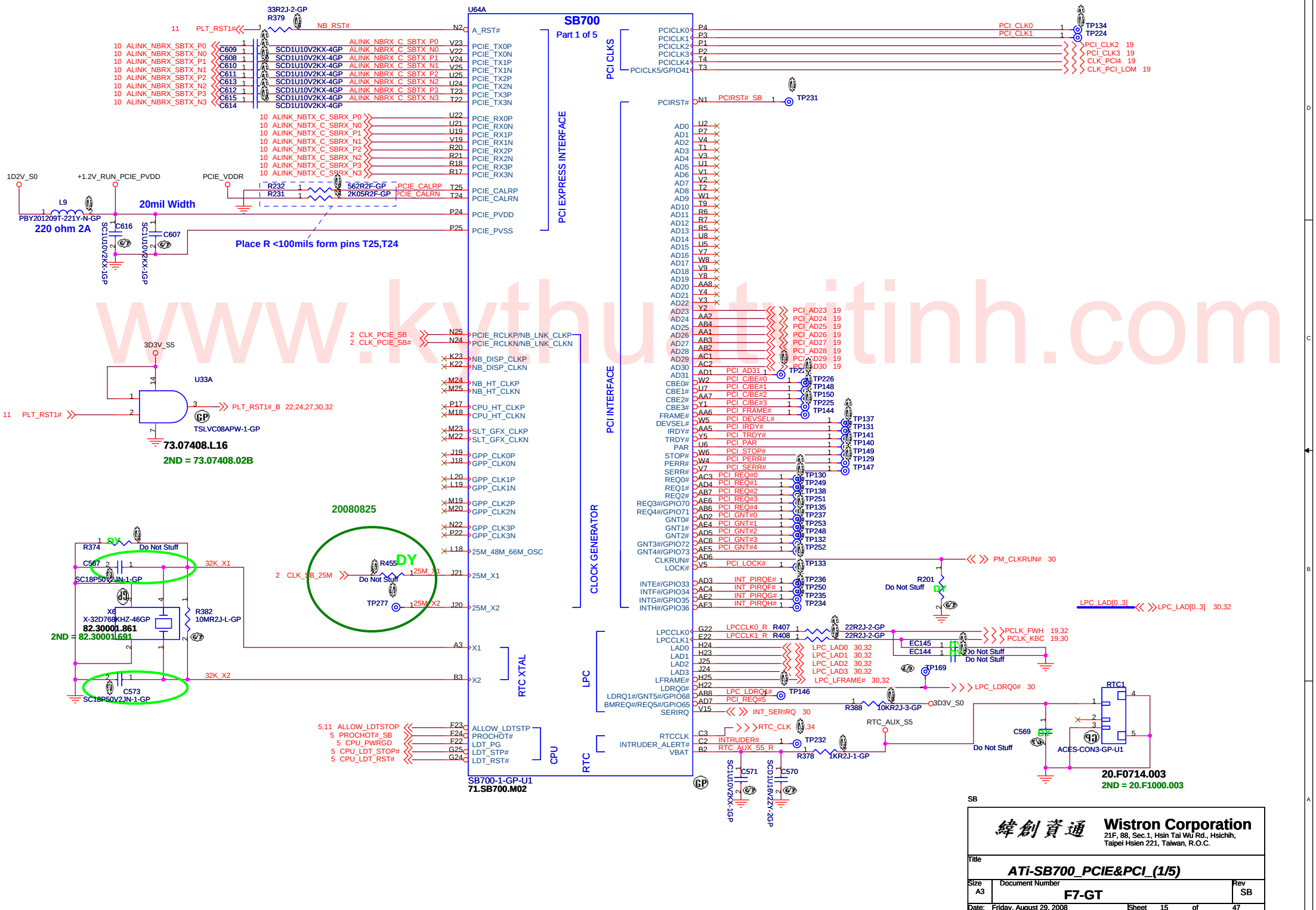


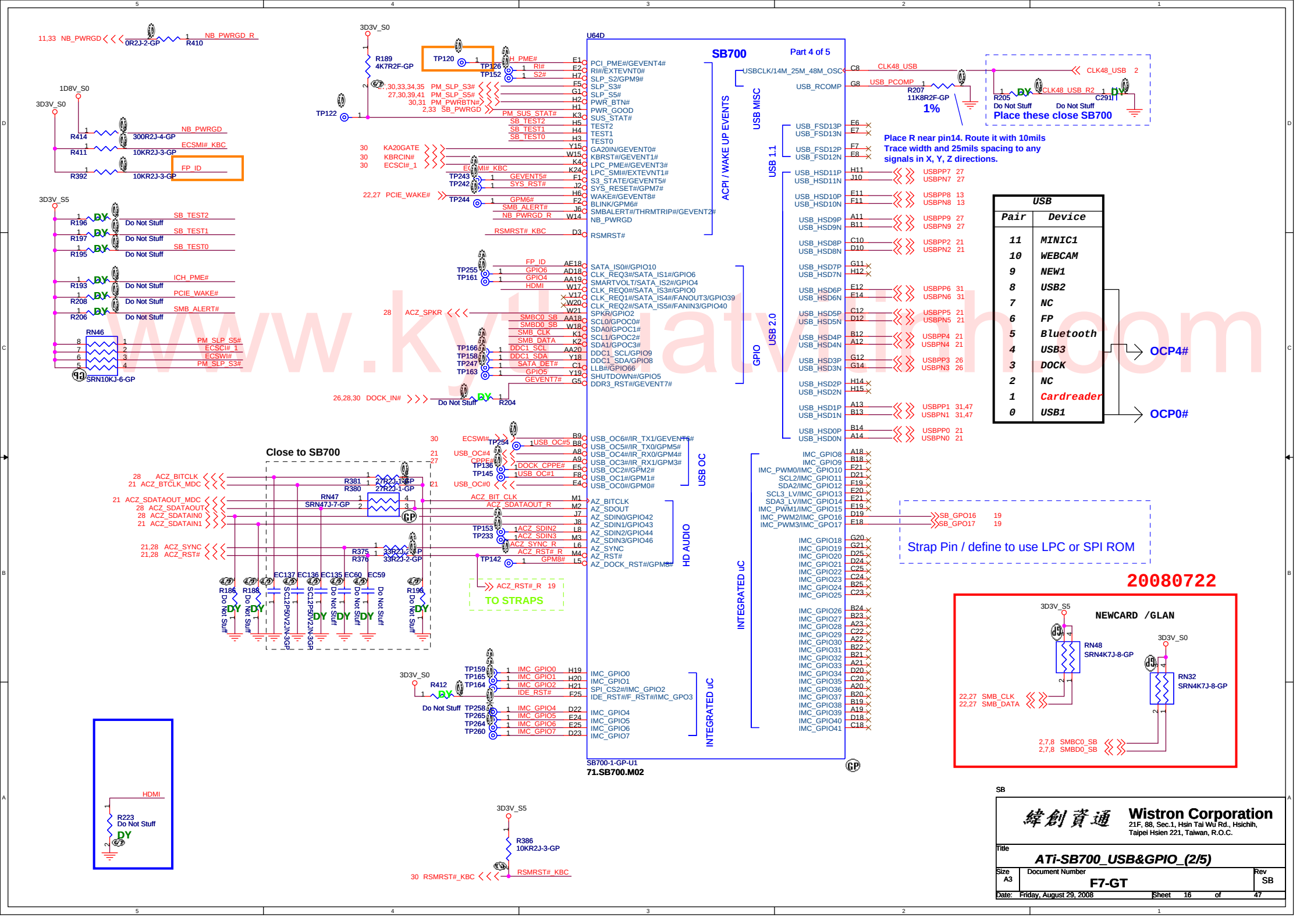
SB

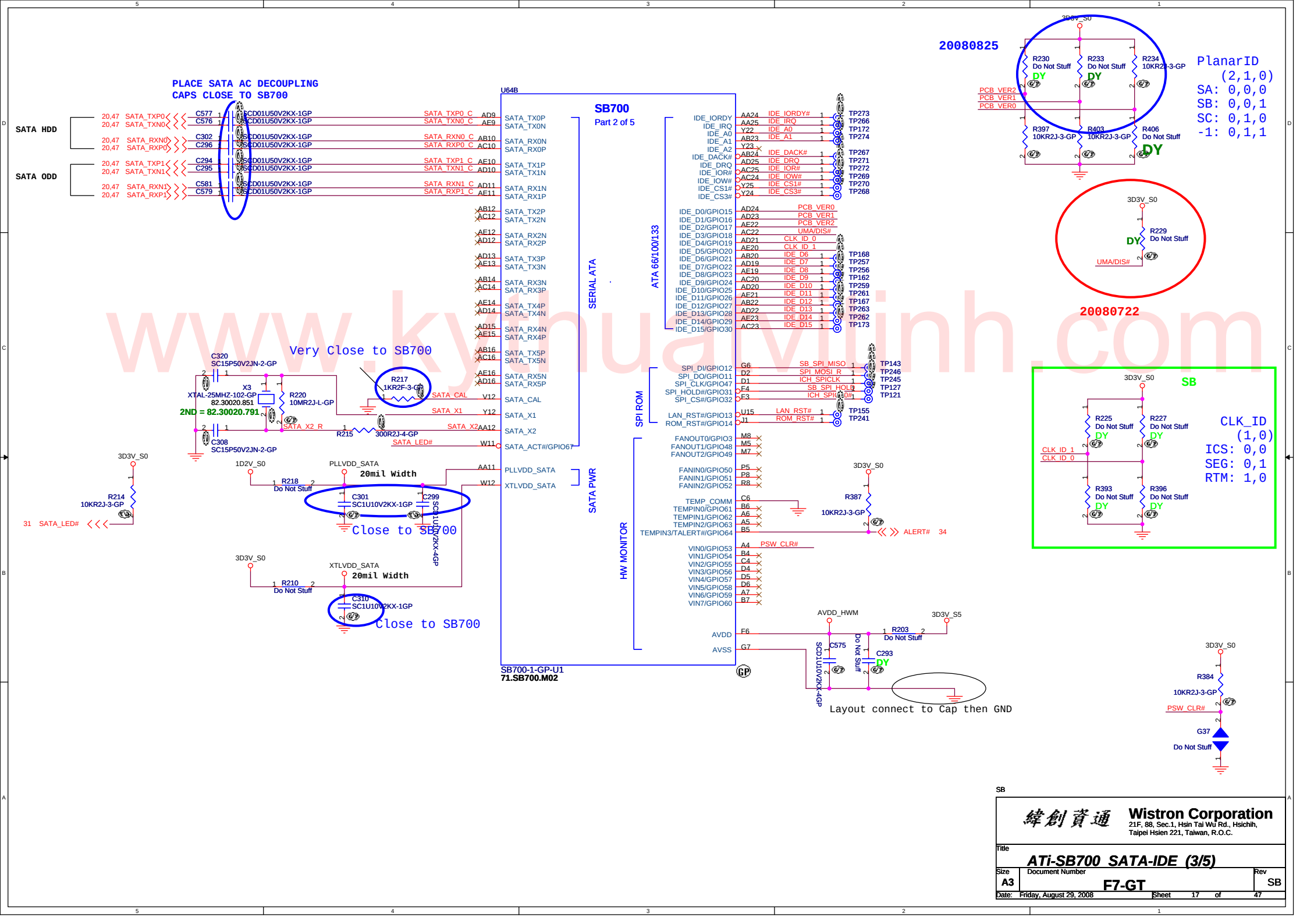
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN & LED		
Size	Document Number: F7-GT	Rev: SB
Date: Tuesday, September 02, 2008	Sheet 13 of 47	

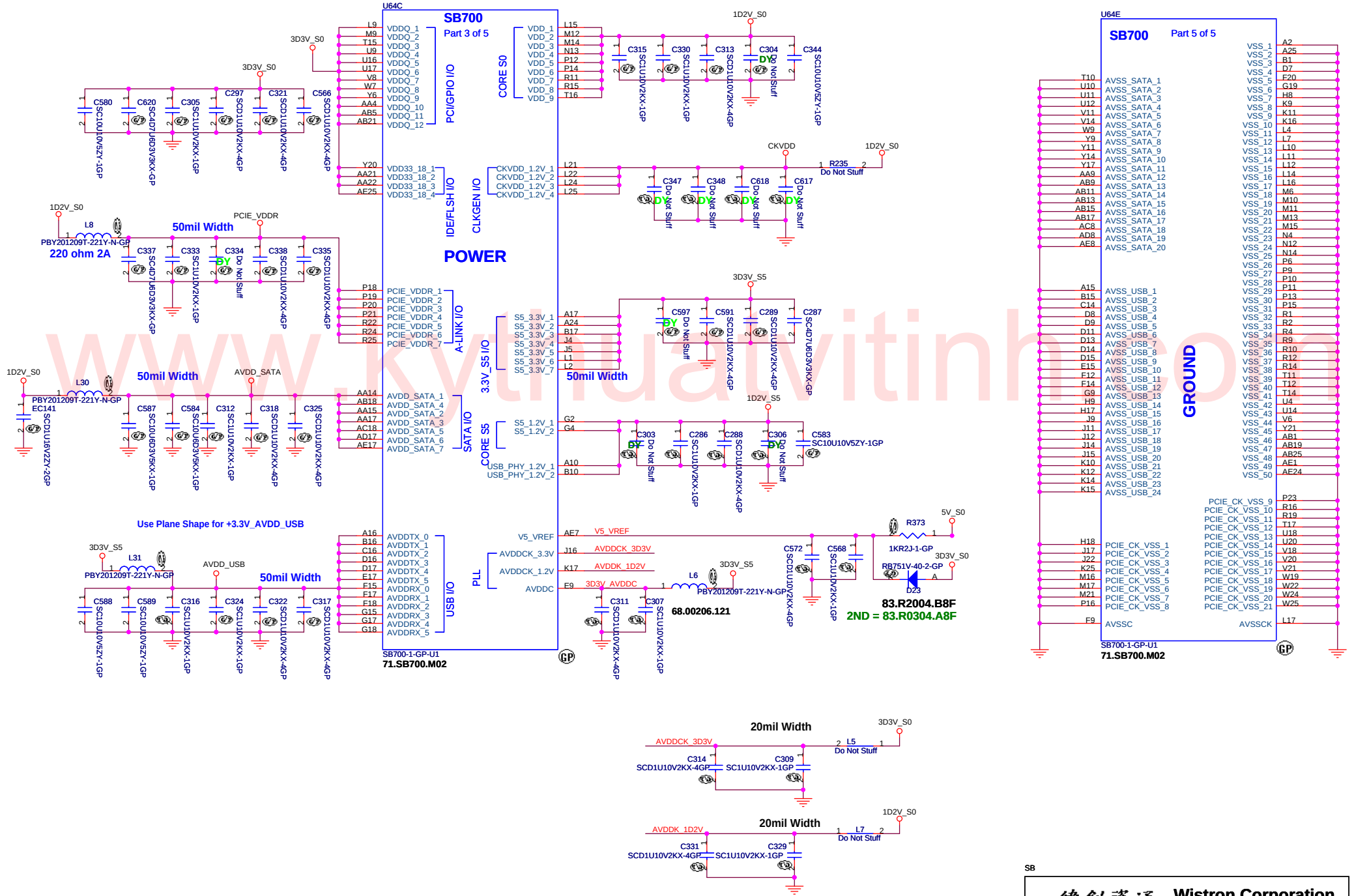


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*CRT/TV Connector*	
Size	Document Number F7-GT	Rev SB
Date: Monday, September 01, 2008	Sheet 14 of 47	




SB700
Part 4 of 5
U64D
SB700-1-GP-U1
71.SB700.M02
USB MISC
USB 1.1
USB 2.0
GPIO
ACPI / WAKE UP EVENTS
USB OC
HD AUDIO
INTEGRATED uC
Close to SB700
TO STRAPS
Strap Pin / define to use LPC or SPI ROM
Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.
Place these close SB700
USB
Pair Device
11 MINIC1
10 WEBCAM
9 NEW1
8 USB2
7 NC
6 FP
5 Bluetooth
4 USB3
3 DOCK
2 NC
1 Cardreader
0 USB1
OCP4#
OCP0#
20080722
NEWCARD /GLAN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700_USB&GPIO_(2/5)
F7-GT
Size A3
Rev SB
Date: Friday, August 29, 2008
Sheet 16 of 47


PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700
SATA HDD
SATA ODD
SB700
Part 2 of 5
SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR
SB700-1-GP-U1
71.SB700.M02
Very Close to SB700
2ND = 82.30020.791
20mil Width
Close to SB700
Layout connect to Cap then GND
20080825
PlanarID
(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
-1: 0,1,1
20080722
SB
CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700 SATA-IDE (3/5)
F7-GT
SB
Friday, August 29, 2008
17 of 47

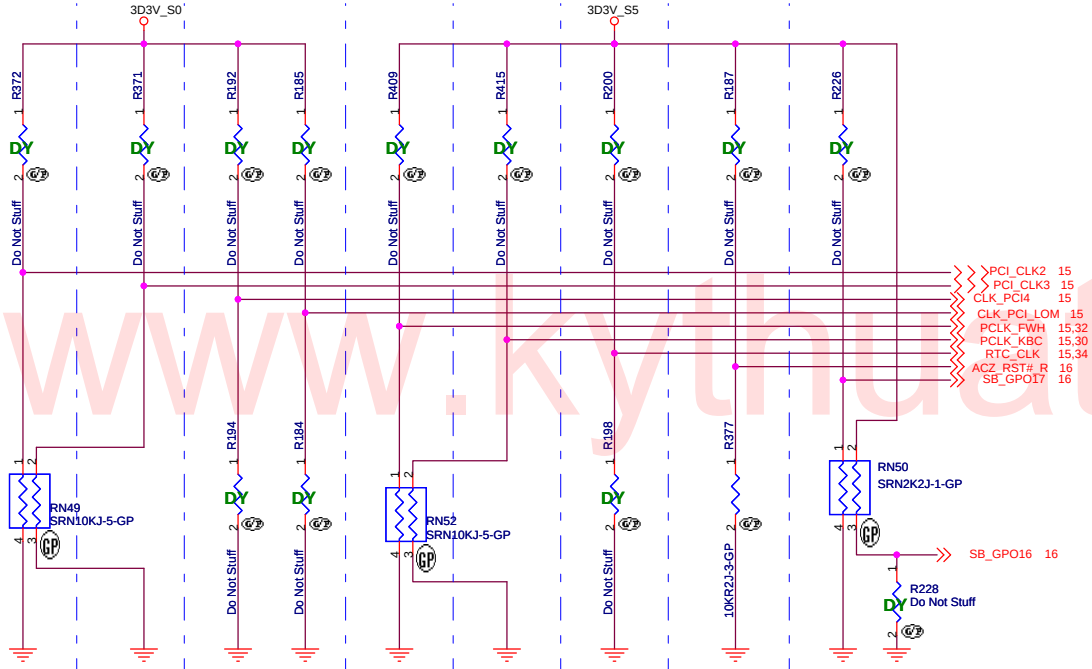


SB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***ATi-SB700 POWER&GND (4/5)***
Size: A3	Document Number: F7-GT
Rev: SB	
Date: Tuesday, August 26, 2008	Sheet 18 of 47

REQUIRED STRAPS

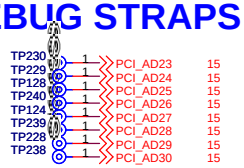
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
								ROM TYPE:
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

SB

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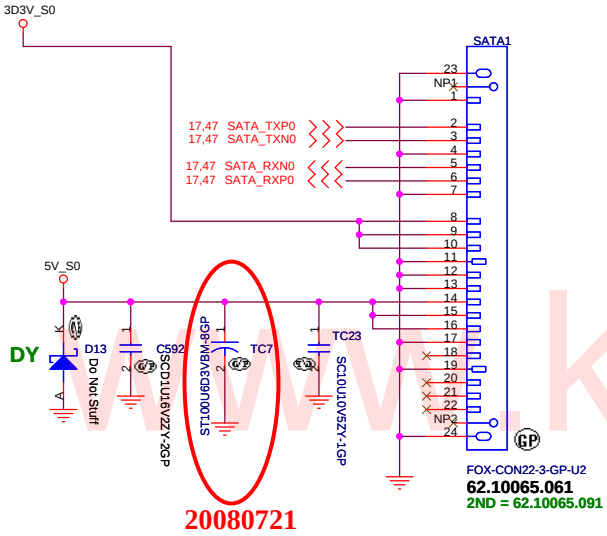
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: F7-GT | Rev: SB

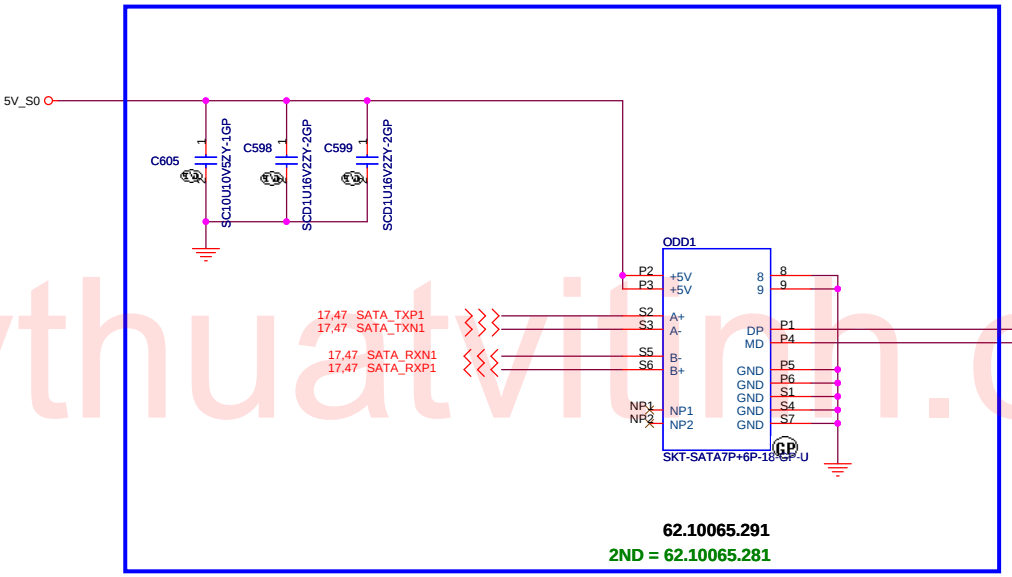
Date: Friday, August 29, 2008 | Sheet 19 of 47

SATA HDD Connector

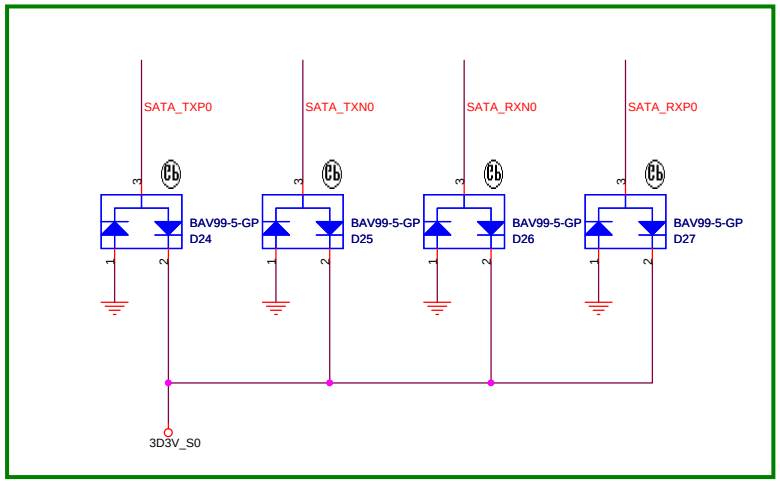


20080714

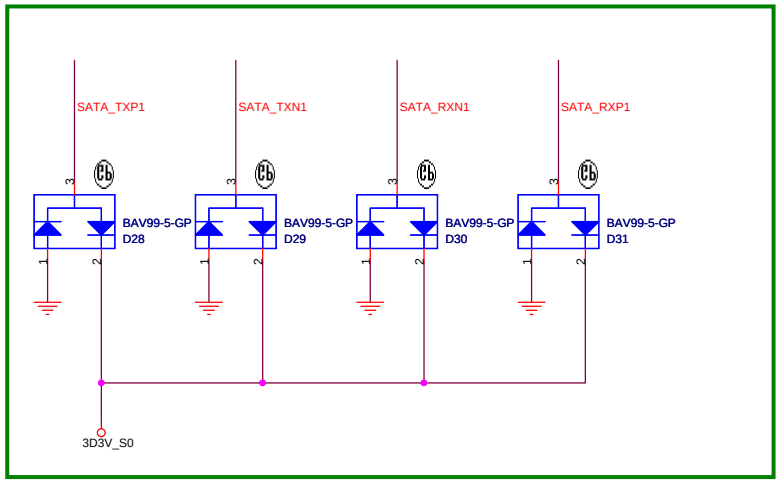
SATA ODD Connector



For HDD



For ODD



SB

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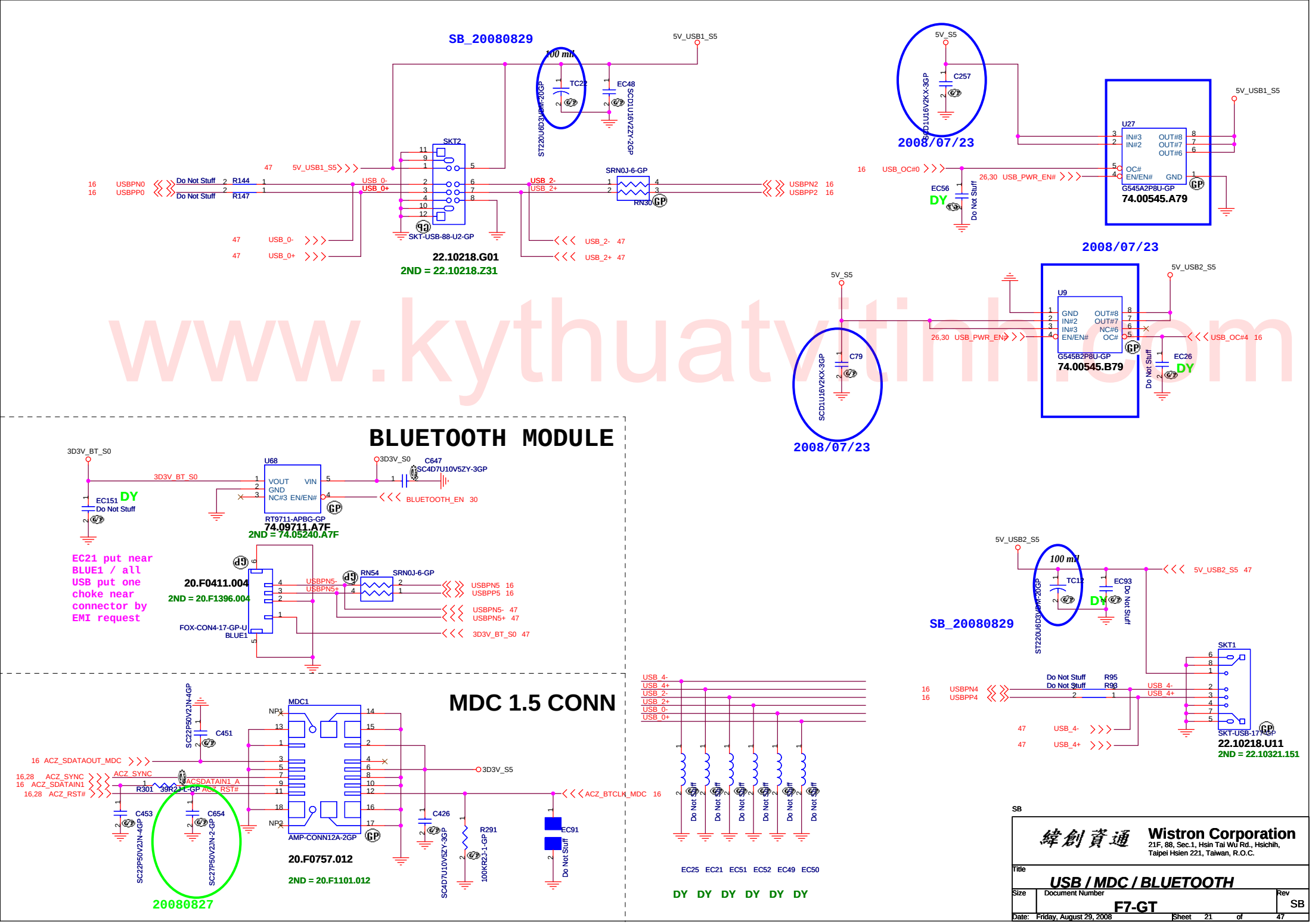
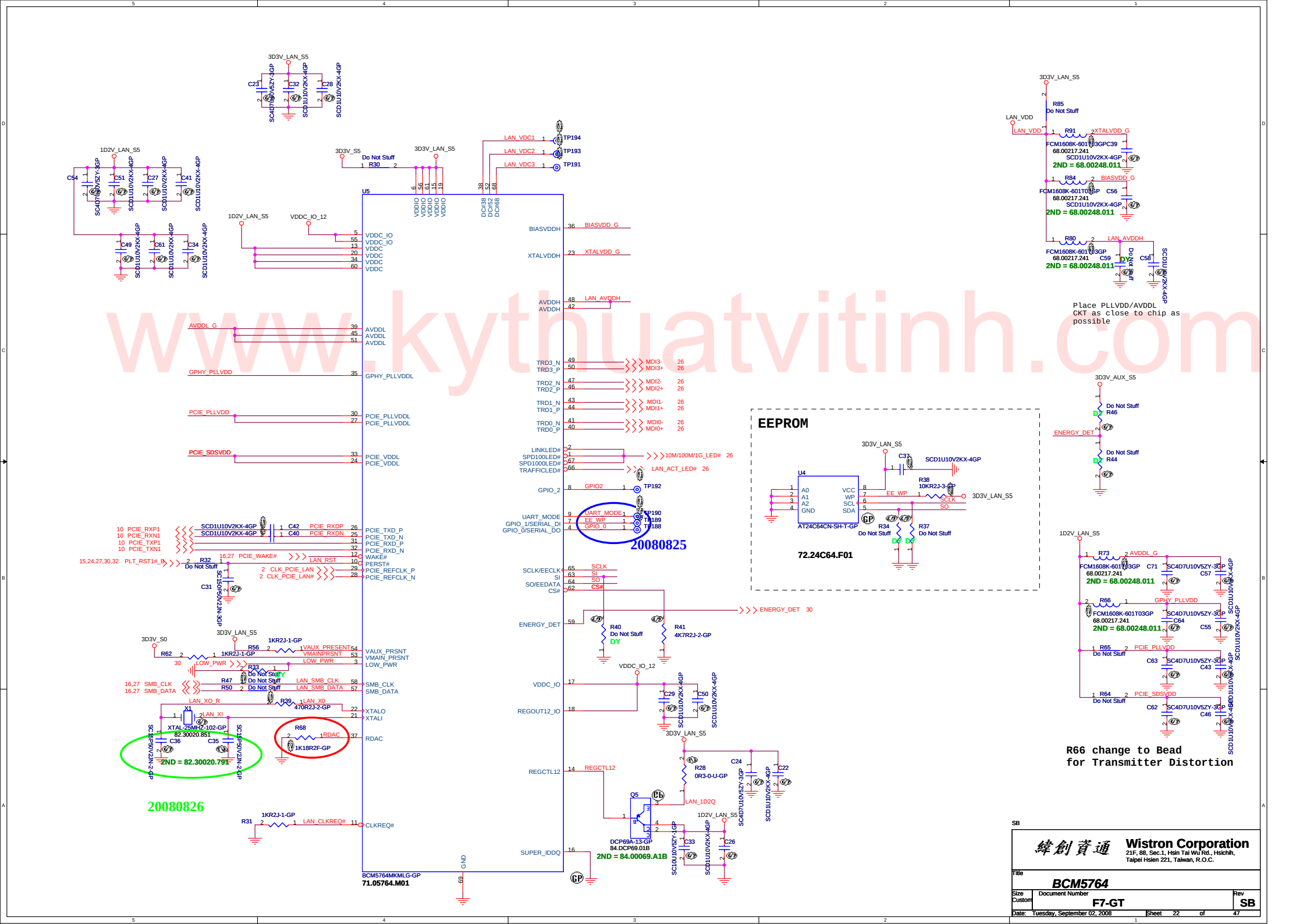
Title: ***HDD and CDROM***

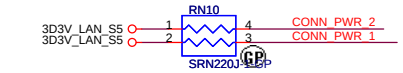
Size	Document Number	Rev
	F7-GT	SB

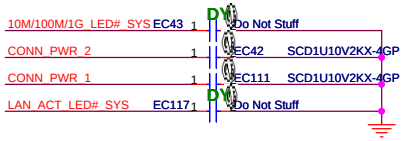
Date: Friday, August 29, 2008 Sheet 20 of 47

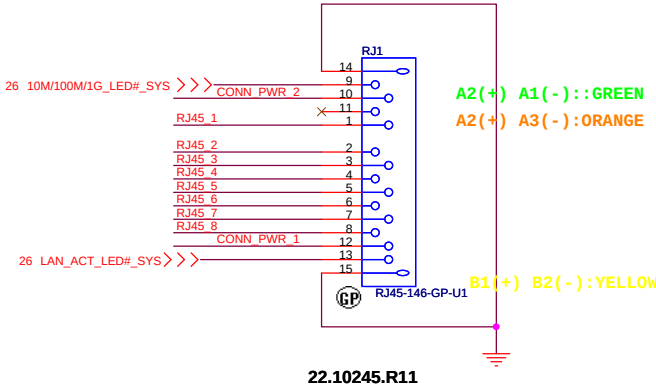



U5
BCM5764MKMLG-GP
71.05764.M01
EEPROM
U4
AT24C64CN-SH-T-GP
72.24C64.F01
20080825
20080826
2ND = 82.30020.791
2ND = 84.00069.A1B
2ND = 68.00248.011
Place PLLVDD/AVDDL CKT as close to chip as possible
R66 change to Bead for Transmitter Distortion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
BCM5764
F7-GT
SB
Tuesday, September 02, 2008
22 of 47

LAN Connector



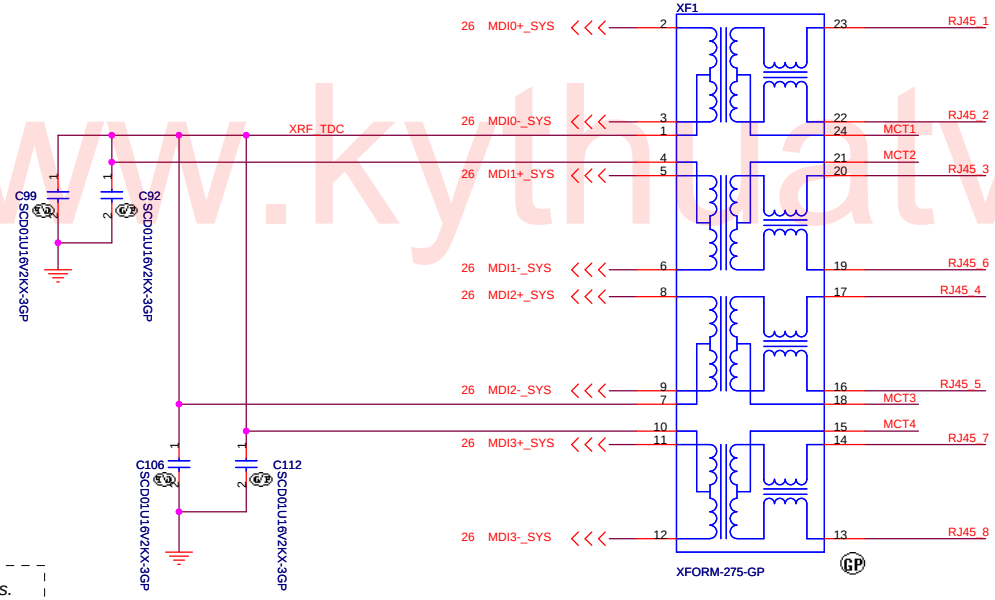




22.10245.R11

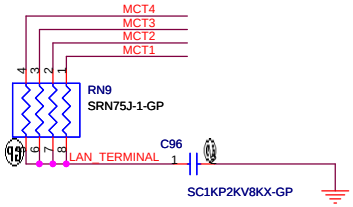
2ND = 22.10245.X61

GIGA Lan Transformer



68.89240.30A

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

SB

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Title: **LAN Connector**

Size: A3 | Document Number: F7-GT | Rev: SB

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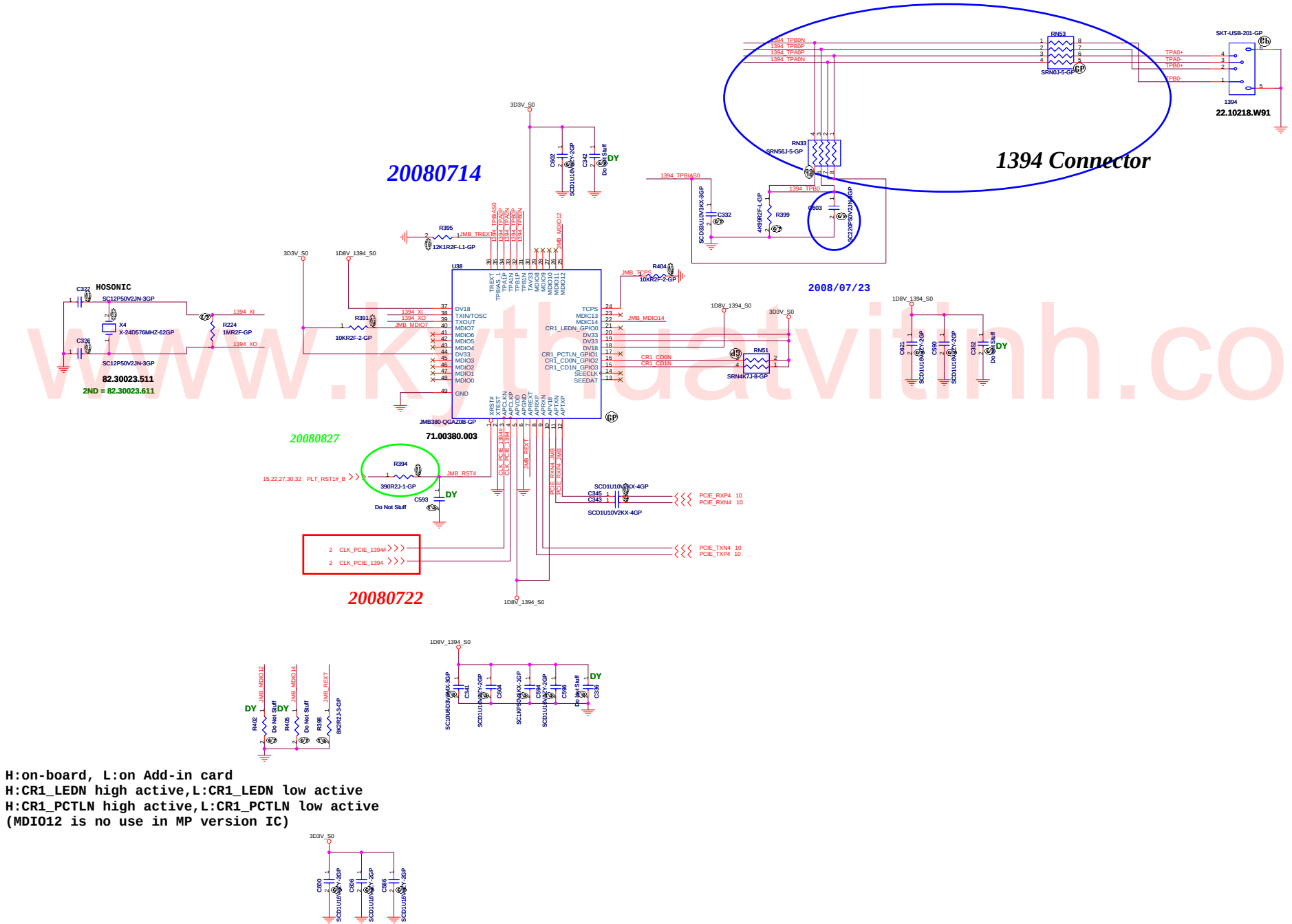

H:on-board, L:on Add-in card
H:CR1_LEDN high active,L:CR1_LEDN low active
H:CR1_PCTLN high active,L:CR1_PCTLN low active
(MDIO12 is no use in MP version IC)

SB

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Taipei Hsien 221, Taiwan, R.O.C.

Title: 1394-JMB380

Size	Document Number	Rev
	F7-GT	SB

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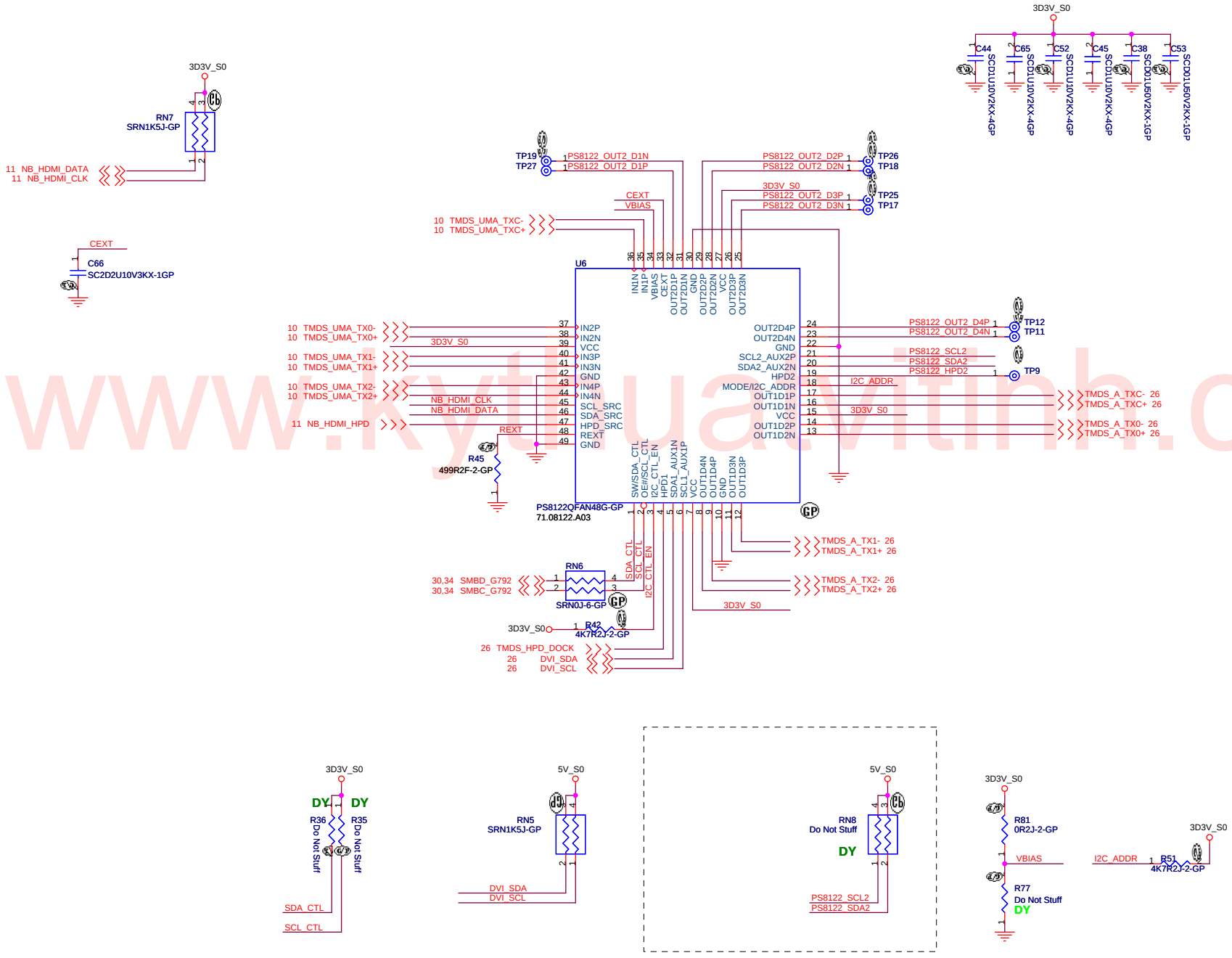

SB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*PS8122*
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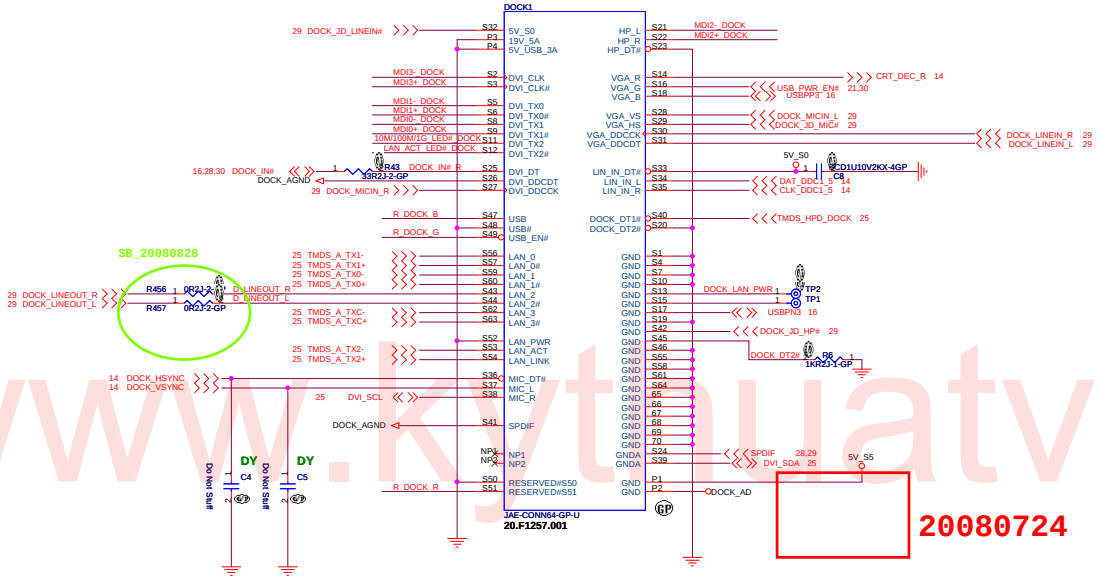
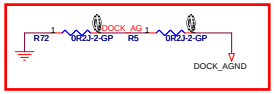
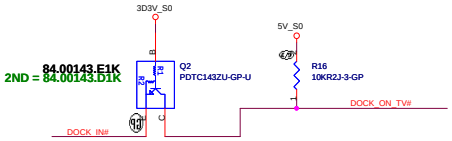
20080709 change to Port Replicator

DOCK

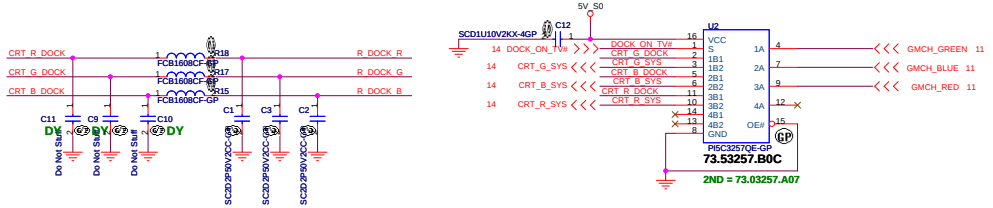




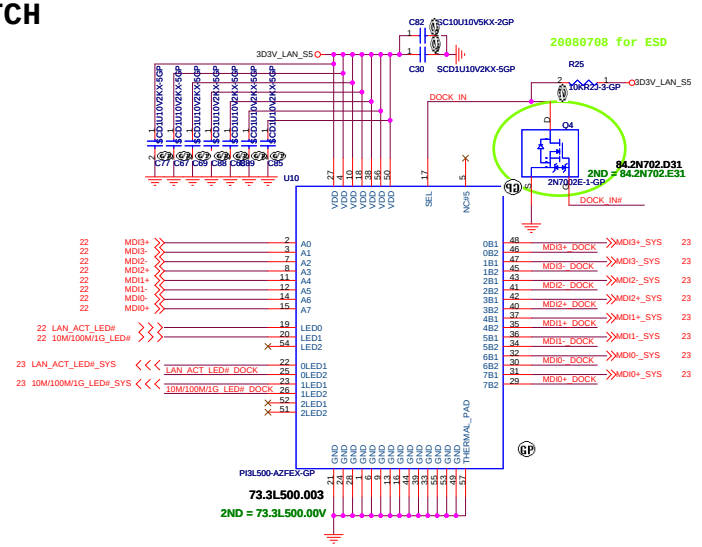
CRT SWITCH



Function	CRT	TV
SYSTEM	H	H
DOCK	L	L



LAN SWITCH



Function	LAN
SYSTEM	L
DOCK	H

SB

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Title: DOCK

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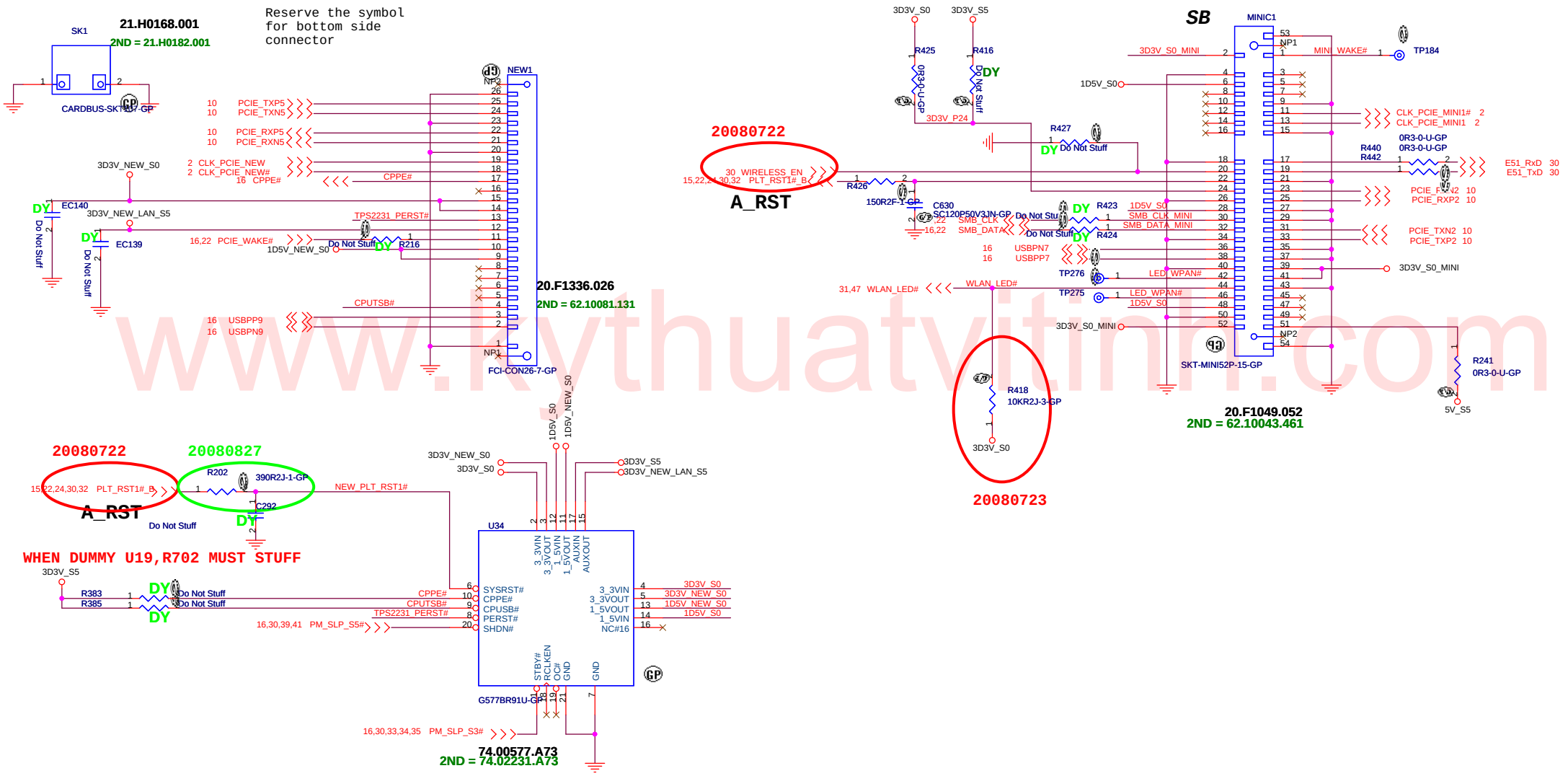
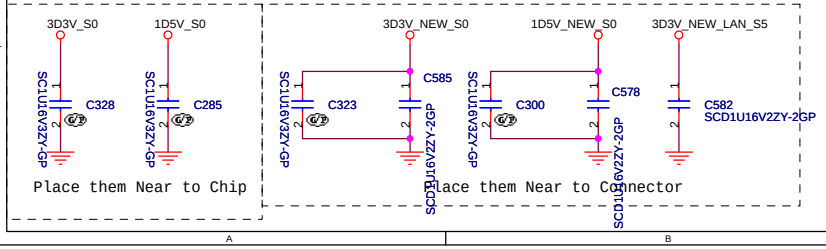
Date: Wednesday, September 03, 2008 | Sheet 26 of 47

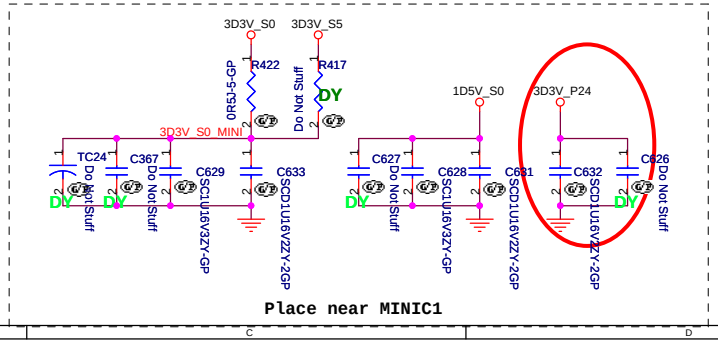
NEWCARD Connector

Mini Card Connector



CHECK WITH COLUMBIA





SB

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Title: MINI CARD / NEW CARD

Size | Document Number: F7-GT | Rev: SB

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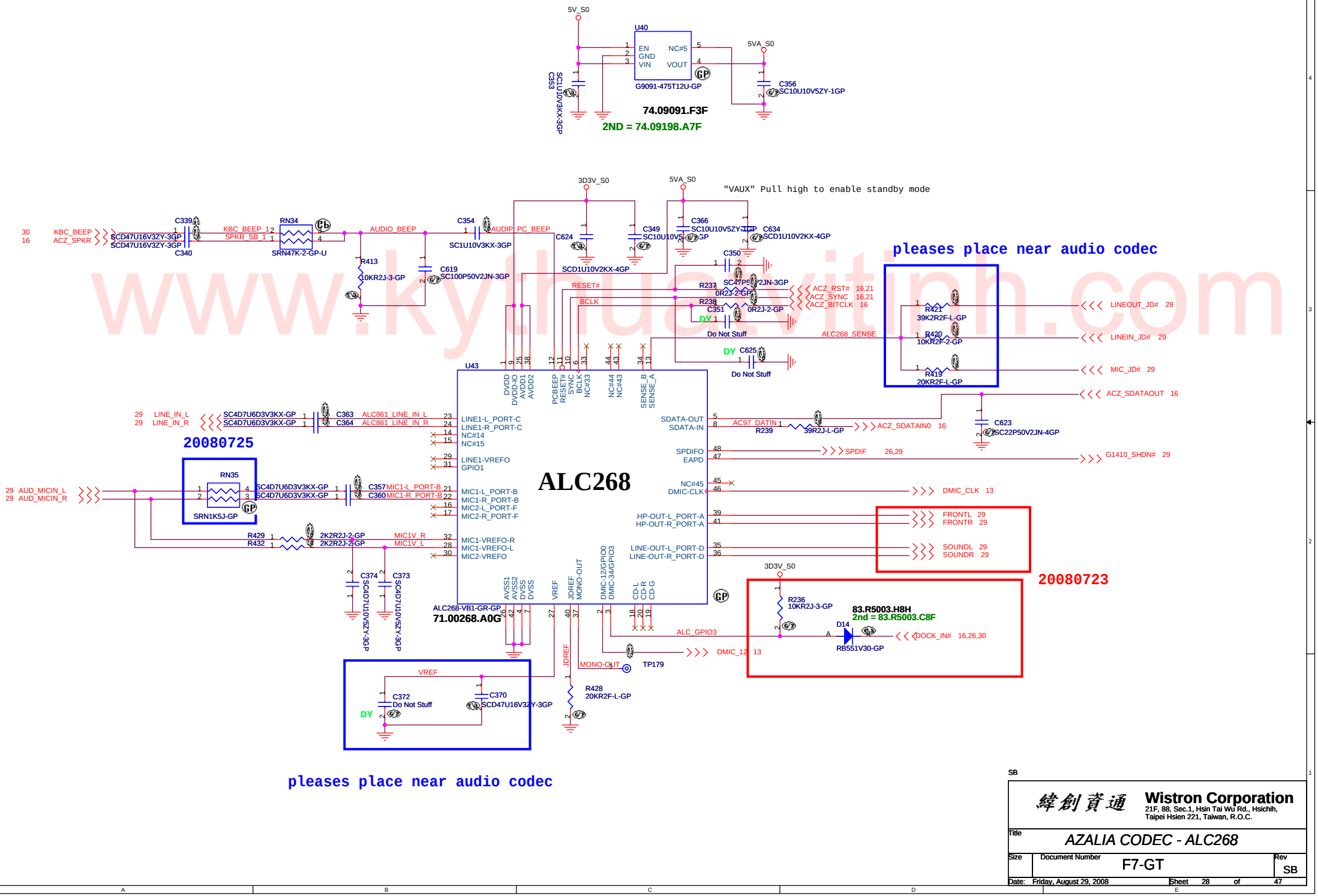

SB

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Taipei Hsien 221, Taiwan, R.O.C.

Title	*AZALIA CODEC - ALC268*	
Size	Document Number: F7-GT	Rev: SB
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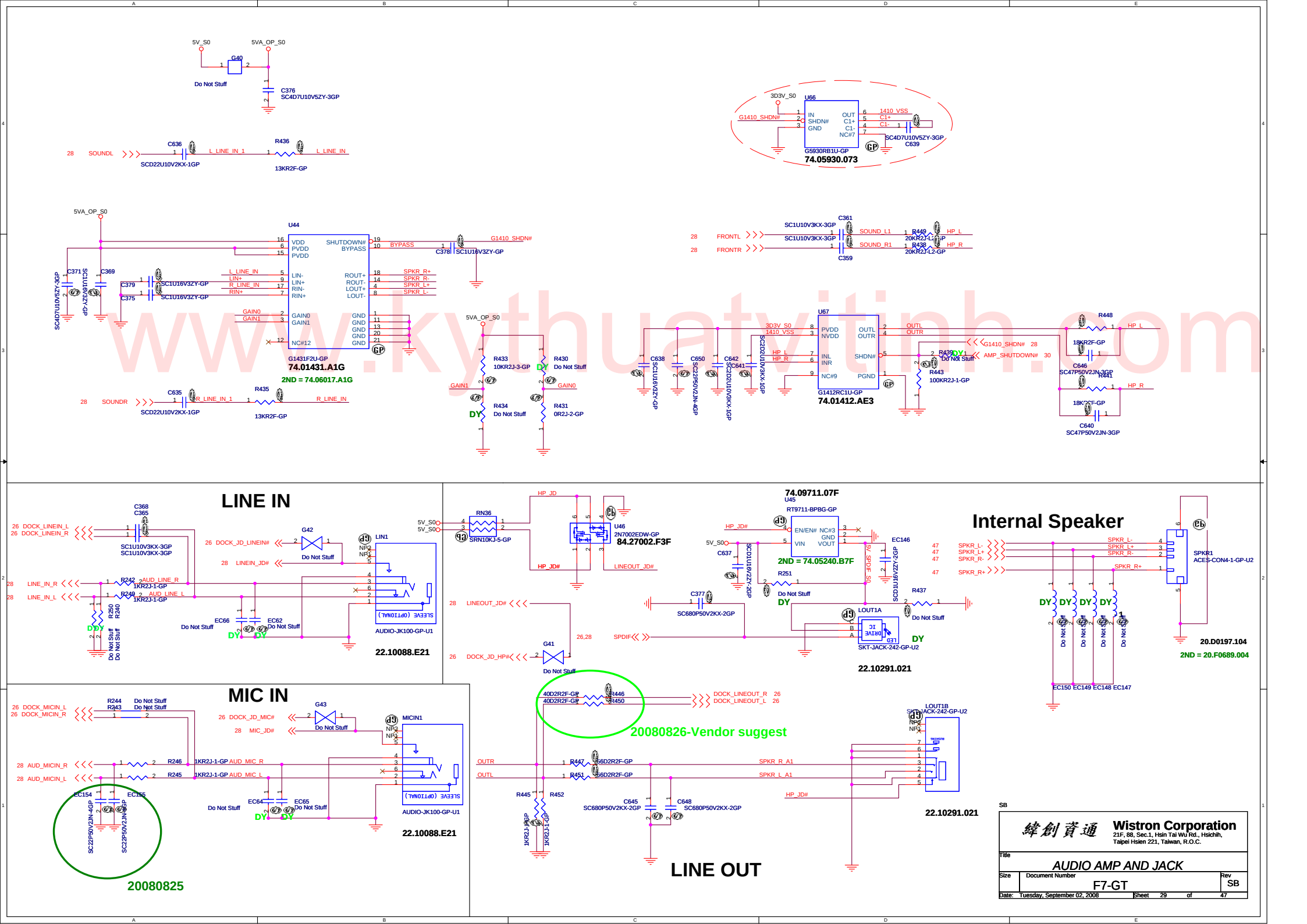
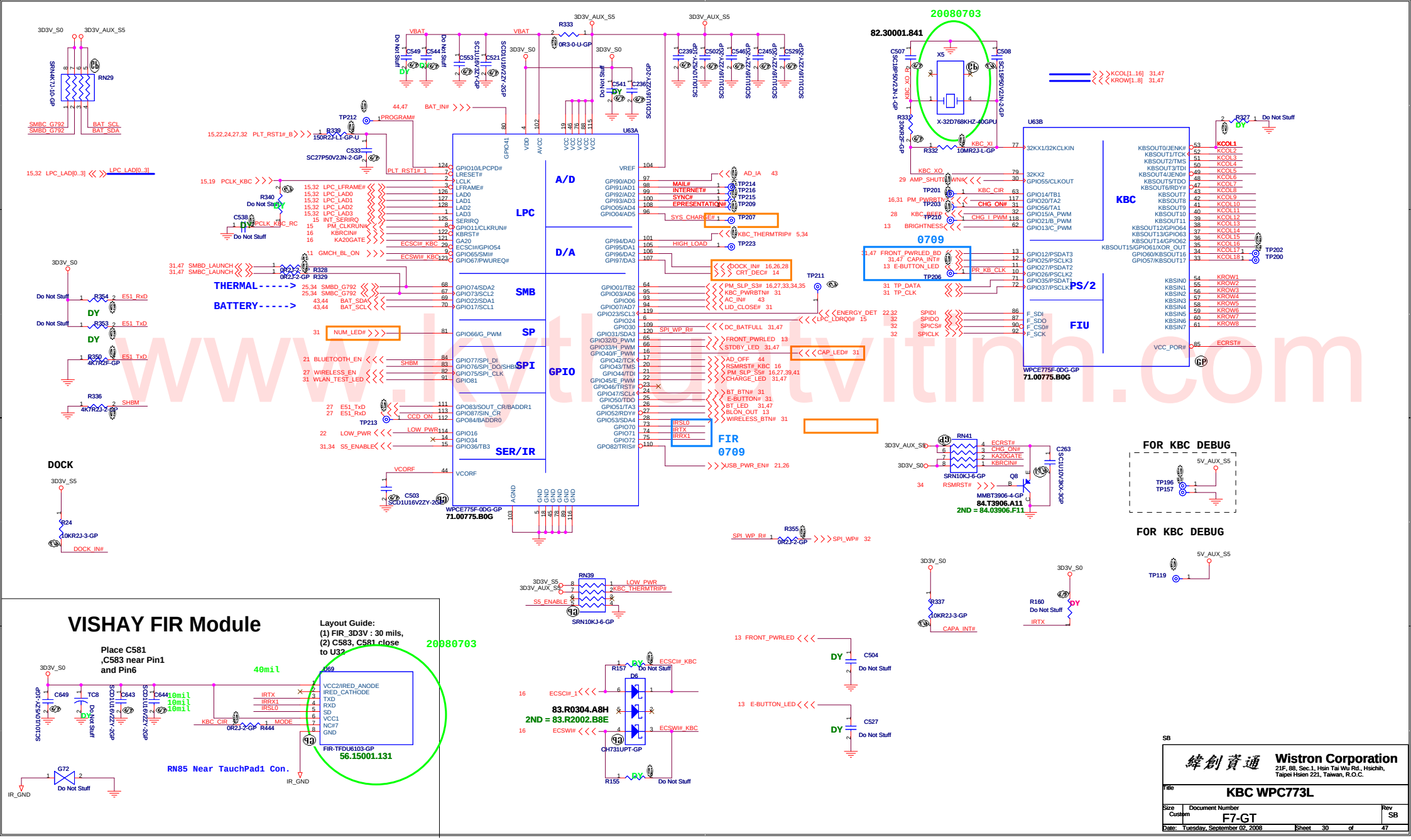
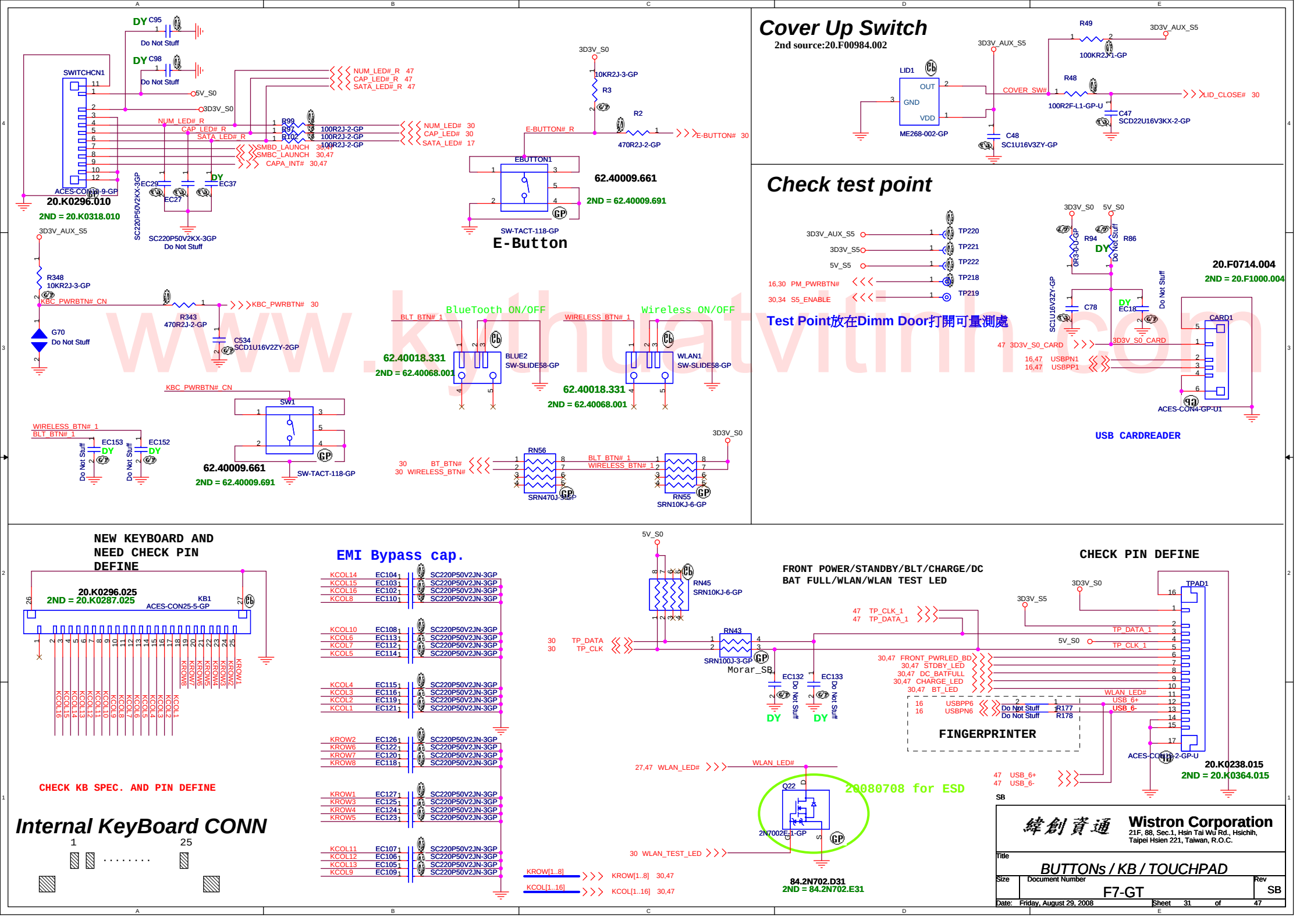
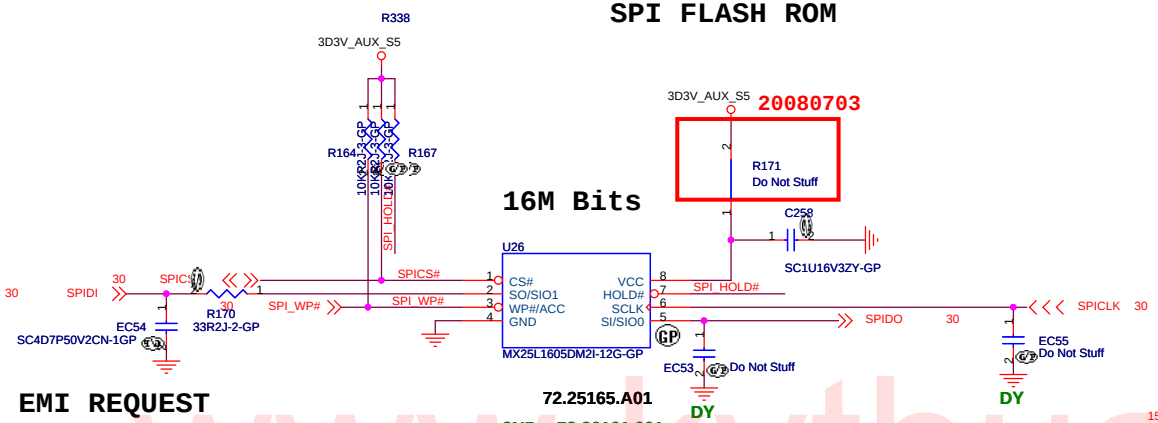






SPI FLASH ROM



EMI REQUEST

72.25165.A01

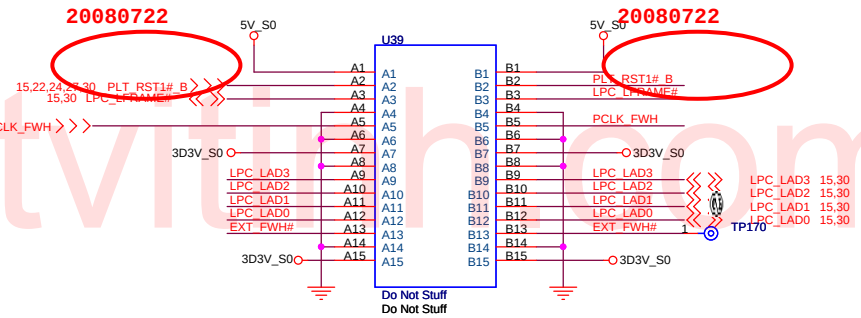
2ND = 72.26161.001

TOP VIEW

A15 (B1)
A14 (B2)
⋮ ⋮
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



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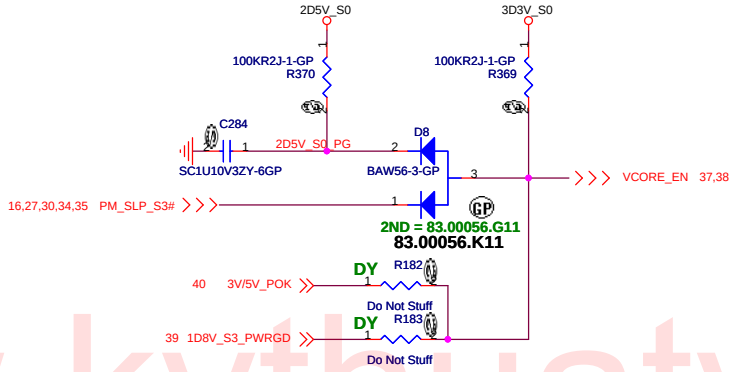
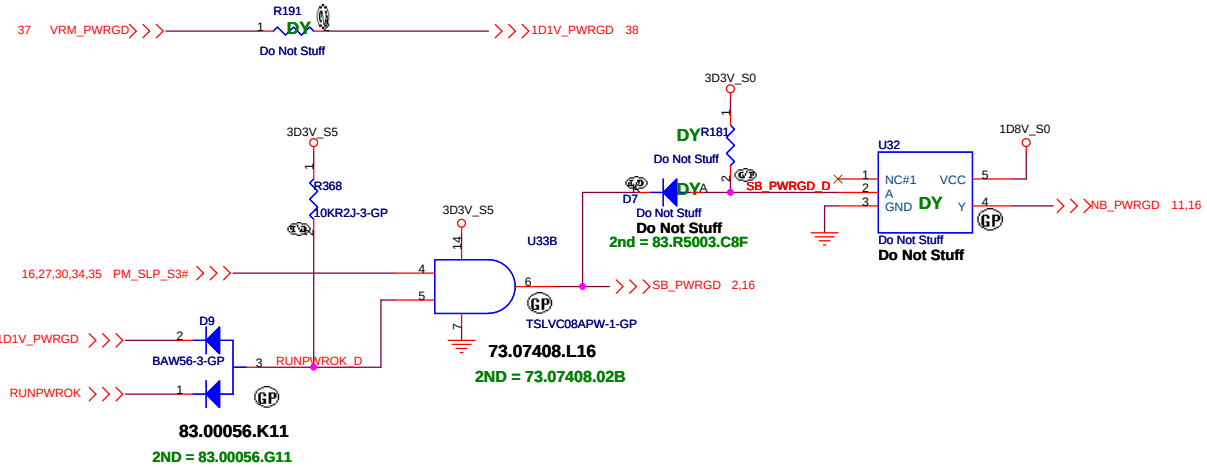
Title: BIOS

Size	Document Number	Rev
A3	F7-GT	SB

Date: Friday, August 29, 2008 Sheet 32 of 47



P/H @ 1D8V_S3 PAGE



SB

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWERGOOD&ENABLES***

Size	Document Number	Rev
A3	F7-GT	SB

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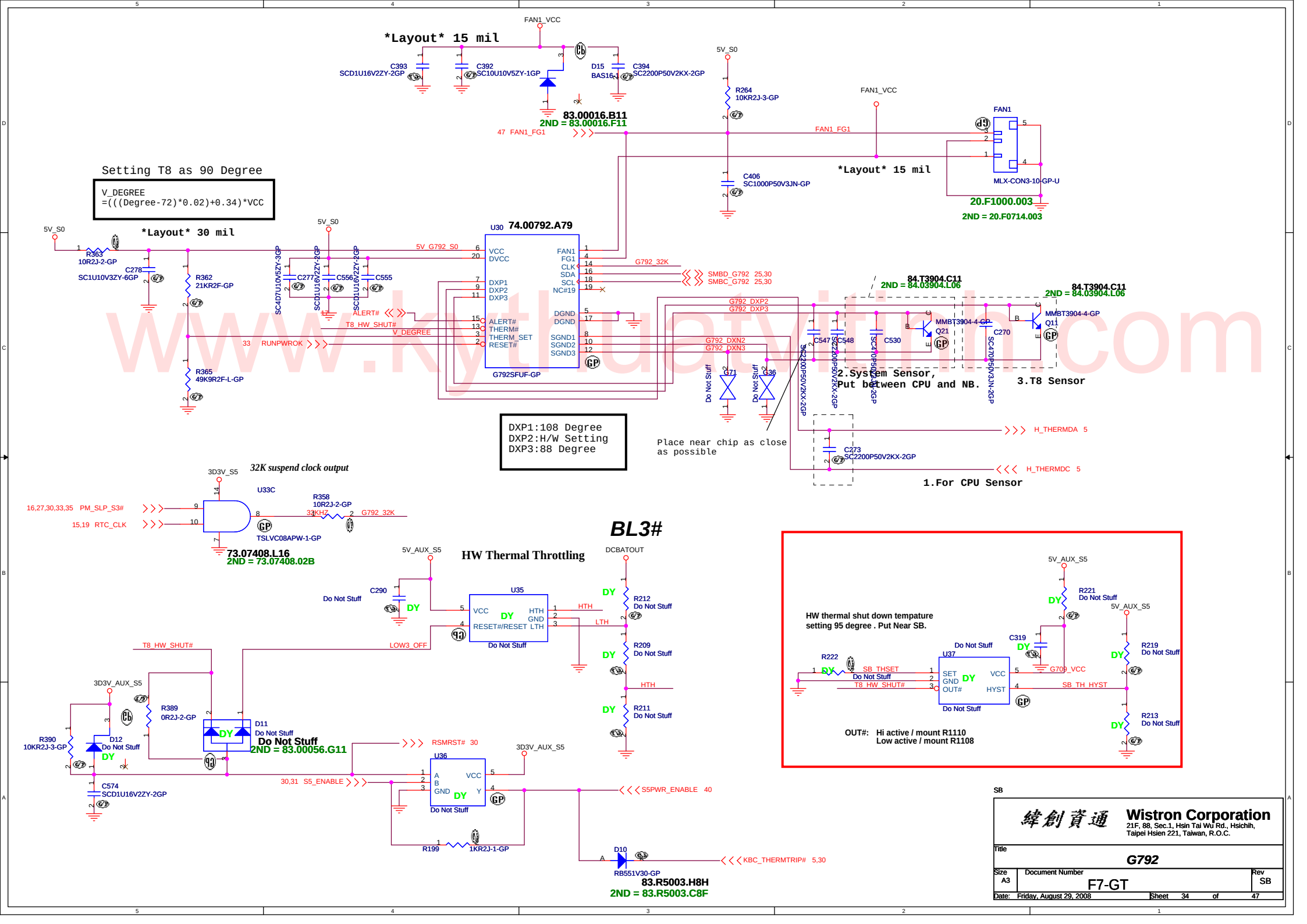

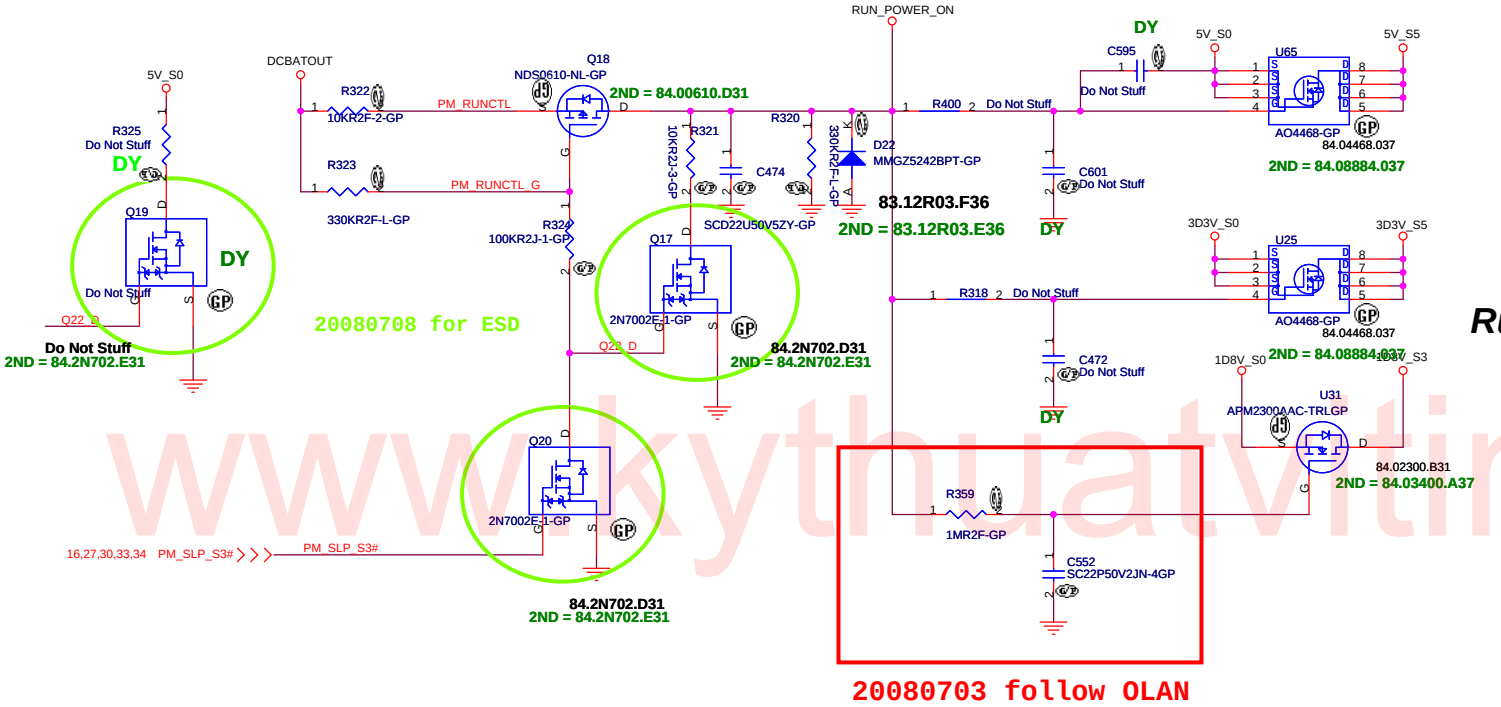

Run Power

SB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***PWR CTL LOGIC / PWR PLANE***
Size: A3	Document Number: F7-GT
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Date: Friday, August 29, 2008	Sheet 35 of 47

CPU_CORE
ISL6264CRZ

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TI TPS51120
3D3V/5V

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

DCBATOUT_51120

Input Power
VIN
REG5V_IN(I / 5V)

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

DCBATOUT_51120

2D5V_S0

3D3V_S0 — INPUT — OUT — 2D5V_S0

APL5913

1D8V_S5

3D3V_S5 — INPUT — OUT — 1D2V_S5

APL5332KAC-TRLGP

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal (I)
Input Power VCC(I) VCC(I)

Output Signal (O)
Output Power VCC(O)

AD_IN
AD+

Charger_ISL6255

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Input Power
DCIN (I)

AD+

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

Output Power
VCC (O)
VCC (O)

AD_IN
CHARGE_LED#
BL2#
DCBATOUT
BT+

TI TPS51116
1.8V / 0.9V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
VCC(I)
VCC(I)

DCBATOUT
5V_S5

Output Power
VCC(O)
VCC(O)

1.8V_S3
0.9V_S3

ISL6268_1D2V

1D2V_S0_EN
5V_S5
DCBATOUT

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Input Power
VCC
VIN

Output Power
1D2V_PWR

1D2V (6.5A)

ISL6268_VGA_CORE

VGA_CORE_EN
5V_S5
DCBATOUT

Input Signal
SS_STBY1(I / 5V) FOR 1.2V

Input Power
VCC
VIN

Output Power
1D2V_PWR

VGA_CORE_S0 (15A)

SB

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

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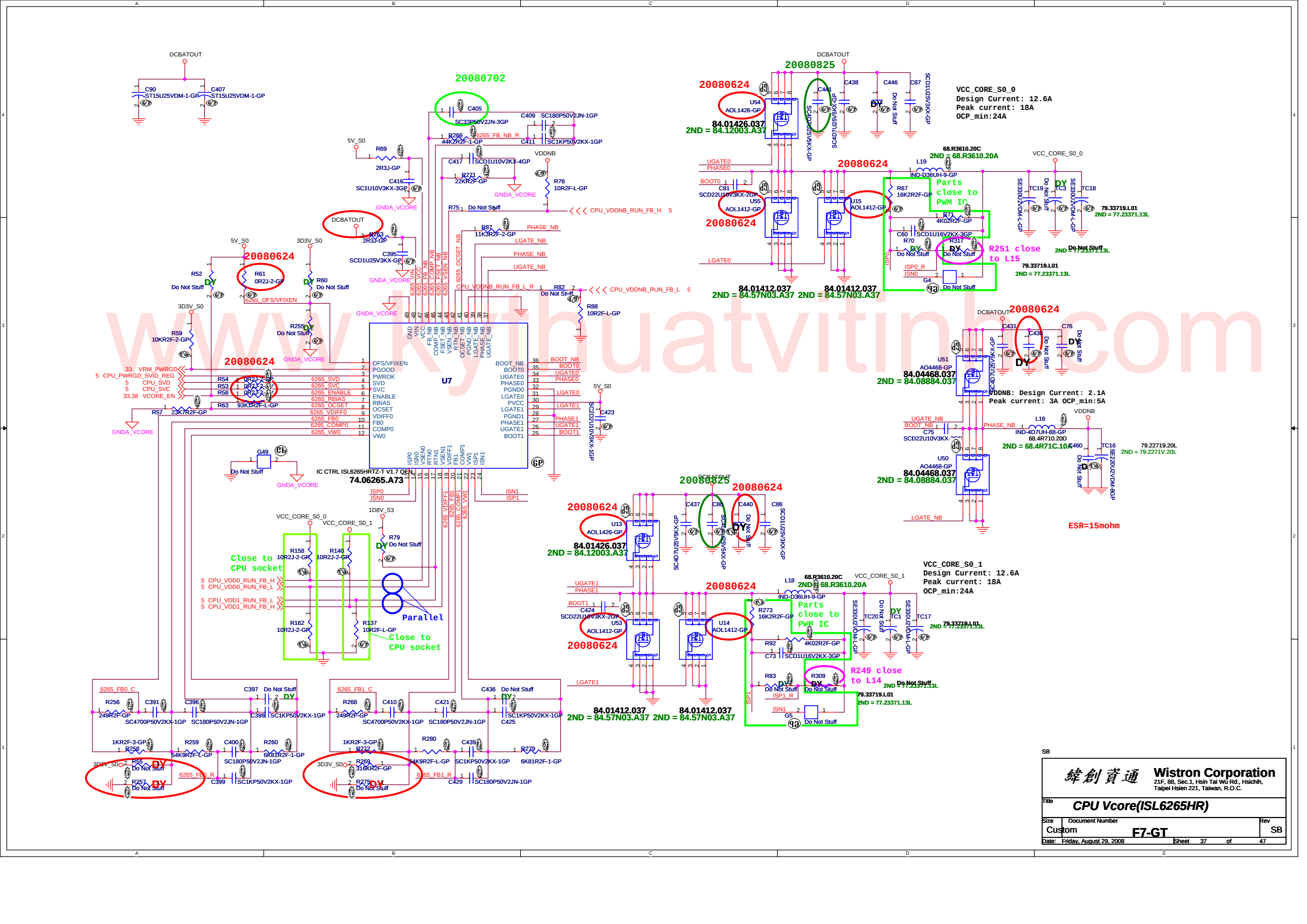
Date: Tuesday, August 19, 2008 | Sheet 36 of 47


20080702
20080825
20080624
U7
IC CTRL ISL6265HRTZ-T V1.7 QFN
74.06265.A73
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
Close to CPU socket
Parallel
Close to CPU socket
Parts close to PWM IC
R251 close to L15
R249 close to L14
ESR=15mohm
84.01426.037
84.12003.A37
84.01412.037
84.57N03.A37
84.04468.037
84.08884.037
79.33719.L01
79.22719.20L
79.22271V.20L
77.23371.13L
68.R3610.20C
68.4R710.20D
68.4R71C.10A
Wistron Corporation
21F., 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
Custom
F7-GT
SB
Friday, August 29, 2008
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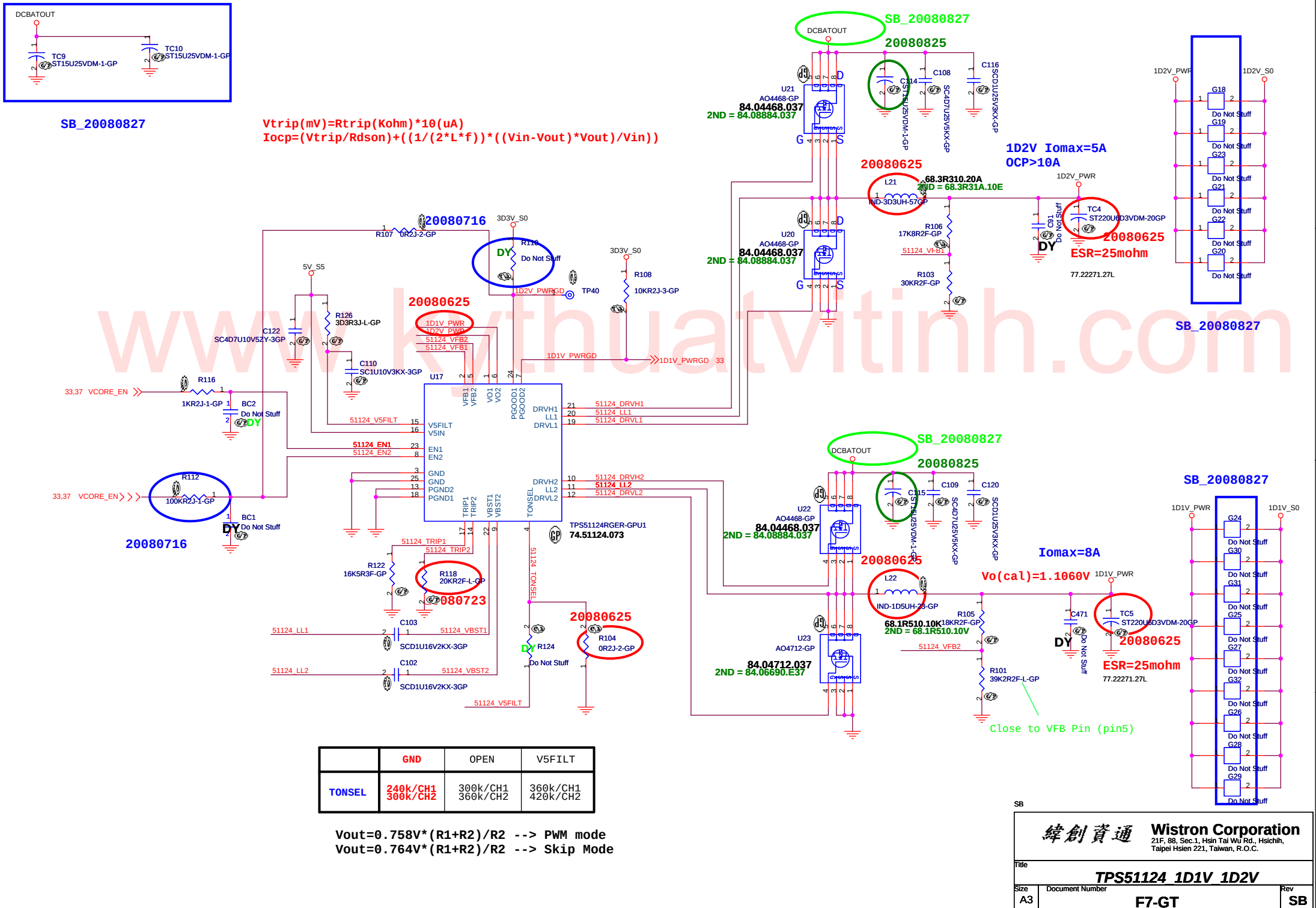

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

SB

緯創資通 Wistron Corporation
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Title: TPS51124_1D1V_1D2V

Size	Document Number	Rev
A3	F7-GT	SB

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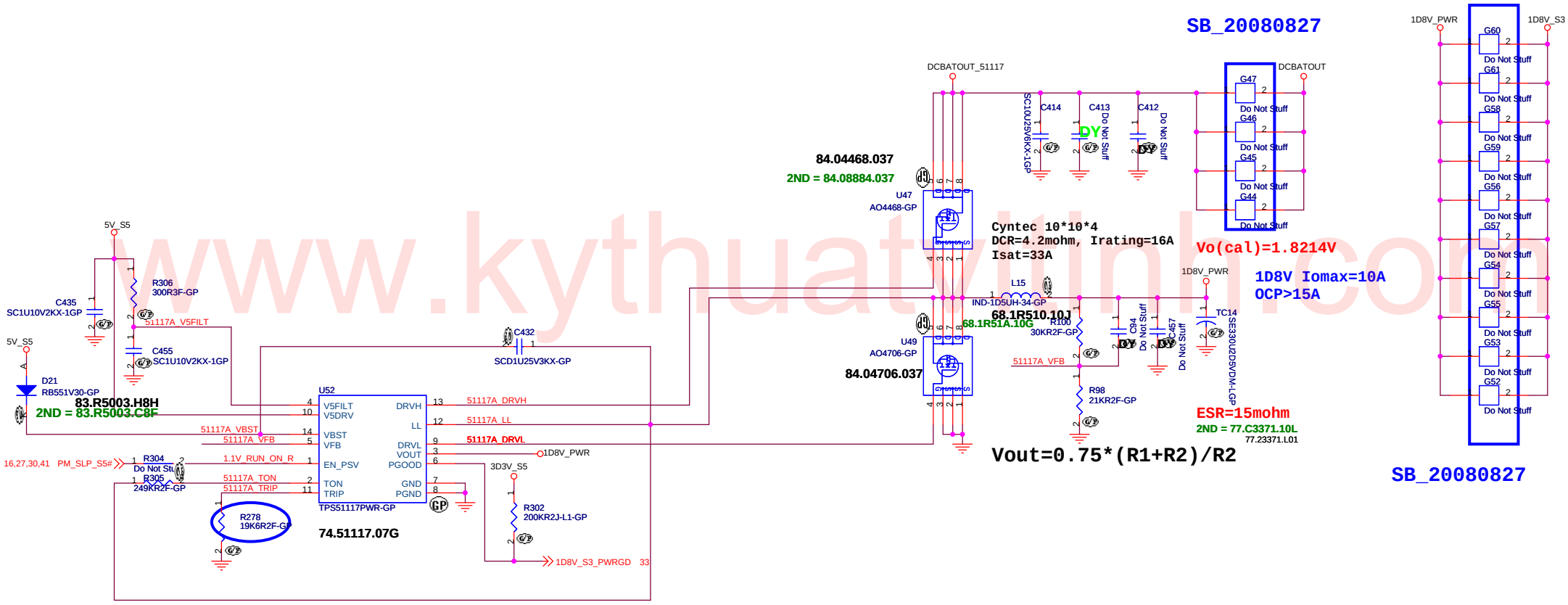

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Title: 1D8V(TPS5117)

Size	Document Number	Rev
A3	F7-GT	SB

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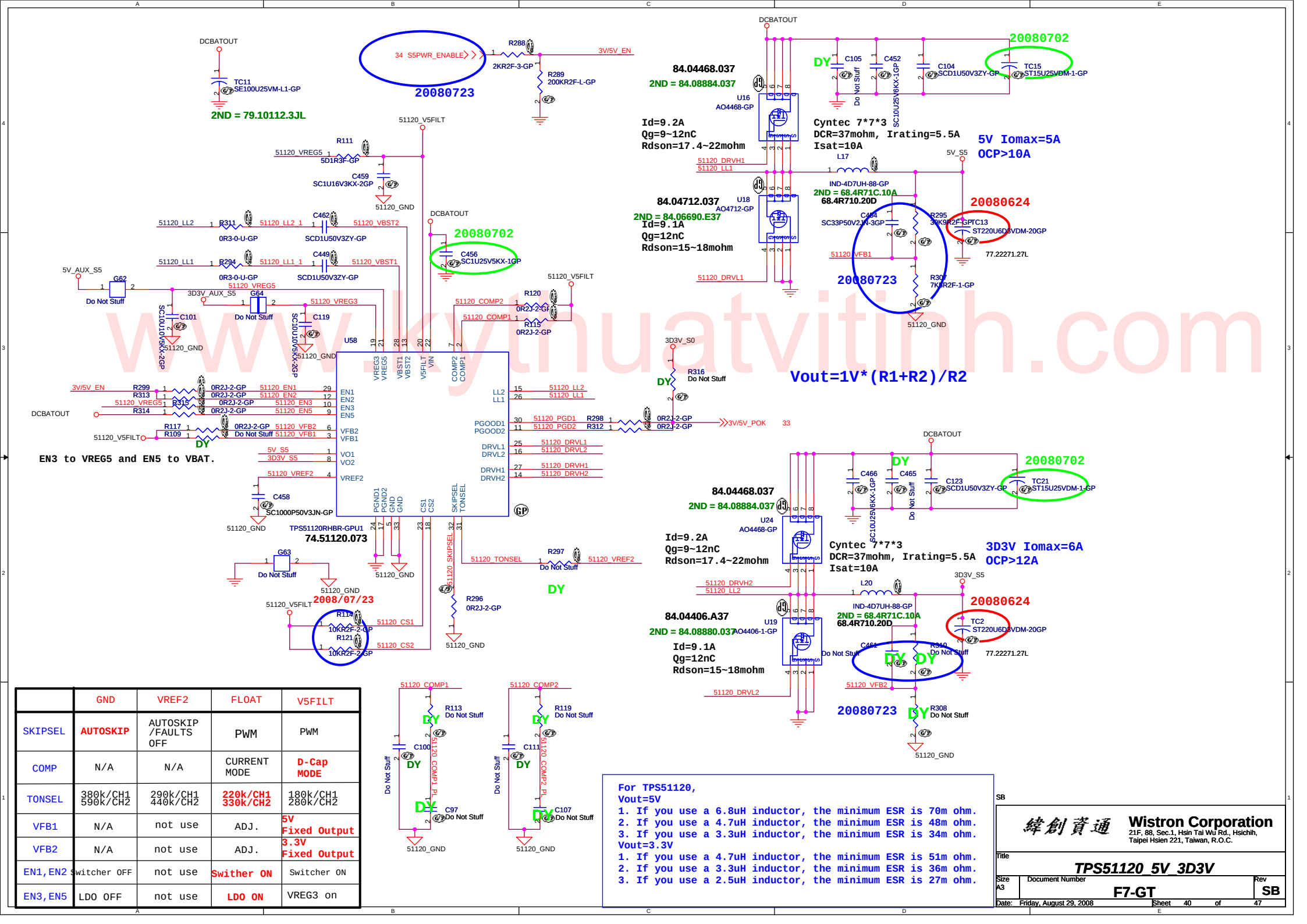

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swither ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

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Title: TPS51120_5V_3D3V

Size: A3 | Document Number: F7-GT | Rev: SB

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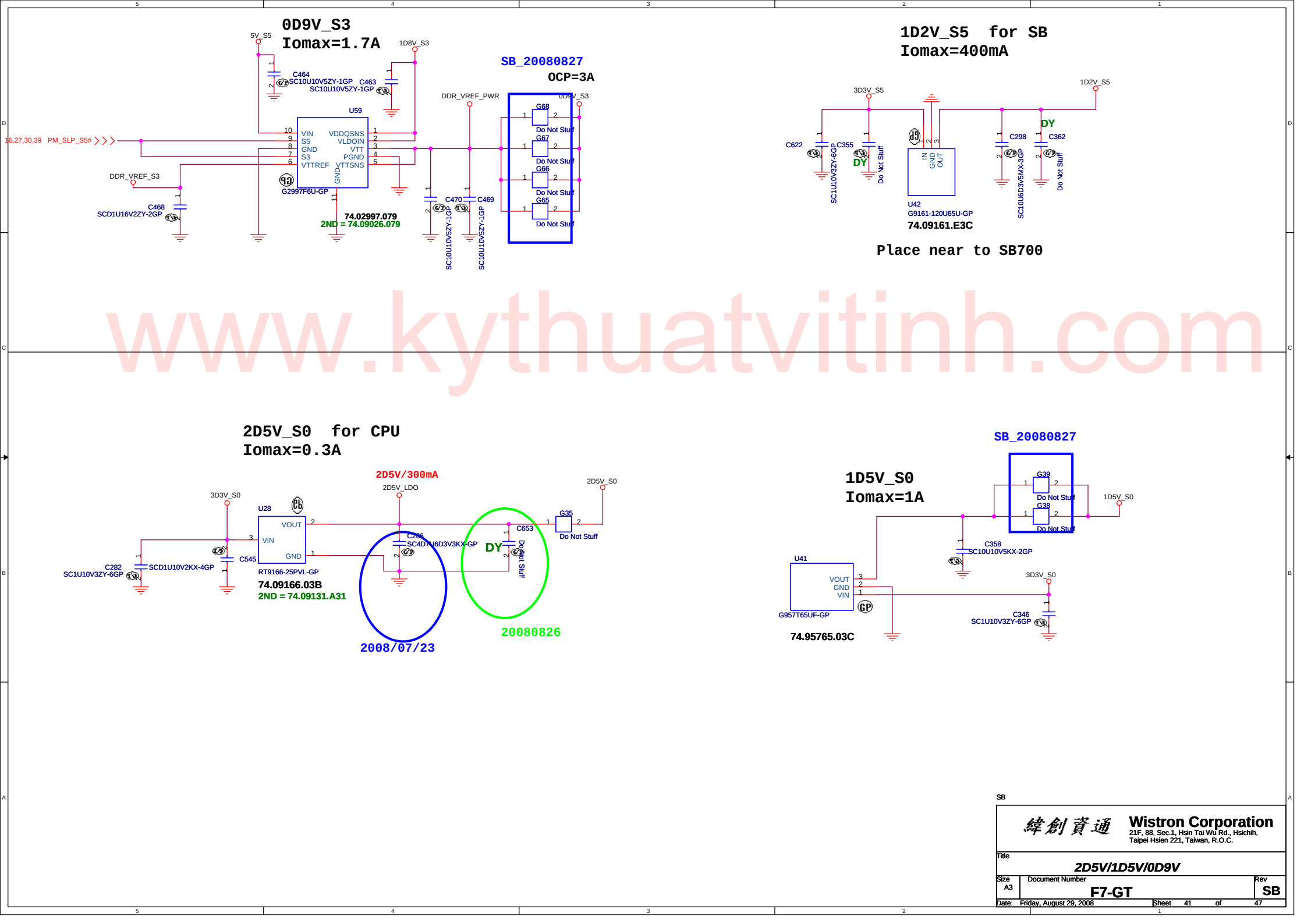

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Title: 2D5V/1D5V/0D9V

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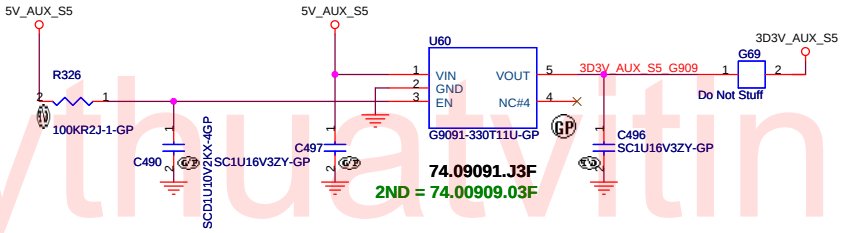
Aux Power 3D3V_AUX_S5



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Title: ***3D3V_AUX***

Size	Document Number	Rev
A3	F7-GT	SB

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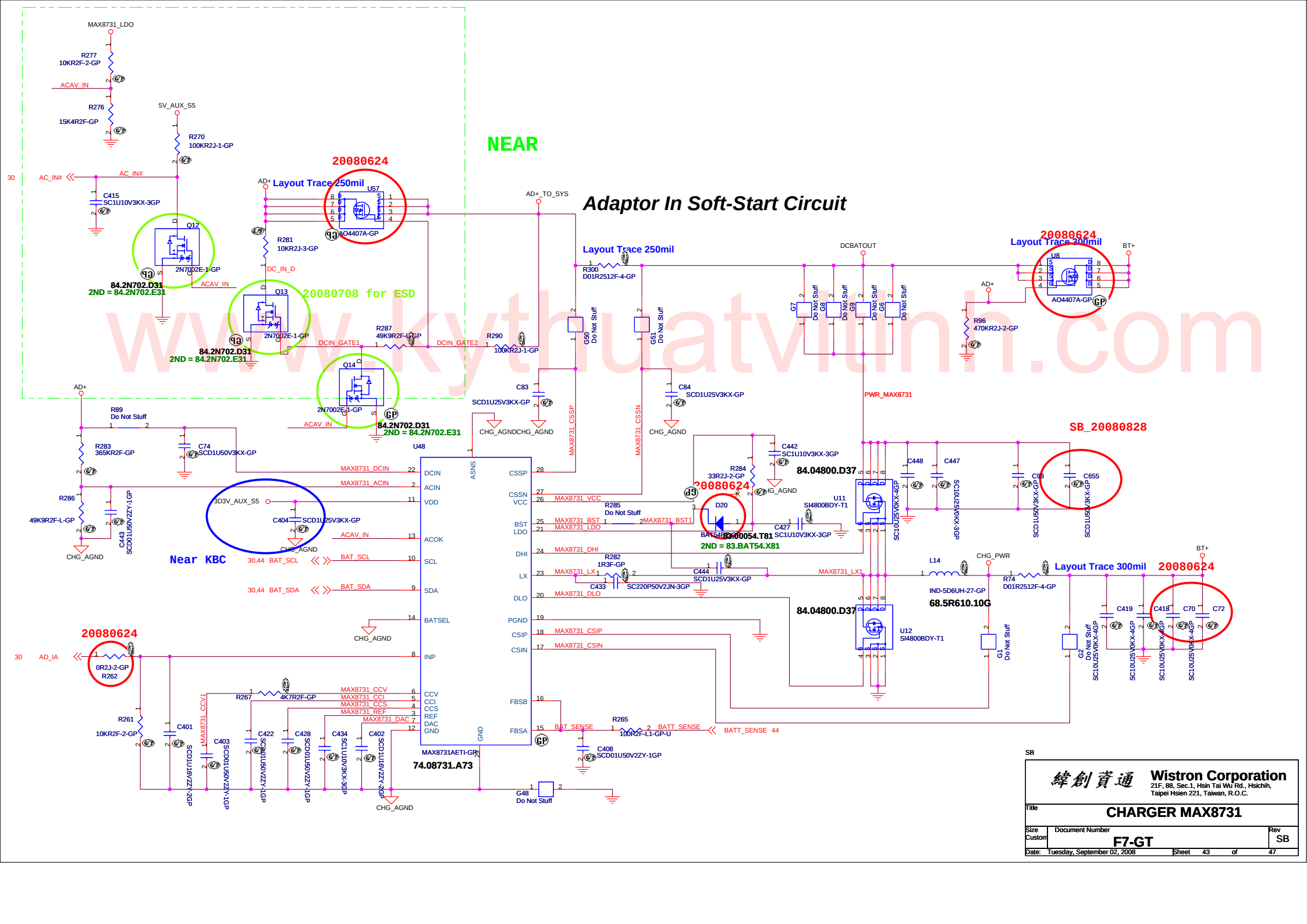
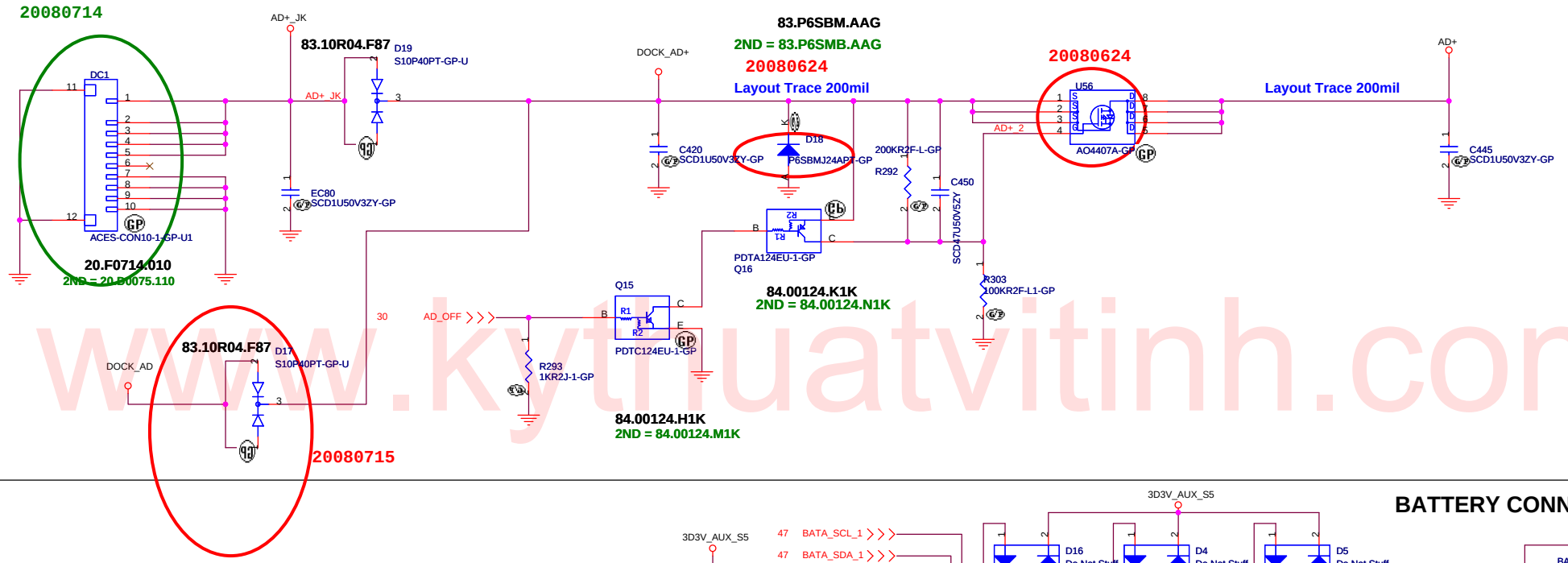
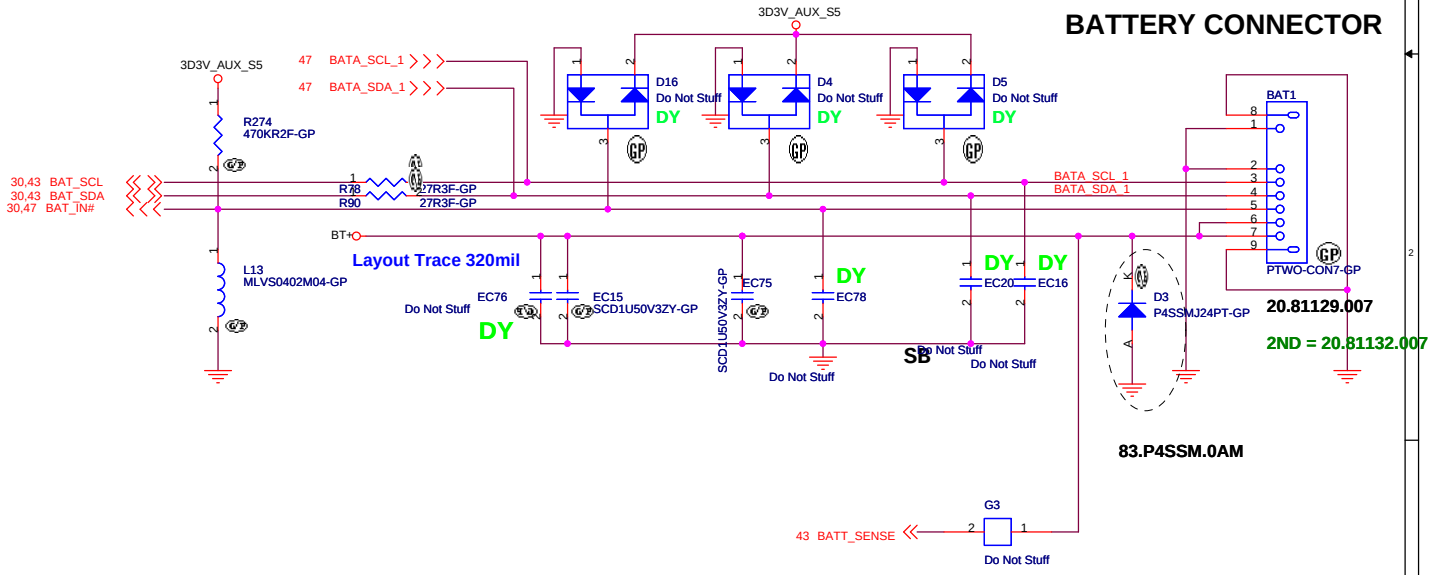


Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title	**AD/BATT CONN**	
Size A3	Document Number **F7-GT**	Rev **SB**
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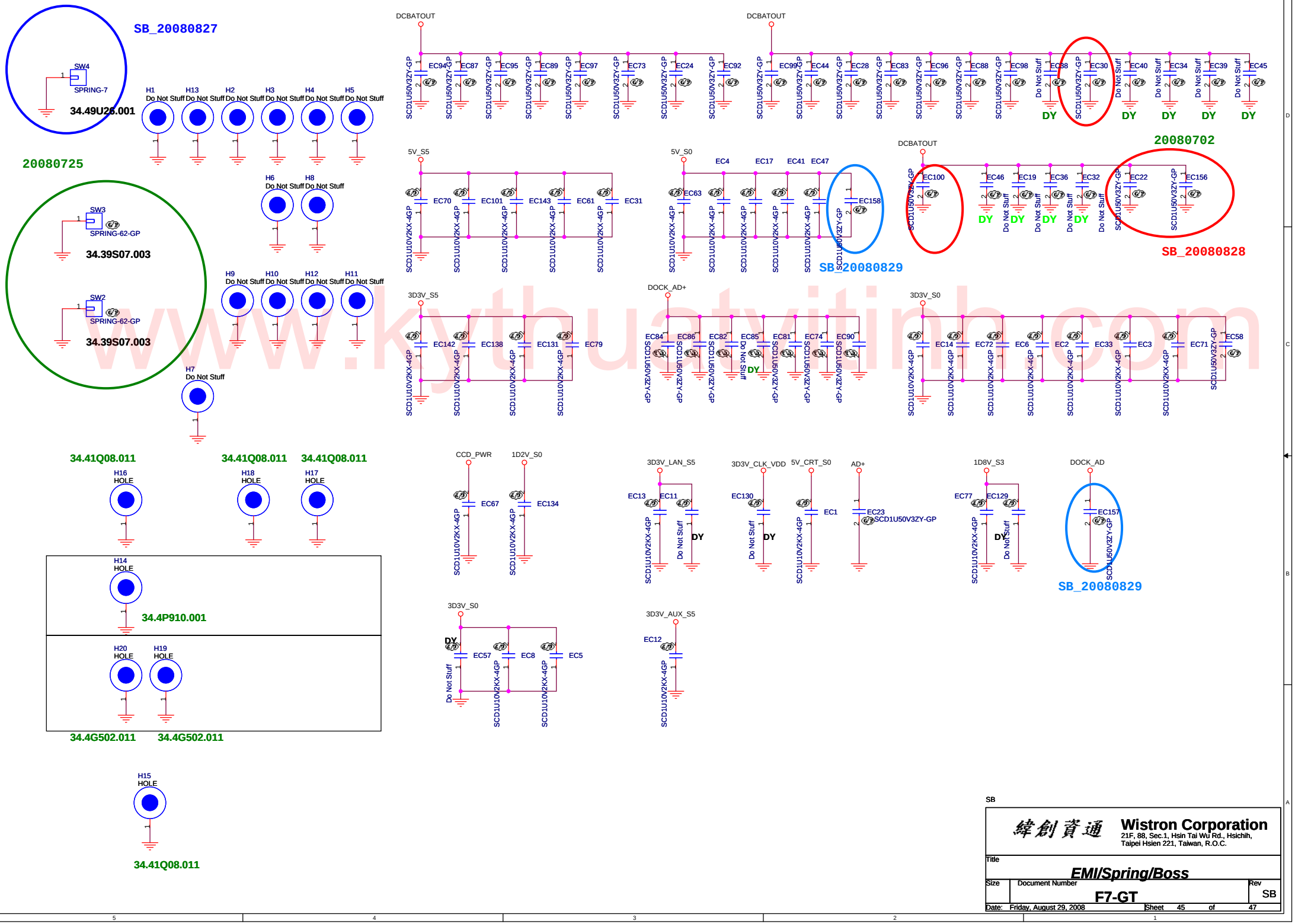

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Title	Change List
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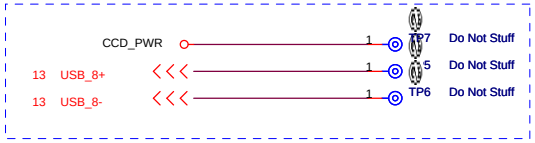
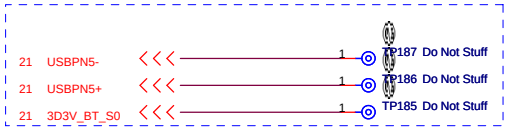
Date: Tuesday, August 19, 2008	Sheet 46 of 47

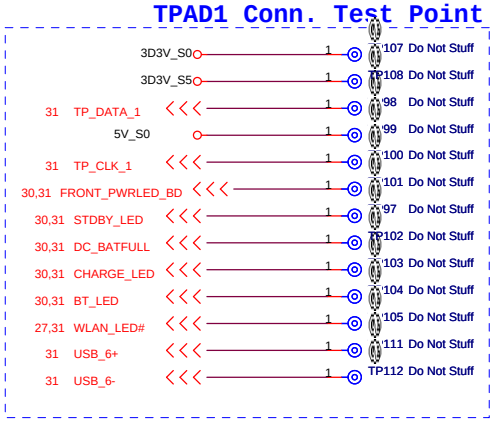
CCD Test Point



BT Conn. Test Point

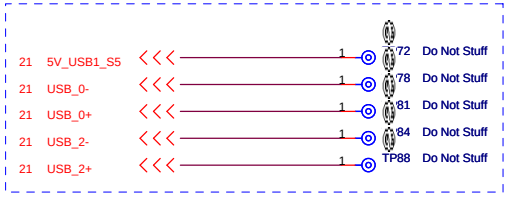


TPAD1 Conn. Test Point

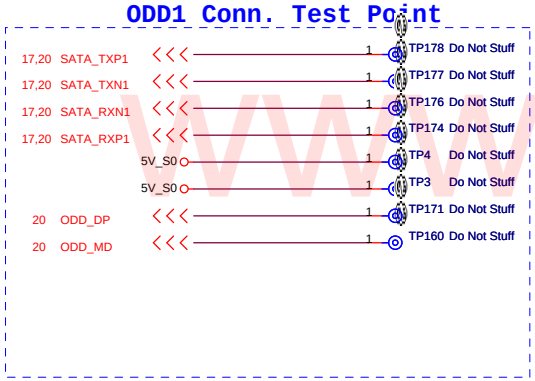


RTC1 CN Test Point

USB Conn2. Test Point

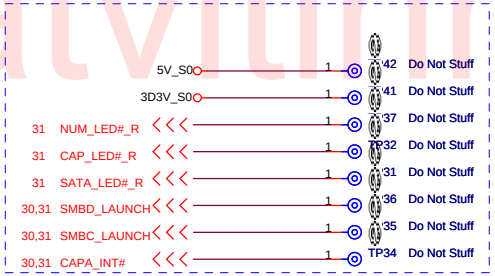


ODD1 Conn. Test Point

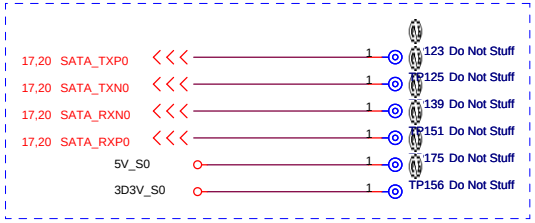


USB Conn1. Test Point

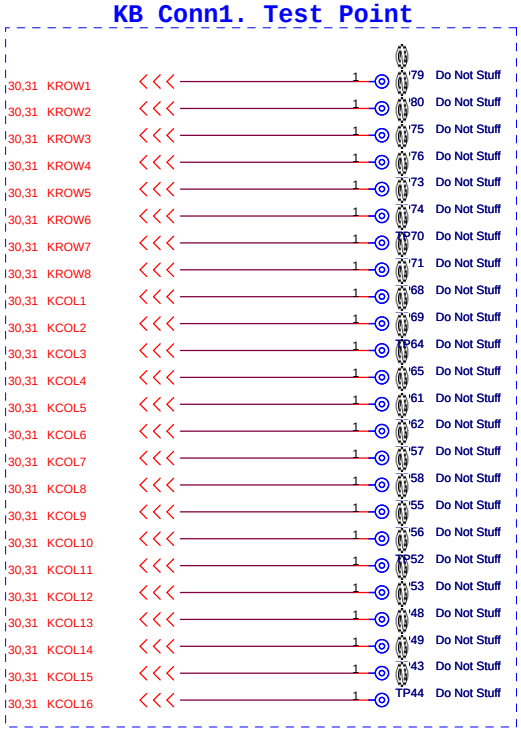
SWITCH Conn. Test Point



HDD Conn. Test Point



KB Conn1. Test Point



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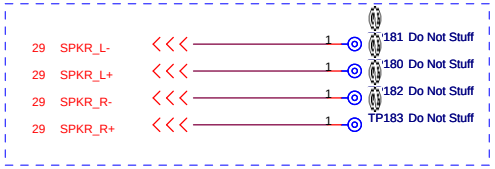

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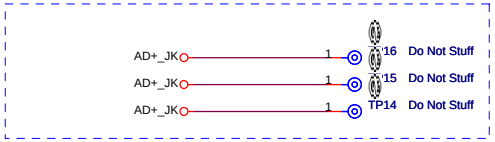
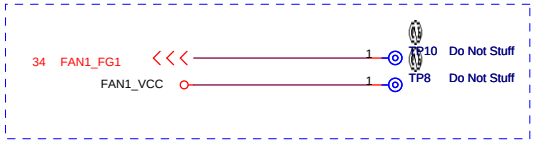
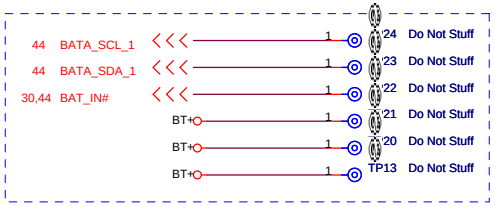


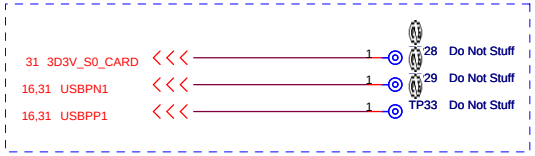
FAN1 Conn. Test Point



BAT1 Conn. Test Point



CARD1 Conn. Test Point



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