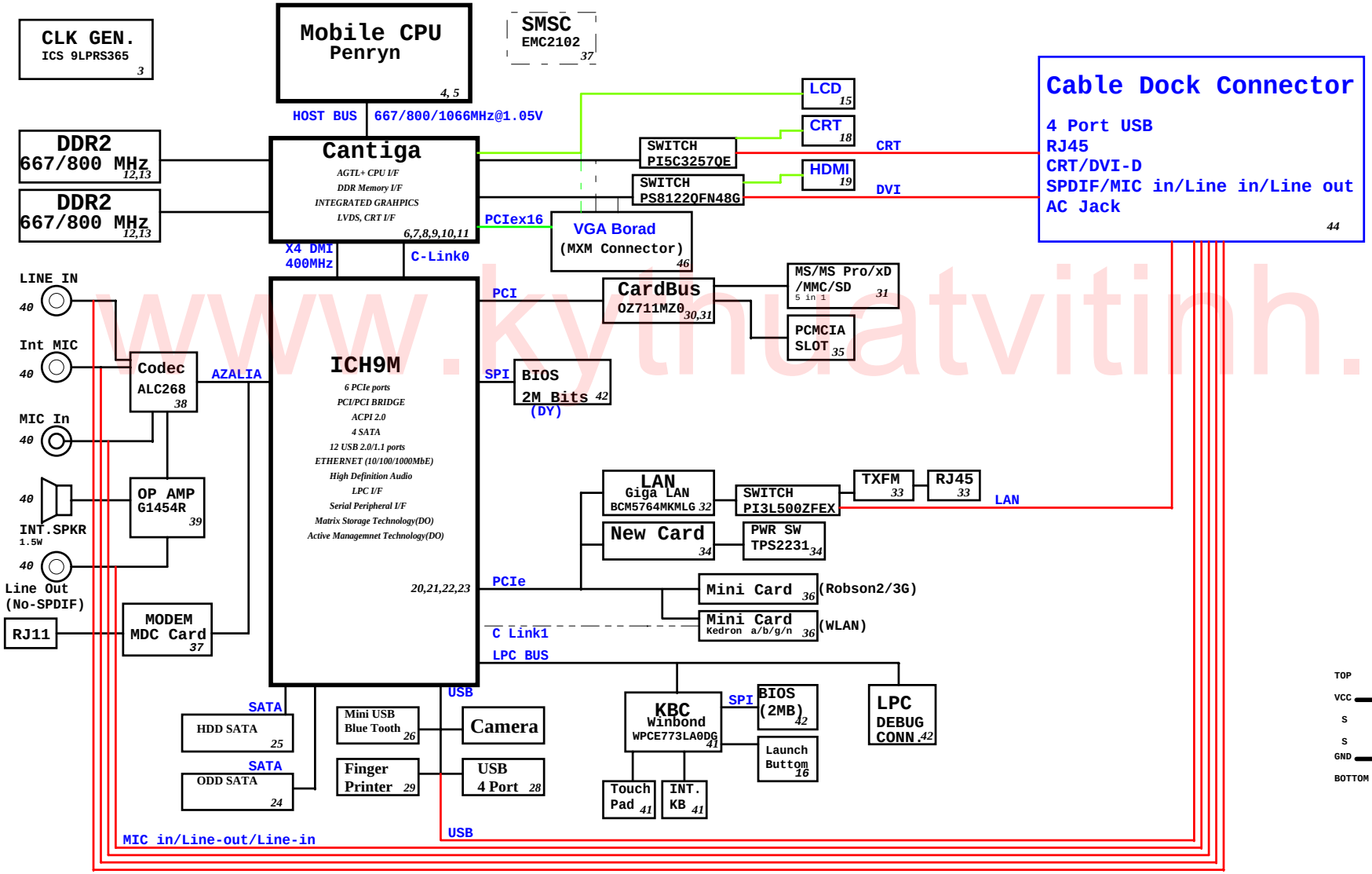
HOMA 3G Block Diagram

Project code: 91.41601.001
PCB P/N : 48.4I601.011
REVISION : -1 08204



SYSTEM DC/DC TPS51125 50

INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 51

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(16A) 1D8V_S3(16A)

RT9026 52

1.8V_S3	DDR_VREF_S3 (1.2A)

G9131 52

3D3V_S0	2D5V_S0 (300mA)

RT9018 52

1D8V_S3	1D5V_S0 (2.5A)

CHARGER BQ24754 54

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ISL6266A 49

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 38A

GFX DC/DC ISL6263 53

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0~1.3V 6.5A

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

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Title: BLOCK DIAGRAM
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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

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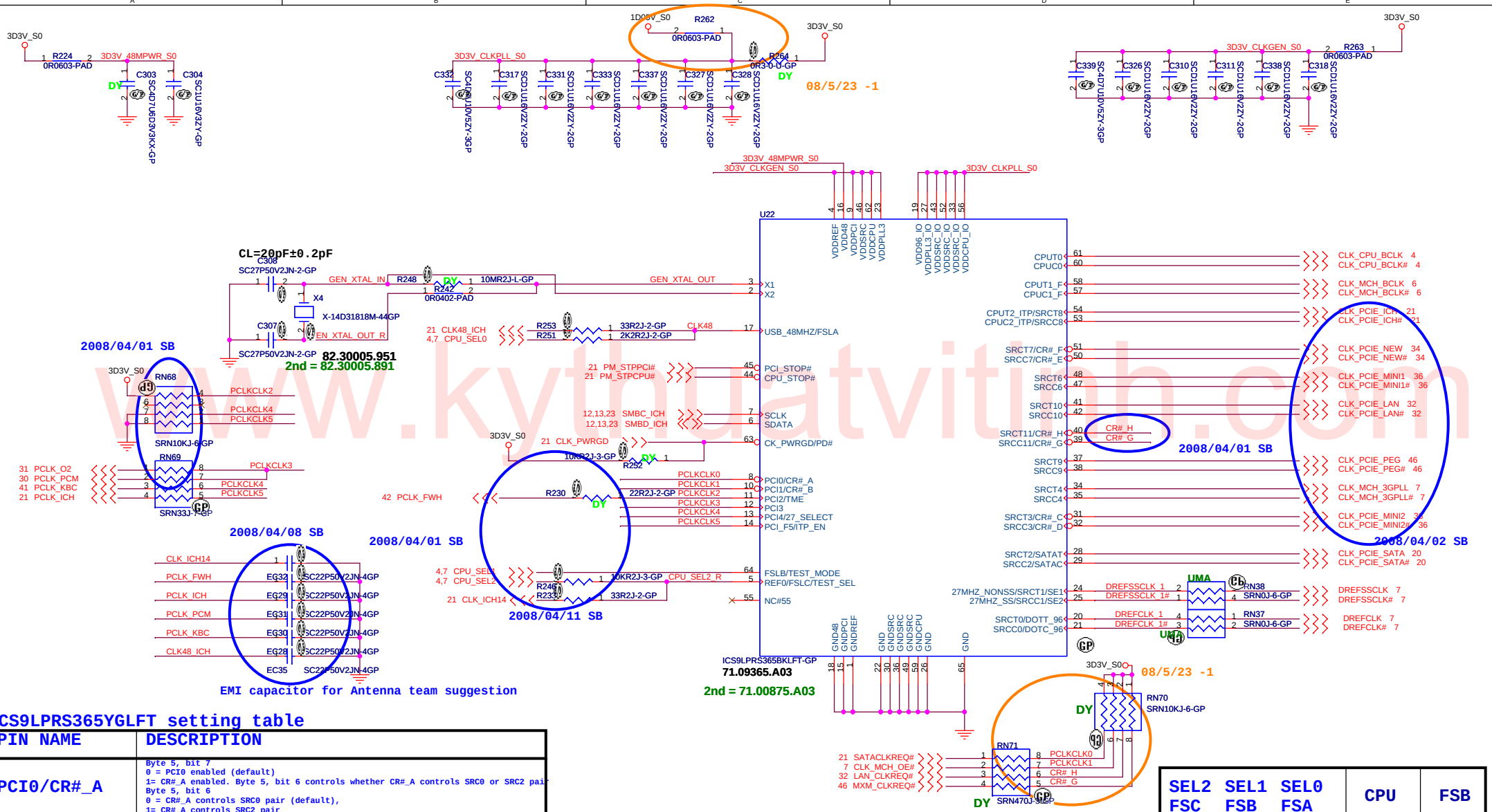

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: Clock Generator

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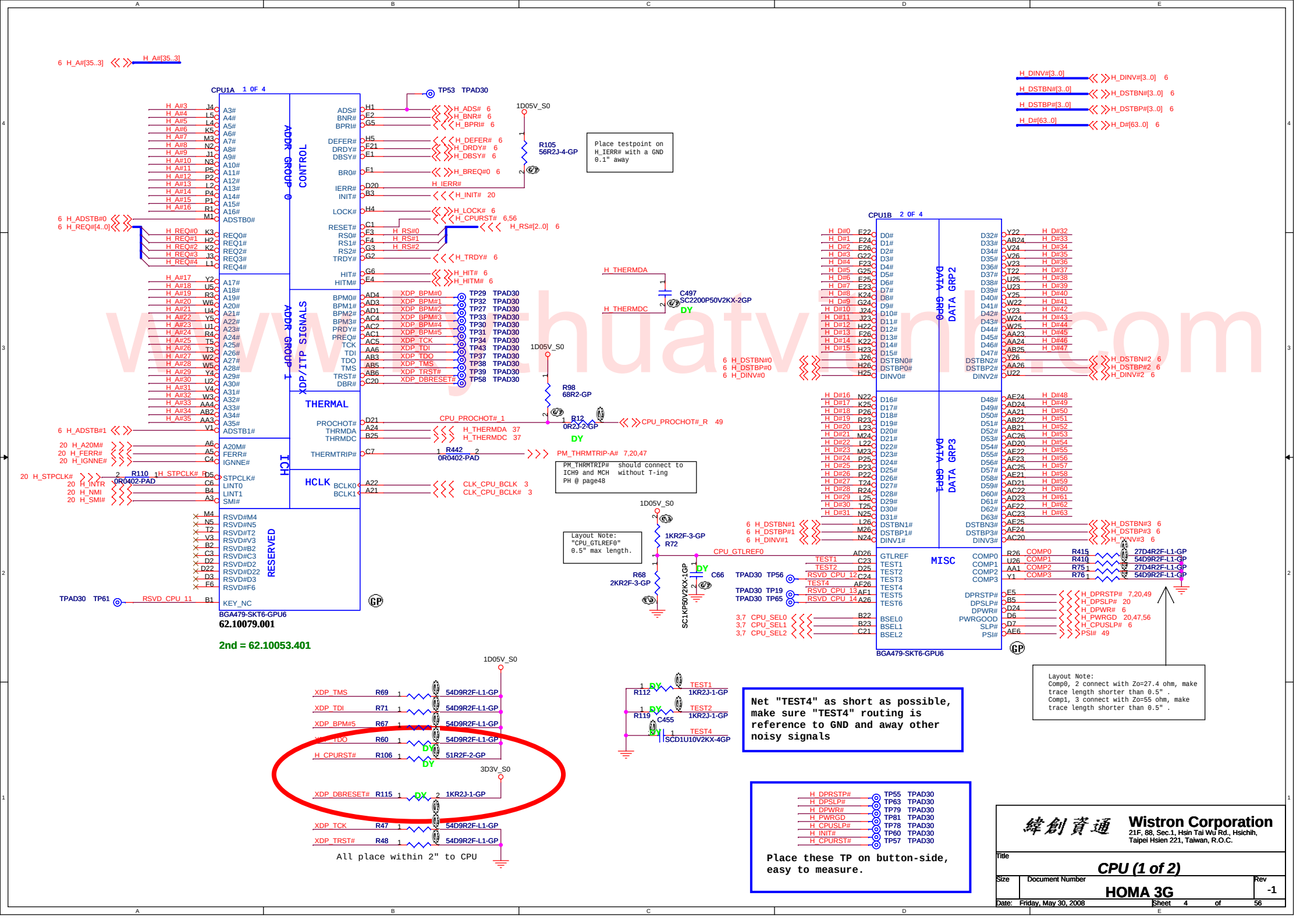
CPU1A 1 0F 4
BGA479-SKT6-GPU6
62.10079.001
2nd = 62.10053.401
CPU1B 2 0F 4
BGA479-SKT6-GPU6
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
DATA GRP2
DATA GRP3
MISC
TP53 TPAD30
R105 56R2J-4-GP
R98 68R2-GP
R12 0R2J-2-GP
R442 0R0402-PAD
R110 0R0402-PAD
C497 SC2200P50V2KX-2GP
C66 SC1KP50V2KX-1GP
R72 1KR2F-3-GP
R68 2KR2F-3-GP
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48
Layout Note: "CPU_GTLREF0" 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
All place within 2" to CPU
Place these TP on button-side, easy to measure.
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Title
CPU (1 of 2)
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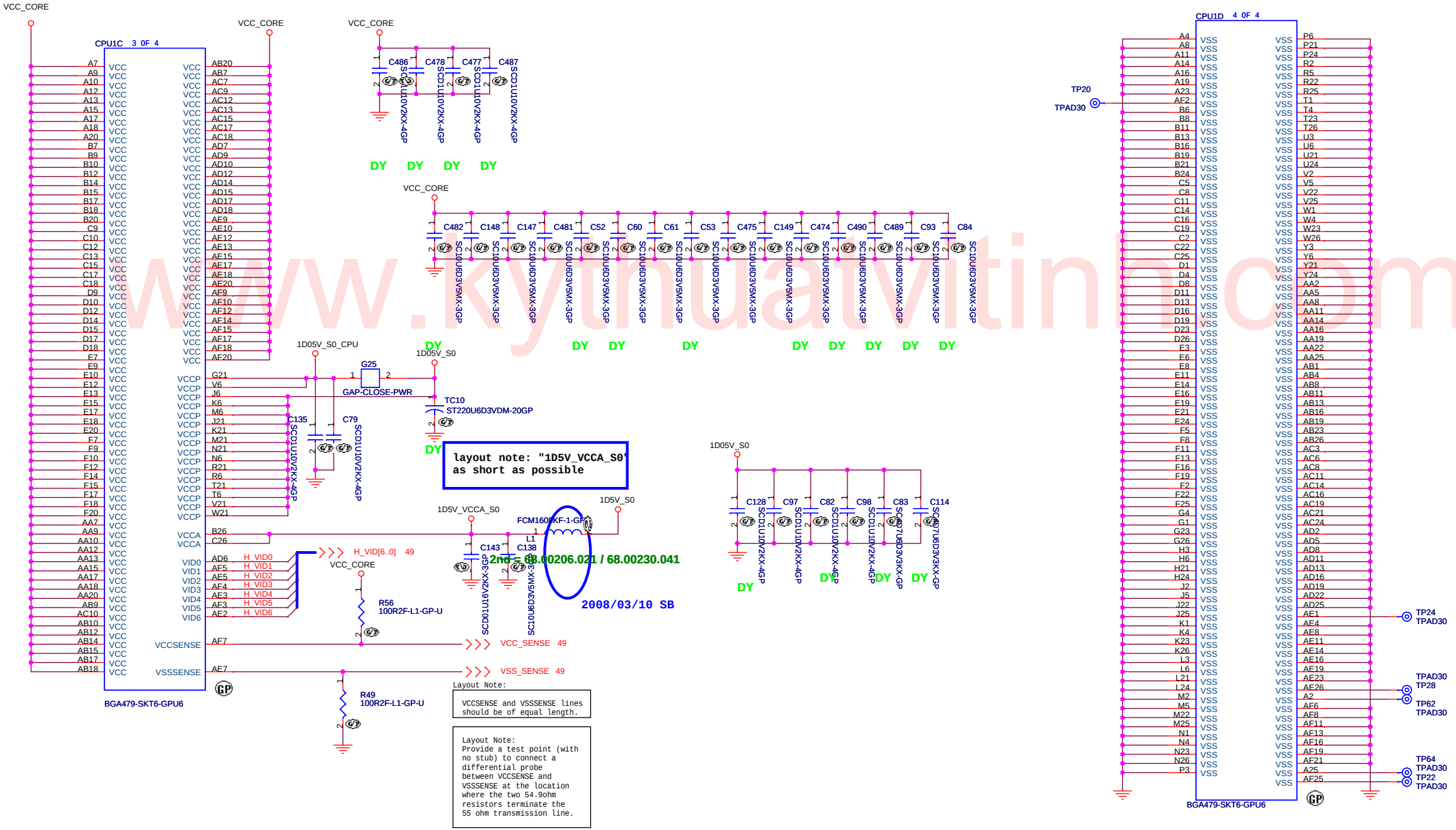

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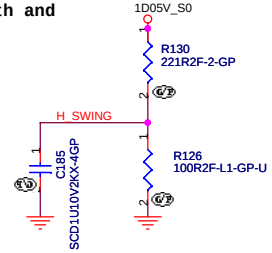
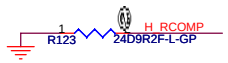
H_SWING routing Trace width and Spacing use 10 / 20 mil

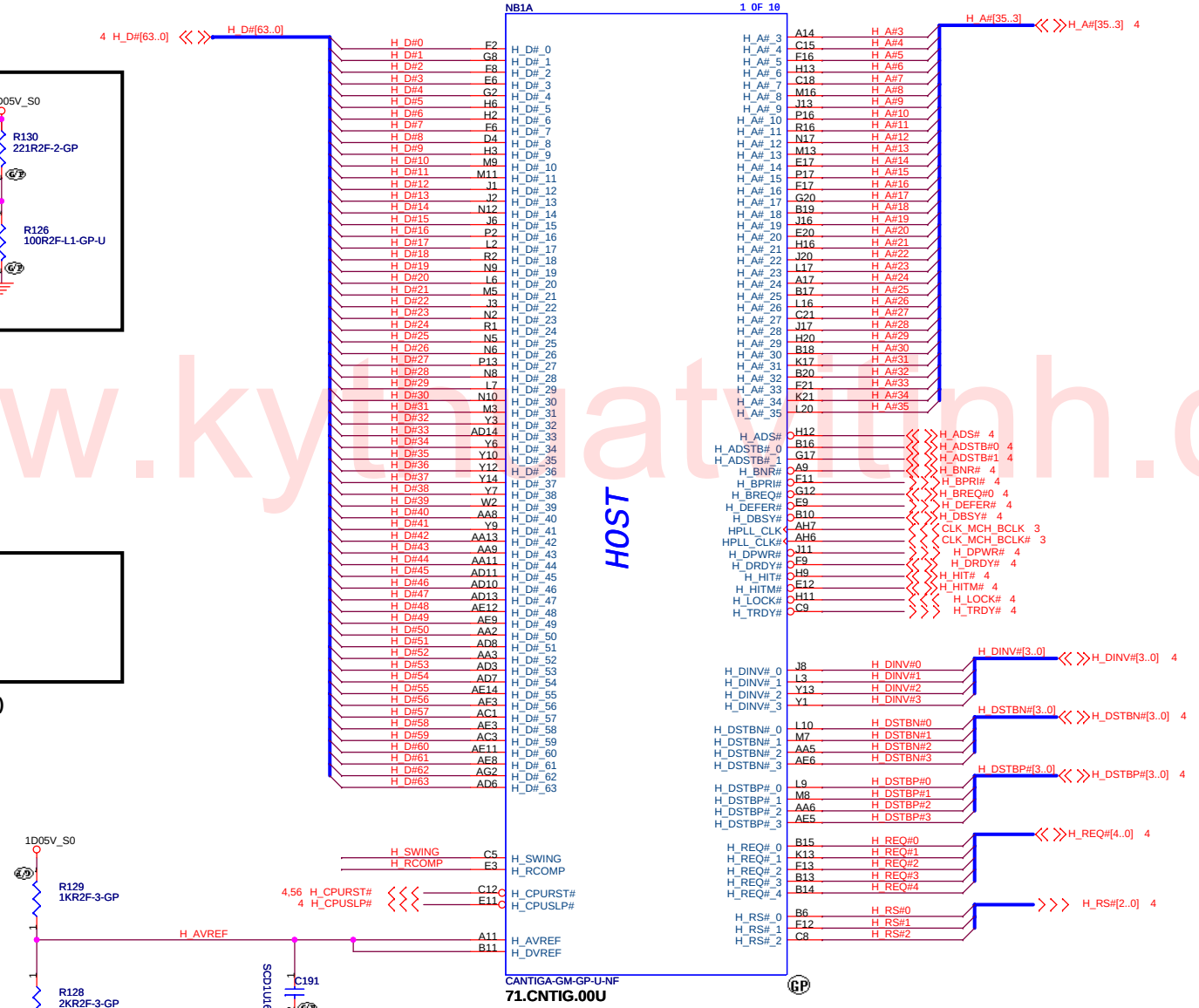
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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Title	Cantiga (1 of 6)	
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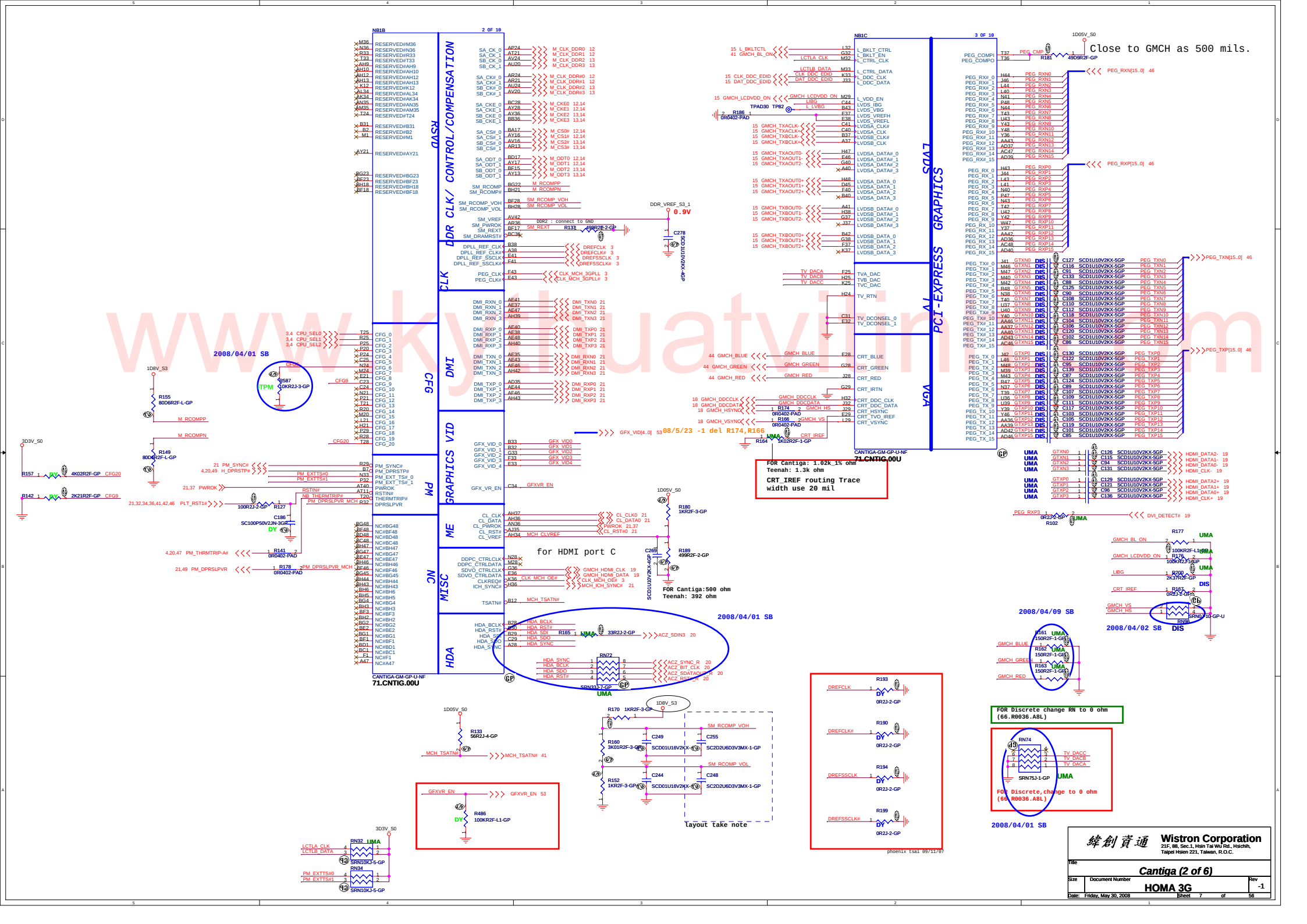
Close to GMCH as 500 mils.
2008/04/01 SB
for HDMI port C
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace
width use 20 mil
08/5/23 -1 del R174,R166
2008/04/09 SB
2008/04/02 SB
DIS
FOR Discrete change RN to 0 ohm
(66.R0036.A8L)
FOR Discrete,change to 0 ohm
(66.R0036.A8L)
2008/04/01 SB
layout take note
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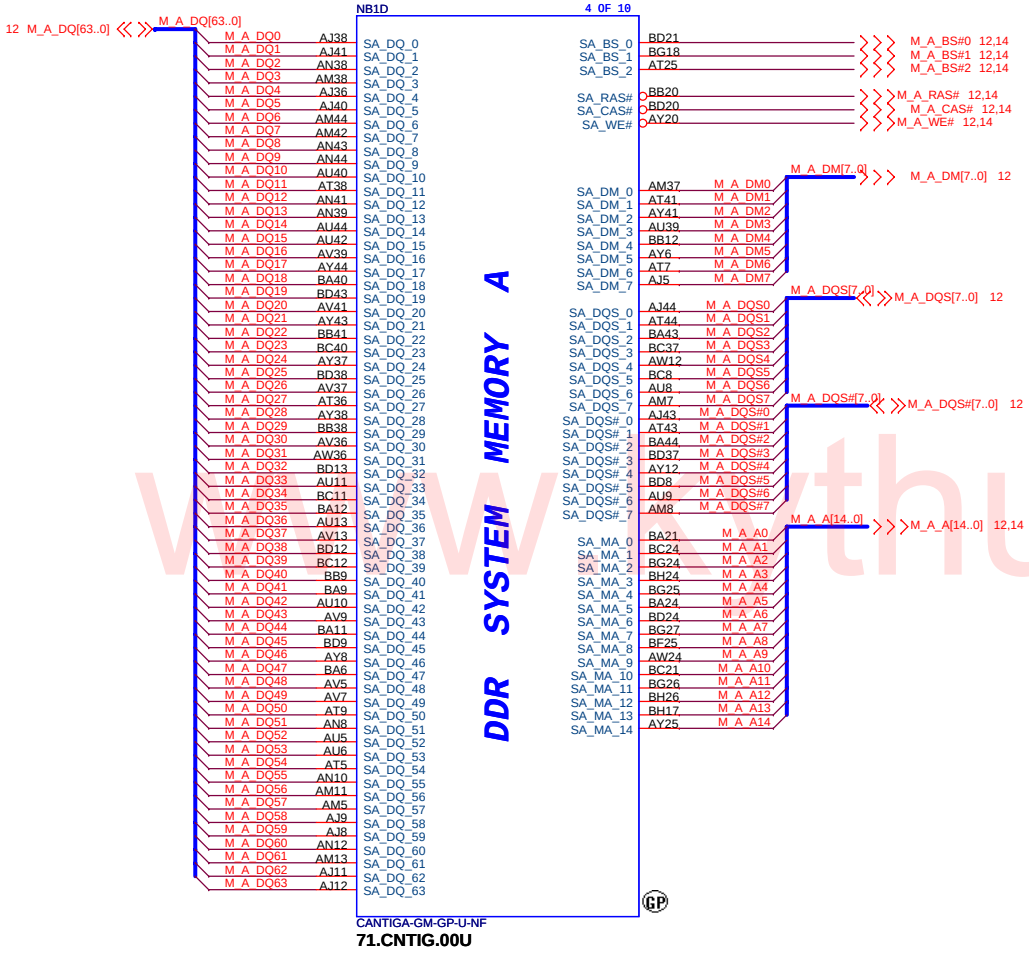

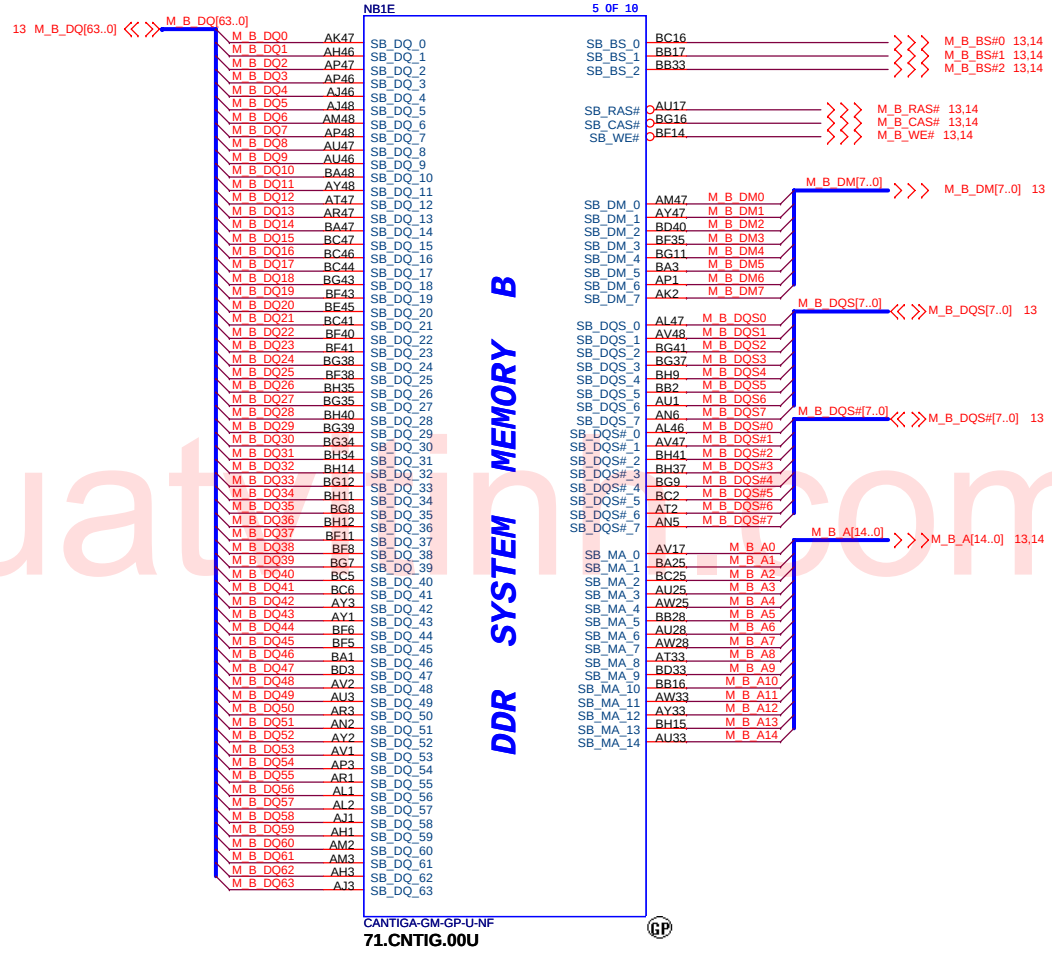

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Title	***Cantiga (3 of 6)***
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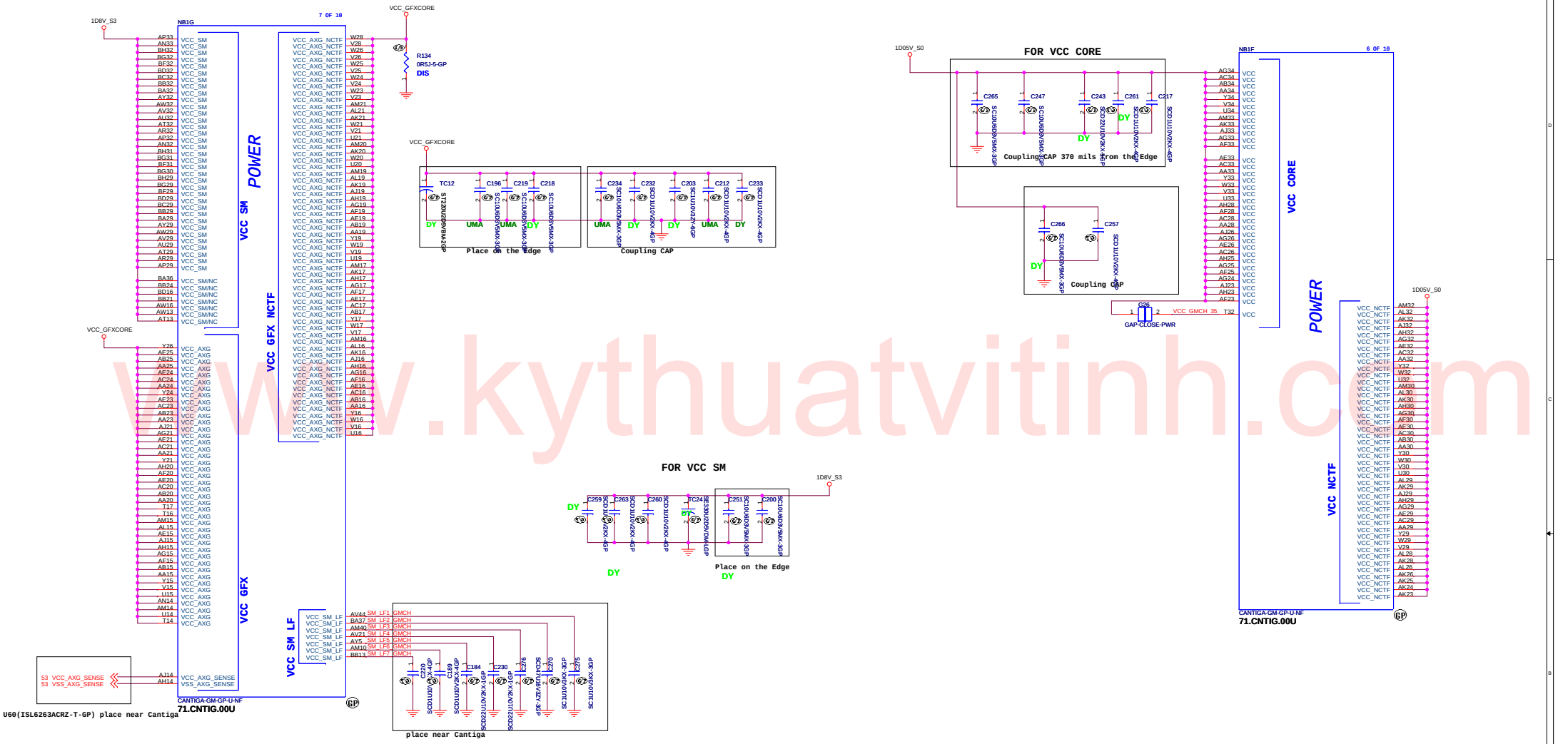

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Title	Cantiga (4 of 6)	
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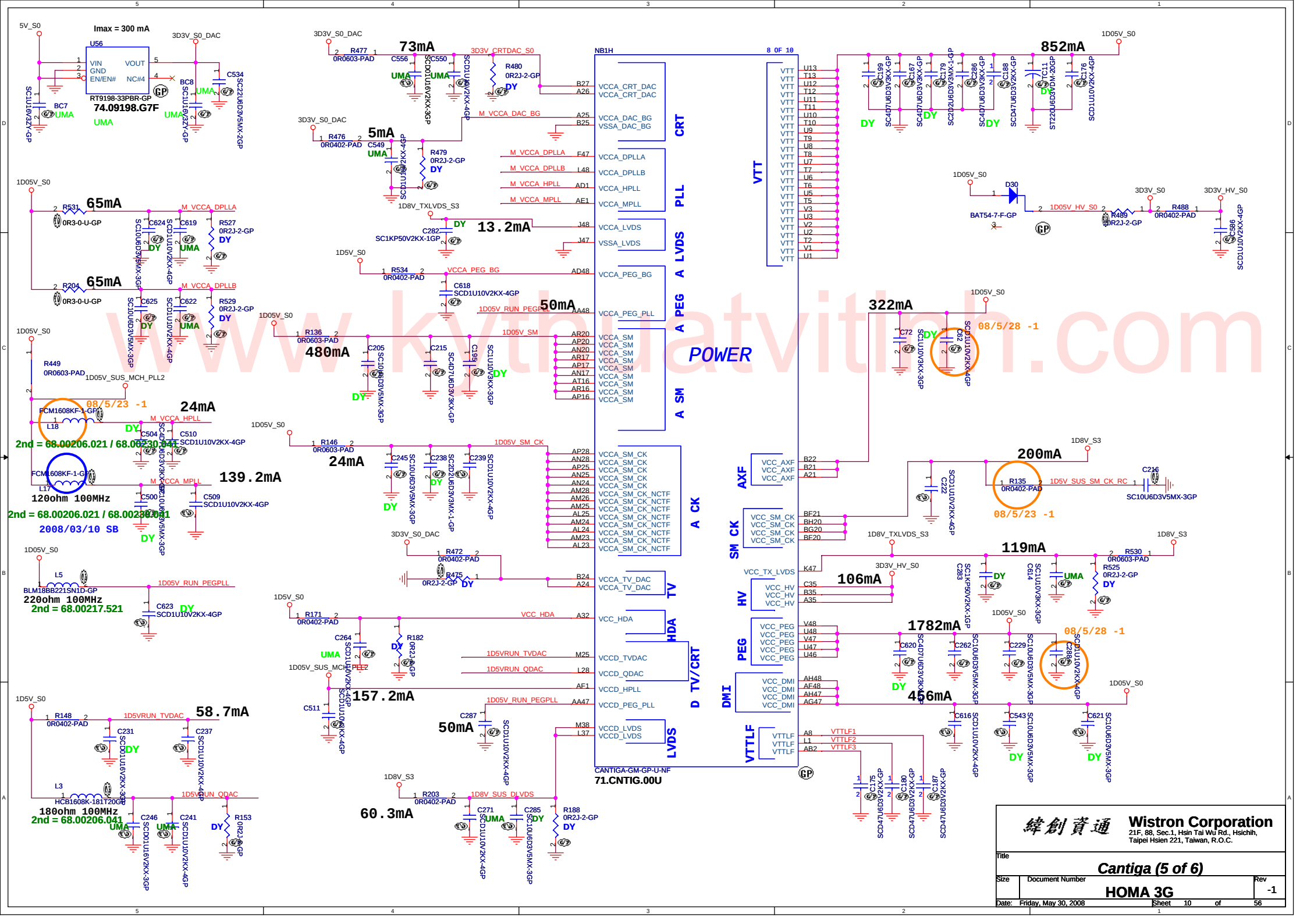

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Title	Cantiga (5 of 6)
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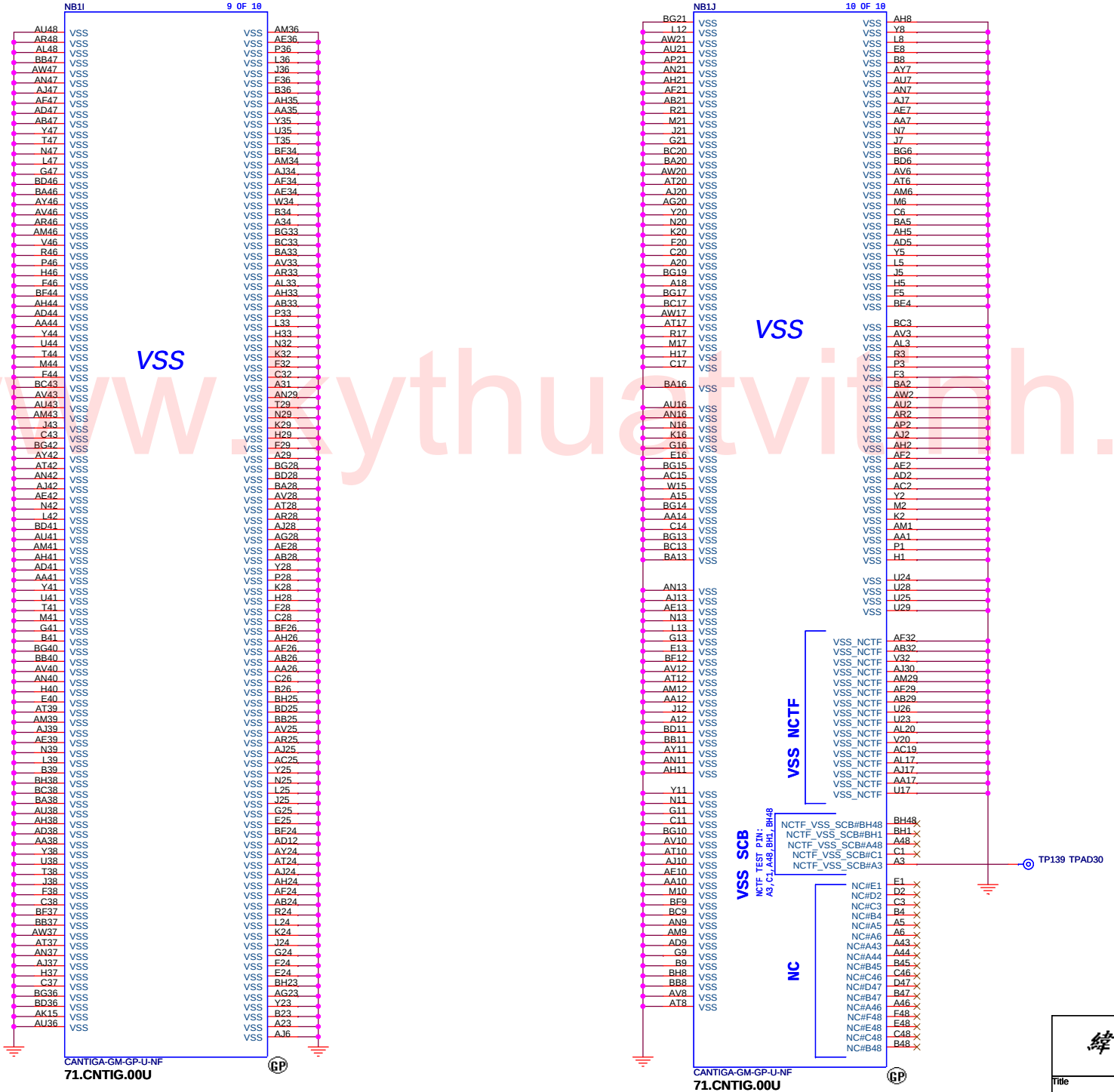

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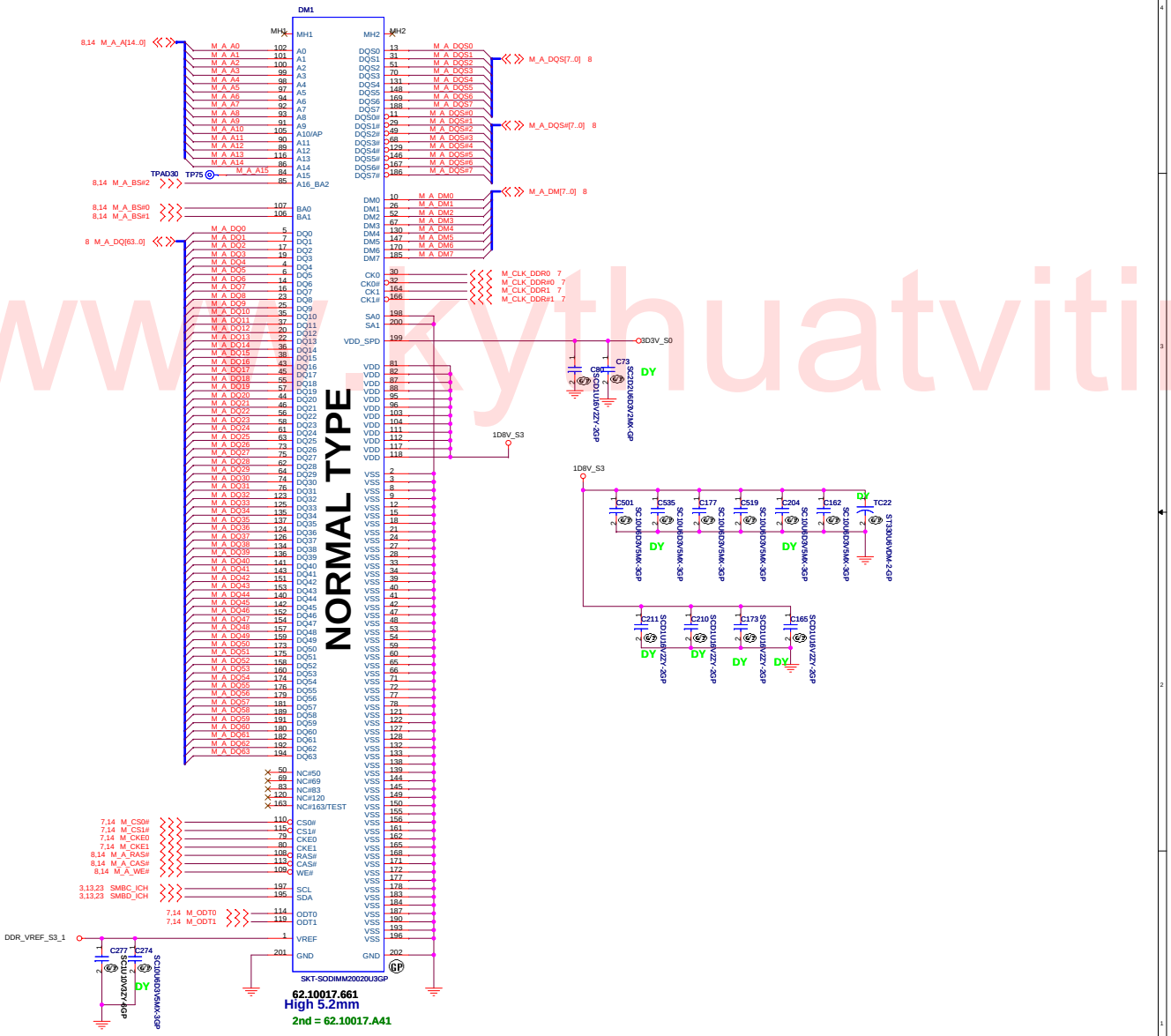
DDR2 SOCKET_1



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Title	DDR2 Socket	
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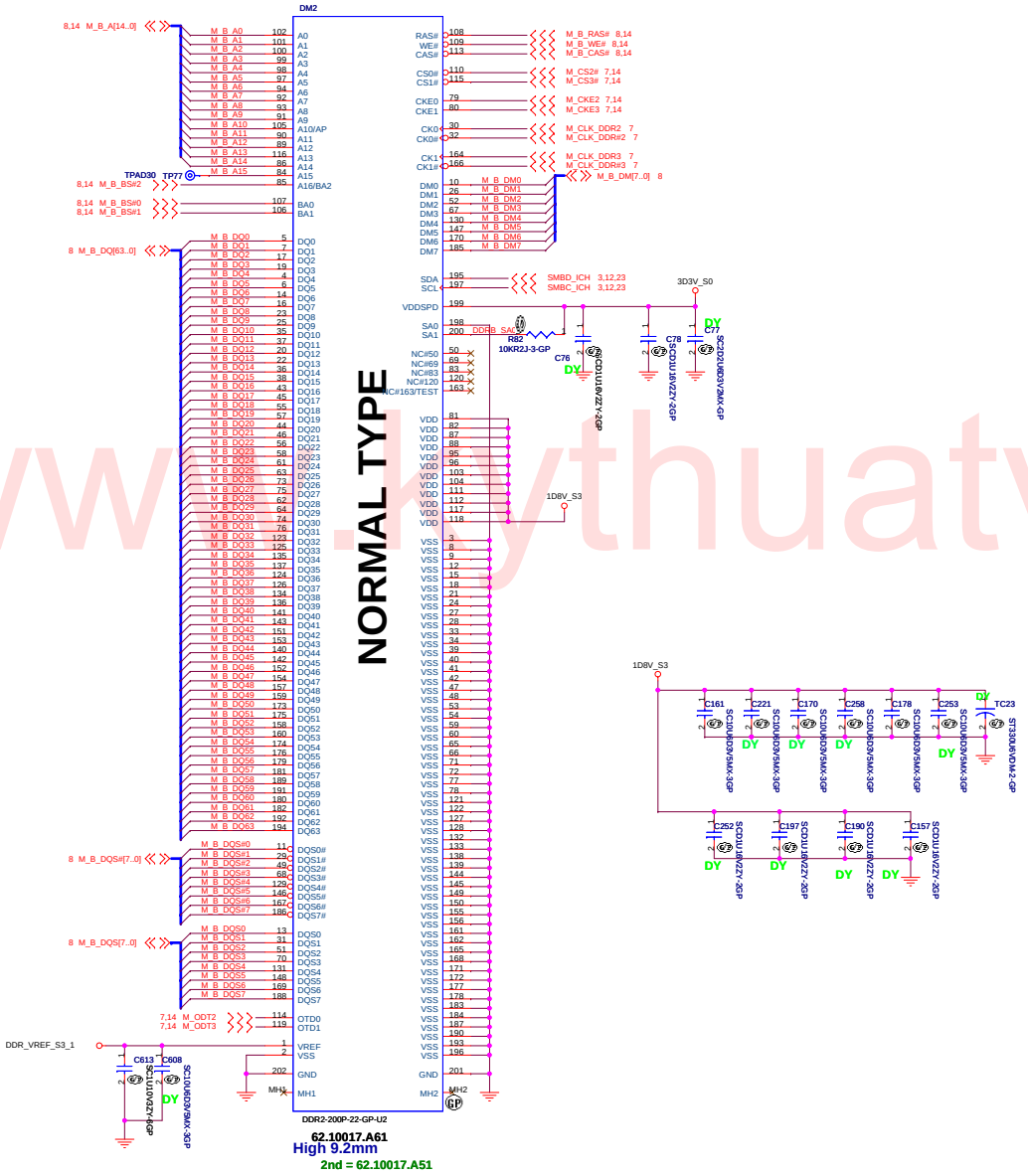
DDR2 SOCKET_2



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Title	DDR2 Termination Resistor	
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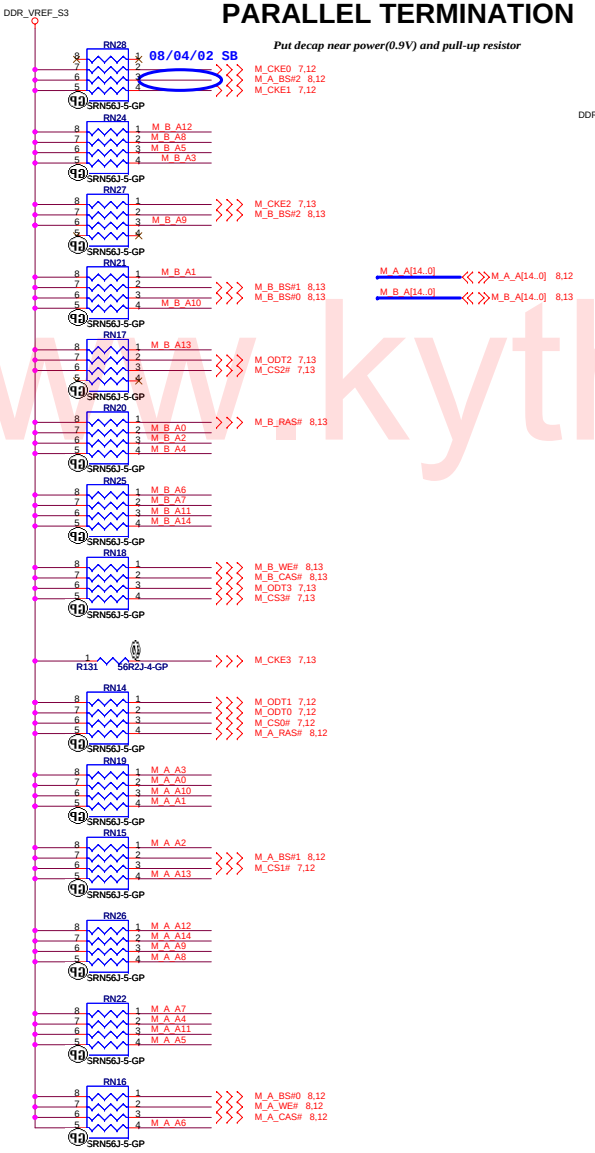
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

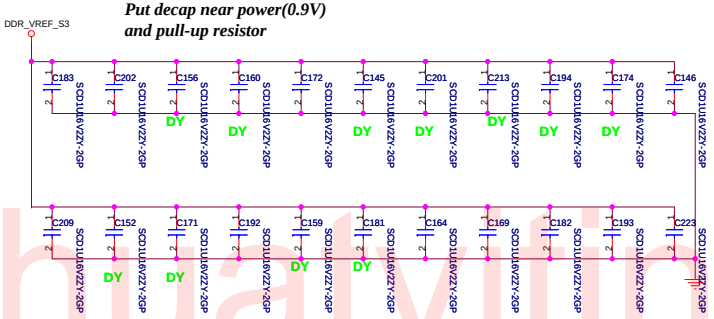


M_A_A[14..0] → M_A_A[14..0] 8,12

M_B_A[14..0] → M_B_A[14..0] 8,13

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



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Title	DDR 2 Termination Resistor
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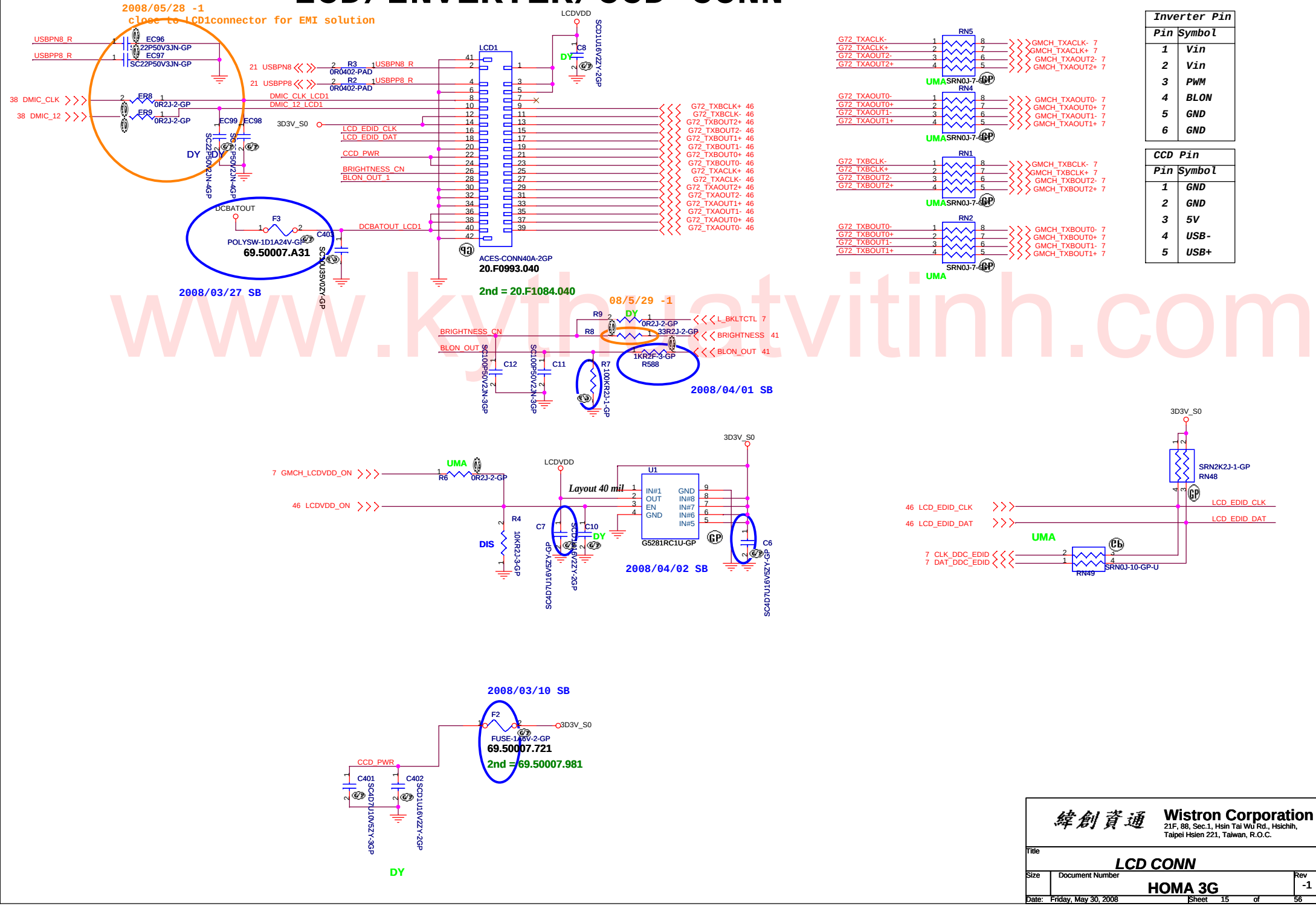
LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	GND
2	GND
3	5V
4	USB-
5	USB+

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Title: LCD CONN

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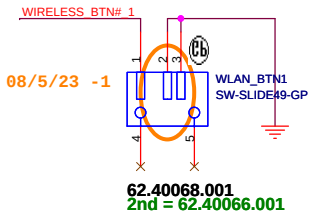
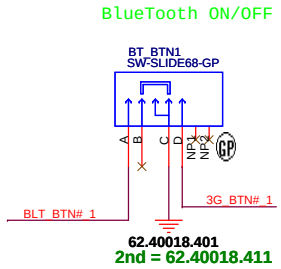
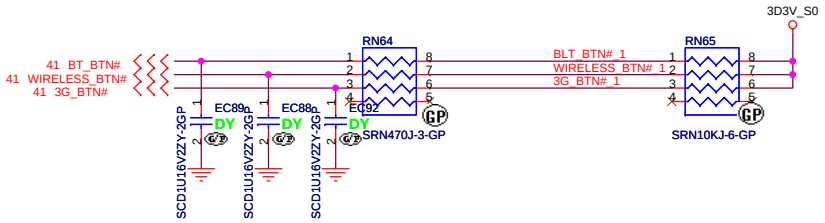
Wireless ON/OFF

Check Wireless Button left or right



BlueTooth ON/OFF





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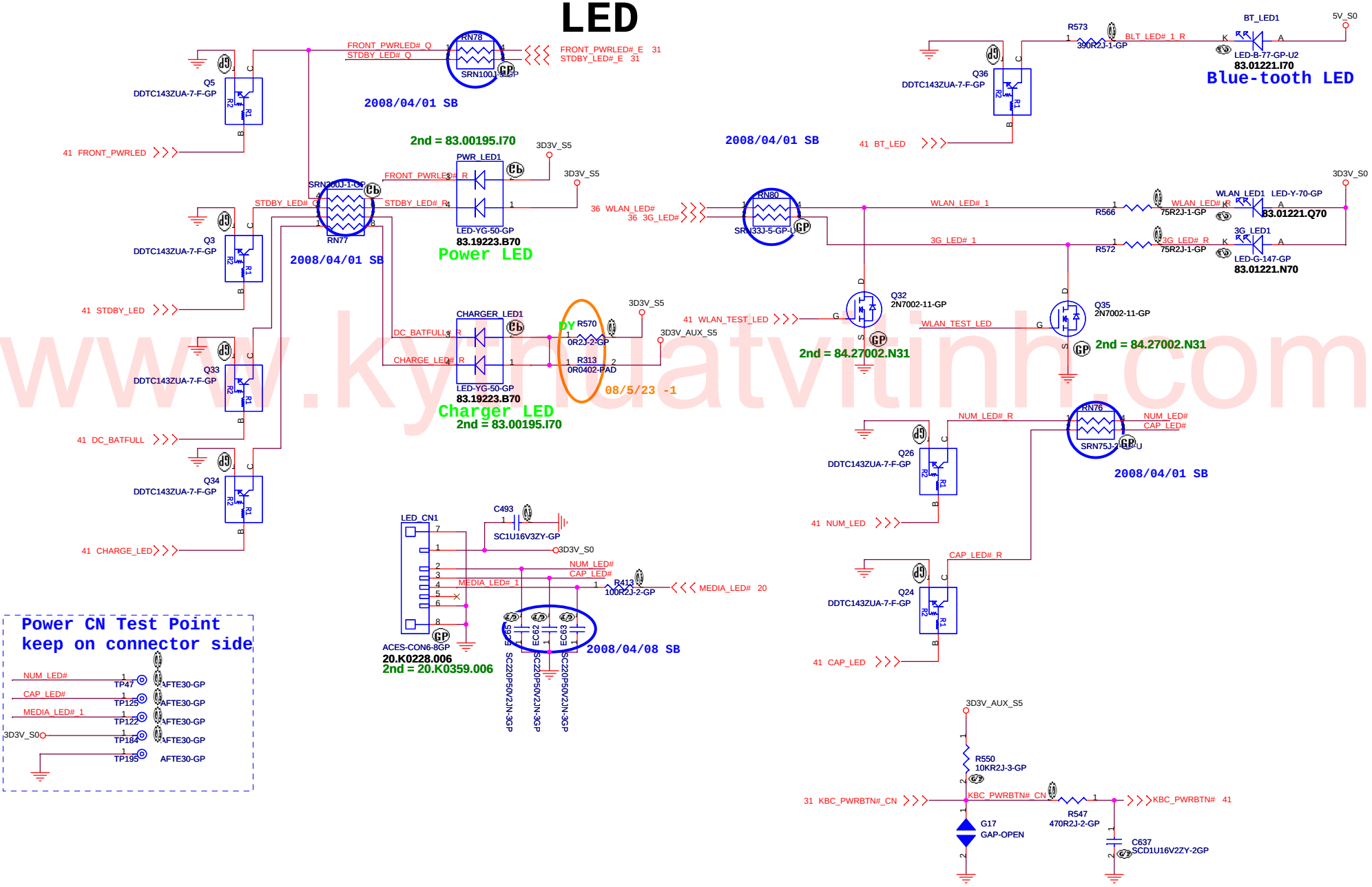
LED

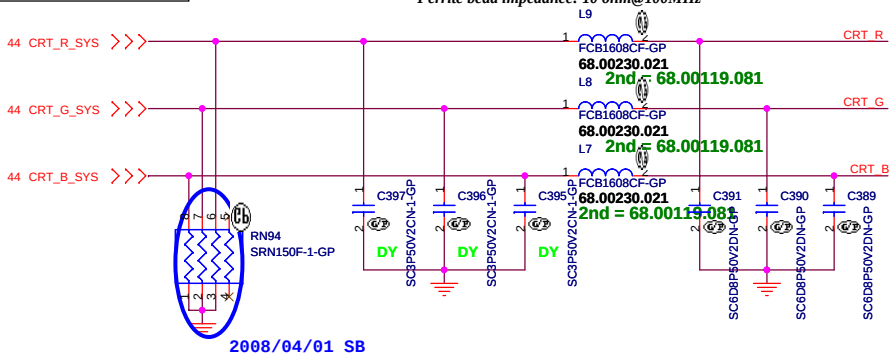


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

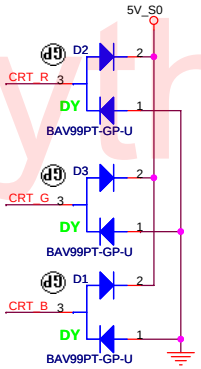
Title	LED&POWERBD CONN	
Size	Document Number: HOMA 3G	Rev: -1
Date: Friday, May 30, 2008	Sheet 17 of 56	

Layout Note:
Place these resistors close to the CRT-out connector

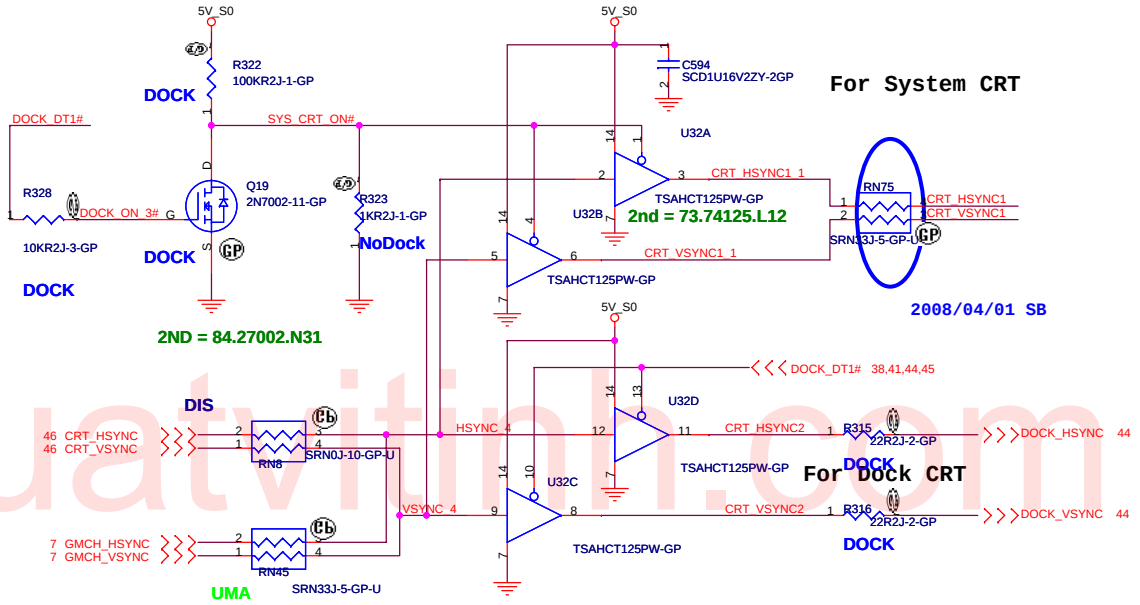
Ferrite bead impedance: 10 ohm@100MHz



Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

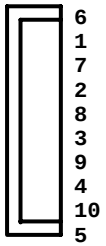


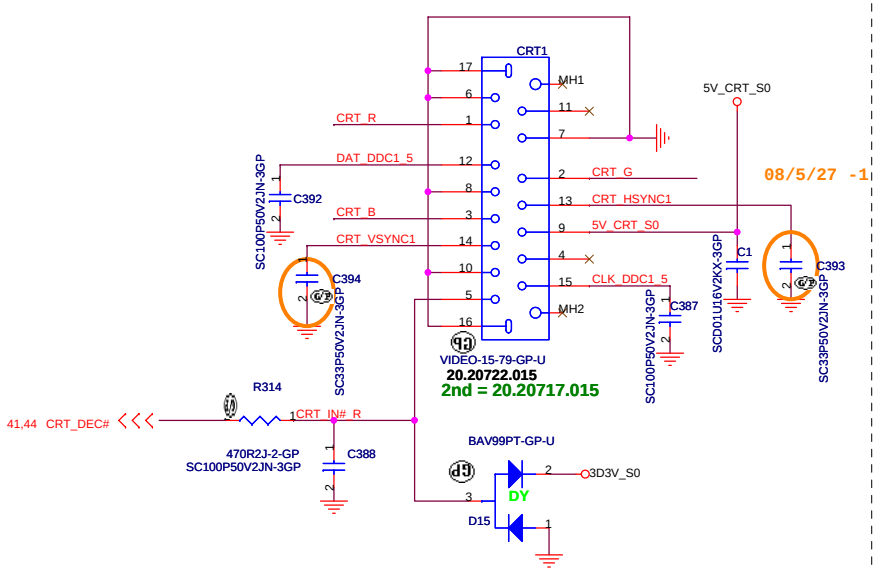
Hsync & Vsync level shift



Function	DOCK_CRT_SEL#
SYSTEM	H
DOCK	L

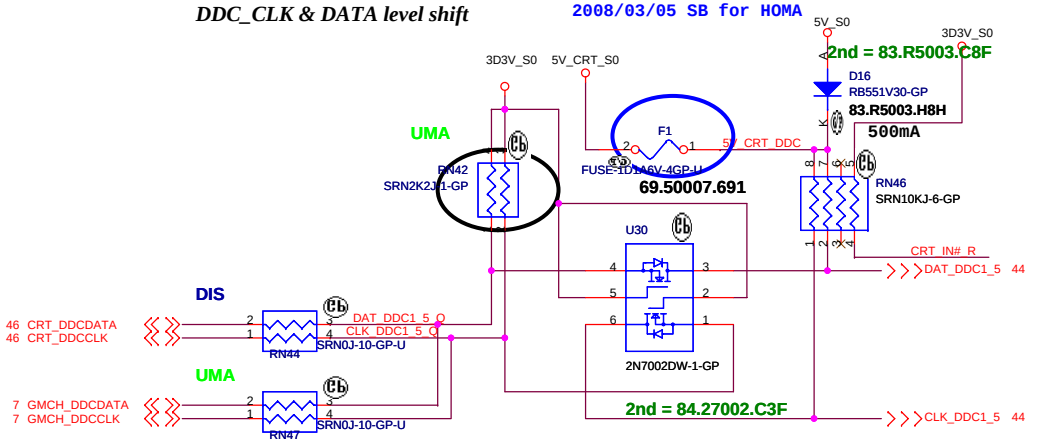
CRT I/F & CONNECTOR





DDC_CLK & DATA level shift

2008/03/05 SB for HOMA



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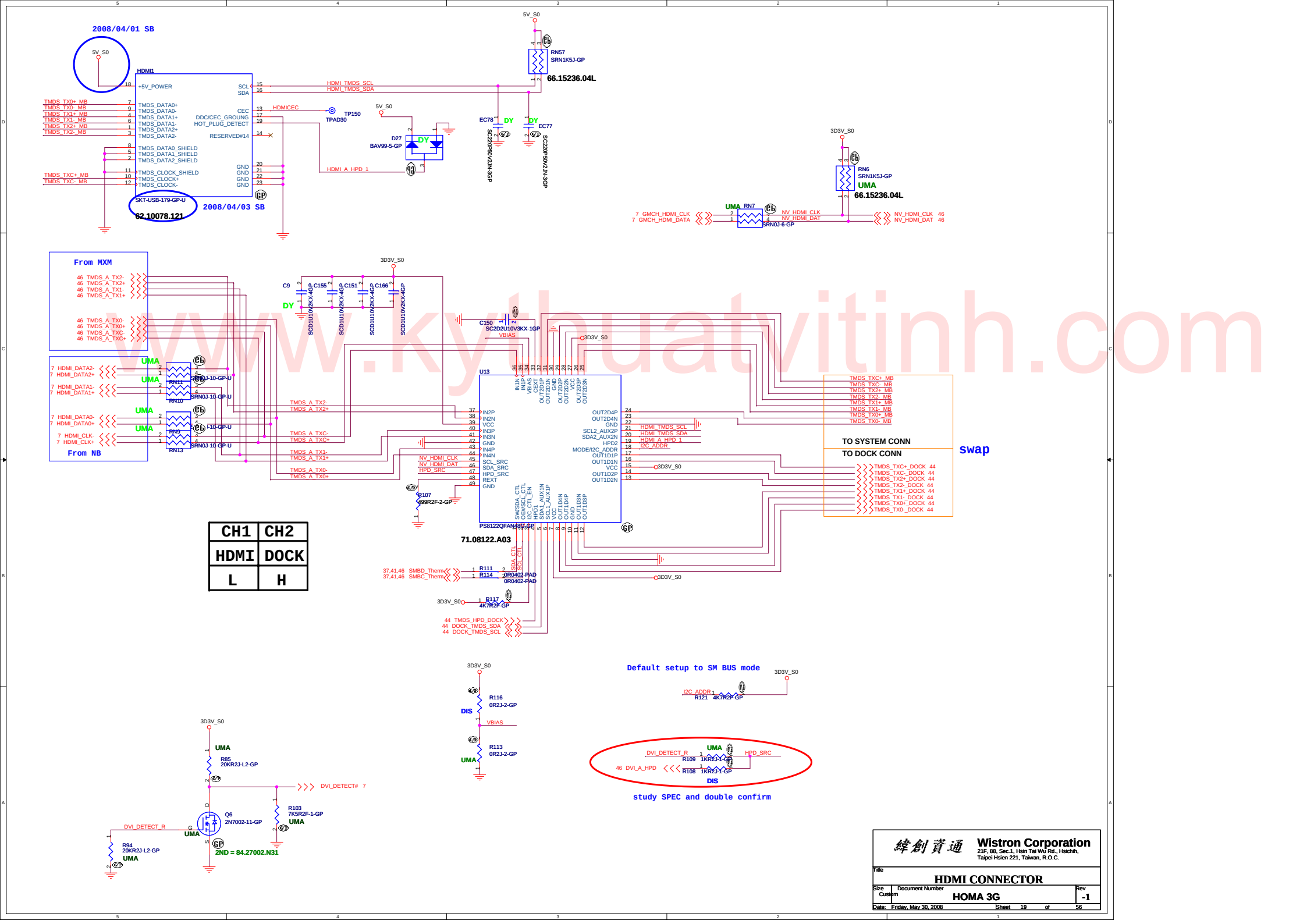
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT CONN	
Size	Document Number HOMA 3G	Rev -1
Date: Friday, May 30, 2008	Sheet 18 of 56	



CH1	CH2
HDMI	DOCK
L	H

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI CONNECTOR

Size	Document Number	Rev
Custom	HOMA 3G	-1

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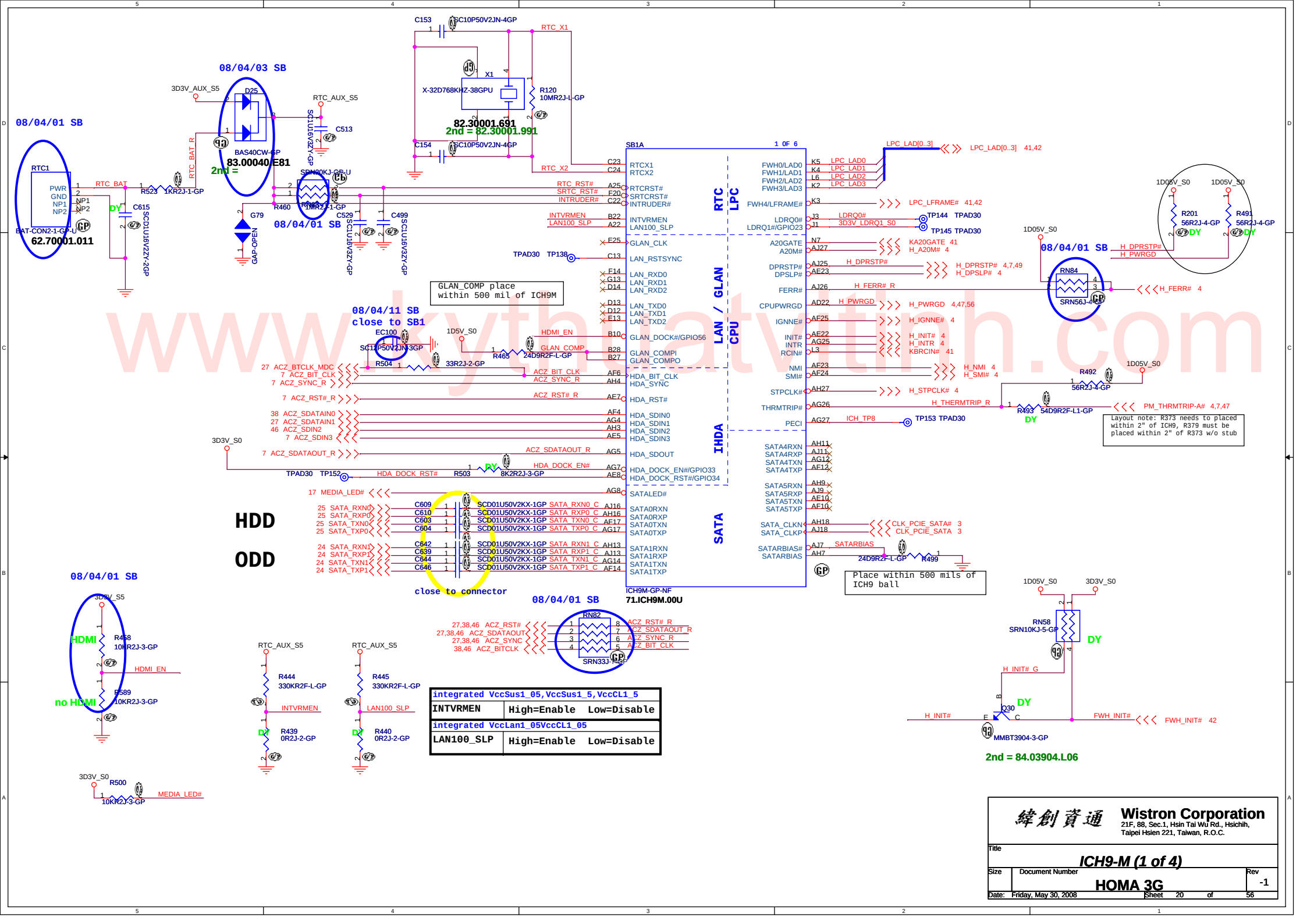
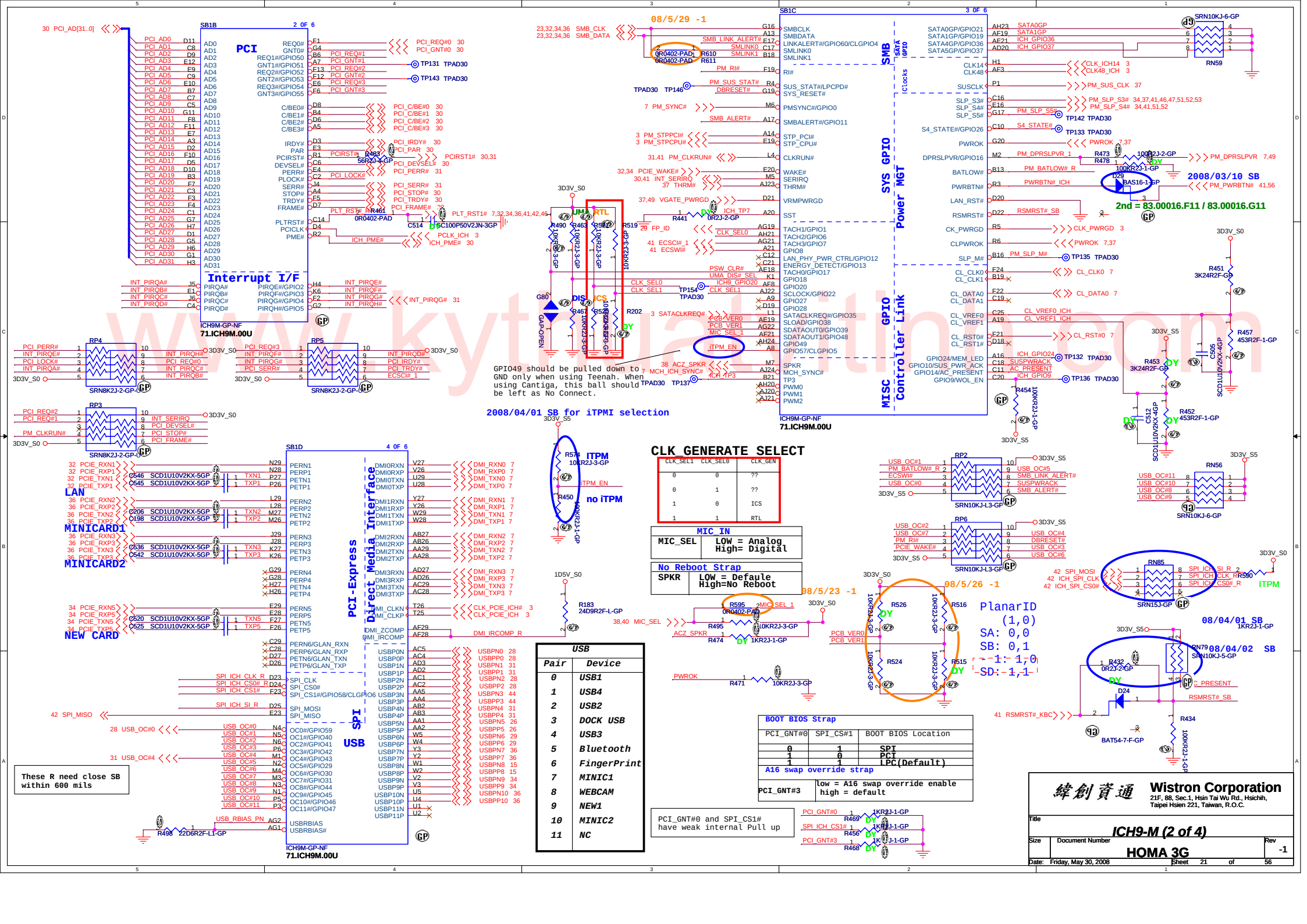
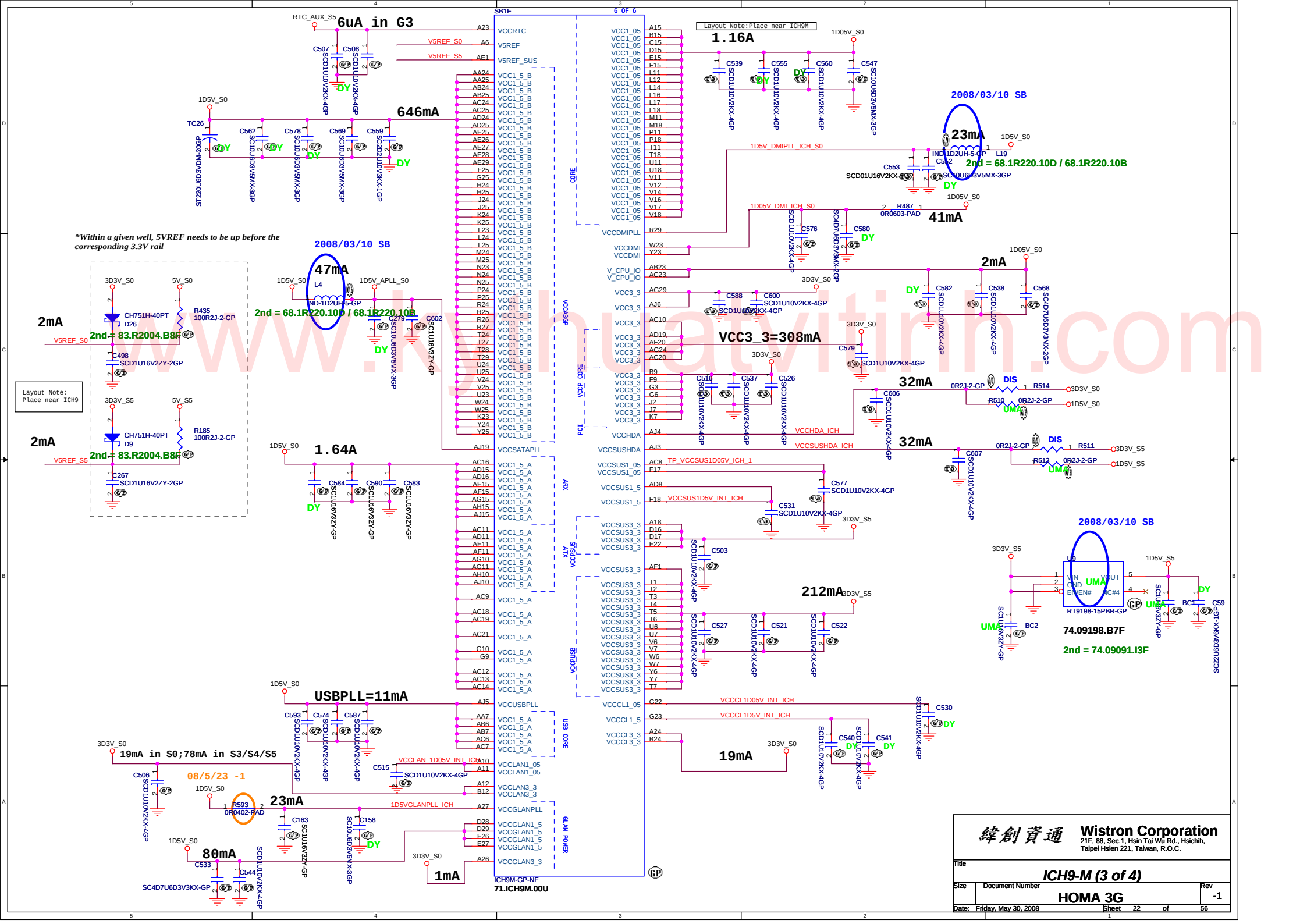

08/04/01 SB
RTC1
PWR
GND
NP1
NP2
BAT-CON2-1-GP-U
62.70001.011
RTC_BAT
R523 1KR2J-1-GP
C615
SCD1U16V2ZY-2GP
08/04/03 SB
3D3V_AUX_S5
D25
BAS40CW-GP
83.00040.E81
2nd =
RTC_BAT_R
RTC_AUX_S5
C513
SCD1U16V2ZY-GP
SRN20KJ-GP-U
R460 1MR2J-1-GP
G79
GAP-OPEN
08/04/01 SB
C529 SCD1U16V3ZY-GP
C499 SCD1U16V3ZY-GP
C153 SC10P50V2JN-4GP
C154 SC10P50V2JN-4GP
X1
X-32D768KHZ-38GPU
R120 10MR2J-L-GP
82.30001.691
2nd = 82.30001.991
RTC_X1
RTC_X2
SB1A
1 OF 6
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
RTC
LPC
GLAN
LAN / CPU
IHDA
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH9M-GP-NF
71.ICH9M.00U
LPC_LAD[0..3]
LPC_LFRAME#
LDRQ0#
LDRQ1#
TP144 TPAD30
TP145 TPAD30
KA20GATE
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
KBRCIN#
H_NMI
H_SMI#
H_STPCLK#
H_THERMTRIP_R
PM_THRMTRIP-A#
ICH_TP8
TP153 TPAD30
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATARBIAS
R499 24D9R2F-L-GP
Place within 500 mils of ICH9 ball
GLAN_COMP place within 500 mil of ICH9M
08/04/11 SB close to SB1
EC100 SC11P50V2JN-3GP
HDMI_EN
R465 24D9R2F-L-GP
GLAN_COMP
R504 33R2J-2-GP
ACZ_BIT_CLK
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDATAIN0
ACZ_SDATAIN1
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDATAOUT_R
HDA_DOCK_RST#
R503 8K2R2J-3-GP
HDA_DOCK_EN#
MEDIA_LED#
HDD
ODD
SCD01U50V2KX-1GP
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_RXN1_C
SATA_RXP1_C
SATA_TXN1_C
SATA_TXP1_C
close to connector
08/04/01 SB
RN82 SRN33J-7-GP
ACZ_RST#_R
ACZ_SDATAOUT_R
ACZ_SYNC_R
ACZ_BIT_CLK
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
08/04/01 SB
HDMI
R458 10KR2J-3-GP
HDMI_EN
no HDMI
R589 10KR2J-3-GP
R500 10KR2J-3-GP
MEDIA_LED#
RTC_AUX_S5
R444 330KR2F-L-GP
INTVRMEN
DY R439 0R2J-2-GP
R445 330KR2F-L-GP
LAN100_SLP
DY R440 0R2J-2-GP
08/04/01 SB
RN84 SRN56J-4-GP
R201 56R2J-4-GP
R491 56R2J-4-GP
DY
R492 56R2J-4-GP
R493 54D9R2F-L1-GP
DY
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
RN58 SRN10KJ-5-GP
DY
H_INIT# G
Q30 MMBT3904-3-GP
DY
FWH_INIT#
2nd = 84.03904.L06
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
Document Number
HOMA 3G
Rev
-1
Date: Friday, May 30, 2008
Sheet 20 of 56




6uA in G3
646mA
1.16A
23mA
2008/03/10 SB
2nd = 68.1R220.10D / 68.1R220.10B
41mA
2mA
47mA
2nd = 68.1R220.10D / 68.1R220.10B
VCC3_3=308mA
32mA
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
08/5/23 -1
23mA
80mA
1mA
212mA
19mA
2mA
2nd = 83.R2004.B8F
2mA
2nd = 83.R2004.B8F
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
2008/03/10 SB
74.09198.B7F
2nd = 74.09091.I3F
RT9198-15PBR-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
HOMA 3G
Rev -1
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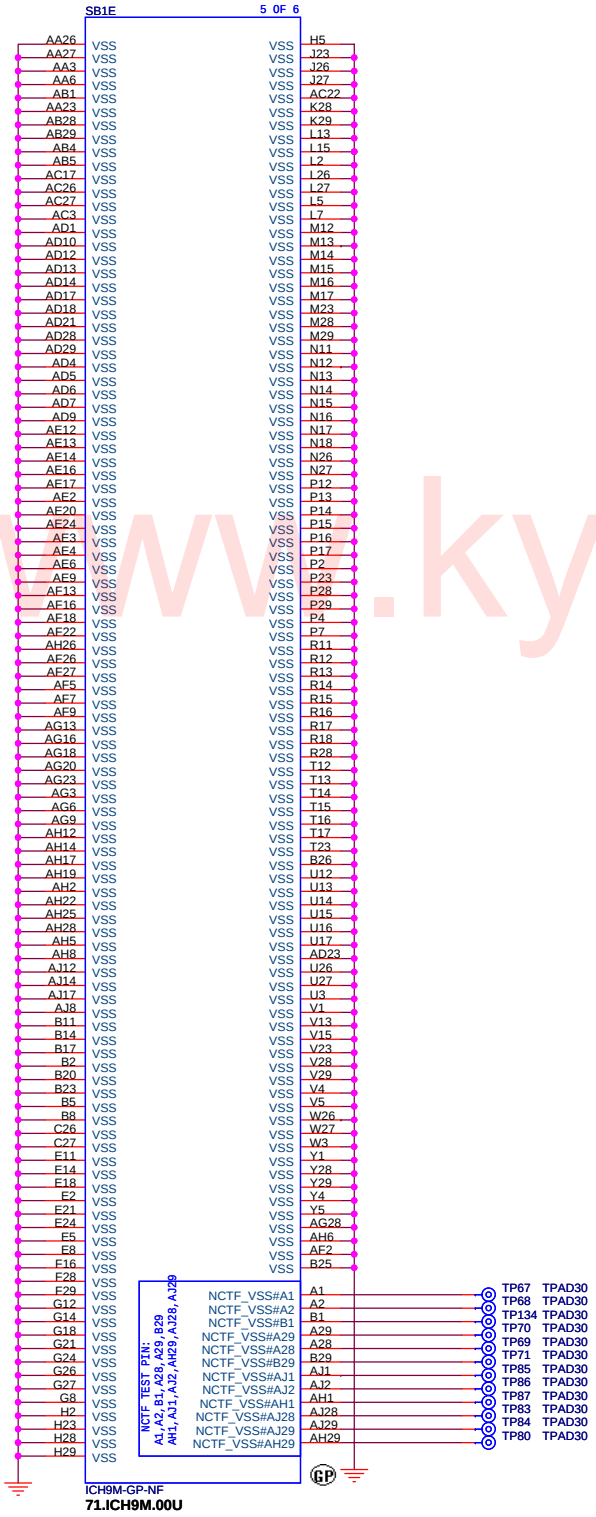

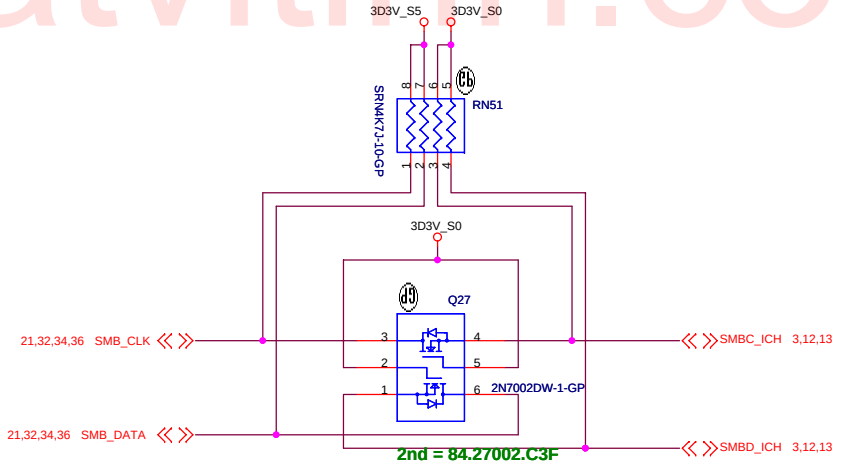

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (4 of 4)

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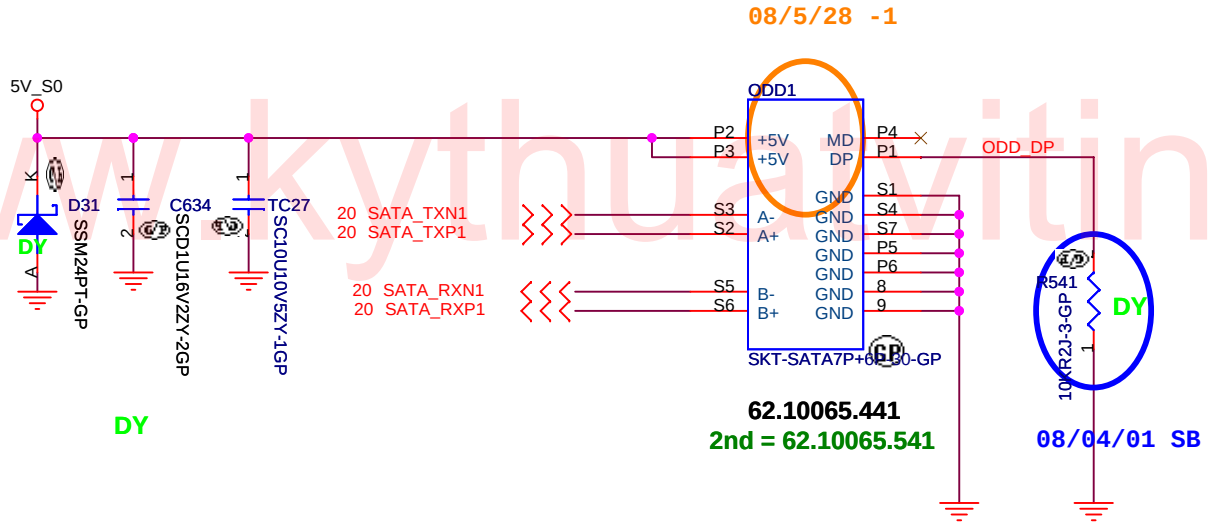
ODD Connector



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***ODD***	
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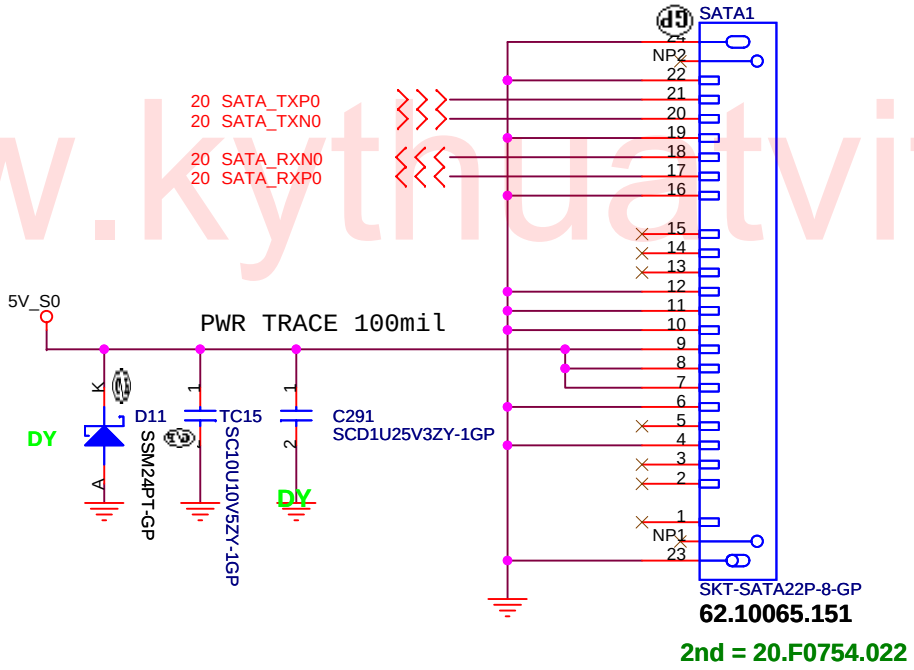
SATA Connector



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD CONN***	
Size	Document Number **HOMA 3G**	Rev -1
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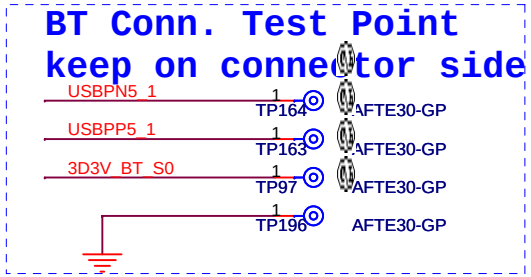
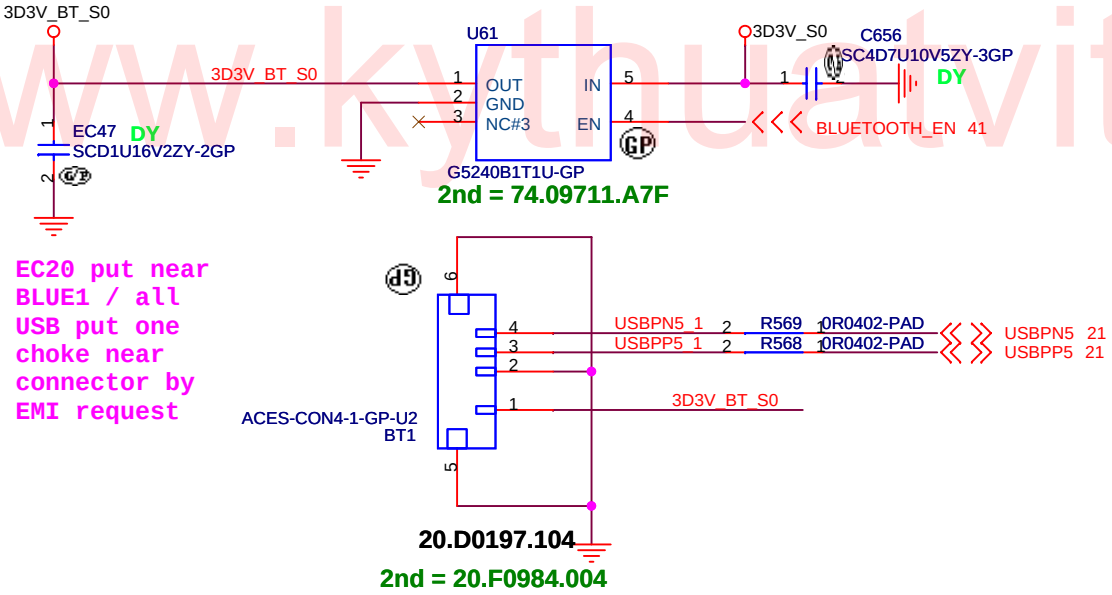
BLUETOOTH MODULE





緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLUETOOTH		
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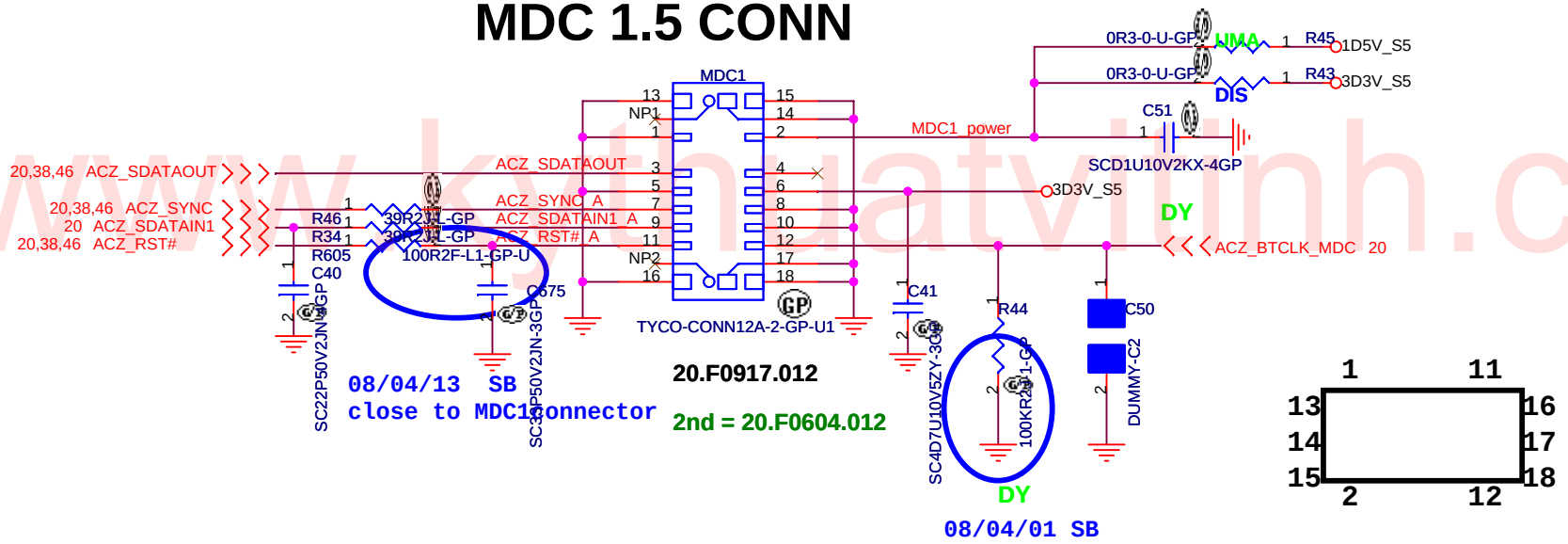
MDC 1.5 CONN



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MDC***	
Size	Document Number **HOMA 3G**	Rev -1
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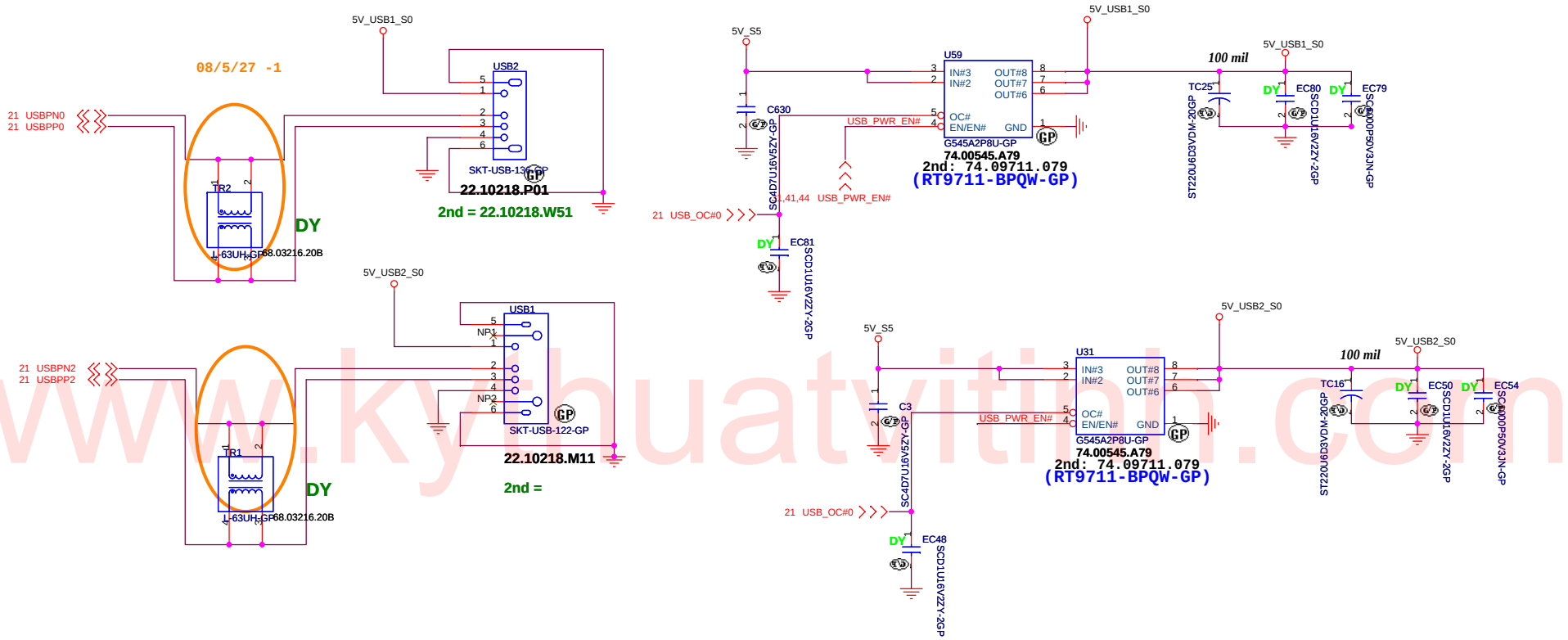

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*USB*	
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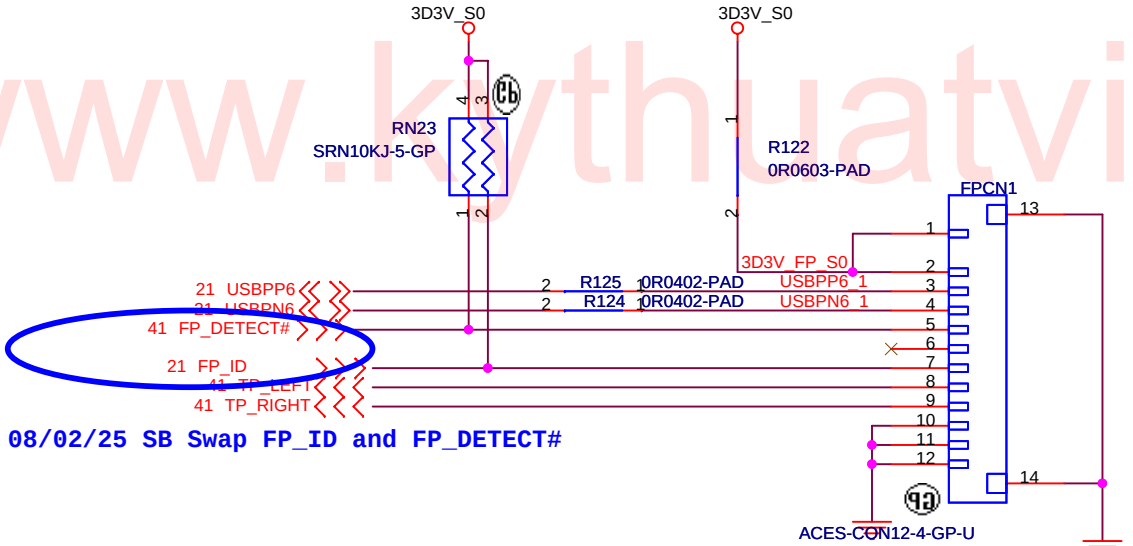
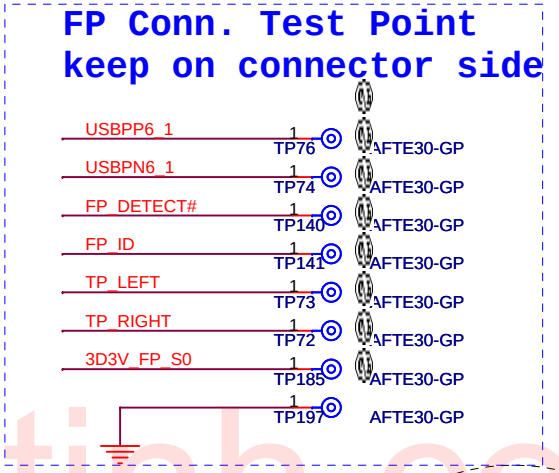
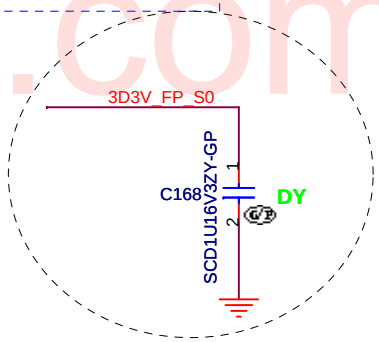
Finger printer







For EMI

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*Finger Printer*	
Size	Document Number: HOMA 3G	Rev: -1
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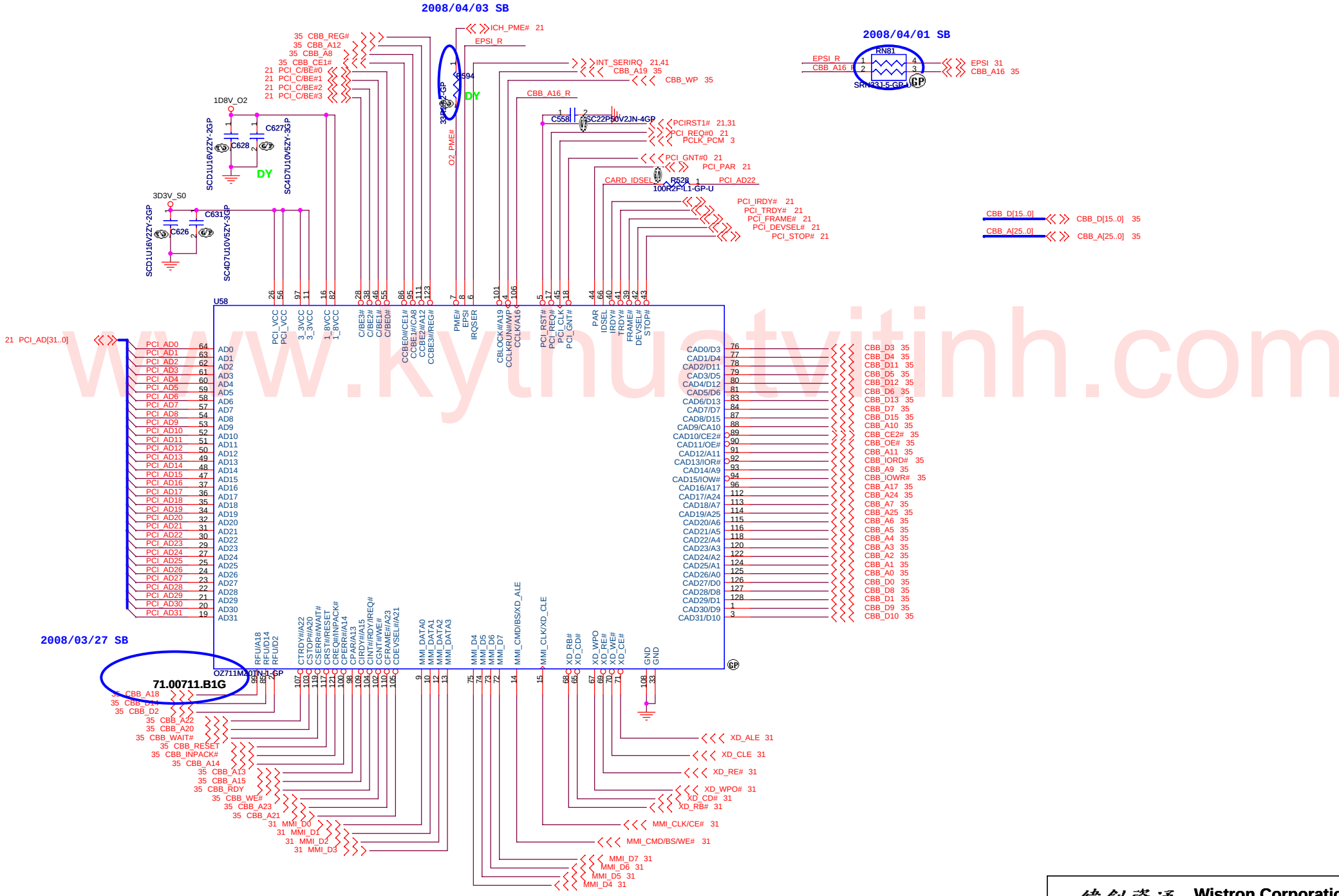

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Card Reader - OZ711MZ0*

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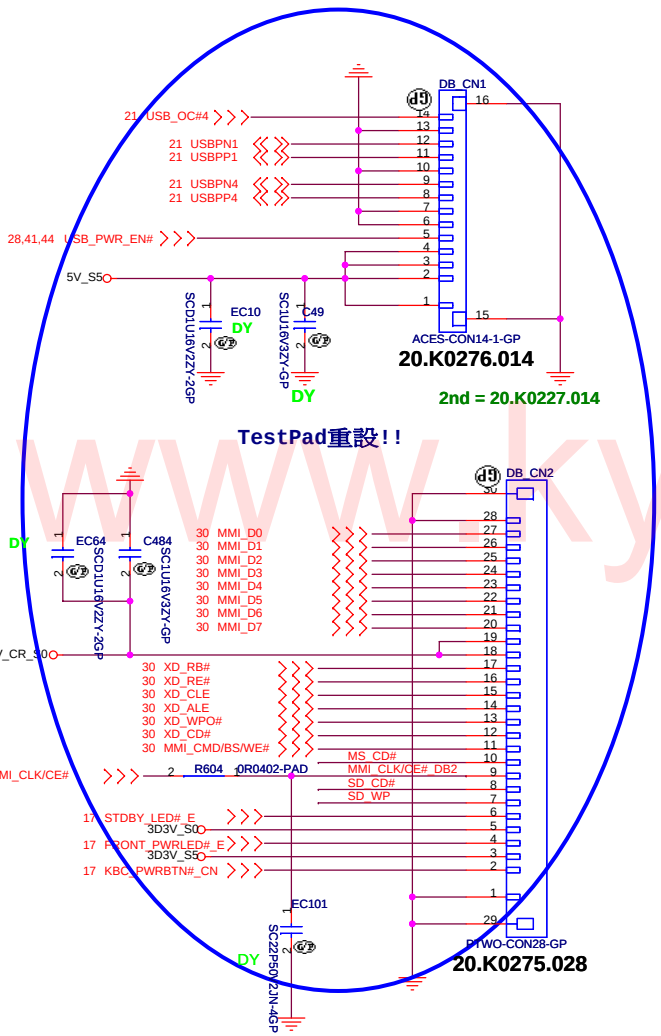
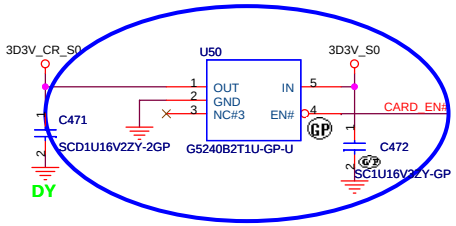
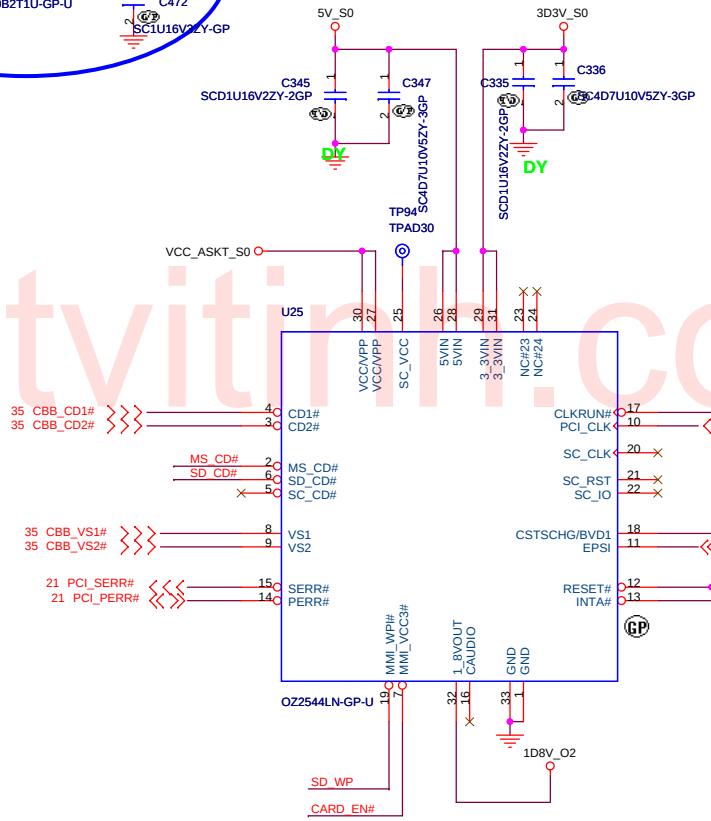
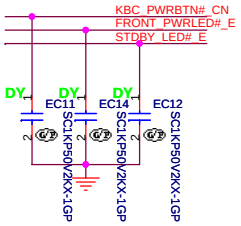
2008/03/27 SB follow 4P

2008/04/02 SB follow 4P

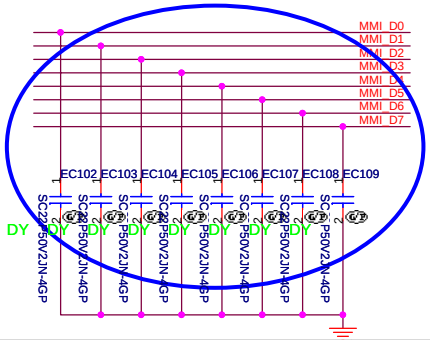




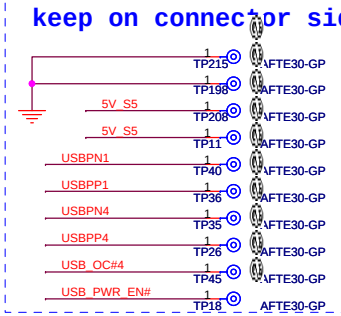




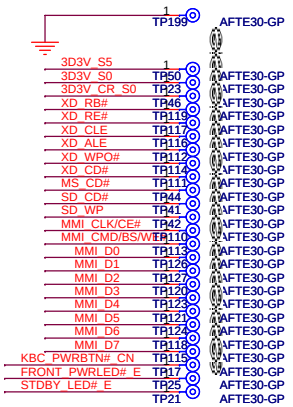
2008/04/11 SB
close to DB_CN2



DB_CN1 Conn. Test Point
keep on connector side



DB_CN2 Conn. Test Point
keep on connector side



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Card Reader Connector	
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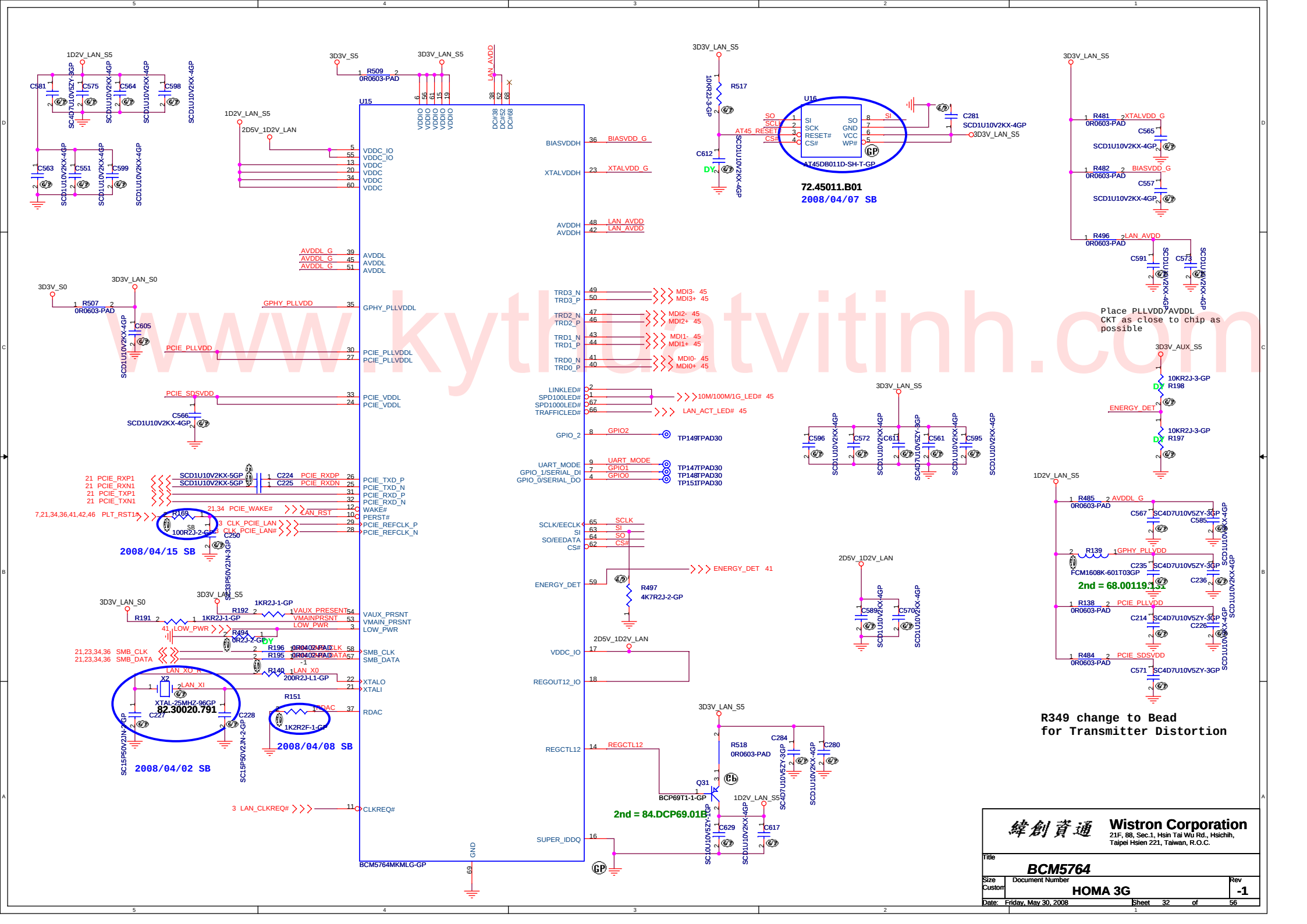
U15
BCM5764MKMLG-GP
U16
AT45DB011D-SH-T-GP
72.45011.B01
2008/04/07 SB
2008/04/15 SB
2008/04/08 SB
2008/04/02 SB
82.30020.791
2nd = 84.DCP69.01D
2nd = 68.00119.152
Place PLLVDD/AVDDL CKT as close to chip as possible
R349 change to Bead for Transmitter Distortion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
BCM5764
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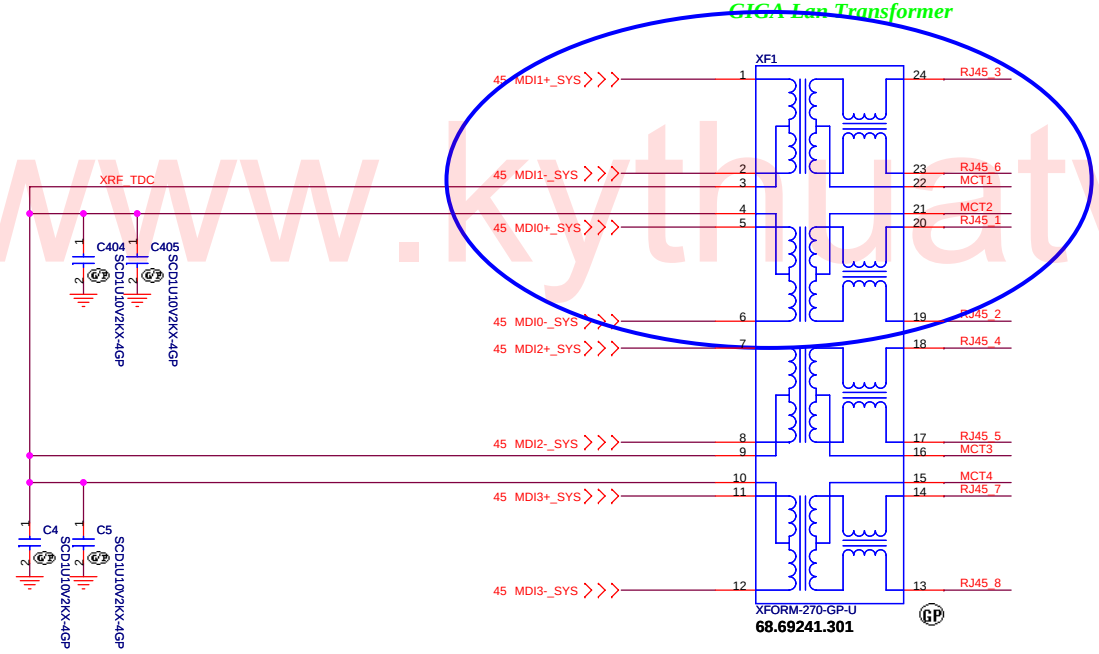
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

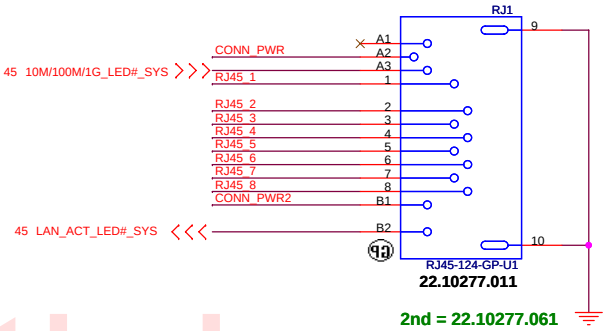
LAN Connector

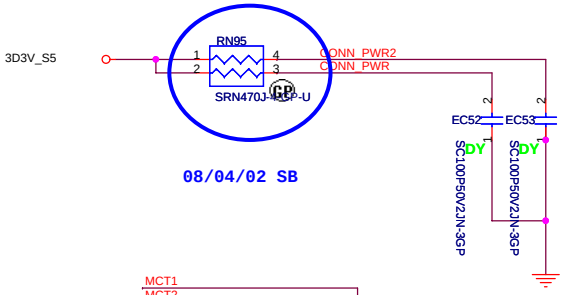
LAN Connector

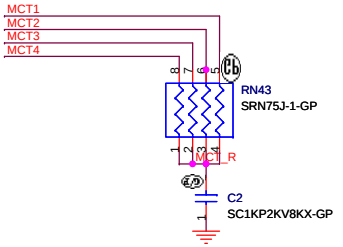
2008/04/09 SB

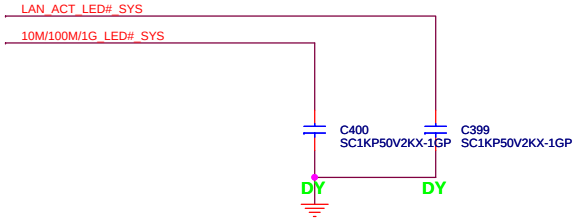
GIGA Lan Transformer











HOMA 3G

HOMA 3G

緯創資通 Wistron Corporation
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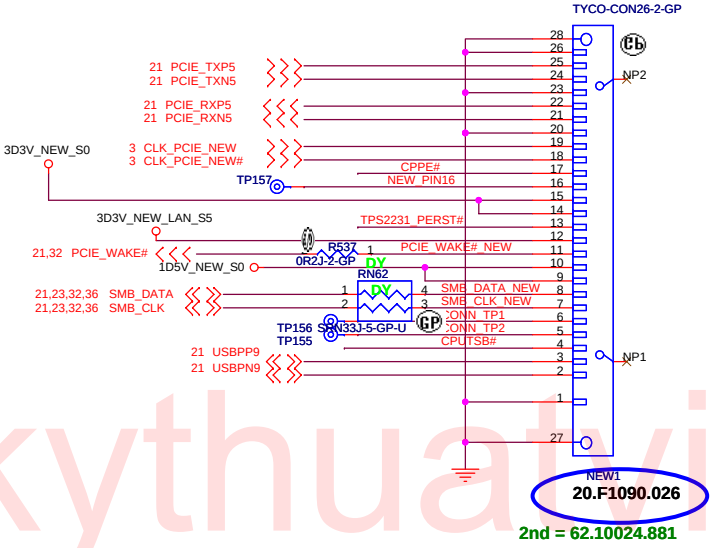
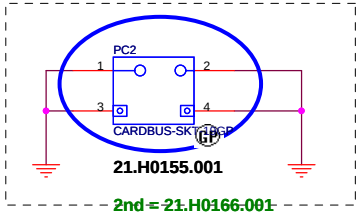
Taipei Hsien 221, Taiwan, R.O.C.

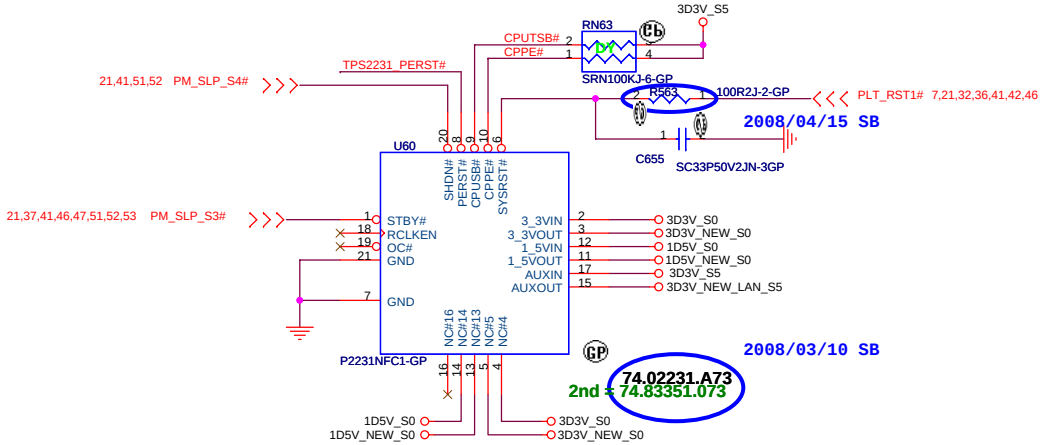
Title: LAN CONN

Size: A3 | Document Number | Rev: -1

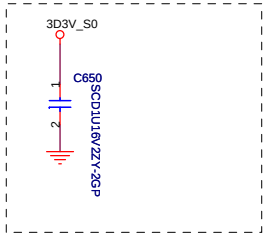
Date: Friday, May 30, 2008 | Sheet 33 of 56



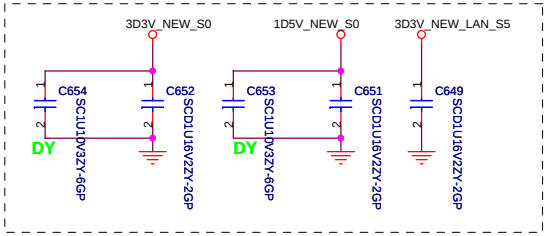




Place them Near to Chip



Place them Near to Connector



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**NEW CARD**
Size	Document Number: **HOMA 3G** Rev: -1
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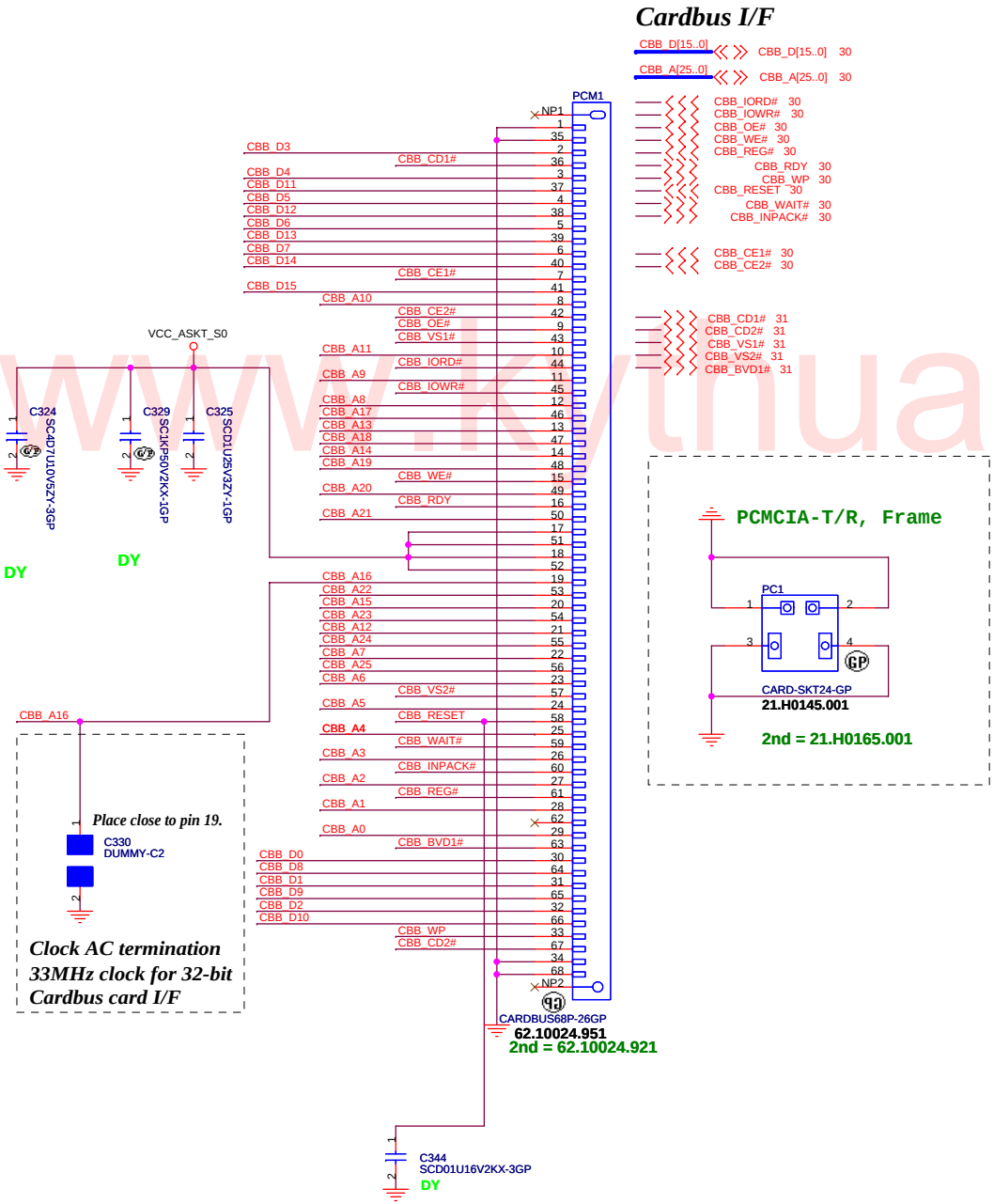
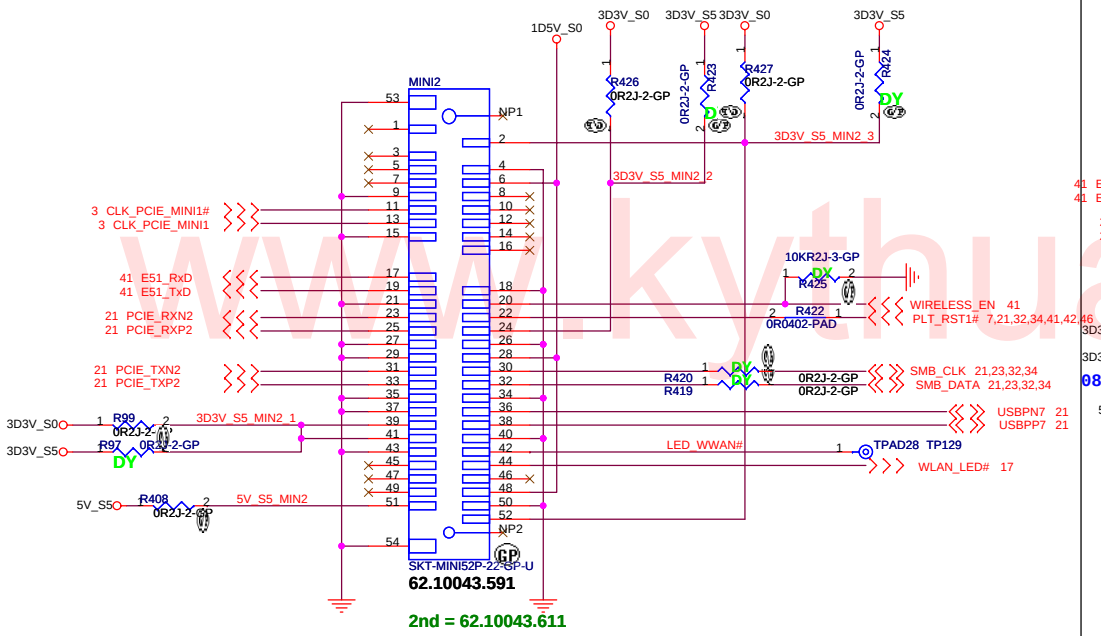
PCMCIA Socket

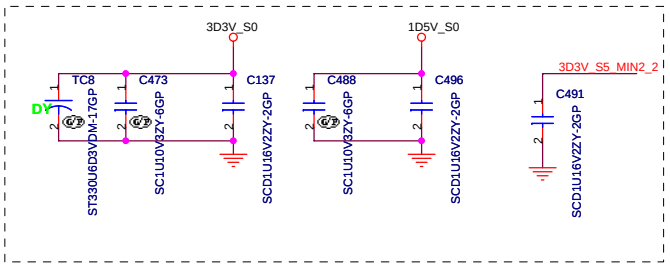


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCMCIA		
Size: A3	Document Number: HOMA 3G	Rev: -1
Date: Friday, May 30, 2008	Sheet 35 of 56	

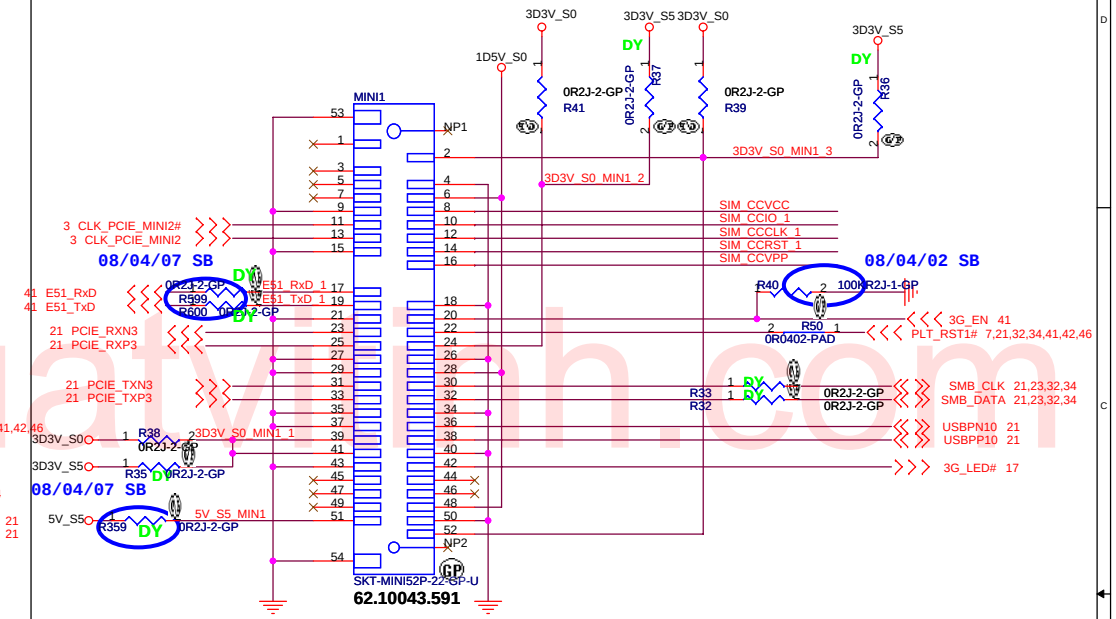
Mini Card Connector(WLAN)



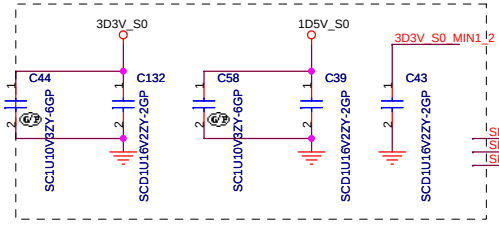
Place near MINIC1

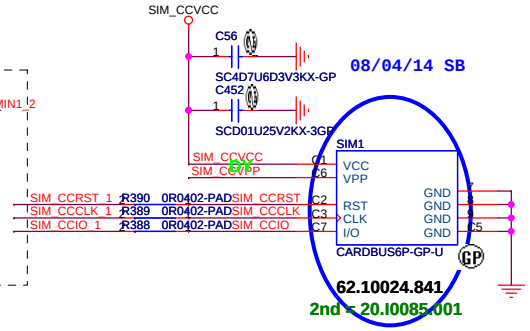


Mini Card Connector(Robson2 and 3G)
Support debug-card



Place near MINIC2





緯創資通 **Wistron Corporation**
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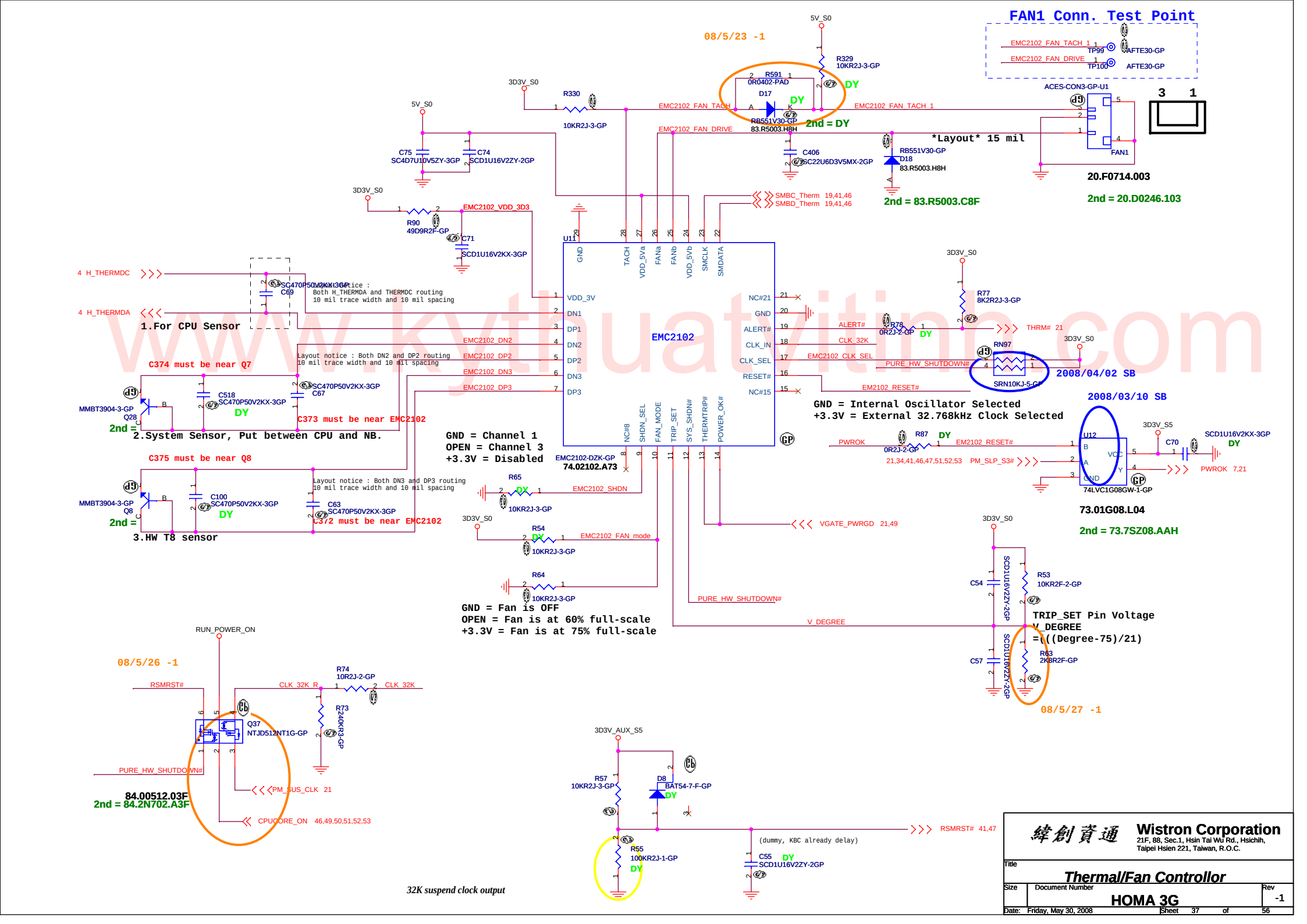
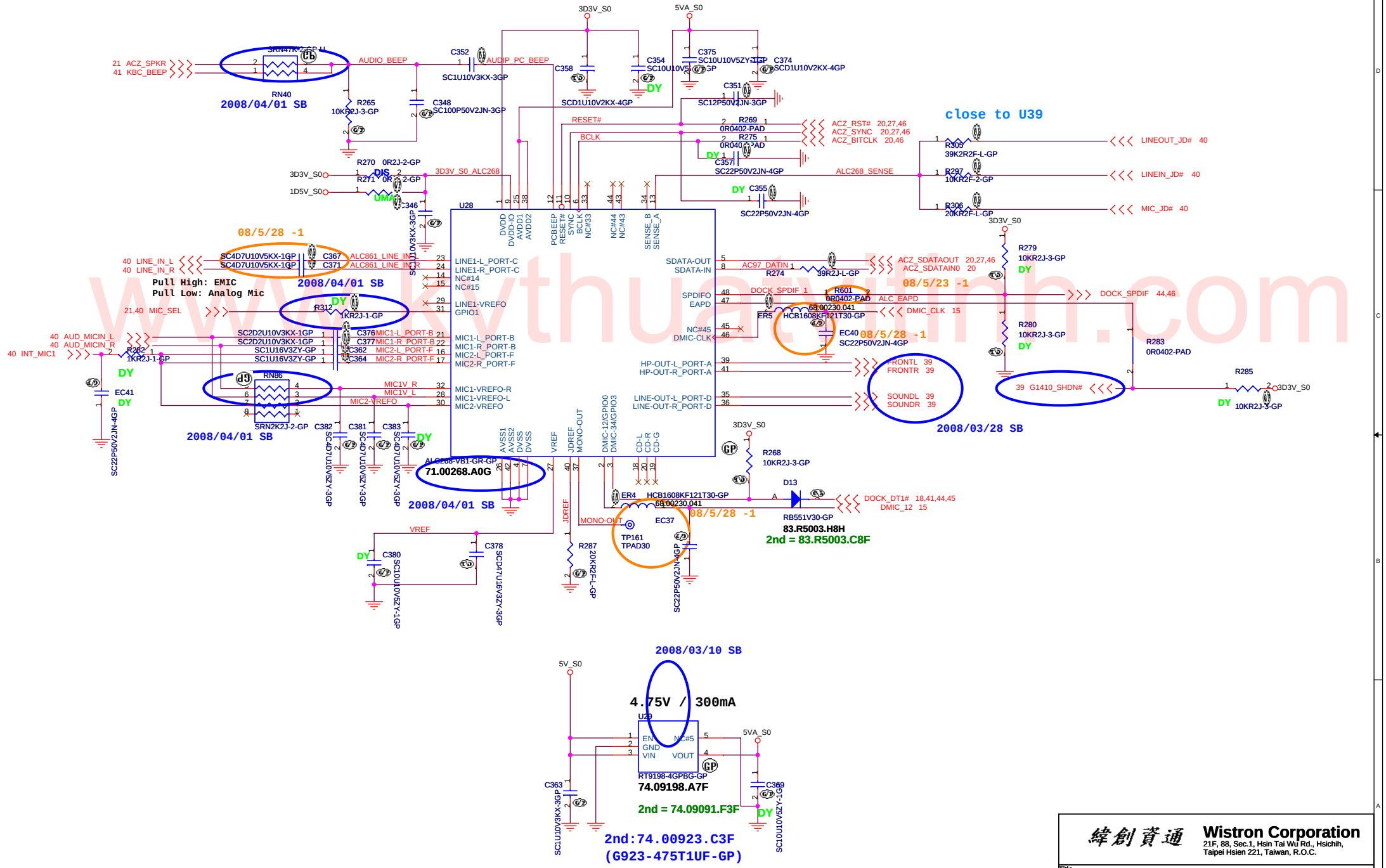
Taipei Hsien 221, Taiwan, R.O.C.

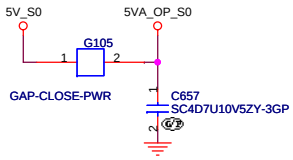
Title	MINI & SIM CARD	
Size A3	Document Number HOMA 3G	Rev -1
Date: Friday, May 30, 2008	Sheet 36 of 56	

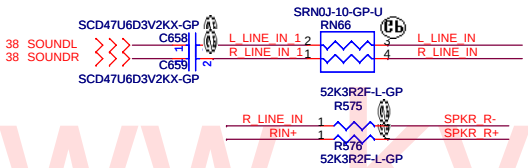


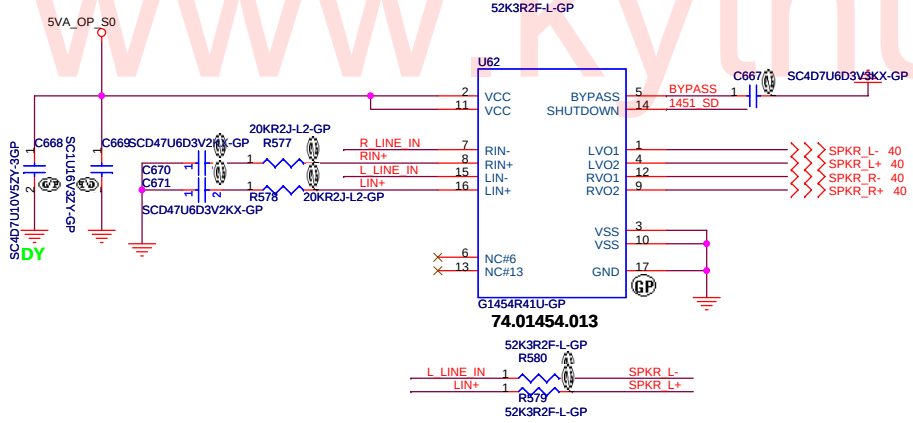


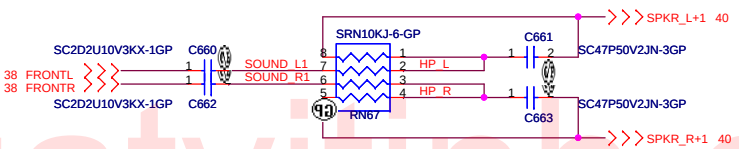
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Azalia codec ALC268		
Size: A3	Document Number: HOMA 3G	Rev: -1
Date: Friday, May 30, 2008	Sheet 38 of 56	

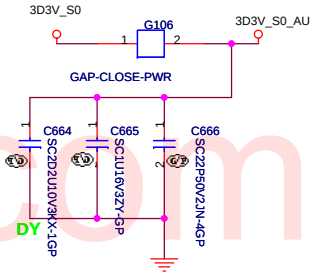
AUDIO OP AMPLIFIER

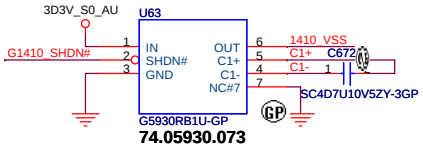


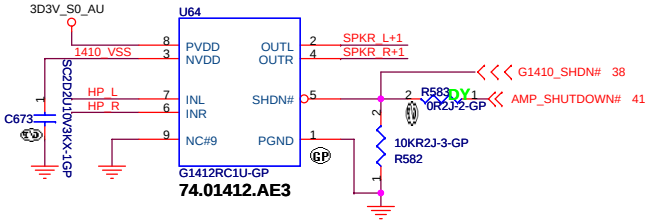


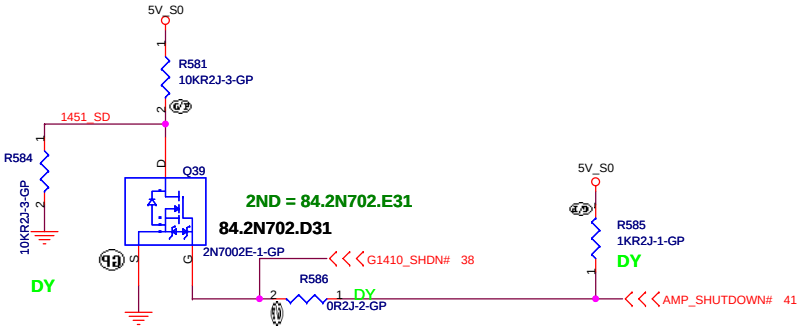












HOMA 3G

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Title: *AUDIO AMP*

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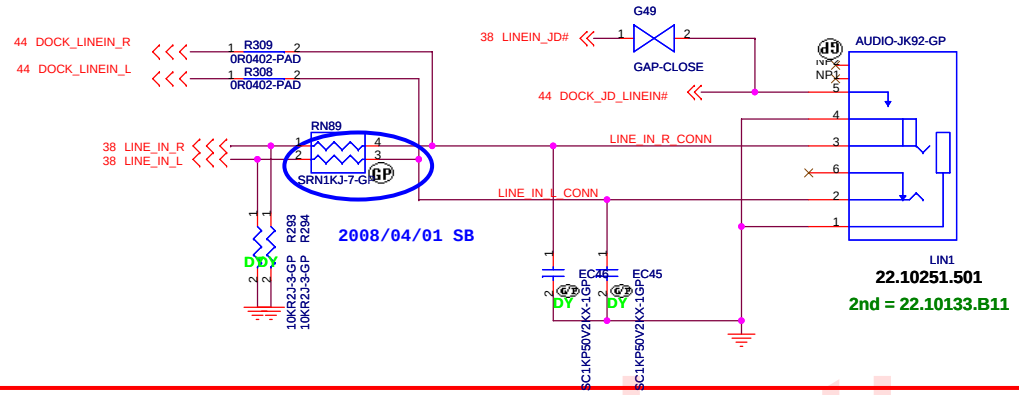
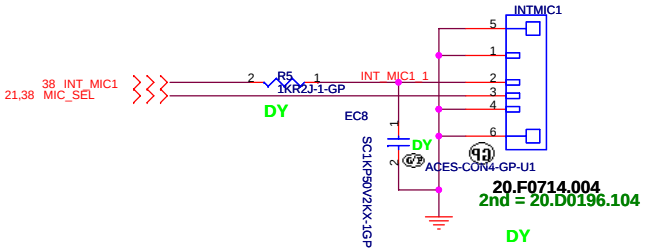
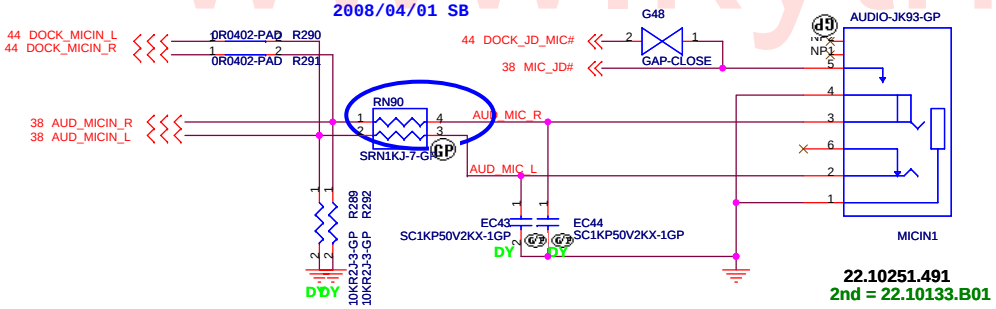
LINE IN



Internal Microphone

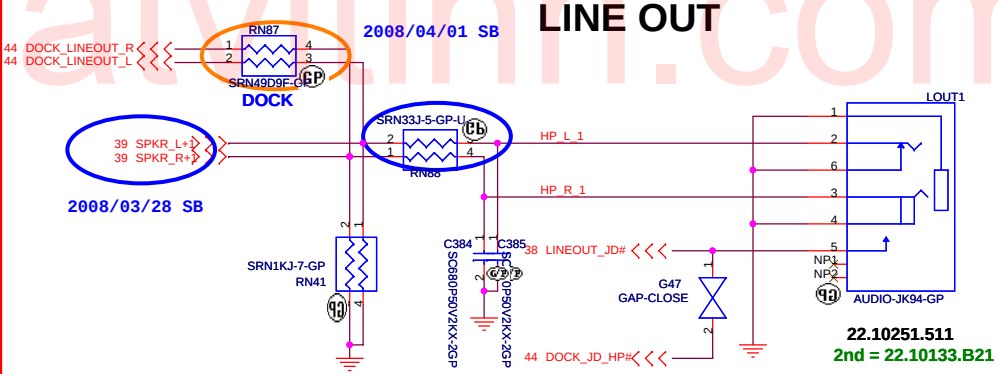


MIC IN

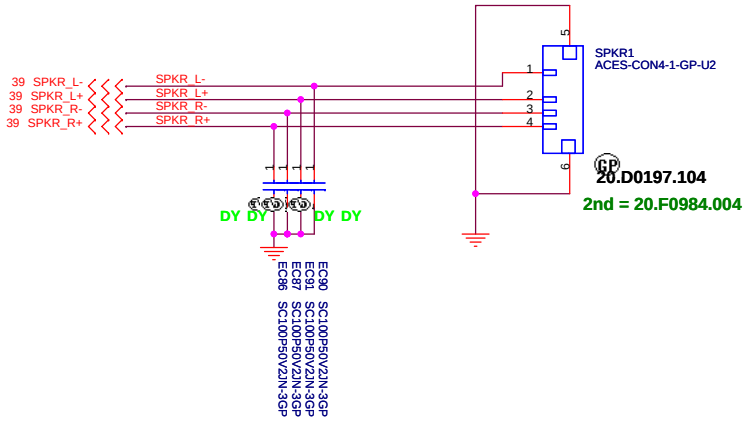


08/5/28 -1
modify to 49.9 ohm

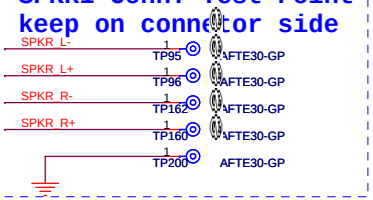
LINE OUT



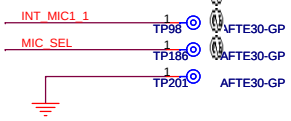
Internal Speaker



SPKR1 Conn. Test Point keep on connetor side



INTMIC1 Conn. Test Point keep on connetor side



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: AUDIO JACK		
Size	Document Number: HOMA 3G	Rev: -1
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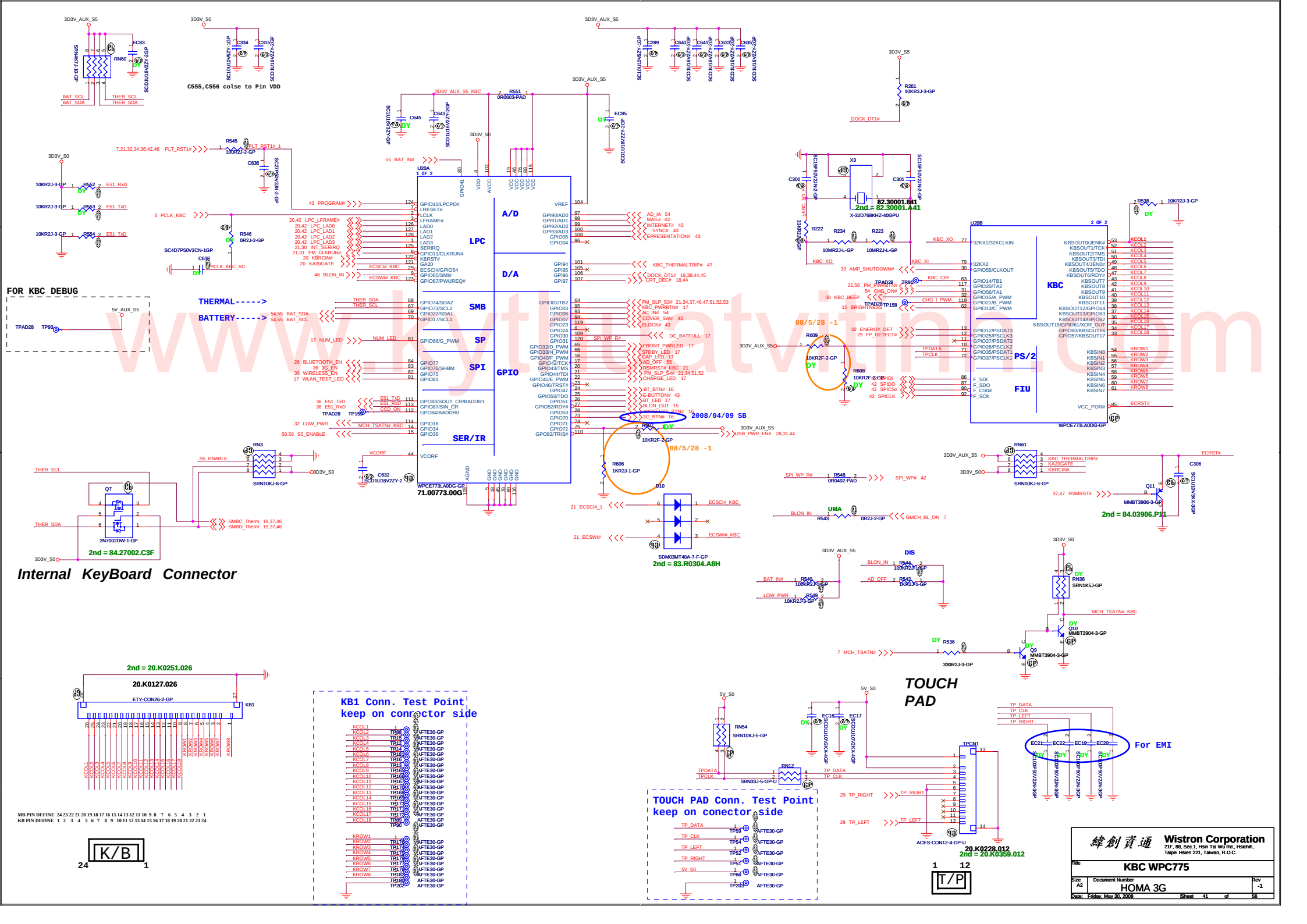
C555,C556 colse to Pin VDD
FOR KBC DEBUG
THERMAL----->
BATTERY----->
Internal KeyBoard Connector
U20A
WPCE773LA0DG-GP
71.00773.00G
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
WPCE773LA0DG-GP
08/5/28 -1
2008/04/09 SB
08/5/28 -1
2nd = 84.27002.C3F
2nd = 84.03906.P11
2nd = 83.R0304.A8H
2nd = 82.30001.A41
82.30001.841
X-32D768KHZ-40GPU
UMA
DIS
TOUCH PAD
KB1 Conn. Test Point keep on connector side
TOUCH PAD Conn. Test Point keep on conector side
For EMI
2nd = 20.K0251.026
20.K0127.026
ETY-CON26-2-GP
20.K0228.012
2nd = 20.K0359.012
ACES-CON12-4-GP-U
MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
K/B
T/P
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775
HOMA 3G
Rev -1
Date: Friday, May 30, 2008
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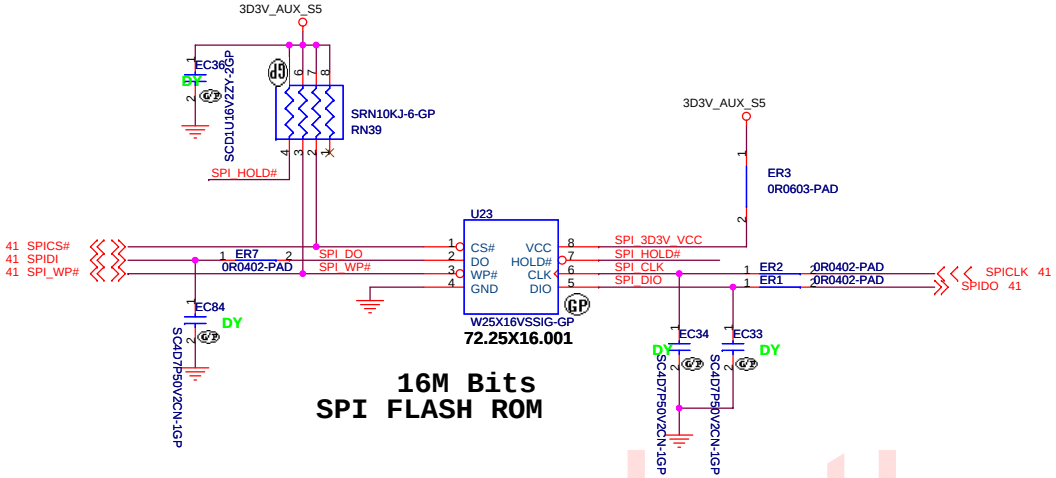
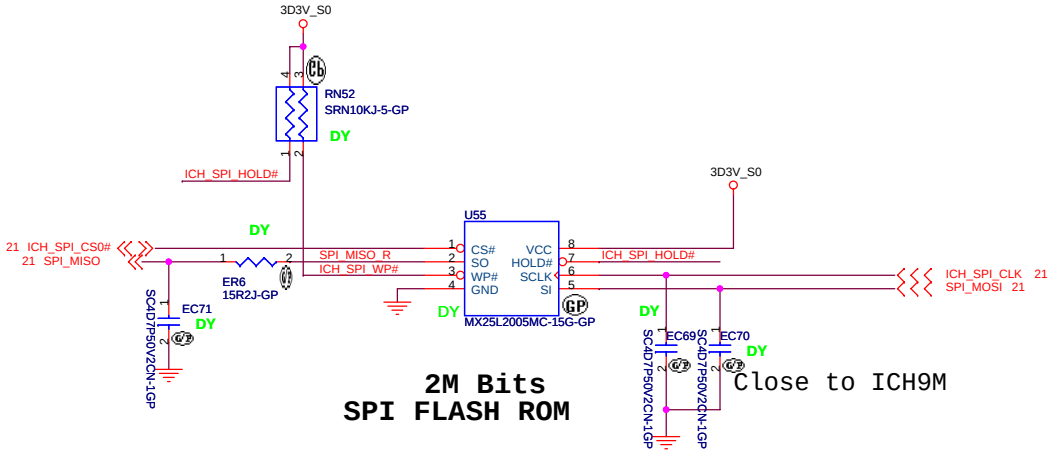
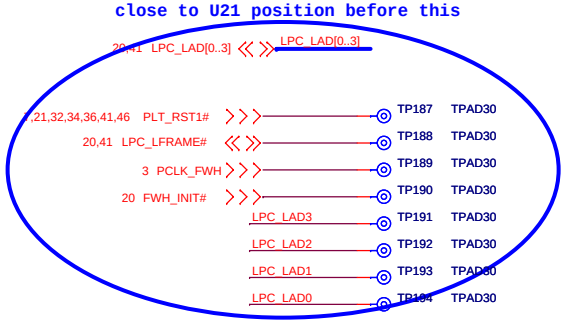




2008/04/11 SB
close to U21 position before this



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Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS		
Size	Document Number: HOMA 3G	Rev: -1
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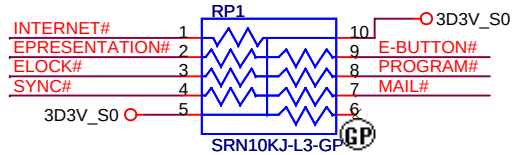
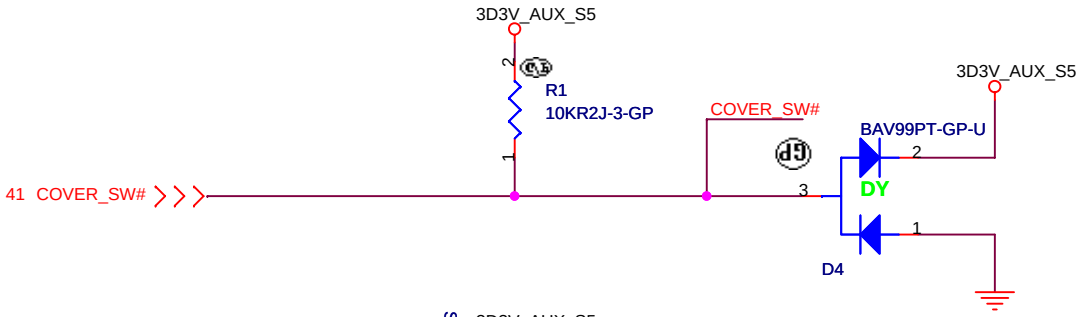
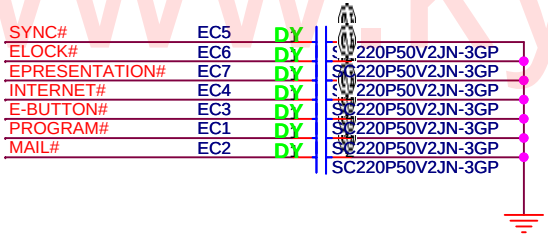
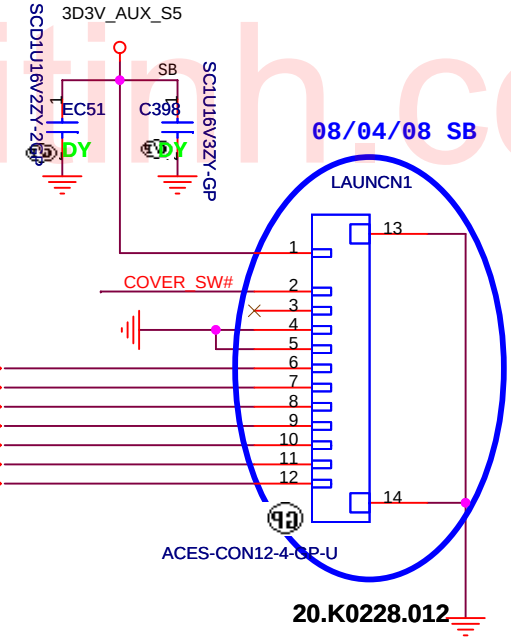
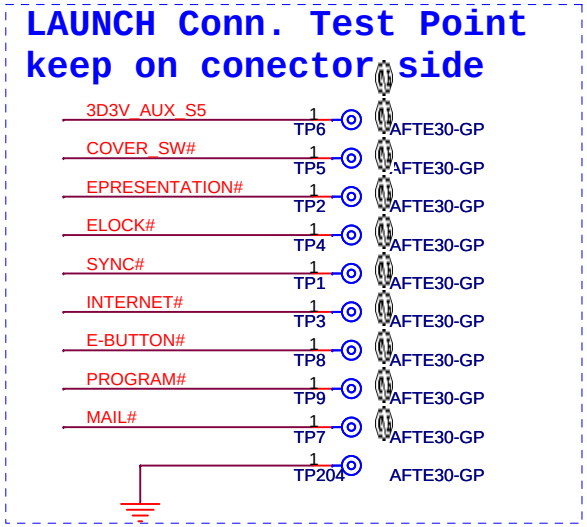
Cover Up Switch



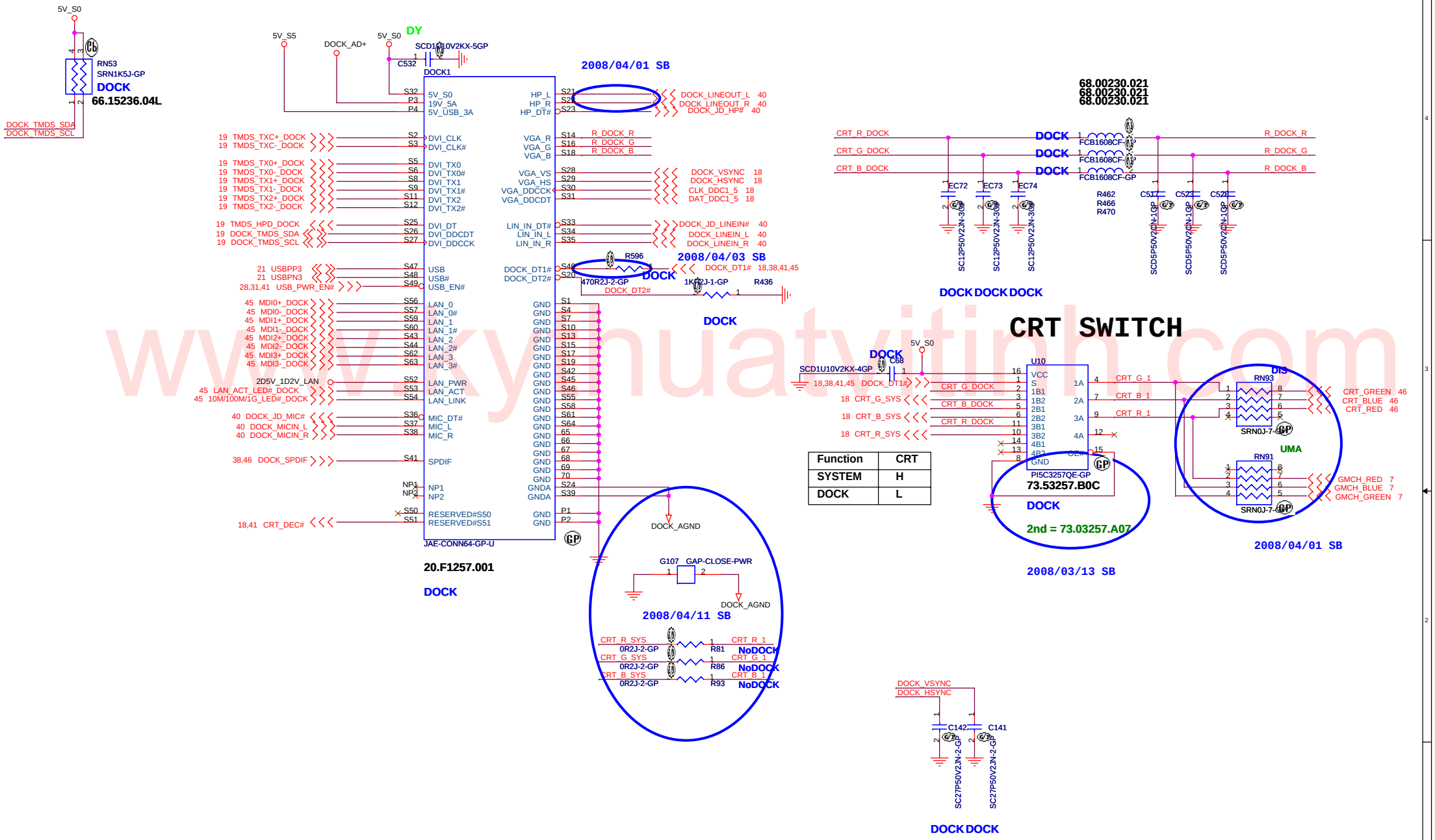






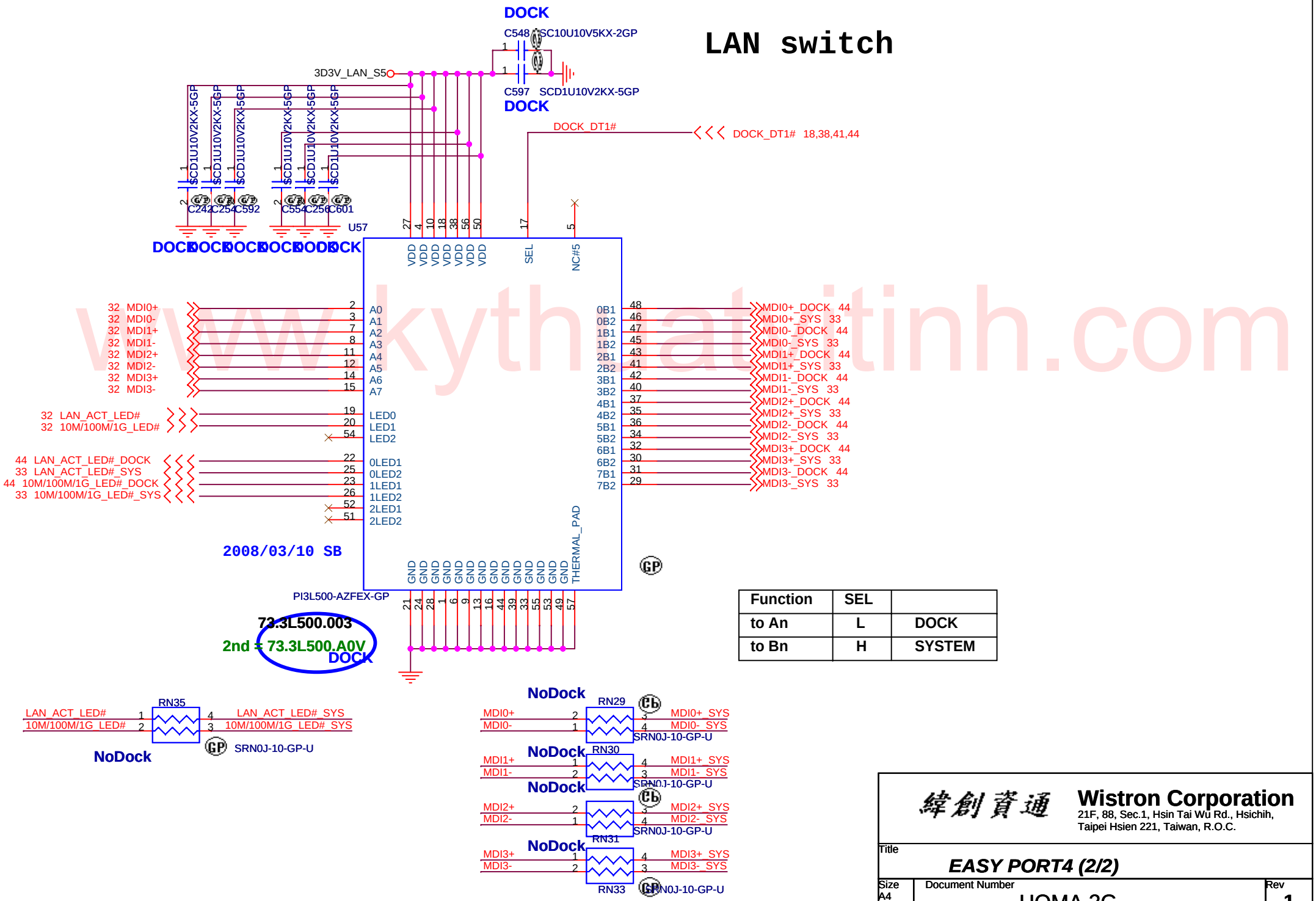


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LAUNCH***	
Size	Document Number **HOMA 3G**	Rev -1
Date: Friday, May 30, 2008	Sheet 43 of 56	



緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***EASY PORT4 (1/2)***
Size: A3	Document Number: **HOMA 3G**
Rev: -1	
Date: Friday, May 30, 2008	Sheet 44 of 56

LAN switch



Function	SEL	
to An	L	DOCK
to Bn	H	SYSTEM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **EASY PORT4 (2/2)**

Size	Document Number	Rev
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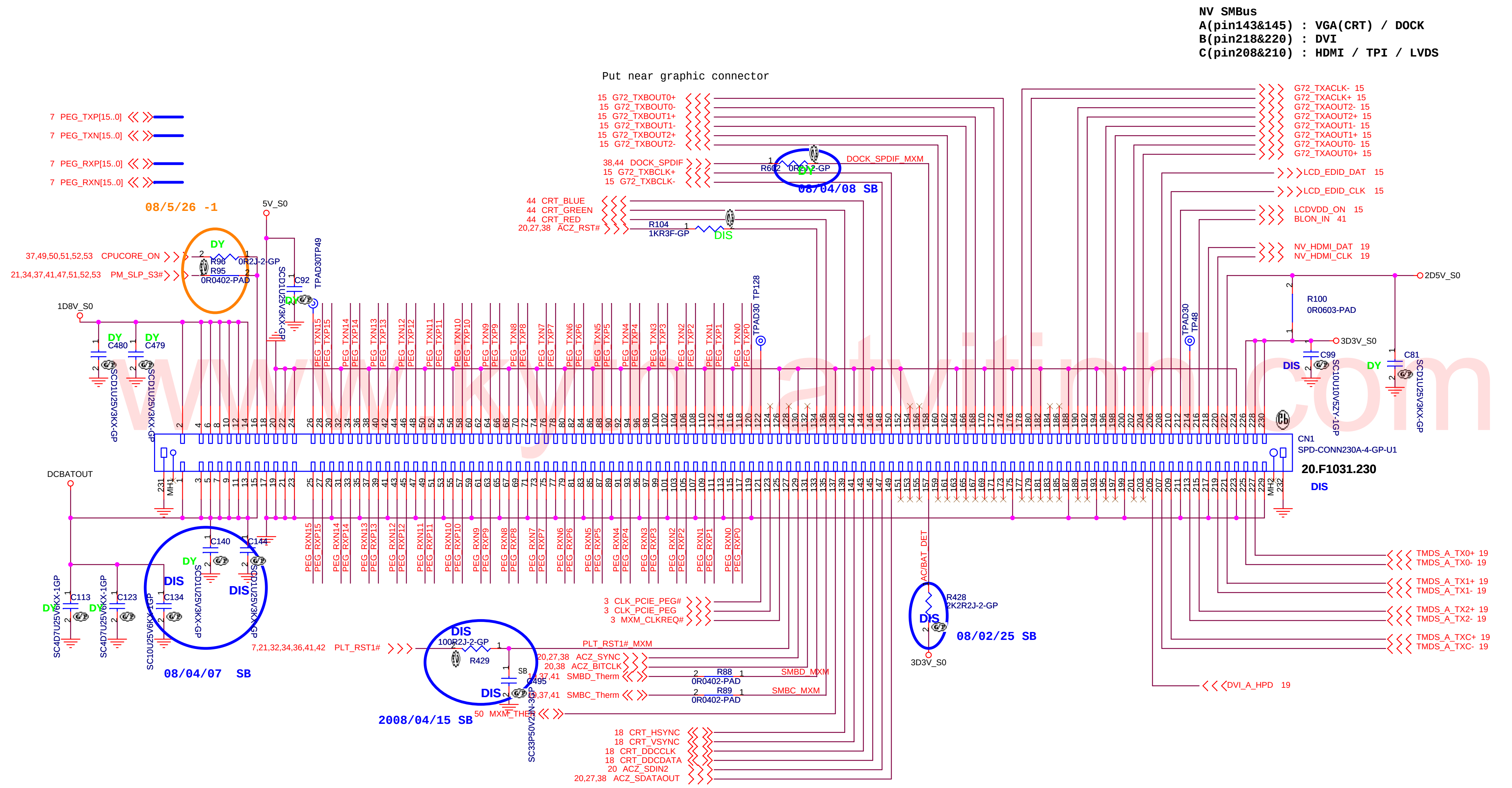
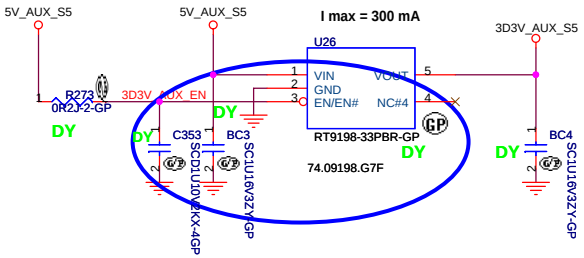


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Graphic MXM CONN		
Size: Custom	Document Number: HOMA 3G	Rev: -1
Date: Friday, May 30, 2008	Sheet 46 of 56	

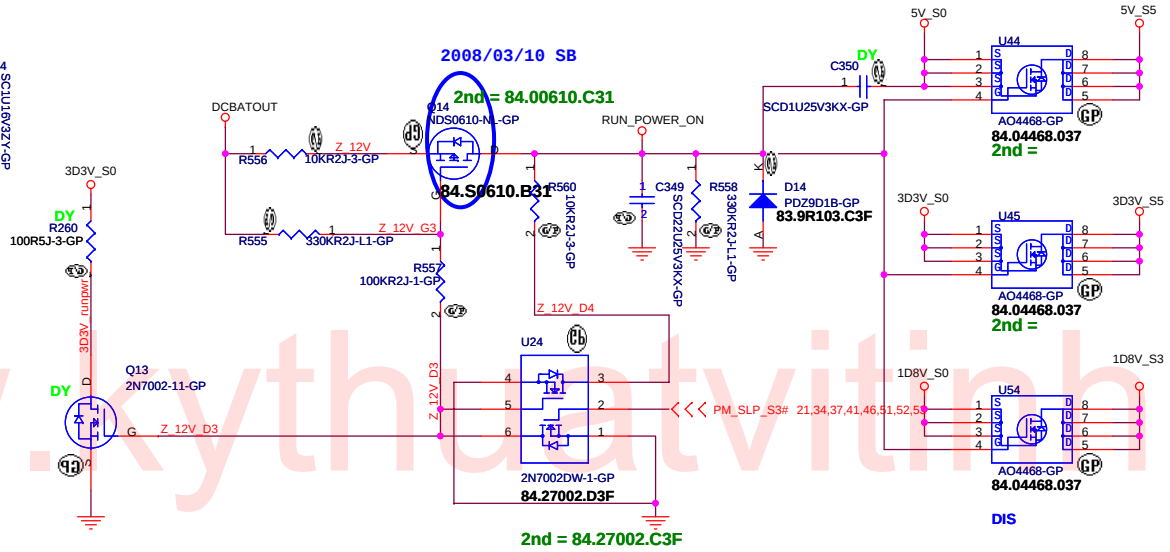
Aux Power

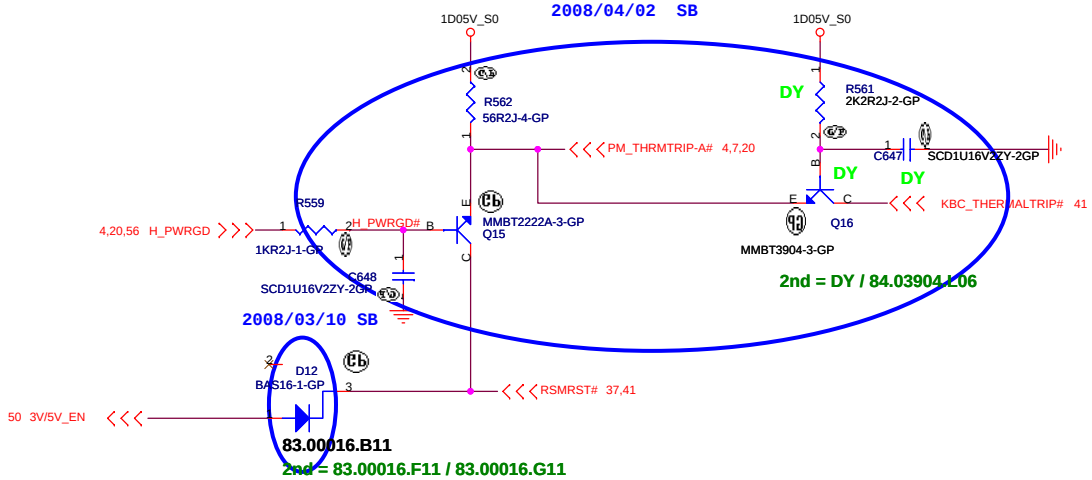
3D3V_AUX_S5



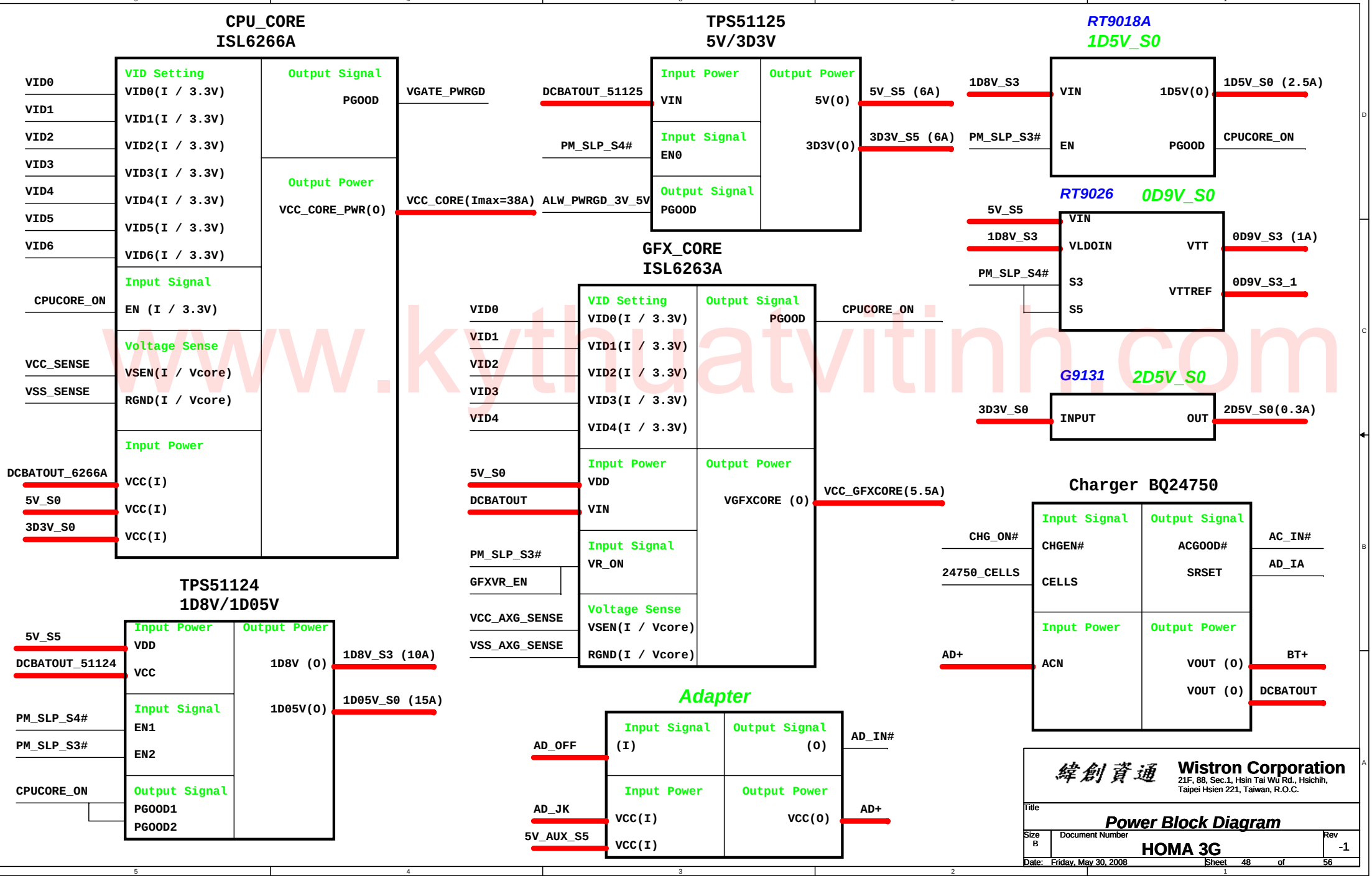
2008/04/02 SB

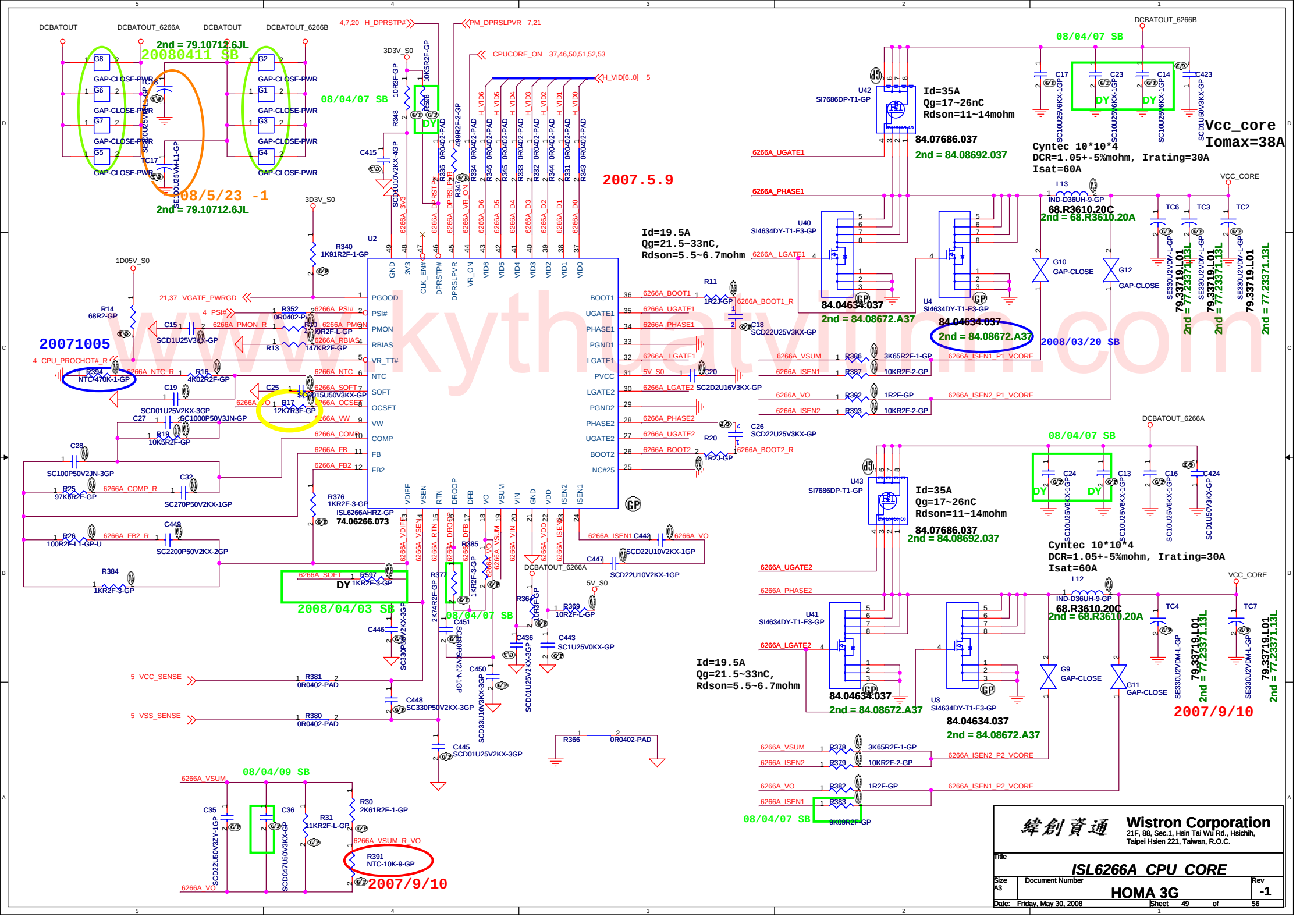
Run Power

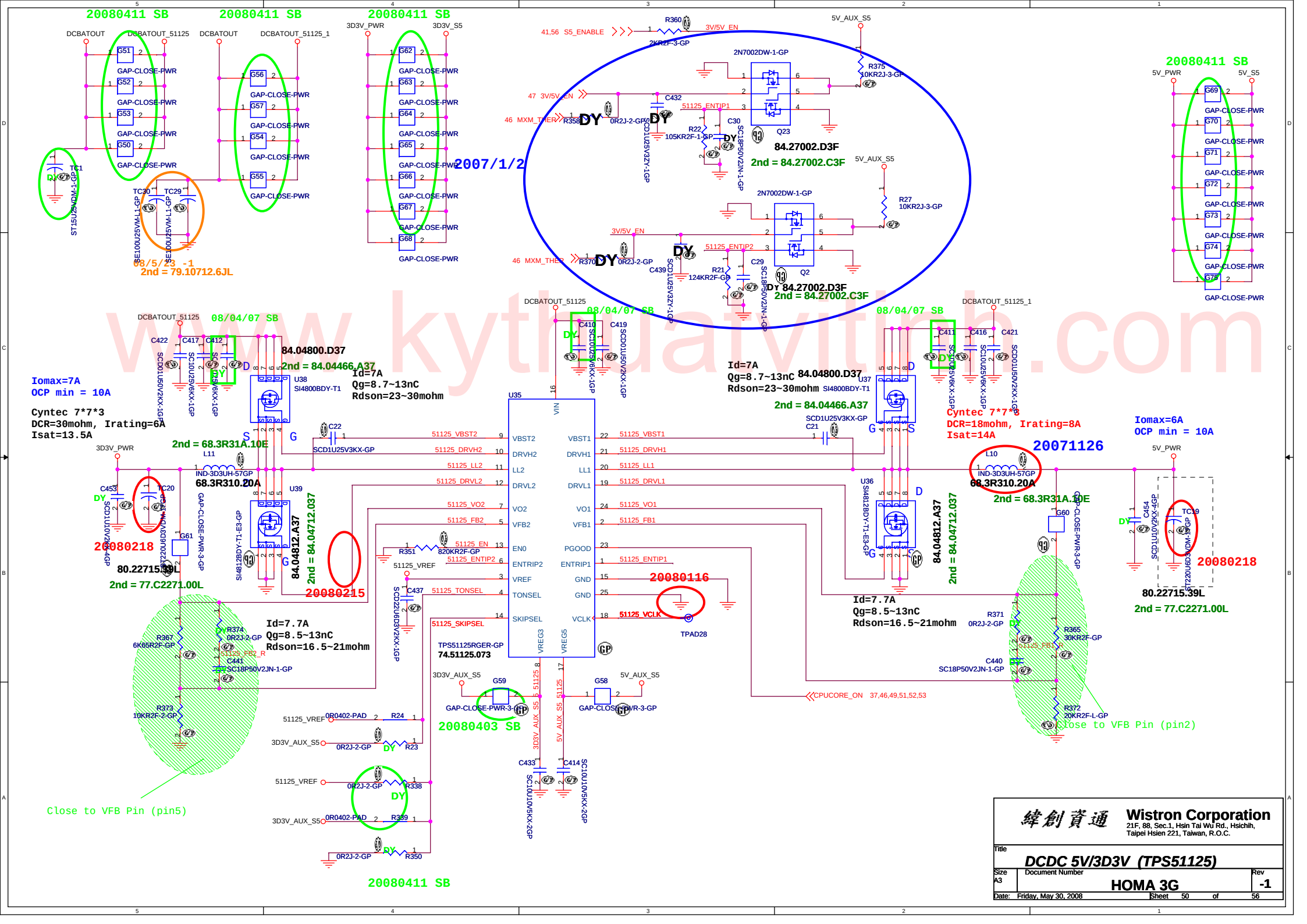


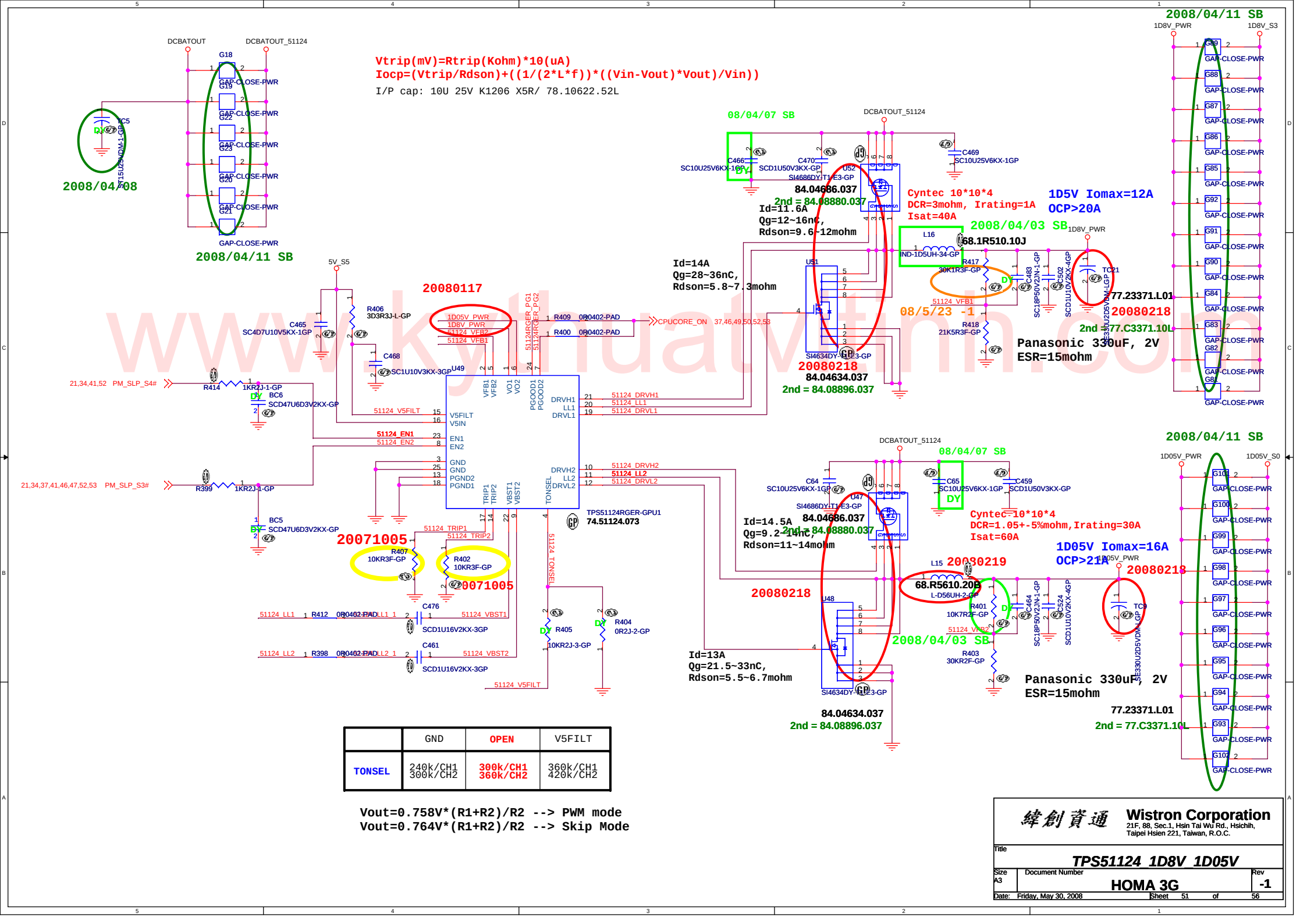


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RUN POWER and 3D3V_AUX_S5	
Size	Document Number: HOMA 3G	Rev: -1
Date: Friday, May 30, 2008	Sheet 47 of 56	



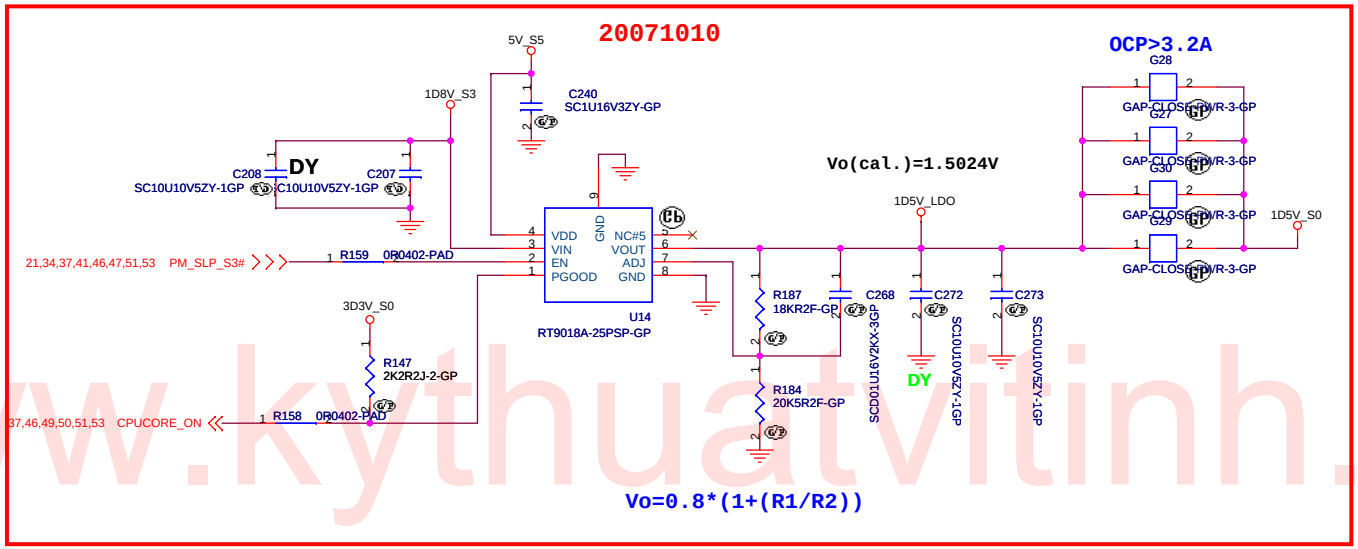

DCBATOUT
DCBATOUT_6266A
DCBATOUT
DCBATOUT_6266B
2nd = 79.10712.6JL
20080411 SB
08/04/07 SB
08/5/23 -1
2nd = 79.10712.6JL
2007.5.9
20071005
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Id=35A
Qg=17~26nC
Rdson=11~14mohm
84.07686.037
2nd = 84.08692.037
84.04634.037
2nd = 84.08672.A37
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
68.R3610.20C
2nd = 68.R3610.20A
79.33719.L01
2nd = 77.23371.13L
2008/03/20 SB
2008/04/03 SB
2007/9/10
08/04/09 SB
74.06266.073
ISL6266AHRZ-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A CPU CORE
HOMA 3G
-1
Friday, May 30, 2008
49
56


20080411 SB
20080411 SB
20080411 SB
20080411 SB
2007/1/2
08/5/23 -1
2nd = 79.10712.6JL
08/04/07 SB
08/04/07 SB
08/04/07 SB
84.04800.D37
2nd = 84.04466.A37
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Iomax=7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
2nd = 68.3R31A.10E
68.3R310.20A
20080218
80.22715.39L
2nd = 77.C2271.00L
20080215
84.04812.A37
2nd = 84.04712.037
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
20080116
TPS51125RGER-GP
74.51125.073
20080403 SB
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
20080411 SB
Cyntec 7*7*3
DCR=18mohm, Irating=8A
Isat=14A
20071126
Iomax=6A
OCP min = 10A
2nd = 68.3R31A.10E
80.22715.39L
2nd = 77.C2271.00L
20080218
84.27002.D3F
2nd = 84.27002.C3F
DY 84.27002.D3F
2nd = 84.27002.C3F
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
HOMA 3G
-1
Friday, May 30, 2008
50
56

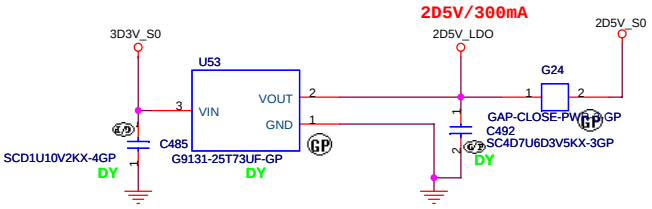


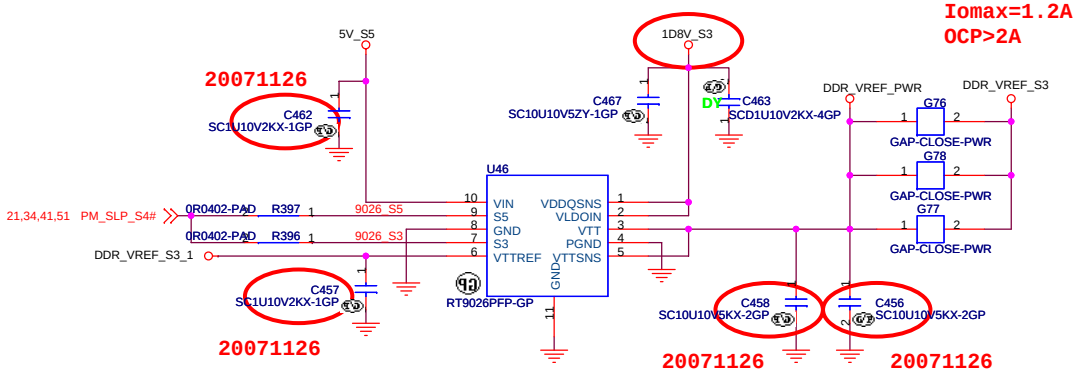
	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

1D5V_S0
Iomax=2.5A

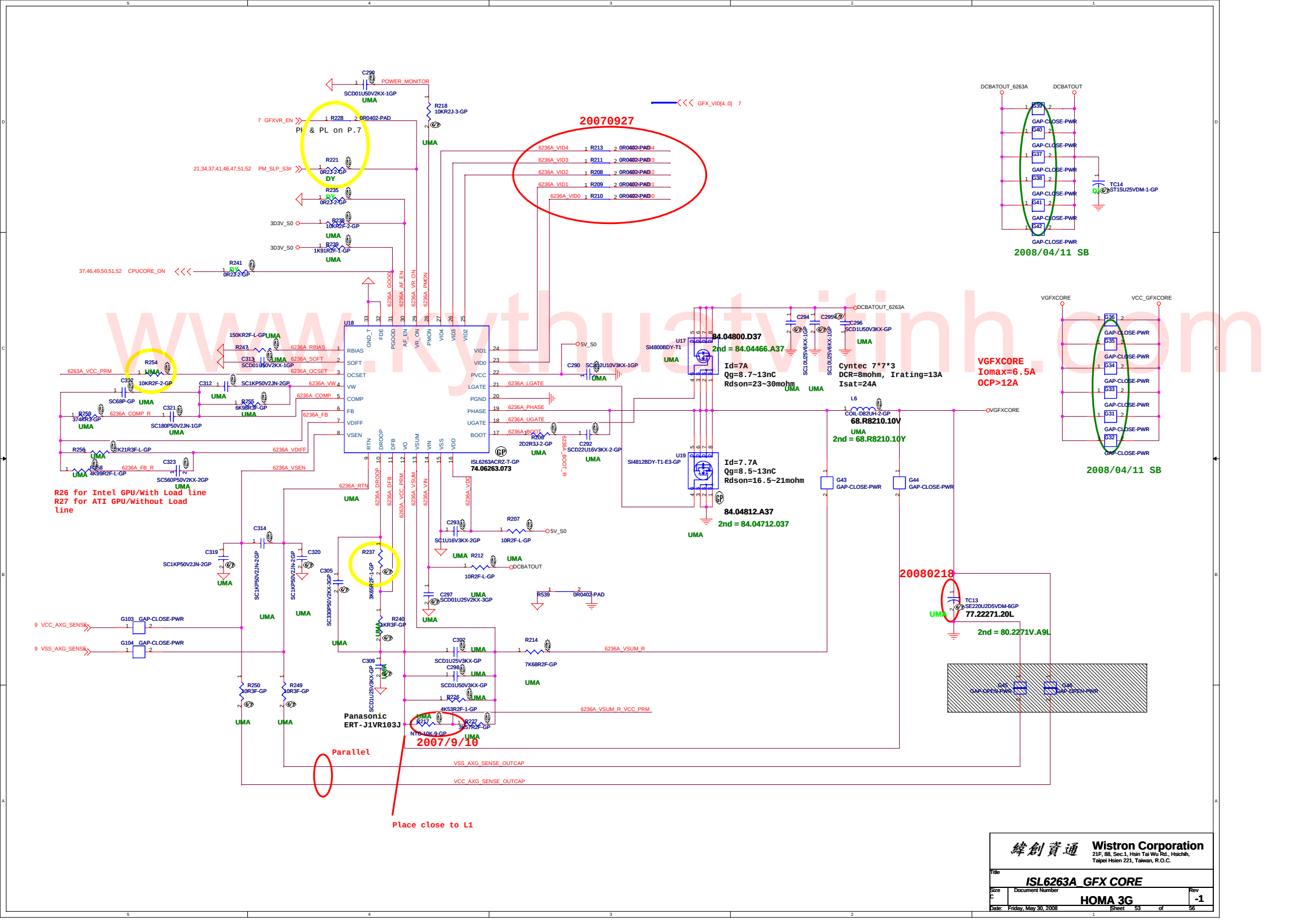


2D5V_S0
Iomax=0.3A

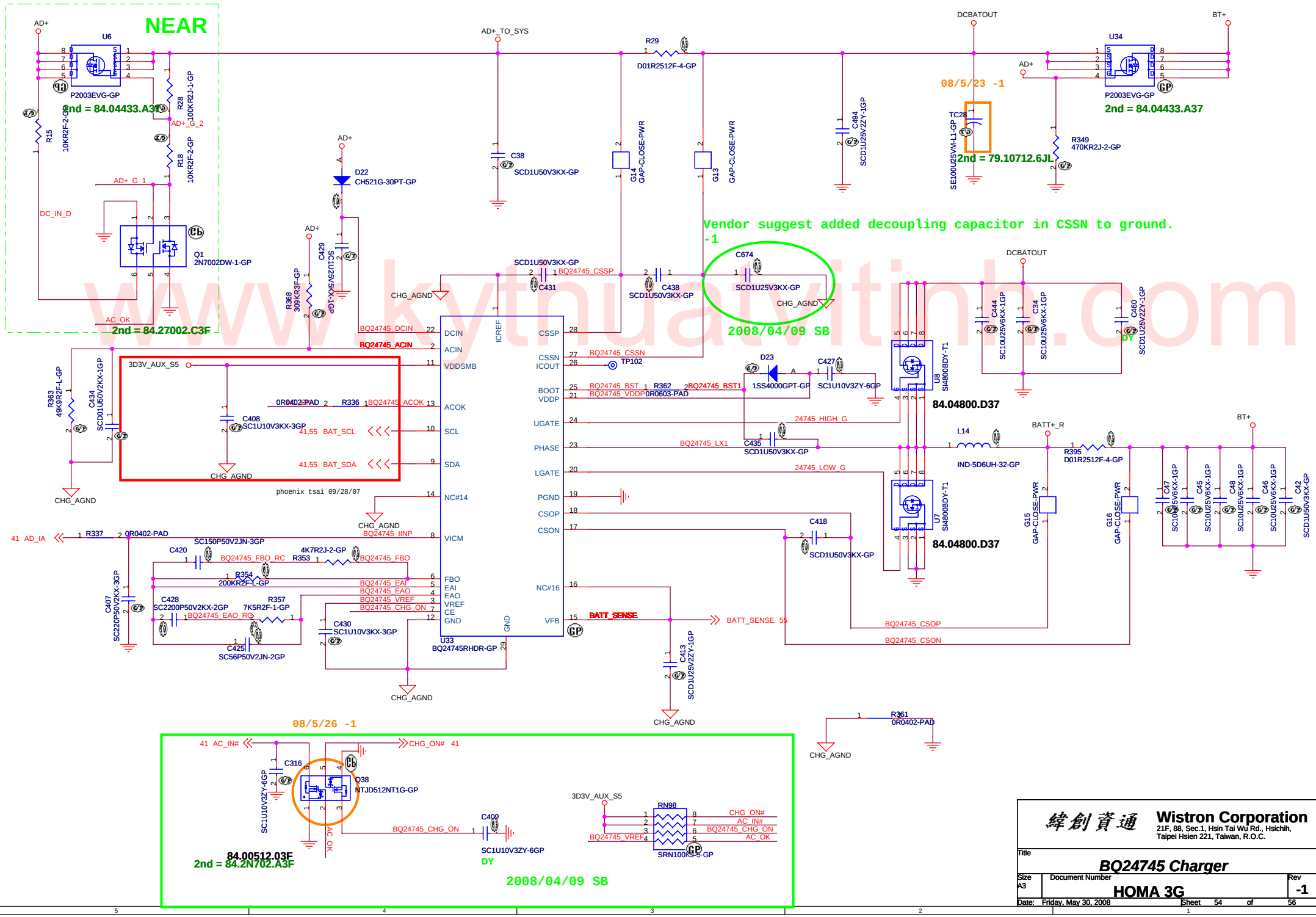




緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D5V & 0D9V & 2D5V		
Size: A3	Document Number: HOMA 3G	Rev: -1
Date: Friday, May 30, 2008	Sheet 52 of 56	



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ISL6263A_GFX CORE	
Size: C	Document Number: HOMA 3G
Rev: -1	
Date: Friday, May 30, 2008	Sheet 53 of 56



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BQ24745 Charger	
Size A3	Document Number HOMA 3G	Rev -1
Date: Friday, May 30, 2008	Sheet 54 of 56	

2008/03/27 SB add 2nd source

1Pin=1A

Adaptor in to generate DCBATOUT

DCIN1
MLX-CON11-1-GP
20.F0070.011
2nd = 20.F1267.011
DOCK_AD+
AD_JK
C33
SCD1U50V3ZY-GP
D7
S10P40PT-GP-U
2nd =
08/5/26 -1
AD_JK+
D6
P6SMB20A-GP
2nd = 83.P6SBM.BAG
C37
SCD1U50V3ZY-GP
Q21
PDTA124EU-1-GP
R356
200KR2J-L1-GP
C426
SC1U50V5ZY-1-GP
U5
P2003EVG-GP
AD+
AD+ 2
2nd = 84.04433.A37
R355
100KR2J-1-GP
2nd = 84.00124.N1K
AD_OFF#_JK
Q22
PDTC124EU-1-GP
D5
S10P40PT-GP-U
R101
10KR2J-3-GP
2nd =
41 AD_OFF

KB Conn. Test Point keep on connector side

AD_JK
TP183 AFTE30-GP
AD_JK
TP207 AFTE30-GP
TP206 AFTE30-GP
TP205 AFTE30-GP

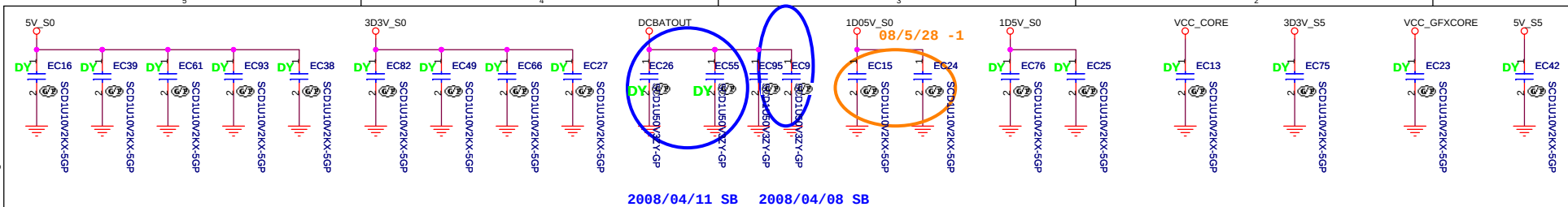
MAIN BATTERY CONNECTOR

3D3V_AUX_S5
D19
BAV99PT-GP-U
D20
BAV99PT-GP-U
D21
BAV99PT-GP-U
2008/03/05 SB add 2nd source
08/04/01 SB
RN50
SRN33J-7-GP
41,54 BAT_SCL
41,54 BAT_SDA
41 BAT_IN#
BATA_SCL_1
BATA_SDA_1
BAT_IN#_1
BT+
D32
BZG05C3V3-GP-U1
EC59
EC60
EC94
EC56
SCD1U50V3ZY-GP
ESC1000P50V3JN-GP
EC58
EC57
SC10P50V2JN-4GP
BAT1
SYN-CON7732-GP-U
20.81021.007
2nd = 20.81049.007
08/5/26 -1
08/04/08 SB
54 BATT_SENSE
R42
0R0402-PAD

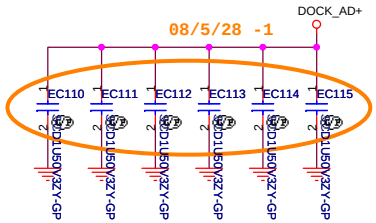
BAT1 Conn. Test Point keep on connector side

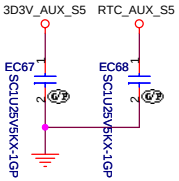
BATA_SCL_1 TP209 AFTE30-GP
BATA_SDA_1 TP210 AFTE30-GP
BAT_IN#_1 TP211 AFTE30-GP
BATT_SENSE TP212 AFTE30-GP
BT+ TP213 AFTE30-GP
BT+ TP214 AFTE30-GP
TP216 AFTE30-GP
TP217 AFTE30-GP

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AD&BTY CONNECTER	
Size	Document Number HOMA 3G	Rev -1
Date: Friday, May 30, 2008	Sheet 55 of 56	

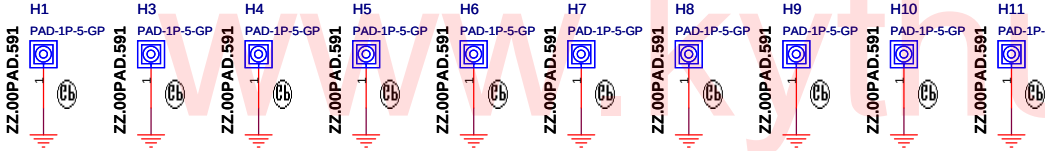


2008/04/11 SB 2008/04/08 SB



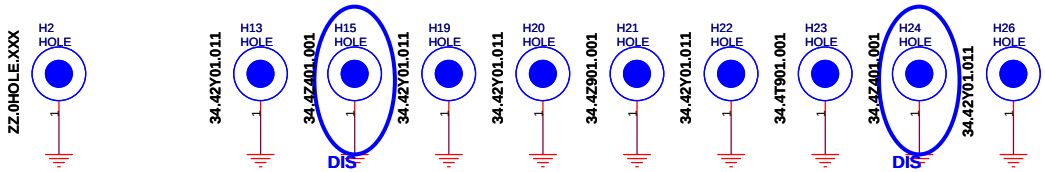


Stand off Location

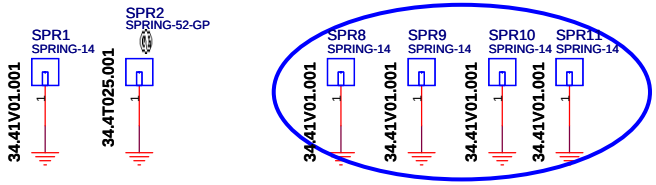


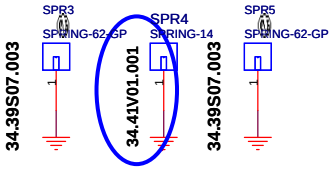
2008/03/20 SB

2008/04/14 SB



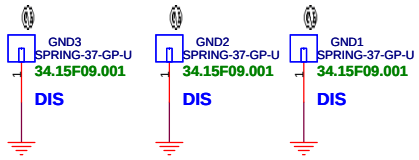
2008/04/09 SB 2008/04/14 SB



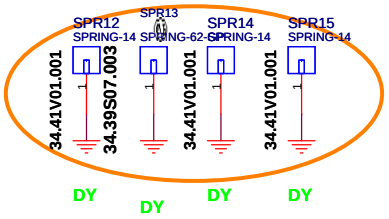


2008/04/14 SB

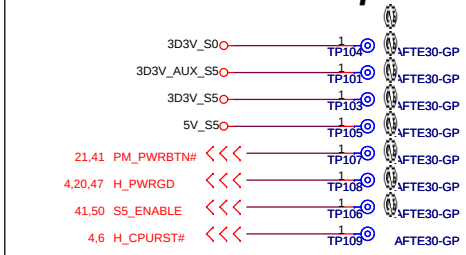
SPRING ON BOTTOM



08/5/29 -1



Check test point



Test Point放在Dimm Door打開可量測處

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	EMI/Spring/Boss	
Size	Document Number: HOMA 3G	Rev: -1
Date: Friday, May 30, 2008	Sheet 56 of 56	