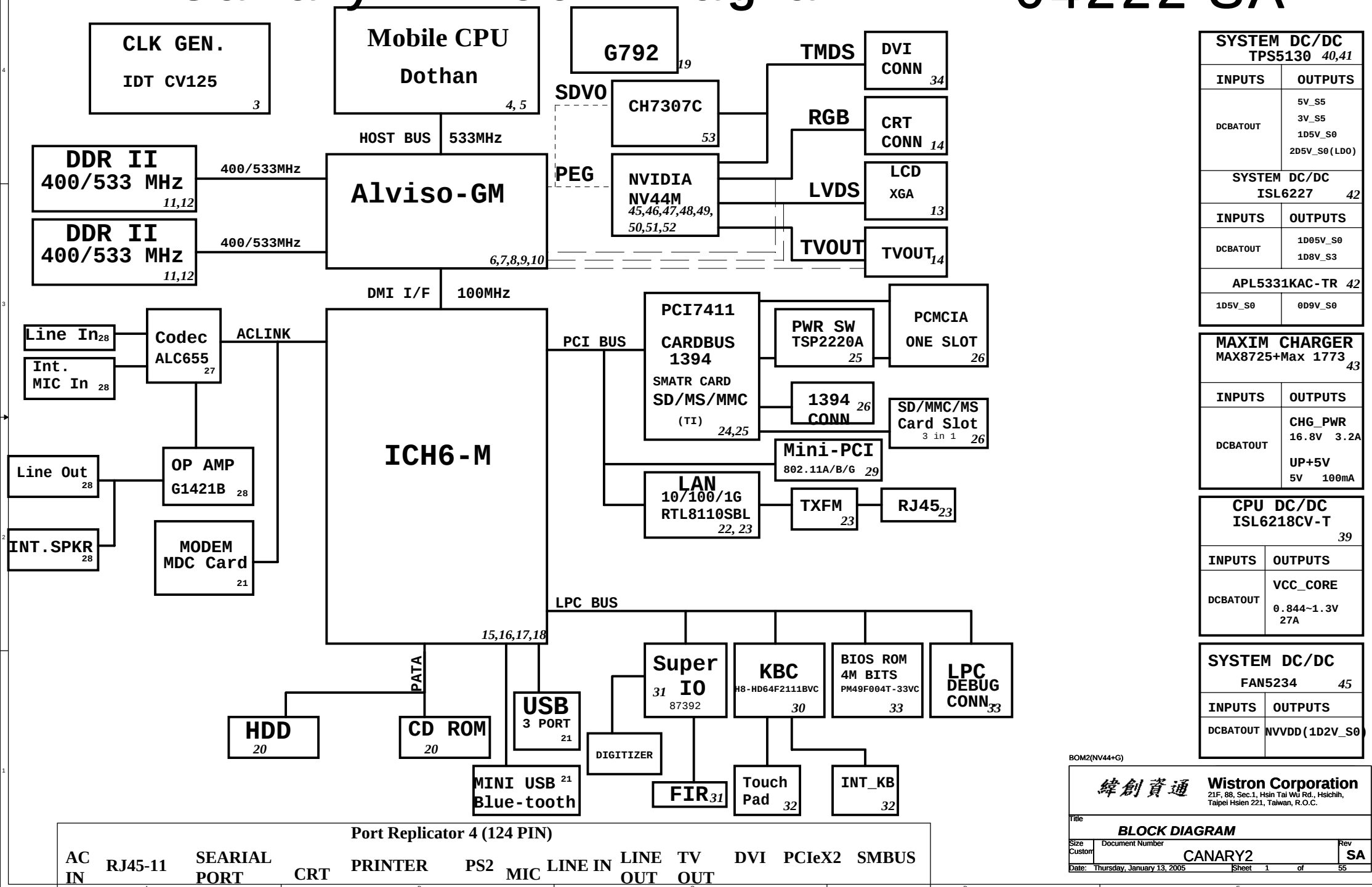


Canary2 Block Diagram

04222-SA



SYSTEM DC/DC TPS5130 40,41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5 1D5V_S0 2D5V_S0(LDO)

SYSTEM DC/DC ISL6227 42	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

APL5331KAC-TR 42	
1D5V_S0	0D9V_S0

MAXIM CHARGER MAX8725+Max 1773 43	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 16.8V 3.2A UP+5V 5V 100mA

CPU DC/DC ISL6218CV-T 39	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

SYSTEM DC/DC FAN5234 45	
INPUTS	OUTPUTS
DCBATOUT	NVVD(1D2V_S0)

BOM2(NV44+G)

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Title	BLOCK DIAGRAM
Size	Document Number
Custom	CANARY2
Date	Thursday, January 13, 2005
Sheet	1 of 55
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Alviso Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott 1 = Dothan (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

CY28411ZC Spread Spectrum Select

SS3	SS2	SS1	Spread Mode	Spread Amount%
0	0	0	Down	0.8
0	0	1	Down	1.25
0	1	0	Down	1.75
0	1	1	Down	2.5
1	0	0	Center	+ -0.3
1	0	1	Center	+ -0.5
1	1	0	Center	+ -0.8
1	1	1	Center	+ -1.25

PCI Routing

	IDSEL	IRQ	REQ/GNT
7411	25	B.F.G	0
MiniPCI	21	E	1
LAN	23	E	2

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

BOM2(NV44+G)

緯創資通

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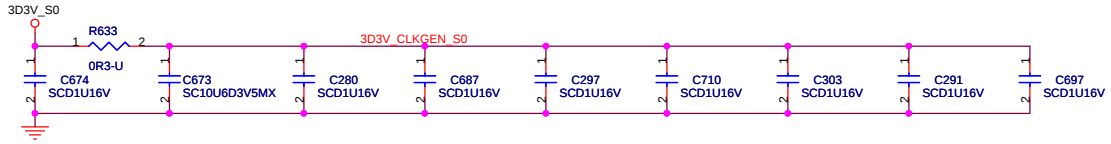
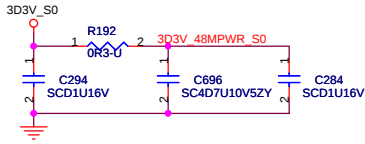
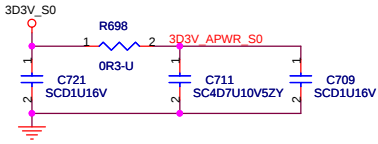
TitleITP

SizeA3

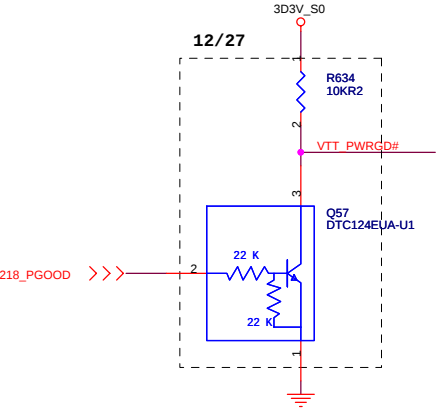
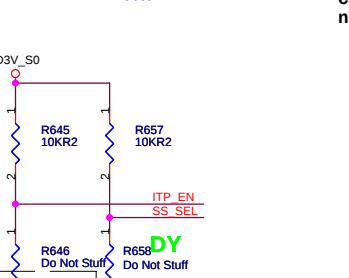
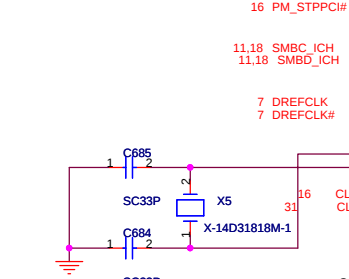
Document NumberCANARY2

RevSA

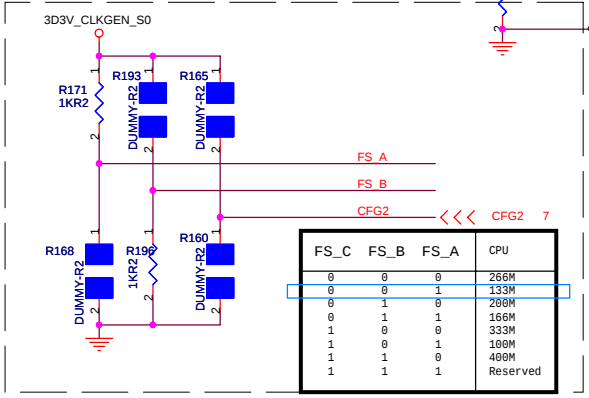
Date: Thursday, January 13, 2005Sheet 2 of 55



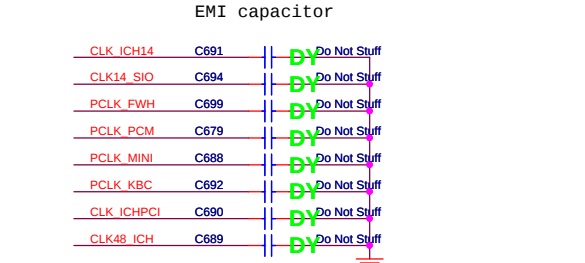
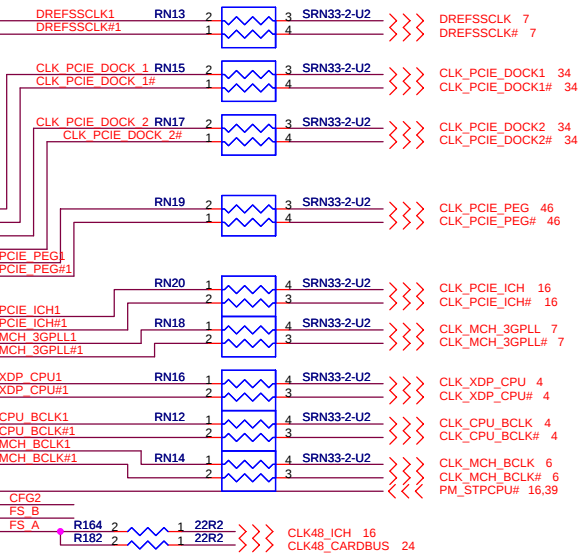
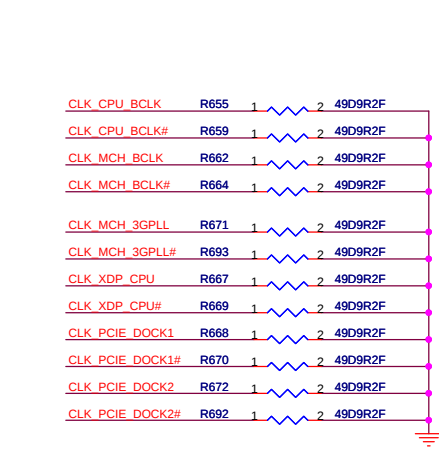
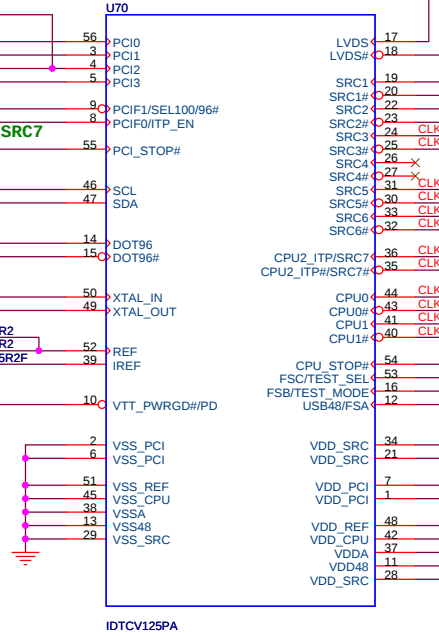
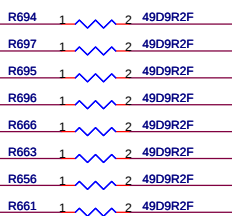
PCLK_PCM & PCLK_SIO
need equal length



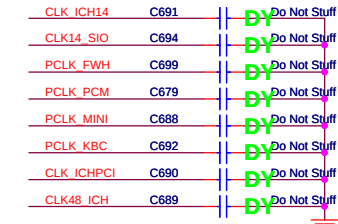
IN (3D3V_S0)	EN (6218_PG00D)	OUT (VTT_PWRGD#)
H	L	H
X	H	H1 - Z



CLK_ICH14 & CLK14_SIO
need equal length



EMI capacitor

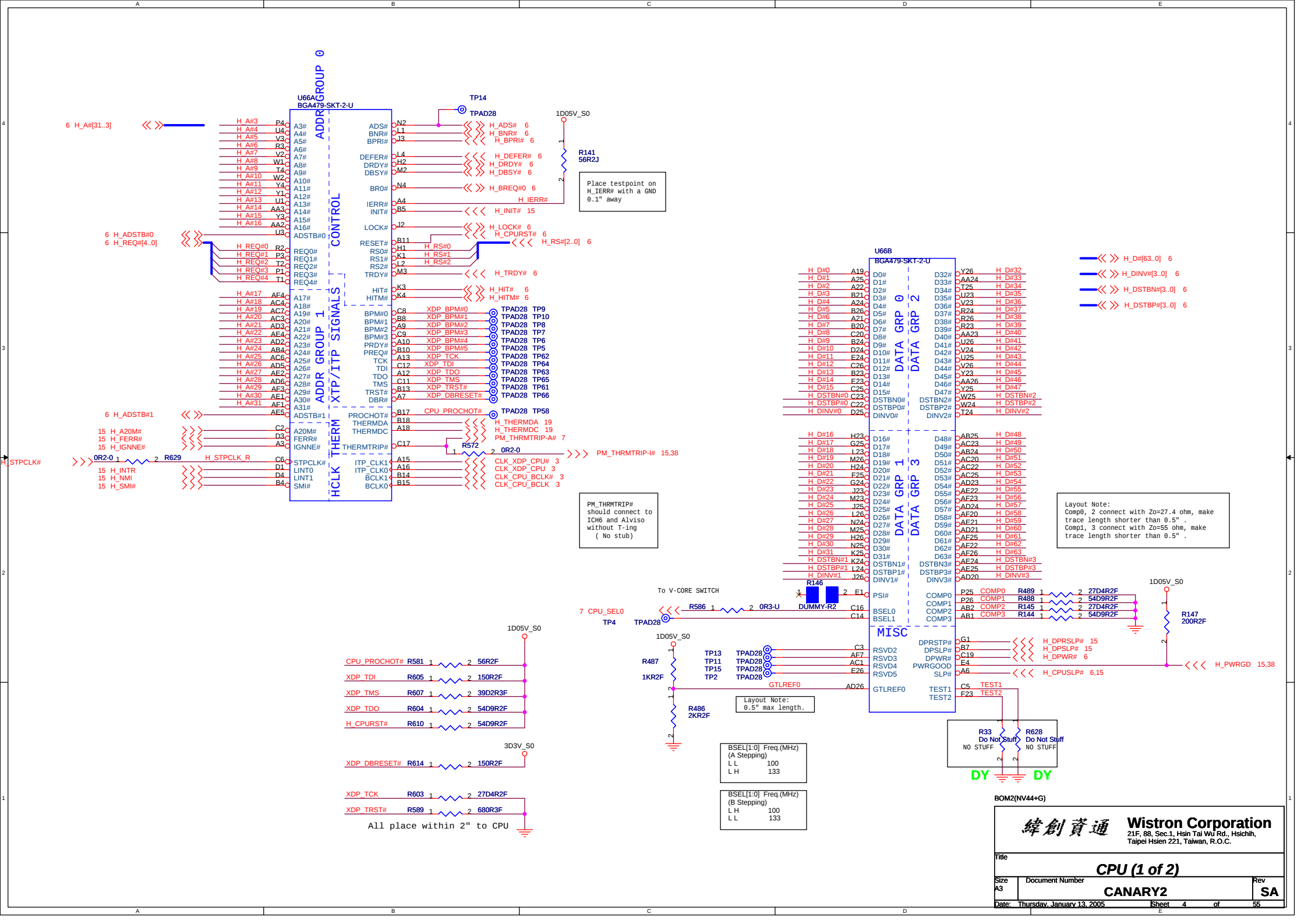


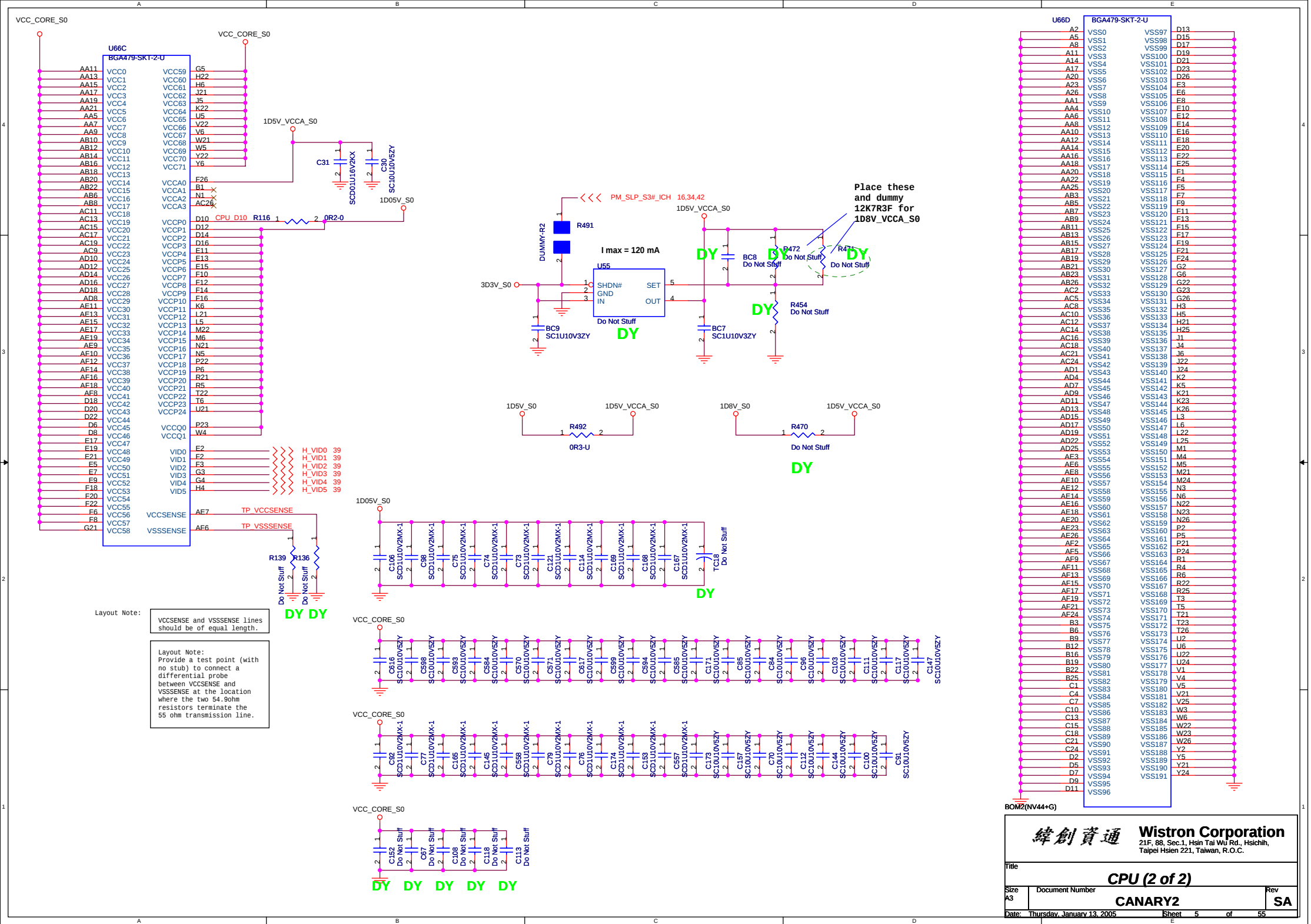
BOM2(NV44+G)

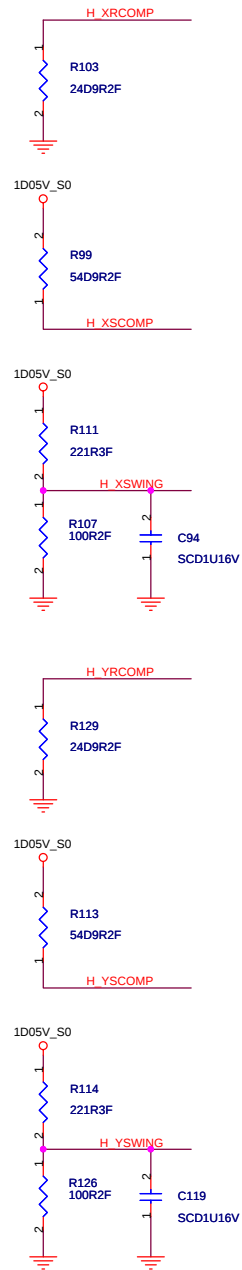
Title		Rev	
Size		Document Number	
A3		CANARY2	
Date		Sheet	
Thursday, January 13, 2005		3 of 55	

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Taipei Hsien 221, Taiwan, R.O.C.

Clock Generator - IDT125



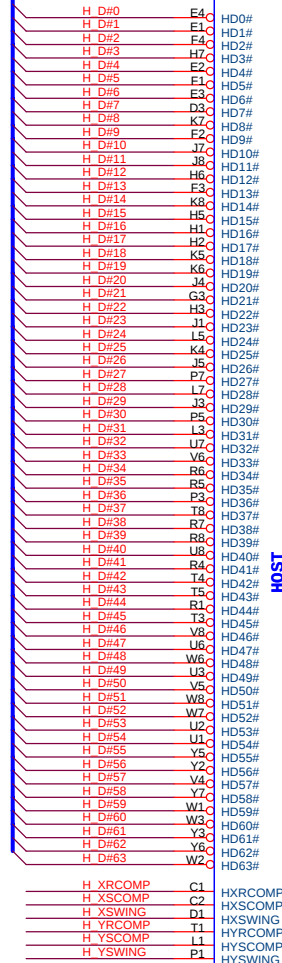




Place them near to the chip

4 H_D#[63..0]

<<<>>>

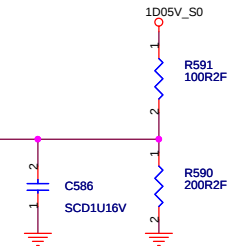


U16A

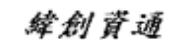
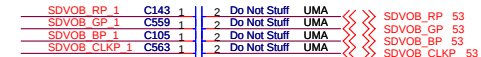
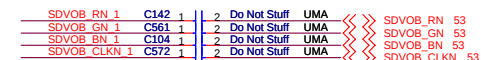
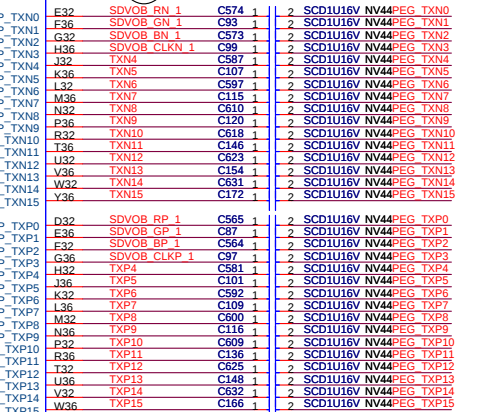
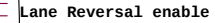
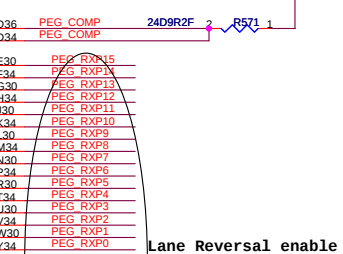
HOST

710GMCH.0XU

<<<>>> H_A#[31..3] 4

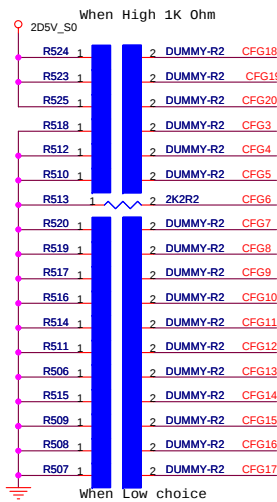
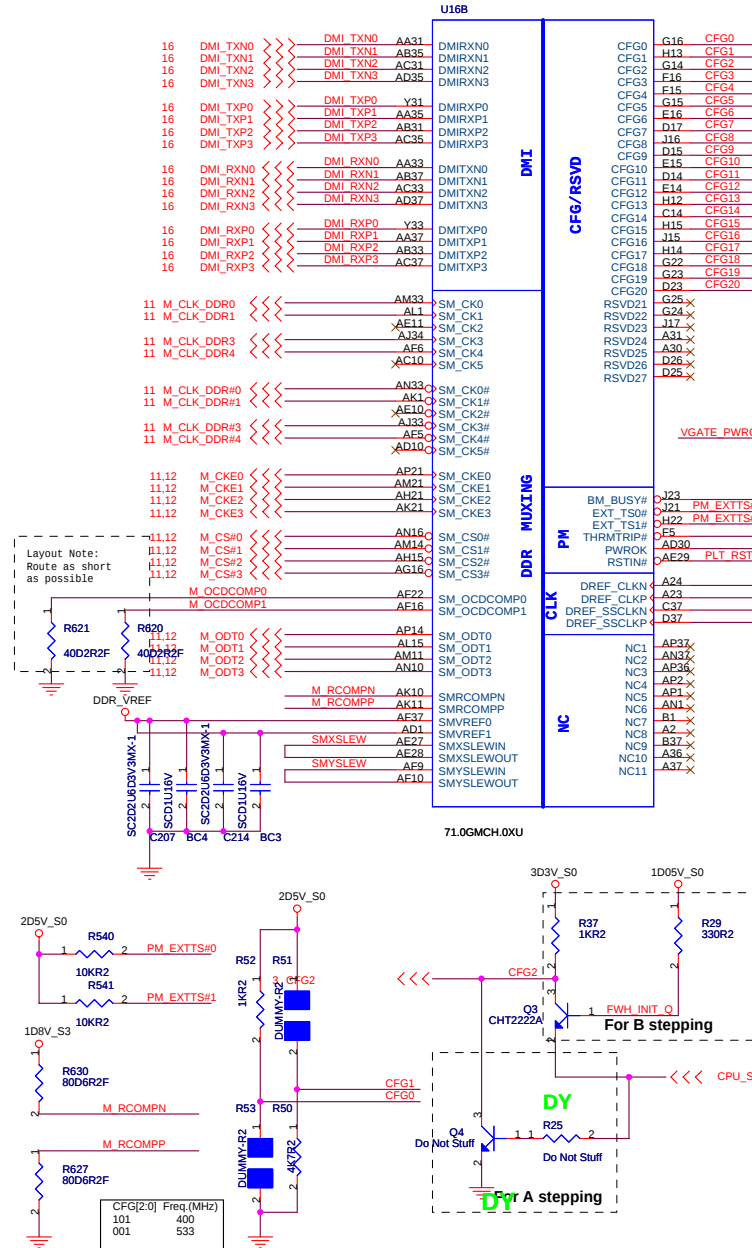
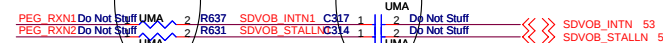
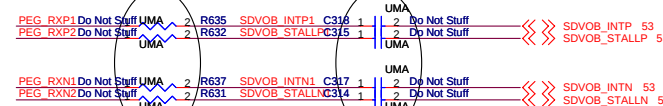


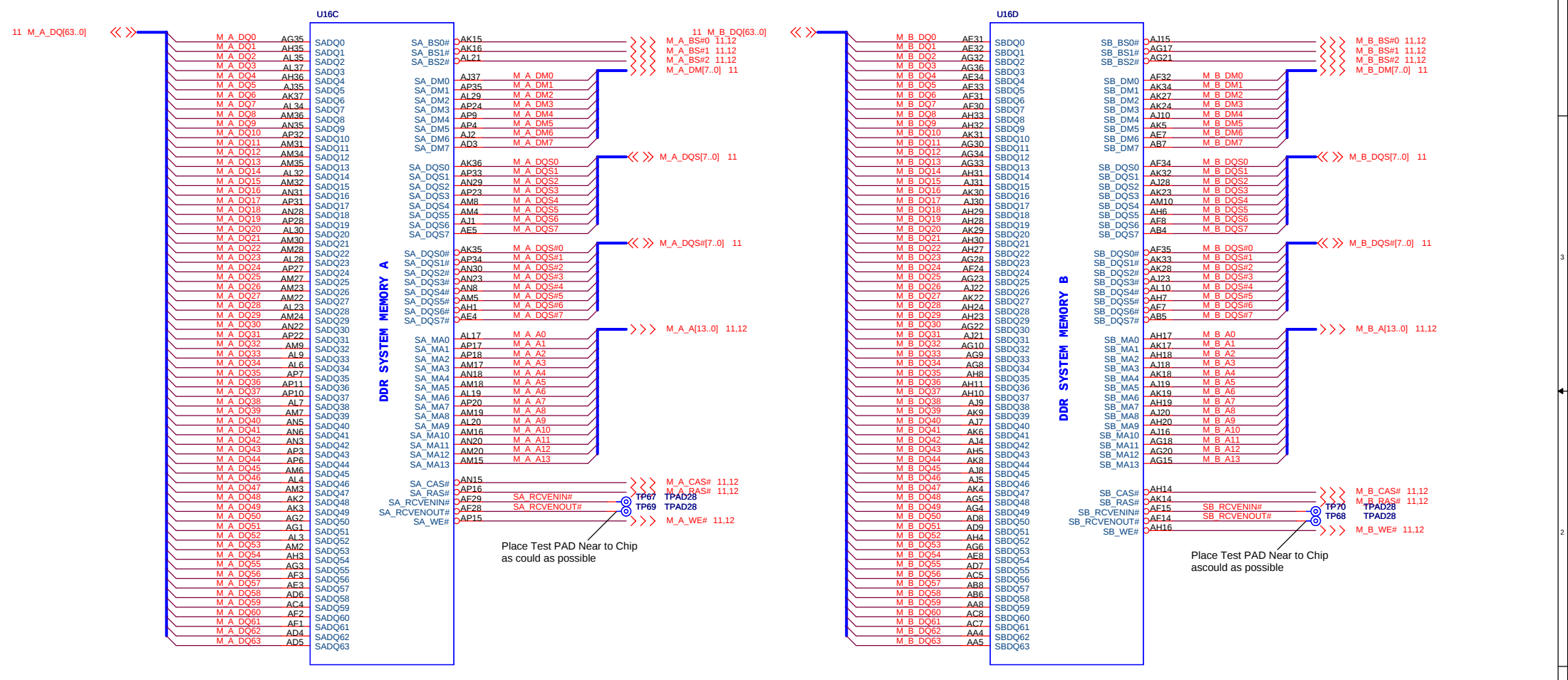
BOM2(NV44+G)

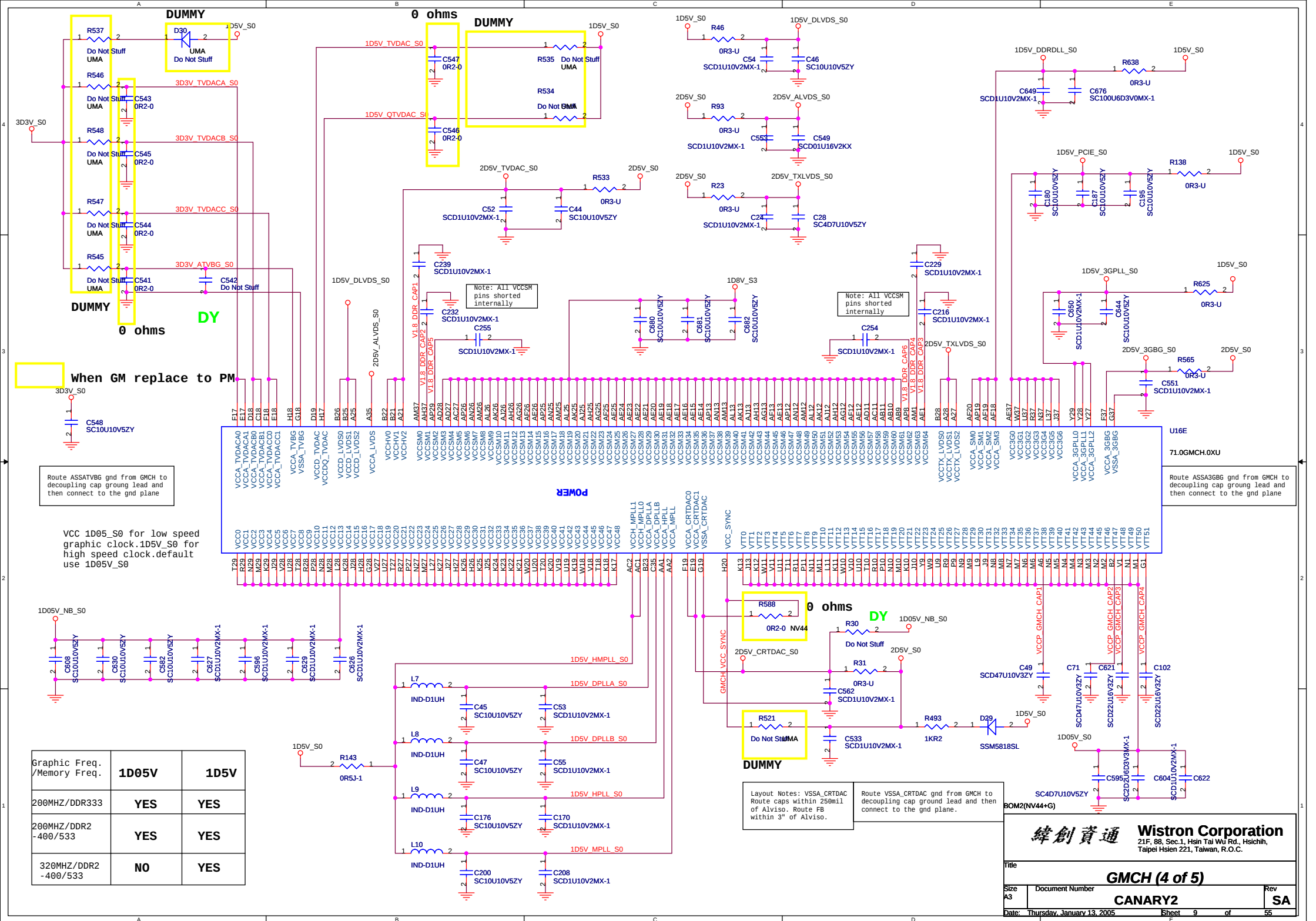
**GMCH (2 of 5)**

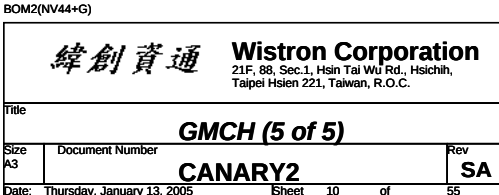
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GMCH (2 of 5)			
Size Custom	Document Number		Rev
	CANARY2		SA
Date:	Thursday, January 13, 2005		Sheet 7 of 55

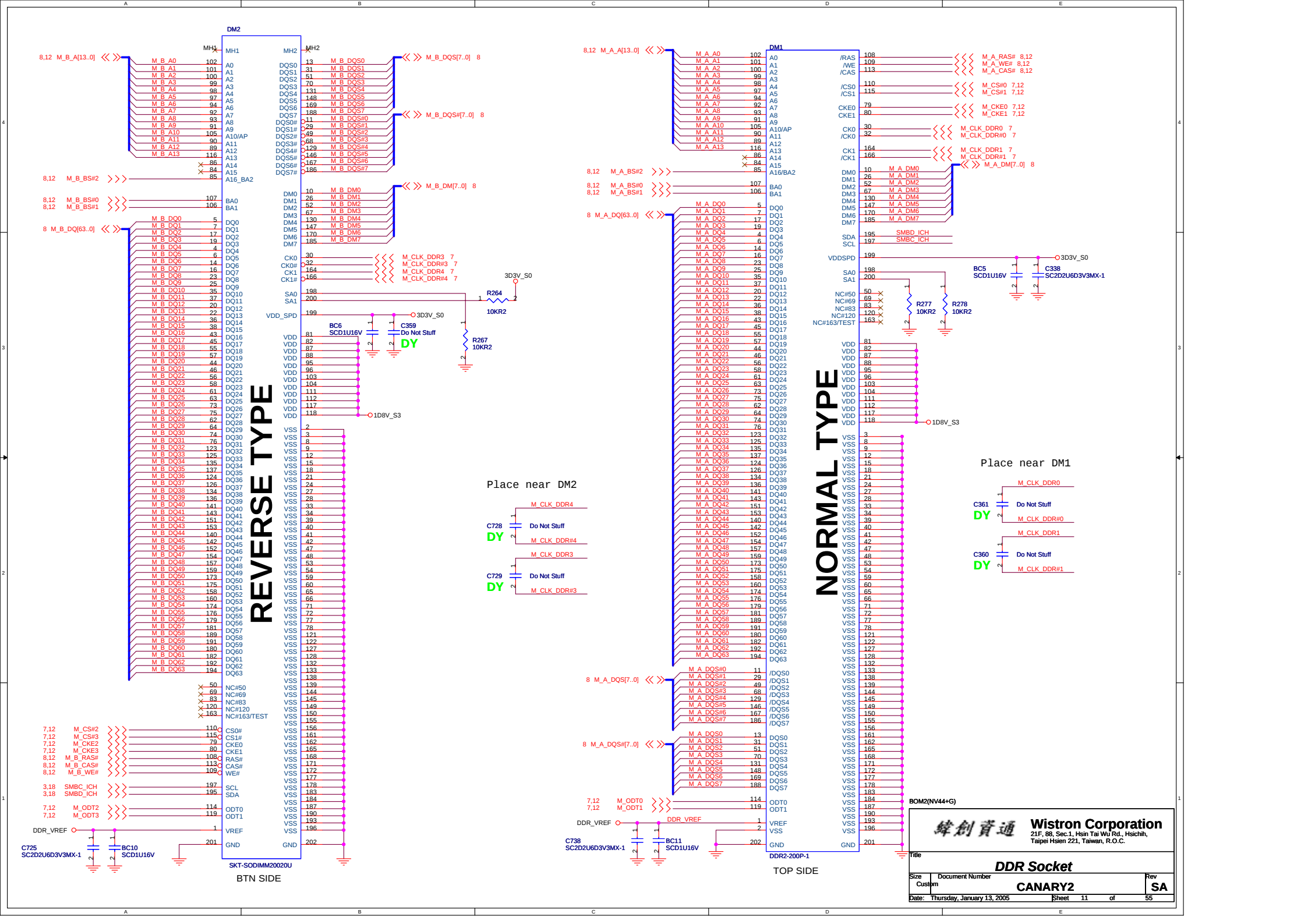
Place near U104





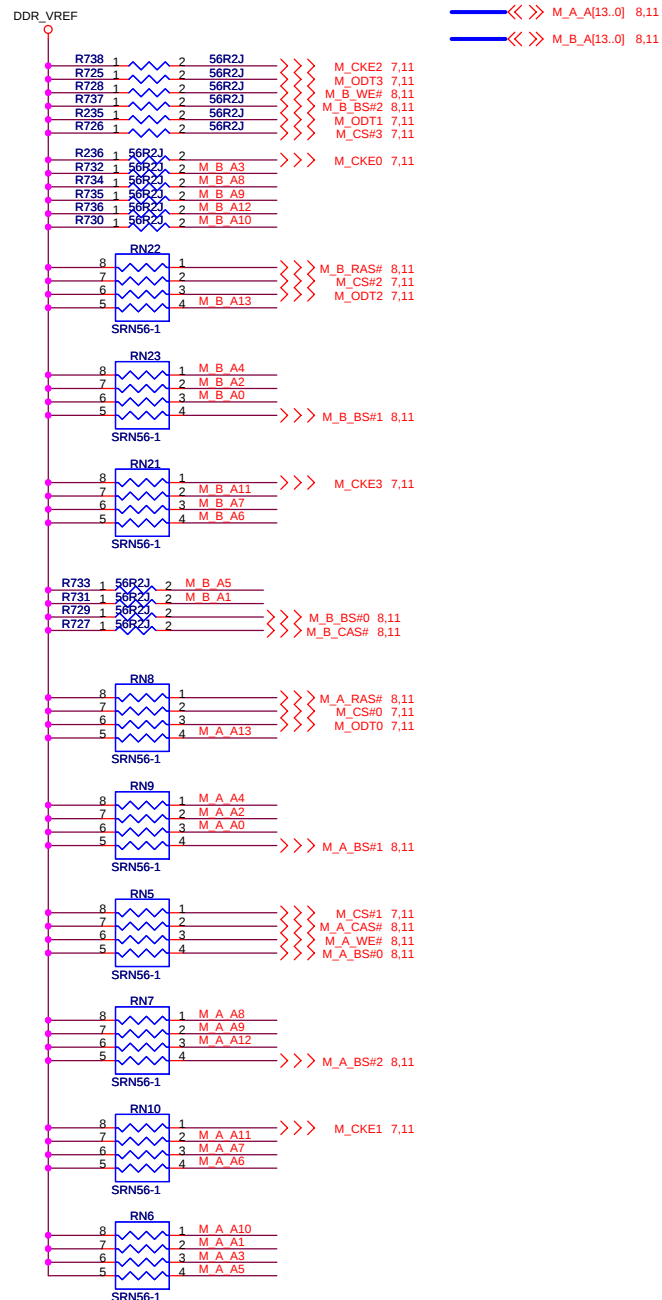






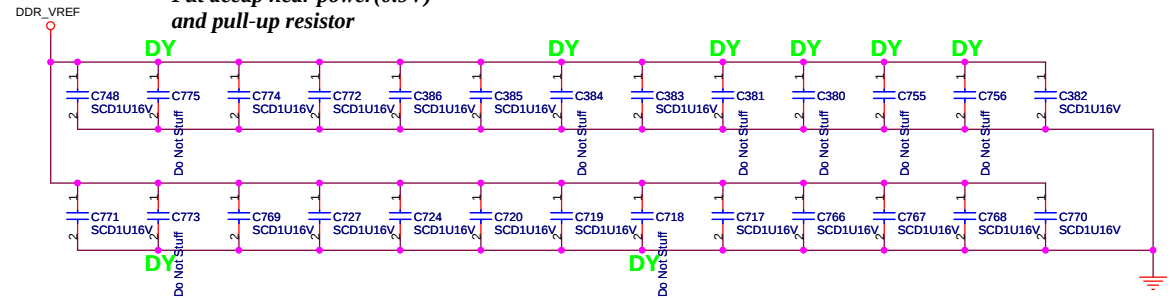
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

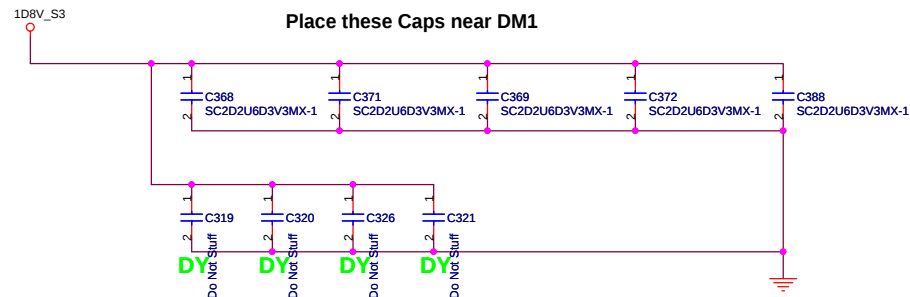


Decoupling Capacitor

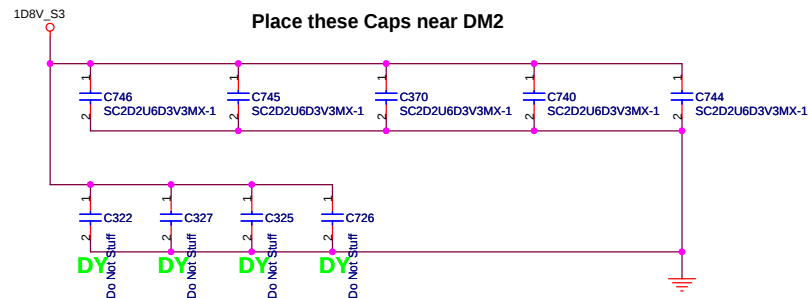
**Put decap near power(0.9V)
and pull-up resistor**



Place these Caps near DM1



Place these Caps near DM2



BOM2(NV44+G)

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Title

DDR2 Termination Resistor

Size

Document Number

CANARY2

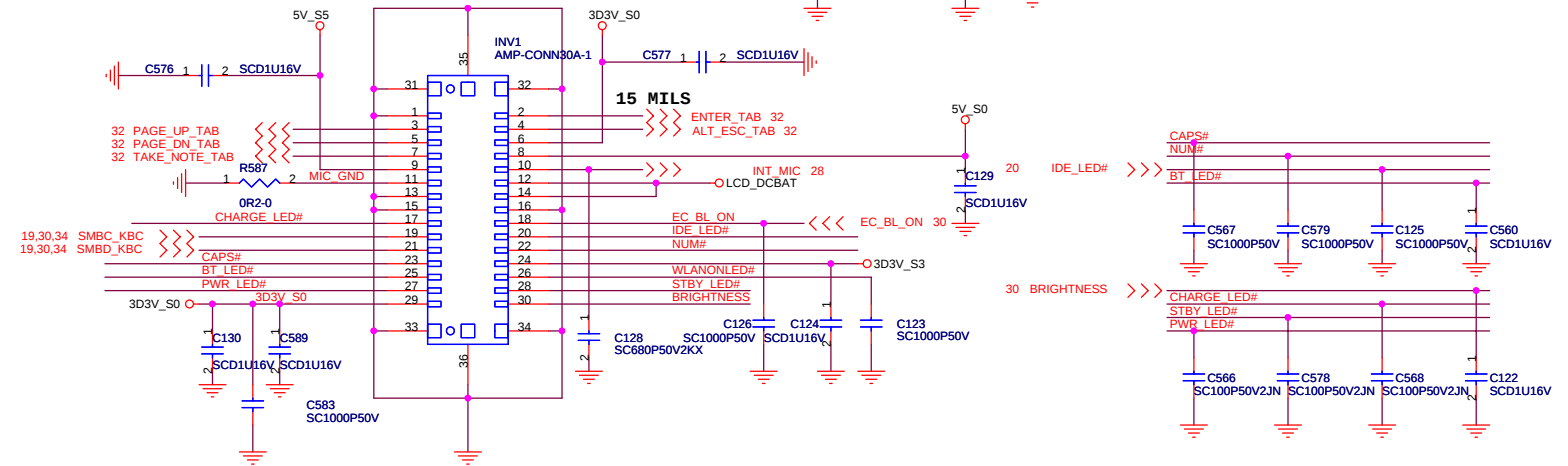
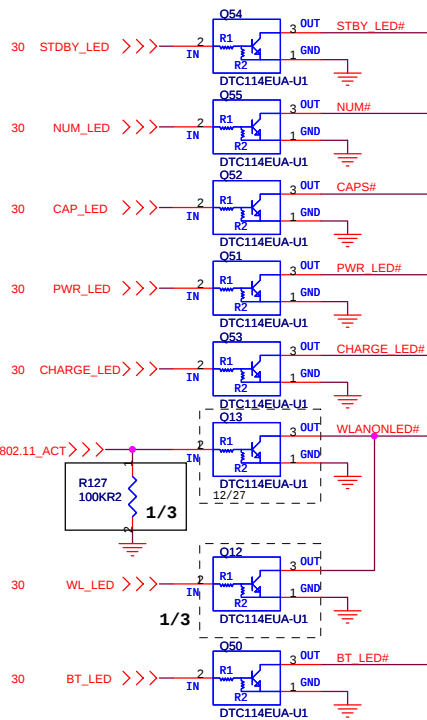
Rev

Date: Thursday, January 13, 2005

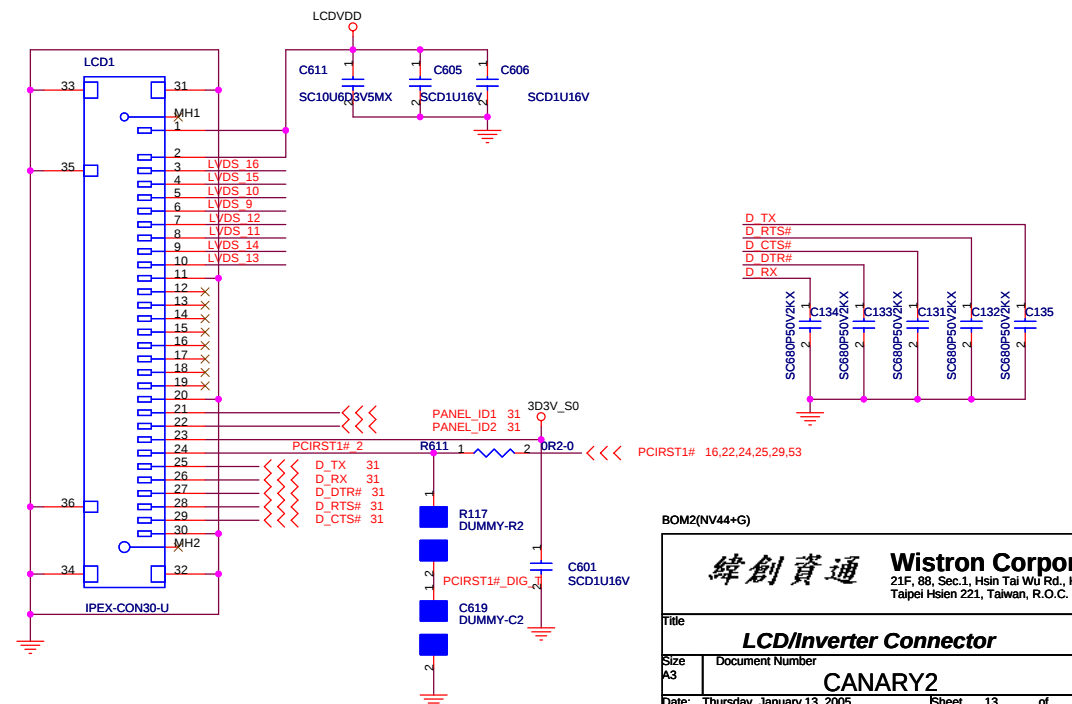
Sheet 12

55

INVERTER INTERFACE



LCD CONN

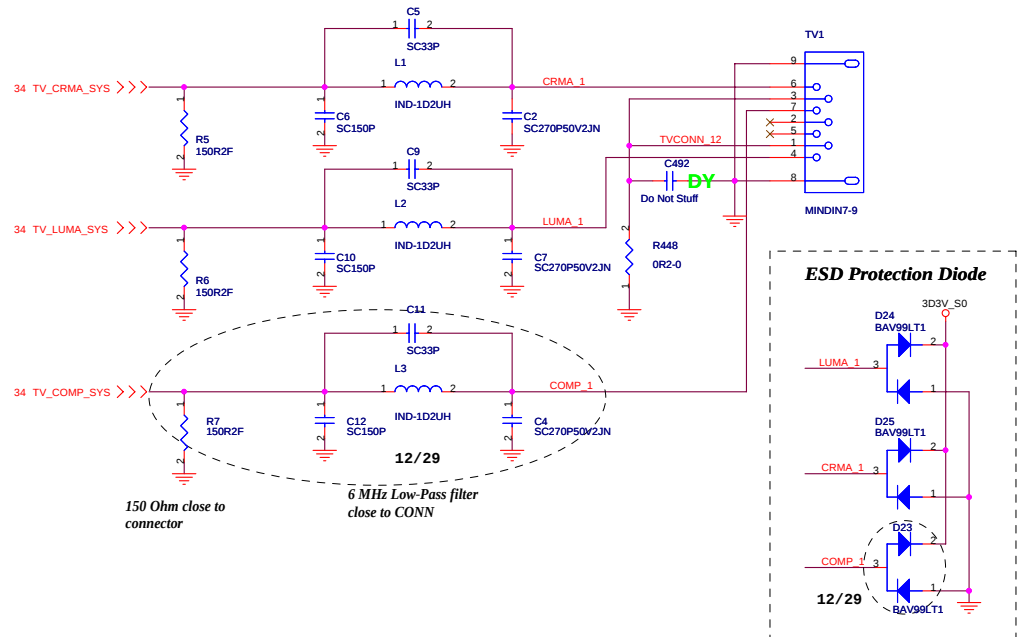
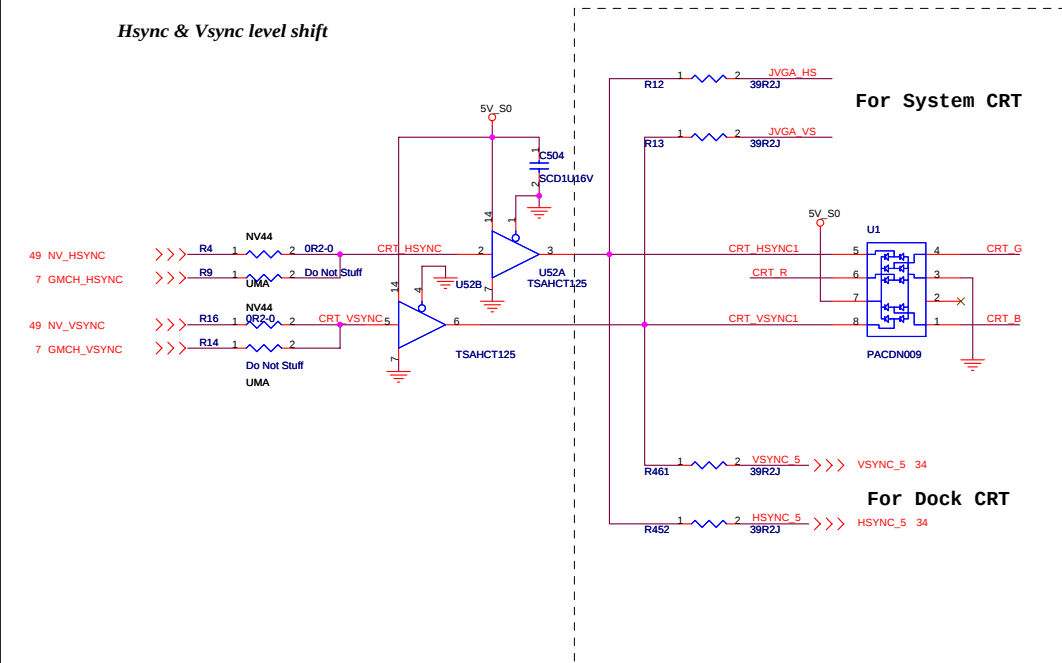
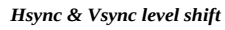
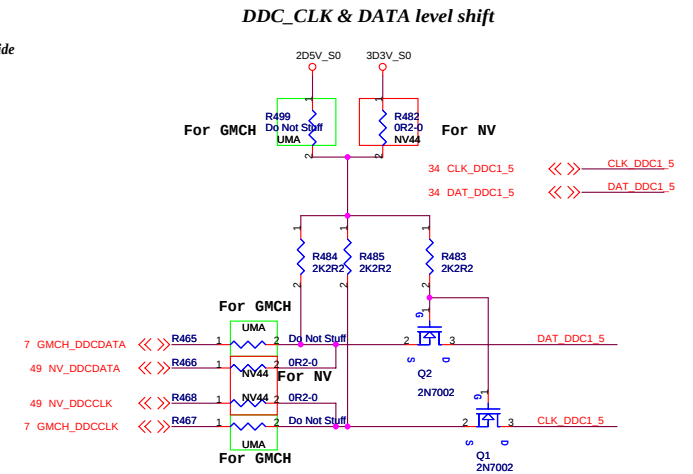
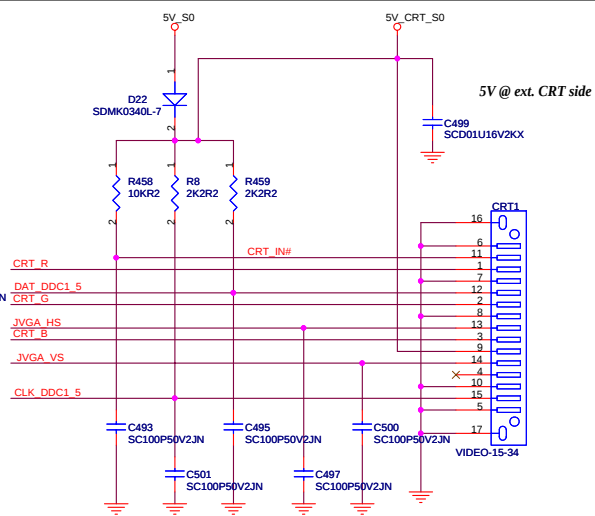
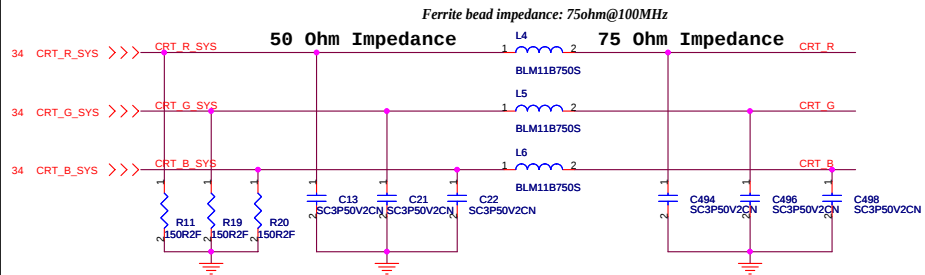


BOM2(NV44+G)

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Title		
LCD/Inverter Connector		
Size	Document Number	Rev
A3	CANARY2	SA
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CRT I/F &TV CONNECTOR



BOM2(NV44+G)

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Connector

Size	Document Number
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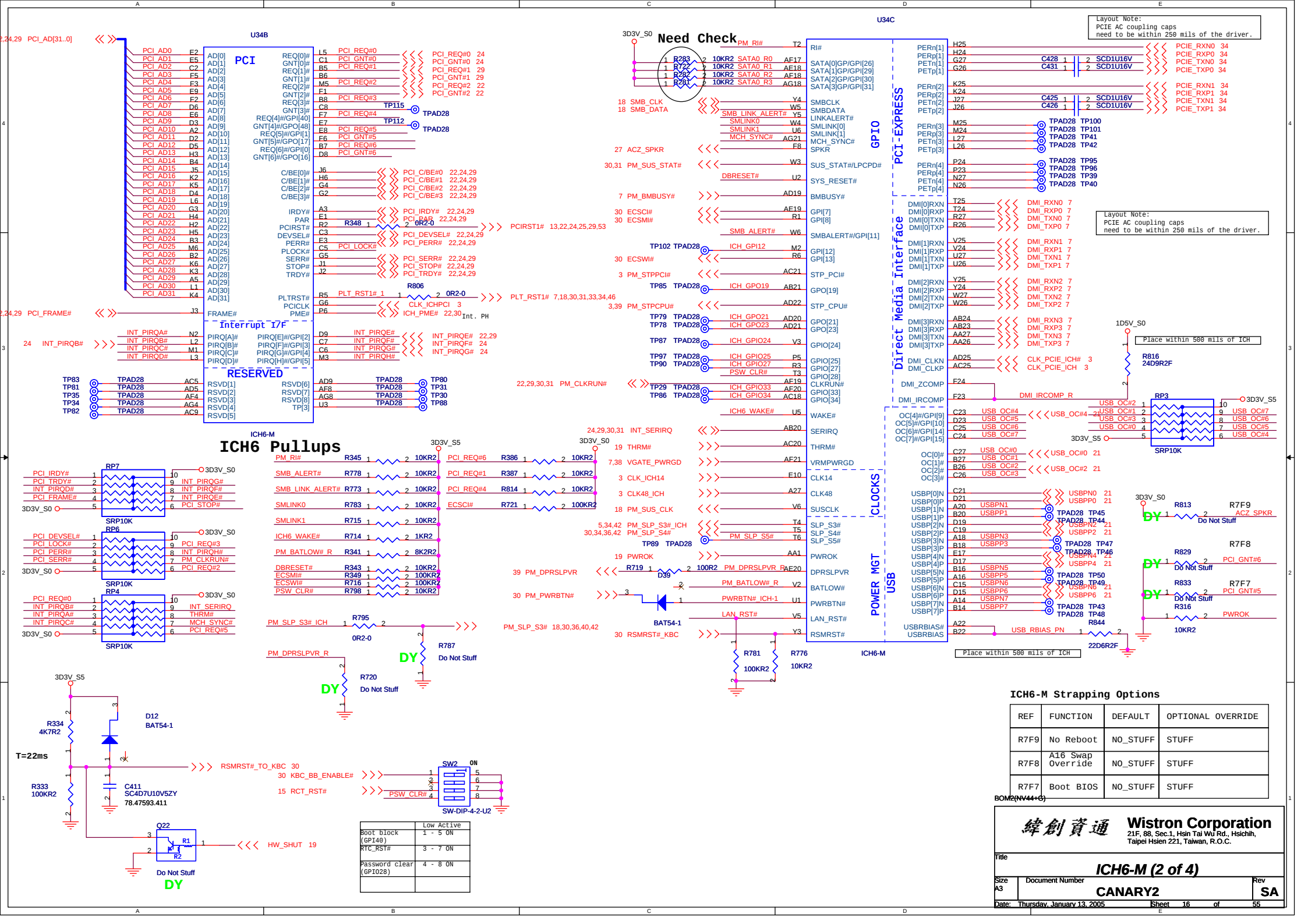
CANARY2

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SA

Date: Thursday, January 13, 2005

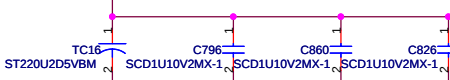
Sheet 14 of 55



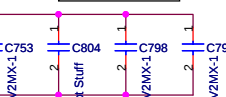
Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27

1D5V_S0

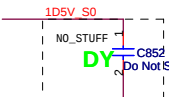
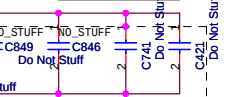
Layout Note:
Place near pin AA19



Layout Note:
IDE decoupling



Layout Note:
PCI decoupling



Place within 100
mils of ICH
near pin AG5

Place within 100
mils of ICH
near pin AG9

Place within 100
mils of ICH

Place within 100
mils of ICH
near E26, E27

Place within 100
mils of ICH
pin AE1

Place within 100
mils of ICH
pin AG10

Place within 100
mils of ICH
pin A13

Place within 100
mils of ICH
pin V7

Place within 100
mils of ICH pin
AG13, AG16

Layout Note:
Distribute in PCI section
near pin A2-A6 near D1-H1

Place both
within 100 mils
of ICH near D27

Layout Note:
Place near AB18

Layout Note:
Place near ICH6

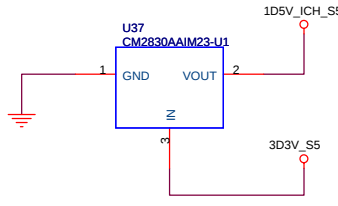
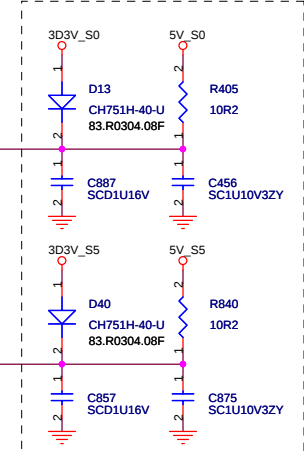
Place within 100
mils of ICH
pin G10

Place within 100
mils of ICH

Layout Note:
Place near AB3

Place within 100
mils of ICH
pin A17

*Within a given well, 5VREF needs to be up before the
corresponding 3.3V rail

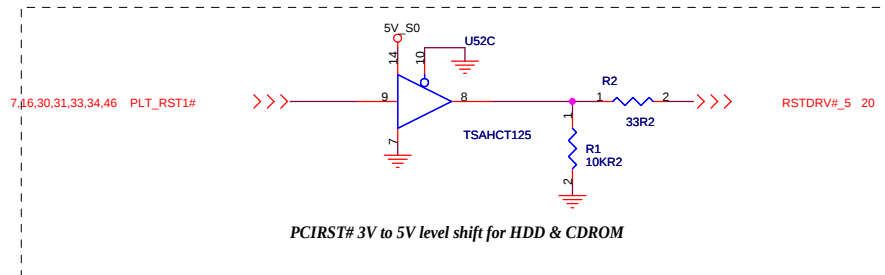
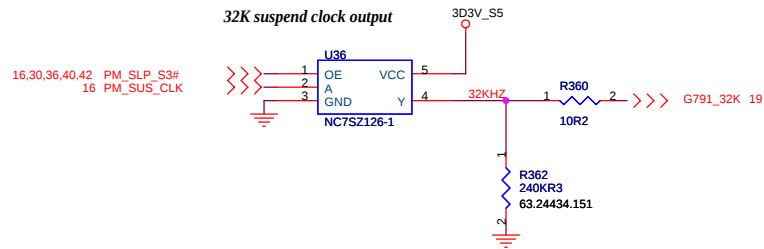


BOM2(NV44+G)

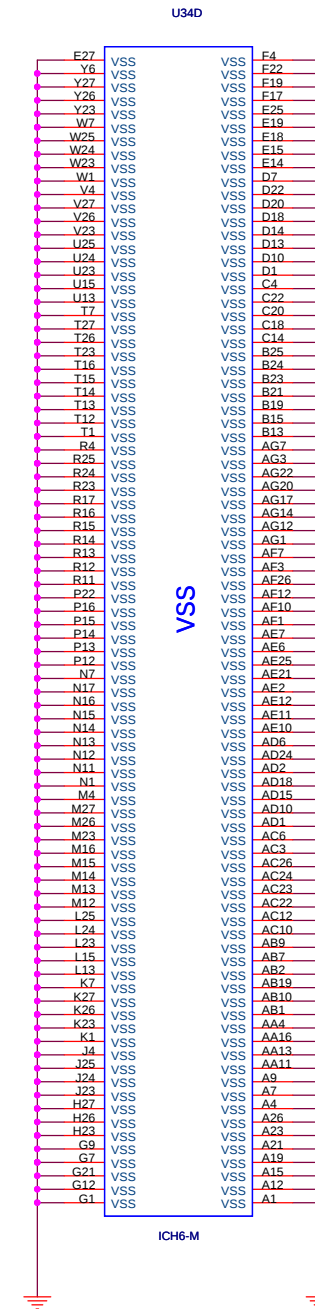
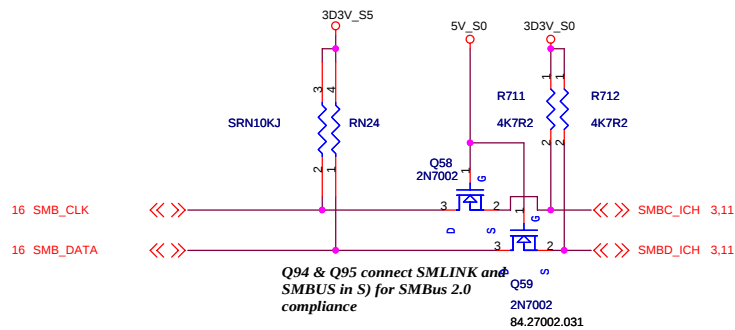
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title ICH6-M (3 of 4)

Size A3	Document Number CANARY2	Rev SA
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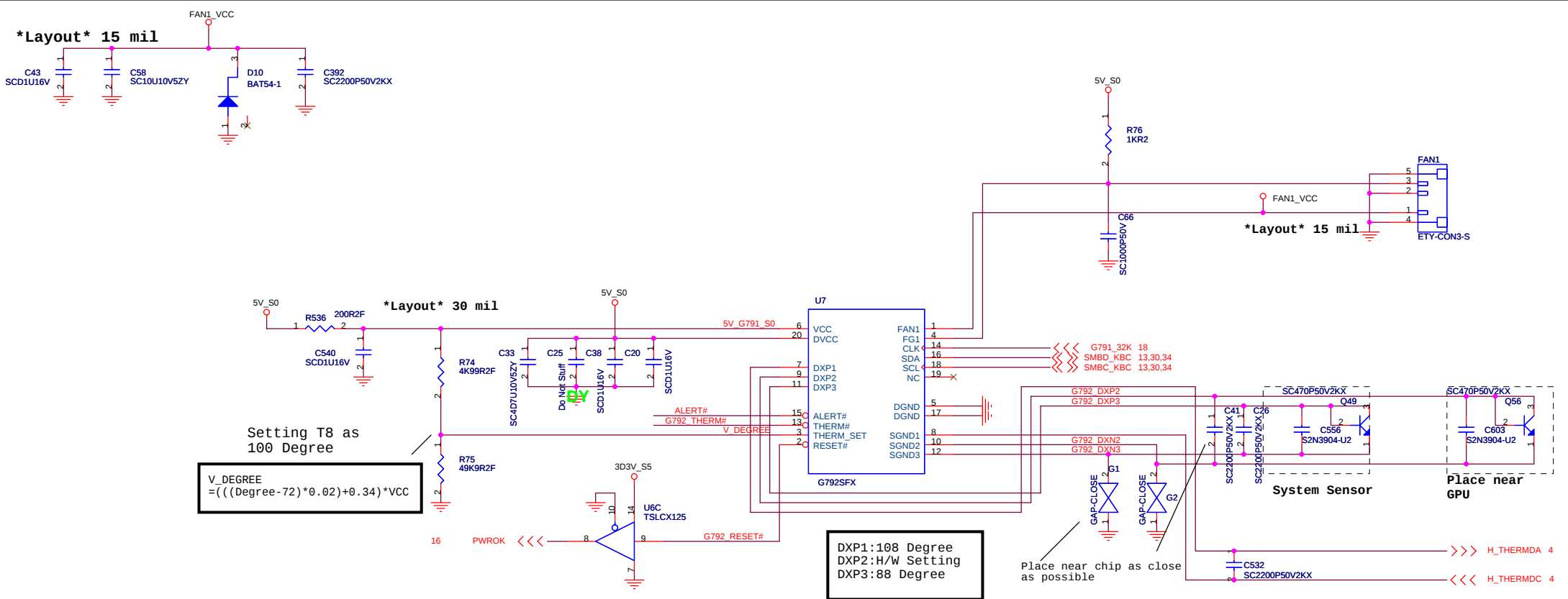
SMBUS



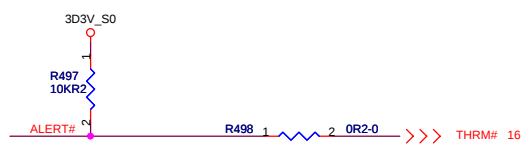
BOM2(NV44+G)

Title		
ICH6-M (4 of 4)		
Size A3	Document Number CANARY2	Rev SA
Date: Thursday, January 13, 2005 Sheet 18 of 55		

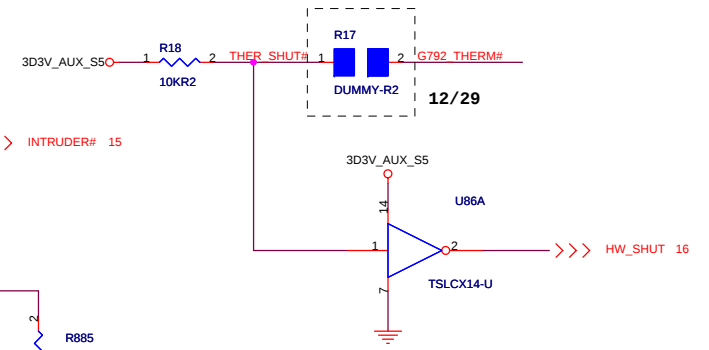
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.



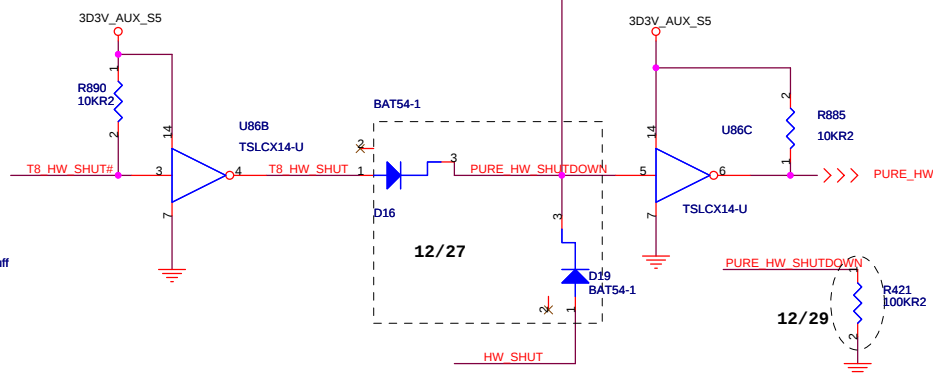
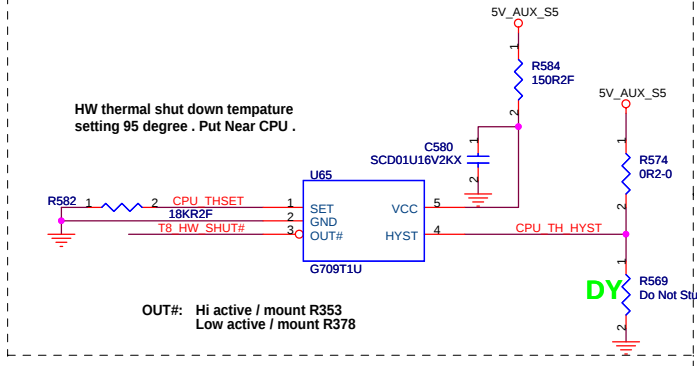
HW thermal shut down temperature setting 95 degree . Put Near CPU .



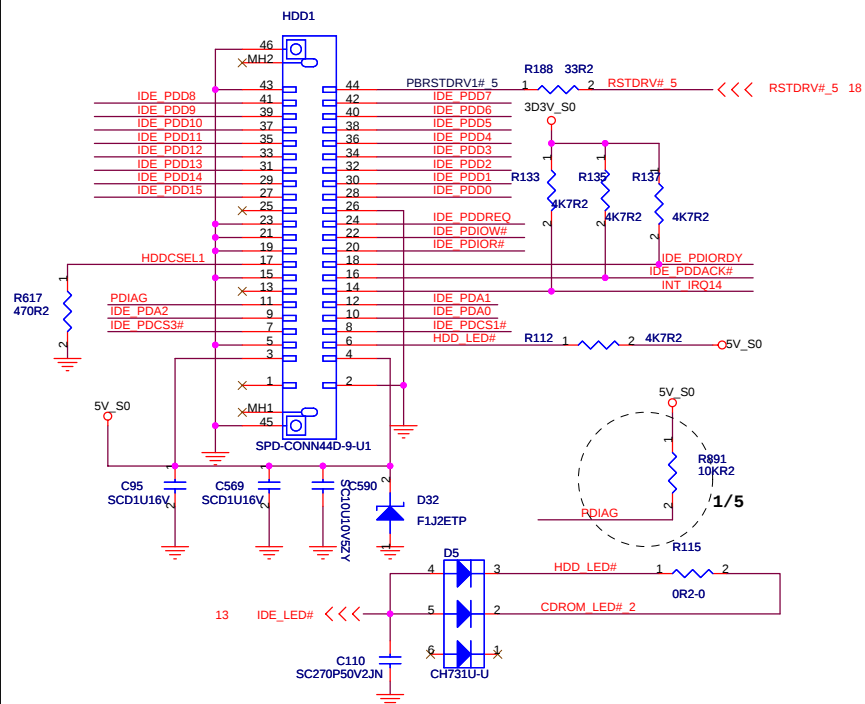
HW Thermal Throttling



Dummy when G791 enhanced T8 function

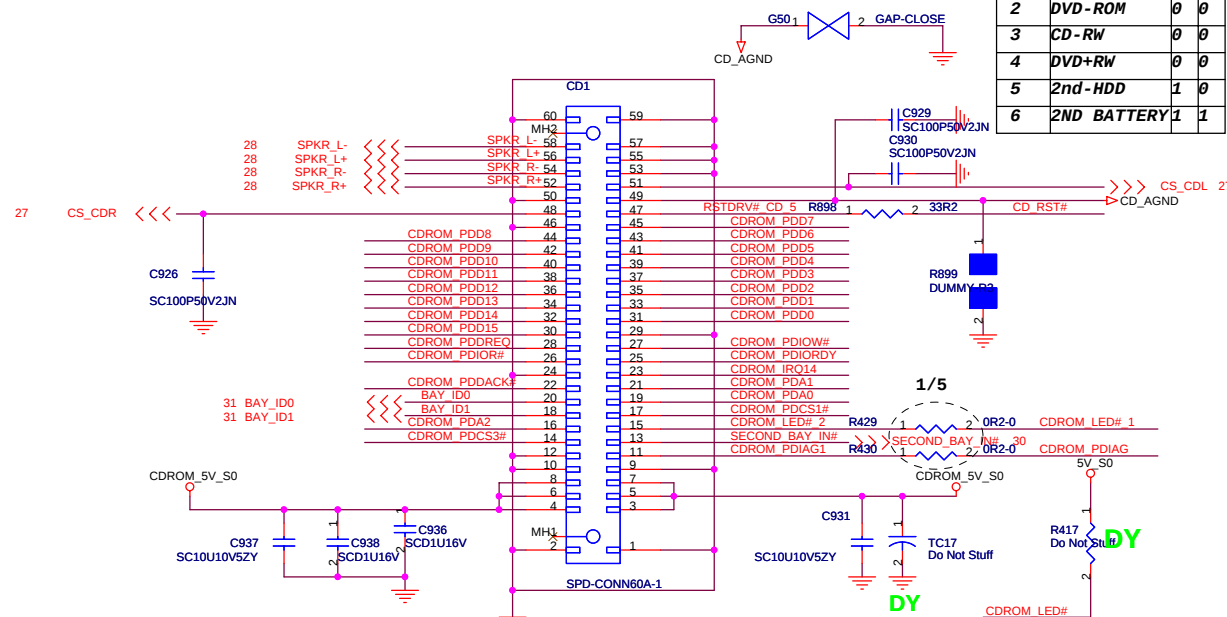


HDD Connector



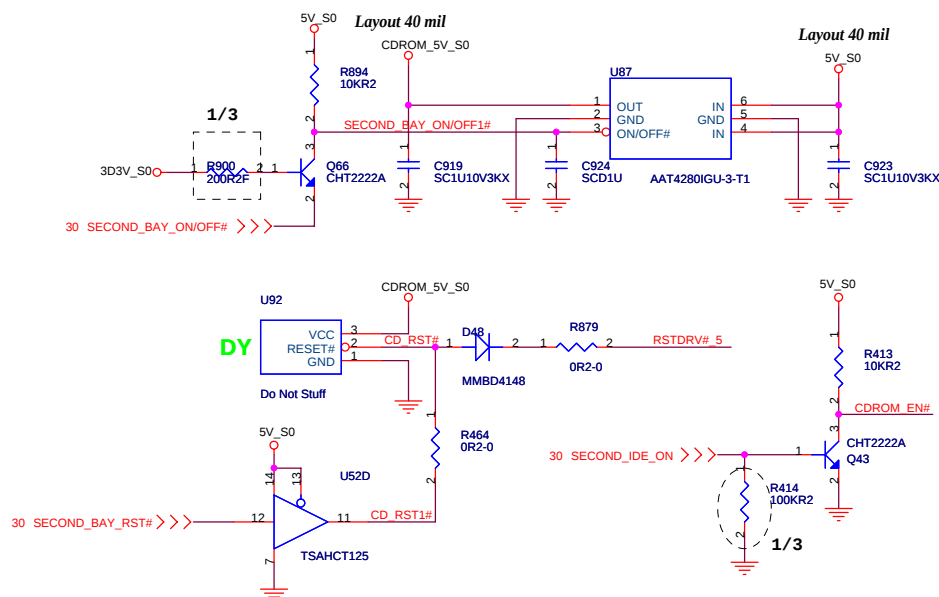
CD-ROM Connector

BAY Option Table			
Type	Device Description	BAY 0	BAY 1
1	CD-ROM	0	0
2	DVD-ROM	0	0
3	CD-RW	0	0
4	DVD+RW	0	0
5	2nd-HDD	1	0
6	2ND BATTERY	1	1

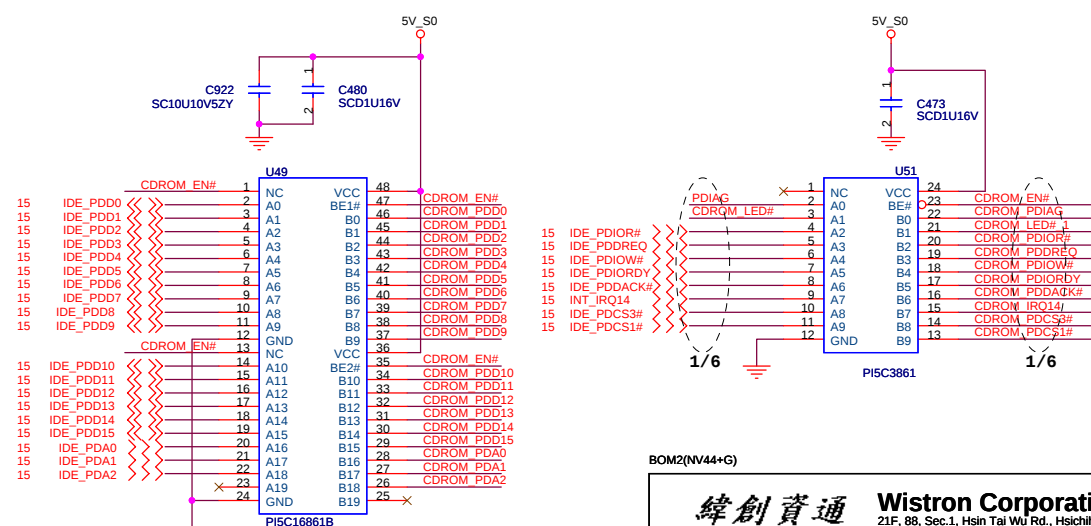


CHECK PIDE/SIDE DIAG# PIN

HOT SWAP CIRCUIT



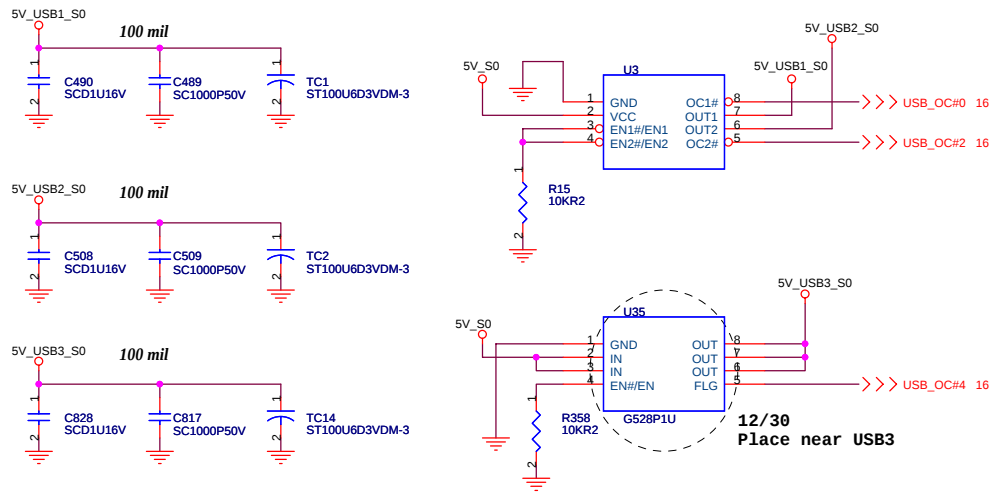
TRI-STATE SWITCH FOR CDROM HOT SWAP



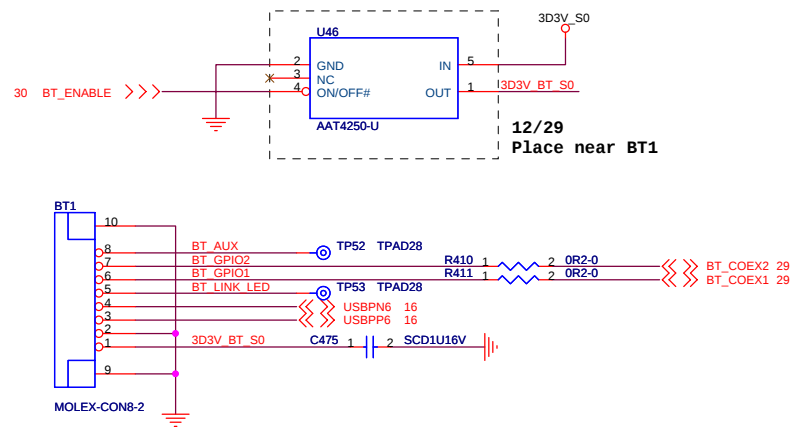
BOM2(NV44+G)

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

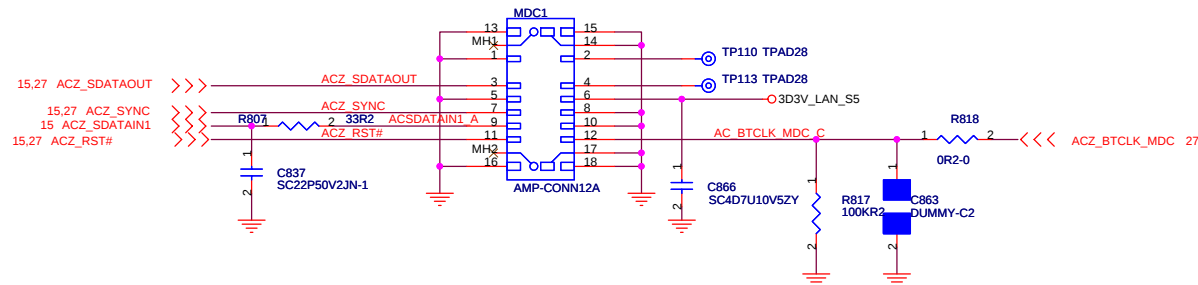
Title			
<i>HDD and CDROM</i>			
Size A3	Document Number		Rev
	CANARY2		S
Date:	Thursday, January 13, 2005	Sheet 20 of	55



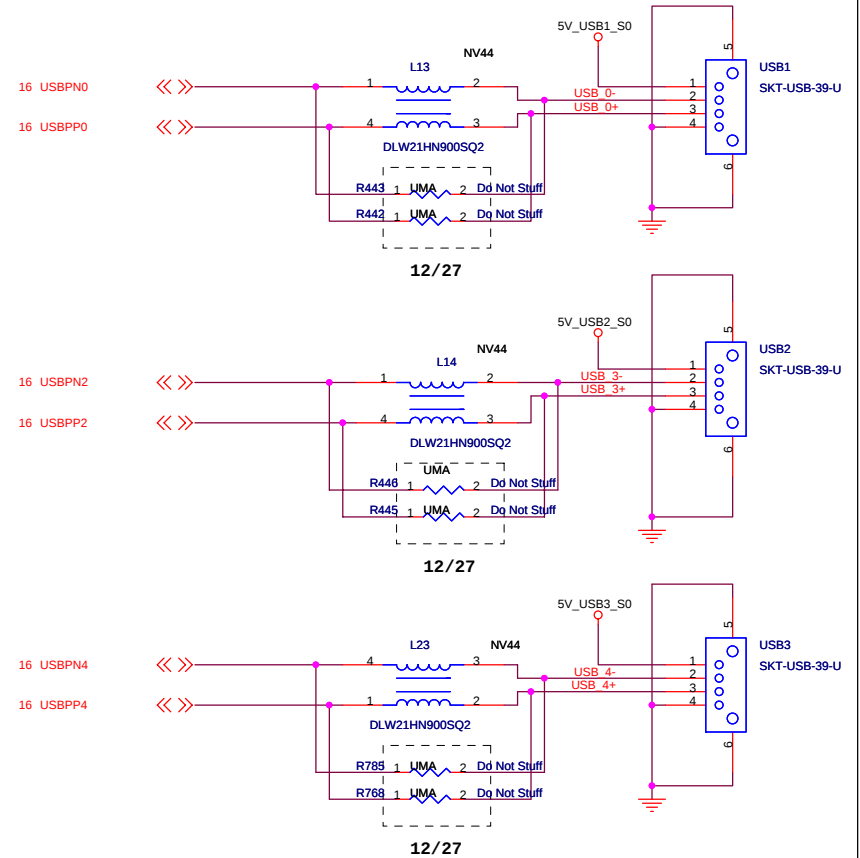
BLUETOOTH MODULE CONNECTOR



MDC 1.5 CONNECTOR



USB PORT



BOM2(NV44+G)

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB & MDC & BTOOTH

Size

A3

Document Number

CANARY2

Rev

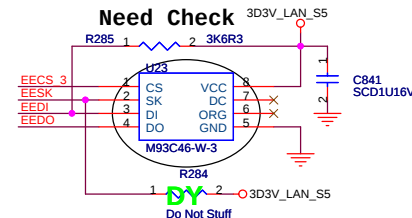
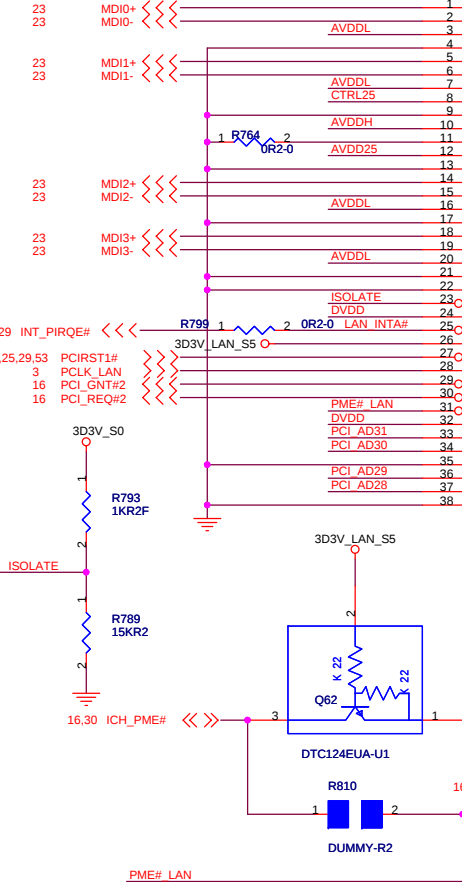
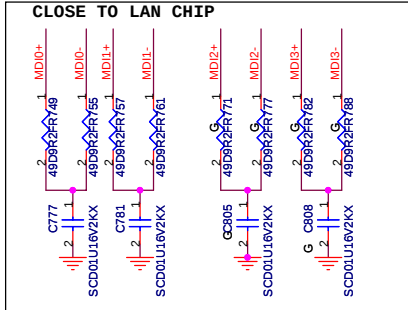
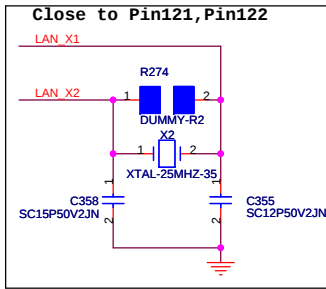
SA

Date: Thursday, January 13, 2005

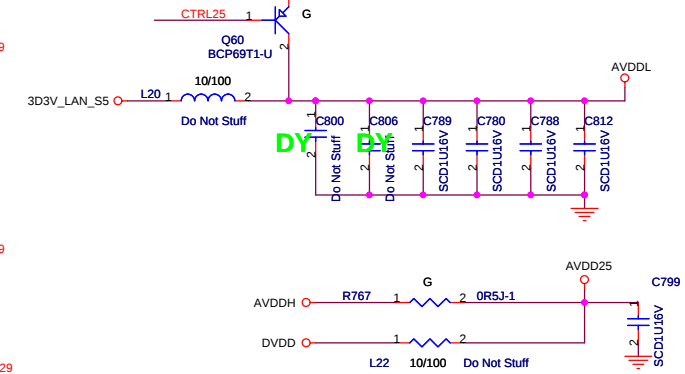
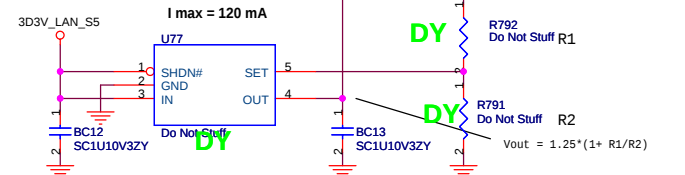
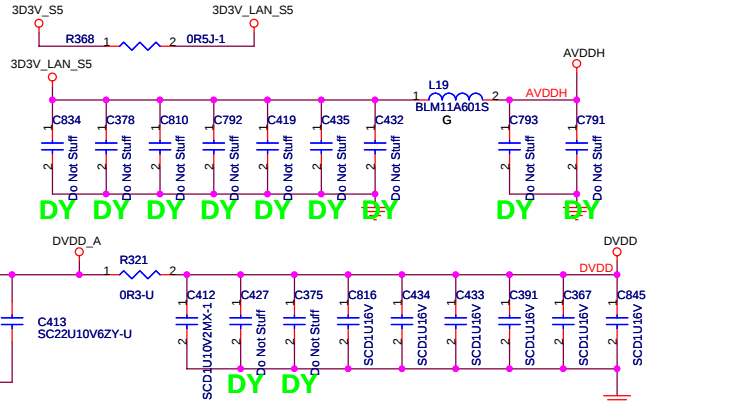
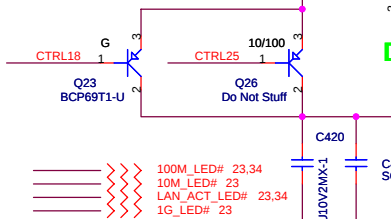
Sheet 21

of

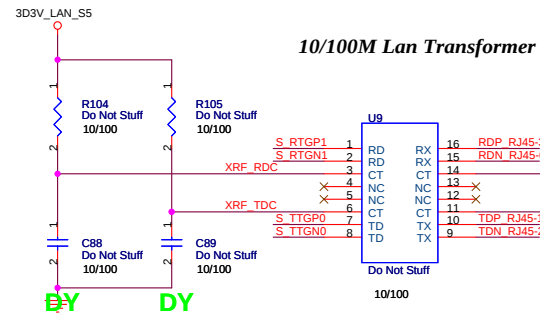
55



R824 is used only at RTL8110S(B) application and only at 93C56 is used.



PIN NAME	8110SBL (Giga)	8100CL (10/100)	SIGNAL NAME
VDD33	3.3	3.3	3D3V_LAN_S5
AVDDH	3.3	N.C.	AVDDH
VDD18	1.2	2.5	DVDD
AVDDL	2.5	3.3	AVDDL
V_12P	3.3	2.5	V_12P

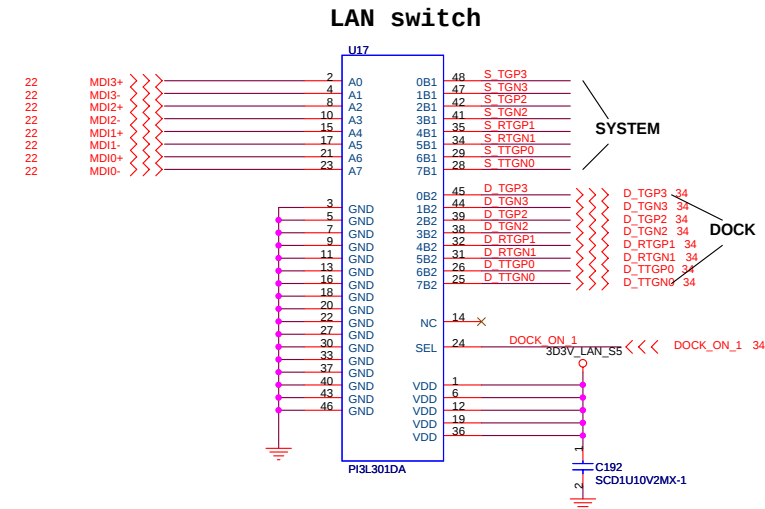
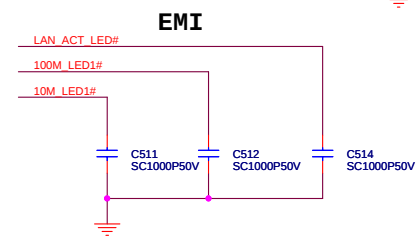
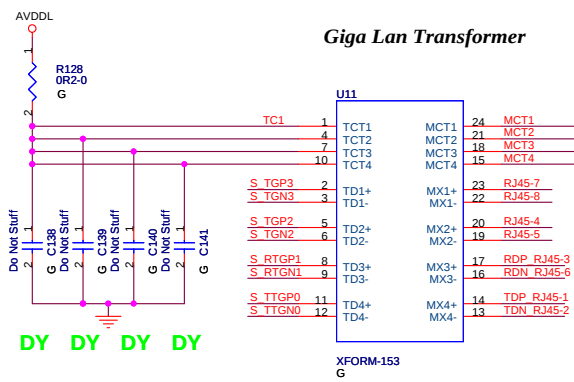


- 1. route on bottom as differential pairs.
- 2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3. No vias, No 90 degree bends.
- 4. pairs must be equal lengths.
- 5. 6mil trace width, 12mil separation.
- 6. 36mil between pairs and any other trace.
- 7. Must not cross ground moat, except RJ-45 moat.

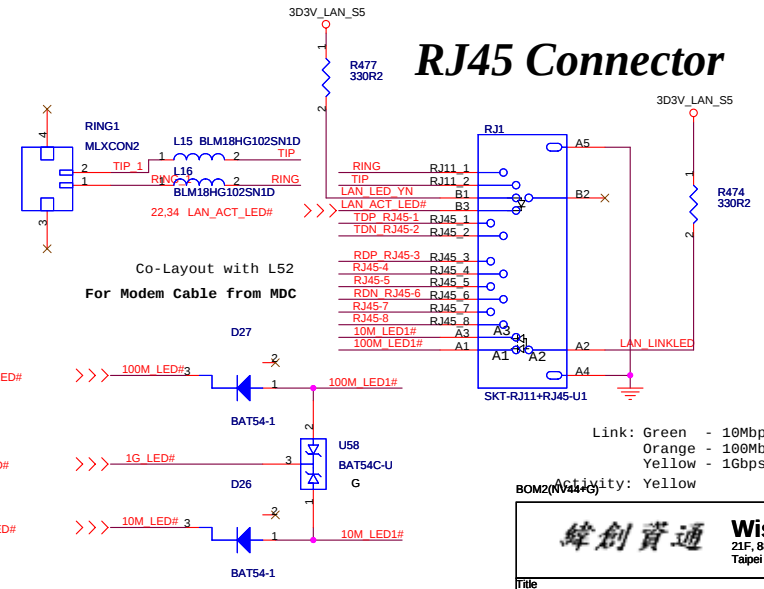
Green LED: Speed 100: ON / Speed 10: OFF
Yellow LED: Link: ON, TX/RX:
Flash(10Hz)

RJ11 signal must leave the other signal
or power plane 100mil.

DOC_TIP, DOC_RING, TIP, RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



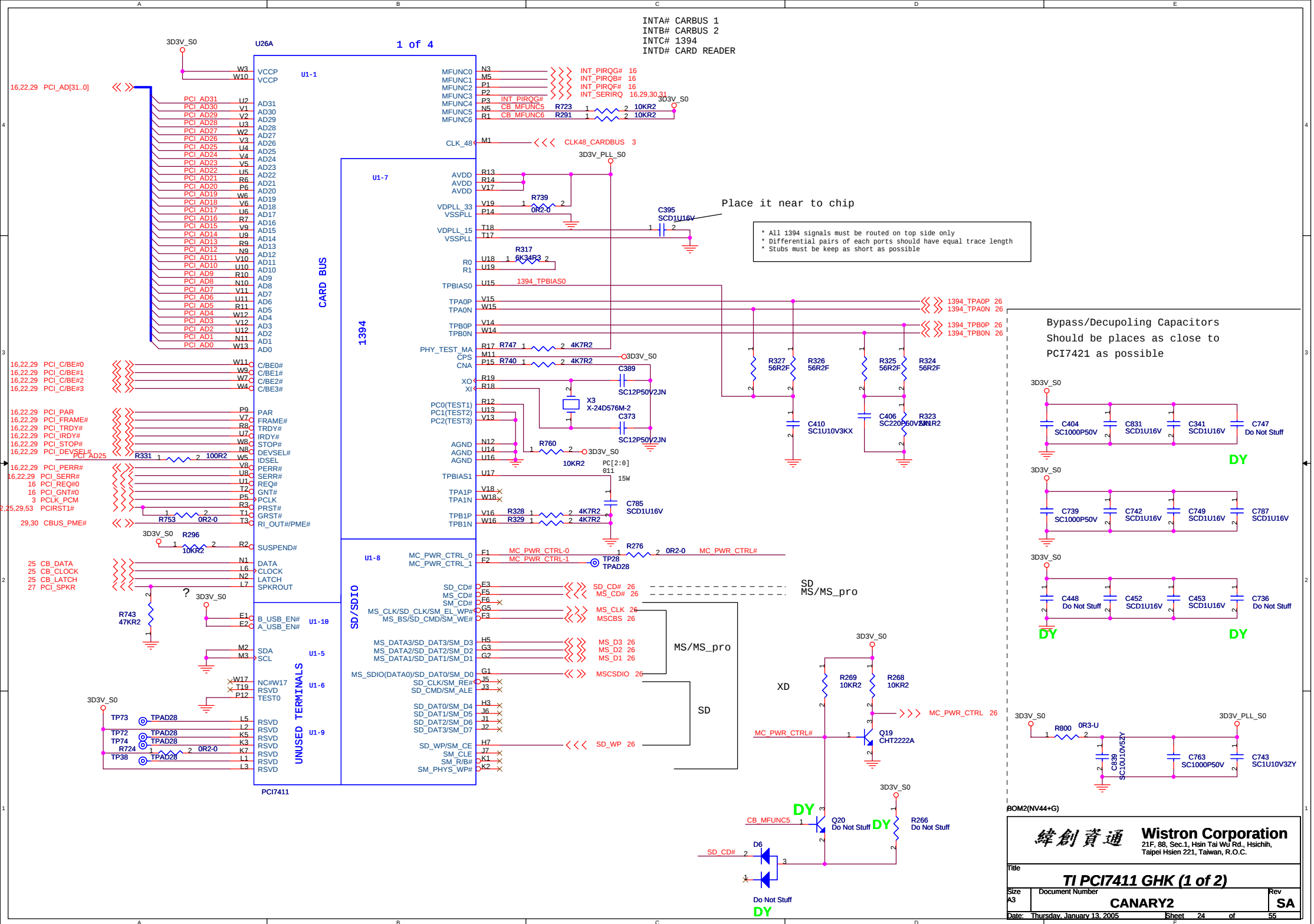
Function	SEL
An to nB1	L
An to nB2	H



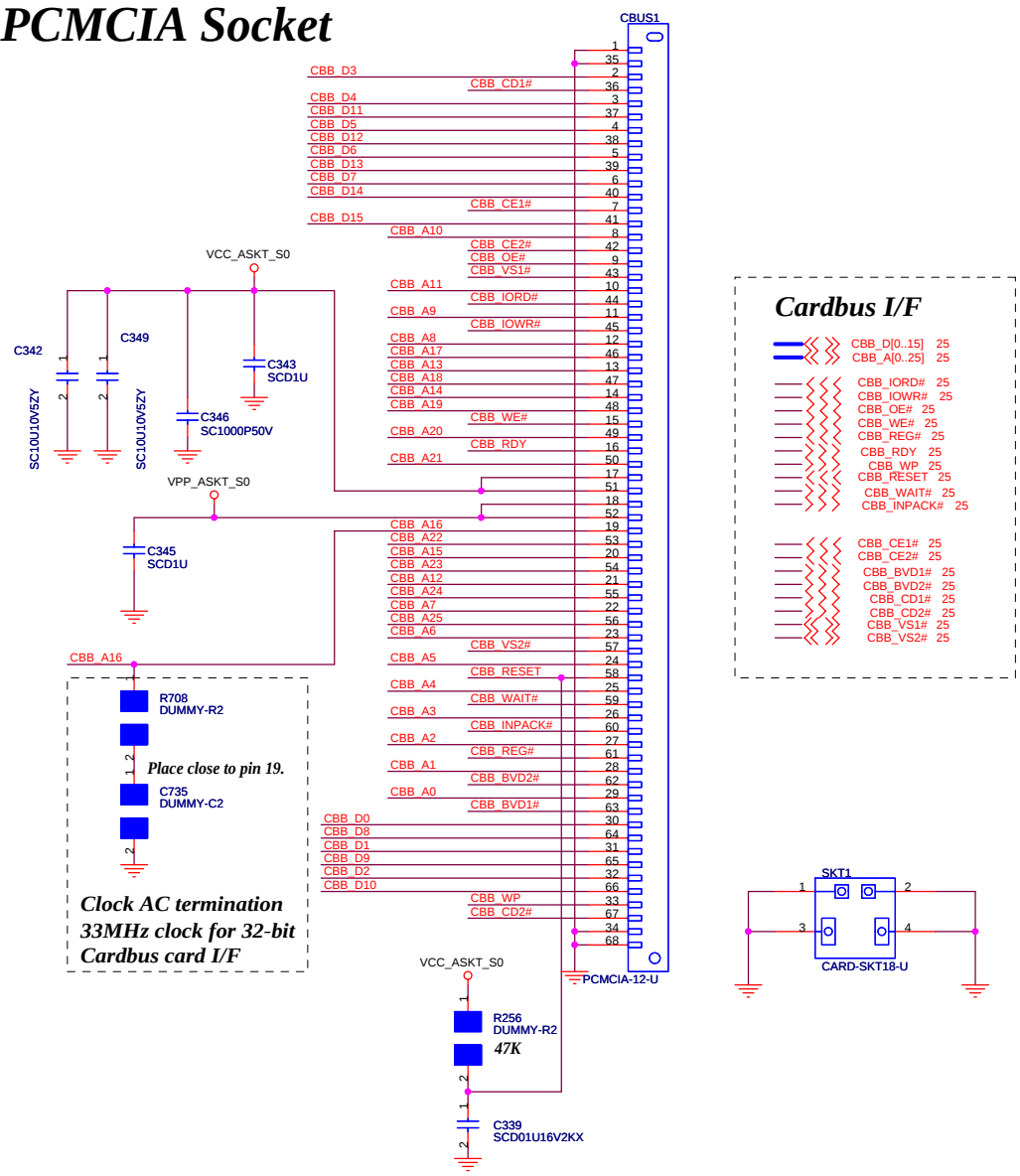
Link: Green - 10Mbps/802.11b
Orange - 100Mbps/802.11a
Yellow - 1Gbps

BOM2(NV44)G

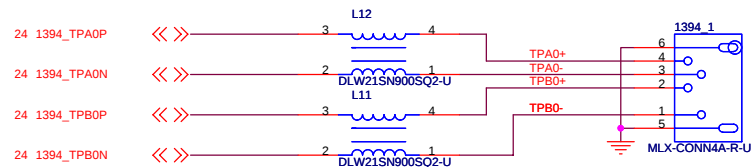
Title		
LAN Connector		
Size	Document Number	Rev
Custom	CANARY2	SA
Date: Thursday, January 13, 2005	Sheet 23 of 55	



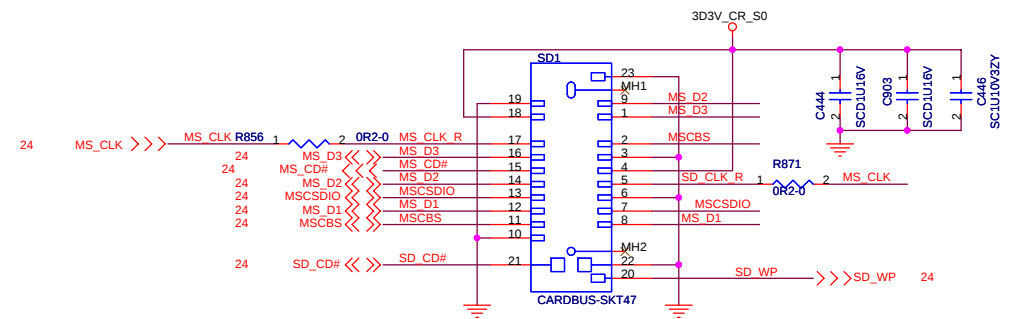
PCMCIA Socket



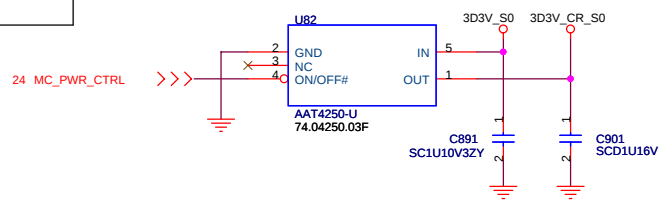
1394 Connector



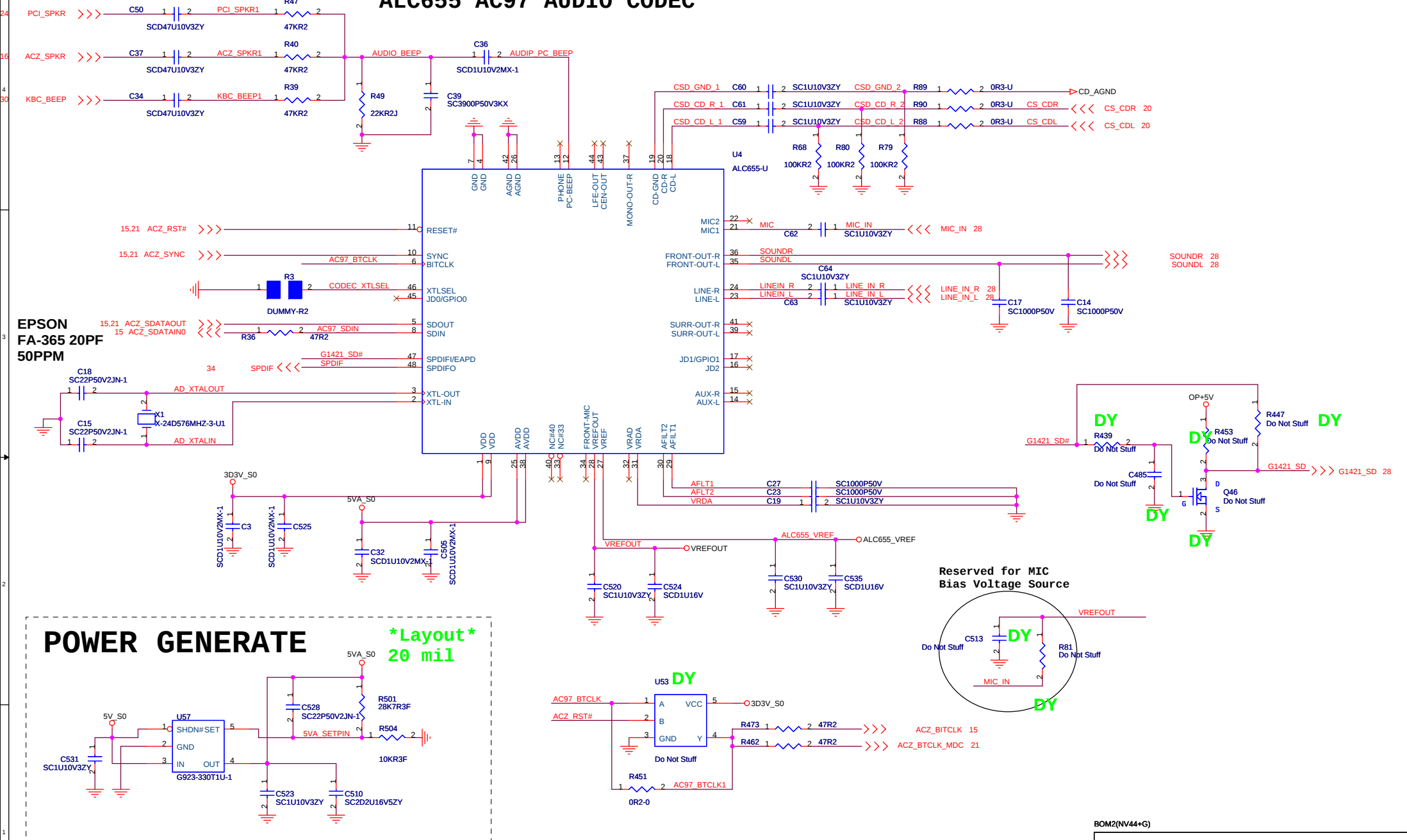
SD/MMC/MS CONN.



POWER SWITCH



ALC655 AC97 AUDIO CODEC



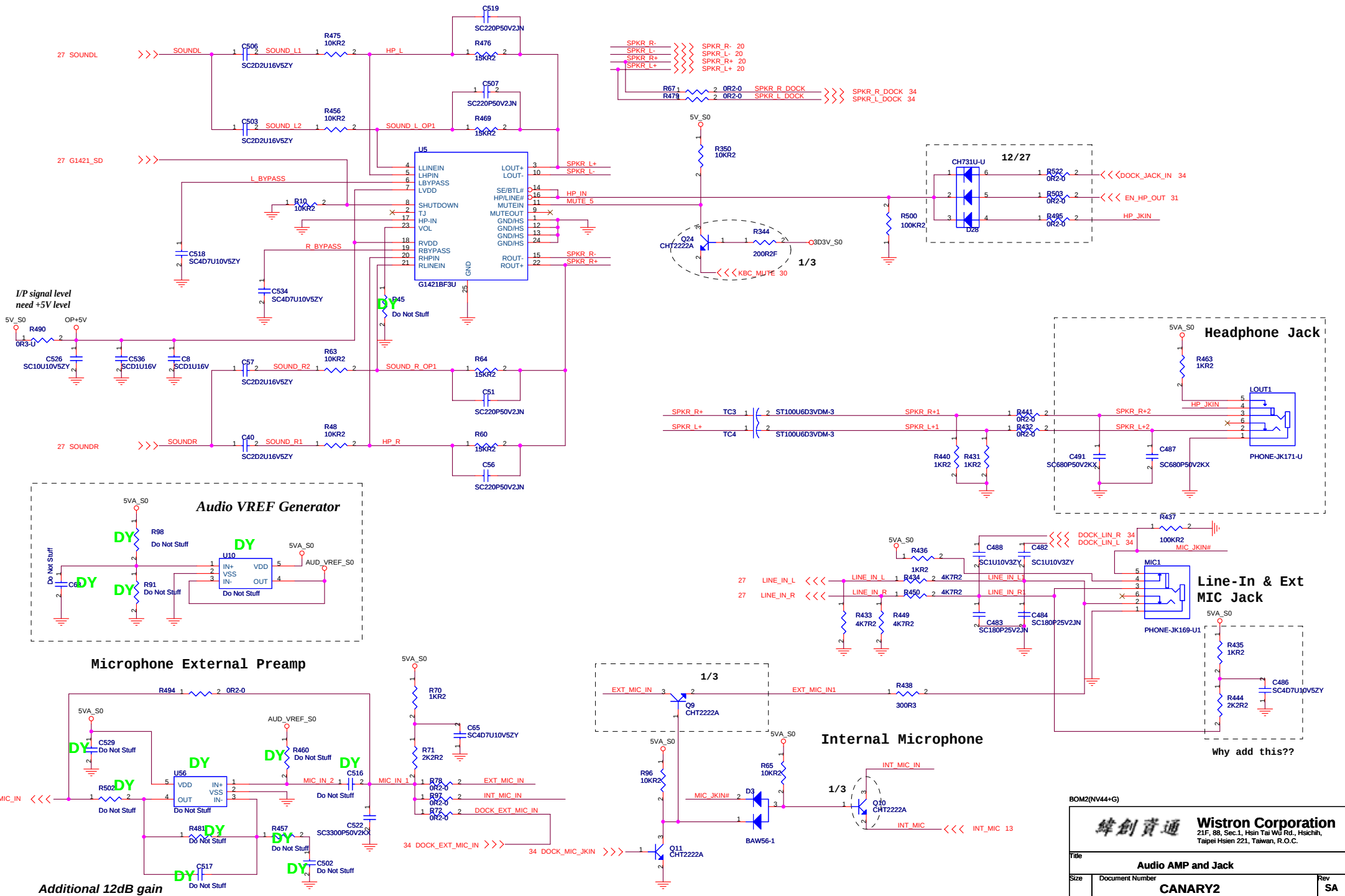
BOM2(NV44+G)

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
AC'97 CODEC - ALC655			
Size A3	Document Number		Rev
	CANARY2		SA
Date:	Thursday, January 13, 2005	Sheet 27 of	55

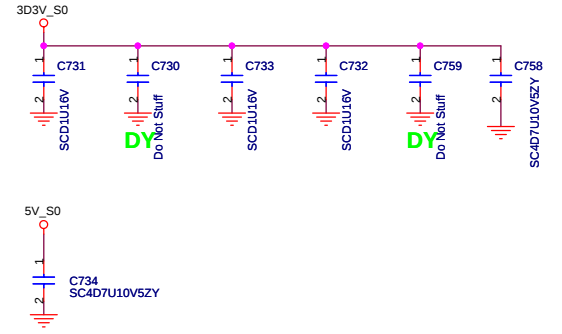
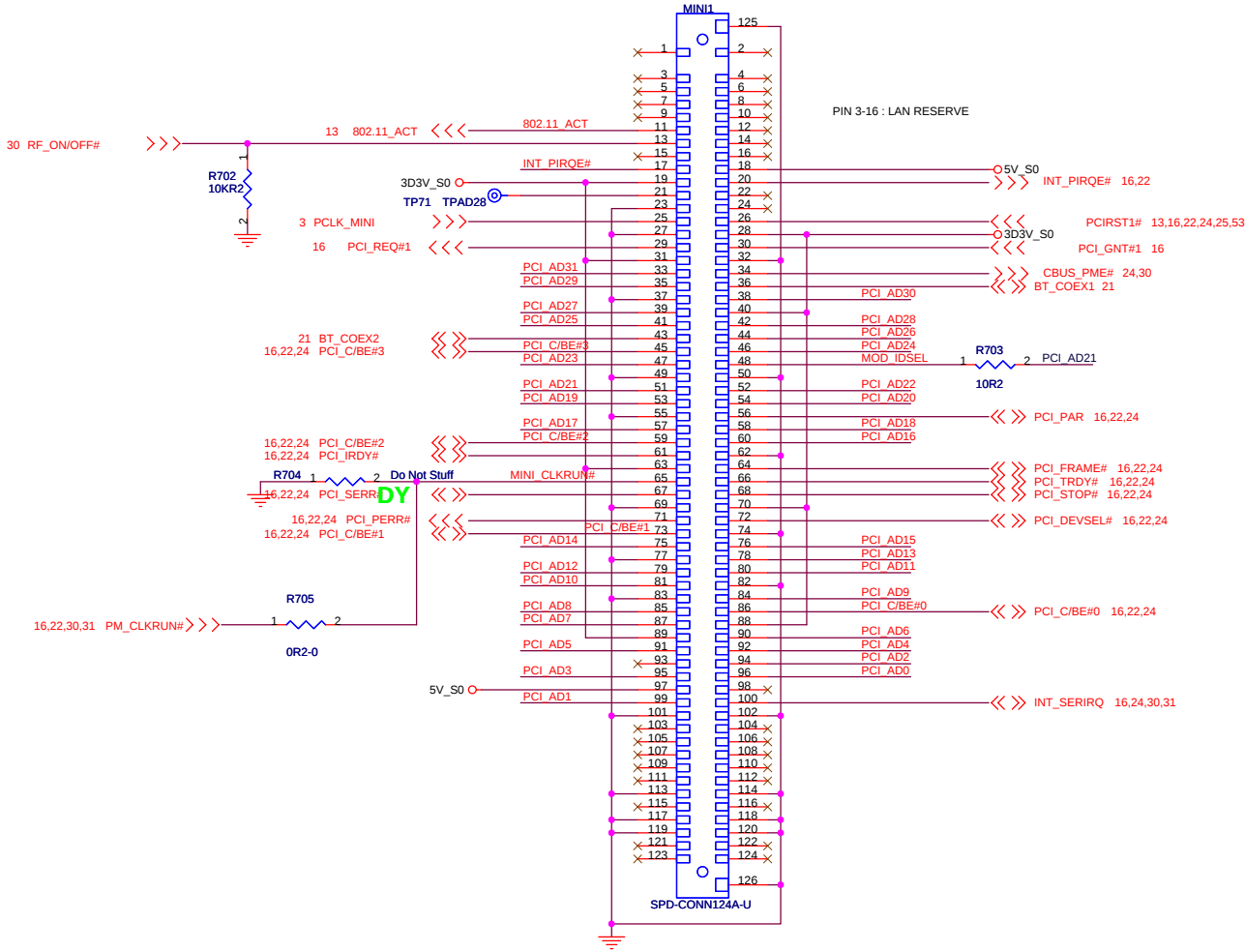
AUDIO OP AMPLIFIER

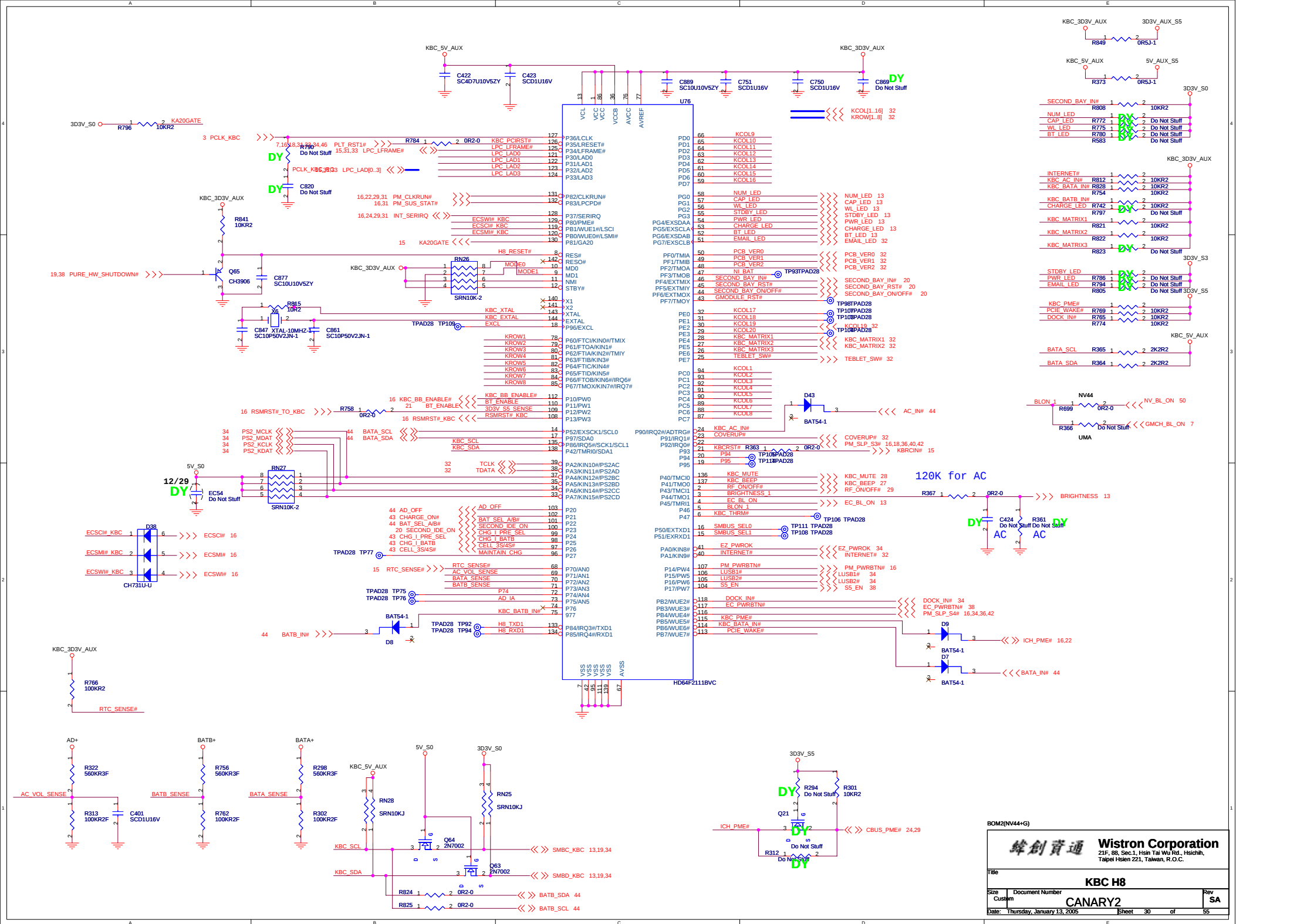


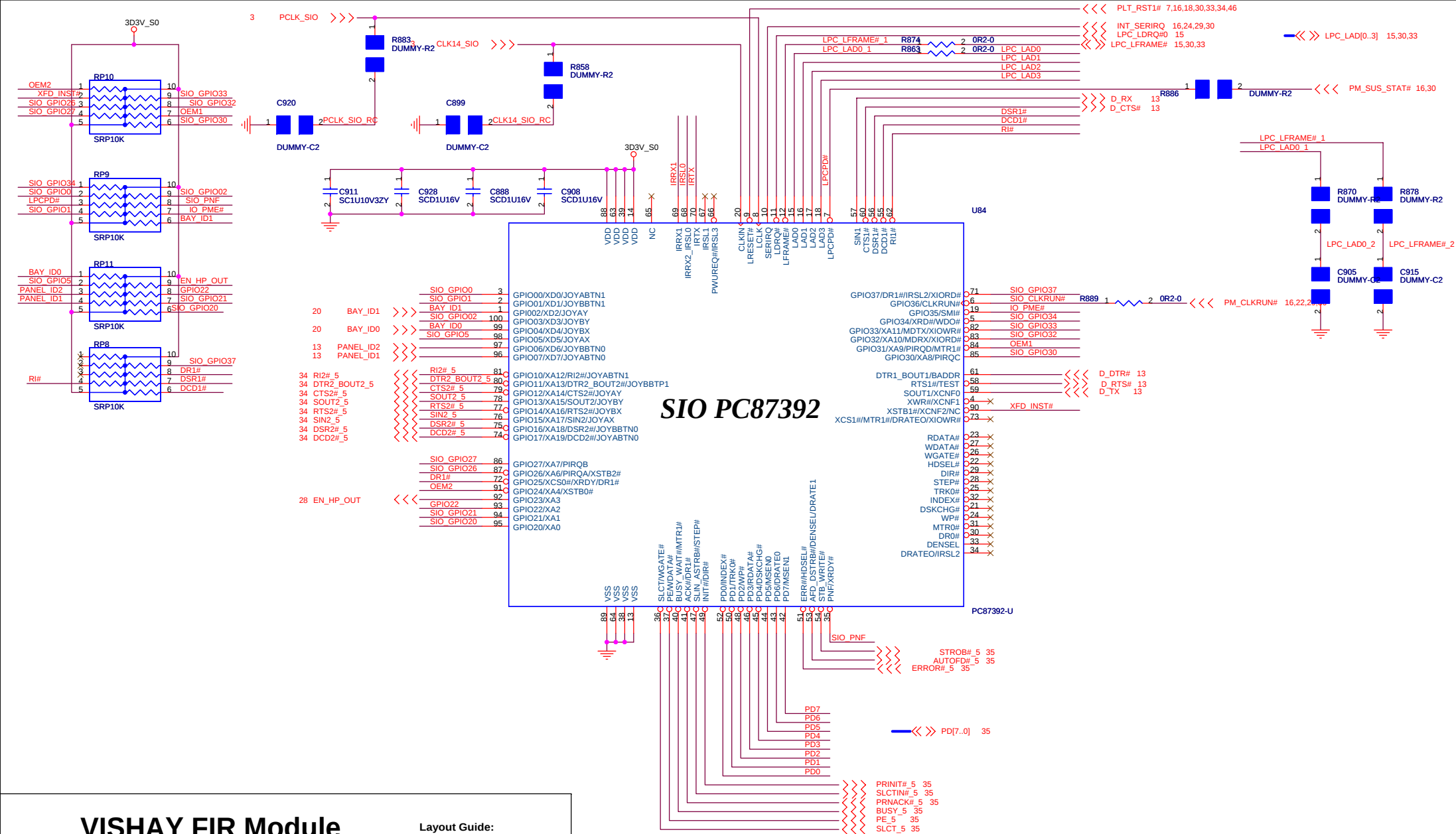
BOM2(NV44+G)

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Audio AMP and Jack			
Size	Document Number	Rev	
	CANARY2	SA	
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16,22,24 PCI_AD[31..0] <<<



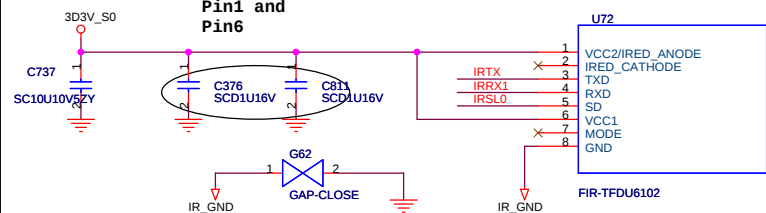




VISHAY FIR Module

Place C857
, C858 near
Pin1 and
Pin6

Layout Guide:
(1) FIR_5V : 30 mils,
(2) BCY1, BC50
close to U3



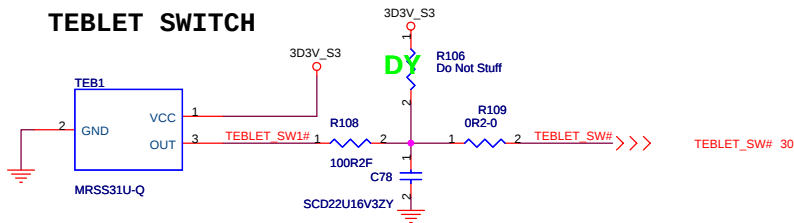
BOM2(NV44-G)

緯創資通

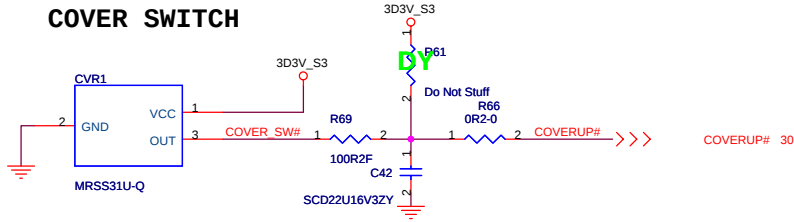
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
SIO		
Size	Document Number	Rev
A3	CANARY2	SA
Date: Thursday, January 13, 2005		
Sheet 31 of 55		

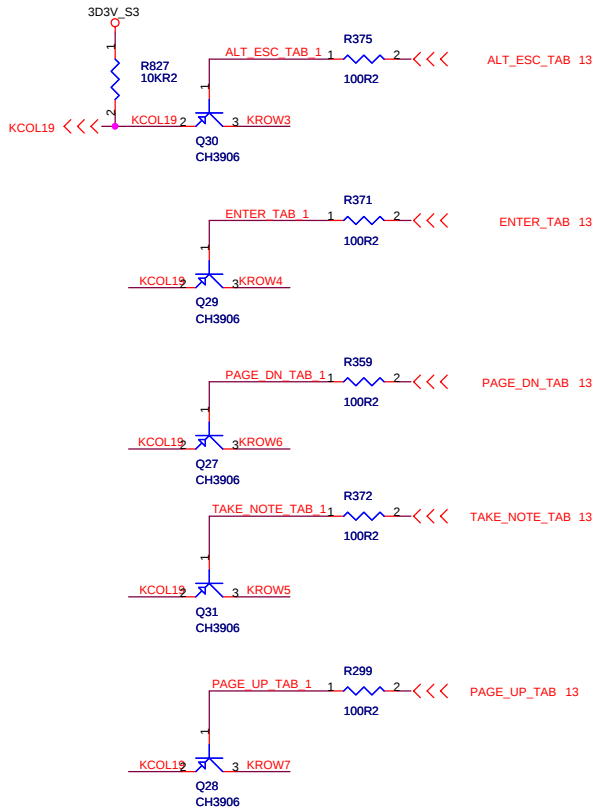
TEBLET SWITCH



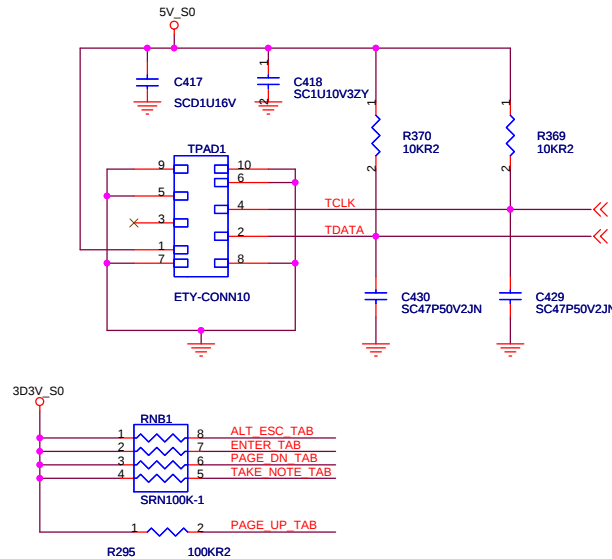
COVER SWITCH



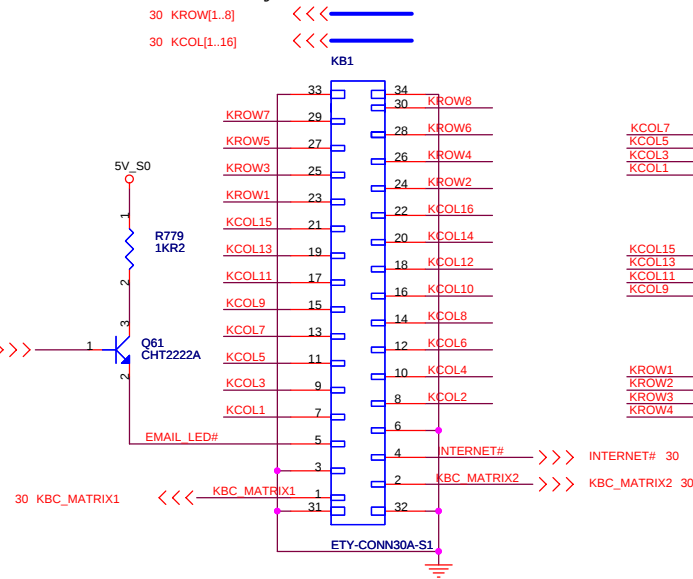
TABLET FUNCTION BUTTON



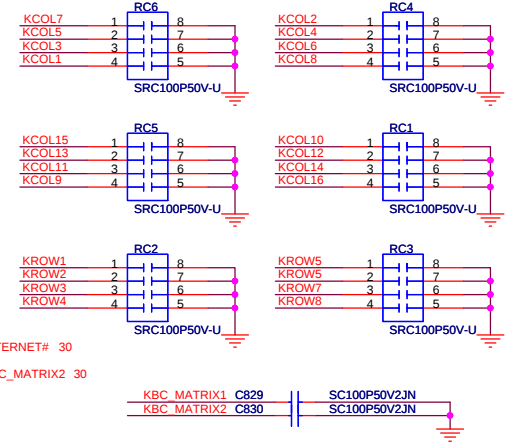
TouchPad Connector



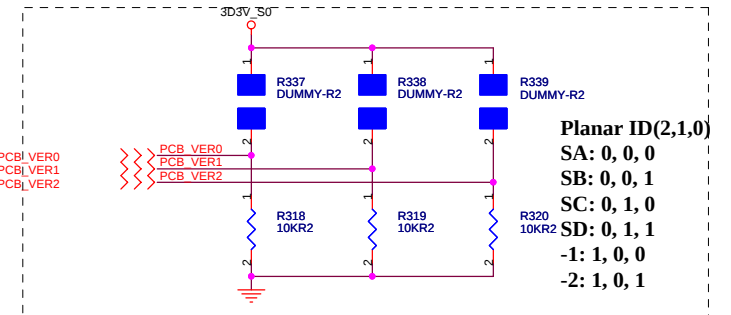
Internal Keyboard Connector



EMI CAPS



Board ID



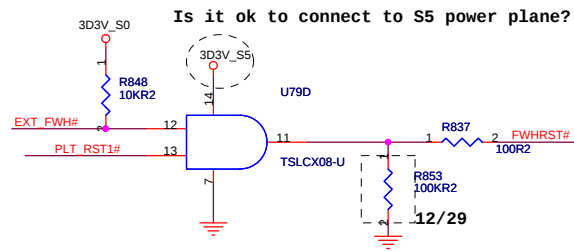
Planar ID(2,1,0)
SA: 0, 0, 0
SB: 0, 0, 1
SC: 0, 1, 0
SD: 0, 1, 1
-1: 1, 0, 0
-2: 1, 0, 1

Keyboard matrix

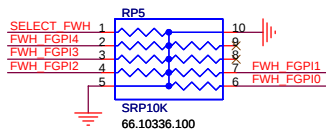
	US	Jap	Europe	US international
MATRIX1	HIGH	LOW	HIGH	HIGH
MATRIX2	HIGH	HIGH	LOW	HIGH

BOM2(NV44+G)

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
KBC&TPAD CONN			
Size A3	Document Number	Rev	
	CANARY2	SA	
Date: Thursday, January 13, 2005	Sheet 32	of	55



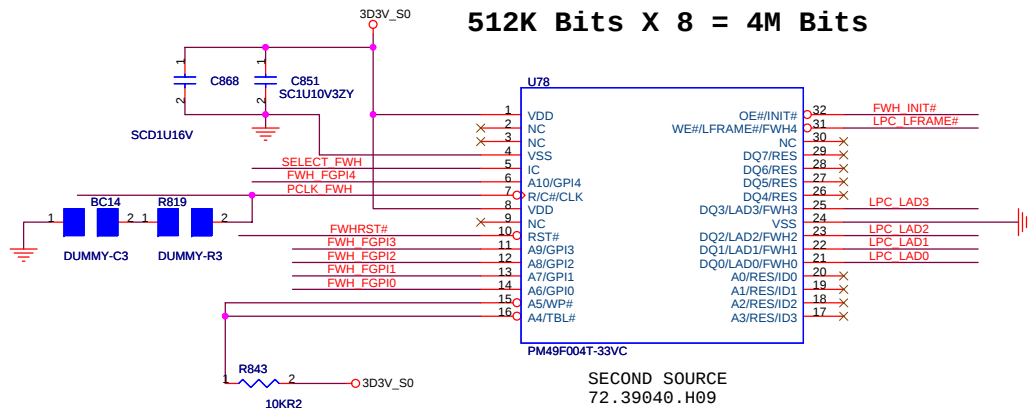
Unused FGPI pins must not be float



15,30,31 LPC_LAD[0:3] << >>

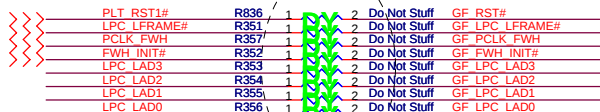
FLASH ROM

512K Bits X 8 = 4M Bits



SECOND SOURCE
72.39040.H09

7,16,18,30,31,34,46 PLT_RST1#
15,30,31 LPC_LFRAME#
3 PCLK_FWH
15 FWH_INIT#



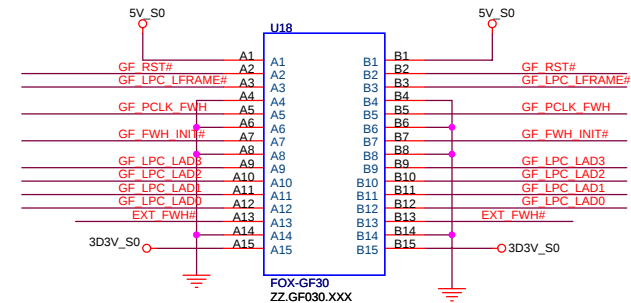
12/30

TOP VIEW

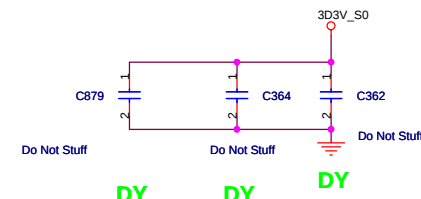
A15 (B1)
A14 (B2)
:
:
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

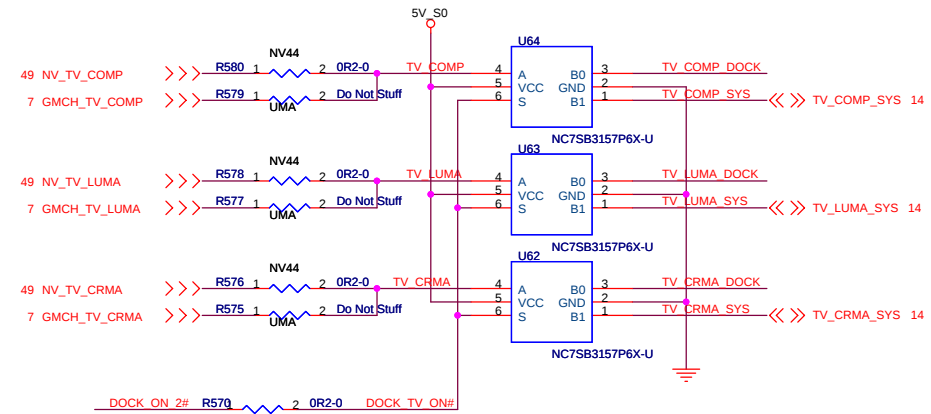


BOM2(NV44+G)

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

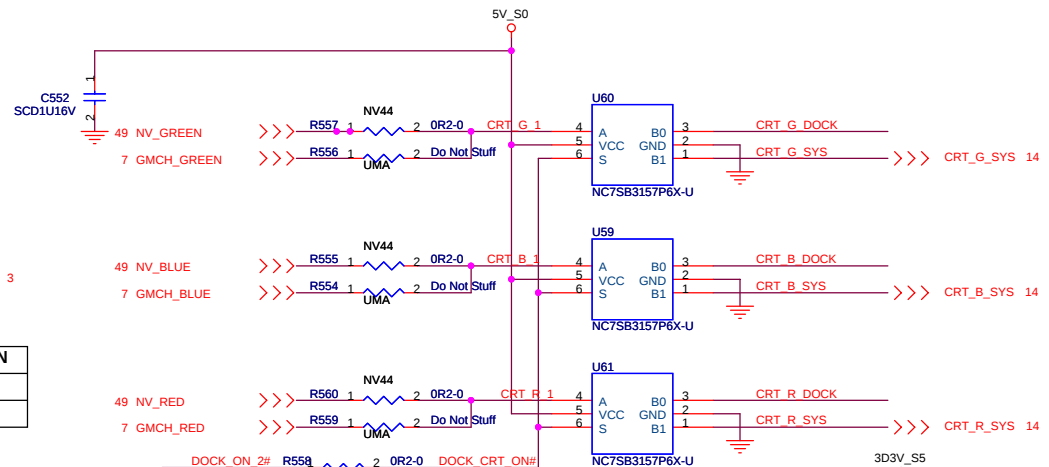
Title	FWH and Debug		
Size	Document Number	Rev	SA
A3	CANARY2		
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TV SWITCH



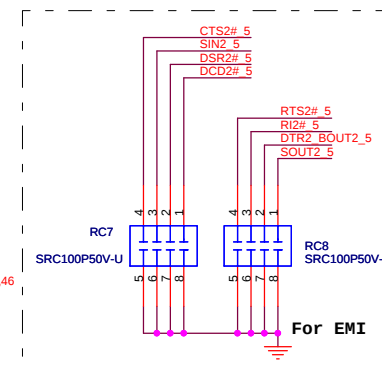
Function	S
A to B0	L
A to B1	H

CRT SWITCH



Function	LAN
SYSTEM	L
DOCK	H

Function	CRT	TV
SYSTEM	H	H
DOCK	L	L



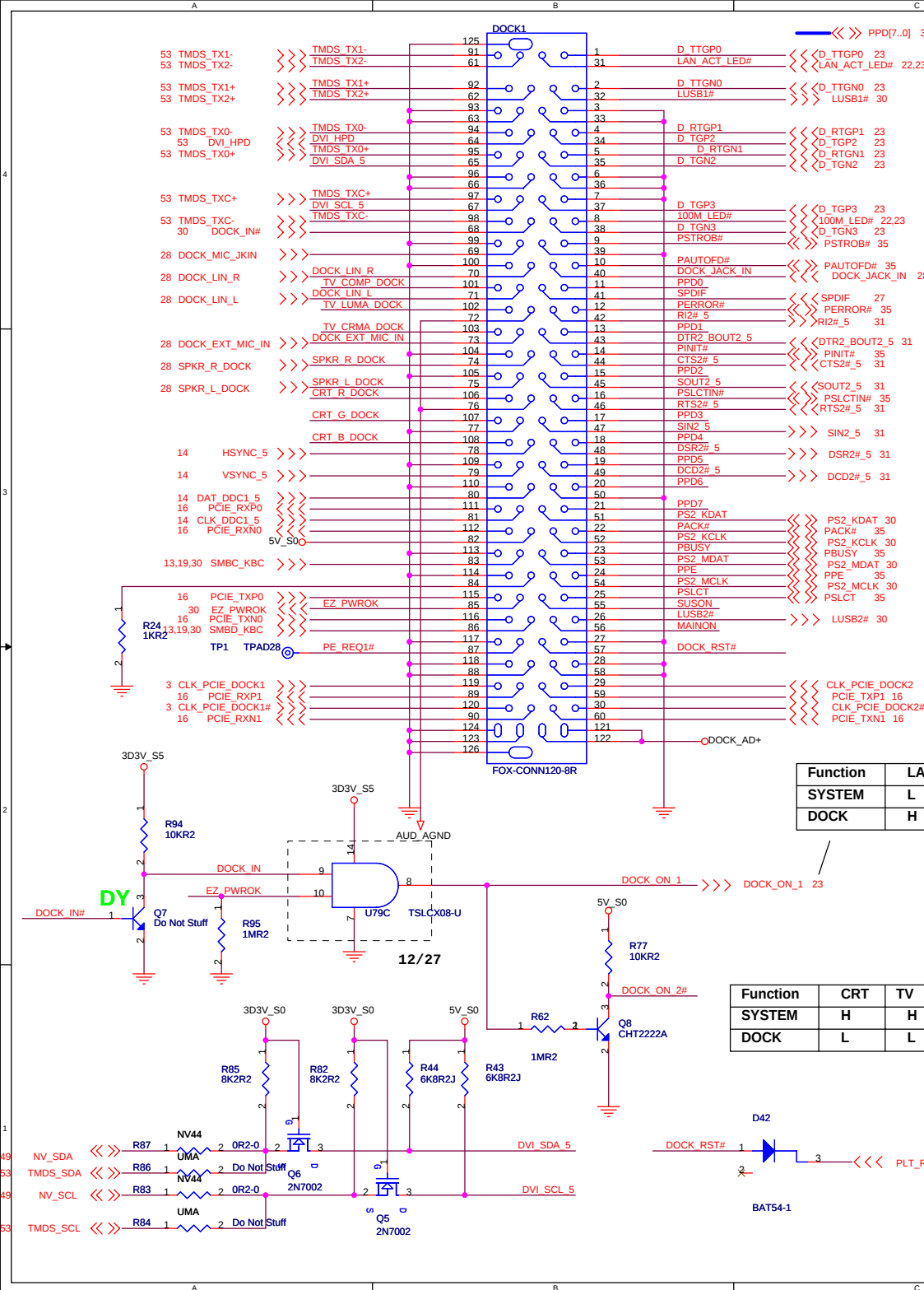
BOM2(NV44+G)

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

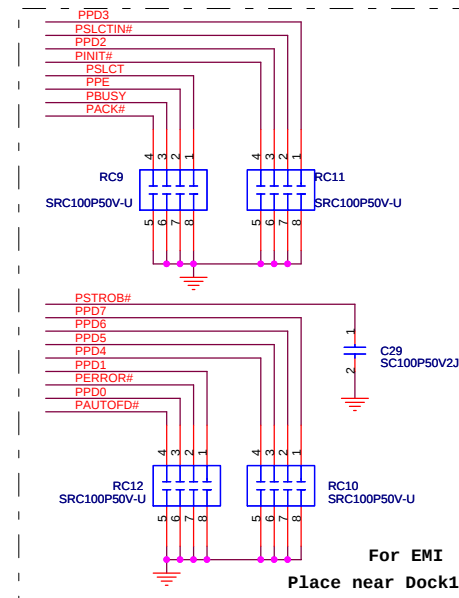
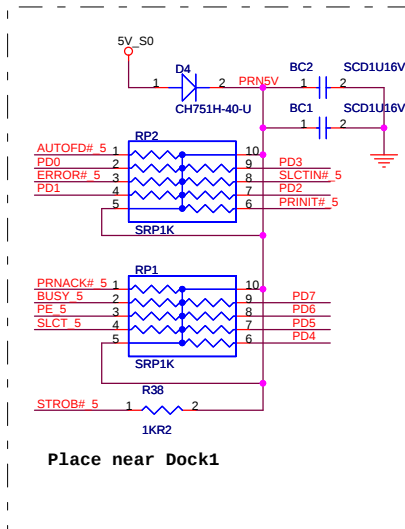
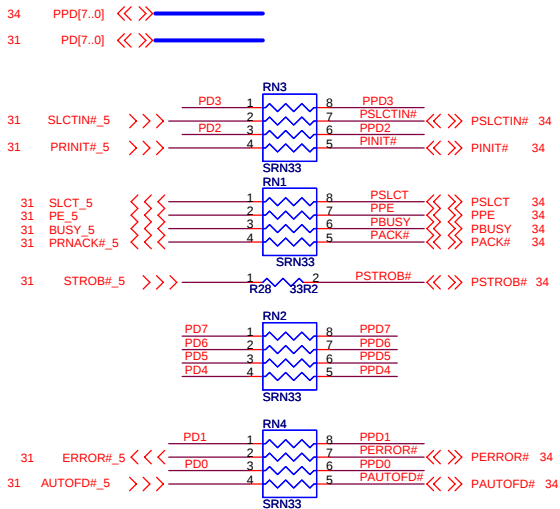
Title: **EASY PORT4 (1/2)**

Size A3 Document Number **CANARY2** Rev **SA**

Date: Thursday, January 13, 2005 Sheet 34 of 55

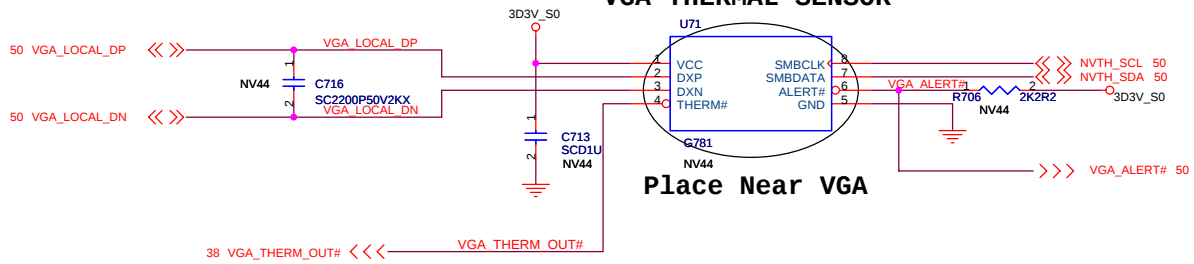


PRINT PORT

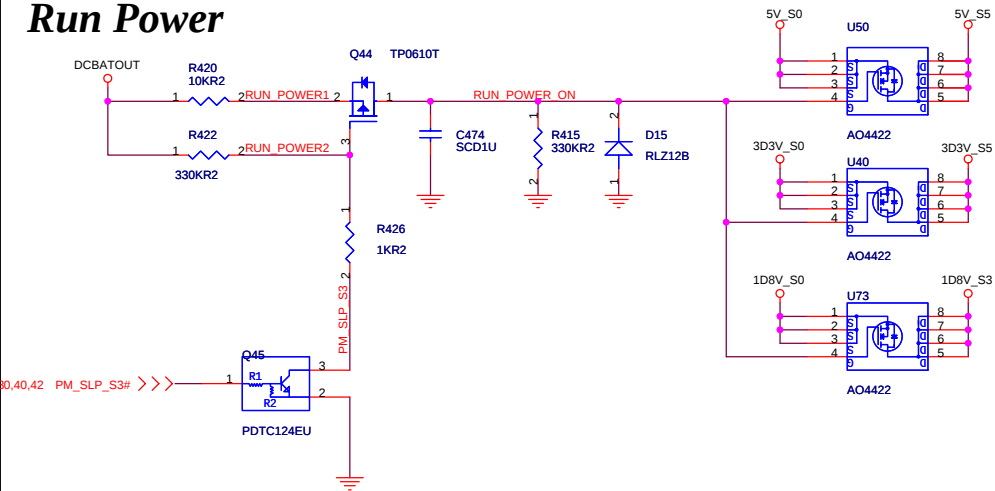


I2C ADDRESS: 0x98H

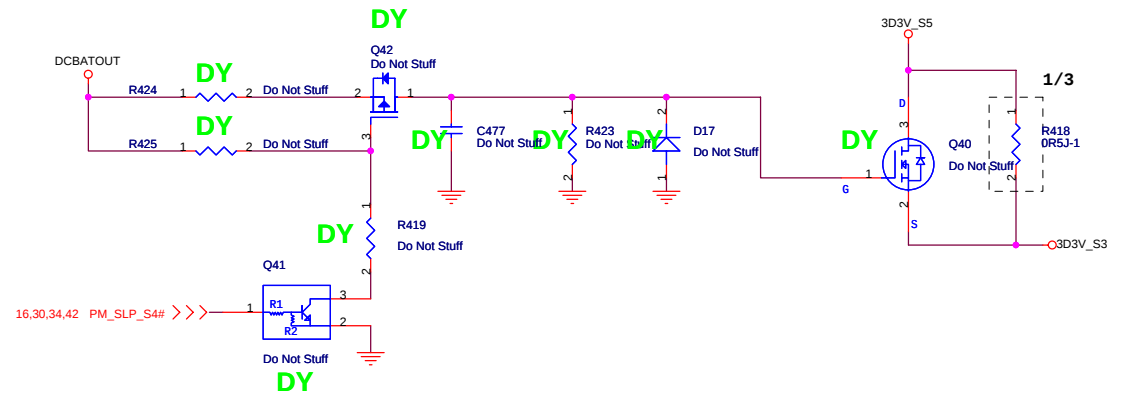
VGA THERMAL SENSOR



Run Power



Suspend Power



BOM2(NV44+G)

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RUN and SUSPEND Power

Size
A3

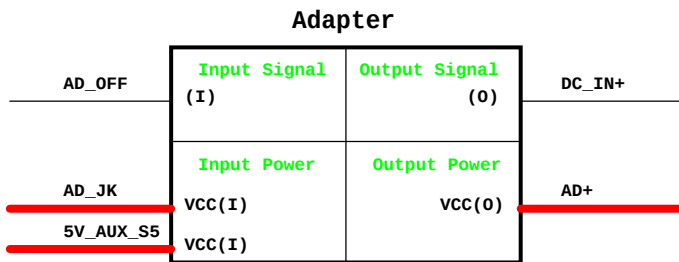
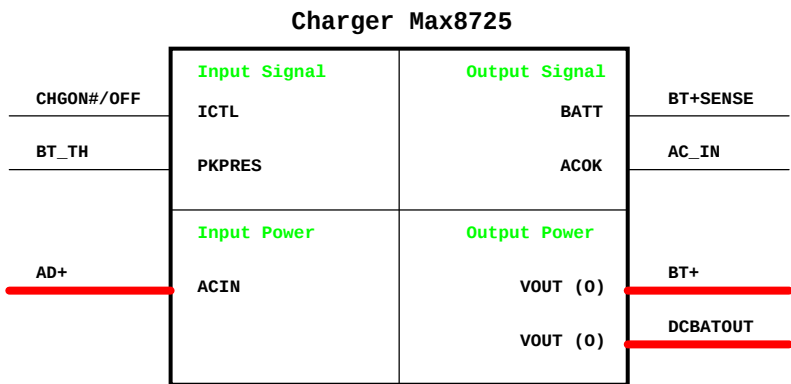
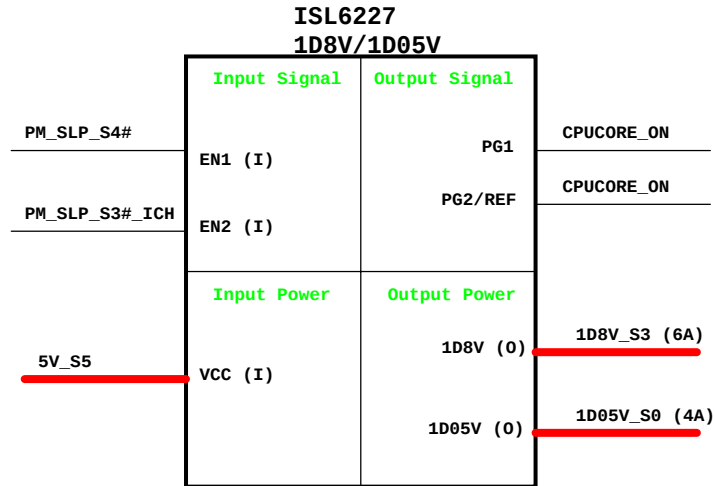
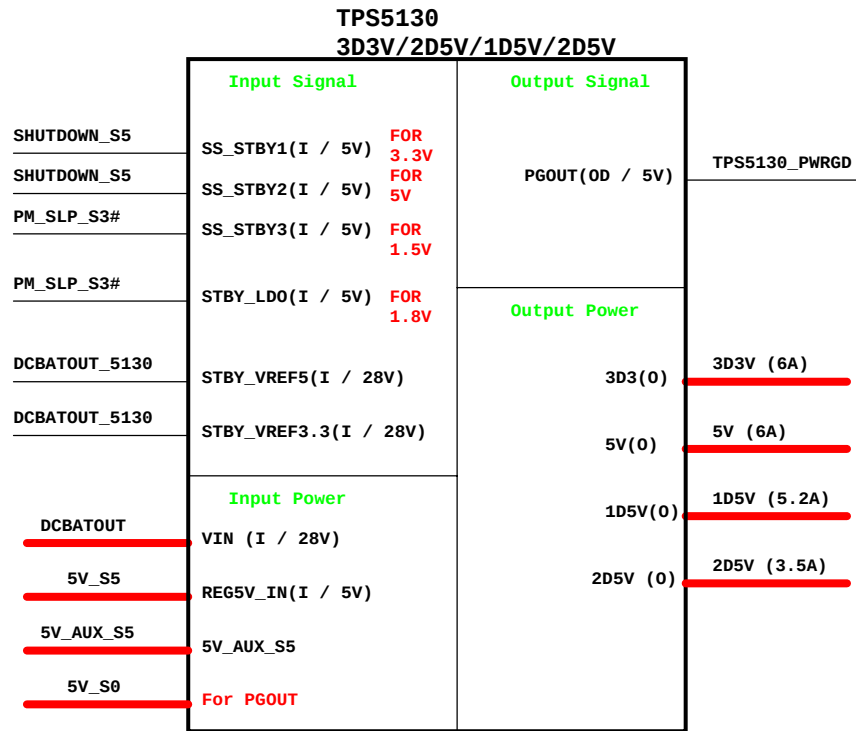
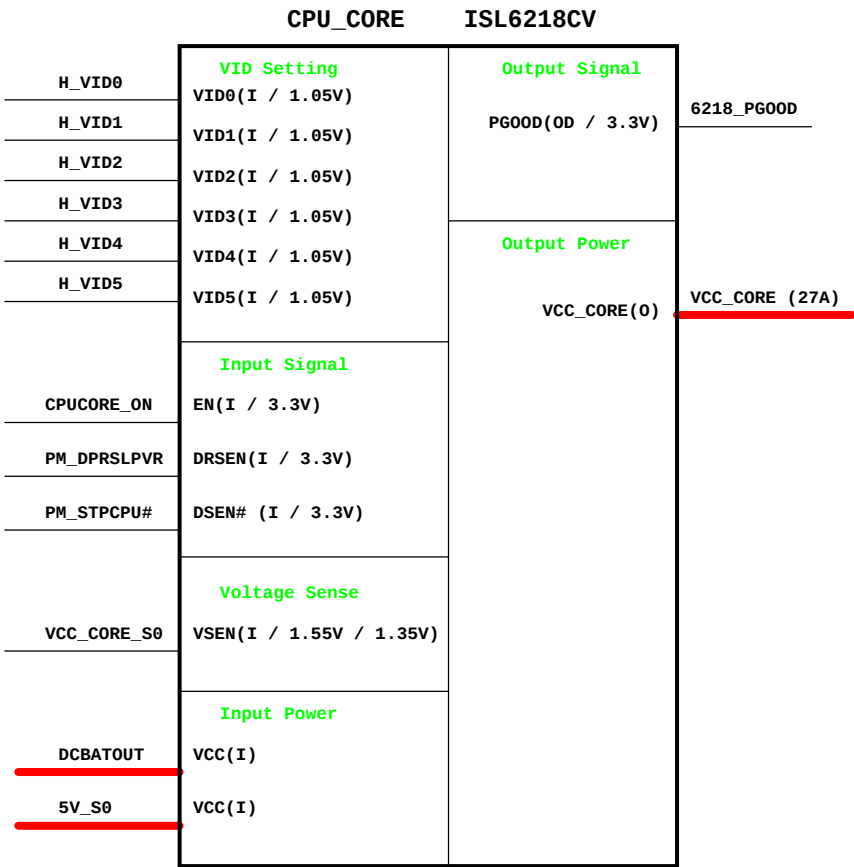
Document Number

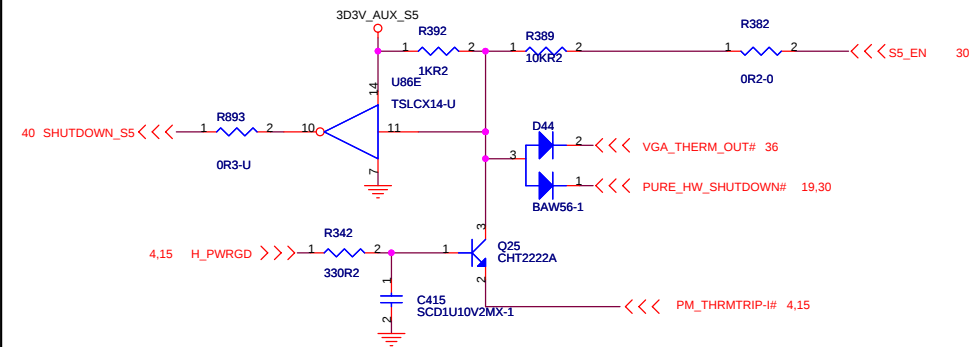
CANARY2

SA

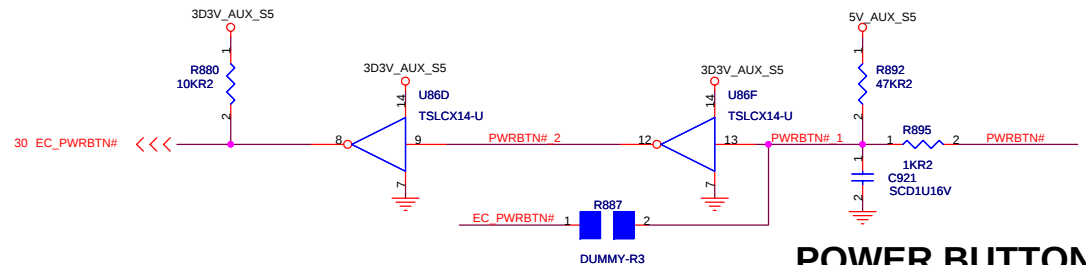
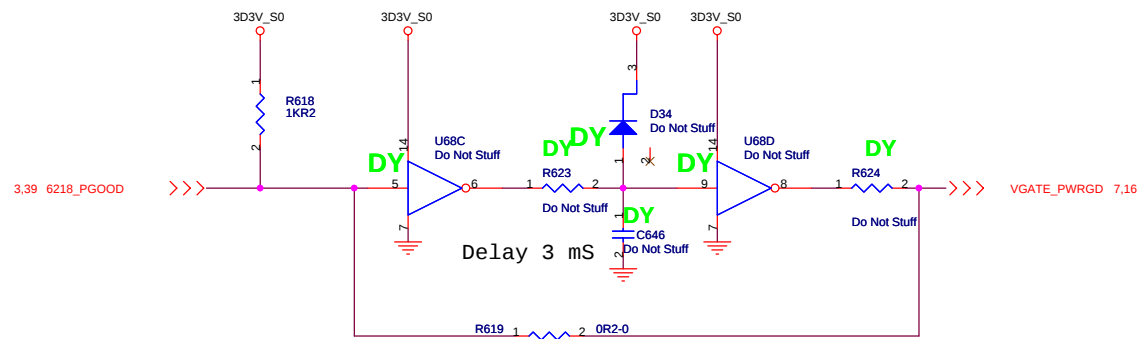
Date: Thursday, January 13, 2005

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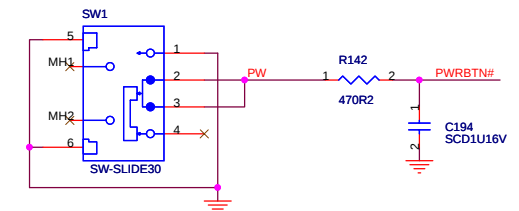


PWRGD for NB and SB



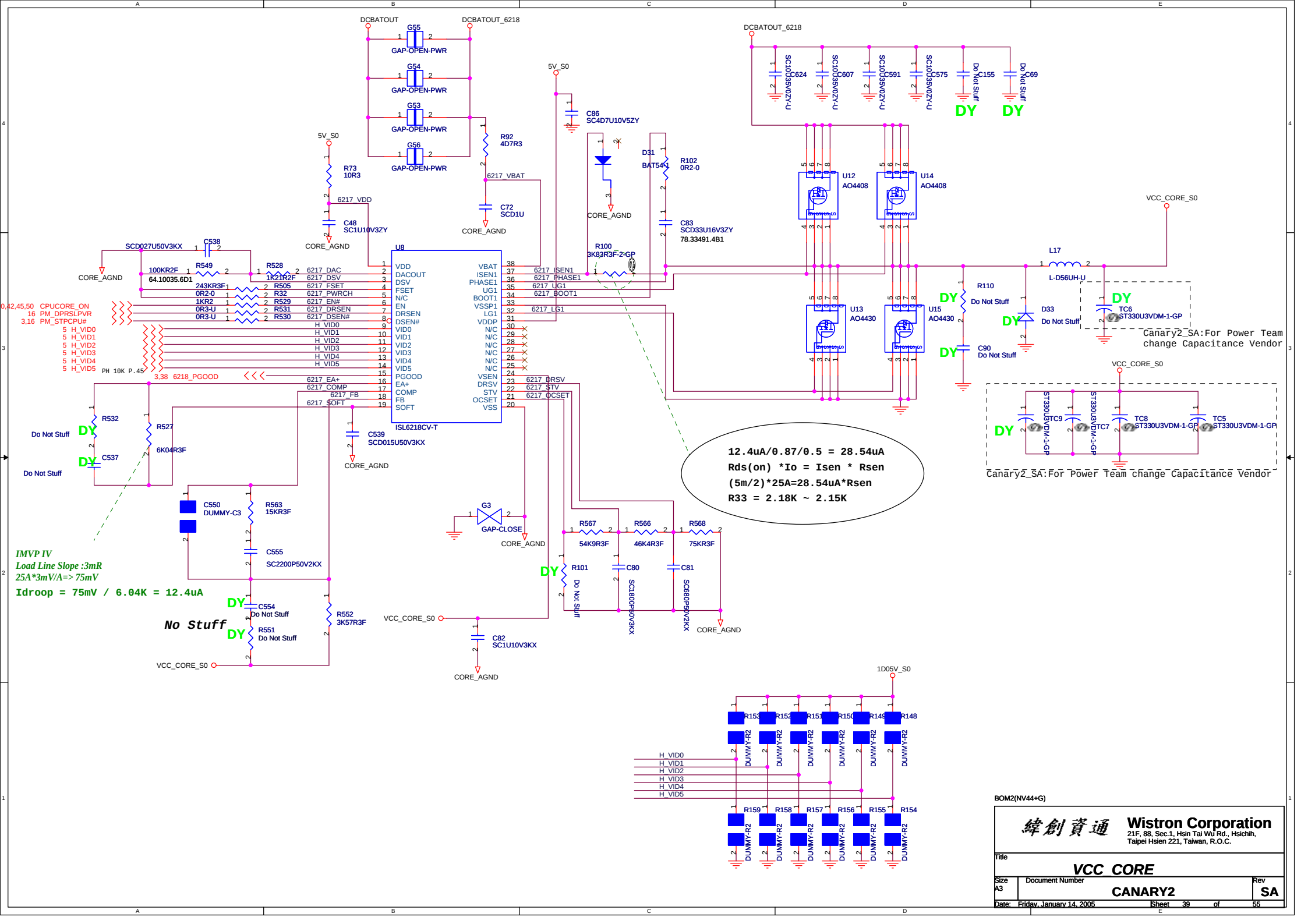
POWER BUTTON

POWERSWITCH



BOM2(NV44+G)

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
POWER ON CIRCUIT			
Size A3	Document Number	Rev	
	CANARY2	SA	
Date: Thursday, January 13, 2005	Sheet 38	of	55

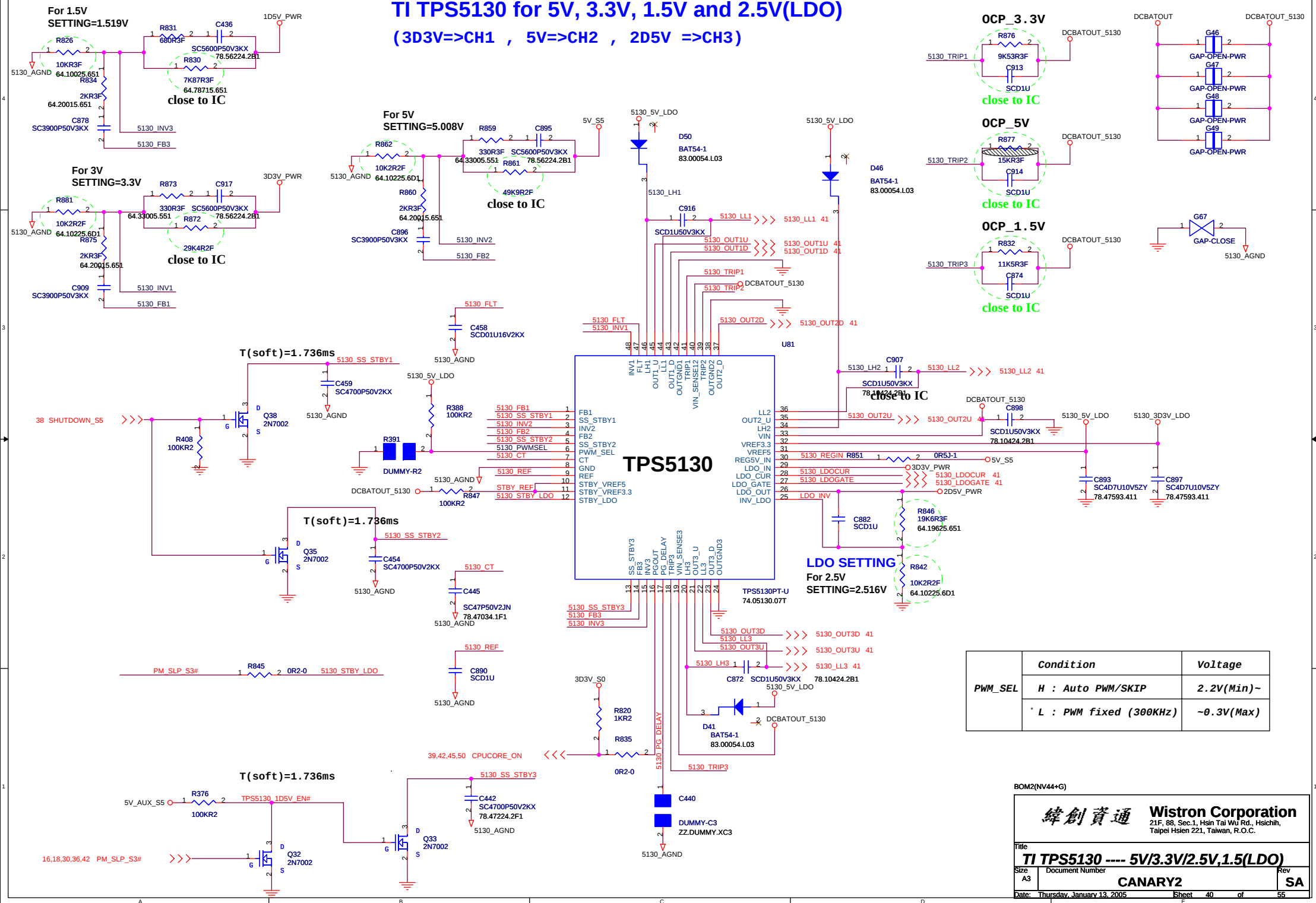


0.2,45,50 CPU CORE ON
16 PM DPRSLPVR
3,16 PM_STPCPU#
5 H_VID0
5 H_VID1
5 H_VID2
5 H_VID3
5 H_VID4
5 H_VID5
PH 18K P.45

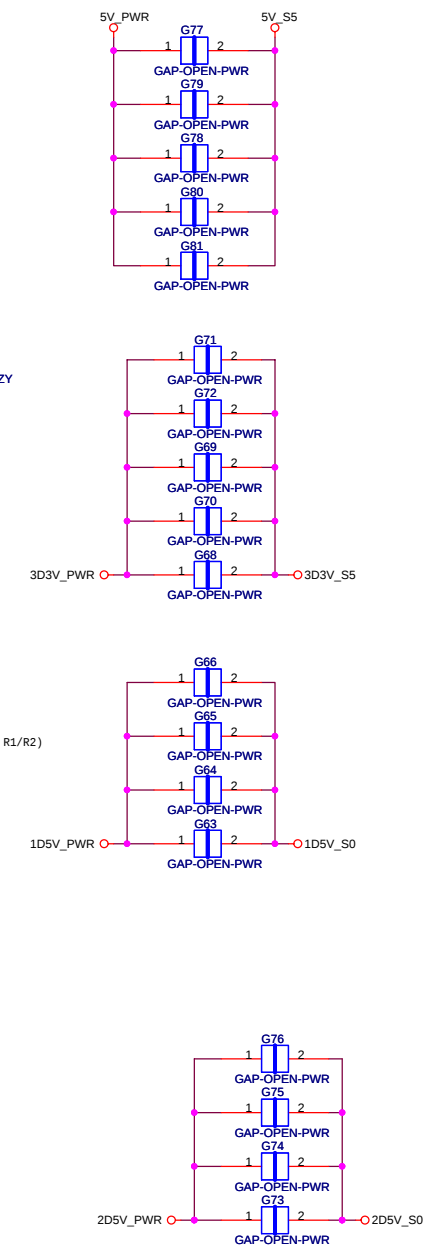
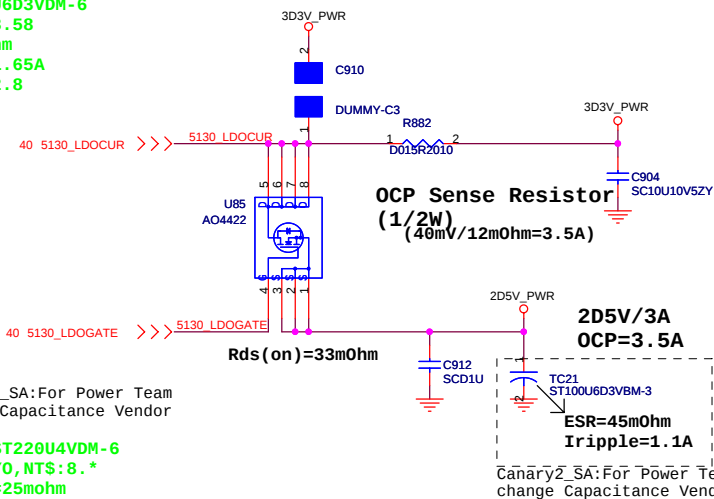
IMVP IV
Load Line Slope :3mR
25A*3mV/A=>75mV
Idroop = 75mV / 6.04K = 12.4uA

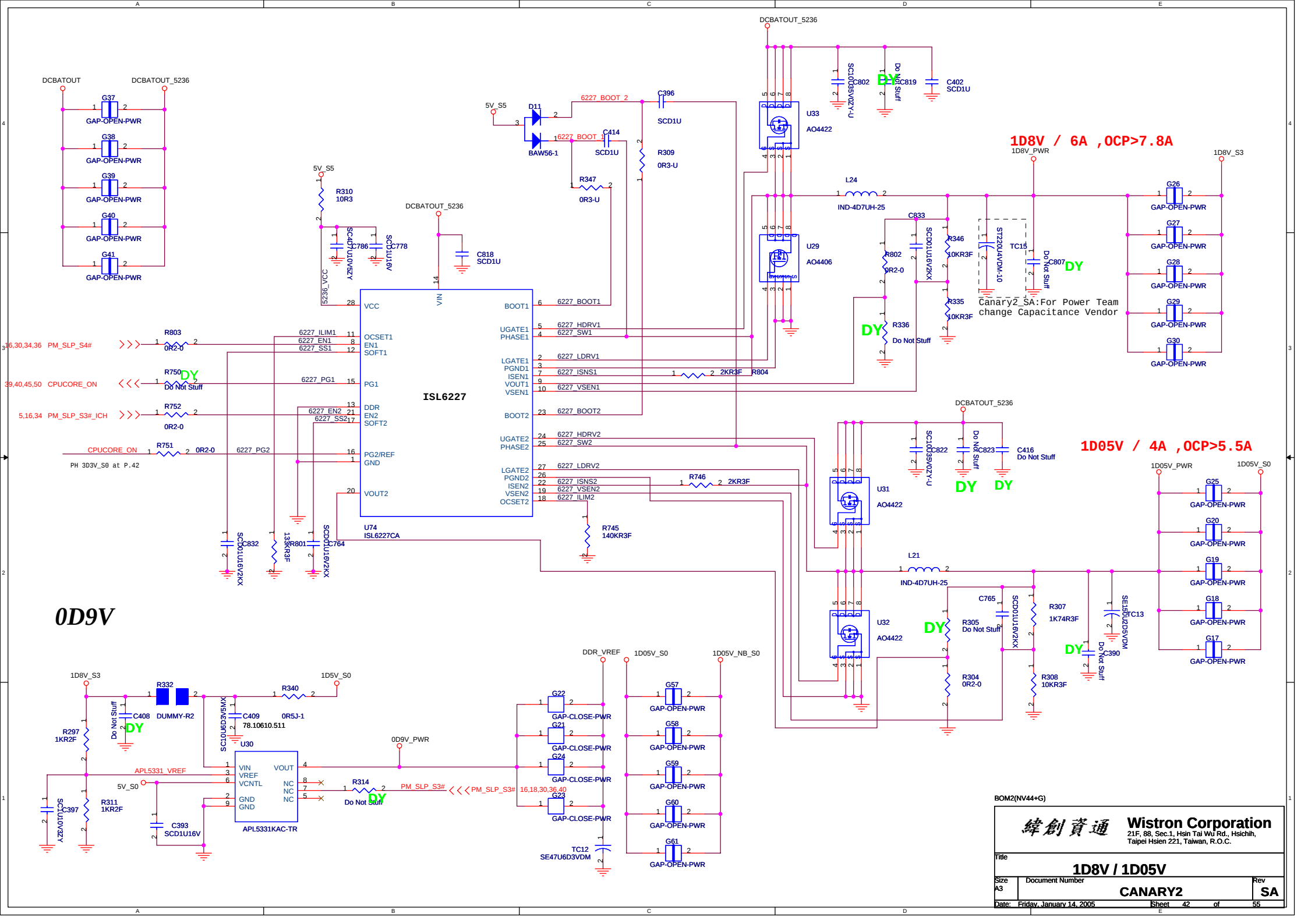
$$12.4\mu A / 0.87 / 0.5 = 28.54\mu A$$
$$R_{ds(on)} * I_o = I_{sen} * R_{sen}$$
$$(5m/2) * 25A = 28.54\mu A * R_{sen}$$
$$R33 = 2.18K \sim 2.15K$$

TI TPS5130 for 5V, 3.3V, 1.5V and 2.5V(LDO) (3D3V=>CH1 , 5V=>CH2 , 2D5V =>CH3)

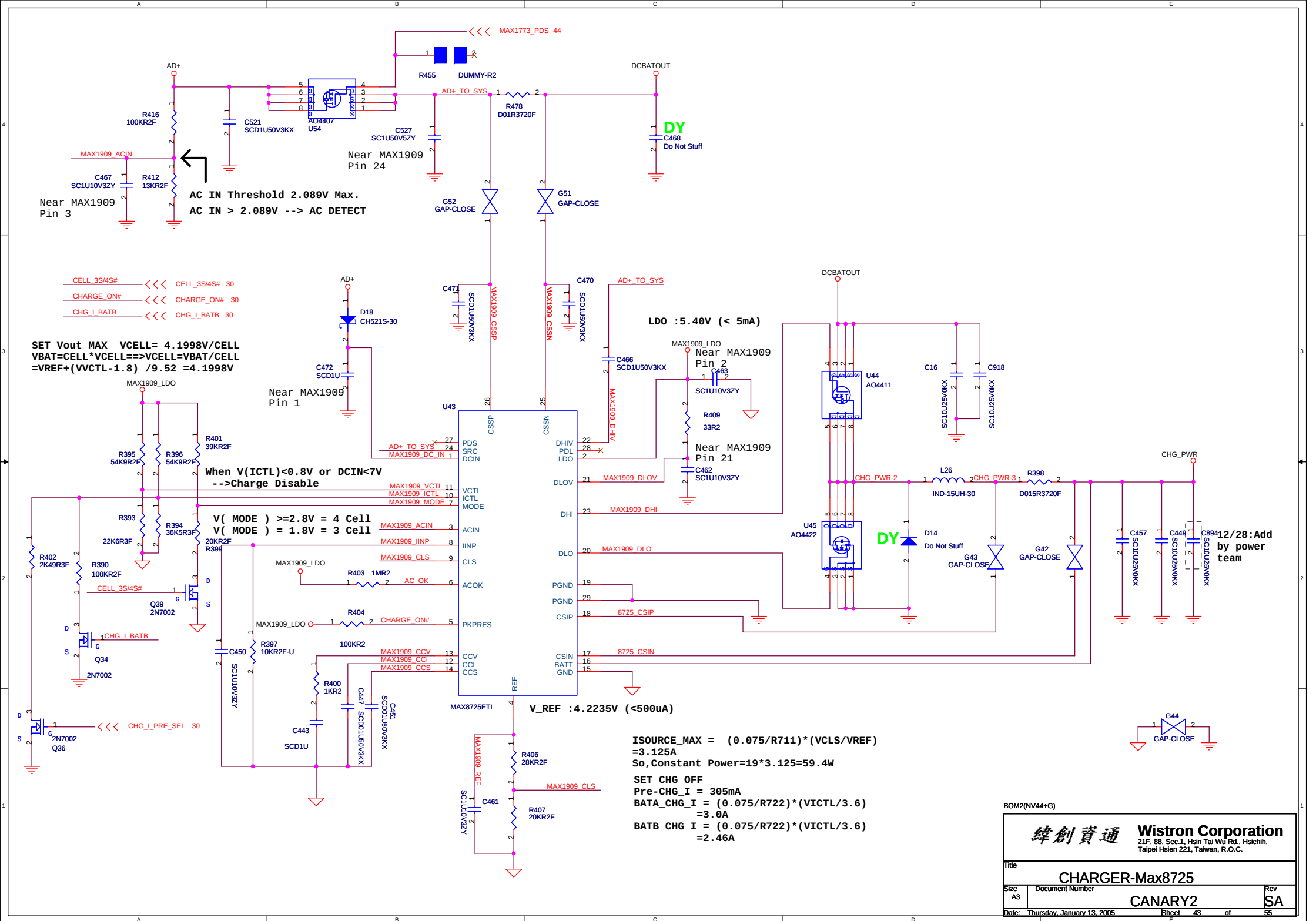


(3D3V=>CH1 , 5V=>CH2 , 2D5V =>CH3)

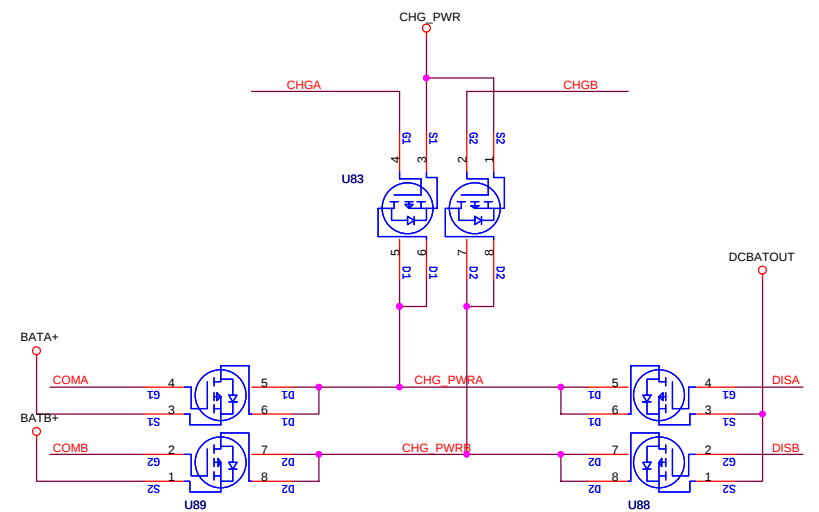
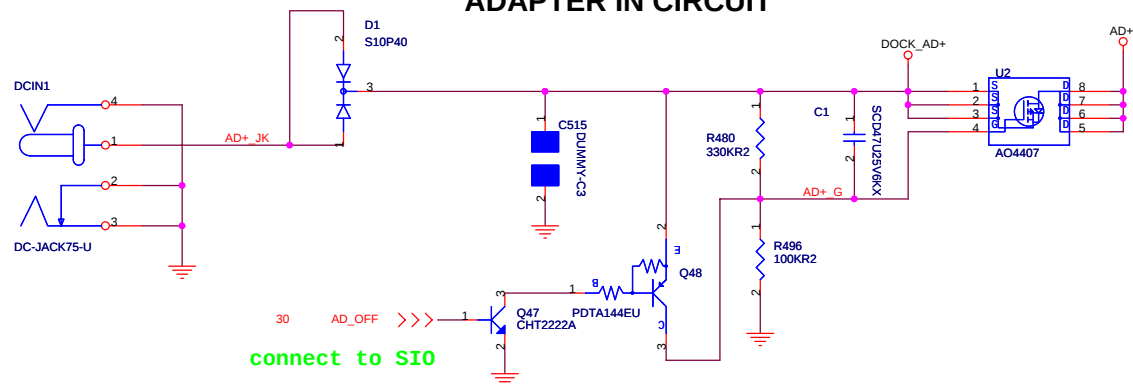




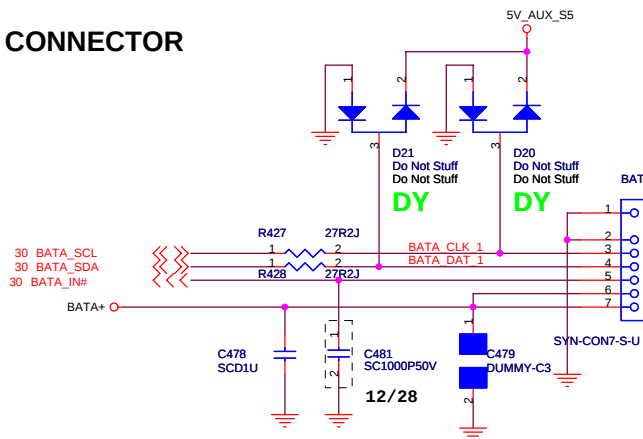
BOM2(NV44+G)		
Title		
1D8V / 1D05V		
Size	Document Number	Rev
A3	CANARY2	SA
Date: Friday, January 14, 2005		
Sheet 42 of 55		



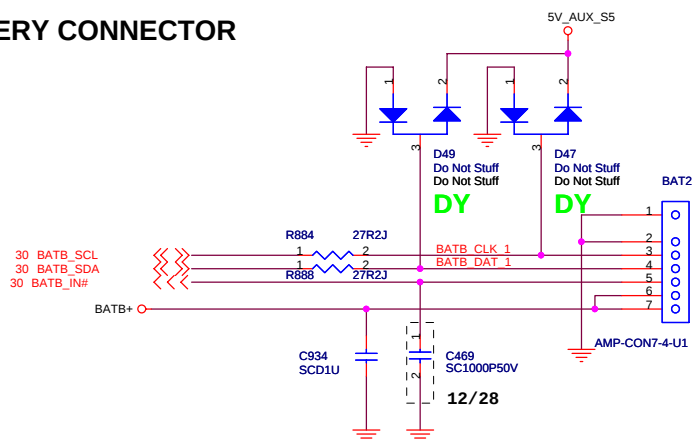
ADAPTER IN CIRCUIT



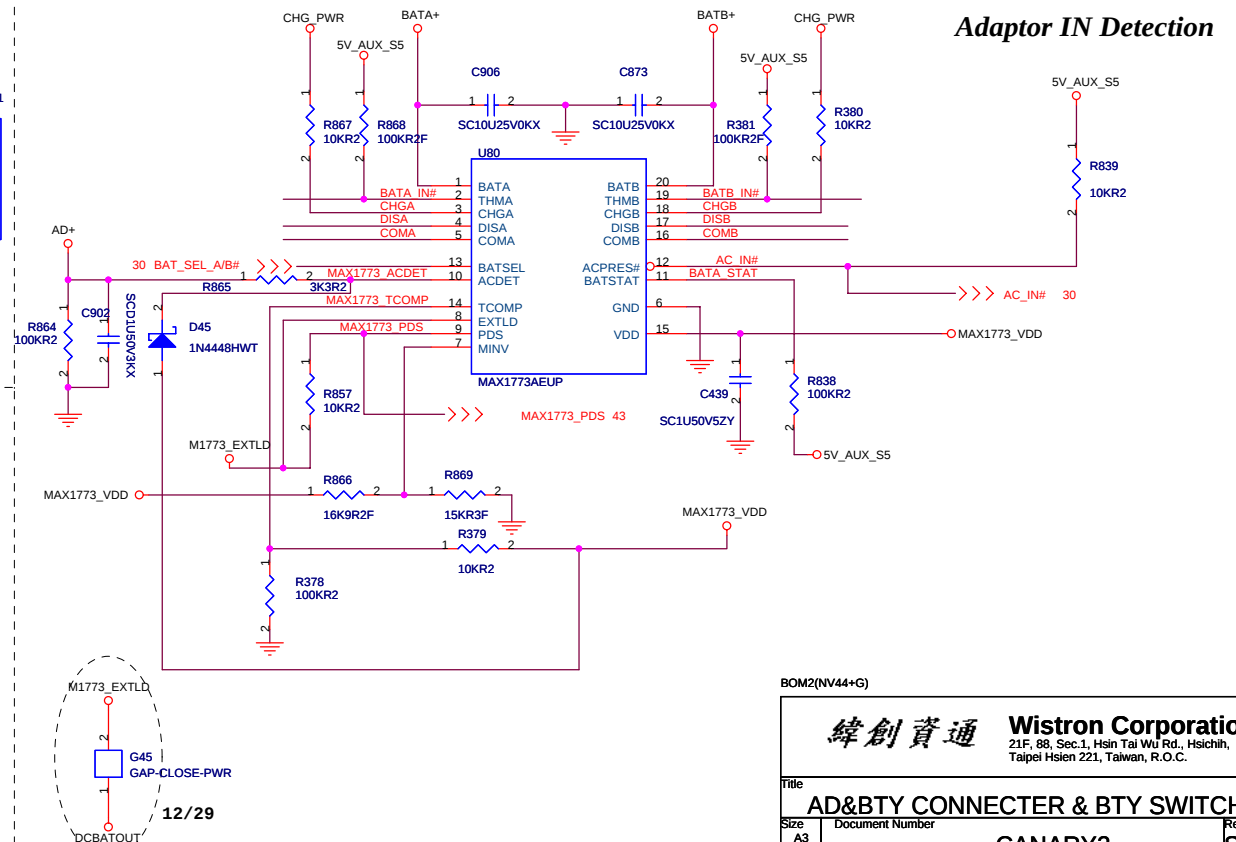
MAIN BATTERY CONNECTOR



2ND BATTERY CONNECTOR



BATTERY SWITCH

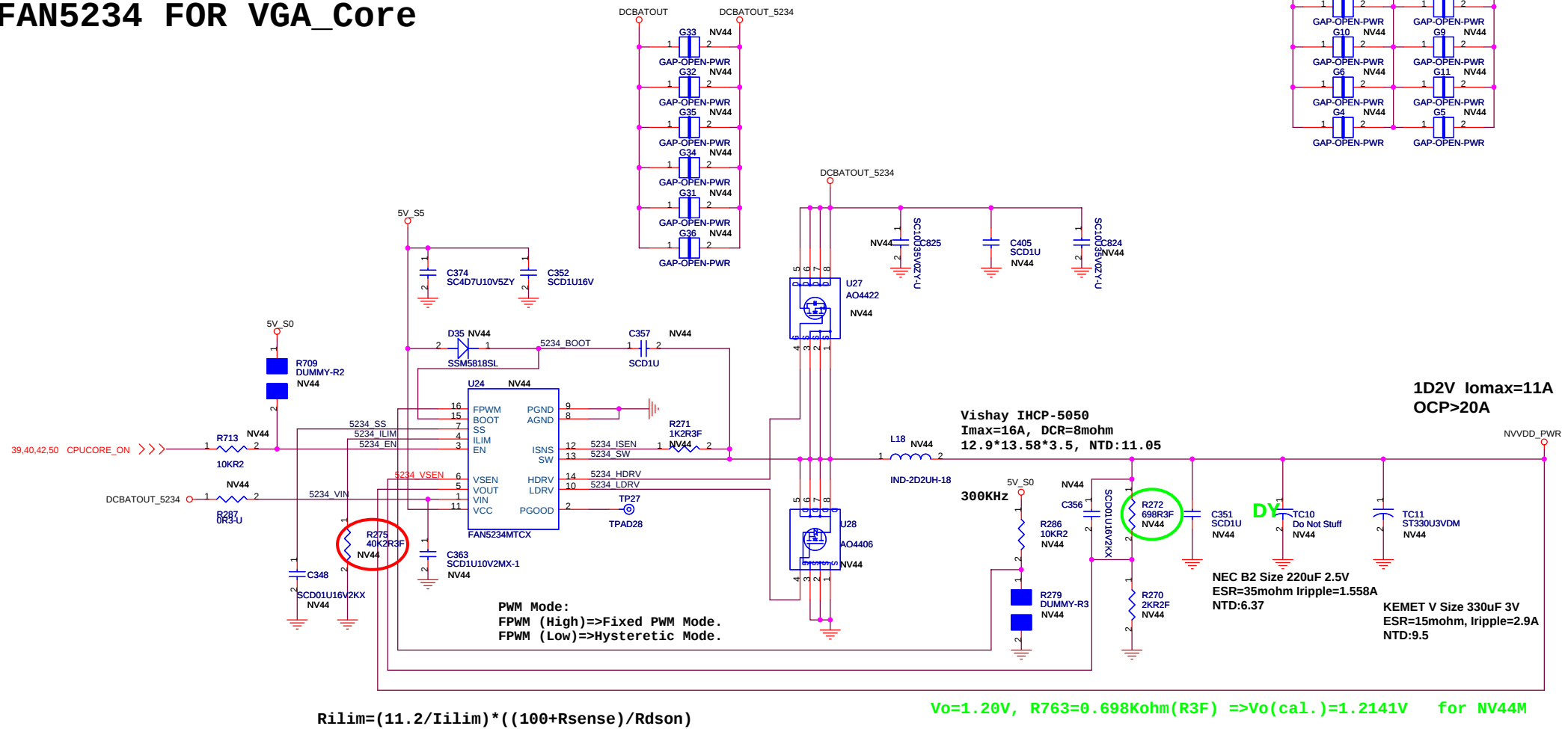


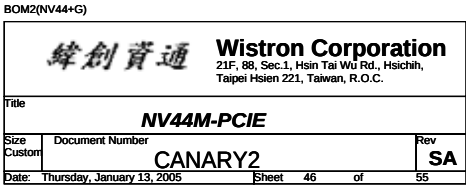
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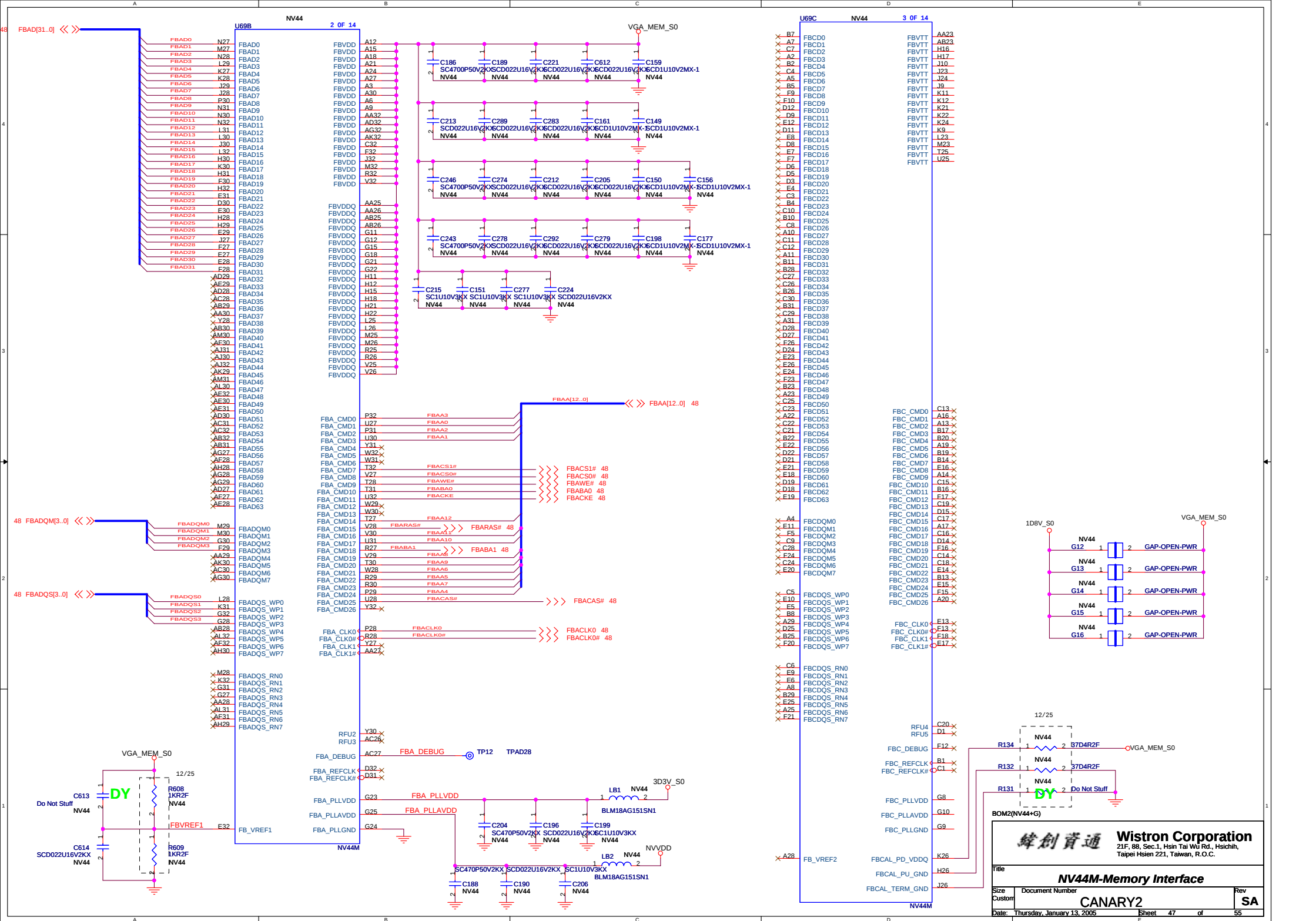
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

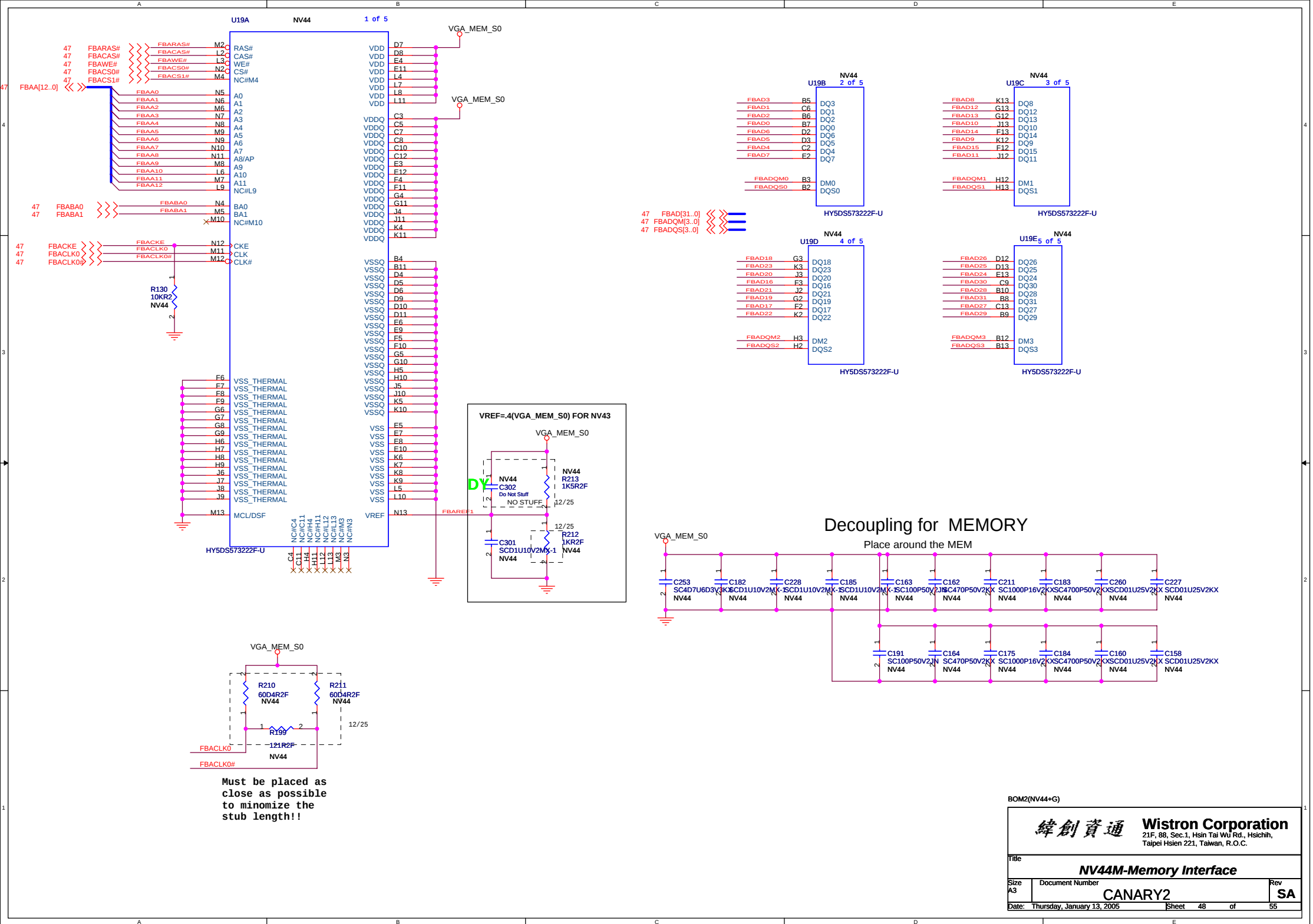
Title			
AD&BTY CONNECTER & BTY SWITCH			
Size	Document Number		Rev
A3	CANARY2		SA
Date:	Monday, January 17, 2005	Sheet 44 of	55

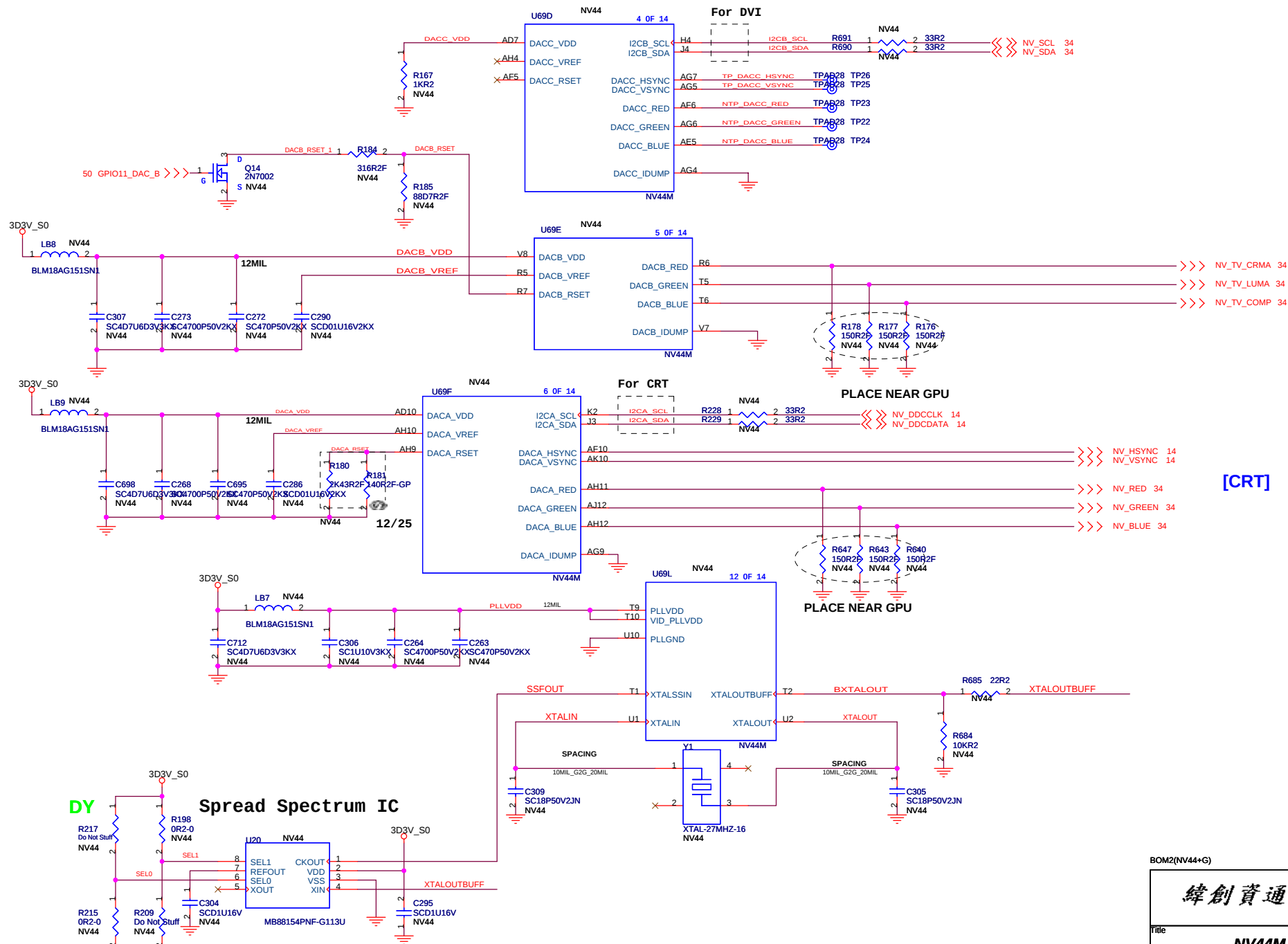
FAN5234 FOR VGA_Core

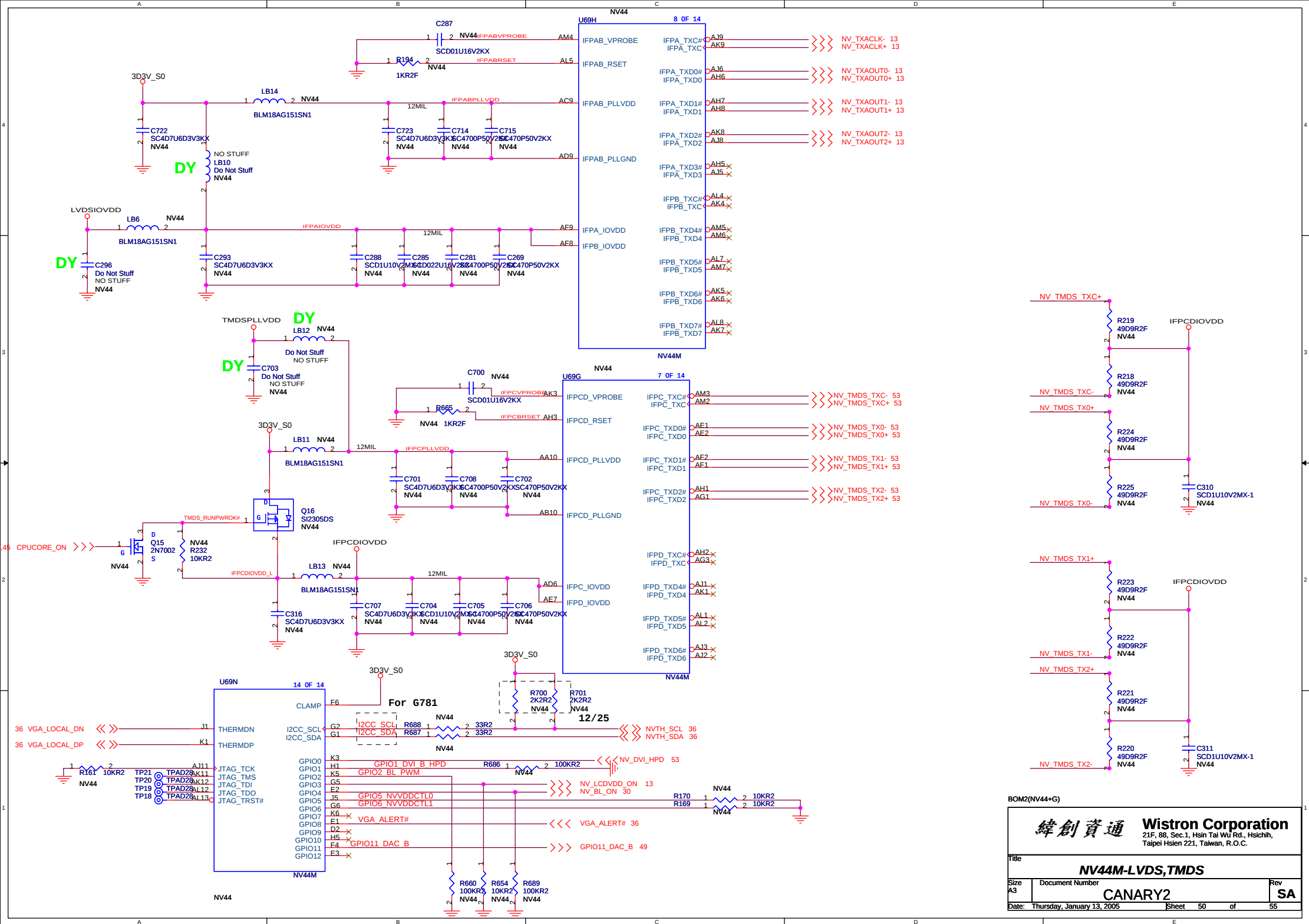


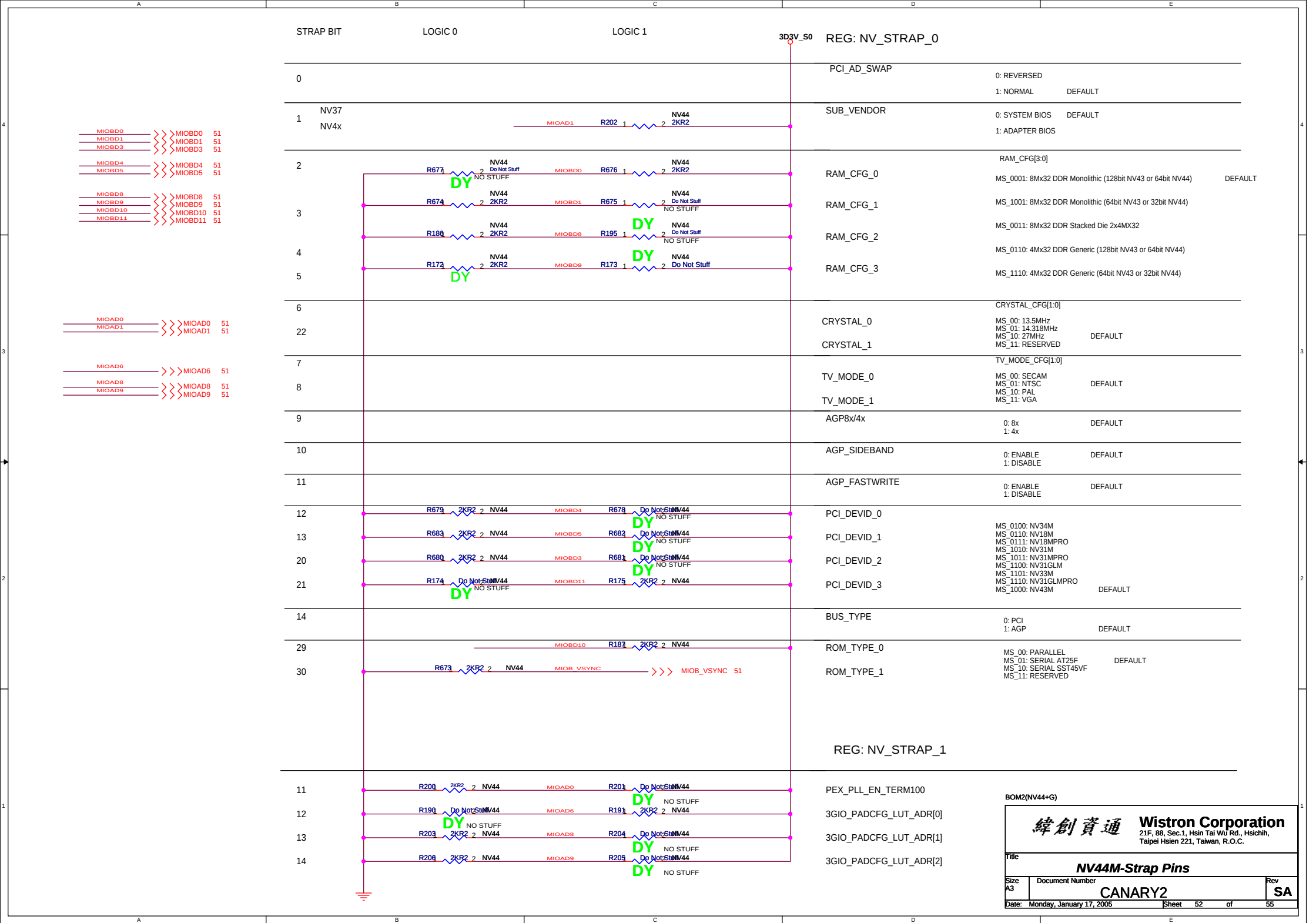


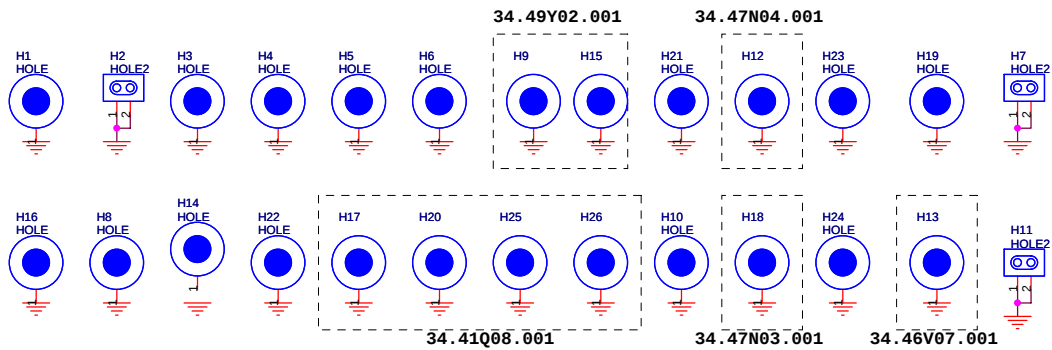
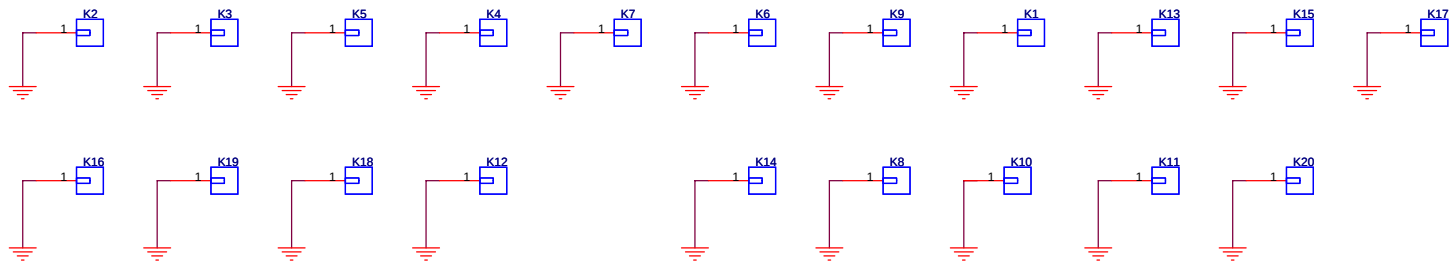
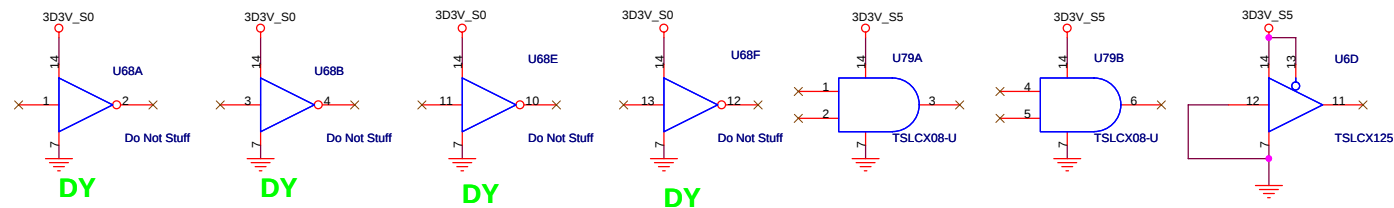




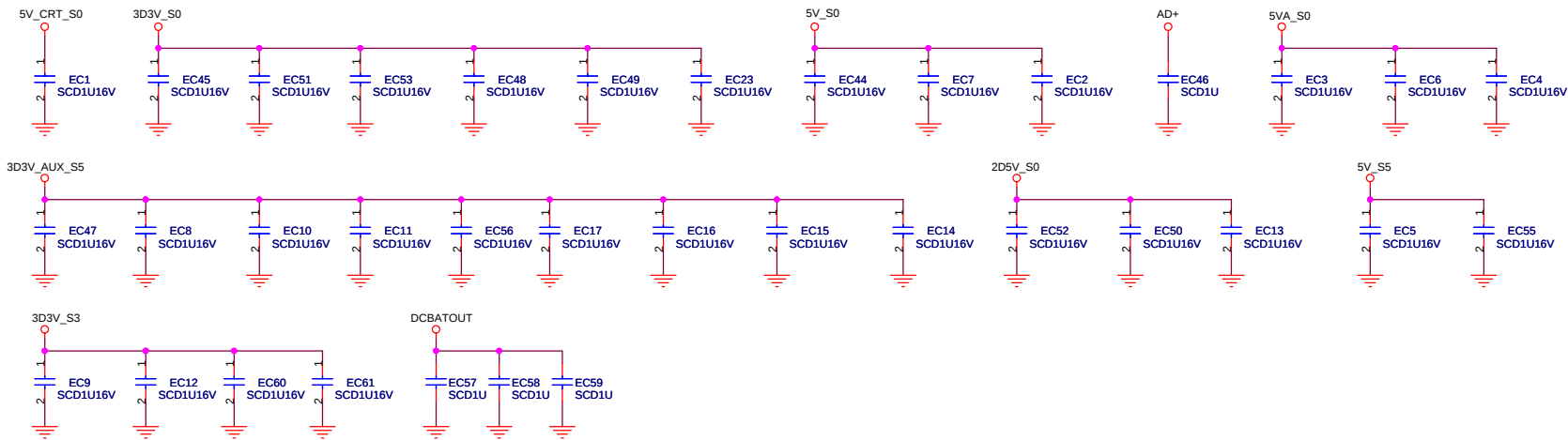








BYPASS CAP



CROSS PLANE CAP