MODEL	REV	CHANGE LIST
ZL9	1A	Preliminary Release
	2A	Page 4 : Add C573 4.7pf for Signal quanlity Page 6 : Add R460 0om for UMA. Page 11 : seprate SATALED# for IDE interrupt. Page 14 :add R45 0ohm for M52-T. Page 19 : enlarge H22,H23 to 6mm for VGA sink Nut. Page 24 : Add 459 10Kohm for keep the GPIO normal Low. Page 25 : Add R239 0ohm for Po Po sound. Page 27 : Add R458 , Q25 for SATALED#. Page 28 : PL14->0.6uH,PR122->680ohm,PR120->680ohm,PR118->470ohm,PC55->220P,PR38->160K for power efficiency. Page 30 : PR40->20K,PD11->CH551,PC39->.22U,PC46->2.2n,PL11->1.5UH,PR59->221K for power efficiency. Page 30 : PC176->1000P,PC182->1000P,PC179->1000P,PC180->100P,PC181->100P,PC177->1000P for EMI. Page 31 : PR142->0 , PR94->100K,PR95->0,PR93->100K for battery charger modify ,PC178->1000P for EMI. Page 32 : PR15->6.65K , PL6->1.0UH for power efficiency.
	3A	Page 25 : R250->100Kohm, Q13->2N7002,Q23->2N7002,Add Q24 AO3403 for SPDIF on/off LED. Page 27 :Del R458 , Q25 for HDD LED can't light issue.

Model	ZL8 MB	
Page	FM	TO
1	1A	
2	1A	
3	1A	
4	2A	
5	1A	
6	2A	
7	1A	
8	1A	
9	1A	
10	1A	
11	2A	
12	1A	
13	1A	
14	2A	
15	1A	
16	1A	
17	1A	
18	1A	
19	2A	
20	2A	
21	1A	
22	1A	
23	1A	
24	2A	
25	2A	3A
26	1A	
27	2A	3A
28	2A	
29	1A	
30	2A	
31	2A	
32	2A	

QUANTA COMPUTER

PROJECT : ZL9	DOC. NO. ???	REV: 1A	ASSY: 31ZL9MB0020	
APPROVED BY : Vic Lin #15598	CHECKED BY: Jerry Lin #15573	DRAWING BY : Jerry Wang #13011		DATE: 2005/12/20

ZL9

CPU CORE
SENTECH
SC451ITSTR
Page:28

SYSTEM 3V/5V
MAXIM
MAX1999
+3VPCU
+3V_S5/+3VSUS
+3V
+5VPCU
+5VSUS
+5V
+15V Page:29

+1.8VSUS
+1.8V
+0.9VSUS
+0.9V ON
NCP5214
+1.5V SENTECH
SC1470
+1.5V_S5
SI9183-AD
+2.5V
SENTECH
SC1565
+1.05V
SENTECH
SC4215
Page:30
+1.2V
SENTECH
SC4215
+NVVDD
SENTECH
SC1470
Page:32

BATTERY CHARGER
MAXIM
MAX8724
Page:31

CLOCK GEN
ICS954206
(RTM865T-433)
Page:4

CELERON-M/PENTIUM-M
INTEL Mobile_479 CPU
Page:2, 3

HOST BUS 533/400MHZ

NB
INTEL
ALVISO 915PM/GM
Page: 5, 6 , 7, 8

PCIE

ATi
M52-T
Page: 14, 15
16, 17

RGB
LVDS

CRT
Page: 19

LVDS
Page: 19

DDR-II

DDR-II SODIMM1
Page: 10

DDR-II SODIMM2
Page: 10

UMA(option)

DMI I/F

SB
INTEL
ICH6-M
Page: 11 , 12 , 13

ATA 66/100

SATA HDD
Page: 20

PATA HDD
Page: 20

IDE-ODD
Page: 20

HD Audio

PCI-E BUS

PCI BUS 33MHZ

USB 2.0

LPC 33MHZ

MINI-PCIE slot
Wireless LAN
(Option)
Page: 21

TI PCMCIA
PCI1510
AD17
REQ1# / GNT1#
INTC#
Page: 23

TYPE II
SLOT
Page: 23

MINI-PCI
Wireless LAN
AD20
REQ2# / GNT2#
INTB# , INTD#
Page: 21

REALTEK
RTL8100CL
AD24
REQ0# / GNT0#
INTA#
Page: 22

RJ45
Page: 22

AUDIO CODEC
Realtek
ALC883 (ALC260)
Page: 24

AMP
MAX9755
Page: 25

MODEM
Page: 24

KBC
NS
PC97551/541V
Page: 26

MIC IN Page: 24

SPEAKER Page: 25

LINE OUT Page: 25

RJ11 Page: 22

Touchpad Page: 27

Keyboard Page: 27

FLASH Page: 26

FAN Page: 27

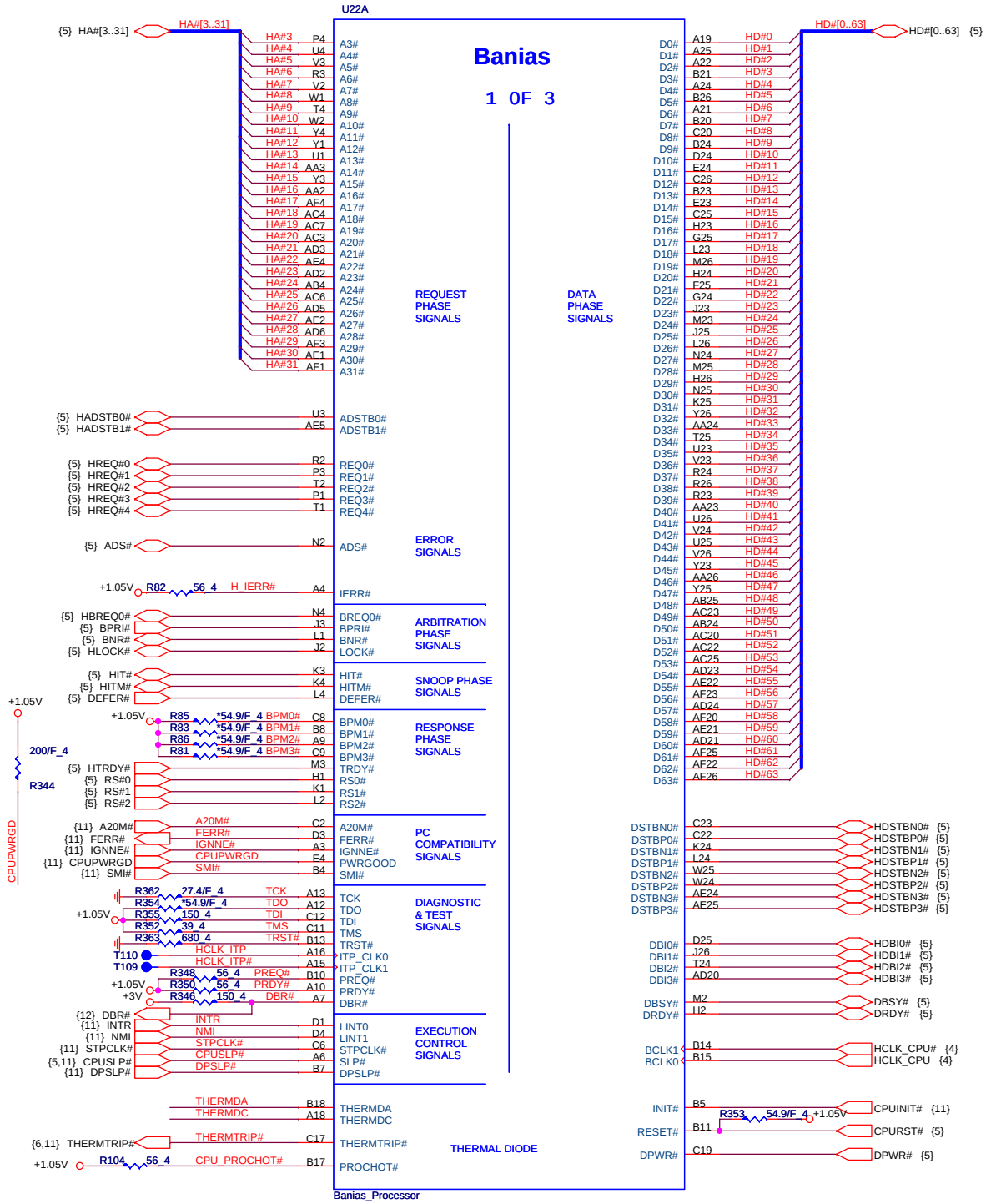
SYSTEM
USB PORT *3
USB2,3,5 Page:21

Bluetooth
USB
interface
USB4 Page:21

PROJECT : ZL9
Quanta Computer Inc.

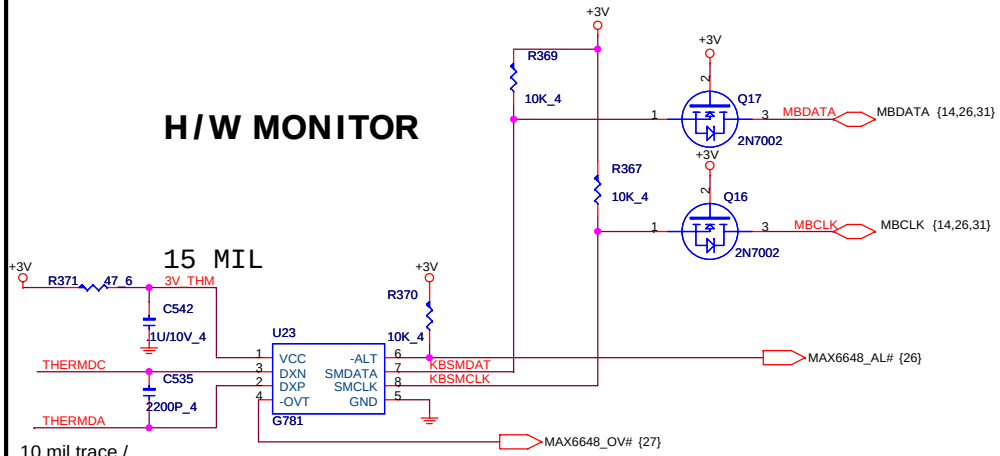
Size	Document Number	Rev
	BLOCK DIAGRAM	3A

Date: Monday, December 19, 2005 Sheet 1 of 32



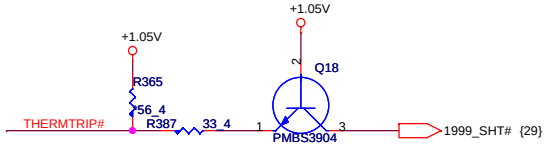
H/W MONITOR

15 MIL



10 mil trace /
10 mil space

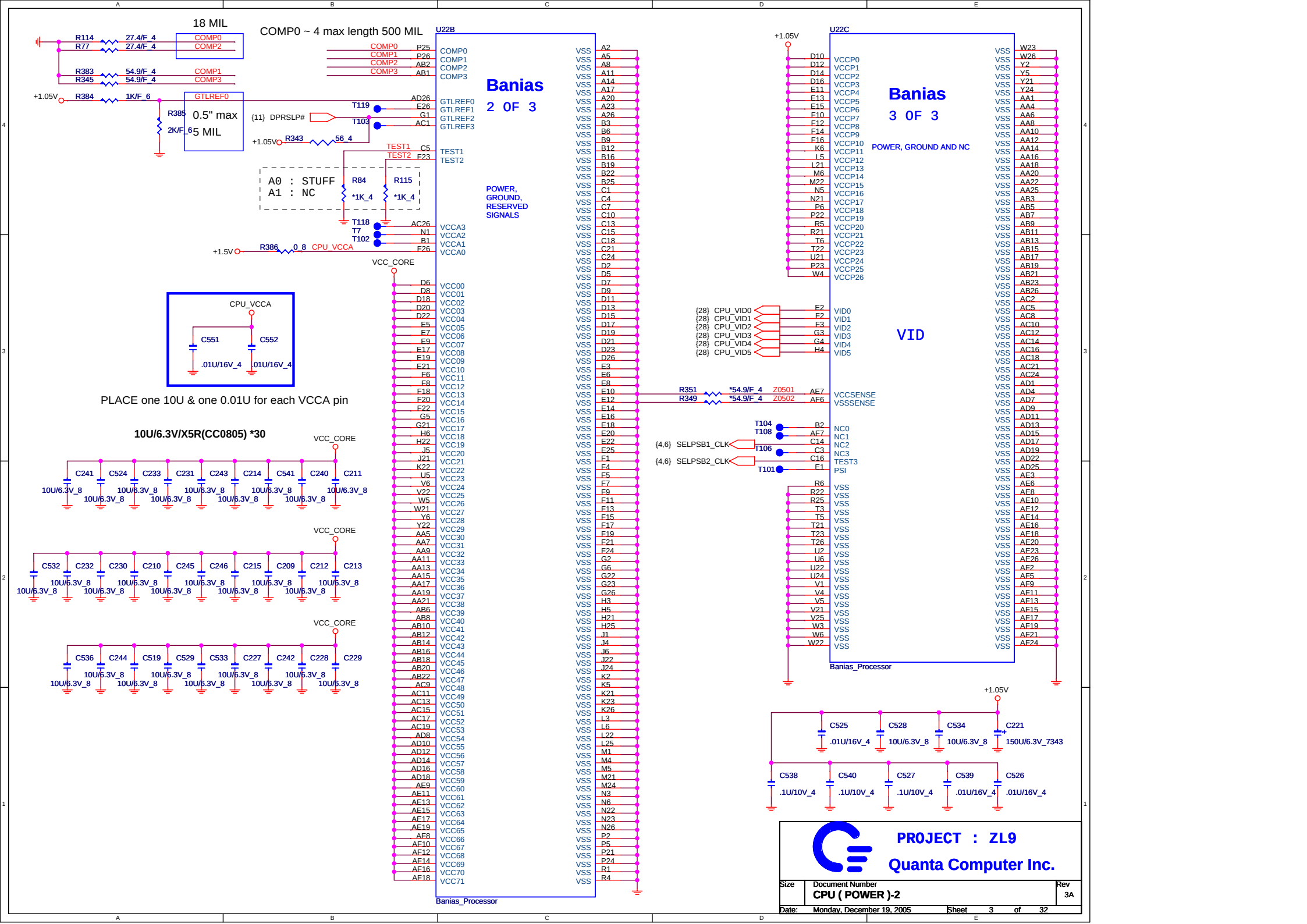
SLAVE ADDRESS: 98



PROJECT : ZL9

Quanta Computer Inc.

Size	Document Number	Rev
	CPU (HOST BUS)-1	3A
Date: Monday, December 19, 2005	Sheet 2 of 32	


18 MIL
COMP0 ~ 4 max length 500 MIL
R114 27.4/F_4 COMP0
R77 27.4/F_4 COMP2
R383 54.9/F_4 COMP1
R345 54.9/F_4 COMP3
+1.05V
R384 1K/F_6
GTLREF0
R385 2K/F_6
0.5" max
5 MIL
{11} DPRSLP#
R343 56_4
+1.05V
A0 : STUFF
A1 : NC
R84 *1K_4
R115 *1K_4
+1.5V
R386 0_8 CPU_VCCA
VCC_CORE
CPU_VCCA
C551 .01U/16V_4
C552 .01U/16V_4
PLACE one 10U & one 0.01U for each VCCA pin
10U/6.3V/X5R(CC0805) *30
VCC_CORE
C241 C524 C233 C231 C243 C214 C541 C240 C211
10U/6.3V_8
VCC_CORE
C532 C232 C230 C210 C245 C246 C215 C209 C212 C213
10U/6.3V_8
VCC_CORE
C536 C244 C519 C529 C533 C227 C242 C228 C229
10U/6.3V_8
U22B
Banias
2 OF 3
COMP0 P25
COMP1 P26
COMP2 AB2
COMP3 AB1
AD26 GTLREF0
E26 GTLREF1
G1 GTLREF2
AC1 GTLREF3
T119
T103
TEST1 C5
TEST2 F23
T118 AC26 VCCA3
T7 N1 VCCA2
T102 B1 VCCA1
F26 VCCA0
POWER, GROUND, RESERVED SIGNALS
VCC00 VCC01 VCC02 VCC03 VCC04 VCC05 VCC06 VCC07 VCC08 VCC09 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71
VSS
Banias_Processor
U22C
Banias
3 OF 3
POWER, GROUND AND NC
+1.05V
VCCP0 VCCP1 VCCP2 VCCP3 VCCP4 VCCP5 VCCP6 VCCP7 VCCP8 VCCP9 VCCP10 VCCP11 VCCP12 VCCP13 VCCP14 VCCP15 VCCP16 VCCP17 VCCP18 VCCP19 VCCP20 VCCP21 VCCP22 VCCP23 VCCP24 VCCP25 VCCP26
{28} CPU_VID0
{28} CPU_VID1
{28} CPU_VID2
{28} CPU_VID3
{28} CPU_VID4
{28} CPU_VID5
VID0 VID1 VID2 VID3 VID4 VID5
VID
R351 *54.9/F_4 Z0501
R349 *54.9/F_4 Z0502
AE7 VCCSENSE
AE6 VSSSENSE
T104
T108
T106
T101
{4,6} SELPSB1_CLK
{4,6} SELPSB2_CLK
B2 NC0
AE7 NC1
C14 NC2
C3 NC3
C16 TEST3
E1 PSI
VSS
Banias_Processor
+1.05V
C525 .01U/16V_4
C528 10U/6.3V_8
C534 10U/6.3V_8
C221 150U/6.3V_7343
C538 .1U/10V_4
C540 .1U/10V_4
C527 .1U/10V_4
C539 .01U/16V_4
C526 .01U/16V_4
PROJECT : ZL9
Quanta Computer Inc.
Size
Document Number
CPU (POWER)-2
Rev
3A
Date: Monday, December 19, 2005
Sheet 3 of 32

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

DOTHAN-A 400

DOTHAN-A 533

2A : change for signal quality

U26

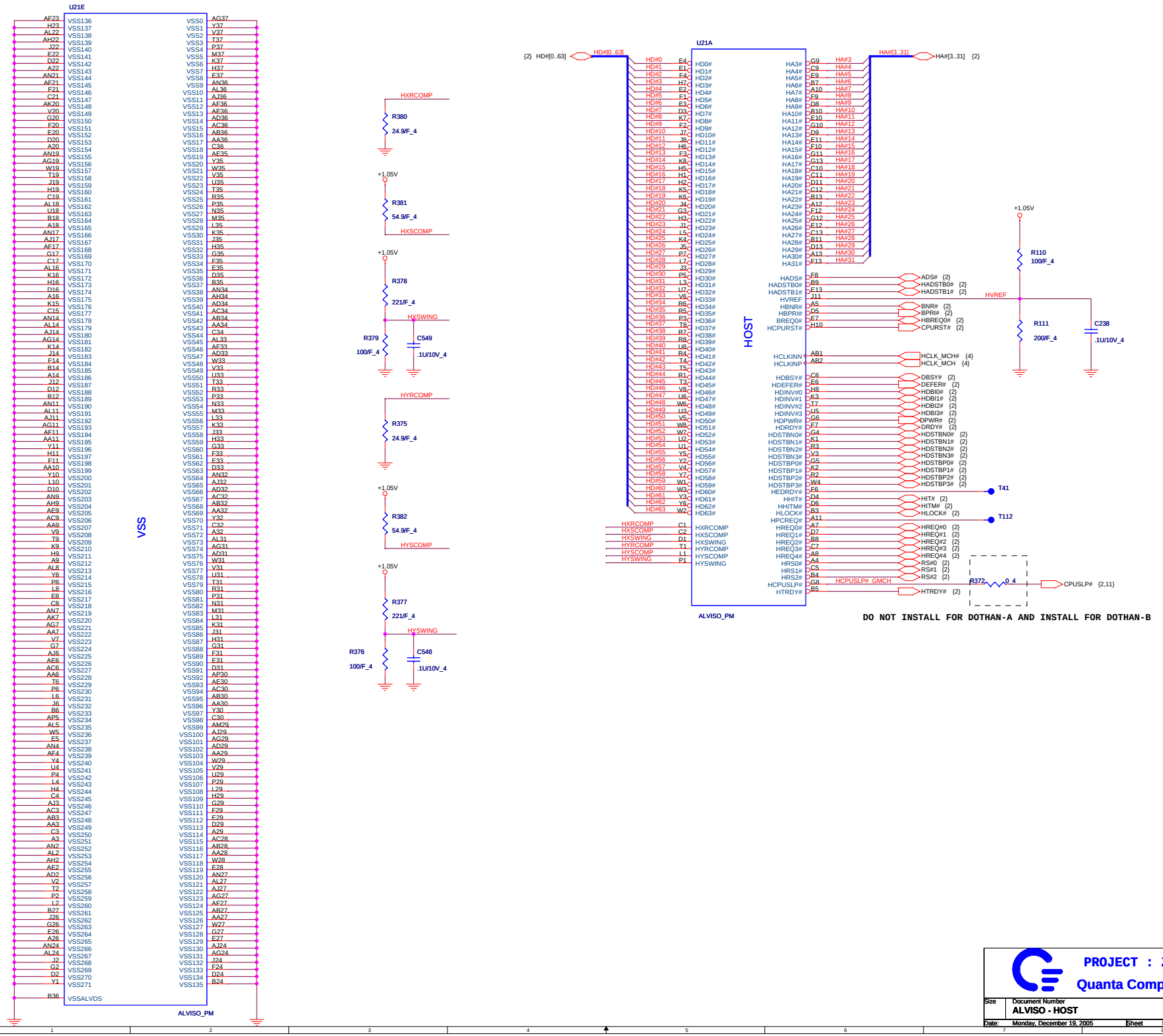
RTM865T-433-VB-LFT <TempChar>

SMbus address : D2

PROJECT : ZL9

Quanta Computer Inc.

Size	Document Number	Rev
	CLK GEN	3A
Date: Monday, December 19, 2005	Sheet 4 of 32	


U21E
VSS
ALVISO_PM
U21A
HOST
ALVISO_PM
HXRCOMP
R380
24.9/F_4
+1.05V
R381
54.9/F_4
HXSCOMP
R378
221/F_4
HYSWING
R379
100/F_4
C549
.1U/10V_4
HYRCOMP
R375
24.9/F_4
R382
54.9/F_4
HYSCOMP
R377
221/F_4
R376
100/F_4
C548
.1U/10V_4
R110
100/F_4
R111
200/F_4
C238
.1U/10V_4
HVREF
T41
T112
R372
0_4
CPUSLP# {2,11}
DO NOT INSTALL FOR DOTHAN-A AND INSTALL FOR DOTHAN-B
PROJECT : ZL9
Quanta Computer Inc.
ALVISO - HOST
Monday, December 19, 2005
Sheet 5 of 32

U21F

MISC
SDVOCTRL_DATA
SDVOCTRL_CLK
GCLKN
GCLKP

TV
TVDAC_A
TVDAC_B
TVDAC_C
TV_REFSET
TV_IRTNA
TV_IRTNB
TV_IRTNC

VGA
DDCCLK
DDCDATA
BLUE
BLUE#
GREEN
GREEN#
RED
RED#
VSYNC
HSYNC
REFSET

LVDS
LBKLT_CTRL
LBKLT_EN
LCTLA_CLK
LCTLB_DATA
LDDC_CLK
LDDC_DATA
LVDD_EN
LIBG
LVBG
LVREFH
LVREFL

LACLKN
LACLKP
LBCLKN
LBCLKP

LADATAN0
LADATAN1
LADATAN2

LADATAP0
LADATAP1
LADATAP2

LBDATAN0
LBDATAN1
LBDATAN2

LBDATAP0
LBDATAP1
LBDATAP2

PCI-EXPRESS GRAPHICS

EXP_COMPI
EXP_ICOMPO

EXP_RXN0 EXP_RXN1 EXP_RXN2 EXP_RXN3 EXP_RXN4 EXP_RXN5 EXP_RXN6 EXP_RXN7 EXP_RXN8 EXP_RXN9 EXP_RXN10 EXP_RXN11 EXP_RXN12 EXP_RXN13 EXP_RXN14 EXP_RXN15

EXP_RXP0 EXP_RXP1 EXP_RXP2 EXP_RXP3 EXP_RXP4 EXP_RXP5 EXP_RXP6 EXP_RXP7 EXP_RXP8 EXP_RXP9 EXP_RXP10 EXP_RXP11 EXP_RXP12 EXP_RXP13 EXP_RXP14 EXP_RXP15

EXP_TXN0 EXP_TXN1 EXP_TXN2 EXP_TXN3 EXP_TXN4 EXP_TXN5 EXP_TXN6 EXP_TXN7 EXP_TXN8 EXP_TXN9 EXP_TXN10 EXP_TXN11 EXP_TXN12 EXP_TXN13 EXP_TXN14 EXP_TXN15

EXP_TXP0 EXP_TXP1 EXP_TXP2 EXP_TXP3 EXP_TXP4 EXP_TXP5 EXP_TXP6 EXP_TXP7 EXP_TXP8 EXP_TXP9 EXP_TXP10 EXP_TXP11 EXP_TXP12 EXP_TXP13 EXP_TXP14 EXP_TXP15

ALVISO_PM

VCC3G_PCIE
R76 24.9/F_4

GMCHEXP_RXN[0..15] {14}
GMCHEXP_RXP[0..15] {14}
GMCHEXP_TXN[0..15] {14}
GMCHEXP_TXP[0..15] {14}

For UMA

2A for sparete UMA and VGA display-on

0.1u Capacitors place at first 1/3 of trace

U21C

DMI
DMIRXN0 DMIRXN1 DMIRXN2 DMIRXN3
DMIRXP0 DMIRXP1 DMIRXP2 DMIRXP3
DMITXN0 DMITXN1 DMITXN2 DMITXN3
DMITXP0 DMITXP1 DMITXP2 DMITXP3

CFG/RSVD
CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17 CFG18 CFG19 CFG20
RSVD21 RSVD22 RSVD23 RSVD24 RSVD25 RSVD26 RSVD27

DDR MUXING
SM_CK0 SM_CK1 SM_CK2 SM_CK3 SM_CK4 SM_CK5
SM_CKE0 SM_CKE1 SM_CKE2 SM_CKE3
SM_CS0# SM_CS1# SM_CS2# SM_CS3#
SM_OCDCOMP0 SM_OCDCOMP1
SM_ODT0 SM_ODT1 SM_ODT2 SM_ODT3
SMRCOMPN SMRCOMPP SMVREF0 SMVREF1 SMXSLEWIN SMXSLEWOUT SMYSLEWIN SMYSLEWOUT

PM
BM_BUSY# EXT_TS0# EXT_TS1# THRMTRIP# PWROK RSTIN#

LCK
DREF_CLKN DREF_CLKP DREF_SSCLKN DREF_SSCLKP

NC
NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11

CFG[0:2]=100 FOR FSB 533
CFG[0:2]=101 FOR FSB 400

CFG5 Low=DMIx2
High=DMIx4
CFG6 Low=DDR2
High=DDR

CFG9 Low=REVERSE LANE
High=NORMAL

CFG11 FOR CPU533

CFG[17:3] have internal pullup resistors.
CFG[19:18] have internal pulldown resistors

For DDR2
It's point to point, 55ohm trace, keep as short as possible.

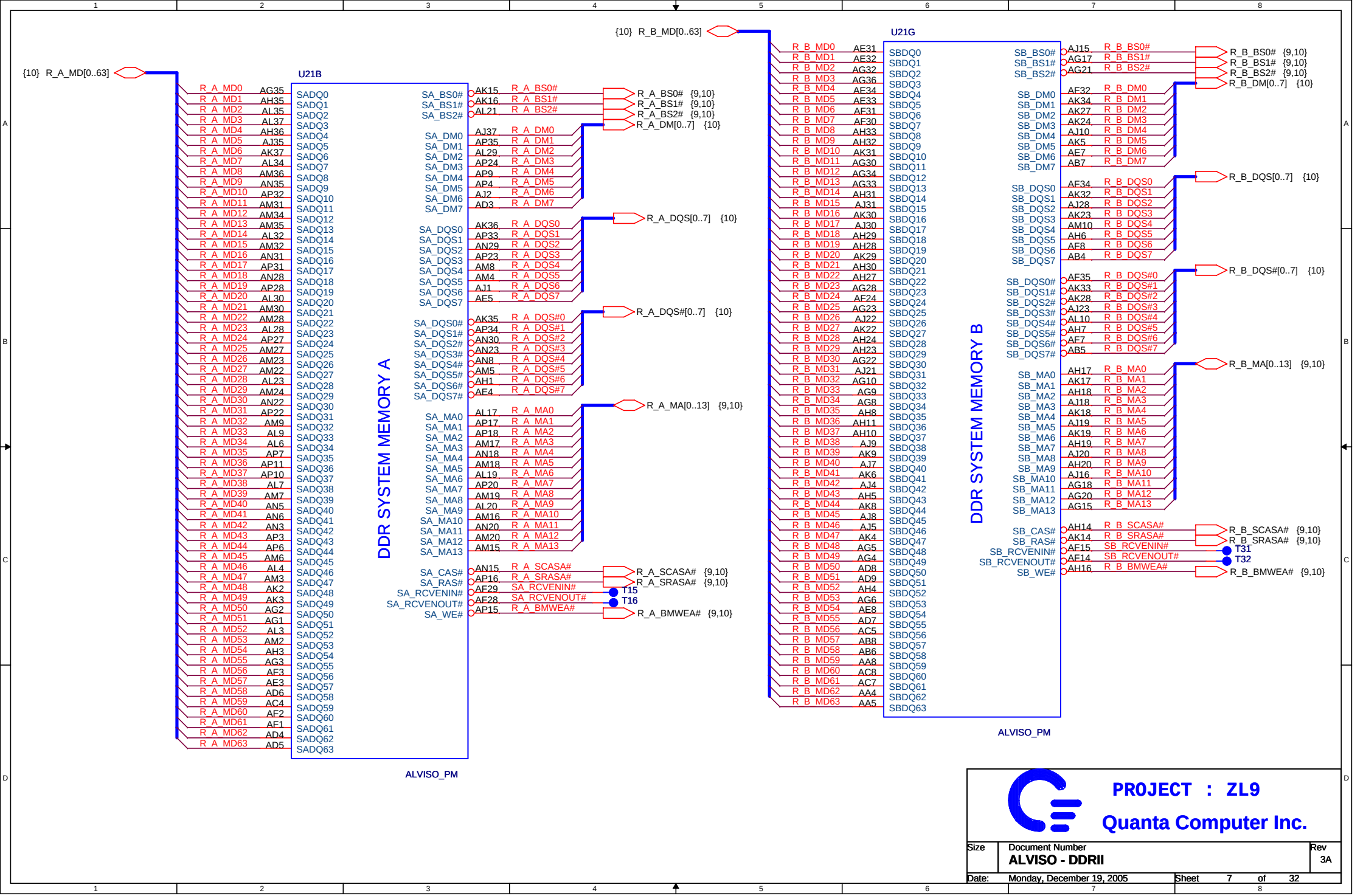
ALVISO_PM

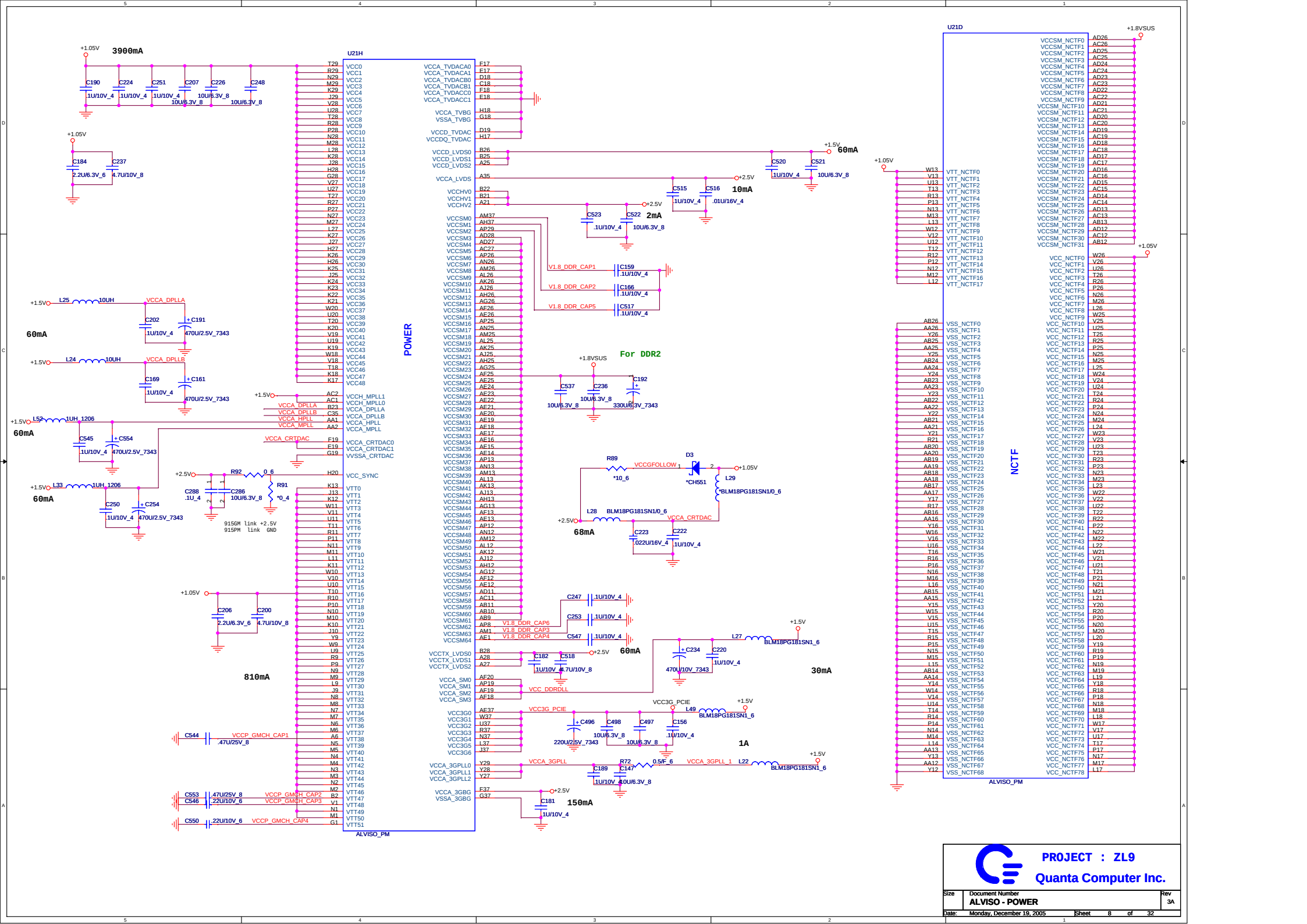
RP3 TXLCLKOUT+_NB TXLCLKOUT-_NB *4P2R-0404_2@UMA
RP7 TXLOUT0-_NB TXLOUT0+_NB *4P2R-0404_2@UMA
RP9 TXLOUT1+_NB TXLOUT1-_NB *4P2R-0404_2@UMA
RP5 TXLOUT2+_NB TXLOUT2-_NB *4P2R-0404_2@UMA

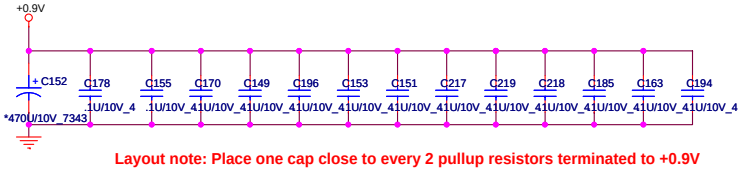
PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	ALVISO - DMI / VGA	3A

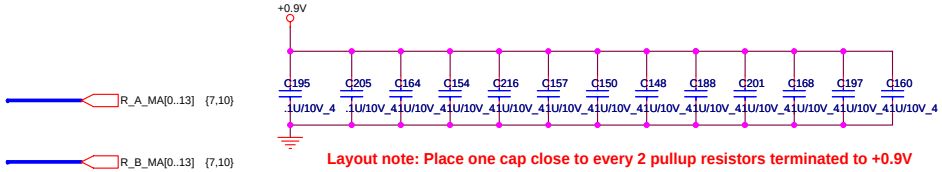
Date: Monday, December 19, 2005 Sheet 6 of 32


{10} R_A_MD[0..63]
U21B
DDR SYSTEM MEMORY A
ALVISO_PM
{10} R_B_MD[0..63]
U21G
DDR SYSTEM MEMORY B
ALVISO_PM
R_A_BS0# {9,10}
R_A_BS1# {9,10}
R_A_BS2# {9,10}
R_A_DM[0..7] {10}
R_A_DQS[0..7] {10}
R_A_DQS#[0..7] {10}
R_A_MA[0..13] {9,10}
R_A_SCASA# {9,10}
R_A_SRASA# {9,10}
R_A_BMWEA# {9,10}
R_B_BS0# {9,10}
R_B_BS1# {9,10}
R_B_BS2# {9,10}
R_B_DM[0..7] {10}
R_B_DQS[0..7] {10}
R_B_DQS#[0..7] {10}
R_B_MA[0..13] {9,10}
R_B_SCASA# {9,10}
R_B_SRASA# {9,10}
R_B_BMWEA# {9,10}
T15
T16
T31
T32
PROJECT : ZL9
Quanta Computer Inc.
Size
Document Number
ALVISO - DDRII
Rev
3A
Date: Monday, December 19, 2005
Sheet 7 of 32

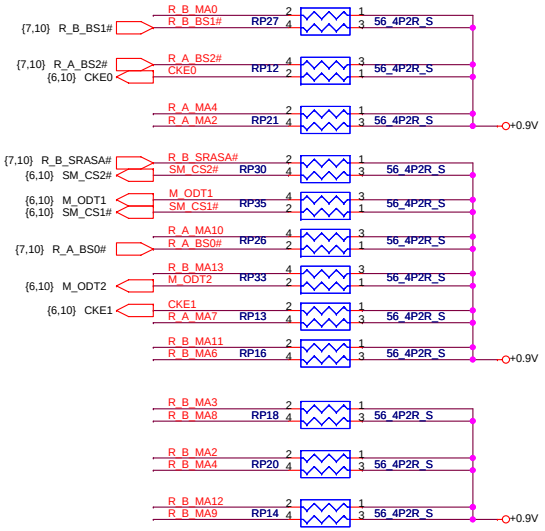

U21H
POWER
ALVISO_PM
U21D
NCTF
ALVISO_PM
For DDR2
3900mA
810mA
60mA
10mA
2mA
1A
150mA
68mA
30mA
PROJECT : ZL9
Quanta Computer Inc.
ALVISO - POWER
Monday, December 19, 2005

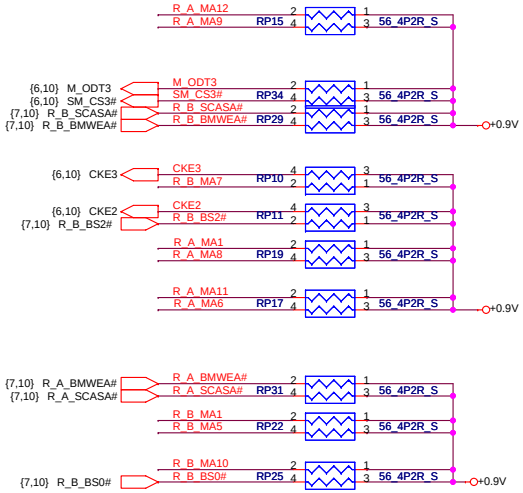


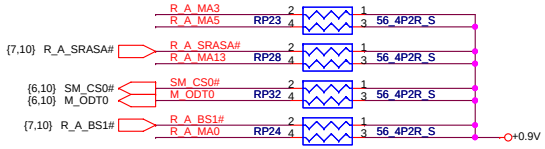
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V



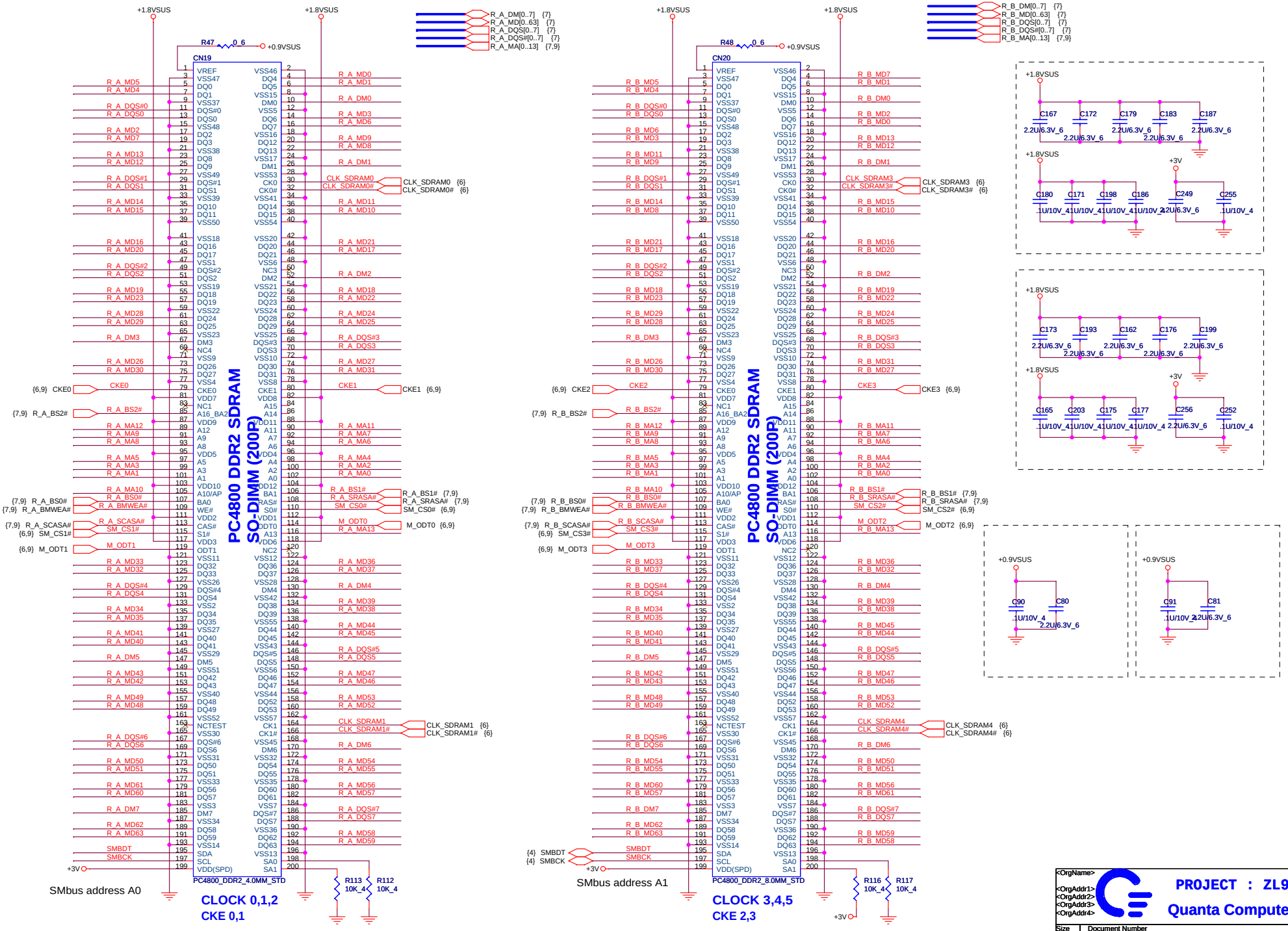




PROJECT : ZL9

Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 TERMINATION	3A
Date: Monday, December 19, 2005	Sheet 9 of 32	



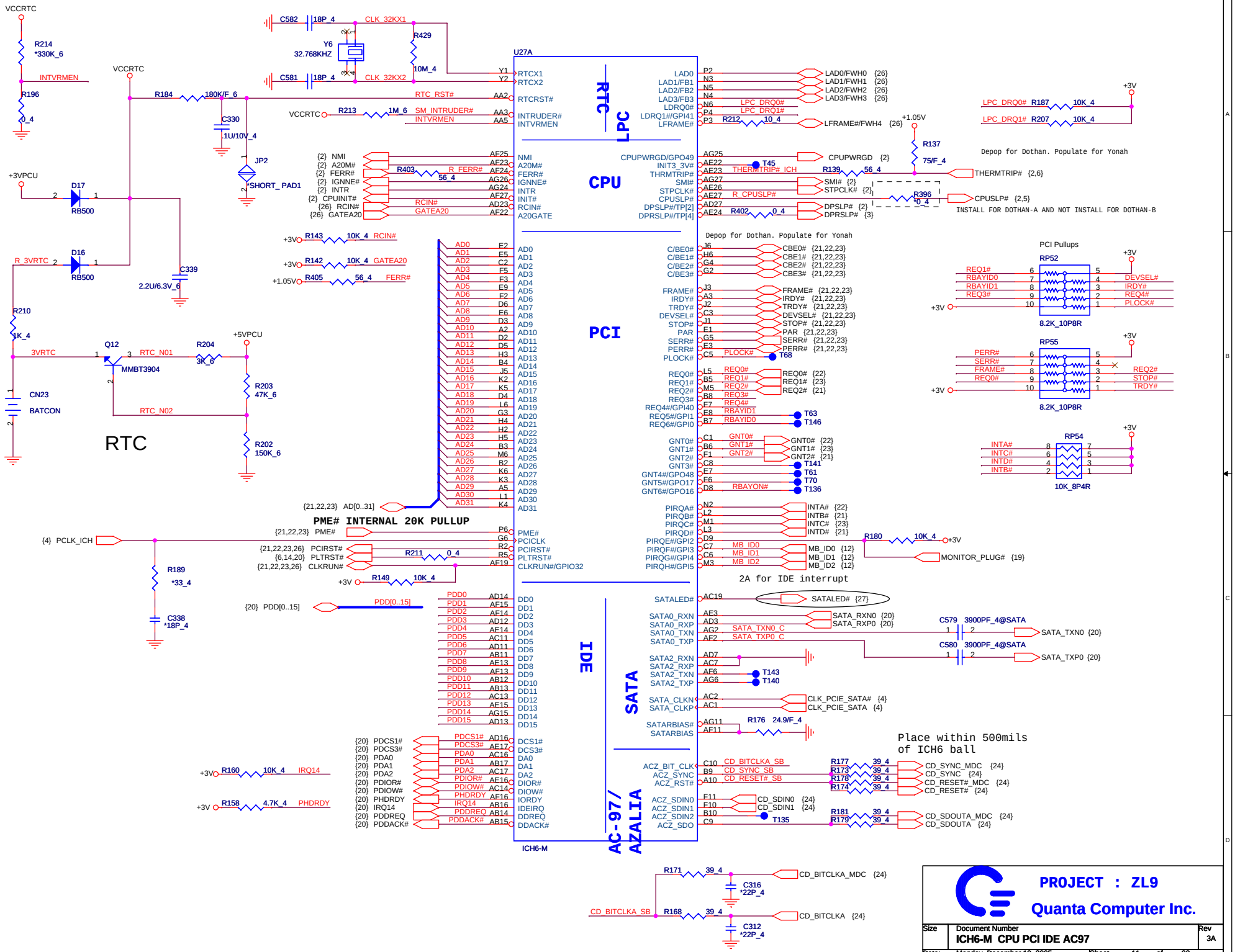
<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>

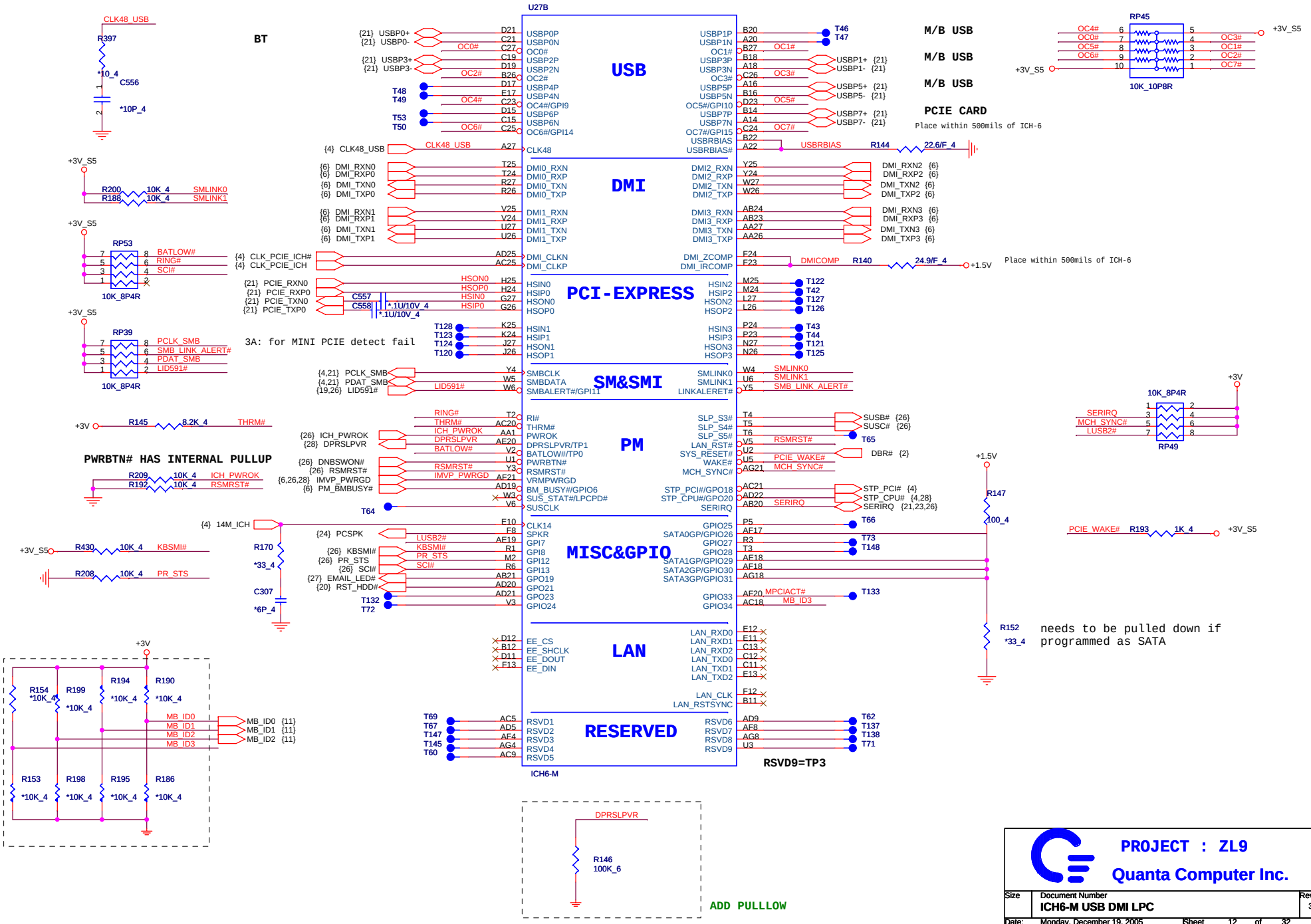
PROJECT : ZL9

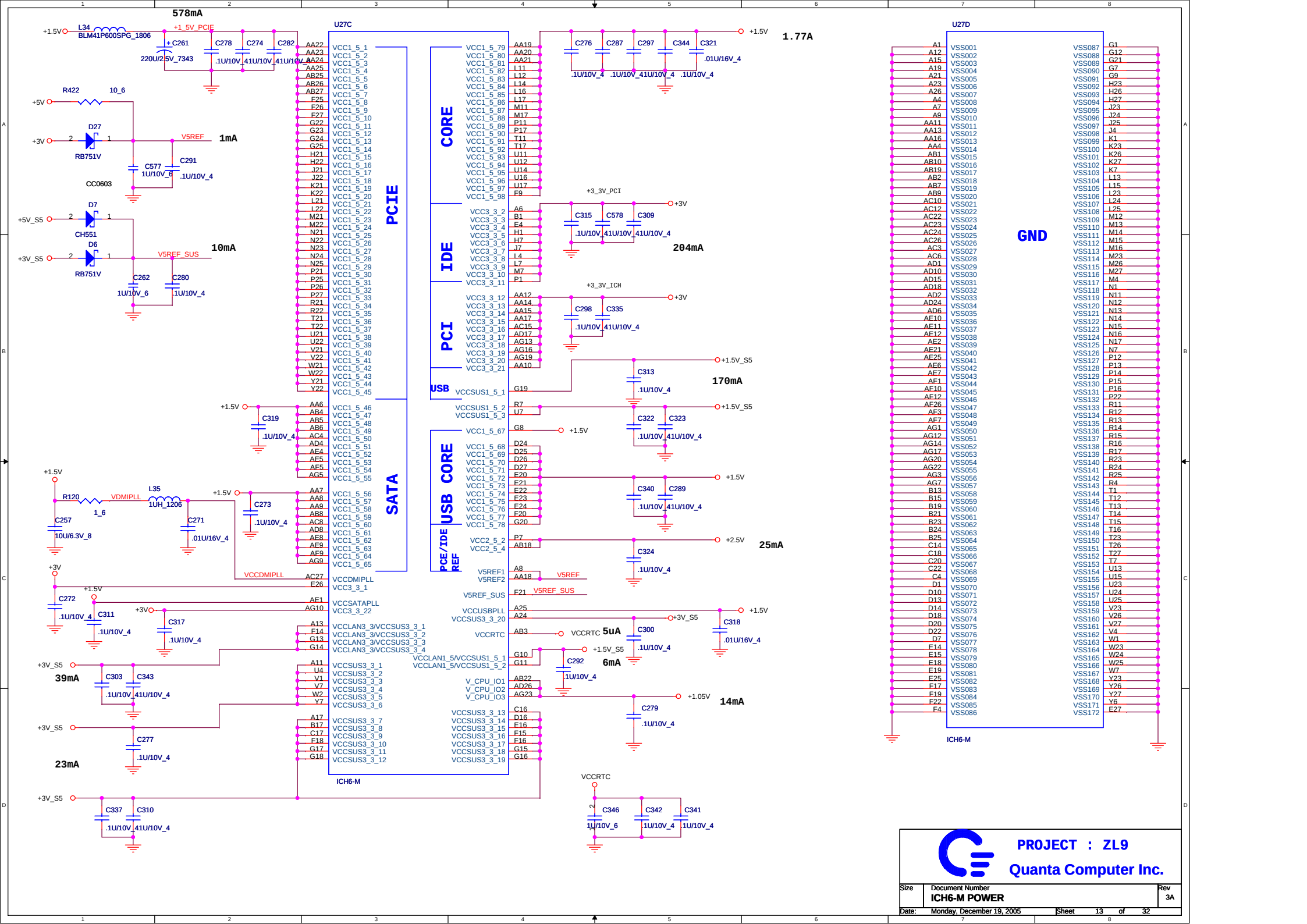
Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 SO-DIMM (200P)	3A

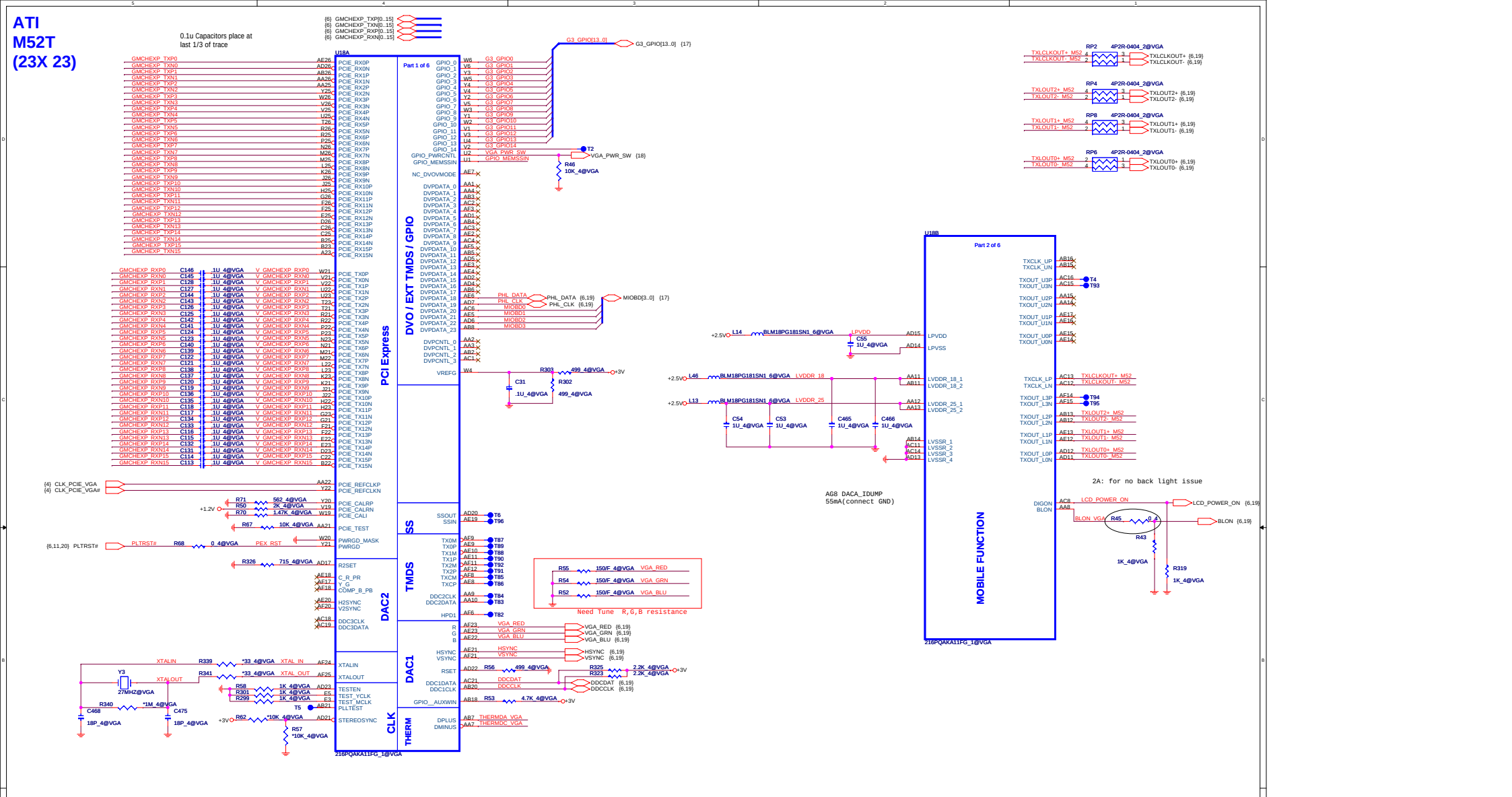
Date: Monday, December 19, 2005 Sheet 10 of 32


RTC
CPU
PCI
IDE
SATA
LPC
AC-97/ AZALIA
ICH6-M
U27A
PME# INTERNAL 20K PULLUP
2A for IDE interrupt
Place within 500mils of ICH6 ball
Depop for Dothan. Populate for Yonah
INSTALL FOR DOTHAN-A AND NOT INSTALL FOR DOTHAN-B
PCI Pullups
8.2K_10P8R
10K_8P4R
PROJECT : ZL9
Quanta Computer Inc.
Document Number
ICH6-M CPU PCI IDE AC97
Rev 3A
Date: Monday, December 19, 2005
Sheet 11 of 32

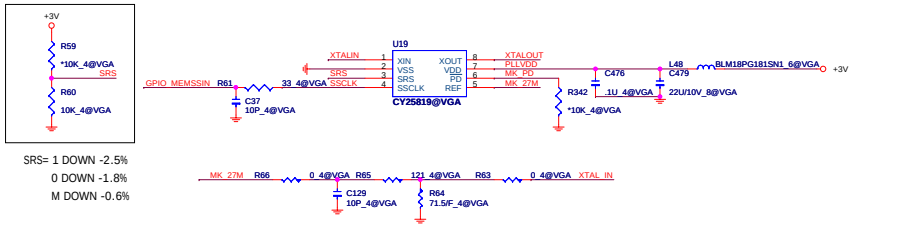

U27B
USB
DMI
PCI-EXPRESS
SM&SMI
PM
MISC&GPIO
LAN
RESERVED
ICH6-M
BT
M/B USB
M/B USB
M/B USB
PCIE CARD
Place within 500mils of ICH-6
Place within 500mils of ICH-6
3A: for MINI PCIE detect fail
PWRBTN# HAS INTERNAL PULLUP
needs to be pulled down if programmed as SATA
RSVD9=TP3
ADD PULLLOW
PROJECT : ZL9
Quanta Computer Inc.
ICH6-M USB DMI LPC
Monday, December 19, 2005


578mA
U27C
ICH6-M
CORE
PCIE
IDE
PCI
USB
USB CORE
SATA
PCE/IDE REF
1.77A
204mA
170mA
25mA
5uA
6mA
14mA
1mA
10mA
39mA
23mA
U27D
GND
ICH6-M
PROJECT : ZL9
Quanta Computer Inc.
ICH6-M POWER
Monday, December 19, 2005

ATI M52T (23X 23)



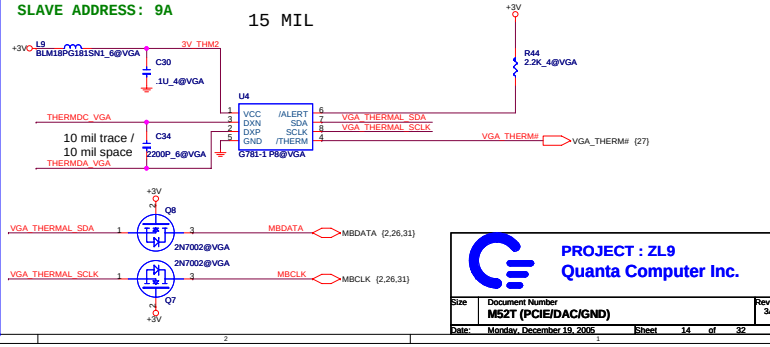
MEMORY CLOCK SPREAD SPECTRUM



Thermal Sensor for Graphic

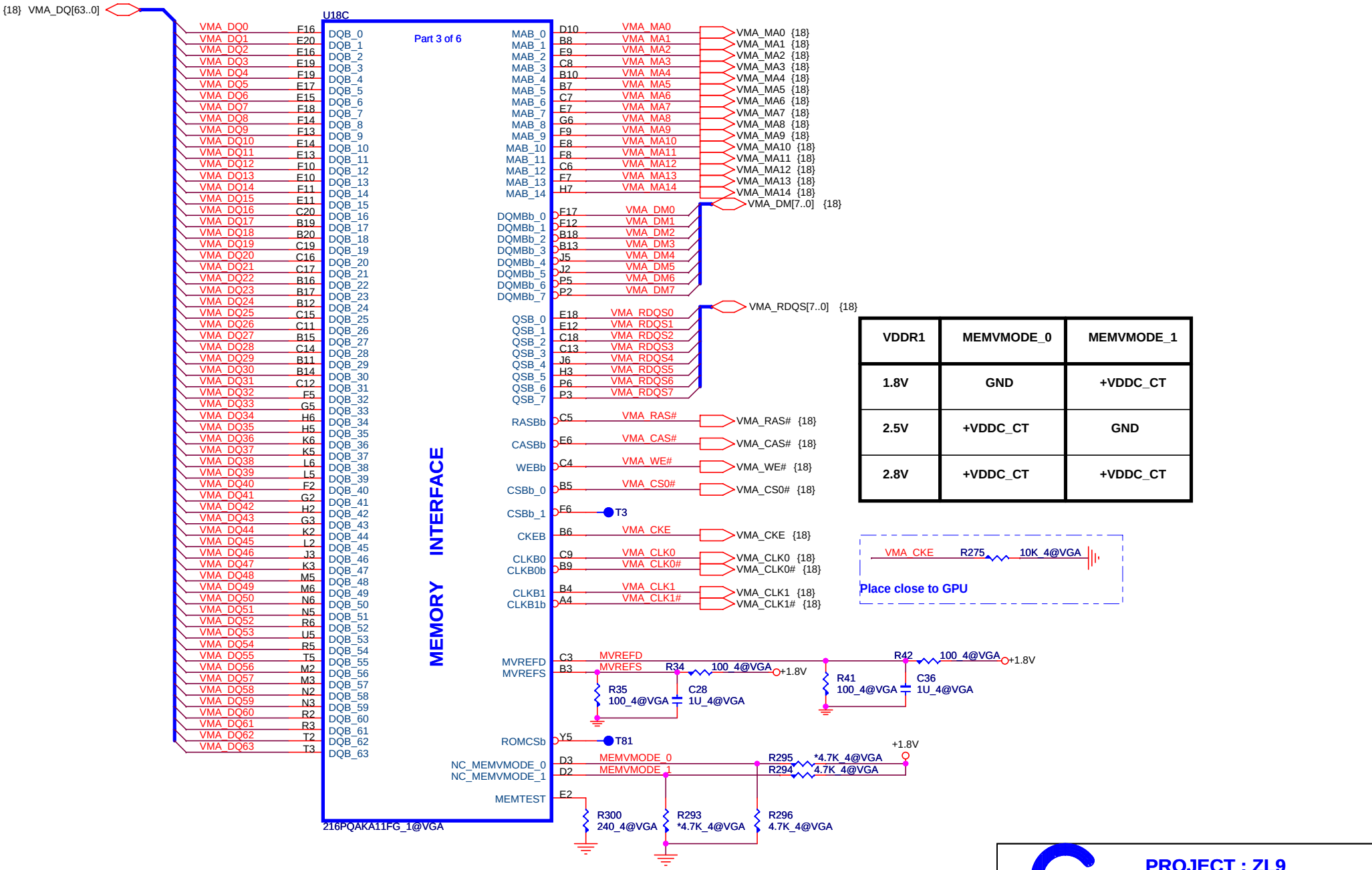
SLAVE ADDRESS: 9A

15 MIL



PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	M52T (PCIE/DAC/GND)	3A
Date: Monday, December 19, 2005	Sheet 14 of 32	



VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	M52T (MEMORY A/B)	3A
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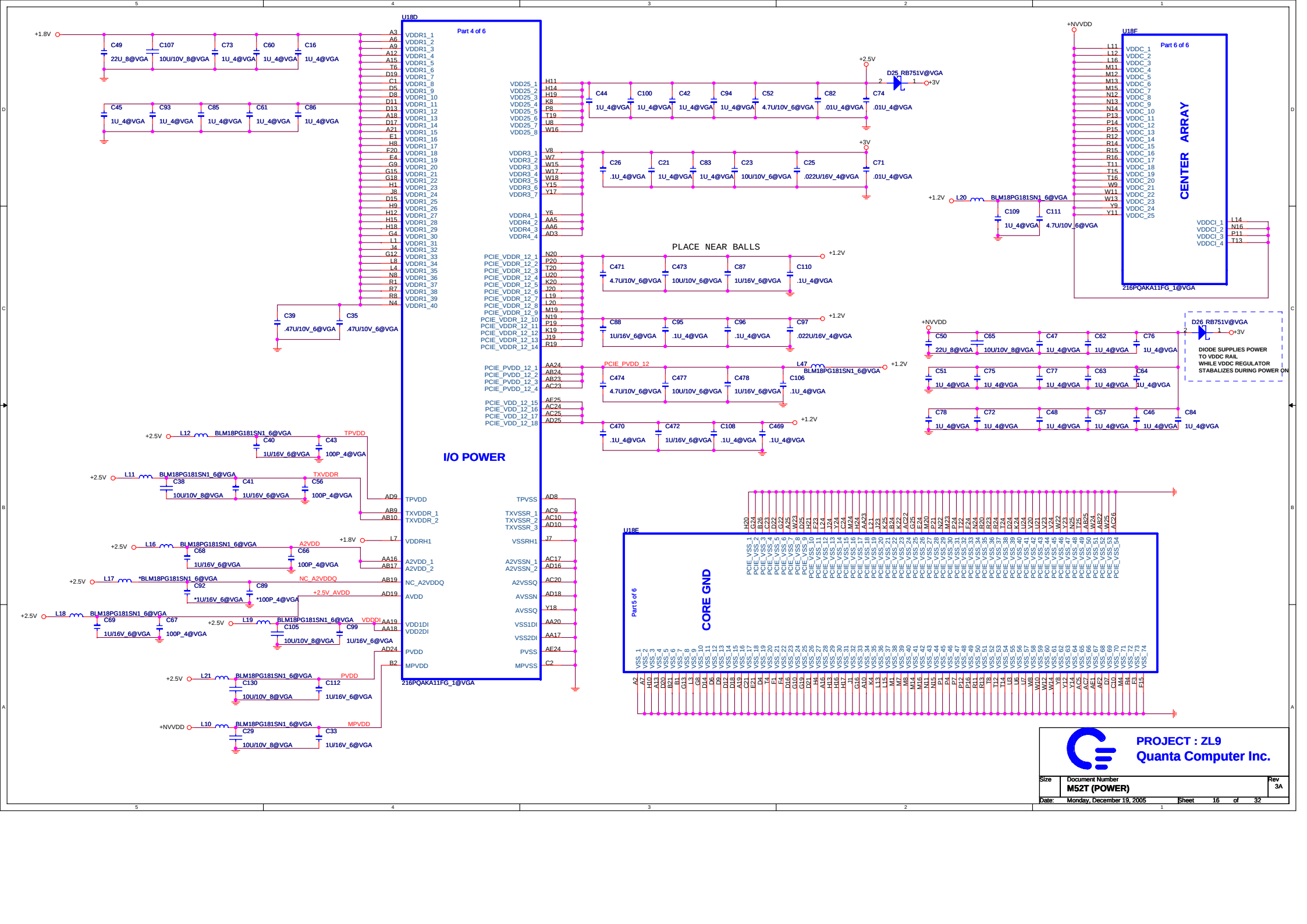
U18D
Part 4 of 6
I/O POWER
216PQAKA11FG_1@VGA
U18F
Part 6 of 6
CENTER ARRAY
216PQAKA11FG_1@VGA
U18E
Part 5 of 6
CORE GND
PLACE NEAR BALLS
DIODE SUPPLIES POWER TO VDDC RAIL WHILE VDDC REGULATOR STABALIZES DURING POWER ON
PROJECT : ZL9
Quanta Computer Inc.
Size
Document Number
M52T (POWER)
Rev 3A
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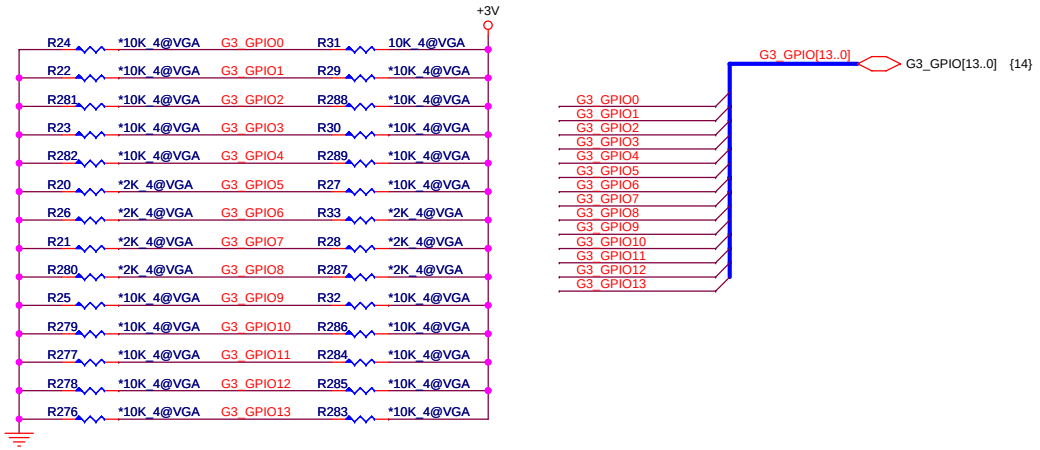
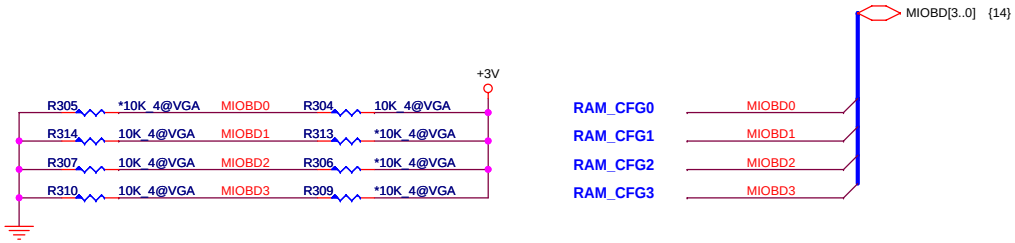


STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	G3_GPIO0	FULL SWING	1
TX_DEEMPH_EN	G3_GPIO1	TRANSMITTER DE-EMPHASIS ENABLE - TX DE-EMPHASIS DISABLED FOR MOBILE	0
DEBUG_ACCESS	G3_GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0
FORCE COMPLIANCE	G3_GPIO8	**Force chip to get to compliance state queckly for tester pruposes**	0
ROMIDCFG(3:0)	G3_GPIO(9,13,12,11)	**128M** **256M** **64M** **Recerved**	**0000** **0010** **0100** **0110**



M52T VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION
0000	DDR2 , 16Mx16 , 2pcs (64M)
0001	DDR2 , 16Mx16 , 4pcs (128M)
0010	DDR2 ,32Mx16 , 2pcs (128M)
0011	DDR2 ,32Mx16 , 4pcs (256M)
others	Reserved

MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select **00 - single function device.** 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function.	00
VIP_DEVICE	LCDDATA(20)	Indicates if any slave VIP host devices drove this low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	0
DWNGRD	LCDDATA(21)	0 - Device remain a workstation grade part. 1 - Part is downgraded to a Normal part	0 (internal pull-down)

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Quanta Computer Inc.

Size	Document Number	Rev
	M52T (STRAP/MISC)	3A

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{15} VMA_DQ[63..0]
{15} VMA_DM[7..0]
{15} VMA_RDQS[7..0]

256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01

U17

VMA_DQ5 B9 UDQ7
VMA_DQ1 B1 UDQ6
VMA_DQ2 D9 UDQ5
VMA_DQ4 D1 UDQ4
VMA_DQ7 D3 UDQ3
VMA_DQ6 D7 UDQ2
VMA_DQ3 C2 UDQ1
VMA_DQ0 C8 UDQ0
VMA_DQ9 E9 LDQ7
VMA_DQ8 F1 LDQ6
VMA_DQ12 H9 LDQ5
VMA_DQ10 H1 LDQ4
VMA_DQ14 H3 LDQ3
VMA_DQ13 H7 LDQ2
VMA_DQ15 G2 LDQ1
VMA_DQ11 G8 LDQ0

VMA_DM0 B3 UDM
VMA_DM1 F3 LDM

VMA_RDQS0 B7 UDQS
VMA_WDQS0 A8 UDQS
VMA_RDQS1 F7 LDQS
VMA_WDQS1 E8 LDQS

{15} VMA_CLK0 → VMA_CLK0 J8 CK
{15} VMA_CLK0# → VMA_CLK0# K8 CK

{15} VMA_MA13 → VMA_MA13 L3 BA1
{15} VMA_MA12 → VMA_MA12 L2 BA0

{15} VMA_MA14 → VMA_MA14 R2 A12
{15} VMA_MA11 → VMA_MA11 P7 A11
{15} VMA_MA10 → VMA_MA10 M2 A10
{15} VMA_MA9 → VMA_MA9 P3 A9
{15} VMA_MA8 → VMA_MA8 P8 A8
{15} VMA_MA7 → VMA_MA7 P2 A7
{15} VMA_MA6 → VMA_MA6 N7 A6
{15} VMA_MA5 → VMA_MA5 N3 A5
{15} VMA_MA4 → VMA_MA4 N8 A4
{15} VMA_MA3 → VMA_MA3 N2 A3
{15} VMA_MA2 → VMA_MA2 M7 A2
{15} VMA_MA1 → VMA_MA1 M3 A1
{15} VMA_MA0 → VMA_MA0 M8 A0

VMA_ODT K9 ODT
{15} VMA_CKE → VMA_CKE K2 CKE
{15} VMA_CS0# → VMA_CS0# L8 CS
{15} VMA_WE# → VMA_WE# K3 WE
{15} VMA_RAS# → VMA_RAS# K7 RAS
{15} VMA_CAS# → VMA_CAS# L7 CAS

VREF J2 ← VMREFA0
R311 499/F_4@VGA +1.8V
R308 499/F_4@VGA
C451 .1U_4@VGA
15mil

VDD1 A1, E1
VDD2 J9
VDD3 M9
VDD4 R1
VDD5 +1.8V

VDDQ1 A9, C1
VDDQ2 C3
VDDQ3 C7
VDDQ4 C9
VDDQ5 E9
VDDQ6 G1
VDDQ7 G3
VDDQ8 G7
VDDQ9 G9
VDDQ10

L45 0_6@VGA
VDDL J1 → VDDL1
15mil
C458 .1U_4@VGA
C457 1U_6@VGA

NC1 A2
NC2 E2
NC3 L1
NC4 R3
NC5 R7
NC6 R8

VSS1 A3
VSS2 E3
VSS3 J3
VSS4 N1
VSS5 P9

VSSQ1 A7
VSSQ2 B2
VSSQ3 B8
VSSQ4 D2
VSSQ5 D8
VSSQ6 E7
VSSQ7 F2
VSSQ8 H2
VSSQ9 H8
VSSQ10

VSSDL J7

GDDR2-BGA84@VGA

VREF_A0
R334 10/F_4@VGA VMA_WDQS0
R333 10/F_4@VGA VMA_WDQS1
R332 10/F_4@VGA VMA_WDQS2
R331 10/F_4@VGA VMA_WDQS3
+1.8V
R335 499/F_4@VGA
R336 499/F_4@VGA
C467 .1U_4@VGA

U5

VMA_DQ16 B9 UDQ7
VMA_DQ21 B1 UDQ6
VMA_DQ19 D9 UDQ5
VMA_DQ23 D1 UDQ4
VMA_DQ20 D3 UDQ3
VMA_DQ17 D7 UDQ2
VMA_DQ22 C2 UDQ1
VMA_DQ18 C8 UDQ0
VMA_DQ25 E9 LDQ7
VMA_DQ30 F1 LDQ6
VMA_DQ28 H9 LDQ5
VMA_DQ26 H1 LDQ4
VMA_DQ31 H3 LDQ3
VMA_DQ24 H7 LDQ2
VMA_DQ29 G2 LDQ1
VMA_DQ27 G8 LDQ0

VMA_DM2 B3 UDM
VMA_DM3 F3 LDM

VMA_RDQS2 B7 UDQS
VMA_WDQS2 A8 UDQS
VMA_RDQS3 F7 LDQS
VMA_WDQS3 E8 LDQS

VMA_CLK0 J8 CK
VMA_CLK0# K8 CK

VMA_MA13 L3 BA1
VMA_MA12 L2 BA0

VMA_MA14 R2 A12
VMA_MA11 P7 A11
VMA_MA10 M2 A10
VMA_MA9 P3 A9
VMA_MA8 P8 A8
VMA_MA7 P2 A7
VMA_MA6 N7 A6
VMA_MA5 N3 A5
VMA_MA4 N8 A4
VMA_MA3 N2 A3
VMA_MA2 M7 A2
VMA_MA1 M3 A1
VMA_MA0 M8 A0

VMA_ODT K9 ODT
VMA_CKE K2 CKE
VMA_CS0# L8 CS
VMA_WE# K3 WE
VMA_RAS# K7 RAS
VMA_CAS# L7 CAS

VREF J2 ← VMREFA1
R49 499/F_4@VGA +1.8V
R51 499/F_4@VGA
C98 .1U_4@VGA

VDD1 A1, E1
VDD2 J9
VDD3 M9
VDD4 R1
VDD5 +1.8V

VDDQ1 A9, C1
VDDQ2 C3
VDDQ3 C7
VDDQ4 C9
VDDQ5 E9
VDDQ6 G1
VDDQ7 G3
VDDQ8 G7
VDDQ9 G9
VDDQ10

L15 0_6@VGA
VDDL J1 → VDDL2
15mil
C79 .1U_4@VGA
C70 1U_6@VGA

NC1 A2
NC2 E2
NC3 L1
NC4 R3
NC5 R7
NC6 R8

VSS1 A3
VSS2 E3
VSS3 J3
VSS4 N1
VSS5 P9

VSSQ1 A7
VSSQ2 B2
VSSQ3 B8
VSSQ4 D2
VSSQ5 D8
VSSQ6 E7
VSSQ7 F2
VSSQ8 F8
VSSQ9 H2
VSSQ10 H8

VSSDL J7

GDDR2-BGA84@VGA

VMA_CLK0 → R316 56/F_4@VGA
VMA_CLK0# → R318 56/F_4@VGA
C454 .01U_4@VGA

C464 1000P_4@VGA
C442 .01U_4@VGA
C459 .1U_4@VGA
C104 10U/10V_6@VGA
+1.8V

C27 1000P_4@VGA
C102 .01U_4@VGA
C101 .1U_4@VGA
C103 10U/10V_6@VGA
+1.8V

C17 1000P_4@VGA
C19 .01U_4@VGA
C20 .1U_4@VGA
C15 10U/10V_6@VGA
+1.8V

C446 1000P_4@VGA
C444 .01U_4@VGA
C445 .1U_4@VGA
C443 10U/10V_6@VGA
+1.8V

U2

VMA_DQ38 B9 UDQ7
VMA_DQ37 B1 UDQ6
VMA_DQ35 D9 UDQ5
VMA_DQ33 D1 UDQ4
VMA_DQ32 D3 UDQ3
VMA_DQ34 D7 UDQ2
VMA_DQ39 C2 UDQ1
VMA_DQ36 C8 UDQ0
VMA_DQ46 E9 LDQ7
VMA_DQ45 F1 LDQ6
VMA_DQ42 H9 LDQ5
VMA_DQ40 H1 LDQ4
VMA_DQ41 H3 LDQ3
VMA_DQ43 H7 LDQ2
VMA_DQ47 G2 LDQ1
VMA_DQ44 G8 LDQ0

VMA_DM4 B3 UDM
VMA_DM5 F3 LDM

VMA_RDQS4 B7 UDQS
VMA_WDQS5 A8 UDQS
VMA_RDQS5 F7 LDQS
VMA_WDQS4 E8 LDQS

{15} VMA_CLK1 → VMA_CLK1 J8 CK
{15} VMA_CLK1# → VMA_CLK1# K8 CK

VMA_MA13 L3 BA1
VMA_MA12 L2 BA0

VMA_MA14 R2 A12
VMA_MA11 P7 A11
VMA_MA10 M2 A10
VMA_MA9 P3 A9
VMA_MA8 P8 A8
VMA_MA7 P2 A7
VMA_MA6 N7 A6
VMA_MA5 N3 A5
VMA_MA4 N8 A4
VMA_MA3 N2 A3
VMA_MA2 M7 A2
VMA_MA1 M3 A1
VMA_MA0 M8 A0

VMA_ODT K9 ODT
VMA_CKE K2 CKE
VMA_CS0# L8 CS
VMA_WE# K3 WE
VMA_RAS# K7 RAS
VMA_CAS# L7 CAS

VREF J2 ← VMREFA2
R12 499/F_4@VGA +1.8V
R13 499/F_4@VGA
C13 .1U_4@VGA
15mil

VDD1 A1, E1
VDD2 J9
VDD3 M9
VDD4 R1
VDD5 +1.8V

VDDQ1 A9, C1
VDDQ2 C3
VDDQ3 C7
VDDQ4 C9
VDDQ5 E9
VDDQ6 G1
VDDQ7 G3
VDDQ8 G7
VDDQ9 G9
VDDQ10

L7 0_6@VGA
VDDL J1 → VDDL3
15mil
C14 .1U_4@VGA
C12 1U_6@VGA

NC1 A2
NC2 E2
NC3 L1
NC4 R3
NC5 R7
NC6 R8

VSS1 A3
VSS2 E3
VSS3 J3
VSS4 N1
VSS5 P9

VSSQ1 A7
VSSQ2 B2
VSSQ3 B8
VSSQ4 D2
VSSQ5 D8
VSSQ6 E7
VSSQ7 F2
VSSQ8 H2
VSSQ9 H8
VSSQ10

VSSDL J7

GDDR2-BGA84@VGA

VREF_A1
R19 10/F_4@VGA VMA_WDQS5
R17 10/F_4@VGA VMA_WDQS4
R16 10/F_4@VGA VMA_WDQS7
R14 10/F_4@VGA VMA_WDQS6
+1.8V
R15 499/F_4@VGA
R18 499/F_4@VGA
C18 .1U_4@VGA

U16

VMA_DQ58 B9 UDQ7
VMA_DQ63 B1 UDQ6
VMA_DQ56 D9 UDQ5
VMA_DQ60 D1 UDQ4
VMA_DQ61 D3 UDQ3
VMA_DQ57 D7 UDQ2
VMA_DQ62 C2 UDQ1
VMA_DQ59 C8 UDQ0
VMA_DQ53 E9 LDQ7
VMA_DQ54 F1 LDQ6
VMA_DQ51 H9 LDQ5
VMA_DQ52 H1 LDQ4
VMA_DQ55 H3 LDQ3
VMA_DQ49 H7 LDQ2
VMA_DQ48 G2 LDQ1
VMA_DQ50 G8 LDQ0

VMA_DM7 B3 UDM
VMA_DM6 F3 LDM

VMA_RDQS7 B7 UDQS
VMA_WDQS7 A8 UDQS
VMA_RDQS6 F7 LDQS
VMA_WDQS6 E8 LDQS

VMA_CLK1 J8 CK
VMA_CLK1# K8 CK

VMA_MA13 L3 BA1
VMA_MA12 L2 BA0

VMA_MA14 R2 A12
VMA_MA11 P7 A11
VMA_MA10 M2 A10
VMA_MA9 P3 A9
VMA_MA8 P8 A8
VMA_MA7 P2 A7
VMA_MA6 N7 A6
VMA_MA5 N3 A5
VMA_MA4 N8 A4
VMA_MA3 N2 A3
VMA_MA2 M7 A2
VMA_MA1 M3 A1
VMA_MA0 M8 A0

VMA_ODT K9 ODT
VMA_CKE K2 CKE
VMA_CS0# L8 CS
VMA_WE# K3 WE
VMA_RAS# K7 RAS
VMA_CAS# L7 CAS

VREF J2 ← VMREFA3
R298 499/F_4@VGA +1.8V
R297 499/F_4@VGA
C448 .1U_4@VGA

VDD1 A1, E1
VDD2 J9
VDD3 M9
VDD4 R1
VDD5 +1.8V

VDDQ1 A9, C1
VDDQ2 C3
VDDQ3 C7
VDDQ4 C9
VDDQ5 E9
VDDQ6 G1
VDDQ7 G3
VDDQ8 G7
VDDQ9 G9
VDDQ10

L8 0_6@VGA
VDDL J1 → VDDL4
15mil
C22 .1U_4@VGA
C24 1U_6@VGA

NC1 A2
NC2 E2
NC3 L1
NC4 R3
NC5 R7
NC6 R8

VSS1 A3
VSS2 E3
VSS3 J3
VSS4 N1
VSS5 P9

VSSQ1 A7
VSSQ2 B2
VSSQ3 B8
VSSQ4 D2
VSSQ5 D8
VSSQ6 E7
VSSQ7 F2
VSSQ8 F8
VSSQ9 H2
VSSQ10 H8

VSSDL J7

GDDR2-BGA84@VGA

VMA_CLK1 → R292 56/F_4@VGA
VMA_CLK1# → R291 56/F_4@VGA
C447 .01U_4@VGA

+1.8V
R37 10K_4@VGA
VMA_ODT
R36 *0_4@VGA
Q6 2N7002@VGA
{14} VGA_PWR_SW → 2

PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	VRAM (GDDR2)	3A
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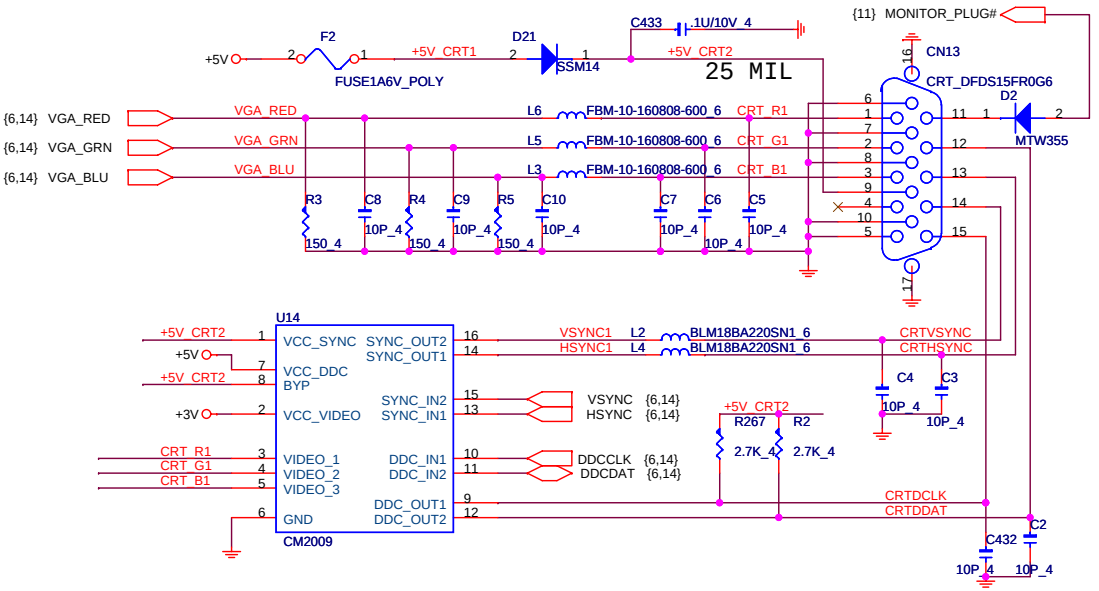
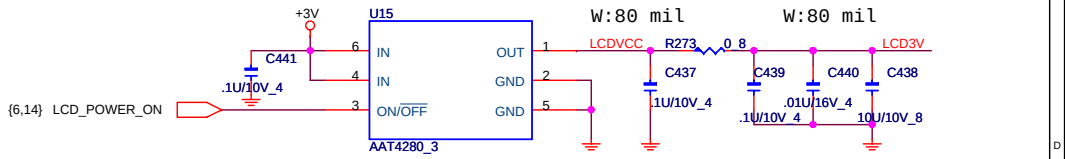
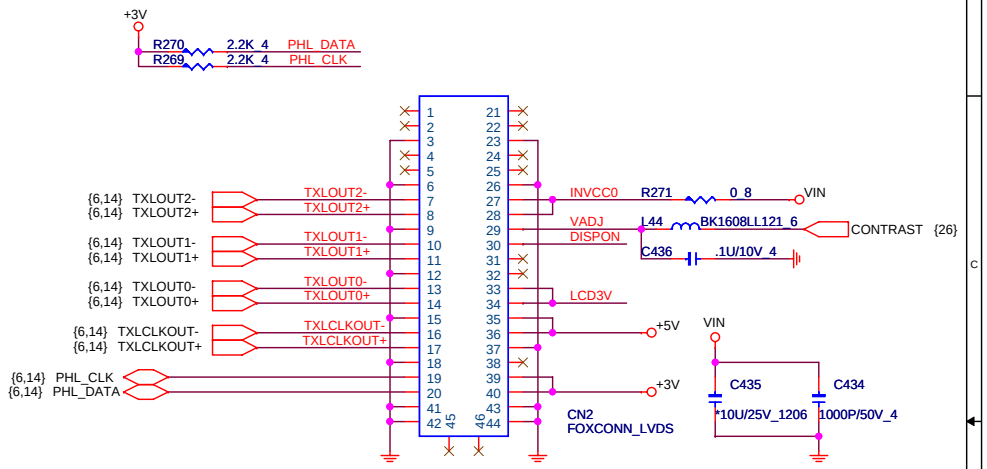
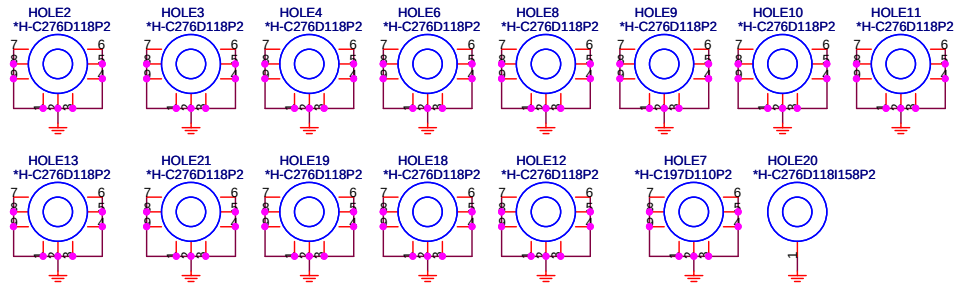
CRT PORT

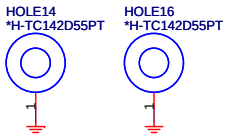




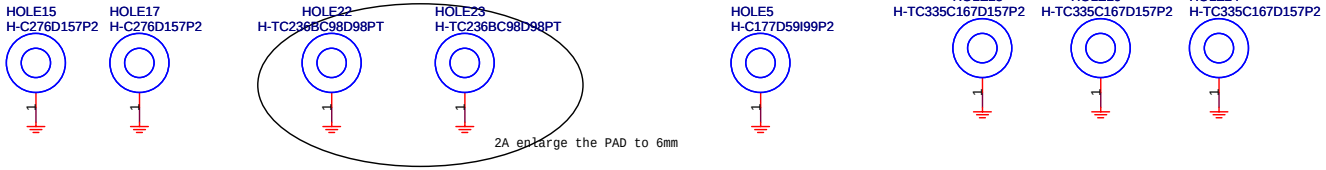


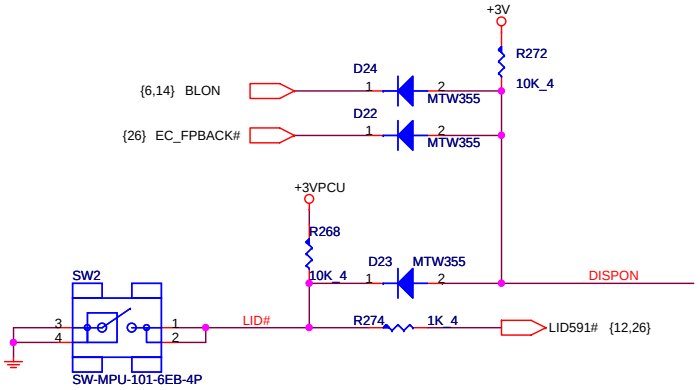


PCIE-CARD NUT



MDC1.5 NUT NB HEATSINK NUT LED/B NUT CPU NUT





Lid Switch

PROJECT : ZL9

Quanta Computer Inc.

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	LVDS,VGA Ports, LID, & HOLES	3A
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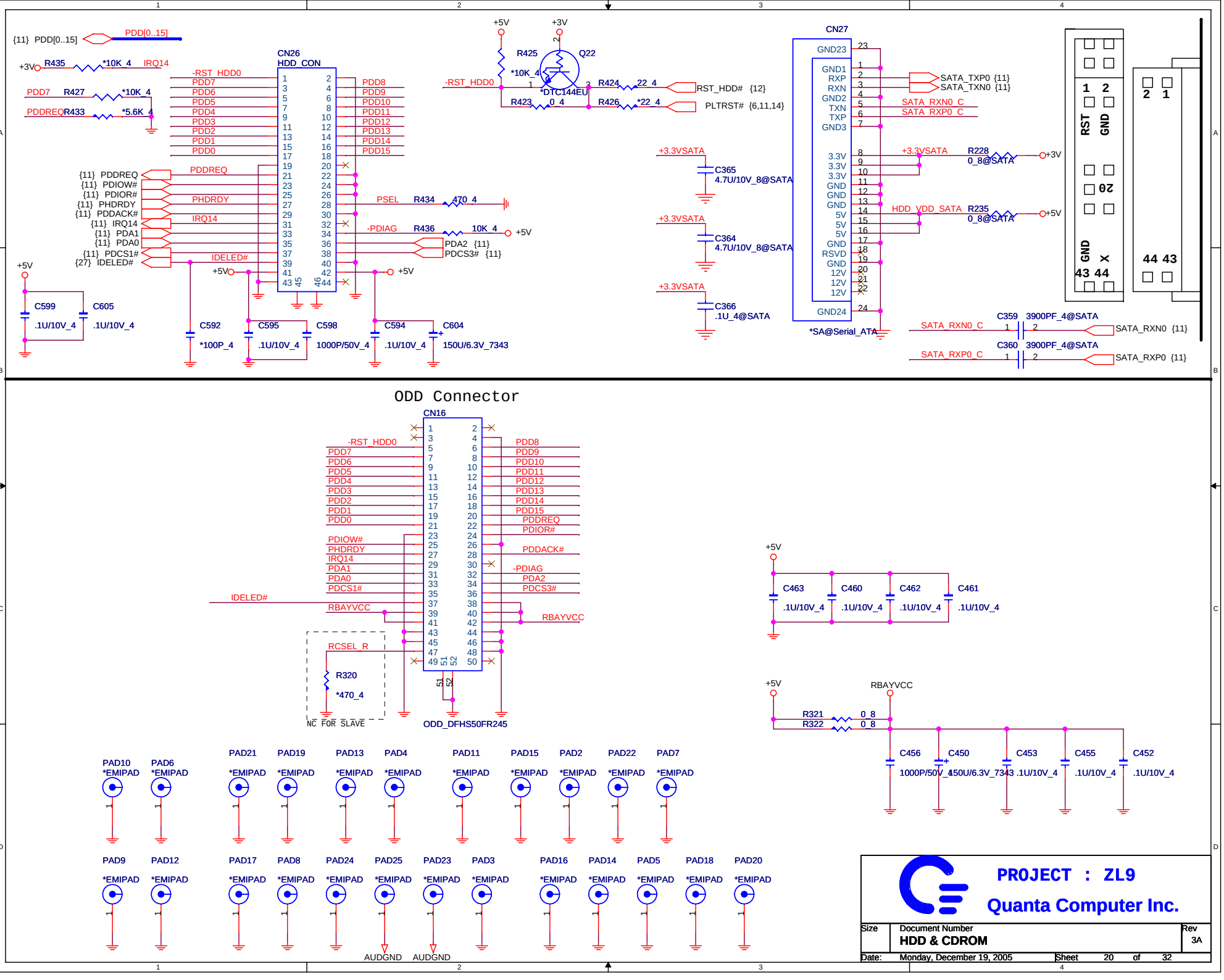
ODD Connector
CN26
HDD_CON
CN27
CN16
ODD_DFHS50FR245
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Quanta Computer Inc.
HDD & CDROM
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MINI-PCI

ID Select : AD20
Interrupt Pin : INTB# , INTD#
Request Indicate : REQ2#
Grant Indicate : GNT2#

CN28
MINIPCI_DGMC4000382

CN24
*67910-0002

Q11 *DTC144EU

Q26 *AO3403

3A : fix PCI-E card can't detect !

3A :reserved

U24 U25 U13 TPS2061DGNR

CN21 CN22 CN29 USB_DFHD04MR671

CN5 PTWO_MINIUSB

Q9 AO3403

DLW21HN900SQ2L

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Quanta Computer Inc.		
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ID Select : AD24
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#

U6

RTL8110SBL/8100CL

RTL8110SBL
VDD33---+3.3V DIGITAL
AVDDH------+3.3V ANALOG
AVDDL-----+2.5V ANALOG
DVDD-----+1.2V DIGITAL
DVDD_A----+1.2V ANALOG

RTL8100CL
VDD33---+3.3V DIGITAL
AVDDL-----+3.3V ANALOG
DVDD-----+2.5V DIGITAL
AVDDH------+2.5V ANALOG

Near Lan chipset

2A : modify for ESD issue

PROJECT : ZL9
Quanta Computer Inc.

Size	Document Number	Rev
	LAN RTL8110SBL/8100CL	3A

Date: Monday, December 19, 2005 Sheet 22 of 32

ID Select : AD17
Interrupt Pin : INTC#
Request Indicate : REQ1#
Grant Indicate : GNT1#

CARDBUS SLOT

U9-1 PCI1510PGE

U9-2 PCI1510PGE

U9-4 PCI1510PGE

CN25 FOX_WZ21131-G2

UPPER PIN

LOWER PIN

U11 TPS2211A

+3V Plane

Near Chipset

Near Slot

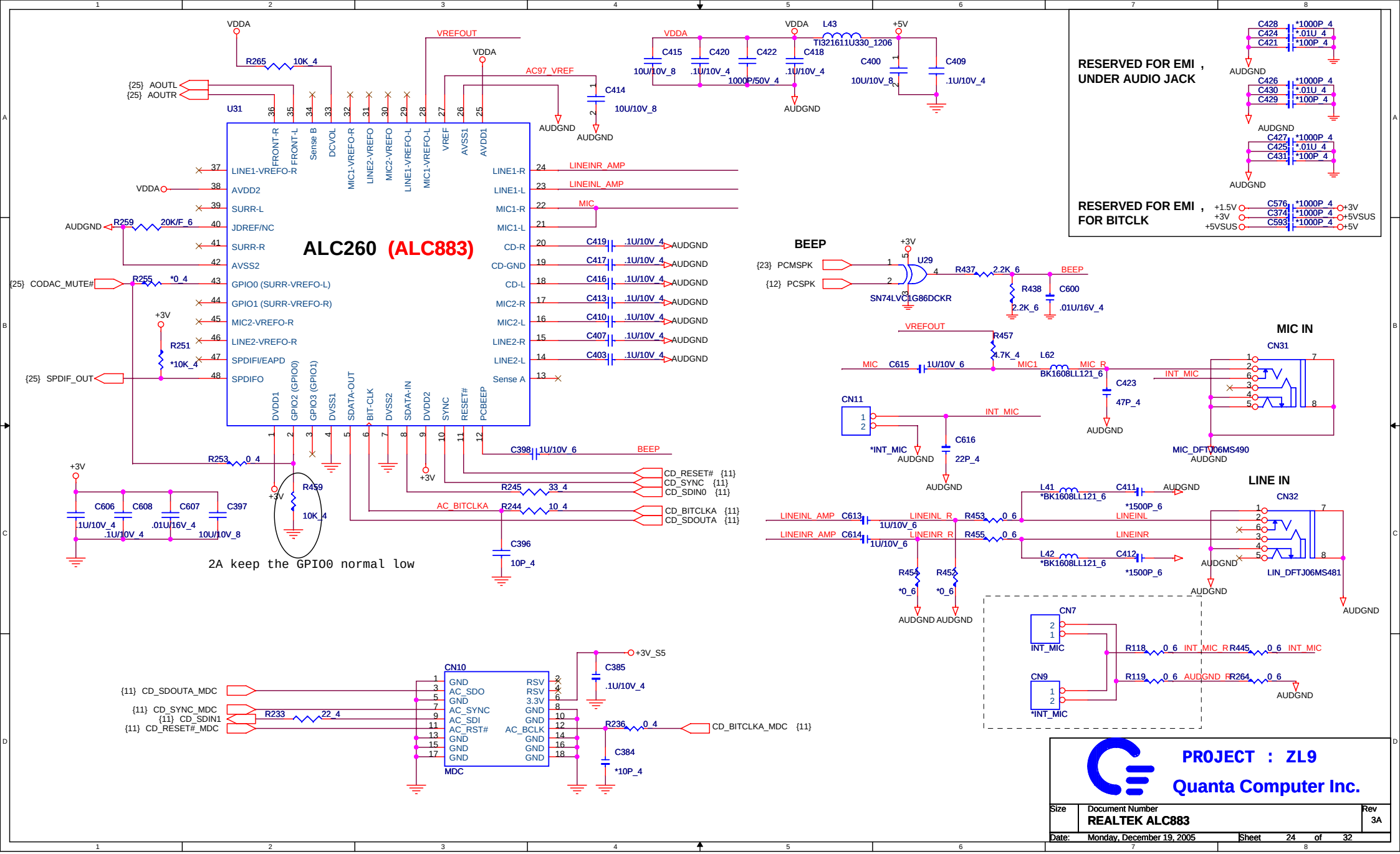
PROJECT : ZL9

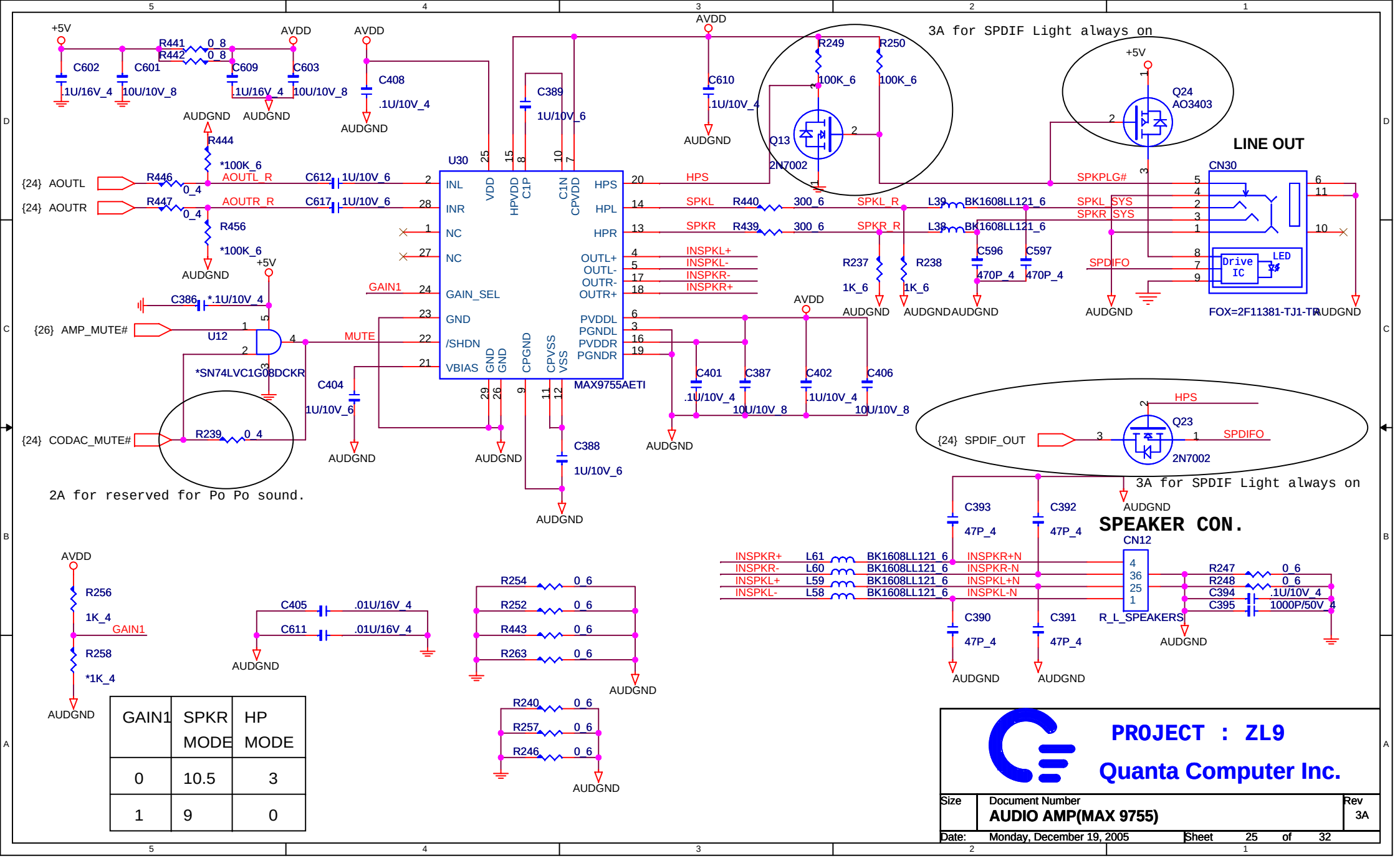
Quanta Computer Inc.

PCMCIA CONTROLLER

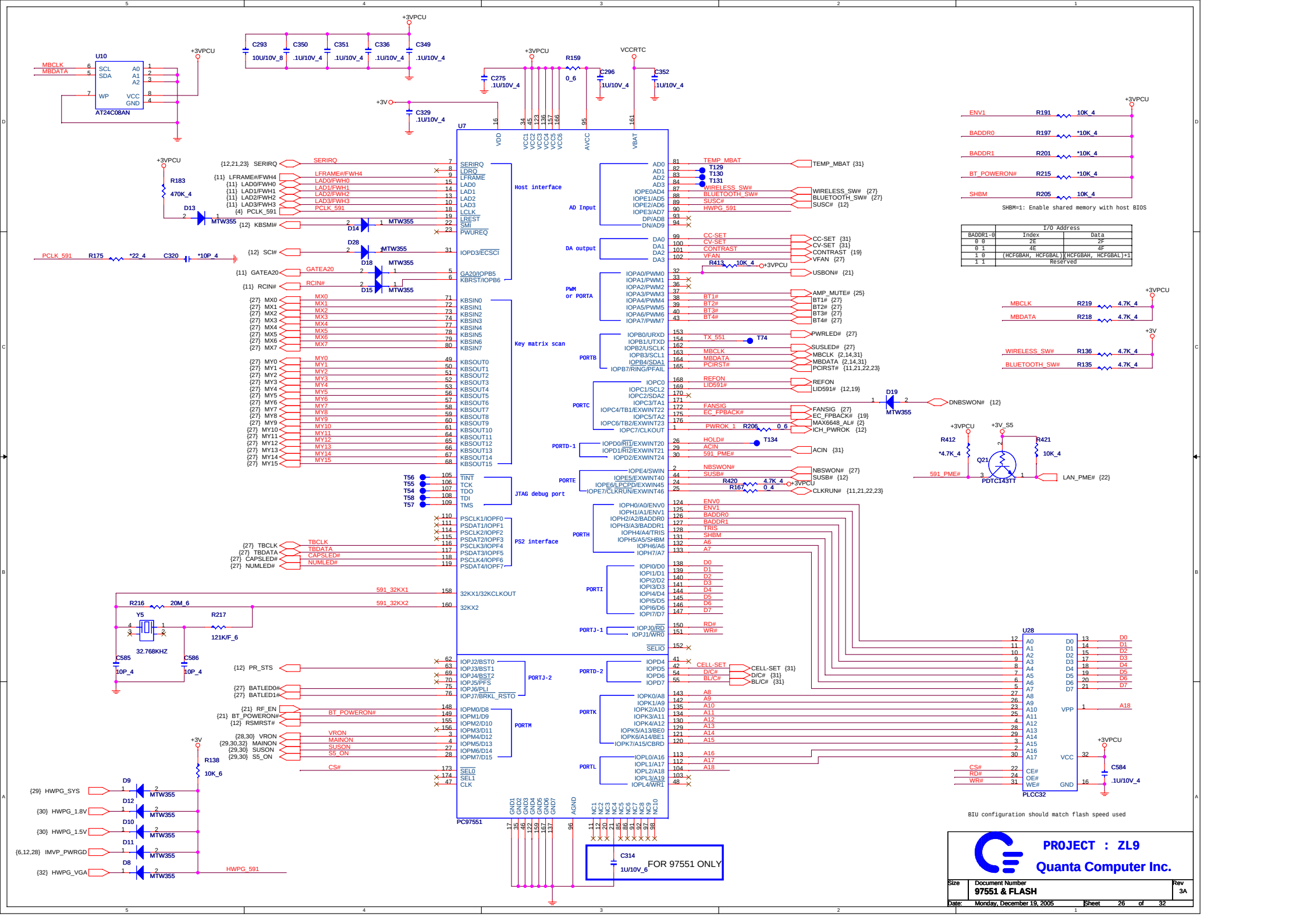
Rev 3A

Date: Monday, December 19, 2005 Sheet 23 of 32

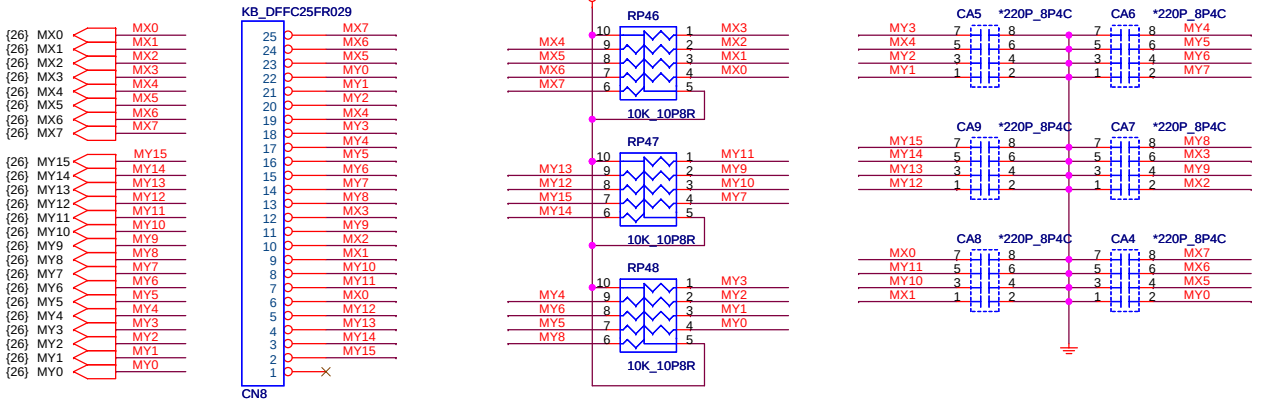

ALC260 (ALC883)
U31
VDDA
VREFOUT
AC97_VREF
AUDGND
R265 10K_4
C414 10U/10V_8
C415 10U/10V_8
C420 .1U/10V_4
C422 1000P/50V_4
C418 .1U/10V_4
L43 TI321611U330_1206
C400 10U/10V_8
C409 .1U/10V_4
{25} AOUTL
{25} AOUTR
FRONT-R
FRONT-L
Sense B
DCVOL
MIC1-VREFO-R
LINE2-VREFO
MIC2-VREFO
LINE1-VREFO-L
MIC1-VREFO-L
VREF
AVSS1
AVDD1
LINE1-VREFO-R
AVDD2
SURR-L
JDREF/NC
SURR-R
AVSS2
GPIO0 (SURR-VREFO-L)
GPIO1 (SURR-VREFO-R)
MIC2-VREFO-R
LINE2-VREFO-R
SPDIFI/EAPD
SPDIFO
LINE1-R
LINE1-L
MIC1-R
MIC1-L
CD-R
CD-GND
CD-L
MIC2-R
MIC2-L
LINE2-R
LINE2-L
Sense A
LINEINR_AMP
LINEINL_AMP
MIC
R259 20K/F_6
R255 *0_4
R251 *10K_4
R253 0_4
R459 10K_4
{25} CODAC_MUTE#
{25} SPDIF_OUT
DVDD1
GPIO2 (GPIO0)
GPIO3 (GPIO1)
DVSS1
SDATA-OUT
BIT-CLK
DVSS2
SDATA-IN
DVDD2
SYNC
RESET#
PCBEEP
C419 .1U/10V_4
C417 .1U/10V_4
C416 .1U/10V_4
C413 .1U/10V_4
C410 .1U/10V_4
C407 .1U/10V_4
C403 .1U/10V_4
C398 1U/10V_6
BEEP
R245 33_4
CD_RESET# {11}
CD_SYNC {11}
CD_SDIN0 {11}
AC_BITCLKA
R244 10_4
CD_BITCLKA {11}
CD_SDOUTA {11}
C396 10P_4
C606 .1U/10V_4
C608 .1U/10V_4
C607 .01U/16V_4
C397 10U/10V_8
2A keep the GPIO0 normal low
RESERVED FOR EMI , UNDER AUDIO JACK
C428 *1000P_4
C424 *.01U_4
C421 *100P_4
C426 *1000P_4
C430 *.01U_4
C429 *100P_4
C427 *1000P_4
C425 *.01U_4
C431 *100P_4
RESERVED FOR EMI , FOR BITCLK
+1.5V
+3V
+5VSUS
C576 *1000P_4
C374 *1000P_4
C593 *1000P_4
BEEP
U29
SN74LVC1G86DCKR
{23} PCMSPK
{12} PCSPK
R437 2.2K_6
R438 2.2K_6
C600 .01U/16V_4
MIC IN
CN31
MIC_DFTJ06MS490
VREFOUT
R457 4.7K_4
MIC C615 1U/10V_6
MIC1
MIC_R
L62 BK1608LL121_6
INT_MIC
C423 47P_4
CN11
*INT_MIC
C616 22P_4
LINE IN
CN32
LIN_DFTJ06MS481
LINEINL_AMP C613 1U/10V_6
LINEINR_AMP C614 1U/10V_6
LINEINL_R
LINEINR_R
R453 0_6
R455 0_6
L41 *BK1608LL121_6
L42 *BK1608LL121_6
C411 *1500P_6
C412 *1500P_6
LINEINL
LINEINR
R454 *0_6
R452 *0_6
CN7
CN9
R118 0_6 INT_MIC_R
R445 0_6 INT_MIC
R119 0_6 AUDGND_R
R264 0_6
CN10
MDC
{11} CD_SDOUTA_MDC
{11} CD_SYNC_MDC
{11} CD_SDIN1
{11} CD_RESET#_MDC
R233 22_4
+3V_S5
C385 .1U/10V_4
C384 *10P_4
R236 0_4
CD_BITCLKA_MDC {11}
PROJECT : ZL9
Quanta Computer Inc.
Size
Document Number
REALTEK ALC883
Rev
3A
Date: Monday, December 19, 2005
Sheet 24 of 32



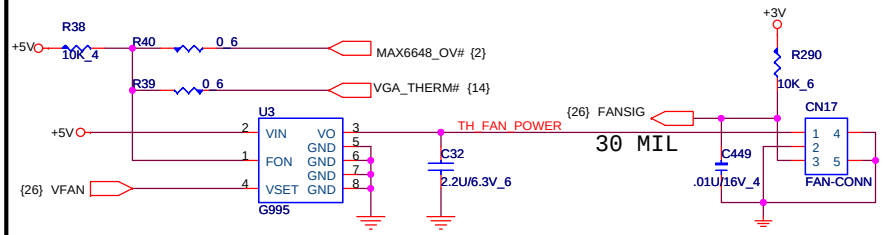
GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0


U10
AT24C08AN
MBCLK
MBDATA
SCL
SDA
WP
A0
A1
A2
VCC
GND
+3VPCU
C293 10U/10V_8
C350 .1U/10V_4
C351 .1U/10V_4
C336 .1U/10V_4
C349 .1U/10V_4
C275 .1U/10V_4
C329 .1U/10V_4
+3V
R159 0_6
C296 .1U/10V_4
VCCRTC
C352 .1U/10V_4
U7
PC97551
VDD
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
AVCC
VBAT
Host interface
SERIRQ
LDRQ
LFRAME
LAD0
LAD1
LAD2
LAD3
LCLK
LRESET
SMI
PWUREQ
IOPD3/ECSCI
GA20/IOPB5
KBRST/IOPB6
AD Input
DA output
PWM or PORTA
PORTB
PORTC
PORTD-1
PORTE
Key matrix scan
JTAG debug port
PS2 interface
PORTH
PORTI
PORTJ-1
PORTJ-2
PORTD-2
PORTK
PORTM
PORTL
SELIO
32KX1/32KCLKOUT
32KX2
TEMP_MBAT
WIRELESS_SW#
BLUETOOTH_SW#
SUSC#
HWPG_591
CC-SET
CV-SET
CONTRAST
VFAN
USBON#
AMP_MUTE#
BT1#
BT2#
BT3#
BT4#
PWRLED#
SUSLED#
MBCLK
MBDATA
PCIRST#
REFON
LID591#
FANSIG
EC_FPBACK#
MAX6648_AL#
ICH_PWROK
HOLD#
ACIN
591_PME#
NBSWON#
SUSB#
CLKRUN#
ENV0
ENV1
BADDR0
BADDR1
TRIS
SHBM
A6
A7
D0
D1
D2
D3
D4
D5
D6
D7
RD#
WR#
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
CELL-SET
D/C#
BL/C#
TBCLK
TBDATA
CAPSLED#
NUMLED#
PR_STS
BATLED0#
BATLED1#
RF_EN
BT_POWERON#
RSMRST#
VRON
MAINON
SUSON
S5_ON
CS#
SELO
SEL1
CLK
TINT
TCK
TDO
TDI
TMS
T56
T55
T54
T58
T57
T129
T130
T131
T74
T134
R183 470K_4
D13 MTW355
D14 MTW355
D28 MTW355
D18 MTW355
D15 MTW355
R175 *22_4
C320 *10P_4
R413 10K_4
R206 0_6
R420 4.7K_4
R167 0_4
D19 MTW355
R216 20M_6
R217 121K/F_6
Y5 32.768KHZ
C585 10P_4
C586 10P_4
R138 10K_6
D9 MTW355
D12 MTW355
D10 MTW355
D11 MTW355
D8 MTW355
{29} HWPG_SYS
{30} HWPG_1.8V
{30} HWPG_1.5V
{6,12,28} IMVP_PWRGD
{32} HWPG_VGA
HWPG_591
C314 1U/10V_6
FOR 97551 ONLY
ENV1 R191 10K_4
BADDR0 R197 *10K_4
BADDR1 R201 *10K_4
BT_POWERON# R215 *10K_4
SHBM R205 10K_4
SHBM=1: Enable shared memory with host BIOS
I/O Address
BADDR1-0 | Index | Data
0 0 | 2E | 2F
0 1 | 4E | 4F
1 0 | (HCFGBAH, HCFGBAL) | (HCFGBAH, HCFGBAL)+1
1 1 | Reserved
MBCLK R219 4.7K_4
MBDATA R218 4.7K_4
WIRELESS_SW# R136 4.7K_4
BLUETOOTH_SW# R135 4.7K_4
R412 *4.7K_4
Q21 PDTC143TT
R421 10K_4
LAN_PME# {22}
U28
PLCC32
C584 .1U/10V_4
BIU configuration should match flash speed used
PROJECT : ZL9
Quanta Computer Inc.
Size
Document Number
97551 & FLASH
Rev
3A
Date: Monday, December 19, 2005
Sheet 26 of 32

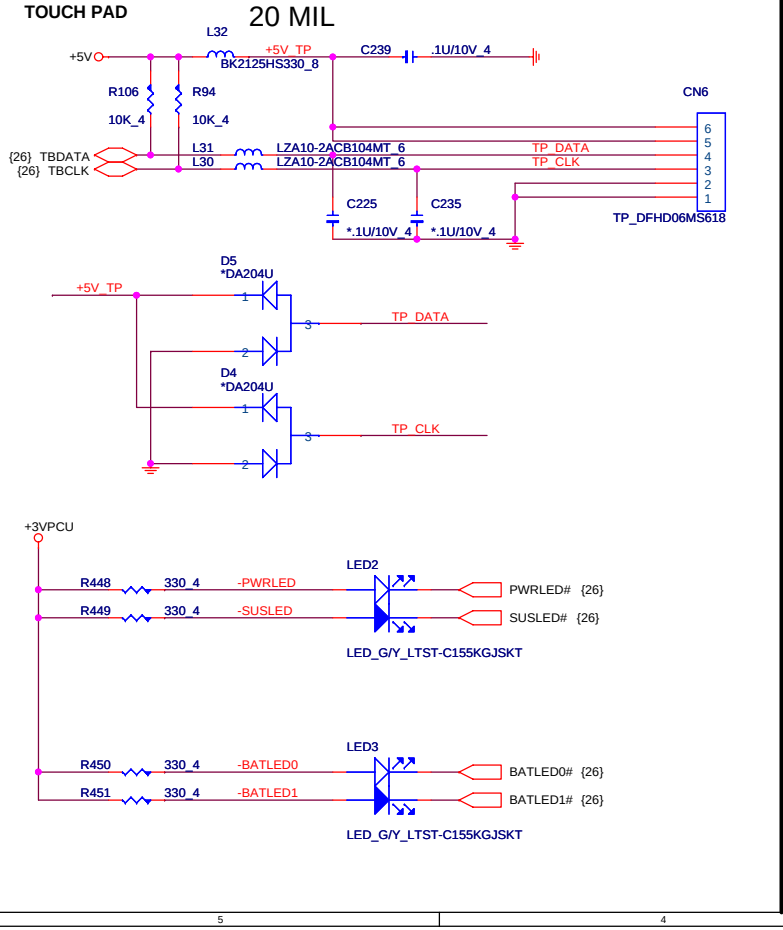
INT K/B

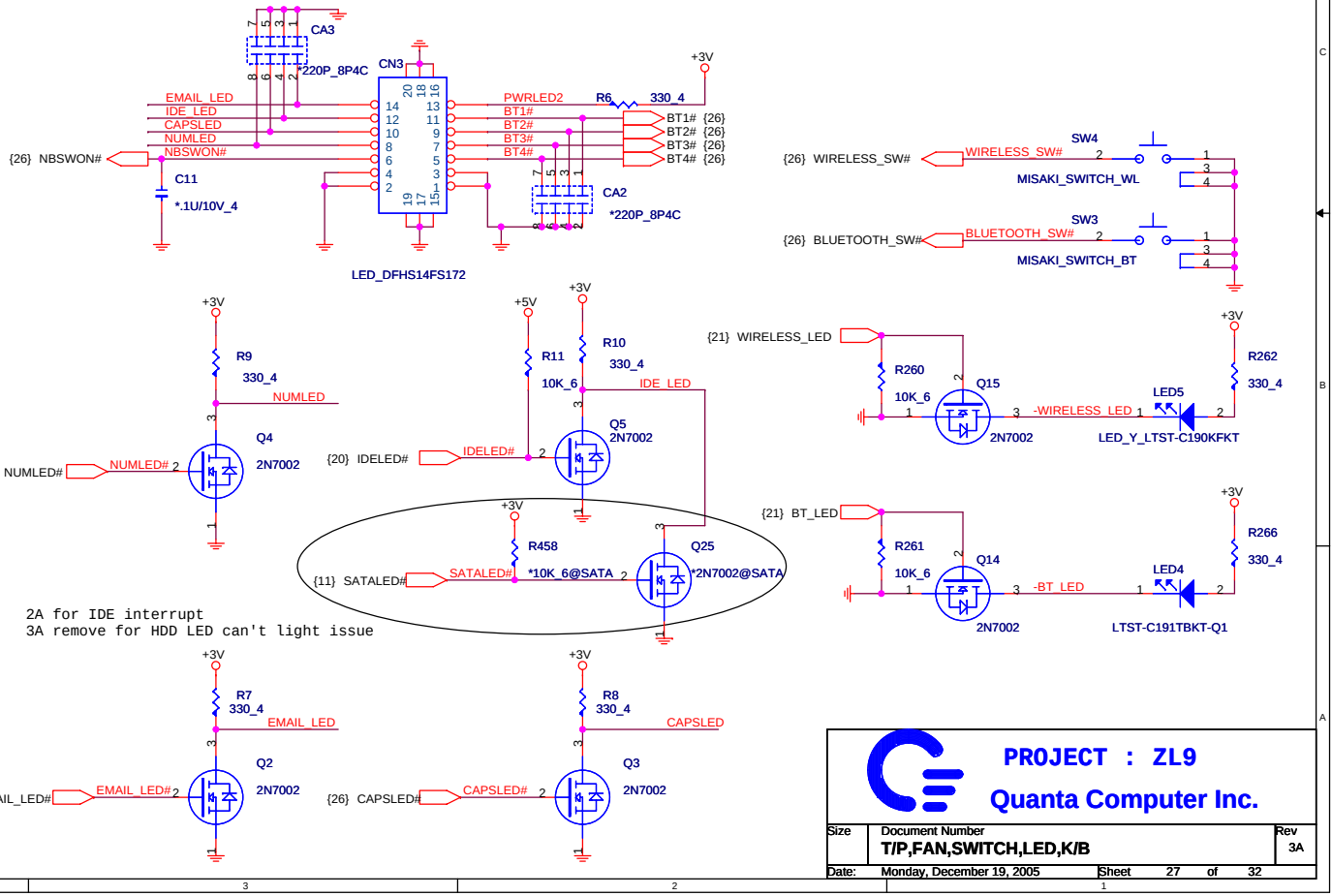


FAN CONTROL

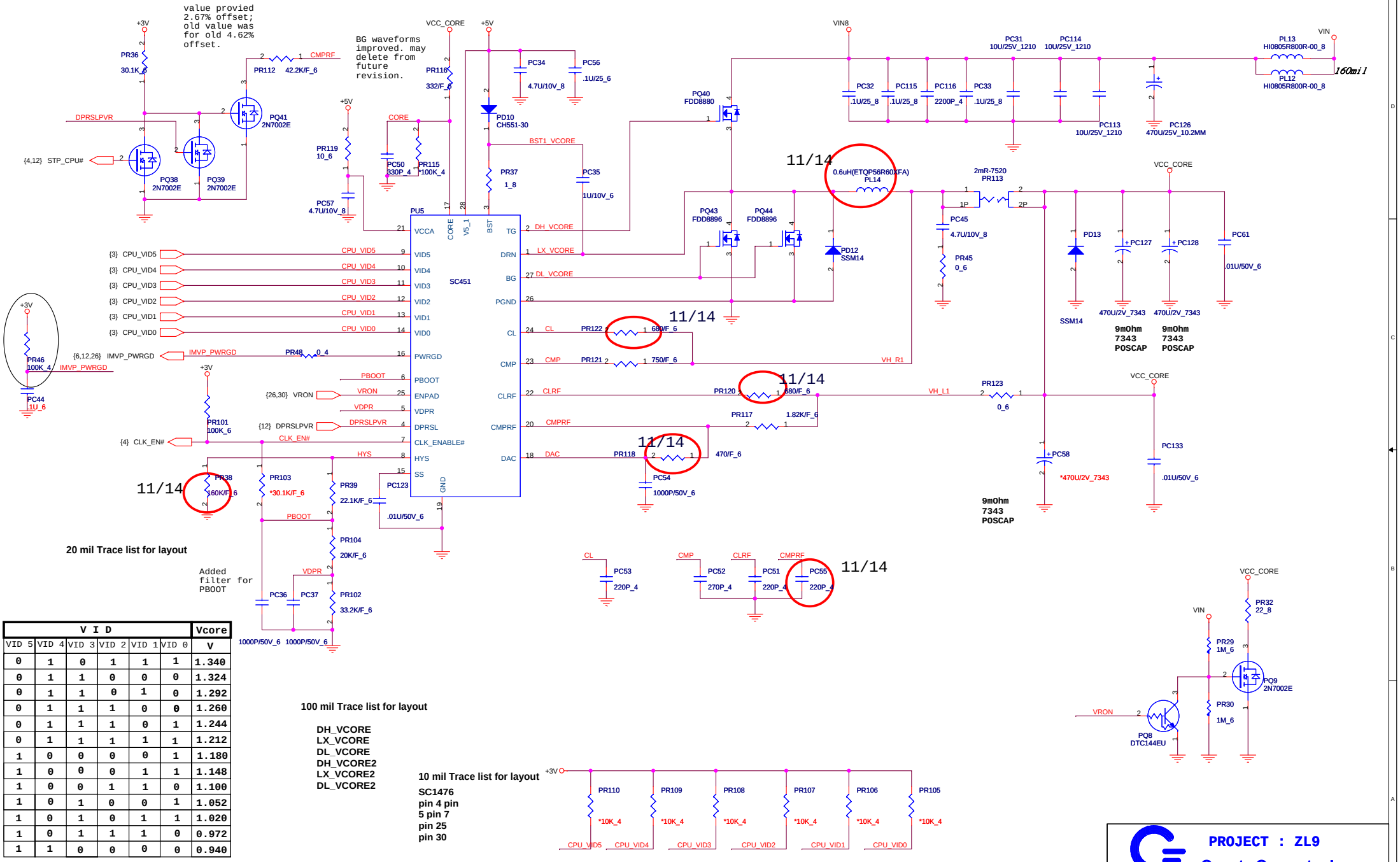


TOUCH PAD





PROJECT : ZL9		
Quanta Computer Inc.		
Size	Document Number: T/P,FAN,SWITCH,LED,K/B	Rev: 3A
Date: Monday, December 19, 2005	Sheet 27 of 32	

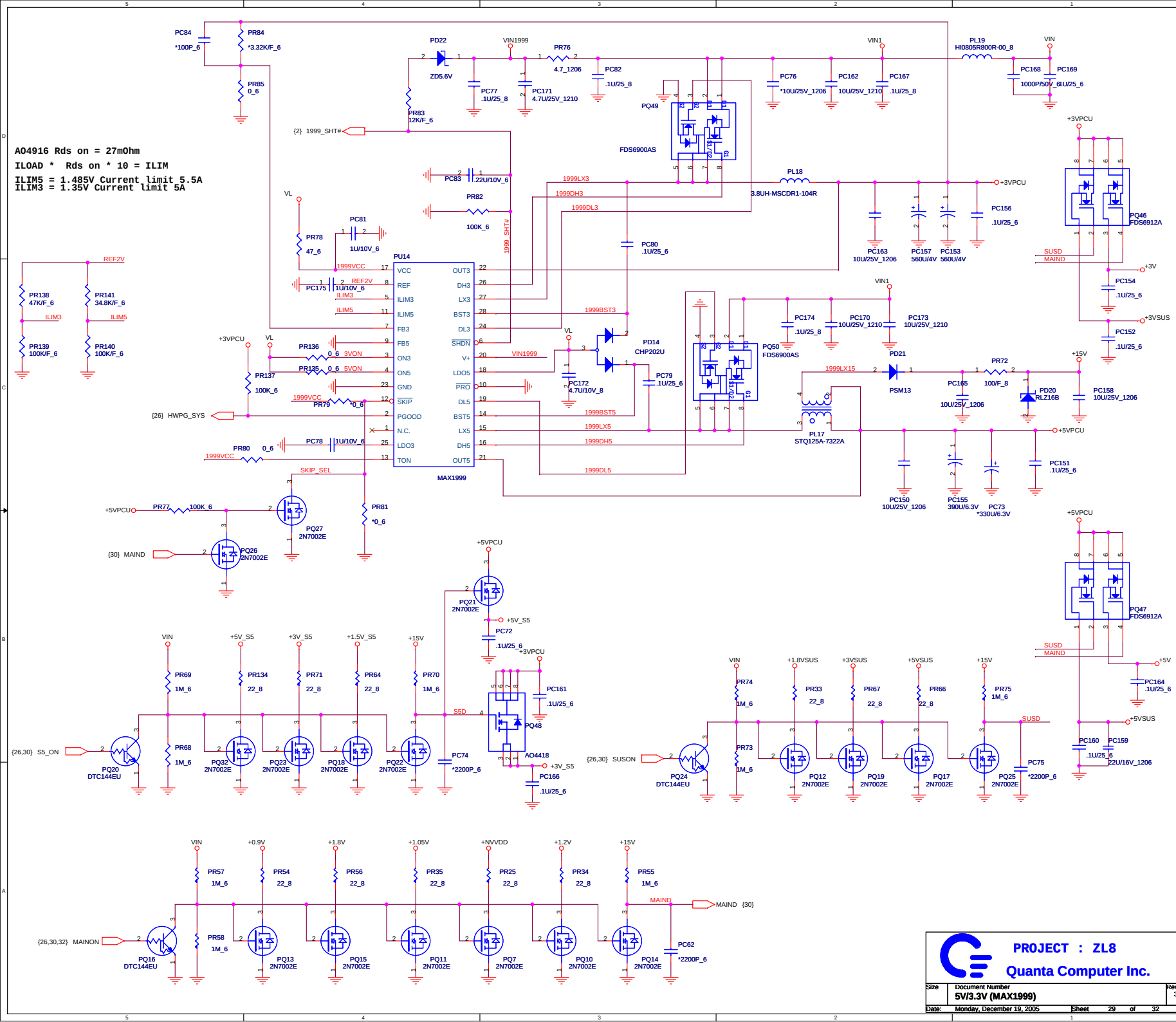


V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

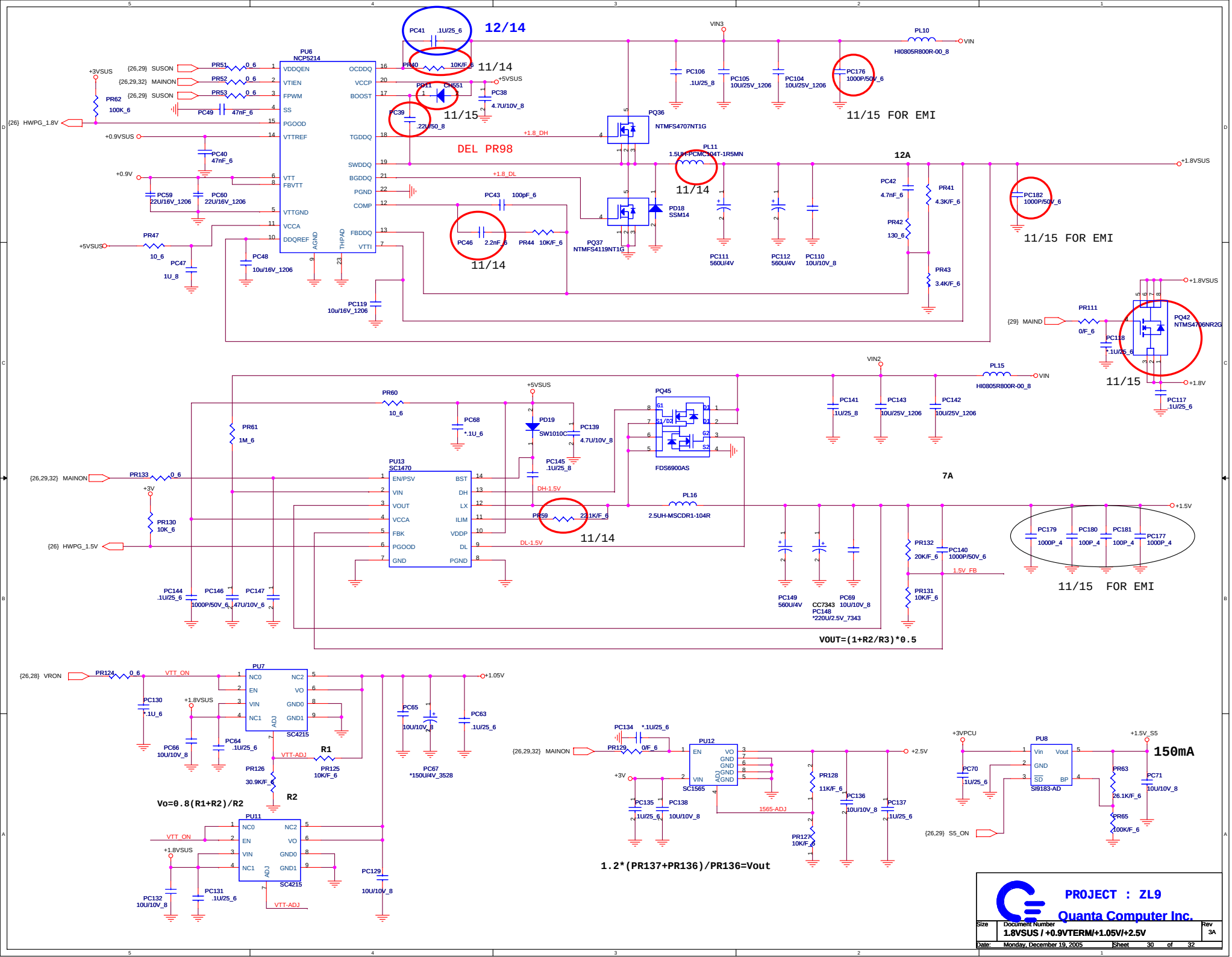
AO4916 Rds on = 27mOhm

ILOAD * Rds on * 10 = ILIM

ILIM5 = 1.485V Current limit 5.5A
ILIM3 = 1.35V Current limit 5A



PROJECT : ZL8		
Quanta Computer Inc.		
Size	Document Number: 5V/3.3V (MAX1999)	Rev: 3A
Date: Monday, December 19, 2005	Sheet 29 of 32	


12/14
11/14
11/15
DEL PR98
11/15 FOR EMI
12A
7A
11/14
11/15
11/15 FOR EMI
11/14
11/15 FOR EMI
VOUT=(1+R2/R3)*0.5
Vo=0.8(R1+R2)/R2
1.2*(PR137+PR136)/PR136=Vout
150mA
PROJECT : ZL9
Quanta Computer Inc.
1.8VSUS / +0.9VTERM/+1.05V/+2.5V
Monday, December 19, 2005
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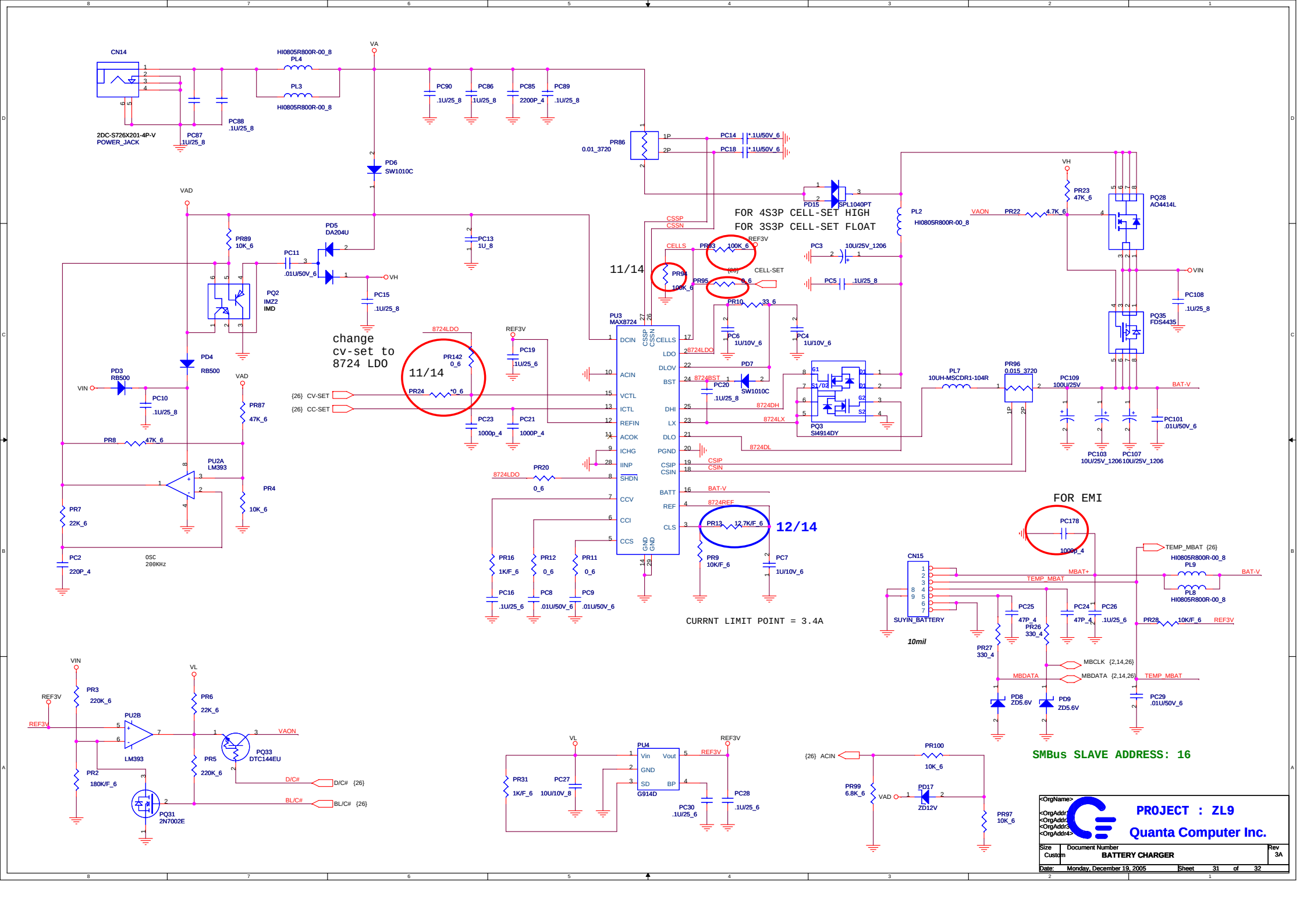
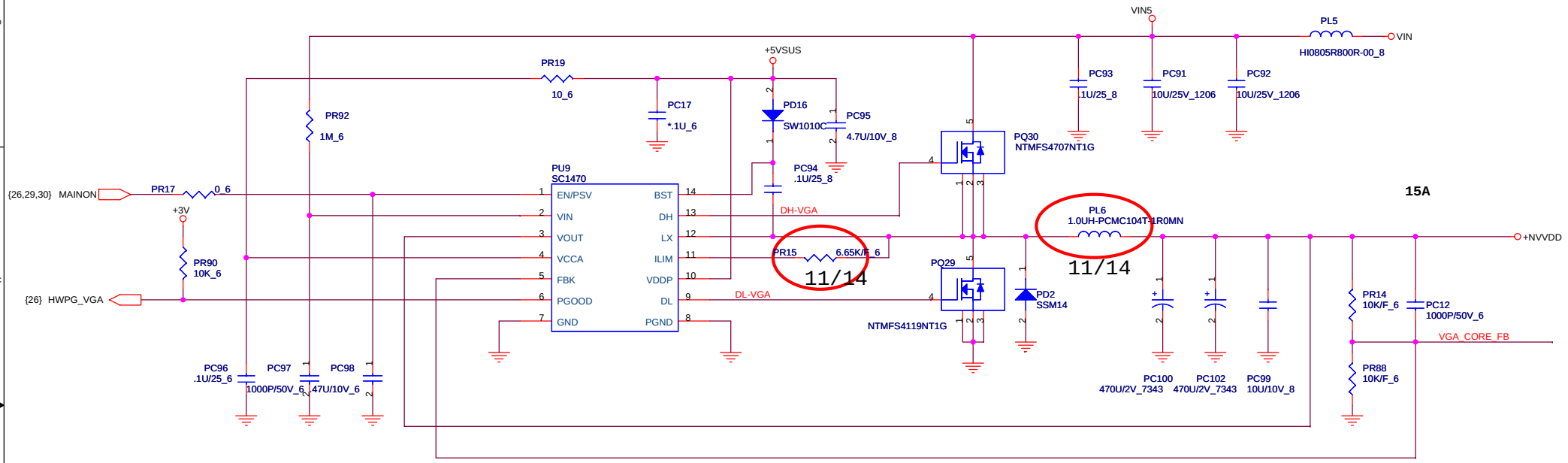
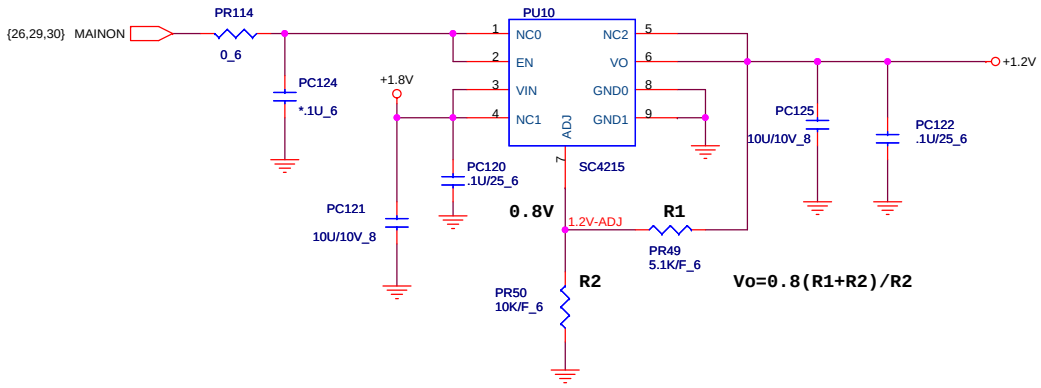

CN14
2DC-S726X201-4P-V
POWER_JACK
PC87 .1U/25_8
PC88 .1U/25_8
HI0805R800R-00_8
PL4
PL3
HI0805R800R-00_8
VA
PC90 .1U/25_8
PC86 1U/25_8
PC85 2200P_4
PC89 .1U/25_8
PD6 SW1010C
PR86 0.01_3720
PC14 *.1U/50V_6
PC18 *.1U/50V_6
PD15 SPL1040PT
PL2 HI0805R800R-00_8
VAON
PR22 4.7K_6
VH
PR23 47K_6
PQ28 AO4414L
PQ35 FDS4435
VIN
PC108 .1U/25_8
PC109 100U/25V
PC103 10U/25V_1206
PC107 10U/25V_1206
PC101 .01U/50V_6
PL7 10UH-MSCDR1-104R
PR96 0.015_3720
BAT-V
PQ3 SI4914DY
PD7 SW1010C
PC20 .1U/25_8
PC6 1U/10V_6
PC4 1U/10V_6
PR10 33_6
PC3 10U/25V_1206
PC5 .1U/25_8
PR93 100K_6
PR94 100K_6
PR95 0_6
CELL-SET
CELLS
REF3V
CSSP
CSSN
FOR 4S3P CELL-SET HIGH
FOR 3S3P CELL-SET FLOAT
11/14
PU3 MAX8724
DCIN
ACIN
VCTL
ICTL
REFIN
ACOK
ICHG
IINP
SHDN
CCV
CCI
CCS
CELLS
LDO
DLOV
BST
DHI
LX
DLO
PGND
CSIP
CSIN
BATT
REF
CLS
GND
8724LDO
8724BST
8724DH
8724LX
8724DL
8724REF
BAT-V
PD5 DA204U
PC11 .01U/50V_6
PC15 .1U/25_8
PC13 1U_8
PD4 RB500
PD3 RB500
PC10 .1U/25_8
PR89 10K_6
PQ2 IMZ2 IMD
VAD
PR87 47K_6
PR8 47K_6
PU2A LM393
PR7 22K_6
PR4 10K_6
PC2 220P_4
OSC 200KHz
change cv-set to 8724 LDO
11/14
PR142 0_6
PR24 *0_6
{26} CV-SET
{26} CC-SET
PC19 1U/25_6
PC23 1000p_4
PC21 1000P_4
PR20 0_6
PR16 1K/F_6
PR12 0_6
PR11 0_6
PC16 .1U/25_6
PC8 .01U/50V_6
PC9 .01U/50V_6
PR13 12.7K/F_6
12/14
PR9 10K/F_6
PC7 1U/10V_6
CURRNT LIMIT POINT = 3.4A
FOR EMI
PC178 1000P_4
CN15
SUYIN_BATTERY
10mil
TEMP_MBAT {26}
HI0805R800R-00_8
PL9
PL8
MBAT+
TEMP_MBAT
PC25 47P_4
PC24 47P_4
PC26 .1U/25_6
PR26 330_4
PR27 330_4
PR28 10K/F_6
MBCLK {2,14,26}
MBDATA
MBDATA {2,14,26}
PD8 ZD5.6V
PD9 ZD5.6V
PC29 .01U/50V_6
SMBus SLAVE ADDRESS: 16
VIN
PR3 220K_6
REF3V
PU2B LM393
PR2 180K/F_6
VL
PR6 22K_6
PR5 220K_6
PQ33 DTC144EU
VAON
D/C#
D/C# {26}
BL/C#
BL/C# {26}
PQ31 2N7002E
PU4 G914D
Vin
Vout
GND
SD
BP
PR31 1K/F_6
PC27 10U/10V_8
PC30 .1U/25_6
PC28 .1U/25_6
{26} ACIN
PR100 10K_6
PR99 6.8K_6
PD17 ZD12V
PR97 10K_6
<OrgName>
<OrgAddr1>
<OrgAddr2>
<OrgAddr3>
<OrgAddr4>
PROJECT : ZL9
Quanta Computer Inc.
Size Custom
Document Number BATTERY CHARGER
Rev 3A
Date: Monday, December 19, 2005
Sheet 31 of 32





PROJECT : ZL9

Quanta Computer Inc.

Size	Document Number	Rev
	VGA CORE/+1.2V	3A

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