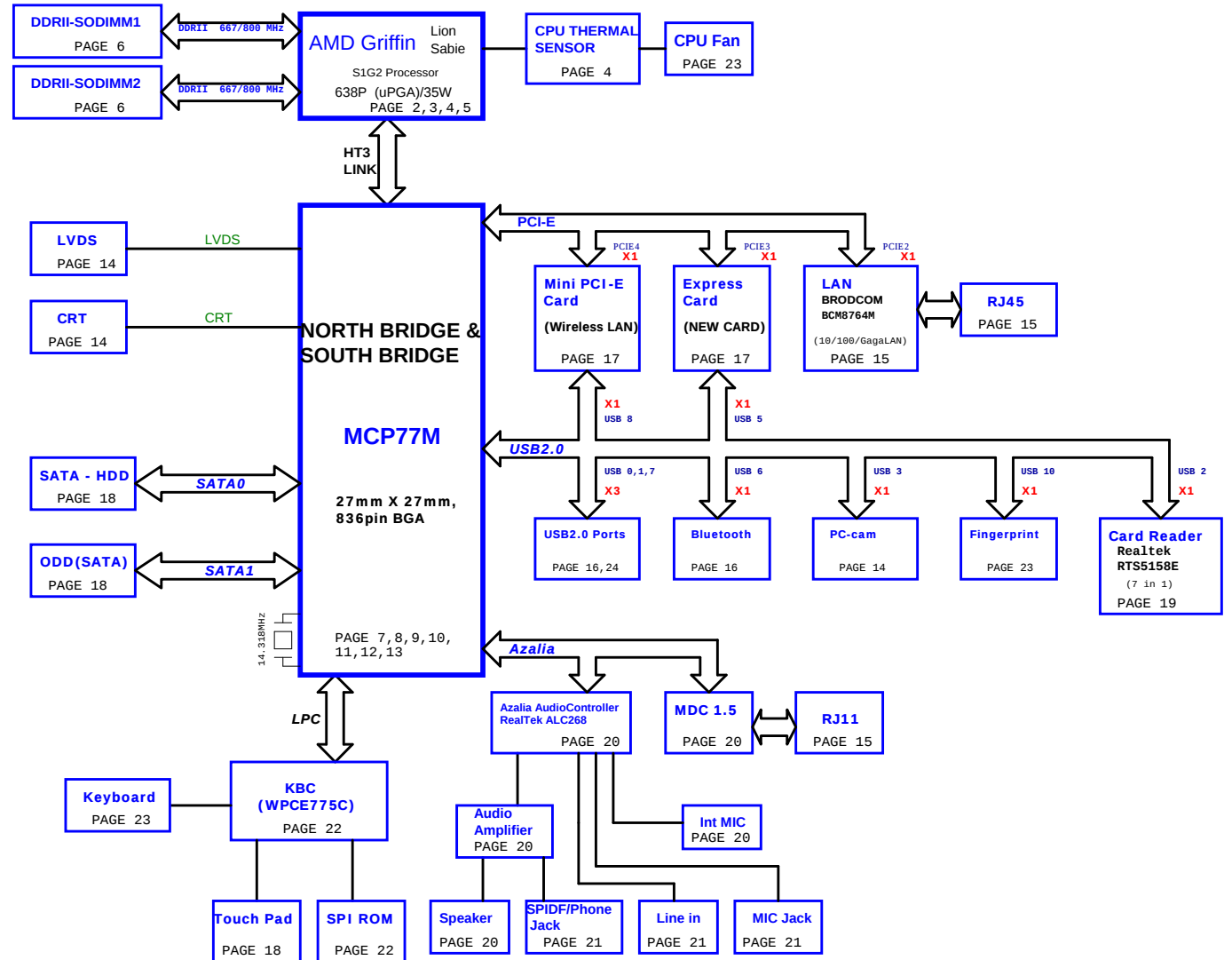


Z05 SYSTEM BLOCK DIAGRAM



CPU CORE / VDDNB (ISL6265A)	PAGE 26
NB_CORE +1.1V (RT8202)	PAGE 28
+1.1V_NB (RT8202)	PAGE 27
DDR II SMDDR_VTERM 1.8VSUS(TPSS116REGR)	PAGE 29
SYSTEM POWER (ISL6237)	PAGE 25
SYSTEM CHARGER (ISL6251A)	PAGE 24



PCB STACK UP

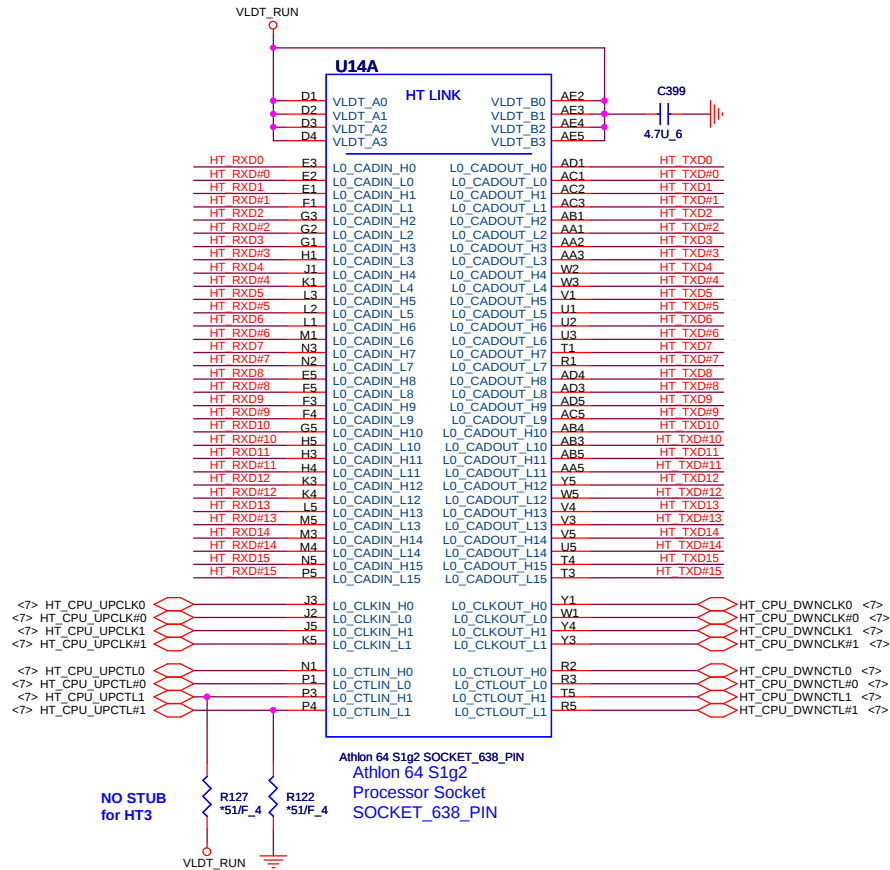
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

<7> HT_RXD#[15..0] HT_RXD#[15..0]
 <7> HT_TXD#[15..0] HT_TXD#[15..0]

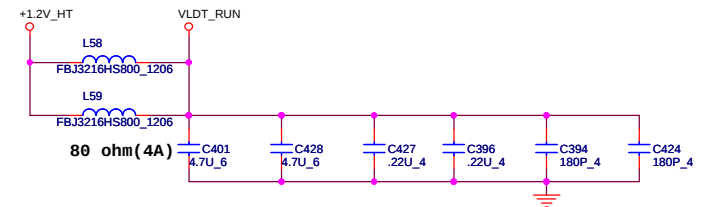


PROCESSOR HYPERTRANSPORT INTERFACE

VLDLT_Ax AND VLDLT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Note: on MCP77, (HT=+1.1V) and CPU(HT=+1.2V) and therefore cannot be connected to the same HT power rail.



LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
 PLACE CLOSE TO VLDLT0 POWER PINS

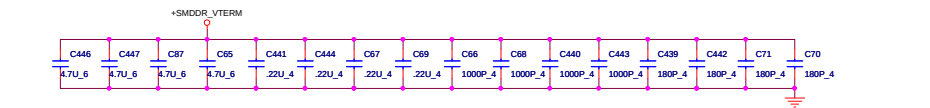
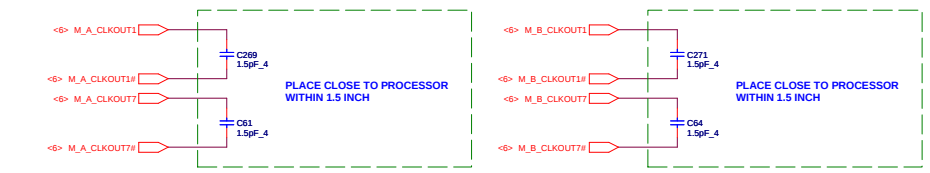
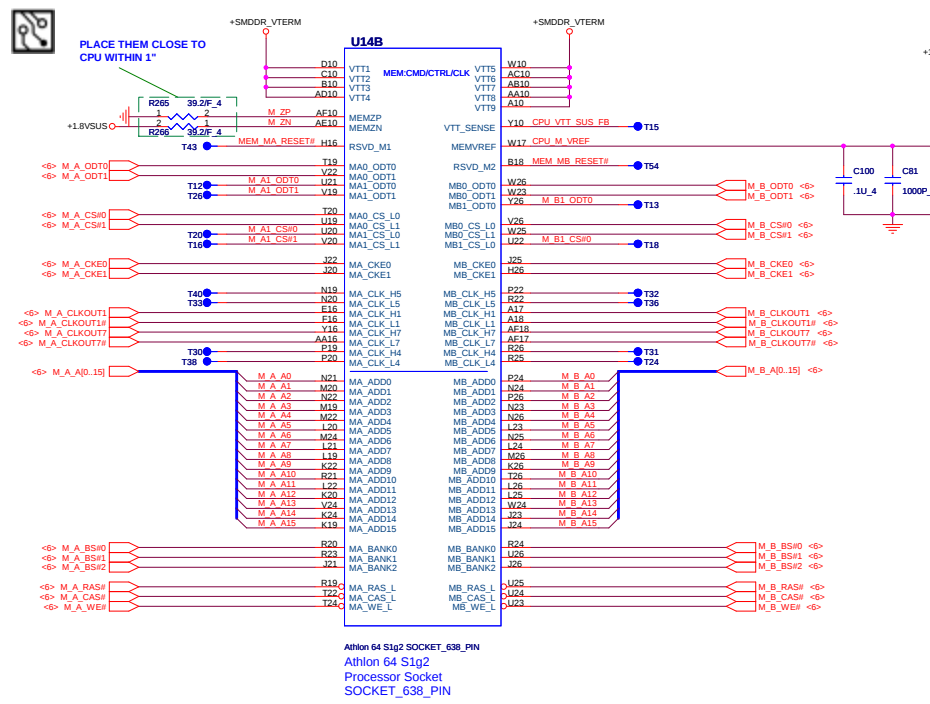
Quanta Computer Inc.
PROJECT : Z05

Size	Document Number	Rev
		1A

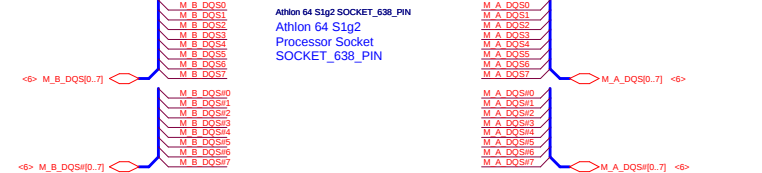
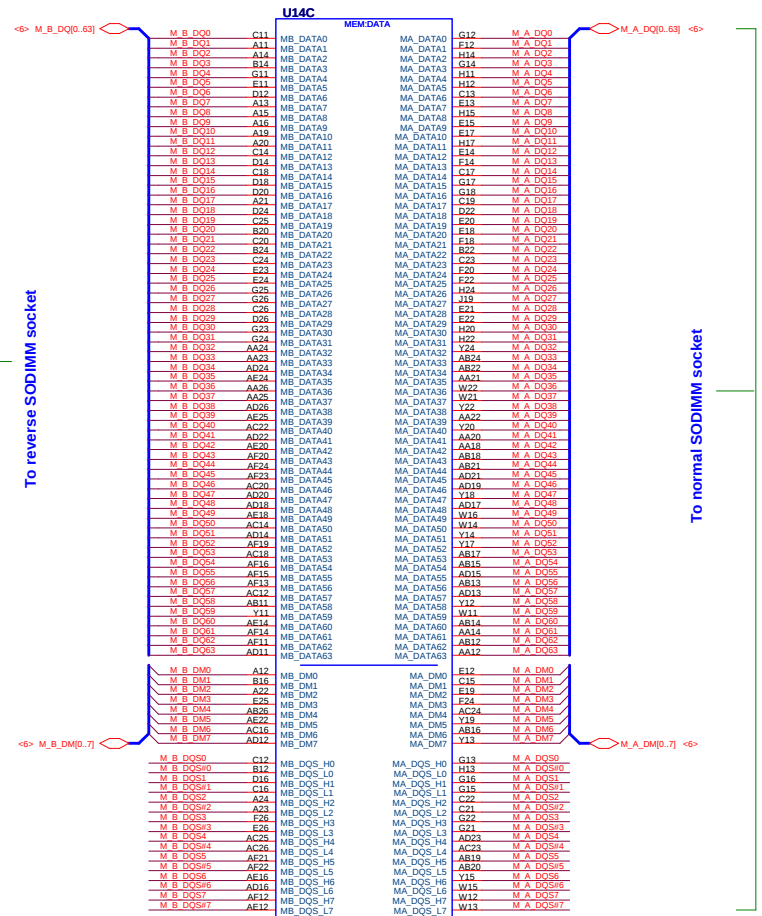
AMD Griffin HT I/F

Date: Monday, February 25, 2008	Sheet 2 of 34
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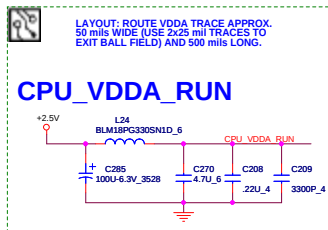
VDD, VTT, SUS, CPU IS CONNECTED TO THE VDD, VTT, SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



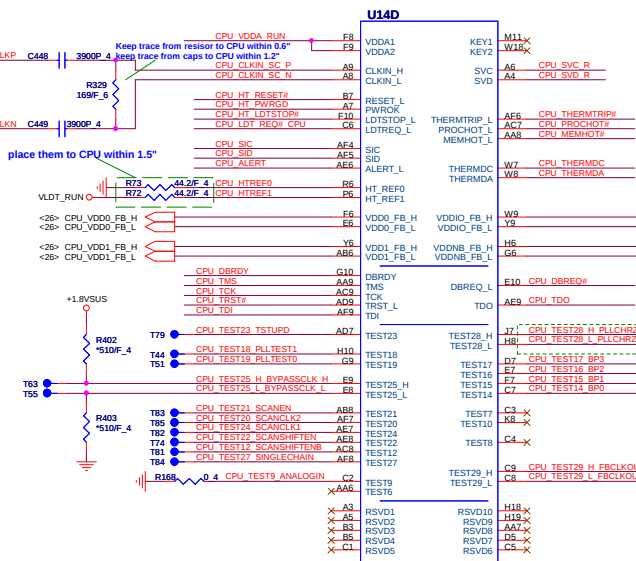
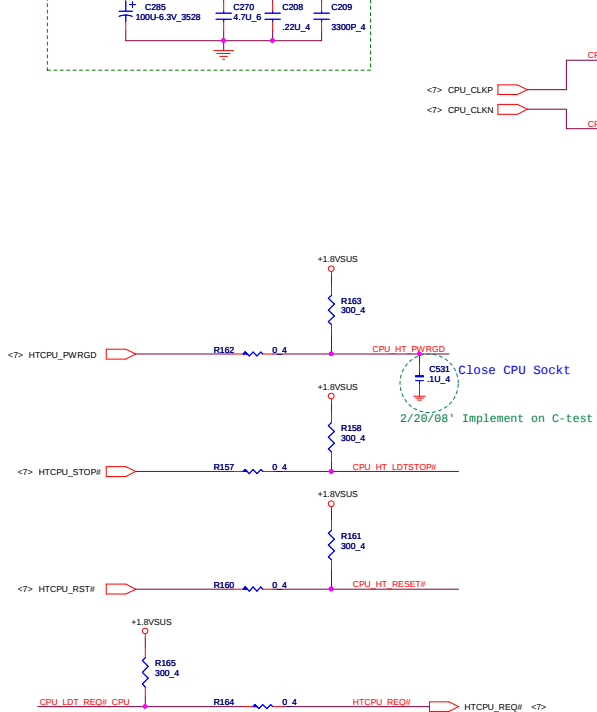
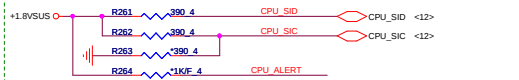
Processor DDR2 Memory Interface



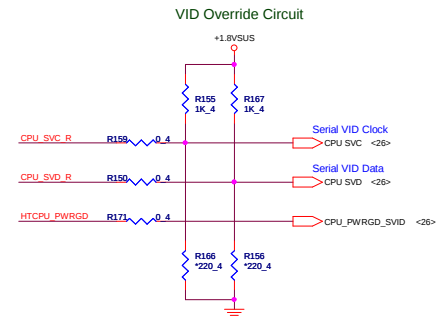
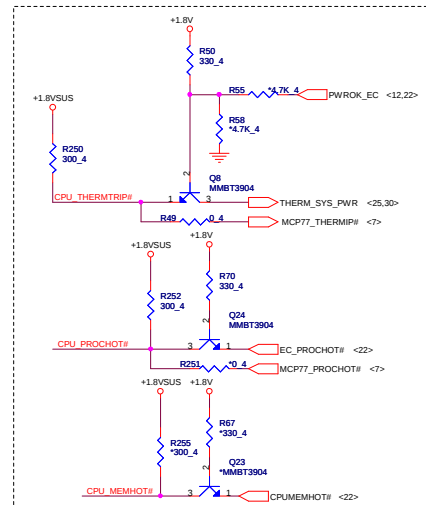
ATHLON Control and Debug



If AMD SI is not used, the SID pin can be left unconnected. The SID pin should have a 390- (±5%) pulldown to VSS.

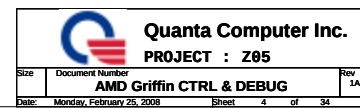
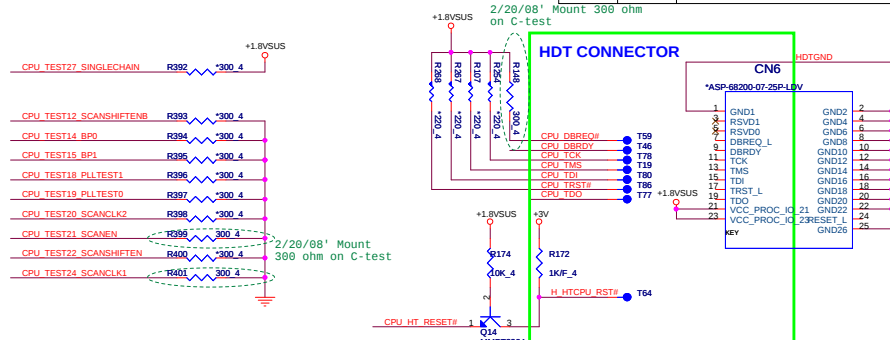
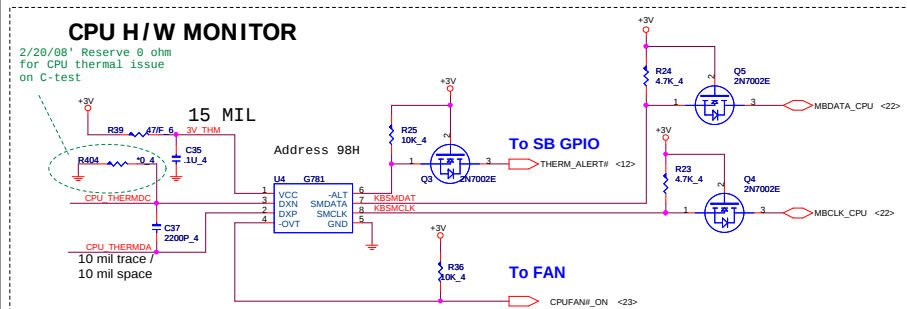


Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN

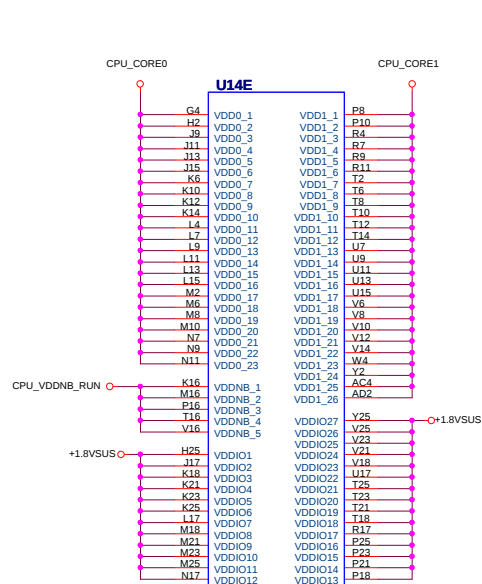


VID Override Circuit

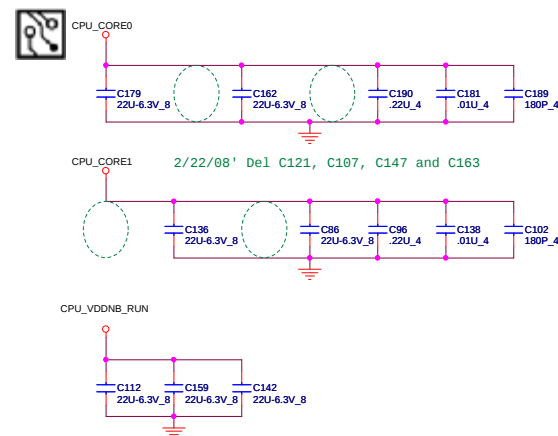
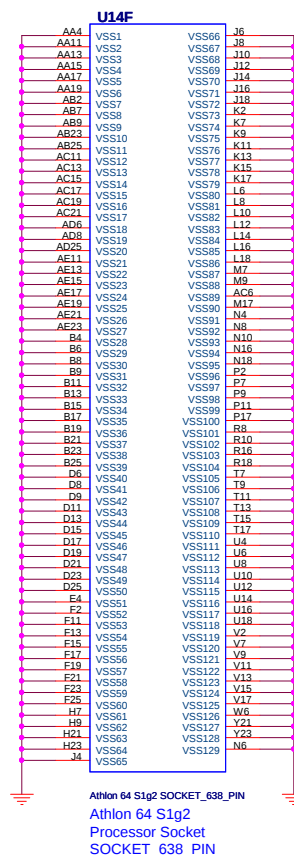
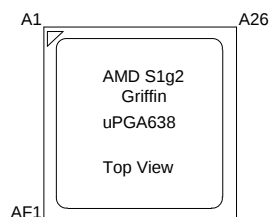
SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V



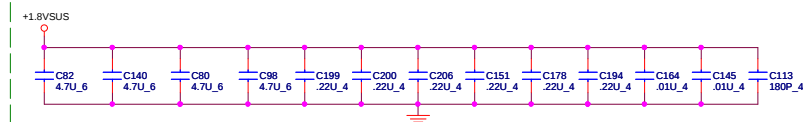
PROCESSOR POWER AND GROUND

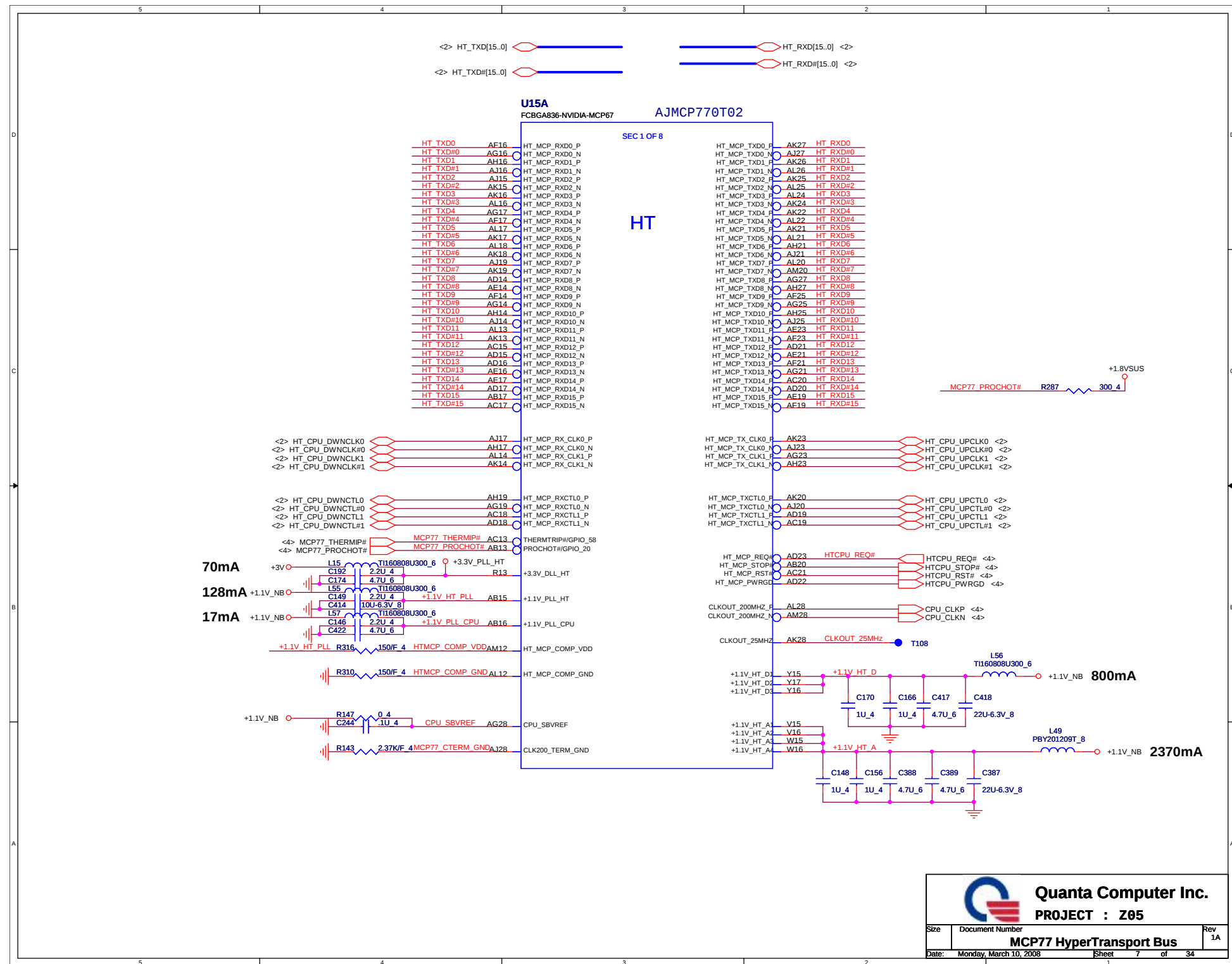


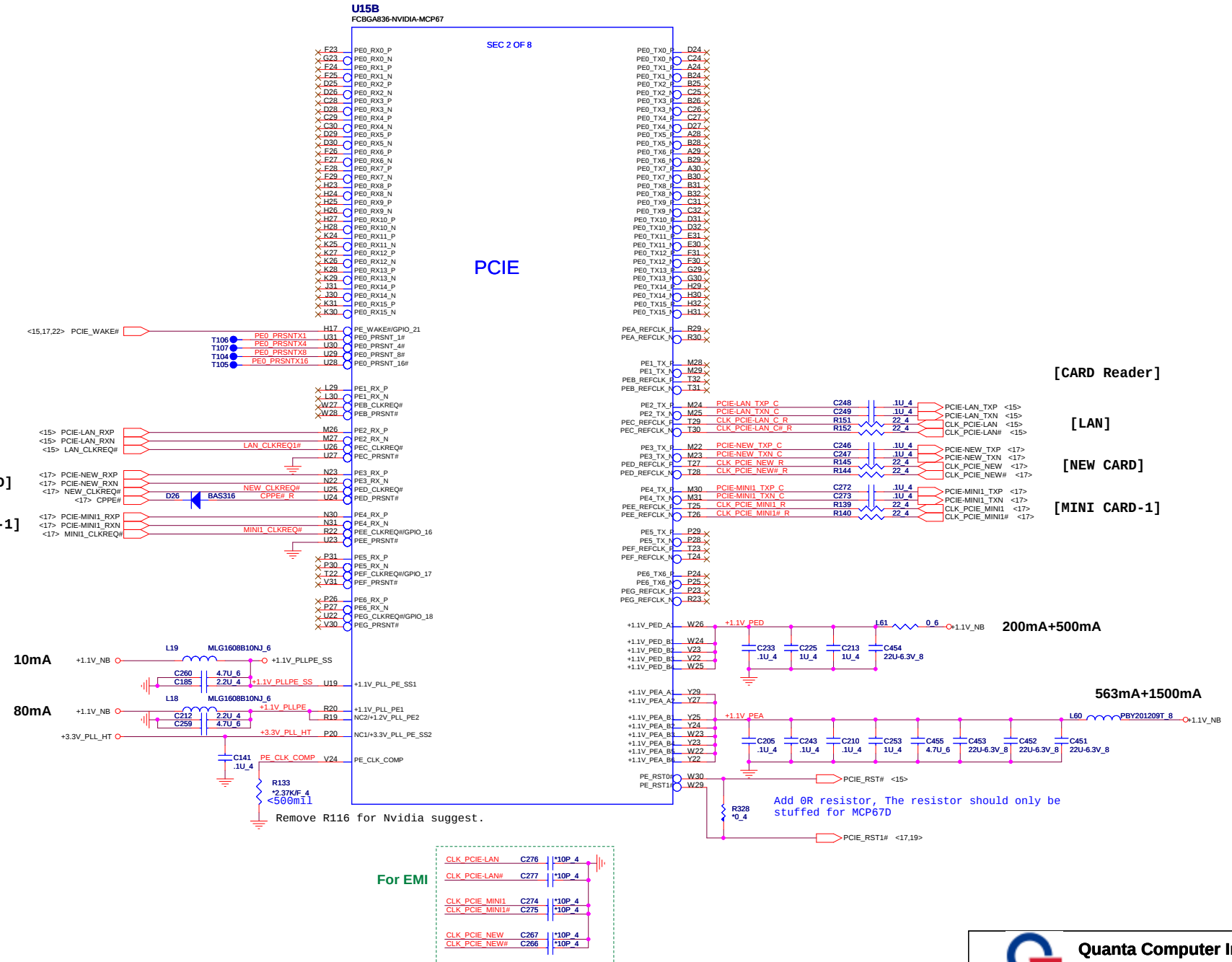
Athlon 64 S1g2 SOCKET_638_PIN
Athlon 64 S1g2
Processor Socket
SOCKET 638 PIN

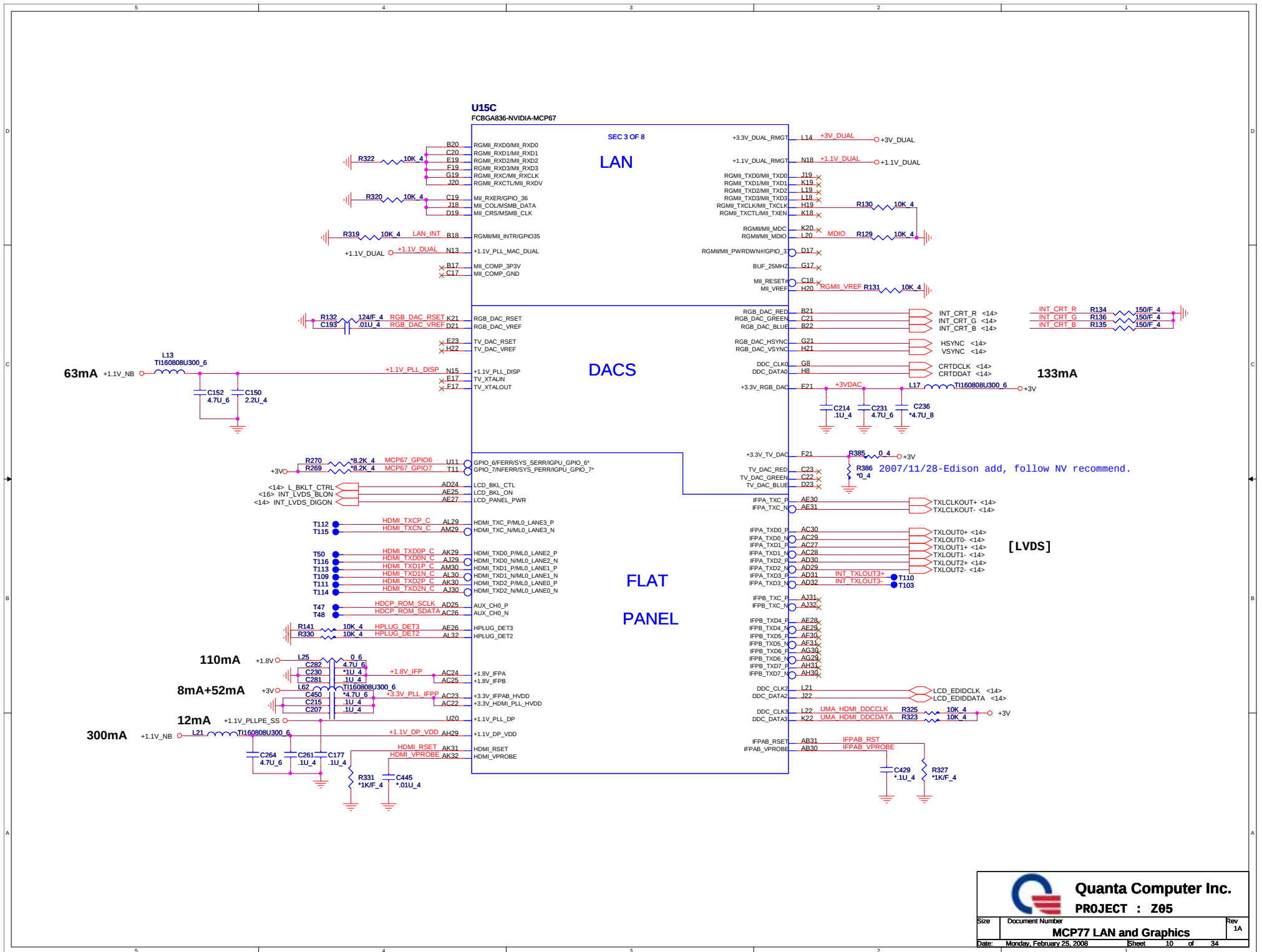


DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE







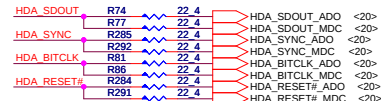


U15F
FCBGA836-NVIDIA-MCP67

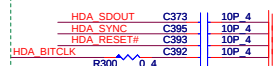
HDA

MISC

HDA

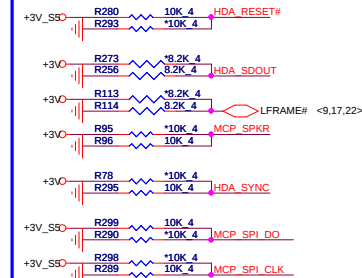


EMI Solution



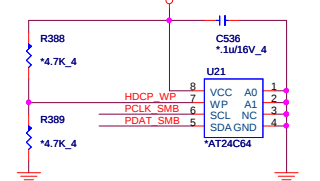
MCP77 STRAPPING

HDA_RESET# (LAN)	0	MI
HDA_RESET# (LAN)	1	RGMI (DEFAULT)
HDA_SDOUT_B (LFRAM# (BIOS)	0	LPC (DEFAULT)
HDA_SDOUT_B (LFRAM# (BIOS)	01	PCI BIOS
HDA_SDOUT_B (LFRAM# (BIOS)	10	SPI BIOS
HDA_SDOUT_B (LFRAM# (BIOS)	11	RESERVED (SPI)
MCP_SPKR (Boot MODE)	0	USER TABLE (DEFAULT)
MCP_SPKR (Boot MODE)	1	SAFE TABLE
HDA_SYNC_R (SIO CLOCK)	0	14.318MHz (DEFAULT)
HDA_SYNC_R (SIO CLOCK)	01	12MHz
HDA_SYNC_R (SIO CLOCK)	10	25MHz
HDA_SYNC_R (SIO CLOCK)	11	1MHz

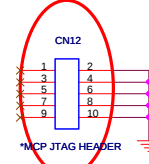


Acer Suggest Reserve HDCP EEPROM 2007/12/05

HDCP EEPROM

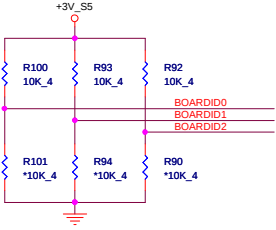
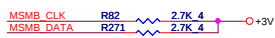


NO PN



M/B ID for 14"/17"

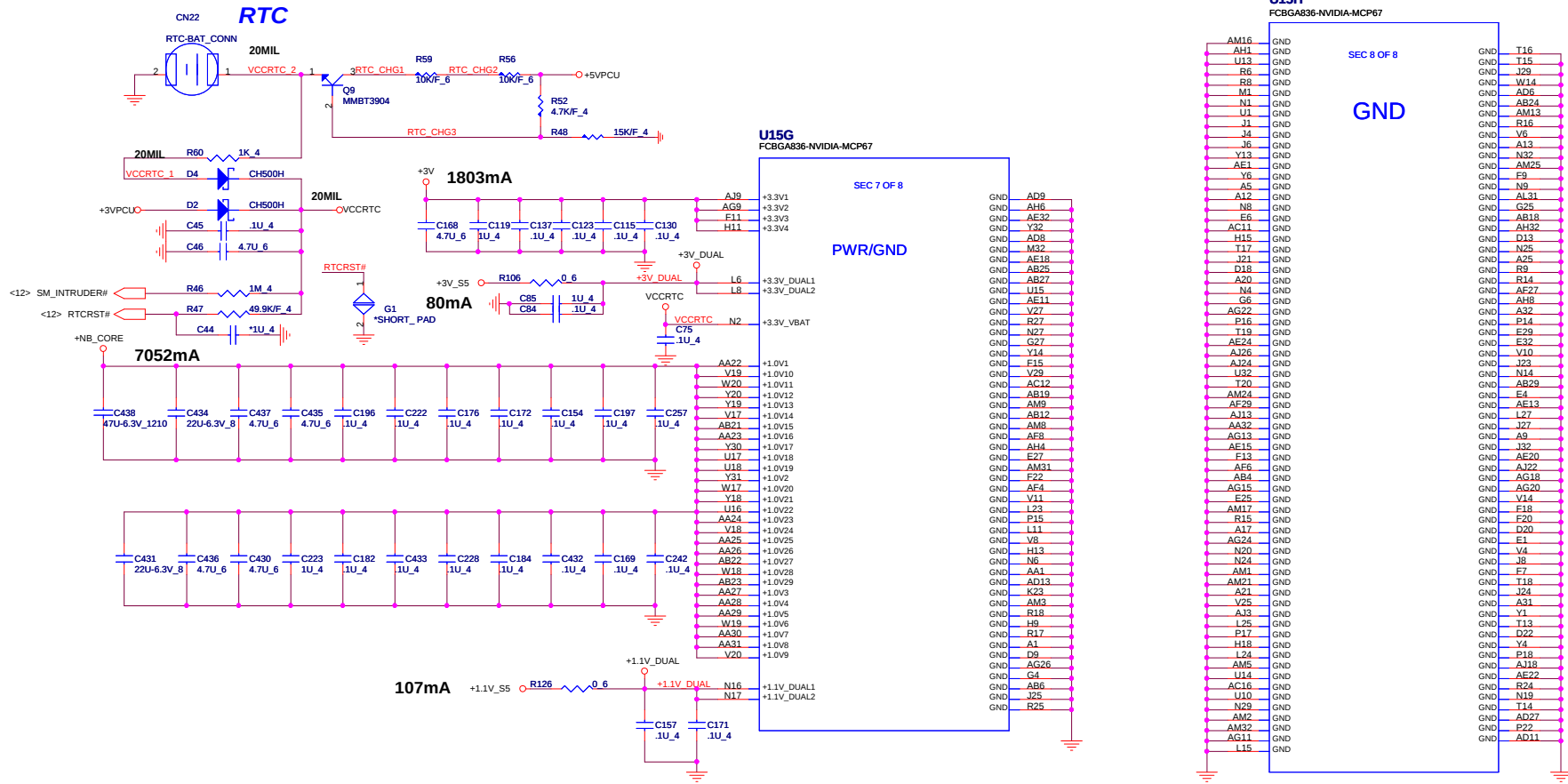
ID0	ID1	ID2	M/B
0	0	0	17" D
0	0	1	X
0	1	0	15" D
1	0	0	15" U
1	0	1	14" Dual Core CPU & MXM
1	1	0	14" Dual Core CPU & UMA
1	1	1	14" Single Core CPU & UMA



Delay 10ms
after S5 powerOK

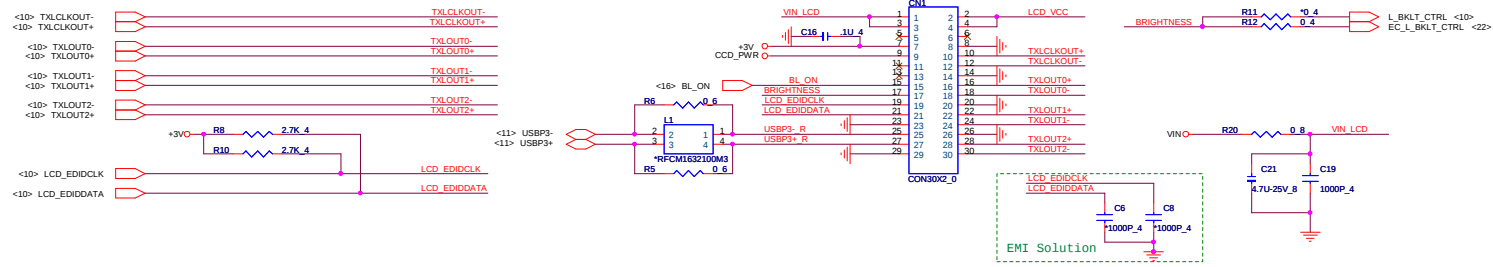
2007/11/28-Edison: Removethese part
R315, R317, R326, R324, C423, Q28, Q29

MCP77 POWER PLANE/GND & BYPASS

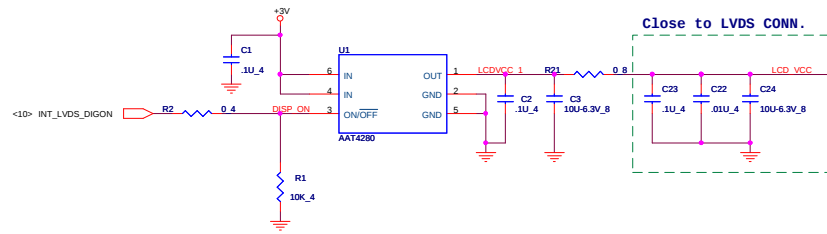


LVDS

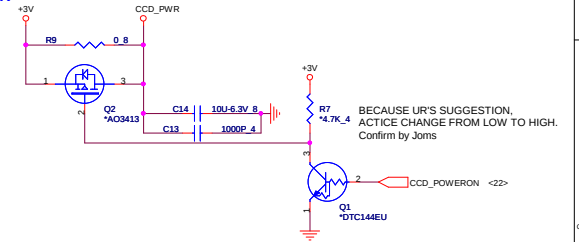
SINGLE_CH



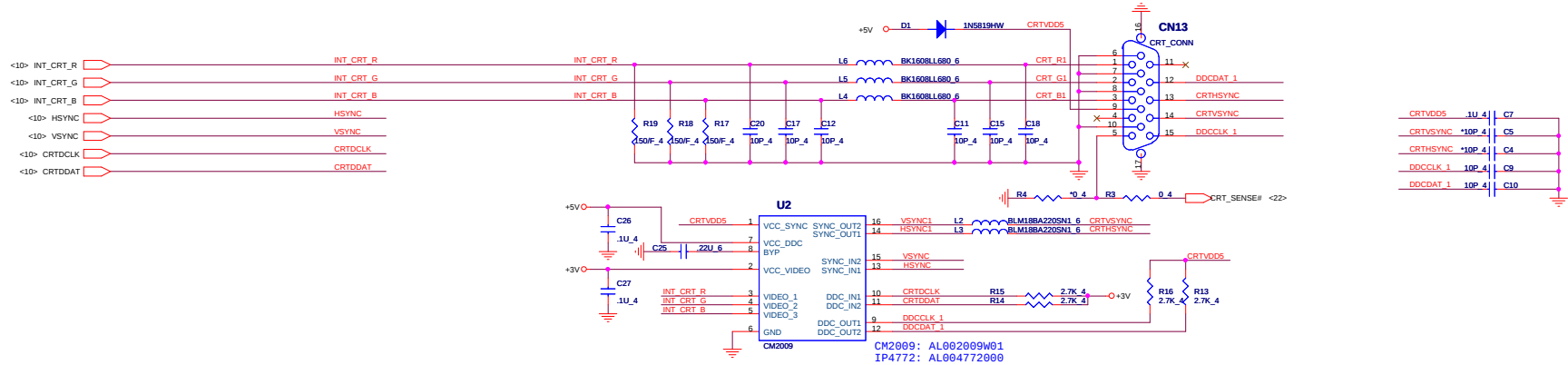
LCD POWER



CAMERA MODULE POWER



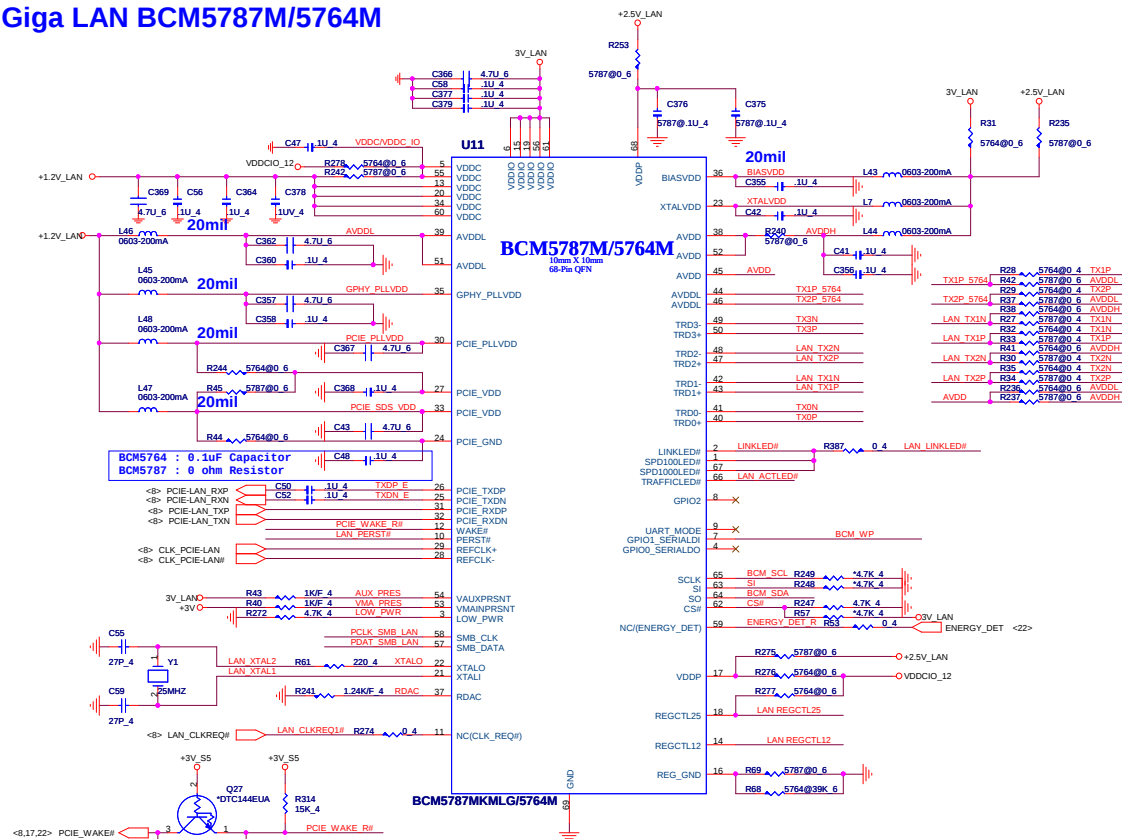
CRT



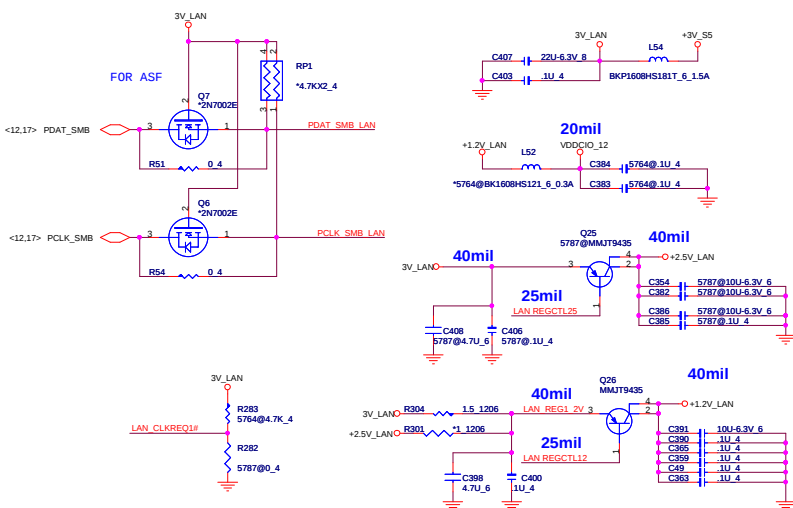
TV Out (SVHS) MiniDIN 7-pin

Delete TVOUT MiniDIN

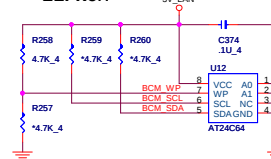
Giga LAN BCM5787M/5764M



LAN POWER



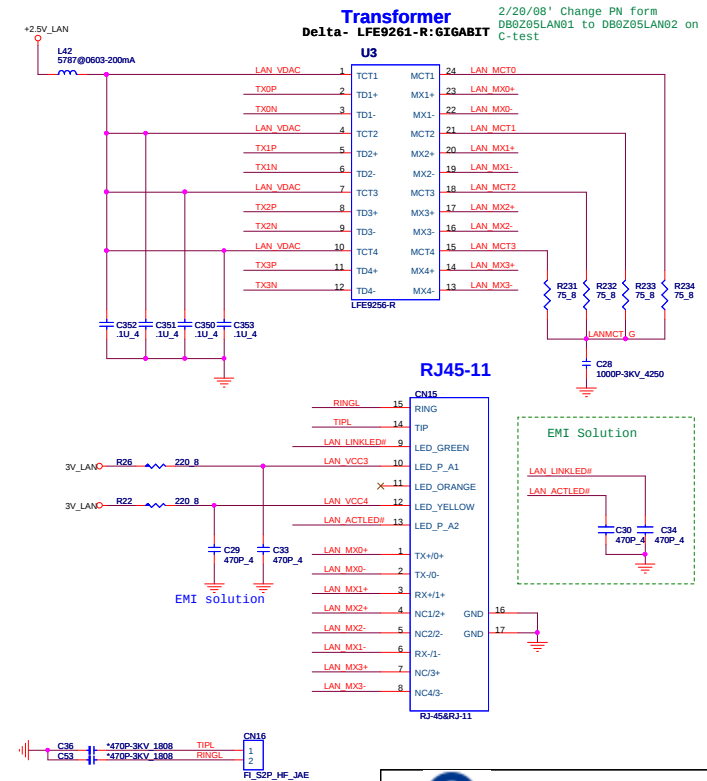
EEPROM



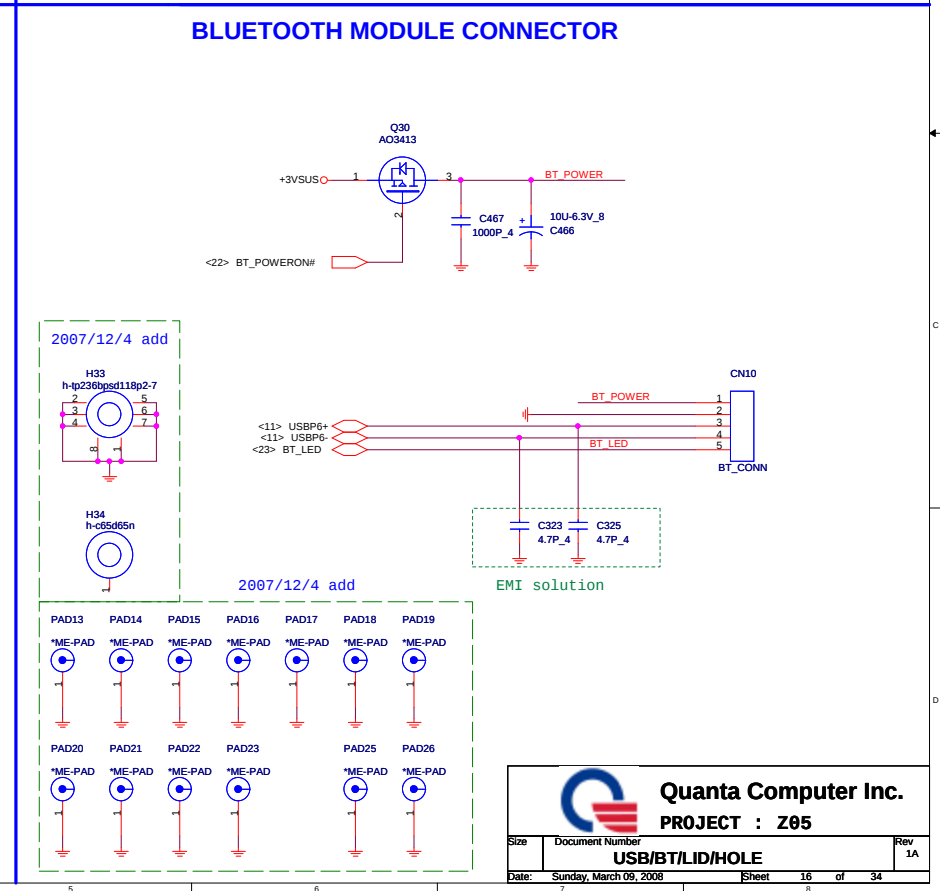
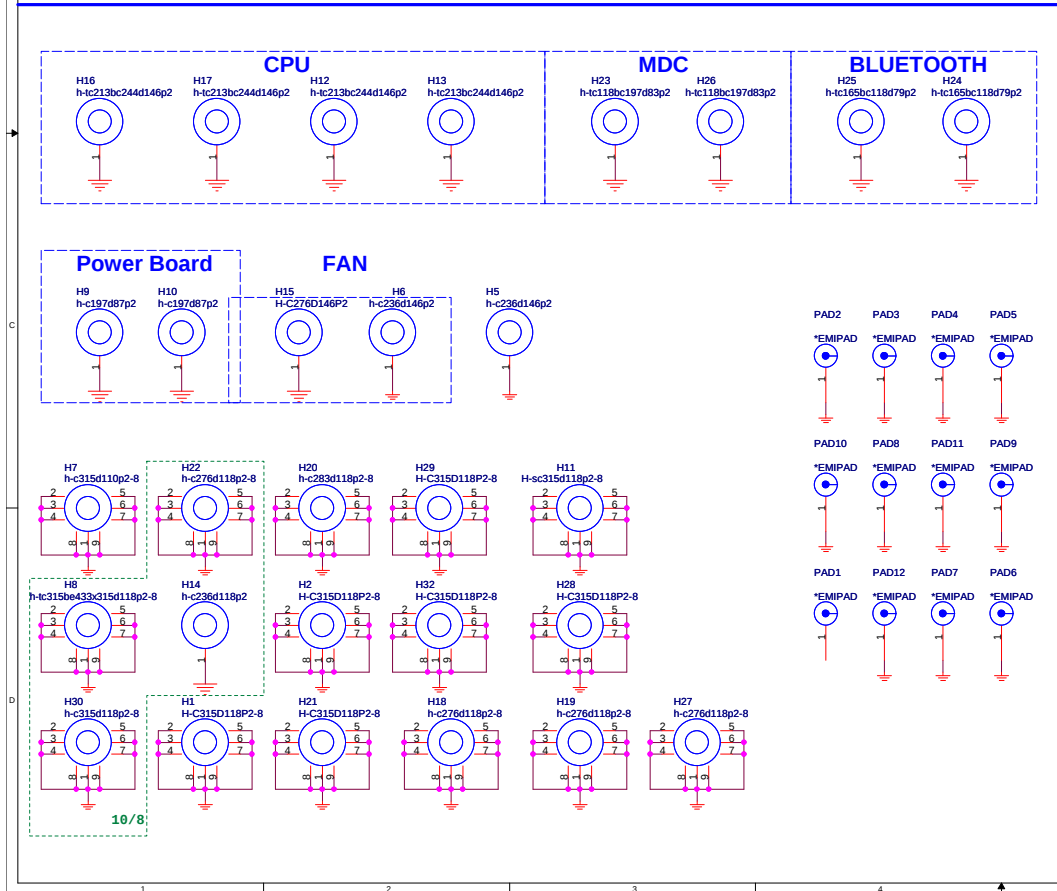
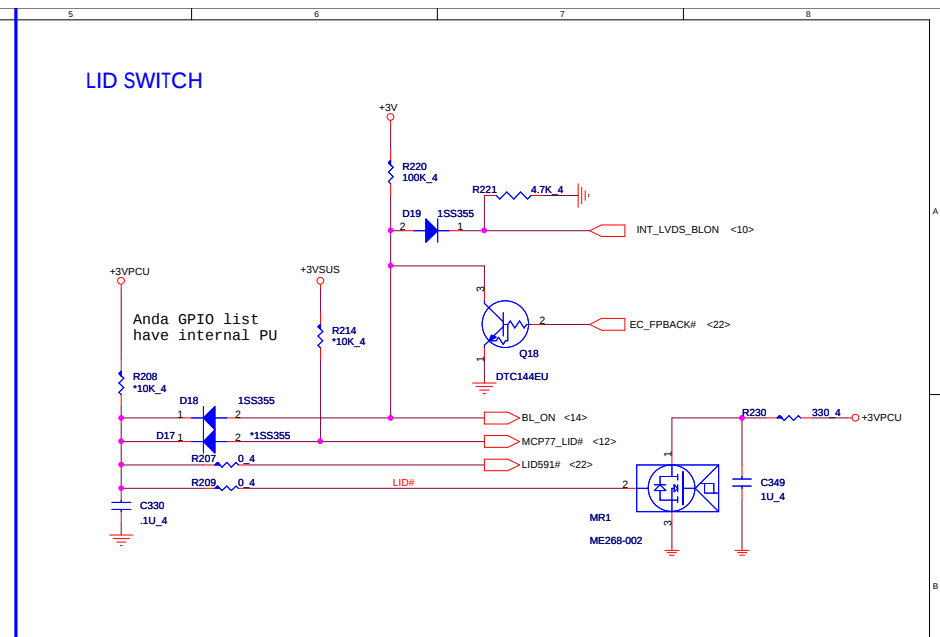
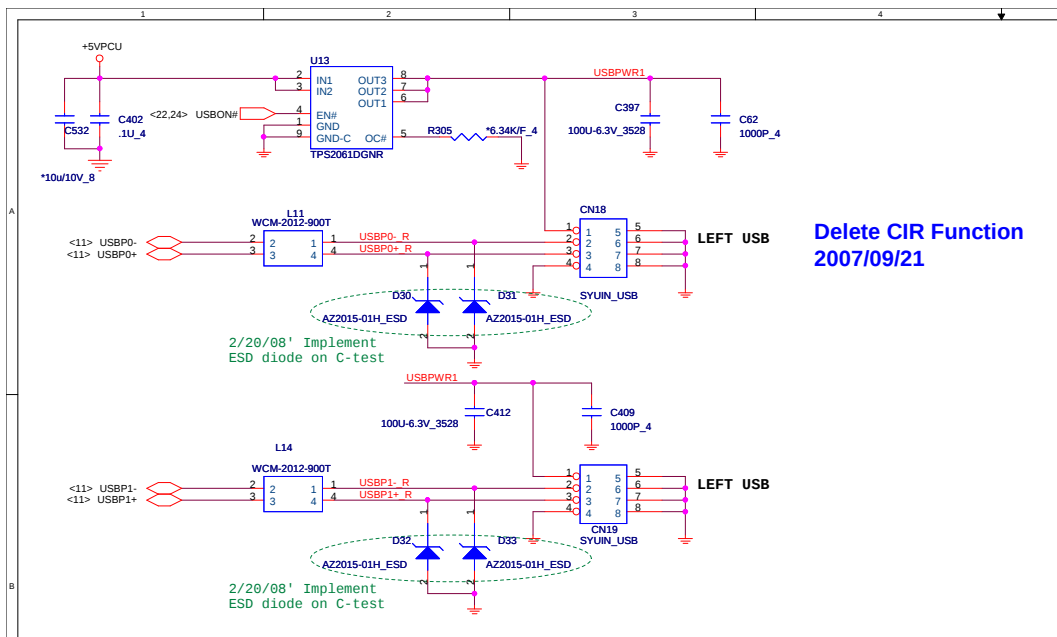
EEPROM Strapping

	SO	SI	CS#	SCLK
24c64	1	1	0	1

Delete LAN within DOCK Selector

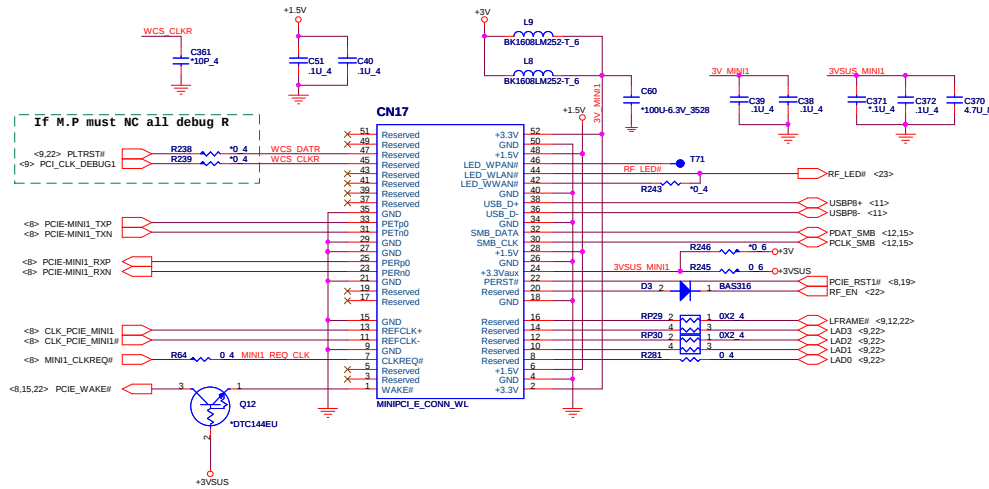


 Quanta Computer Inc. PROJECT : Z05		
Size	Document Number	Rev
	GigaLAN BCM5787/RJ45 & RJ11	1A
Date:	Friday, March 07, 2008	Sheet 15 of 34

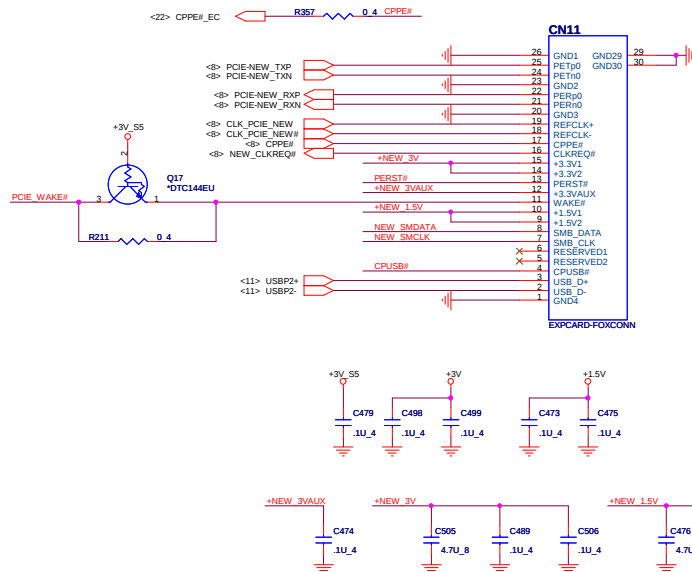


MINI-Card

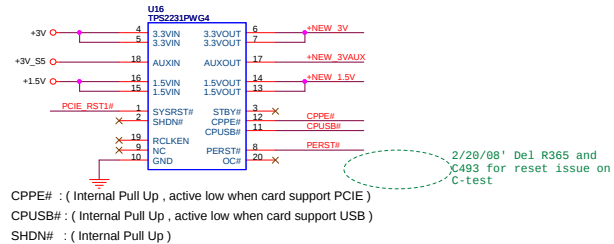
MINI-Card Port-1



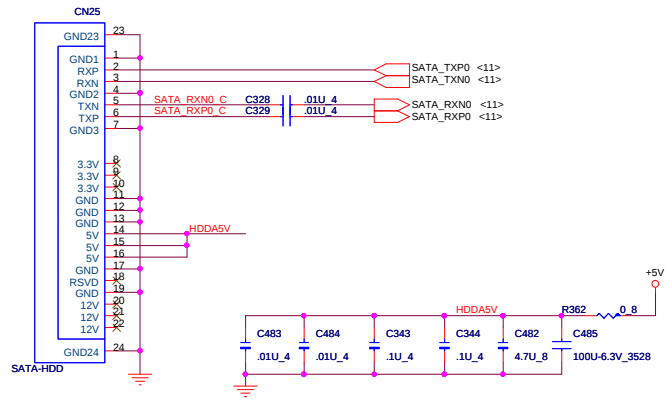
New card



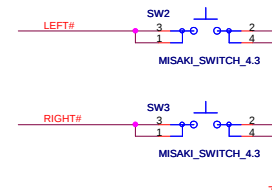
NEW CARD'S POWER SWITCH



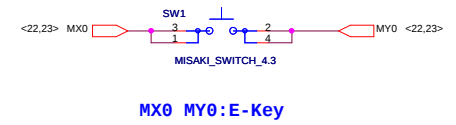
SATA HDD



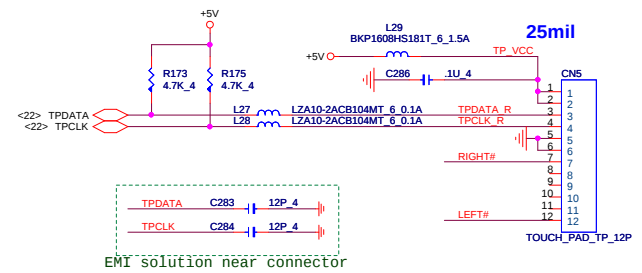
TP SWITCH



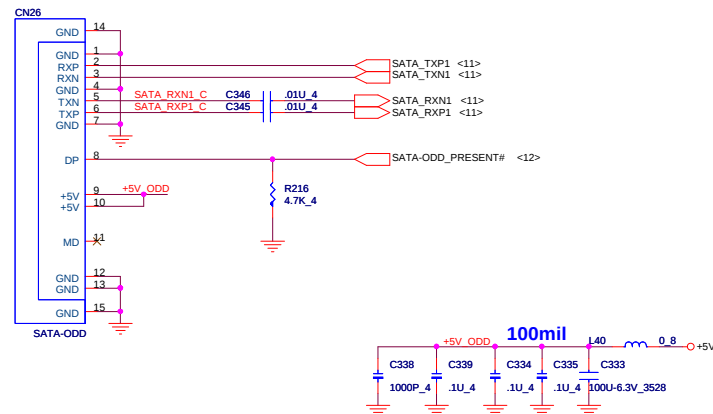
E-KEY

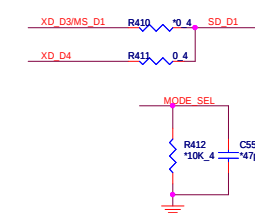
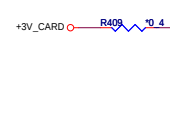
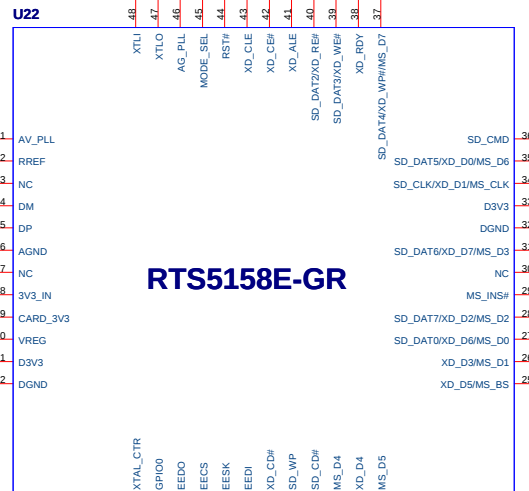
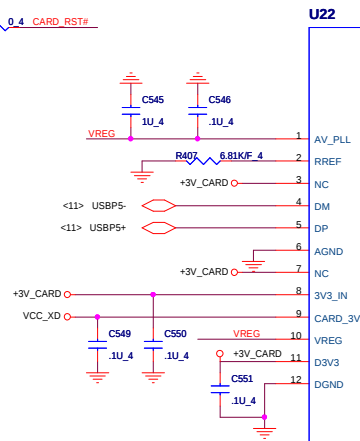
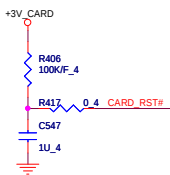
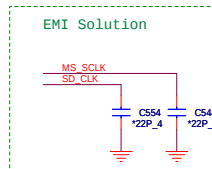
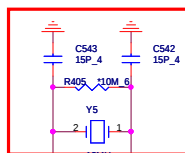
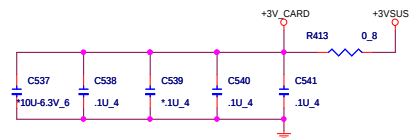


TP CONN



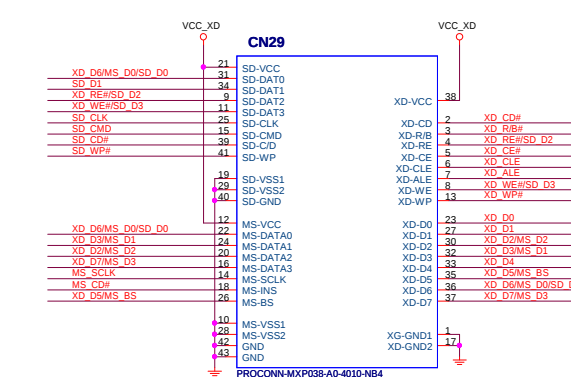
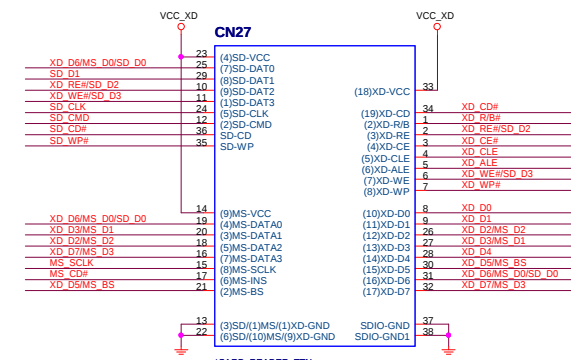
ODD (SATA)



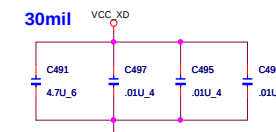


R412/C553 = 10K/47pF => R410 Reside
R412/C553 = NC / NC => R411 Reside

7 IN 1 CARD READER



CARDREADER POWER



[illegible]

$V_0 = 1.2 \cdot (R_{371} + R_{372}) / R_{371} = 4.8V$

AGC Attack (4 pin)	Attack time
LOW	1 ms
Hi	2 ms

AGC ON/OFF selection

AGC ON/OFF (6 pin)	AGC ON/OFF
LOW	ON
Hi	OFF

AGC Recovery1 (10 pin)	AGC Recovery2 (11 pin)	Recovery Time
LOW	LOW	1.0 s
LOW	Hi	2.0 s
Hi	LOW	4.0 s
Hi	Hi	8.0 s

AGC Lv1 (2 pin)	AGC Lv2 (3 pin)	AGC ON Level	Output Po (RL=8 ohm)
LOW	LOW	9.8 dBV	1.2 W
LOW	Hi	9.0 dBV	1.0 W
Hi	LOW	8.1 dBV	0.8 W
Hi	Hi	6.0 dBV	0.5 W

[illegible]

SPEAKER M195

1 25
2 25
3 25
4 25
5 25
6 25

INSPKR- L31 BK1608LL121 6 0.15A INSPKR-N
INSPKR- L32 BK1608LL121 6 0.15A INSPKR-N
INSPKR+ L33 BK1608LL121 6 0.15A INSPKR+N
INSPKR+ L35 BK1608LL121 6 0.15A INSPKR+N

C301 *47P_4
C287 *47P_4
C290 *47P_4
C289 *47P_4

C31 .10U_4

ADOGND

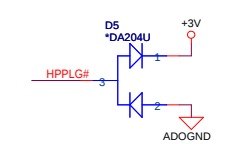
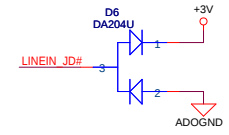
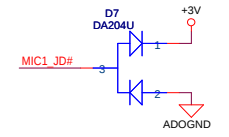
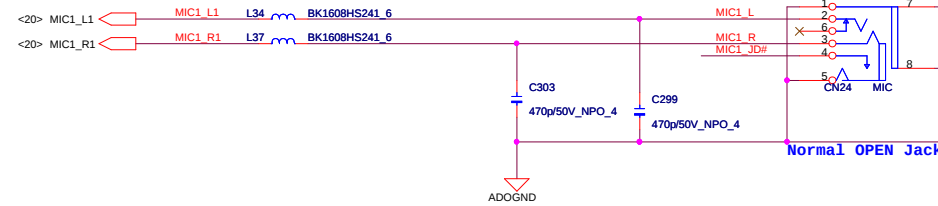
SP STBY1 (33 pin)	SP STBY2 (34 pin)	SP STBY ON/OFF
LOW	LOW	ON
LOW	Hi	OFF
Hi	LOW	OFF
Hi	Hi	OFF

HP STBY1 (35 pin)	HP STBY2 (36 pin)	HP STBY ON/OFF
LOW	LOW	ON
LOW	Hi	OFF
Hi	LOW	OFF
Hi	Hi	OFF

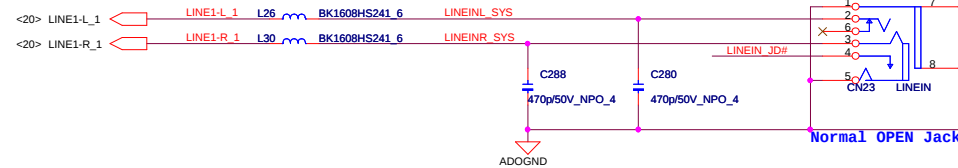
[illegible]

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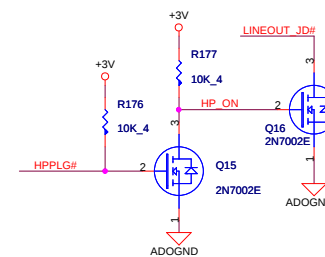
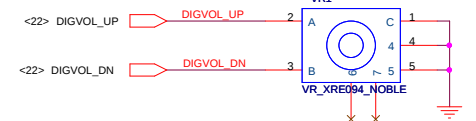
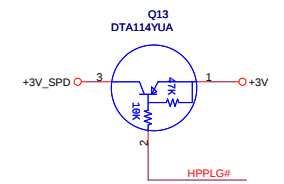
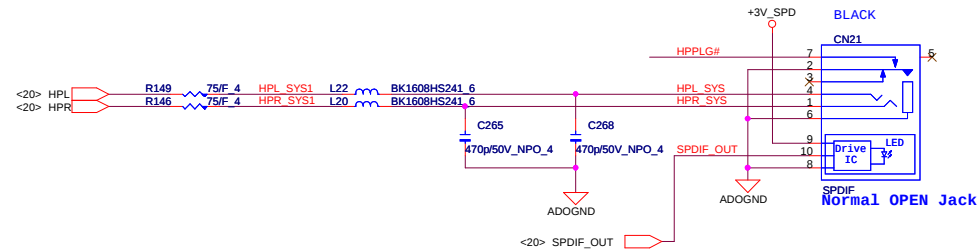
MIC



LINE IN

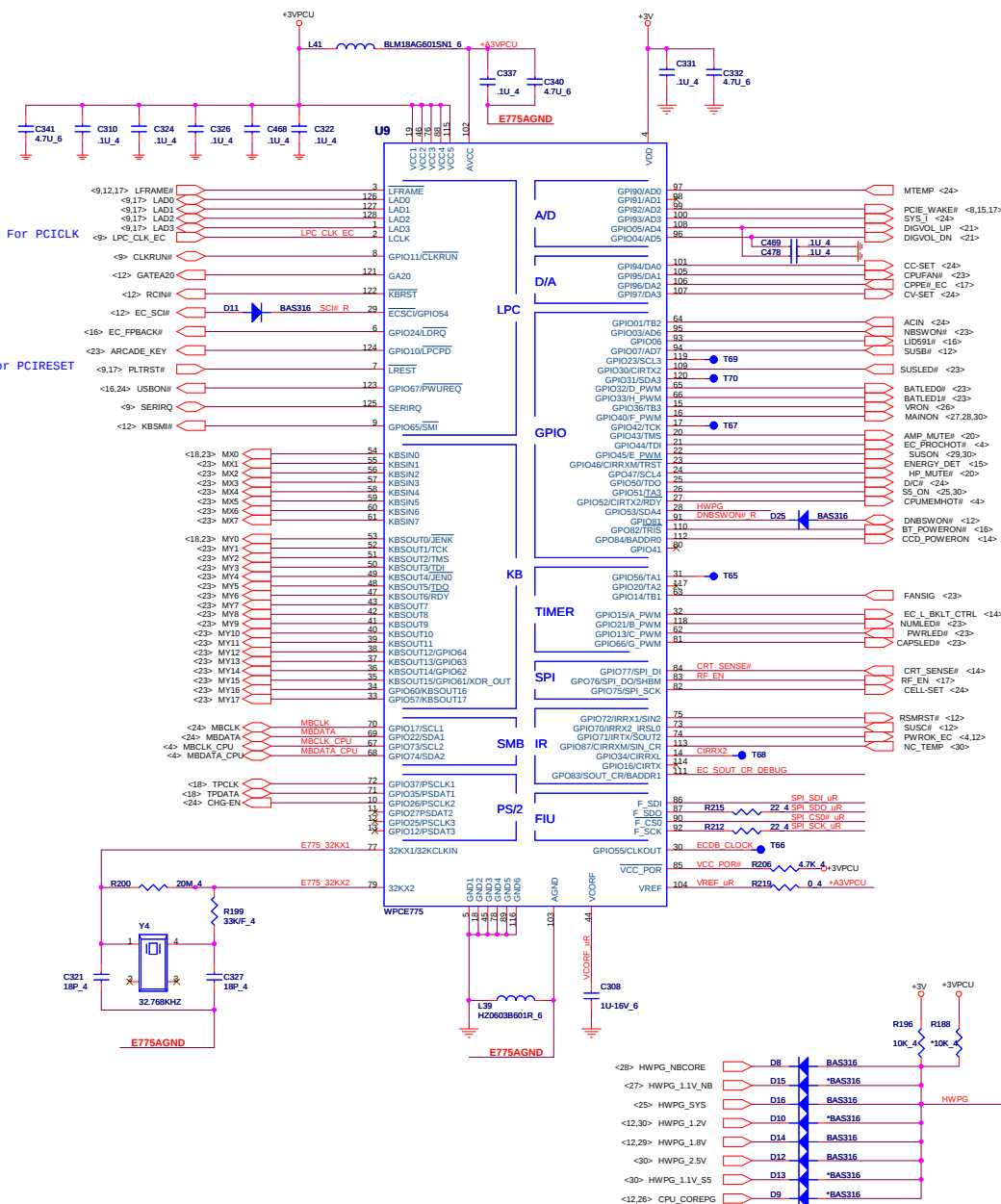


HeadPhone OUT/SPDIF



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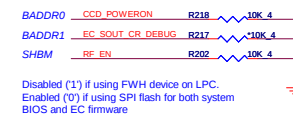
WPCE775C



I/O ADDRESS SETTING

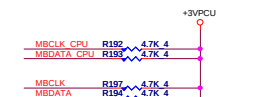
I/O Address	
BADDR1-0	Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

SHBM=0: Enable shared memory with host BIOS

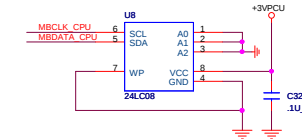


Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system
BIOS and EC firmware

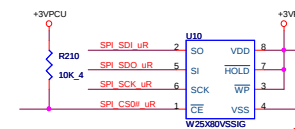
SMBUS PULL-UP



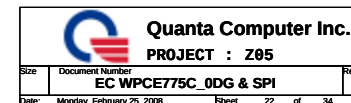
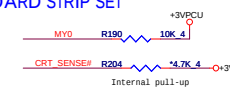
ACER ID



SPI FLASH



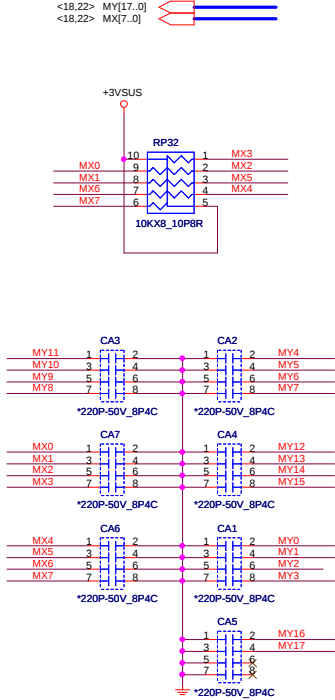
INTERNAL KEYBOARD STRIP SET



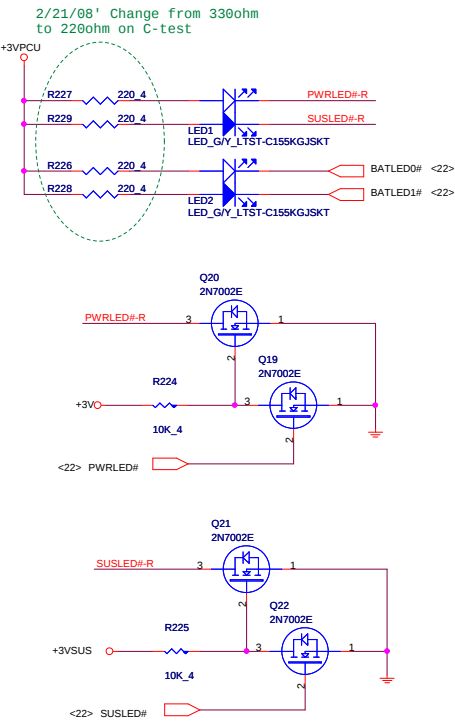
INT K/B

CN4	
1	MY0
2	MY1
3	MY2
4	MY3
5	MY4
6	MY5
7	MY6
8	MY7
9	MY8
10	MY9
11	MY10
12	MY11
13	MY12
14	MY13
15	MY14
16	MY15
17	MY16
18	MX7
19	MX6
20	MX5
21	MX4
22	MX3
23	MX2
24	MX1
25	MX0
26	

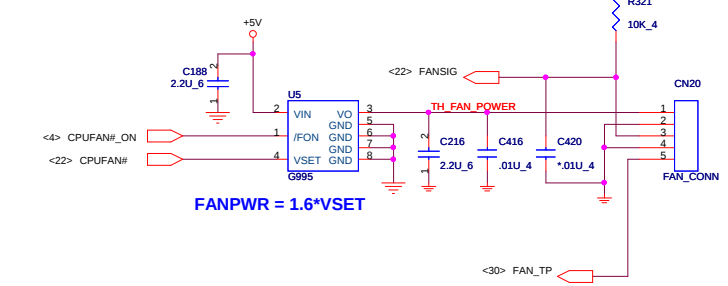
FFC_26P_KB



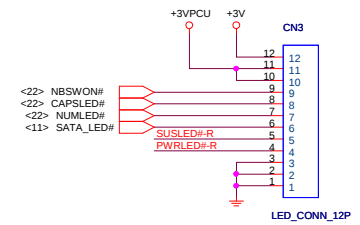
LED



CPU FAN



LED BOARD CONN.



Debug

Delete Debug Port(PCI & IDE)

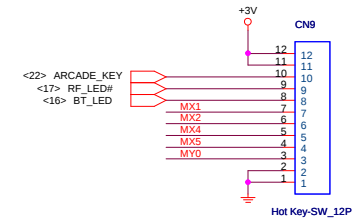
Fingerprint BOARD CONN.

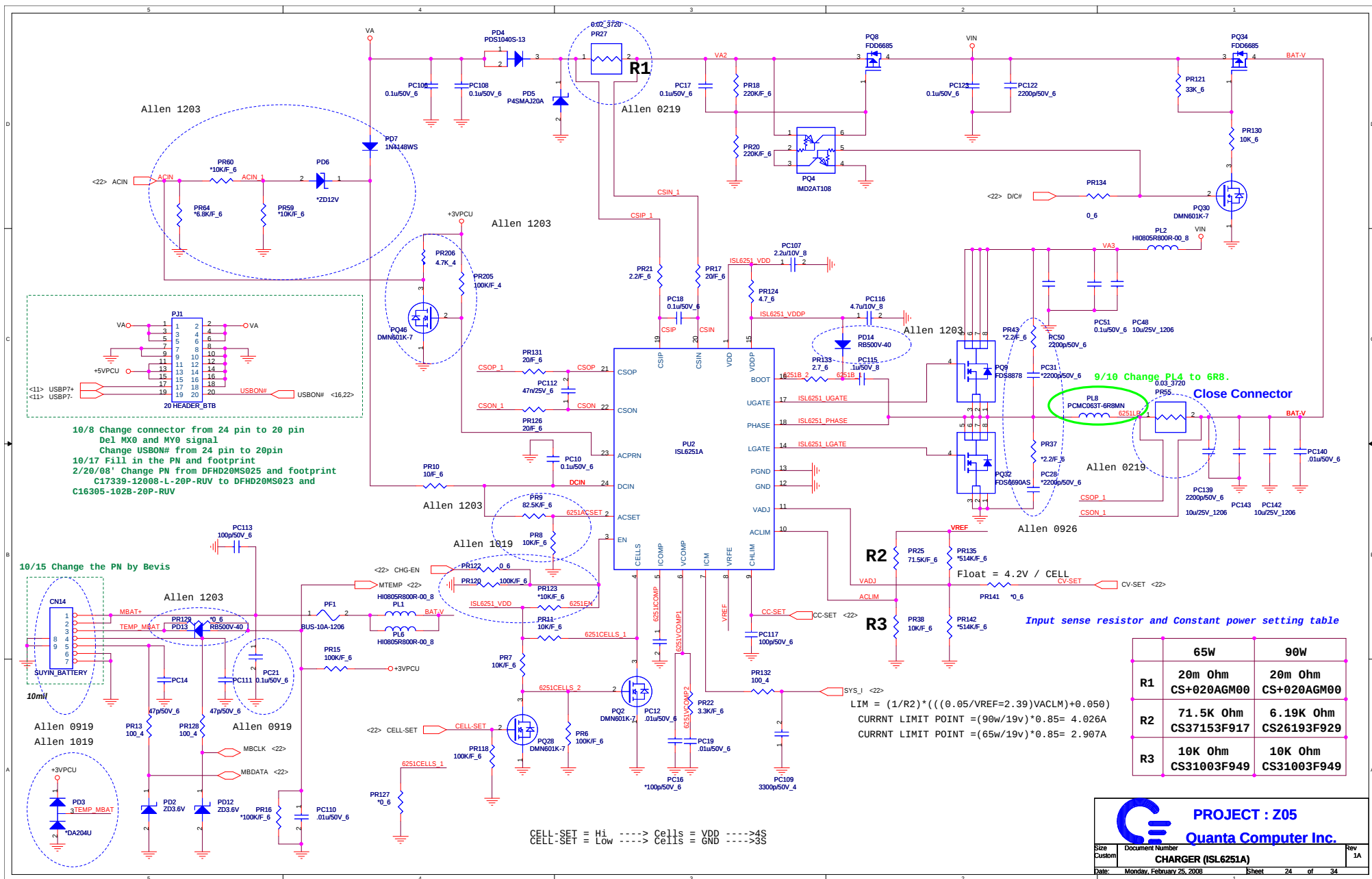


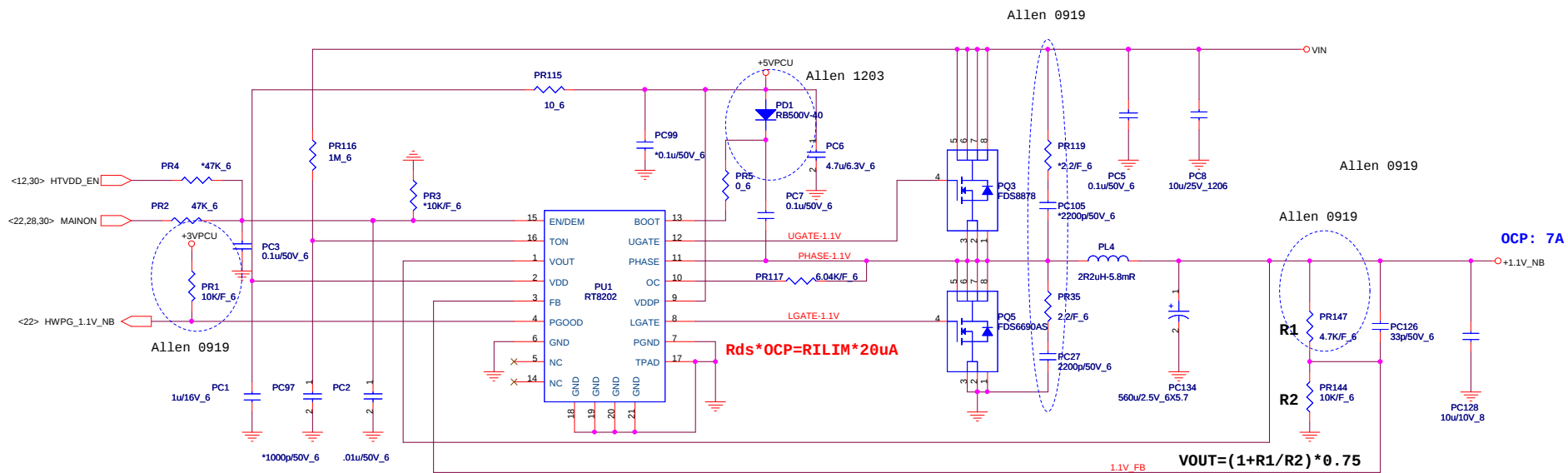
Button BOARD CONN.

BUTTON MATRIX

	MY0
MX1	MAIL
MX2	WWW
MX4	WIRELESS
MX5	BLUETOOTH







$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

$$FDS6690AS \ R_{ds} = 12 \sim 15m\Omega$$

$$OCP = 7 - 0.8A$$

$$L(ripple \ current) = (19 - 1) * 1 / (2.2u * 272k * 19) \sim 1.58A$$

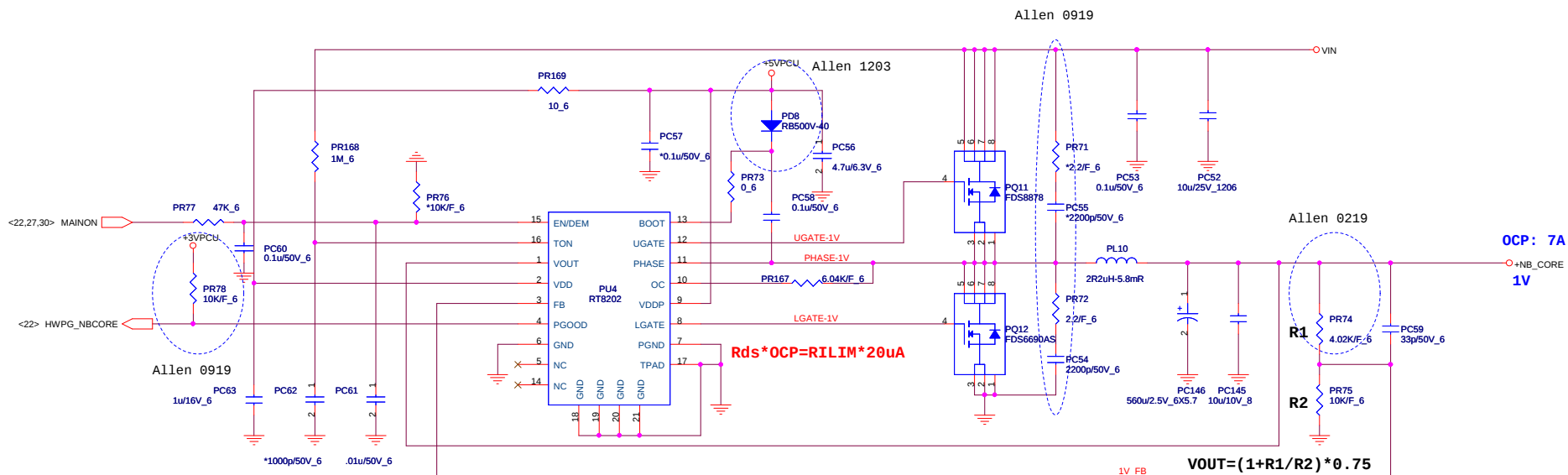
$$12m * 6 = RILIM * 20\mu A$$

$$RILIM = 3.6K (2.5 \sim 8K)$$



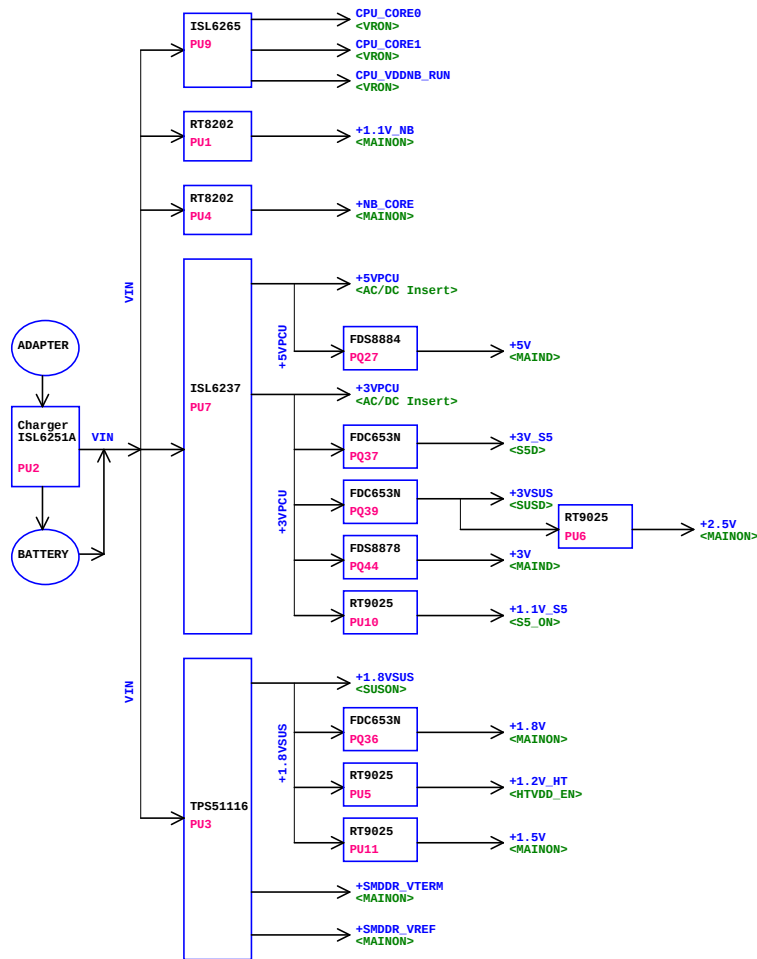
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1. +1.1V_S5MCP77M Power(+1.1V_DUAL)
2. +5VPCUPower IC VCC, USB PORT POWER(S3 control)
3. +5VAudio, FAN, Touch pad, SATA HDD, ODD, CRT
4. +3V_S5MCP77M, New Card, LAN Power
5. +3VPCUKBC WPCE755C, SPI ROM, LED, LID Switch, Fingerprint Module
6. +3VSUSBluetooth, Mini Card, MDC
7. +3VCPU Thermal Sense, MCP77M, System Memory, LCD Panel, PC Camera, Mini card, New Card, Audio, Codec, Card Reader, KBC WPCE775C, LED
8. +2.5VPCU VDDA
9. +3V_LANLAN Power(BCM5764M)
10. +1.2V_LANLAN Power(BCM5764M)
11. +2.5V_LANLAN Power(BCM5787M)
12. +1.5VMini Card, New Card
13. +1.8VSUSCPU VDD I/O, System Memory
14. SMDDR_VTEMCPU Memory Interface , SYSTEM DDR DIMM Memory Termination
15. +1.8VMCP77M LCD Interface
16. +1.1V_NBMCP77M (HT Interface, PCI-E Interface, I/O Power, SATA Interface)
17. +NB_COREMCP77M Core Power
18. +1.2V_HTCPU HT Power
19. CPU_CORE0 CPU Power
20. CPU_CORE1 CPU Power
21. CPU_VDDNB_RUNCPU NB Power
- 22.