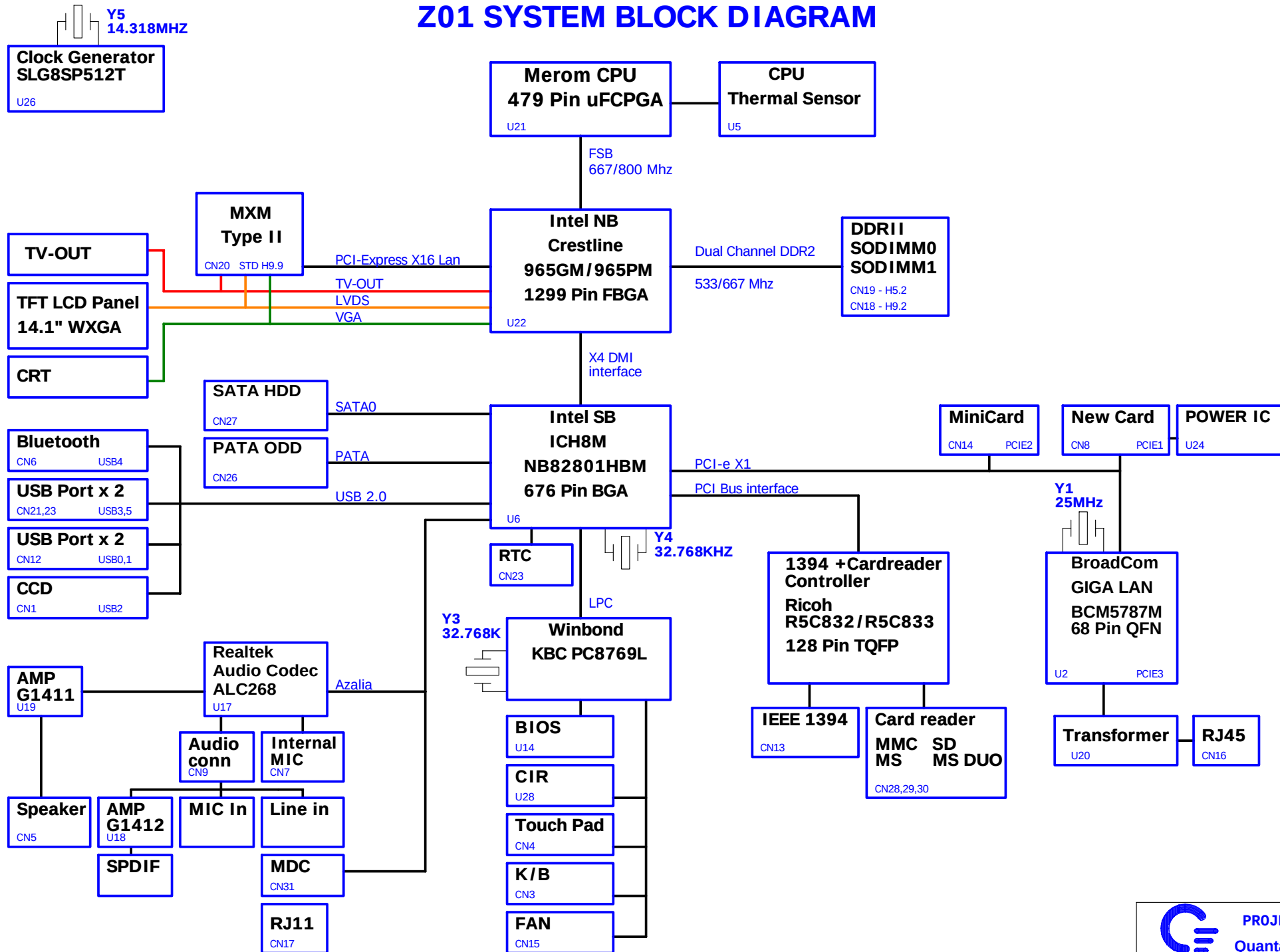


MODEL :	REV:	CHANGE LIST:	MODEL : Z01 MB			
Z01 MotherBoard	1A	FIRST RELEASE	PAGE	FROM	TO	
	1B	PAGE02. 1. R447 455 456 MODIFY to EP P/N:CS14752FB11 PAGE03. 1. STUFF HOLE6 P/N:FBZ01007010 2. STUFF HOLE7 8 15 P/N:FBED8001016 , 3. STUFF HOLE5 P/N:FBZ01006010 PAGE03. 1. STUFF HOLE23 25 P/N:FBZ01003010 2. STUFF HOLE18 P/N:FBZ01004010 3. STUFF HOLE31 P/N:FBZ01005010 PAGE05. 1. U22 MODIFY to GM965 P/N:AJ00N120T04 , 2. R193,194 MODIFY to EP P/N:CS03902FB11 PAGE06. 1. R242 MODIFY to EP P/N:CS33002JB23 PAGE08. 1. L52 53 MODIFY to EP P/N:CV01004KN00 PAGE11. 1. R332 MODIFY to EP P/N:CS23243F930 2. U6 MODIFY to ICH8 P/N:AJ00M740T03 PAGE12. 1. R244, R347, R353 MODIFY to EP P/N:CS00004JA40 , 2. L28 MODIFY to P/N:CV-1005MZ01 PAGE13. 1. CN10 MODIFY to CRT P/N:DFDS15FR611 PAGE15. 1. R467 MODIFY to EP P/N:CS00004JA40 2. R50 MODIFY to EP P/N:CS31003J941, 3. CN27 MODIFY to SATA P/N:DFHS22FR005 PAGE16. 1. CN16 MODIFY to RJ45/11 P/N:DFJJ15FR057 PAGE18. 1. R317, 323 MODIFY to 0603 P/N:CS31003F949 , 2. R310 MODIFY to EP P/N:CS31003J941 PAGE20. 1. PR100 MODIFY to EP P/N:CS51002FB11 PAGE21. 1. PR86 MODIFY to EP P/N:CS24022FB13 , 2. PR38 82 MODIFY to 1% P/N:CS31002FB26 , 3. PR83 MODIFY to EP P/N:CS00004JA40 PAGE22. 1. PR1 MODIFY to EP P/N:CS32002FB29 , 2. PR6 MODIFY to 1% P/N:CS51003F934 PAGE23. 1. PR106 MODIFY to 0 ohm P/N:CS00002JB38 2. UN-STUFF PR107, PC111 PAGE24. 1. PR29 MODIFY to EP P/N:CS31003J941 2. PJ1 MODIFY to BATTERY P/N:DFHD07MR006 PAGE25. 1. PR70 MODIFY to EP P/N:CS32002FB29	1	1A		
	2A	PAGE02. 1. Connect VDDIO CLK to +1.25V 2. un-stuff R292;R445;R308 3. stuff C575,C574,C576,C578,C573,C546 for EMI issue PAGE06. 1. Connect ICH PWROK SIGNAL TO NB CLPWROK 2.un-stuff R242;R235;R422;R222;R421;R423 3. R360,R361 only stuff for UMA PAGE07. 1. MODIFY 22u to 10u PAGE08. 1. R489 MODIFY to 0805 2. Stuff L50;R182;C238 for EV@ (MXM) PAGE09. 1. Add PU for SMA MA14 1. SMB MA14 PAGE10. 1. un-stuff R337,C115,C127,C129,C298,C302,C294,C283,C291 PAGE11. 1. Q18 MODIFY to P/N:AL07S204C27 2. R395 connect to VCCRTC 3. R336;R251;R419;R255 un-stuff 4. R226 connect to +3V S5 5. ICH PWROK to SB CLPWROK PAGE11. 1. stuff C500, C509, C300, C513 33pF P/N:CH03306JB04 2. C507, C508 10pF change to 15pF P/N:CH01506JB06 , 3. stuff R238, R392, C2989 for Contr-LINK1 PAGE12. 1. VCCDA & VCCSUSHA change to 3V PAGE13. 1. ADD CRT DDC IN PU 2. L8, L9, L10 P/N change to 0.47UH for MXM , 3. C22, C24, C25, C27, C31, C32 P/N change to 47pF for MXM PAGE14. 1. CN6 MODIFY CONN. to 5 PIN P/N:DFHD05MR098 PAGE15. 1. MODIFY SWITCH BOARD PIN DEFINE 2. Modify FAN circuit 2. MR1 P/N change to AL000268000 PAGE16. 1. C46, C47 27pF change to 33pF P/N:CH03306JB04 2. stuff C104, C105, C119, C112 0.1uF P/N:CH41003ZB35 PAGE17. 1. CARD READER COLAY to CN28, DEL CN30 2. C311 change to 27pF P/N:CH02706JB06 3. stuff R209 4. un-stff R213, C325, U11 PAGE18. 1. CHANGE MDC & CODEC to 3V 2. Delete D12 3. stuff R314, R483, C393, C595 PAGE19. 1. SWAP NBSWON# & ACIN 2. C363, C364 5.6pF change to 18pF P/N:CH01806JB07 PAGE20. 1. Modify PQ19 P/N PAGE21. 1. Modify Capacitor P/N to meet ME height limit PAGE22. 1. stuff PR74, PC69 2. Remove JP Pad PAGE23. 1. stuff PR126, PC131, PC137 2. Remove JP Pad 3. un-stuff +1.8V PAGE25. 1. un-stuff PR101, PQ21, PR22, PQ2, PR26, PR9, PR5, PC33, PC38, PC39, PC19, PC22, PU2	10	3A	3B	
	2B	PAGE02. 1. Change R293 to 2.2K for meet Intel Design checklist PAGE03. 1. Change XDP PU/PD resistors value to meet Intel Design checklist PAGE04. 1. Un-stuff C28, C457 PAGE05. 1. Add LVDS VREF strap PAGE06. 1. Add SDVO I2C strap PAGE07. 1. Remove NB resistors to GND PAGE08. 1. Remove DIODE for D27 2. Remove VCCA_DPLLA&B for external VGA PAGE10. 1. Add CRT & LVDS I2C Strap PAGE11. 1. Un-stuff Control Link Vref1 PAGE12. 1. Remove reserve ICH8 HDA 1.5V power rail PAGE13. 1. Modify LCD VCC enable power rail 2. Add LVDS INV I2C Strap PAGE14. 1. Add EMI solution for debug port PCi clock PAGE15. 1. Change Q33, Q34 to MOSFET PAGE16. 1. Add PIN 59 & 3 PAGE18. 1. Change CN31 pin2 to +3V_S5 for Modem can't wake up from S3 PAGE19. 1. Add GPIO46 , 47 PAGE20~25. 1. Add EMI solution 2. Update Power component P/N	21	3A		
	3A	PAGE10. 1. Add +2.5V & +1.8V capacitors for nVIDIA MXM card PAGE11. 1. Change C507, C508 to 15pF for RTC PAGE13. 1. Add C609 & C610 to meet CM2009 specification PAGE14. 1. Reserve +5VPCU & Add Q40, R540 for CIR PAGE15. 1. Add C611 for PLC hall IC 2. Stuff R60 for G995 PAGE19. 1. CN24 un-stuff 2. D322, D332 reserve for ESD PAGE21. 1. Modify PC85 value PAGE22. 1. Modify PR4, PC13 value for sequence PAGE23. 1. Add PQ22 for nVIDIA MXM +1.8V PAGE24. 1. Modify PF1 P/N PAGE25. 1. Add PU2 for nVIDIA MXM +2.5V				
	3B	PAGE10. 1. Remove R337 & Add R542, Q41, Q42 for Nvidia ACIN function PAGE13. 1. Add D34~D36, D40 for ESD solution PAGE15. 1. R484, R485, R486 from 330 change to 220 ohm for LED light issue 2. Add D41, D42, D43 for ESD 3. Stuff Q39 PAGE16. 1. Add C621, C622 for EMI solution 2. C112, C119 change to 100pF/50V for EMI PAGE18. 1. Un-Stuff L55 Stuff U16 R470 R471 for internal Mic. issue PAGE19. 1. Modify D32, D33 package to 0402 for ESD PAGE23. 1. Add PR140, PR141 for +1.8V voltage PAGE25. 1. Stuff PR22, PR101, PQ2, PQ21 for nVIDIA MXM +1.8V & +2.5V Discharge				
				10	3A	
				11	2B	
				12	2B	
				13	3A	3B
				14	3A	
				15	3A	3B
				16	3A	3B
				17	2A	
				18	2B	3A
				19	3A	3B
				20	2B	
				21	3A	
				22	3A	
				23	3A	3B
				24	3A	
				25	3A	3B
			</			

Z01 SYSTEM BLOCK DIAGRAM



PCB layout for the REV:B board showing power and clock connections. The top section shows a +3V supply connected to a network of capacitors (C384-C398) and ground planes. A note states "Each Power pin have one 0.1u Capacitor". The bottom section shows a list of clock signals (CLKREQ_A#, CLKREQ_B#, CLKREQ_C#, CLKREQ_D#, CLKREQ_E#) connected to specific pins (R445-R449) and their respective components (475/F, 33 4, 22 4, 33 4, 33 4). A note "REV:B MODIFY" is present next to the clock signal list.

Pin-to-pin connection diagram for the SLG8SP512 device. The diagram shows connections between the device pins (left) and various external components or internal blocks (right).

Left Side (Device Pins):

- 9: U26
- 2: VDD_48
- 16: VDD_PCI
- 39: VDD_PLL3
- 55: VDD_SRC
- 61: VDD_REF
- 55: VDD_CPU
- 12: VDD_96_IO
- 20: VDD_PLL3_IO
- 26: VDD_SRC_IO_1
- 45: VDD_SRC_IO_3
- 36: VDD_SRC_IO_2
- 49: VDD_CPU_IO
- 1: CLKREQ#_R
- 3: C_DB_R
- 4: CM_R
- 1: I_R
- 5: CLK#
- 7: H_R
- 60: XTAL_IN
- 59: XTAL_OUT
- 10: USB_48/FSA
- 57: ELI
- 62: FSB/TEST/MODE
- 62: REF0/FSC/TESTSEL
- 8: VSS_PCI
- 11: VSS_48
- 15: VSS_IO
- 19: VSS_PLL3
- 52: VSS_CPU
- 23: VSS_SRC1
- 29: VSS_SRC2
- 42: VSS_SRC3
- 58: VSS_REF
- 58: CKPWRGD/PWRDNW#

Right Side (External Components/Internal Blocks):

- 48: NC
- 64: SMBCK
- 63: SMBDT
- 38: PM_STPCPU#_11
- 37: PM_STPCPU#_11
- 54: CLK_CPU_BCLK_R
- 53: CLK_CPU_BCLK#_R
- 51: CLK_MCH_BCLK_R
- 50: CLK_MCH_BCLK#_R
- 47: SRC8/ITP
- 46: SRC8#/ITP
- 34: CLK_PCIE_3GPLL_R
- 35: CLK_PCIE_3GPLL#_R
- 32: CLK_MCH_REQ#_R
- 30: NEW_CLKREQ#_R
- 31: CLK_PCIE_NEW_C_R
- 31: CLK_PCIE_NEW_C#_R
- 44: CLK_PCIE_MXM_R
- 43: CLK_PCIE_MXM#_R
- 41: CLK_PCIE_ICH_R
- 40: CLK_PCIE_ICH#_R
- 27: CLK_PCIE_MINI1_R
- 26: CLK_PCIE_MINI1#_R
- 24: CLK_PCIE_LAN_R
- 25: CLK_PCIE_LAN#_R
- 21: CLK_PCIE_SATA_R
- 22: CLK_PCIE_SATA#_R
- 17: DREFSSCLK_R
- 18: DREFSSCLK#_R
- 13: DREFCLK_R
- 14: DREFCLK#_R
- 47: CK_PWRGD_11

Internal Blocks/Components:

- CLOCK_GEN
- SLG8SP512
- PCI_STOP#
- CPU0_STOP#
- CPU0
- CPU1_MCH
- CPU1_MCH#
- SRC8/ITP
- SRC8#/ITP
- SRC10
- SRC10#
- SRC11/CR#_H
- SRC11#/CR#_G
- SRC9
- SRC9#
- SRC7/CR#_F
- SRC7#/CR#_E
- SRC6
- SRC6#
- SRC4
- SRC4#
- SRC3/CR#_C
- SRC3#/CR#_D
- SRC2
- SRC2#
- SRC0/DOT96
- SRC0#/DOT96#
- LCDCCLK/27M
- LCDCCLK#/27M#
- PM_STPCPU#_11
- CLK_CPU_BCLK_3
- CLK_CPU_BCLK#_3
- CLK_MCH_BCLK_5
- CLK_MCH_BCLK#_5
- CLK_PCIE_3GPLL_6
- CLK_PCIE_3GPLL#_6
- CLK_PCIE_NEW_C_14
- CLK_PCIE_NEW_C#_14
- CLK_PCIE_MXM_10
- CLK_PCIE_MXM#_10
- CLK_PCIE_ICH_11
- CLK_PCIE_ICH#_11
- CLK_PCIE_MINI1_14
- CLK_PCIE_MINI1#_14
- CLK_PCIE_LAN_16
- CLK_PCIE_LAN#_16
- CLK_PCIE_SATA_11
- CLK_PCIE_SATA#_11
- DREFSSCLK_6
- DREFSSCLK#_6
- DREFCLK_6
- DREFCLK#_6

The schematic diagram illustrates the SMBus interface circuit. It consists of two identical signal paths, one for PDAT_SMB and one for PCLK_SMB. Each path is driven by a 3V supply through a 4.7K pull-up resistor (R444 and R449 respectively) and a 2N7002 MOSFET (Q29 and Q21 respectively). The MOSFETs are configured as source followers, with their sources connected to ground and their drains connected to the SMBD and SMBCK signals. The input signals PDAT_SMB and PCLK_SMB are connected to the gates of the MOSFETs. The output signals SMBD and SMBCK are connected to the drains of the MOSFETs.

REV:C MODIFY

Signal	Pin	Frequency
PCLK_LPC_DB	C575	22p_4
PCLK_PCM	C574	10p_4
PCLK_591	C576	*10p_4
CLKUSB_48	C573	10p_4
PCLK_ICH	C578	10p_4
14M_ICH	C546	4.7p_4

SILEGO

0 : Pin 13,14 & 17,18 for Internal VGA

1 : 27M & 27M_SS & SRC0 for external VGA

SILEGO
0 : Pin 46,47 as SRC output
1 : Pin 46,47 as CPU output

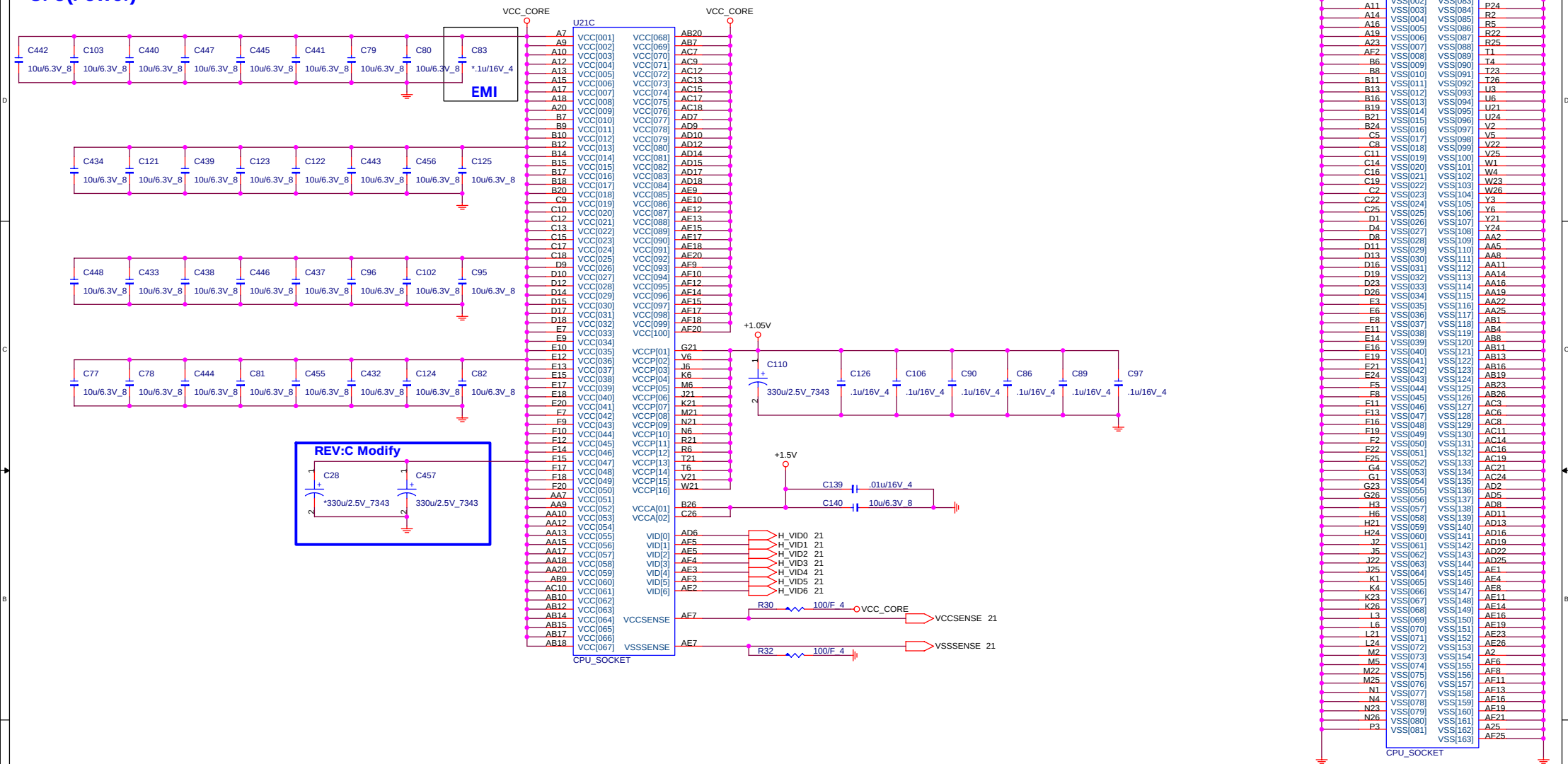
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	0	200Mhz
0	1	1	166Mhz
1	0	0	333Mhz
1	0	1	100Mhz
1	1	0	400Mhz
1	1	1	Reserved



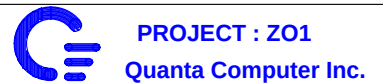
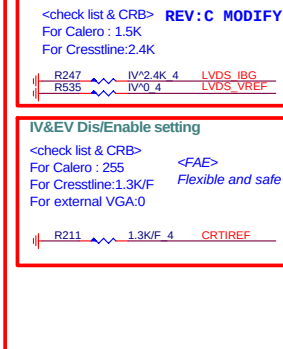
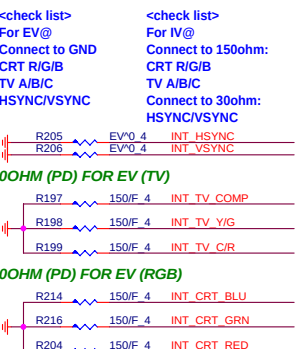
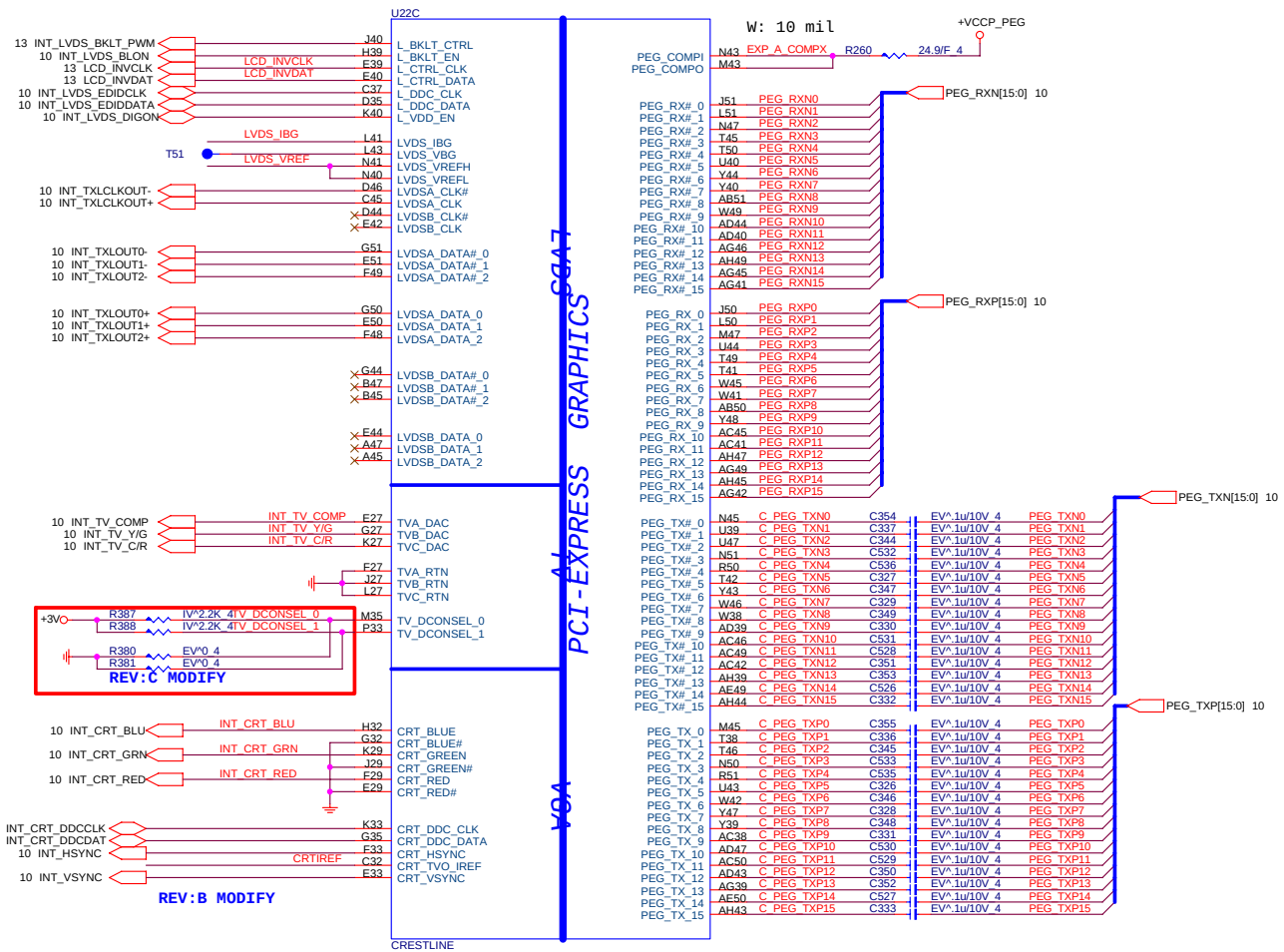
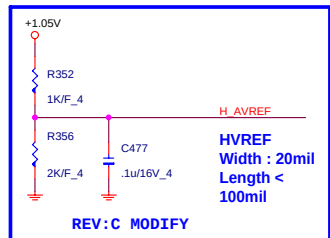
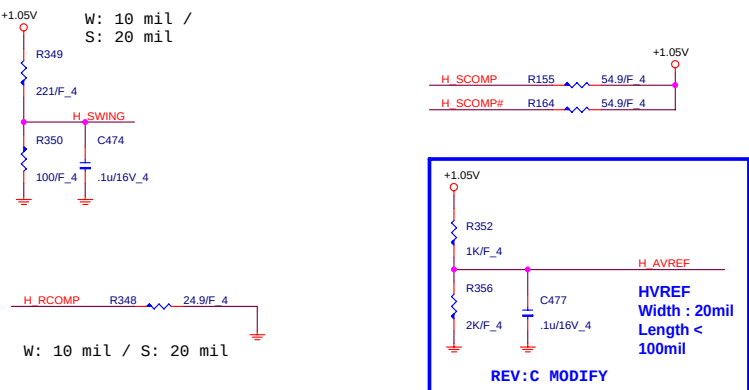
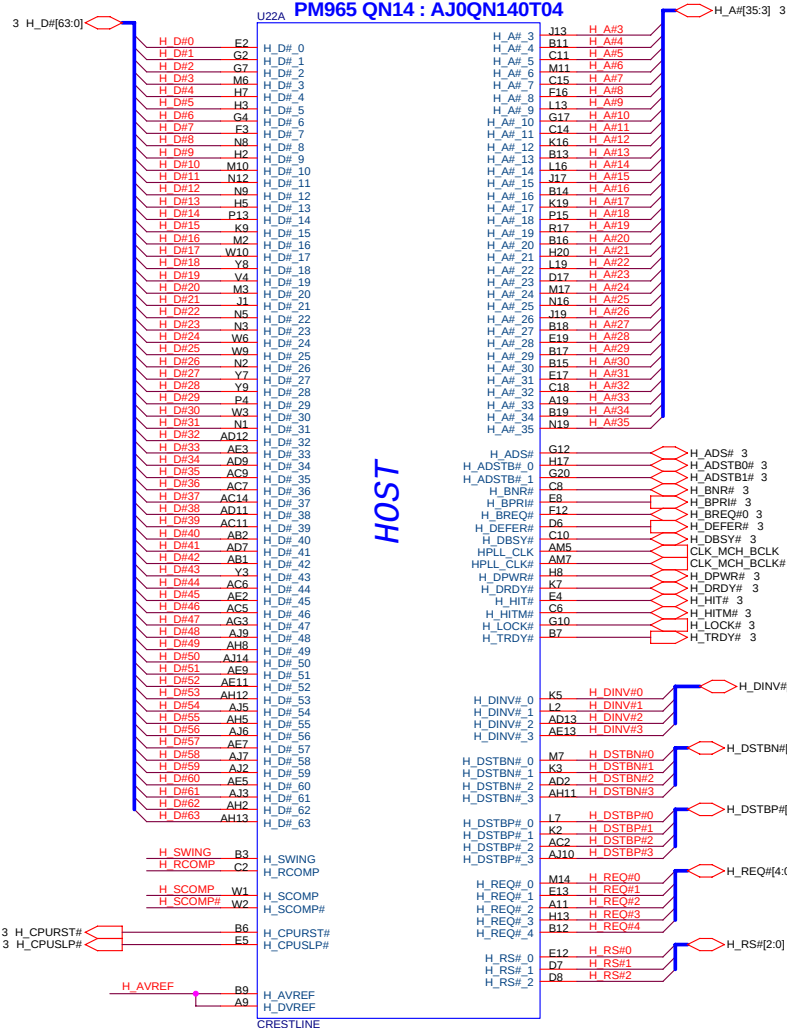
PROJECT : ZO1
Quanta Computer Inc.

Size	Document Number CLOCK GENERATOR CK505 W/REGULATOR	Rev 2B
Date:	Thursday, May 17, 2007	Sheet 3 of 26

CPU(Power)

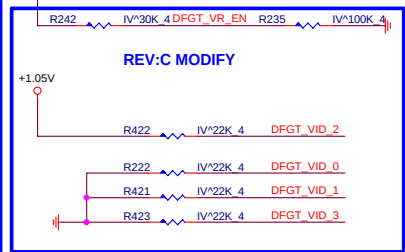
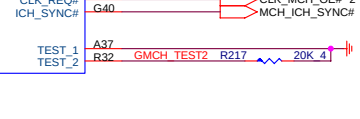
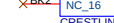
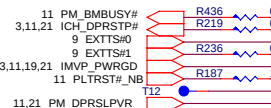


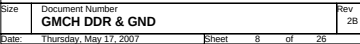
GM965 QN12 : AJ0QN120T04
PM965 QN14 : AJ0QN140T04



Any CFG signal strapping option not list below should be left NC Pin

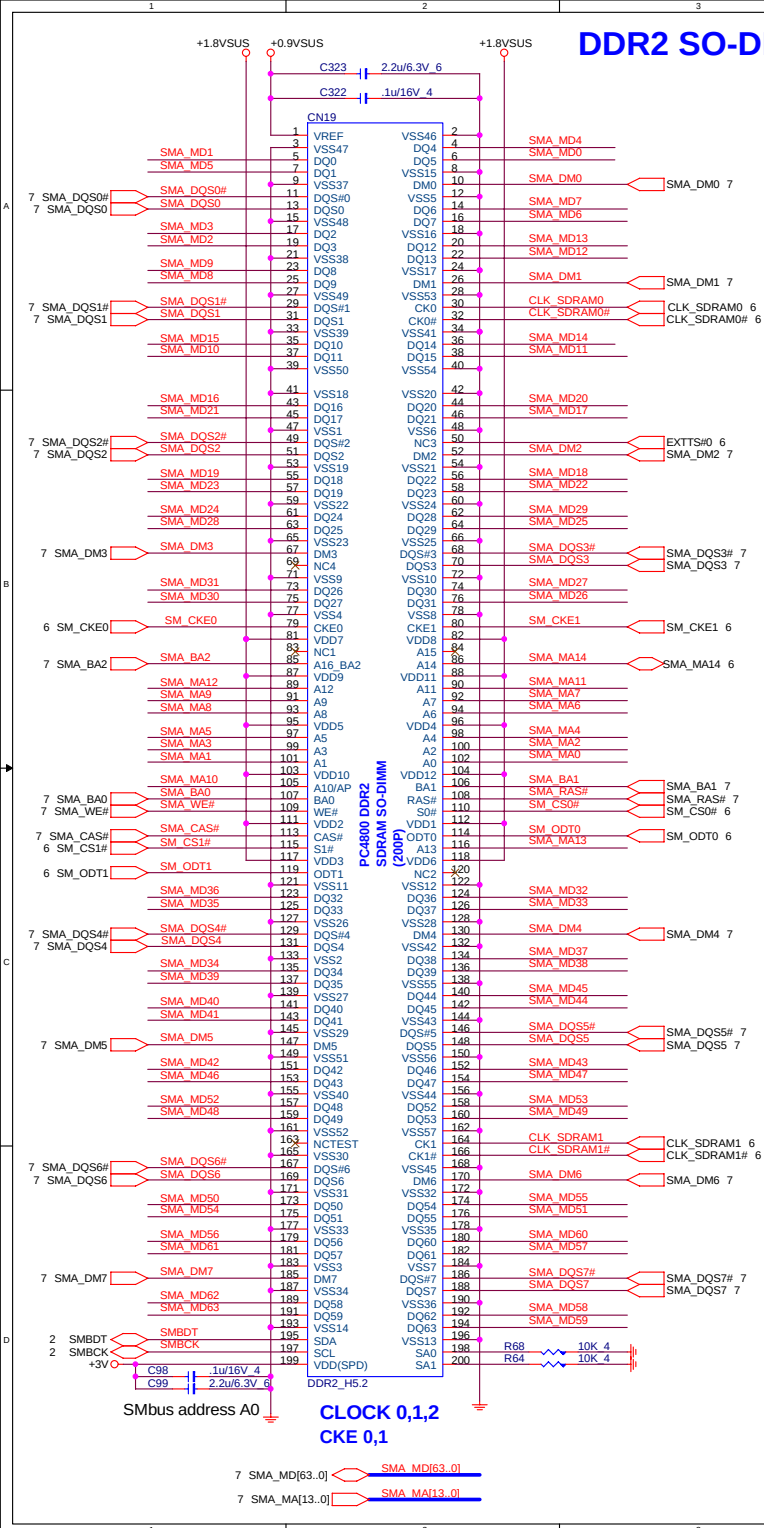
CF620	SDVO/PCie concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port
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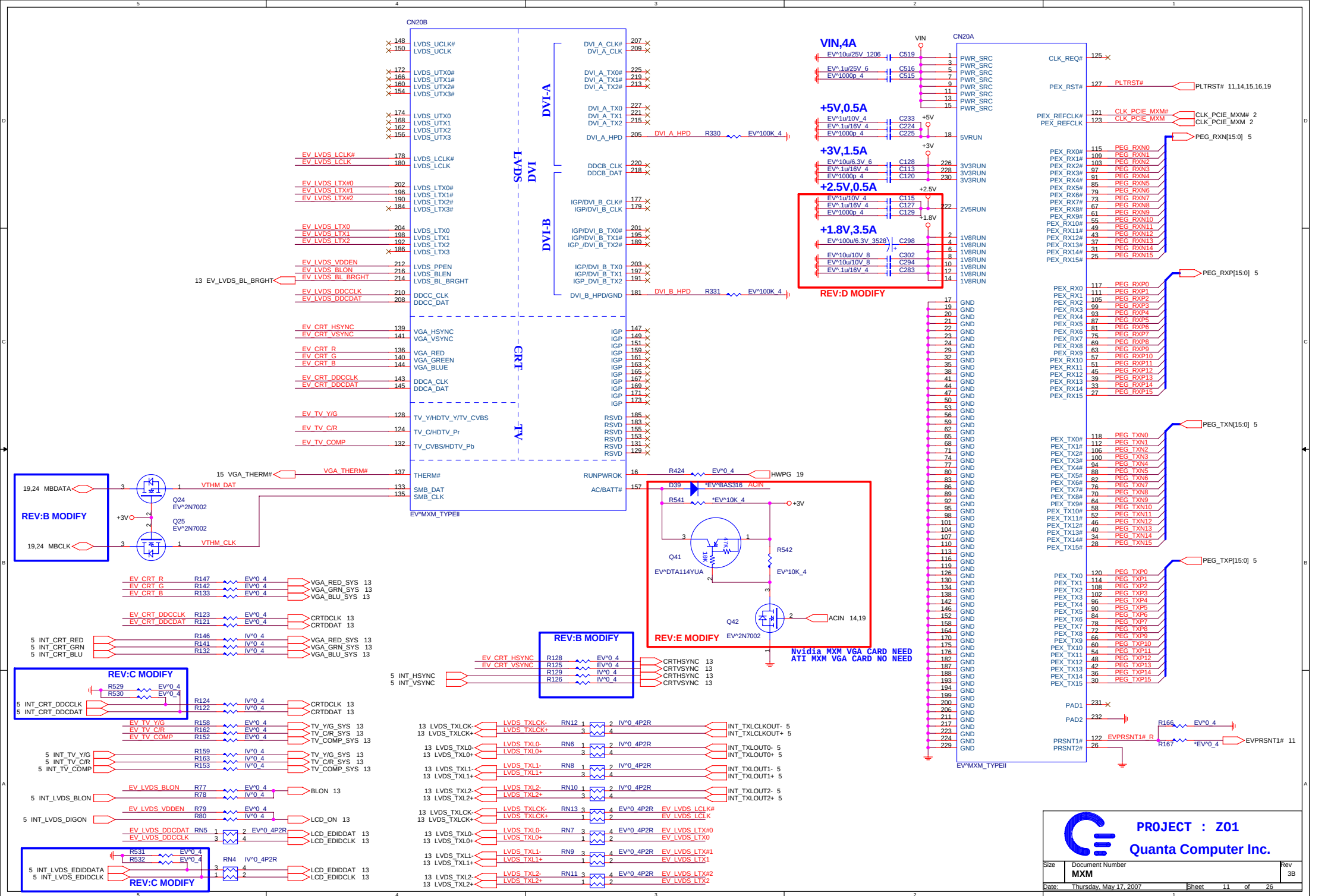


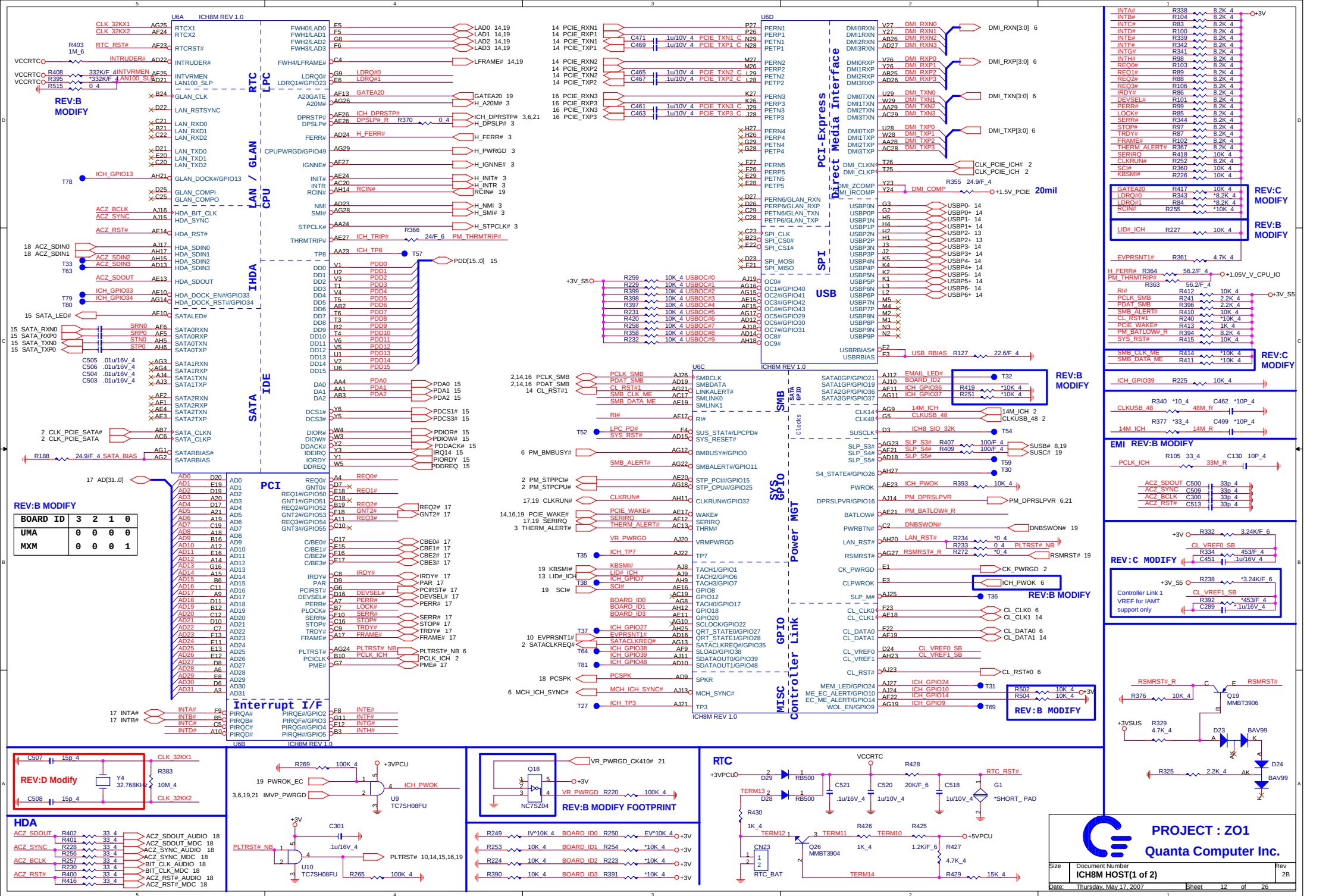


DDR2 SO-DIMM SOCKET

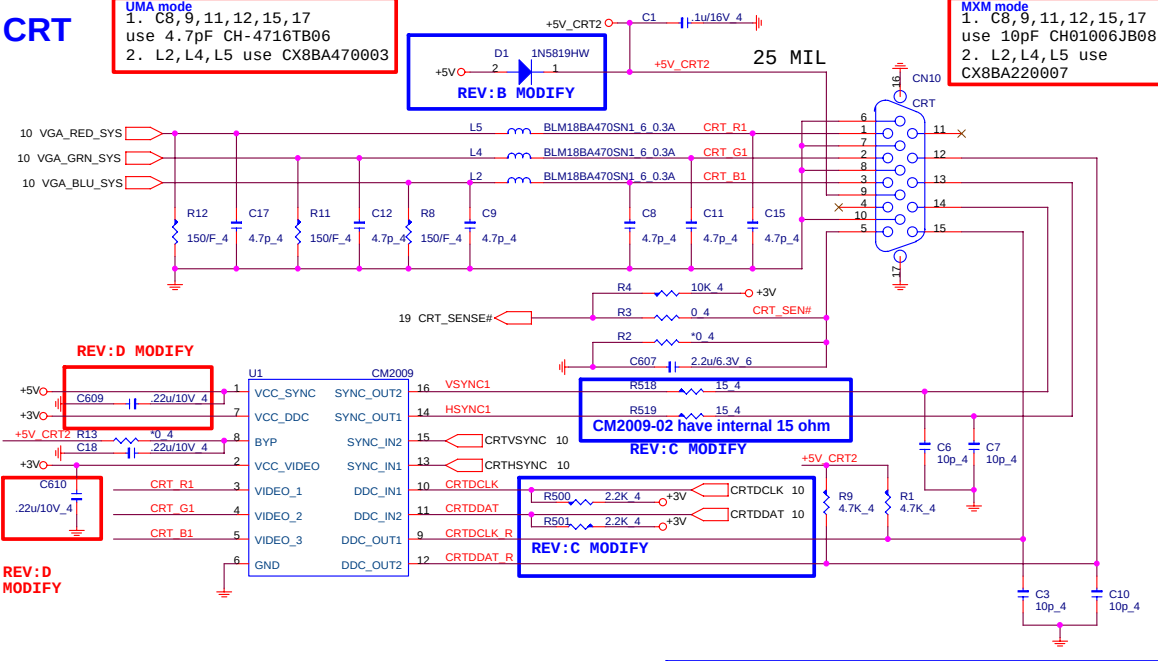
DDR2 TERMINATOR



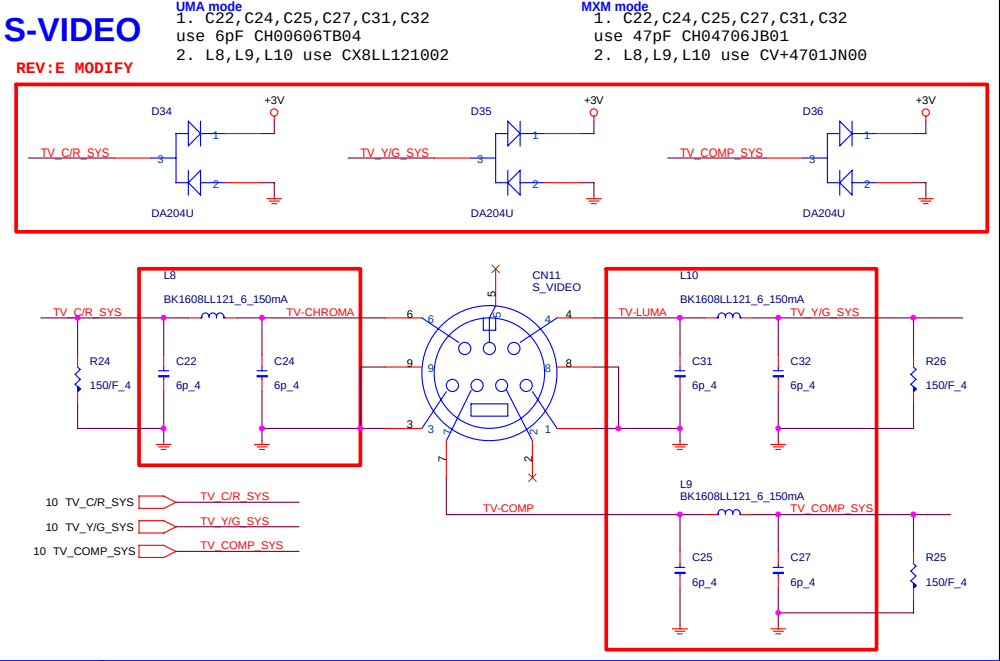




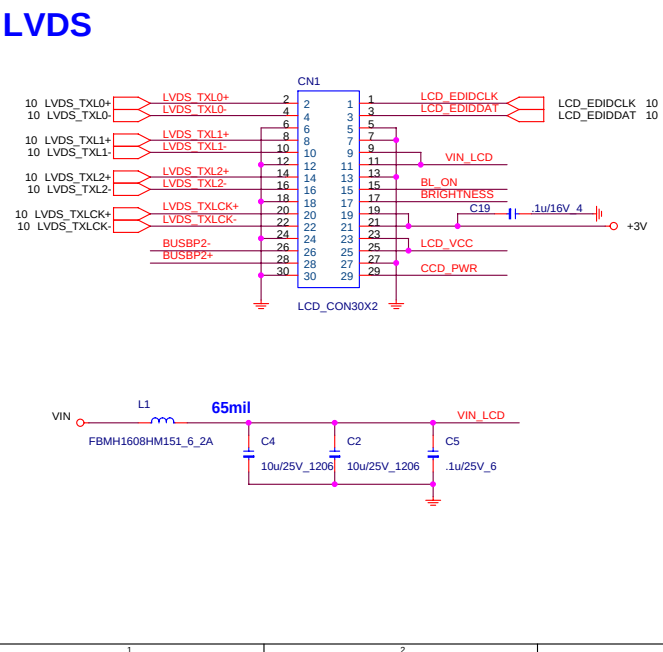
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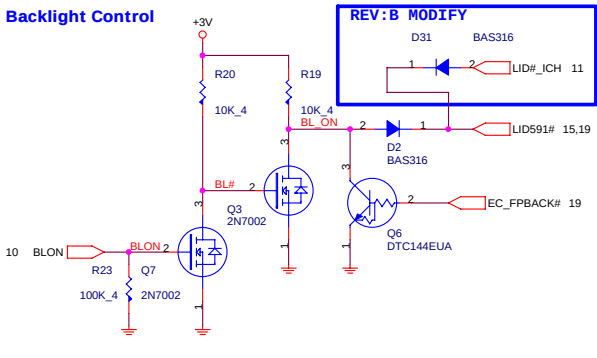
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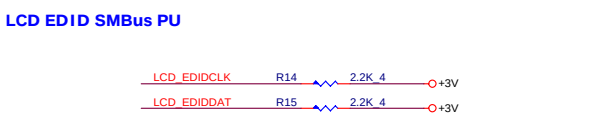
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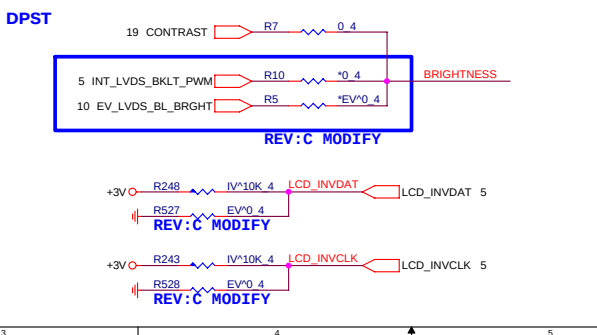
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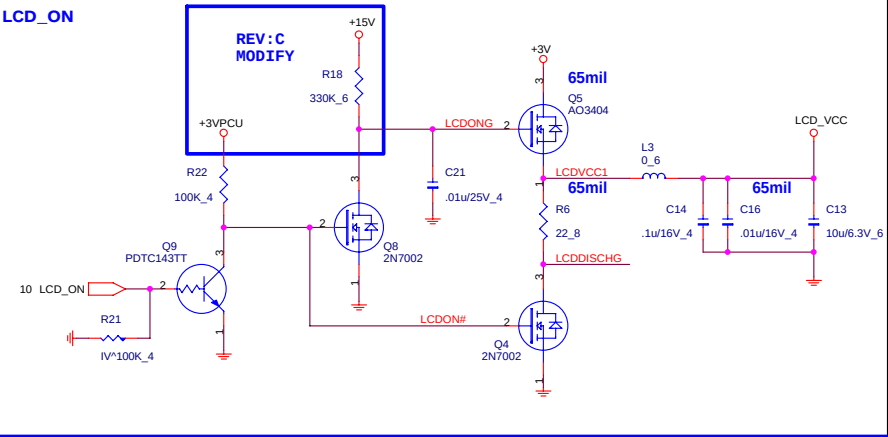
LCD EDID SMBus PU



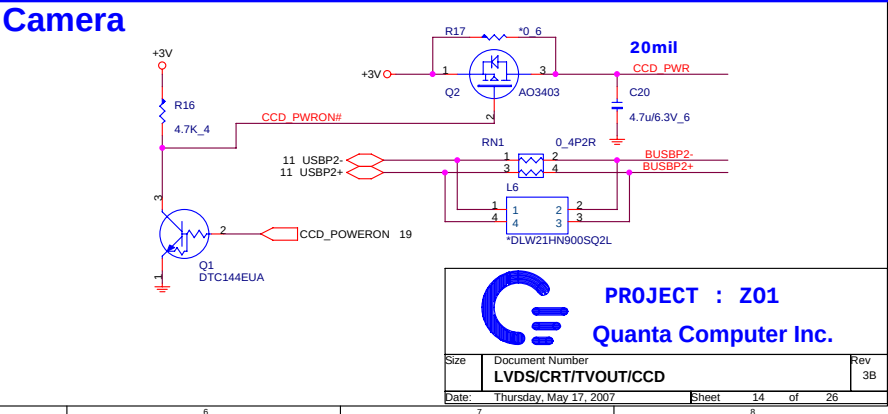
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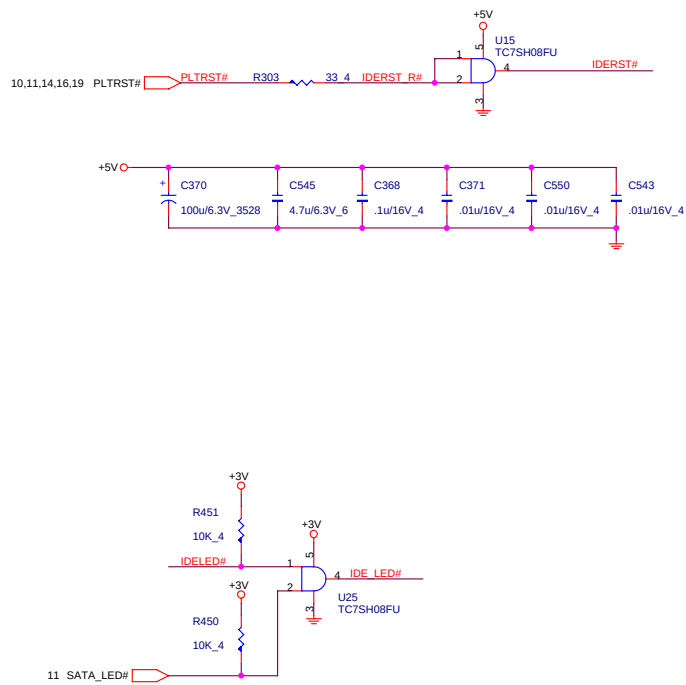
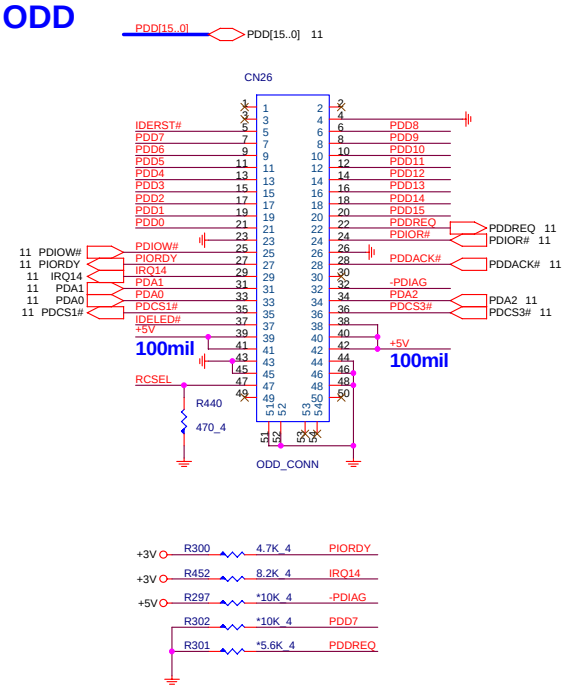
LCD_ON



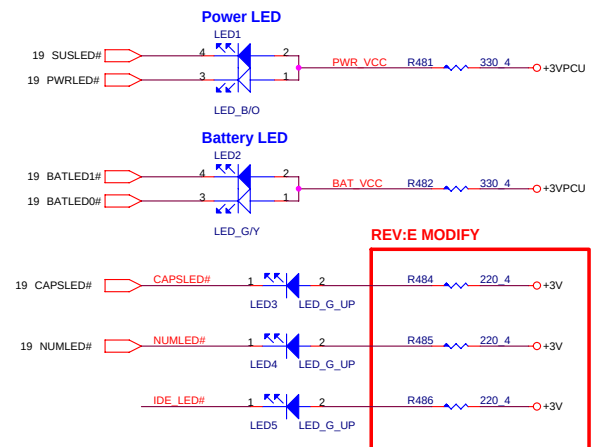
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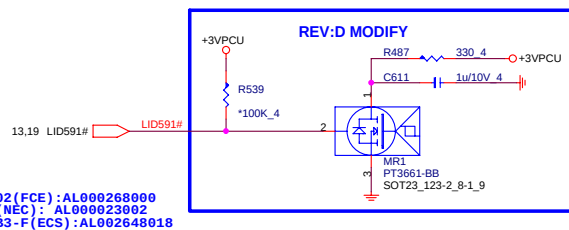
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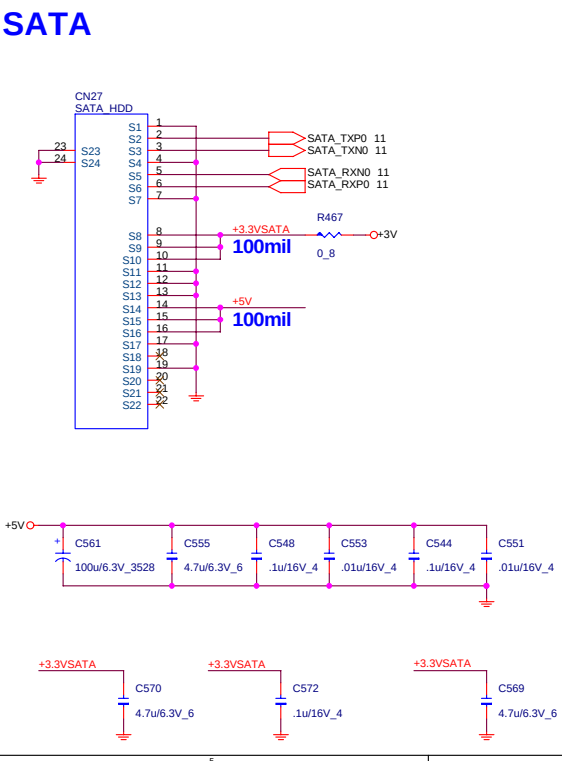
LED



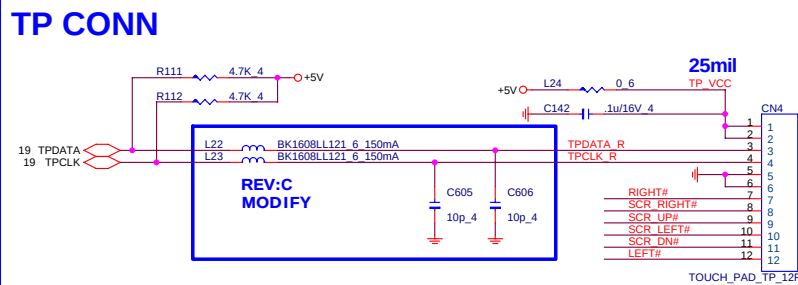
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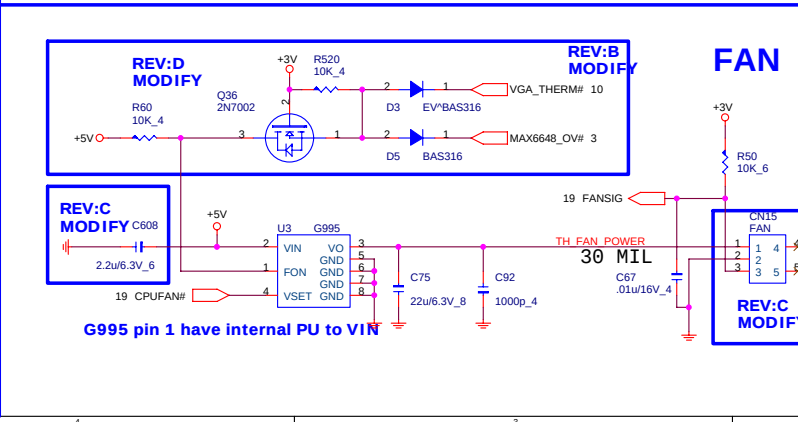


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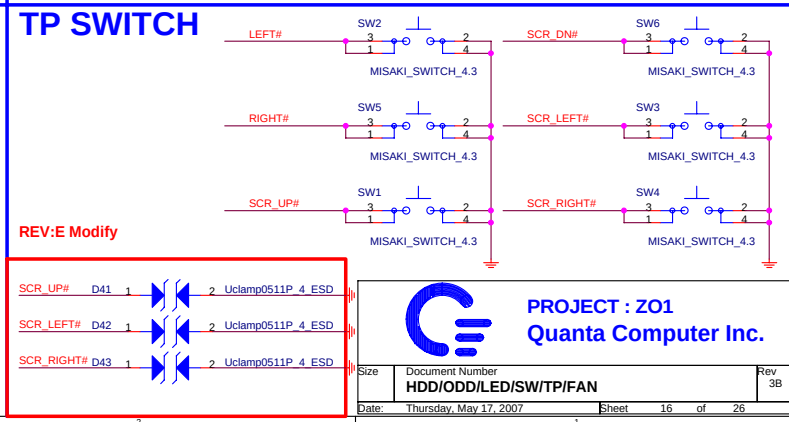


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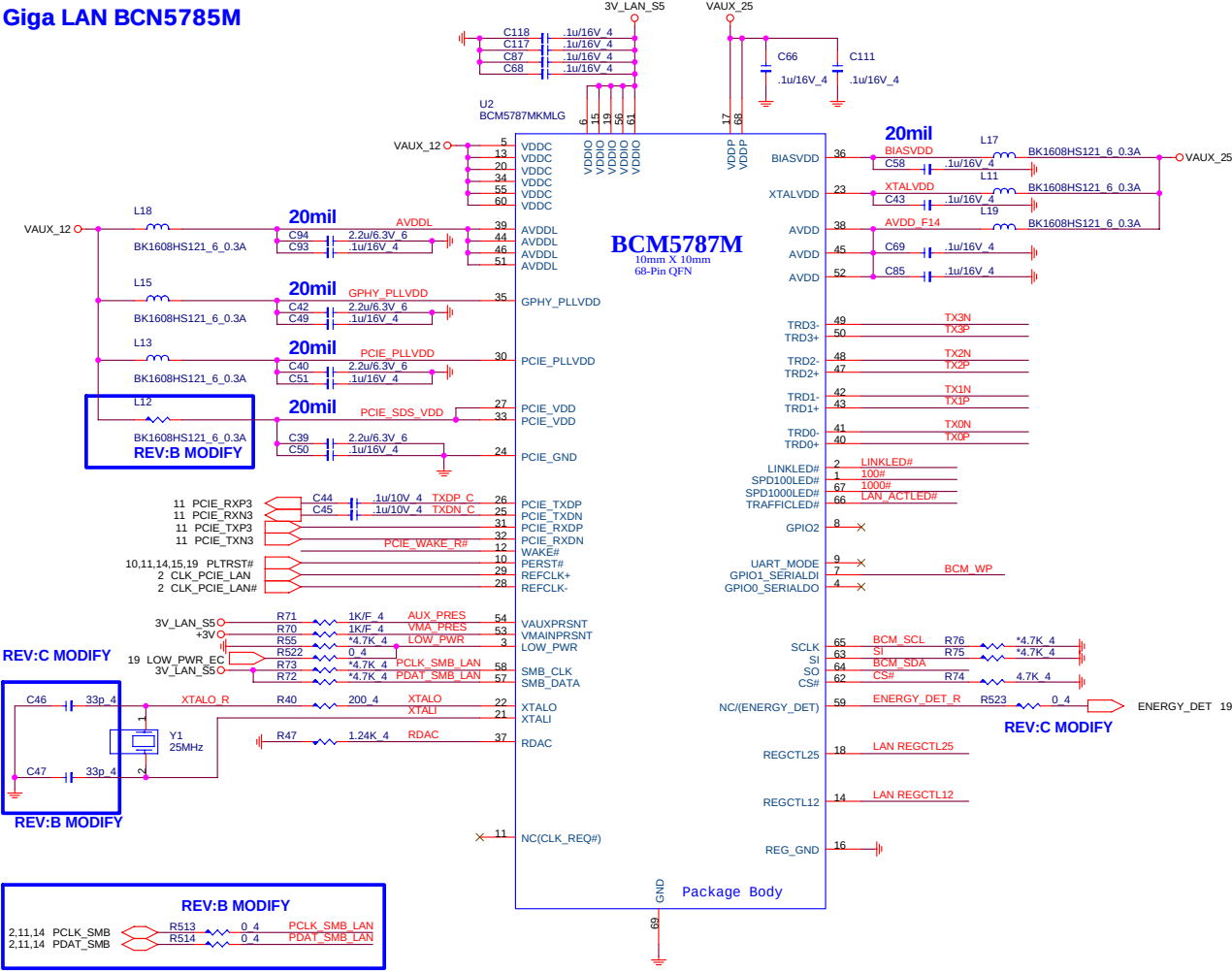




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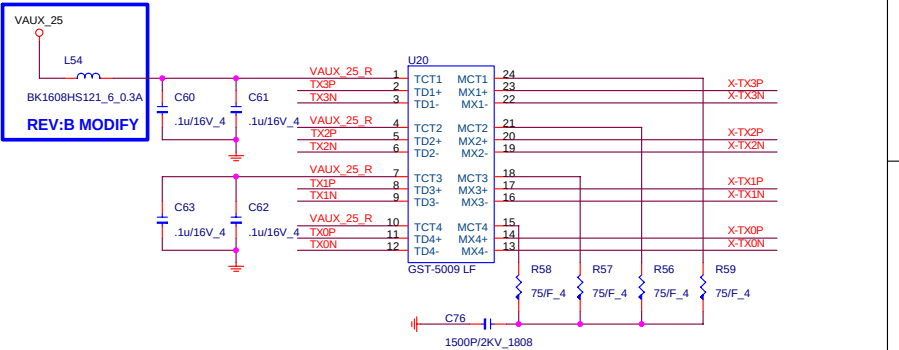


Giga LAN BCN5785M

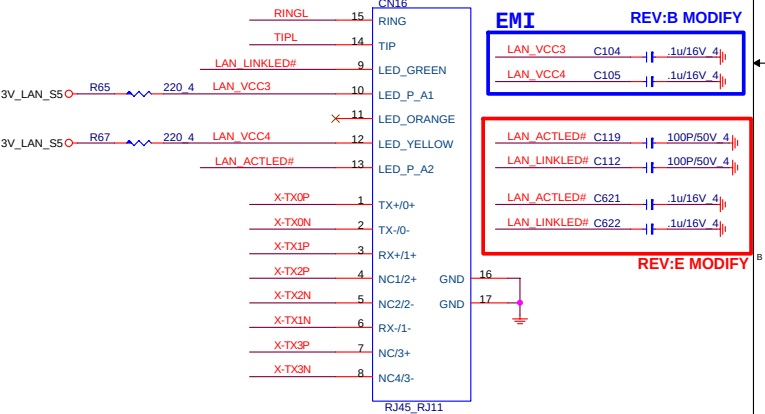


Transformer

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Source 2: Bothand GST5009 DBKN1NLAN03
Source 3: FCE NS892402 DB0ZH1LAN06



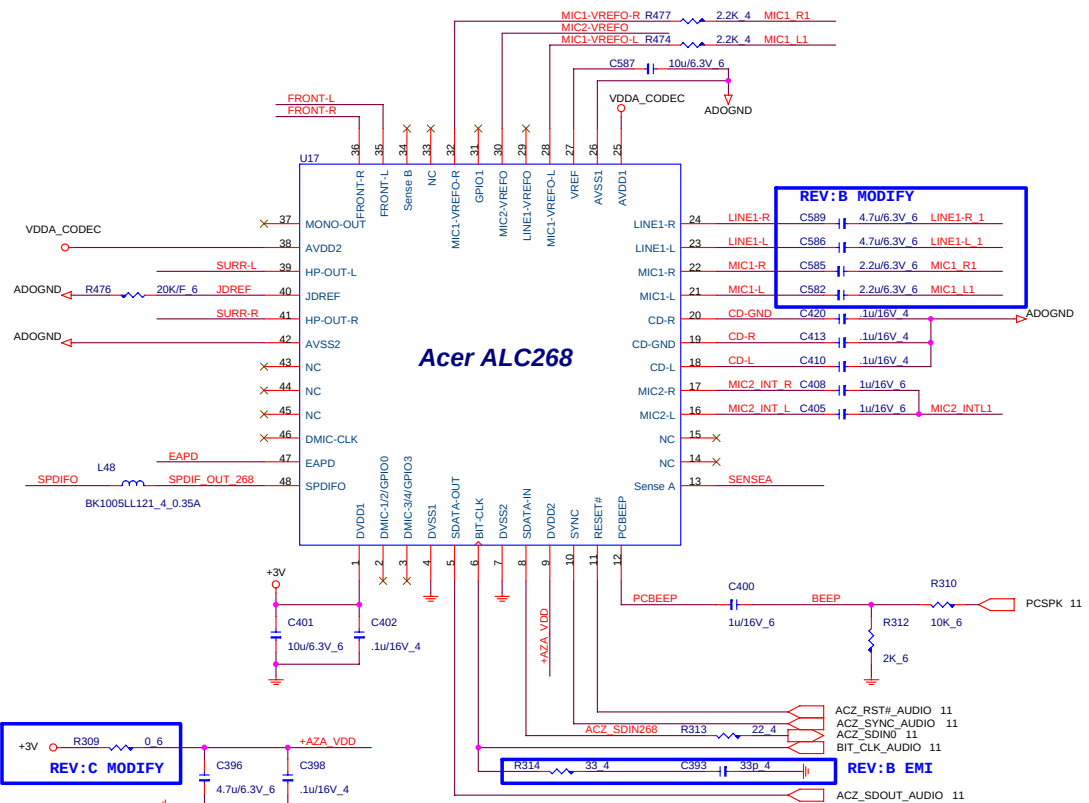
RJ45 & RJ11 connector



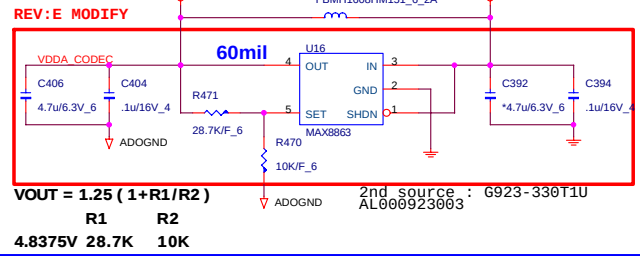
RJ11 cable



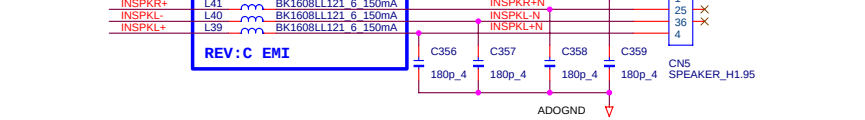
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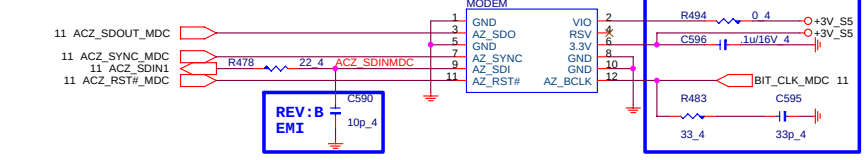
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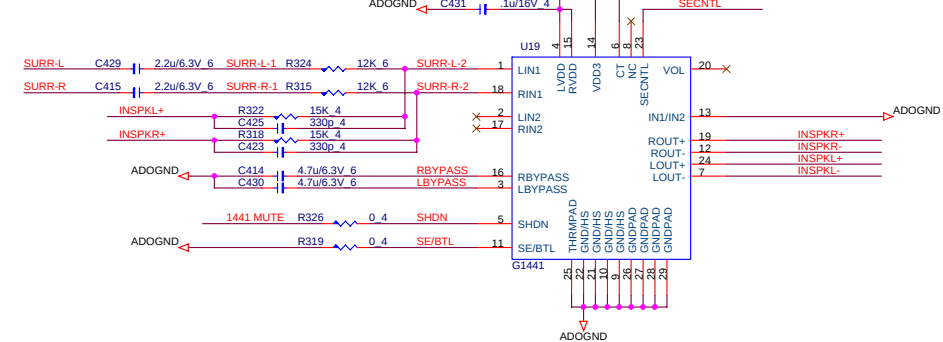
SPEAKER



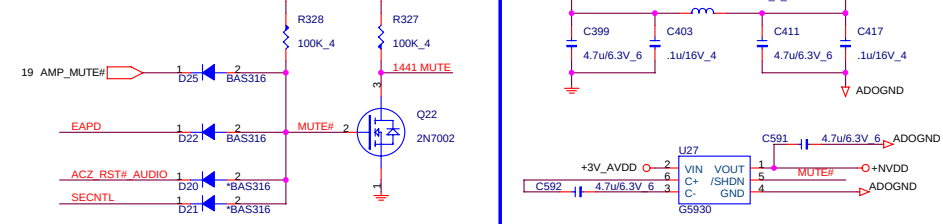
MDC



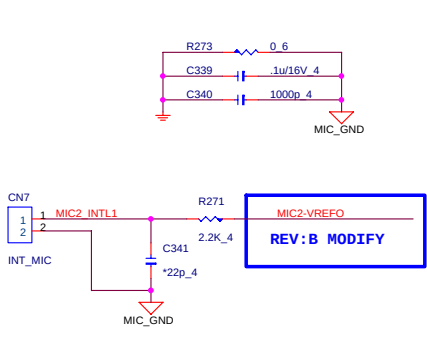
Speaker Amplifier



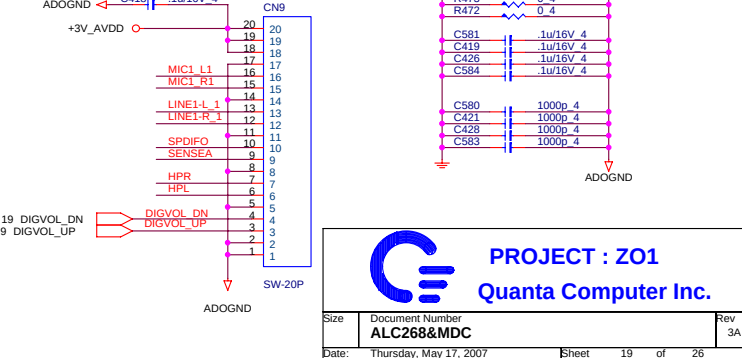
LINE OUT Amplifier



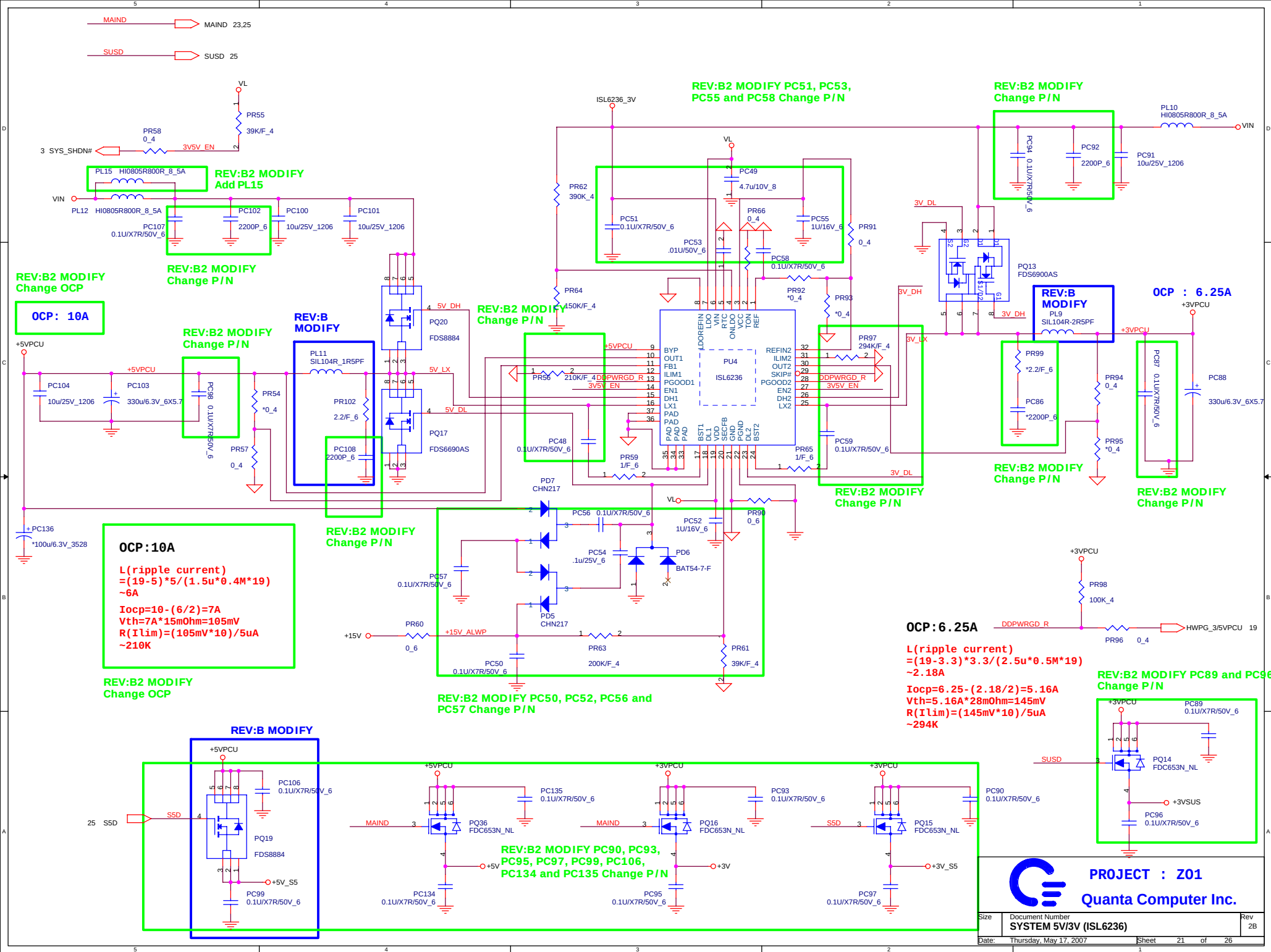
INT MIC array

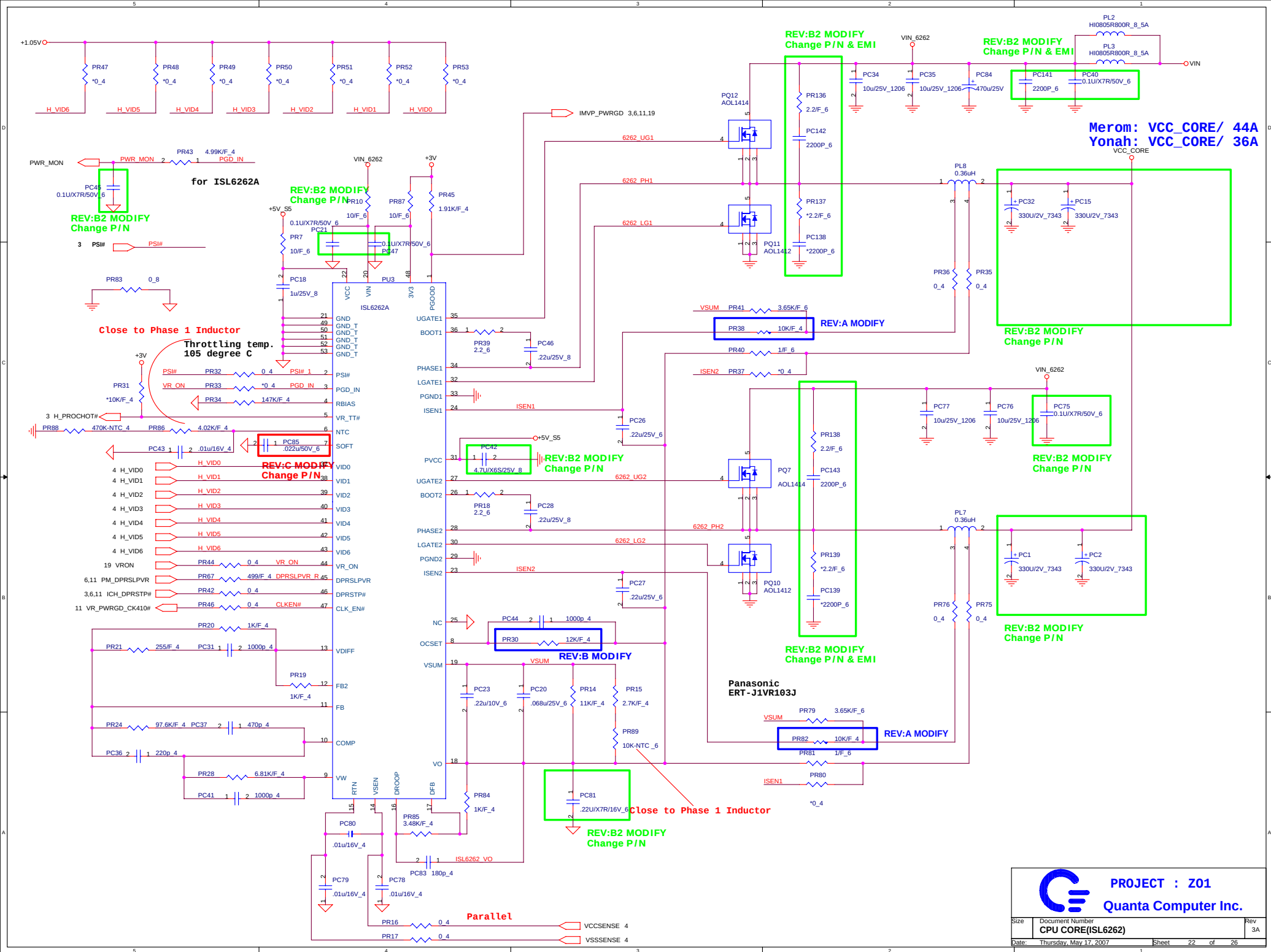


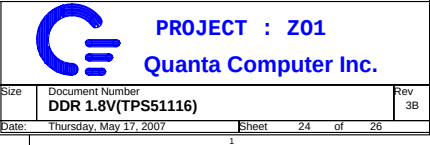
AUDIO/B

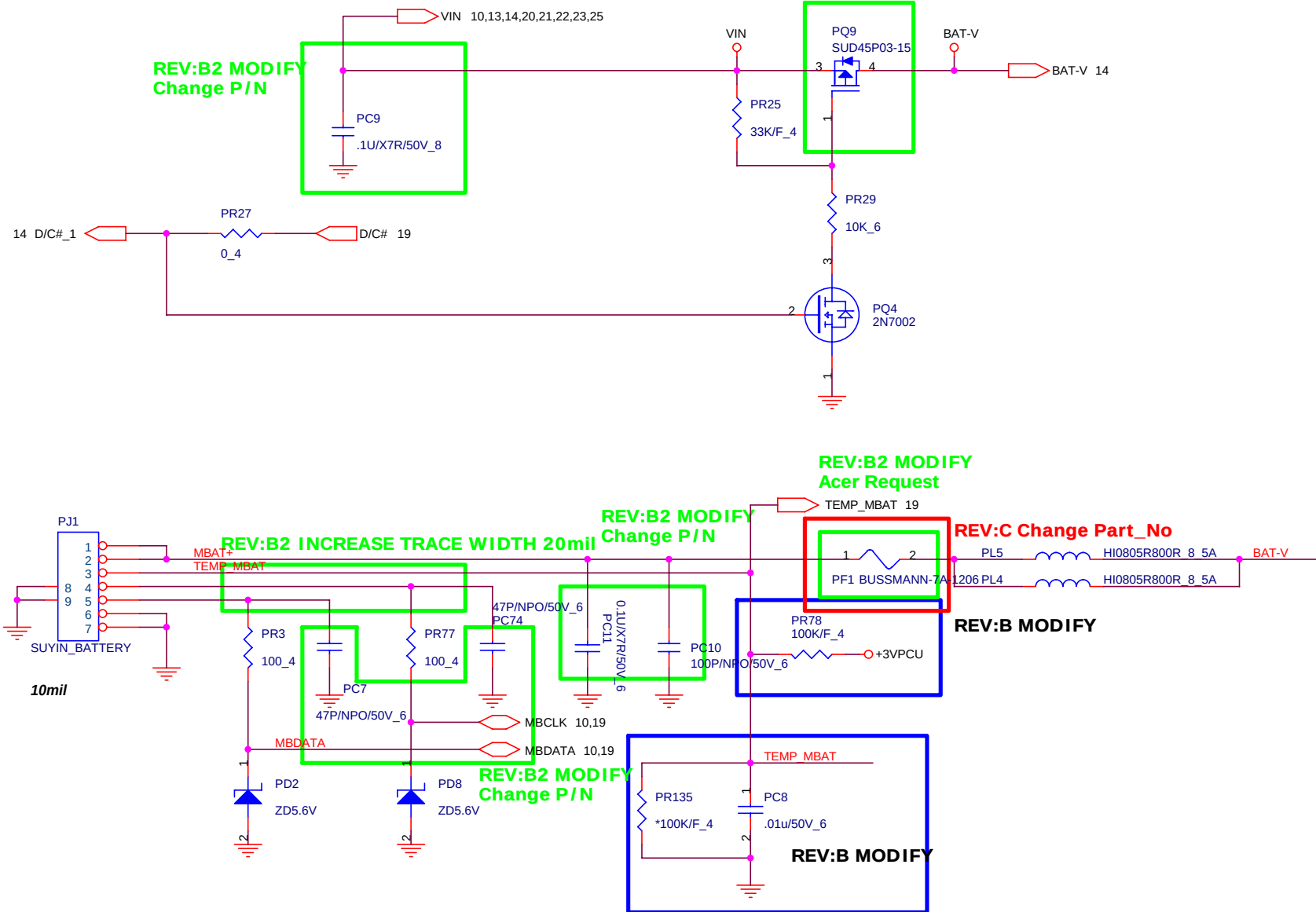


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