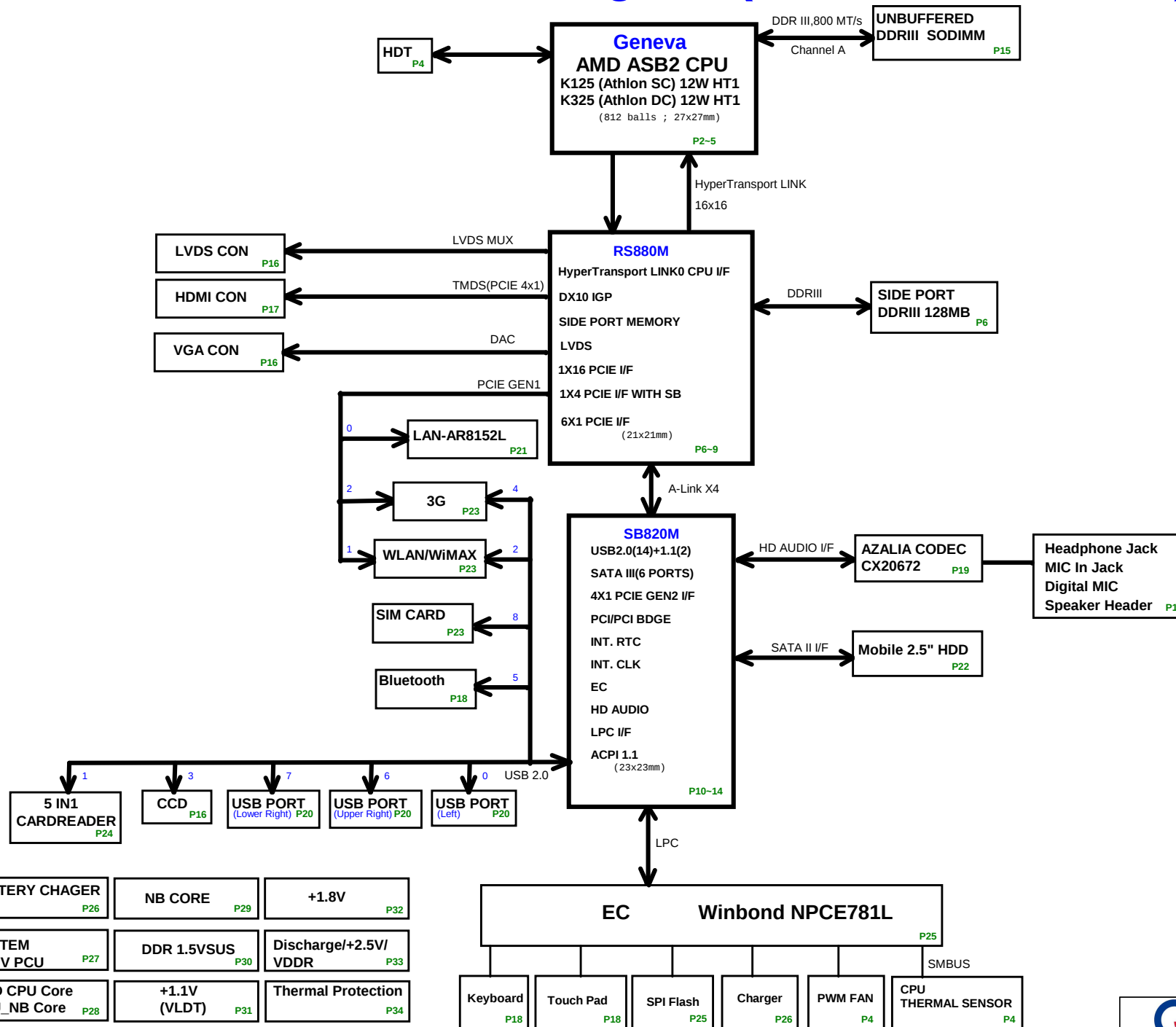


ZH9 Block Diagram (AMD Nile Platform)



U16A

HT_CADINP15	W7	L0_CADIN_H15	L0_CADOUT_H15	AB6	HT_CADOUTP15
HT_CADINP15	W6	L0_CADIN_L15	L0_CADOUT_L15	AB5	HT_CADOUTN15
HT_CADINP14	U6	L0_CADIN_H14	L0_CADOUT_H14	AB9	HT_CADOUTP14
HT_CADINP14	U5	L0_CADIN_L14	L0_CADOUT_L14	AB8	HT_CADOUTN14
HT_CADINP13	R7	L0_CADIN_H13	L0_CADOUT_H13	AC7	HT_CADOUTP13
HT_CADINN13	R6	L0_CADIN_L13	L0_CADOUT_L13	AC6	HT_CADOUTN13
HT_CADINP12	P6	L0_CADIN_H12	L0_CADOUT_H12	AE6	HT_CADOUTP12
HT_CADINN12	P5	L0_CADIN_L12	L0_CADOUT_L12	AE5	HT_CADOUTN12
HT_CADINP11	L6	L0_CADIN_H11	L0_CADOUT_H11	AE9	HT_CADOUTP11
HT_CADINN11	L5	L0_CADIN_L11	L0_CADOUT_L11	AE8	HT_CADOUTN11
HT_CADINP10	J6	L0_CADIN_H10	L0_CADOUT_H10	AH3	HT_CADOUTP10
HT_CADINN10	J5	L0_CADIN_L10	L0_CADOUT_L10	AH4	HT_CADOUTN10
HT_CADINP9	H4	L0_CADIN_H9	L0_CADOUT_H9	AK3	HT_CADOUTP9
HT_CADINN9	H3	L0_CADIN_L9	L0_CADOUT_L9	AK4	HT_CADOUTN9
HT_CADINP8	G6	L0_CADIN_H8	L0_CADOUT_H8	AH1	HT_CADOUTP8
HT_CADINN8	G5	L0_CADIN_L8	L0_CADOUT_L8	AH2	HT_CADOUTN8
HT_CADINP7	T3	L0_CADIN_H7	L0_CADOUT_H7	Y1	HT_CADOUTP7
HT_CADINN7	T4	L0_CADIN_L7	L0_CADOUT_L7	Y2	HT_CADOUTN7
HT_CADINP6	T2	L0_CADIN_H6	L0_CADOUT_H6	Y4	HT_CADOUTP6
HT_CADINN6	T1	L0_CADIN_L6	L0_CADOUT_L6	Y3	HT_CADOUTN6
HT_CADINP5	P3	L0_CADIN_H5	L0_CADOUT_H5	AB1	HT_CADOUTP5
HT_CADINN5	P4	L0_CADIN_L5	L0_CADOUT_L5	AB2	HT_CADOUTN5
HT_CADINP4	P2	L0_CADIN_H4	L0_CADOUT_H4	AB4	HT_CADOUTP4
HT_CADINN4	P1	L0_CADIN_L4	L0_CADOUT_L4	AB3	HT_CADOUTN4
HT_CADINP3	M2	L0_CADIN_H3	L0_CADOUT_H3	AD4	HT_CADOUTP3
HT_CADINN3	M1	L0_CADIN_L3	L0_CADOUT_L3	AD3	HT_CADOUTN3
HT_CADINP2	K3	L0_CADIN_H2	L0_CADOUT_H2	AE1	HT_CADOUTP2
HT_CADINN2	K4	L0_CADIN_L2	L0_CADOUT_L2	AE2	HT_CADOUTN2
HT_CADINP1	K2	L0_CADIN_H1	L0_CADOUT_H1	AE4	HT_CADOUTP1
HT_CADINN1	K1	L0_CADIN_L1	L0_CADOUT_L1	AE3	HT_CADOUTN1
HT_CADINP0	H2	L0_CADIN_H0	L0_CADOUT_H0	AK1	HT_CADOUTP0
HT_CADINN0	H1	L0_CADIN_L0	L0_CADOUT_L0	AK2	HT_CADOUTN0
HT_CLKINP1	M8	L0_CLKIN_H1	L0_CLKOUT_H1	AE6	HT_CLKOUTP1
HT_CLKINN1	M7	L0_CLKIN_L1	L0_CLKOUT_L1	AE5	HT_CLKOUTN1
HT_CLKINP0	M3	L0_CLKIN_H0	L0_CLKOUT_H0	AD1	HT_CLKOUTP0
HT_CLKINN0	M4	L0_CLKIN_L0	L0_CLKOUT_L0	AD2	HT_CLKOUTN0
HT_CTLINP1	Y6	L0_CTLIN_H1	L0_CTLOUT_H1	Y8	HT_CTLOUTP1
HT_CTLINN1	Y5	L0_CTLIN_L1	L0_CTLOUT_L1	Y9	HT_CTLOUTN1
HT_CTLINP0	V2	L0_CTLIN_H0	L0_CTLOUT_H0	V4	HT_CTLOUTP0
HT_CTLINN0	V1	L0_CTLIN_L0	L0_CTLOUT_L0	V3	HT_CTLOUTN0

HT LINK

<6> HT_CADINP[15..0]	HT_CADINP[15..0]
<6> HT_CADINN[15..0]	HT_CADINN[15..0]
<6> HT_CLKINP[1..0]	HT_CLKINP[1..0]
<6> HT_CLKINN[1..0]	HT_CLKINN[1..0]
<6> HT_CTLINP[1..0]	HT_CTLINP[1..0]
<6> HT_CTLINN[1..0]	HT_CTLINN[1..0]
<6> HT_CADOUTP[15..0]	HT_CADOUTP[15..0]
<6> HT_CADOUTN[15..0]	HT_CADOUTN[15..0]
<6> HT_CLKOUTP[1..0]	HT_CLKOUTP[1..0]
<6> HT_CLKOUTN[1..0]	HT_CLKOUTN[1..0]
<6> HT_CTLOUTP[1..0]	HT_CTLOUTP[1..0]
<6> HT_CTLOUTN[1..0]	HT_CTLOUTN[1..0]

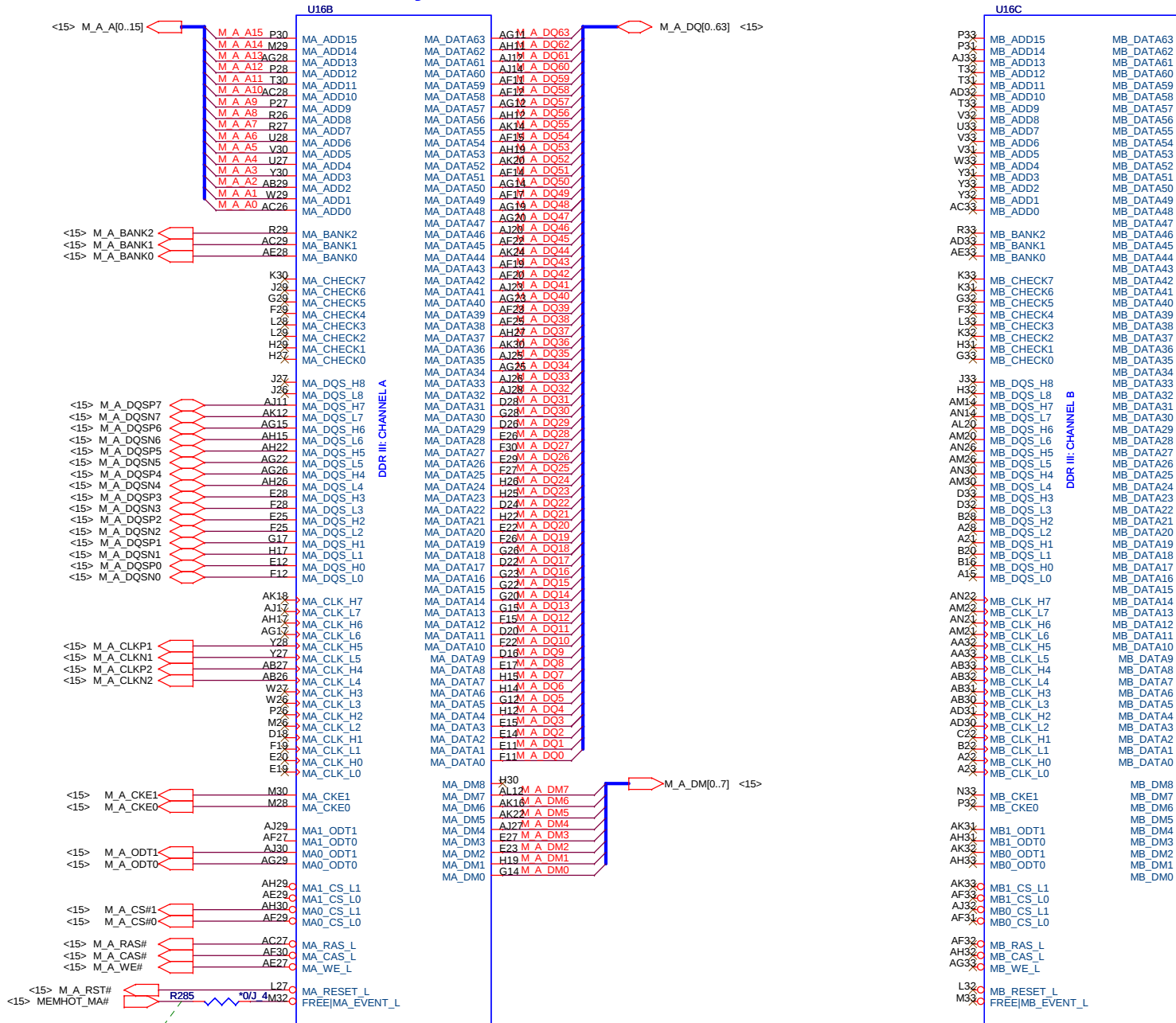


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PROJECT : ZH9

Size	Document Number	Rev
	ASB2 HT I/F 1/4	4A
Date:	Sunday, March 28, 2010	Sheet 2 of 40

Processor Memory Interface



BOM@ASB2_CPU

BOM@ASB2_CPU

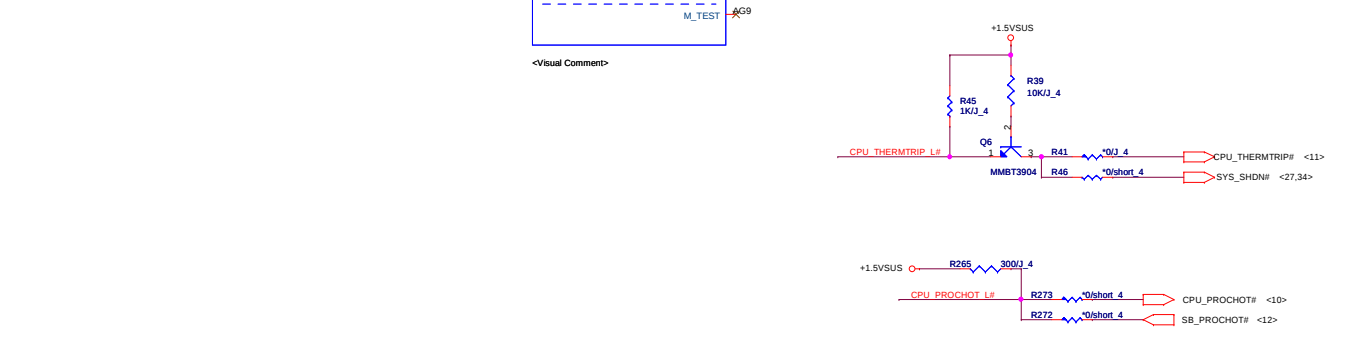
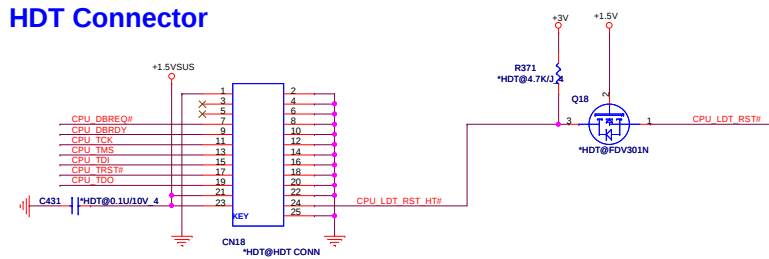
<Layout note>
Route as 60 ohms with
5/10 W/S from CPU pins.

<BOM Note>
V105 : AJ00105VT00
K125 : AJ0K125VT02
K325 : AJ0K325VT02
K625 : AJ0K625VT03

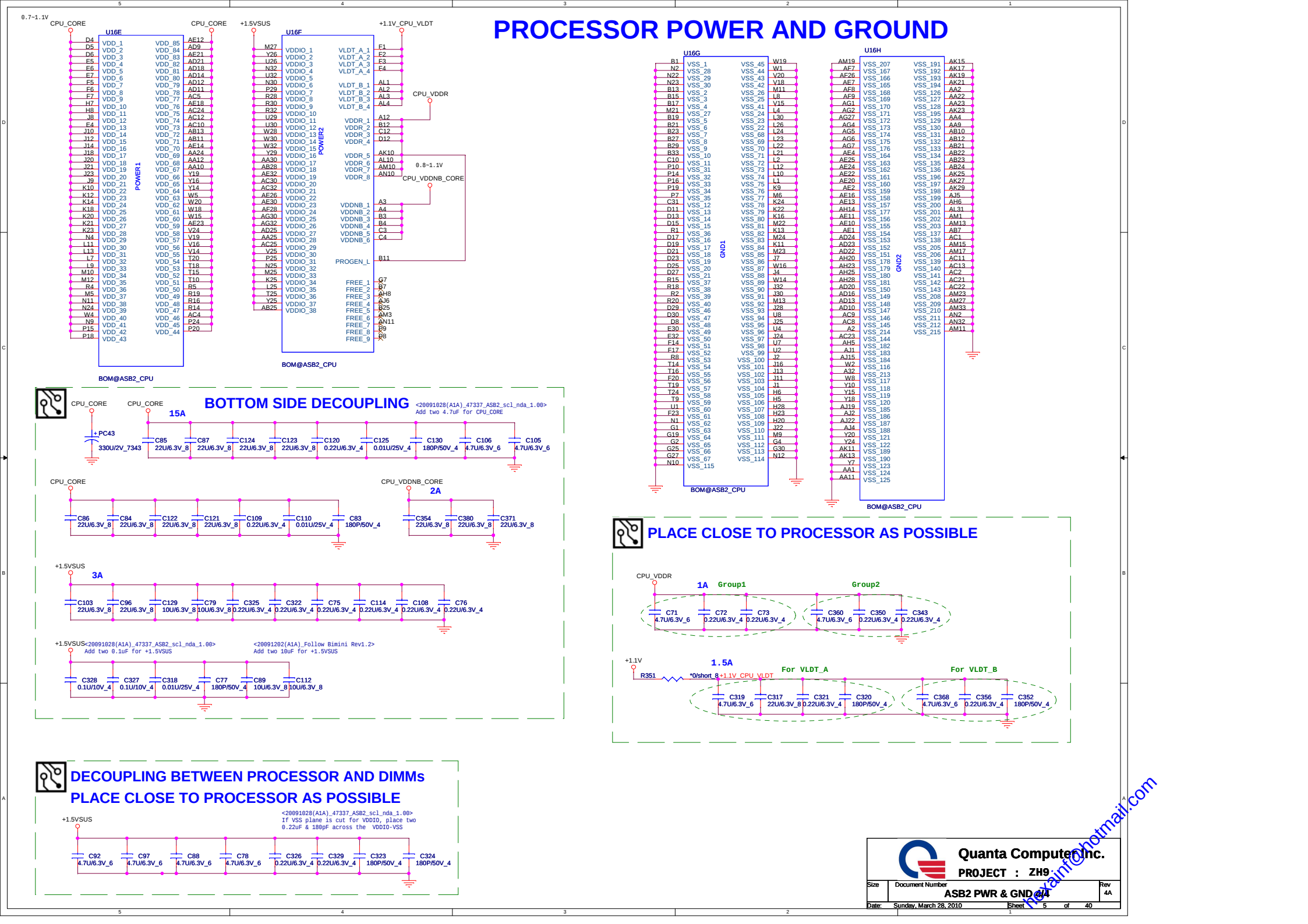
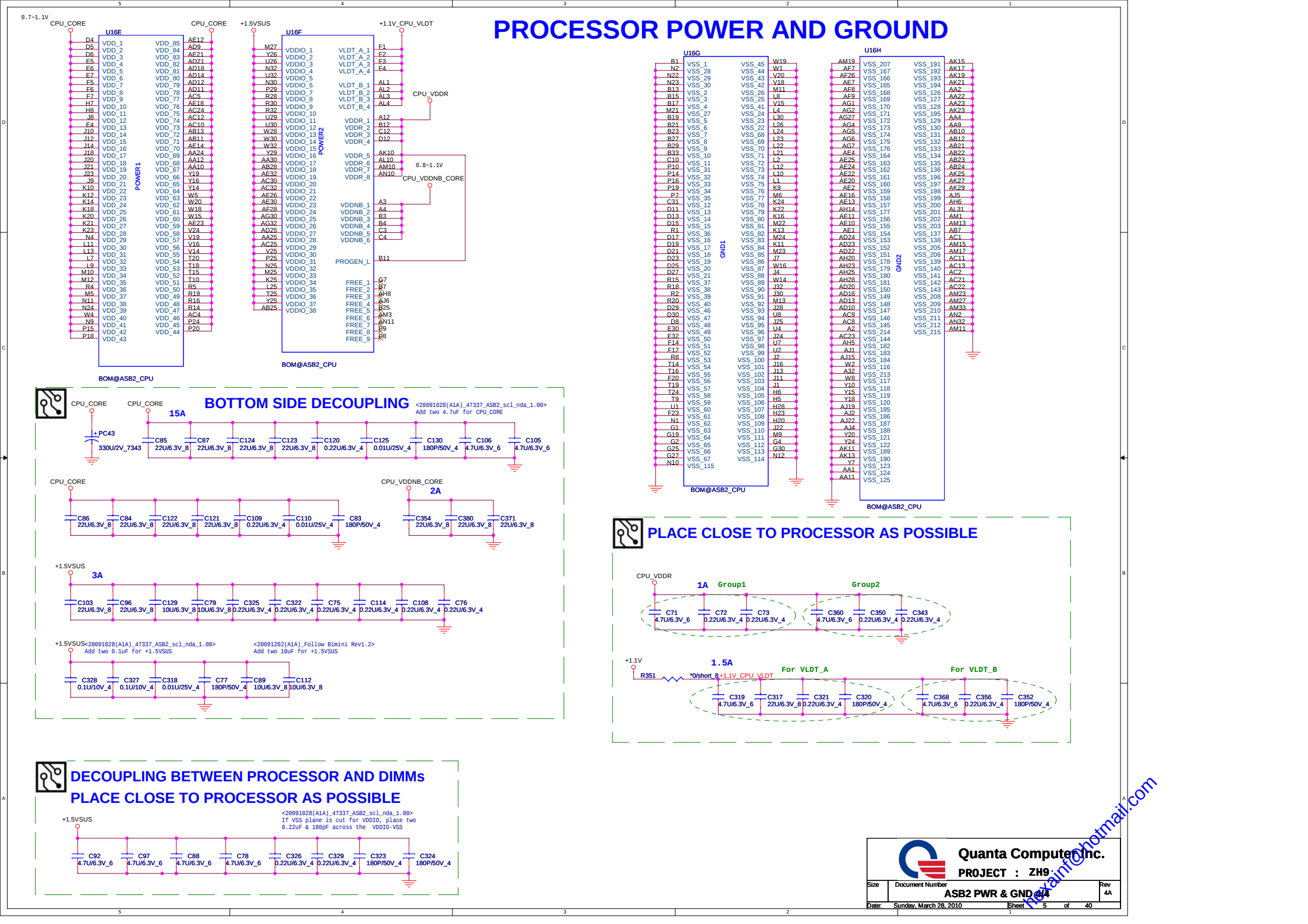
Quanta Computer Inc.
PROJECT : PH9

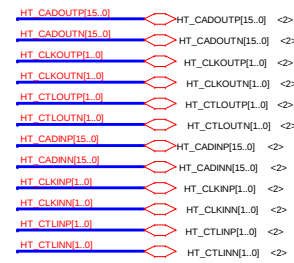
Size	Document Number	Rev
	ASB2 DDRIII MEMORY 2/4	4A
Date:	Sunday, March 28, 2010	Sheet 3 of 40

Reserve R266, C315, C316, U15, R276, R410 and stuff R51~R53, R48, Q7~Q9, D2, D3, R411, for AMD SB-TSI.

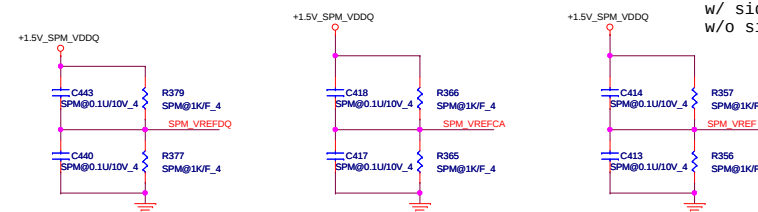
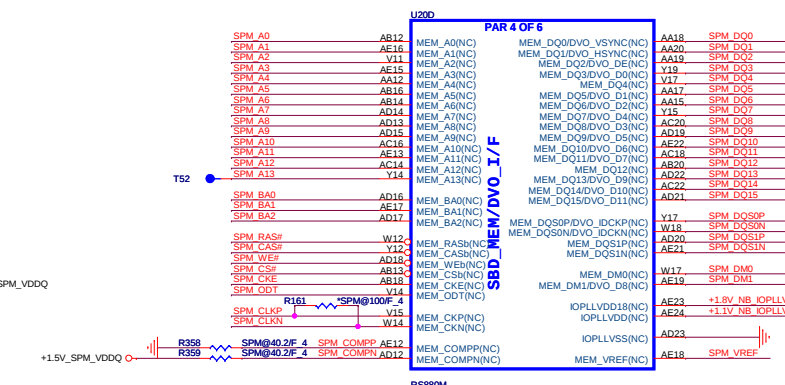
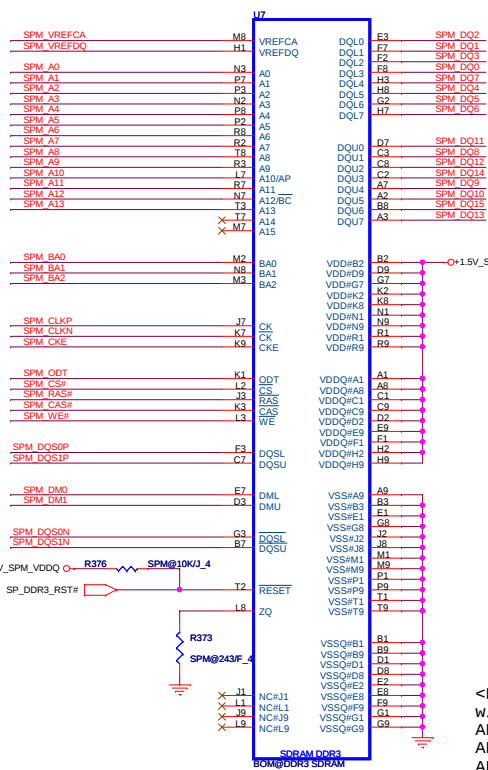
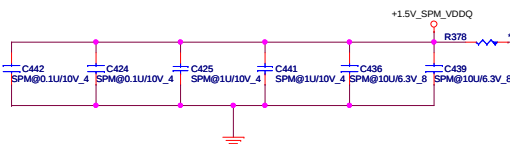


Quanta Computer Inc. PROJECT : ZH9	
Size	Document Number
	ASB2 CTRL & DEBUG 3/4
Date:	Sunday, March 28, 2010
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[illegible]



25mils 0.5A



<BOM Note>

```
w/ sideport: U7:
```

AKD5LGGT506 : SAMSUNG DDRIII 800 1Gb K4W1G1646E-HC12 LF

AKD5LZGTW04 : HYNIX DDRIII 800 1Gb H5TQ1G63BFR-12C LF

AKD5LGGT700 : ATI DDRIII 800 1Gb 23EY2387MA12-SZ LF+HF

w/o sideport: U7 Non-stuff

<BOM NOTE>

w/ sideport: L45,L46:CX8PG221003

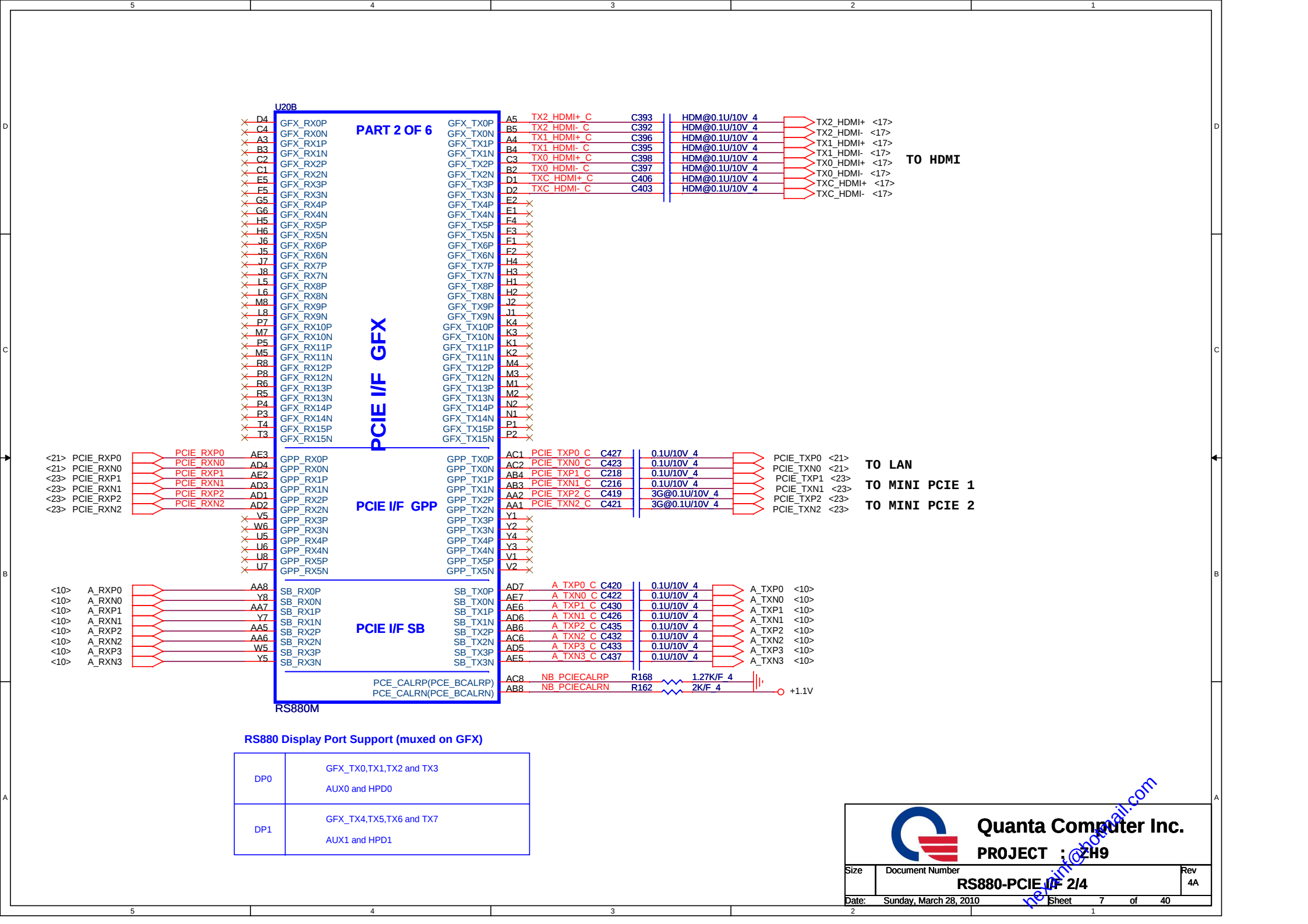
w/o sideport: L45,L46:CS00003J951(0ohm)



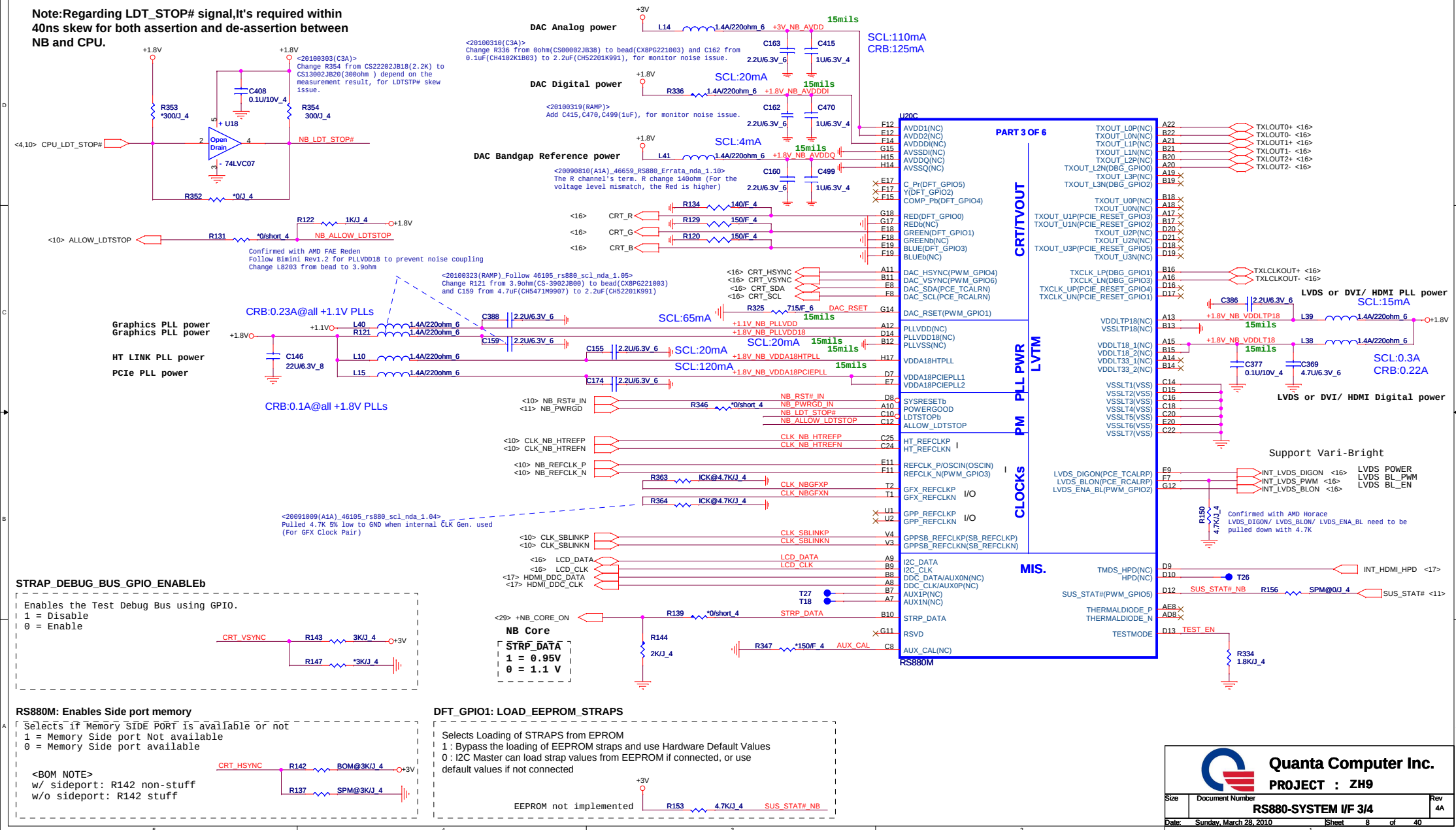
Quanta Computer Inc.

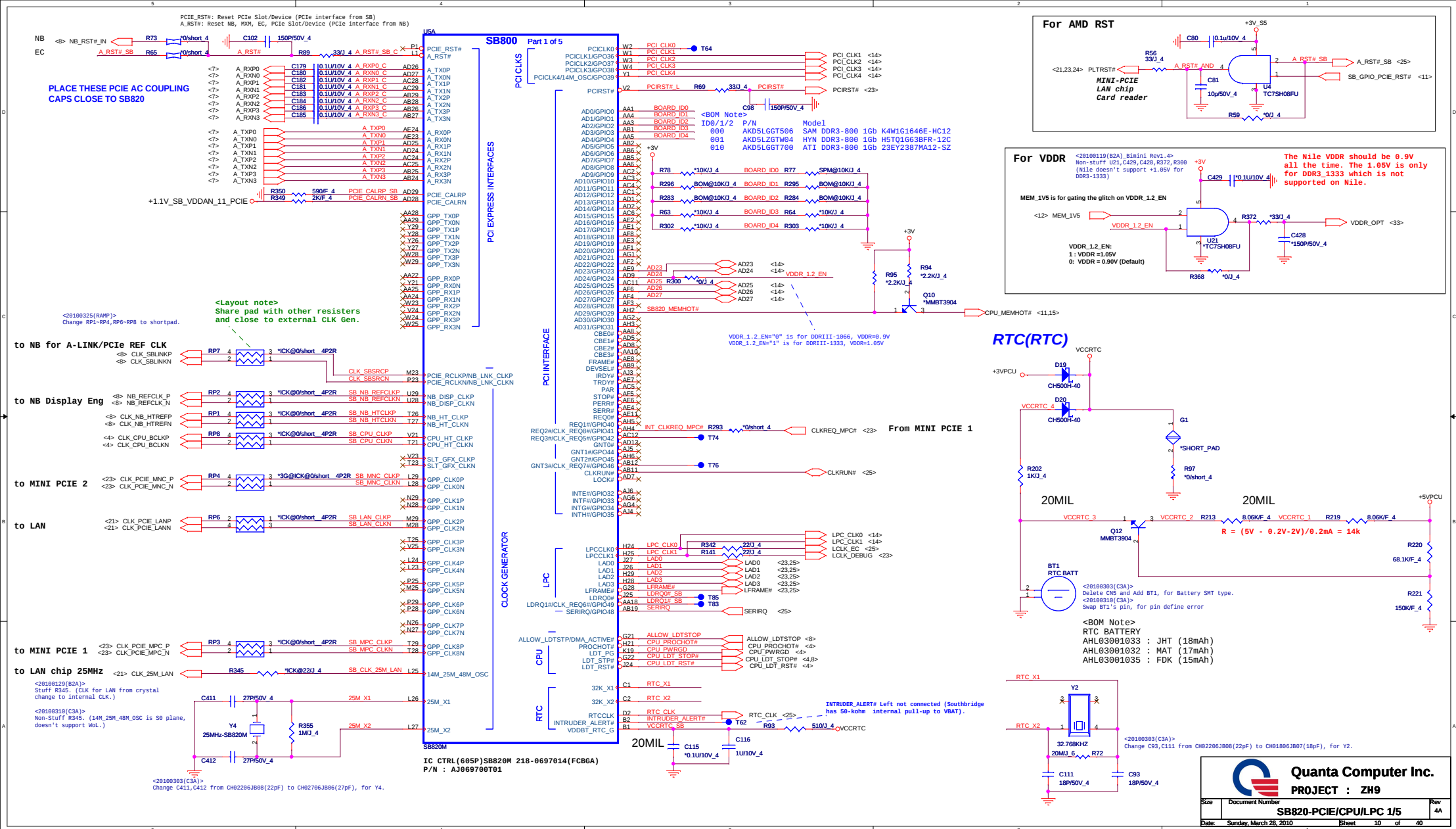
PROJECT : ZH9

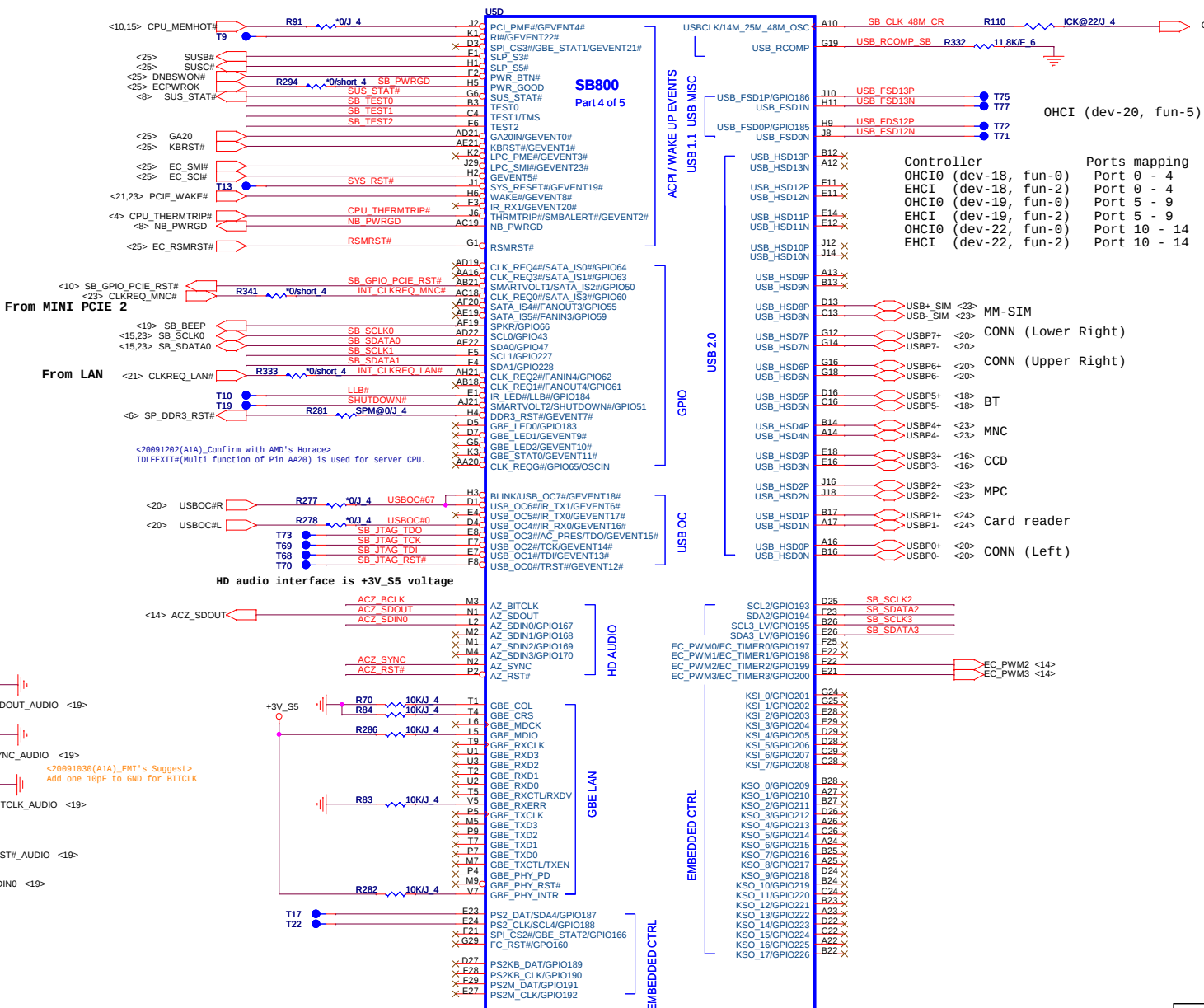
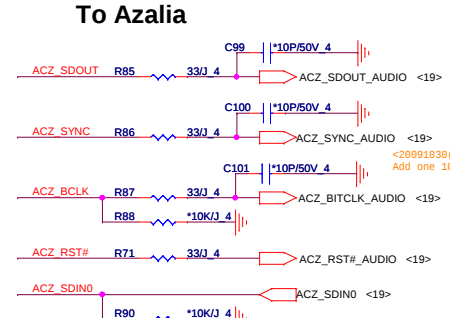
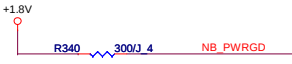
Size	Document Number	R
	RS880-HT LINK/SPMEM I/F 1/4	
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Note:Regarding LDT_STOP# signal,It's required within 40ns skew for both assertion and de-assertion between NB and CPU.







Controller	Ports mapping
OHCI0 (dev-18, fun-0)	Port 0 - 4
EHCI (dev-18, fun-2)	Port 0 - 4
OHCI0 (dev-19, fun-0)	Port 5 - 9
EHCI (dev-19, fun-2)	Port 5 - 9
OHCI0 (dev-22, fun-0)	Port 10 - 14
EHCI (dev-22, fun-2)	Port 10 - 14

MM-SIM
CONN (Lower Right)
CONN (Upper Right)

BTMNCCCDMPCCardCONNCONN

EC_PWM

2

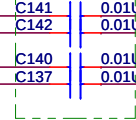
SATA PORT 0,1,2,3
can support AHCI
mode

SATA HDD

<22> SATA_TXP0
<22> SATA_TXN0

<22> SATA_RXN0
<22> SATA_RXP0

PLACE SATA AC COUPLING
CAPS CLOSE TO SB820



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

+1.1V_SB_VDDAN_11_SATA



To meet SB800 SCL1.02:
DNI SATA XTAL circuit's parts

<22> SATALED#

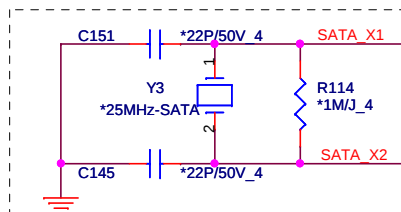
+3V

R304

10K/J 4

AD11

SATA_ACT#/GPIO67



T67
T12
T11
T65
T66

USB

SB800
Part 2 of 5

SERIAL ATA

HW MONITOR

SPI ROM

SB820M

The flash controller function is NOT
supported by the SB820M.

FC_CLK AH28
FC_FBCLKOUT AG28
FC_FBCLKIN AF26

FC_OE#/GPIO145 AF28
FC_AVD#/GPIO146 AG29
FC_WE#/GPIO148 AG26
FC_CE1#/GPIO149 AE27
FC_CE2#/GPIO150 AE29
FC_INT1#/GPIO144 AE29
FC_INT2#/GPIO147 AH27

FC_ADQ0#/GPIO128 AJ27
FC_ADQ1#/GPIO129 AJ26
FC_ADQ2#/GPIO130 AH25
FC_ADQ3#/GPIO131 AH24
FC_ADQ4#/GPIO132 AG23
FC_ADQ5#/GPIO133 AH23
FC_ADQ6#/GPIO134 AJ22
FC_ADQ7#/GPIO135 AG21
FC_ADQ8#/GPIO136 AE21
FC_ADQ9#/GPIO137 AH22
FC_ADQ10#/GPIO138 AJ23
FC_ADQ11#/GPIO139 AE23
FC_ADQ12#/GPIO140 AJ24
FC_ADQ13#/GPIO141 AJ25
FC_ADQ14#/GPIO142 AG25
FC_ADQ15#/GPIO143 AH26

FANOUT0#/GPIO52 W5
FANOUT1#/GPIO53 W6
FANOUT2#/GPIO54 Y9

FANIN0#/GPIO56 W7
FANIN1#/GPIO57 V9
FANIN2#/GPIO58 W8

TEMPIN0#/GPIO171 B6
TEMPIN1#/GPIO172 A6
TEMPIN2#/GPIO173 A5
TEMPIN3/TALERT#/GPIO174 B5
TEMP_COMM C7

VIN0#/GPIO175 A3
VIN1#/GPIO176 B4
VIN2#/GPIO177 A4
VIN3#/GPIO178 C5
VIN4#/GPIO179 A7
VIN5#/GPIO180 B7
VIN6/GBE_STAT3#/GPIO181 B8
VIN7/GBE_LED3#/GPIO182 A8

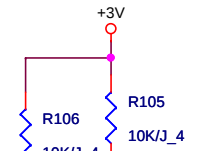
NC1
NC2

T45
T31
T39

T38
T37
T36
T43
T44
T32
T33

T42
T30
T29
T28
T23
T24
T21
T16
T80
T20
T25
T84
T34
T35
T40
T41

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY



SB_PROCHOT# <4>

THERM_ALERT# <4>

<20100119(B2A)_Bimini Rev1.4>
Non-stuff R408 ; stuff R409
(Nile doesn't support VDDR = +1.05V for DDR3-1333)

MEM_1V5 <10>



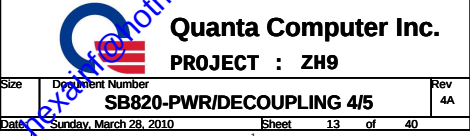
Quanta Computer Inc.
PROJECT : ZH9

Size	Document Number	Rev
	SB820-SATA/HWM/SPI 3/5	4A
Date:	Sunday, March 28, 2010	Sheet 12 of 40

SB800 Part 3 of 5

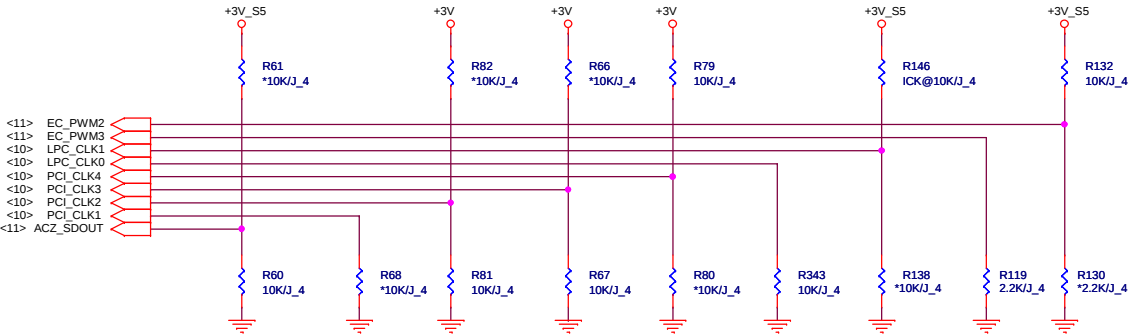
DDIO_33_PCGIPG_1	CORE S0	VDDCR_11
DDIO_33_PCGIPG_2		VDDCR_11
DDIO_33_PCGIPG_3		VDDCR_11
DDIO_33_PCGIPG_4		VDDCR_11
DDIO_33_PCGIPG_5		VDDCR_11
DDIO_33_PCGIPG_6		VDDCR_11
DDIO_33_PCGIPG_7		VDDCR_11
DDIO_33_PCGIPG_8		VDDCR_11
DDIO_33_PCGIPG_9		VDDCR_11
DDIO_33_PCGIPG_10		VDDCR_11
DDIO_33_PCGIPG_11		VDDAN_11_CLK_
DDIO_33_PCGIPG_12		

PCI/GPIO I/O



STANDARD STRAPS

<20091202(A1A)_Confirm with AMD's Horace>
PCI_CLK4 PU with 10K for both internal and external CLK Gen.



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM3	EC_PWM2
PULL HIGH	LOW POWER MODE	PCIe Gen II	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLK MODE ICK@DEFAULT	EC ENABLED	CLKGEN ENABLED ICK@DEFAULT	H, H=Reserved H, L=SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	PCIe Gen I	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	FUSION CLK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED ECK@DEFAULT	L, H=LPC ROM L, L=Reserved	DEFAULT

This is required as the low power mode is not supported on the SB8xx.

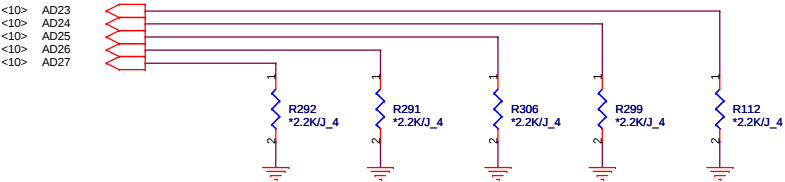
Not Applicable to SB820M--Leave provision for PD.

PCICLK4:
CPU/NB HT Clock Selection
This strap is not used if the strap CLKGEN is configured for external clock generator mode.

internal have pull Hi 10K

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

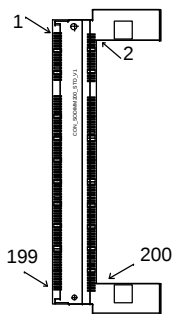


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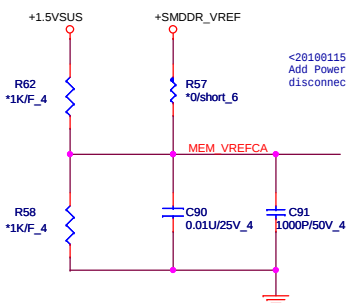
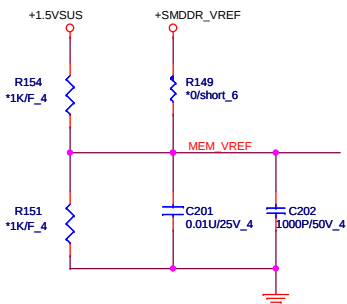
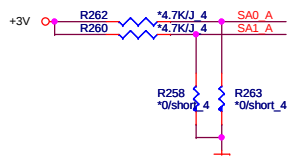
PROJECT : ZH9

Size	Document Number	Rev
	SB820-STRAPS,PWRGD 5/5	4A
Date:	Sunday, March 28, 2010	Sheet 14 of 40

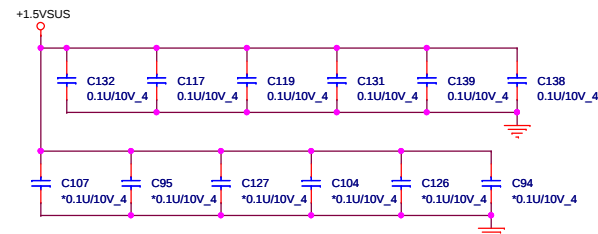
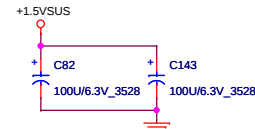
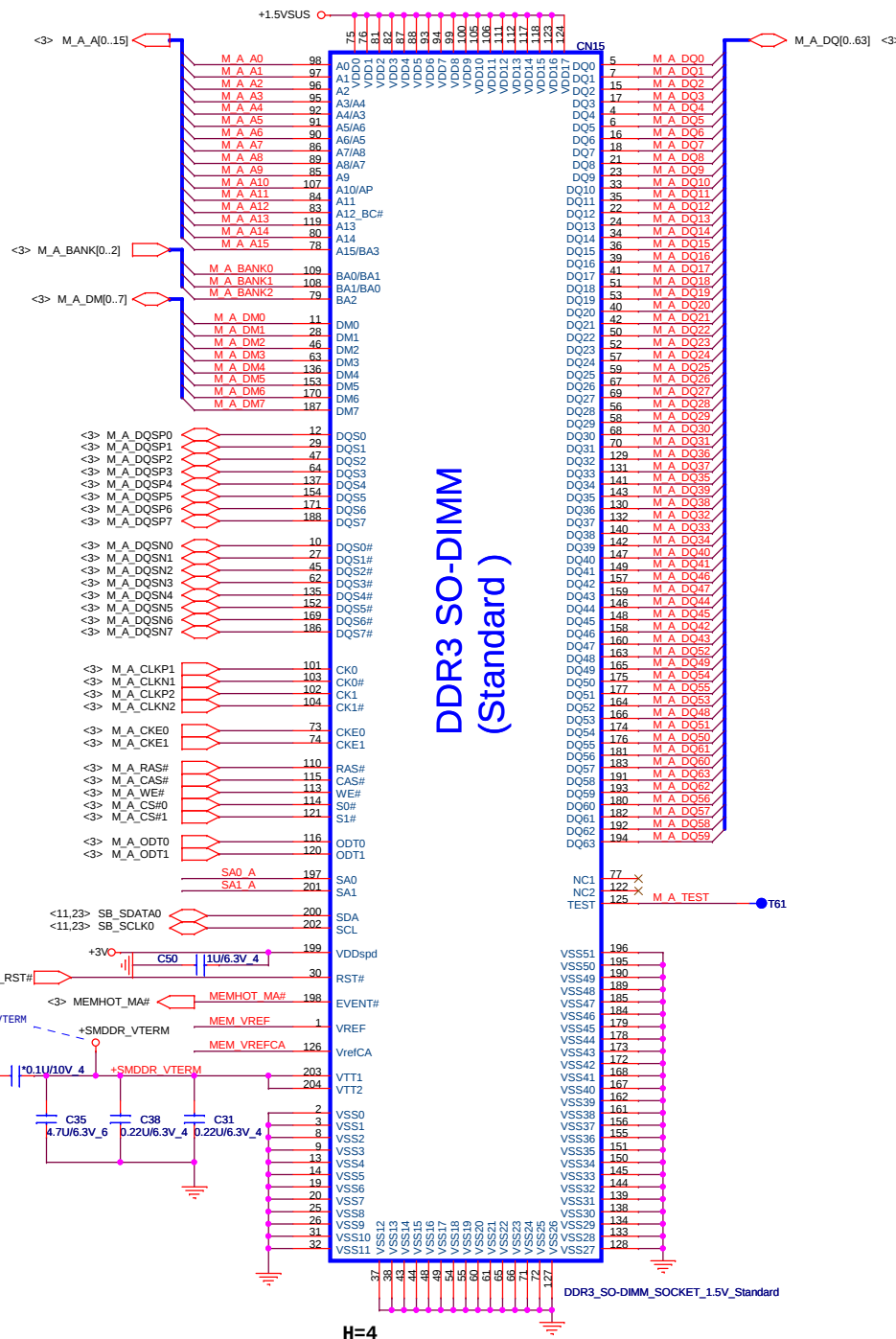
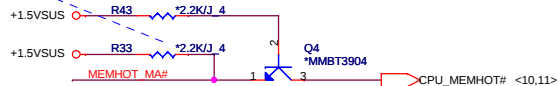
Standard Connector



SMbus address A0

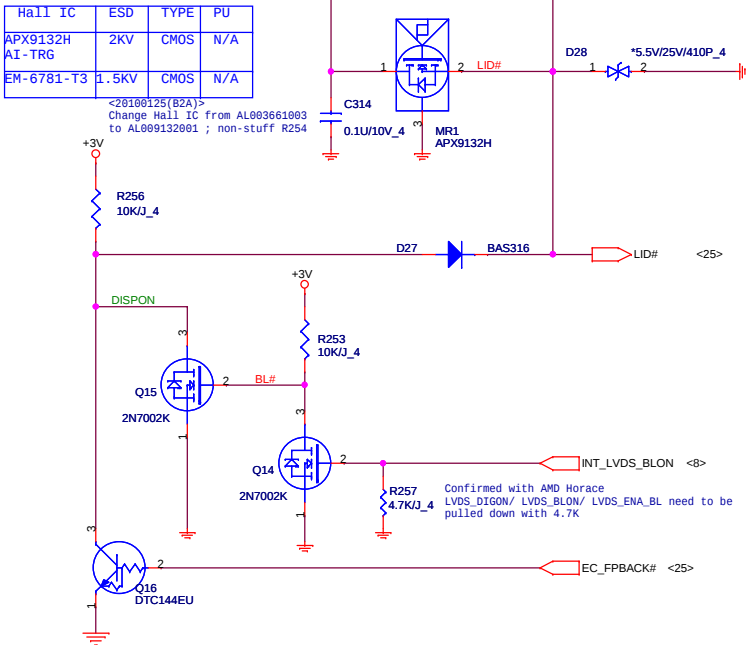


Confirmed with AMD FAE Reden
MA_EVENT_L should be PU(R8084) with 2.2K, not 1K
Not installed by default

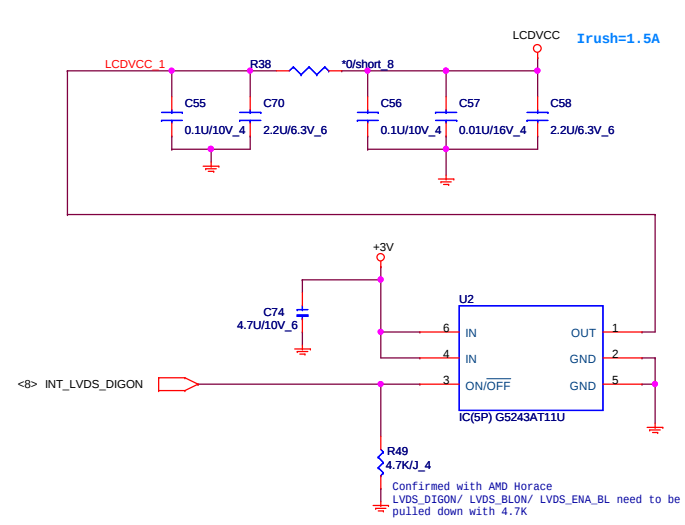


+SMDDR_VTERM <30>
+SMDDR_VREF <30>

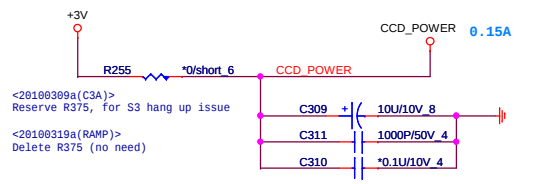
HALL IC(HSR)



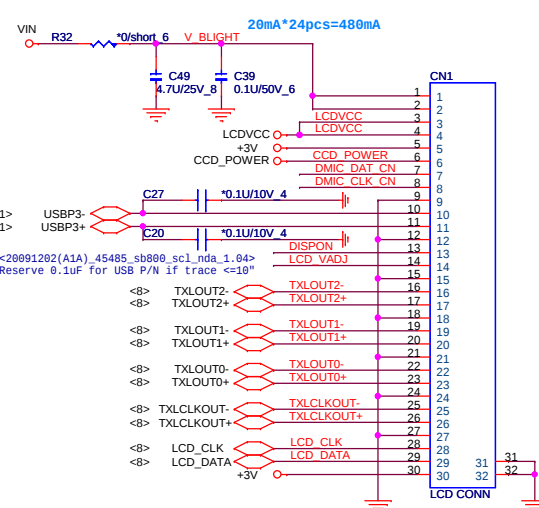
LCD POWER SWITCH(LDS)



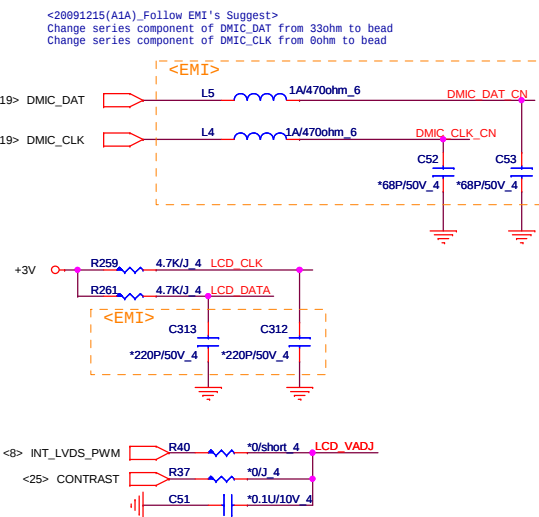
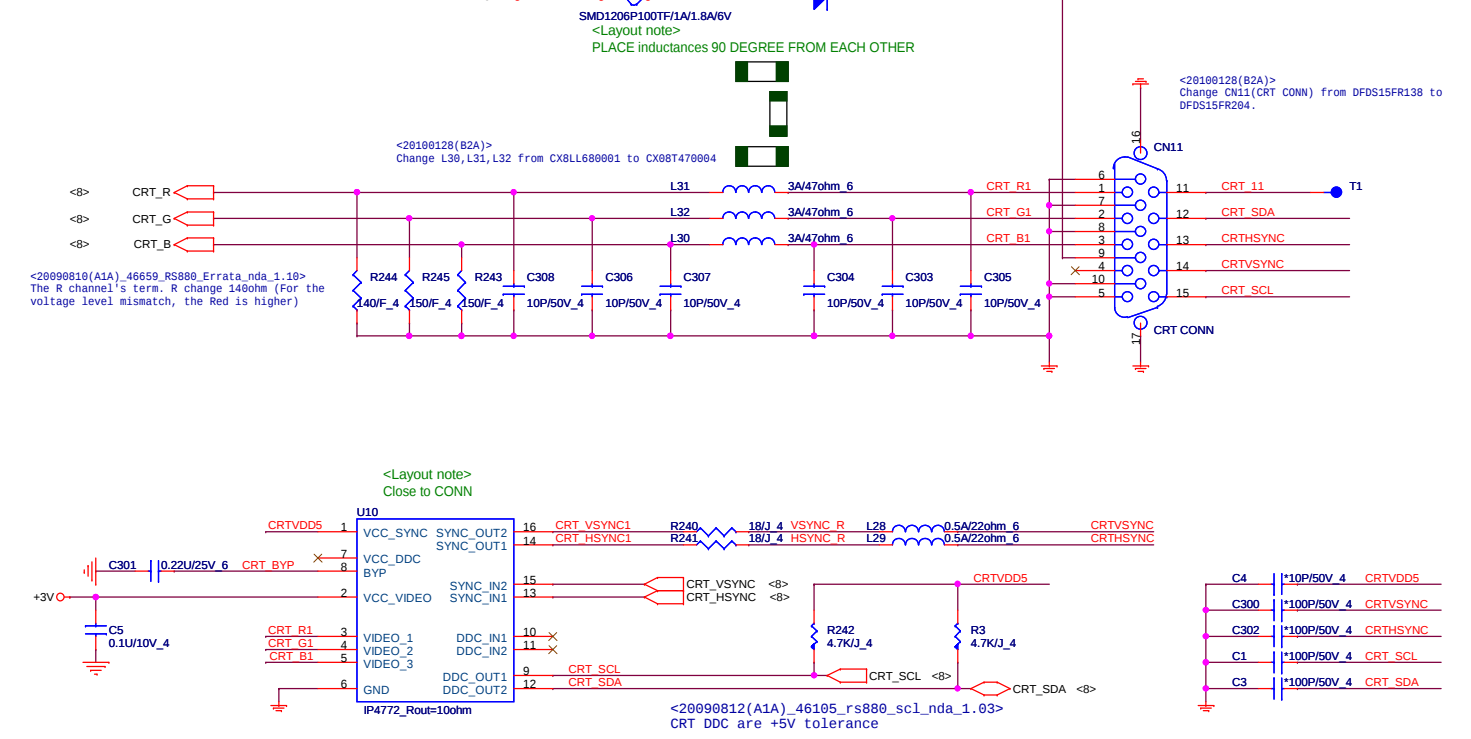
CAMERA POWER(CCD)



LCD MODULE(LDS)



CRT(CRT)





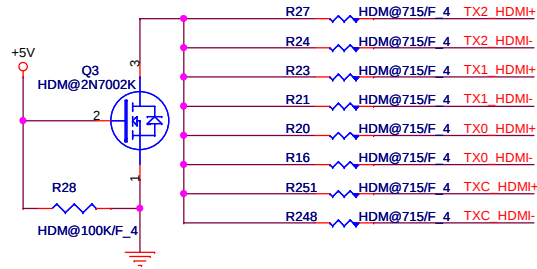
Quanta Computer Inc.

PROJECT : ZH9

Size	Document Number	Rev
	CRT/LVDS	4A
Date:	Sunday, March 28, 2010	Sheet 16 of 40

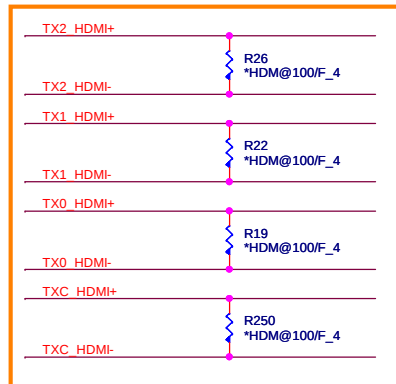
(HDM)

Close to HDMI Connector



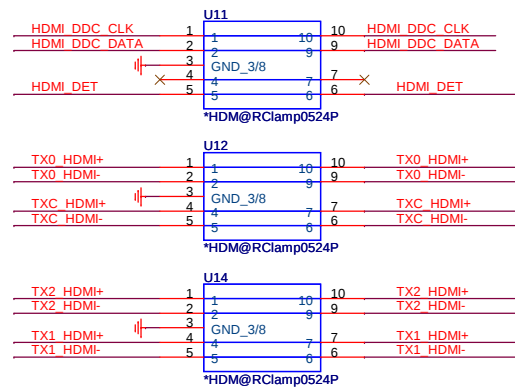
EMI reserve for HDMI(HDM)

Close connector

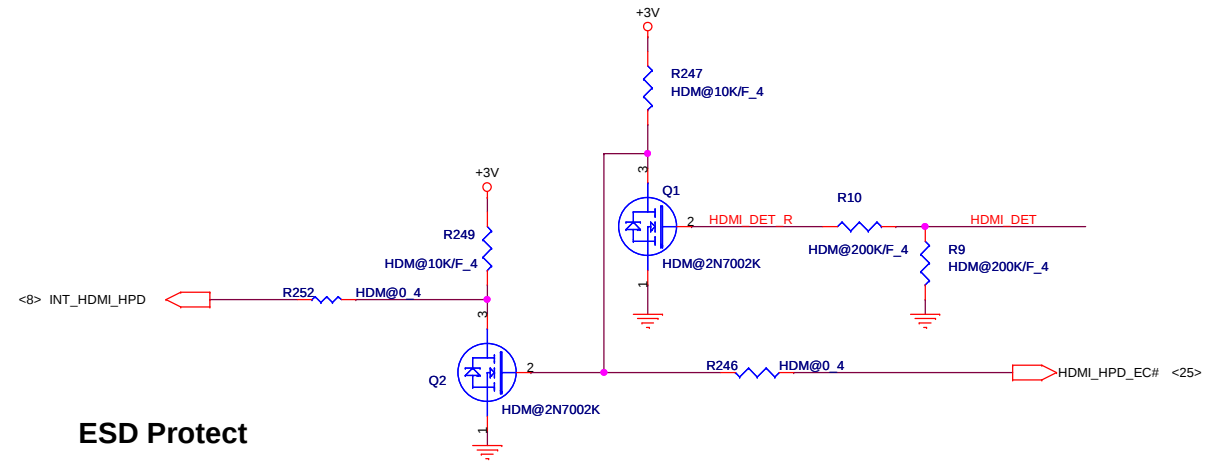


ESD Protect

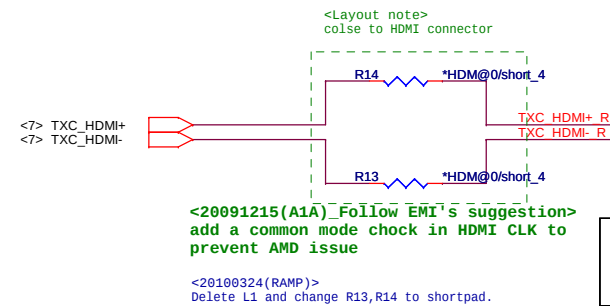
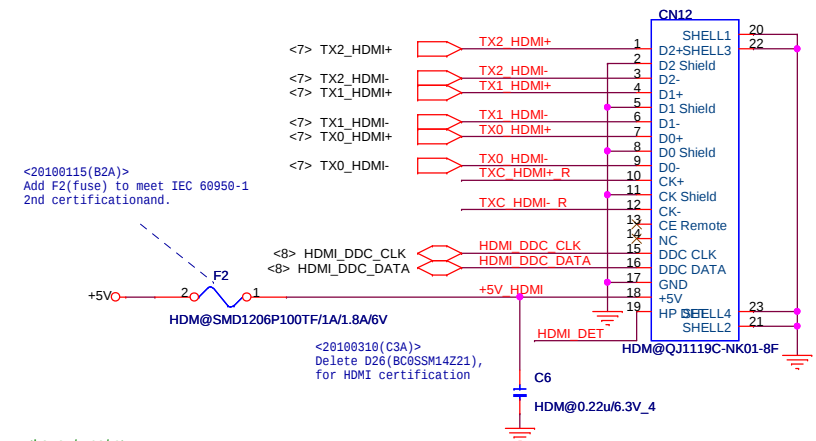
close to HDMI connector



HDMI HPD SENSE

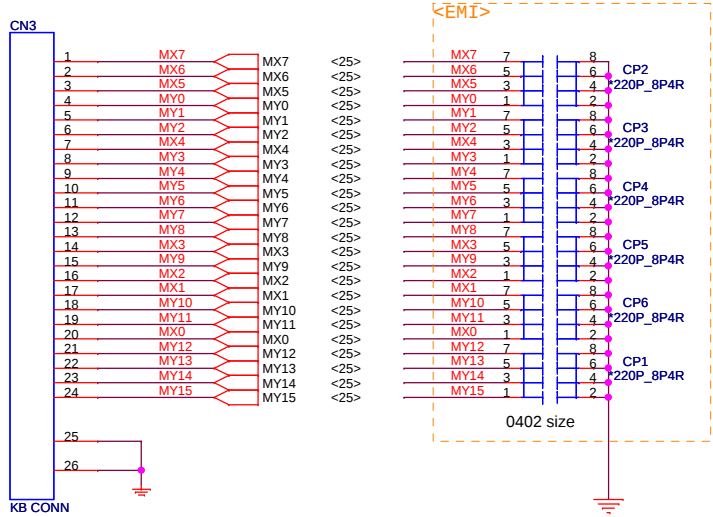


HDMI PORT



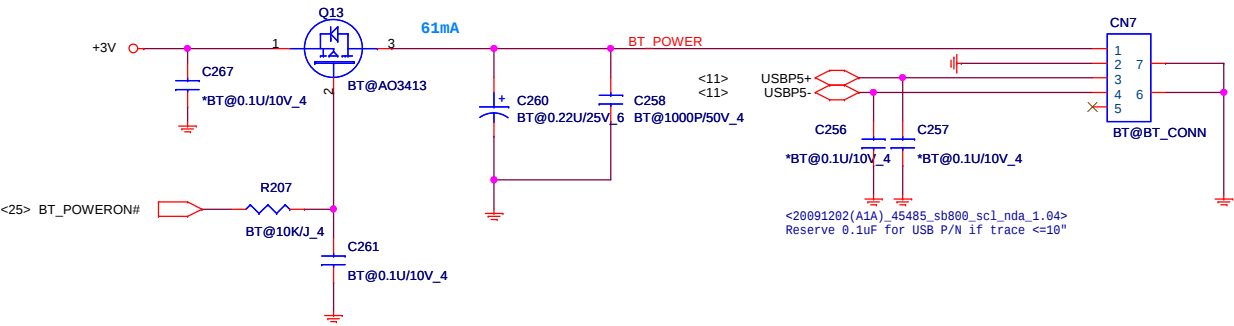
KEYBOARD(KBC)

<20100303(C3A)>
Change CP1-CP6 footprint from 8p4r-0402 to 8p4r-0402-smt, for SMT open issue.

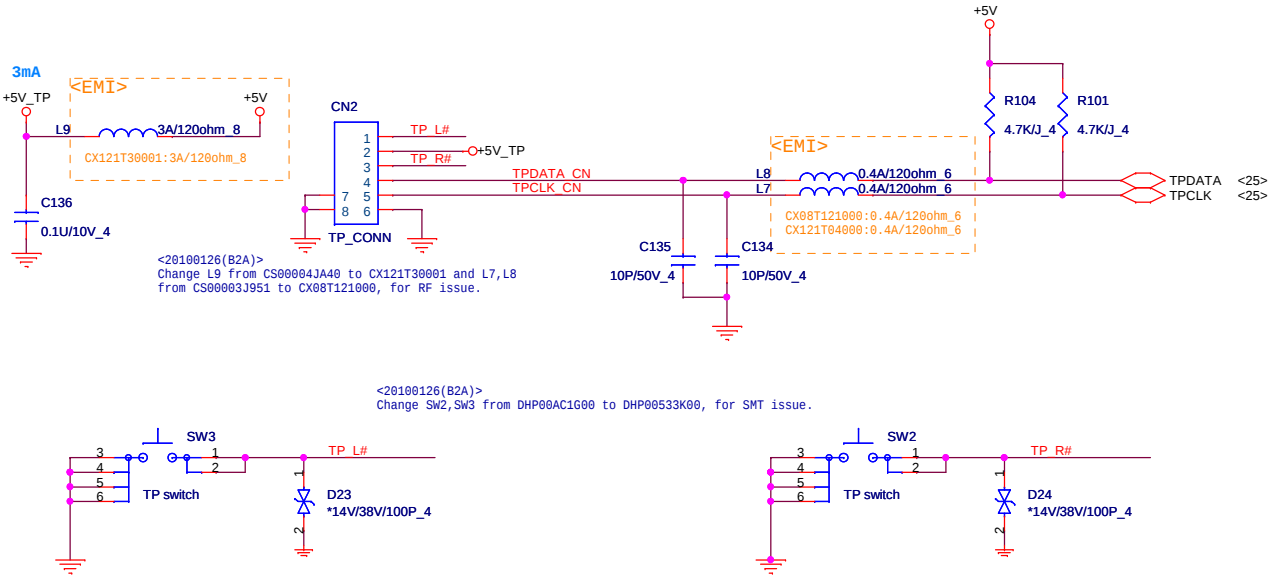


BLUETOOTH(BTM)

BT	PWR	LED
T77H056.00	+3V	
T60H928.33	+3V	



TOUCH PAD(TPD)



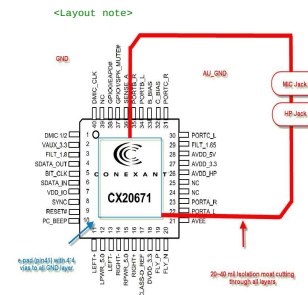
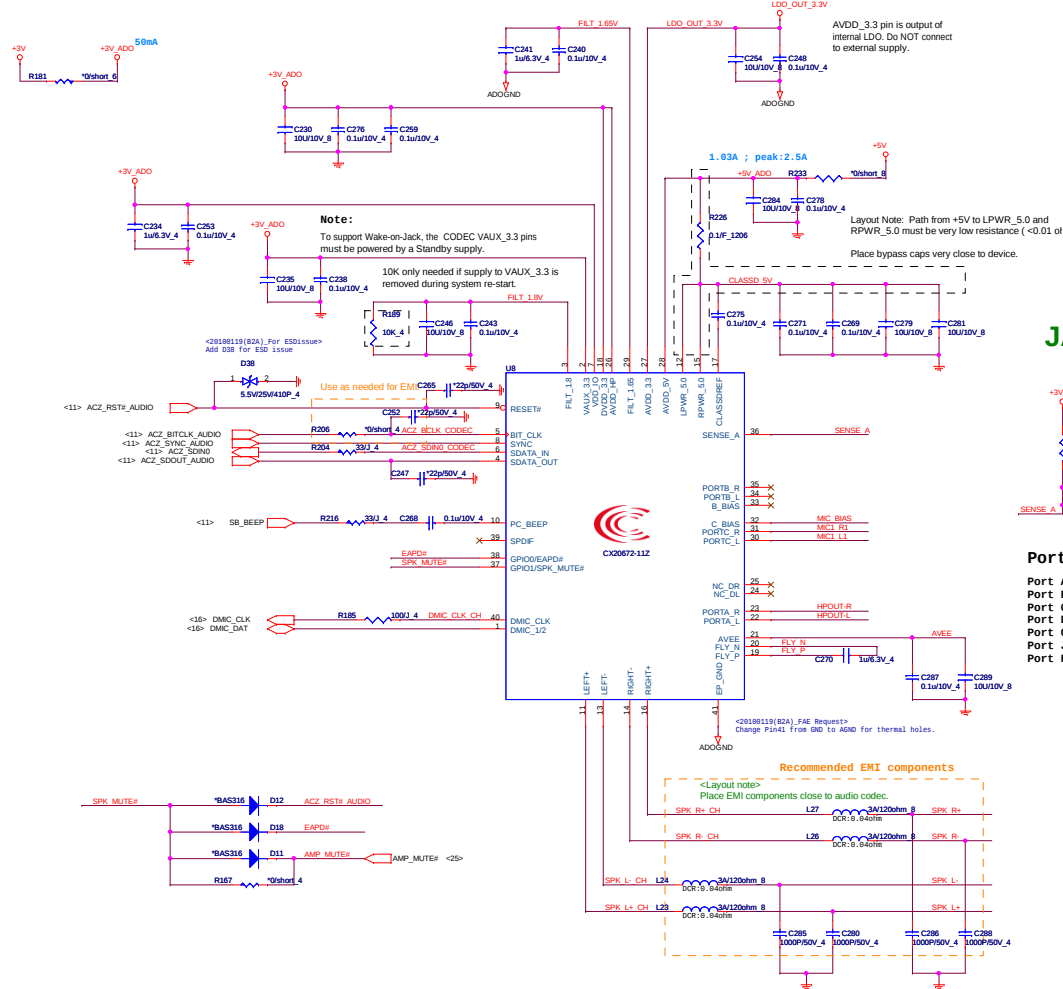


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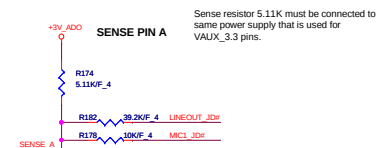
PROJECT : ZH9

Size	Document Number	Rev
	KB/BT/TP/LED/Power Connector	4A
Date:	Sunday, March 28, 2010	Sheet 18 of 40

AUDIO CODEC

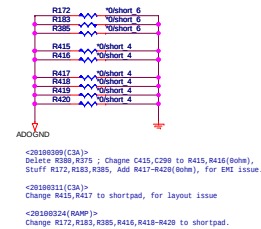


JACK DETECT RESISTORS

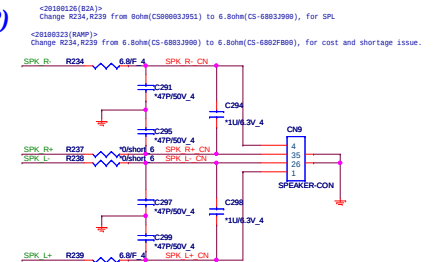


Port Configuration

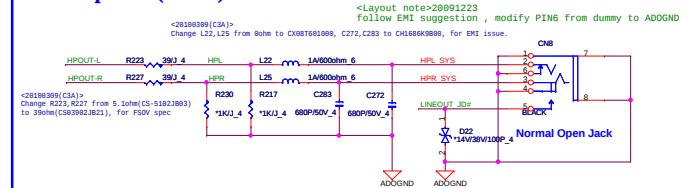
Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal analog mono mic (stereo option)/Line In
Port C: Microphone jack
Port D: LineOut jack(need cap) or Headphone jack(cap less)
Port G: Internal stereo speakers
Port J: Optional Internal stereo digital mic
Port H: S/PDIF (jack shared with headphone)



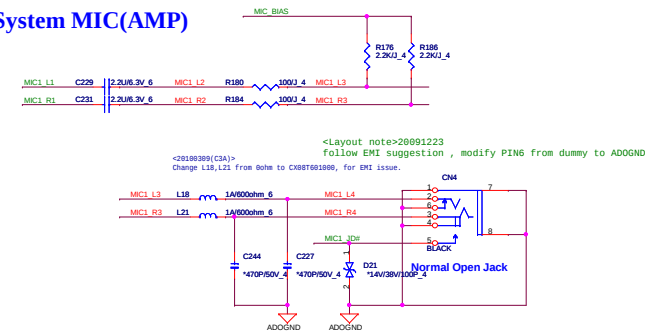
Speaker (AMP)



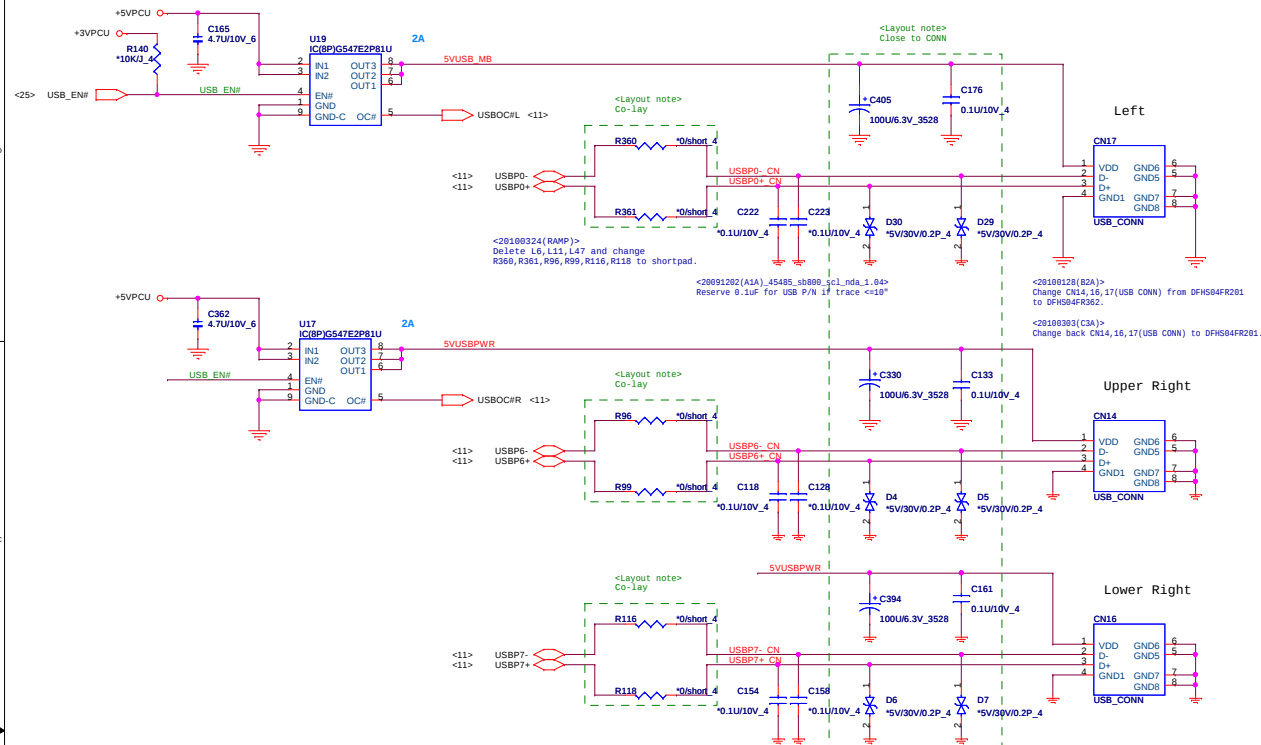
Earphone(AMP)



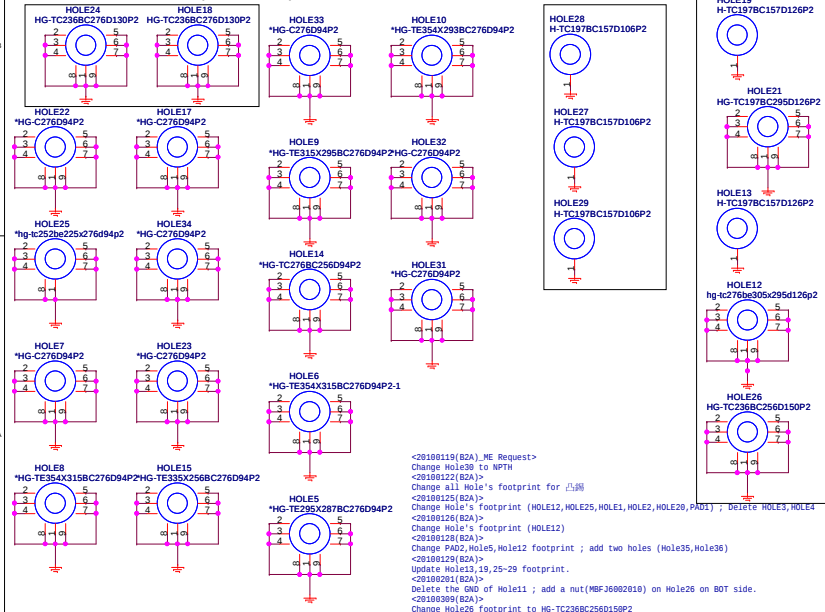
System MIC(AMP)



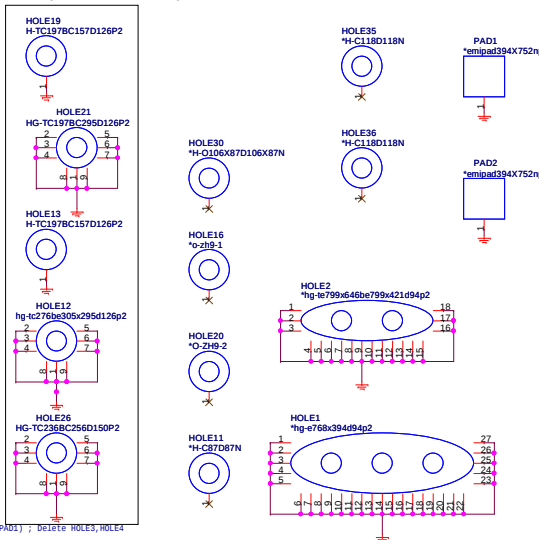
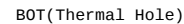
USB(USB)



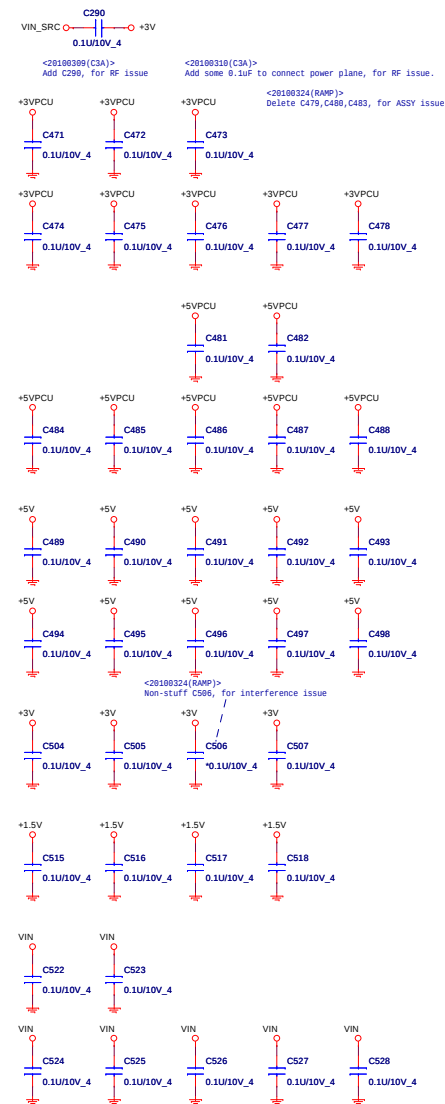
HOLE(OTH)_{TOP(HDD Hole)}



BOT
(Mini-PCIE Hole)



EMI (EMC)

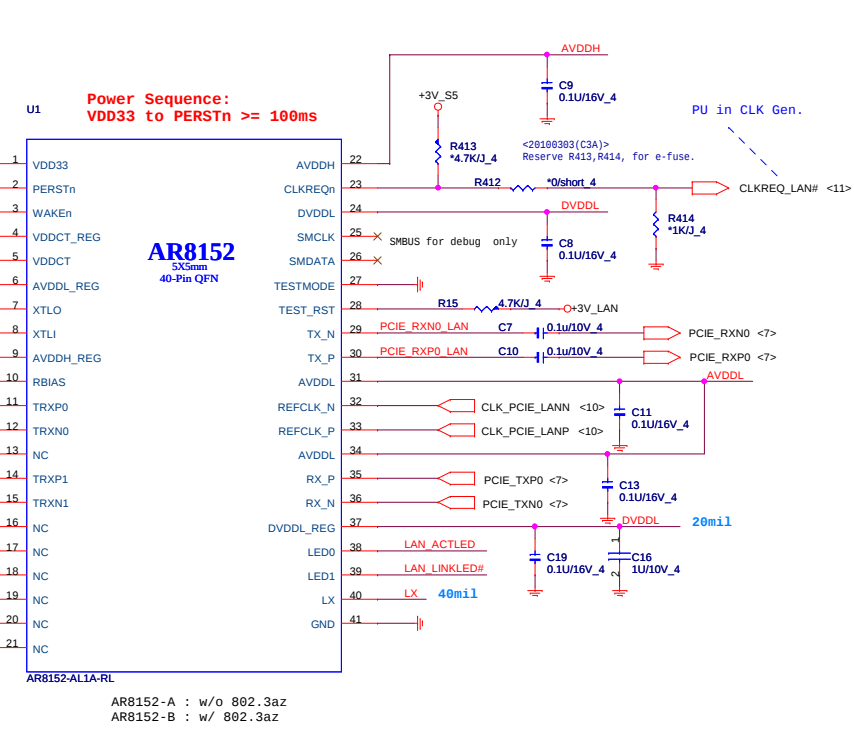
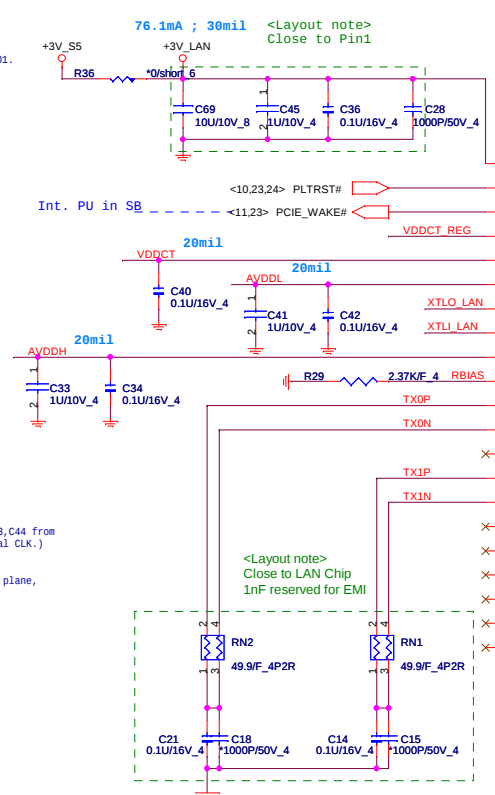
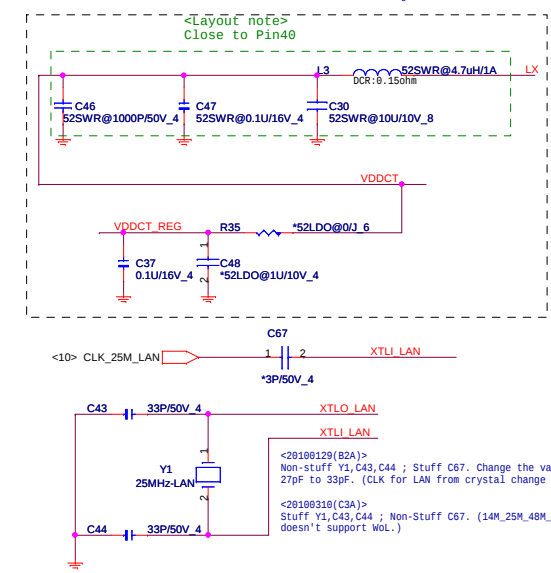


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PROJECT : ZH9

Size	Document Number	Rev
	USB on Board/LED/SW/HOLE	4A
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<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@
<20100303(C3A)_FAE's suggestion>
Change L3 from CV-4710NM63 to CV-4710T201.



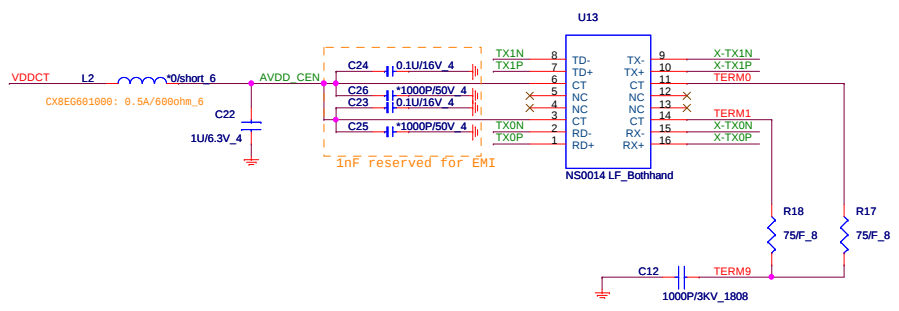
Power Sequence:
VDD33 to PERSTn >= 100ms

AR8152
5X5mm
40-Pin QFN

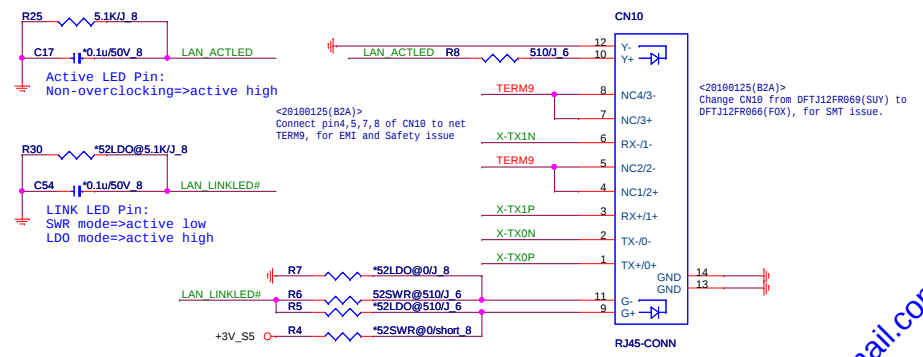
AR8152-A : w/o 802.3az
AR8152-B : w/ 802.3az

+3V_S5	1	VDD33	6	AVDDL_REG	+1.1V regulator output (For all the analog 1.1V supply pins)
+1.1V analog power	31/34	AVDDL	9	AVDDH_REG	+2.7V regulator output (Connected to pin 22)
+1.1V digital power	24	DVDDL	37	DVDDL_REG	+1.1V regulator output (For all the digital 1.1V supply pins)
+2.7V analog power	22	AVDDH	4	VDDCT_REG	+1.8V regulator output (For VDDCT when LDO mode)
+1.7V analog power	5	VDDCT	40	LX	+1.7V Switching regulator (For VDDCT when switching mode)

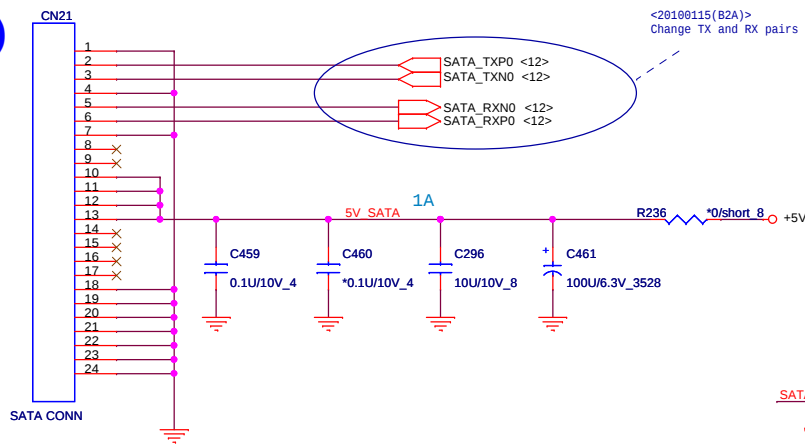
TRANSFORMER



RJ45



2.5" SATA HDD(HDD)

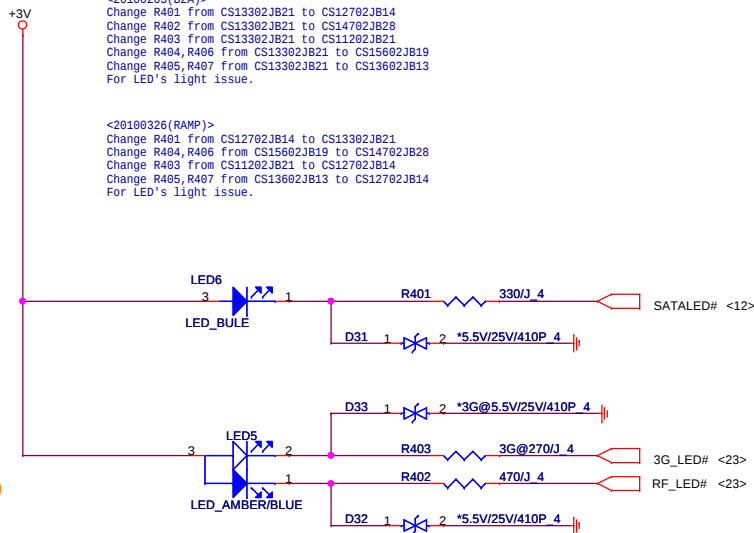


LED/SW(UIF)

<20091214(A1A)_Confirm with Acer Johnson_Yeh>
The JV01_NL and SJV01_NL had 4 LEDs --> Power / Battery / HDD / Communication

<20100203(B2A)>
Change R401 from CS13302JB21 to CS12702JB14
Change R402 from CS13302JB21 to CS14702JB28
Change R403 from CS13302JB21 to CS11202JB21
Change R404, R406 from CS13302JB21 to CS15602JB19
Change R405, R407 from CS13302JB21 to CS13602JB13
For LED's light issue.

<20100326(RAMP)>
Change R401 from CS12702JB14 to CS13302JB21
Change R404, R406 from CS15602JB19 to CS14702JB28
Change R403 from CS11202JB21 to CS12702JB14
Change R405, R407 from CS13602JB13 to CS12702JB14
For LED's light issue.



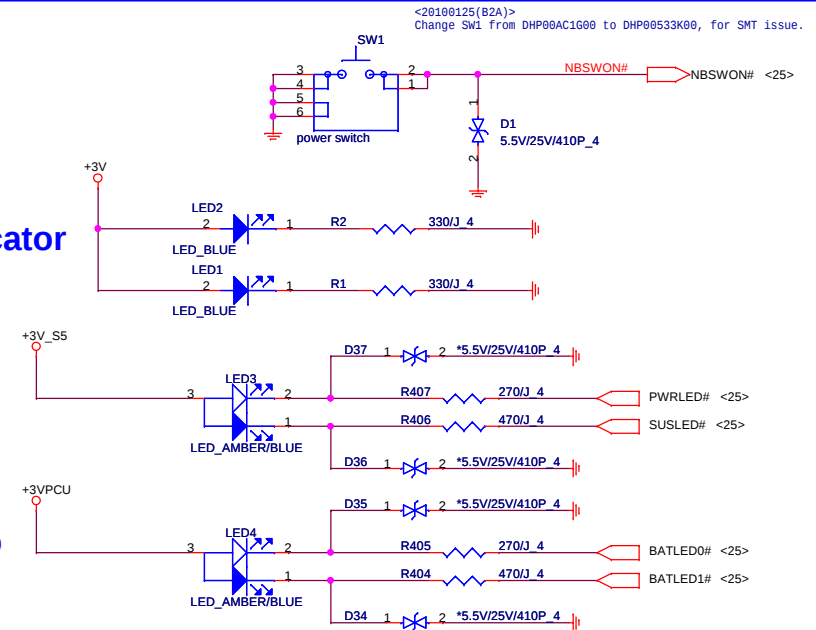
ID(Left-->Right)
Power LED/BATT LED/HDD LED/WiFi LED

<LED spec>
BLUE :
Vf = 2.7~3.2V ; If = 5mA
BLUE/ORANGE :
BH-Vf = 2.7~3.7V ; If = 20mA max=25mA
S2-Vf = 1.7~2.4V ; If = 20mA max=25mA

PWR indicator

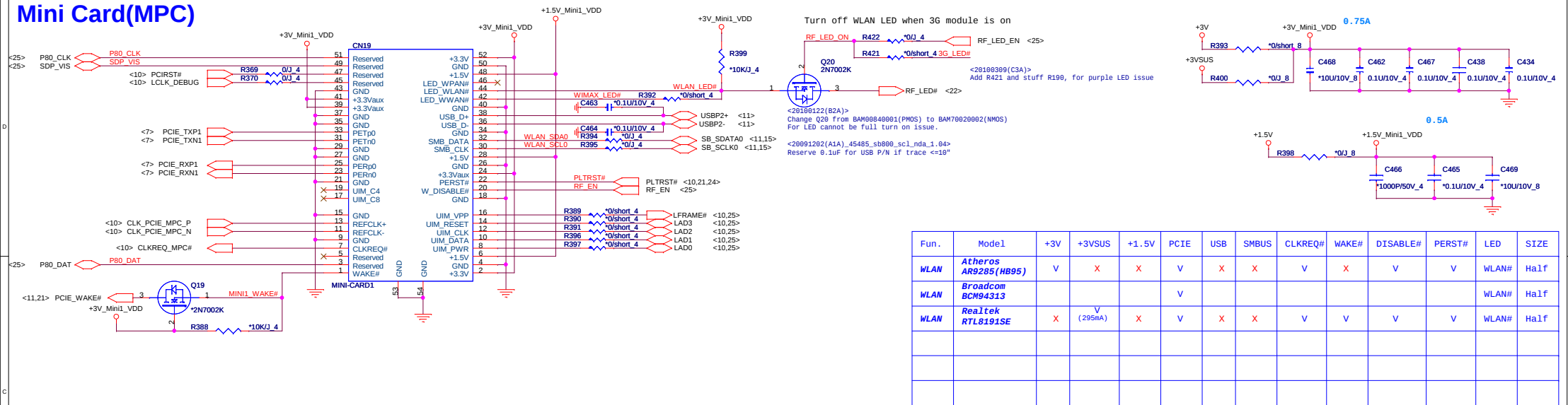
PWR LED SUS LED

FULL LED CHG LED

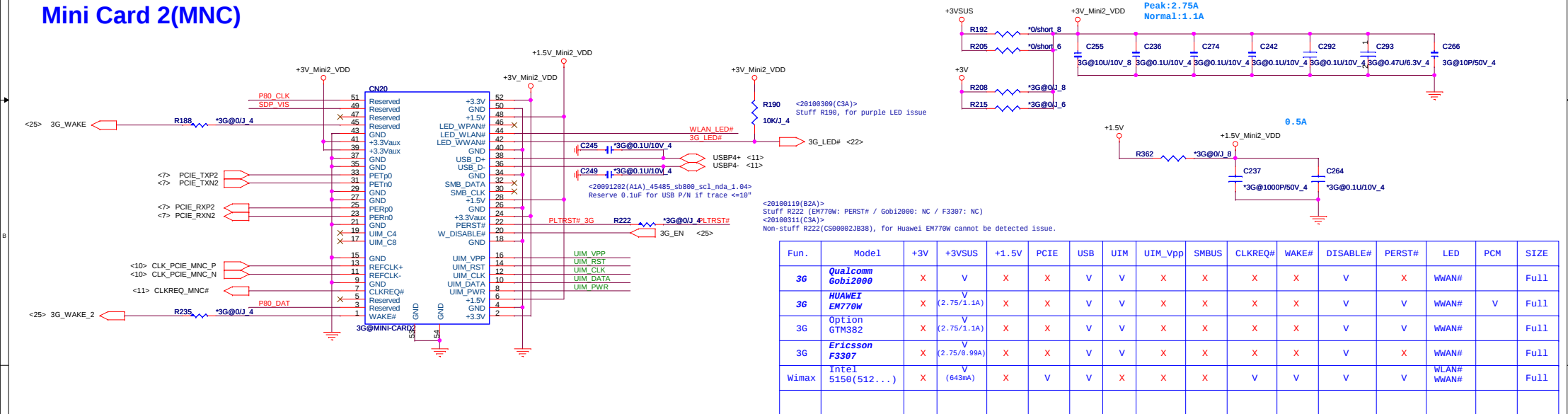


		Quanta Computer Inc. PROJECT : ZH9	
		SATA HDD/LED/SW	
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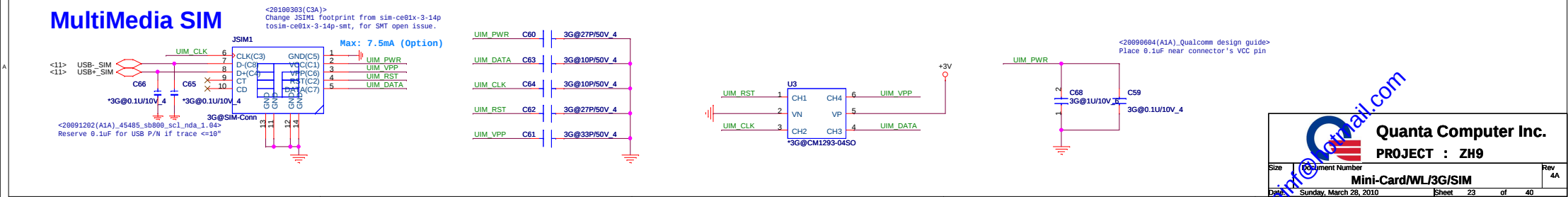
Mini Card(MPC)



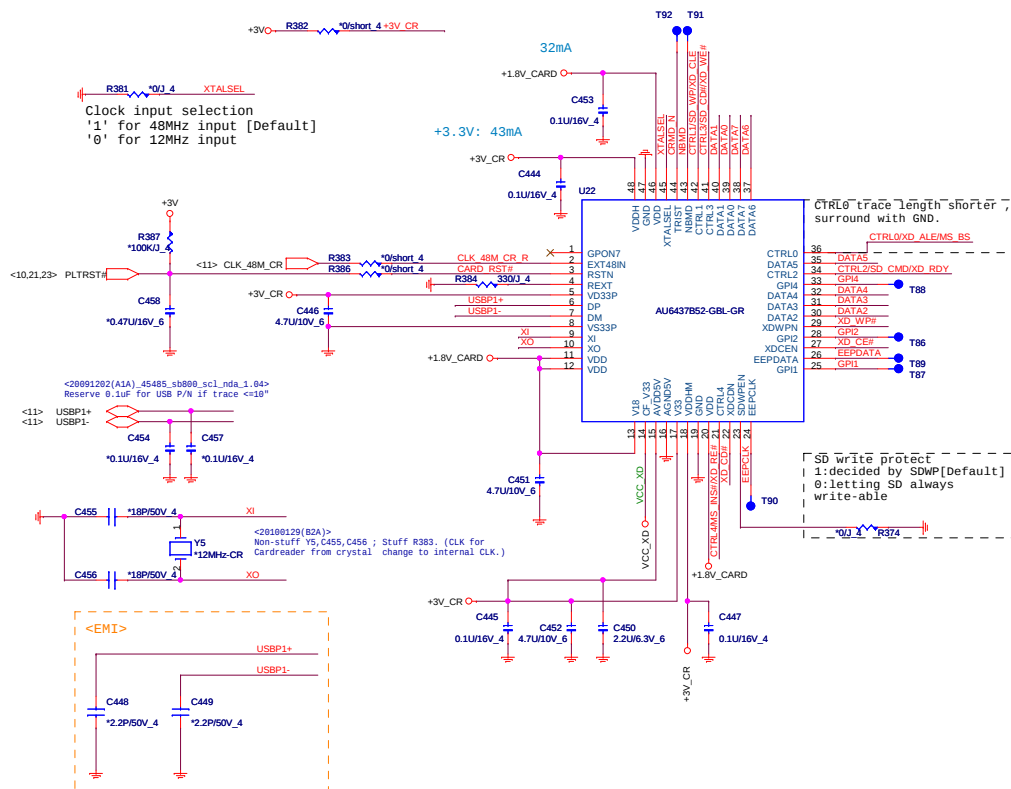
Mini Card 2(MNC)



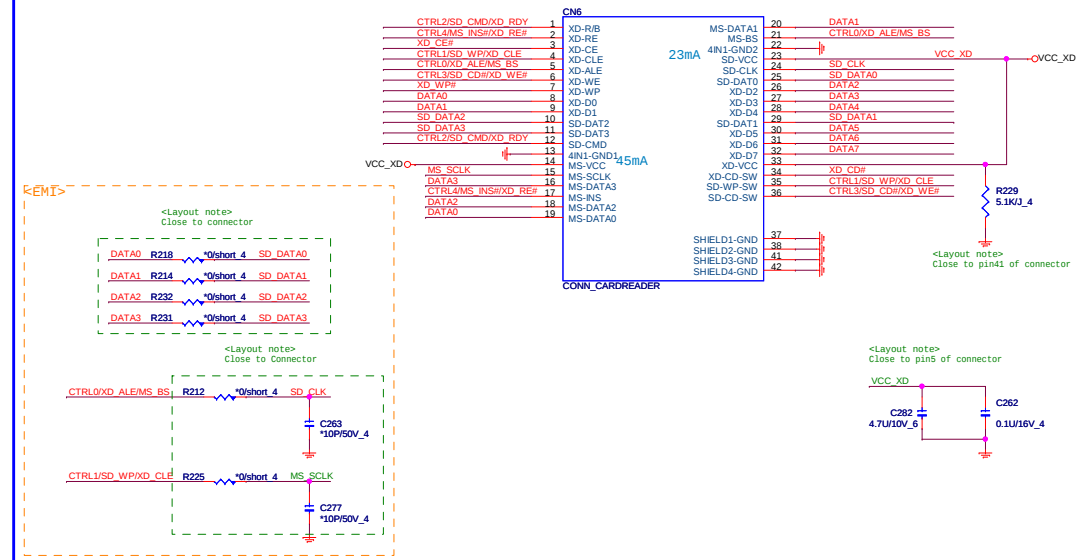
MultiMedia SIM



AU6437B52-GBL-GR (MMC)



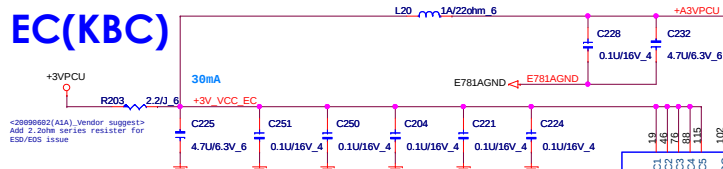
4 IN 1 CARD READER (MMC)



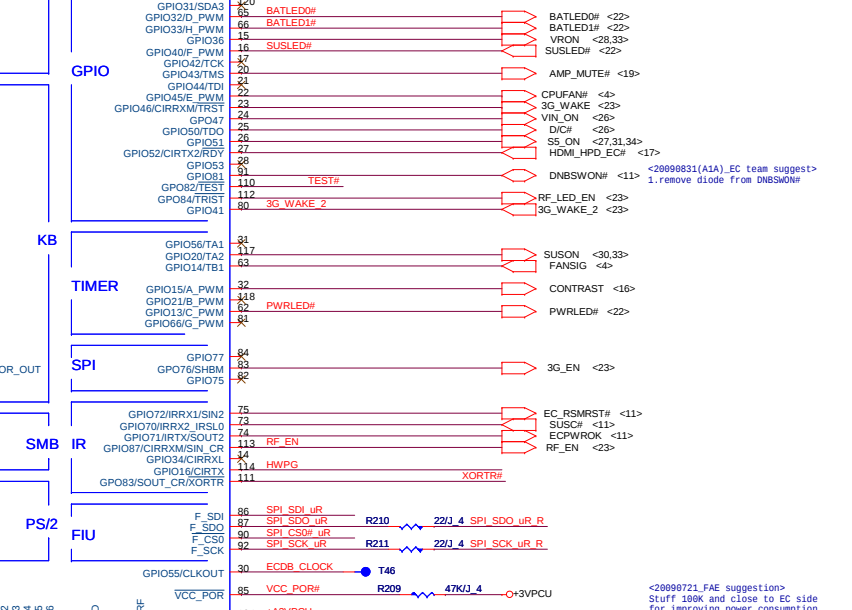
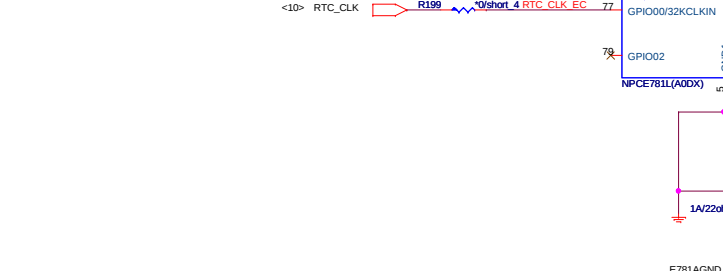
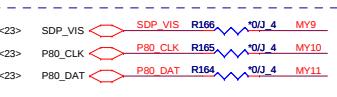
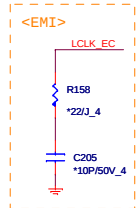
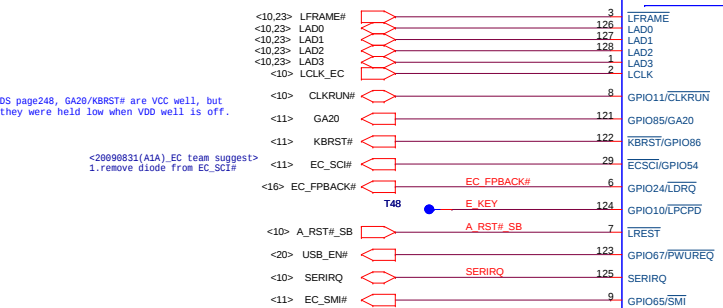
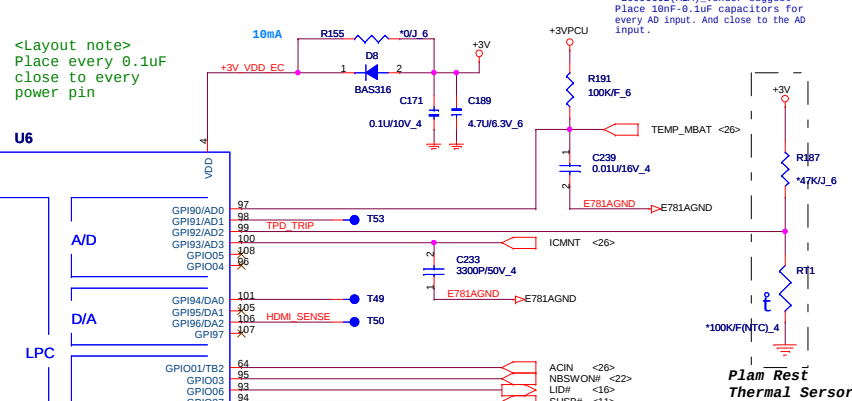
Quanta Computer Inc.
PROJECT : ZH9

Size	Document Number	Rev
	AU6437 (Card Reader)	4.
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EC(KBC)



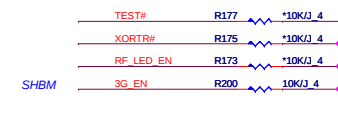
<Layout note>
Place every 0.1uF
close to every
power pin



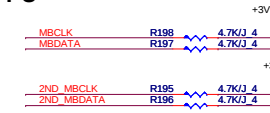
I/O ADDRESS SETTING

TEST Mode	TEST#	XORT#	TRIST#
no test mode selected (normal operation)	1	X	X
XOR-tree test mode	0	0	1
ICT mode	0	1	0
Reserved exclusively for Nuvoton use	0	00 or 11	

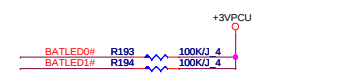
SHBM=0: Enable shared memory with host BIOS



SM BUS PU

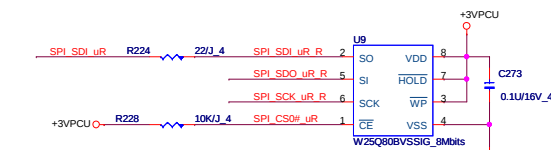


```
1ST: Battery
2ND: CPU Thermal Sensor / DTS
3RD: VGA Thermal Sensor
```



<20090831(A1A)_EC team suggest>
1.change R7027/R7028 to 1M or 100K ohm
2.change PWR/SUS LED's power from +3VPC
can reduce pull-high resistor of SUSLED

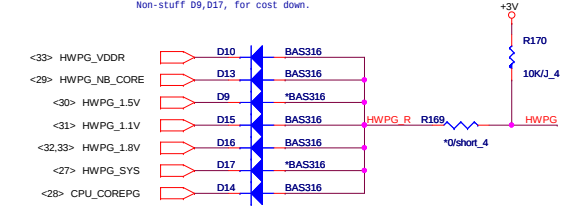
SPI FLASH



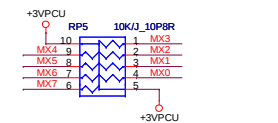
1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the
flash device should be 50MHz (or faster)

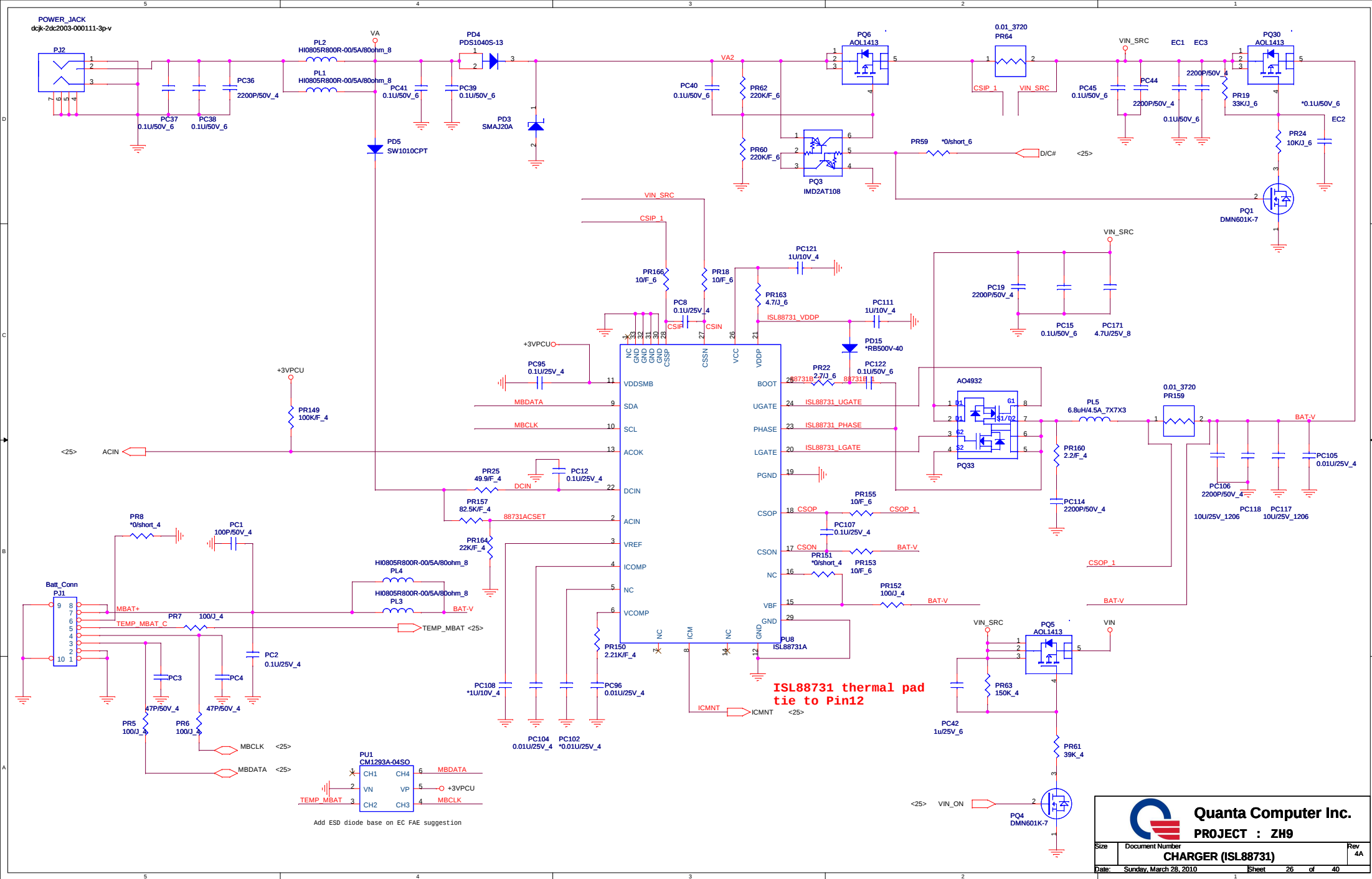
HWPG

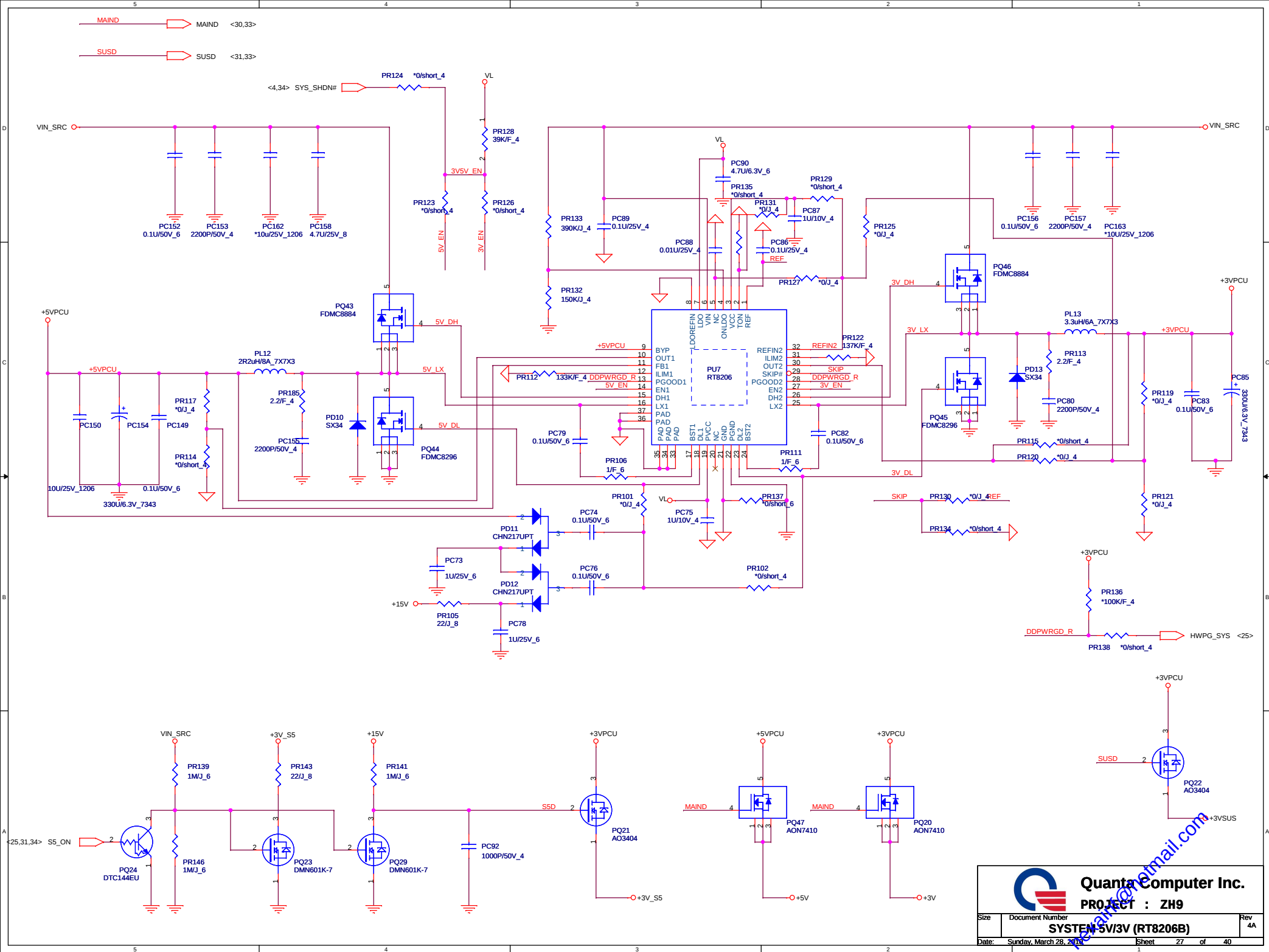
<20100319(RAMP)>
Non-stuff D9,D17, for cost down.

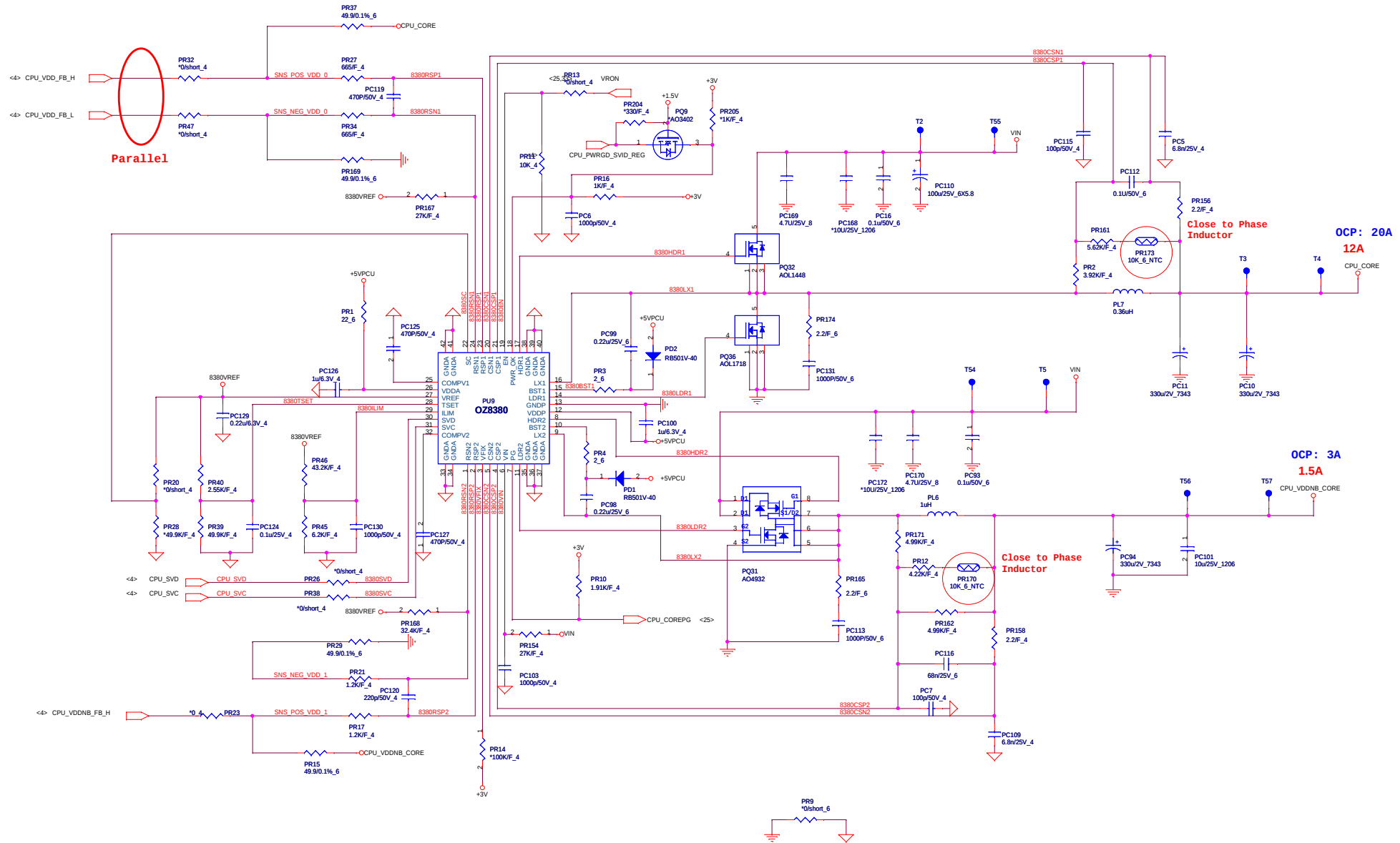


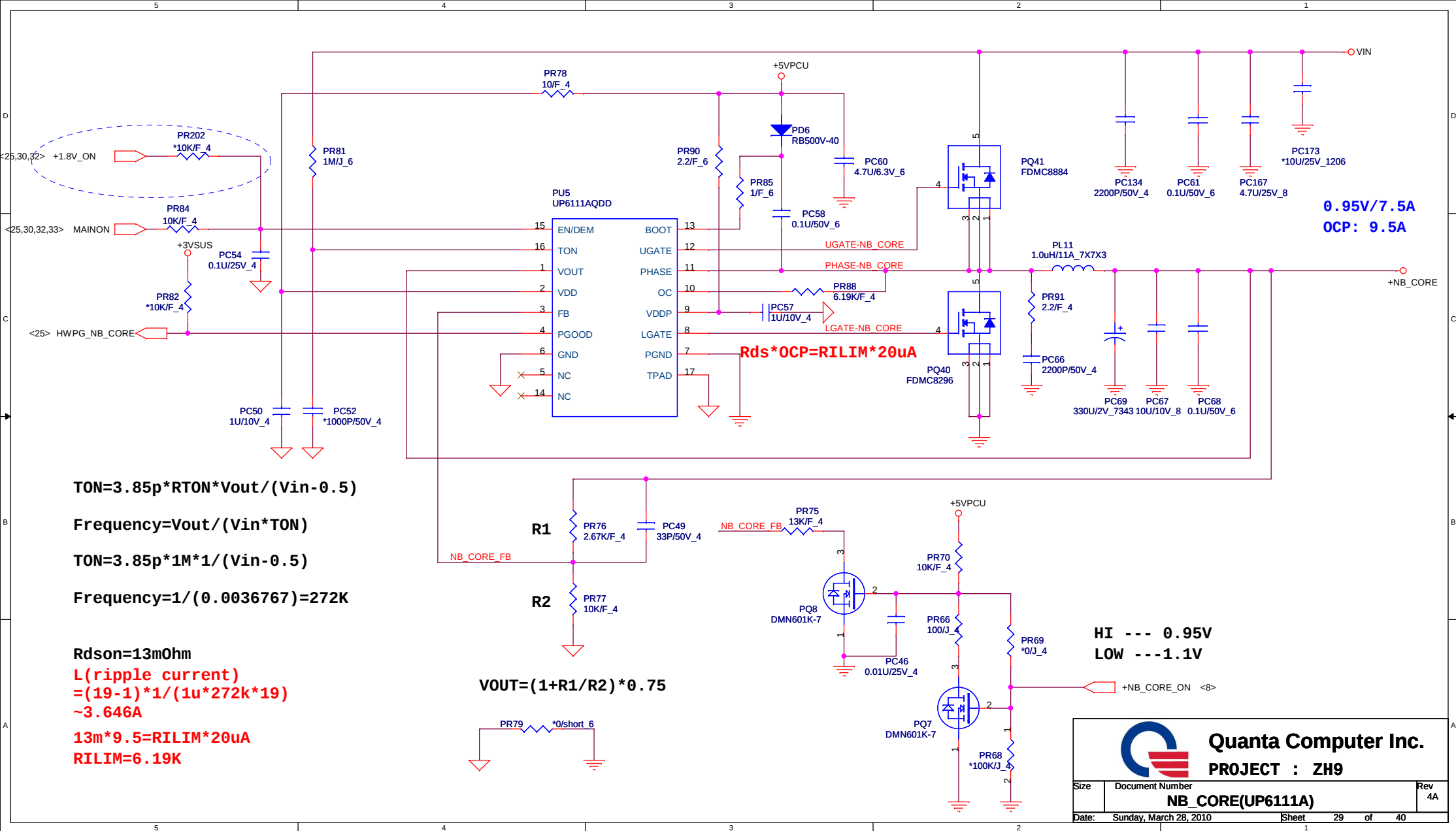
INTERNAL KEYBOARD STRIP SET



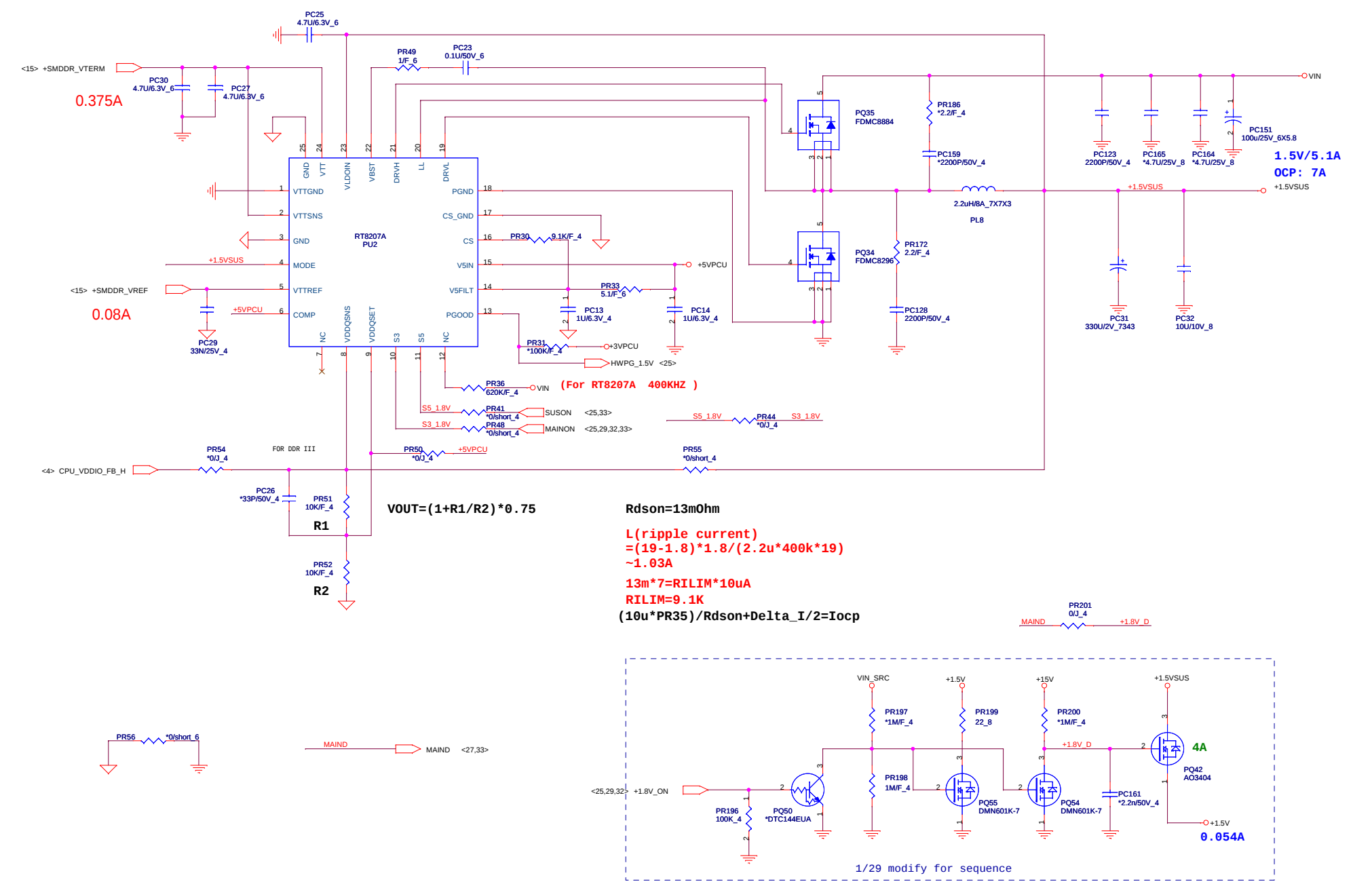








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0.375A

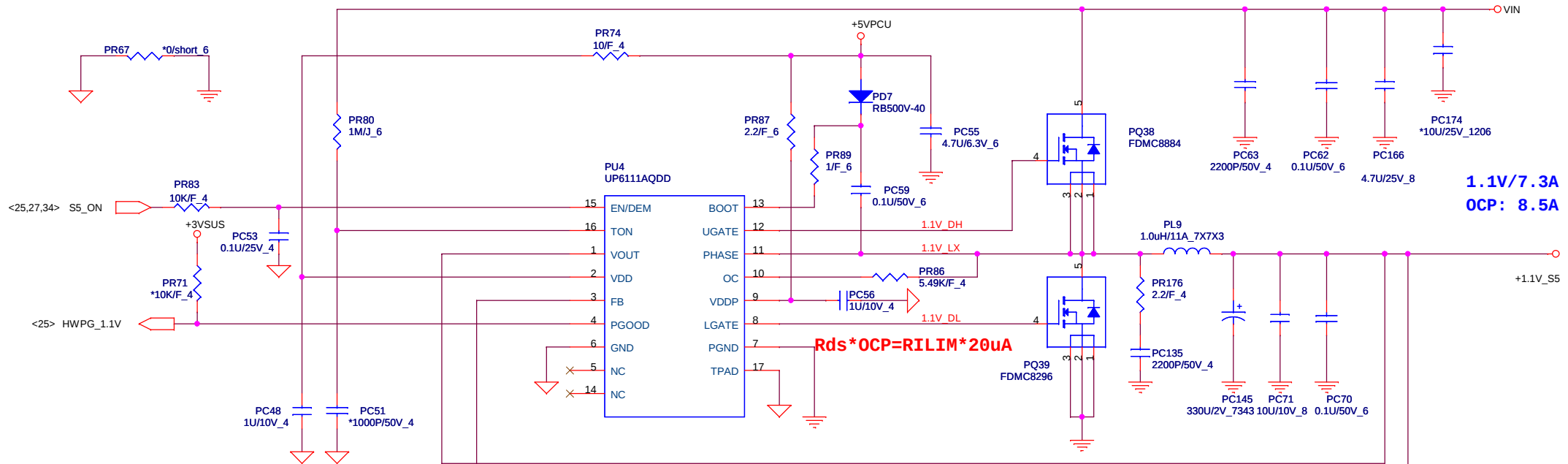
0.08A

1.5V/5.1A
OCP: 7A

$V_{OUT} = (1 + R1/R2) * 0.75$

$R_{ds(on)} = 13m\Omega$
 $L(\text{ripple current}) = (19 - 1.8) * 1.8 / (2.2u * 400k * 19) \sim 1.03A$
 $13m * 7 = RILIM * 10uA$
 $RILIM = 9.1K$
 $(10u * PR35) / R_{ds(on)} + \Delta I / 2 = I_{ocp}$

0.054A



**1.1V/7.3A
OCP: 8.5A**

$R_{ds} * OCP = RILIM * 20\mu A$

$$VOUT = (1 + R1/R2) * 0.75$$

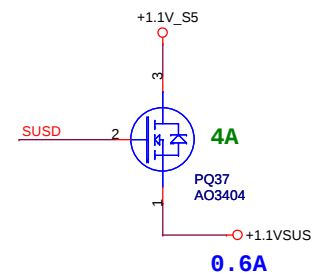
$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

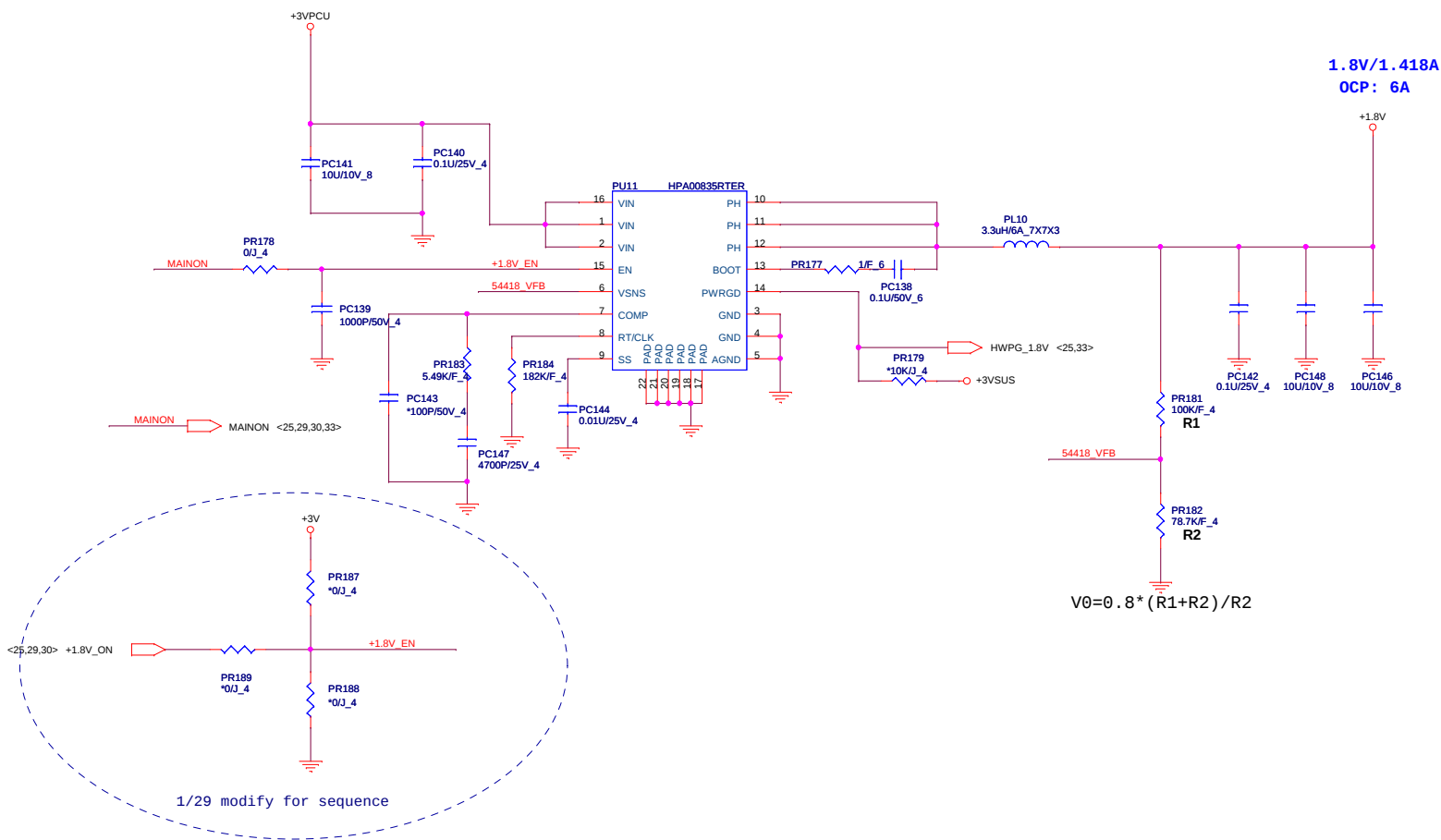
$R_{dson} = 13m\Omega$
 $L(\text{ripple current})$
 $= (19 - 1.1) * 1.1 / (1\mu * 272k * 19)$
 $\sim 3.81A$
 $13m * 8.5 = RILIM * 20\mu A$
 $RILIM = 5.49K$

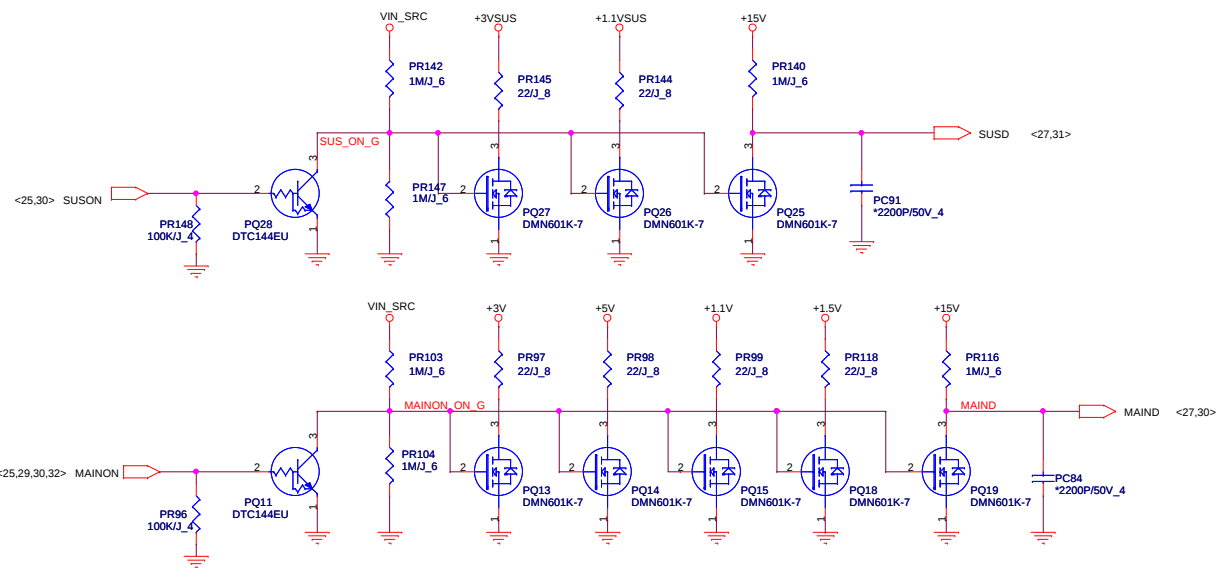
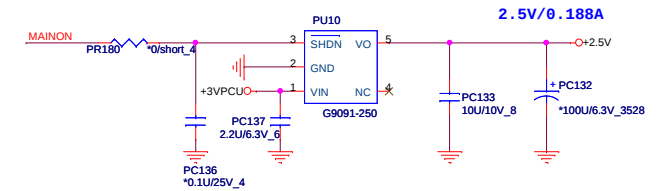
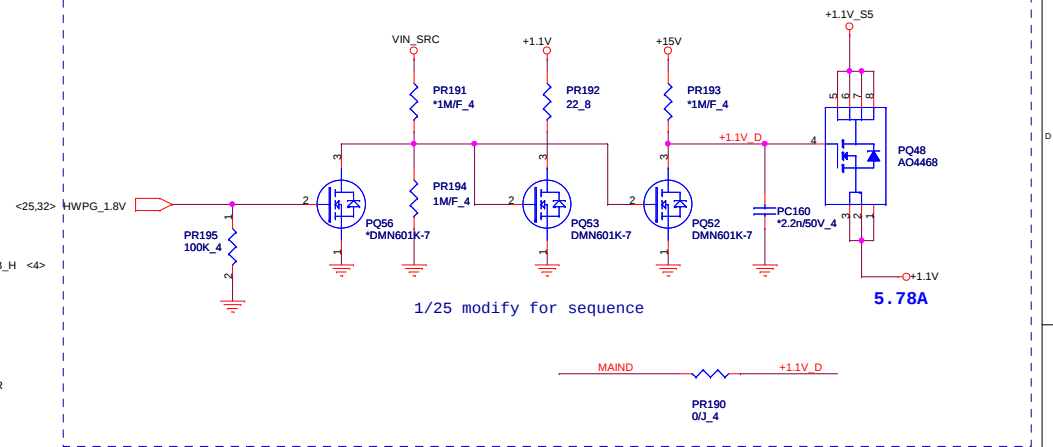
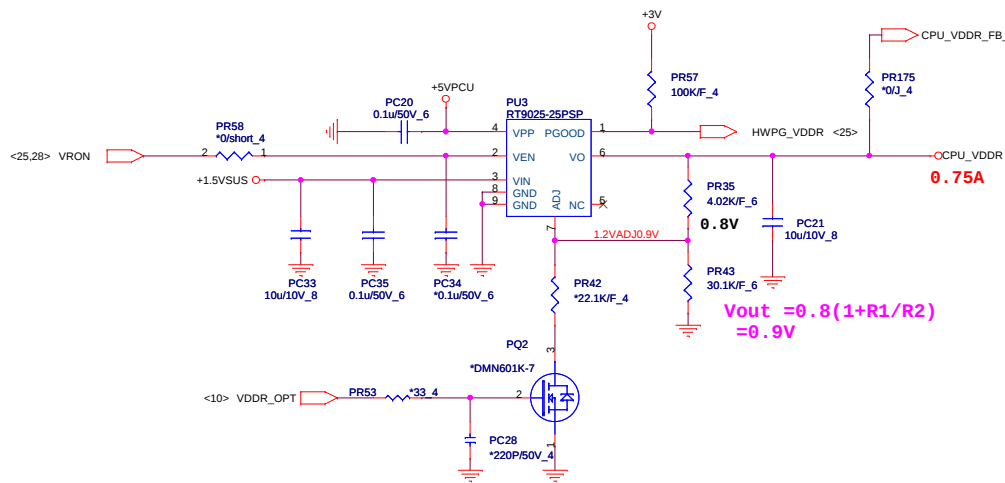


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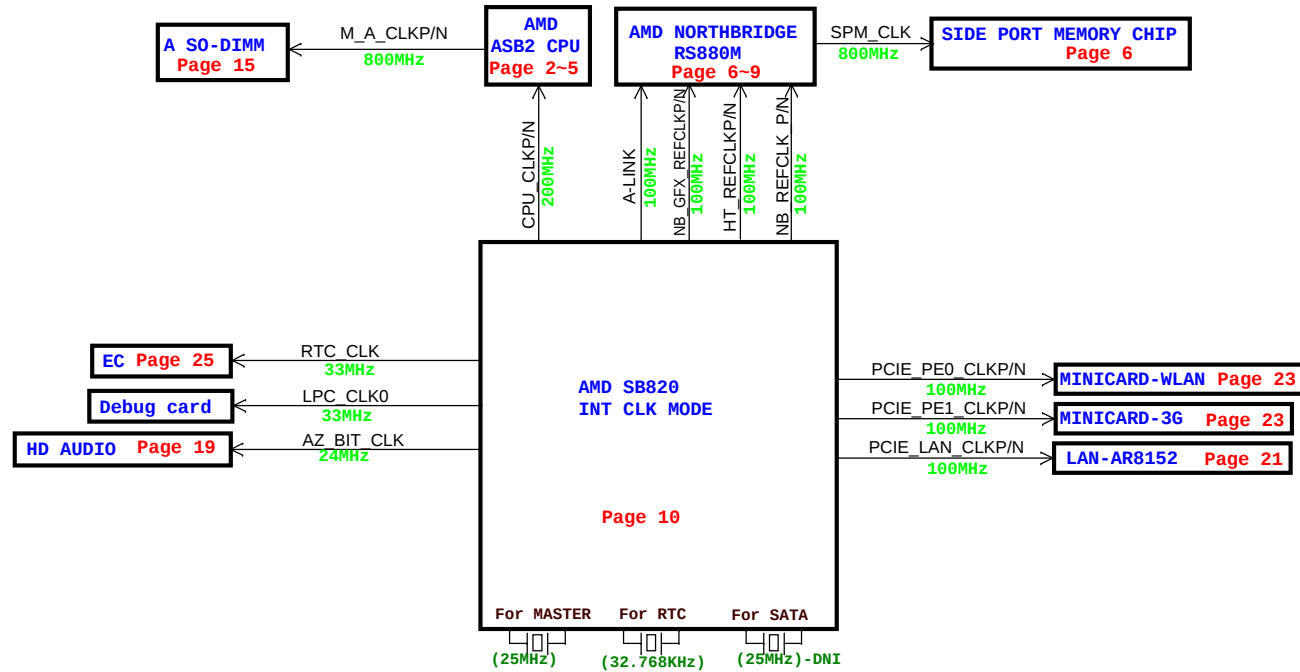
Size	Document Number	Rev
	VCCP 1.1V(UP6111A)	4A
Date:	Sunday, March 28, 2010	Sheet 31 of 40

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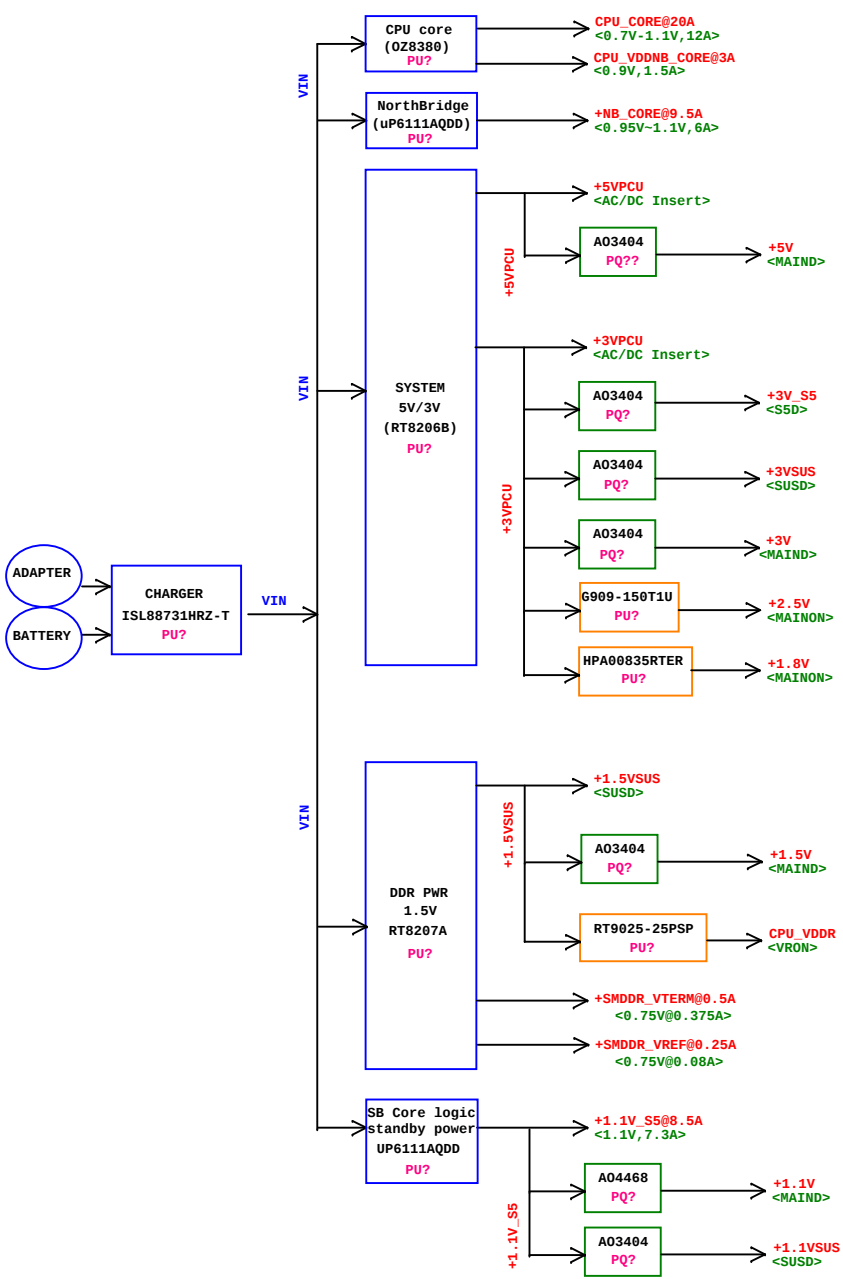
INTERNAL CLOCK MODE



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Size	Document Number	Rev
	Clock Distribution Diagram	4A
Date:	Sunday, March 28, 2010	Sheet 35 of 40

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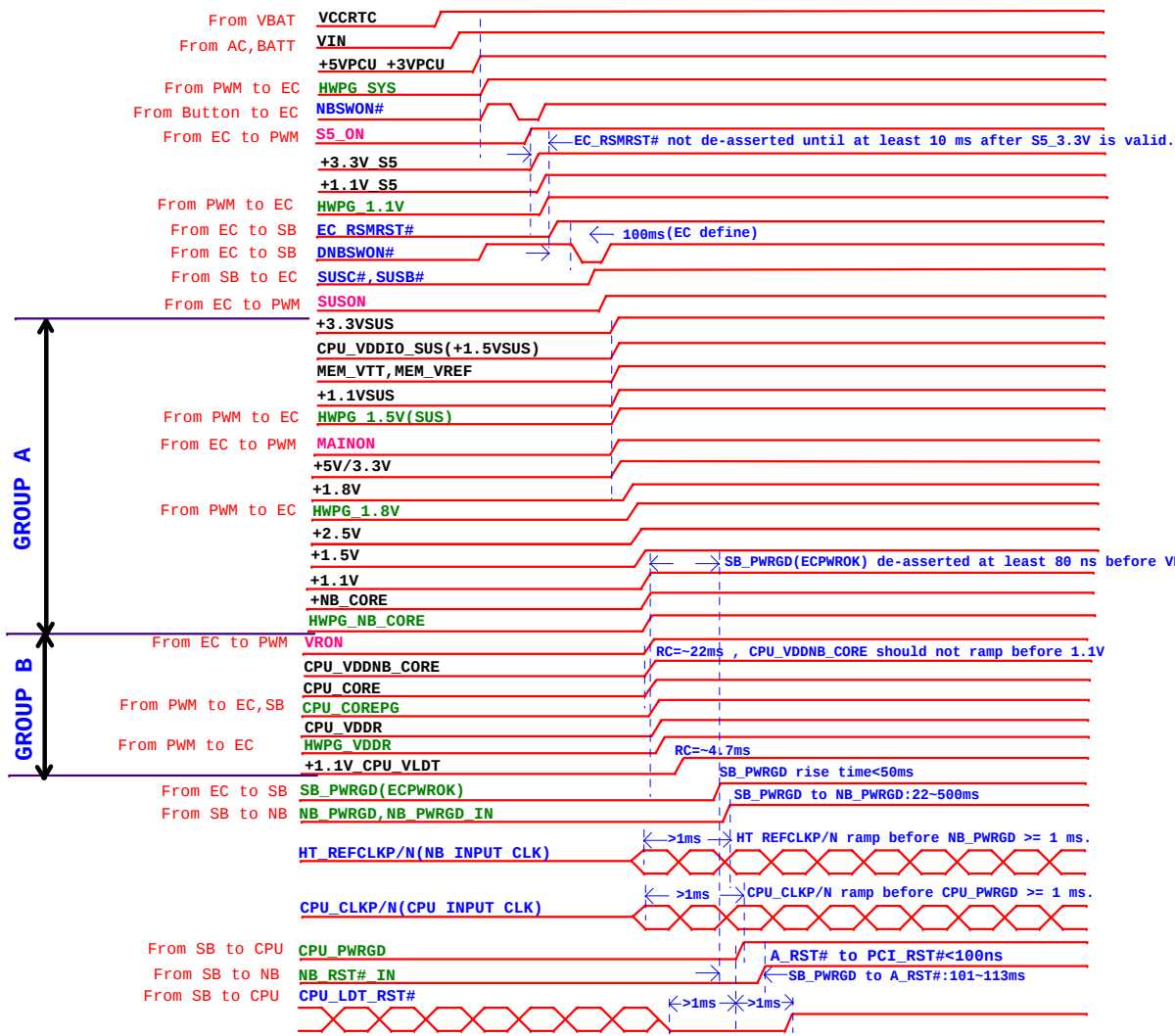


POWER	Distribution
VIN	LCD Backlight, CPU_CORE,NB_CORE, +5VPCU, +3VPCU, +1.5VSUS, +1.1V_S5
CPU_CORE	CPU
CPU_VDDNB_CORE	power supply for on-die NorthBridge
NB_CORE	NorthBridge power supply
+5VPCU	USB Connector
+5V	CRT,Touch Pad ,Audio codec,SATA
+1.8V	NB & SB power supply
+3VPCU	RTC, Hall Sensor, System LED, EC, BIOS, Acer ID EEPROM, +3V_S5, +3VSUS, +3V
+3V_S5	SouthBridge,LAN , LAN EEPROM , RJ45 LED
+3VSUS	3G
+3V	CLK_GEN, CPU, NB,SB, LCD power switch,CCD, DMIC, BT, System LED, Codec, WLAN/Wimax, Card reader, EC
+2.5V	CPU,Discharge
+1.5VSUS	CPU,DDR,Discharge
+1.5V	CPU,DDR,NB
+SMDDR_VTERM	DDR
+SMDDR_VREF	CPU, DDR
+1.1V_S5	NorthBridge,Discharge
+1.1VSUS	Southbridge
+1.1V	CLK_GEN, CPU, NB, SB
CPU_VDDR	CPU

BOM Structure	
Fun.	Description
SPM@	w/ Sideport RAM
3G@	w/ 3G module
BT@	w/ BT module
HDM@	w/ HDMI
BOM@	BOM Control

BOM@		
Function		Description
CPU	CPU V105	U16: AJ00105VT00
	CPU K125	U16: AJ0K125VT02
	CPU K325	U16: AJ0K325VT02
	CPU K625	U16: AJ0K625VT03
w/ Sideport	w/ Sideport	L45,L46: Stuff(CX8PG221003) R142: Non-stuff C214: Stuff(CH4102K1B03) C416: Stuff(CH5102K9B06) Check U7,R295,R296,R283,R284
	w/ SAM Sideport	U7: AKD5LGGT506 ; R295,R284: Stuff ; R296,R283: Non-stuff
	w/ Hynix Sideport	U7: AKD5LZGTW04 ; R295,R283: Stuff ; R296,R284: Non-stuff
	w/ ATI Sideport	U7: AKD5LGGT700 ; R296,R284: Stuff ; R295,R283: Non-stuff
w/o Sideport	w/o Sideport	L45,L46: CS00003J951(0ohm) R142: Stuff(CS23002JB13) C214,C416: CS00002JB38(0ohm) U7,R295,R296,R283,R284: Non-stuff

Nile Power On Sequence



Power on sequence required:

SB820:

- 1.EC_RSMRST# ramp up time (10% to 90%) <= 50 ms
- 2.SB_PWRGD(ECPWRGD) rise time <= 50 ms
- 3.SB_PWRGD(ECPWRGD) fail time <= 1 ms
- 4.SB_PWRGD(ECPWRGD) de-asserted at least 1 ns before EC_RSMRST# is asserted when entering G3 state.
- 5.VBAT will be valid at least 5 seconds before S5_3.3V and S5_1.1V are ramped up to allow start time for internal RTC.
- 6.50us<=all power rails rise time except +3.3V_S5<=40ms
- 7.100us<=+3.3V_S5 rise time<=40ms
- 8.+1.8V_S0 rails cannot ramp before the +3.3V_S0 rails.
- 9.+1.1V_S0 rails cannot ramp before the +1.8V_S0 rails.
- 10.+1.1V_S0 rails cannot ramp before the +3.3V_S0 rails.
- 11.+1.1V_S5 rails cannot ramp before the +3.3V_S5 rails.
- 12.+3V_S5 ramp down time > 300 μs.

RS880:

- 1.+1.1V valid before NB_PWRGD HIGH >= 1 ms
- 2.+1.8V_NB_IOPLLVDD18c(+1.8V) cannot ramp before the 3.3-V rails
- 3.+1.5V_SPM_VDDQ(+1.5V)cannot ramp before the 3.3-V rails
- 4.+1.8V_NB_VDDLTP18(+1.8V)cannot ramp before the 3.3-V rails
- 5.+1.8V_NB_PLLVDD18(1.8V)cannot ramp before the 3.3-V rails
- 6.3.3-V rails cannot exceed the 1.8/1.5-V Sideport or 1.8-V Display and PLL rails by > 2.1 V.
- 7.IOPLLVDD/PLLVD(+1.1V) cannot ramp up before the 1.8/1.5-V Sideport or 1.8-V Display and PLL rails.
- 8.VDDC(+NB_CORE) rail cannot ramp before the 1.1-V PLL rails.

Notice:

- 1.CPU_LDT_RST# msut be asserted a minimum of 1ms prior to the assertion of CPU_PWRGD
- 2.CPU_CLKP/N must be within specification a minimum of 1ms prior to the assertion of CPU_PWRGD
- 3.CPU_PWRGD remains deasserted at least 1ms after both CPU_CLKP/N and all voltages to the processor are within specification for operation
- 4.all NB power rails(1.8V/1.2V/1.1V) valid before NB_PWRGD at least 1ms
- 5.stable input clocks from CLKGEN(HT_REFCLKP/N) to NB before NB_PWRGD at least 1ms

SB SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)
(SB_DA0)/(SB_CL0) (+3V)	V	V	V
Power Plane	+3V	+3V	+3V
MOS CKT (Level shift)	X	X	X*

*Reserve: There is not SMBUS function in AVL

EC SMBUS Table

	Battery	CPU thermal Sensor
EC775 SDA1 / SCL1 (+3VPCU)	V	
EC775 SDA2 / SCL2 (+3V)		V
EC775 SDA3 / SCL3 ()		
Power Plane	+3VPCU	+3V
MOS CKT (Level shift)	X	X

SLP_S5#(SUSC#):
S5 Sleep Power plane control - Assertion of SLP_S5# shuts power off to non-critical components when system transitions to S4 or S5 state.

