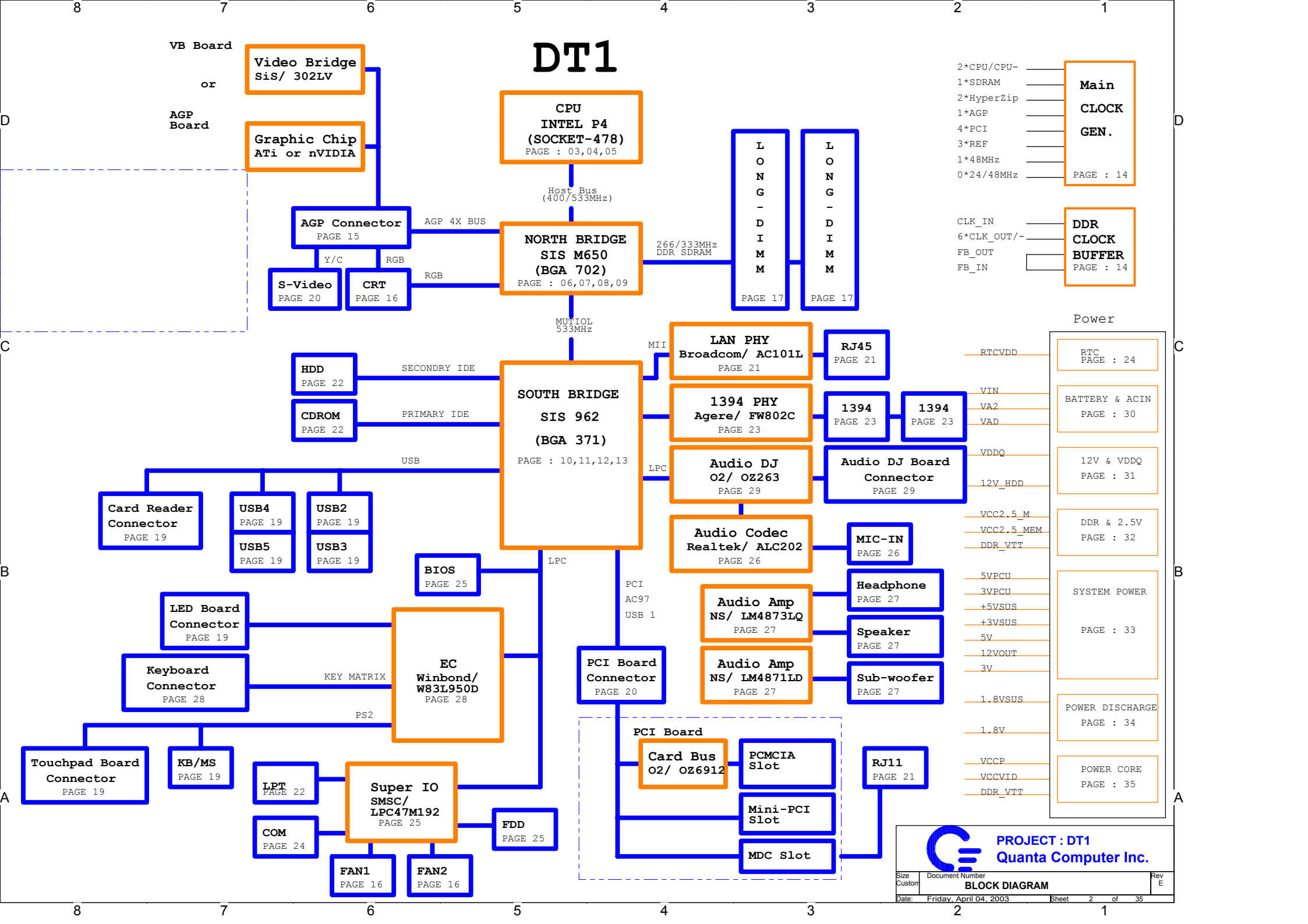
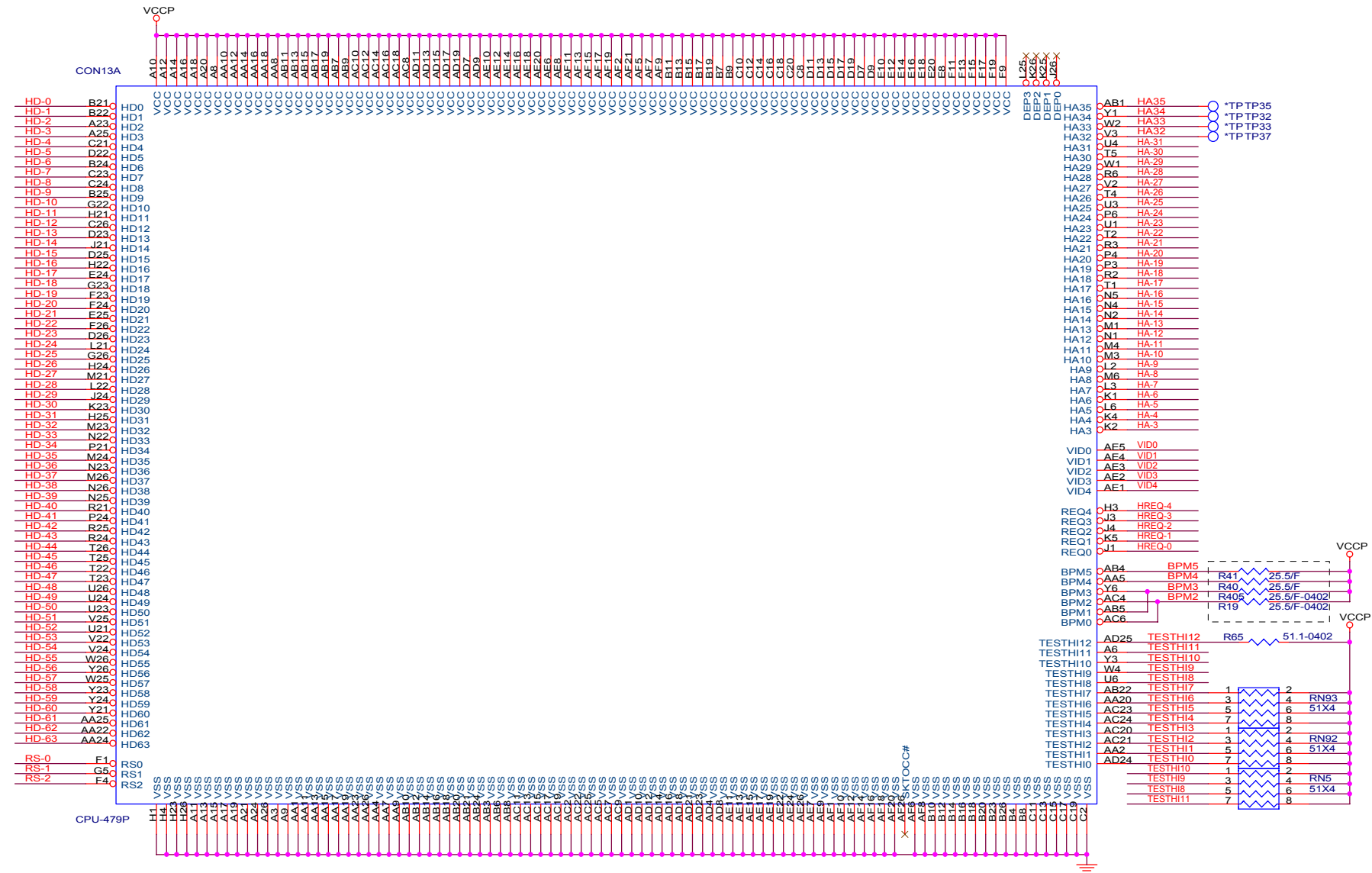


QUANTA COMPUTER INC.

(March/31/2003) Rev : E

PAG	Content	PAG	Content
1	Cover Page	31	POWER 12V_HDD & AGP (VDDQ)
2	650 System Block Diagram	32	POWER - DDR & 2.5V
3	SOCKET 478 - 1	33	SYSTEM POWER
4	SOCKET 478 - 2	34	POWER DISCHARGE
5	SOCKET 478 - 3	35	POWER CORE
6	650-1 (Host/AGP)	36	
7	650-2 (Memory for DDR)	37	
8	650-3 (HyperZip/VGA/Misc.)	38	
9	650-4 (Powers)	39	
10	962-1 (PCI/IDE/HyperZip)	40	
11	962-2 (Misc. Signals)	41	
12	962-3 (USB/1394/IPB)	42	
13	962-4 (Powers)	43	
14	Main Clock Generator & BUFFER	44	
15	AGP SLOT	45	
16	CRT,LCD LID,BLON & FAN CONTROL	46	
17	DIMM1 & DIMM2	47	
18	DDR_TERMINASION	48	
19	USB,LED/B,PS2,PW & RST CONN	49	
20	PCI CONN & PULL UP	50	
21	LAN PHY (AC101L) & RJ45,RJ11	51	
22	IDE (HDD & CDROM) & LPT	52	
23	1394 (RTL8801B)	53	
24	HOLE,EMI,RTC & COM1	54	
25	SUPER_I/O & BIOS ROM	55	
26	AUDIO CODEC (ALC650)	56	
27	AUDIO AMPLIFIER (LM4873 & 4871)	57	
28	EC W83L950D	58	
29	AUDIO DJ (0Z263)	59	
30	BATTERY CONN & POWER JACK	60	



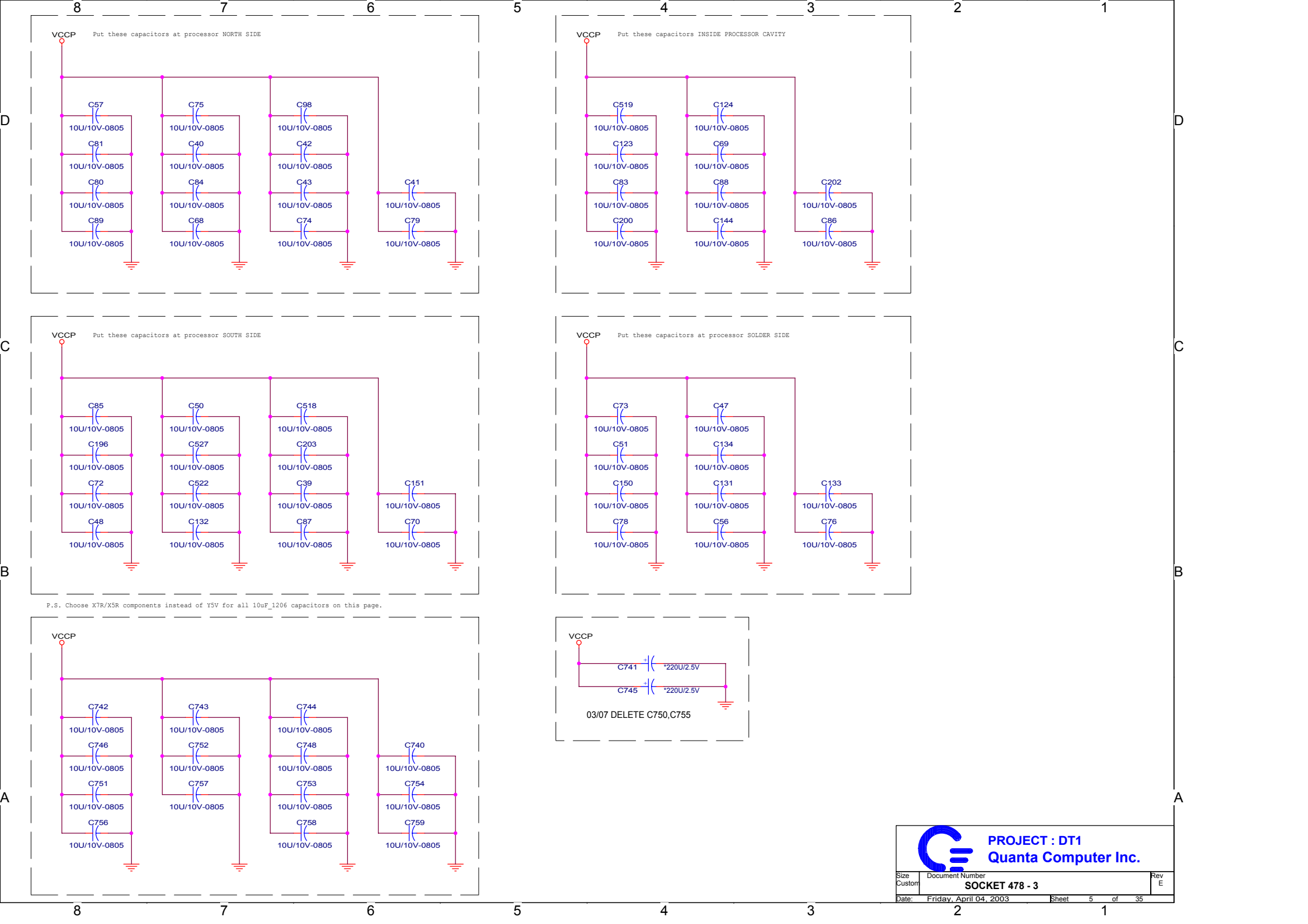


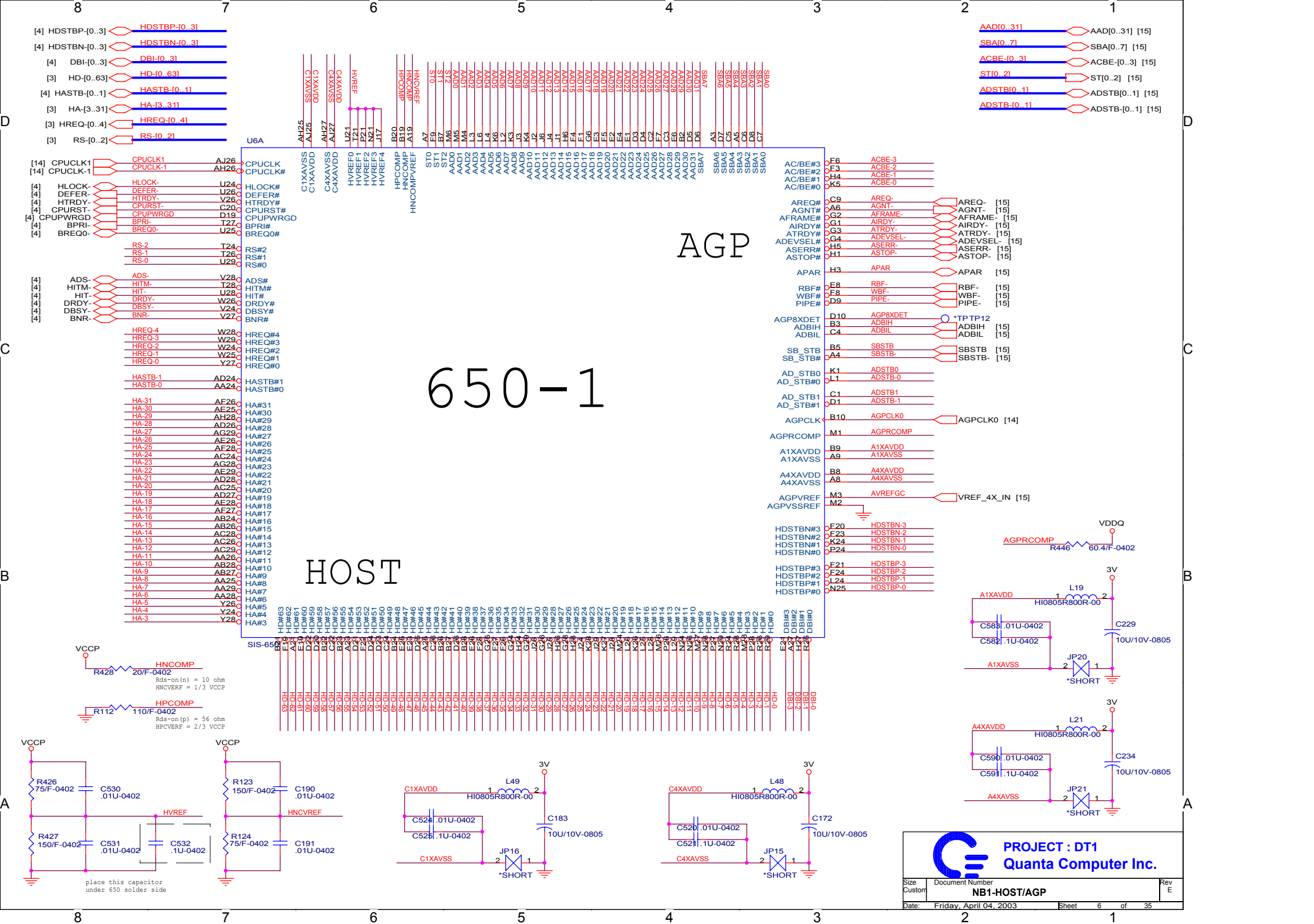
- [6] RS-[0..2] RS-[0..2]
- [6] HD-[0..63] HD-[0..63]
- [6] HA-[3..31] HA-[3..31]
- [6] HREQ-[0..4] HREQ-[0..4]
- [35] VID[0..4] VID[0..4]

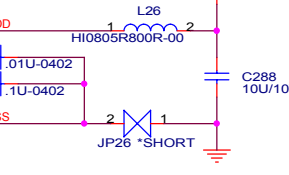
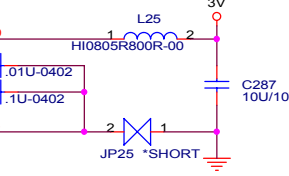
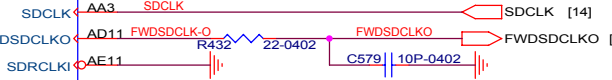
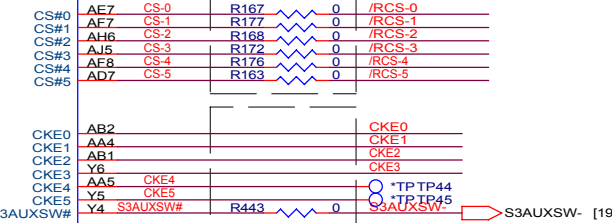
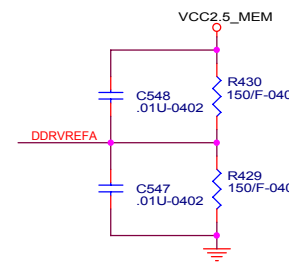
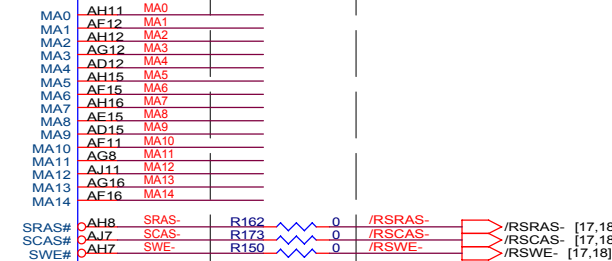
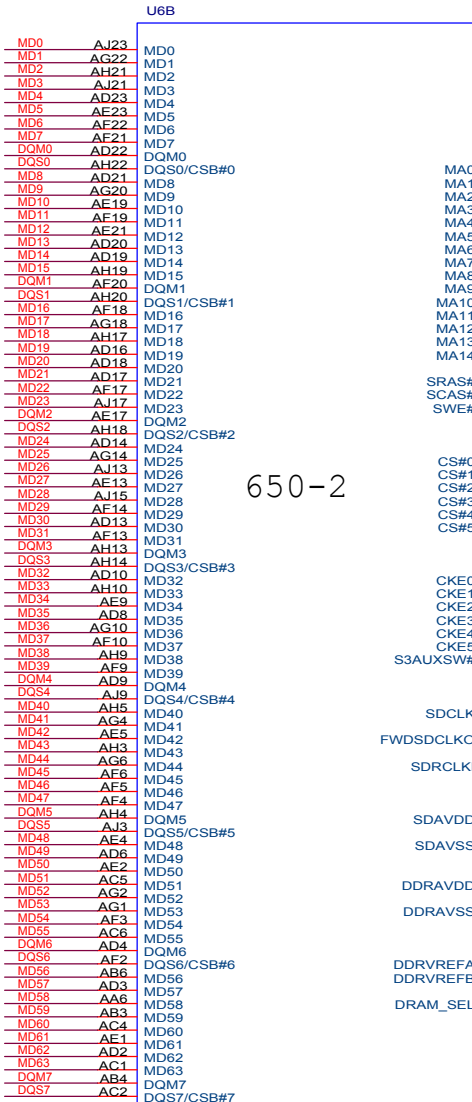
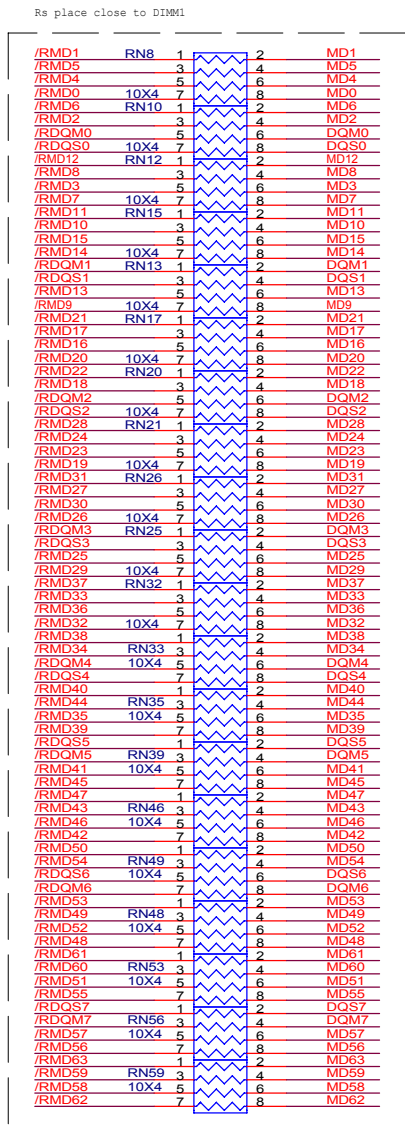
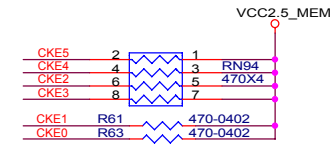
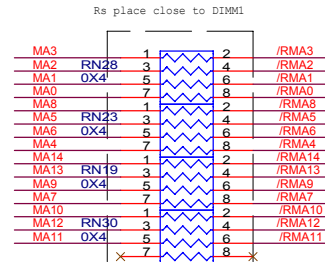
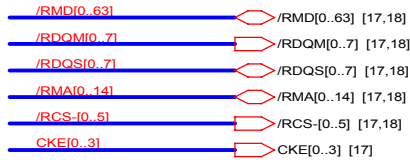


PROJECT : DT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SOCKET 478 - 1	E
Date:	Friday, April 04, 2003	Sheet 3 of 35

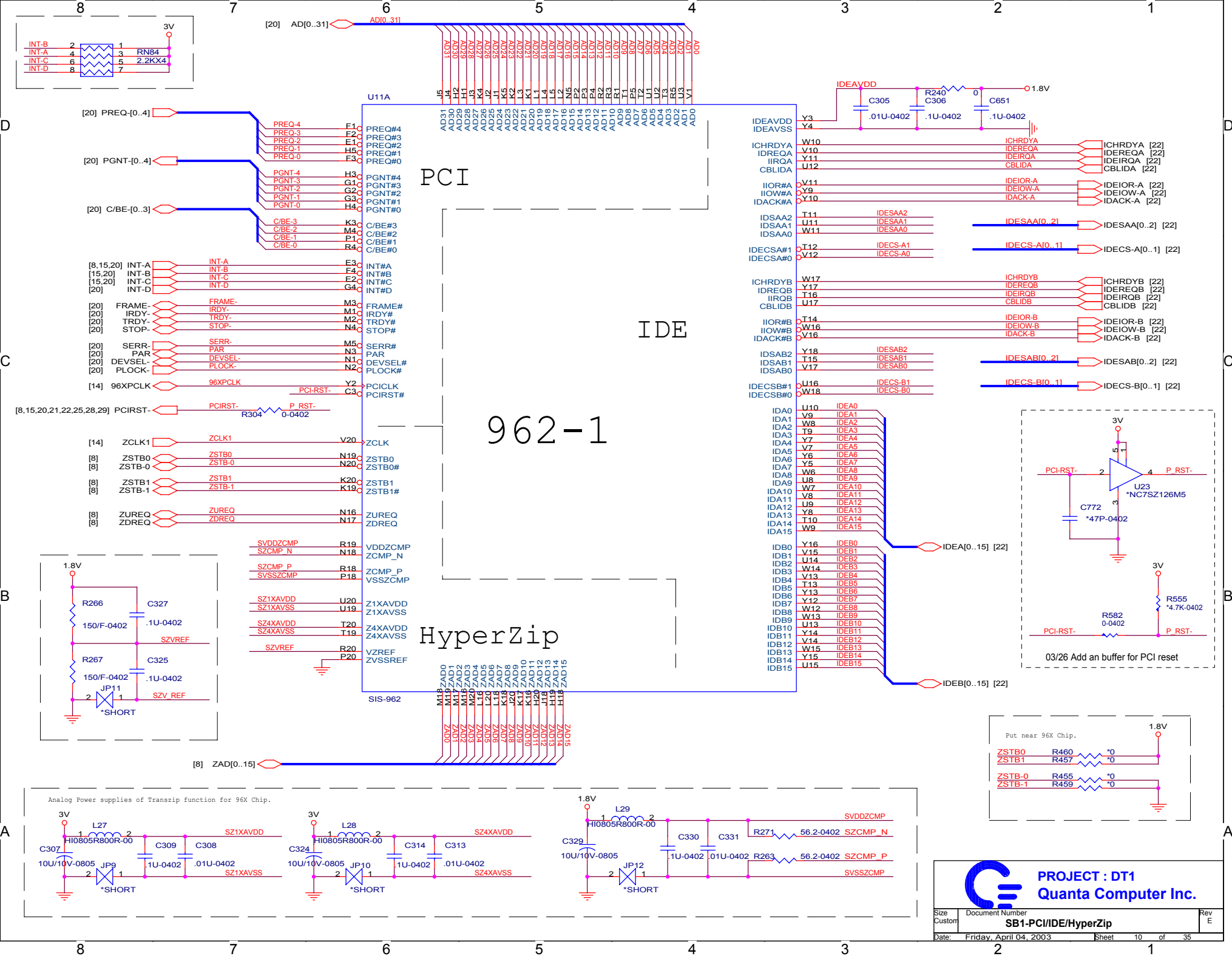




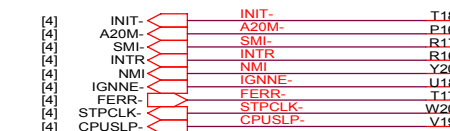


PROJECT : DT1
Quanta Computer Inc.

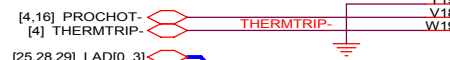
NB Hardware Trap Table					
		0	1	Default	embedded pull-low
DILEN#	enable PLL		disable PLL	0	(30-50K Ohm)
DRAM SEL	SDR		DDR	1 (DDR)	yes
TRAP0	normal		NB debug mode	0	yes
TRAP1	TV selection, NTSC/PAL(0/1)			0	
CSYNC	enable V8			0	
RSYNC	enable VGA interrupt			1	
LSYNC	enable panel link			0	



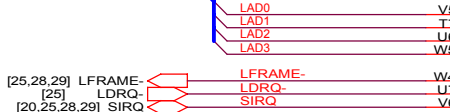
D



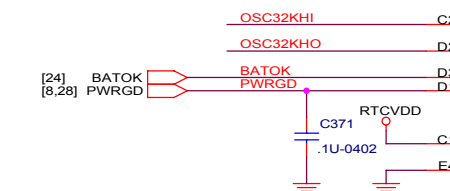
CPU_S



APIC

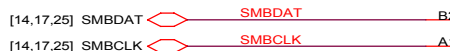


LPC

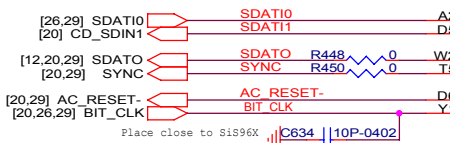


RTC

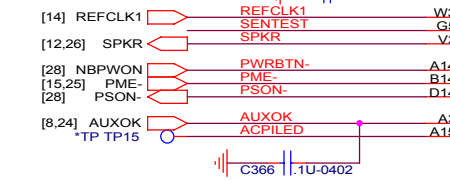
962-2



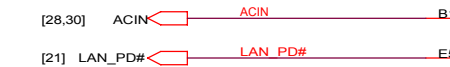
GPIO



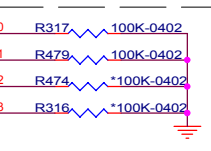
AC97



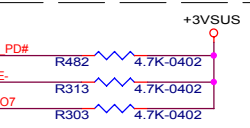
ACPI
/others



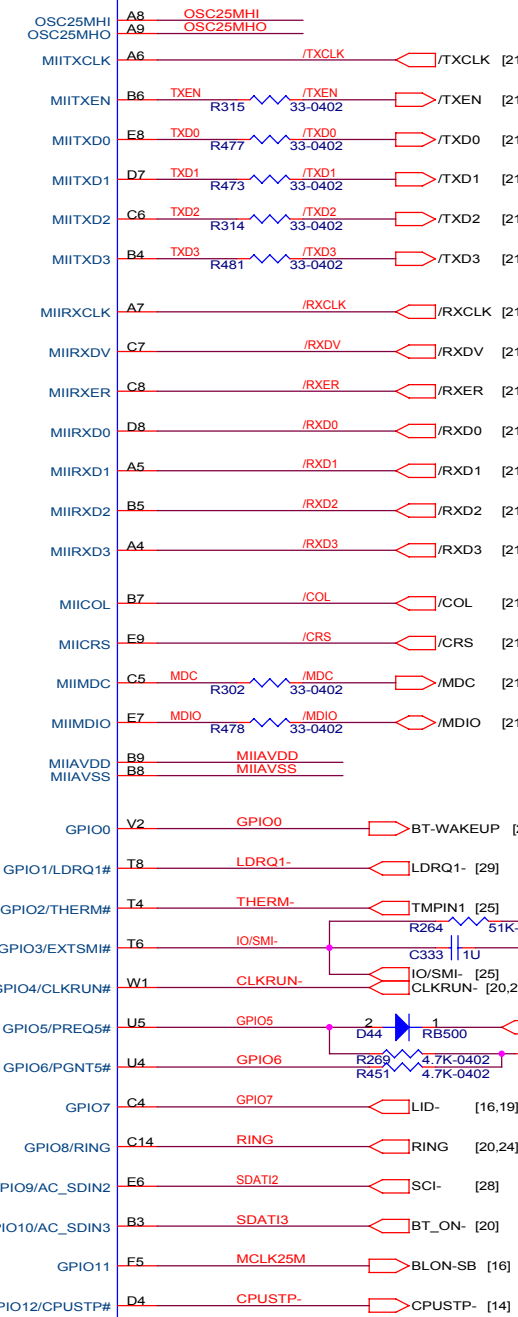
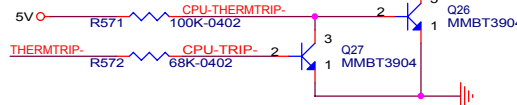
GPIO



KBC
/geyserville



SIS-962



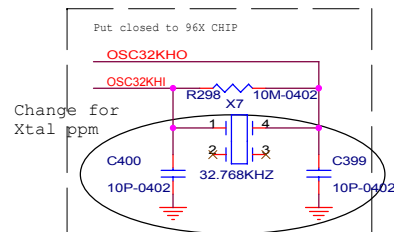
MII

C

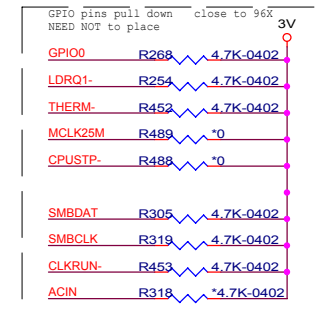
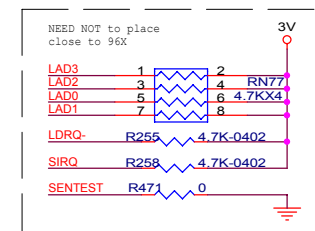
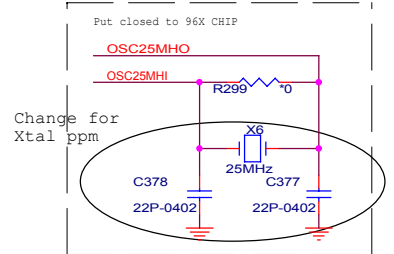
B

A

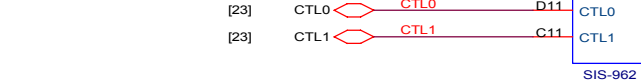
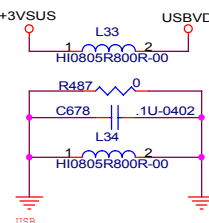
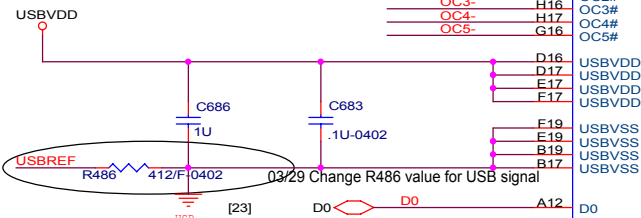
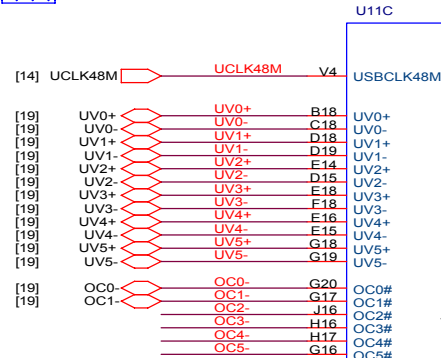
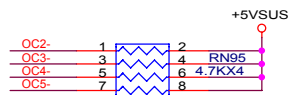
02/28 X7 COMPONENT FROM BG332768721 TO BG33768216



02/28 C399 FROM 20P TO 10P, C400 FROM 15P TO 10P



PROJECT : DT1
Quanta Computer Inc.



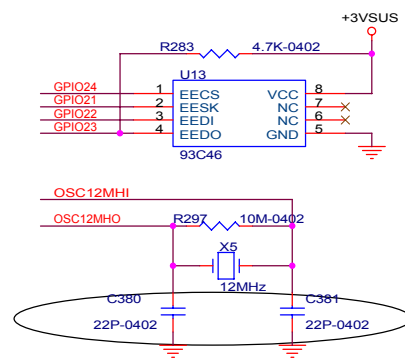
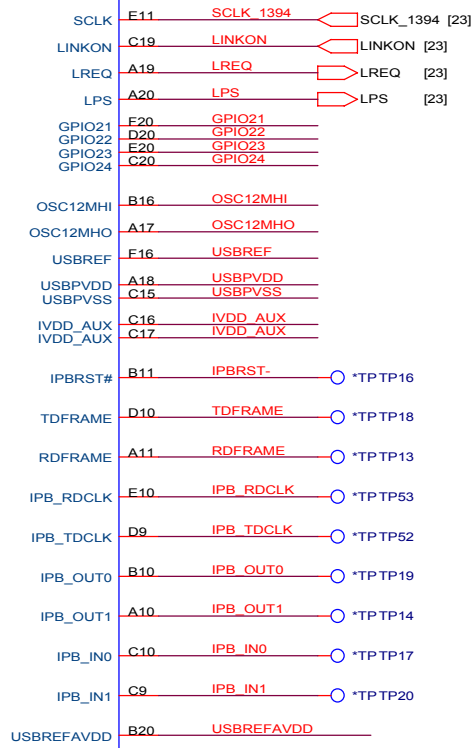
OTHERS

USB

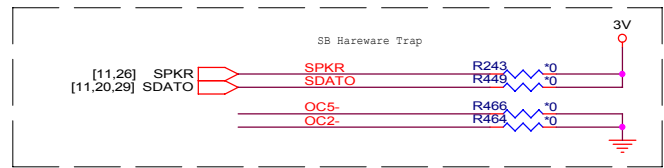
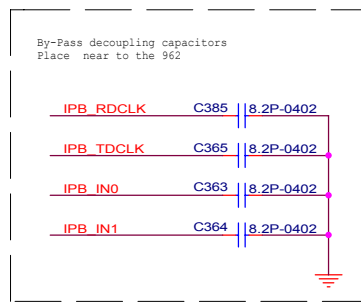
962-3

ACR-IPB
/ADSL
(For 962,963)

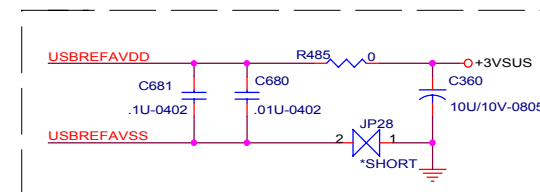
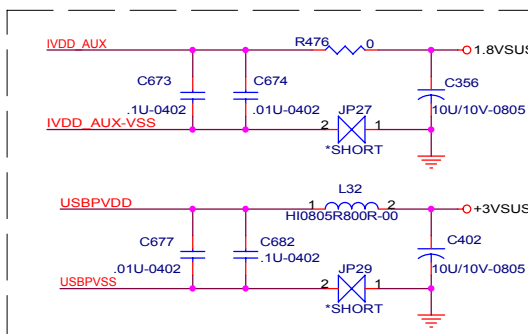
ACR-WIRELESS
/BLUETOOTH
(ONLY FOR 963)



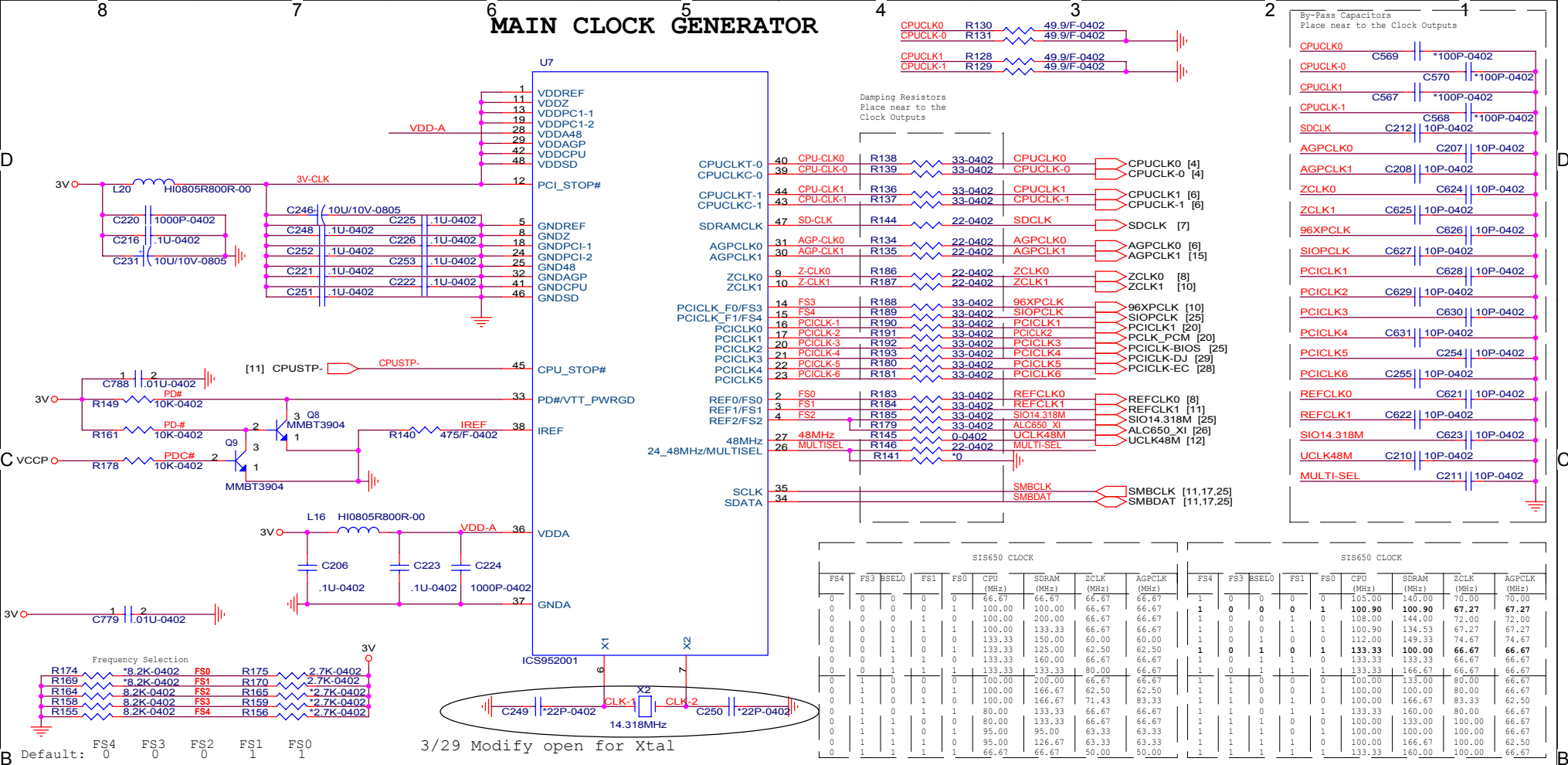
3/29 Modify for Xtal



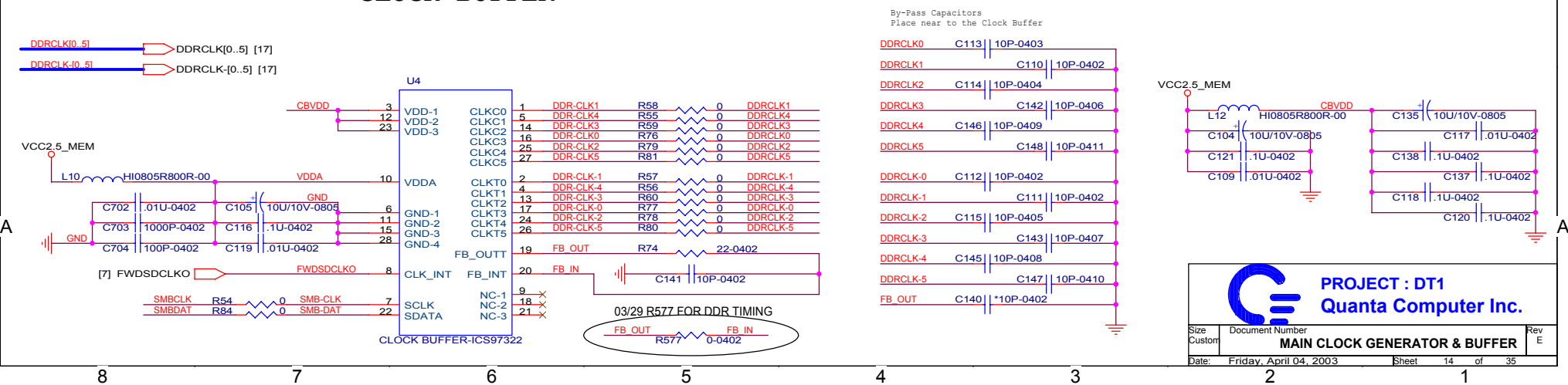
	0	1	Default
SPKR (LPC addr mapping)	disable	enable	0
SDATO (Trap mode)	ROM	PCI_AD	0
OC2-	enable	disable	1
OC5-	enable	disable	1



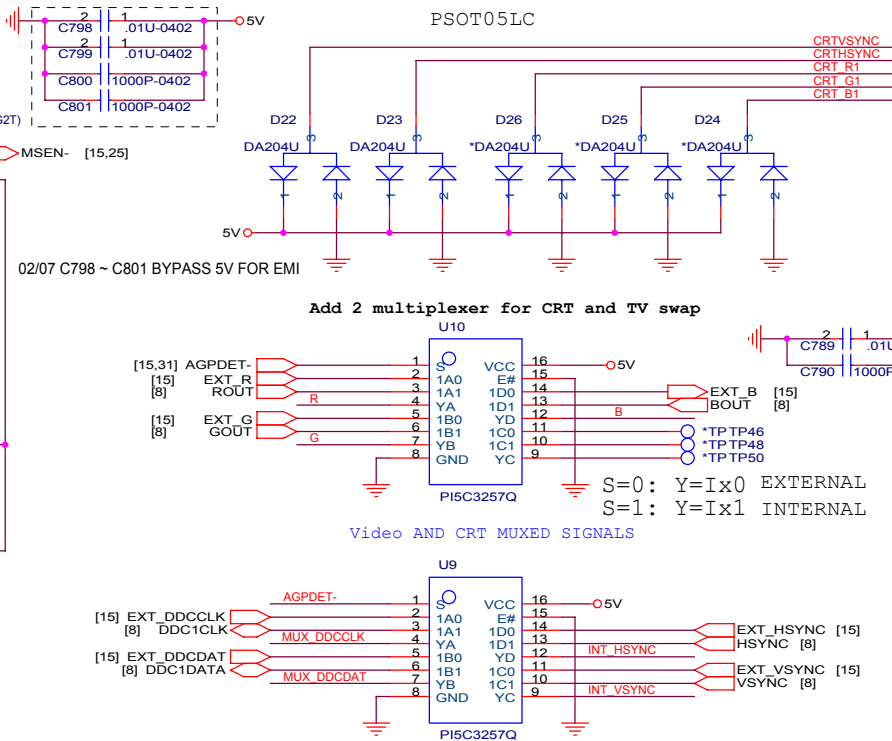
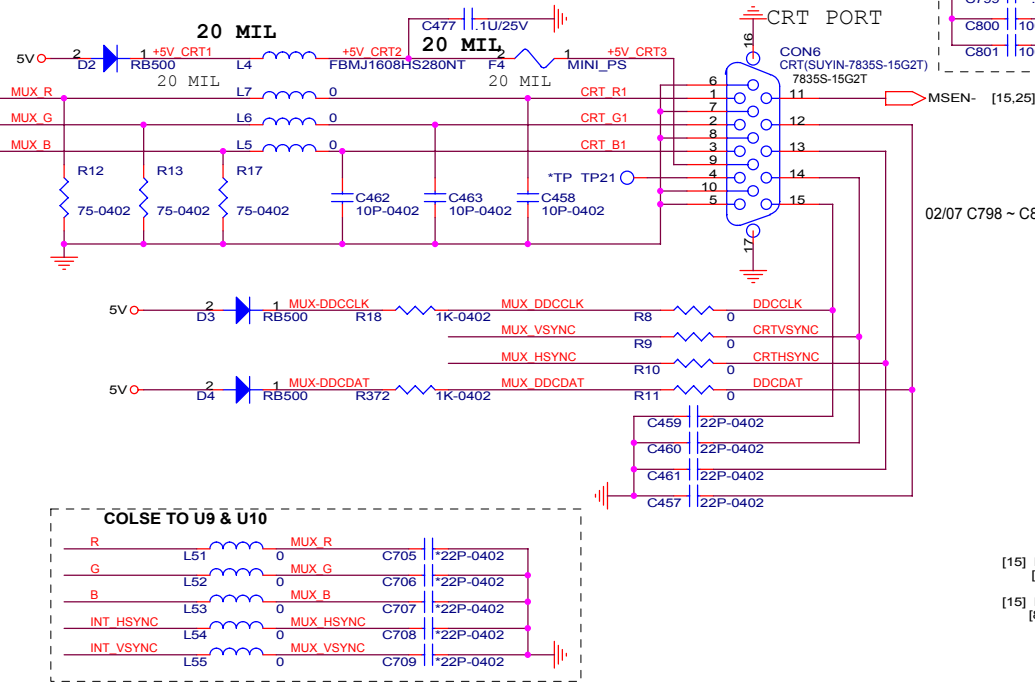
⁶MAIN CLOCK ⁵GENERATOR



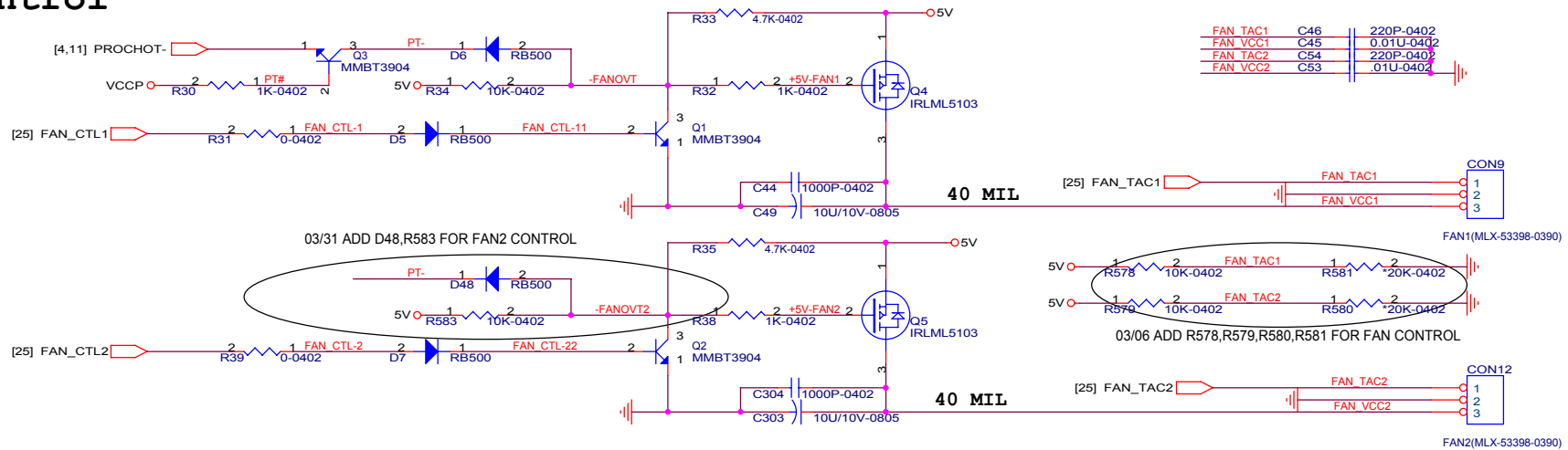
CLOCK BUFFER



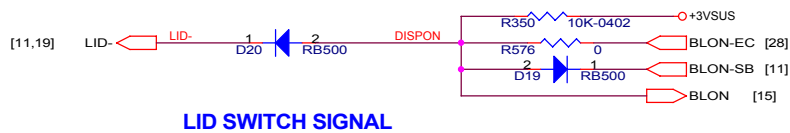
CRT



FAN Control

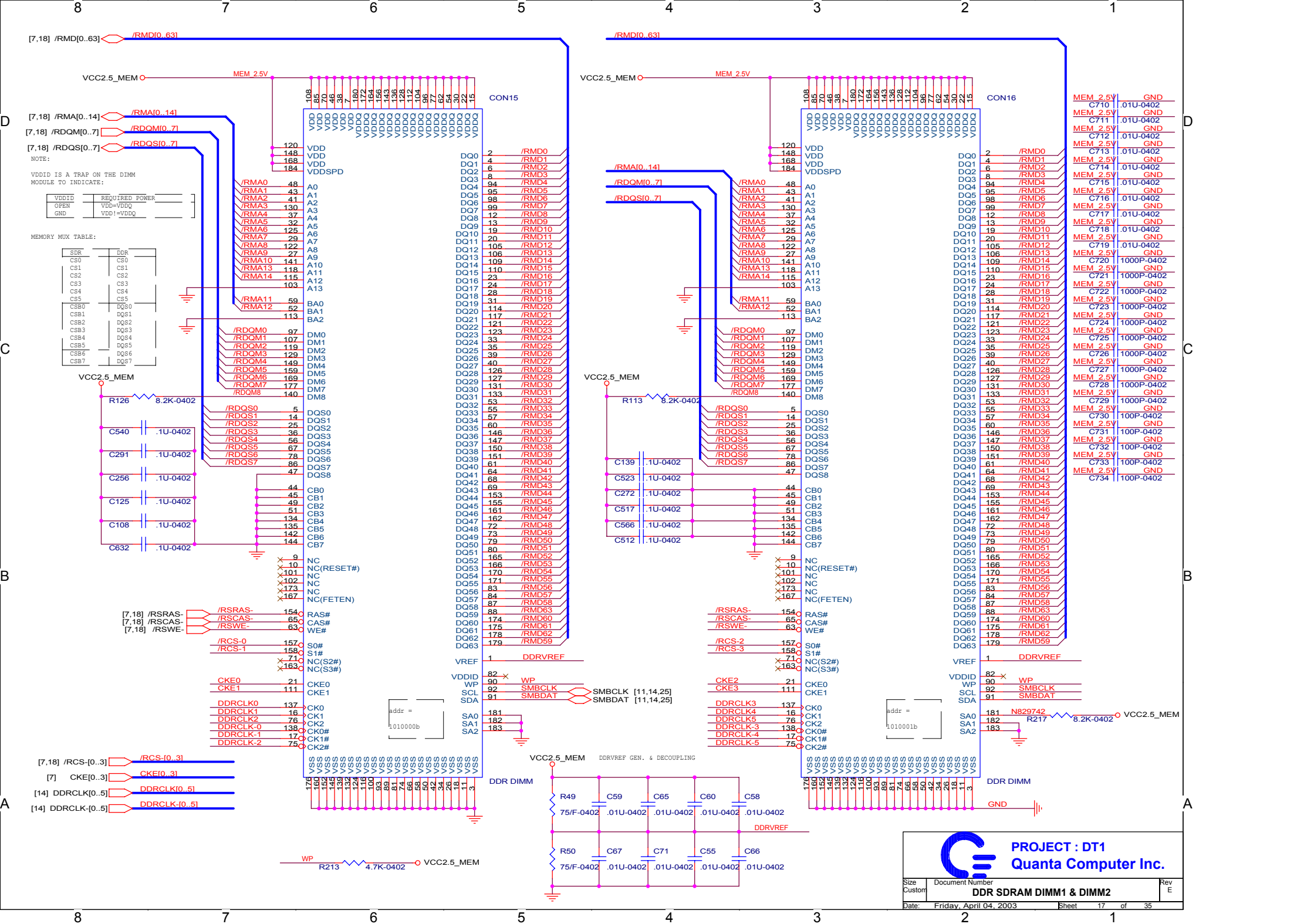


LCD-LID



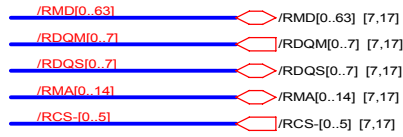
PROJECT : DT1
Quanta Computer Inc.

Size: Custom
Document Number: CRT,LCD LID,BLON & FAN CONTROL
Date: Friday, April 04, 2003
Sheet: 16 of 35
Rev: E



SSTL-2 Termination Resistors

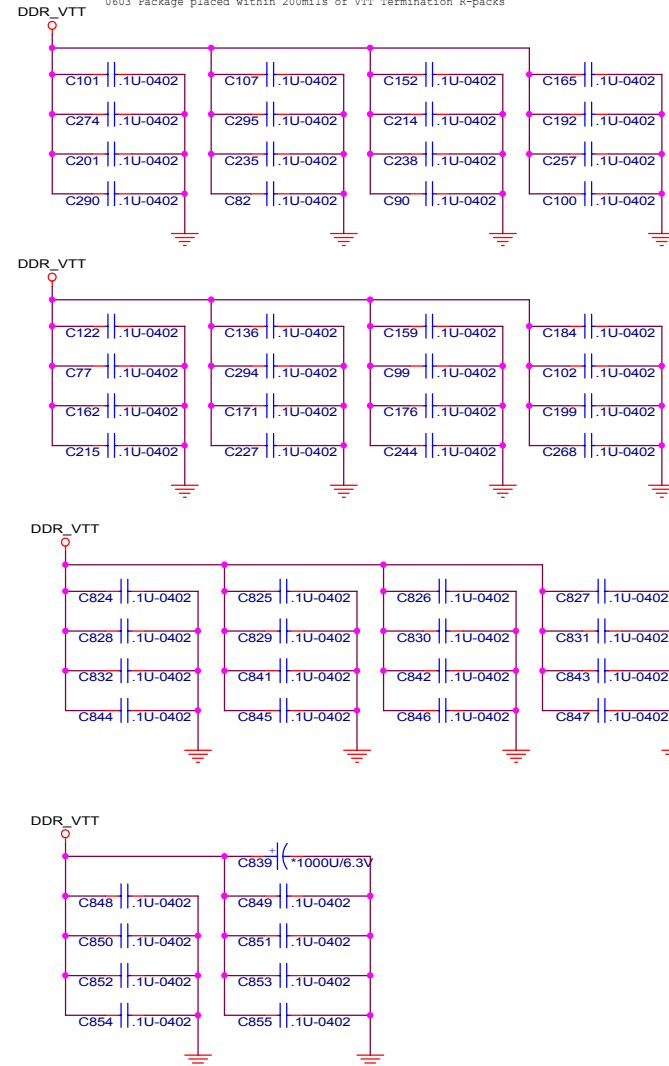
	SDR		DDR		
MD/DQM (/DQS)	LV-CMOS	Rs	SSTL-2	Rs	Rtt
MA/Control	LV-CMOS	0/10/-	SSTL-2	10	33
CS	LV-CMOS	10	SSTL-2	0	33
CKE	OD 3.3V	0	SSTL-2	0	47
			OD 2.5V		



01/07 MEMORY TERMINATIO PIN SWAP



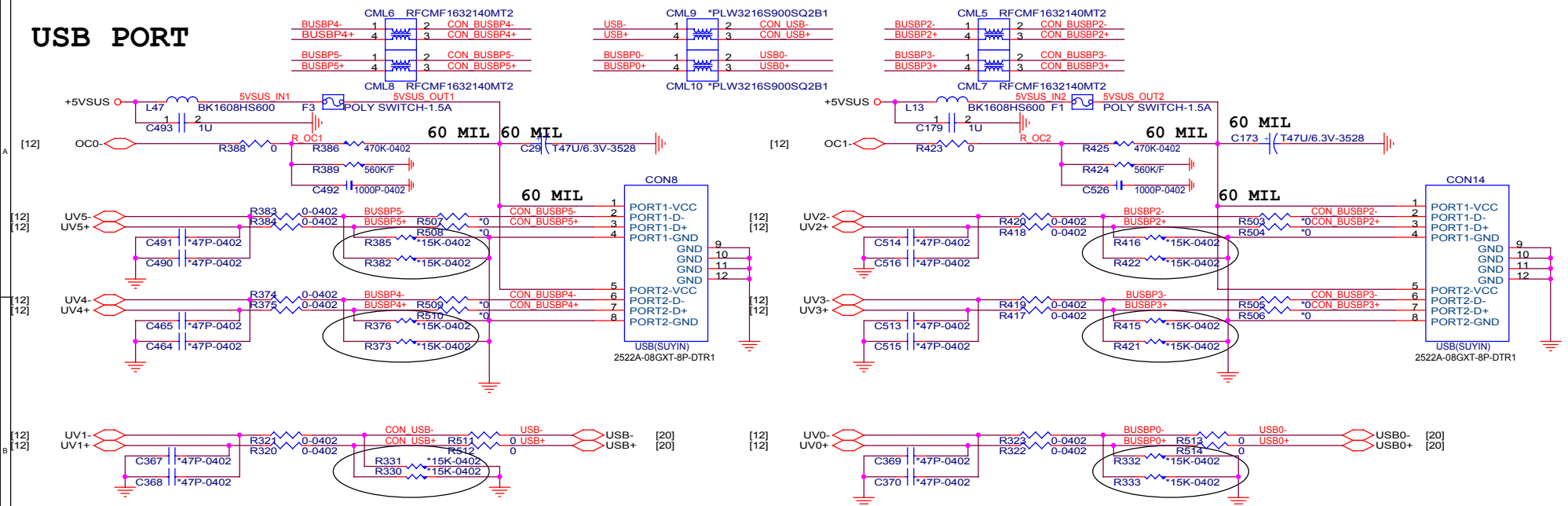
DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
0603 Package placed within 200mils of VTT Termination R-packs



PROJECT : DT1
Quanta Computer Inc.

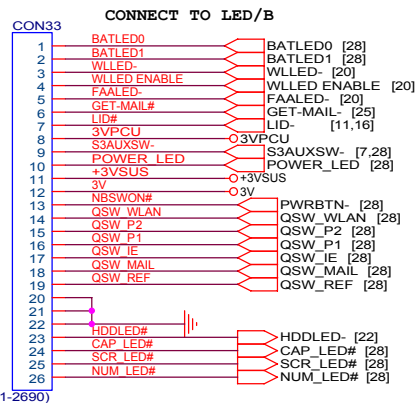
Size	Document Number	Rev
Custom	SSTL-2 TERMINATION RESISTORS	E
Date:	Friday, April 04, 2003	Sheet 18 of 35

USB PORT

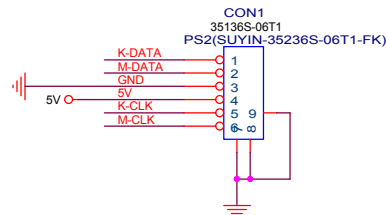


03/07 R330,R331,R332,R333,R373,R376,R382,R385,R416,R422 UNSTAFF

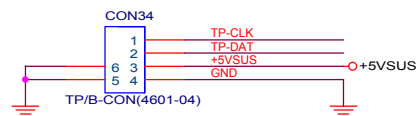
LED/B CONNECTOR



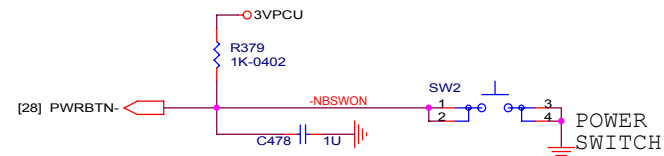
PS/2



TP/B CONNECTOR



POWER SW



RESET SW



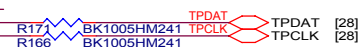
02/28 C45,C455,C456,C457 FROM 100P CHANGE TO 270P FOR EMI



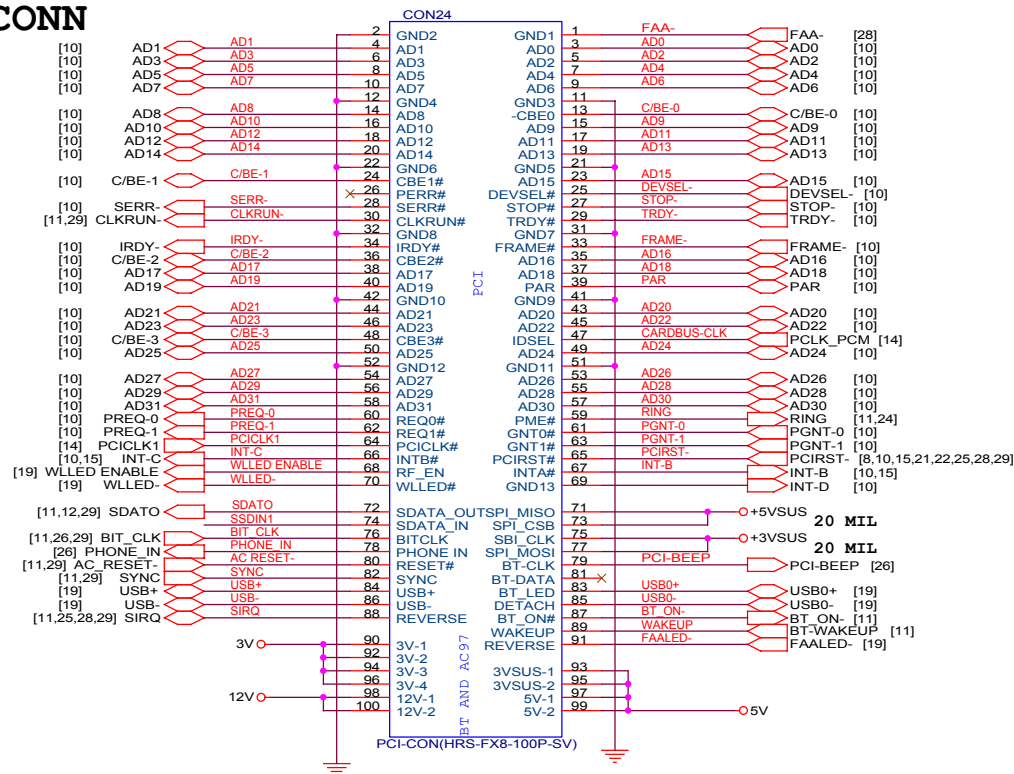
03/06 C453,C454,C455,C456 UNSTAFF

QSW P1		C262	* 1U-0402	C452	1U-0402	3V
QSW P2						+5VUS
NBSW#N	C266	* 1U-0402		C482	1U-0402	3VPCPU
WLED ENABLE	C263	* 1U-0402	C484	1U-0402		+5VUS
FAILED	C233	220P-0402	C245	1U-0402		QSW_REF
QSW WLAN		C236	220P-0402	C269	* 1U-0402	BATTLED
QSW SMAIL	C247	220P-0402		C228	* 1U-0402	BATTLED
WLED		C458	* 1U-0402	C230	* 1U-0402	WLED
HDDLED	C260	* 1U-0402		C232	220P-0402	GET-MAIL#
CAP_LED#	C273	220P-0402	C239	220P-0402		TP-DAT
SCR_LED#	C275	220P-0402		C242	* 47P-0402	TP-CLK
NUM_LED#	C281	220P-0402	C241	* 47P-0402	C240	220P-0402
						LED#

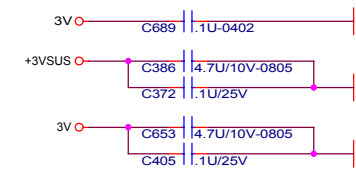
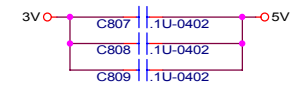
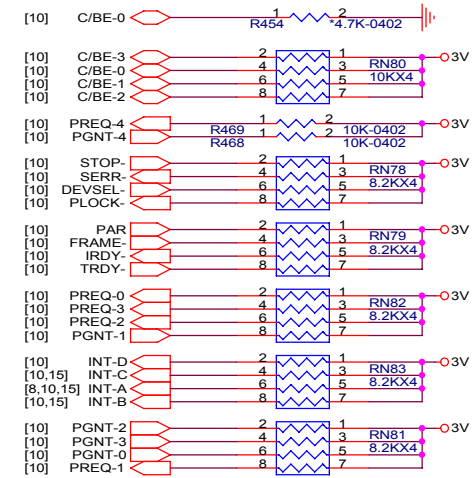
03/06 C241,C241 47P UNSTAFF



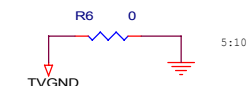
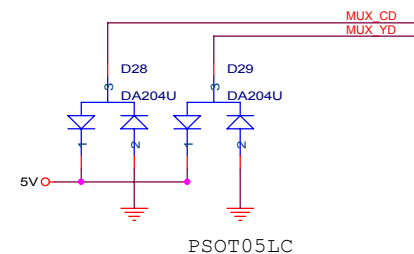
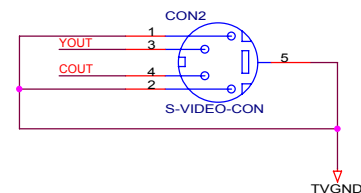
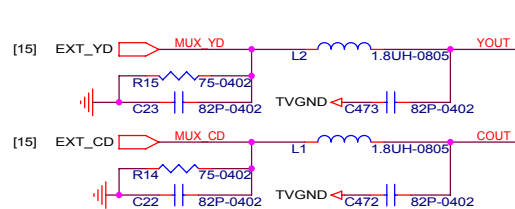
PCI-CONN



PCI PULL UP

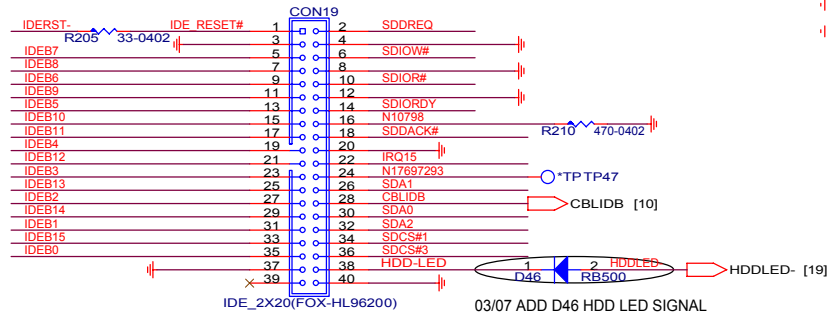


S-VIDEO (TV OUT)

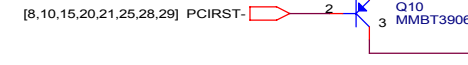
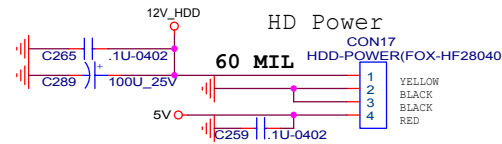


HDD,CD-ROM CONNECTOR

12/18 CON19 CHANGE COMPONENT

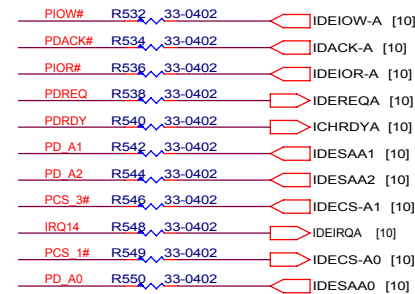


HDD POWER CONNECTOR

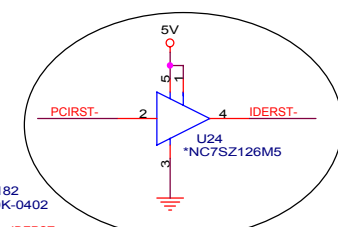
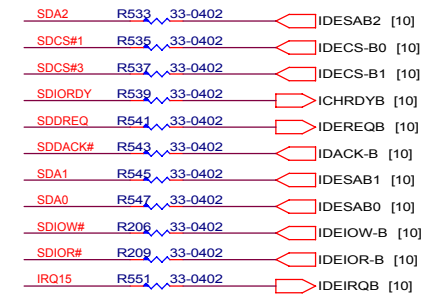


PLACEMENT ON BOT SIDE

CLOSE TO CHIPSET SIDE

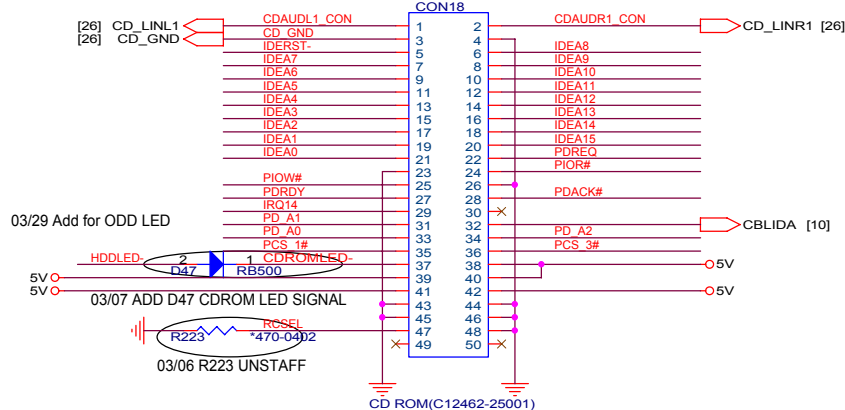


CLOSE TO CHIPSET SIDE

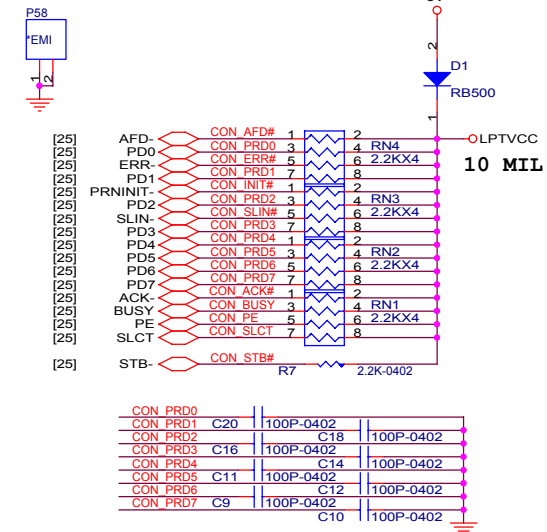
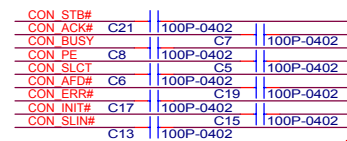
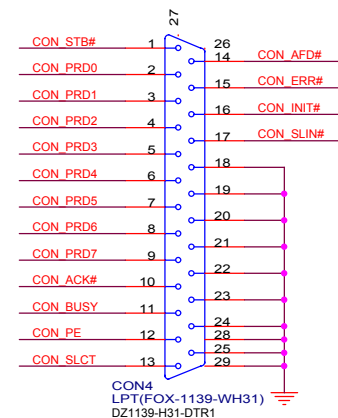


03/26 Add an buffer for IDE reset

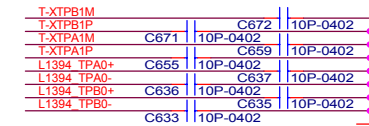
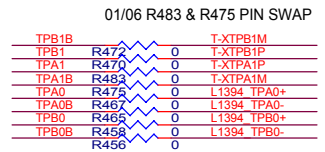
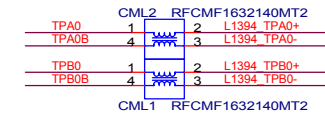
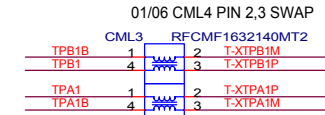
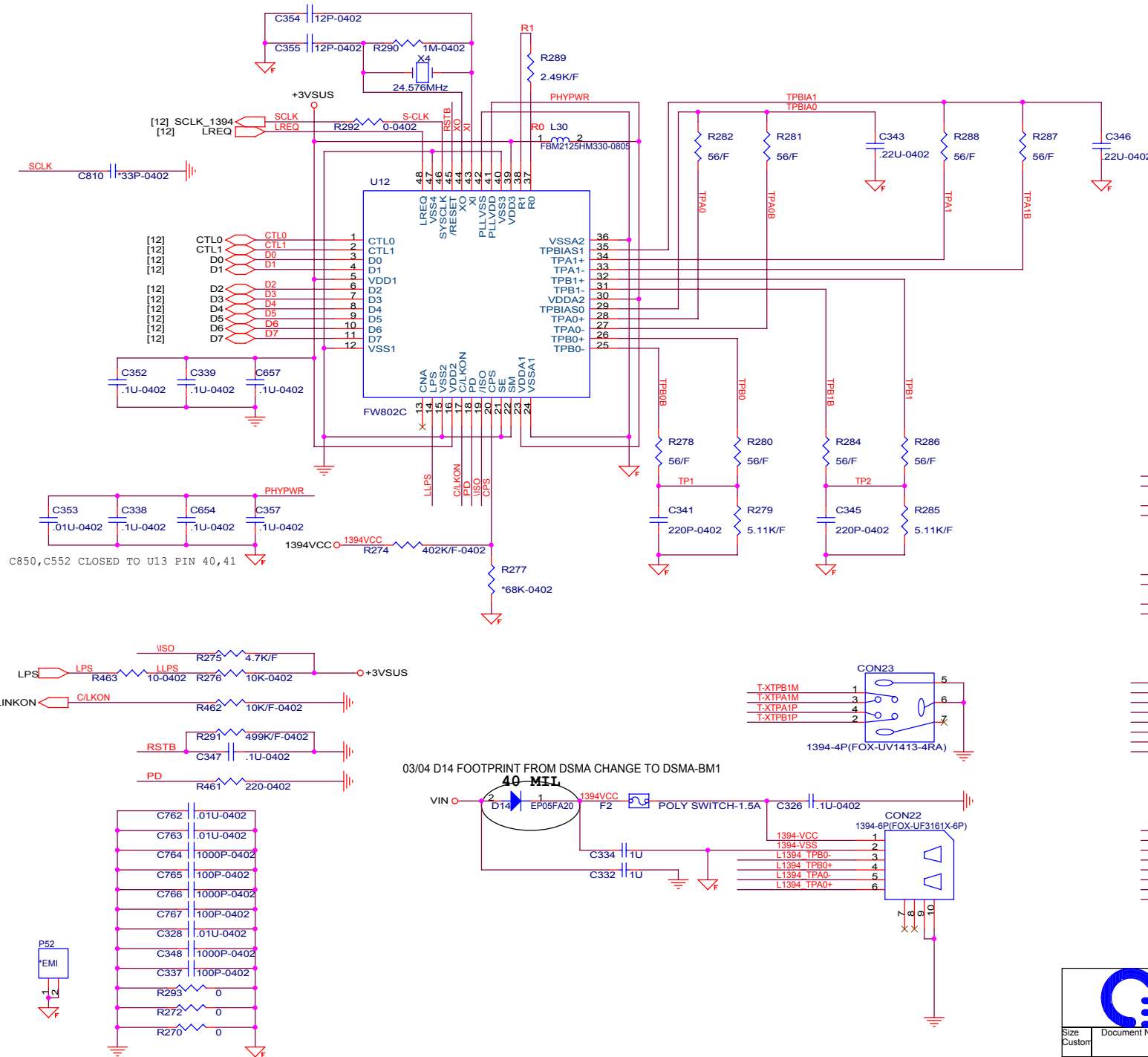
CD-ROM connector



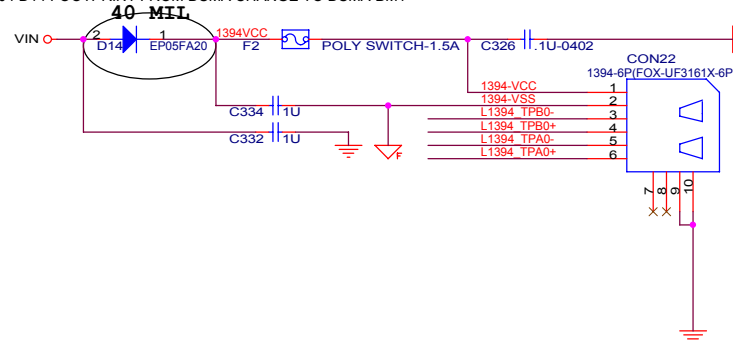
LPT CONN.



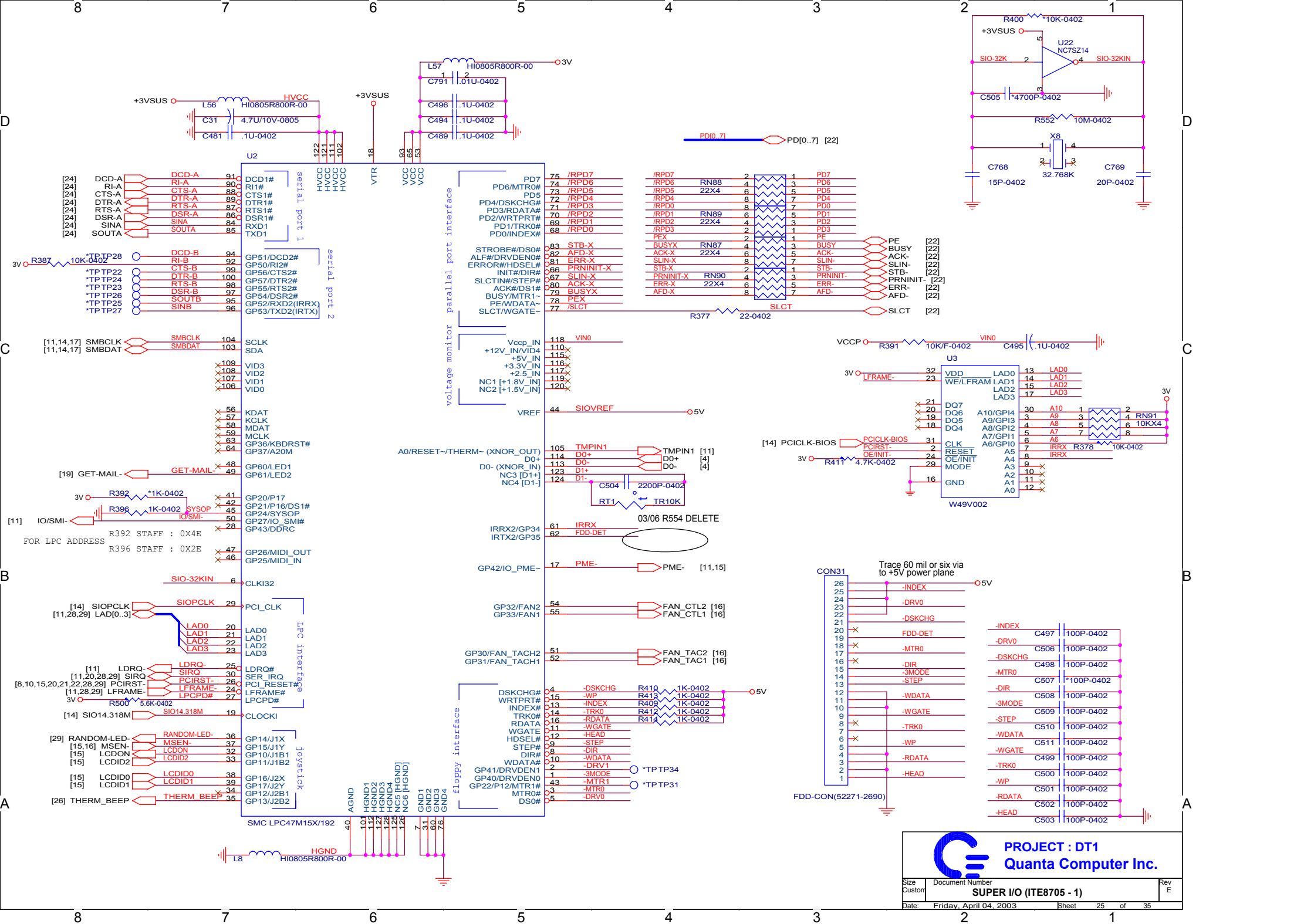
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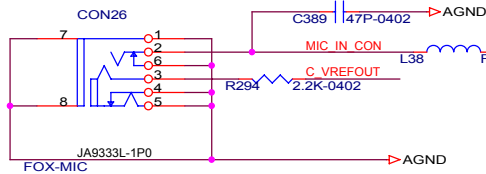
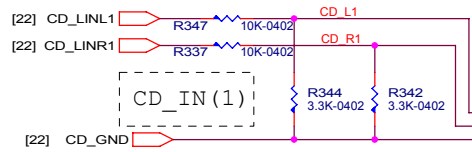
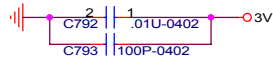


03/04 D14 FOOTPRINT FROM DSMA CHANGE TO DSMA-BM1

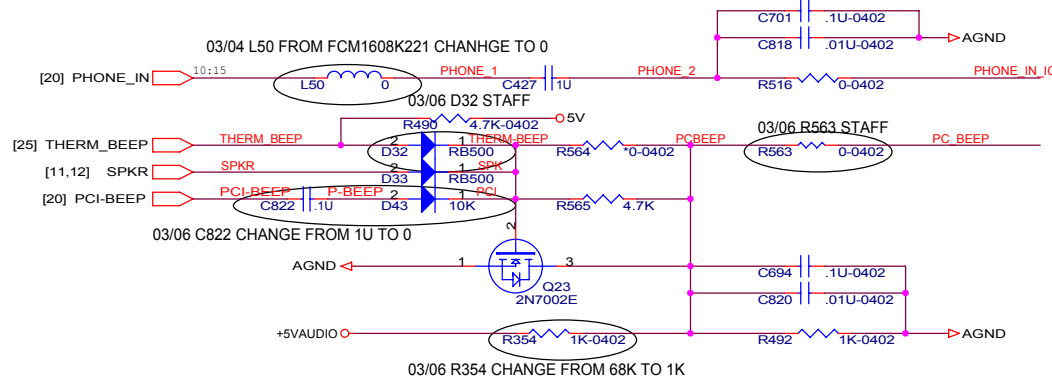


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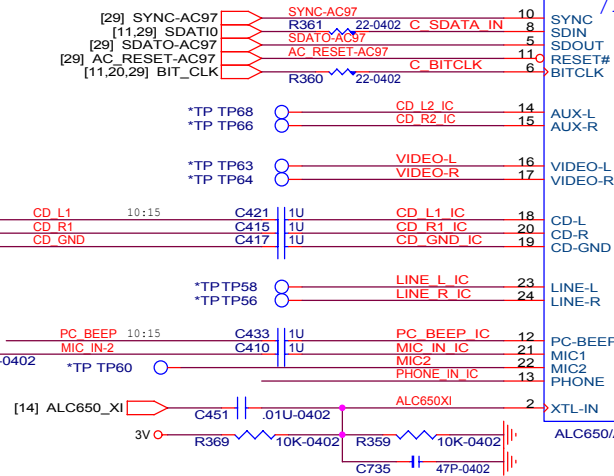
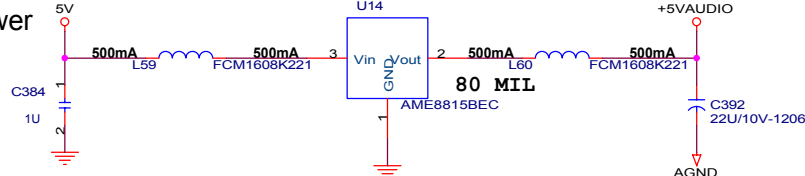




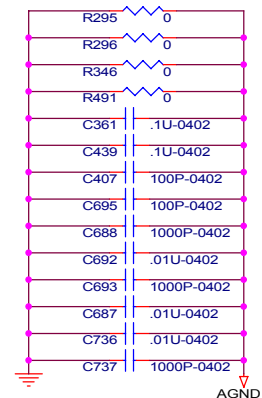
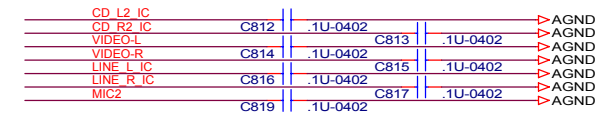
MIC_IN (PINK)



Audio Power

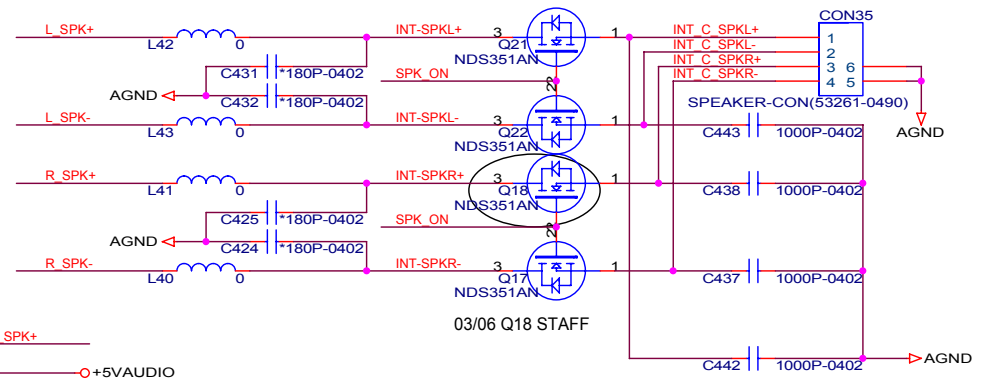
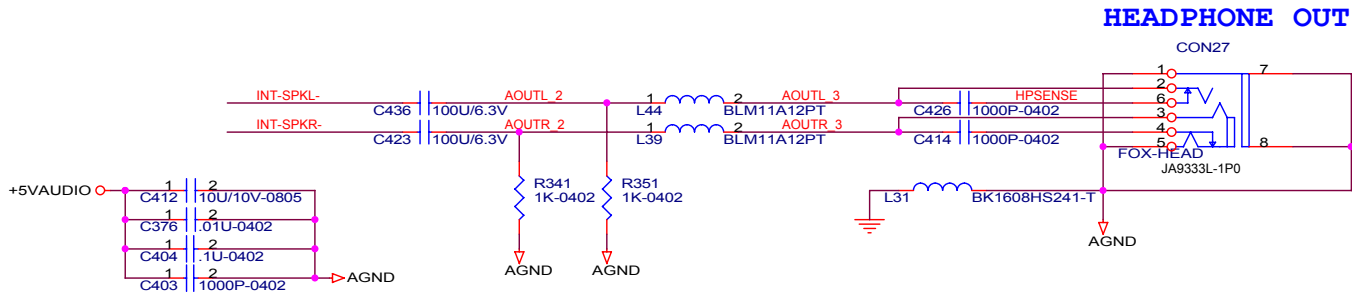
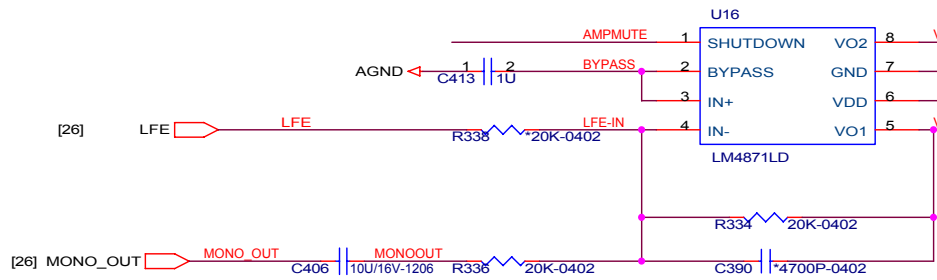
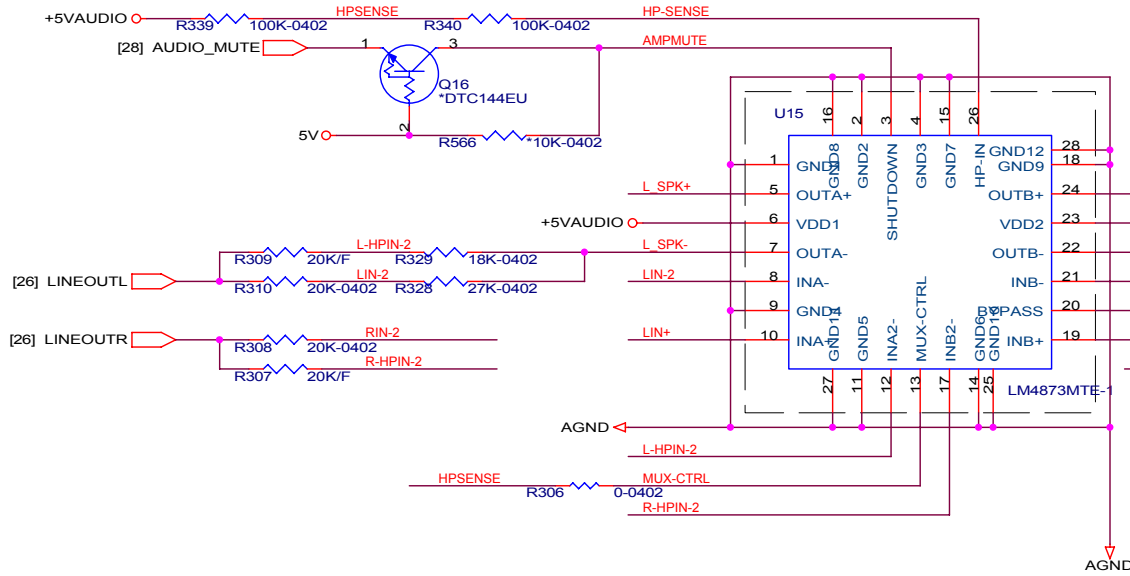


ALC650
/ALC202
/ALC201
/ALC101

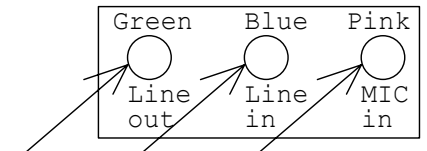
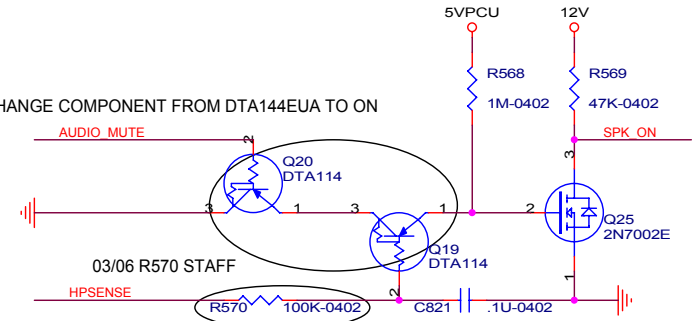


Audio amplifier

03/06 U15 CHANGE COMPONENT FROM LM4873LQ TO LM4873MTE-1

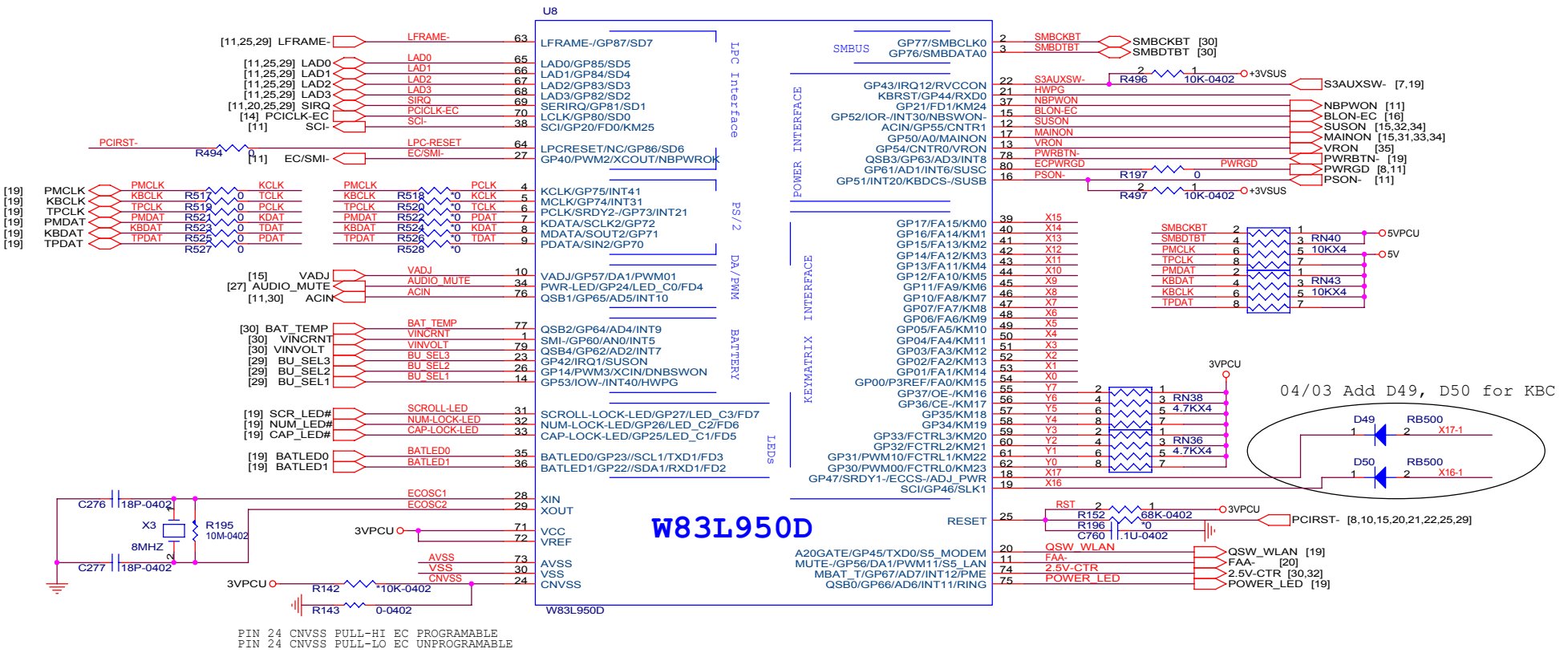


03/06 Q19, Q20 CHANGE COMPONENT FROM DTA144EUA TO ON

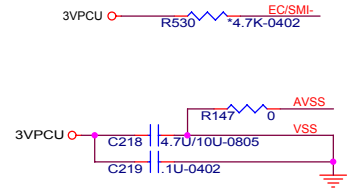
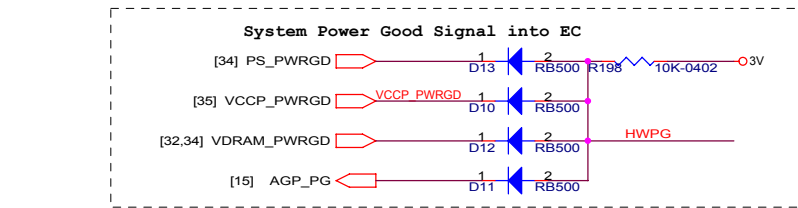


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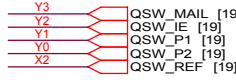
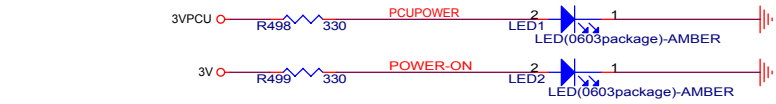
Size Custom	Document Number AUDIO AMPLIFIER(LM4873 & 4871)	Rev E
Date:	Friday, April 04, 2003	Sheet 27 of 35



PIN 24 CNVSS PULL-HI EC PROGRAMABLE
PIN 24 CNVSS PULL-LO EC UNPROGRAMABLE



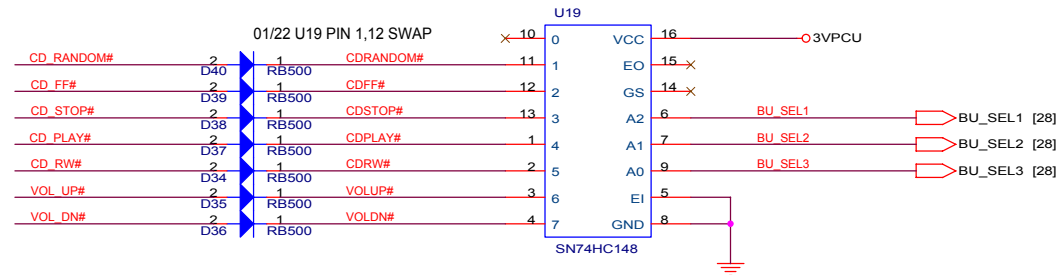
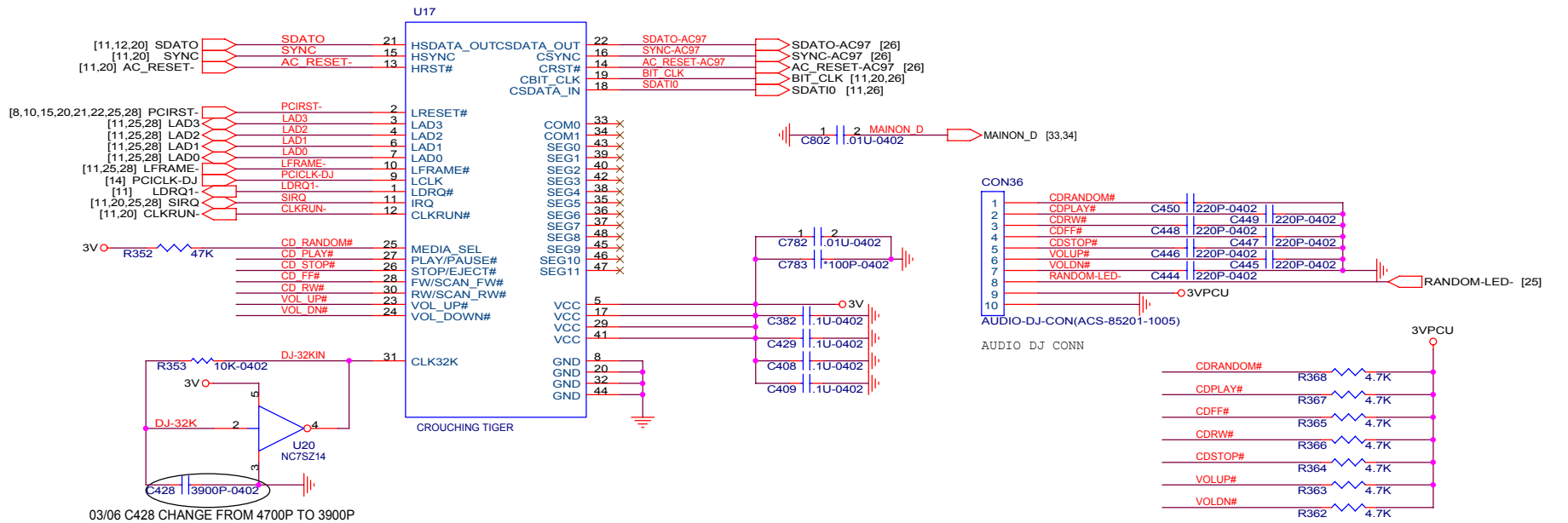
X2 & Y3: E-MAIL
X2 & Y2: EXPLORER
X2 & Y1: P1
X2 & Y0: P2



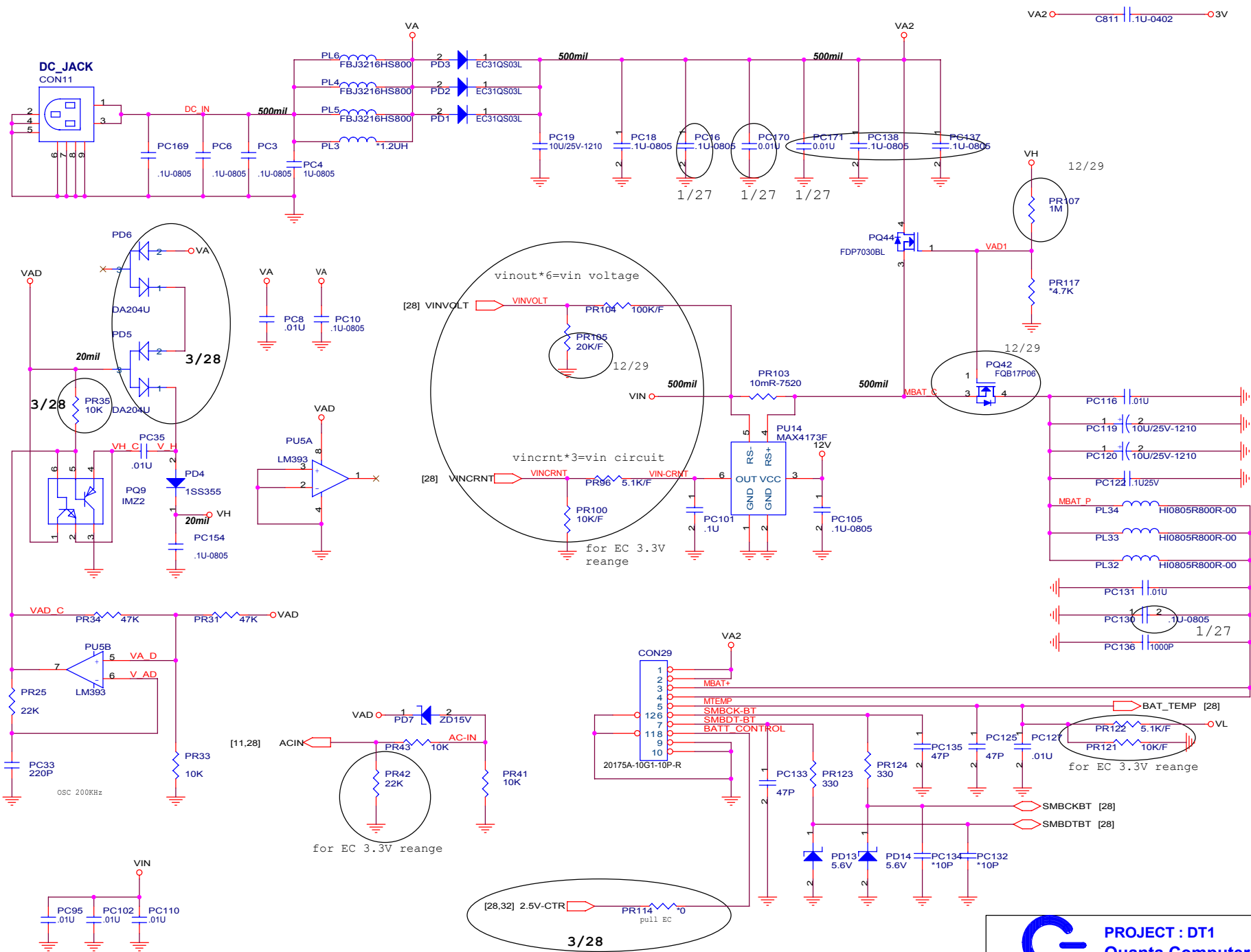
PROJECT : DT1
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Size: Document Number: Rev: E
Customer: EC W83L950D

Date: Friday, April 04, 2003 Sheet 28 of 35



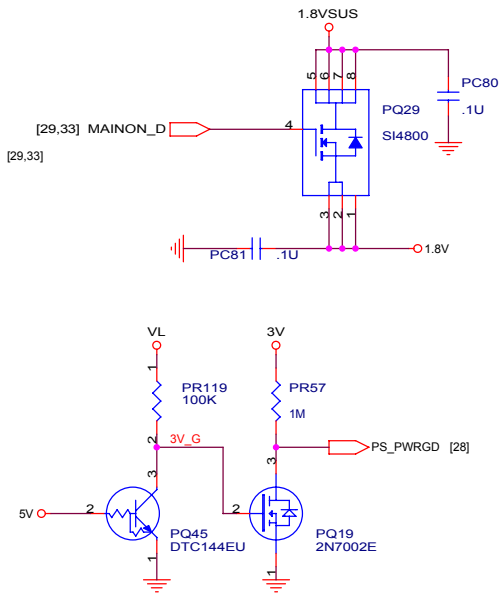
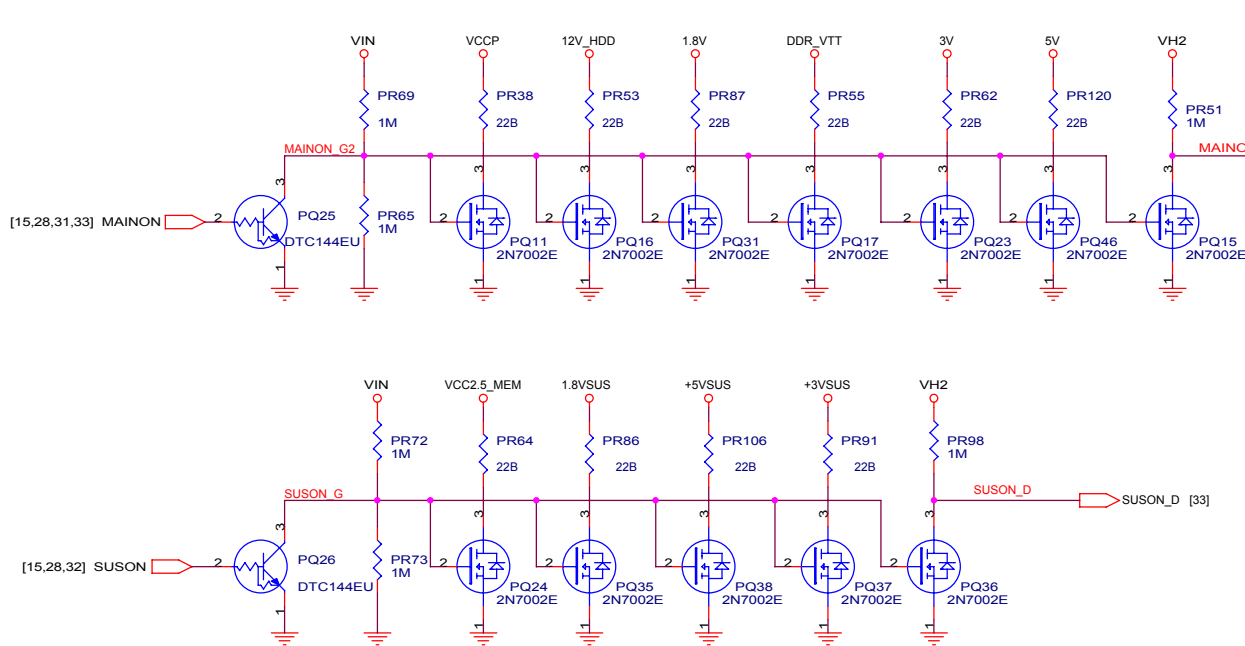
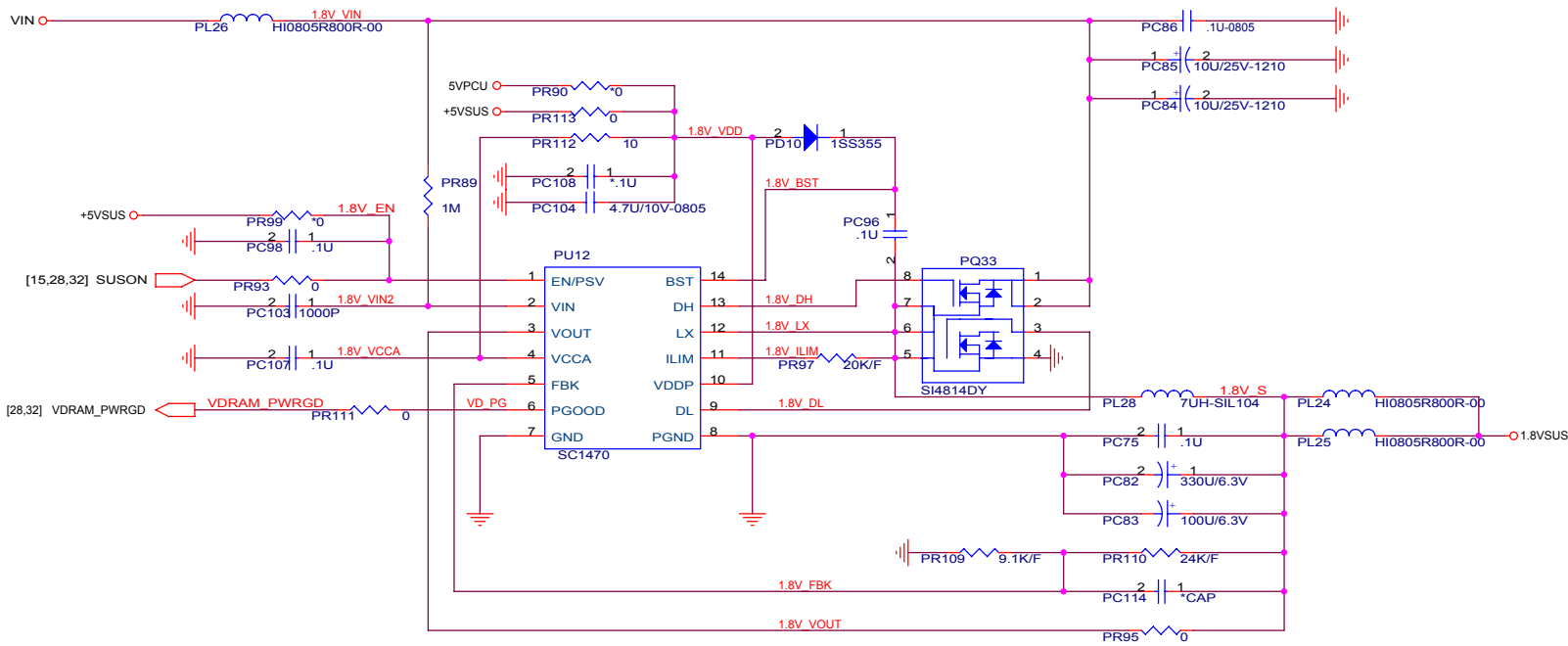
SN74HC148 TABLE												
EI	INPUTS							OUTPUTS				
	0	1	2	3	4	5	6	7	A2	A1	A0	GS EO
H	X	X	X	X	X	X	X	X	H	H	H	H H
L	H	H	H	H	H	H	H	H	H	H	H	H L
L	X	X	X	X	X	X	X	L	L	L	L	L H
L	X	X	X	X	X	X	L	H	L	L	H	L H
L	X	X	X	X	L	H	H	H	L	H	H	L H
L	X	X	X	L	H	H	H	H	H	L	L	L H
L	X	X	L	H	H	H	H	H	H	L	H	L H
L	X	L	H	H	H	H	H	H	H	H	L	L H
L	L	H	H	H	H	H	H	H	H	H	H	L H



PROJECT : DT1
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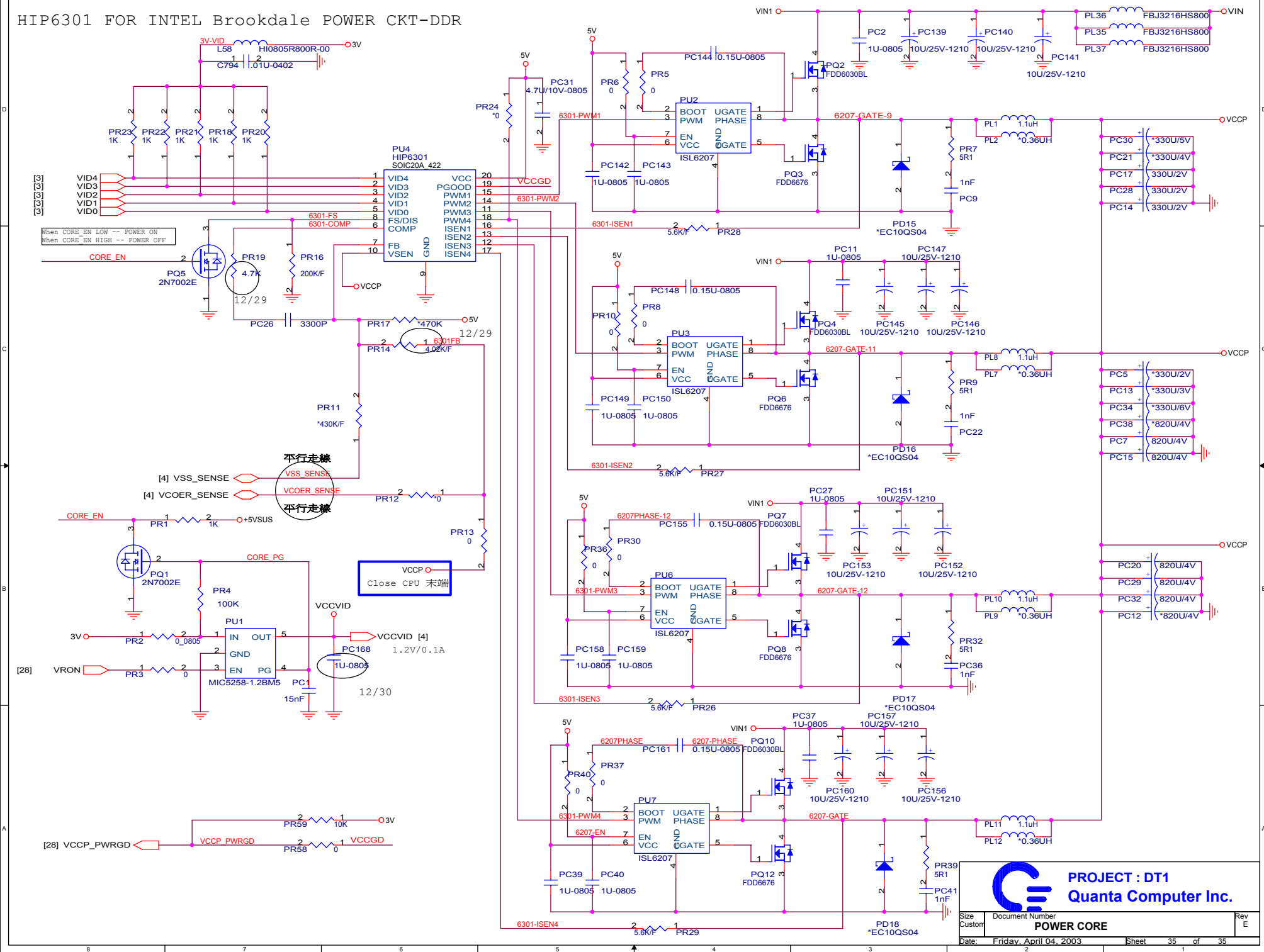
Size Custom Document Number **BATTERY CONN & POWER JACK** Rev E

Date: Friday, April 04, 2003 Sheet 30 of 35



PROJECT : DT1
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H1P6301 FOR INTEL Brookdale POWER CKT-DDR



PROJECT : DT1
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Size Custom	Document Number POWER CORE		
Date:	Friday, April 04, 2003	Sheet	35 of 35