

ICH9M Functional Strap Definitions

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Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPI020	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPI049	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPI033/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

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SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPI016	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN. GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

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Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default). 1 = Digital Display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

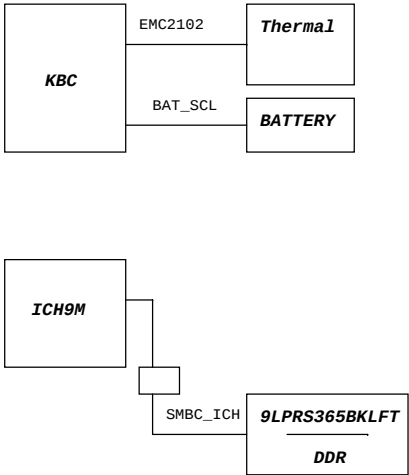
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	NC
LANE4	NC
LANE5	NewCard
LANE6	NC

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	Bluetooth
6	NC
7	MINIC1
8	WEBCAM
9	NEW1
10	Card Reader
11	NC

SMBus



緯創資通 Wistron Corporation	
21F, 80, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Reference	
Size A3	Document Number
Cathedral Peak II	
Date: Friday, June 20, 2008	Rev SB
Sheet 2	of 43

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Side Band
Non GTL

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BGA479-SKT6-GPU6

62.10079.001

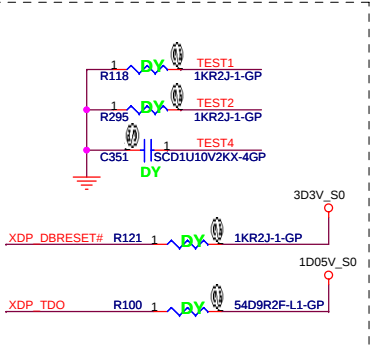
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1005V_S0

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XDP TDI R101 1 54D9R2F-L1-GP
XDP BPM#5 R97 1 54D9R2F-L1-GP
H_CPURST# R116 1 51R2F-2-GP
XDP TRCK R94 1 54D9R2F-L1-GP
XDP TRST# R96 1 54D9R2F-L1-GP

All place within 2" to CPU

Follow Demo Circuit

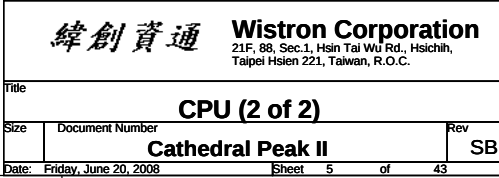


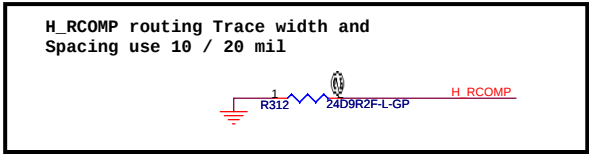
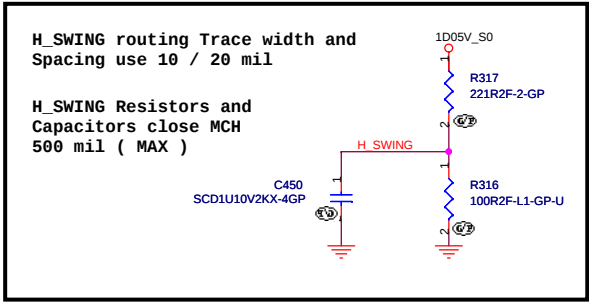
Net "TEST4" as short as possible,
make sure "TEST4" routing is
reference to GND and away other
noisy signals

Layout Note:
Comp0, 2 connect with Z0=27.4 ohm, make
trace length shorter than 0.5"
Comp1, 3 connect with Z0=55 ohm, make
trace length shorter than 0.5"

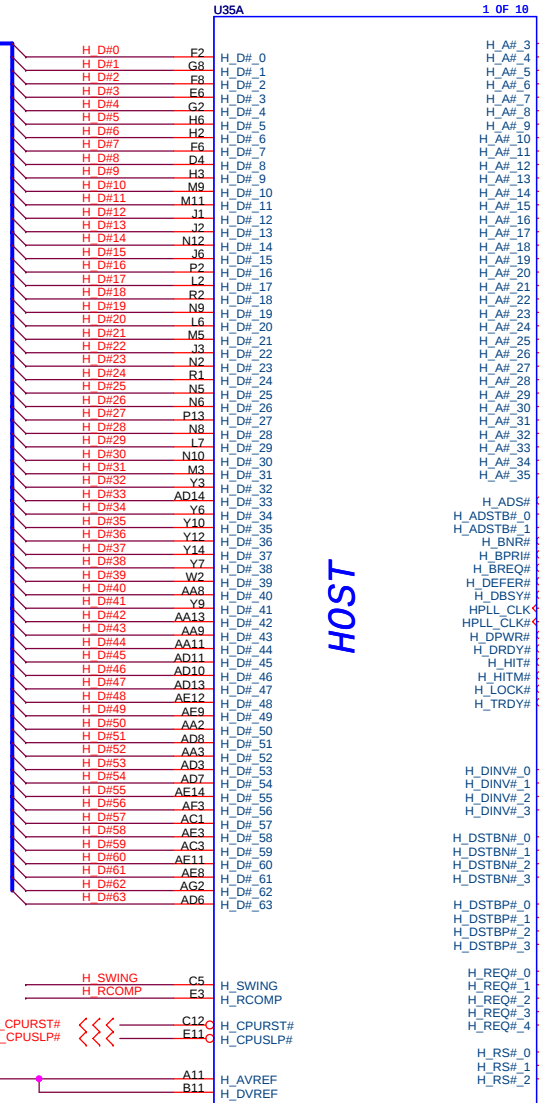
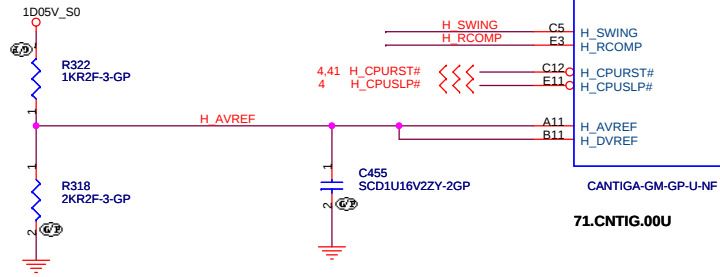
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Title			CPU (1 of 2)	
Size	Document Number		Rev	SB
Date: Friday, June 20, 2008			Sheet 4 of 43	

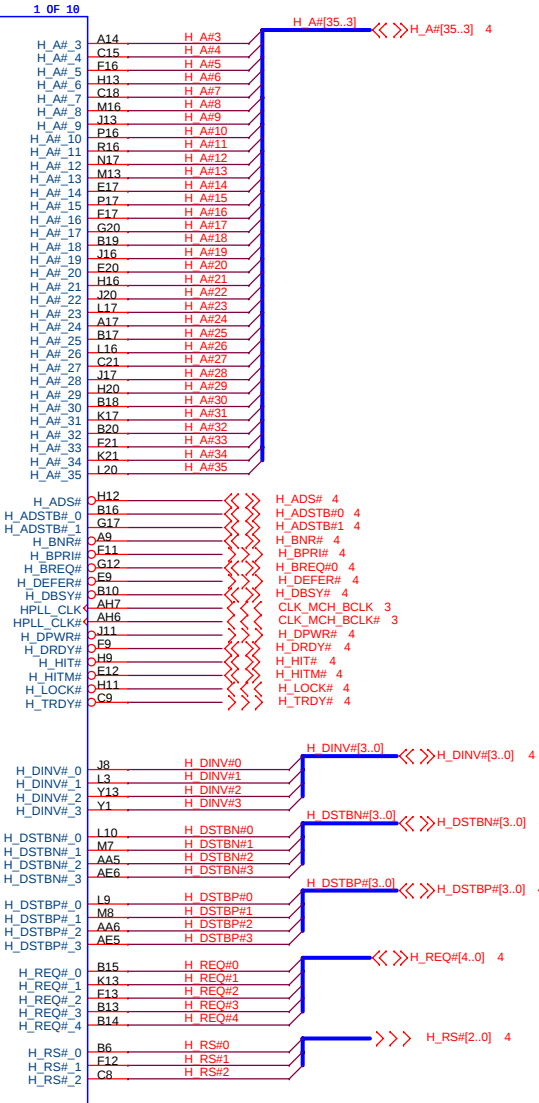


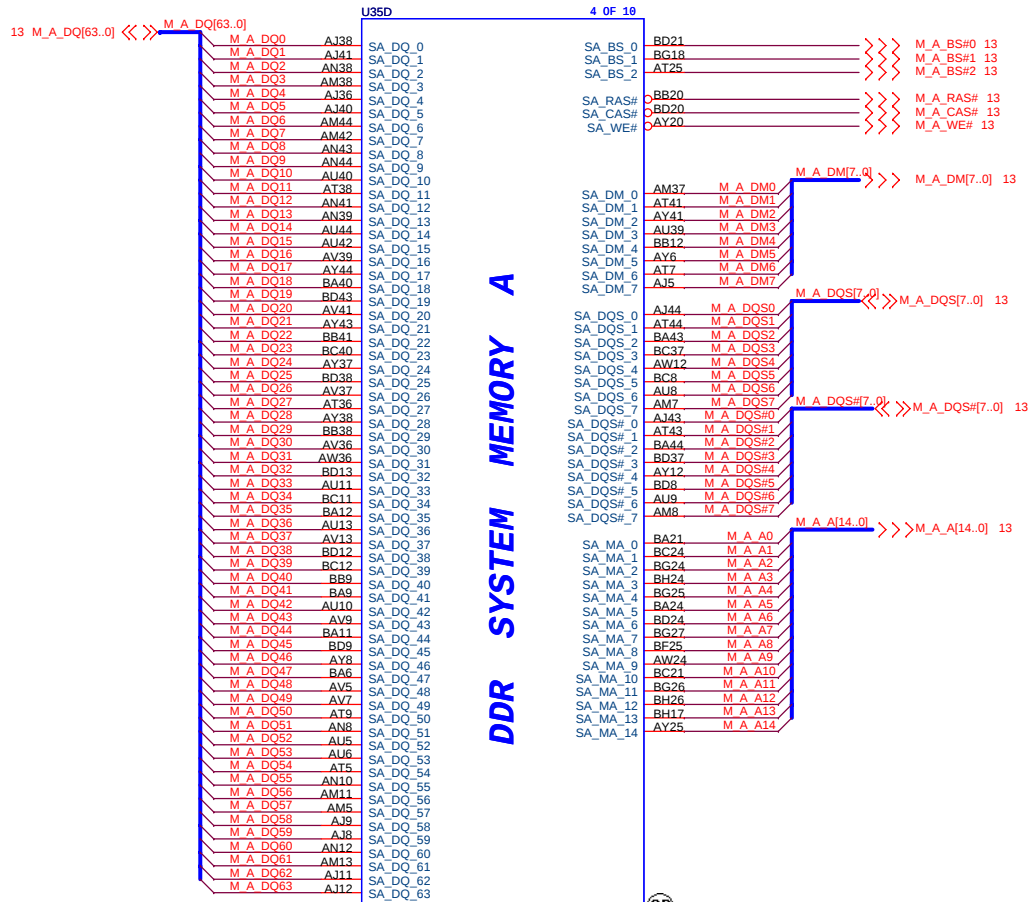


Place them near to the chip (< 0.5")



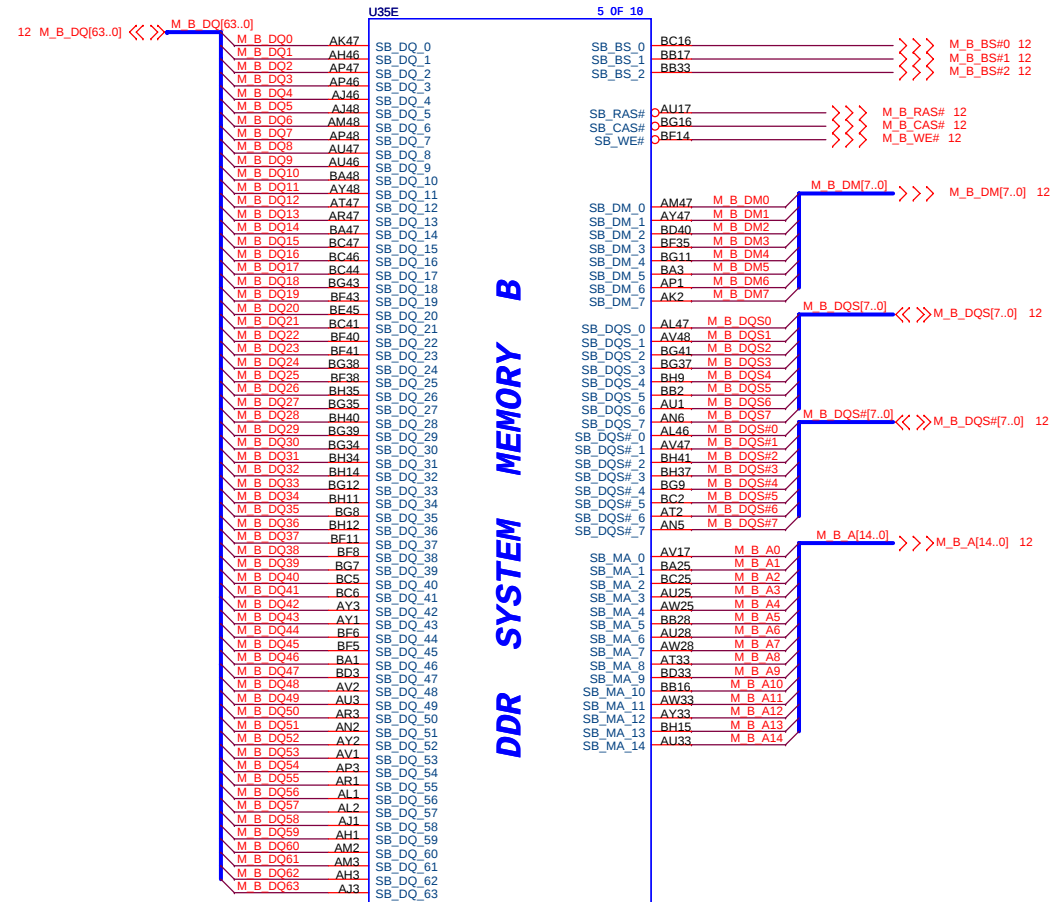
HOST





CANTIGA-GM-GP-U-NF

71.CNTIG.00U

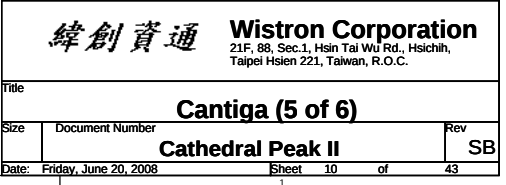


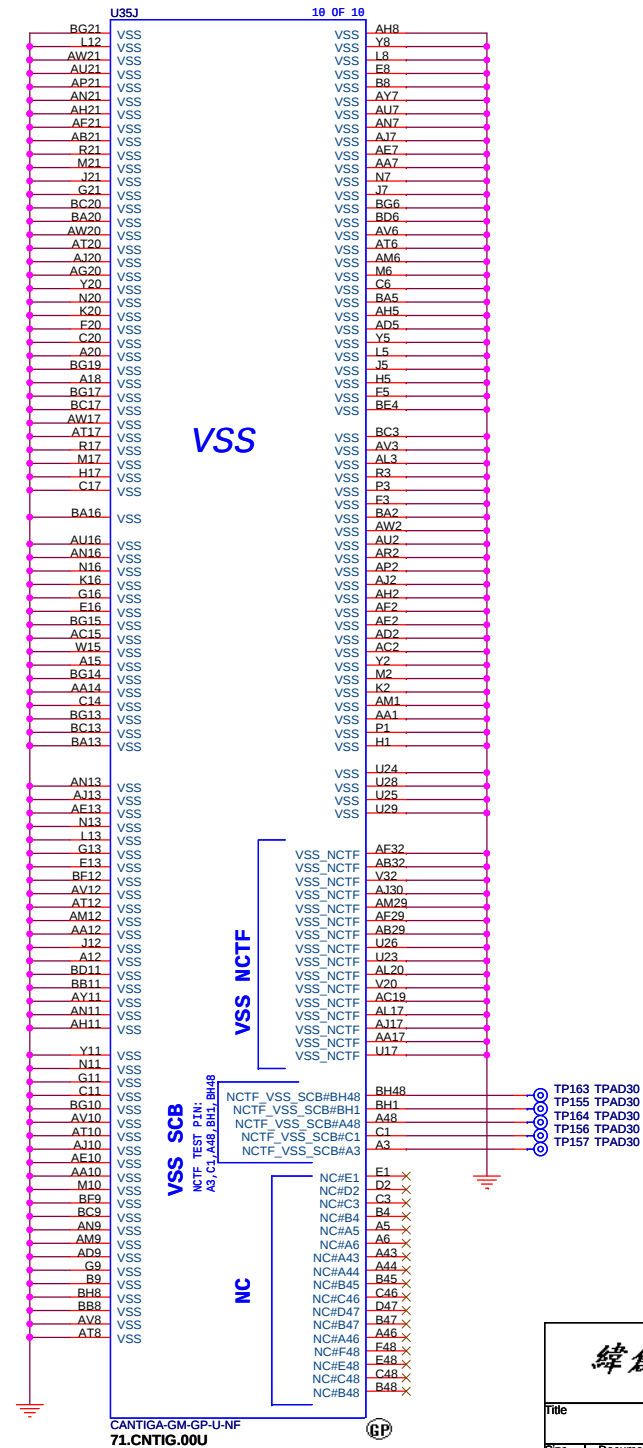
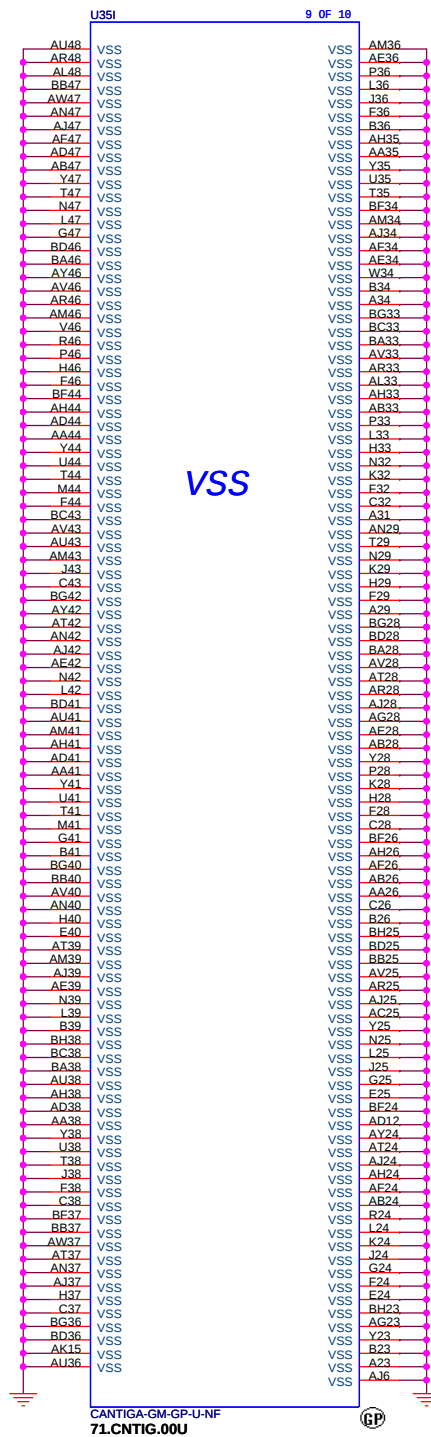
CANTIGA-GM-GP-U-NF

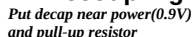
71.CNTIG.00U

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Title		
Cantiga (3 of 6)		
Size	Document Number	Rev
Cathedral Peak II		SB
Date:	Friday, June 20, 2008	Sheet 8 of 43



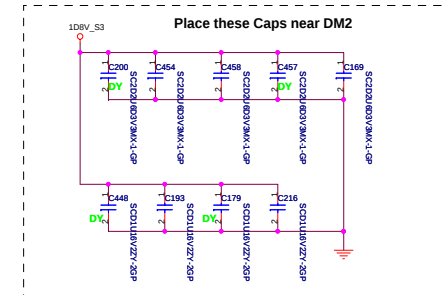
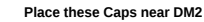




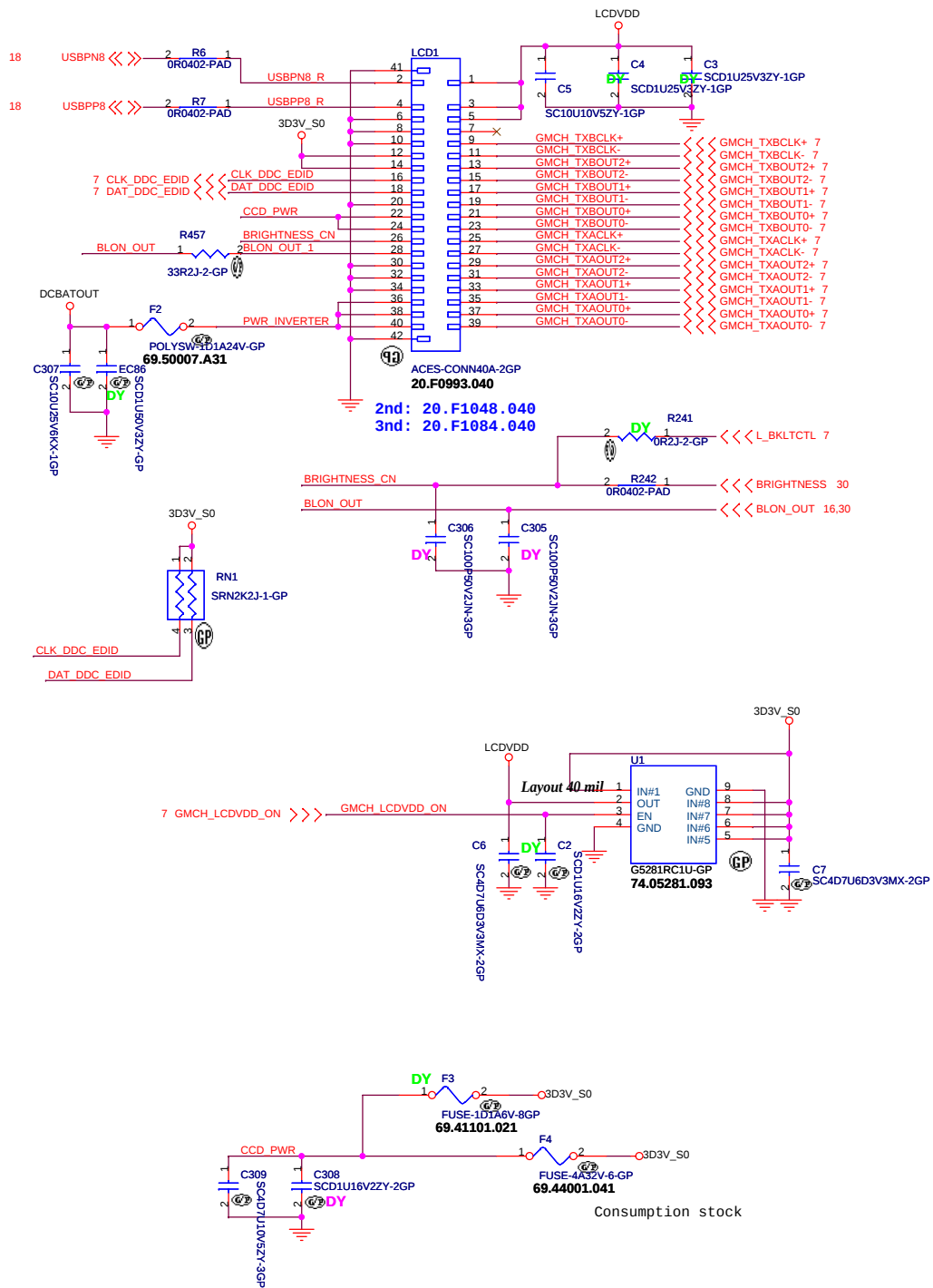
Put decap near power(0.9V) and pull-up resistor



**Put decap near power(0.9V)
and pull-up resistor**



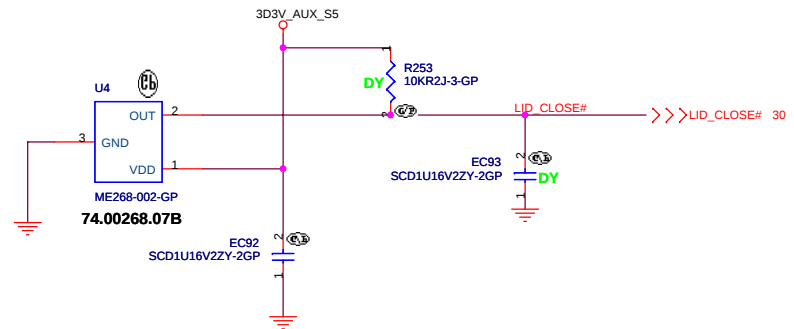
LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

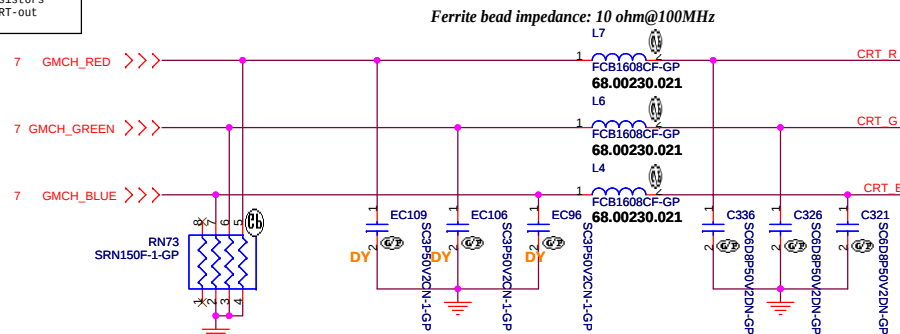
Cover Up Switch



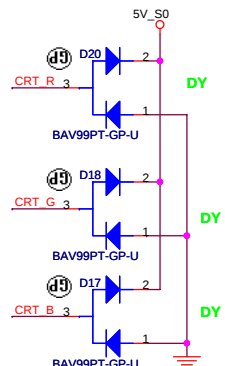
74.00268.A7B

74.00268.C7B

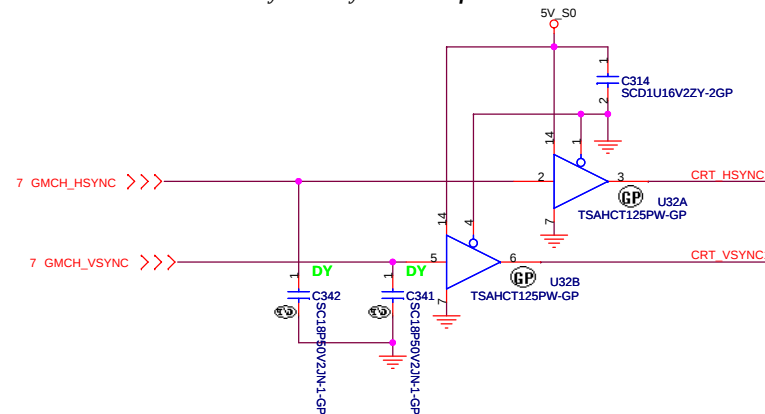
Layout Note:
Place these resistors
close to the CRT-out
connector



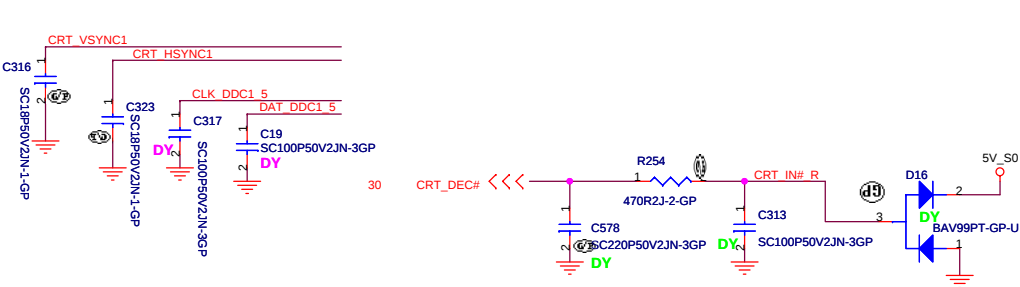
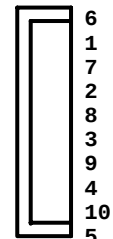
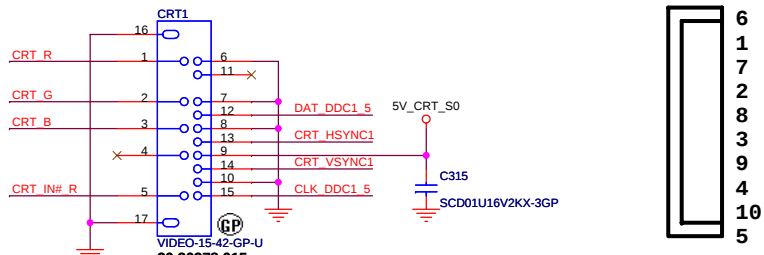
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



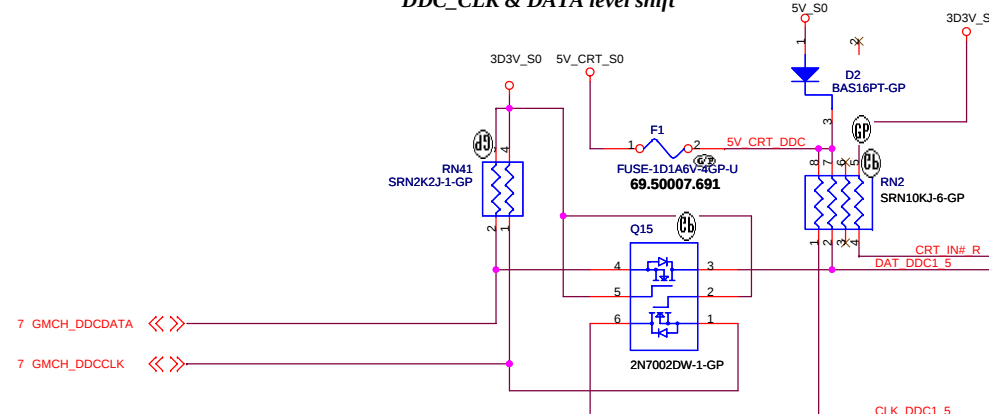
Hsync & Vsync level shift



CRT I/F & CONNECTOR

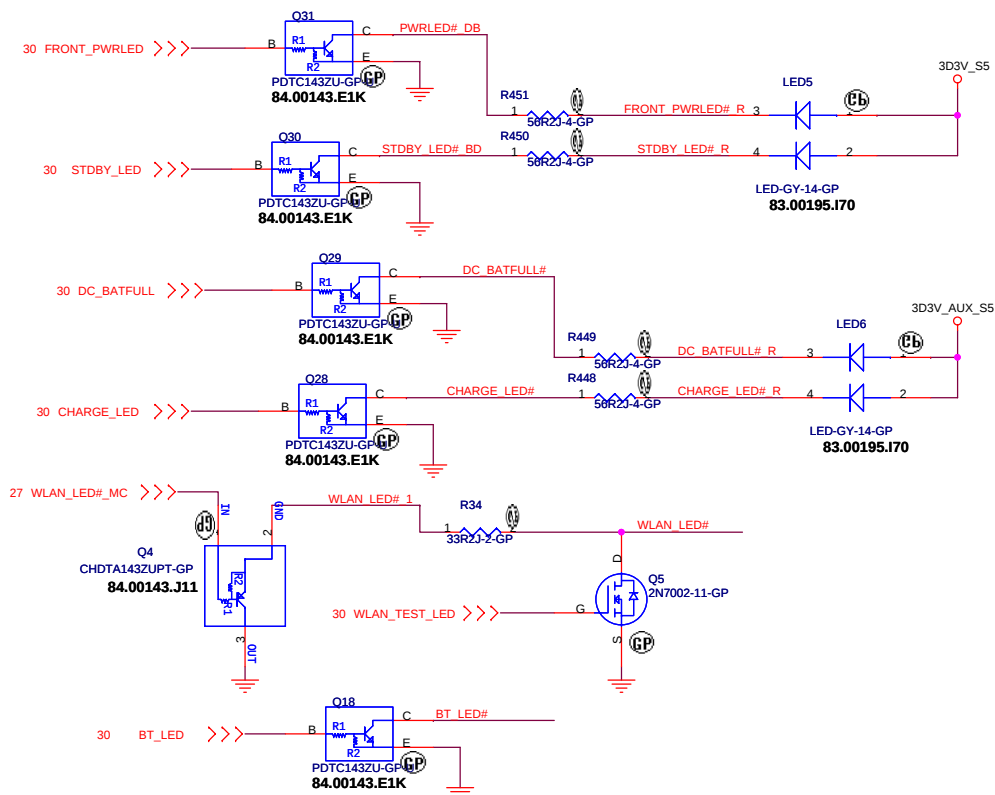


DDC_CLK & DATA level shift

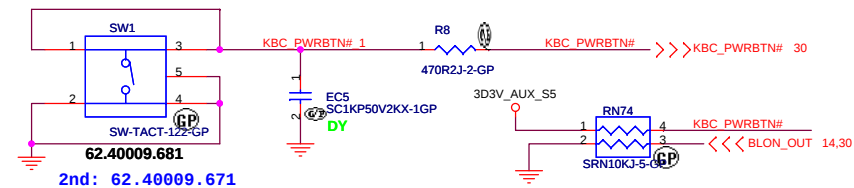


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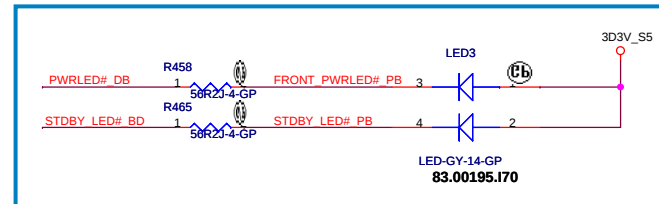
Title		CRT Connector	
Size	Document Number	Rev	
Date: Friday, June 20, 2008		Sheet 15 of 43	
Cathedral Peak II		SB	



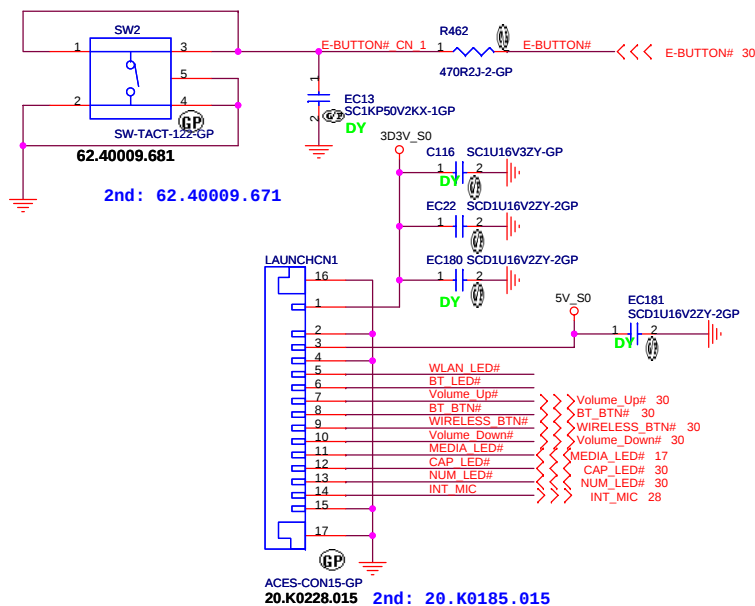
Power Button



SB



E Power Button

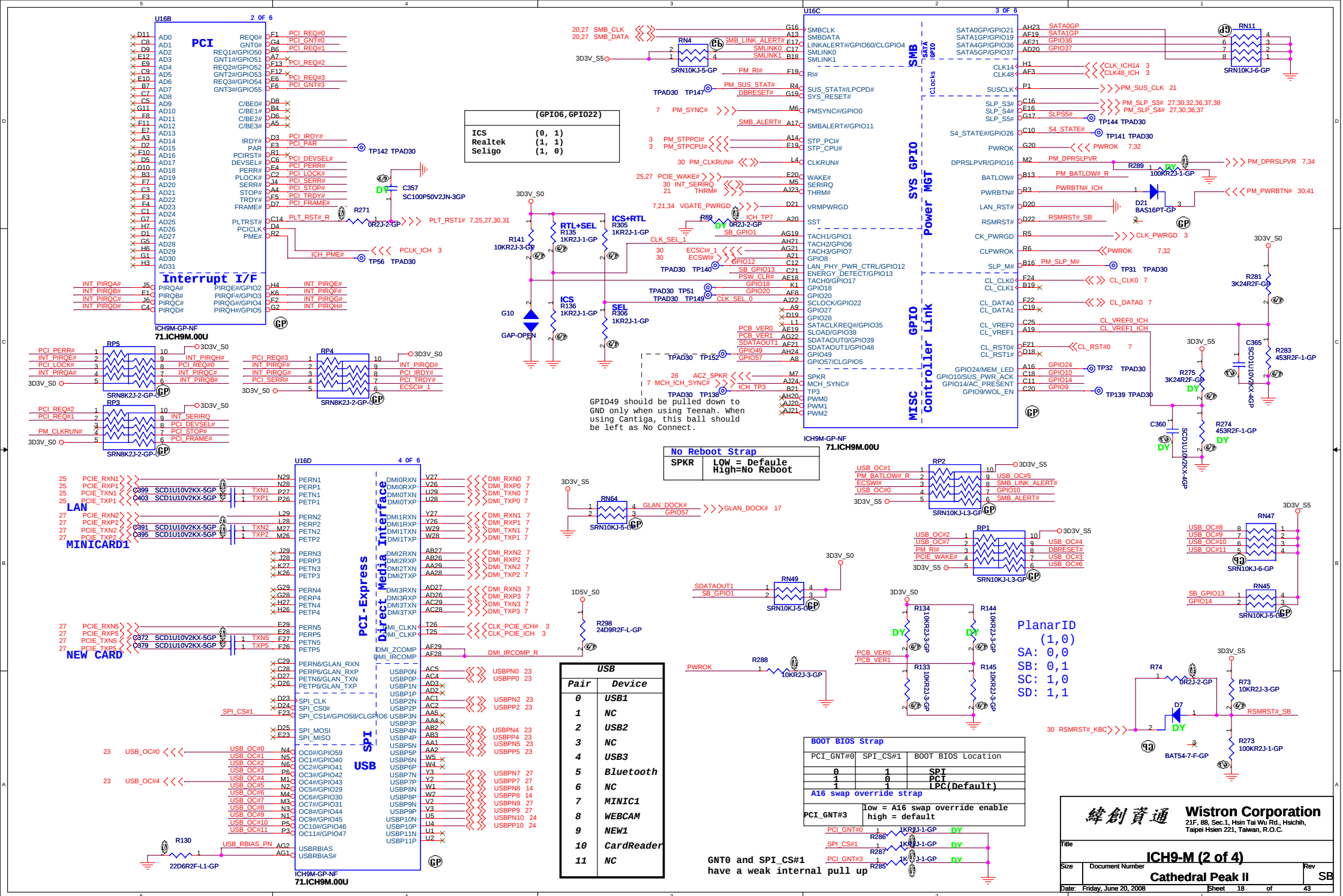


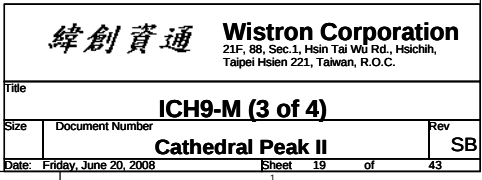
WLAN_LED#	DY	EC11	SC220P50V2JN-3GP
BT_LED#	DY	EC182	SC220P50V2JN-3GP
Volume_Up#	DY	EC141	SC220P50V2JN-3GP
BT_BTN#	DY	EC142	SC220P50V2JN-3GP
WIRELESS_BTN#	DY	EC143	SC220P50V2JN-3GP
Volume_Down#	DY	EC144	SC220P50V2JN-3GP
MEDIA_LED#	DY	EC123	SC220P50V2JN-3GP
CAP_LED#	DY	EC122	SC220P50V2JN-3GP
NUM_LED#	DY	EC121	SC220P50V2JN-3GP
INT_MIC	DY	EC149	SC220P50V2JN-3GP

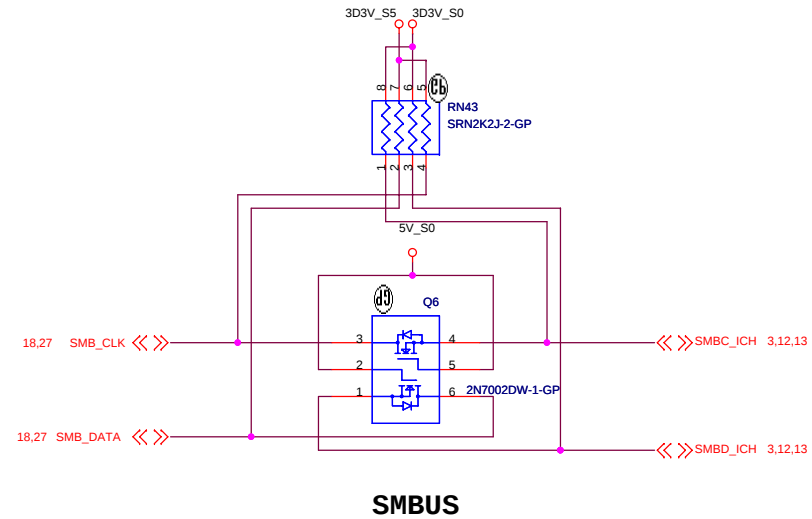
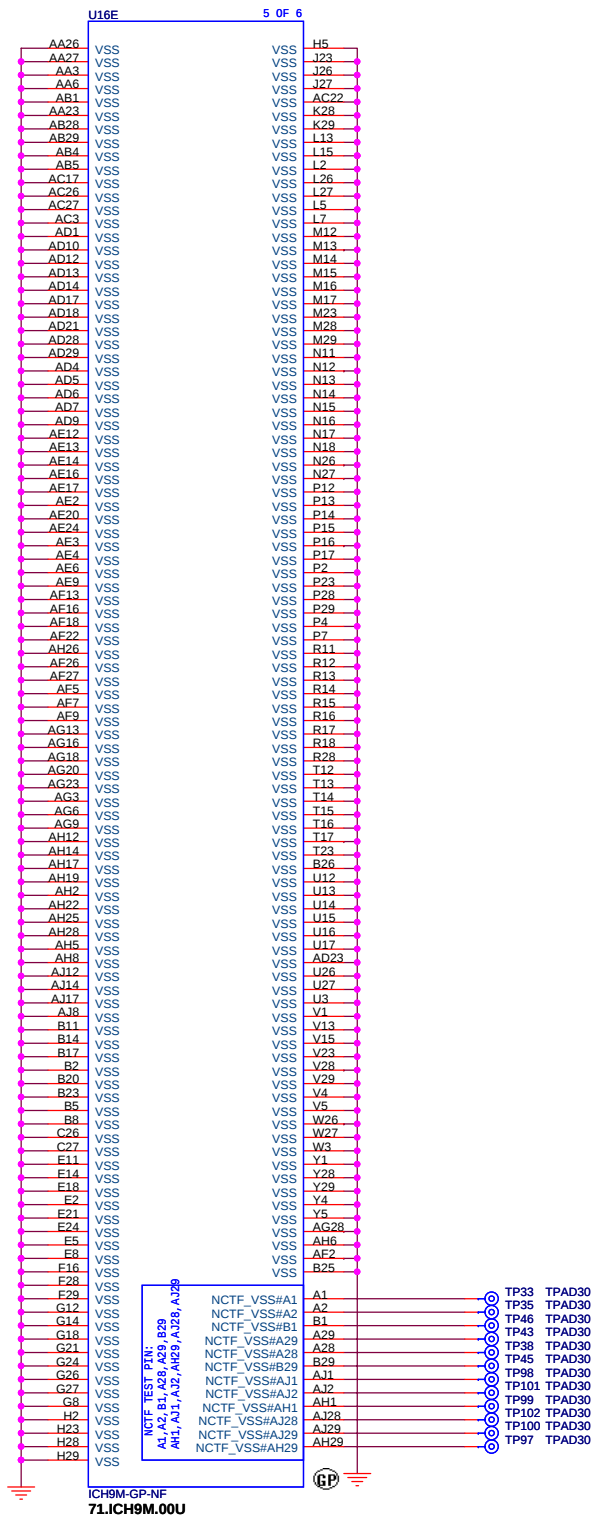
3D3V_S0	1	AFTE30-GP	TP58
5V_S0	1	AFTE30-GP	TP189
WLAN_LED#	1	AFTE30-GP	TP190
BT_LED#	1	AFTE30-GP	TP191
Volume_Up#	1	AFTE30-GP	TP192
BT_BTN#	1	AFTE30-GP	TP193
WIRELESS_BTN#	1	AFTE30-GP	TP194
Volume_Down#	1	AFTE30-GP	TP195
MEDIA_LED#	1	AFTE30-GP	TP53
CAP_LED#	1	AFTE30-GP	TP54
NUM_LED#	1	AFTE30-GP	TP55
INT_MIC	1	AFTE30-GP	TP178

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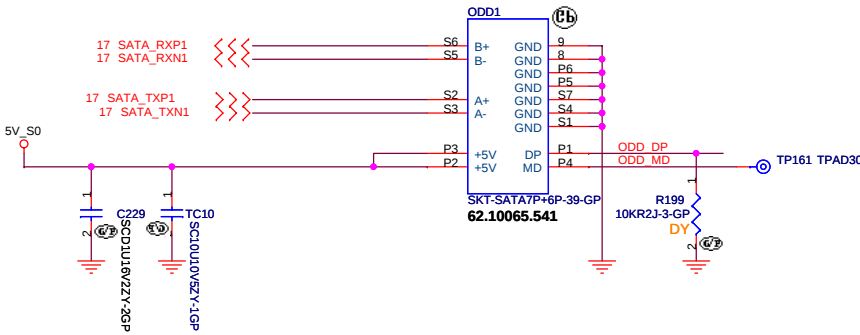
Title	POWER /LAUNCH/LED BOARD		
Size	Document Number	Rev	
Cathedral Peak II		SB	
Date: Friday, June 20, 2008	Sheet	16	of 43



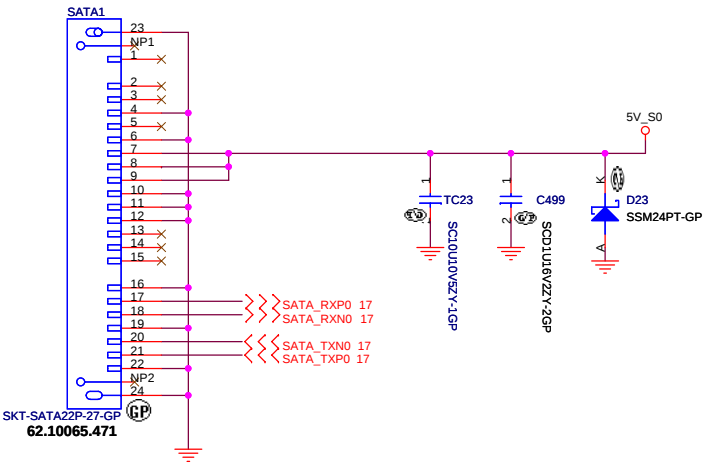


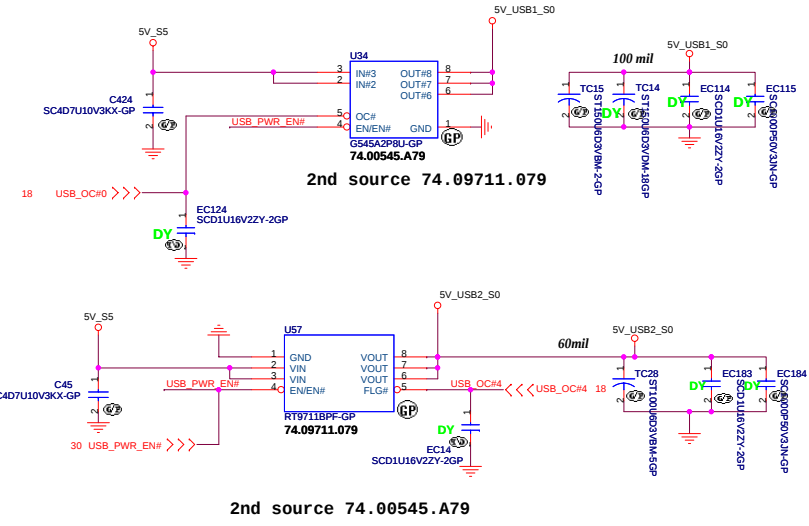
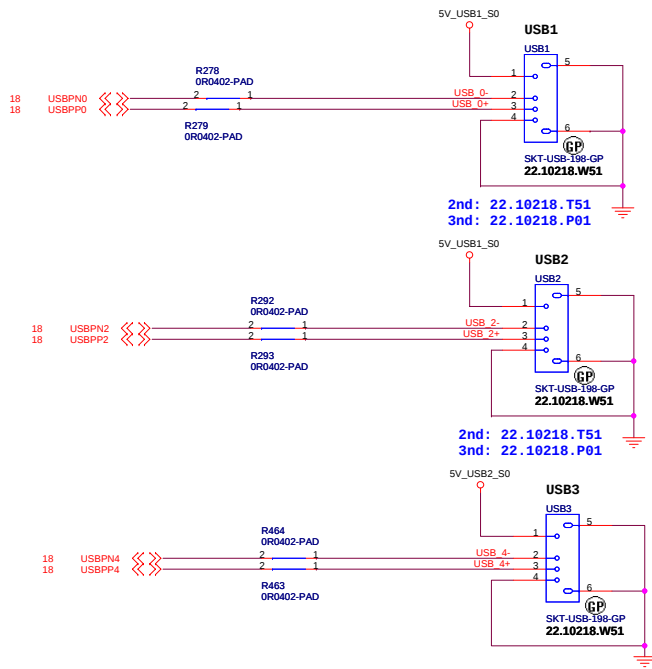


SATA ODD Connector



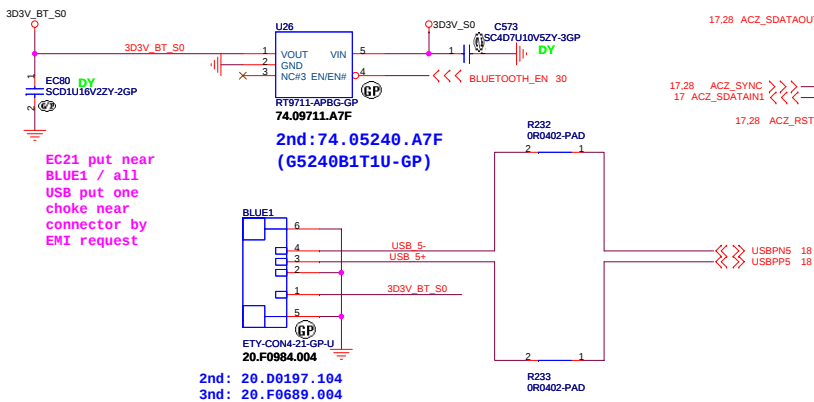
SATA Connector



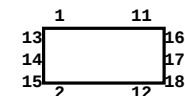
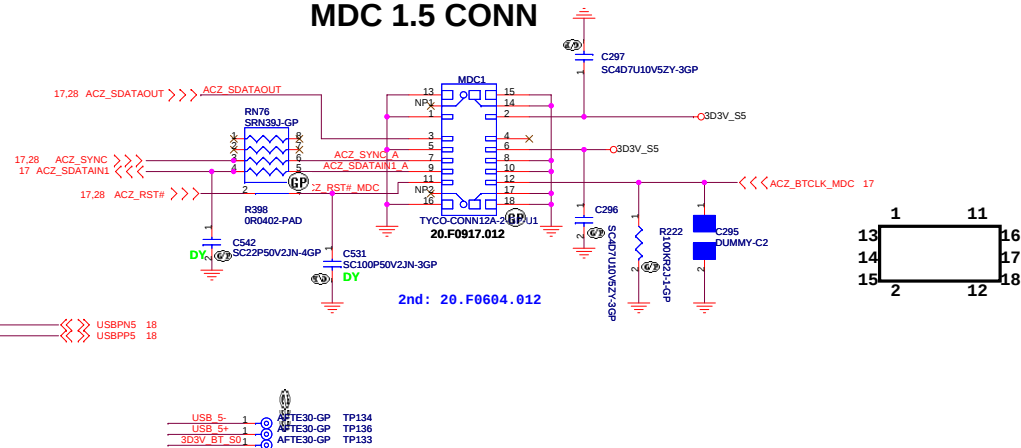


BLUETOOTH MODULE

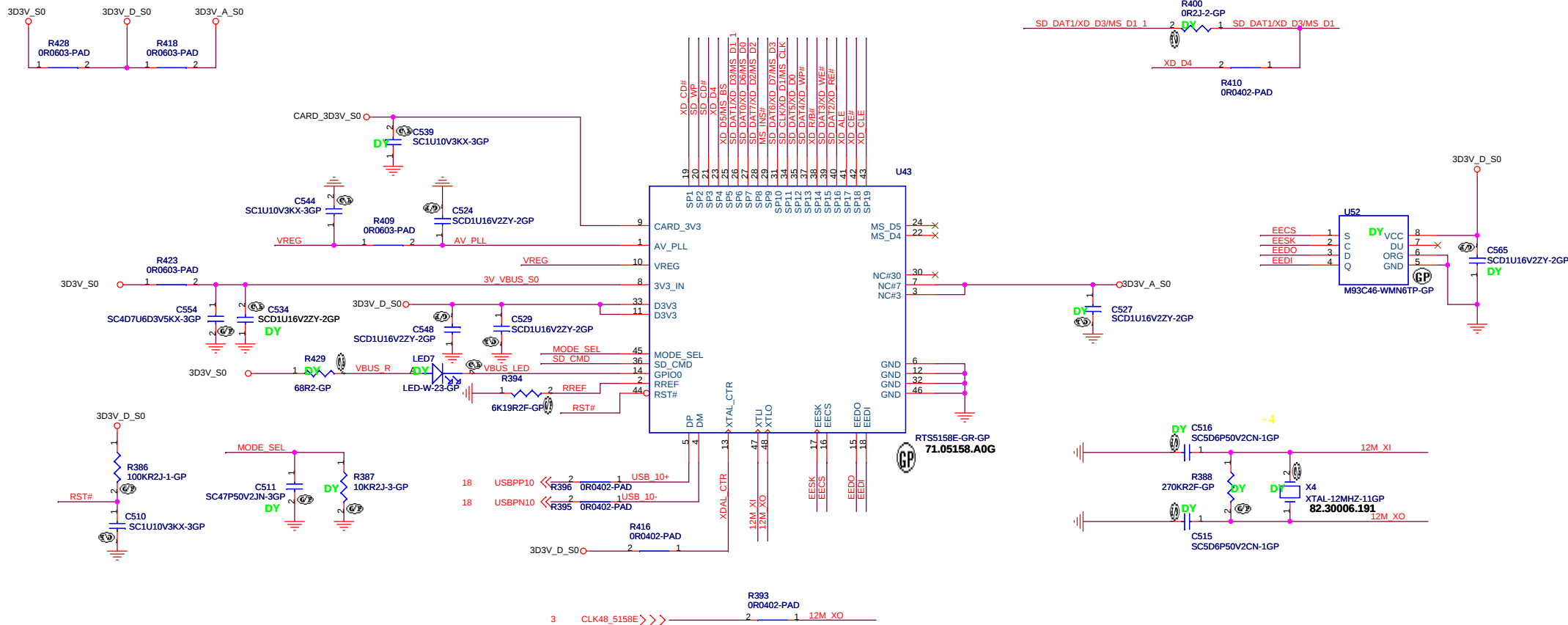
1.5A / High Active Voltage 2V



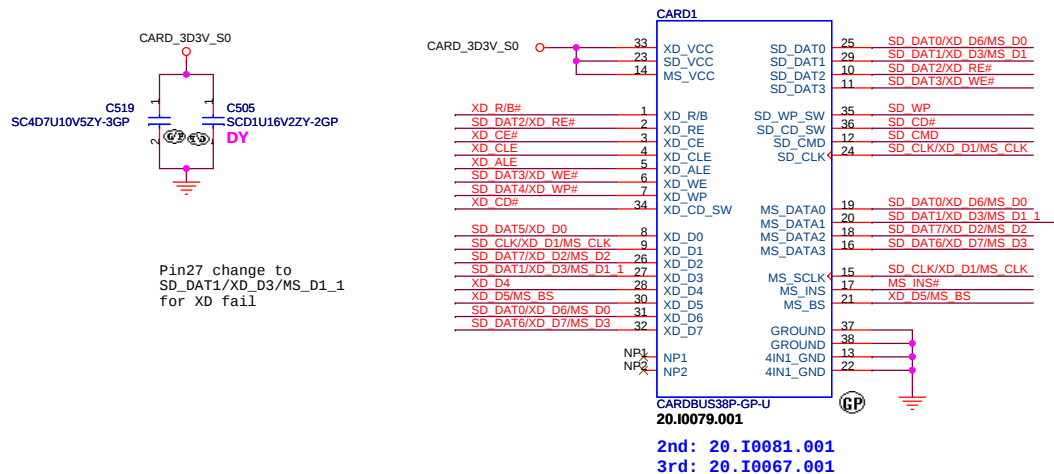
MDC 1.5 CONN

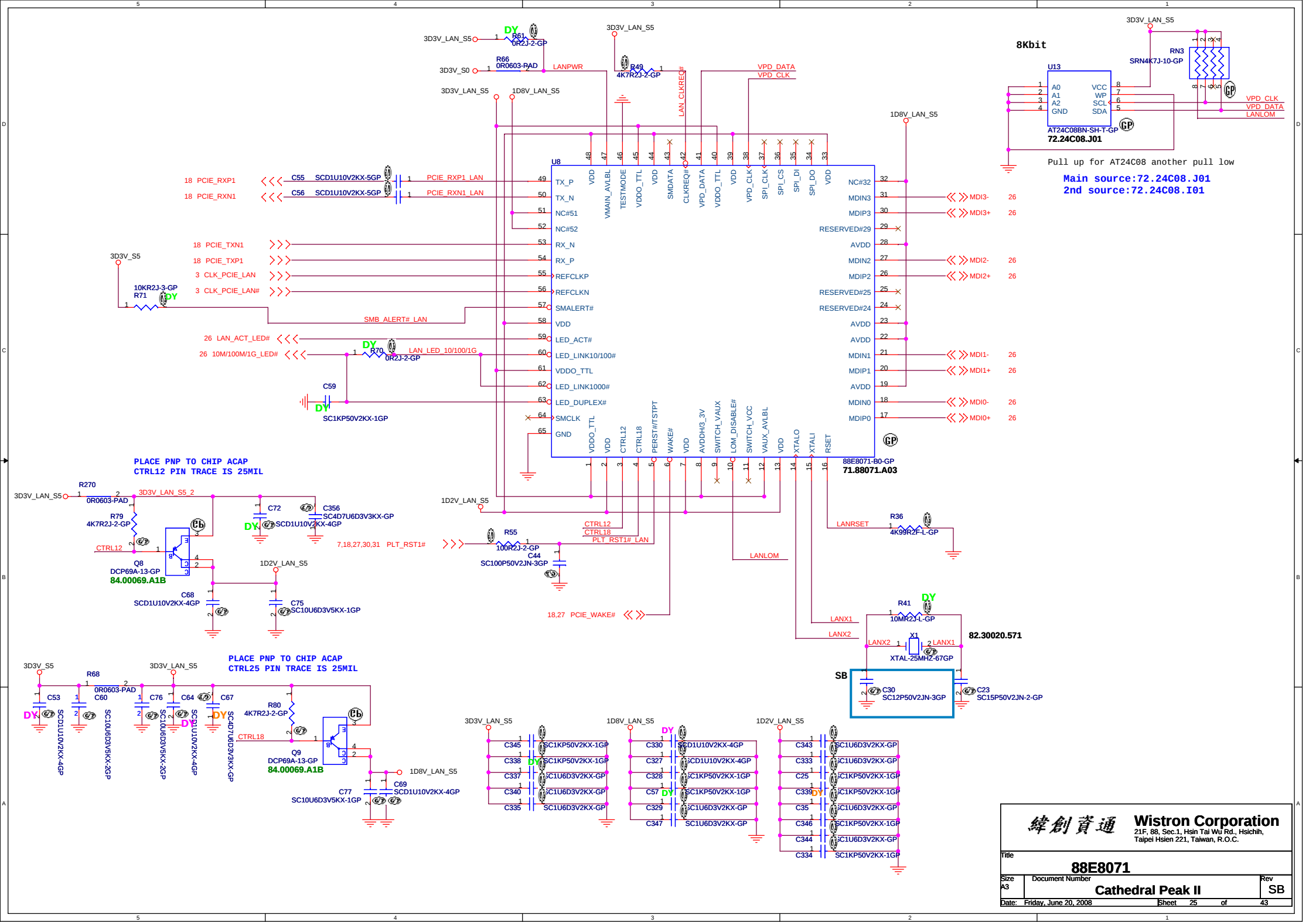


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Title			
USB/BLUETOOTH/MDC			
Size	Document Number	Cathedral Peak II	Rev
			SB
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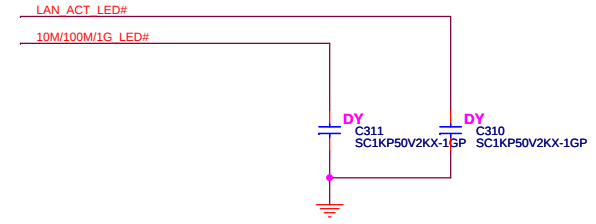
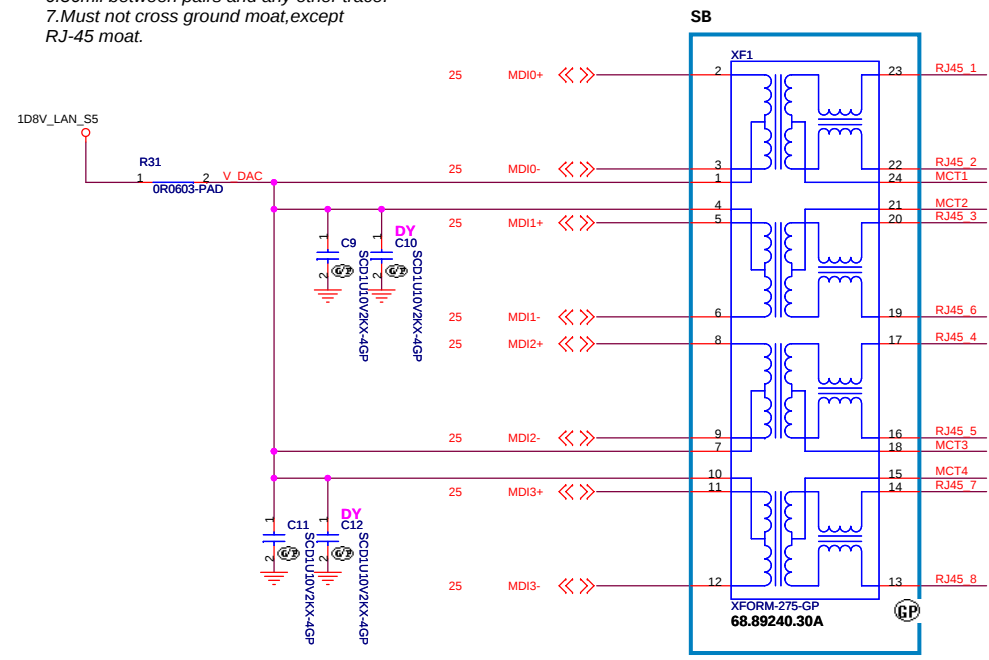
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



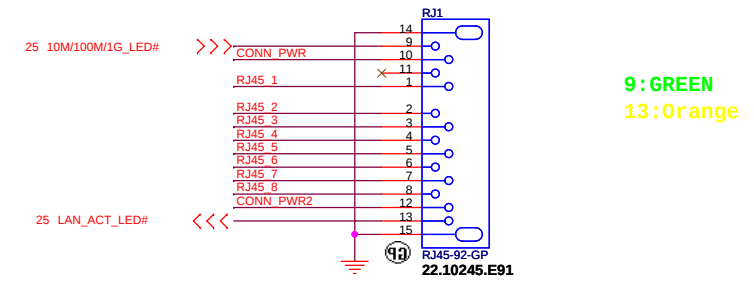


LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



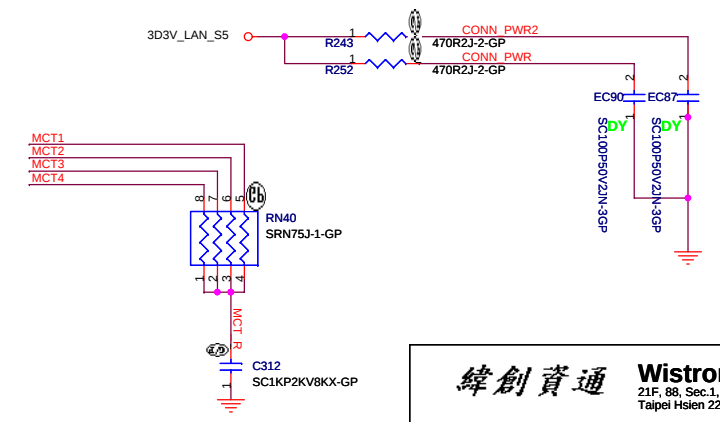
LAN Connector



LAN Link: Green(9), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(13), when LAN is transferring data.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



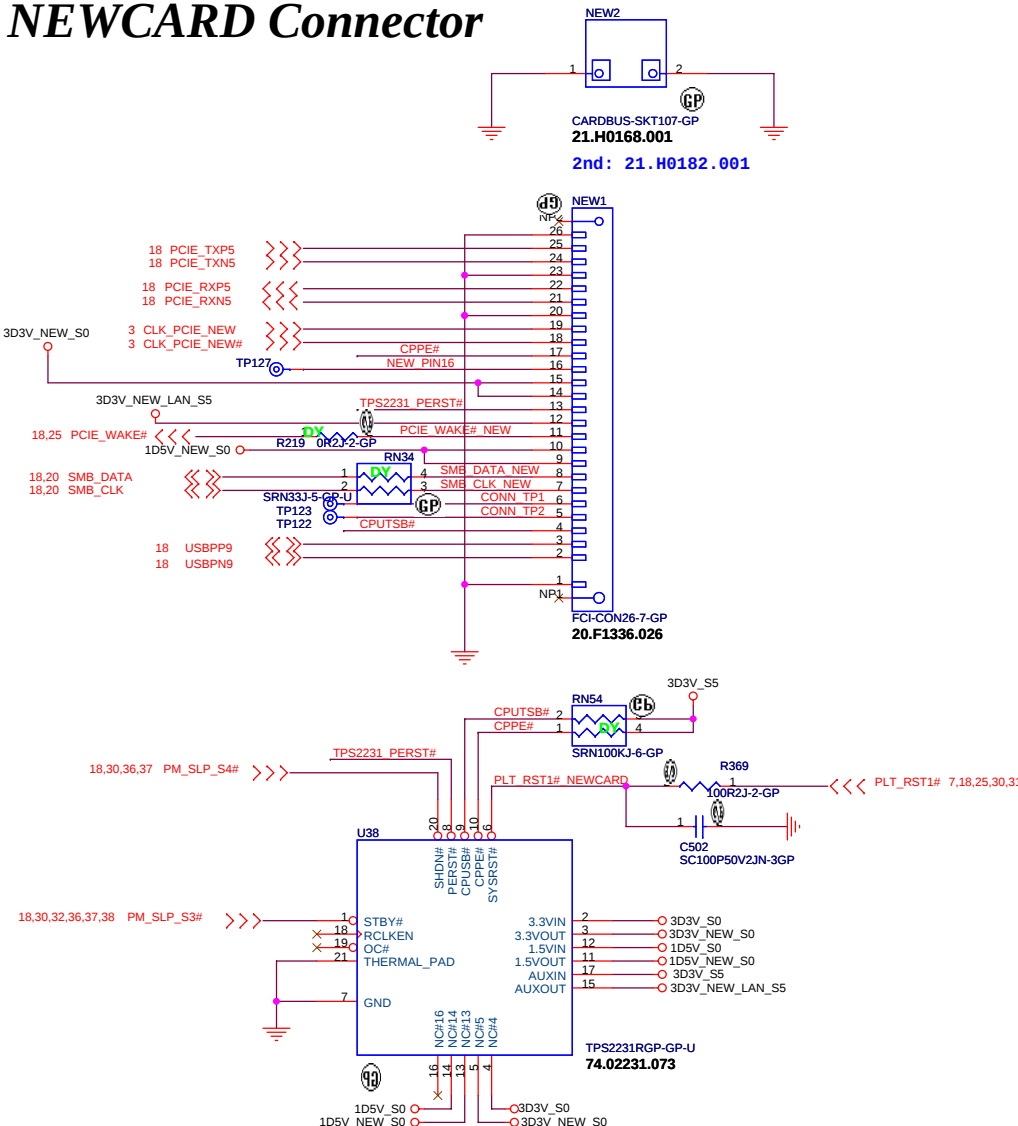
緯創資通

Wistron Corporation

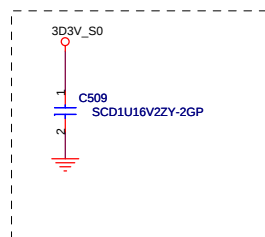
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Title		
LAN CONN		
Size	Document Number	Rev
A3	Cathedral Peak II	SB
Date:	Friday, June 20, 2008	Sheet 26 of 43

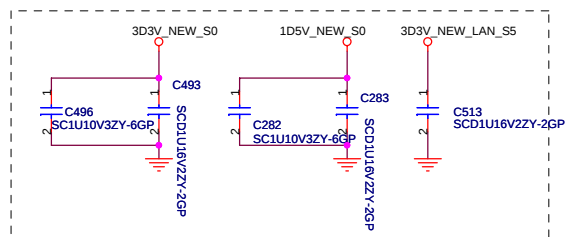
NEWCARD Connector



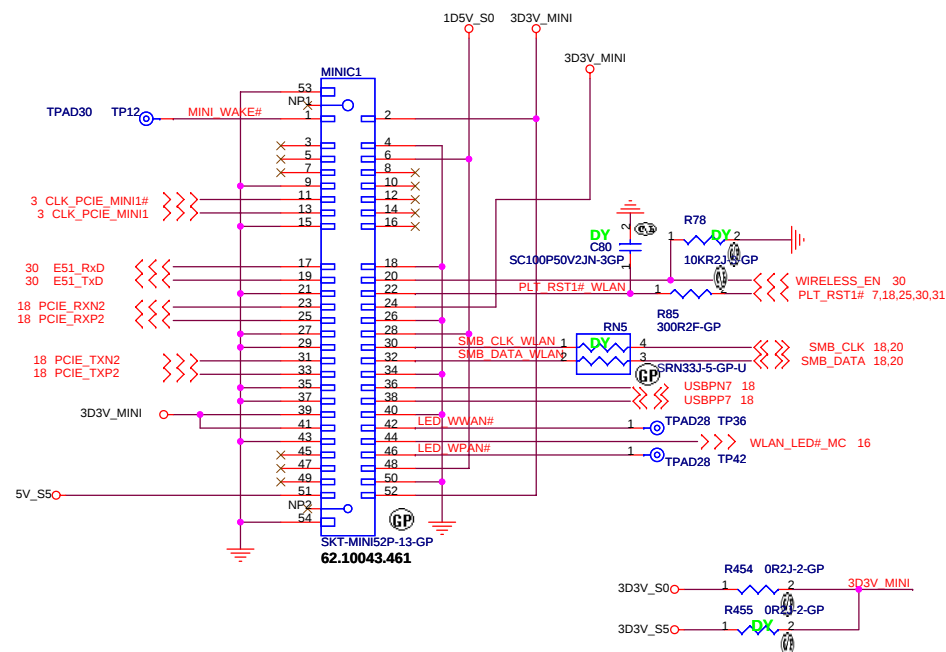
Place them Near to Chip



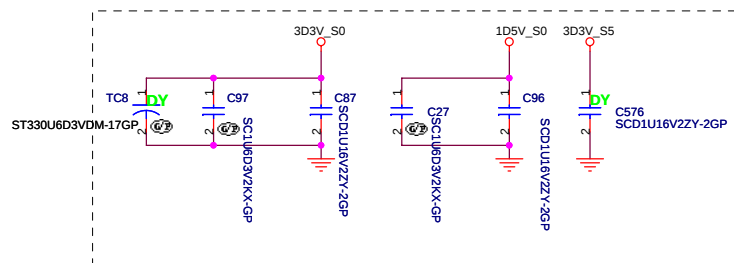
Place them Near to Connector

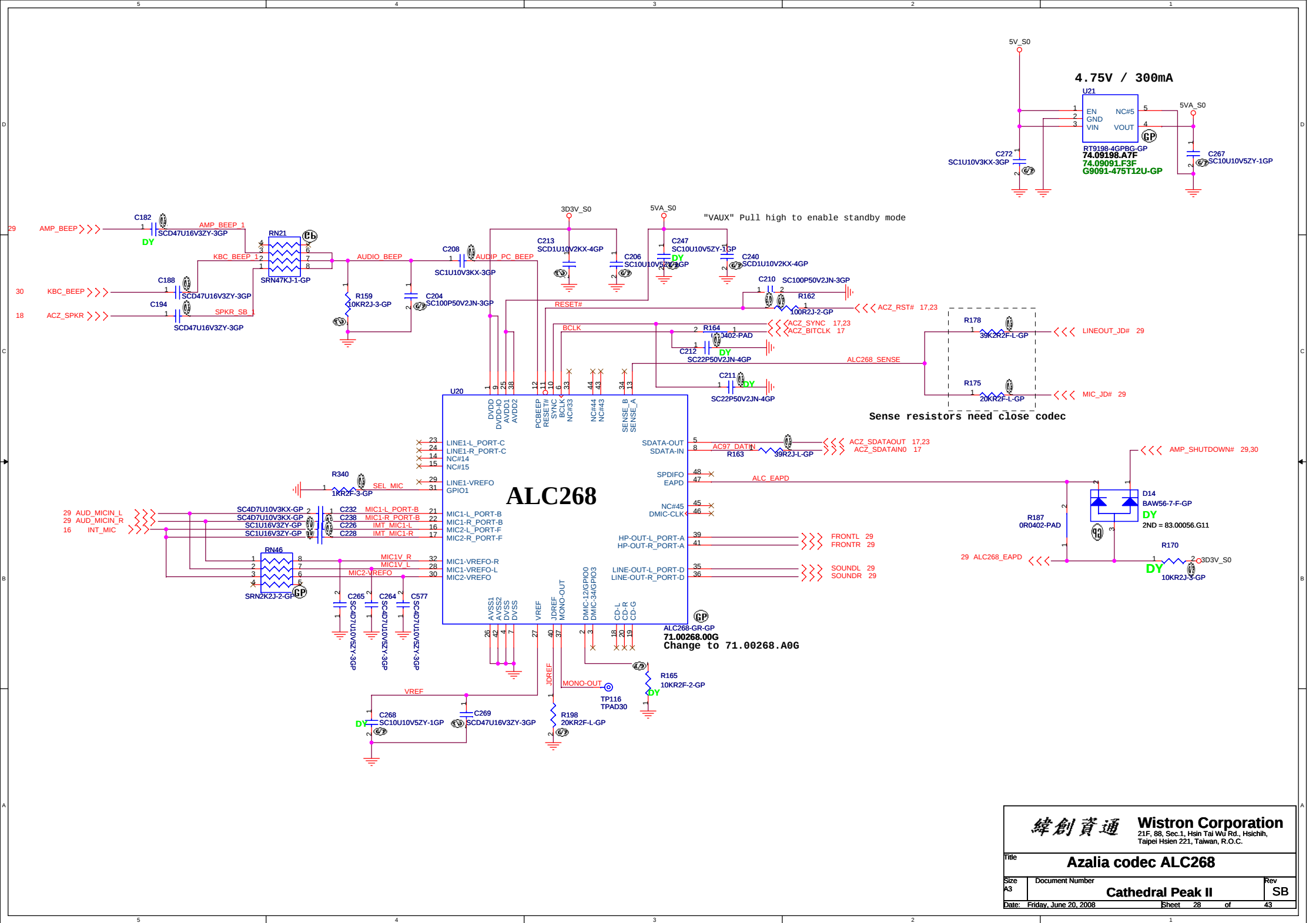


Mini Card Connector(WLAN)

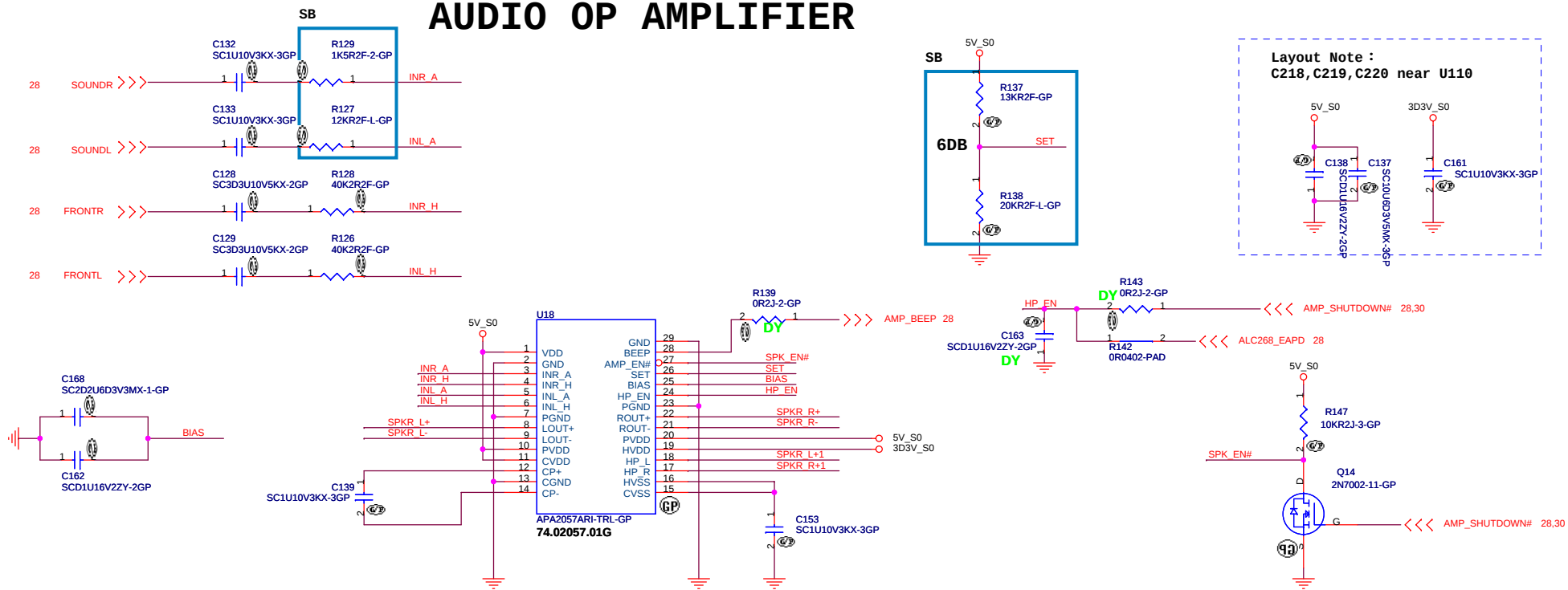


Place near MINIC1

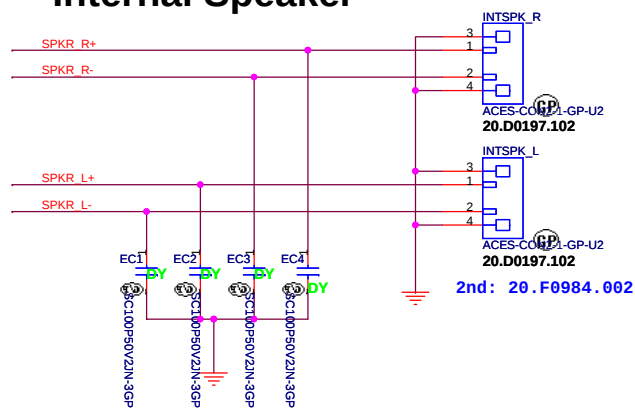




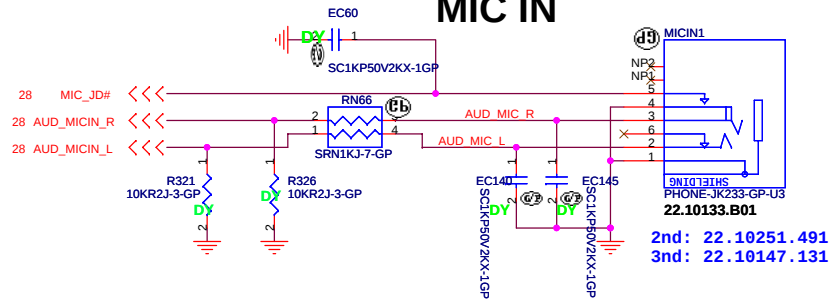
AUDIO OP AMPLIFIER



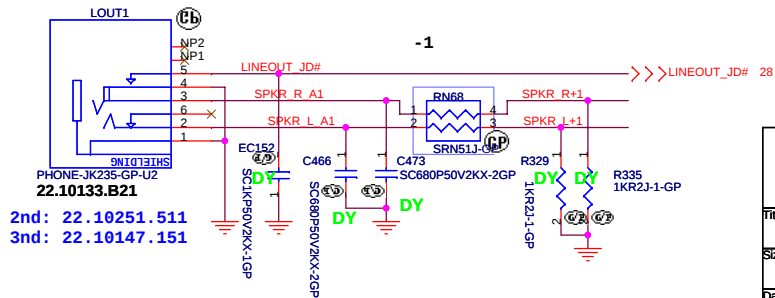
Internal Speaker



MIC IN



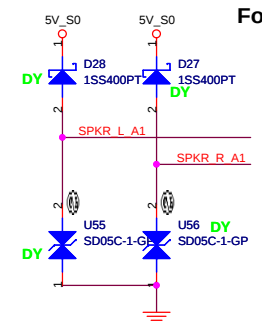
LINE OUT

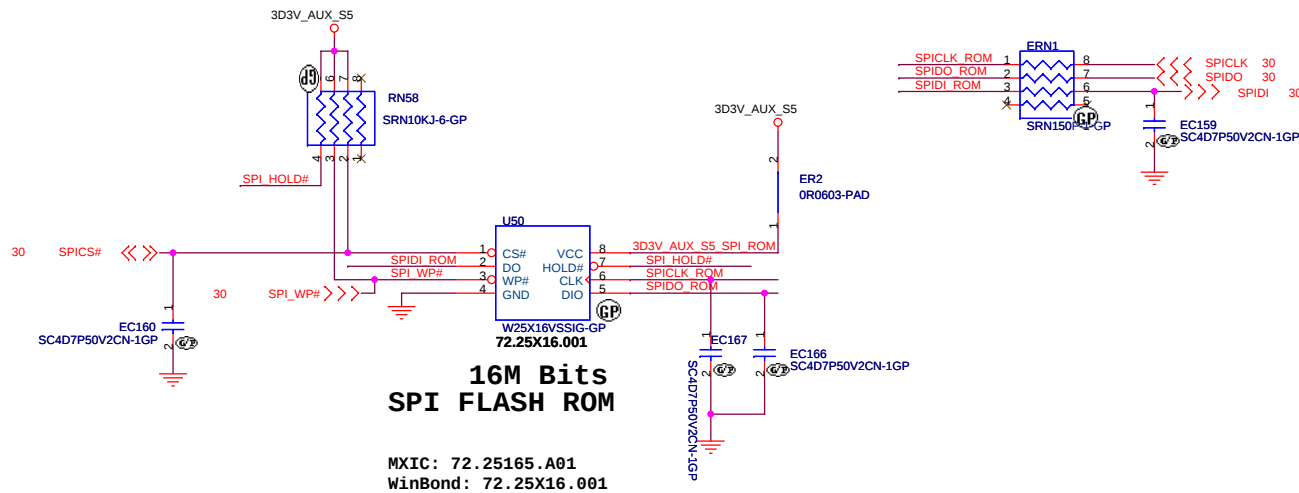


Analog Int. Mic

remove to LED Board

For ESD

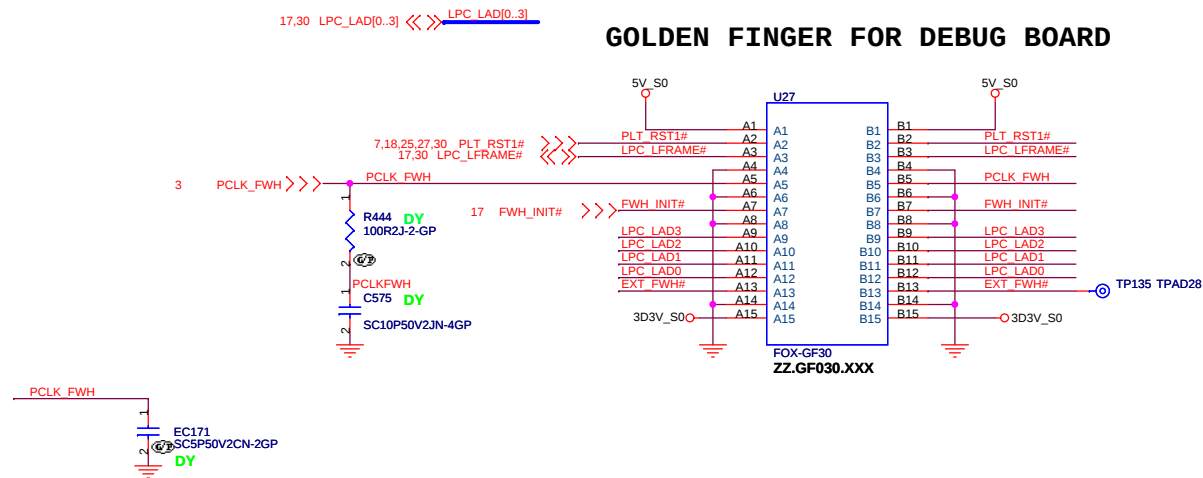


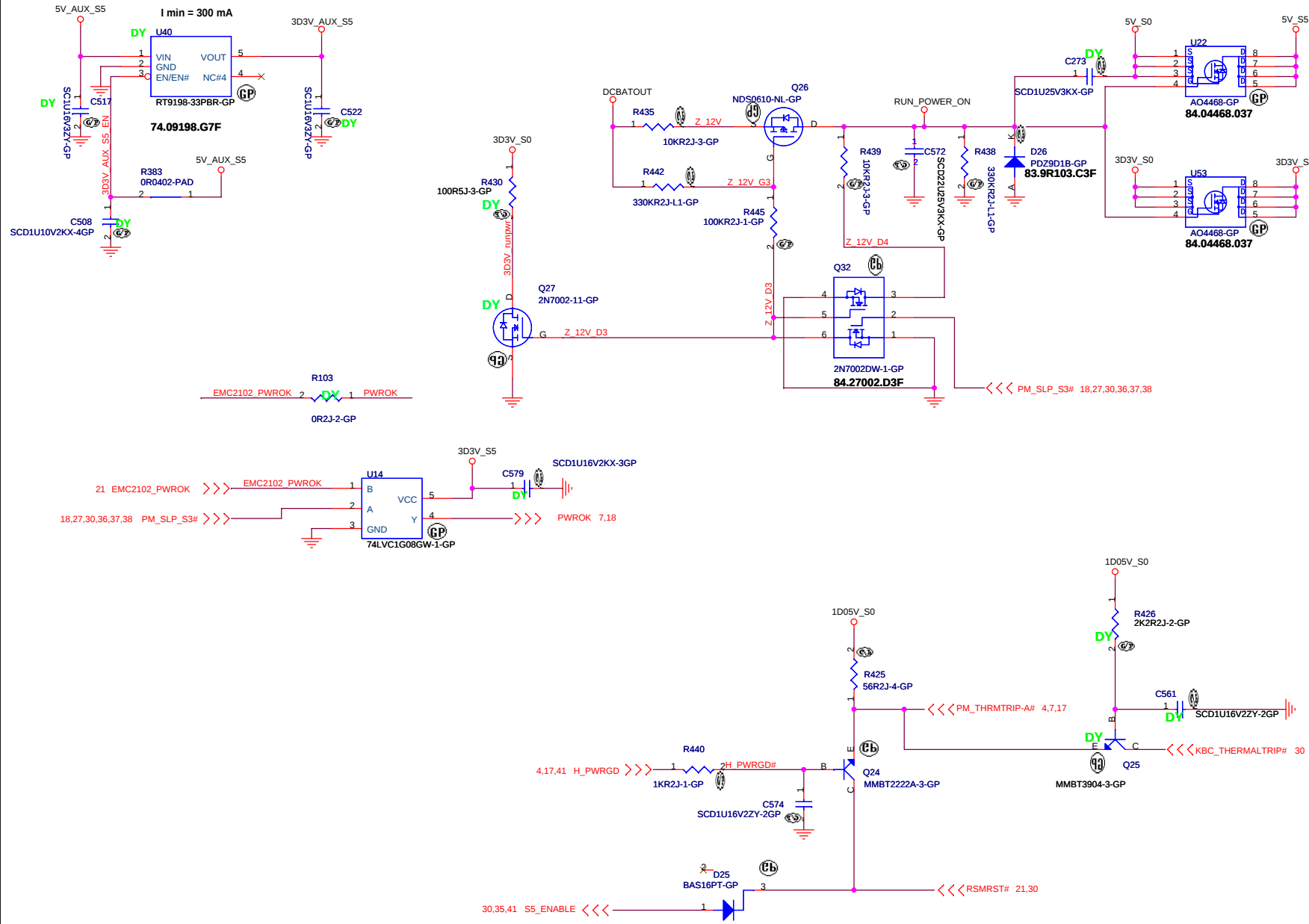


TOP VIEW

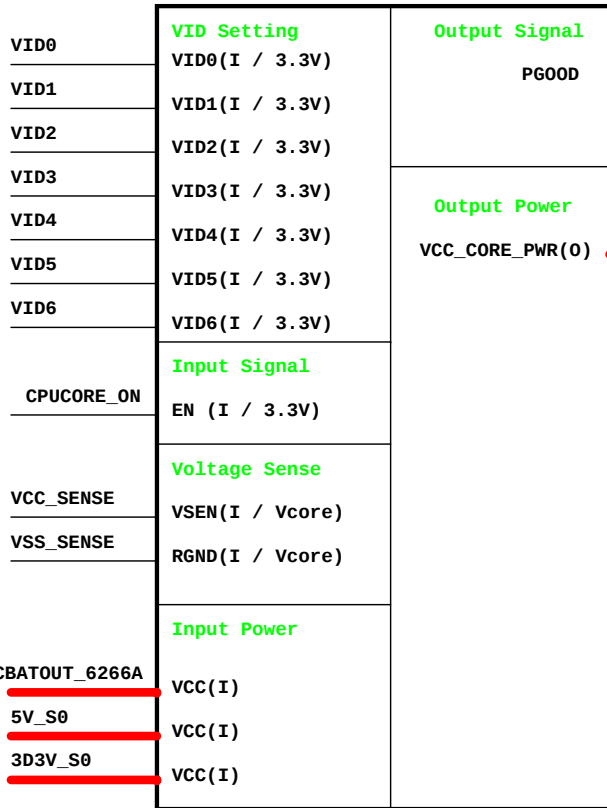
A15	(B1)
A14	(B2)
...	...
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

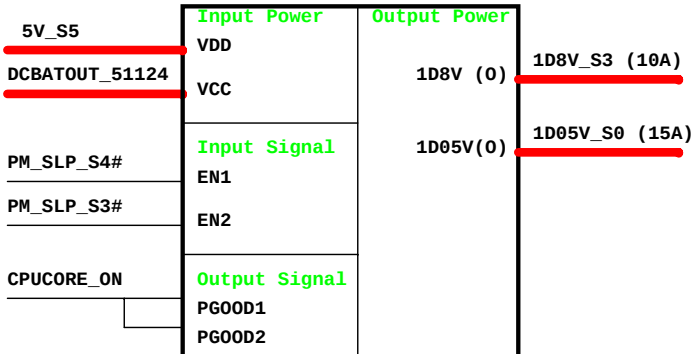




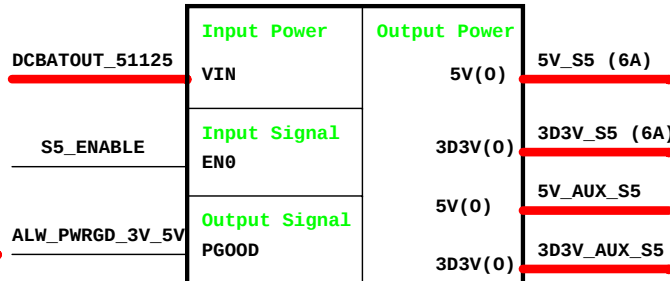
CPU_CORE
ISL6266A



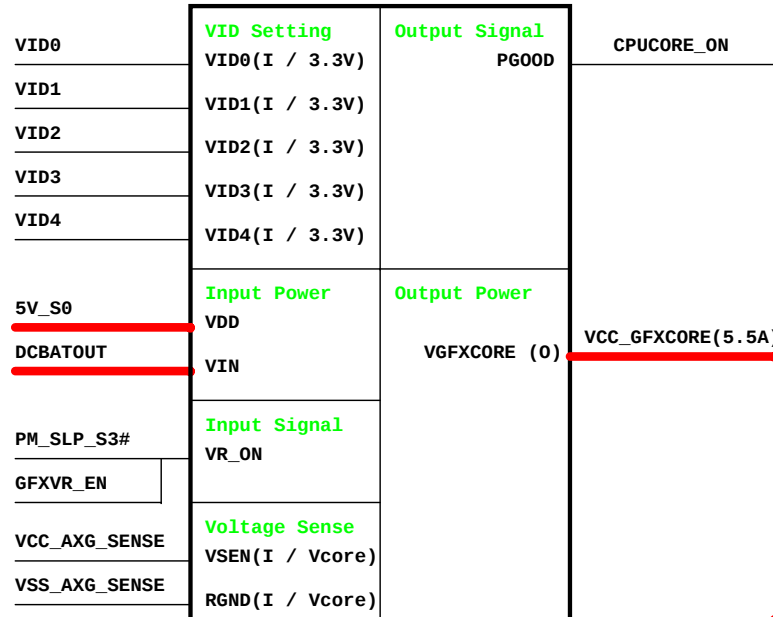
TPS51124
1D8V/1D05V



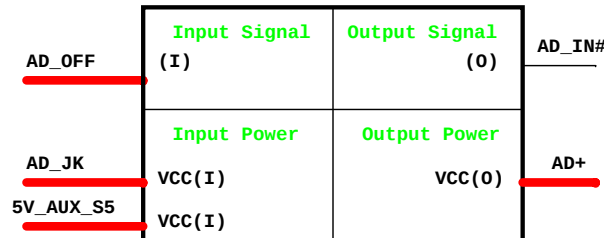
TPS51125
5V/3D3V



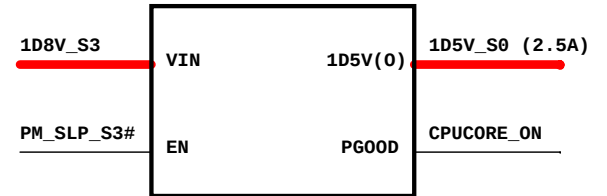
GFX_CORE
ISL6263A



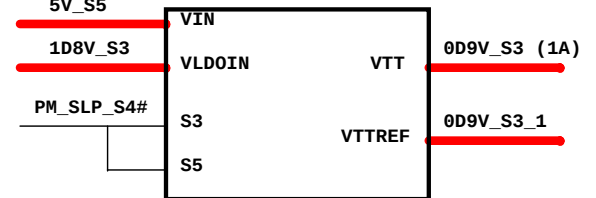
Adapter



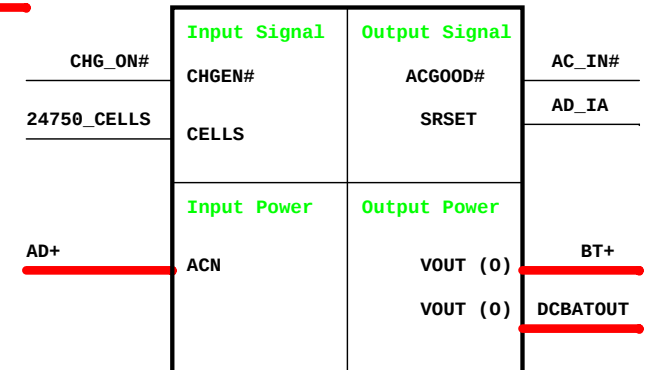
RT9018A
1D5V_S0



RT9026 0D9V_S0



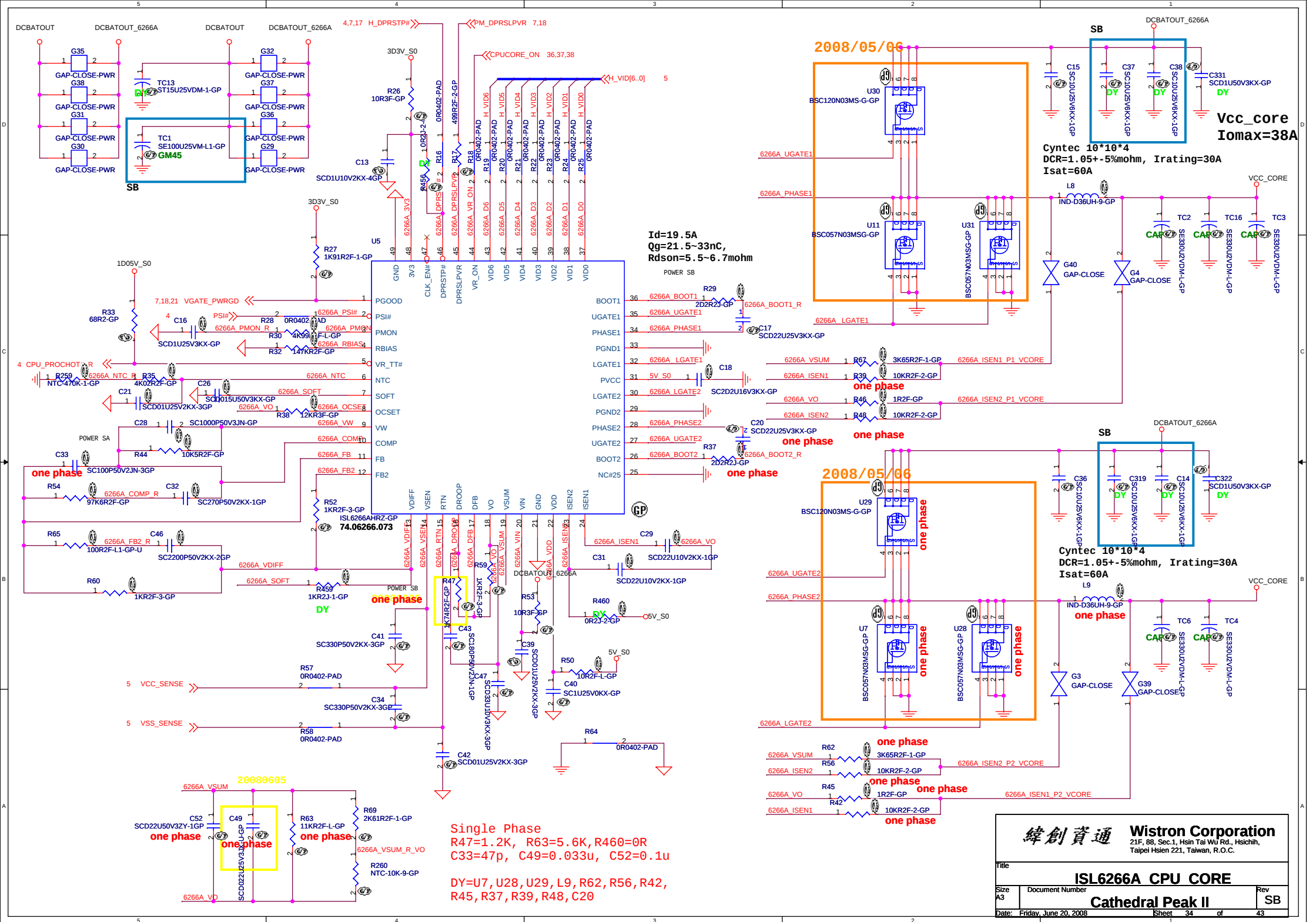
Charger BQ24745

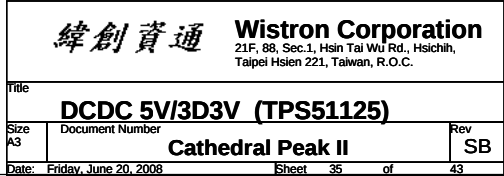


緯創資通

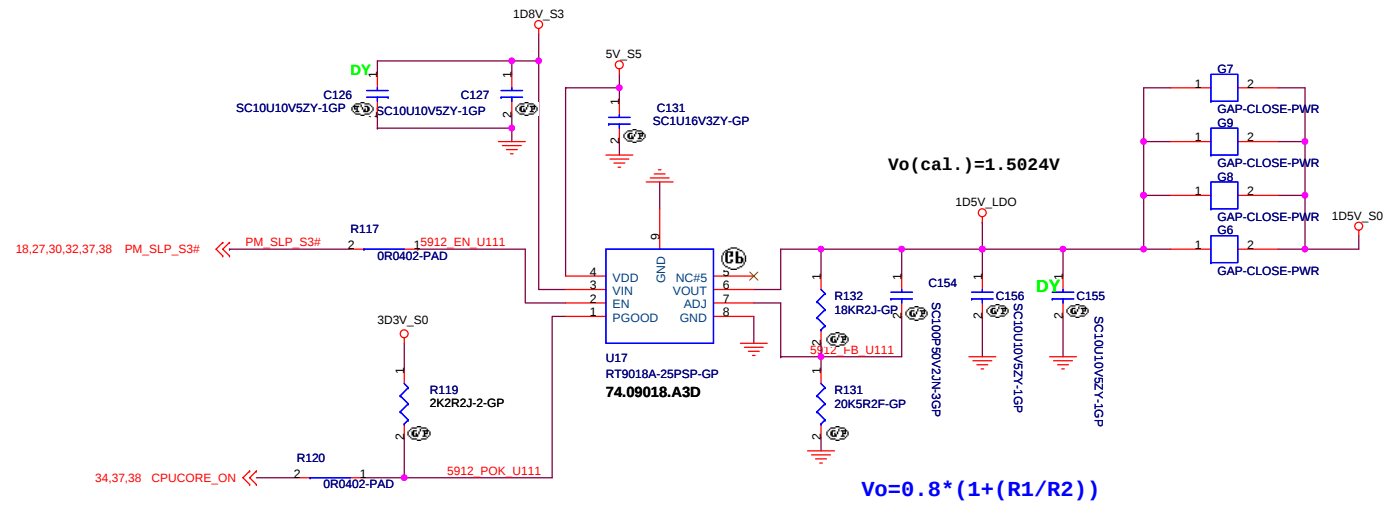
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Title				
Power Sequence Logic				
Size B	Document Number			Rev
	Cathedral Peak II			SB
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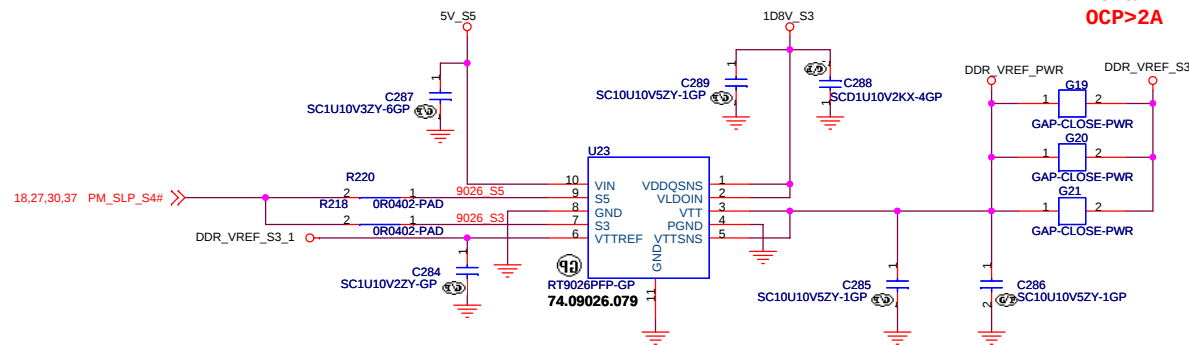




1D5V_S0
Iomax=2.5A



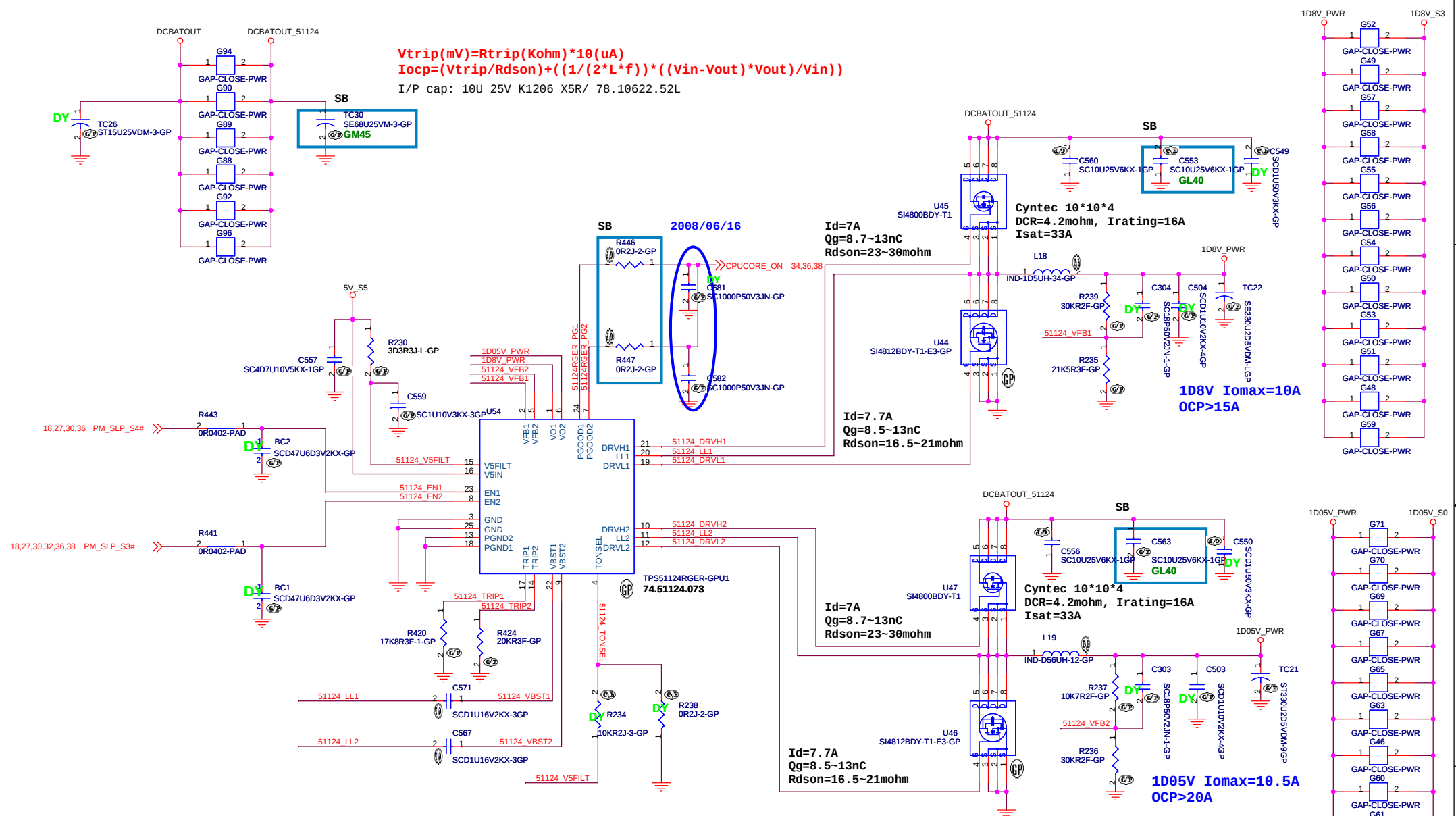
Iomax=1A
OCP>2A



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Title		
1D5V & 0D9V		
Size A3	Document Number	Rev
	Cathedral Peak II	SB
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$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out})/V_{in})$
 I/P cap: 10u 25V K1206 X5R/ 78.10622.52L



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2)/R2$ --> PWM mode
 $V_{out} = 0.764V * (R1+R2)/R2$ --> Skip Mode

緯創資通

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TPS51124 1D8V 1D05V

Size A3

Document Number

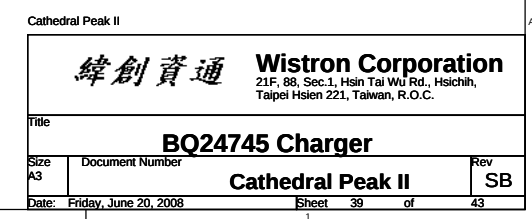
Rev

Cathedral Peak II

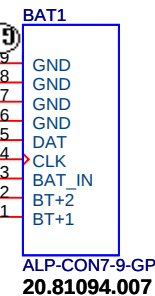
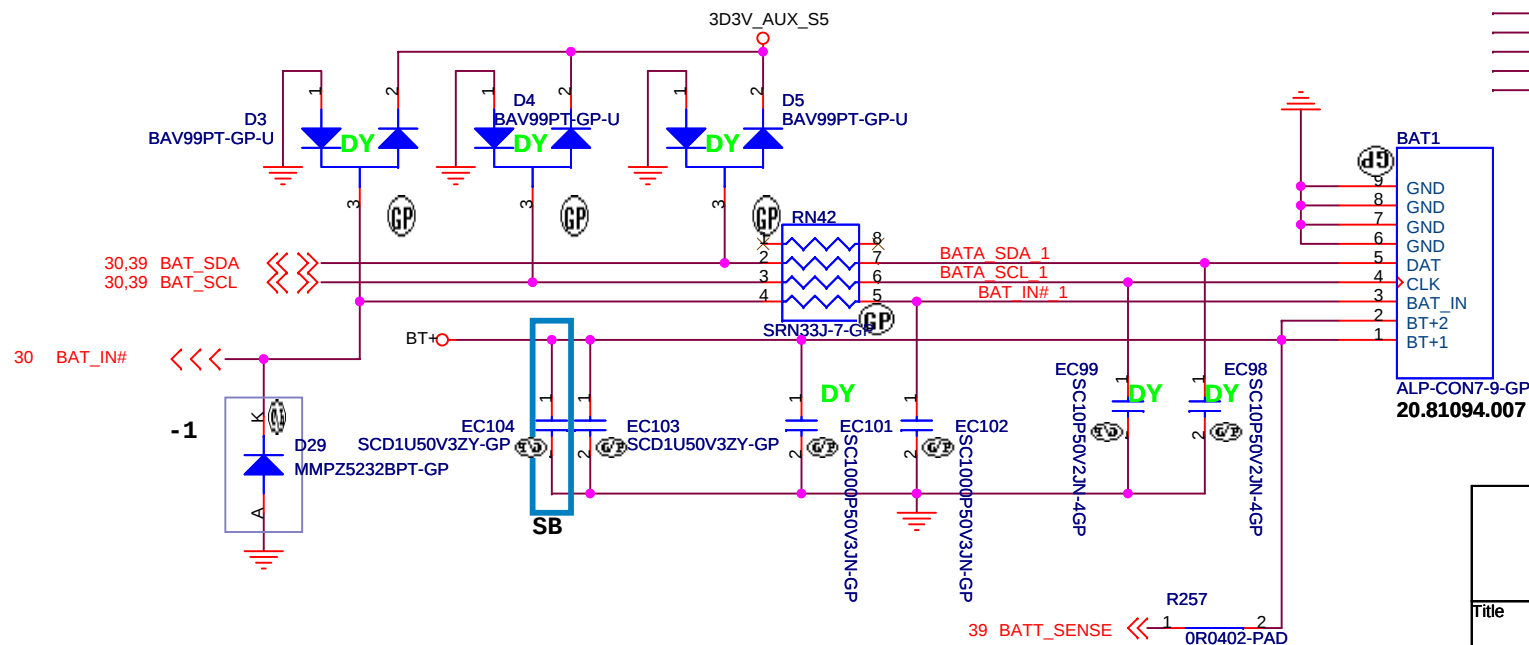
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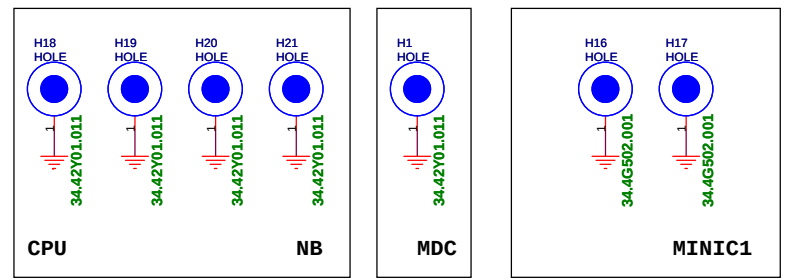
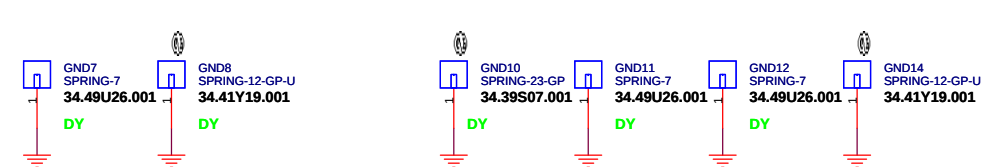
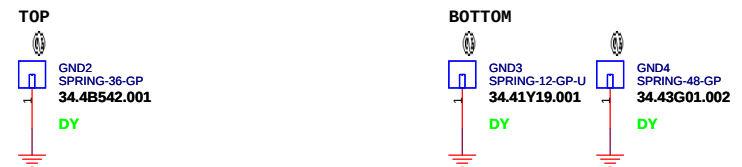
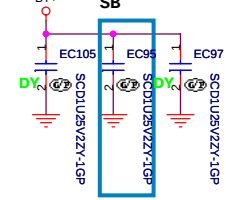
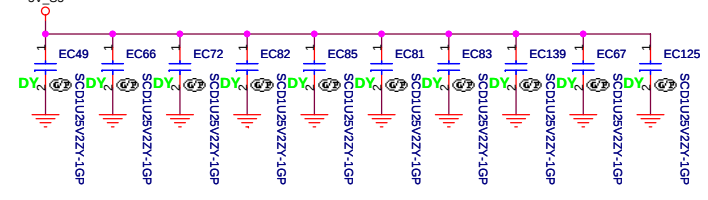
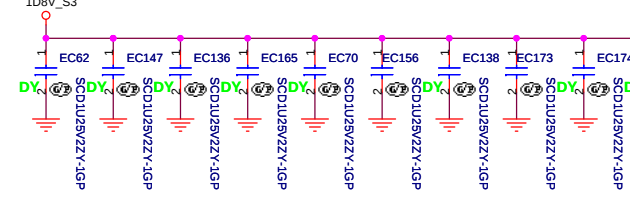
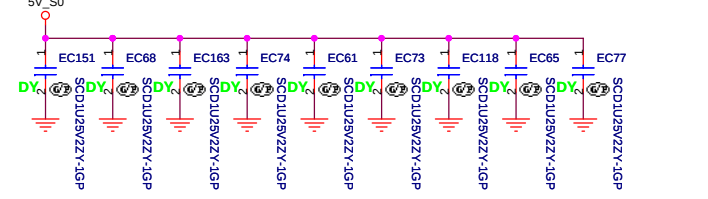
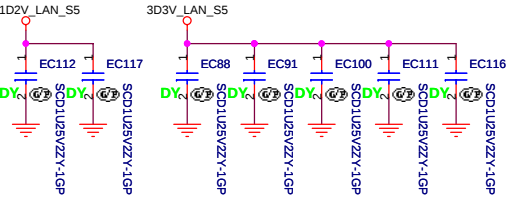
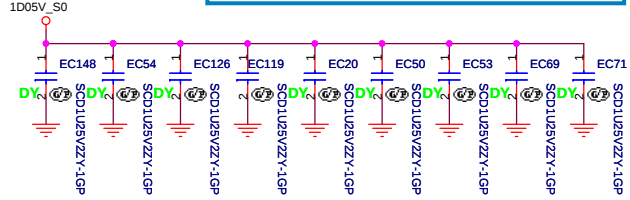
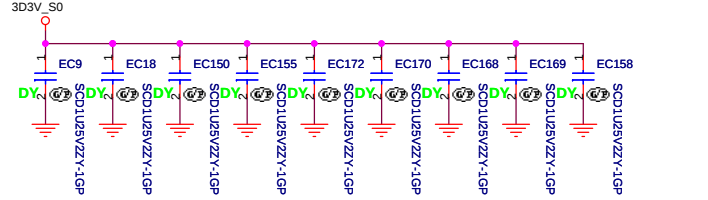
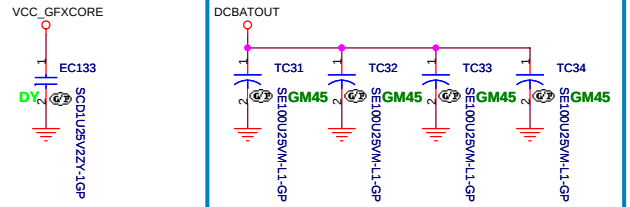
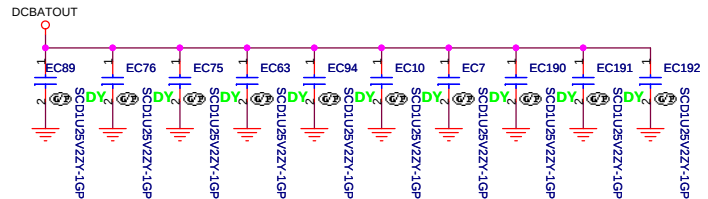
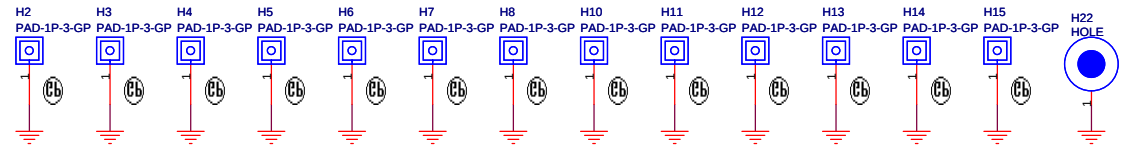
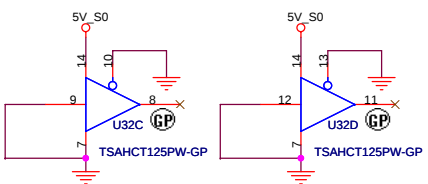
BATTERY CONNECTOR



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SB

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Check test point



Test Point放在Dimm Door打開可量測處

緯創資通

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
EMI/Spring/Boss		
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SA to SB
1.No Power.
change KBC to B0 (71.03310.A0G)
2.XD Card function fail
Cut CARD1 pin27. connect to R400 pin2
3.leakage
GFX power VDD connect to S0
4.Gain=8db.1.83W R137=16K.R138=30K
5.Int MIC voice to small
add VREF C577=4.7U
6.Realtek Audio report
change R327=68 ohm.R333=68 ohm.merge to RN68
7.SIV reset
R140=300,R55=100.C44=100p,R398=0,R369=100.C502=100p,R85=300,R162=100.C210=100p,R392=0,
8.SIV Azalia
DY C542
BITCLK rise and fall time fail RN10 change to R453=22ohm(MDC).R452=0ohm(codec)
9.add MINICard power option for customer ask
R454.R455
10.interfere HDD
C390.C401.C419. change 0603 4.7U
11.power team
R38=12K.R47=2.74K .R361=110K.R221=100K.R237=10.7K .R424=20K.R420=17.8K .R227=10.5K
R48=10K.R29=2.2 .R37=2.2 .R401=3.3 .C49=0.1u.add R456.add C580.D8=83.R0203.08F .
TC11 change to 77.C2271.00L
TC9 change to 77.E9071.001 (power ripple)
add R458=1K.R459=1k.R460
12.Oscillation
C30=15p.C23=15P.C537=27p.C538=22p
13.audio S3.S4 resume bobo sound
R143 DY. R187 0ohm pad
14.AC mode have hight frequency noise
R390 DY.R389 0ohm pad
15.ESD issue
BAT_IN# series 33 ohm
RN42 change to 8p4r
add R457.D27.D28.D29.U55.U56.C578.R457.
16.noise
DY C523.TC25 change to 77.C1561.01L
20.LED brightness
R2.R1.R4.R5.R451.R450.R449.R448=56

EMI
1.EC23 ---EC48.EC134.EC135.EC167.EC121.EC122.EC123.
2.EC89.EC12.EC8.EC119.EC156.EC173.
3.EC174---EC179.
4.GND13.GND14.

Merge
1.R313.R314.R315.R319.R320.R149. change to RN59
2.RN6.RN46. change to RN6
3.R341.R343.R344 change to RN46
4.R385 change to 100K merge R382 to RN56
5.RN53.RN56. change to RN53
6.Q20.Q21 change to Q21. Q21.Q23 change to Q21.
7.R367.R368 change to RN60
8.Q16.Q17 change to Q16
9.R262.R264.R268.R277 change to RN61
10.R205.R204.R206 change to RN62
11.RN33.R215 change to RN33
12.R209.R210.R348 change to RN63
13.R280=10K.merge R269 to RN64
14.R109.R112.R111.R290 change to RN65
15.R325.R323 change to RN66
16.R304.R307 change to RN67
17.U14 change to 73.01608.L04 .add C579
18.R51.R399 vchange to RN69.

0 Ohm change to PAD
R427.R403.R415.R413.R411.R408.R404.R146.R197.R157.R153.R353.R352.R358.R357.R310.R196.R346.R342.R351.
R191.R203.L14.R212.R350.R179.R217.R6.R7.R242.R294.R278.R279.R292.R293.R232.R233.R410.R393.
R416.R250.R251.R248.R249.R246.R247.R244.R245.R129.R127.R376.ER2.R383.R28.R16.R19.R20.R21.
R22.R23.R24.R25.R57.R58.R365.R164.

05/05

Page16: merge LAUNCHCN1 LEDCN1 to LAUNCHCN1 15pins

Page15: change CRT1 from 20.20717.015 to 20.20378.015

Page26: change RJ1 from 22.10277.011 to 22.10245.E91

Page23: change BLUE1 from 20.D0197.004 to 20.F0984.004

Page24: change CARD1 from 20.I0081.001 to 20.I0067.001

Page21: change FAN1 from 20.F0714.003 to 20.F1000.003

Page27: change MINIC1 from 20.F1049.052 to 62.10043.331

Page30: change TPAD1 from 20.K0286.012 to 20.K0174.012

Page34: change U29 U30 from 84.07686.037 to 84.12003.A37 and change U7 U11 U28 U31 from 84.04634.037 to 84.57N03.A37

Page16: delete LED1 LED2 R1 R2 R4 R5

05/07

Page17: change RTC1 from 62.70001.011 to 20.F0700.003

Page41: delete EC51

Page10: delete C159

Page25: change U13 from 72.24256.R01 to 72.24C08.J01

05/08

Page30: change KB1 from 20.K0127.026 to 20.K0204.026

Page26: delete RN36 RN37 RN38 RN39

Page23: change TC28 from 80.15715.34L to 77.C1071.081

Page26: change TC15 from 80.15715.34L to 80.15715.12L

Page23: delete R244 R245 R246 R247 R248 R249 R250 R251

Page24: change CARD1 from 20.0067.001 to 20.I0079.001

05/09

Page41: delete GND13

05/12

Page24: add EC127 EC128 EC185 EC186

Page35: change TC27 from 77.C1561.01L to 77.C1561.03L

Page40: change BAT1 from 20.80697.007 to 20.80906.007

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

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05/013
Page16: change pin1 pin2 of LED6 from 3D3V_S5 to 3D3V_AUX_S5

05/014
Page17: add EC187 EC188

Page16: add EC189 TP189~TP195

Page30: change TPAD1 from 20.K0174.012 to 20.K0228.012

Page41: add EC190~EC195

05/015
Page17: change U15 pin13 pin14 from pull high 3D3V_S0 to VGATE_PWRGD

Page17: change Q11 G from 3D3V_S0 to VGATE_PWRGD

Page40: change D1 from 83.P4SSM.BAM to 83.P6SBM.AAG

SB
05/015
Page30: change KBC_GPI00C from pull-high 3D3V_AUX_S5 with 10K to pull-low GND with 1K

06/06
Page3: change C176 C177 from 78.27034.1FL (27p) to 78.33034.1FL (33p)

Page22: delete D15

Page29: change R127 R129 from 0ohm pad to 12K 1K5 and change R137 R138 from 16K 30K to 13K 20K

Page34: change TC1 from 77.C1561.01L (15u) to 79.10712.L02 (100u) and C14 C37 C38 C319 dummy

Page35: change TC25 from 77.C1561.01L (15u) to 79.68612.30L (68u) and change C292 to dummy

Page37: add TC30 79.68612.30L (68u) and change C553 C563 to dummy

Page38: change C536 to dummy and change TC24 from 77.C1561.01L (15u) to 79.68612.30L (68u)

Page39: change C61 to dummy

Page41: add TC31 TC32 TC33 TC34 and delete GND9

06/09
Page16: add LED3 R458 R465

06/11
Page30: change R379 from 10K to 1K

06/13
Page3: add EC59 DY

06/13
Page37: change R446 R447 from 0ohm pad to 0ohm resistor

Page26: change XF1 from 68.69241.301 to 68.89240.30A

06/17
Page39: C320 mount

Page40: EC104 mount

Page41: EC95 mount

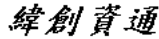
Page39: change R11 from 10K to 49K9

Page34: change C49 from 47nF to 22nF and change R47 from 2.74K to 1.74K

Page37: add C581 C582

Page41: delete GND6

06/20
Page25: change C30 from 15p to 12p

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
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