Colossus 15/17
DIS_OPT Schematic
IVY Bridge (rPGA989)
Intel PCH (Panther Point)

REV:-1
2012-01-05.

DY:No stuff
DIS_OPT:DISCRTE OPTIMUS installed
DY_35W:No stuff on 35W CPU
DY_45W:No stuff on 45W CPU
CR_Balen17:Stuff for 17"
CR_Goya:Stuff for 15"

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page

Size: A4 | Document Number: Colossus | Rev: 1

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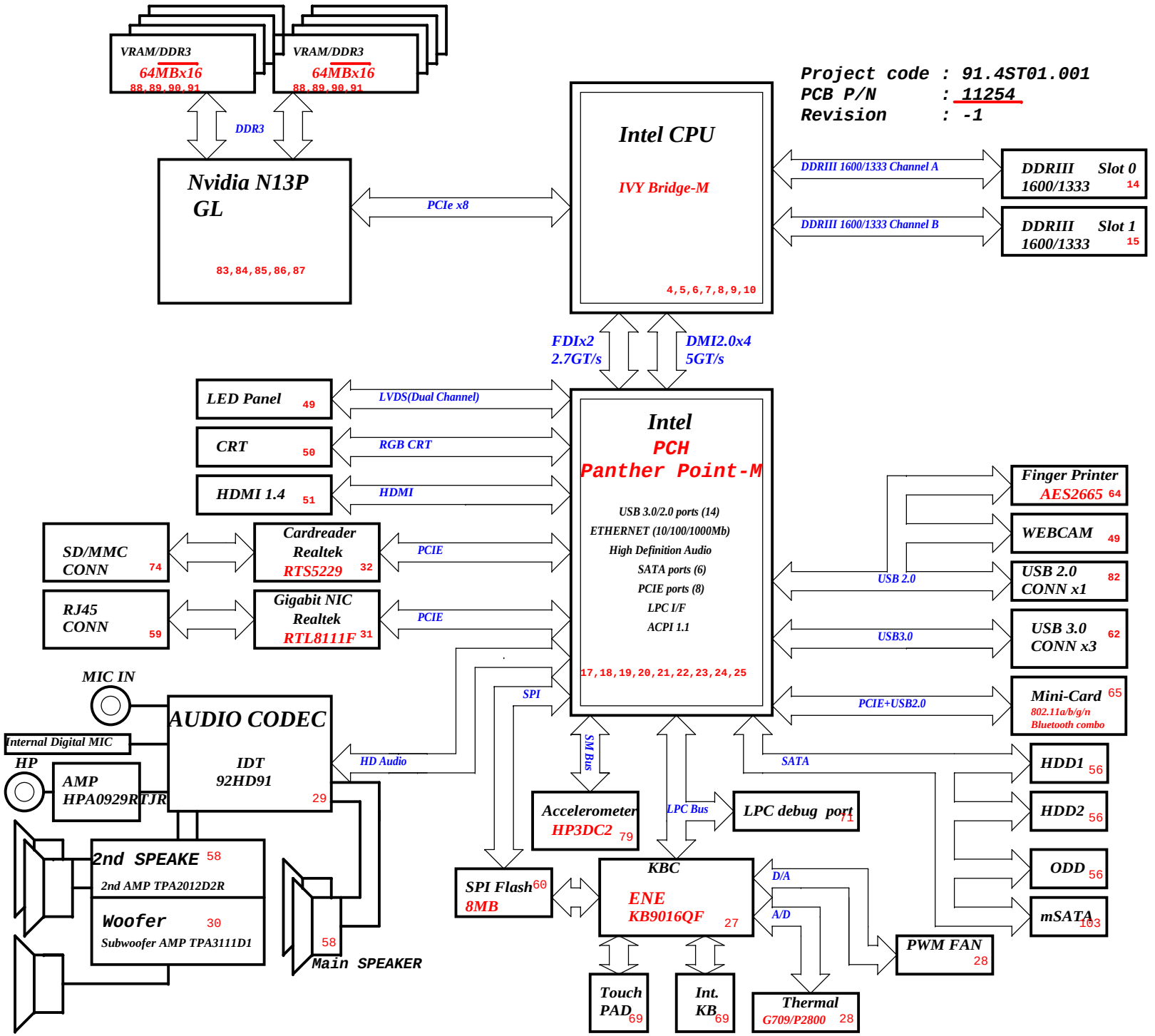
COLOSSUS Block Diagram



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
5V_S5	VCCSA=0D85V_S0

CPU DC/DC VT1323 42~44	
INPUTS	OUTPUTS
DCBATOUT(5V_S5)	VCC_CORE

SYSTEM DC/DC SN1003055RUWR 45	
INPUTS	OUTPUTS
5V_S5/3D3V_S5	1D05V_S0

SYSTEM DC/DC RT8223M_5V/3D3V 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207MZ 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC VT1323 42~44	
INPUTS	OUTPUTS
DCBATOUT(5V_S5)	VCC_GFXCORE

VGA NCP3218G 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24738 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC VT385FCX 93	
INPUTS	OUTPUTS
3D3V_S0 1D5V_S0 1D5V_S3	3D3V_VGA_S0 1D5V_VGA_S0 1V05_VGA_S0

Switches 36	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER (DISCRETE)

L1:Top	L5:Vcc
L2:GND	L6:Signa
L3:Signal	L7:GND
L4:Signal	L8::Bottom

<Core Design>

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Title: Block Diagram

Size	Document Number	Rev
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PCH Strapping

Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_S0 VCCSA_0D85V 0D75V_S0 VCC_CORE VCC_GFXCORE 3D3V_VGA_S0 1D5V_VGA_S0 1D05V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 3.3V 1D5V 1D05V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

PCIe Routing

LANE1	N/A
LANE2	17"Card Reader
LANE3	15"Card Reader
LANE4	Mini Card1(WLAN)
LANE5	N/A
LANE6	Intel GBE LAN / LAN
LANE7	N/A
LANE8	N/A

USB2.0 Table

Pair	Device
0	USB 3.0 I/O CONN. 1
1	N/A
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN.
10	Camera
11	FREE
12	FREE
13	FREE

USB3.0 Table

USB	
Pair	Device
1	I/O CONN. 1
2	FREE
3	I/O CONN. 2
4	I/O CONN. 3

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	HDD2
3	N/A
4	ODD
5	N/A

<Core Design>

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Title: Table of Content

Size	Document Number	Rev
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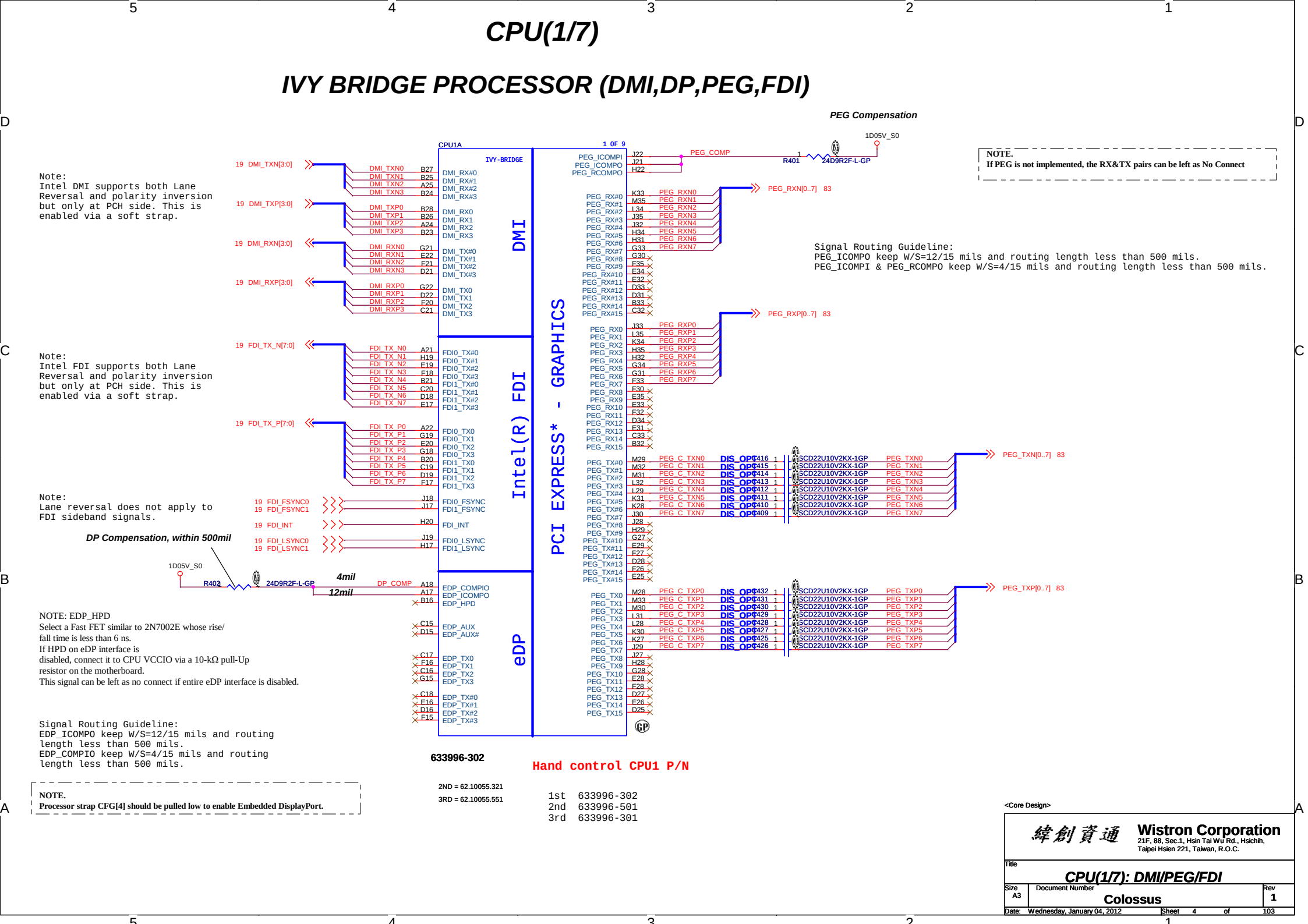
CPU(1/7)

IVY BRIDGE PROCESSOR (DMI,DP,PEG,FDI)



633996-302

2ND = 62.10055.321

3RD = 62.10055.551

Hand control CPU1 P/N

1st 633996-302
2nd 633996-501
3rd 633996-301

<Core Design>

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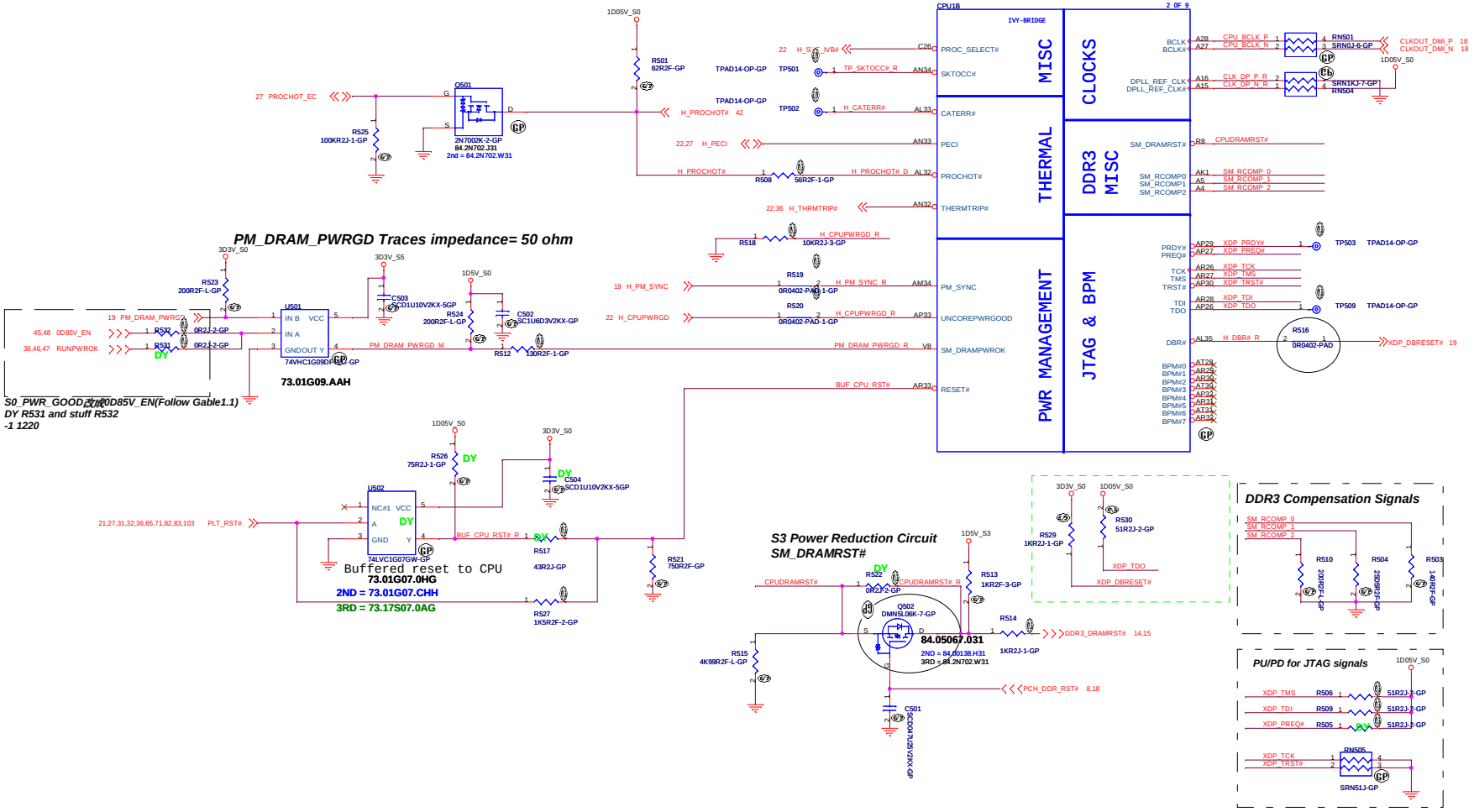
Title: CPU(1/7): DMI/PEG/FDI

Size: A3 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 4 of 103

CPU(2/7)

IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



<Core Design>

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Title: CPU(2/7): CLK/MISC/JTAG

Size: A2 | Document Number: Colossus | Rev: 1

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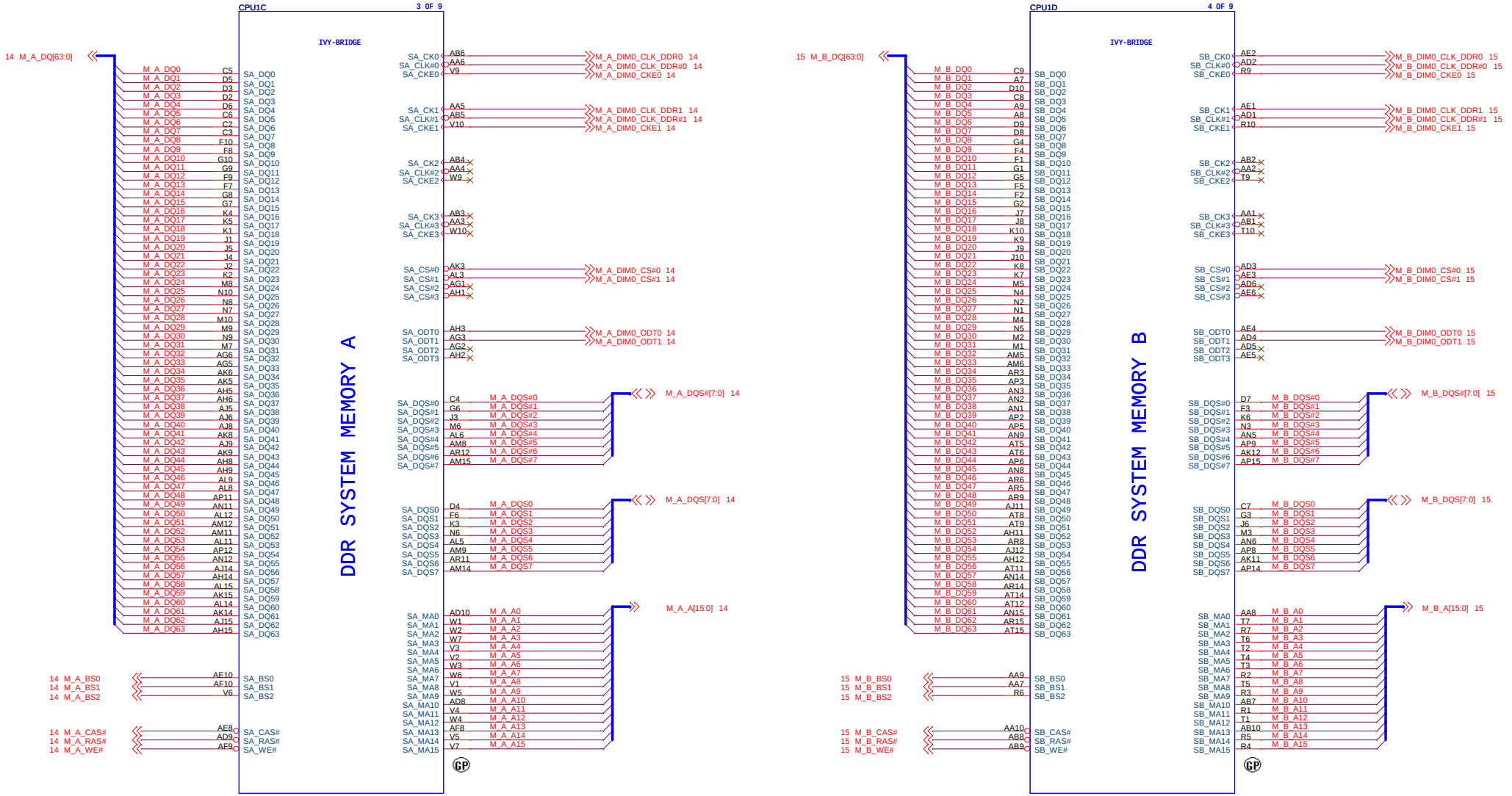
CPU(3/7)

IVY BRIDGE PROCESSOR (DDR3)



<Core Design>

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Title	***CPU(3/7): DDR3***	
Size: Custom	Document Number: **Colossus**	Rev: 1
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CPU(4/7)

IVY BRIDGE PROCESSOR (POWER)

POWER

CPU1F

6 OF 9

IVY-BRIDGE

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

Place Bottom

Place Top

PROCESSOR CORE POWER

53A

VCC_CORE

C713 C722 C727 C736 C714 — SC22U6D3V5MX-2GP / SC10U6D3V5KX-2GP

C735 C721 C726 C728 C723 — SC22U6D3V5MX-2GP / SC10U6D3V5KX-2GP

C742 C701 C741 C703 C709 — SC22U6D3V5MX-2GP / SC10U6D3V5KX-2GP

C738 C702 C706 C707 C708 — SC22U6D3V5MX-2GP (C708: DY)

C740 C739 C704 C712 C710 C711 — SC22U6D3V5MX-2GP (C739, C704: DY)

Power 78.22610.51L

C746 C745 C744 C743 C752 C751 — SC22U6D3V5MX-2GP / SC10U6D3V5KX-1GP (C746, C744, C743: DY)

C748 C749 C750 C747 — SC22U6D3V5MX-2GP / SC10U6D3V5KX-1GP (C748, C749, C747: DY)

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

PROCESSOR UNCORE POWER

8.5A

1D05V_S0

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C729 C730 C731 C732 C715 C716 C717 C718 C733 C734 C719 C720 — SC22U6D3V5MX-2GP / SC10U6D3V5KX-2GP / SC10U6D3V5KX-1GP

C725 C737 C705 C724 — SC22U6D3V5MX-2GP (DY)

SVID

1D05V_S0

R709 75R2F-2-GP

VIDALERT# AJ29 — VIDALERT# — R705 43R2F-2-GP

VIDSCLK AJ30

VIDSOUT AJ28

VR_SVID_ALERT# 42

H_CPU_SVIDCLK 42

H_CPU_SVIDDAT 42

R703 130R2F-1-GP — 1D05V_S0

SENSE LINES

VCC_CORE

R706 100R2F-L1-GP-U

R704 100R2F-L1-GP-U

VCC_SENSE AJ35 — VCC_SENSE_R — R702 0R0402-PAD

VSS_SENSE AJ34 — VSS_SENSE_R — R701 0R0402-PAD

VCCSENSE 42

VSSSENSE 42

VCCIO_SENSE B10 — VTT_SENSE 45

VSS_SENSE_VCCIO A10 — VSSP_SENSE 45

R707 10R2F-L-GP — R708 10R2F-L-GP — 1D05V_S0

Differential Sense feedback

<Core Design>

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Title: CPU(4/7): PWR

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CPU(5/7)
IVY BRIDGE PROCESSOR (GRAPHICS POWER)

M3 - Processor Generated SO-DIMM VREF_DQ

33A

VCC_GFXCORE

470U*2 22U*6

Under Socket and Closed to CPU

C820 C821 C822 C823 C824 C825 — SC22U6D3V5MX-2GP

VCC_GFXCORE

22U*6

Closed to CPU Socket

C826 C827 C828 C829 C830 C831 — SC22U6D3V5MX-2GP

Power 78.22610_51L

C837 C836 C835 C834 C833 — SC22U6D3V5MX-2GP; C832 DY — SC22U6D3V5MX-2GP

1.5A

1D8V_S0

C819 C816 C817 C818 — SC10U6D3V5KX-1GP / SC1U10V2KX-1GP

CPU1G — IVY-BRIDGE — 7 OF 9

POWER

SENSE LINES

VAXG_SENSE AK35 → VCC_AXG_SENSE 42
VSSAXG_SENSE AK34 → VSS_AXG_SENSE 42

VREF

SM_VREF AL1 ← +V_SM_VREF_CNT

CAD Note: +V_SM_VREF should have 10 mil trace width

B4:VREF_DQ CHA
D1:VREF_DQ CHB

SA_DIMM_VREFDQ B4 ← DDR_VREF_S3_B4
SB_DIMM_VREFDQ D1 ← DDR_VREF_S3_D1

R815 1KR2F-3-GP DY
R816 1KR2F-3-GP DY

C801 DY SC1U16V2ZY-2GP
C802 DY SC2D2U10V2ZY-1GP

DDR3 -1.5V RAILS

12~16A

1D5V_S0

330U*1 10U*6

VDDQ1 AE7
VDDQ2 AE4
VDDQ3 AE1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

C803 C804 — SC4D7U6D3V3KX-1GP
C805 C806 C807 — SC10U6D3V5KX-1GP
C808 — SC10U10V5KX-2GP
TC801 — ST330U2D5VDM-9GP

77.23371.13L
2nd = 79.33719.L01

SA RAIL

6A

0D85V_S0

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

C813 C814 C815 — SC10U6D3V5KX-1GP

0D85V_S0 — R801 DY 100R2J-2-GP

VCCSA_SENSE H23 → VCCUSA_SENSE
VCCUSA_SENSE → VCCUSA_SENSE 48

1.8V RAIL

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

MISC

VCCSA_VID0 C22
VCCSA_VID1 C24
H_FC_C22 → H_FC_C22 48
VCCSA_SEL → VCCSA_SEL 48

VCCIO_SEL A19 ← H_VCCP_SEL

RN801 SRN1KJ-11-GP-U

SNB: No Connect
IVB: VSS

R817 0R2J-2-GP DY
H_SNB_IVB#_PWRCTRL → TP801 TPAD14-OP-GP
R818 0R2J-2-GP DY

H_VCCP_SEL	Voltage
1	1.05V
0	1.0V

DDR_VREF_S3

R808 0R2J-2-GP DY
R809 0R2J-2-GP DY

14 M_VREF_DQ_DIMM0 → R808
15 M_VREF_DQ_DIMM1 → R809

84.05067.031
2ND = 84.00138.H31
3RD = 84.2N702.W31
Q802 DMN5L06K-7-GP
R810 0R2J-2-GP DY

PCH_DDR_RST# → Q802 G
0R2J-2-GP R812 M_VREF_DQ_DMM0_R
0R2J-2-GP R813 M_VREF_DQ_DMM1_R

M_VREF_DQ_DMM0_R → DDR_VREF_S3_B4
M_VREF_DQ_DMM1_R → DDR_VREF_S3_D1

3RD = 84.2N702.W31
2ND = 84.00138.H31
84.05067.031
Q803 DMN5L06K-7-GP
R814 0R2J-2-GP DY

5,18 PCH_DDR_RST# → Q803 G

-1 1221

S3 Power Reduction Circuit Processor VREF_DQ Implementation

DDR_VREF_S3

R807 0R2J-2-GP
R811 DY 0R2J-2-GP

14 M_VREF_DQ_DIMM0 → R805 DY 0R2J-2-GP → +V_SM_VREF

Q801 DMN5L06K-7-GP
84.05067.031
2ND = 84.00138.H31
3RD = 84.2N702.W31

+V_SM_VREF_CNT
R803 100KR2J-1-GP

5,18 PCH_DDR_RST# → R802 DY 0R2J-2-GP

19,27,36,46,47,92 PM_SLP_S3#

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Title: CPU(5/7): GFX/PWR

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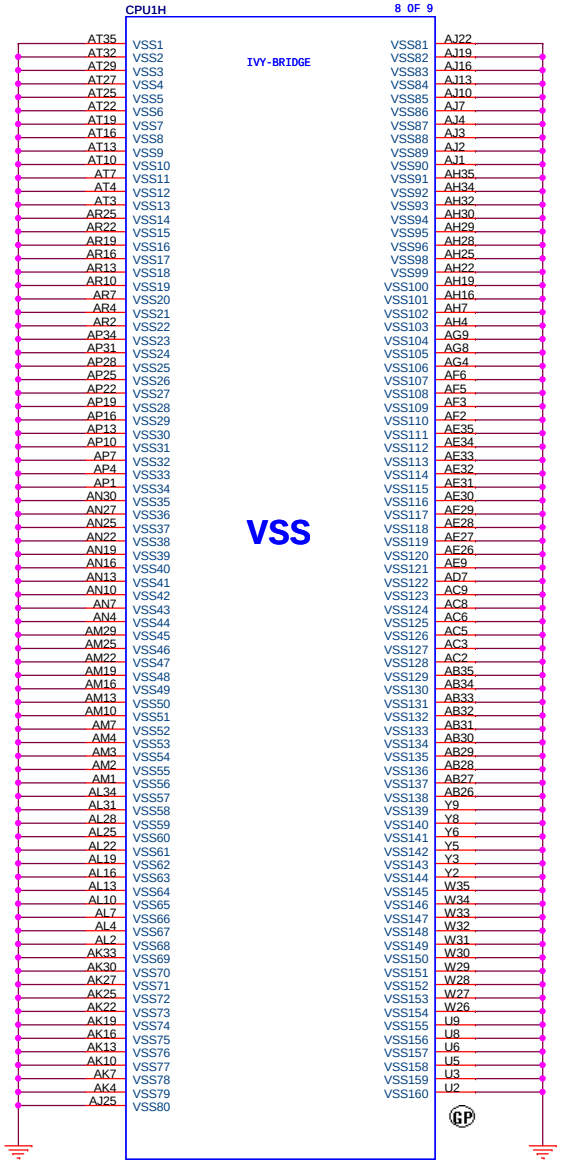
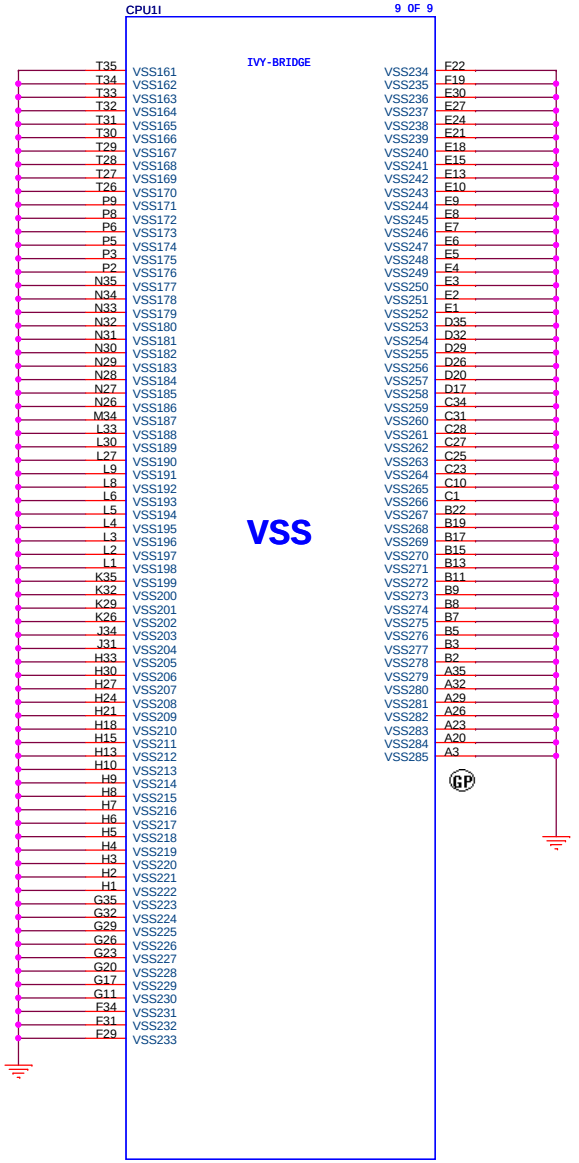
CPU(6/7)

IVY BRIDGE PROCESSOR (GND)





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Title: **CPU (6/7):GND**

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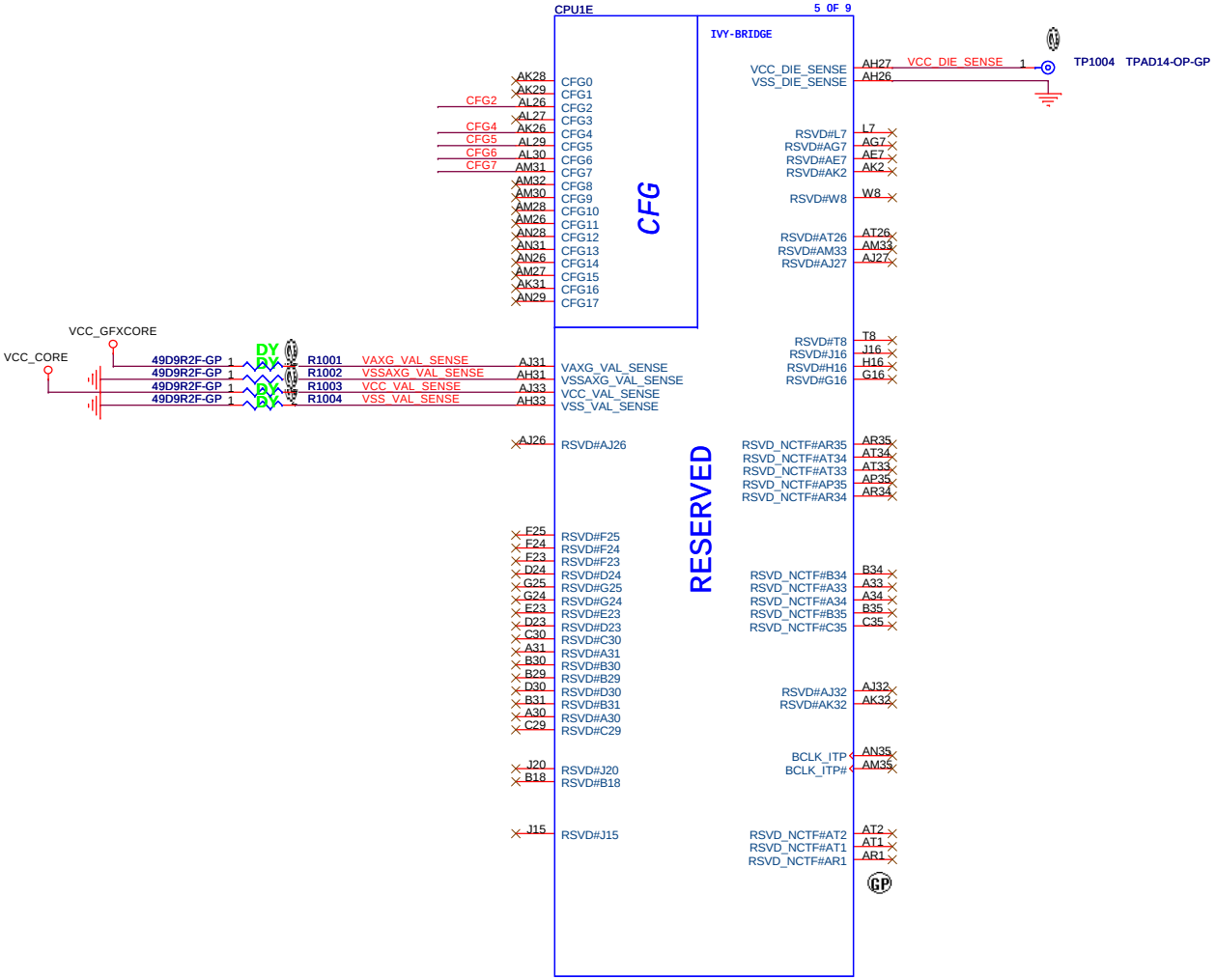
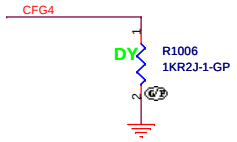
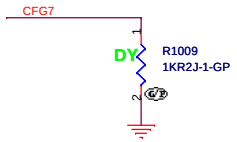
CPU(7/7)

IVY BRIDGE PROCESSOR (RESERVED)

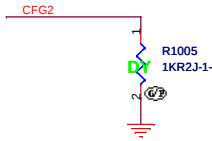




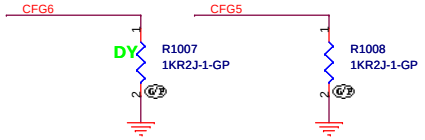
Display Port Presence Strap	0:Enable eDP
CFG4	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



PEG Static Lane Reversal	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(7/7): CFG/RSVD/DDR3_VRE**

Size	Document Number	Rev
A3	Colossus	1

Date: Tuesday, December 27, 2011 Sheet 10 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU_XDP*		
Size: A3	Document Number: Colossus	Rev: 1
Date: Monday, December 26, 2011	Sheet 11 of 103	

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 12 of 103

<Core Design>

緯創資通 **Wistron Corporation**

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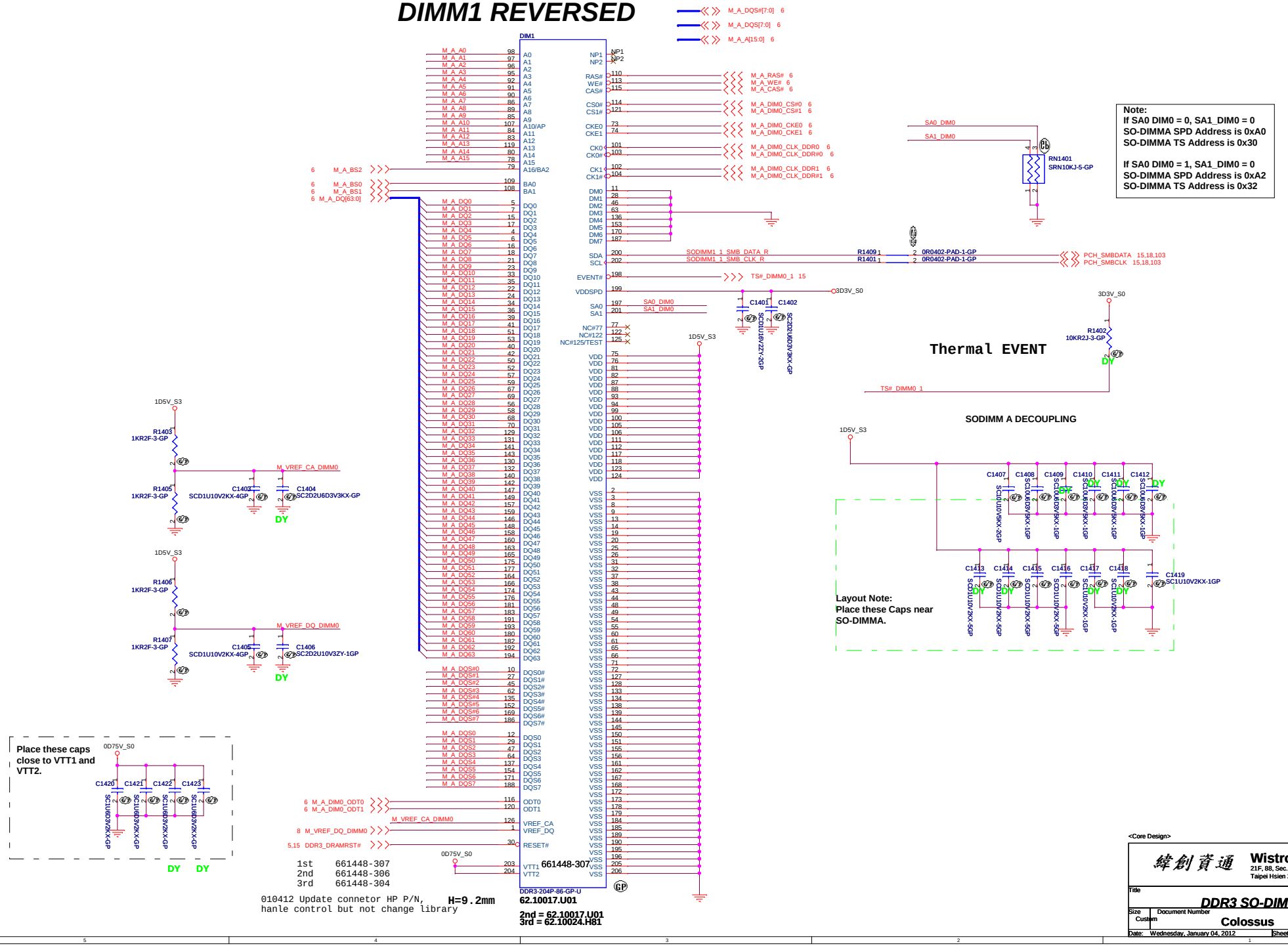
Title

AOAC

Size	Document Number	Rev
A3	**Colossus**	1

Date: Monday, December 26, 2011 Sheet 13 of 103

DIMM1 REVERSED



1st 661448-307
2nd 661448-306
3rd 661448-304

010412 Update connetor HP P/N, H=9.2mm
hanle control but not change library

62.10017.U01

2nd = 62.10017.U01
3rd = 62.10024.H81

<Core Design>

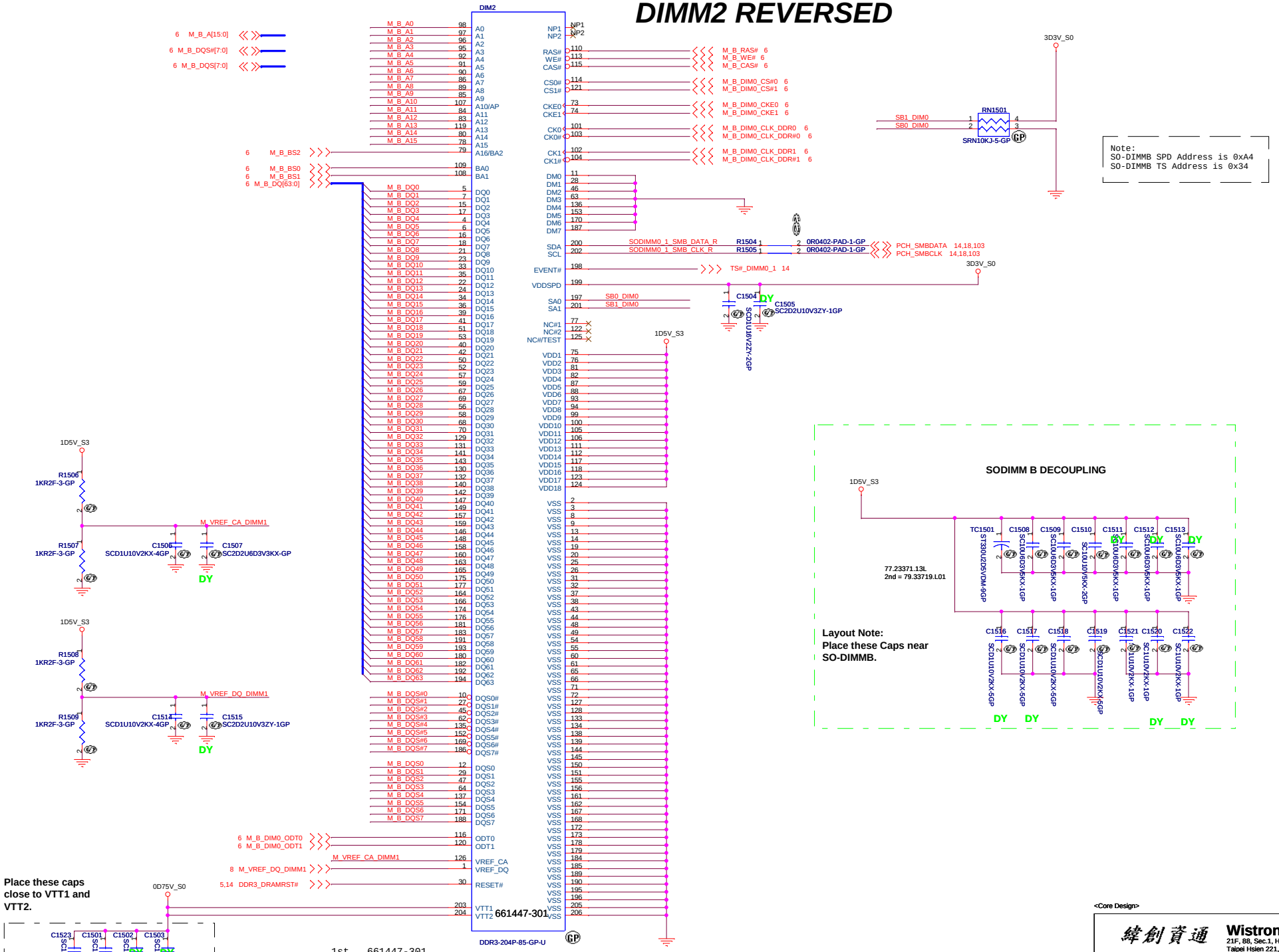
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3 SO-DIMM1

Size	Document Number	Rev
Custom	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 14 of 103

DIMM2 REVERSED



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3 SO-DIMM2

Size	Document Number	Rev
Custom	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 15 of 103

(Blanking)

<Core Design>

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Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 16 of 103

PCH(1/9)

INTVRMEN- Integrated
SUS 1.05V VRM Enable
High - Enable internal VRs

PCH1A — 1 OF 10 — PANTHER-GP-NF

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
LPC: FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME#, LDRQ0#, LDRQ1#/GPIO23, SERIRQ
IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO13
SATA: SATA 6G — SATA0RXN/RXP, SATA0TXN/TXP, SATA1RXN/RXP, SATA1TXN/TXP, SATA2RXN/RXP, SATA2TXN/TXP, SATA3RXN/RXP, SATA3TXN/TXP, SATA4RXN/RXP, SATA4TXN/TXP, SATA5RXN/RXP, SATA5TXN/TXP, SATAICOMPO, SATAICOMPI, SATA3RCOMPO, SATA3COMPI, SATA3RBIAS, SATALED#, SATA0GP/GPIO21, SATA1GP/GPIO19
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

HDD1 / mSATA / HDD2 / ODD

NEED TO PLACE CLOSE TO PCH

RTC Battery

RTC1 — ACES-CON2-18-GP — 20.F1637.002
U1701 — M715FPT-GP — 83.R0304.B81
C1705 SC1U10V3ZY-6GP
2ND = 20.F1864.002
2ND = 83.R2004.C81

NO REBOOT STRAP

No Reboot Strap R1722	
HDA_SPKR	Low = Default High = No Reboot

LAYOUT NOTE:

JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP
JTAG_TCK TERMINATIONS NEED TO BE PLACED NEAR PCH

<Core Design>

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Title: PCH(1/9): HDA/JTAG/SATA
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 17 of 103

PCH(2/9)

PCH1B

2 OF 10

15DY_17UP
15DY_17UP

17"Card Read

82 PCIE_RXN2_MEDIA17
82 PCIE_RXP2_MEDIA17
82 PCIE_TXN2_MEDIA17
82 PCIE_TXP2_MEDIA17

C1808 1 SCD1U10V2KX-5GP PCIE_TXN2_C
C1812 1 SCD1U10V2KX-5GP PCIE_TXP2_C

15"Card Read

32 PCIE_RXN3_MEDIA
32 PCIE_RXP3_MEDIA
32 PCIE_TXN3_MEDIA
32 PCIE_TXP3_MEDIA

C1805 1 SCD1U10V2KX-5GP PCIE_TXN3_C
C1806 1 SCD1U10V2KX-5GP PCIE_TXP3_C

15UP_17DY
15UP_17DY

WLAN

65 PCIE_RXN4_WLAN
65 PCIE_RXP4_WLAN
65 PCIE_TXN4_WLAN
65 PCIE_TXP4_WLAN

C1809 1 SCD1U10V2KX-5GP PCIE_TXN4_C
C1807 1 SCD1U10V2KX-5GP PCIE_TXP4_C

LAN

31 PCIE_RXN6_LAN
31 PCIE_RXP6_LAN
31 PCIE_TXN6_LAN
31 PCIE_TXP6_LAN

C1810 1 SCD1U10V2KX-5GP PCIE_TXN6_C
C1811 1 SCD1U10V2KX-5GP PCIE_TXP6_C

PCI-E*

BG34 PERN1
BJ34 PERP1
AV32 PETN1
AU32 PETP1
BE34 PERN2
BF34 PERP2
BB32 PETN2
AY32 PETP2
BG36 PERN3
BJ36 PERP3
AV34 PETN3
AU34 PETP3
BF36 PERN4
BE36 PERP4
AY34 PETN4
BB34 PETP4
BG37 PERN5
BH37 PERP5
AY36 PETN5
BB36 PETP5
BJ38 PERN6
BG38 PERP6
AU36 PETN6
AV36 PETP6
BG40 PERN7
BJ40 PERP7
AY40 PETN7
BB40 PETP7
BE38 PERN8
BC38 PERP8
AW38 PETN8
AY38 PETP8

3D3V_S0_WLAN

R1808 1KR2J-1-GP

Q1801 2N7002K-2-GP

65 CLKRQ_WLAN#_C

CLKRQ_WLAN#

R1809 0R2J-2-GP

DY

17"Card Read

82 CLK_PCIE_MEDIA17#
82 CLK_PCIE_MEDIA17

82 CLKREQ_MEDIA#17

15"Card Read

32 CLK_PCIE_MEDIA#
32 CLK_PCIE_MEDIA

32 CLKREQ_MEDIA#

WLAN

65 CLK_PCIE_WLAN#
65 CLK_PCIE_WLAN

CLKRQ_WLAN#

LAN

31 CLK_PCIE_LAN#
31 CLK_PCIE_LAN

31 CLKREQ_LAN#

CLOCKS

Y40 CLKOUT_PCIE0N
Y39 CLKOUT_PCIE0P
GPIO73 J2 PCIECLKRQ0#/GPIO73
AB49 CLKOUT_PCIE1N
AB47 CLKOUT_PCIE1P
GPIO18 M1 PCIECLKRQ1#/GPIO18
AA48 CLKOUT_PCIE2N
AA47 CLKOUT_PCIE2P
V10 PCIECLKRQ2#/GPIO20
Y37 CLKOUT_PCIE3N
Y36 CLKOUT_PCIE3P
A8 PCIECLKRQ3#/GPIO25
Y43 CLKOUT_PCIE4N
Y45 CLKOUT_PCIE4P
L12 PCIECLKRQ4#/GPIO26
V45 CLKOUT_PCIE5N
V46 CLKOUT_PCIE5P
GPIO44 L14 PCIECLKRQ5#/GPIO44
AB42 CLKOUT_PEG_B_N
AB40 CLKOUT_PEG_B_P
GPIO56 E6 PEG_B_CLKRQ#/GPIO56
V40 CLKOUT_PCIE6N
V42 CLKOUT_PCIE6P
T13 PCIECLKRQ6#/GPIO45
V38 CLKOUT_PCIE7N
V37 CLKOUT_PCIE7P
CLKRQ_WWAN# K12 PCIECLKRQ7#/GPIO46
AK14 CLKOUT_ITPXDP_N
AK13 CLKOUT_ITPXDP_P

PANTHER-GP-NF

SMBUS

SMBALERT#/GPIO11 E12
SMBCLK H14 PCH_SMB_CLK
SMBDATA C9 PCH_SMB_DATA

SML0ALERT#/GPIO60 A12
SML0CLK C8 PCH_SML0_CLK
SML0DATA G12 PCH_SML0_DATA

SML1ALERT#/PCHHOT#/GPIO74 C13 PCH_GPIO74
SML1CLK/GPIO58 E14 PCH_SML1CLK
SML1DATA/GPIO75 M16 PCH_SML1DATA

Controller Link

CL_CLK1 M7
CL_DATA1 T11
CL_RST1# P10

FLEX CLOCKS

CLKOUTFLEX0/GPIO64 K43 CLK_48_USB30
CLKOUTFLEX1/GPIO65 F47 CLK_27_NSSC
CLKOUTFLEX2/GPIO66 H47
CLKOUTFLEX3/GPIO67 K49 CLK_14M_KBC_P

3D3V_S5

R1806 10KR2J-3-GP
EC_SW# 27

PCH_SMB_CLK 69
PCH_SMB_DATA 69

R1807 1KR2J-1-GP

PCH_DDR_RST# 5,8

TP1803 TPAD14-OP-GP
TP1805 TPAD14-OP-GP

14,15,103 PCH_SMBDATA

3D3V_S0

RN1803 SRN2K2J-1-GP

U1801 DMN66D0LDW-7

PCH_SMB_DATA
PCH_SMB_CLK
PCH_SMBCLK 14,15,103

84.DMN66.03F

XTAL25_IN
XTAL25_OUT

C1801 SC15P50V2JN-2-GP
C1802 SC15P50V2JN-2-GP

R1805 1MR2J-1-GP

X1801 XTAL-25MHZ-155-GP

12pF30PPM

82.30020.D41
2ND = 82.30020.G71
3RD = 82.30020.G61

-1 1220

R1804 0R0402-PAD-1-GP

PEG_A_CLKRQ#/GPIO47 M10 CLKREQ_PEG_A#
CLKREQ_PEG_A# 83

CLKOUT_PEG_A_N AB37
CLKOUT_PEG_A_P AB38

RN1810 SRN0J-6-GP

CLK_PCIE_VGA# 83
CLK_PCIE_VGA 83

CLKOUT_DMI_N AV22
CLKOUT_DMI_P AU22

CLKOUT_DMI_N 5
CLKOUT_DMI_P 5

CLKOUT_DP_N AM12
CLKOUT_DP_P AM13

3D3V_AUX_S5

RN1802 SRN2K2J-4-GP

PCH_SML1CLK
PCH_SML1DATA

U1802 DMN66D0LDW-7

27,29,79,86 SML1_CLK
PCH_SML1DATA
SML1_DATA 27,29,79,86
PCH_SML1CLK

84.DMN66.03F

CLOCK TERMINATION FOR FCIM

CLKIN_DMI_N BF18
CLKIN_DMI_P BF18

RN1806 SRN10KJ-5-GP

CLKIN_GND1_N BJ30
CLKIN_GND1_P BG30

RN1807 SRN10KJ-5-GP

CLKIN_DOT_96N G24
CLKIN_DOT_96P E24

RN1808 SRN10KJ-5-GP

CLKIN_SATA_N AK7
CLKIN_SATA_P AK5

RN1809 SRN10KJ-5-GP

REFCLK14IN K45 CLK_BUF_REF14

R1802 10KR2J-3-GP

All resistors need very close to PCH

CLKIN_PCILOOPBACK H45
CLK_PCI_FB 21

XTAL25_IN V47
XTAL25_OUT V49

XCLK_RCOMP Y47

1D05V_S0

R1803 90D9R2F-1-GP

RN1801 SRN2K2J-1-GP

PCH_SMB_CLK
PCH_SMB_DATA

CLK_14M_KBC_P

DY

C1803 SC68P50V2JN-1GP

TP1801 TPAD14-OP-GP
TP1802 TPAD14-OP-GP
CLK_27M_VGA
TP1804 TPAD14-OP-GP

<Core Design>

RN1804 SRN10KJ-L3-GP

CLKREQ_LAN#
PCH_GPIO74
CLKRQ_WWAN#
GPIO44

3D3V_S5

CLKRQ_WLAN#
GPIO56
CLKREQ_MEDIA#
GPIO73

RN1805 SRN10KJ-3GP

3D3V_S0

GPIO18
CLKREQ_MEDIA#17

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Taipei Hsien 221, Taiwan, R.O.C.

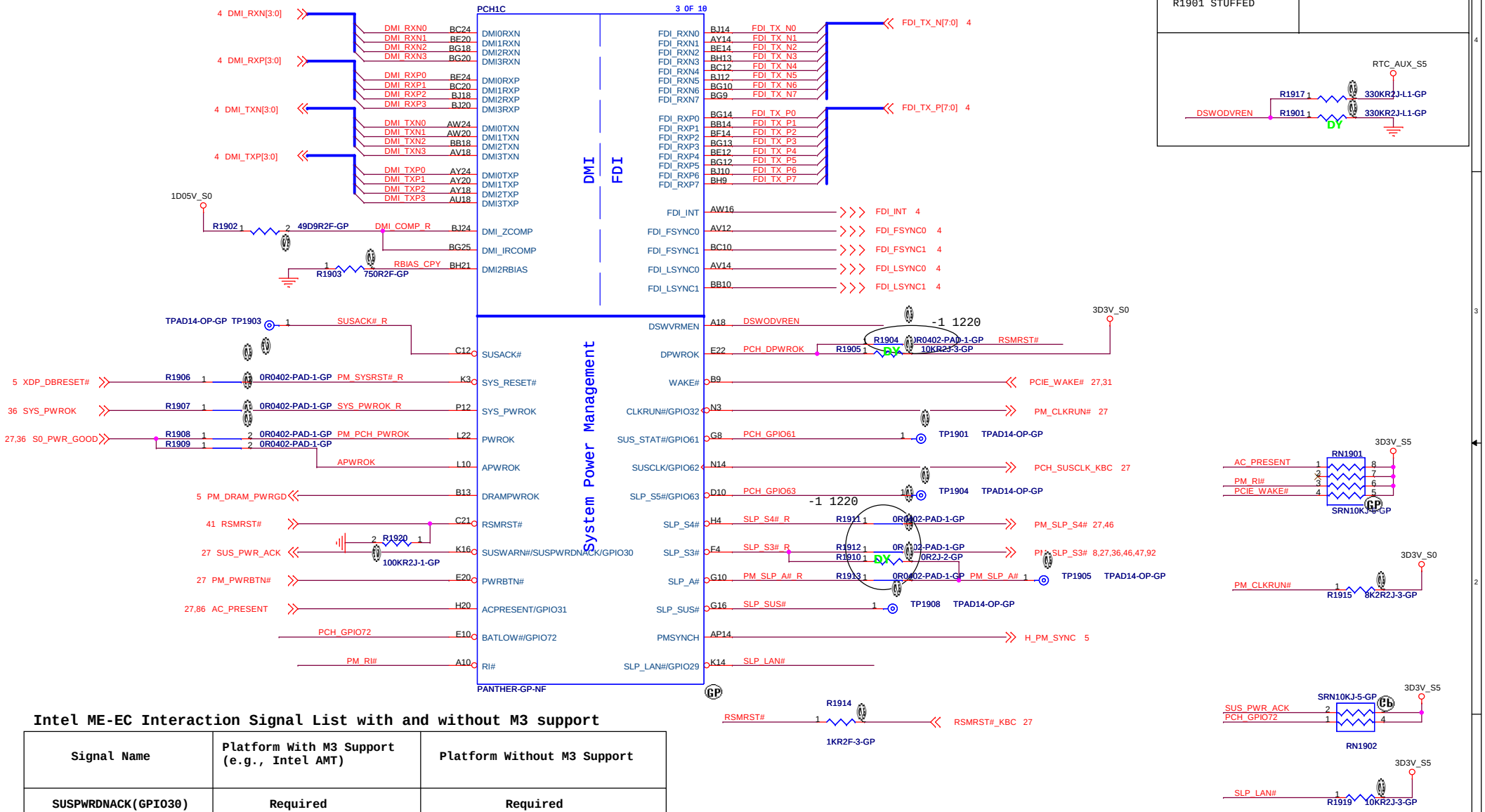
Title: PCH(2/9): PCIE/SMBUS/CLK

Size: A3 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 18 of 103

PCH(3/9)

DSWODVREN - On Die DSW VR Enable	
HIGH (R1917 STUFFED, R1901 UNSTUFFED	Enabled (DEFAULT)
LOW (R1917 UNSTUFFED, R1901 STUFFED	Disabled



Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC prespecrive.

<Core Design>

Wistron Corporation
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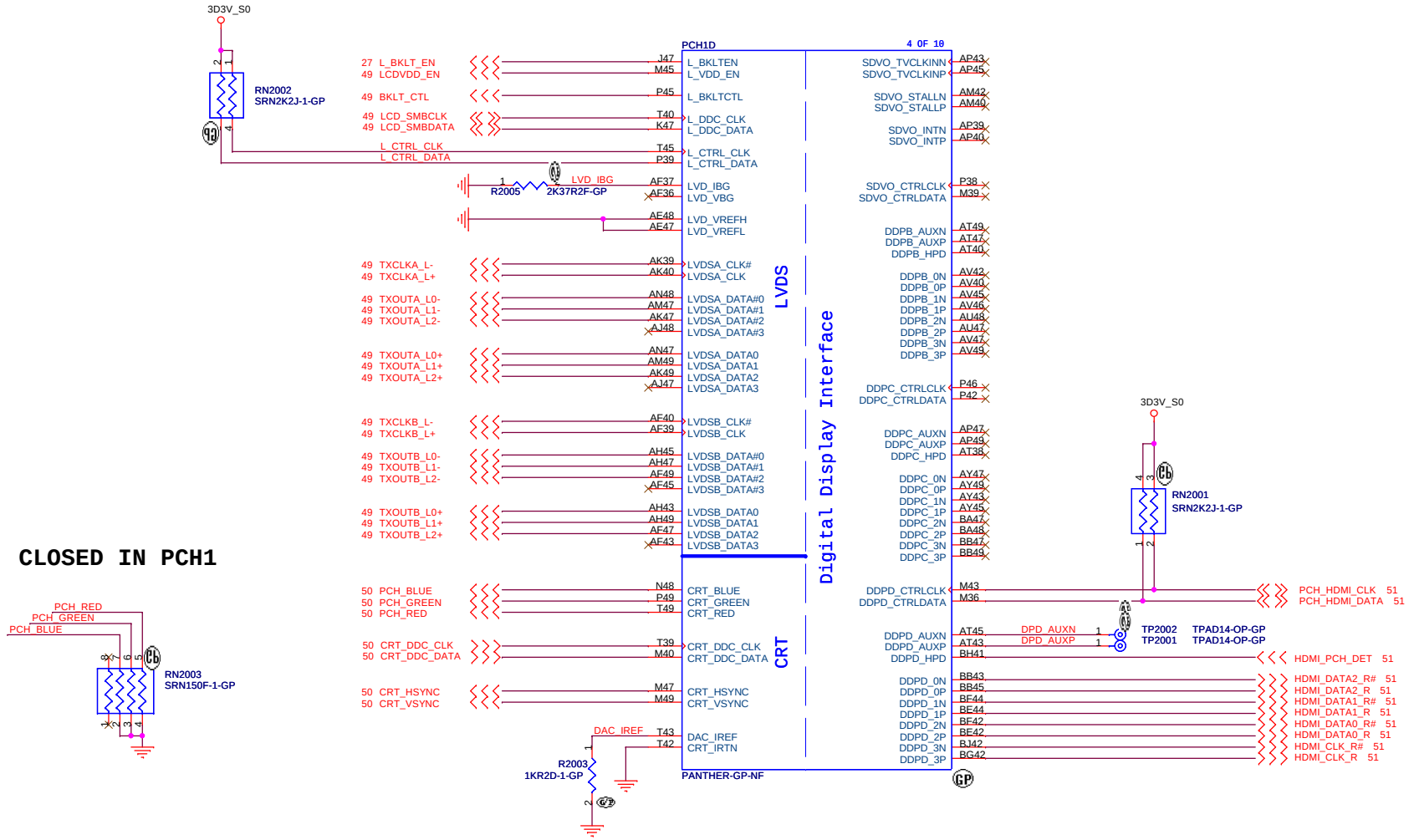
Title: PCH(3/9): DMI/FDI/PM

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 19 of 103

PCH(4/9)



CLOSED IN PCH1

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH(4/9): LVDS/CRT/DDI**

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 20 of 103

PCH(5/9)

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB3.0 Table

USB	
Pair	Device
1	I/O CONN. 1 LEFT_DOWN
2	FREE
3	I/O CONN. 2 LEFT_UP
4	I/O CONN. 3 RIGHT_UP

USB2.0 Table

USB	
Pair	Device
0	USB 3.0 I/O CONN.
1	N/A
2	USB 3.0 I/O CONN.
3	USB 3.0 I/O CONN.
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 CONN(Debug)
10	Camera
11	FREE
12	FREE
13	FREE

USB 3.0 Conn. 1
USB 3.0 Conn. 2
USB 3.0 Conn. 3 (UB1)
BT WLAN combo
Fingerprint
USB 2.0 Conn. 1 (UB1)
Camera
-1 12/15

USB 3.0/2.0 Port Pairing

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

(UB2)
(UB2)
-1 12/15

73.01G08.L04
2ND = 73.7SZ08.EAH
3RD = 73.7SZ08.DAH

Wistron Corporation	緯創資通
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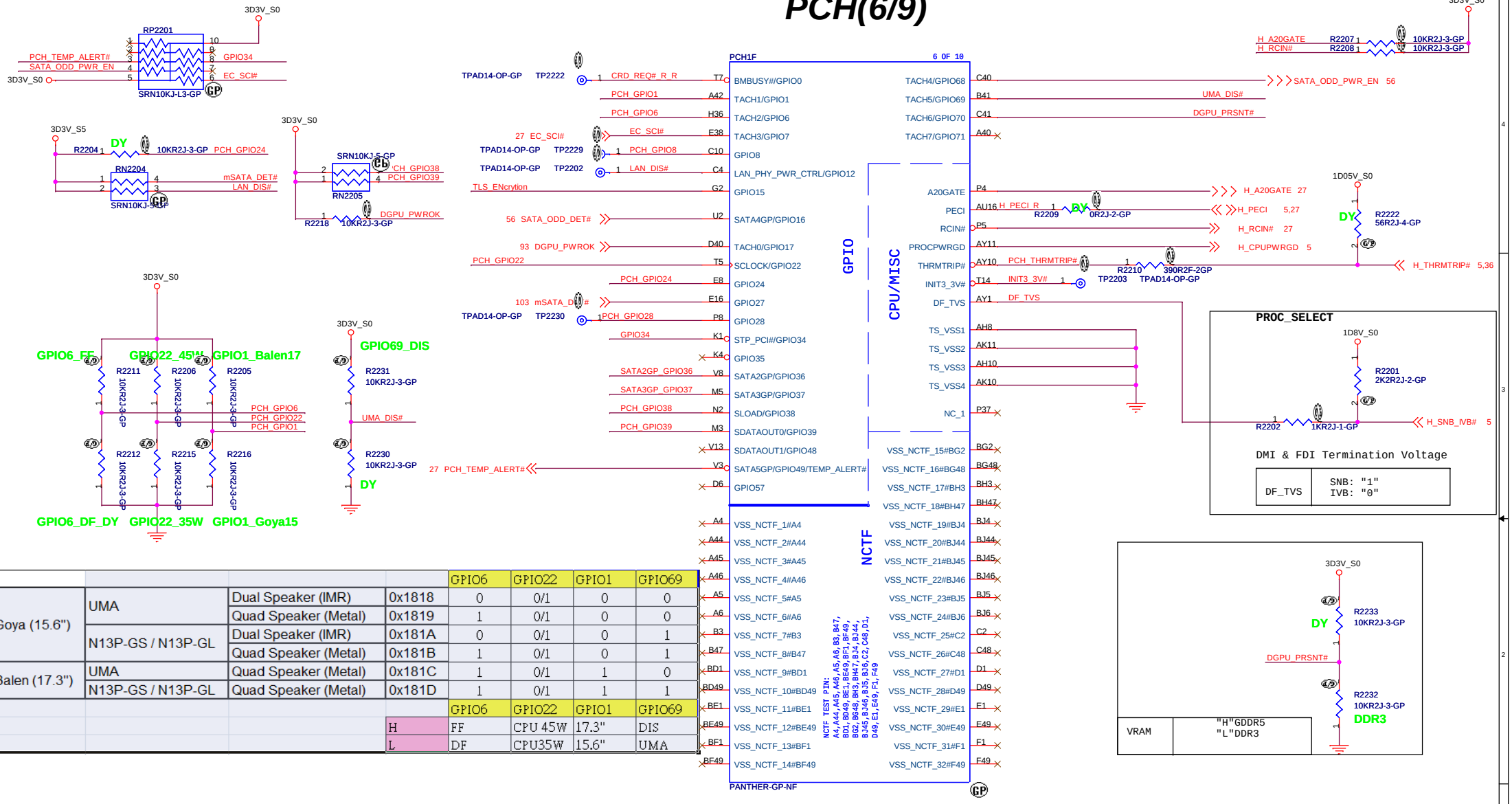
Title: PCH(5/9): PCI/USB/NVM	
Size: A3	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 21 of 103

PCH(6/9)



				GPIO6	GPIO22	GPIO1	GPIO69
Goya (15.6")	UMA	Dual Speaker (IMR)	0x1818	0	0/1	0	0
		Quad Speaker (Metal)	0x1819	1	0/1	0	0
	N13P-GS / N13P-GL	Dual Speaker (IMR)	0x181A	0	0/1	0	1
		Quad Speaker (Metal)	0x181B	1	0/1	0	1
Balen (17.3")	UMA	Quad Speaker (Metal)	0x181C	1	0/1	1	0
	N13P-GS / N13P-GL	Quad Speaker (Metal)	0x181D	1	0/1	1	1
				GPIO6	GPIO22	GPIO1	GPIO69
			H	FF	CPU 45W	17.3"	DIS
			L	DF	CPU35W	15.6"	UMA

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

<Core Design>

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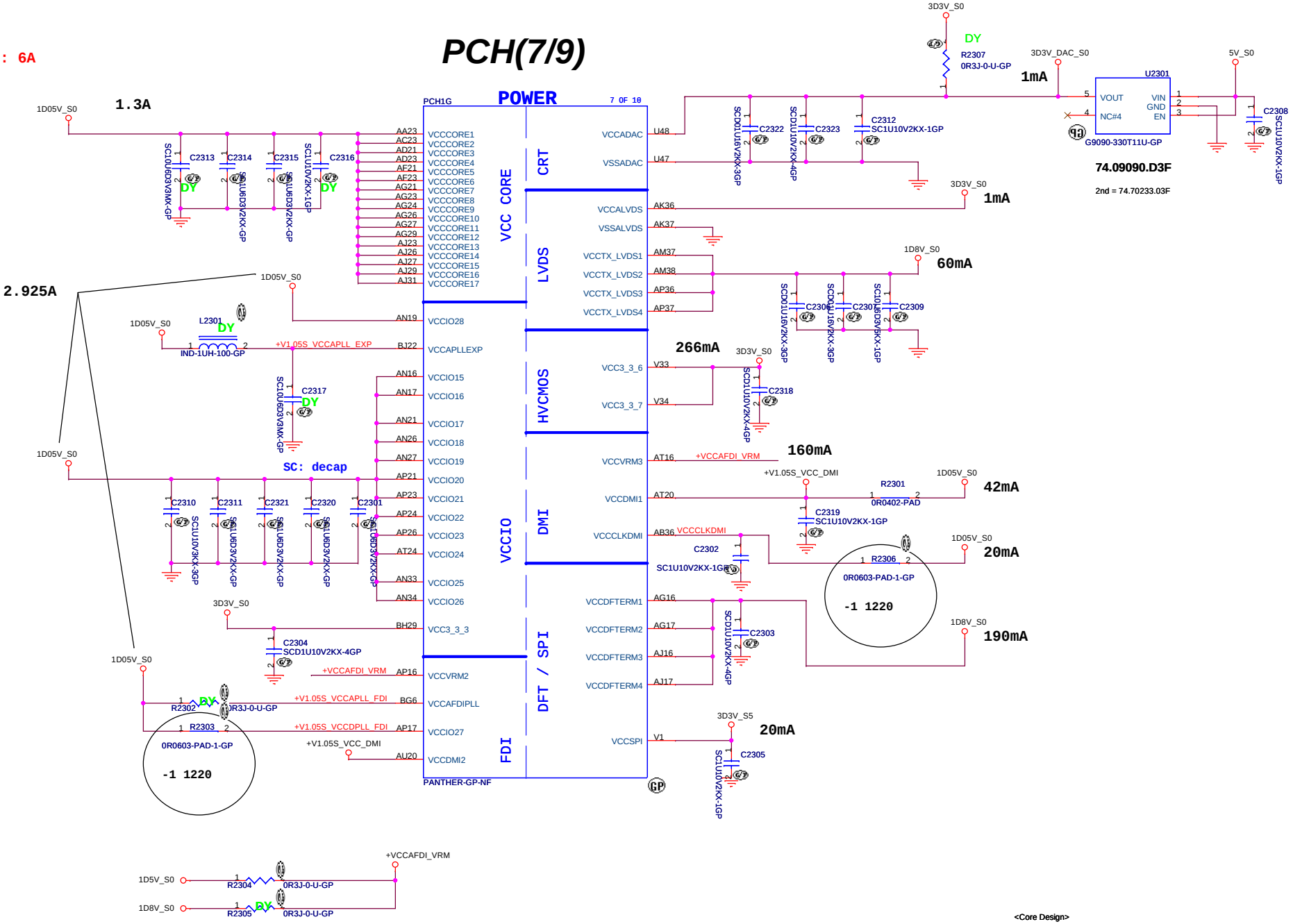
Title: PCH(6/9): GPIO/NTCF/RSVD

Size	Document Number	Rev
A3	Colossus	1

Date: Thursday, January 05, 2012 Sheet 22 of 103

VCC_PCH: 6A

PCH(7/9)



<Core Design>

Wistron Corporation
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Title: PCH(7/9): PWR1

Size	Document Number	Rev
A3	Colossus	1

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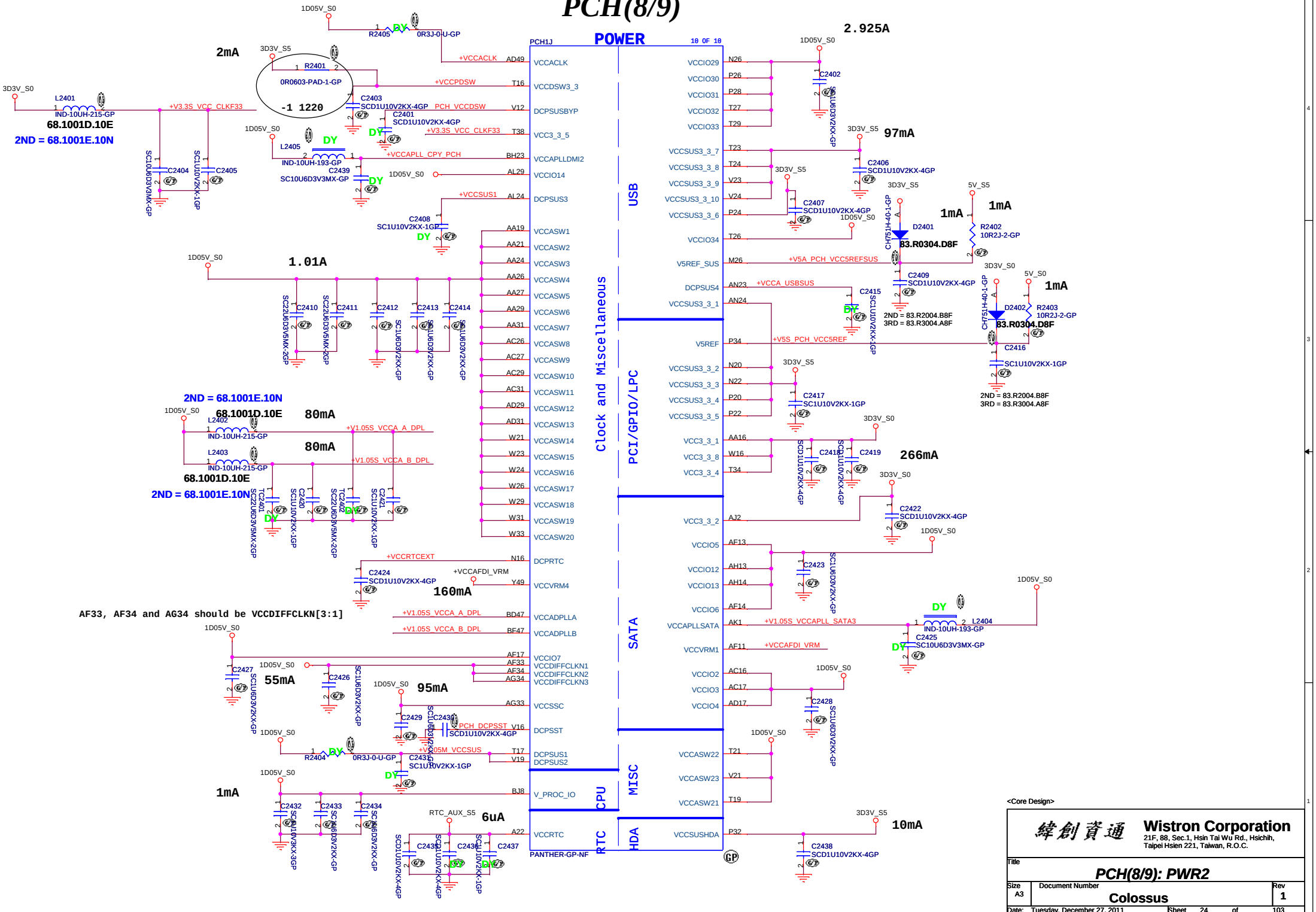
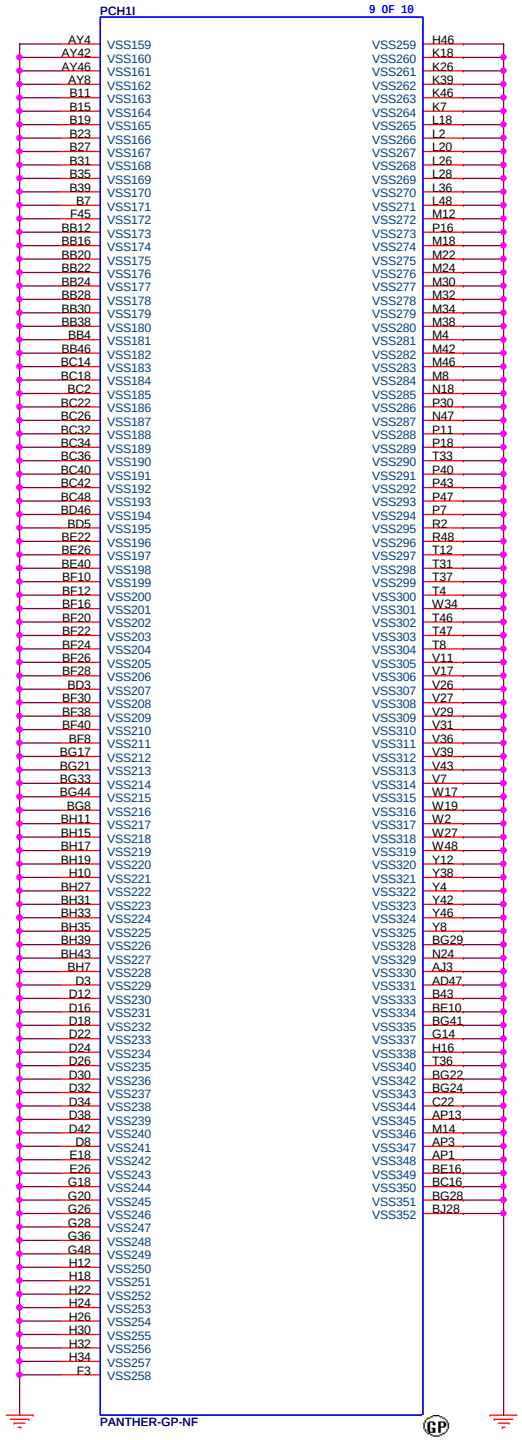
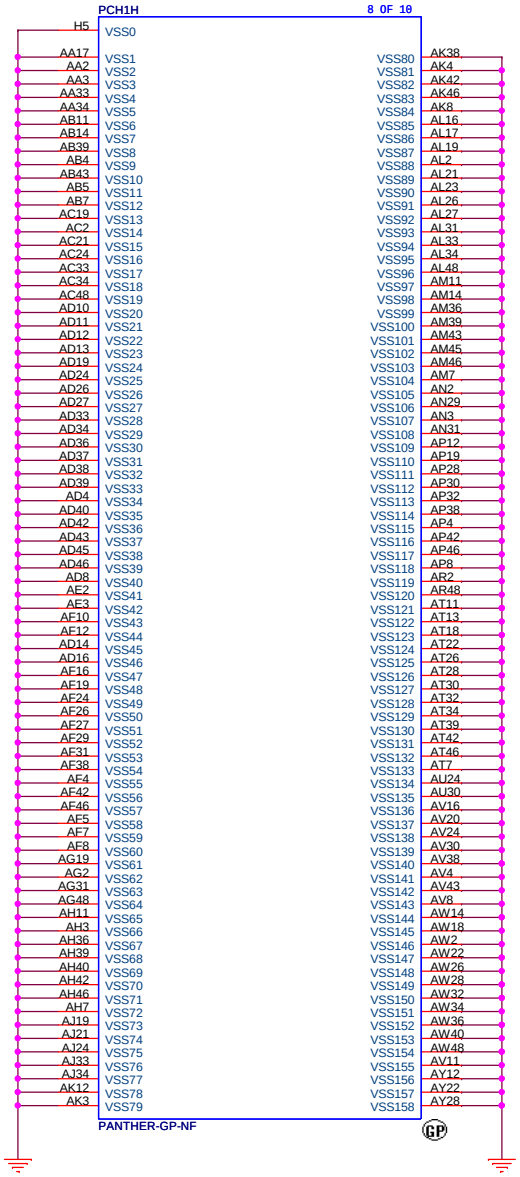
PCH(8/9)


POWER
10 OF 10
PCH1J
PANTHER-GP-NF
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA
2.925A
2mA
1.01A
80mA
80mA
160mA
55mA
95mA
1mA
6uA
97mA
1mA
1mA
266mA
10mA
68.1001D.10E
2ND = 68.1001E.10N
AF33, AF34 and AG34 should be VCCDIFFCLKN[3:1]
2ND = 83.R2004.B8F
3RD = 83.R3004.A8F
83.R0304.D8F
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH(8/9): PWR2
Size A3
Document Number
Colossus
Rev 1
Date: Tuesday, December 27, 2011
Sheet 24 of 103

PCH(9/9)





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH(9/9): GND**

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 25 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***PCH XDP***	
Size: A3	Document Number: **Colossus**	Rev: 1
Date: Monday, December 26, 2011	Sheet 26 of 103	

SSID = KBC

U2701

20110608 for vendor debug

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

MODEL ID

Model_ID	Model_ID (SI2)	Pull-Low Register	Pull-High Register	Typical Voltage
Goya(15.6")	UMA	UMA (35W)	100.0 K	10.0 K	3.000 V
	UMA	UMA (45W)	100.0 K	20.0 K	2.750 V
Goya(15.6")	DIS	DIS GL (35W)	100.0 K	33.0 K	2.481 V
	DIS	DIS GL (45W)	100.0 K	47.0 K	2.245 V
Balen(17.3")	UMA	UMA (35W)	100.0 K	64.9 K	2.001 V
Balen(17.3")	DIS	DIS GL (35W)	100.0 K	76.8 K	1.867 V
Balen(17.3")		DIS GL (45W)	100.0 K	100.0 K	1.650 V
Balen(17.3")	eserved for project u	DIS GT (35W)	100.0 K	143.0 K	1.358 V
Balen(17.3")	eserved for project u	DIS GT (45W)	100.0 K	174.0 K	1.204 V
Balen(17.3")	eserved for project u	UMA (45W)	100.0 K	215.0 K	1.048 V
Goya(15.6")	eserved for project u	DIS GT (35W)	100.0 K	237.0 K	0.979 V
Goya(15.6")	eserved for project u	DIS GT (45W)	100.0 K	261.0 K	0.914 V

Prevent BIOS data loss solution

HP Limit Signal Detect

HP AIRLINE COMBO

EC GPIO standard PH/PL

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Taipei Hsien 221, Taiwan, R.O.C.

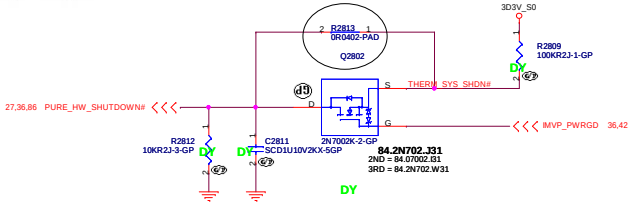
Title: EC CONTROLLER

Size: A2 | Document Number: Colossus | Rev: 1

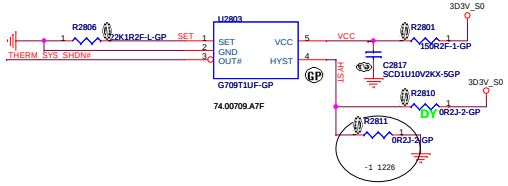
Date: Thursday, January 05, 2012 | Sheet 27 of 103

$R_{SET}(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$

where T is the trip temperature in Centigrade. R_{SET} is the set- point resistance.



90 C

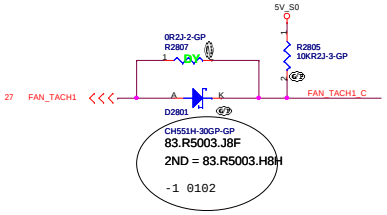


Global Mixed-mode Technology Inc. G709/G710

Pin Description

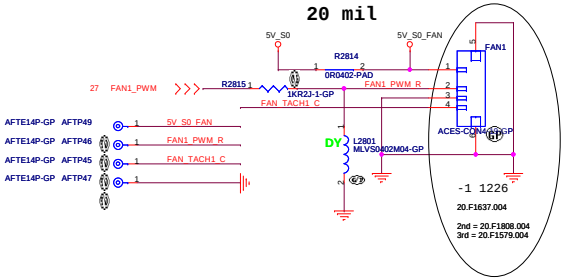
PIN		NAME	FUNCTION
G709	G710		
1	1	SET	Temperature Set Point, Connect an external 1% resistor from SET to GND to set trip point.
2	2	GND	Ground
3	3	$\overline{OT}$	Open-Drain Active Low Output.
4	4	HYST	Hysterisis Selection. Hysterisis is 10°C for HYST = V_{CC}, 2°C for HYST = GND.
	5	N.C.	Not Connected.
5	6	VCC	Power-Supply Input.

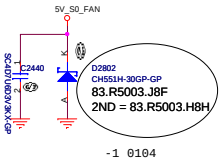
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
HYST Input Threshold	V_{IH}		0.7 x V_{CC}	---	---	V
	V_{IL}		---	---	0.3 x V_{CC}	V



FOR PWM FAN

20 mil





<Core Design>

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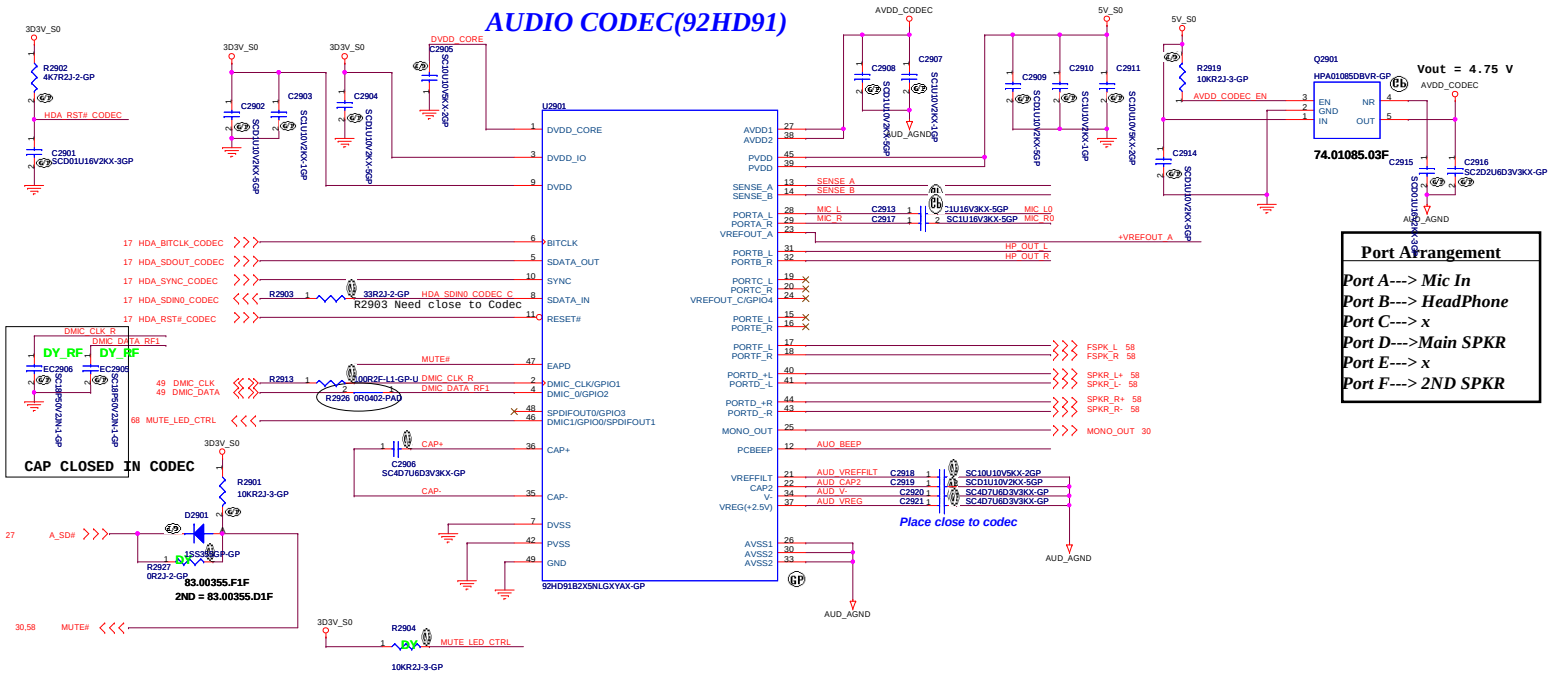
Title: Thermal/FAN

Size: A2 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 28 of 103

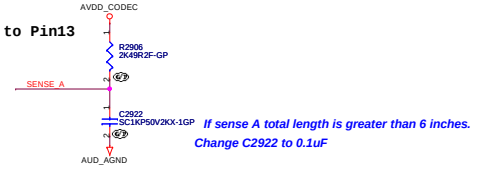
AUDIO CODEC(92HD91)



SENSE Detect

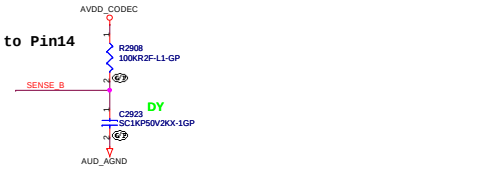
Headphone Trace = 15mil

Close to Pin13



If sense A total length is greater than 6 inches.
Change C2922 to 0.1uF

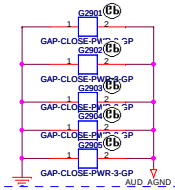
Close to Pin14



Digital GND & AUD_AGND

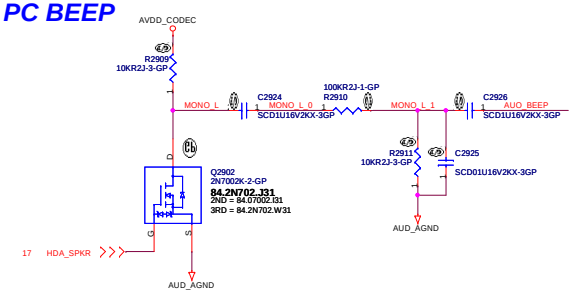
Tie Analog GND and Digital GND under codec by a single point

0818 IDT request
Place under U2901



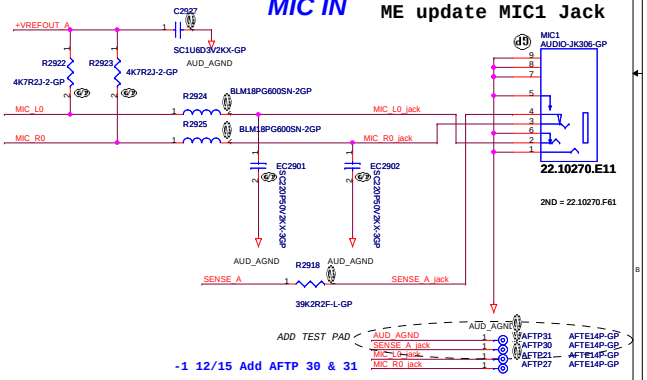
audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

PC BEEP



MIC IN

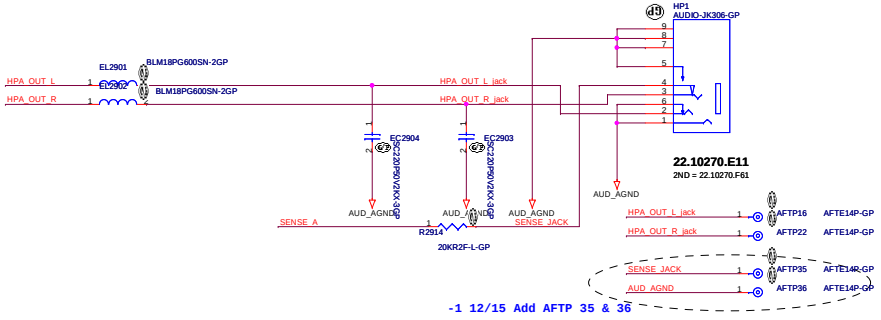
ME update MIC1 Jack



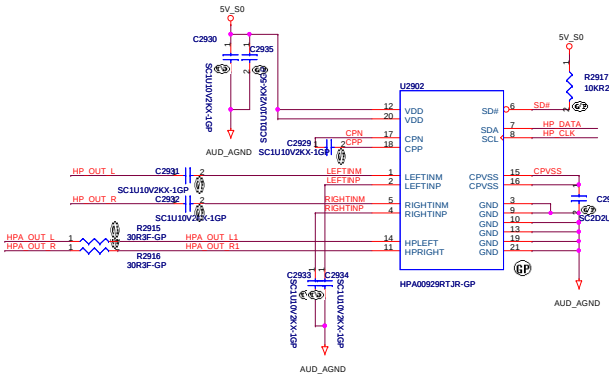
-1 12/15 Add AFTP 30 & 31

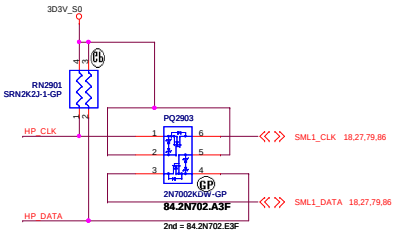
HeadPhone

ME update HP1 Jack



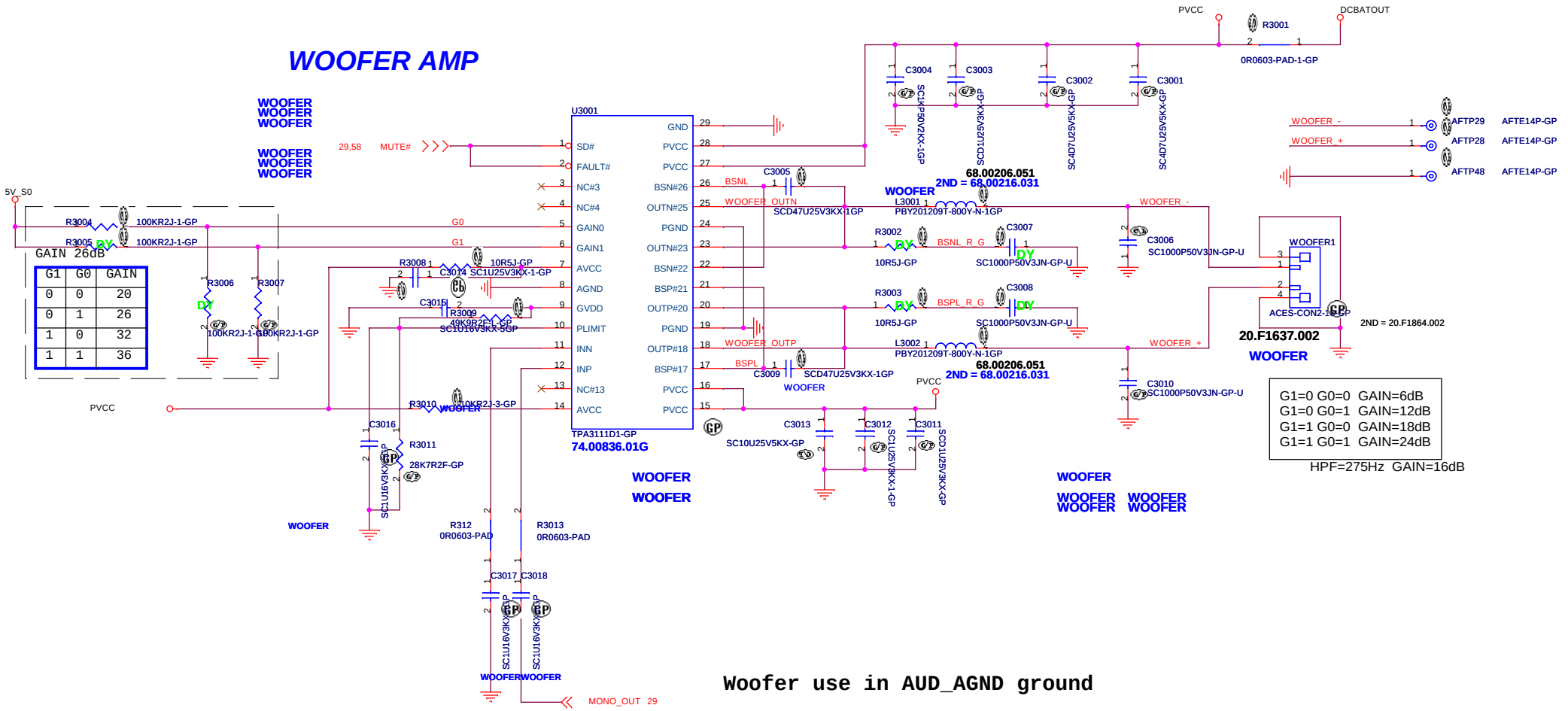
-1 12/15 Add AFTP 35 & 36





<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Audio Codec 92HD91/HeadphoneAMP
Size: A2	Document Number: Colossus
Rev	1
Date: Wednesday, January 04, 2012	Sheet 29 of 103



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

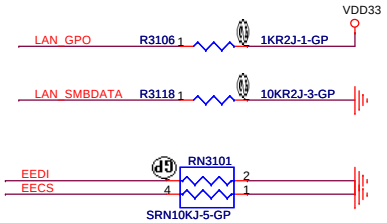
Title: Audio AMP SPK/WOOFER

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 30 of 103

LAN CHIP-RTL8111F

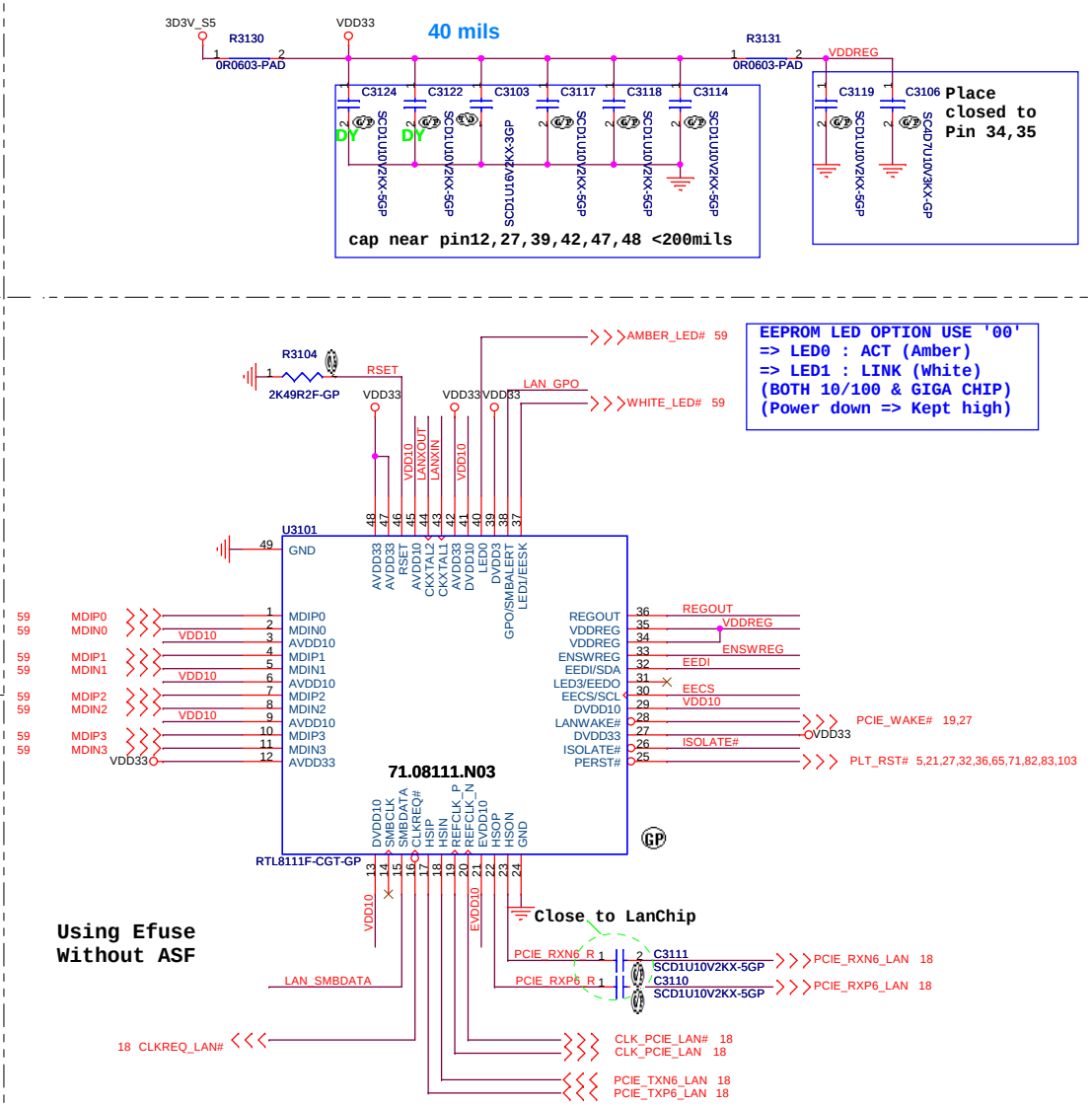
USE EFuse No ASF



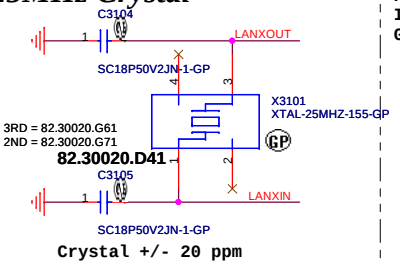
Avoid Leakage

LanChip Power

+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1mS and <100mS

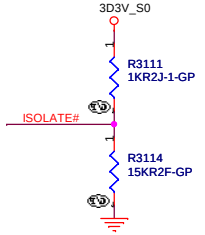


25MHz Crystal

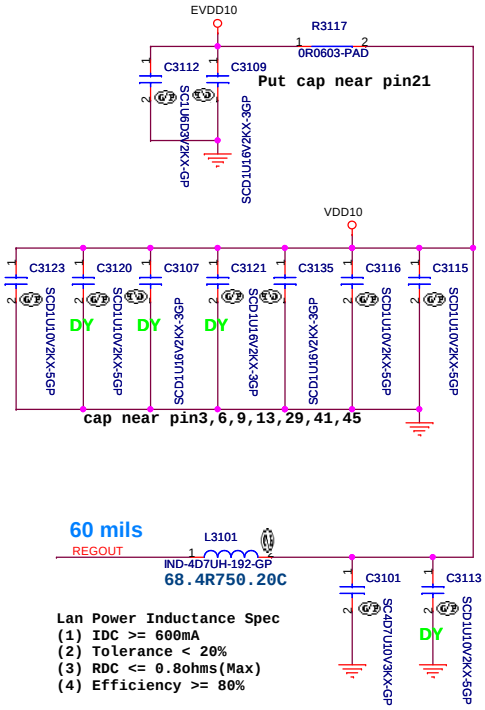


KBC Reserved Pin
Isolate# => Low , Isolate LanChip
GPO => EFuse Strap Pin

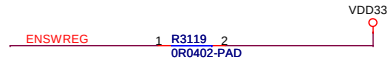
Isolate Strap Pin



Regout power plane(1D05V)



Regout Switch



ENSWREG (REGOUT 1D05V)
PH = Enable
PL = Disable

<Core Design>

緯創資通 Wistron Corporation
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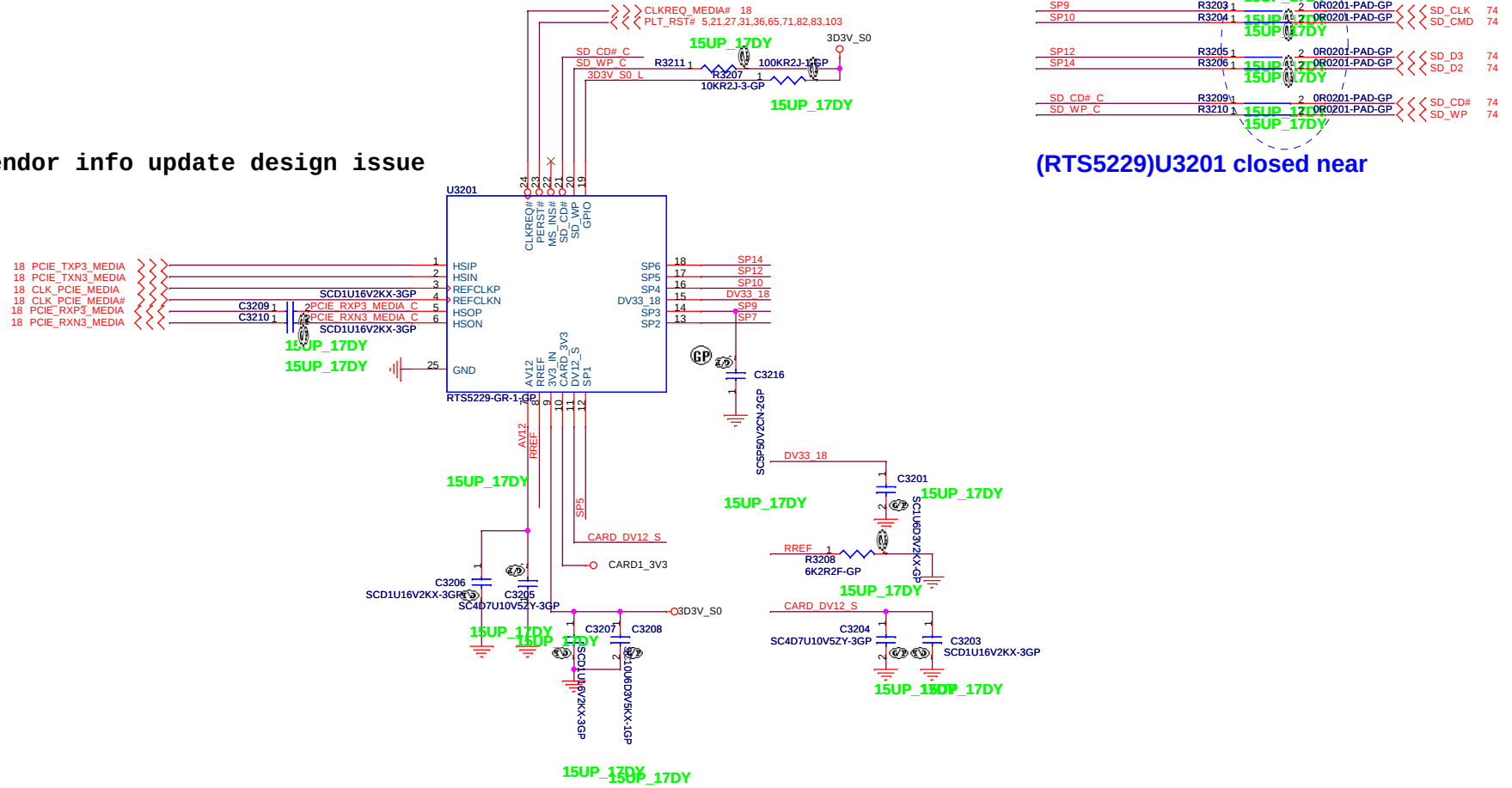
Title: LAN_RTL8111F
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 31 of 103

RTS5229

-1 12/15 0201 0 Ohm change to short pad

Vendor info update design issue

(RTS5229)U3201 closed near



<Core Design>

Wistron Corporation
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Title: Card Reader-RTS5229

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 32 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 34 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

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Power Sequence

R3614
CRB 1K

28,42 IMVP_PWRGD — R3614 0R0201-PAD-GP — SYS_PWROK
SYS_PWROK 19
19,27 S0_PWR_GOOD — D3603 BAS16-6-GP
C3612 SCD01U50V2KX-1GP
83.00016.K11
2ND = 83.00016.F11

R3623 0R0402-PAD
5,46,47 RUNPWROK
8,19,27,46,47,92 PM_SLP_S3#
U3608 74LVC1G08GW-1-GP
3D3V_S5
PWR_1D05V_1V_EN 45
73.01G08.L04
2ND = 73.7SZ08.DAH
DY

ANNIE Run Power

Run power follow TOP-1

DCBATOUT
R3619 330KR2J-L1-GP
RUN_ENABLE
R3622 0R0402-PAD
D3602 MMPZ5239BPT-GP
83.9R103.D3F
2ND = 83.9R103.F3F
R3618 470R2J-2-GP
RUN_PWR_ON_G
C3615 SCD01U50V2KX-1GP
78.10324.2FL

3D3V_AUX_S5
R3612 100KR2J-1-GP
Q3603 DMN66D0LDW-7-GP
84.DMN66.03F
8,19,27,46,47,92 PM_SLP_S3#
PS_S3CNTRL

PS_S3CNTRL
0D75V_S0
R3621 22R2J-2-GP
Q3604 DMN66D0LDW-7-GP
84.DMN66.03F
R3620 220R2F-GP
1D5V_S0

5V_S0
C3607 SCD1U25V2KX-GP
U3604 QM3004M3-GP
C3608 SCD1U25V2KX-GP
84.30043.037
2nd = 84.02657.037
5V_S5

3D3V_S0
C3616 SCD1U25V2KX-GP
U3607 QM3004M3-GP
C3609 SCD1U25V2KX-GP
84.30043.037
2nd = 84.02657.037
3D3V_S5

1D5V_S0
C3611 SCD1U25V2KX-GP
U3605 TPCA8062-H-GP
C3610 SCD1U25V2KX-GP
84.08062.037
2ND = 84.00460.037
1D5V_S3

-1 0103 check Power list

5V_S0
C3613 SCD1U10V2KX-5GP
5V_S5
C3614 SCD1U10V2KX-5GP

5V_S0
R3624 1KR2J-1-GP
Q3605 2N7002K-2-GP
PS_S3CNTRL

1D5V_S0
MAX Current 3000 mA
Design Current 2100 mA

Total= 11.39A

H_THRMTRIP# 5,22
H_PWRGD_R
Q3601 MMBT2222ALT1G-GP
84.02222.X11
2ND = 84.02222.V11
C3602 SCD1U10V2KX-5GP
5,21,27,31,32,65,71,82,83,103 PLT_RST#
R3616 4K7R2J-2-GP
R3632 2K2R2J-2-GP
83.R0304.D8F
2ND = 83.R2004.B8F
3RD = 83.R3004.A8F
41 3V_5V_EN
D3601 CH751H-40-1-GP
R3603 2KR2F-3-GP
R3602 200KR2J-L1-GP
DY
PURE_HW_SHUTDOWN# 27,28,86
S5_ENABLE 27

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 36 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

Size: A3 | Document Number: Colossus | Rev: 1

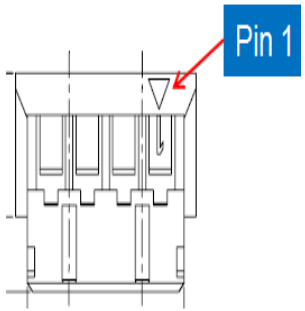
Date: Monday, December 26, 2011 | Sheet 37 of 103

Adaptor in to generate DCBATOUT

LIMIT_SIGNAL
AD_JK
AD+
PC3808 SC1KP50V2KX-1GP
PD3802 SM24DTCT-GP-U
PD3803 P6SMB27A-1-GP
DY
PC3807 SCD1U50V3KX-GP
PU3802 SI7121DN-T1-GE3-GP
PWR_AD+_2
84.07121.037
2ND = 84.06675.030
PC3805 SC1KP50V2KX-1GP
DY
EC3801 SCD1U25V2KX-GP
PC3806 SCD1U50V3KX-GP
PR3807 200KR2F-L-GP
DCIN1
DC_PIN2
DC_PIN1
LIMIT_SIGNAL
AD_JK
ACES-CON-10D-4-GP
20.81633.010
2nd = 20.81772.010
1Pin=3A
83.0SM24.A11
2ND = 83.0024V.0A1
83.P6SMB.KAG
2ND = 83.P6SBM.DAG
PWR_ADJK_EN
PQ3802
PDTA124EU-1-GP
84.00124.K1K
PR3808 100KR2J-1-GP
PQ3801
PDTC124EU-1-GP
84.00124.H1K
2ND = 84.05124.011
27 AD_OFF
PWR_ADJK_EN 40
2ND = 84.00024.01K

-1 1222 PR3802 to save 100mW when battery full.

Pin	Description	Wire color
Pin 1	White LED	White
Pin 2	Amber LED	Yellow
Pin 3	ID	Brown
Pin 4	GND	Black
Pin 5	GND	Black
Pin 6	GND	Black
Pin 7	-	
Pin 8	+VA	Red
Pin 9	+VA	Red
Pin 10	+VA	Red



PQ3803_C
PR3802 510R2J-1-GP
DC_PIN2
PL3801 MLVS0402M04-GP
PU3801
27 DC_BATFULL
CHARGE_LED 27
5V_AUX_S5
PR3811 510R2J-1-GP
84.DM601.03F
DMN601DWK-7-GP
2nd = 84.2N702.E3F
PL3802 MLVS0402M04-GP
DC_PIN1

ADD TEST PAD
PG3801 GAP-CLOSE-PWR
PG3802 GAP-CLOSE-PWR
PG3803 GAP-CLOSE-PWR
PG3804 GAP-CLOSE-PWR
PG3805 GAP-CLOSE-PWR
PG3806 GAP-CLOSE-PWR
PG3807 GAP-CLOSE-PWR
LIMIT_SIGNAL AFTP32 AFTE14P-GP
DC_PIN2 AFTP33 AFTE14P-GP
DC_PIN1 AFTP34 AFTE14P-GP
AD_JK
AFTP20 AFTE14P-GP
AFTP23 AFTE14P-GP
AFTP24 AFTE14P-GP
AFTP25 AFTE14P-GP
AFTP26 AFTE14P-GP
AFTP50 AFTE14P-GP

AD_JK
PR3809 200KR2F-L-GP
AD_DETECT 27
PC3809 SCD1U50V3KX-GP
PR3810 34K8R2F-1-GP

AC Present = White
Standby = White pulsing
Charging = Amber
***LED's are off if no AC jack pluged in**

-1 1222 PR3802 to save 100mW when battery full.

5V_AUX_S5
CHARGE_LED
PQ3804 2N7002K-2-GP
84.2N702.J31
2nd = 84.2N702.W31
PR3803 10KR2J-3-GP
PQ3803 MMBT3906-4-GP
84.T3906.A11
2nd = 84.C3906.A11
3rd = 84.03906.R11
PQ3803_C

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN JACK

Size	Document Number	Rev
A4	Colossus	1

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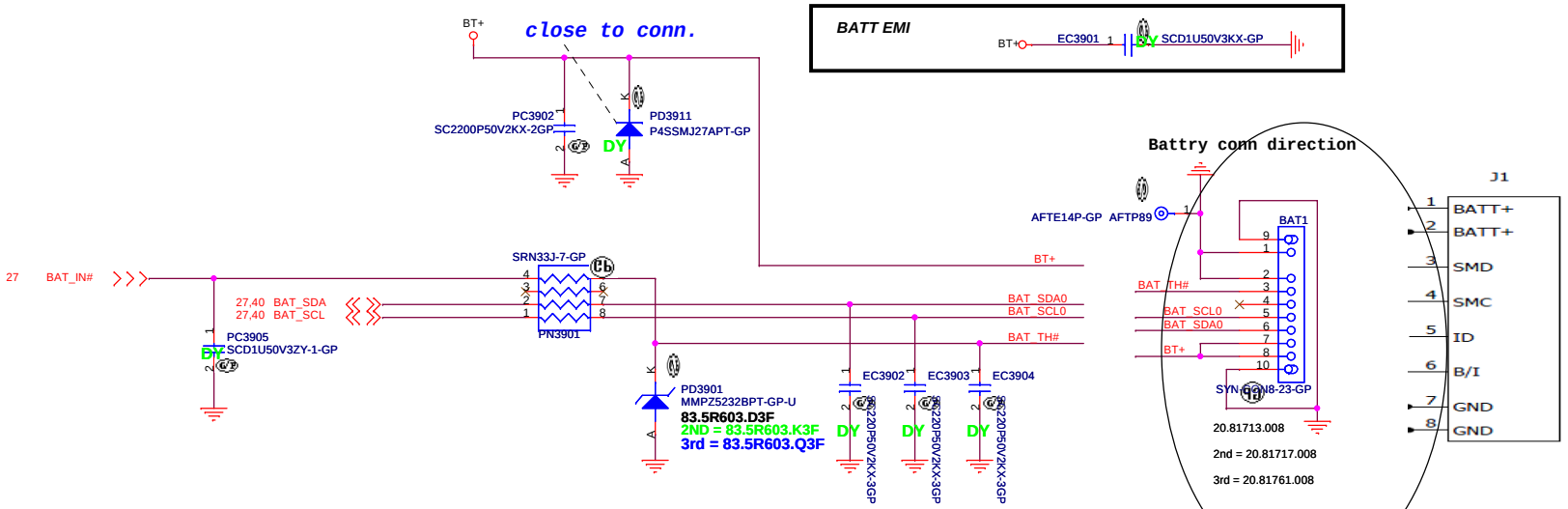
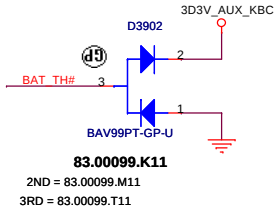
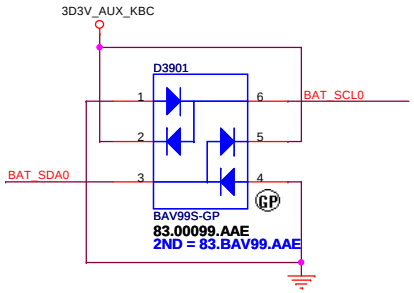
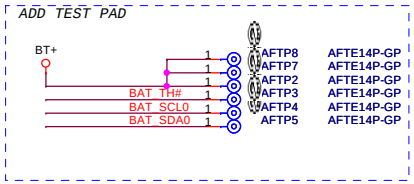
BATT Connector





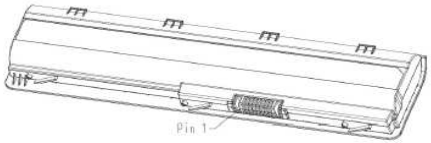




3. Interface

Connector ; 8pin
(Alltop C19029-10803-B, Foxconn BR0208C-B61H5-4H, Octek BTK-08ABEB)

Pin No.	Symbol	Description
1	BATT+	Batt+, Battery Positive Terminal
2	BATT+	Batt+, Battery Positive Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	BATT CONN	
Size: A3	Document Number: Colossus	Rev: 1
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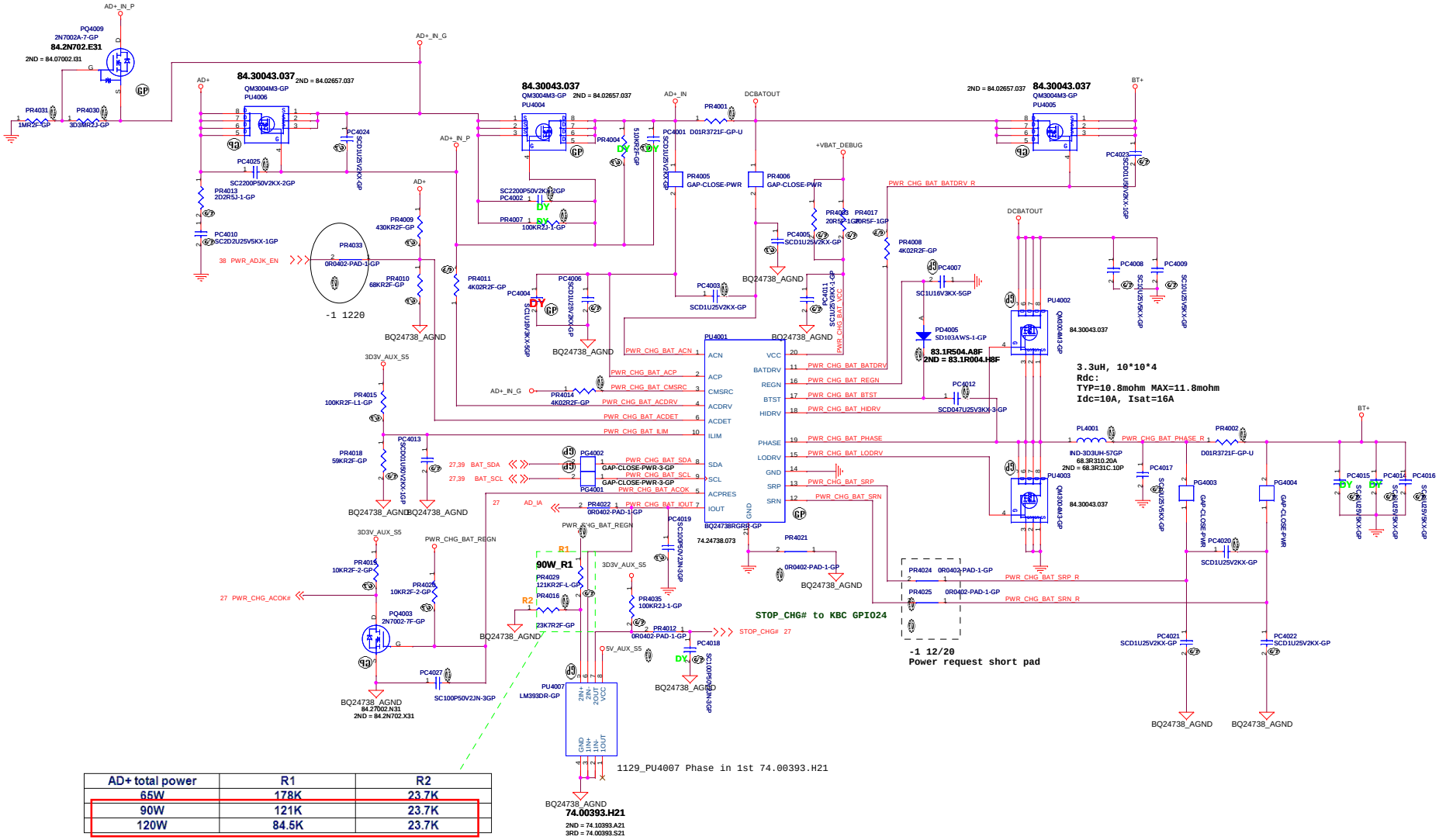

AD+ total power	R1	R2
65W	178K	23.7K
90W	121K	23.7K
120W	84.5K	23.7K

<Core Design>

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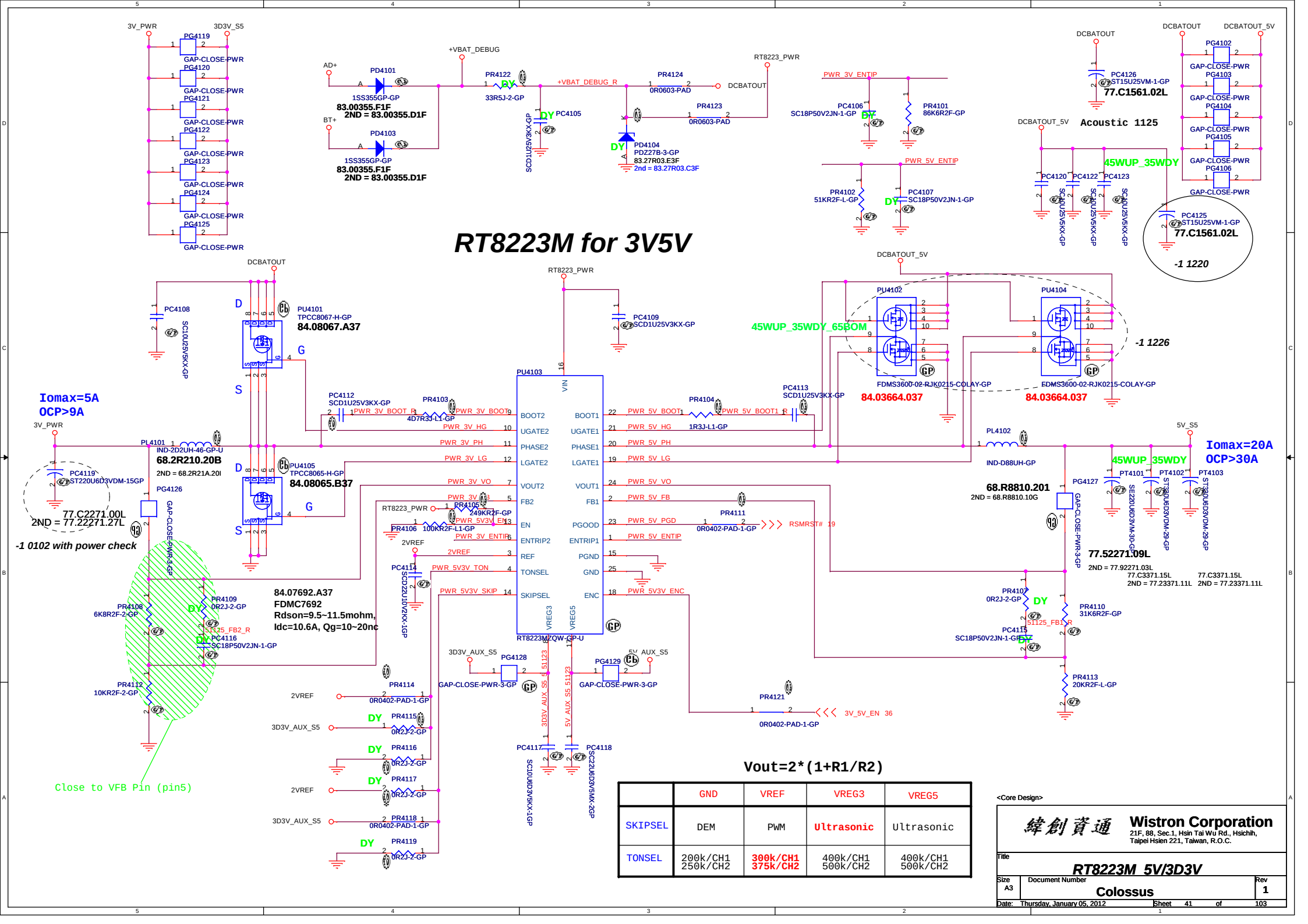
Title: Charger_BQ24738

Size: A2 | Document Number: Colossus | Rev: 1

Date: Thursday, January 05, 2012 | Sheet 40 of 103

RT8223M for 3V5V



Vout=2*(1+R1/R2)

	GND	VREF	VREG3	VREG5
SKIPSEL	DEM	PWM	**Ultrasonic**	Ultrasonic
TONSEL	200k/CH1 250k/CH2	**300k/CH1** **375k/CH2**	400k/CH1 500k/CH2	400k/CH1 500k/CH2

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8223M 5V/3D3V**

Size	Document Number	Rev
A3	Colossus	1

Date: Thursday, January 05, 2012 Sheet 41 of 103

SSID = CPU.Regulator

Volterra's suggestion:
The total output MLCC is 30x22uF for 3-PHASE VCC
The total output MLCC is 20x22uF+4x10uF for 2-PHASE VCCAXG

Boot Voltage	PR4265	PR4204
0V	887ohm	825ohm
1V	215ohm	191ohm

74.01318.B73
-1 1228 by power

<Core Design>

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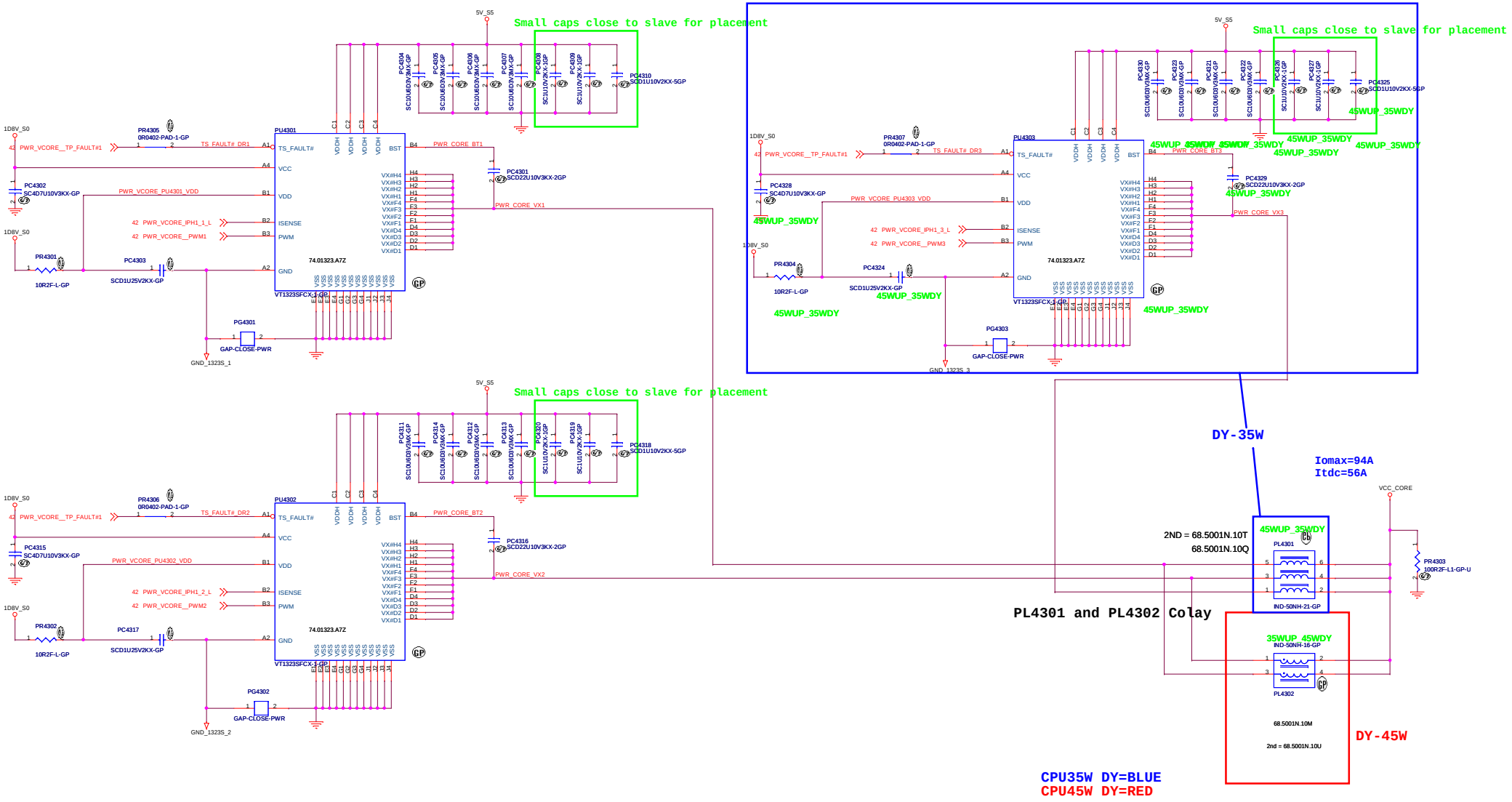
Title: VT1318_CPUCORE(1/3)

Size: A2 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 42 of 103



<Core Design>

Wistron Corporation
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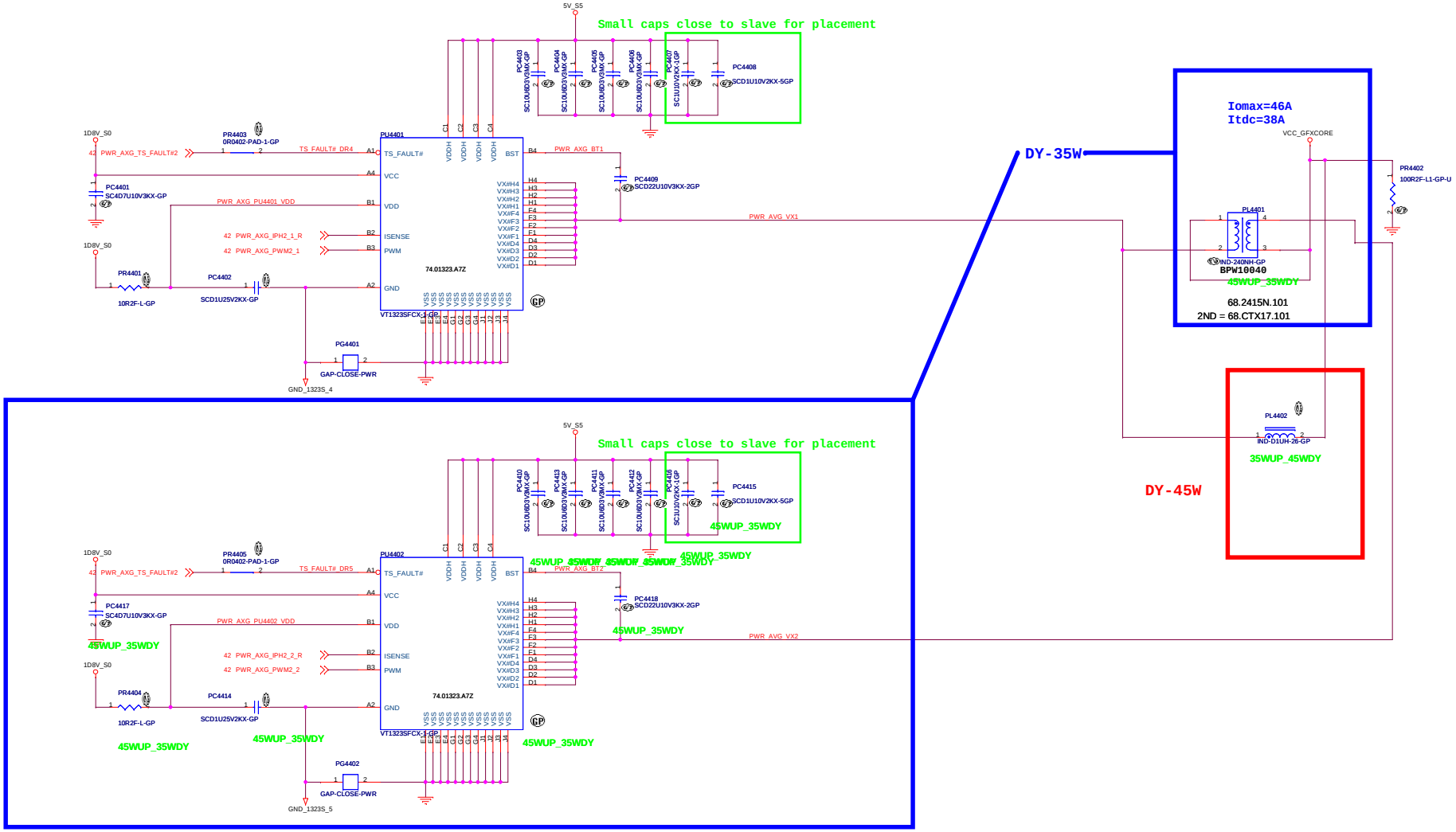
Title: VT1323_CPUCORE(2/3)

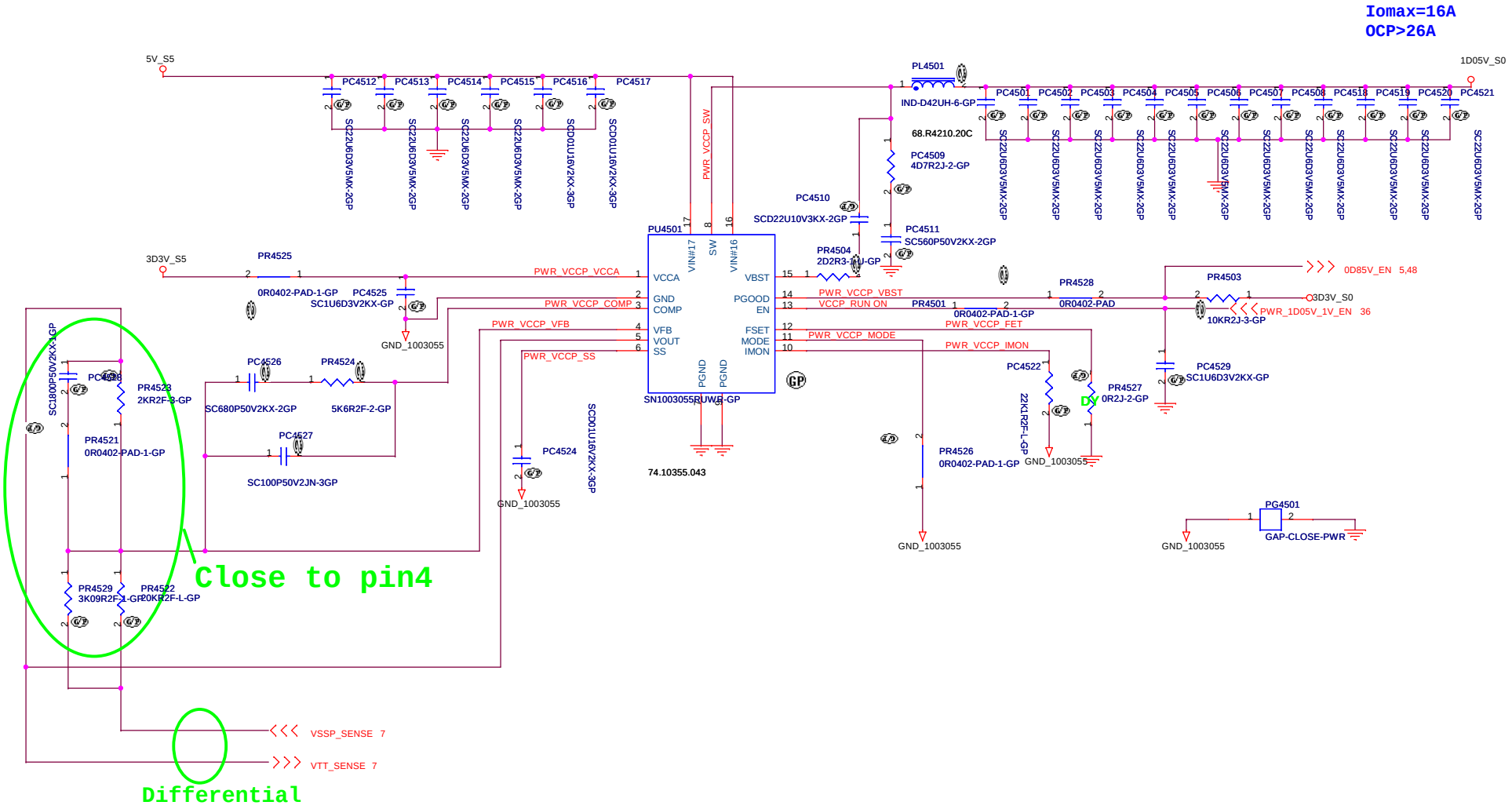
Size: A2 | Document Number: Colossus | Rev: 1

Date: Thursday, January 05, 2012 | Sheet 43 of 103



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	VT1323_CPUCORE(3/3)
Size: A2	Document Number: Colossus
Rev: 1	
Date: Wednesday, January 04, 2012	Sheet 44 of 103



<Variant Name>

緯創資通 **Wistron Corporation**
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Title: ***SN1003055RUWR***

Size	Document Number	Rev
A3	**Colossus**	1

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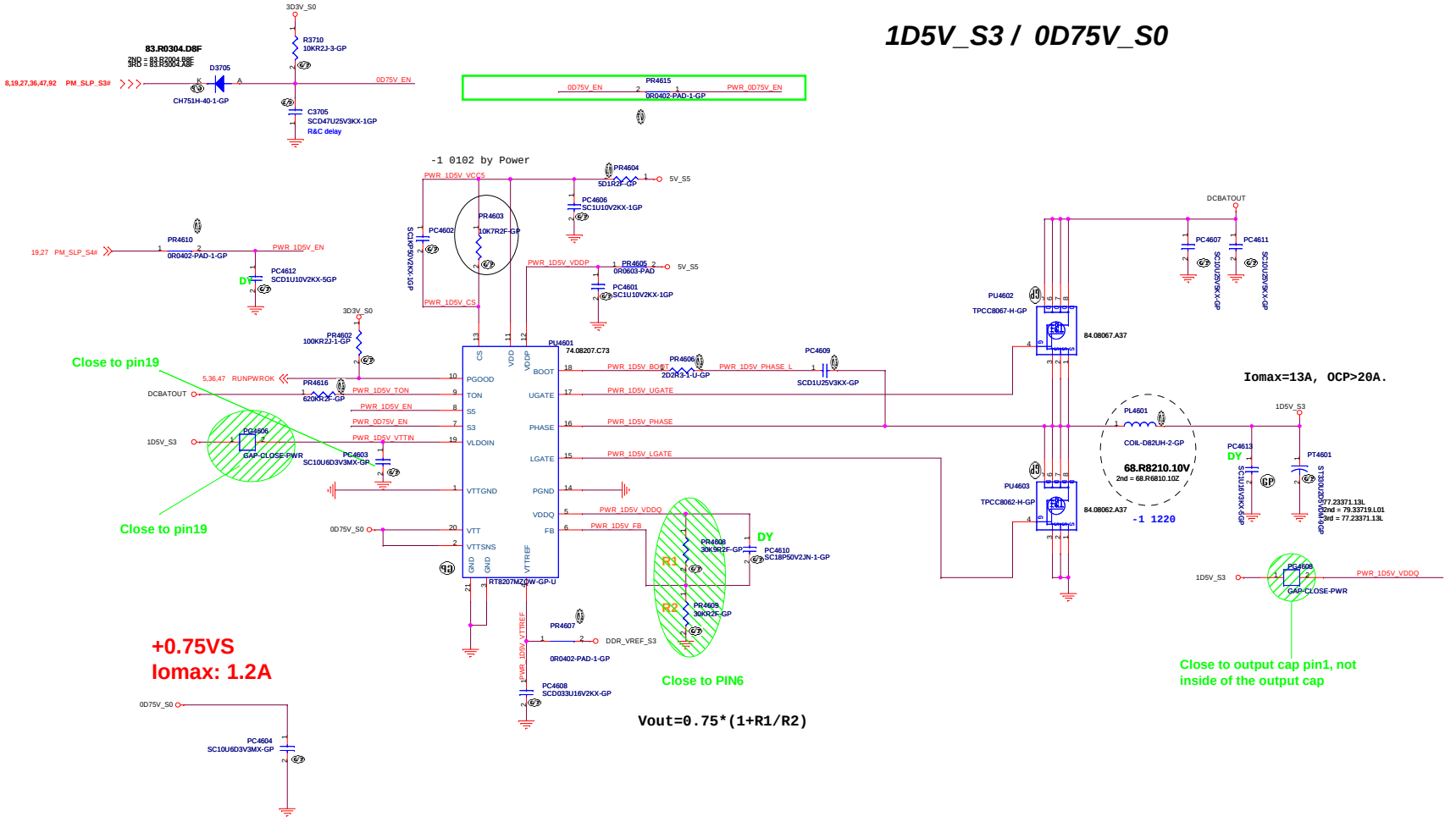
SSID = PWR.Plane.Regulator_1p5v0p75v

⑤

1D5V_S3 / 0D75V_S0



<Core Design>

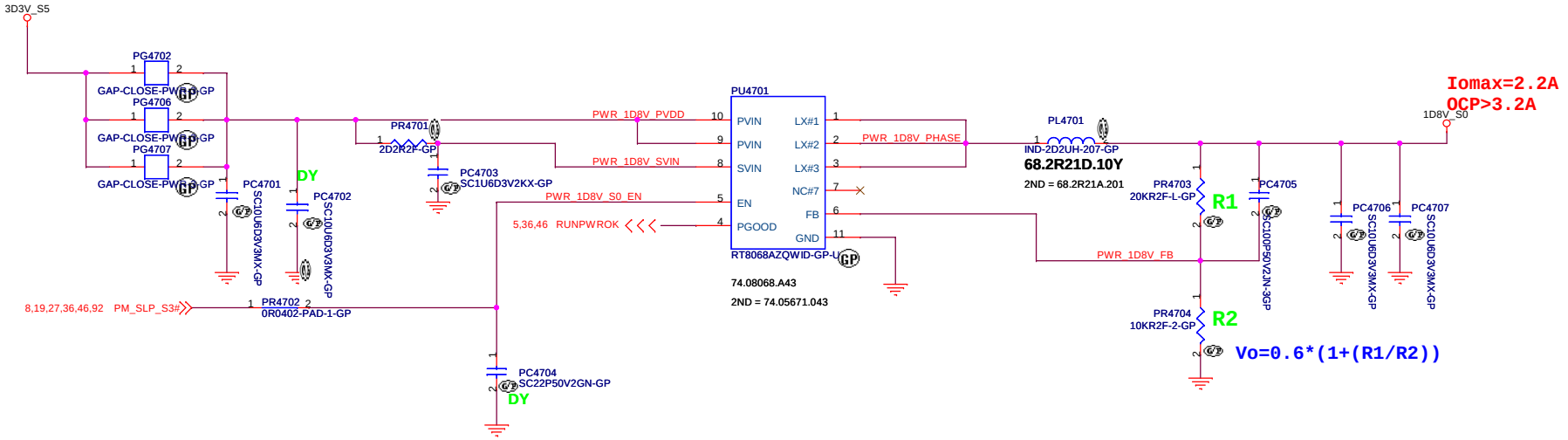
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8207MZ_1D5V & 0D75V

Size: A2 | Document Number: Colossus | Rev: 1

Date: Thursday, January 05, 2012 | Sheet 46 of 103

RT8068A for 1D8V_S0



<Core Design>

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Title	***RT8068A_1D8V***	
Size: A3	Document Number: **Colossus**	Rev: 1
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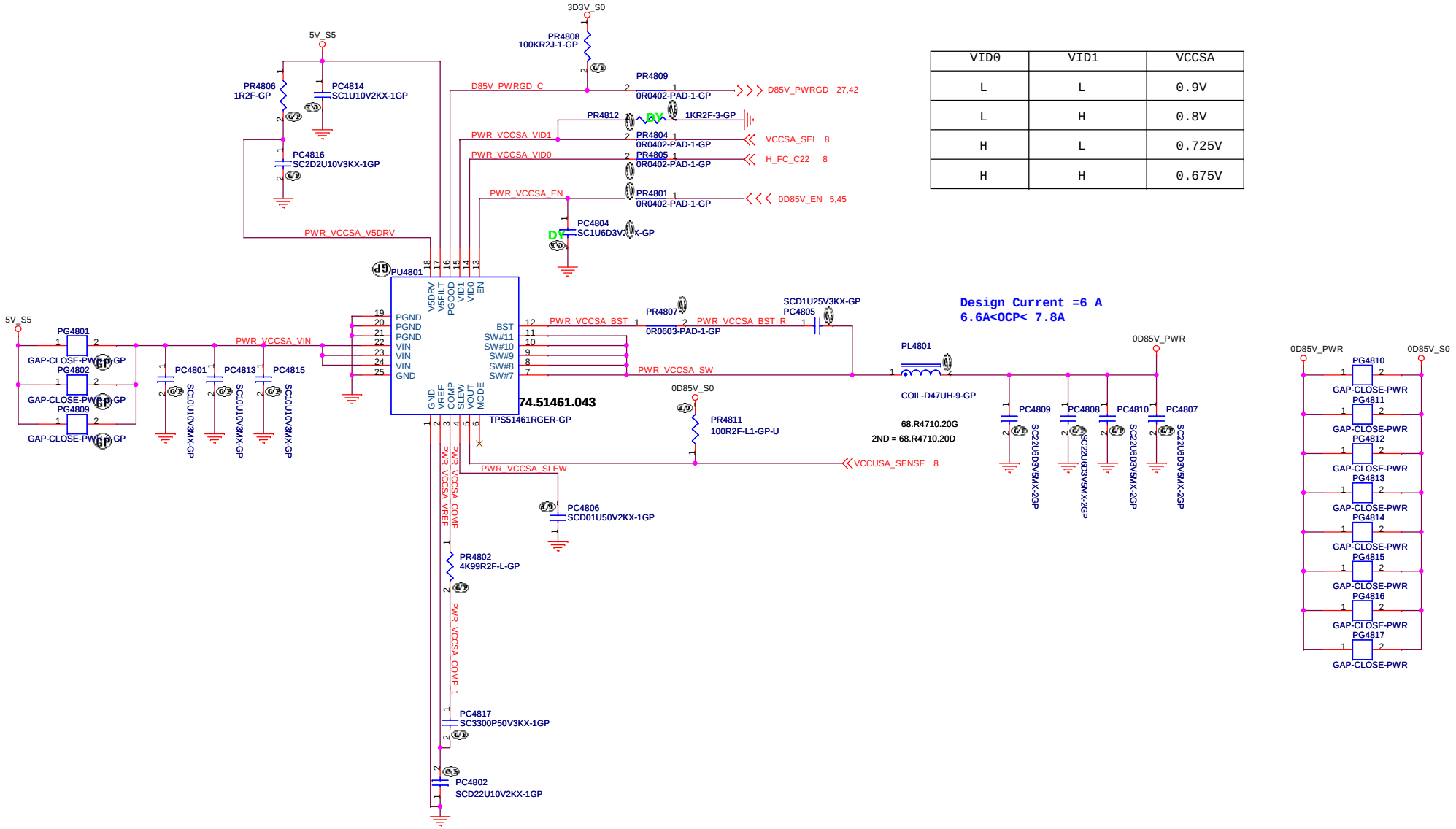
TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Core Design>

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Title: **TPS51461 VCCSA**

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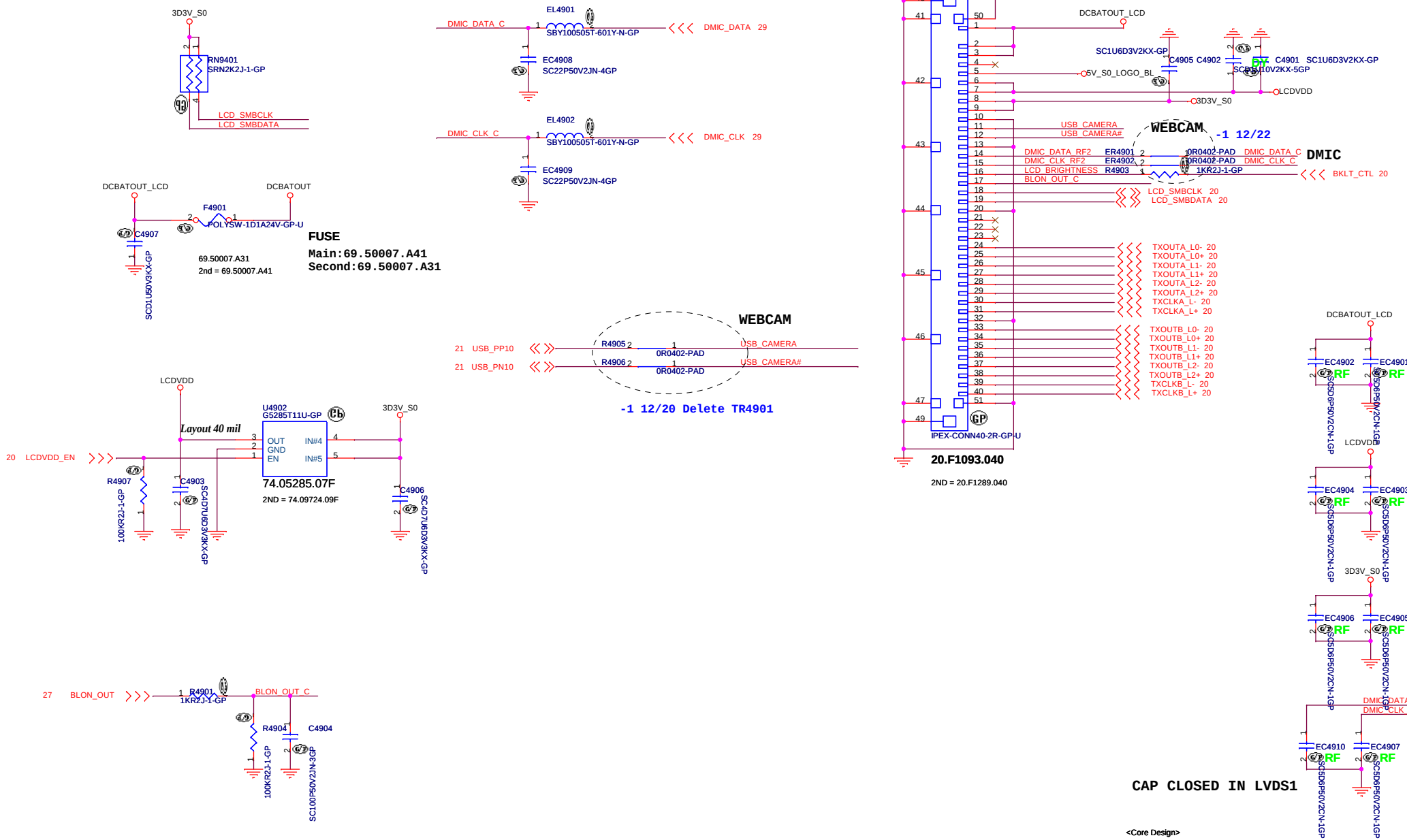
LVDS CONNECTOR
AUO B156HB01 V0

D_MIC by EMI

LVDS Impedance:90 ohm



<Core Design>

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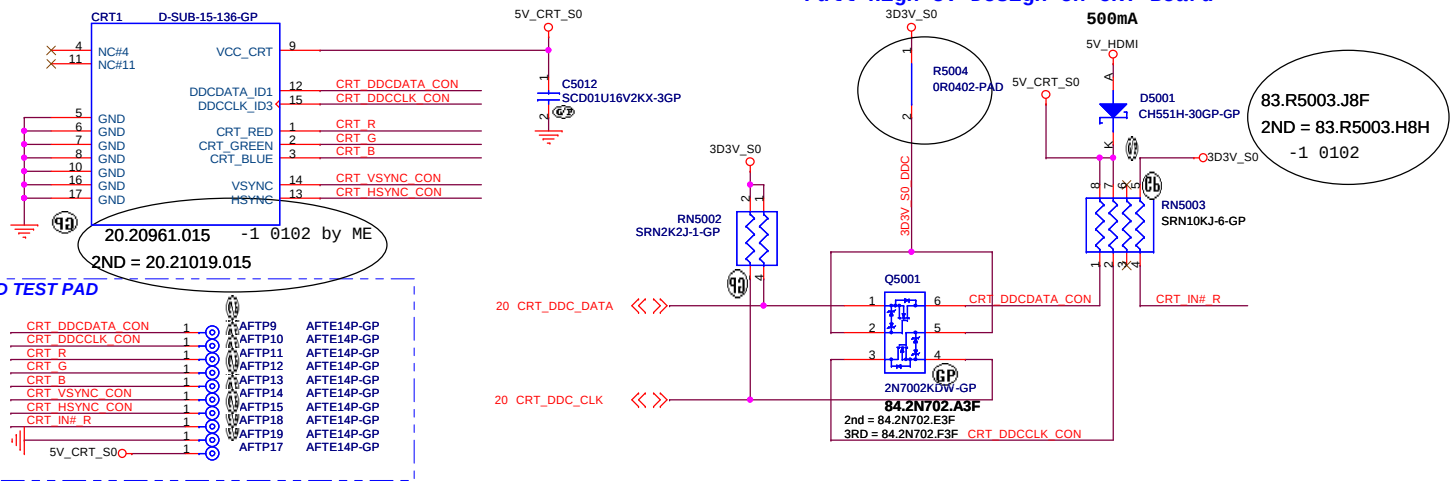
Title: LCD Connector

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 49 of 103

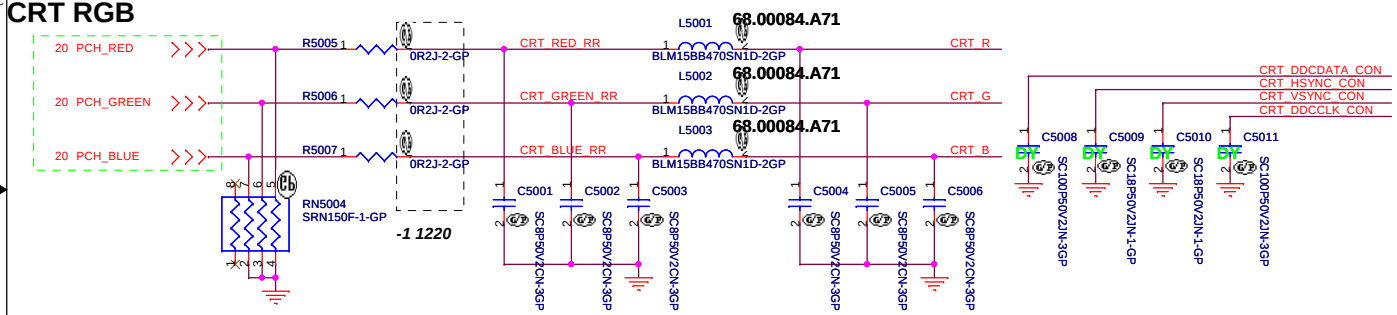
CRT Connector

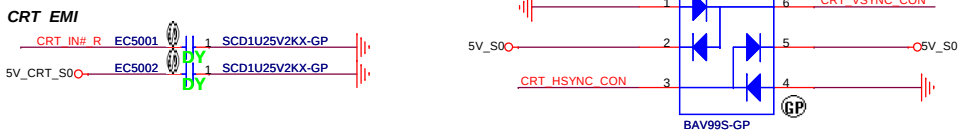


CRT DDCDATA & DDCCLK level shift

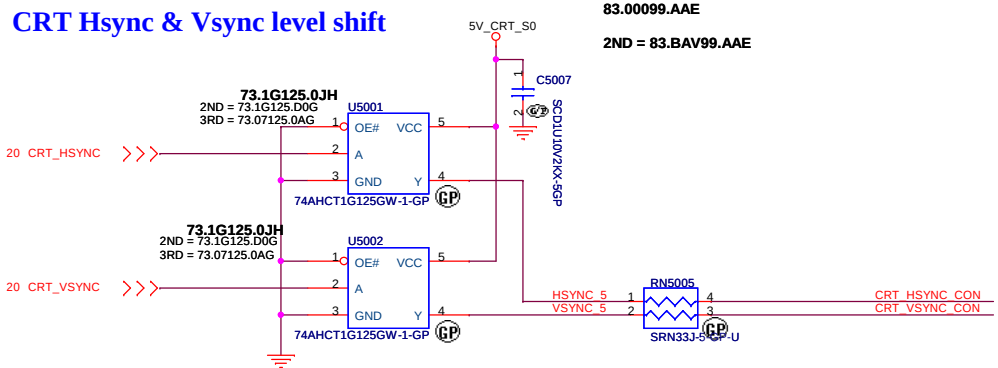
Pull High 5V Design on CRT Board

CRT RGB





CRT Hsync & Vsync level shift



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CRT_CONN		
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HDMI Level Shifter & CONNECTOR

HDMI_CLK_R_C — TR5101 FILTER-4P-49-GP — HDMI_CLK_R_C_CON
HDMI_CLK_R_C# — HDMI_CLK_R_C#_CON
69.10118.111

HDMI_DATA1_R_C — TR5103 FILTER-4P-49-GP — HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C# — HDMI_DATA1_R_C#_CON
69.10118.111

HDMI_DATA0_R_C — TR5102 FILTER-4P-49-GP — HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C# — HDMI_DATA0_R_C#_CON
69.10118.111

HDMI_DATA2_R_C — TR5104 FILTER-4P-49-GP — HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C# — HDMI_DATA2_R_C#_CON
69.10118.111

Close to GPU

HDMI DISCRETE/ UMA Co-lay

20 HDMI_CLK_R# / 20 HDMI_CLK_R — C5103 C5104 SCD1U10V2KX-5GP — HDMI_CLK_R_C# / HDMI_CLK_R_C
20 HDMI_DATA0_R# / 20 HDMI_DATA0_R — C5105 C5106 SCD1U10V2KX-5GP — HDMI_DATA0_R_C# / HDMI_DATA0_R_C
20 HDMI_DATA1_R# / 20 HDMI_DATA1_R — C5110 C5107 SCD1U10V2KX-5GP — HDMI_DATA1_R_C# / HDMI_DATA1_R_C
20 HDMI_DATA2_R# / 20 HDMI_DATA2_R — C5108 C5109 SCD1U10V2KX-5GP — HDMI_DATA2_R_C# / HDMI_DATA2_R_C

66.05136.08L=>680ohm for UMA
66.47136.A8L=>470ohm for GPU

Close to HDMI Connector

RN5106 SRN470J-5-GP
RN5107 SRN470J-5-GP
HDMI_PLL_GND

HDMI CONN

HDMI1 — SKT-HDMI21-4-GP
22.10296.711
2ND = 22.10296.751

HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
DDC_CLK_HDMI
DDC_DATA_HDMI

5V_HDMI — F5101 — 5V_S0
FUSE-1D1A6V-4GP-U
69.50007.691
2nd = 69.50007.771
3RD = 69.50007.C21

C5102 SCD1U10V2KX-5GP

HPD_HDMI_CON

3D3V_S0
R5111 150KR2J-L1-GP — HDMI_HPD_B
Q5102 PMBS3904-1-GP
84.03904.L06
2nd = 84.03904.P11
HDMI_HPD_E
R5128 0R0402-PAD — HDMI_PCH_DET 20
R5110 200KR2J-L1-GP DY
R5112 20KR2F-L-GP

5V_HDMI
AFTP95 AFTE14P-GP
AFTP94 AFTE14P-GP
HDMI_DATA2_R_C_CON — AFTP41 AFTE14P-GP
HDMI_DATA2_R_C#_CON — AFTP42 AFTE14P-GP
HDMI_DATA1_R_C_CON — AFTP37 AFTE14P-GP
HDMI_DATA1_R_C#_CON — AFTP38 AFTE14P-GP
HDMI_DATA0_R_C_CON — AFTP43 AFTE14P-GP
HDMI_DATA0_R_C#_CON — AFTP44 AFTE14P-GP
HDMI_CLK_R_C_CON — AFTP72 AFTE14P-GP
HDMI_CLK_R_C#_CON — AFTP81 AFTE14P-GP
DDC_CLK_HDMI — AFTP80 AFTE14P-GP
DDC_DATA_HDMI — AFTP93 AFTE14P-GP
HPD_HDMI_CON — AFTP130 AFTE14P-GP

5V_S0
D5102 BAW56-5-GP
83.00056.Q11
2nd = 83.00056.G11
3RD = 83.00056.K11
DDC_CLK_PH1
DDC_DATA_PH1
RN5101 SRN2K2J-1-GP

3D3V_S0
Q5104 ME2N7002DKW-G-GP
84.2N702.F3F
2ND = 84.2N702.E3F
DDC_CLK_Q — DDC_CLK_HDMI
DDC_DATA_Q — DDC_DATA_HDMI
RN5117 SRN0J-6-GP
20 PCH_HDMI_CLK / 20 PCH_HDMI_DATA

3D3V_S0
Q5106 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.W31
HDMI_PLL_GND

<Core Design>

Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

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Title: HDMI Level Shifter/Conn
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<Core Design>

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Title: ***Display Port***

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<Core Design>

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Title: ***Reserved***

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(Blanking)

<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 54 of 103

(Blanking)

<Core Design>

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Title: ***Reserved***

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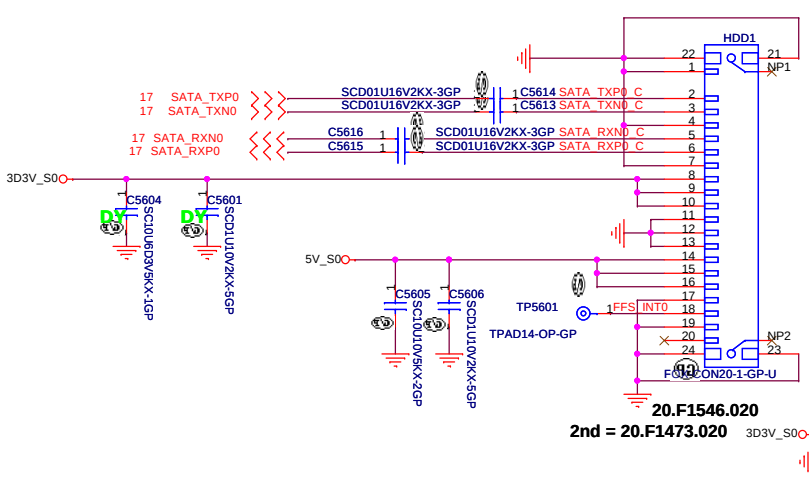
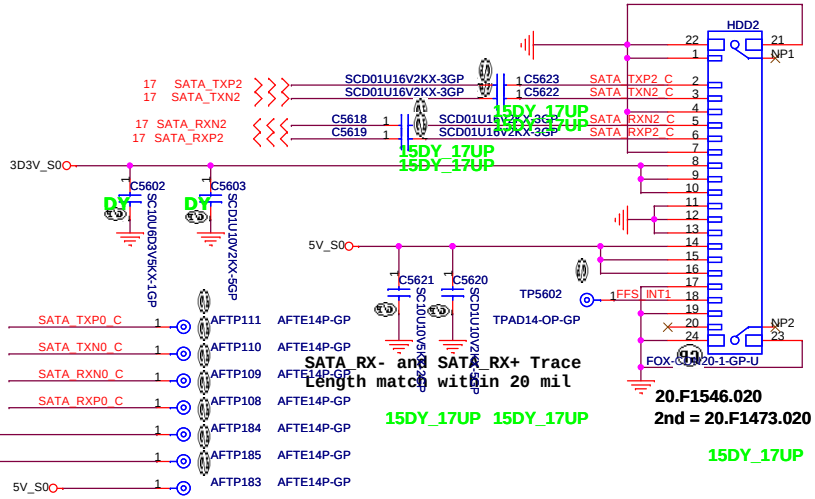
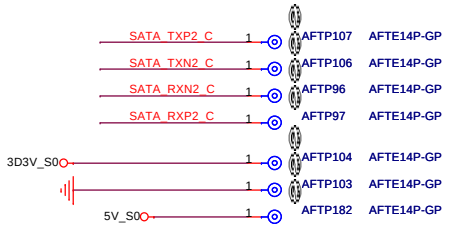
SATA HDD1 Connector

CHECK HDD conn model pin define_ME wire

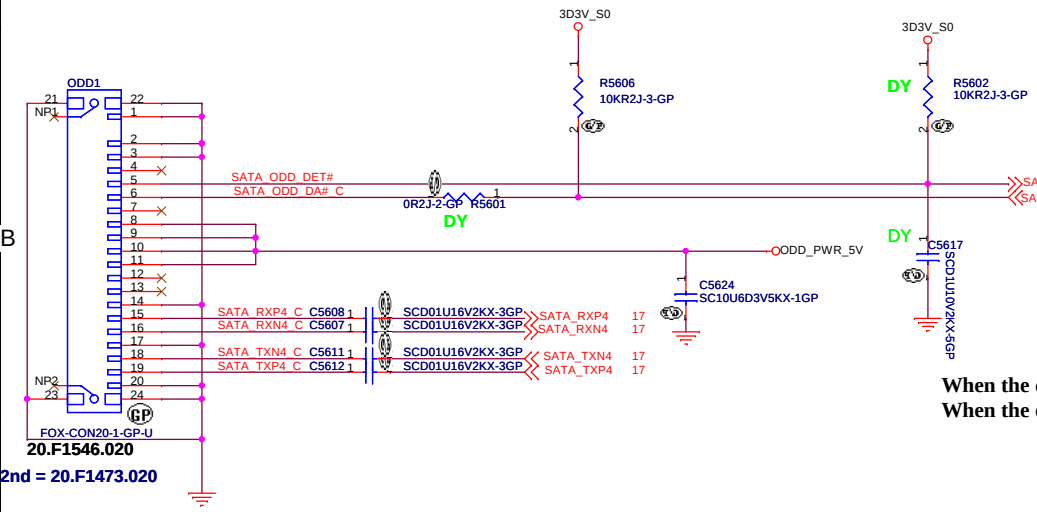


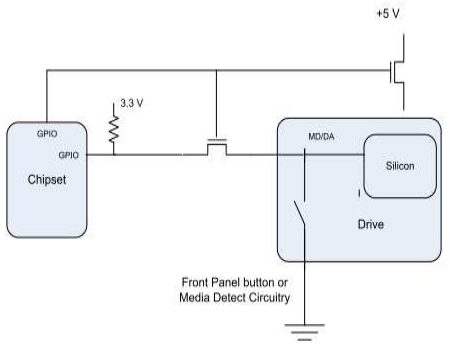
SATA HDD2 Connector





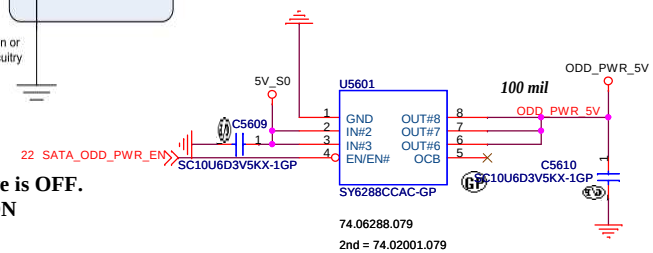
ODD Connector



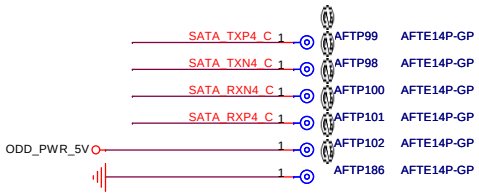


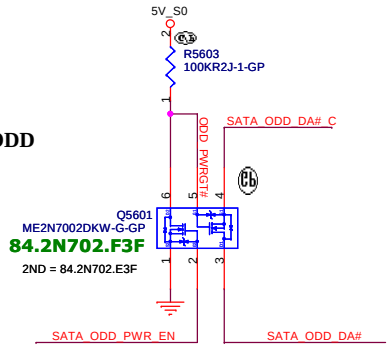
When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

SATA Zero Power ODD



SUPPORT ZERO SATA ODD





<Core Design>

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Title: HDD/ODD

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA

Size: A3 | Document Number: Colossus | Rev: 1

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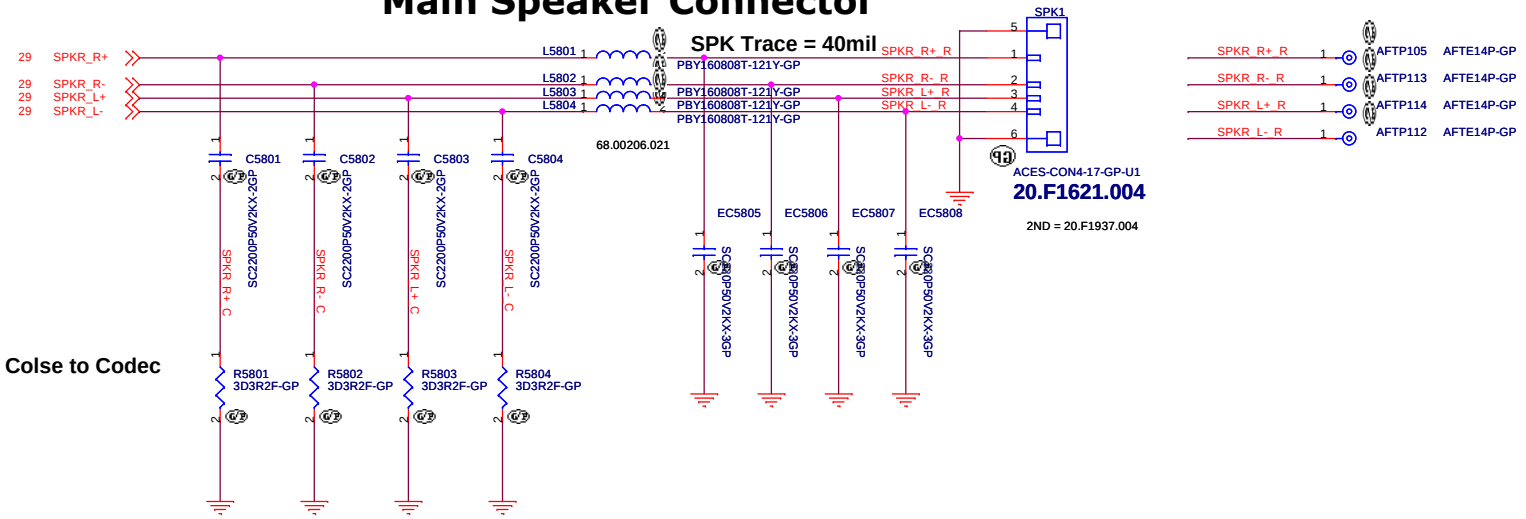
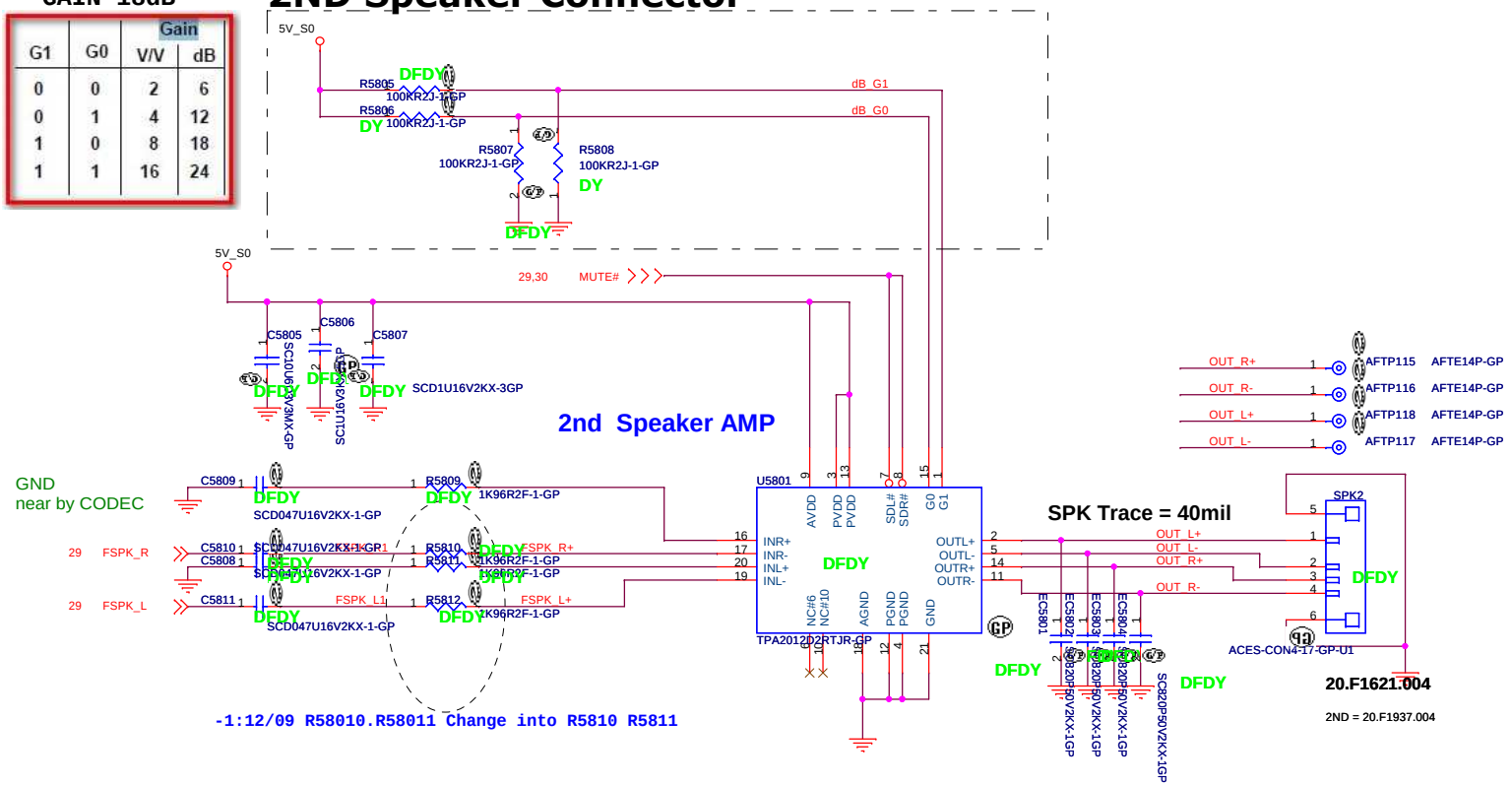
Main Speaker Connector



2ND Speaker Connector

GAIN 18dB

Gain			
G1	G0	V/V	dB
0	0	2	6
0	1	4	12
1	0	8	18
1	1	16	24



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Taipei Hsien 221, Taiwan, R.O.C.

<Core Design>

Title: **SPEAKER CONN**

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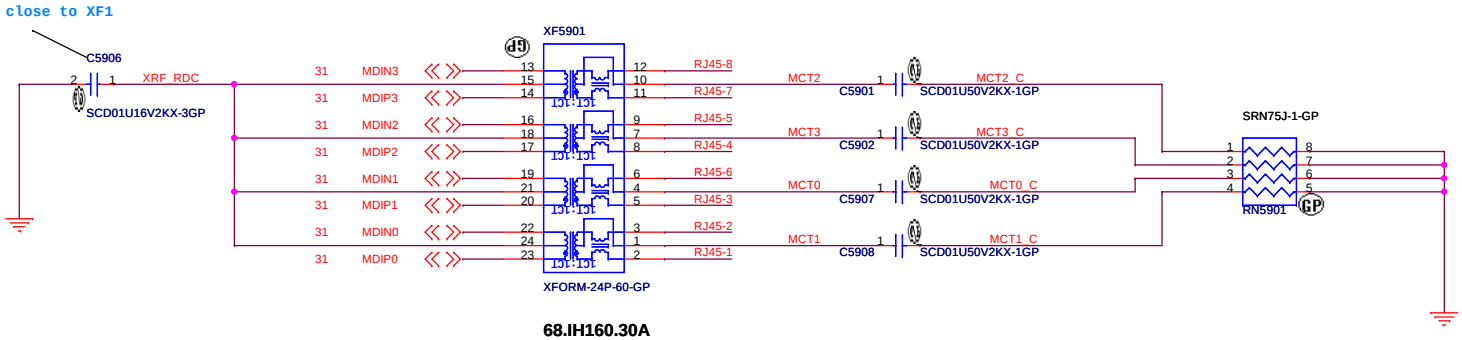
White LED for connectivity and Amber LED for activity located on RJ-45 connector

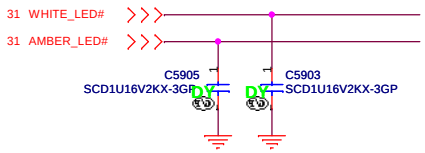
close to XF1



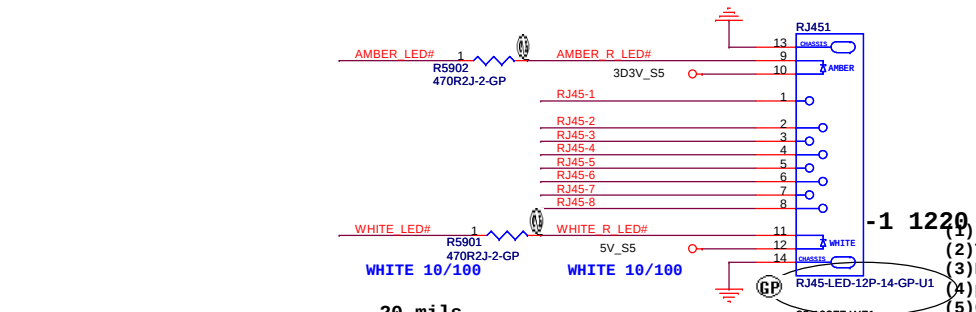
68.IH160.30A

2ND = 68.89246.301

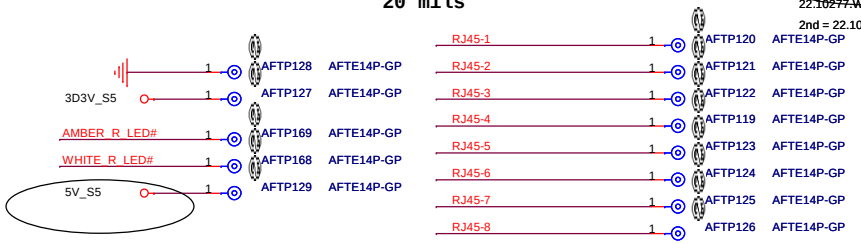
AMBER = LAN ACK



RJ451



20 mils



-1 1220

(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat, except RJ-45 moat.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

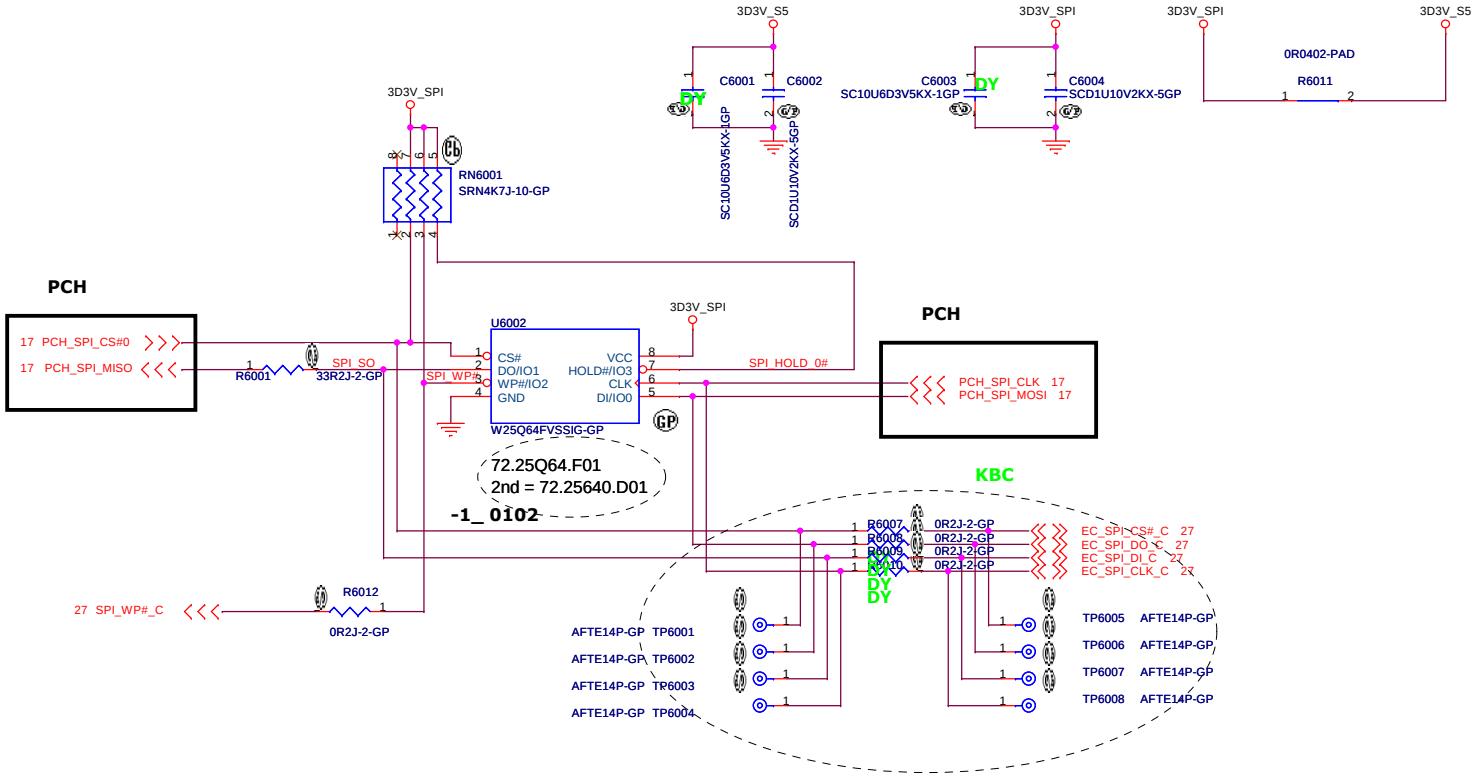
Title: RJ45+Transformer

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 59 of 103

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH & KBC



Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

-1 1223 Reversed TP6001~TP6008 / R6007~R6010 is DY
1, 測試點請使用14mil, 測試之間距離75mil以上。
2，測試點必須在Top層.

<Core Design>

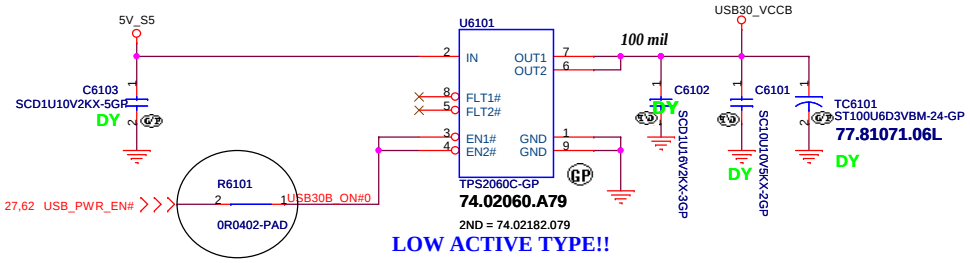
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash		
Size: A3	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 60 of 103	

RESERVED USB 2.0/3.0 BD

SSID = USB

Power switcher Low active

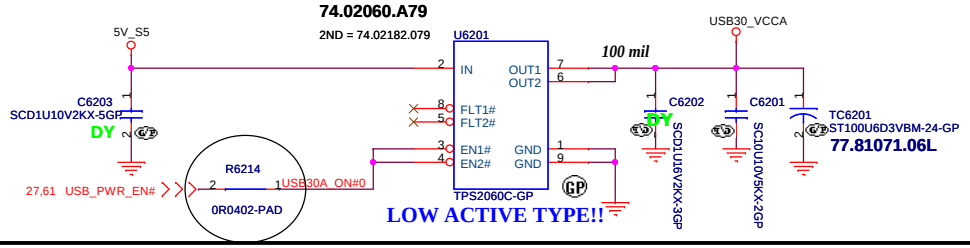


LOW ACTIVE TYPE!!

<Core Design>

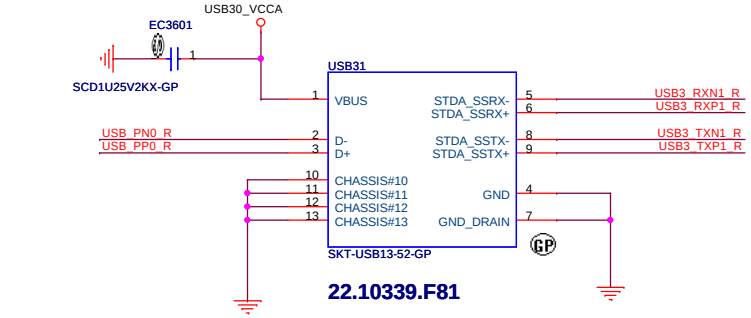
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: *USB Power SW_USB IO*	
Size: A3	Document Number: Colossus — Rev: 1
Date: Wednesday, January 04, 2012	Sheet 61 of 103

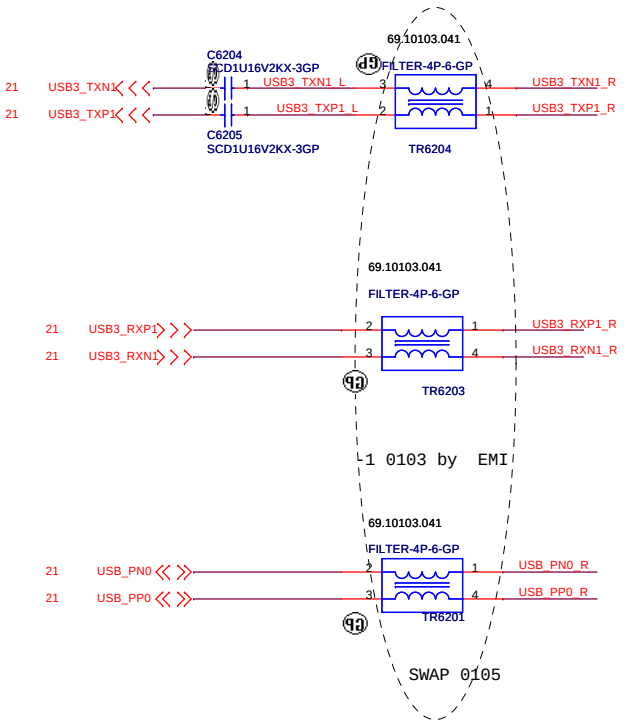
Power switcher Low active



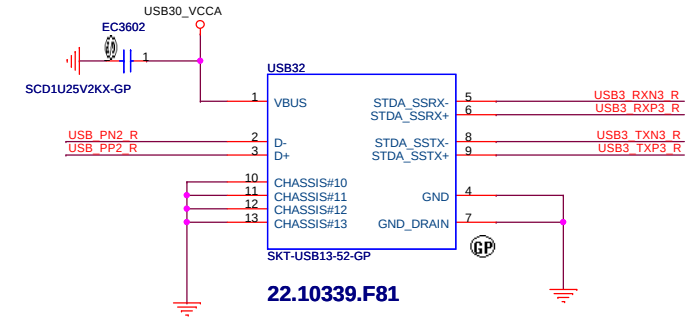
USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

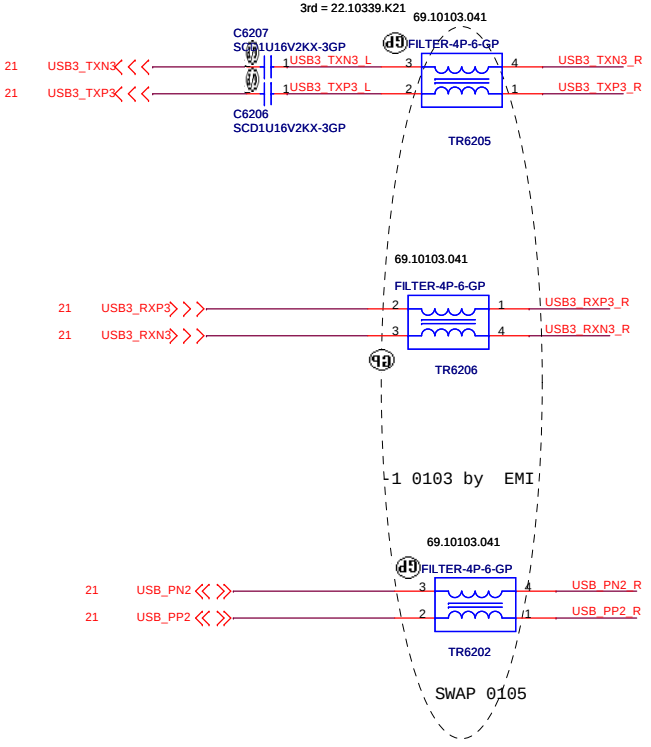
USB3_1

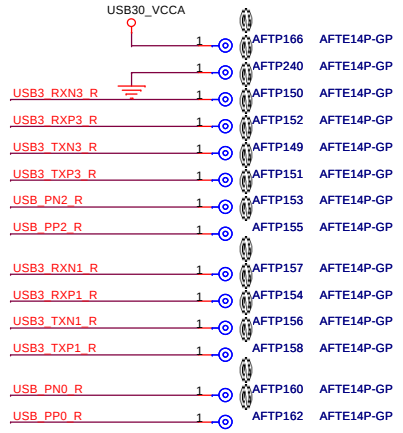




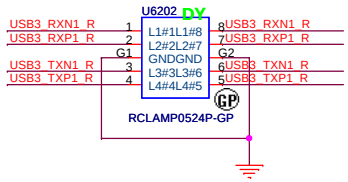
USB3_2



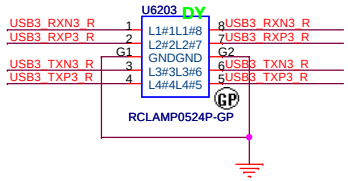




Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB3.0**

Size	Document Number	Rev
A3	Colossus	1

Date: Thursday, January 05, 2012 Sheet 62 of 103

(Blanking)

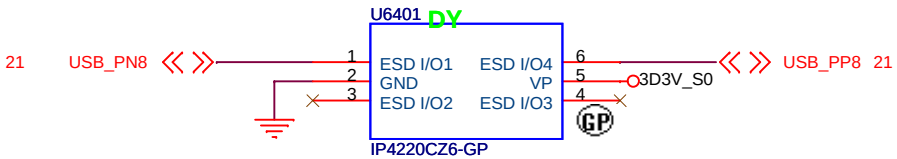
<Variant Name>

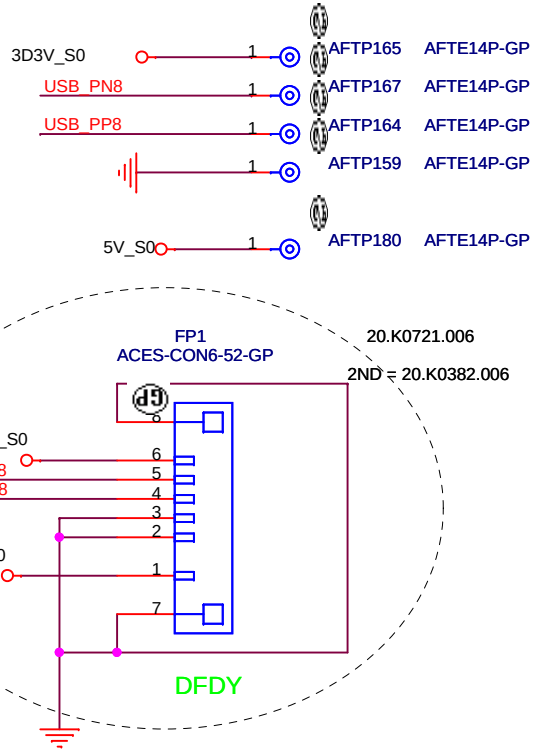
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Resered(Bluetooth)*

Size	Document Number	Rev
A3	Colossus	1

Finger Printer





-1 12/23 FP1 change source

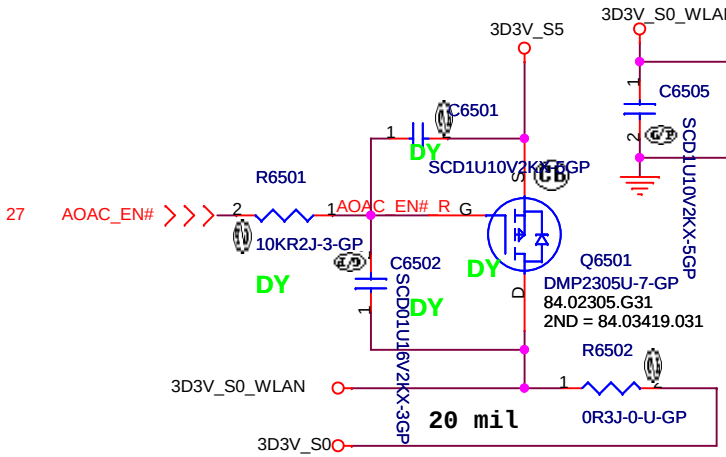
<Core Design>

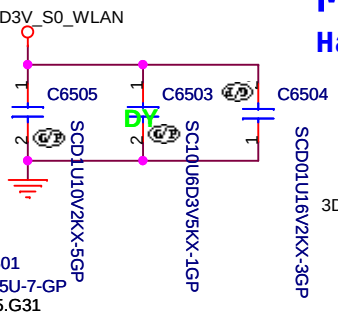
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Finger Print Conn*		
Size: A4	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 64 of 103	

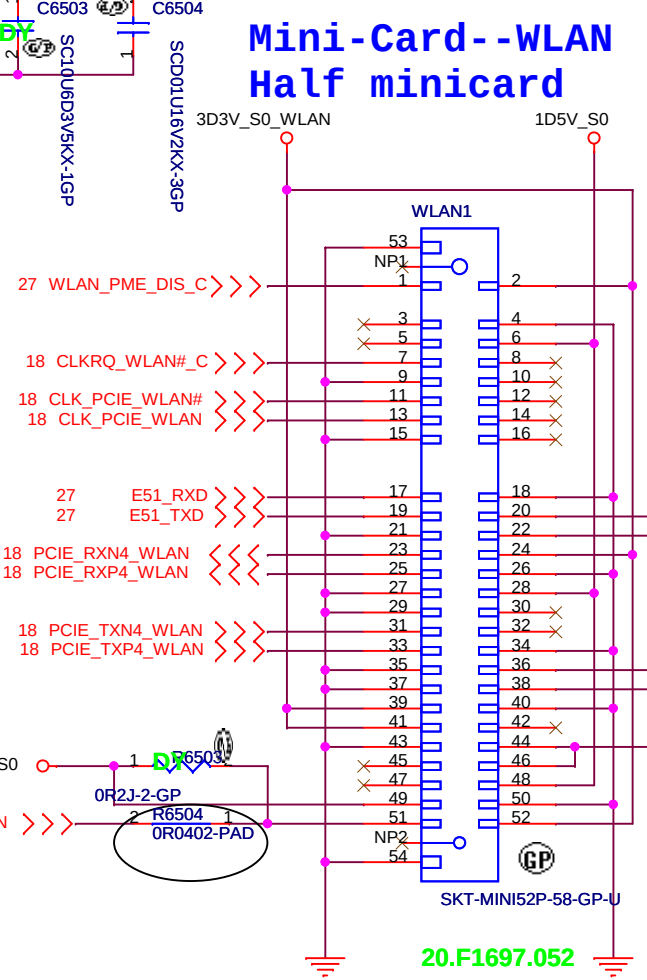
SSID = Wireless

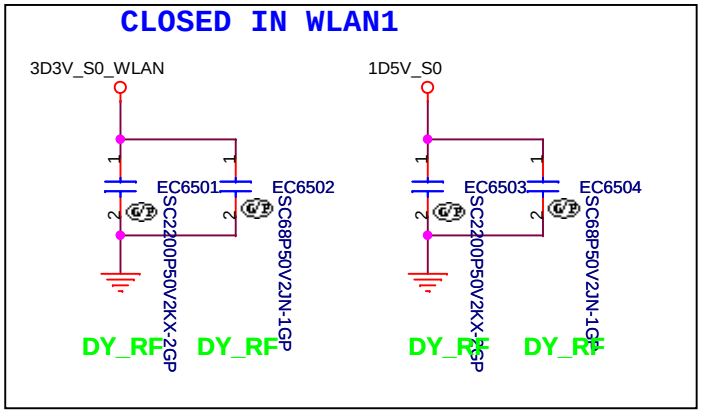
Mini-Card--WLAN

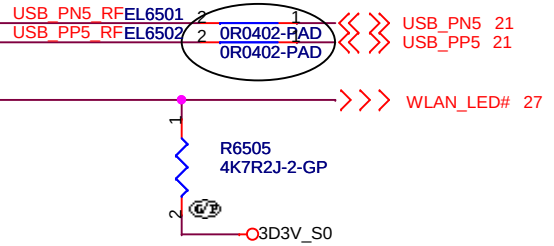
Half minicard











51	BT_ DISABLE_L (low active to disable Bluetooth)

Pin	Active	Function
5	High(3V)	GPIO/BT_WAKE
20	High(3V)	WIFI_Enable
47	Reserved	BT_PRISEL(coexistence)
51	Reserved	BTCX_STAT(coexistence)

WIFI_RF_EN 27
PLT_RST# 5,21,27,31,32,36,71,82,83,103

1-1 1226 del TR6501

<Core Design>

677869-FM8

1st	677869-FM8
2nd	677869-AM8
3rd	677869-BM8
4th	677869-LM8

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINICARD(WLAN+Bluetooth)/CONN***

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 65 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

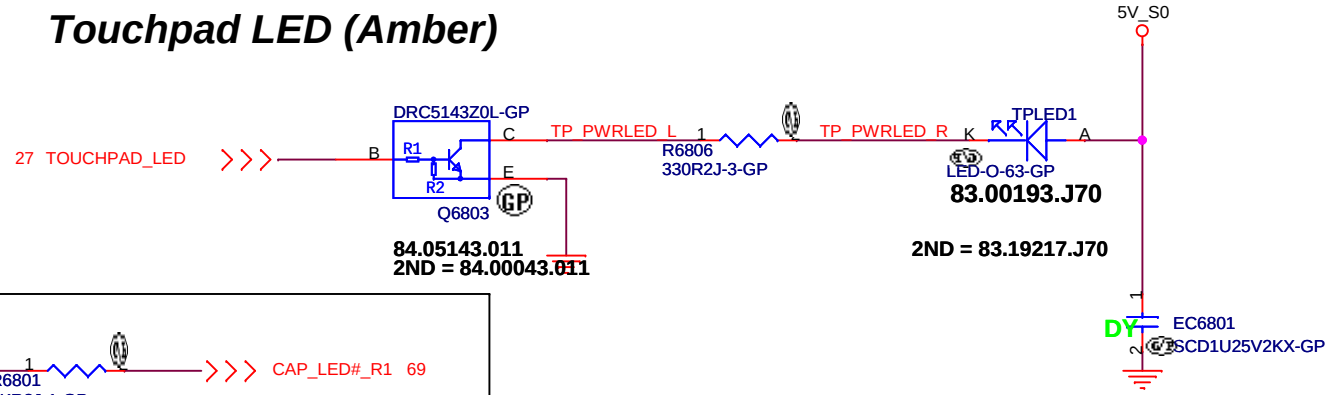
Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

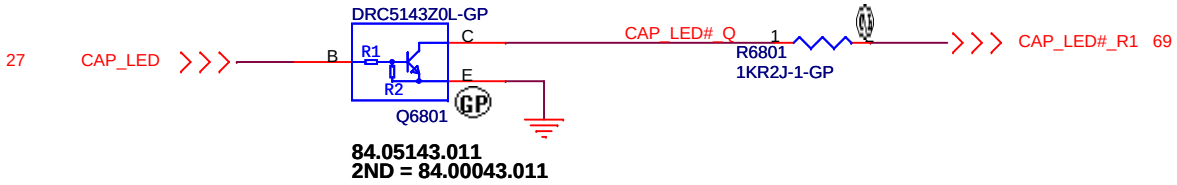
SSID = User.Interface

On Keyboard LEDs

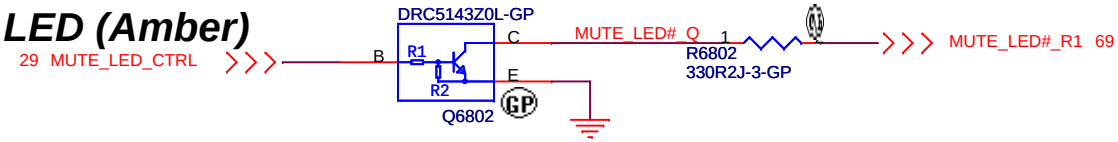
Touchpad LED (Amber)



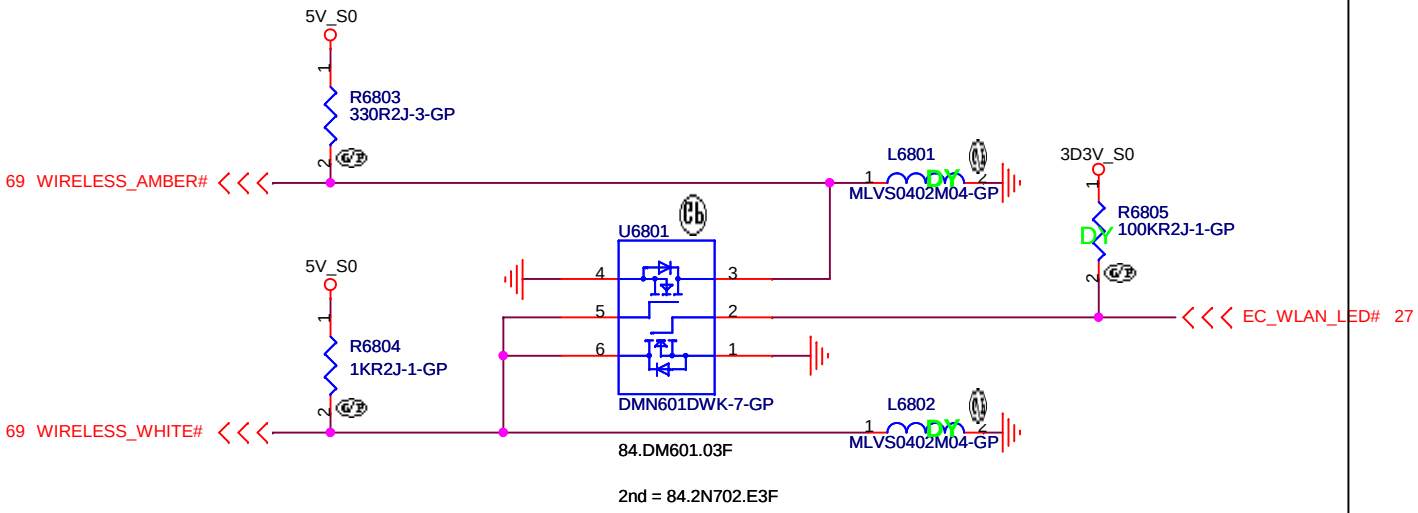
Cap locks LED (White)



Mute LED (Amber)



Wireless LED (White-On, Amber-Off)



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

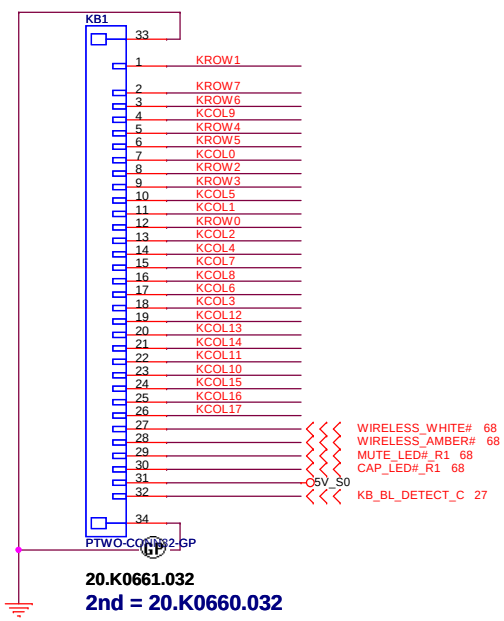
Title: LED Bard/Power Button

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 68 of 103

SSID = KBC

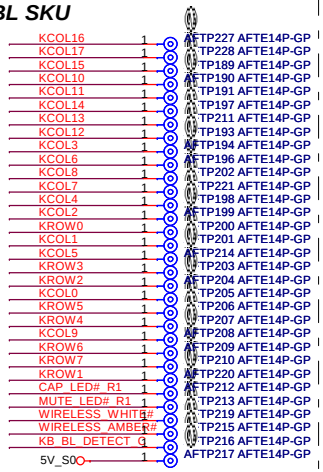
Internal KeyBoard Connector



20.K0661.032
2nd = 20.K0660.032
3rd = 20.K0676.032

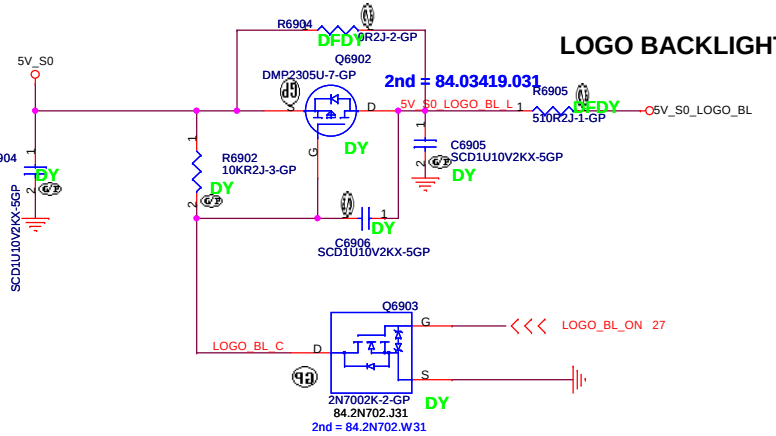
KROW[0..7] 27
KCOL[0..17] 27

KB_BL_DETECT
HIGH = BL SKU
LOW = NON-BL SKU

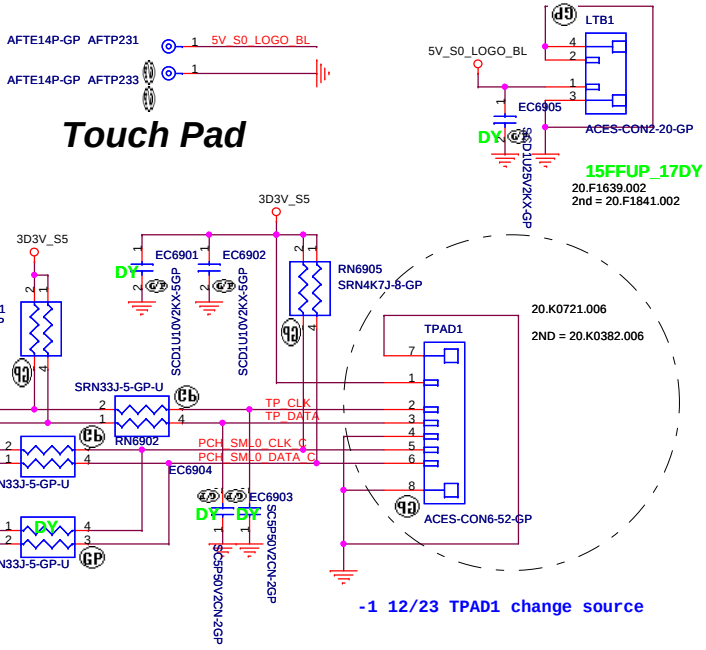


A Cover Logo Backlight

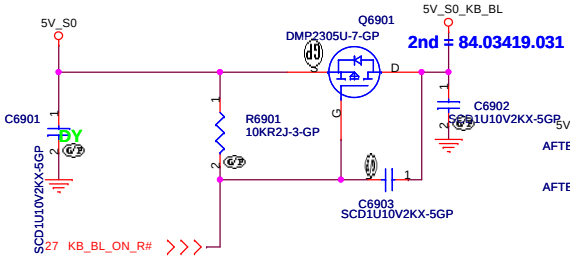
LOGO BACKLIGHT(LVDS1)

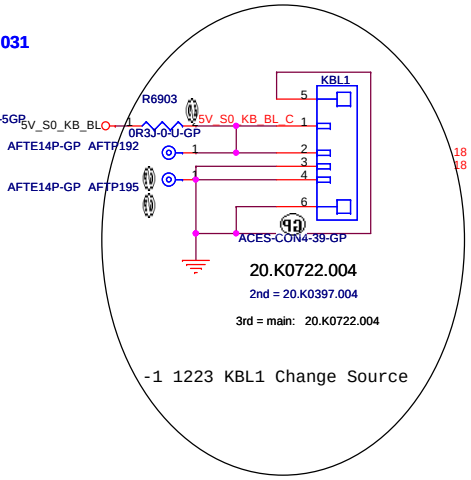


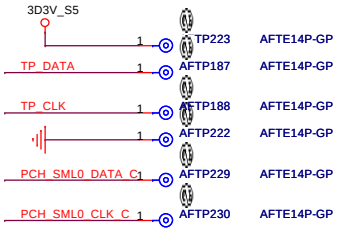
Touch Pad



Internal KeyBoard Backlight Connector







<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Key Board/Touch Pad*

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 69 of 103

(Hall sensor at Power BD)

<Core Design>

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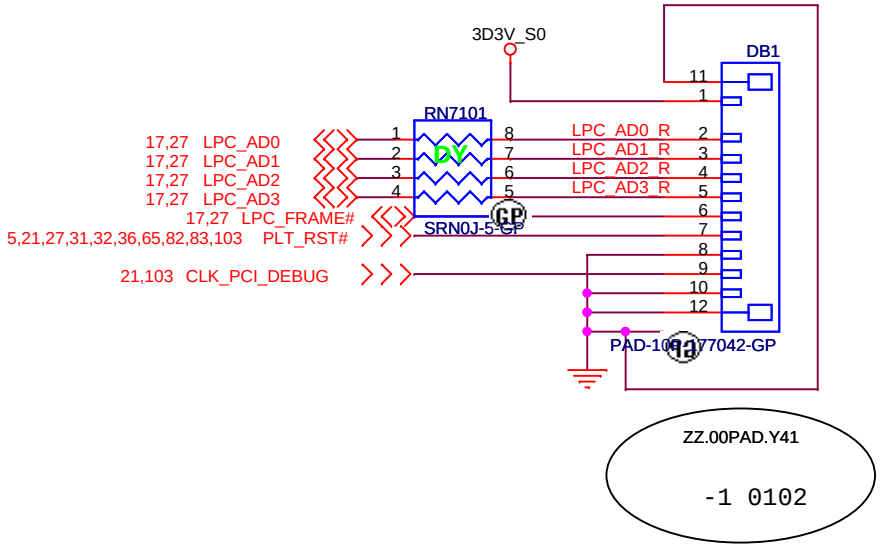
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 70 of 103

DEBUG BD for Factory Test



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***Dubug connector***		
Size: A4	Document Number: **Colossus**	Rev: **1**
Date: Wednesday, January 04, 2012	Sheet 71 of 103	

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 72 of 103

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<Core Design>

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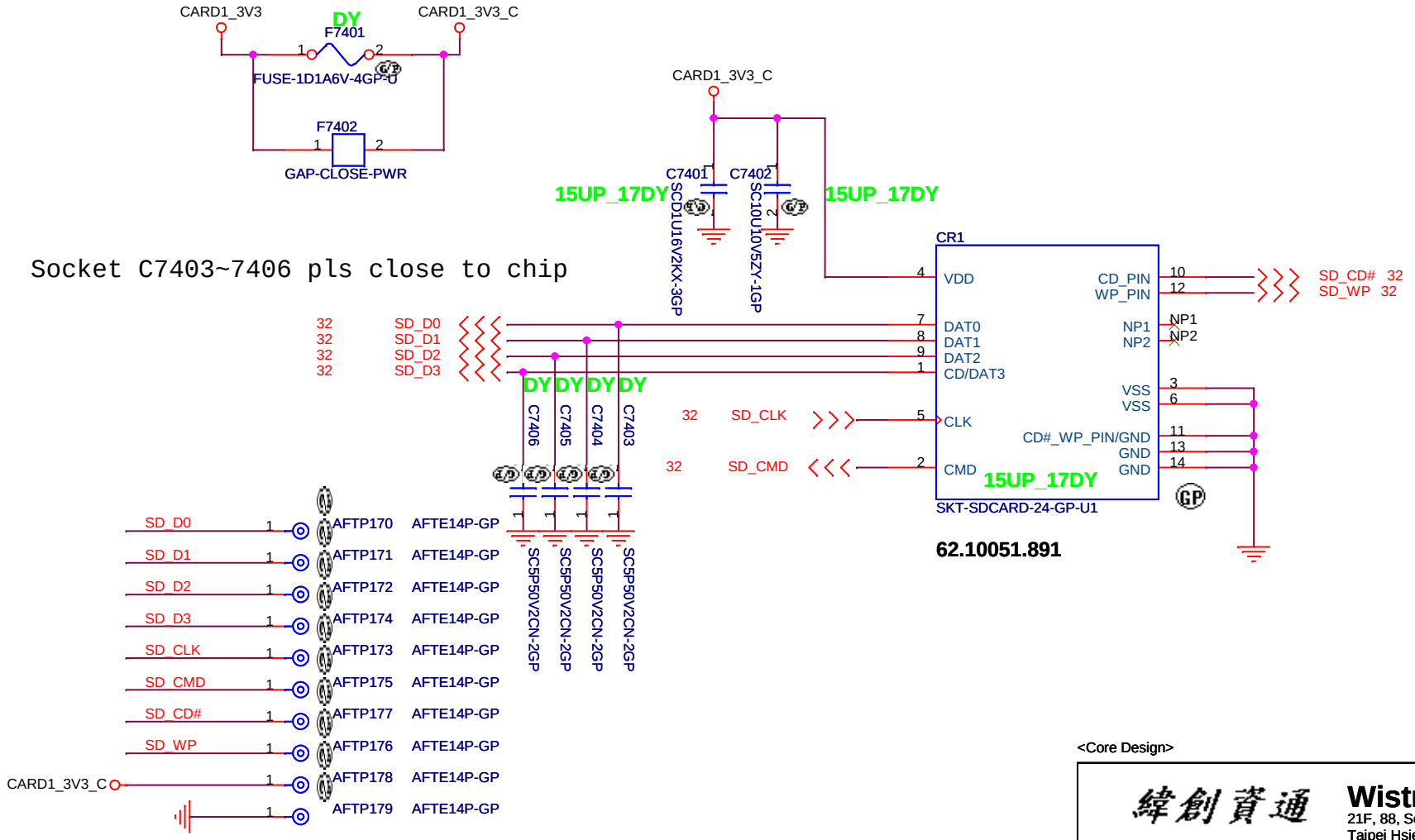
Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 73 of 103

2 IN1 CARD-READER (SD/MMC)



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CARD Reader CONN***

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 74 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Express Card*

Size	Document Number	Rev
A3	Colossus	1

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 76 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TPM*		
Size: A3	Document Number: Colossus	Rev: 1
Date: Monday, December 26, 2011	Sheet 77 of 103	

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<Core Design>

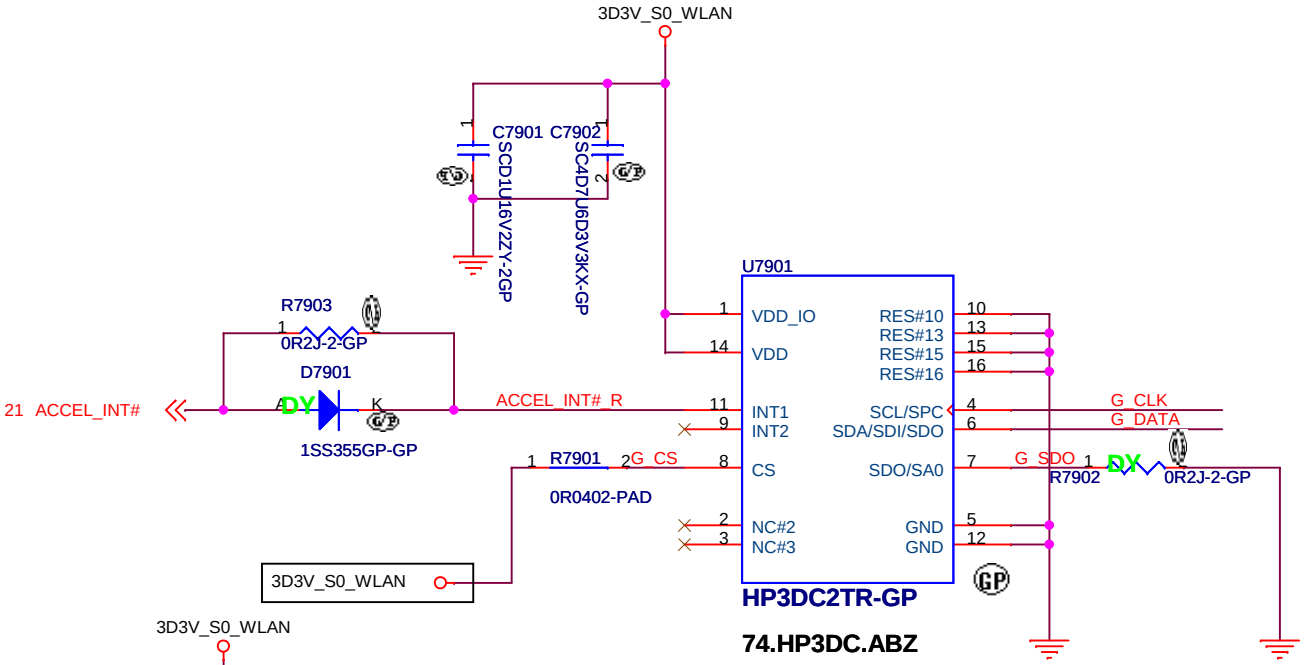
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

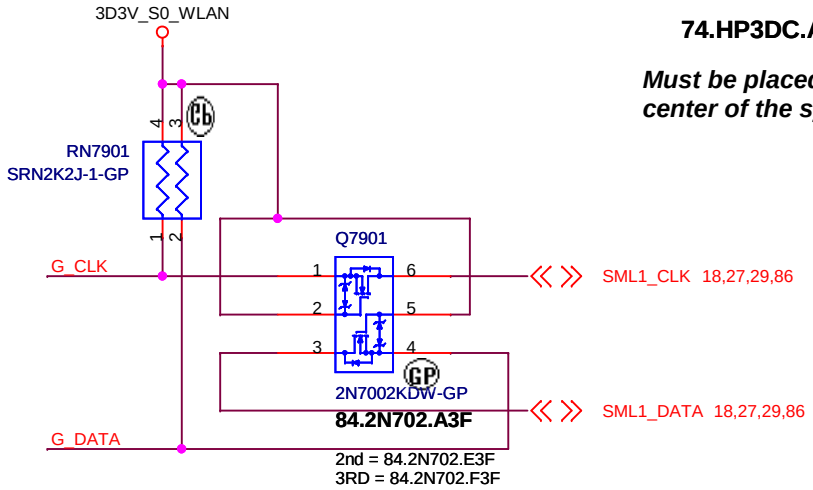
Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 78 of 103

ACCELEROMETER





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ACCELEROMETER

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 79 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 80 of 103

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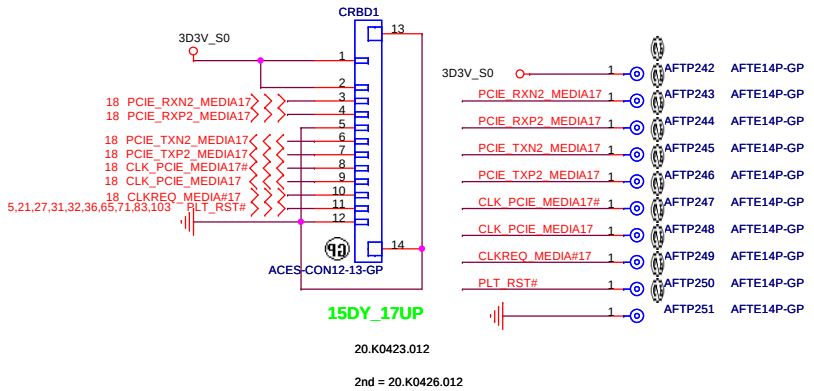
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

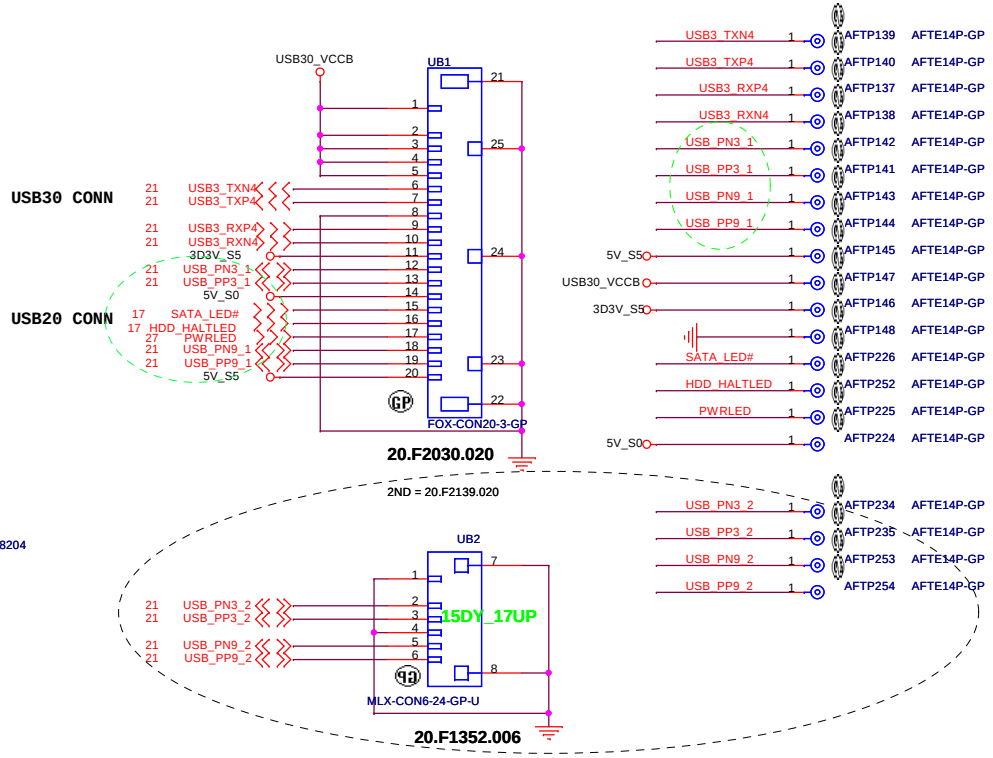
Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

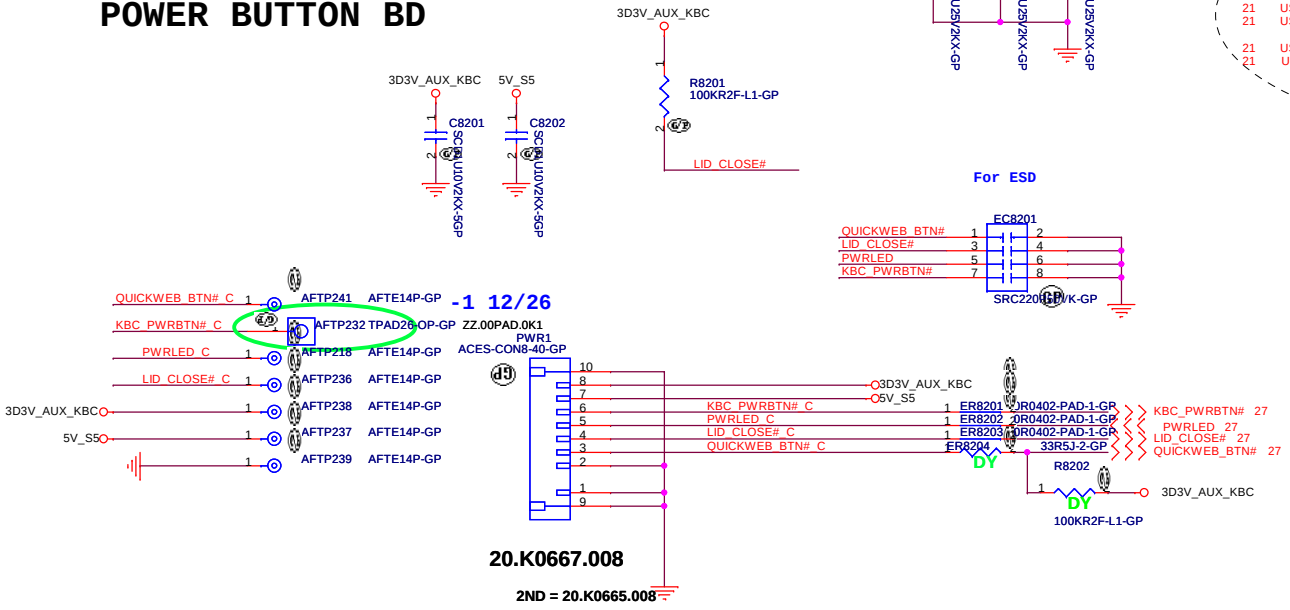
Card Reader BD 15"=DY 17"=PHASE IN



USB BD(USB3.0*1+USB2.0*1)



POWER BUTTON BD



TOUCHPAD BD PAGE 69

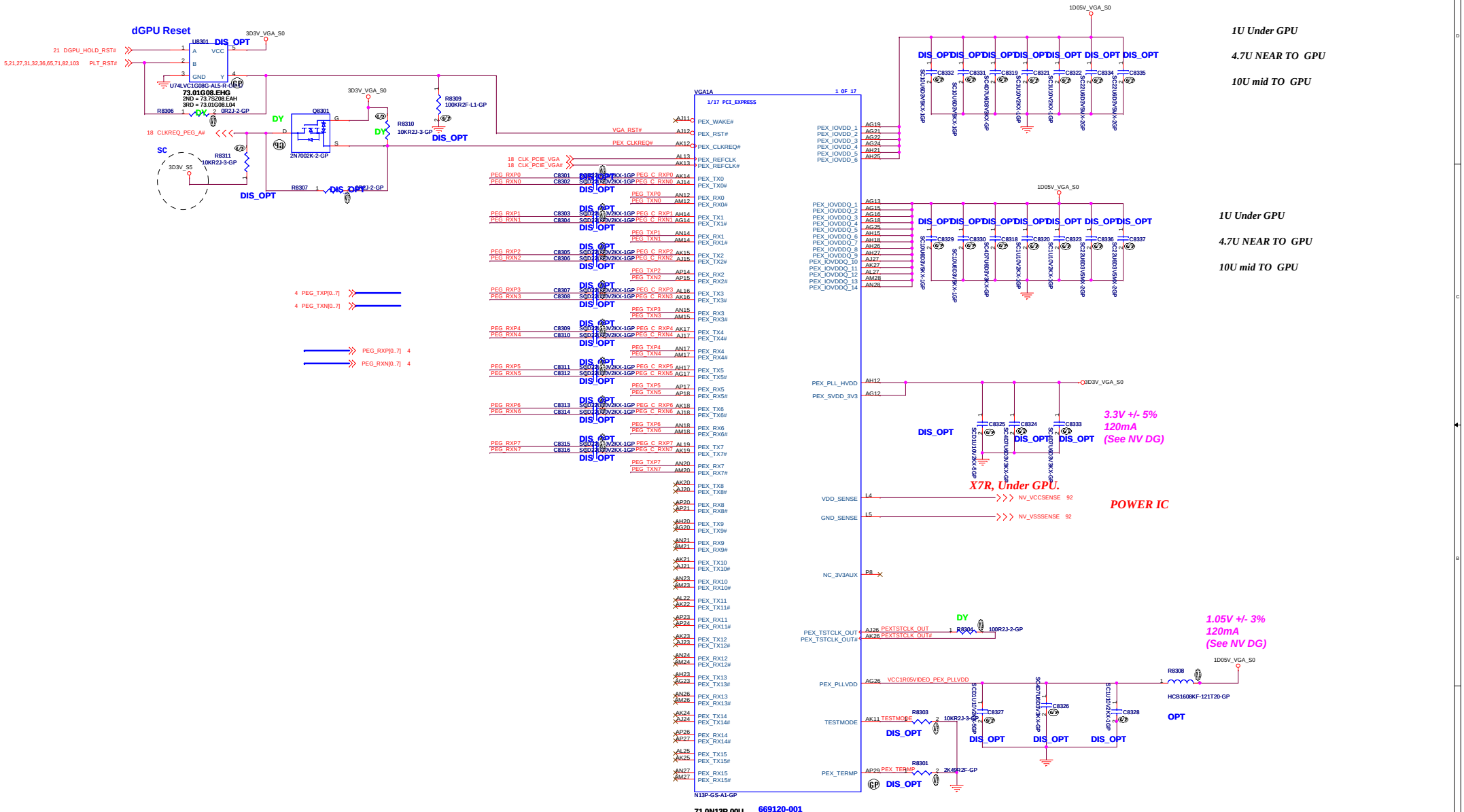
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 82 of 103



<Variant Name>

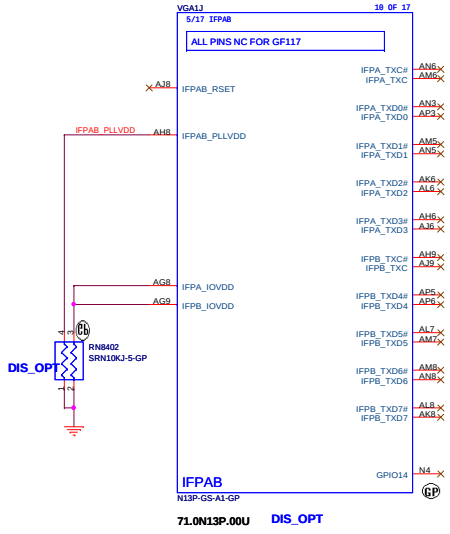
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

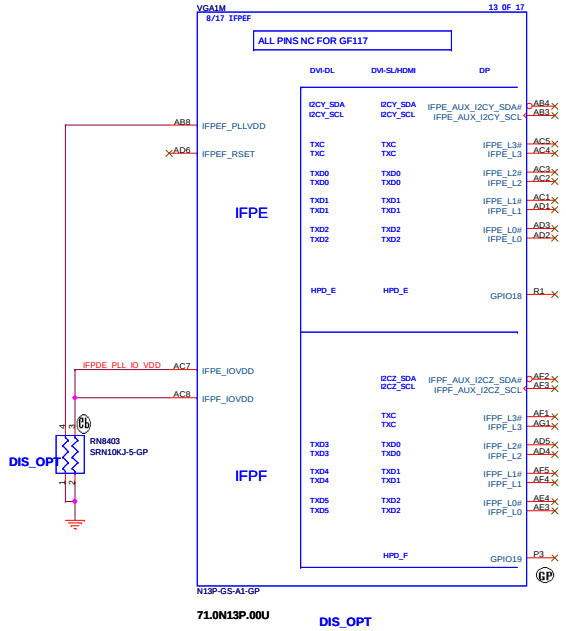
Size	Document Number	Rev
A2	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 83 of 103

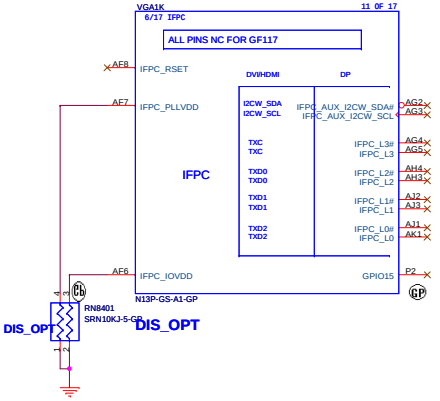
LVDS Interface



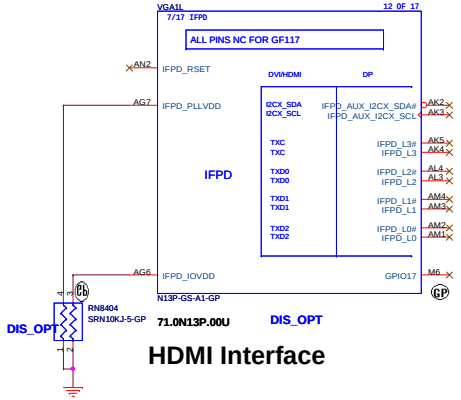
71.0N13P.00U DIS_OPT



71.0N13P.00U DIS_OPT



DIS_OPT



71.0N13P.00U DIS_OPT

HDMI Interface

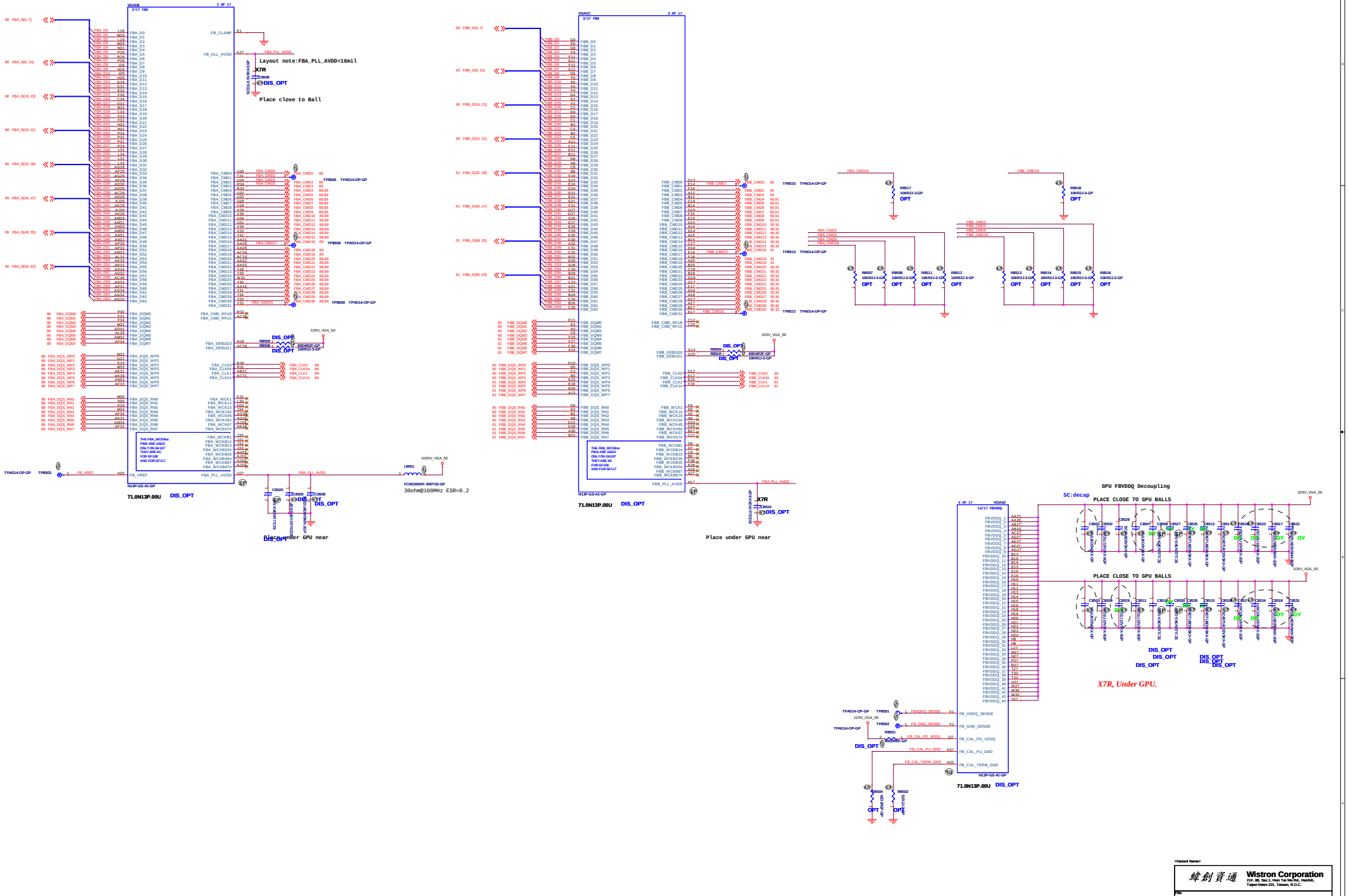
<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

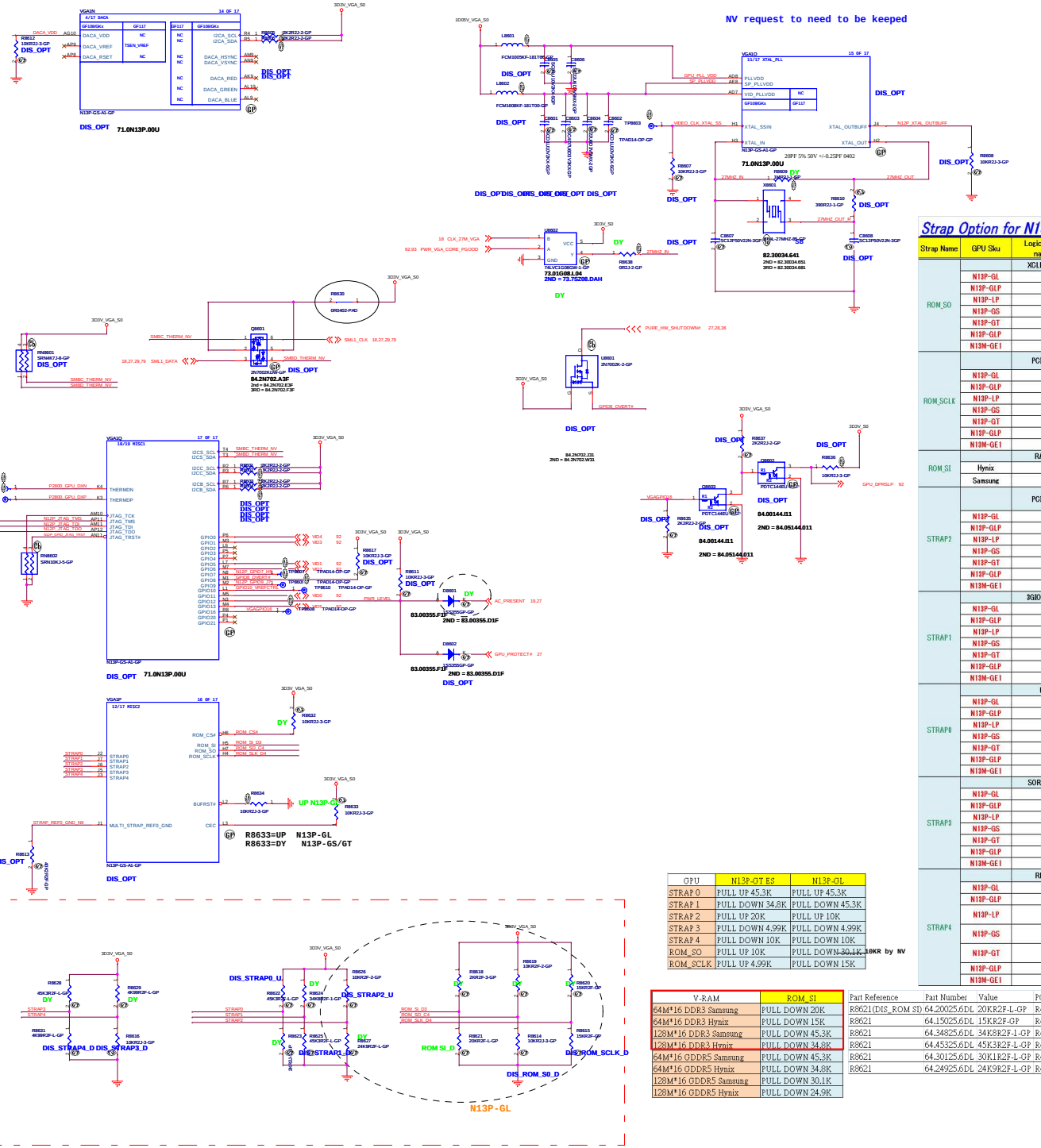
Size: A2 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 84 of 103



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	GPU_DP/LVDS/CRT/GPIO(3/5)	
Size: A2	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 85 of 103	



01/04/12 N13P-GL

Strap Option for N13P-GL/LP/GS/GT

Strap Name	GPU Sku	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0	Set your BOM according to this column	Comment from NVIDIA
		XCLK_417/FB[1]	FB_0_BAR_SIZE/FB[0]	SMB_ALT_ADDR	VGA_DEVICE		
ROM_SO	N13P-GL	0	0	0	1	PULL DOWN 10K	
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13P-LP	1	0	0	1	PULL UP 10K	
	N13P-GS	1	0	0	1	PULL UP 10K	
	N13P-GT	1	0	0	1	PULL UP 10K	
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13M-GE1	0	1	0	1	PULL DOWN 30.1K	
		PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM		
ROM_SCLK	N13P-GL	0	0	1	0	PULL DOWN 15K	
	N13P-GLP	0	0	1	0	PULL DOWN 15K	
	N13P-LP	1	0	0	0	PULL UP 4.99K	
	N13P-GS	1	0	0	0	PULL UP 4.99K	
	N13P-GT	1	0	0	0	PULL UP 4.99K	
	N13P-GLP	0	0	1	0	PULL DOWN 15K	
	N13M-GE1	1	0	0	0	PULL UP 4.99K	
		RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]		
ROM_SI	Hynix	X	X	X	X	This is depends on what Vram you will use. Please check latest RVL.	
	Samsung	X	X	X	X		
		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]		
STRAP2	N13P-GL	1	0	0	1	PULL UP 10K	N13P-GL DID => 0x0DE9
	N13P-GLP	1	0	0	0	PULL UP 4.99K	N13P-GLP DID => 0x0DE8
	N13P-LP	0	0	1	1	PULL DOWN 20K	N13P-LP DID => 0x0FD3
	N13P-GS	0	0	1	0	PULL DOWN 15K	N13P-GS QS DID =>0x0FD2
	N13P-GT	0	0	0	1	PULL DOWN 10K	N13P-GT QS DID =>0x0FD1
	N13P-GLP	1	0	0	0	PULL UP 4.99K	N13P-GLP DID => 0x0DE8
	N13M-GE1	1	0	0	0	PULL UP 4.99K	N13M-GE1 DID => 0x1058
		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]		
STRAP1	N13P-GL	0	1	1	1	PULL DOWN 45.3K	
	N13P-GLP	0	1	1	1	PULL DOWN 45.3K	
	N13P-LP	0	1	1	0	PULL DOWN 34.8K	
	N13P-GS	0	1	1	0	PULL DOWN 34.8K	
	N13P-GT	0	1	1	0	PULL DOWN 34.8K	
	N13P-GLP	0	1	1	1	PULL DOWN 45.3K	
	N13M-GE1	0	1	1	0	PULL DOWN 34.8K	
		USER[3]	USER[2]	USER[1]	USER[0]		
STRAP0	N13P-GL	1	1	1	1	PULL UP 45.3K	
	N13P-GLP	1	1	1	1	PULL UP 45.3K	
	N13P-LP	1	1	1	1	PULL UP 45.3K	
	N13P-GS	1	1	1	1	PULL UP 45.3K	
	N13P-GT	1	1	1	1	PULL UP 45.3K	
	N13P-GLP	1	1	1	1	PULL UP 45.3K	
	N13M-GE1	1	1	1	1	PULL UP 45.3K	
		SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED		
STRAP3	N13P-GL	0	0	0	0	PULL DOWN 4.99K	No display for Optimus sku
	N13P-GLP	0	0	0	0	PULL DOWN 4.99K	
	N13P-LP	0	0	0	0	PULL DOWN 4.99K	
	N13P-GS	0	0	0	0	PULL DOWN 4.99K	
	N13P-GT	0	0	0	0	PULL DOWN 4.99K	
	N13P-GLP	0	0	0	0	PULL DOWN 4.99K	
	N13M-GE1	0	0	0	0	PULL DOWN 4.99K	
		RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V		
STRAP4	N13P-GL	0	0	0	1	PULL DOWN 10K	
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13P-LP	0	1	1	1	PULL DOWN 45.3K	For GEN2 only system, pull down 20K
	N13P-GS	0	1	1	1	PULL DOWN 45.3K	For GEN2 only system, pull down 20K
	N13P-GT	0	1	1	1	PULL DOWN 45.3K	For GEN2 only system, pull down 20K
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13M-GE1	0	0	0	1	PULL DOWN 10K	

GPU	N13P-GT ES	N13P-GL
STRAP 0	PULL UP 45.3K	PULL UP 45.3K
STRAP 1	PULL DOWN 34.8K	PULL DOWN 45.3K
STRAP 2	PULL UP 20K	PULL UP 10K
STRAP 3	PULL DOWN 4.99K	PULL DOWN 4.99K
STRAP 4	PULL DOWN 10K	PULL DOWN 10K
ROM_SO	PULL UP 10K	PULL DOWN ~~30.1K~~ 10KR by NV
ROM_SCLK	PULL UP 4.99K	PULL DOWN 15K

V-RAM	ROM_SI
64M*16 DDR3 Samsung	PULL DOWN 20K
64M*16 DDR3 Hynix	PULL DOWN 15K
128M*16 DDR3 Samsung	PULL DOWN 45.3K
128M*16 DDR3 Hynix	PULL DOWN 34.8K
64M*16 GDDR5 Samsung	PULL DOWN 45.3K
64M*16 GDDR5 Hynix	PULL DOWN 34.8K
128M*16 GDDR5 Samsung	PULL DOWN 30.1K
128M*16 GDDR5 Hynix	PULL DOWN 24.9K

Part Reference	Part Number	Value	PCB Footprint
R8621(DIS_ROM SI)	64.20025.6DL	20KR2F-L-GP	R402H16
R8621	64.15025.6DL	15KR2F-GP	R402H16
R8621	64.34825.6DL	34K8R2F-L-GP	R402H16
R8621	64.45325.6DL	45K3R2F-L-GP	R402H16
R8621	64.30125.6DL	30K1R2F-L-GP	R402H16
R8621	64.24925.6DL	24K9R2F-L-GP	R402H16

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

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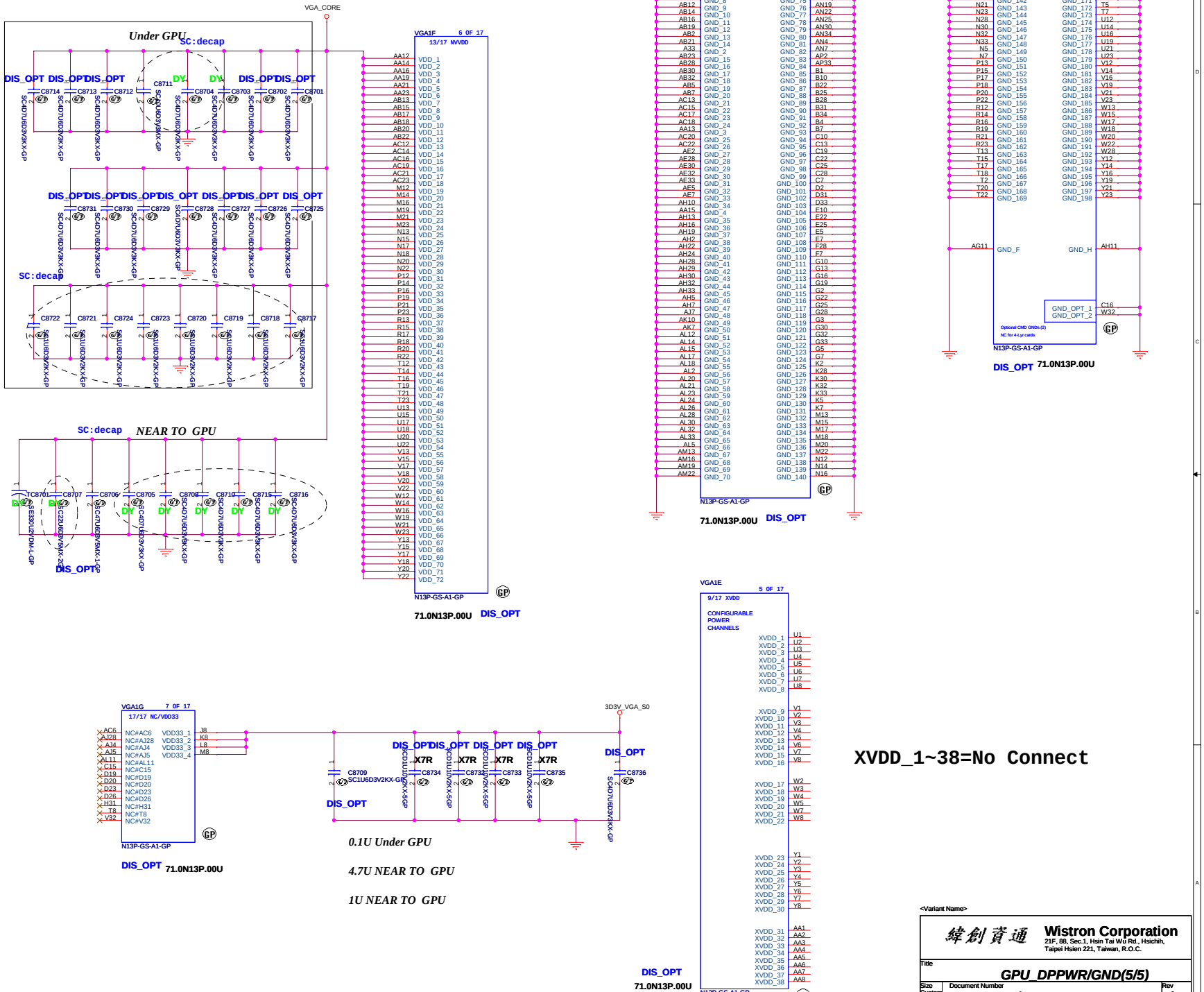
EDP 60A (TDP 55W)



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

Size: Custom | Document Number: Colossus | Rev: 1

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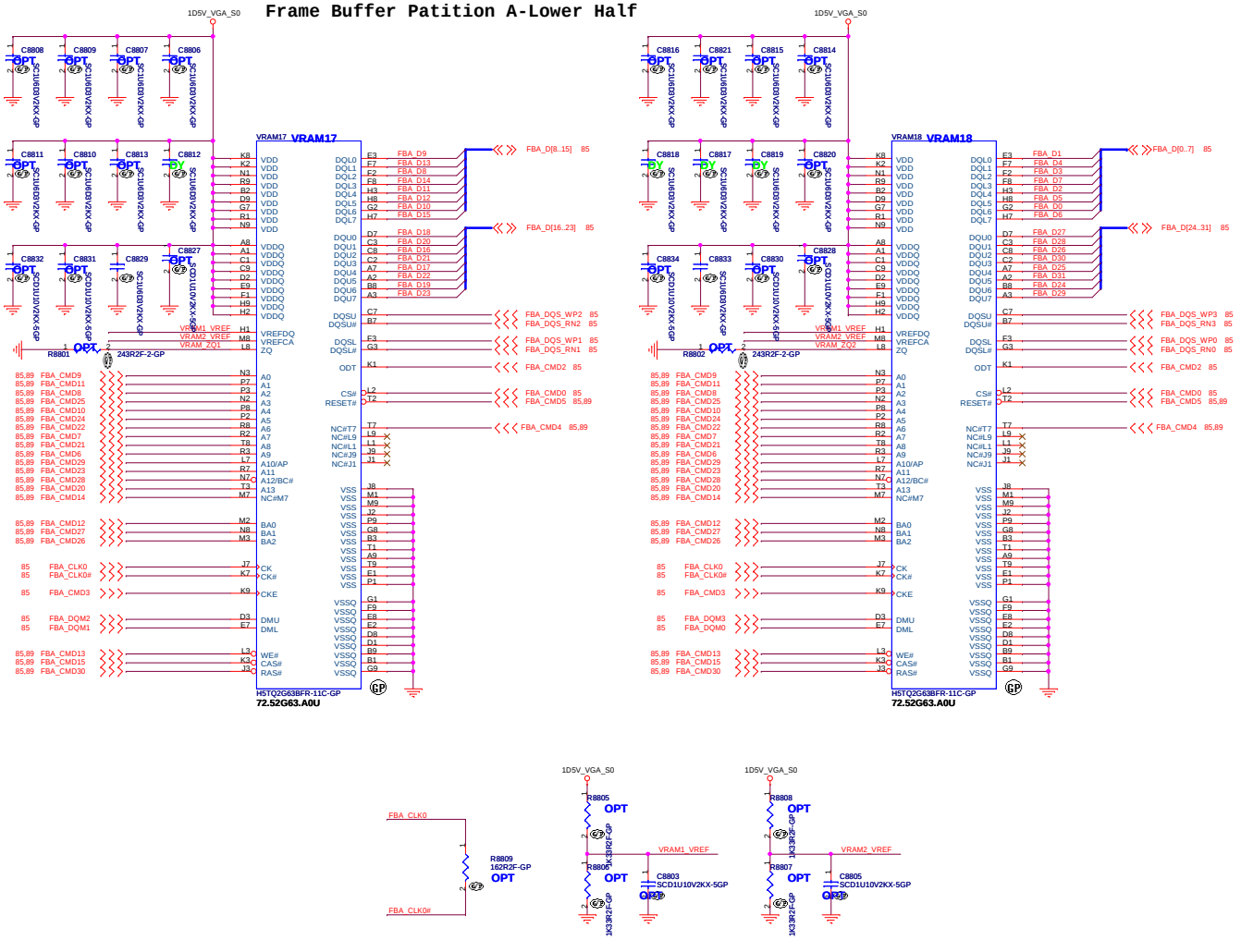
Frame Buffer Patition A-Lower Half



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU-VRAM1,2 (1/4)***	
Size: A2	Document Number: **Colossus**	Rev: 1
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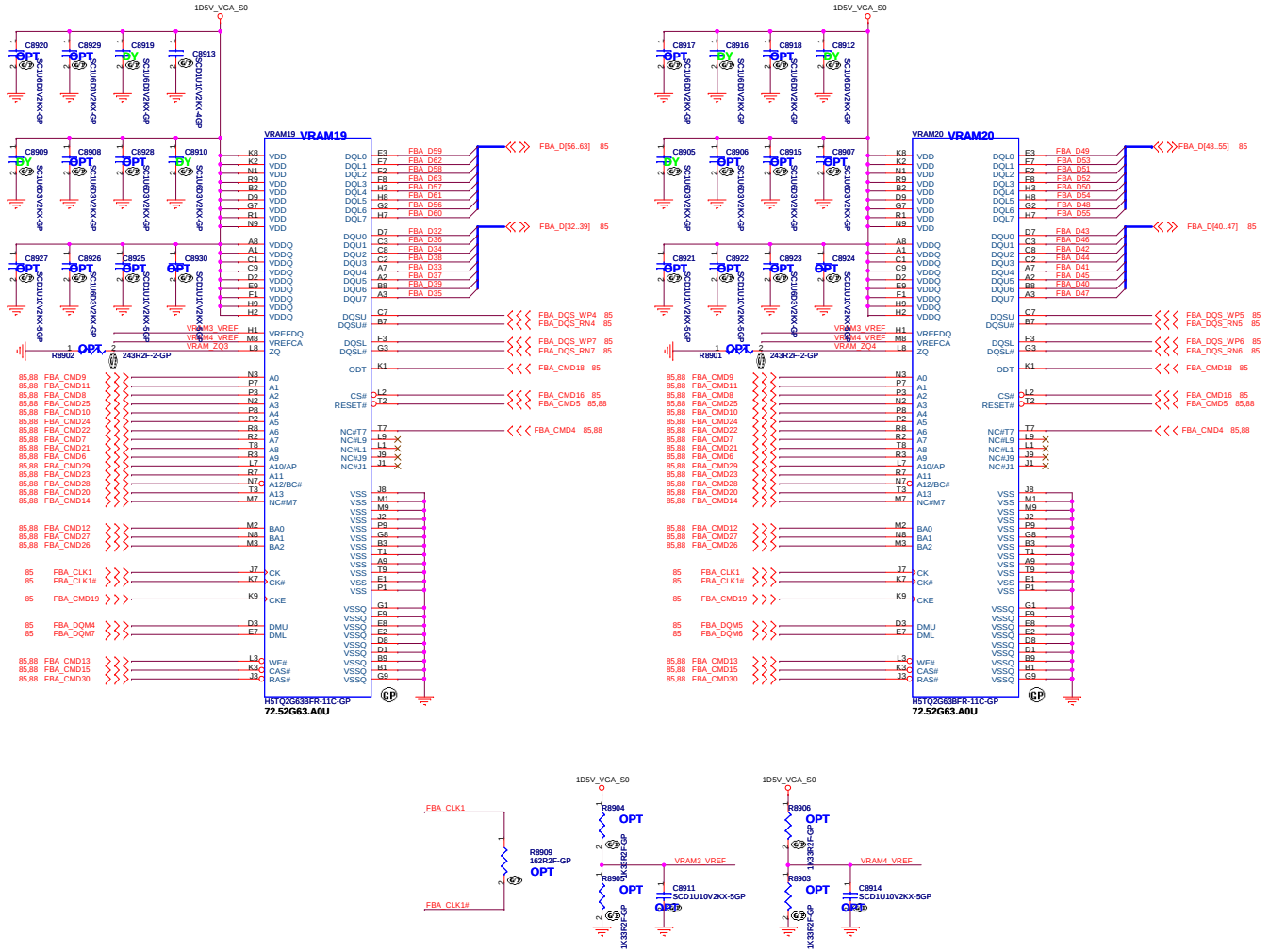
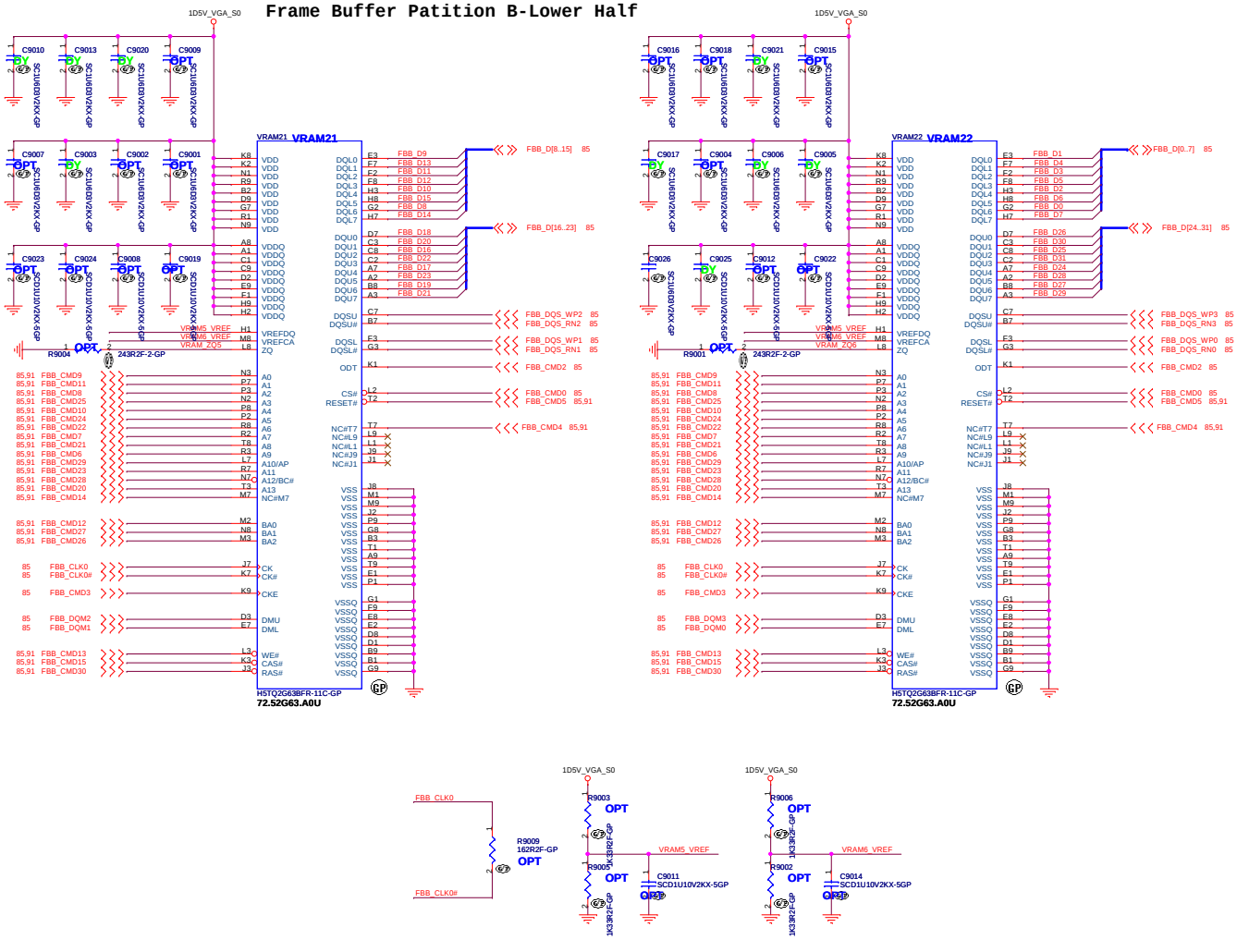
Frame Buffer Patition A-Upper Half



<Variant Name>	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU-VRAM3,4 (2/4)	
Size: A2	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 89 of 103	

Frame Buffer Patition B-Lower Half



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM5,6 (3/4)

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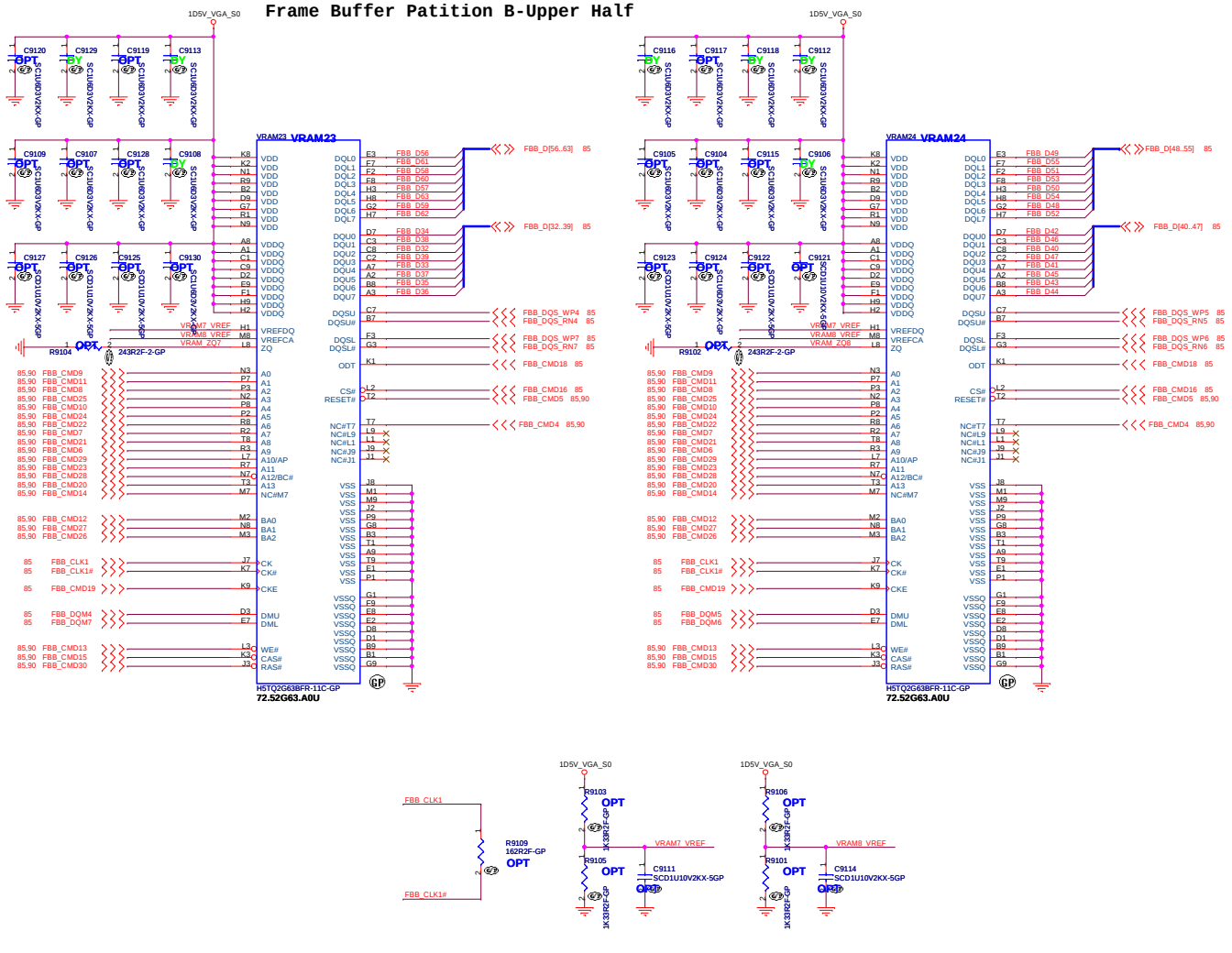
Frame Buffer Patition B-Upper Half



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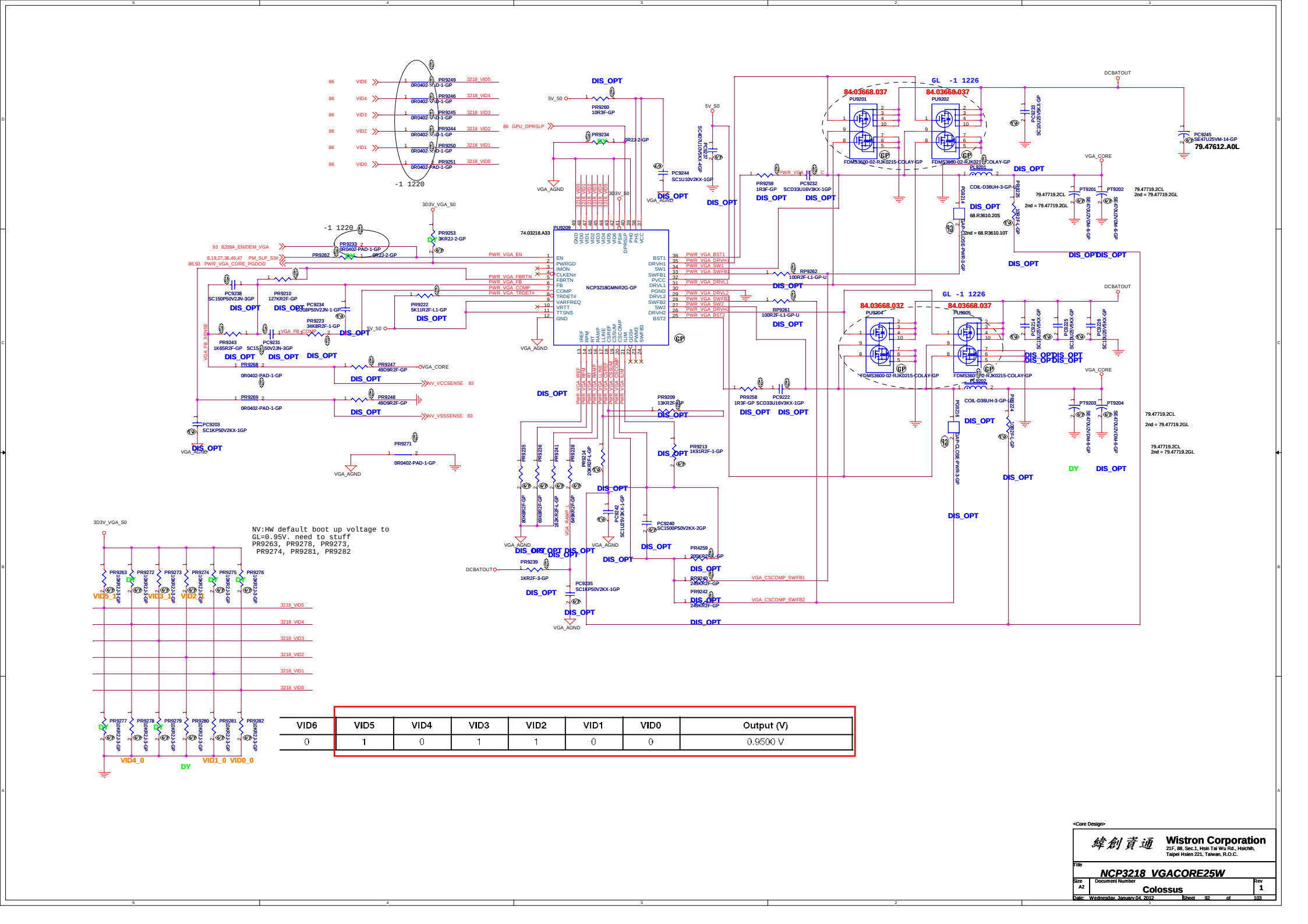
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU-VRAM7,8 (4/4)		
Size: A2	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 91 of 103	



VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	1	0	1	1	0	0	0.9500 V

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP3218 VGACORE25W

Size: A2 | Document Number: Colossus | Rev: 1

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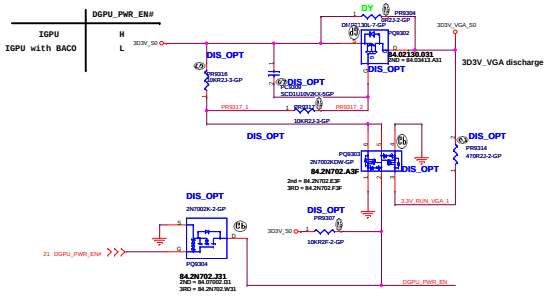
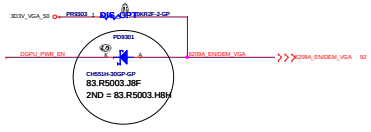
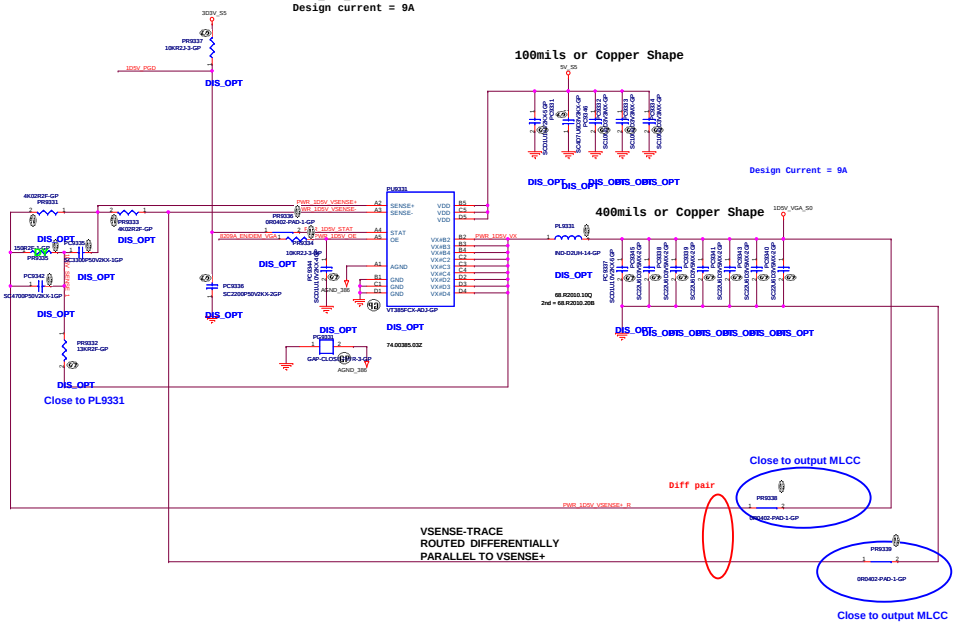
VGA chip sequence: 3V_VGA_S0>VGA_CORE>1D5V_VGA>1D05V_VGA

3V_VGA_S0 → VGA_CORE → 1.5V_VGA_S0





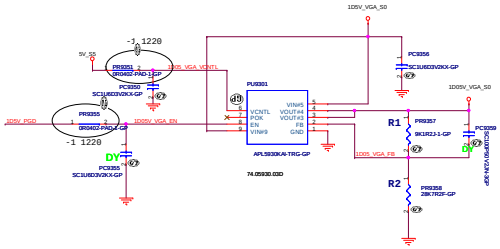
1D5V_VGA_S0
Design current = 9A

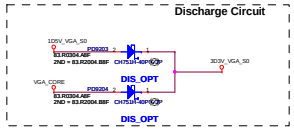


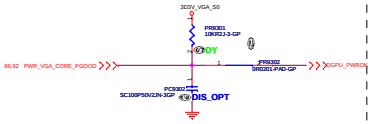
1D05V_VGA

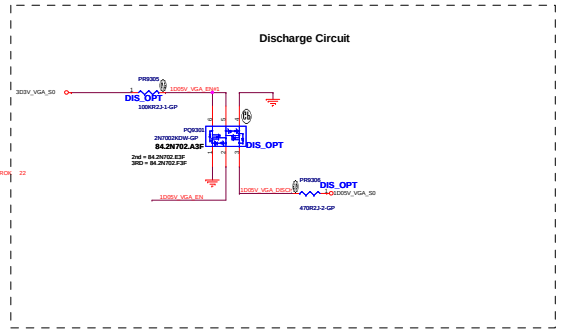
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D5V_VGA_S0 should ramp up
so 1D05V_VGA_S0 EN have to fine tune RC delay after VGA_Core

1D05V_VGA_S0
Design current = 3.8A









蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER
Size: A1 | Document Number: Colossus | Rev: 1
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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	Colossus	1

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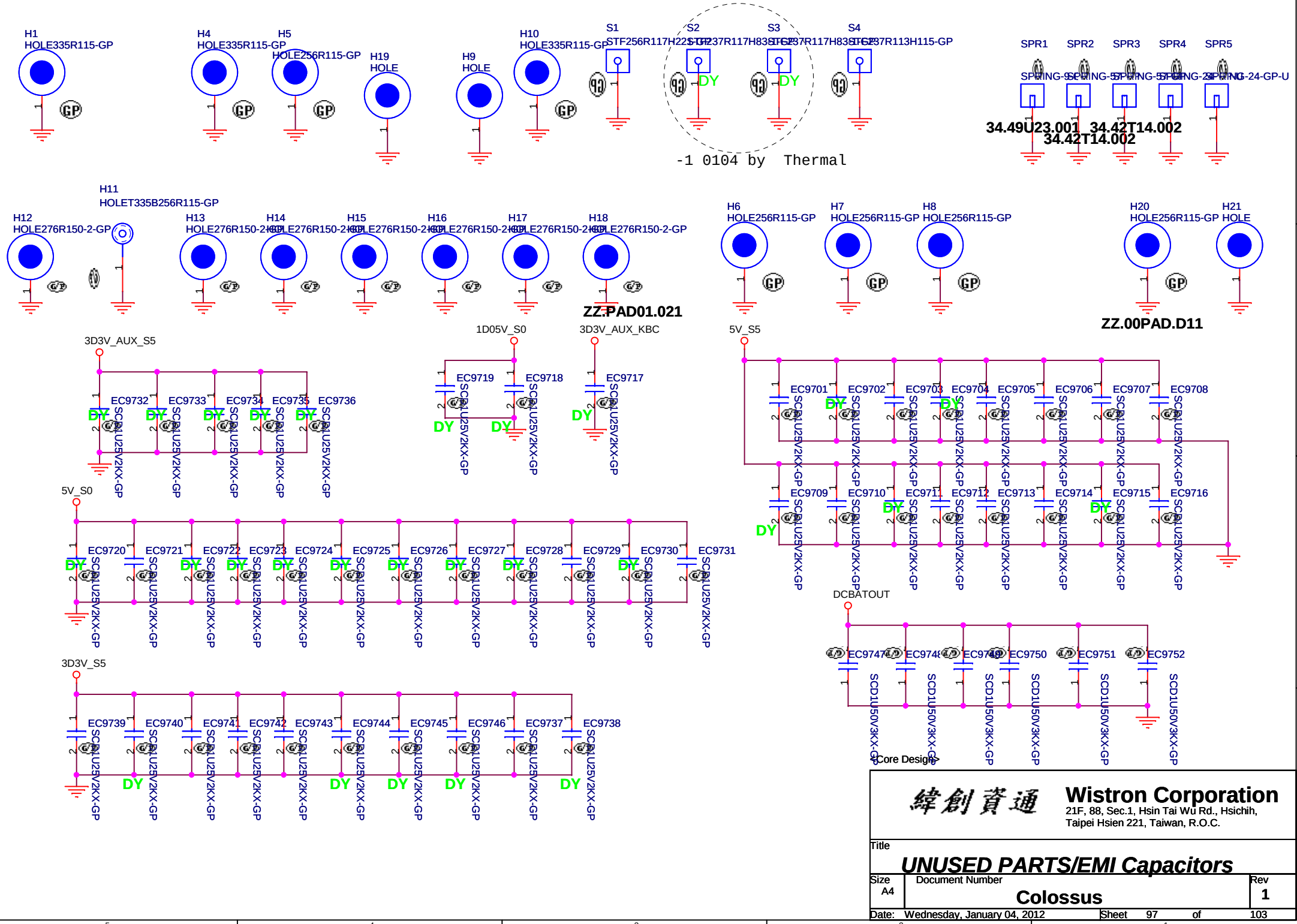
H1
HOLE335R115-GP
H4
HOLE335R115-GP
H5
HOLE256R115-GP
H19
HOLE
H9
HOLE
H10
HOLE335R115-GP
S1
S2
S3
S4
DY
-1 0104 by Thermal
SPR1
SPR2
SPR3
SPR4
SPR5
34.49U23.001
34.42T14.002
34.42T14.002
H11
HOLET335B256R115-GP
H12
HOLE276R150-2-GP
H13
H14
H15
H16
H17
H18
ZZ.PAD01.021
H6
HOLE256R115-GP
H7
HOLE256R115-GP
H8
HOLE256R115-GP
H20
HOLE256R115-GP
H21
HOLE
ZZ.00PAD.D11
3D3V_AUX_S5
EC9732
EC9733
EC9734
EC9735
EC9736
1D05V_S0
EC9719
EC9718
3D3V_AUX_KBC
EC9717
5V_S5
EC9701
EC9702
EC9703
EC9704
EC9705
EC9706
EC9707
EC9708
EC9709
EC9710
EC9711
EC9712
EC9713
EC9714
EC9715
EC9716
5V_S0
EC9720
EC9721
EC9722
EC9723
EC9724
EC9725
EC9726
EC9727
EC9728
EC9729
EC9730
EC9731
DCBATOUT
EC9747
EC9748
EC9749
EC9750
EC9751
EC9752
3D3V_S5
EC9739
EC9740
EC9741
EC9742
EC9743
EC9744
EC9745
EC9746
EC9737
EC9738
SCD1U25V2KX-GP
SCD1U50V3KX-GP
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緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
UNUSED PARTS/EMI Capacitors
Size
A4
Document Number
Colossus
Rev
1
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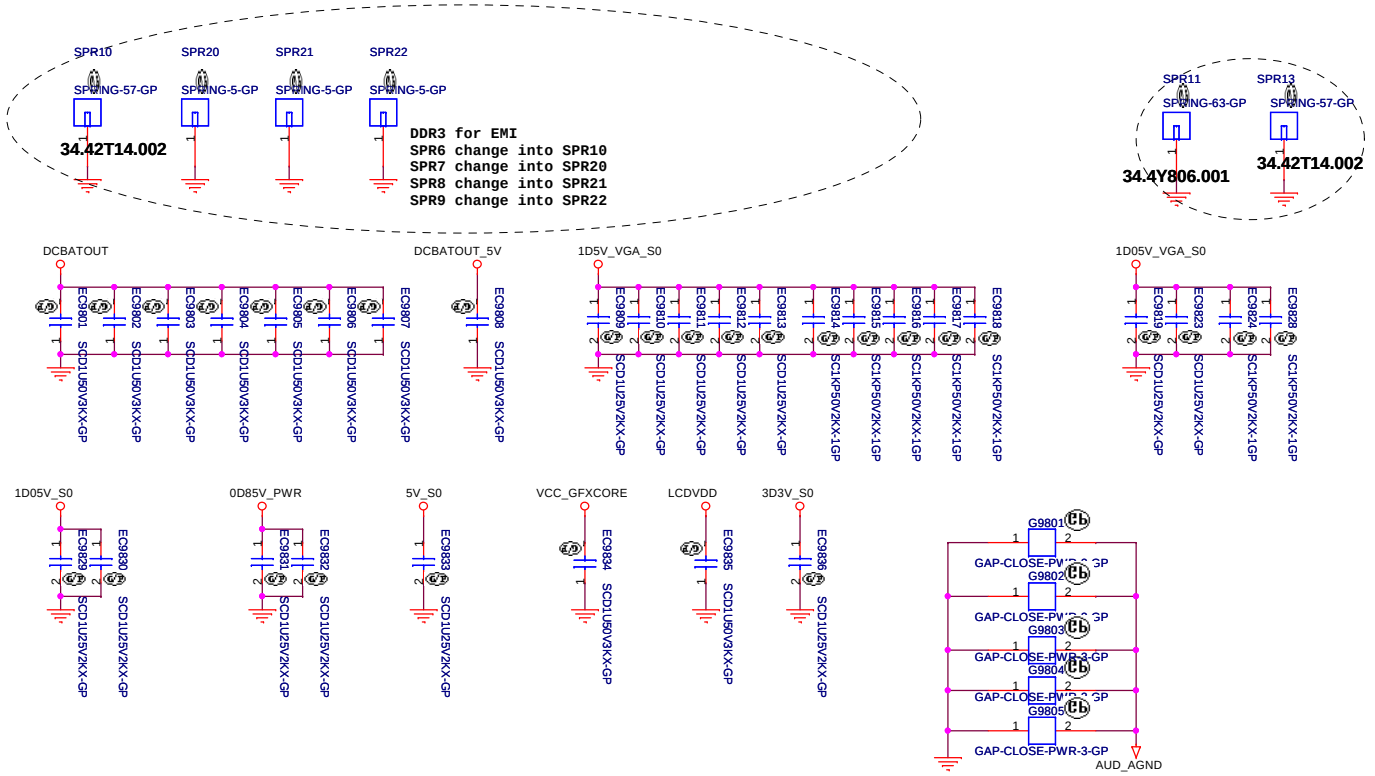

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Change History***

Size	Document Number	Rev
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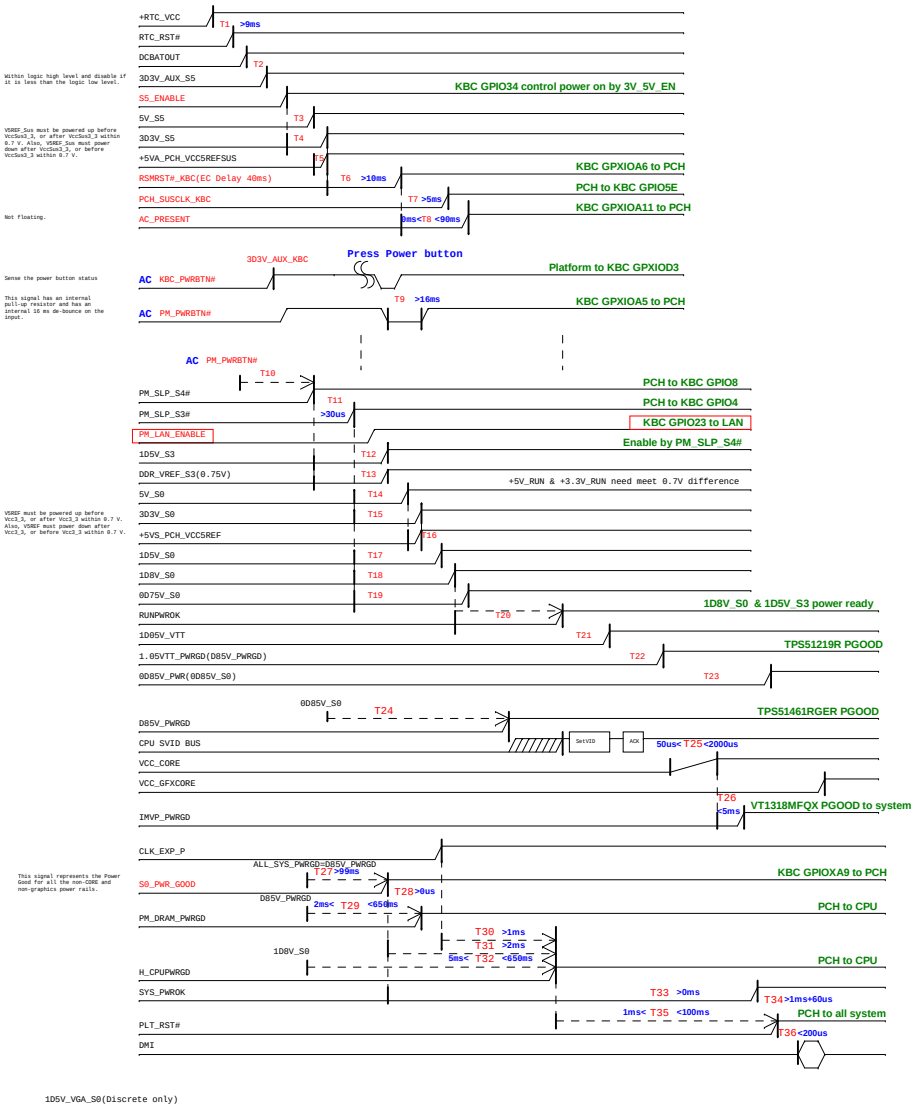
Chief River Platform Power Sequence

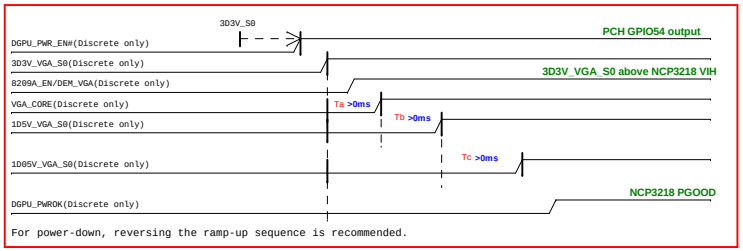
(AC mode)

red word: KBC GPIO



1D5V_VGA_S0(Discrete only)

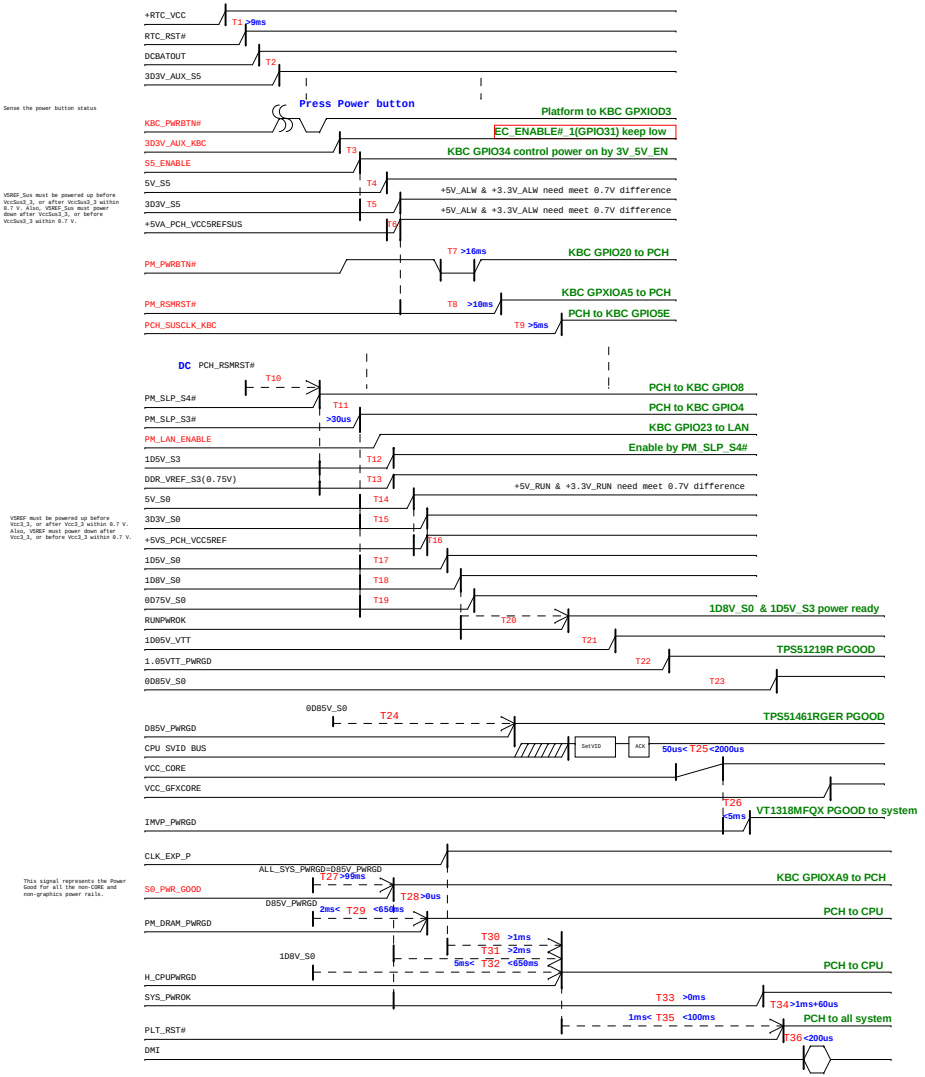
N13P Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

red word: KBC GPIO



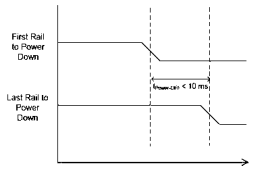


Figure 18. Recommended Power Off Sequencing Order

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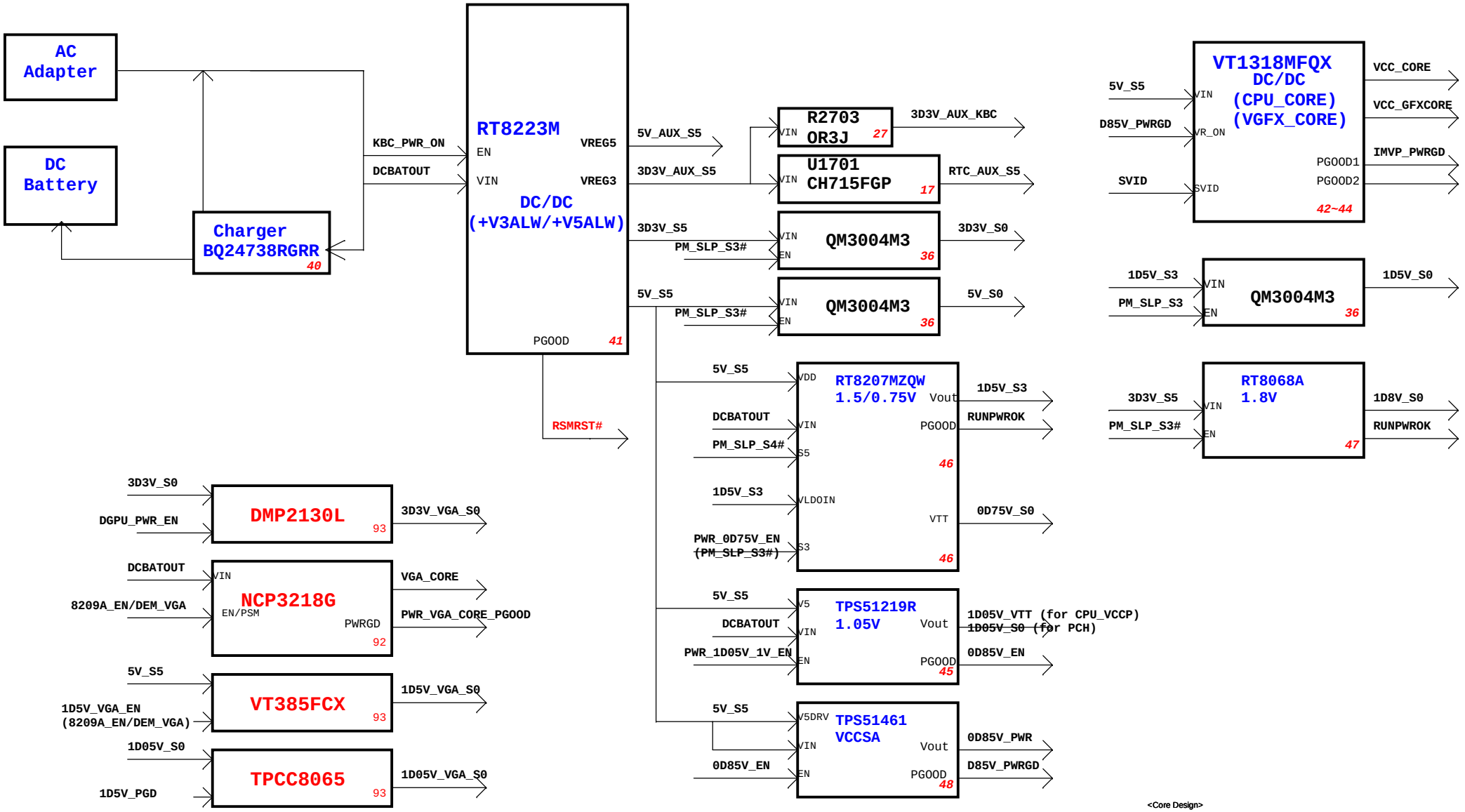
COLOSUSS POWER BLOCK DIAGRAM



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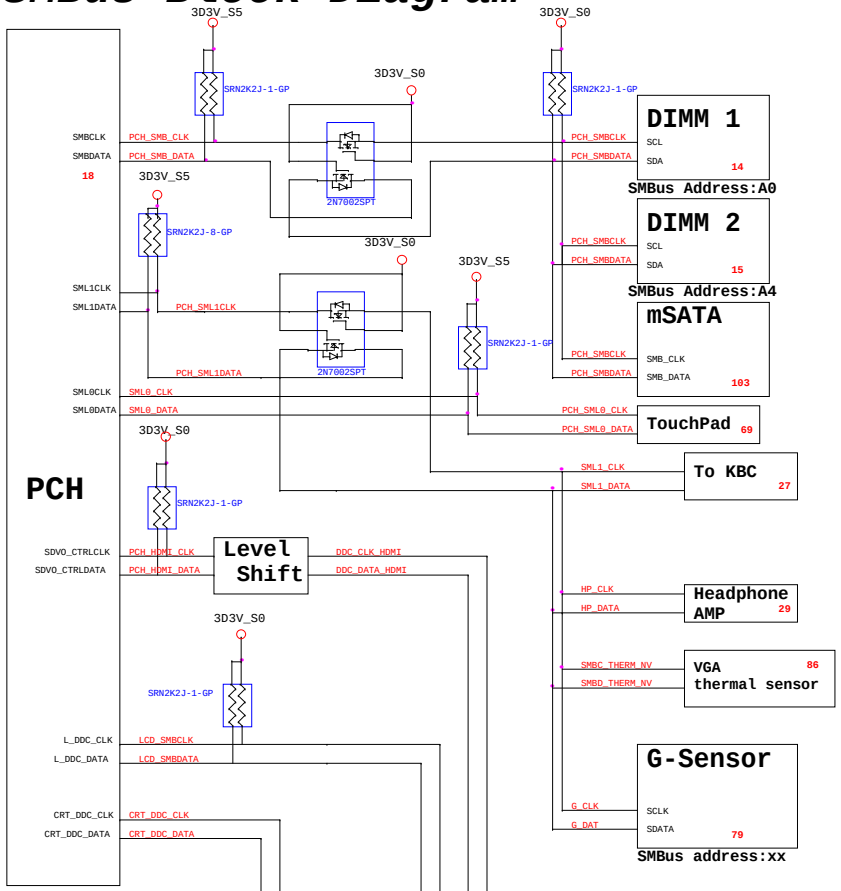
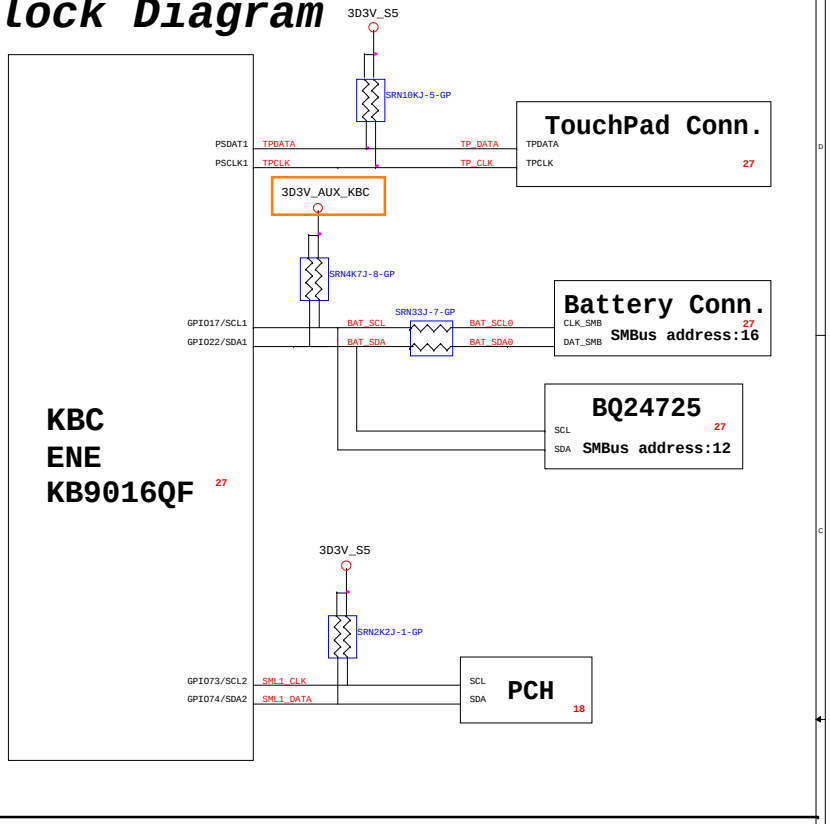
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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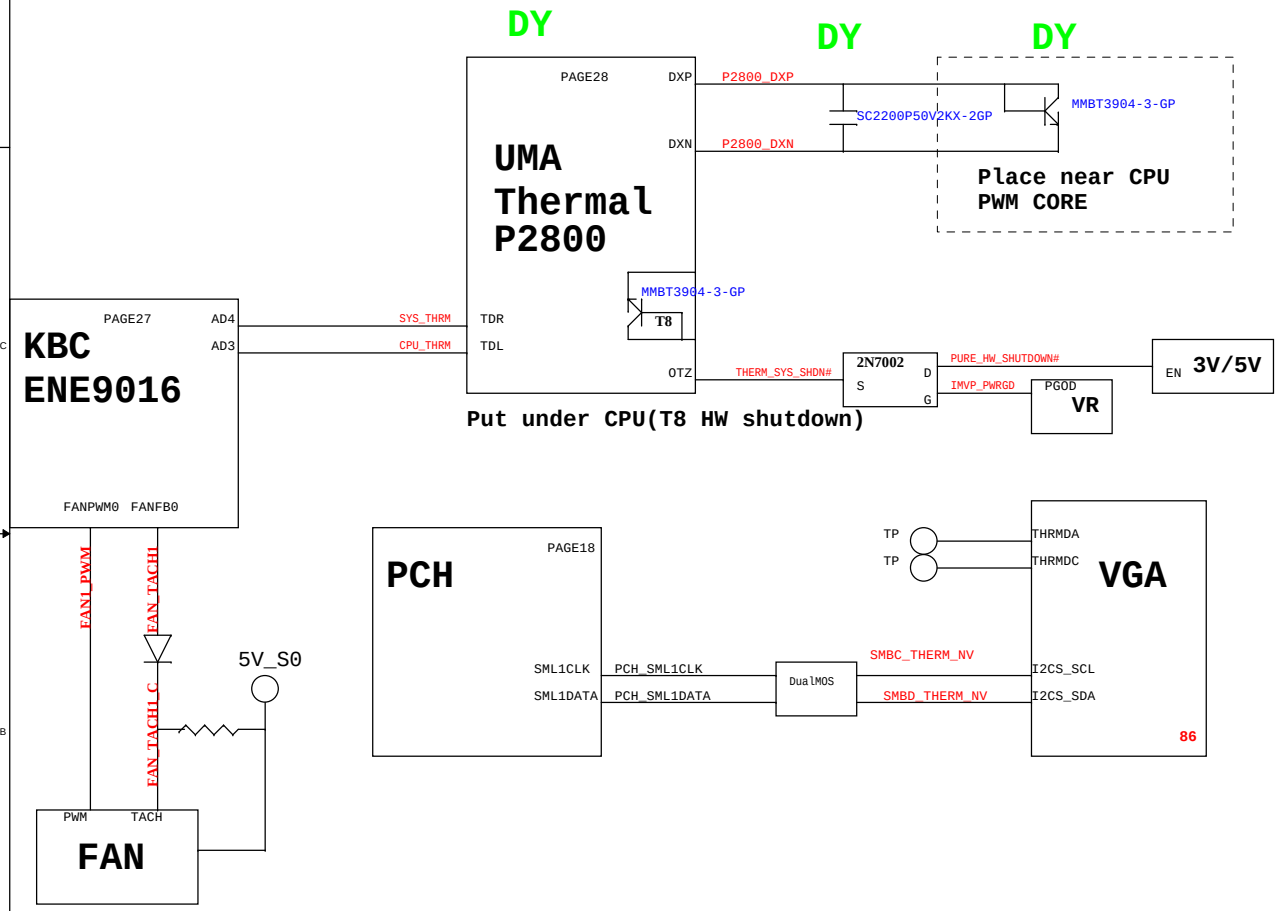
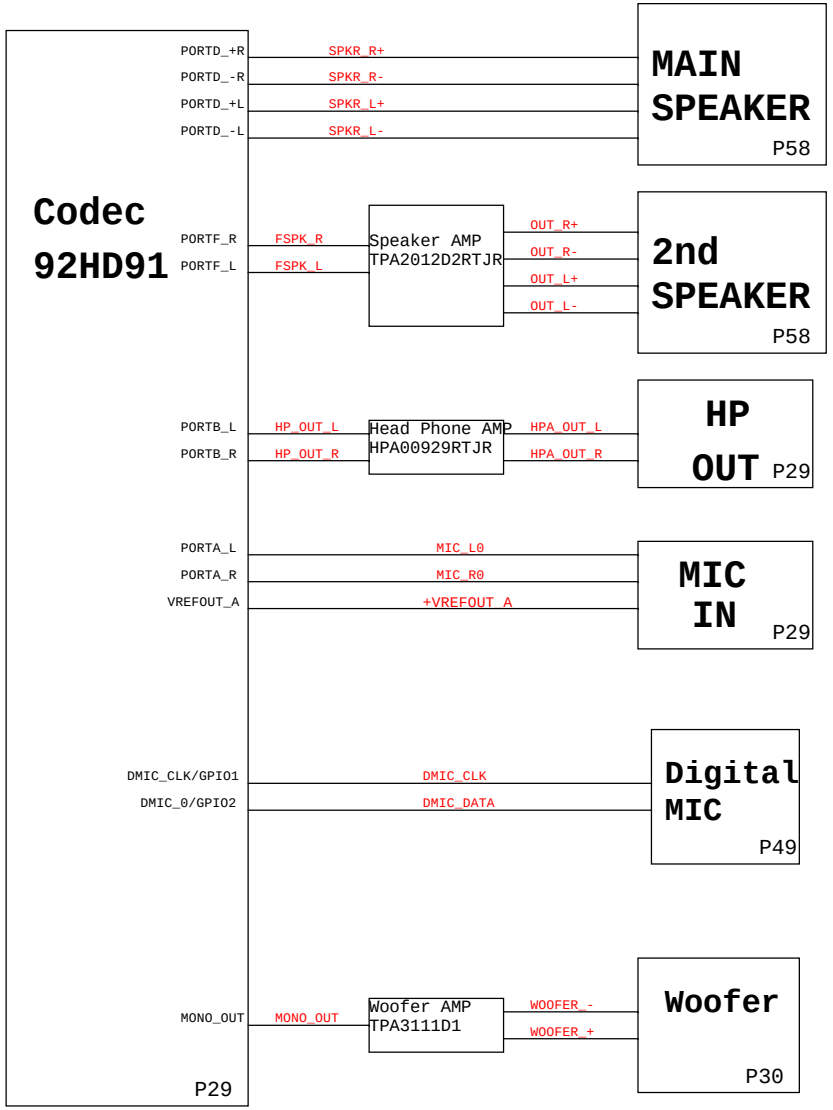
Thermal Block Diagram



Audio Block Diagram



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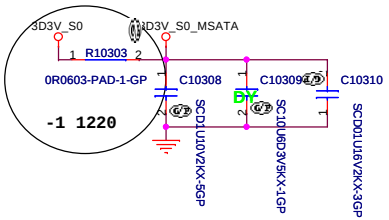
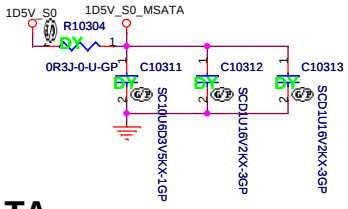
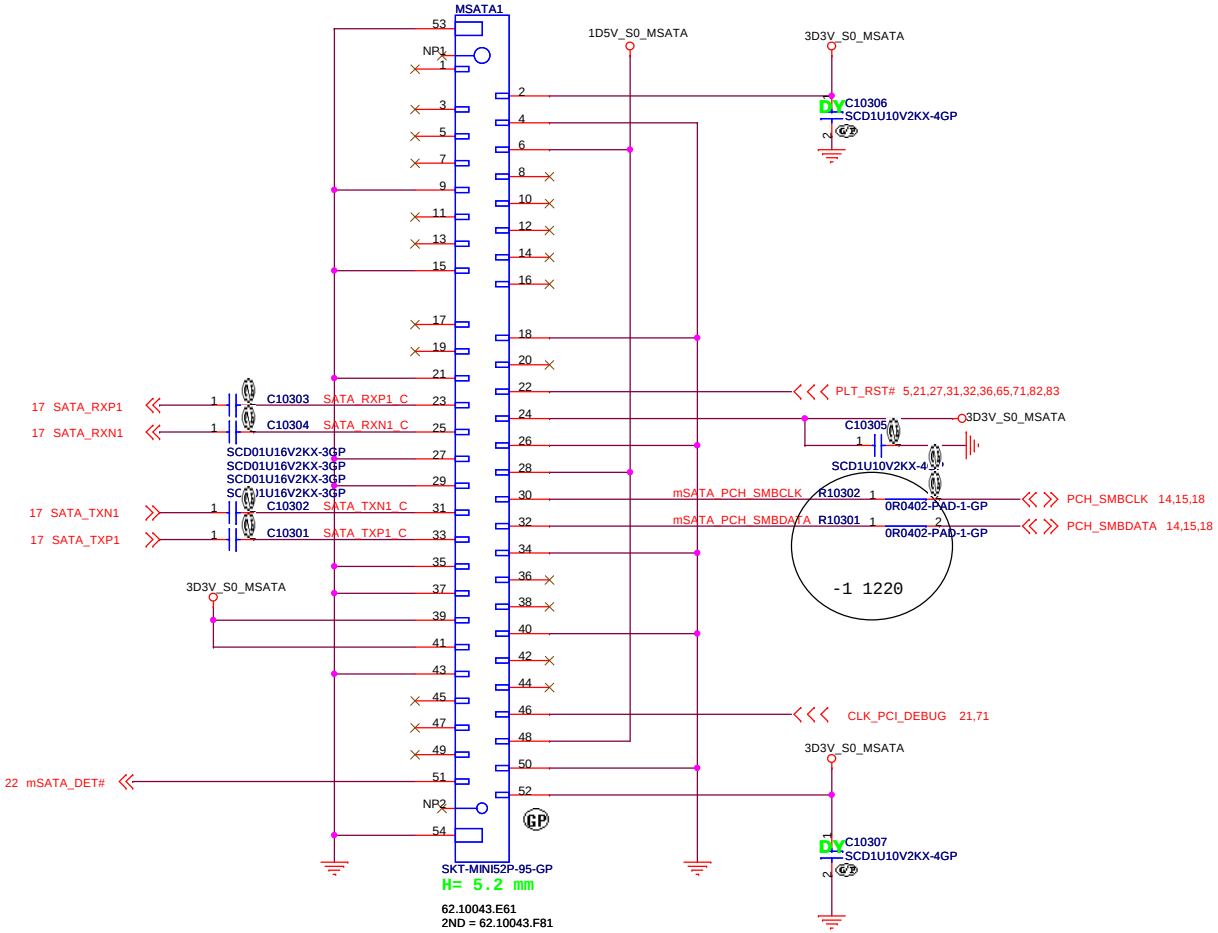




mSATA



677867-FM5

Pin #	Name	Description		Pin #	Name	Description
1	Reserved	NC		2	V33	3.3V power
3	Reserved	NC		4	GND	Return Current Path
5	Reserved	NC		6	V15	1.5V power (Unused)
7	Reserved	NC		8	Reserved	NC
9	GND	Return Current Path		10	Reserved	NC
11	Reserved	NC		12	Reserved	NC
13	Reserved	NC		14	Reserved	NC
15	GND	Return Current Path		16	Reserved	NC
Key						
17	Reserved	NC		18	GND	Return Current Path
19	Reserved	NC		20	Reserved	NC
21	GND	Return Current Path		22	Reserved	NC
23	B+	Differential Signal Pair B (Device Tx)		24	V33	3.3V power
25	B-			26	GND	Return Current Path
27	GND	Return Current Path		28	V15	1.5V power (Unused)
29	GND	Return Current Path		30	Reserved	NC
31	A-	Differential Signal Pair A (Device Rx)		32	Reserved	NC
33	A+			34	GND	Return Current Path
35	GND	Return Current Path		36	Reserved	NC
37	GND	Return Current Path		38	Reserved	NC
39	V33	3.3V power		40	GND	Return Current Path
41	V33	3.3V power		42	Reserved	NC
43	GND	Return Current Path		44	Reserved	NC
45	Vendor	No connect at Host side		46	Reserved	NC
47	Vendor	No connect at Host side		48	V15	1.5V power (Unused)
49	DAS/DSS*1	Drive Activity Signal		50	GND	Return Current Path
51	Presense*2	Device Presense		52	V33	3.3V power

Note: *1: DAS/DSS signal is not use for this drive. (DAS Signal output is optional)

*2: Presense pin is Connected to GND by device side. (220Ω Pull Down)

1st	677867-FM5
2nd	677867-AM5
3rd	677867-BM5
4th	677867-LM5

<Core Design>

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