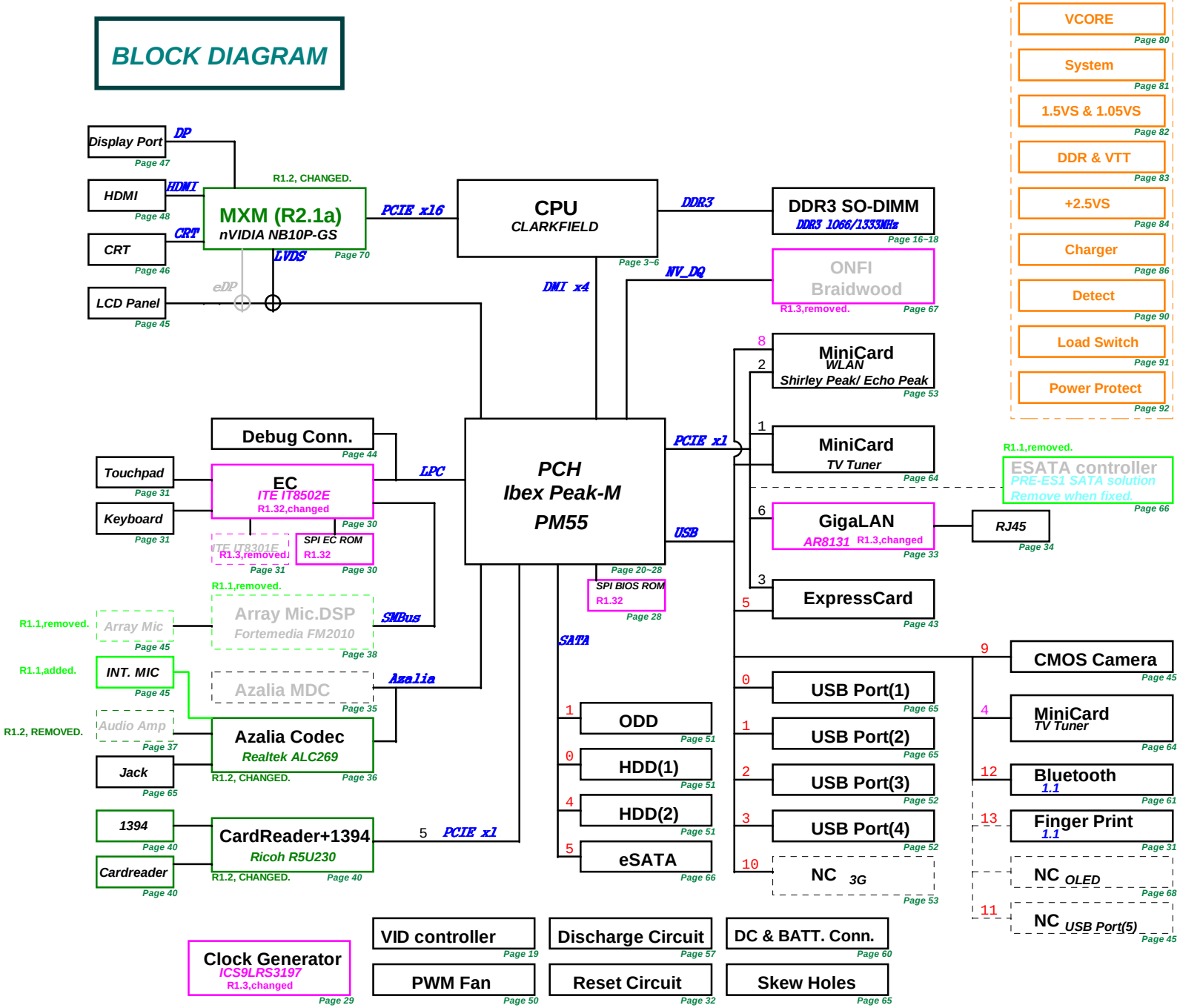
M60J SCHEMATIC Revision 2.00

SYSTEM PAGE REF.

PAGE	Content
1	Block Diagram
2	System Setting
3	CPU(1)_DMI,PEG,FDI,CLK,MISC
4	CPU(2)_DDR3
5	CPU(3)_CFG,RSVD,GND
6	CPU(4)_PWR
7	CPU(5)_XDP
16	DDR3 SO-DIMM_0
17	DDR3 SO-DIMM_1
18	DDR3 CA_DQ VOLTAGE
19	VID CONTROLLER
20	PCH_IBEX(1)SATA,IHDA,RTC,LPC
21	PCH_IBEX(2)_PCIE,CLK,SMB,PEG
22	PCH_IBEX(3)_FDI,DMI,SYS PWR
23	PCH_IBEX(4)_DP,LVDS,CRT
24	PCH_IBEX(5)_PCI,NVRAM,USB
25	PCH_IBEX(6)CPU,GPIO,MISC
26	PCH_IBEX(7)_POWER,GND
27	PCH_IBEX(8)_POWER,GND
28	PCH_SPI ROM,OTH
29	CLK_ICS9LRS3197
30	EC_IT8502(1/2)
31	EC_IT8502(2/2)KB, TP,FP
32	RST_Reset Circuit
33	HANKSVILLE
34	LAN-AR8131
36	AUD-ALC269
37	AUD-HEADPHONE & SPEAKER
40	CB_R5U230
43	CB_NewCard
44	BUG_Debug
45	CRT_LCD Panel
46	CRT_D-Sub
47	Display Port
48	TV_HDMI
50	FAN_Fan & Sensor
51	XDD_HDD & ODD
52	USB_USB Port *2
53	MINICARD(WLAN)
56	LED_Indicator
57	DSG_Discharge
58	PW_PROTECT
60	DC_DC & BAT Conn.
61	BT_Bluetooth
64	TUN_TV Tuner
65	ME_Conn & Skew Hole
66	ESA_ESATA
67	PCH_XDP, ONFI
70	VGA_MXM

80	PW_VCORE(MAX17034)
81	PW_SYSTEM(MAX17020)
82	PW_I/O_VTT_CPU&+1.1VM
83	PW_I/O_DDR & VTT& +1.8VS
84	PW_I/O_3VM & ME_+VM_PWEGD
86	PW_+VGFX_CORE(MAX17028)
88	PW_CHARGER(MAX17015)
90	PW_DETECT
91	PW_LOAD SWITCH
93	PW_SIGNAL
94	PW_FLOWCHART

BLOCK DIAGRAM



ASUS	Title : Block Diagram		
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Thursday, July 09, 2009	Sheet 1 of 99		

PCH_IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	NC_TP	-	+3VS
GPIO 01	GPO	NC_TP	INT TBD	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	EXT PU	+5VS
GPIO 06	GPO	NC_TP	INT TBD	+3VS
GPIO 07	GPO	NC_TP	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	NC_PU	EXT PU	+3VSUS
GPIO 10	Native	NC_PU	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	NC_TP	-	+3VSUS
GPIO 13	GPO	NC_TP	-	+3VSUS
GPIO 14	GPO	NC_PU	EXT PU	+3VSUS
GPIO 15	GPO	BT_LED	INT PD	+3VSUS
GPIO 16	GPI	DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 17	GPI	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	GPI	CLKREQ1#_TV	EXT PD	+3VS
GPIO 19	GPI	SATA1GP	EXT PU	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PD	+3VS
GPIO 21	GPI	SATA0GP	EXT PU	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	Native	NC_TP	INT PU	+3VS
GPIO 24	GPO	NC_TP	-	+3VSUS
GPIO 25	GPI	CLKREQ3#_NEWCARD	EXT PD	+3VSUS
GPIO 26	GPI	CLK_REQ4#_CB	EXT PD	+3VSUS
GPIO 27	GPO	NC_TP	INT WEAK PU	+3VSUS
GPIO 28	GPO	WLAN_ON#	EXT PD	+3VSUS
GPIO 29	Native	NC_TP	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	GPO	ME_SusPwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	GPIO	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPI	HDA_DOCK_EN#	-	+3VS
GPIO 34	Native	NC_TP	-	+3VS
GPIO 35	GPO	SATA_CLK_REQ#	EXT PD	+3VS
GPIO 36	GPI	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSNT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	NC_PU	EXT PU	+3VSUS
GPIO 41	Native	NC_PU	EXT PU	+3VSUS
GPIO 42	Native	NC_PU	EXT PU	+3VSUS
GPIO 43	Native	NC_PU	EXT PU	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU	+3VSUS
GPIO 45	Native	NC_TP	EXT PU	+3VSUS
GPIO 46	Native	NC_TP	EXT PU	+3VSUS
GPIO 47	GPI	CLKREQ_PEG#	EXT PU	+3VSUS
GPIO 48	GPO	NC_TP	-	+3VS
GPIO 49	GPIO	PCH_TEMP_ALERT#	EXT PU	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	Native	DGPU_SELECT#_R	EXT PU	+5VS
GPIO 53	GPO	NC_TP	INT PU	+3VS
GPIO 54	Native	PCI_REQ3#	EXT PU	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	GPI	CLKREQ_GLAN#	EXT PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	GPIO	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	NC_PU	EXT PU	+3VSUS
GPIO 60	Native	SML0ALERT#	EXT PU	+3VSUS
GPIO 61	Native	NC_TP	-	+3VSUS
GPIO 62	Native	NC_TP	-	+3VSUS
GPIO 63	Native	NC_TP	-	+3VSUS
GPIO 64	Native	NC_TP	INT TBD	+3VS
GPIO 65	Native	NC_TP	INT TBD	+3VS
GPIO 66	Native	NC_TP	INT TBD	+3VS
GPIO 67	Native	NC_TP	INT TBD	+3VS
GPIO 72	Native	PM_BATLOW#	EXT PU	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU	+3VSUS
GPIO 74	Native	SML1ALERT#	EXT PU	+3VSUS
GPIO 75	GPIO	SML1_DATA	EXT PU	+3VSUS

EC IT8541

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2		-
GPA3		-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN0_PWM
GPA6		-
GPA7		-
GPB0	O	BATSEL_0
GPB1	O	BATSEL_1
GPB2	O	ME_AC_PRESENT_EC
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RCIN#
GPB7	O	PM_RSMRST#
GPC0		-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7		-
GPE0	O	VSUS_ON
GPE1	O	EGAD (IT8301 Address/Data connect)
GPE2	O	EGCS (IT8301 Cycle Start connect)
GPE3	O	EGCLK (IT8301 Clock connect)
GPE4	I	PWR_SW#
GPE5		-
GPE6	I	LID_SW#
GPE7		-
GPF0	O	-
GPF1		-
GPF2	I	EXP_GATE#
GPF3		-
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7	O	PCH_SPI_OV
GPG0	I	ME_SusPwrDnAck_EC
GPG1	I	PM_SUSB#
GPG2		-
GPG6		-
GPH0	IO	PM_CLKRUN#
GPH1	O	GFX_VR_ON
GPH2	O	CHG_EN
GPH3	O	SUSC_EC#
GPH4	O	SUSB_EC#
GPH5	O	NUM_LED#
GPH6	O	CAP_LED#
GPI0		-
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	PCH_TEMP_ALERT#
GPI5	I	ALS_AD
GPI6	I	CAP_ACK_A#
GPI7	I	CAP_ACK_B#
GPJ0	O	CPU_VRON
GPJ1	O	PM_PWROK
GPJ2	O	VSET_EC
GPJ3	O	ISET_EC
GPJ4	O	TP_LED
GPJ5		-

EC IT8301 R1.3 removed

EC GPIO	Use As	Signal Name
GPIO0	I	ME_PM_SLP_M#
GPIO1	I	ME_SusPwrDnAck
GPIO2		-
GPIO3		-
GPIO4	I	ME_+VM_PWRGD
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	O	ME_AC_PRESENT
GPIO7		-
GPIO8		-
GPIO9		-
GPIO10		-
GPIO11		-
GPIO12	O	ME_PWROK
GPIO13		-
GPIO14	O	ME_SLP_M_EC#
GPIO15		-
GPIO16		-
GPIO17		-
GPIO18		-
GPIO19		-
GPIO20		-
GPIO21		-
GPIO22		-
GPIO23		-
GPIO24		-
GPIO25		-
GPIO26		-
GPIO27		-
GPIO28		-
GPIO29		-
GPIO30		-
GPIO31		-
GPIO32		-
GPIO33		-
GPIO34		-
GPIO35		-
GPIO36		-
GPIO37		-

PCIE 1	Minicard TV Tuner
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	Card reader
PCIE 6	GLAN
PCIE 7	
PCIE 8	

SATA 0	SATA HDD (1)
SATA1	SATA ODD
SATA4	SATA HDD (2)
SATA5	ESATA

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	USB Port (4)
USB 4	Minicard TV Tuner
USB 5	NewCard
USB 6	
USB 7	
USB 8	WLAN
USB 9	CMOS Camera
USB 10	
USB 11	
USB 12	Bluetooth
USB 13	Finger Printer

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
Clock Generator(ICS9LRS3197)	1101001x (D2)	
SO-DIMM 0	1010000x (A0)	
SO-DIMM 1	1010001x (A2)	
VID Controller(ASM8272)	0011011x (36)	
WiFi/WiMax	N/A	
EC Master (SMB1)		
SM-Bus Device	**SM-Bus Address**	
CPU Thermal Sensor	-	
VGA Thermal IC(G781-1)	1001101x (9A)	

Device Identification

	CPU Thermal Sensor P/N:	component name
1st		
S		
S		
S		

	Clock Gen P/N:	component name
1st	06G011604010	ICS9LRS3197
S		
S		

	VGA Thermal Sensor	component name
1st	06G023048020	G781-1
S		
S		

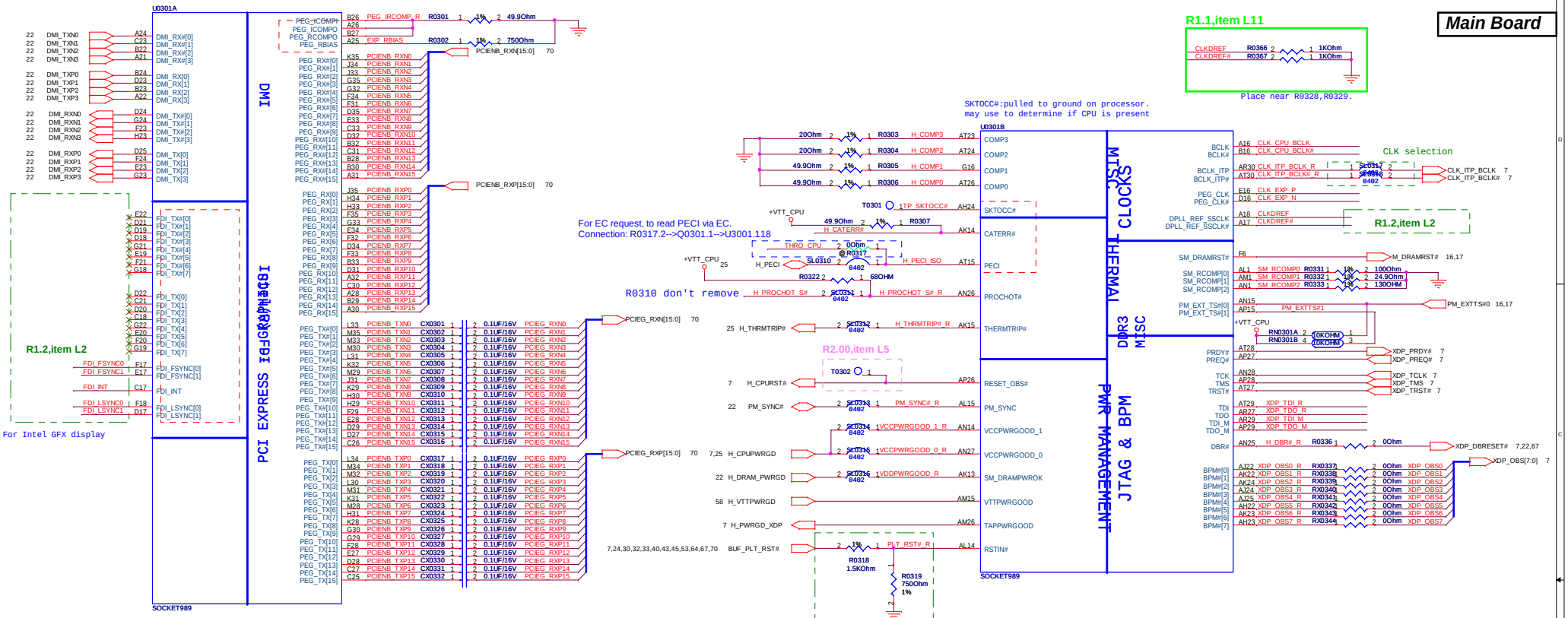
ASUSTeK COMPUTER INC. NB4

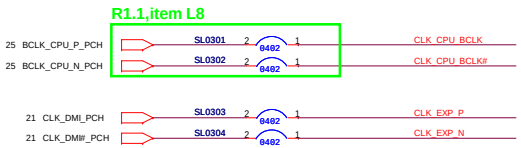
Title : System Setting

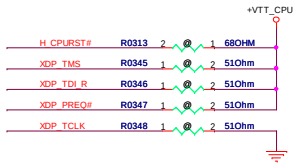
Engineer: James1_Wu

Size	Project Name	Rev
C	M60J	2.00

Date: Thursday, July 09, 2009 Sheet 2 of 99

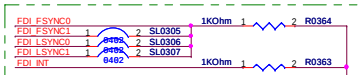




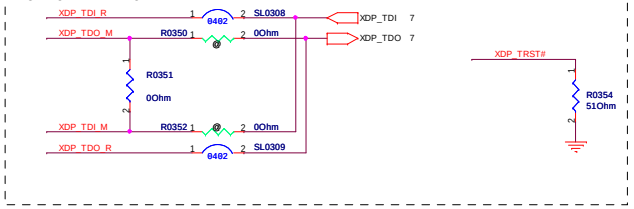


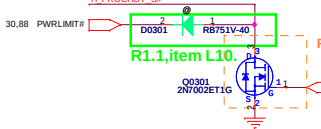
FDI disable: (For discrete graphic)

1. **NC:**
   FDI_TX#[0:7],FDI_TX[0:7],FDI_RX#[0:7],FDI_RX[0:7]
   VCC_AXGSENSE,VSS_AXGSENSE
2. **Pull-down to GND via 1KΩ ± 5% resistor:**
   FDI_FSYNC[0:1],FDI_LSYNC[0:1],FDI_INT,GFX_IMON
   ~15mW power saving.(DG R0.8 P.70)
3. **Connected to GND:**
   VCCAXG,
4. **Can be connected to GND directly:**
   DPLL_REF_CLK,DPLL_REF_CLK#
5. **Connect to +V1.05S rail:**
   VCCFDIPLL

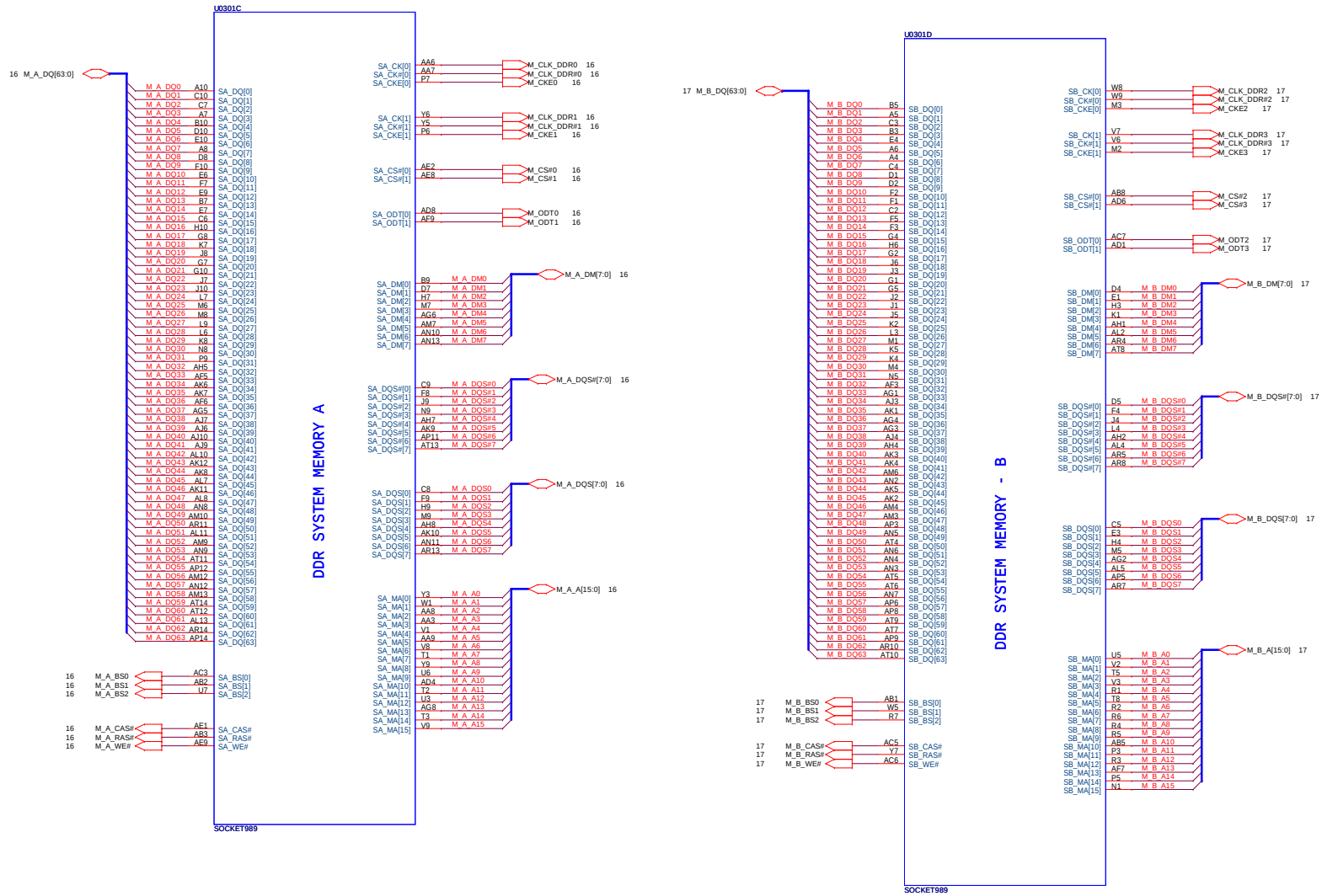


DG R1.1 P.83:
*FDI_FSYNC[0],FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1] can be ganged together with one resistor.
*On the other hand,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on PCH side can be left as no connect without any power or functional impact.

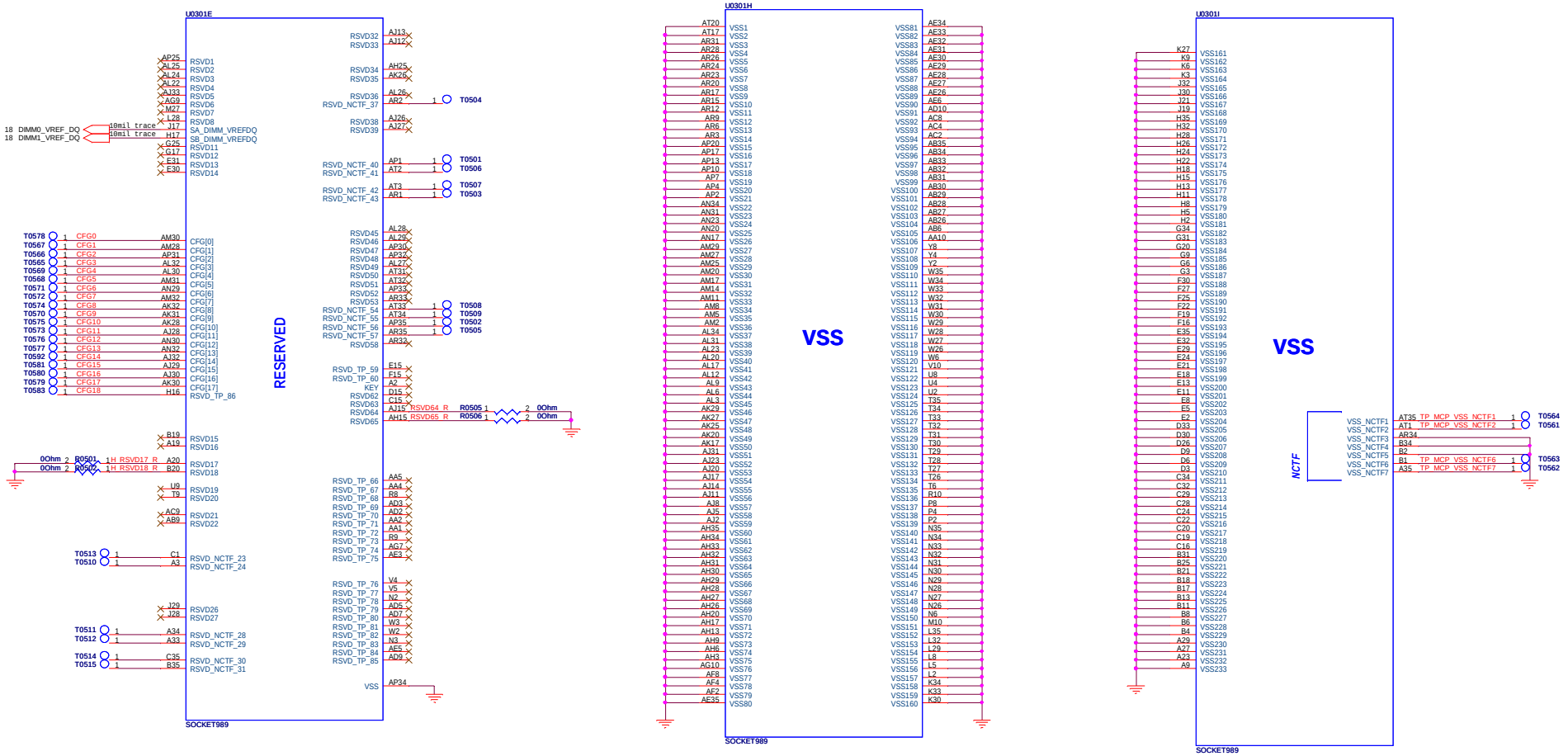




ASUSTeK COMPUTER INC. NB1	Title :	CPU(1)_DMI,PEG,FDI,CLK,MISC	
	Engineer:	James1_Wu	
Size: C	Project Name: M60J		Rev: 2.00
Date: Friday, July 10, 2009	Sheet 3 of 99		



ASUSTeK COMPUTER INC. NB1	Title : CPU(2)_DDR3		
	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Friday, July 10, 2009	Sheet 4 of 99		



CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)
- 11 = 1 x 16 PEG (Default)
- 10 = 2 x 8 PEG

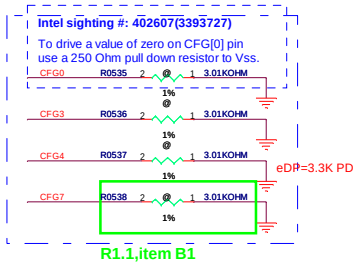
CFG[3]: PCIE Static Numbering Lane Reversal.(Auburndale Only)
- 1:Normal Operation (Default)
- 0:Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection.(Auburndale Only)
- 1:Disabled - No Physical Display Port attached to Embedded DisplayPort
- 0:Enabled - An external Display Port device is connected to the Embedded Display Port

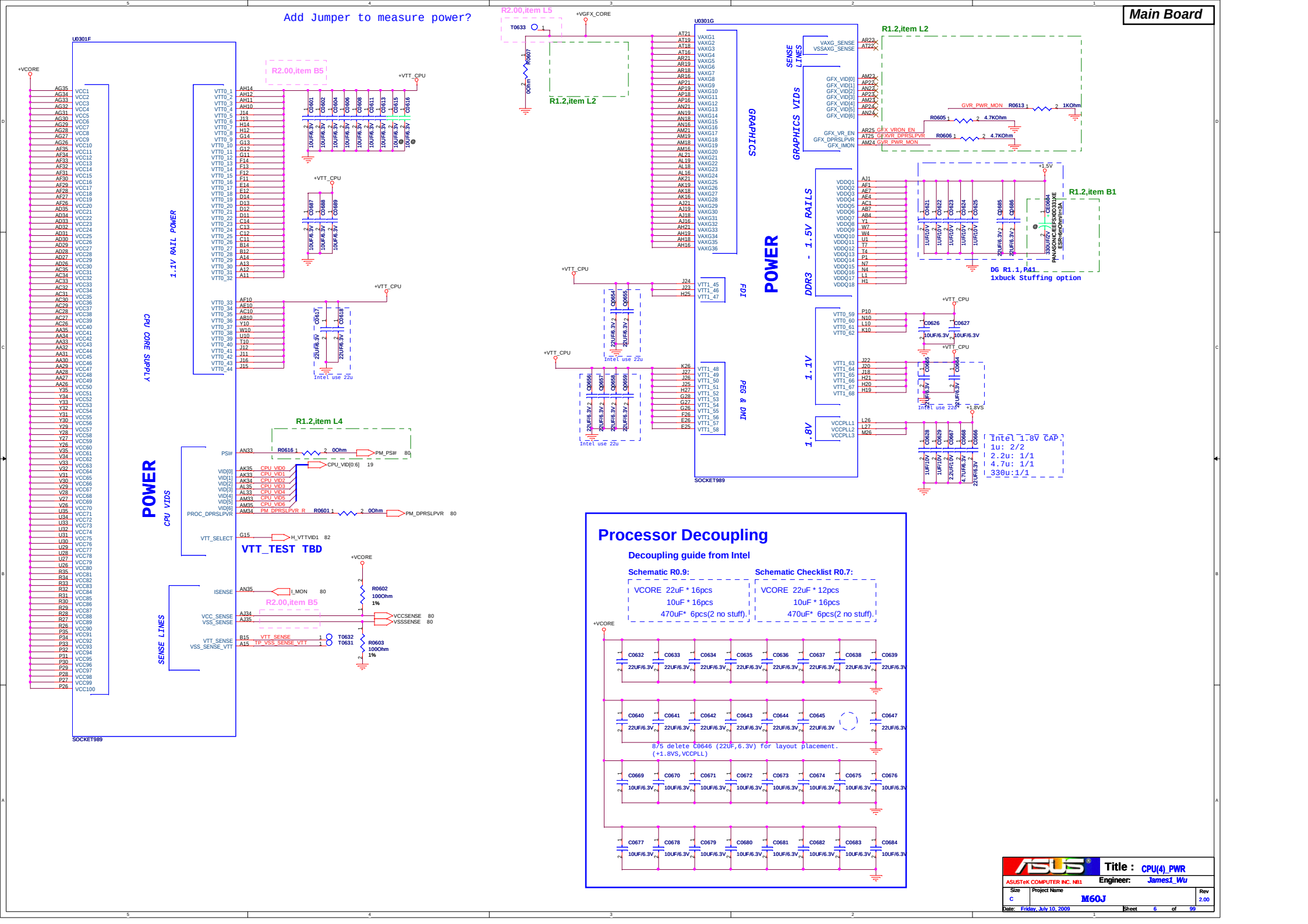
CFG[7]: Fixed for PCI Express 2.0 jitter specifications.(Clarksfield)
Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor
For a common motherboard design (for AUB and CFD),
the pull-down resistor should be used. Does not impact AUB functionality.
Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

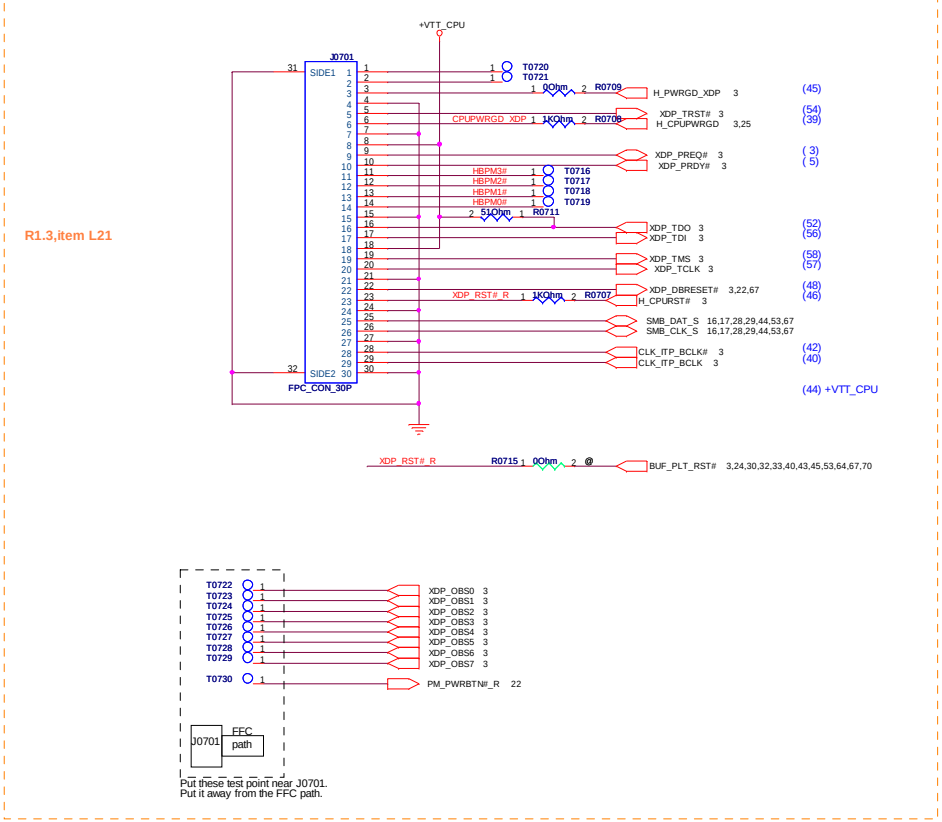
Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.



ASUSTeK COMPUTER INC. NB1	Title : CPU(3)_CFG,RSVD,GND	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 5 of 99	


Main Board
Add Jumper to measure power?
U0301F
POWER
CPU CORE SUPPLY
1.1V RAIL POWER
CPU VIDS
SENSE LINES
SOCKET989
R2.00,item B5
R2.00,item L5
R1.2,item L2
R1.2,item L4
R1.2,item B1
VTT_TEST TBD
U0301G
GRAPHICS
GRAPHICS VIDS
DDR3 - 1.5V RAILS
1.1V
1.8V
FDI
PEG & DMI
DG R1.1,P41
1xbuck Stuffing option
Intel 1.8V CAP.
1u: 2/2
2.2u: 1/1
4.7u: 1/1
330u:1/1
Processor Decoupling
Decoupling guide from Intel
Schematic R0.9:
VCORE 22uF * 16pcs
10uF * 16pcs
470uF* 6pcs(2 no stuff).
Schematic Checklist R0.7:
VCORE 22uF * 12pcs
10uF * 16pcs
470uF* 6pcs(2 no stuff).
875 delete C0646 (22UF,6.3V) for layout placement.
(+1.8VS,VCCPLL)
Title : CPU(4)_PWR
Engineer: James1_Wu
ASUSTeK COMPUTER INC. NB1
Size C
Project Name M60J
Rev 2.00
Date: Friday, July 10, 2009
Sheet 6 of 99

CPU XDP connector



R1.3,item L21

ASUSTeK COMPUTER INC. NB1	Title : CPU(5)_XDP	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 7 of 99	

ASUS	Title : NB_****		
ASUSTeK COMPUTER INC. NB1	Engineer: James1_Wu		
Size: Custom	Project Name: M60J		Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 8 of 99		

Main Board

ASUS	Title : NB_****	
ASUSTeK COMPUTER INC. NB1	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 9 of 99	

Main Board

ASUS	Title : NB_****	
ASUSTeK COMPUTER INC. NB1	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 10 of 99	

Main Board

ASUS	Title : NB_****	
ASUSTeK COMPUTER INC. NB1	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 11 of 99	

Main Board

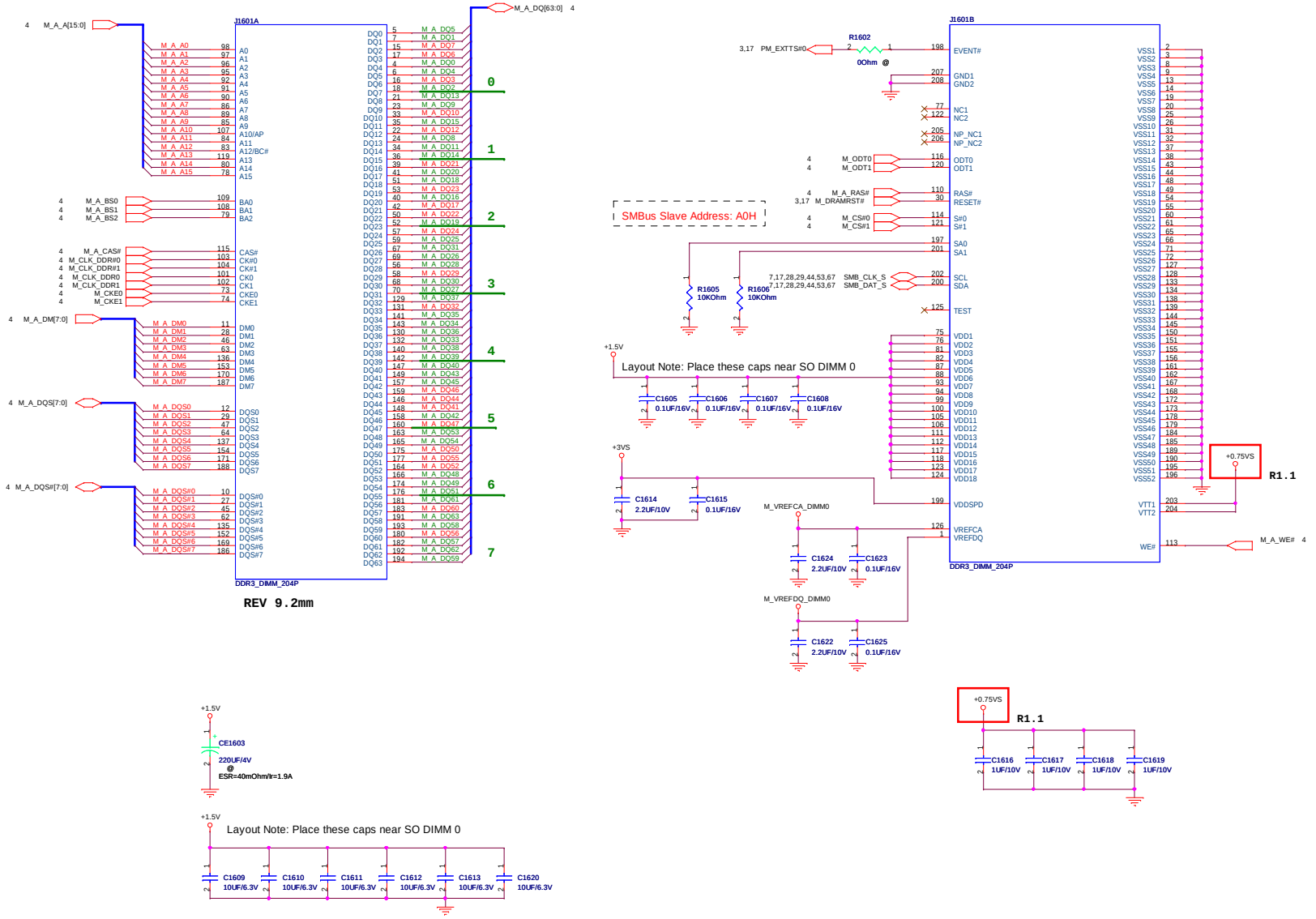
ASUS	Title : NB_****	
ASUSTeK COMPUTER INC. NB1	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 12 of 99	

Main Board

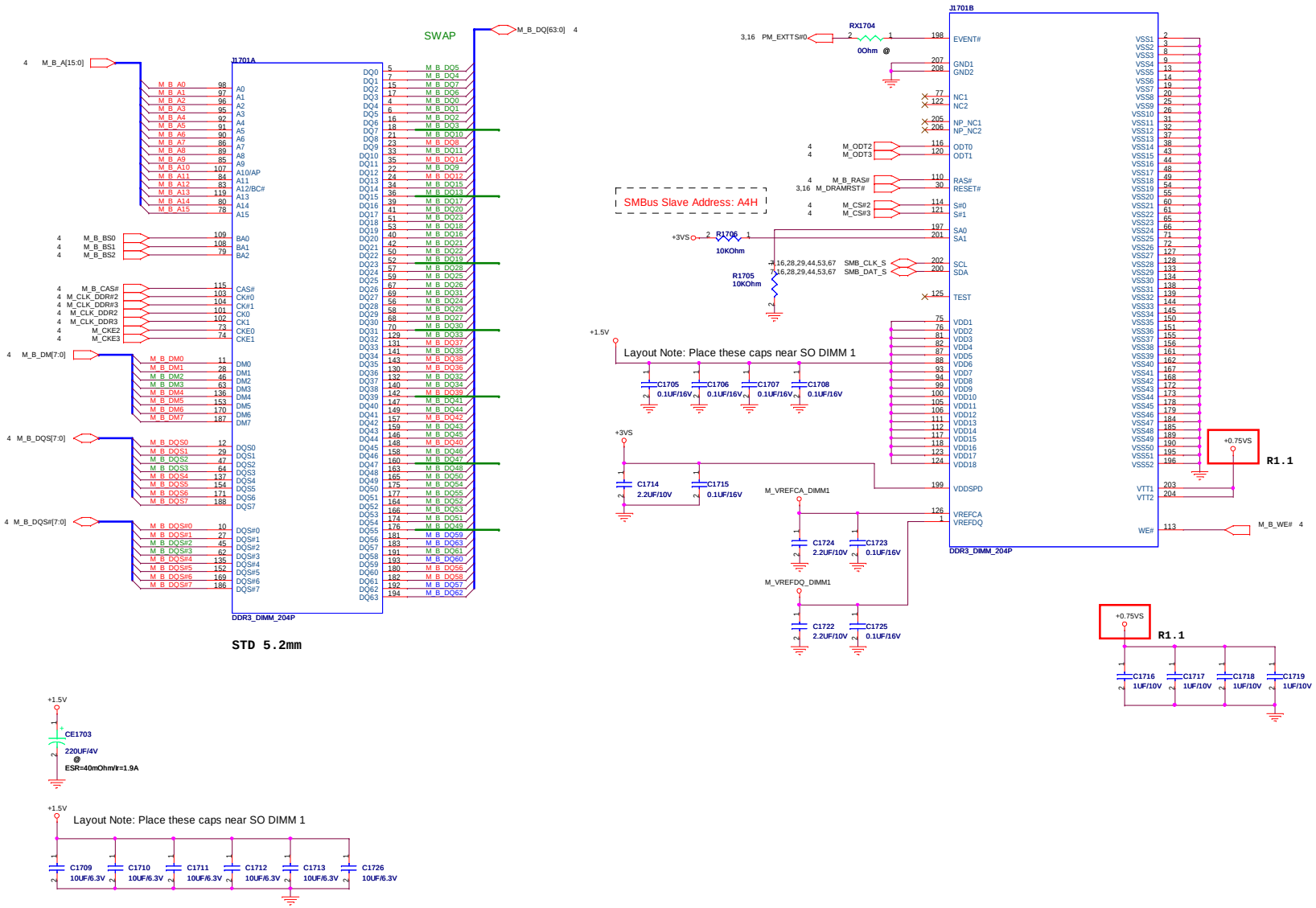
ASUS	Title : NB_****	
ASUSTeK COMPUTER INC. NB1	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 13 of 99	

Title :				
ASUSTeK COMPUTER INC. NB6	Engineer: James1_Wu			
Size A	Project Name M60J			Rev 2.00
Date: Thursday, July 02, 2009		Sheet 14 of 99		

Title :			
ASUSTeK COMPUTER INC. NB6	Engineer: James1_Wu		
Size: A	Project Name: M60J		Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 15 of 99		



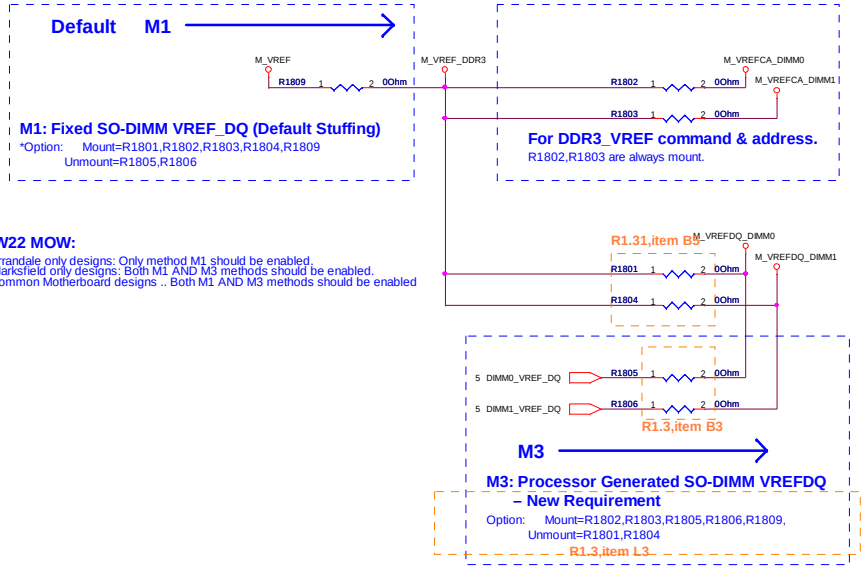
ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_0		
	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Friday, July 10, 2009	Sheet 16 of 99		



ASUSTeK COMPUTER INC. NB6	Title DDR3 SO-DIMM_1	Engineer: James1_Wu
Size C	Project Name M60J	Rev 2.00
Date: Friday, July 10, 2009	Sheet 17 of 99	

DDR3 Vref

Intel Document Number: 400755
Calpella Clarksfield DDR3 SO-DIMM VREFDQ
Platform Design Guide Change Details

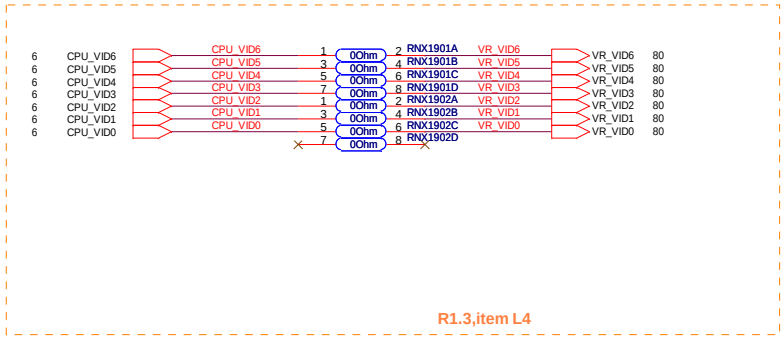


WW22 MOW:

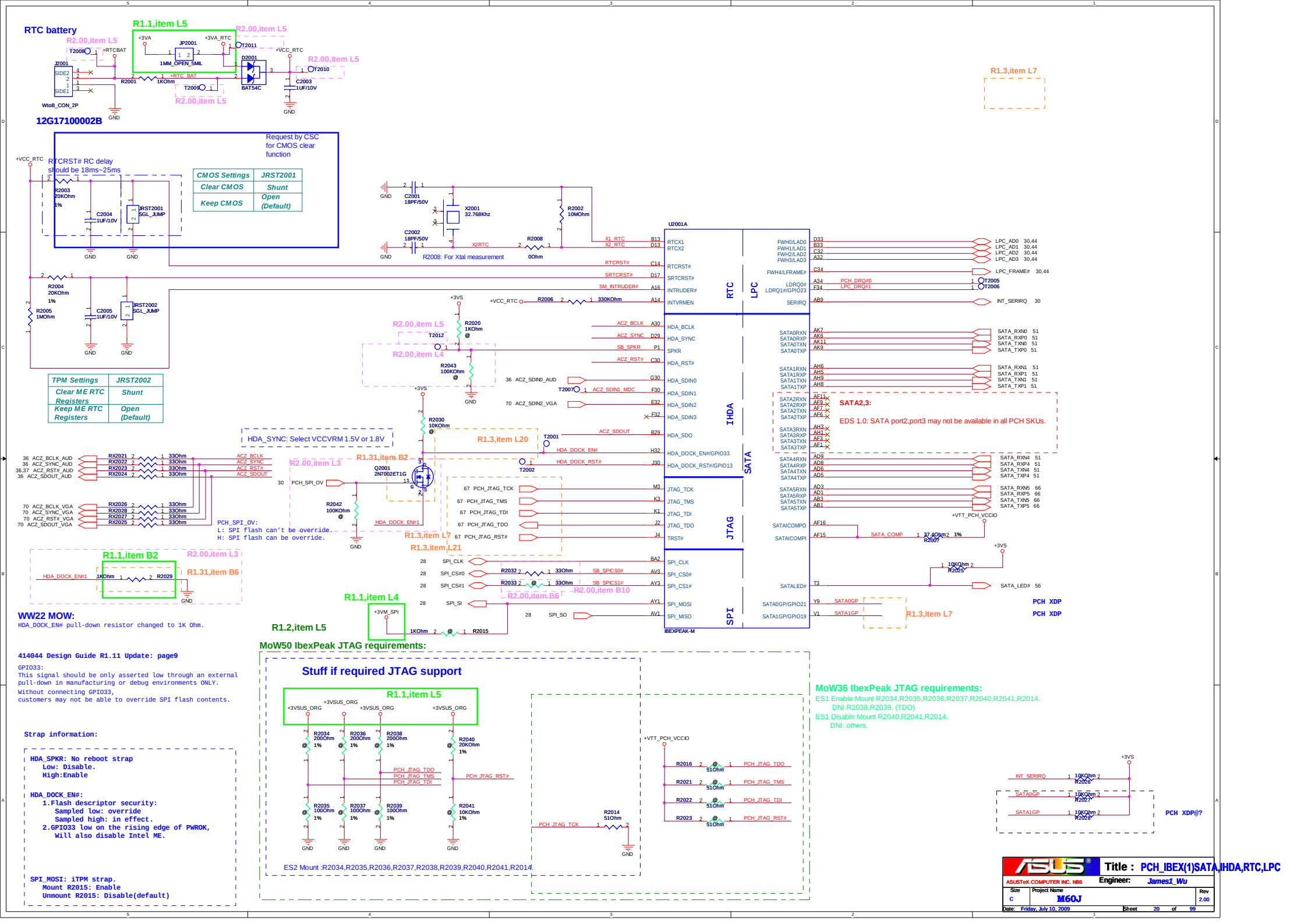
For Arrandale only designs: Only method M1 should be enabled.
For Clarksfield only designs: Both M1 AND M3 methods should be enabled.
For Common Motherboard designs .. Both M1 AND M3 methods should be enabled

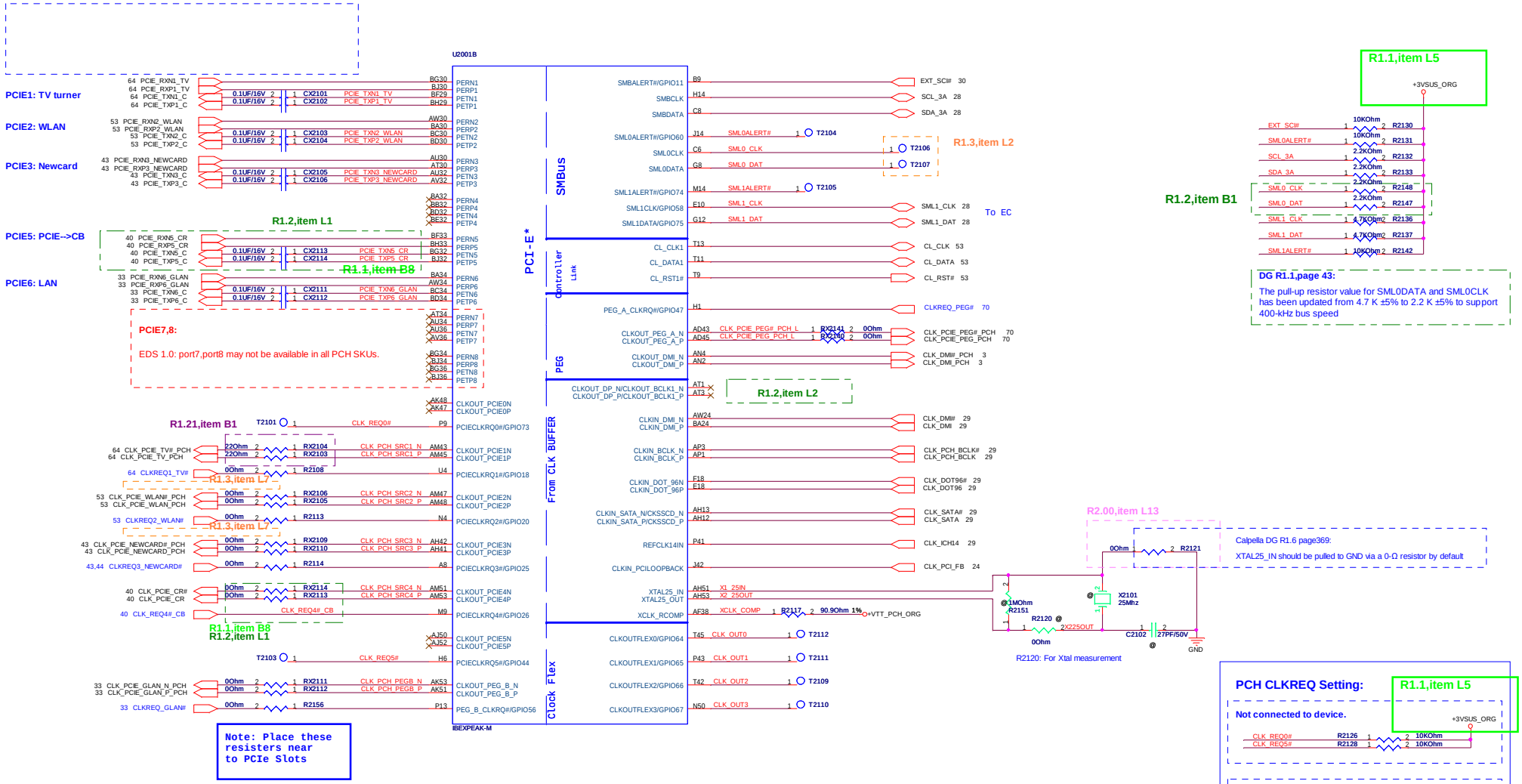
R1.3,item L3

ASUSTeK COMPUTER INC. NB6	Title DDR3 CA_DQ VOLTAGE	
	Engineer: James1_Wu	
Size C	Project Name M60J	Rev 2.00
Date: Friday, July 10, 2009	Sheet 18 of 99	

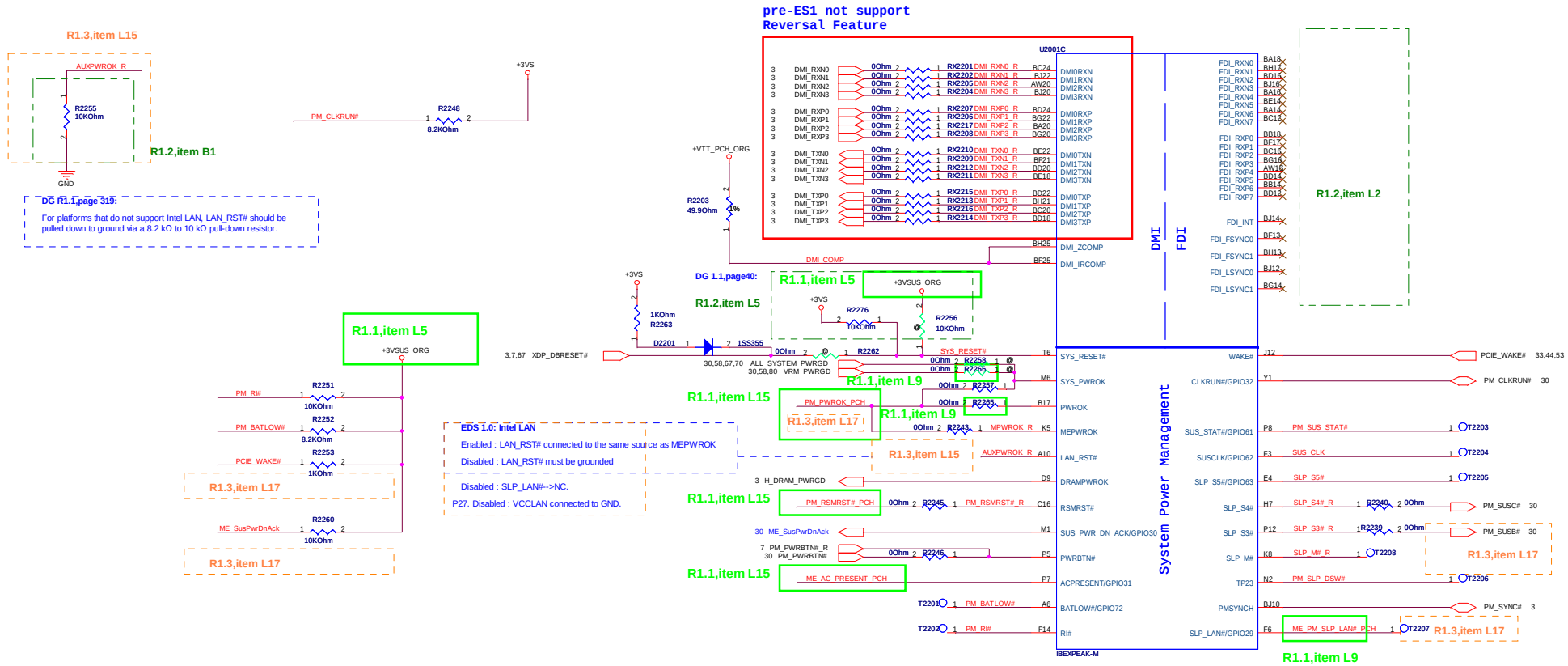


ASUS	Title : VID		
ASUSTeK COMPUTER INC. NB1	Engineer:		
Size: Custom	Project Name: M60J		Rev: 2.00
Date: Friday, July 10, 2009	Sheet 19 of 99		

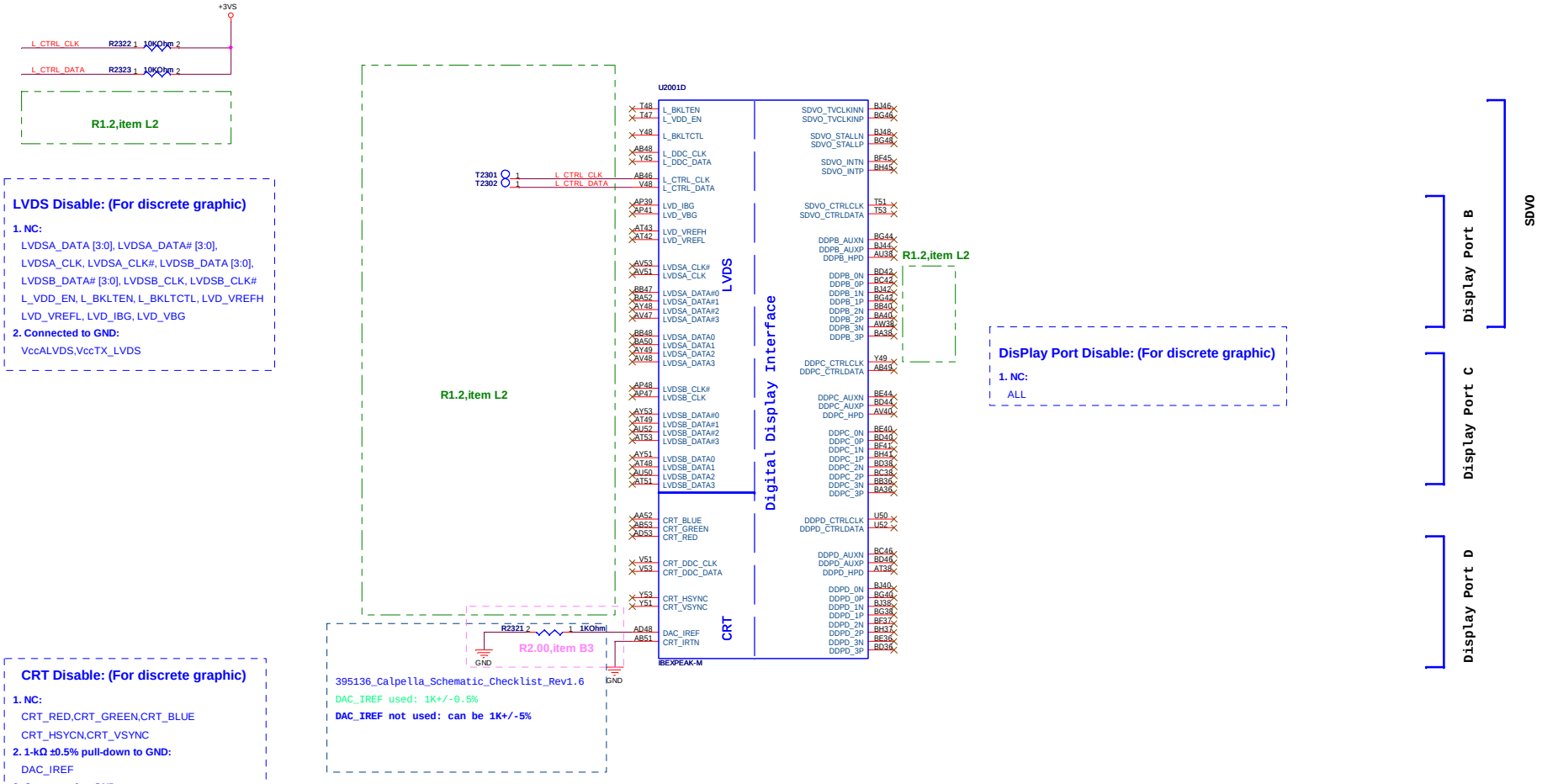

RTC battery
R1.1,item L5
R2.00,item L5
12G17100002B
Request by CSC for CMOS clear function
RTCRST# RC delay should be 18ms~25ms
CMOS Settings | JRST2001
Clear CMOS | Shunt
Keep CMOS | Open (Default)
TPM Settings | JRST2002
Clear ME RTC Registers | Shunt
Keep ME RTC Registers | Open (Default)
R2008: For Xtal measurement
U2001A
RTC
LPC
IHDA
SATA
JTAG
SPI
IBEXPEAK-M
SATA2,3:
EDS 1.0: SATA port2,port3 may not be available in all PCH SKUs.
HDA_SYNC: Select VCCVRM 1.5V or 1.8V
PCH_SPI_0V:
L: SPI flash can't be override.
H: SPI flash can be override.
R1.3,item L7
R1.3,item L20
R1.3,item L21
R1.31,item B2
R1.31,item B6
R2.00,item B6
R2.00,item B10
R1.1,item L4
R1.2,item L5
WW22 MOW:
HDA_DOCK_EN# pull-down resistor changed to 1K Ohm.
414044 Design Guide R1.11 Update: page9
GPIO33:
This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.
Without connecting GPIO33,
customers may not be able to override SPI flash contents.
Strap information:
HDA_SPKR: No reboot strap
Low: Disable.
High:Enable
HDA_DOCK_EN#:
1.Flash descriptor security:
Sampled low: override
Sampled high: in effect.
2.GPIO33 low on the rising edge of PWROK,
Will also disable Intel ME.
SPI_MOSI: iTPM strap.
Mount R2015: Enable
Unmount R2015: Disable(default)
MoW50 IbexPeak JTAG requirements:
Stuff if required JTAG support
ES2 Mount :R2034,R2035,R2036,R2037,R2038,R2039,R2040,R2041,R2014.
MoW36 IbexPeak JTAG requirements:
ES1 Enable:Mount R2034,R2035,R2036,R2037,R2040,R2041,R2014.
DNI R2038,R2039. (TDO)
ES1 Disable:Mount R2040,R2041,R2014.
DNI: others.
PCH XDP
PCH XDP
PCH XDP@?
Title : PCH_IBEX(1)SATA,IHDA,RTC,LPC
ASUSTeK COMPUTER INC. NB6
Engineer: James1_Wu
Size C
Project Name M60J
Rev 2.00
Date: Friday, July 10, 2009
Sheet 20 of 99



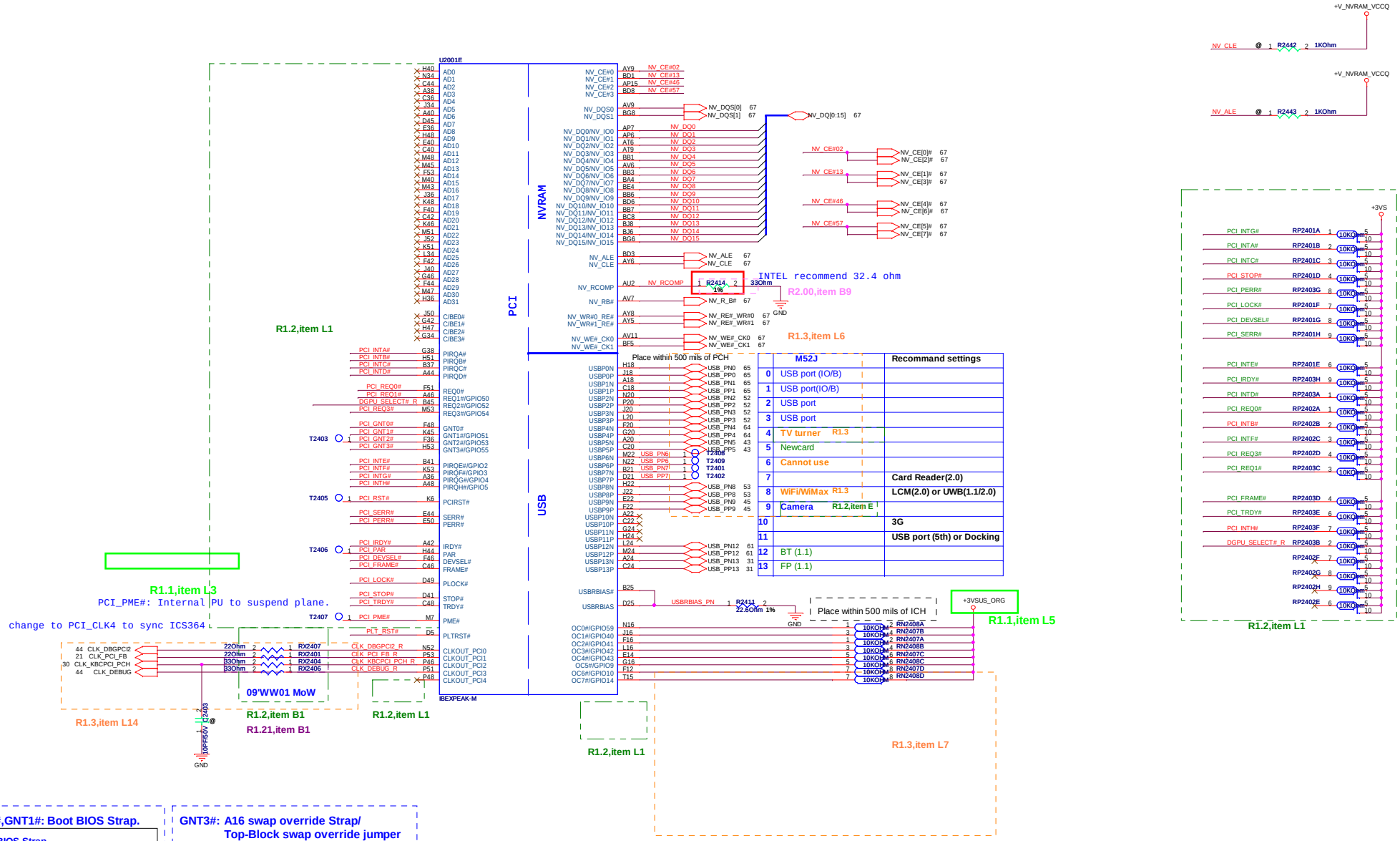
Title : PCH_IBEX(2)_PCIE,CLK,SMB,PEG		
ASUSTeK COMPUTER INC. NB6	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 21 of 99	



ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(3)_FDI,DMI,SYS PWR		
	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Friday, July 10, 2009	Sheet 22 of 99		



ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(4)_DP,LVDS,CRT		
	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Monday, July 06, 2009	Sheet 23 of 99		



	M52J	Recommand settings
0	USB port (IO/B)	
1	USB port(IO/B)	
2	USB port	
3	USB port	
4	TV turner R1.3	
5	Newcard	
6	Cannot use	
7		Card Reader(2.0)
8	WiFi/WiMax R1.3	LCM(2.0) or UWB(1.1/2.0)
9	Camera R1.2,item E	
10		3G
11		USB port (5th) or Docking
12	BT (1.1)	
13	FP (1.1)	

GNT0#,GNT1#: Boot BIOS Strap.

Boot BIOS Strap

PCI_GNT1#	PCI_GNT0#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI **(PCH)**

Sampled on rising edge of PWROK.

PCI_GNT0# R2440 1 @ 2 1KOhm
PCI_GNT1# R2441 1 @ 2 1KOhm
GND

GNT3#: A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default

PCI_GNT3# R2444 1 @ 2 1KOhm
GND

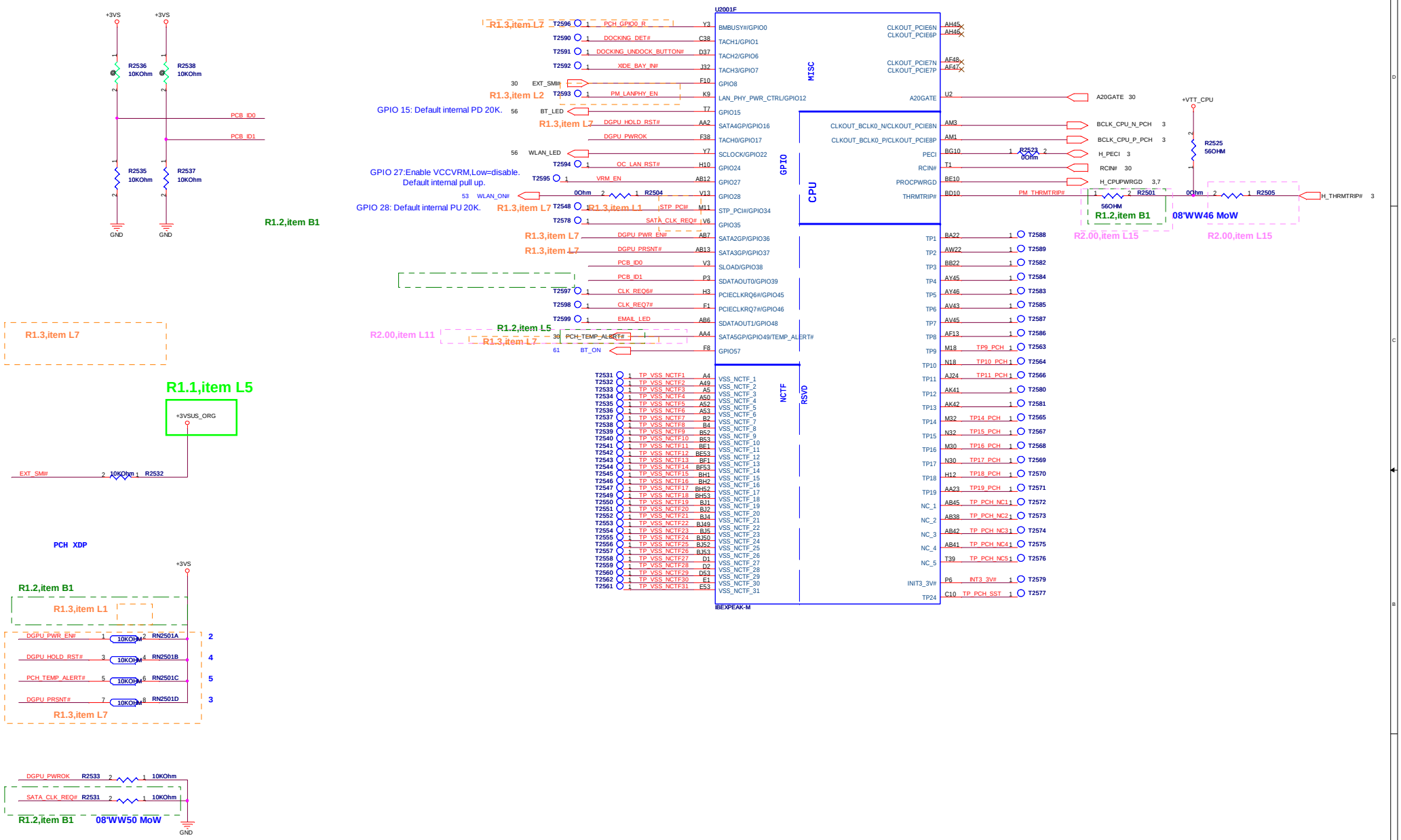
ASUSTeK COMPUTER INC. NB6

Title : PCH_IBEX(5)_PCI,NVRAM,USB

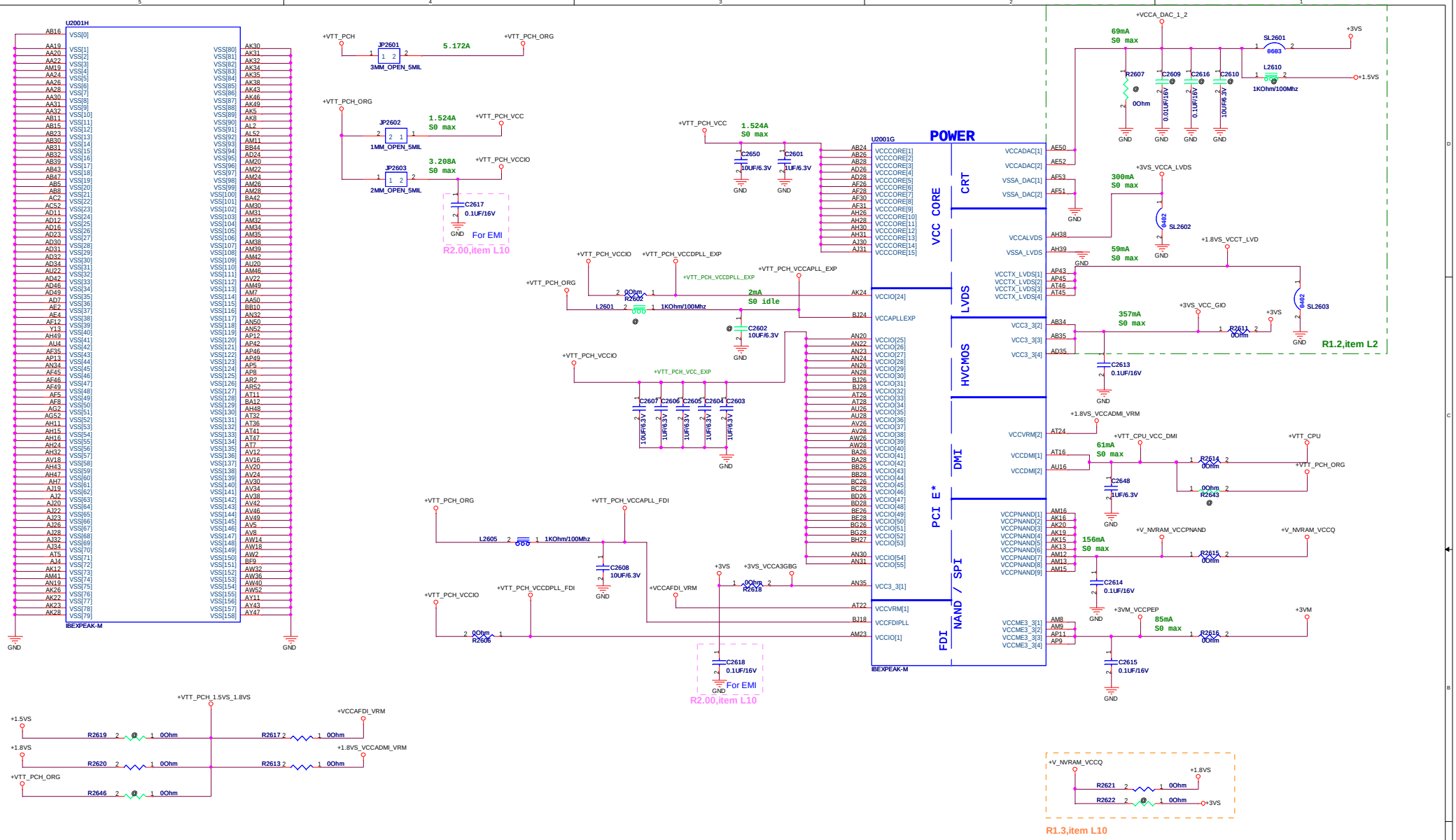
Engineer: James1_Wu

Size	Project Name	Rev
C	M60J	2.00

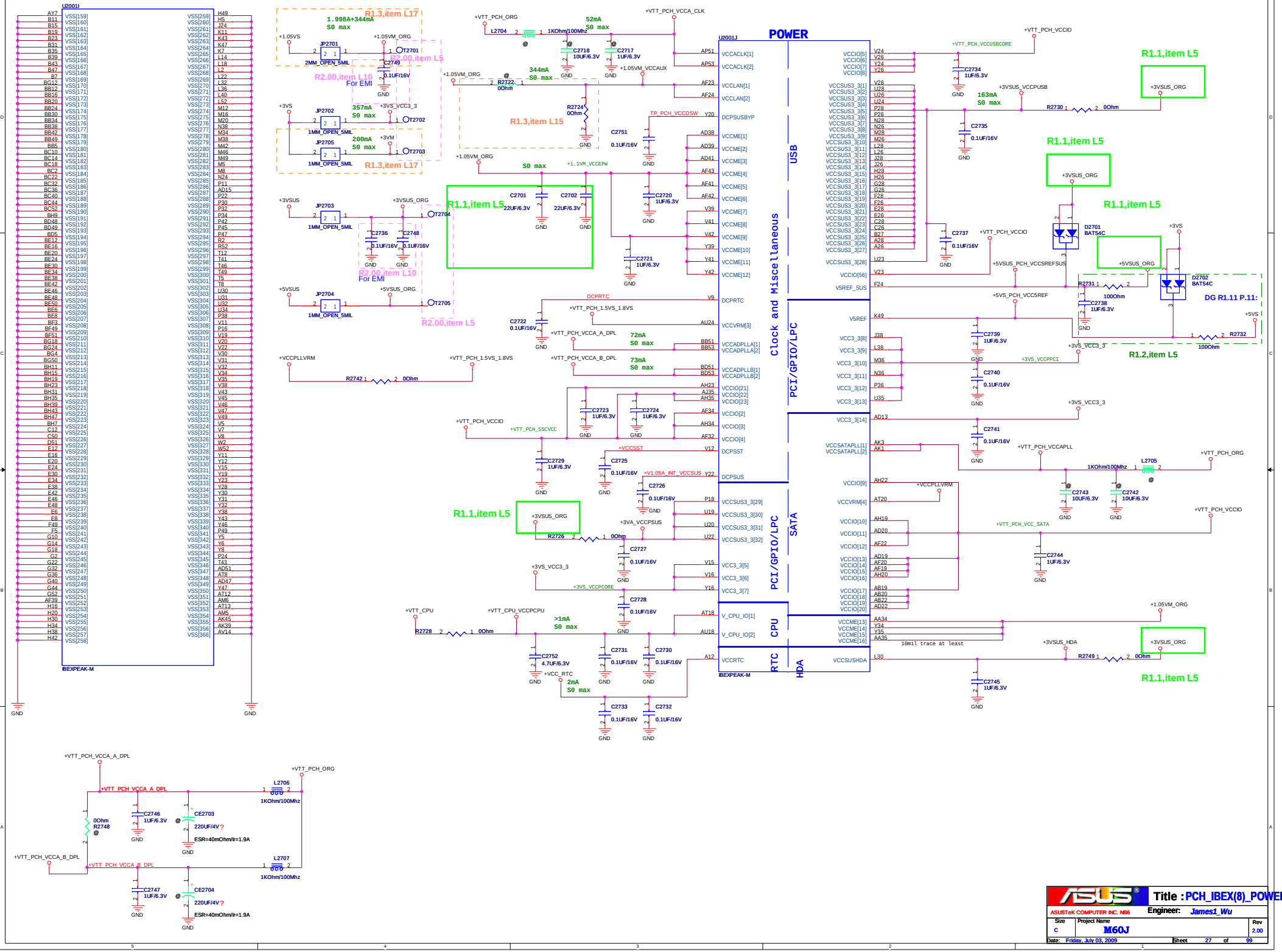
Date: Friday, July 10, 2009 Sheet 24 of 99



Title : PCH_IBEX(6)CPU,GPIO,MISC		
ASUSTeK COMPUTER INC. NB6	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 25 of 99	



ASUSTeK COMPUTER INC. NB6	Title : PCH_IBEX(7)_POWER,GND		
	Engineer: James1_Wu		
Size: C	Project Name: M60J		Rev: 2.00
Date: Friday, July 03, 2009	Sheet 26 of 99		



Title : PCH_IBEX(8)_POWER,GND

ASUSTeK COMPUTER INC. N86

Engineer: James1_Wu

Size	Project Name	Rev
C	M60J	2.00

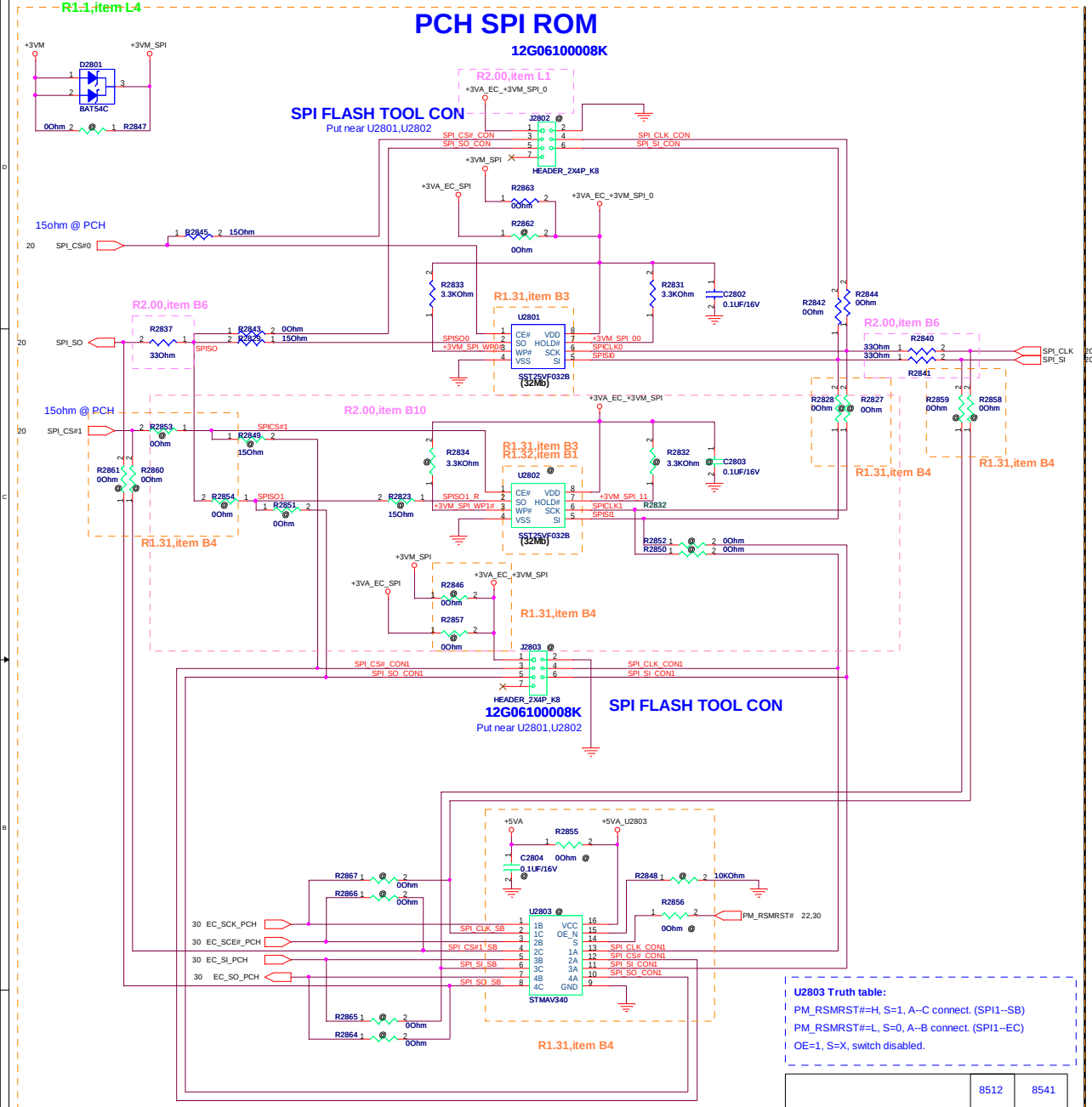
Date: Friday, July 03, 2009 Sheet 27 of 99

PCH SPI ROM

12G06100008K

R1.1,item L4

R1.2,item L6



U2803 Truth table:

PM_RSMRST#=H, S=1, A--C connect. (SPI1--SB)

PM_RSMRST#=L, S=0, A--B connect. (SPI1--EC)

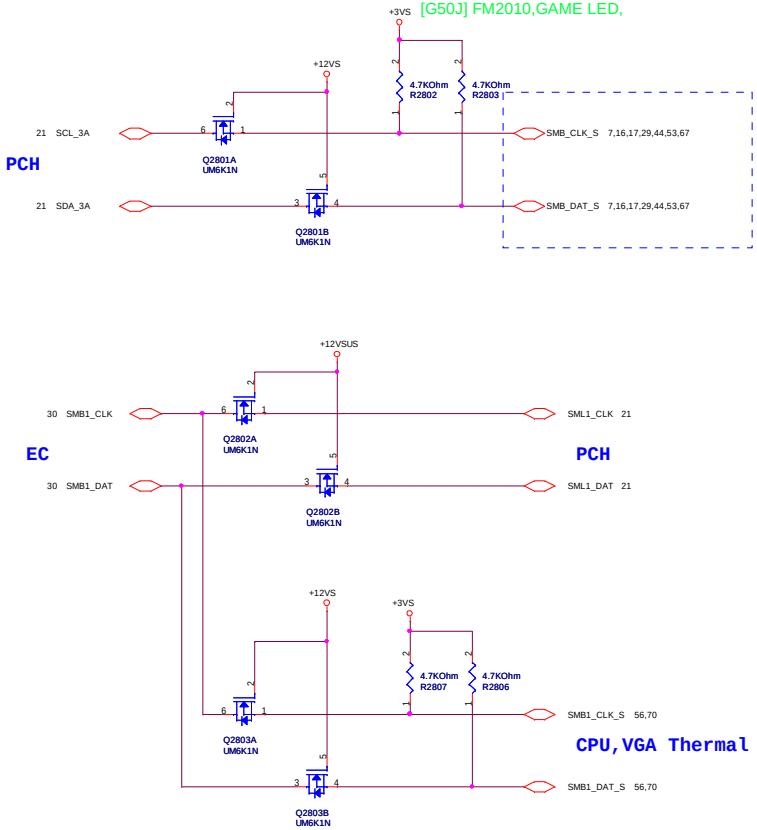
OE=1, S=X, switch disabled.

	8512	8541
R2853,U3003,R2440 R2854,R3053,R2441 R2827,R3043, R2828,C3019 R2846 R3002,R2858, R3003,R2859, R3004,R2860, R3005,R2861, R2855 R2857 U2803 R2848 C2804 R2849, R2850, R2851, R2852,	Mount	DNI
R3002,R2858,R2849, R3003,R2859,R2850, R3004,R2860,R2851, R3005,R2861,R2852, R2855 R2857 U3003,R2440 R3053,R2441 R3043, C3019	DNI	Mount

SMBUS Link device:

[M52J] SPD, CLKGEN,DEBUG,WLAN, CPU XDP,PCH XDP,VID CONTROLLER

[G50J] FM2010,GAME LED,



SUBSYSTEM ID : SB_

SUBSYSTEM ID : ROM

ASUS	Title : PCH_SPI ROM,OTH
ASUSTeK COMPUTER INC. NB6	Engineer: James1_Wu
Size: C	Project Name: M60J
Rev: 2.00	
Date: Friday, July 10, 2009	Sheet 28 of 99

R1.3,item L1

Layout note:

R2916,R2917:as close as possible to the net FSLC of RX2907.

The oc and uc pin of ASM8272 are open drain in next version.

R1.31,item B2

R2906: For Xtal measurement

R1.3,item B10

BCLK	FSLC
133	0
100	1

Layout note:

VDD_3.3: 5pin -->0.1uF to each pin put it at pin5,29

Layout note:

VDD: 5pin -->0.1uF to each pin put it at pin1,15,17,18,24

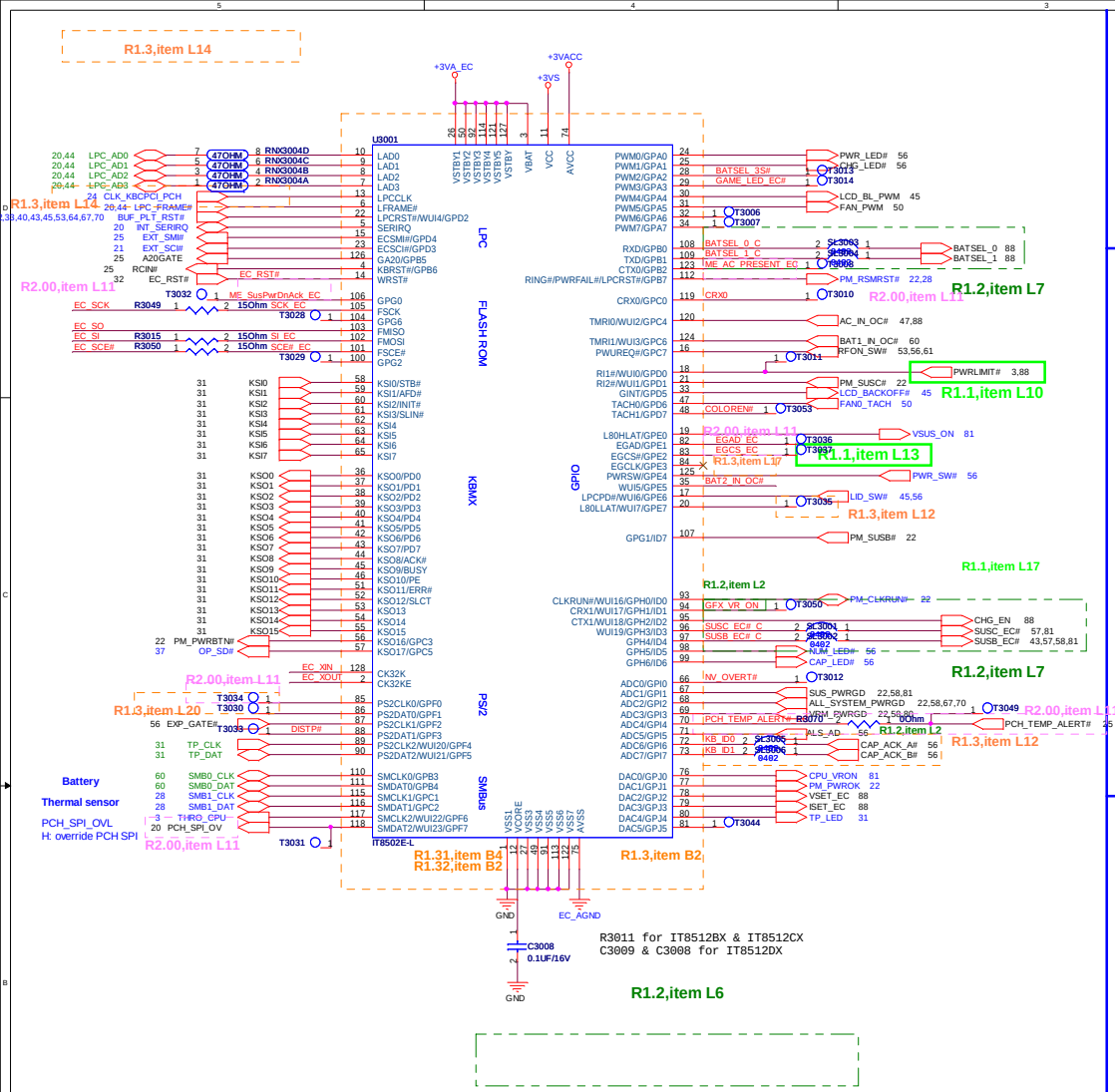
9LRS3197 / 9LVS3162 Colay

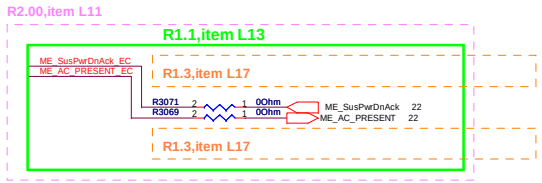
9LRS3197----mount L2904,unmount L2903

9LVS3162----mount L2903,unmount L2904,R2921

R2.00,item L14

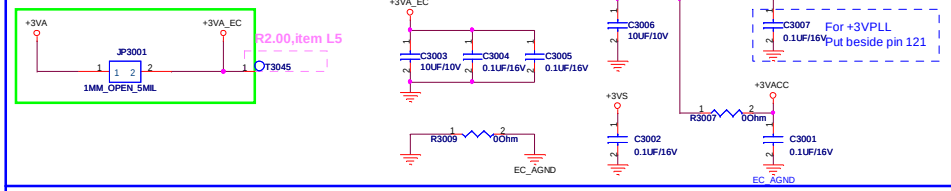
Title :	CLK_ICS9LRS3197
Engineer:	James1_Wu
ASUSTeK COMPUTER INC. NB4	
Size: C	Project Name: M60J
Rev: 2.00	
Date: Friday, July 10, 2009	Sheet 29 of 99



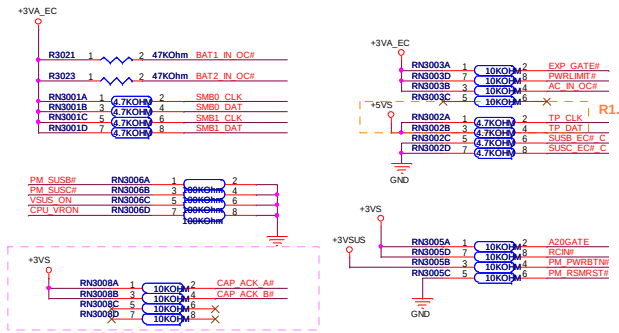


Calpella DG R1.6,page 237:
ME_SusPwrDnAck: Required for all platforms
ME_AC_PRESENT: Required for all platforms except platforms with Ignition Firmware.(10K PU optional)

For IT8752 Power



For PU / PD

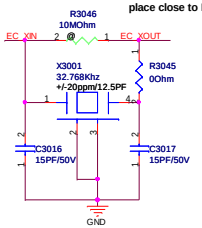


iAMT EC strapping need to check

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH9 GPIO.

For X'tal

Note:
Cload=12.5PF place close to EC



For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

Note: It can be programmable by EC fireware.

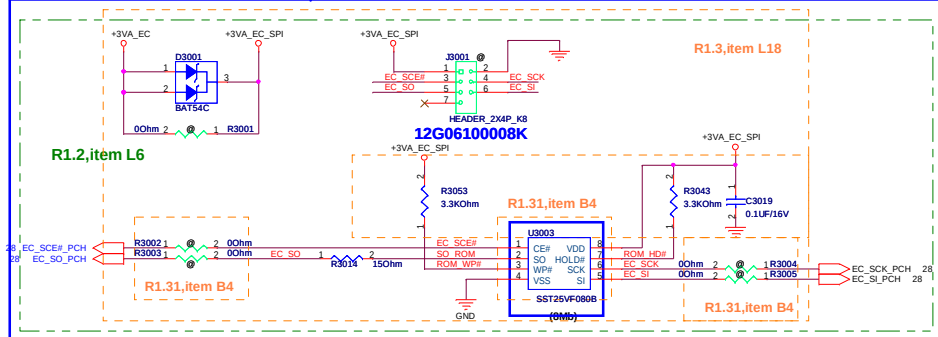
PP Enable

Note: Default Int. Pull-Low

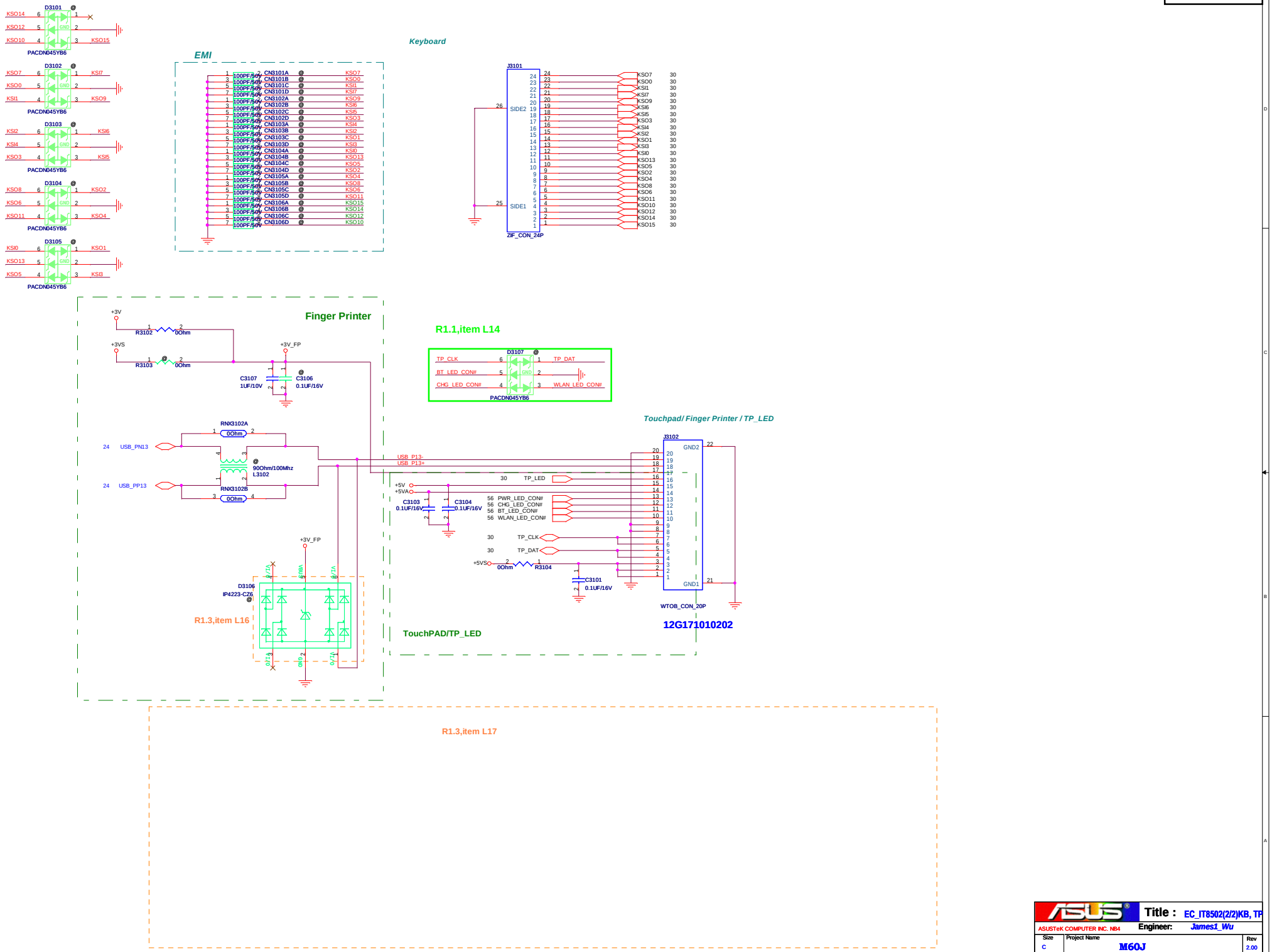
R3045: For Xtal measurement

For iAMT pin name

AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

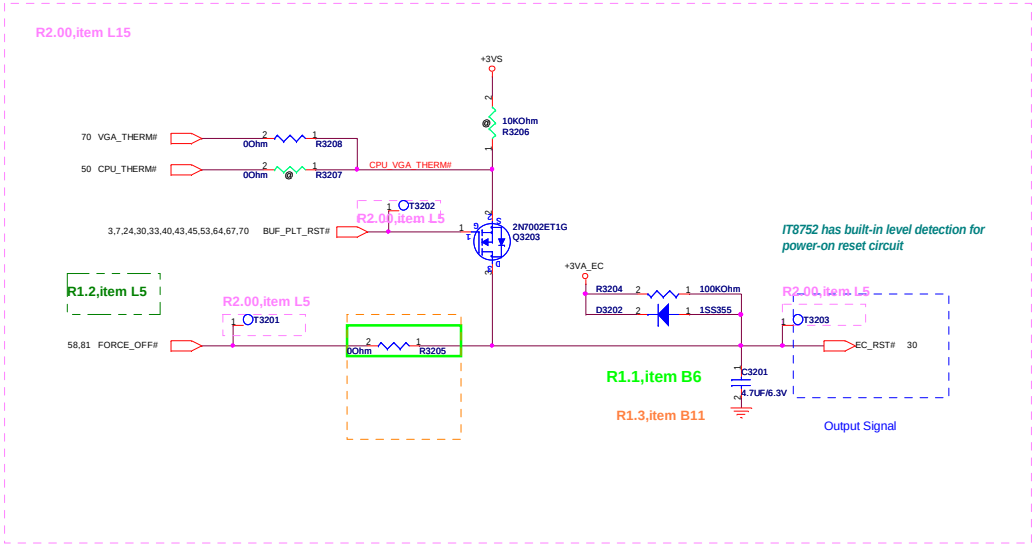


ASUSTeK COMPUTER INC. NB4	Title : EC_IT8502	Engineer: James1_Wu
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 30 of 99	

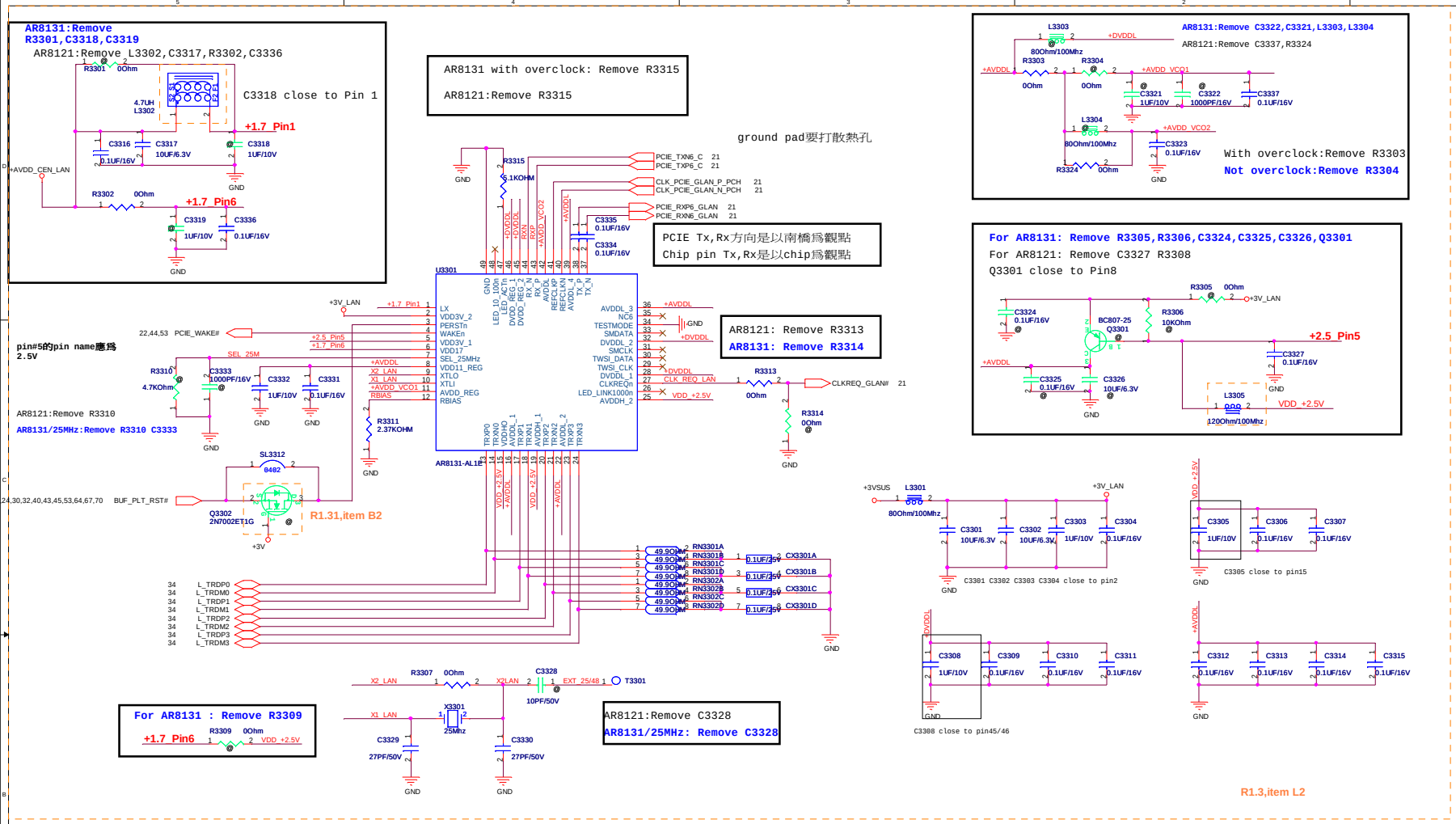


ASUSTeK COMPUTER INC. NB4	Title : EC_IT8502(2/2)KB, TP	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 31 of 99	

Thermal Policy

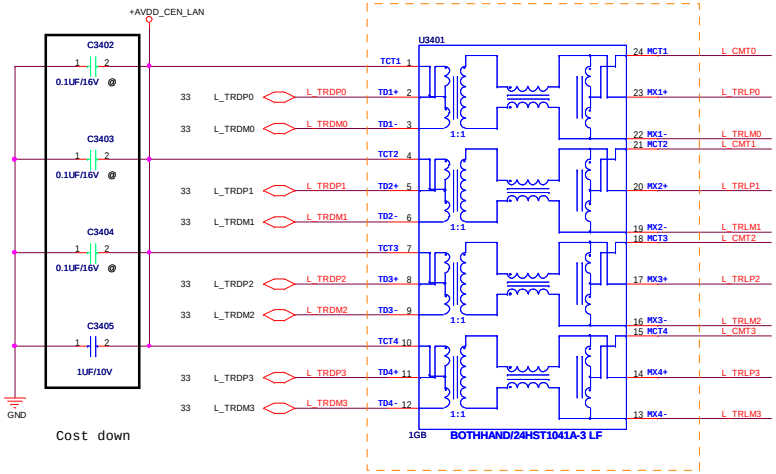


ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 32 of 99	

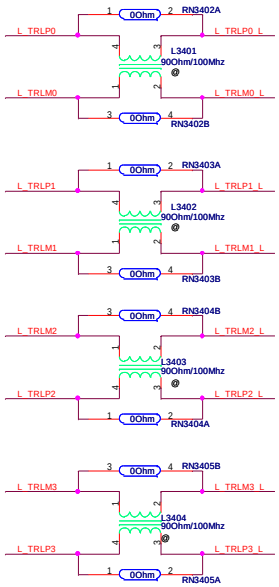


ASUS	Title : LAN-AR8131	
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu	
Size C	Project Name M60J	Rev 2.00
Date: Friday, July 10, 2009	Sheet 33 of 99	

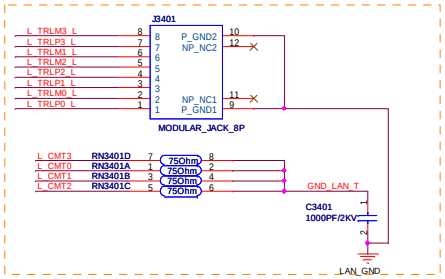
R1.3,item L2

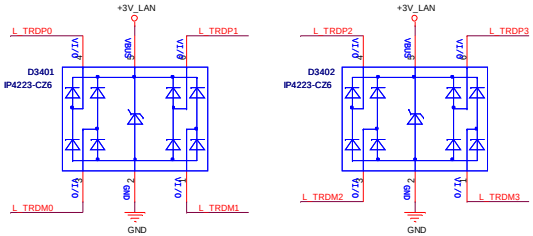


Cost down



connector without modem



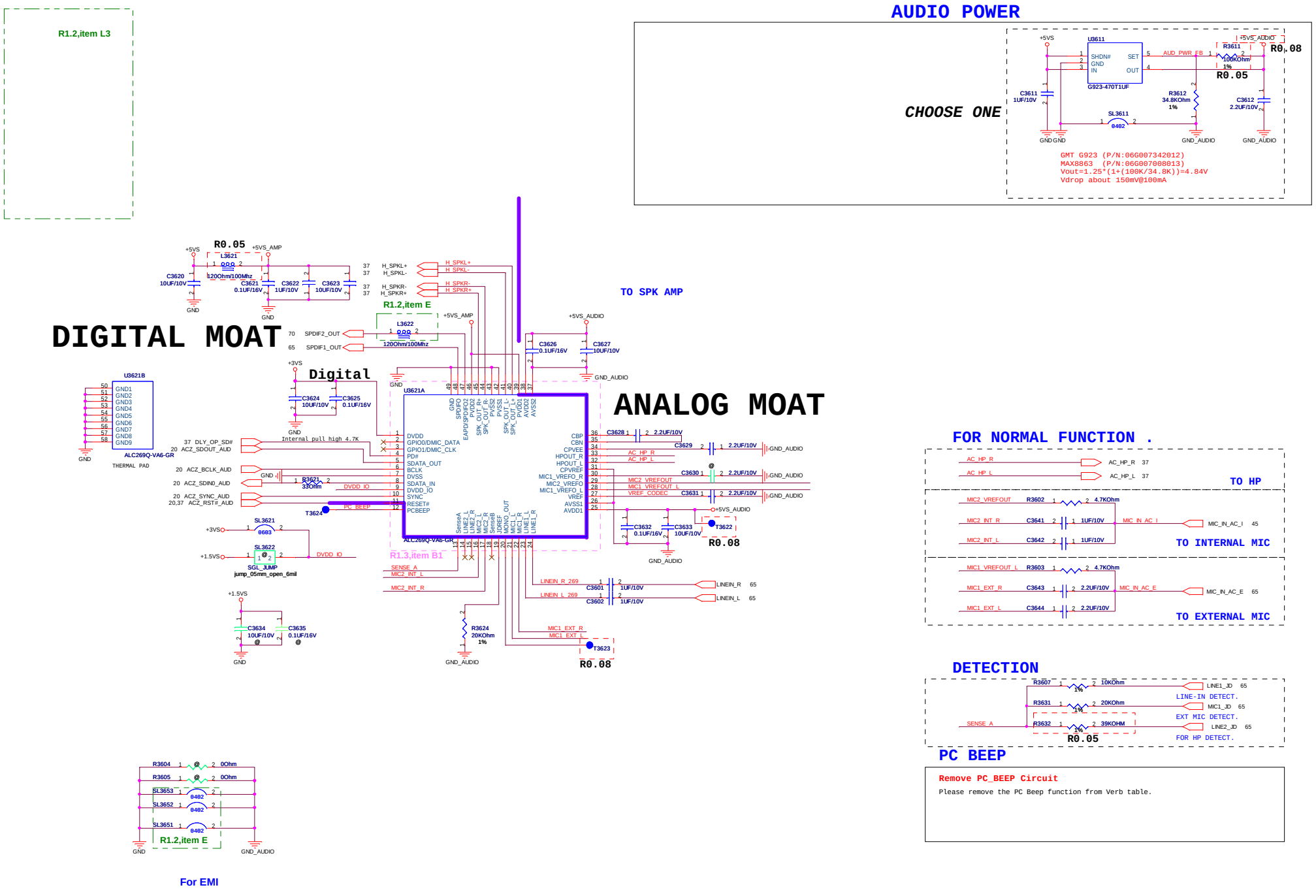


R2.00,item L10
For EMI

Place near chassis GND

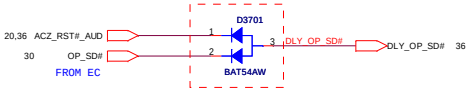
ASUSTeK COMPUTER INC. NB4	Title : LAN_RJ45		
	Engineer: James1_Wu		
Size C	Project Name M52J		Rev 2.00
Date: Friday, July 10, 2009	Sheet 34 of 99		

ASUSTeK COMPUTER INC. NB4	Title : MDC_****	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 35 of 99	

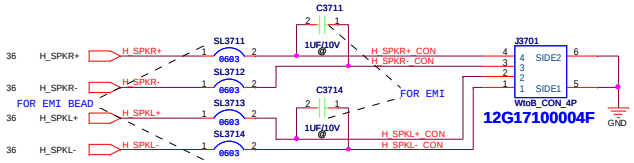

AUDIO POWER
CHOOSE ONE
U3611
G923-470T1UF
GMT G923 (P/N:06G007342012)
MAX8863 (P/N:06G007008013)
Vout=1.25*(1+(100K/34.8K))=4.84V
Vdrop about 150mV@100mA
R1.2,item L3
DIGITAL MOAT
ANALOG MOAT
TO SPK AMP
R1.2,item E
U3621B
ALC269Q-VA6-GR
THERMAL PAD
U3621A
Digital
R1.3,item B1
FOR NORMAL FUNCTION .
TO HP
TO INTERNAL MIC
TO EXTERNAL MIC
DETECTION
LINE-IN DETECT.
EXT MIC DETECT.
FOR HP DETECT.
PC BEEP
Remove PC_BEEP Circuit
Please remove the PC Beep function from Verb table.
For EMI
Title : CODEC ALC 269
Engineer: James1_Wu
ASUSTeK COMPUTER INC. NB2
M60J
Rev 2.00
Date: Friday, July 10, 2009
Sheet 36 of 99

R1.2,item L3

MUTE CONTROL



R0.05 R0.06



ASUSTeK COMPUTER INC. NB2	Title : AUDIO AMP		
	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Friday, July 10, 2009	Sheet 37 of 99		

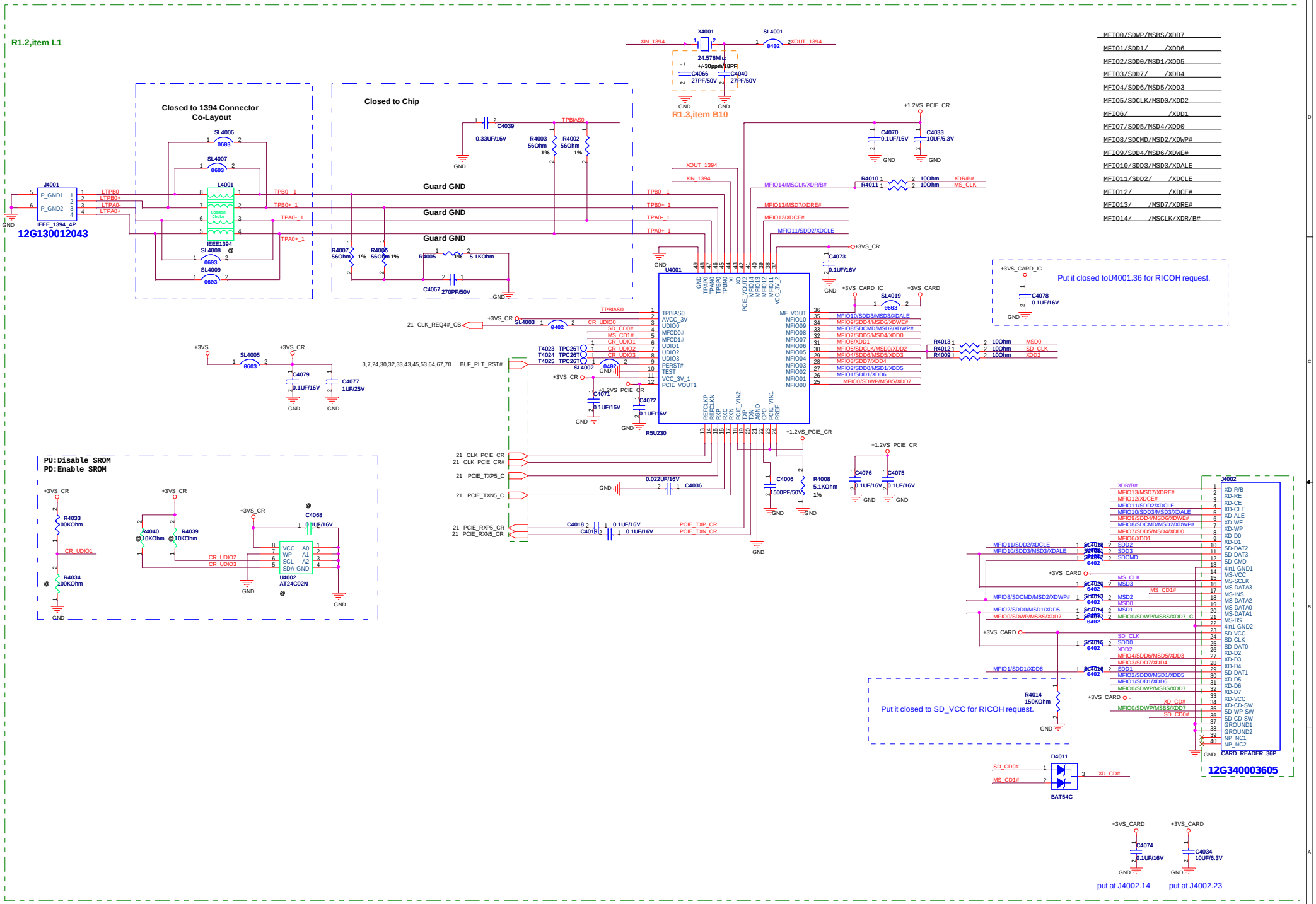
R1.2,item L3

<Variant Name>

ASUSTeK COMPUTER INC. NB2	Title : AUD_****	
	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 38 of 99	

Main Board

ASUS	Title : AUD_****	
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 39 of 99	



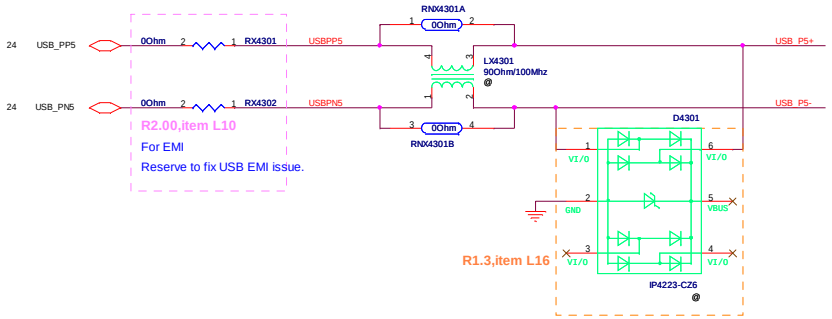
ASUSTeK COMPUTER INC. NB1	Title : R5U230		
	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Friday, July 10, 2009	Sheet 40 of 99		

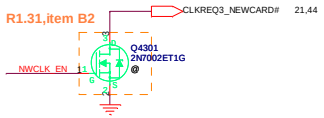
R1.2,item L1

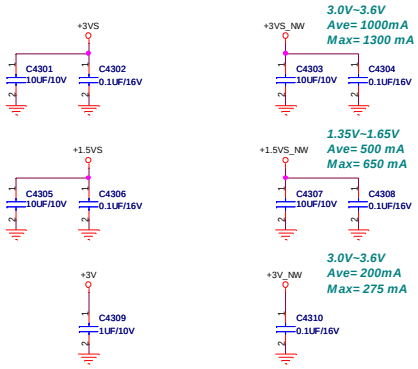
ASUS	Title : CB_****	
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 41 of 99	

R1.2,item L1

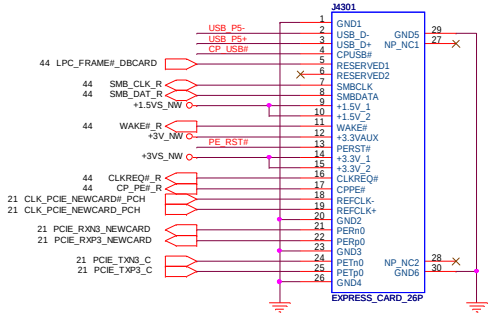
Main Board



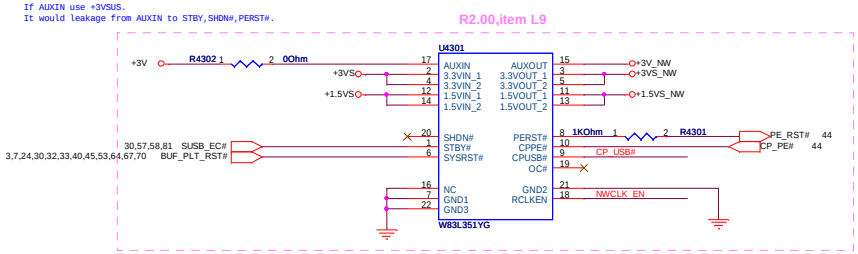




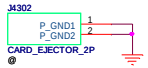
NewCard Header



If AUXIN use +3VSUS.
It would leakage from AUXIN to STBY,SHDN#,PERST#.

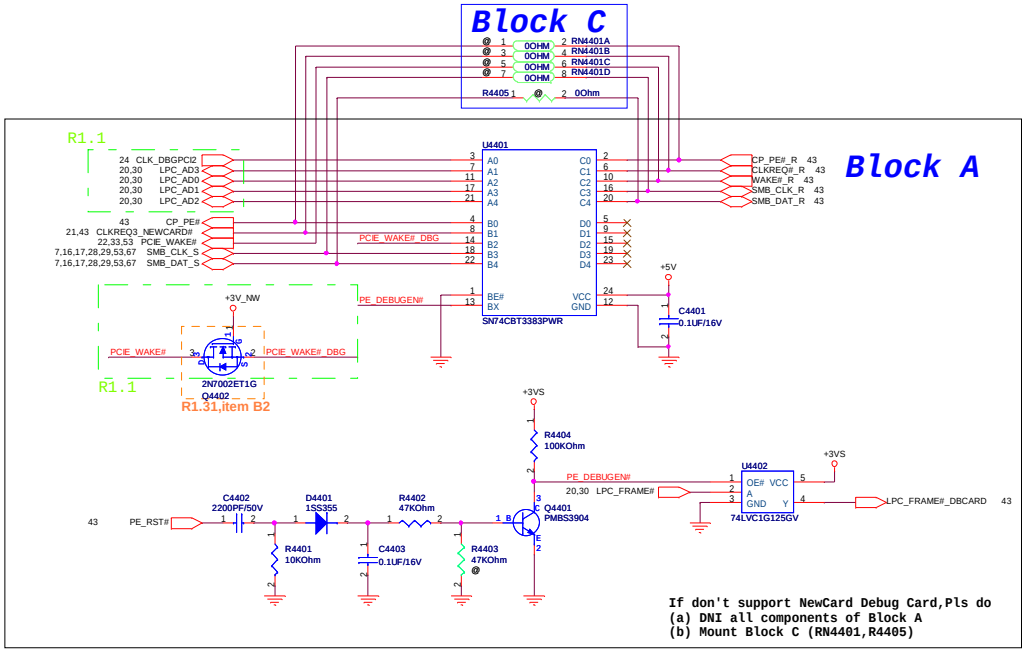


NewCard Ejecter

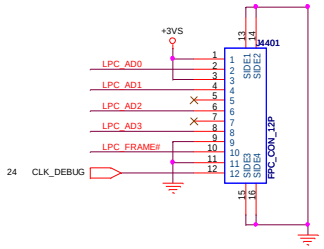


ASUSTeK COMPUTER INC. NB4	Title : CB_NewCard	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 43 of 99	

For NewCard Debug Card

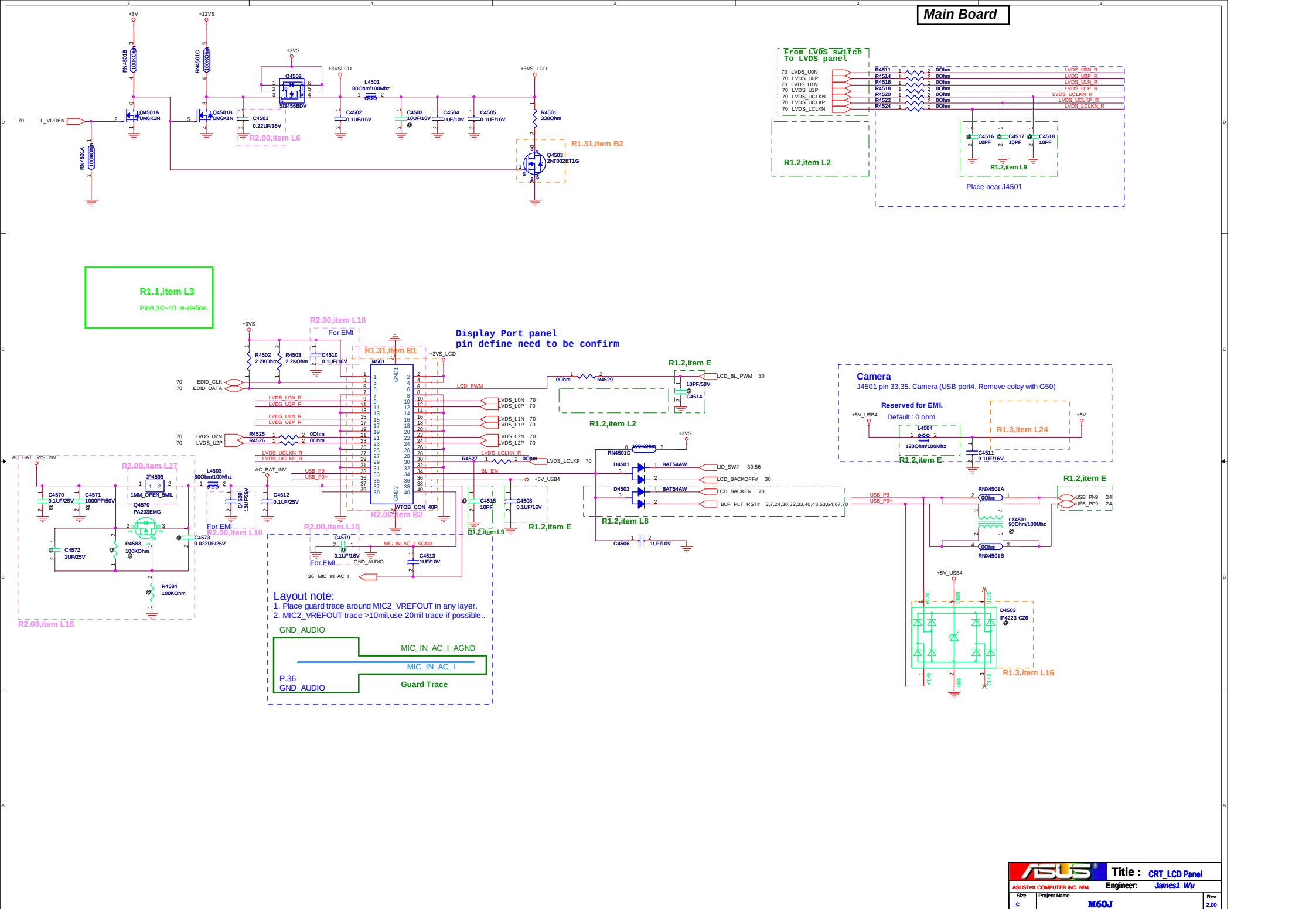


LPC Debug Port

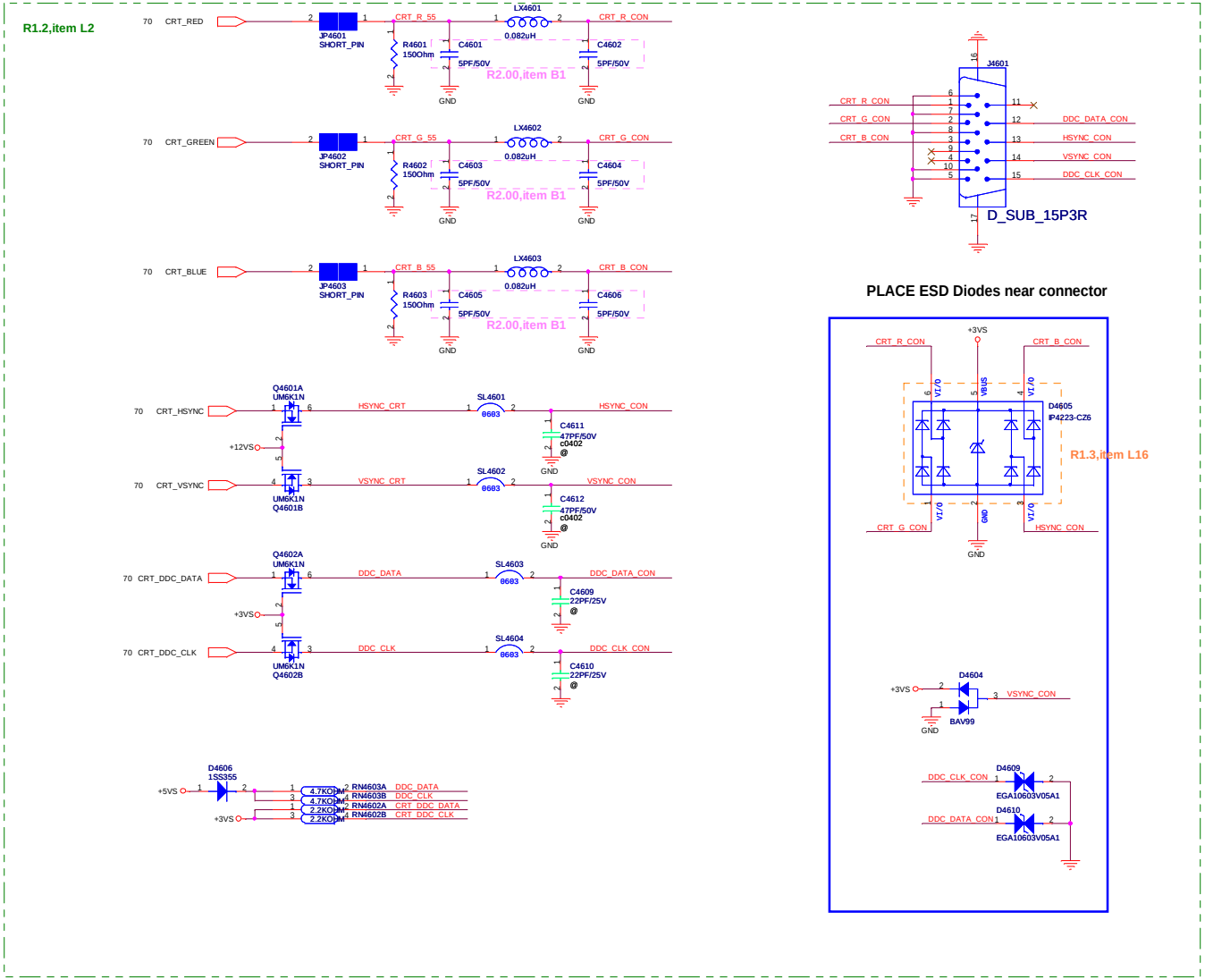


ASUS	Title : BUG_Debug	
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu	
Size C	Project Name M60J	Rev 2.00
Date: Friday, July 10, 2009	Sheet 44 of 99	

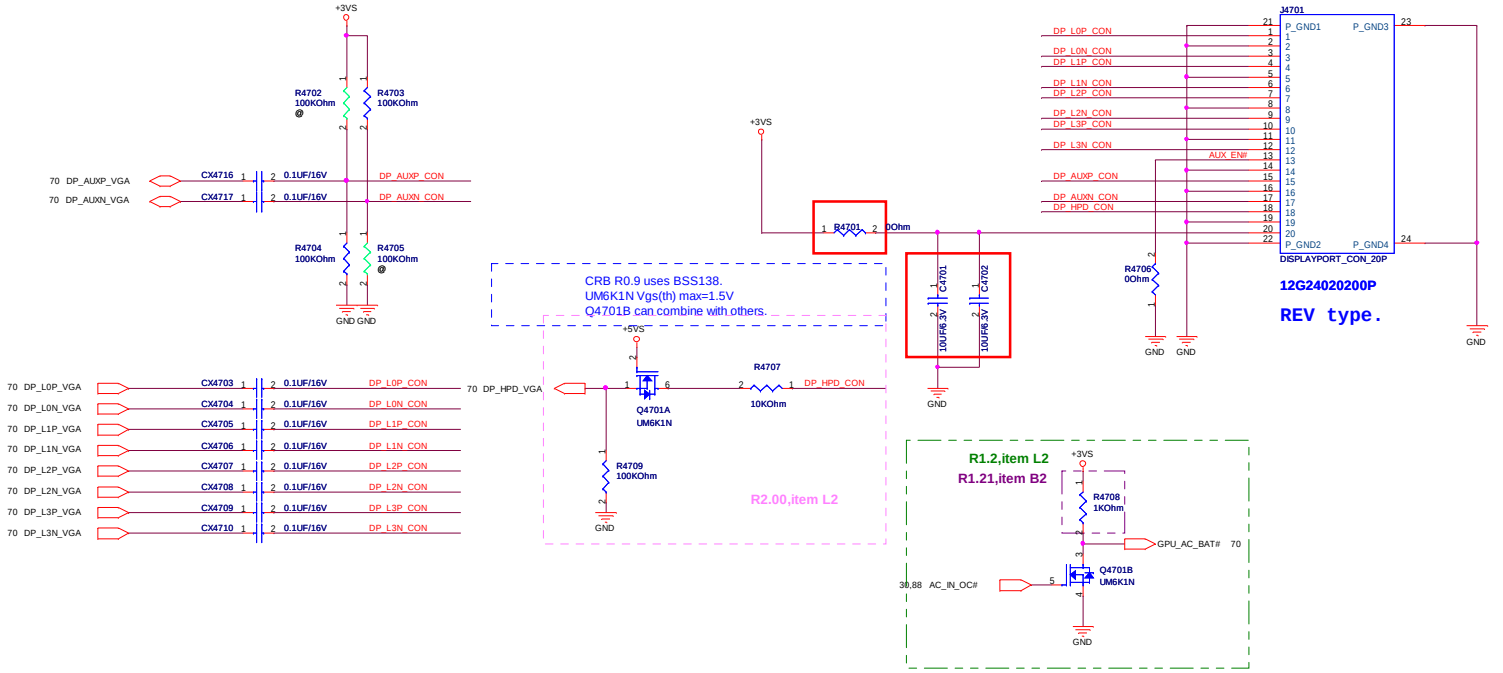
Main Board

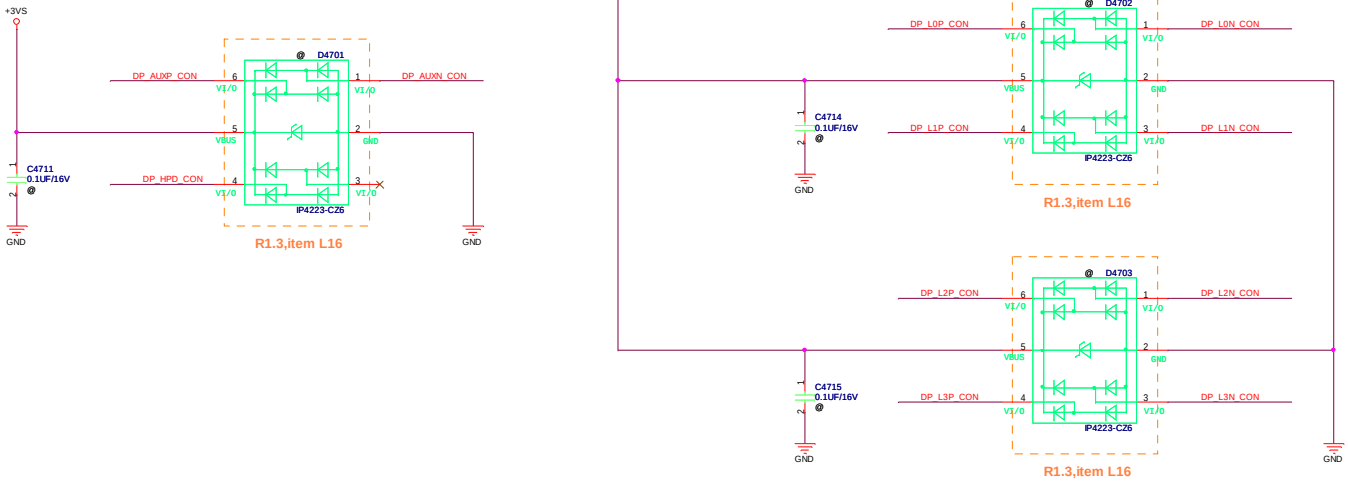


ASUS / ASUSTeK COMPUTER INC. NB4	Title : CRT_LCD Panel	Engineer: James1_Wu
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 45 of 99	



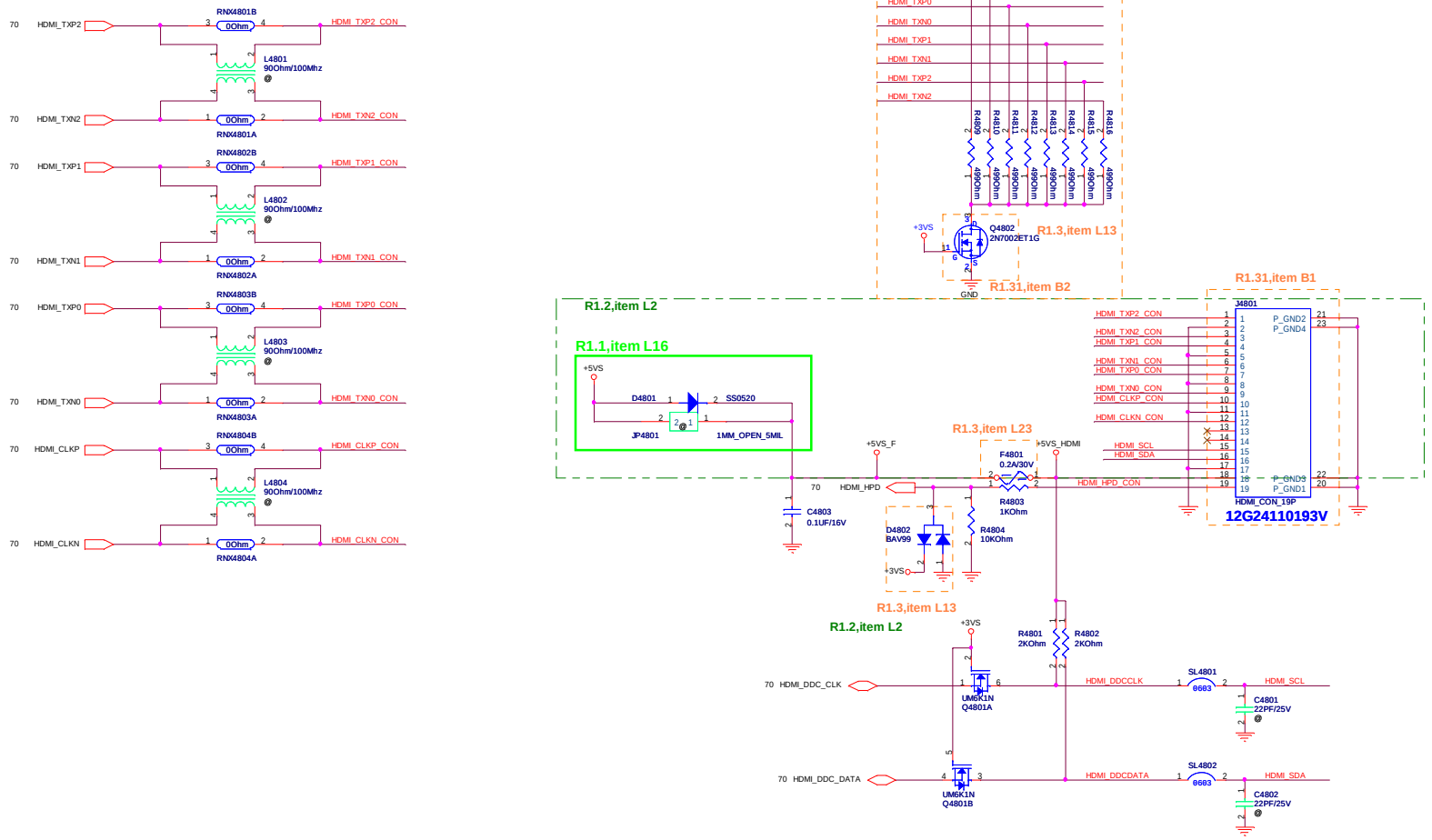
ASUSTeK COMPUTER INC. NB4	Title : CRT_D-Sub		
	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Friday, July 10, 2009	Sheet 46 of 99		





ASUSTeK COMPUTER INC. NB4	Title : Display Port	
	Engineer: James1_Wu	
Size C	Project Name M60J	Rev 2.00
Date: Friday, July 10, 2009	Sheet 47 of 99	

Main Board

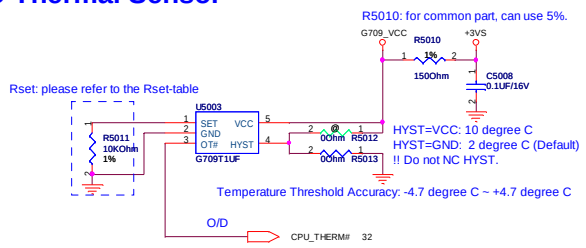


ASUSTeK COMPUTER INC. NB4	Title : TV_HDMI		
	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Friday, July 10, 2009	Sheet 48 of 99		

ASUSTeK COMPUTER INC. NB4	Title : TV_****	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 49 of 99	

R2.00,item L15

CPU Thermal Sensor



Layout note:

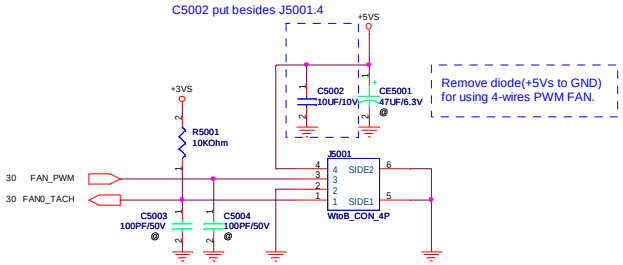
Place U5003 at the center of the CPU socket.

Rset(Kohm)=0.0012T*T-0.9308*T+96.147

Rset table:

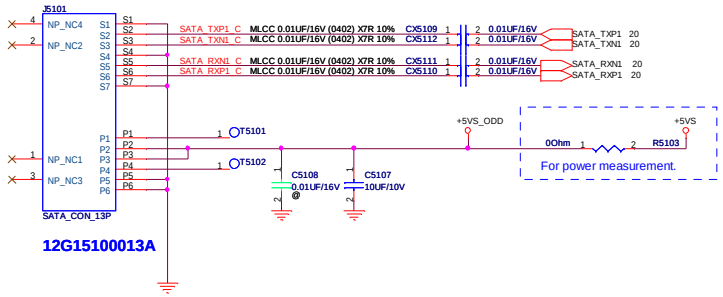
T= degree C	Rset= Kohm	
100	15.07	
101	14.38	
102	13.69	
103	13.01	
104	12.32	
105	11.64	
106	10.97	
107	10.29	
107.43	**10.00**	**default**
109	8.95	
110	8.28	
111	7.61	
112	6.95	
113	6.29	
114	5.23	
115	4.98	

PWM Fan



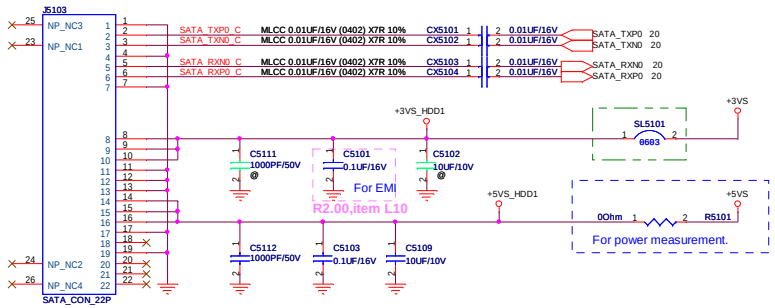
ASUS	Title : FAN_Fan & Sensor	
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu	
Size C	Project Name M60J	Rev 2.00
Date: Friday, July 10, 2009	Sheet 50 of 99	

ODD



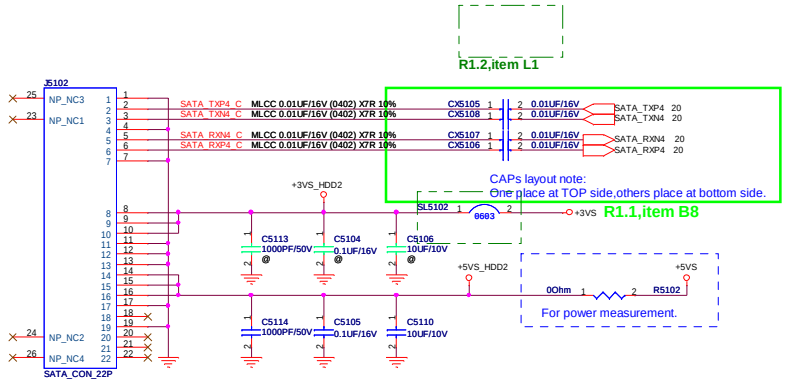
12G15100013A

HDD (1st)



12G15101022M

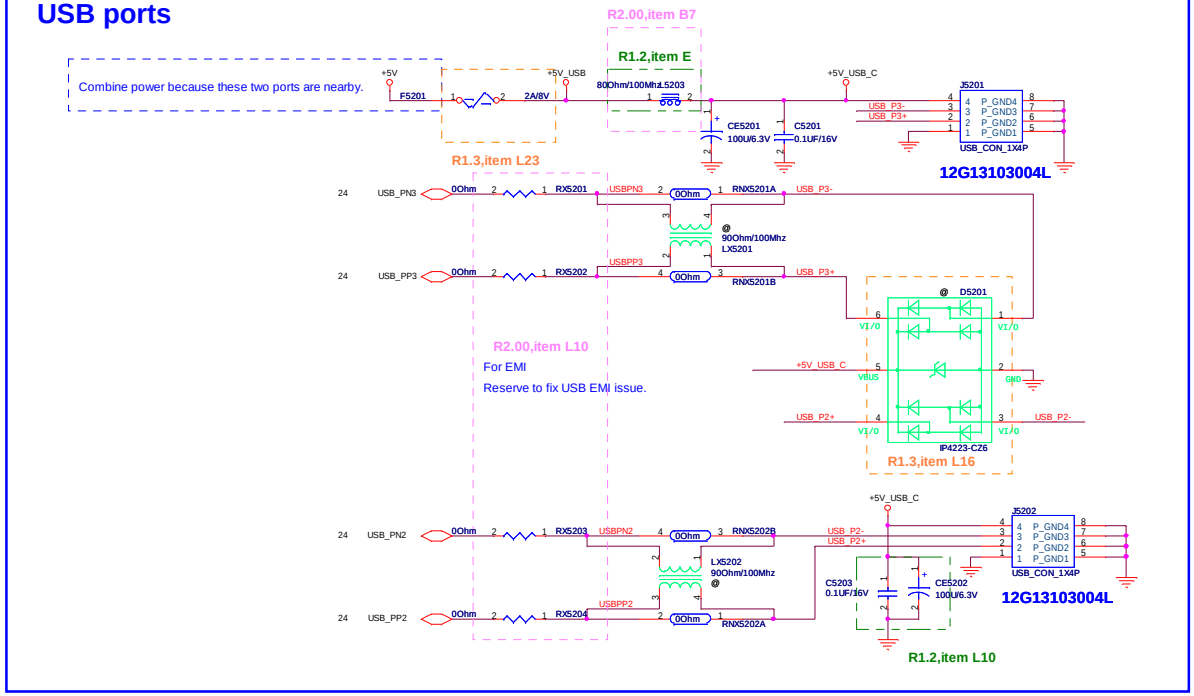
HDD (2nd)



12G15111022J

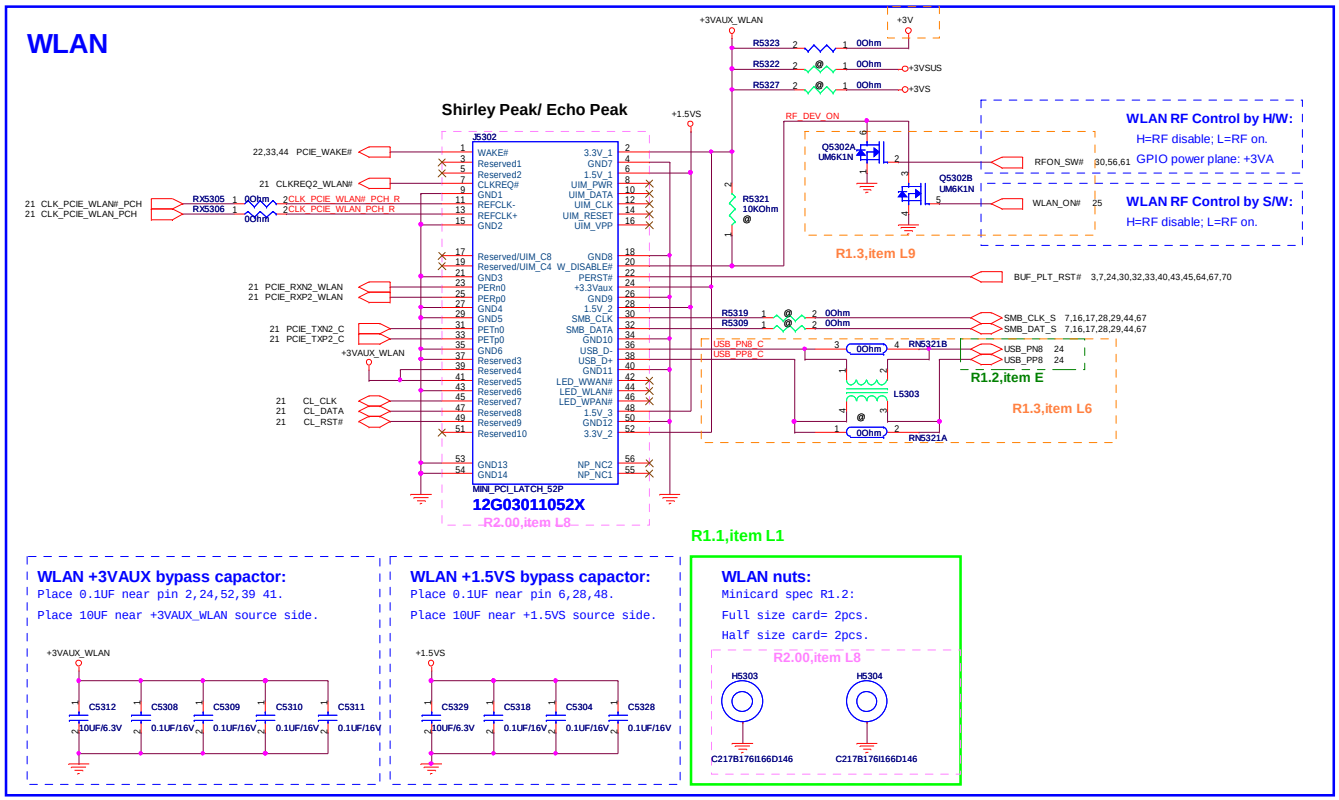
ASUSTeK COMPUTER INC. NB4	Title : XDD_HDD & ODD		
	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Friday, July 10, 2009	Sheet 51 of 99		

USB ports



ASUSTeK COMPUTER INC. NB4	Title : USB_USB Port *2	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 52 of 99	

WLAN



R1.1,item L1

WLAN +3VAUX bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

Place 10UF near +3VAUX_WLAN source side.

WLAN +1.5VS bypass capactor:

Place 0.1UF near pin 6,28,48.

Place 10UF near +1.5VS source side.

WLAN nuts:

Minicard spec R1.2:

Full size card= 2pcs.

Half size card= 2pcs.

R2.00,item L8

ASUSTeK COMPUTER INC. NB6

Title : MINICARD(WLAN)

Engineer: James1_Wu

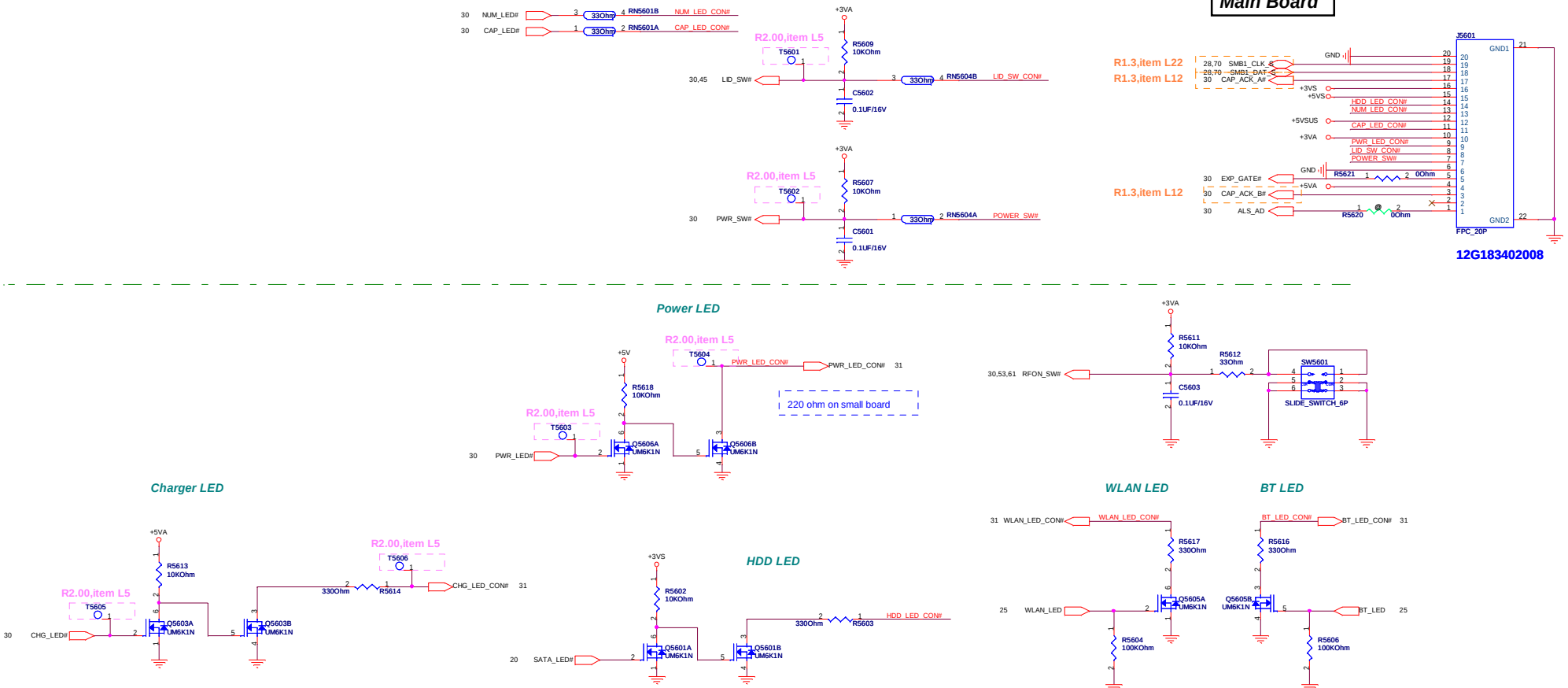
Size	Project Name	Rev
C	M60J	2.00

Date: Friday, July 10, 2009 Sheet 53 of 99

ASUSTeK COMPUTER INC. NB4	Title : BAR_****	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 54 of 99	

ASUS	Title : SIO_****	
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu	
Size C	Project Name M60J	Rev 2.00
Date: Thursday, July 02, 2009	Sheet 55 of 99	

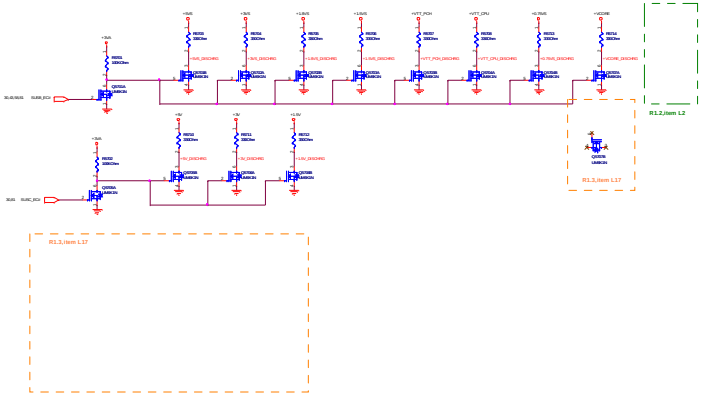
Main Board



ASUSTeK COMPUTER INC. NB4	Title : LED_Indicator		
	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Friday, July 10, 2009	Sheet 56 of 99		

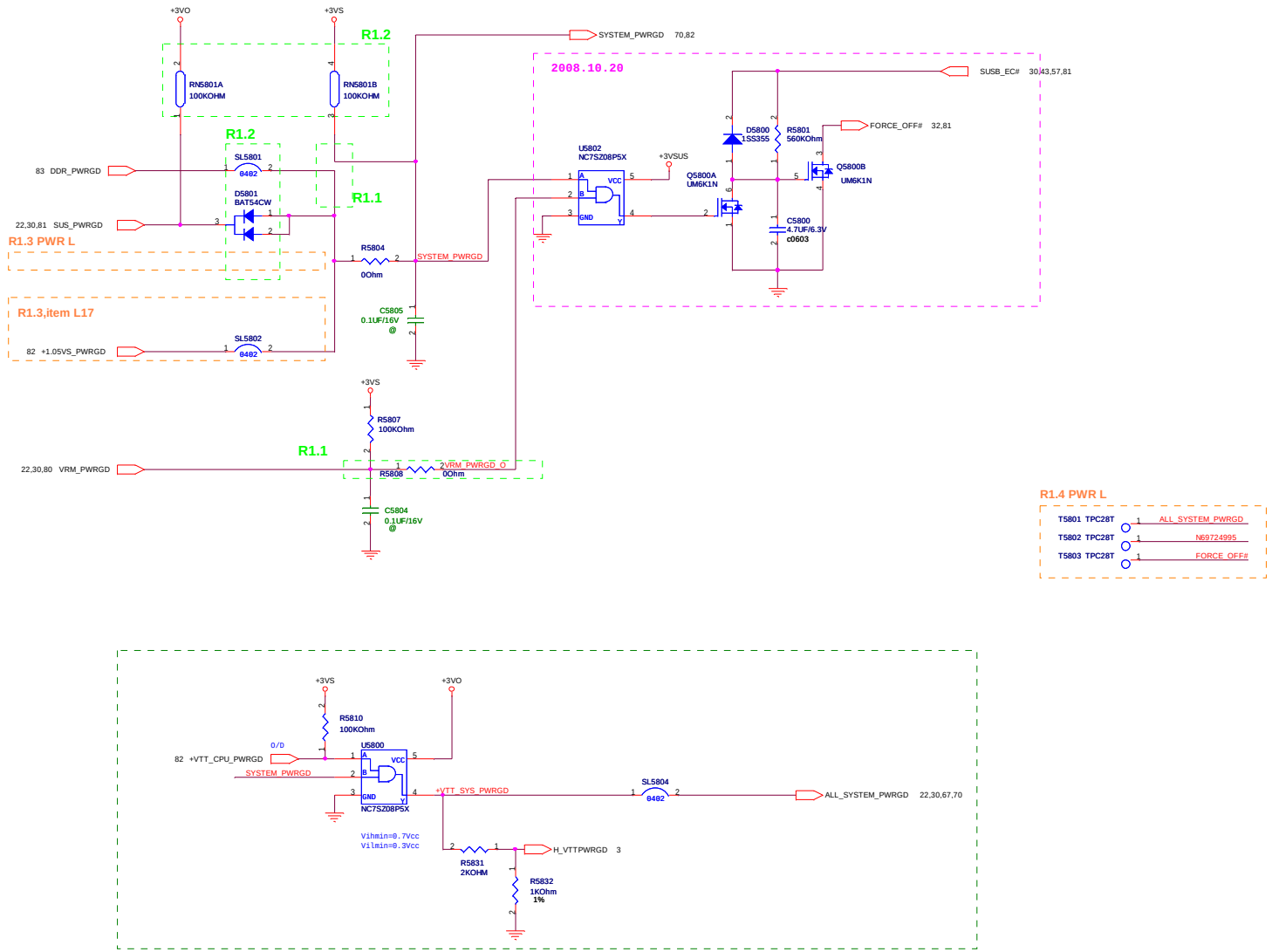
Main Board

Remove +2.5Vs is for ATI GFX



ASUS COMPUTER INC.	Title :	DSG_Discharge	
	Engineer:	James.I_Wu	
Size	Project Name		Rev
A	M60J		2.0

POWER GOOD DETECTER



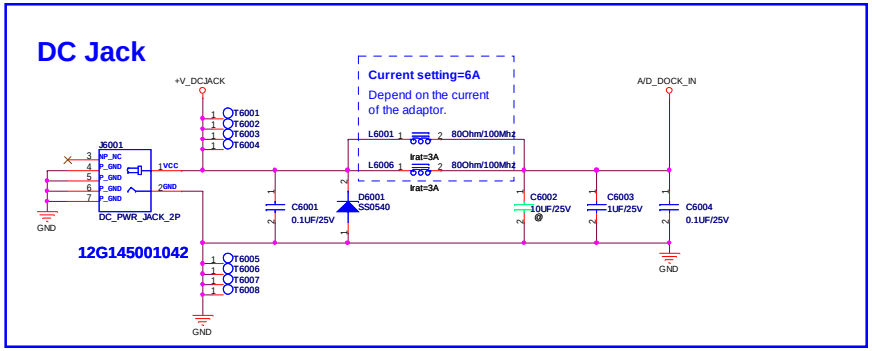
2008-08-04,James Wu add.

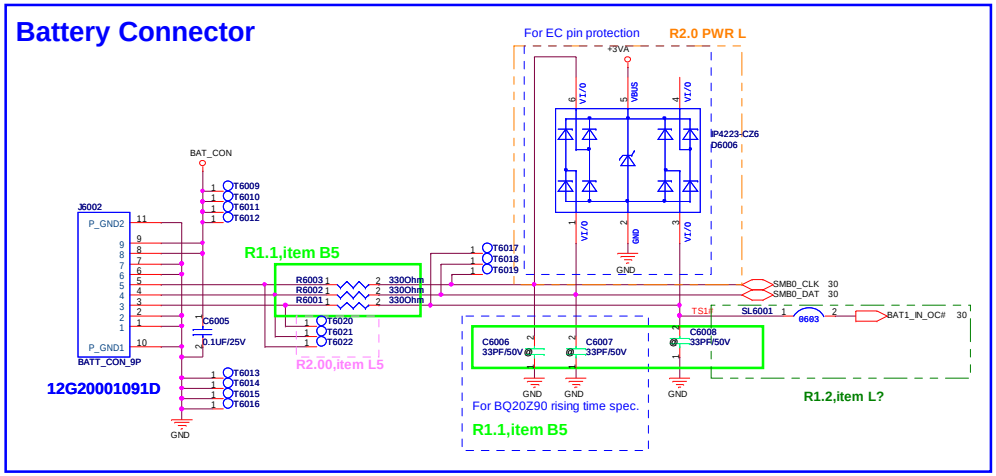
R2.00,item B4

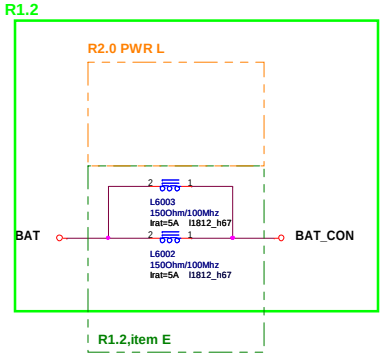
ASUSTeK COMPUTER INC. NB3	Title : POWER_PROTECT	
	Engineer: Kenny Chu	
Size: C	Project Name: M52J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 58 of 99	

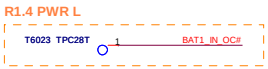
Main Board

ASUS	Title : DJ_****	
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 59 of 99	



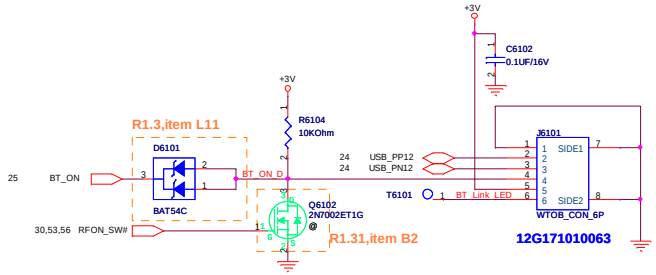






ASUS	Title : DC_DC & BAT Conn.	
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu	
Size C	Project Name M60J	Rev 2.00
Date: Friday, July 10, 2009	Sheet 60 of 99	

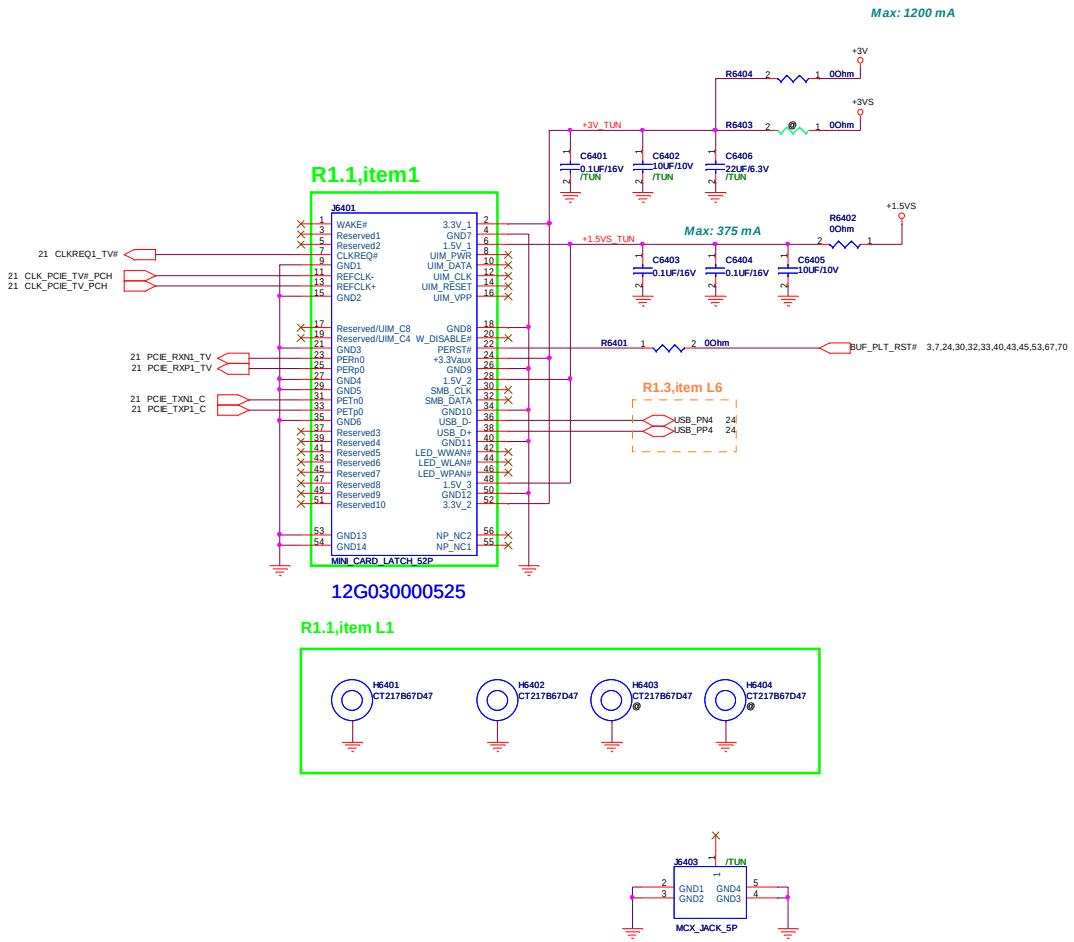
BLUETOOTH



ASUSTeK COMPUTER INC. NB4	Title : BT_Bluetooth	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 61 of 99	

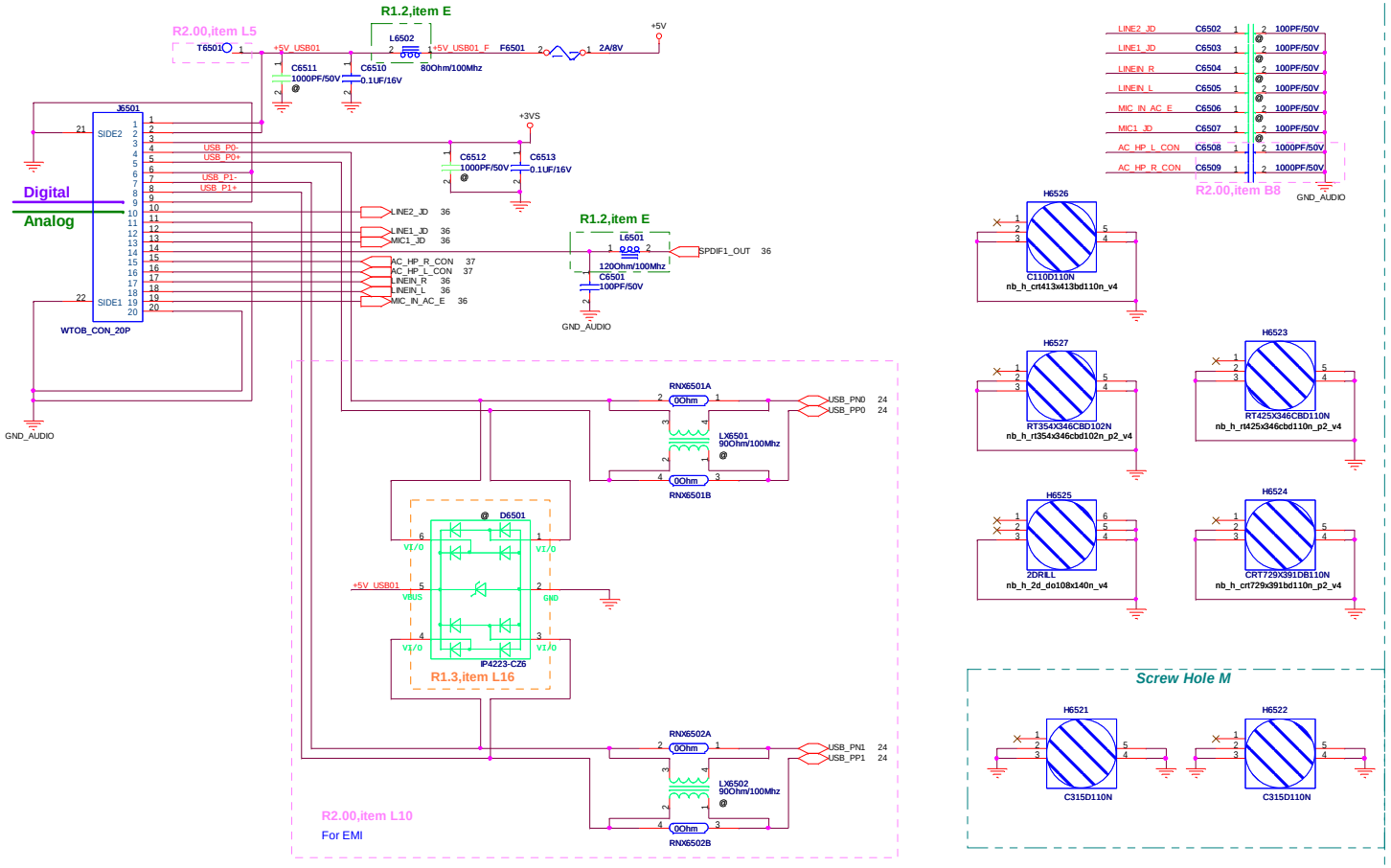
ASUSTeK COMPUTER INC. NB4	Title : TPM_****	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 62 of 99	

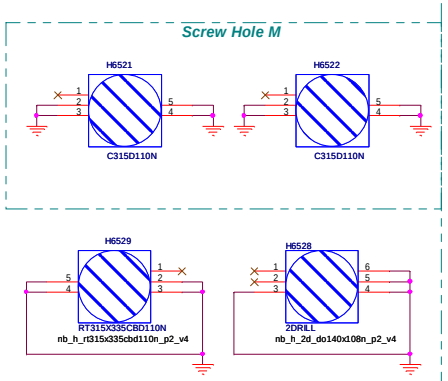
ASUSTeK COMPUTER INC. NB4	Title : FP_FP Conn	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 63 of 99	

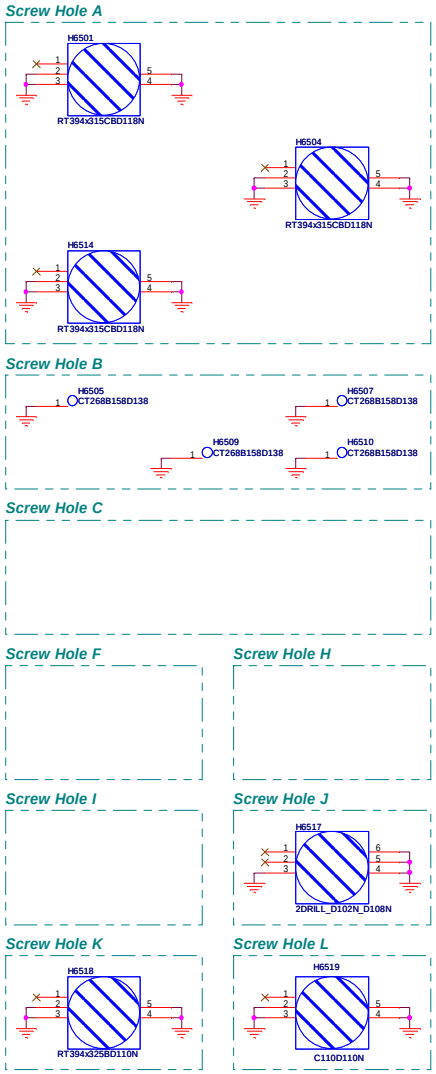


ASUSTeK COMPUTER INC. NB4	Title : TUN_TV Tuner	Engineer: James1_Wu
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 64 of 99	

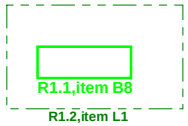
Main Board



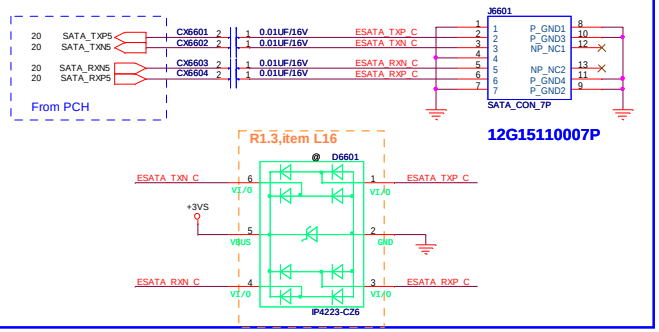




ASUS	Title : ME_Conn & Skew Hole		
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Friday, July 10, 2009	Sheet 65 of 99		

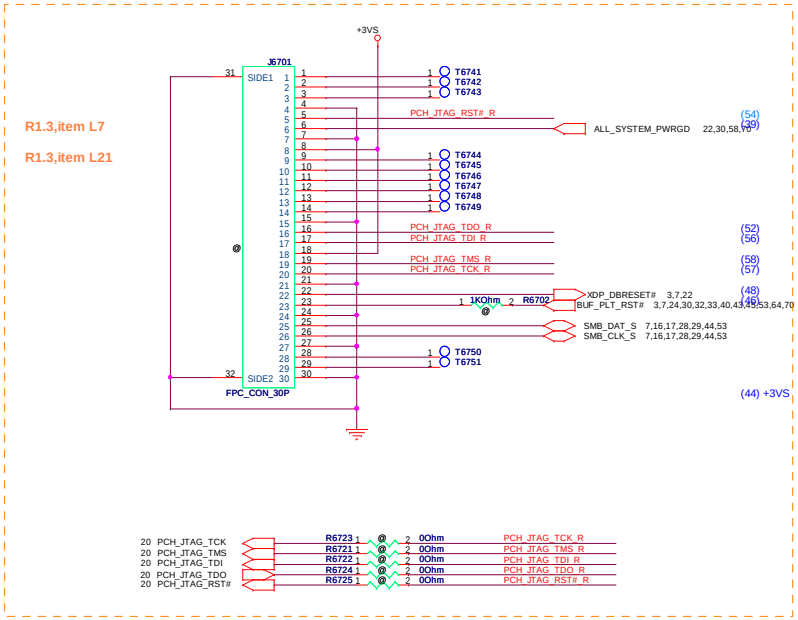


E-SATA connector

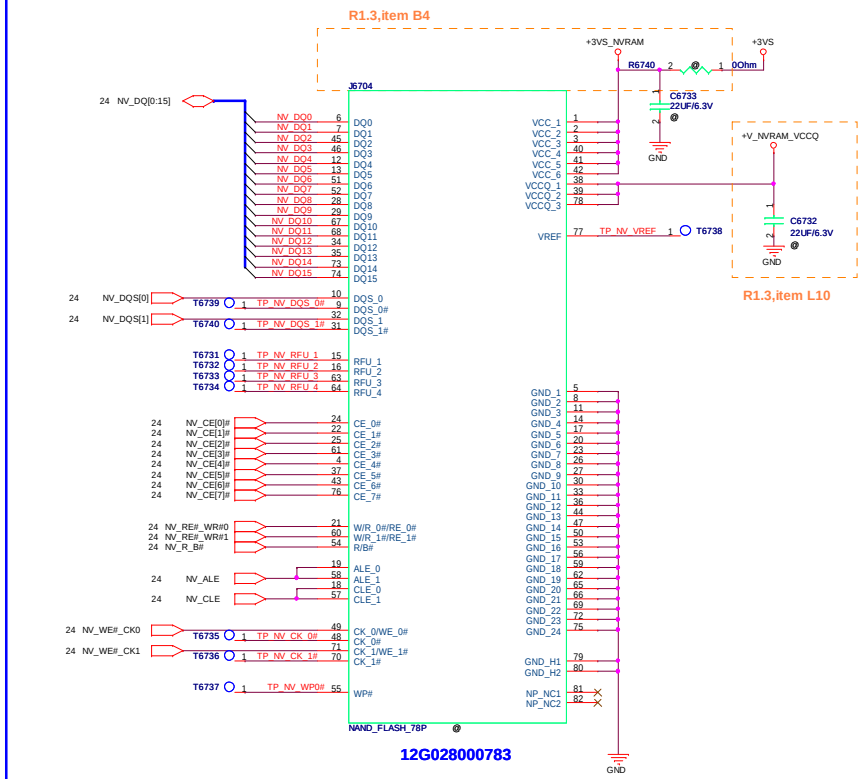


ASUSTeK COMPUTER INC. NB4	Title : ESA_ESATA		
	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Friday, July 10, 2009	Sheet 66 of 99		

PCH XDP



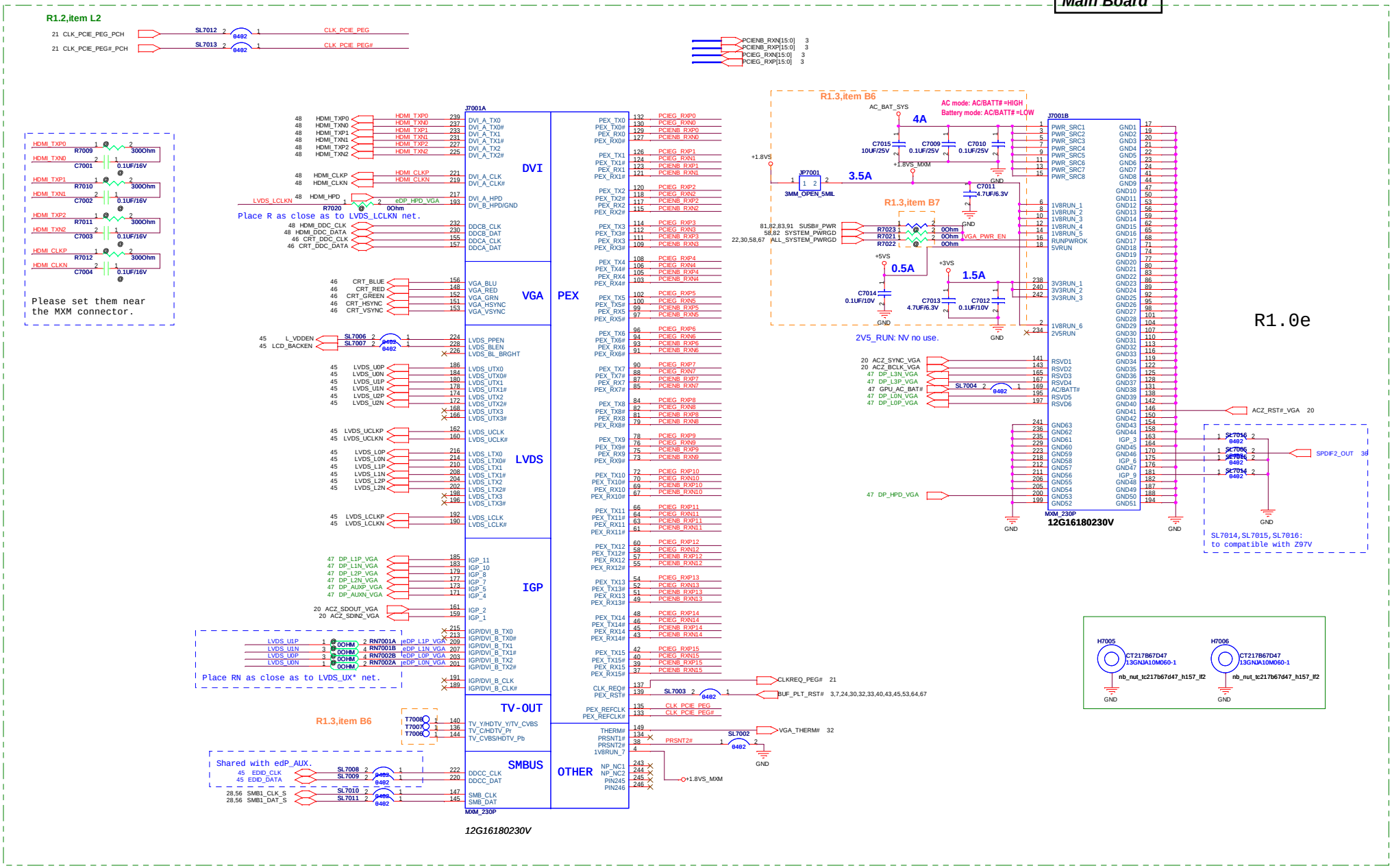
BRAIDWOOD (ONFI)



ASUSTeK COMPUTER INC. NB4	Title : OTH_LCM		
	Engineer: James1_Wu		
Size: C	Project Name: M60J		Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 68 of 99		

ASUSTeK COMPUTER INC. NB4	Title : OTH_GAME-LED*****	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Tuesday, July 07, 2009	Sheet 69 of 99	

Main Board



Title : VGA_MXM(2.1a)		
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 70 of 99	

R1.2,item L2

ASUSTeK COMPUTER INC. NB4	Title : VGA_LVDS Switch****	
	Engineer: James1_Wu	
Size: C	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 71 of 99	

Main Board

ASUSTeK COMPUTER INC. NB4	Title : VGA_****	Engineer: James1_Wu
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 72 of 99	

Main Board

ASUSTeK COMPUTER INC. NB4	Title : VGA_****	
	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 73 of 99	

Main Board

ASUSTeK COMPUTER INC. NB4	Title : VGA_****	
	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 74 of 99	

ASUS	Title : VGA_****	
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 75 of 99	

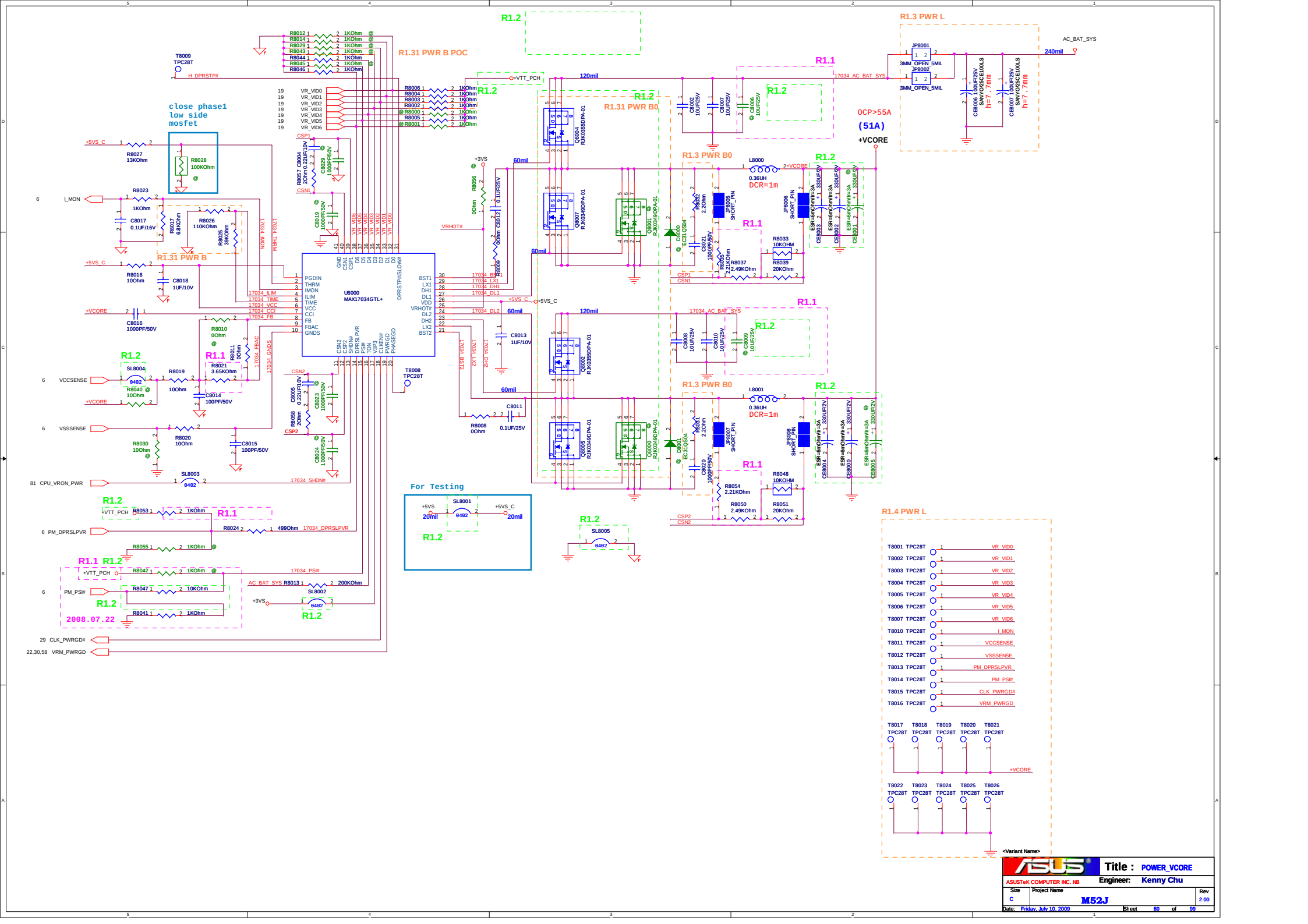
ASUSTeK COMPUTER INC. NB4	Title : VGA_****	
	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 76 of 99	

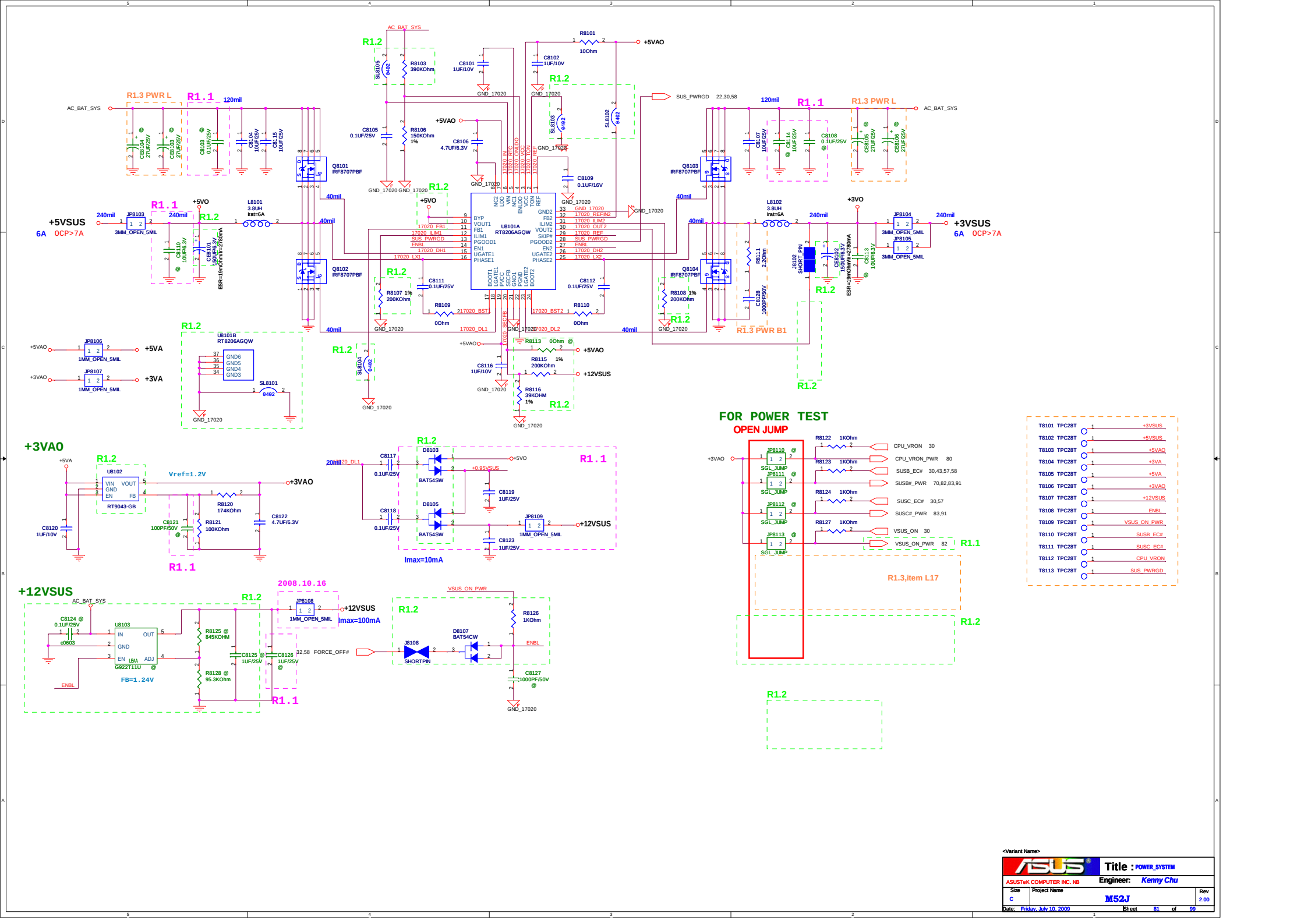
ASUSTeK COMPUTER INC. NB4	Title : VGA_****		
	Engineer: James1_Wu		
Size C	Project Name M60J		Rev 2.00
Date: Thursday, July 02, 2009	Sheet 77 of 99		

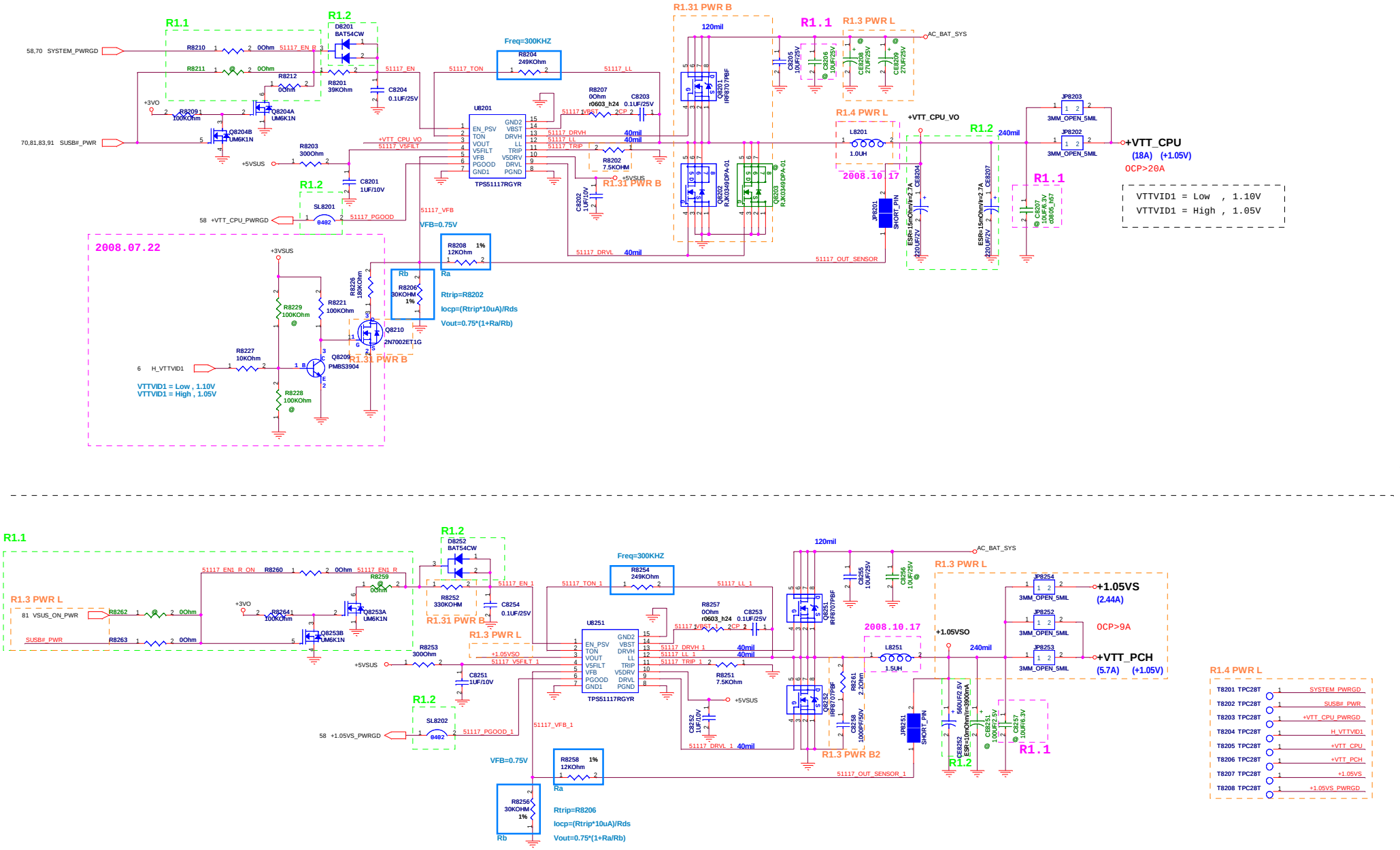
ASUS	Title : VGA_****	
ASUSTeK COMPUTER INC. NB4	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 78 of 99	

Main Board

ASUSTeK COMPUTER INC. NB4	Title : VGA_****	
	Engineer: James1_Wu	
Size: Custom	Project Name: M60J	Rev: 2.00
Date: Thursday, July 02, 2009	Sheet 79 of 99	

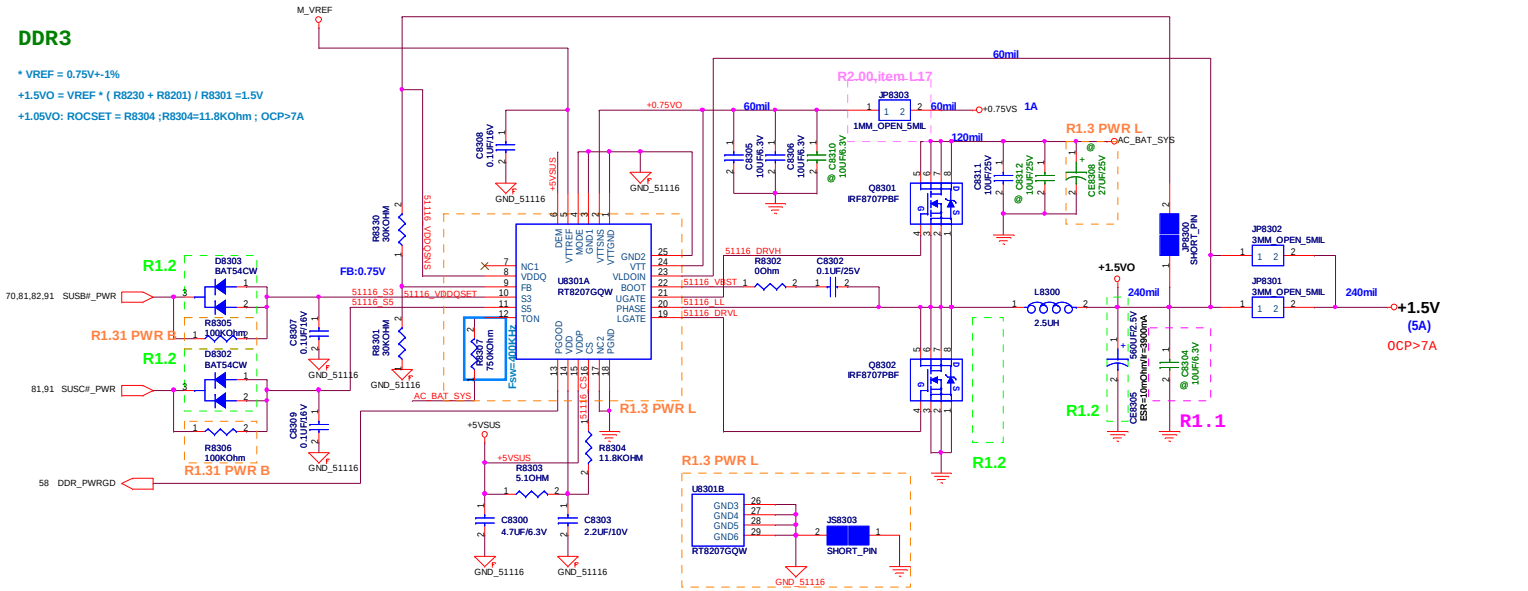

R1.2
R1.31 PWR B POC
R1.3 PWR L
R1.1
R1.31 PWR B
R1.3 PWR B0
R1.4 PWR L
close phase1
low side
mosfet
For Testing
U8000
MAX17034GTL+
OCP>55A
(51A)
+VCORE
AC_BAT_SYS
240mil
120mil
60mil
DCR=1m
0.36UH
2008.07.22
Title : POWER_VCORE
Engineer: Kenny Chu
ASUSTeK COMPUTER INC. NB
Size C
Project Name M52J
Rev 2.00
Date: Friday, July 10, 2009
Sheet 80 of 99

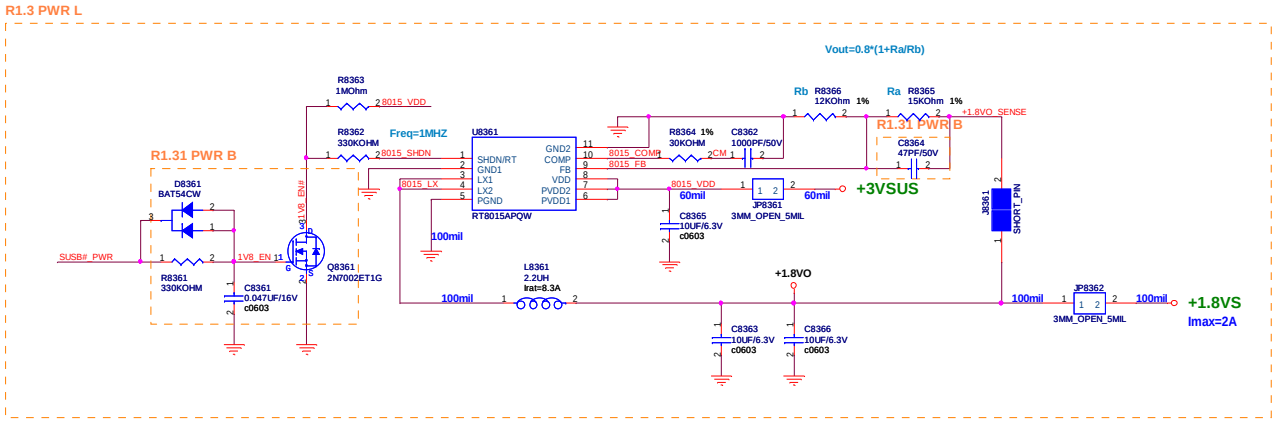

+5VSUS
6A OCP>7A
+3VSUS
6A OCP>7A
+3VAO
+12VSUS
FOR POWER TEST
OPEN JUMP
U8101A RT8206AGQW
U8101B RT8206AGQW
U8102 RT9043-GB
U8103 G922T11U
Q8101 IRF8707PBF
Q8102 IRF8707PBF
Q8103 IRF8707PBF
Q8104 IRF8707PBF
R1.1
R1.2
R1.3 PWR L
R1.3 PWR B1
R1.3,item L17
2008.10.16
Title : POWER_SYSTEM
Engineer: Kenny Chu
ASUSTeK COMPUTER INC. NB
Size C
Project Name M52J
Rev 2.00
Date: Friday, July 10, 2009
Sheet 81 of 99



<Variant Name>

ASUS	Title : PW_I/O_VTT_CPU&VTT_PCH	
ASUSTeK COMPUTER INC. NB	Engineer: Kenny Chu	
Size: C	Project Name: M52J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 82 of 99	





R1.4 PWR L

T8301	TPC28T	1	+1.5V
T8302	TPC28T	1	+1.8VS
T8303	TPC28T	1	M_VREF
T8304	TPC28T	1	+0.75VS
T8305	TPC28T	1	DDR_PWRGD
T8306	TPC28T	1	8015_VDD

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_DDR & VTT

Engineer: Kenny Chu

Size	Project Name	Rev
C	M52J	2.00

Date: Friday, July 10, 2009 Sheet 83 of 99

+3VM

R1.3,item L17

R1.3,item L17

ASUSTeK COMPUTER INC. NB3	Title: +3VM & +3VS_TVDAC	
	Engineer: Kenny Chu	
Size: C	Project Name: M52J	Rev: 2.00
Date: Wednesday, July 08, 2009	Sheet 84 of 99	

<Variant Name>

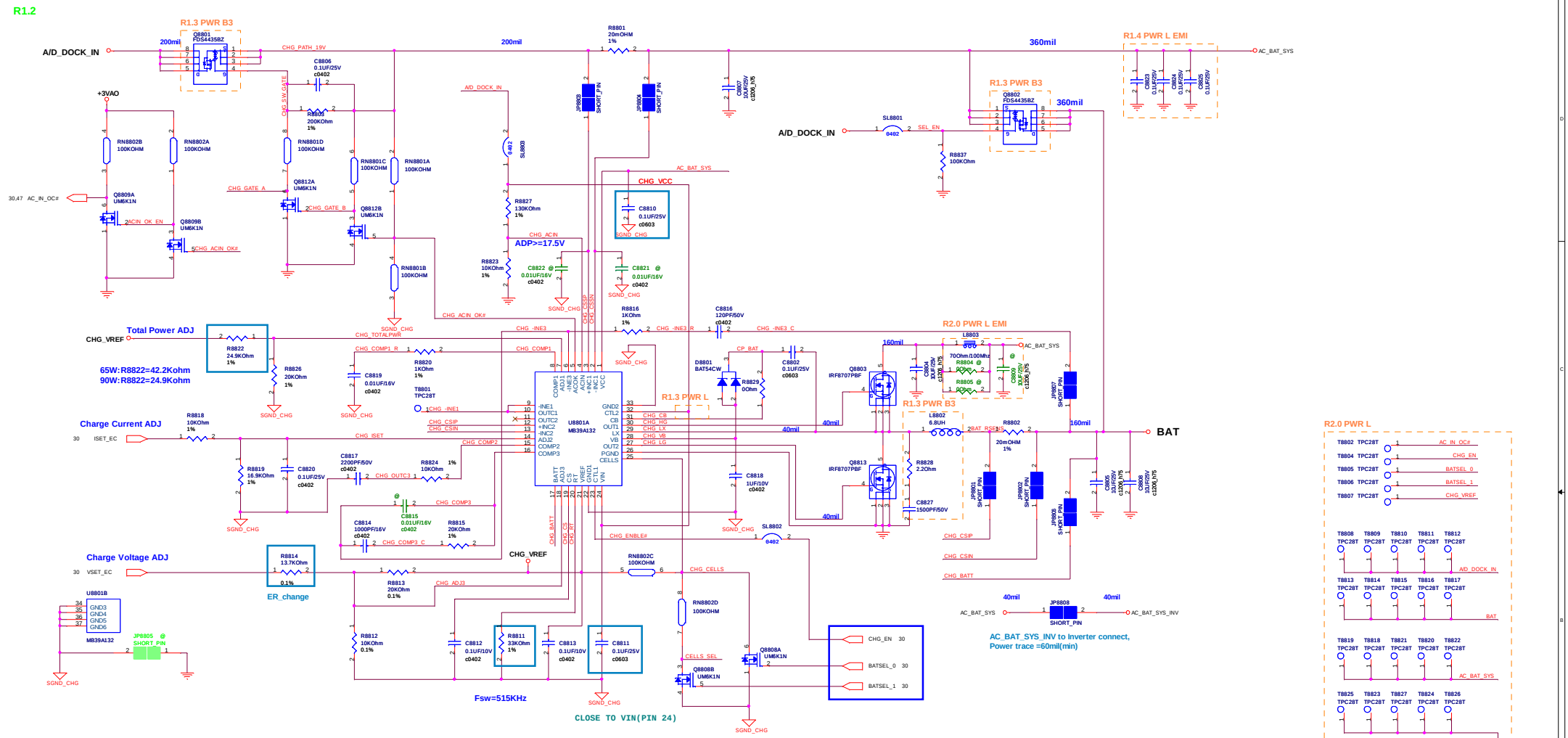
Title : <Title>

ASUSTeK COMPUTER INC. NB

Engineer: Kenny Chu

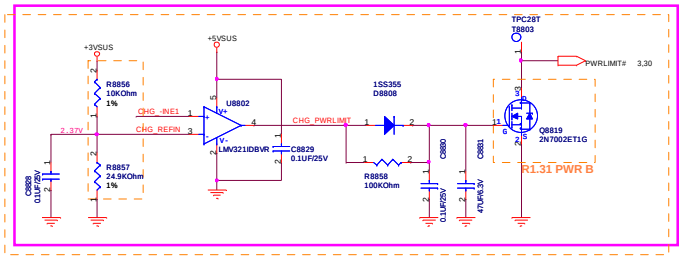
Size	Project Name	Rev
C	M52J	2.00

Date: Tuesday, July 07, 2009 Sheet 86 of 99



Power Limit

R1.3 PWR L 2008.10.17



TOTAL COUNT:66 PCS

Battery Cells		
BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet :
Charger MAX8725 => EC CODE : 200
Charger MAX17015 => EC CODE : 201
Charger MB39A132 => EC CODE : 202

ASUSTeK COMPUTER INC. NB3

Title : POWER_CHARGER_202

Engineer: Kenny Chu

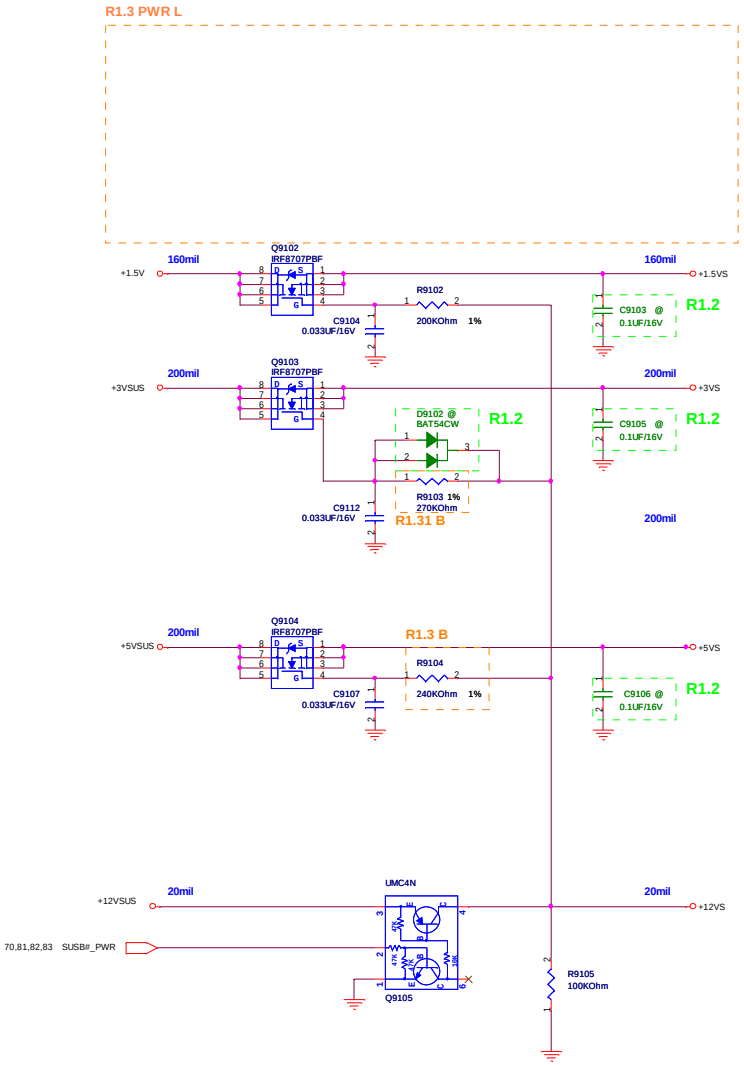
Size	Project Name	Rev
Custom	M52J	2.00

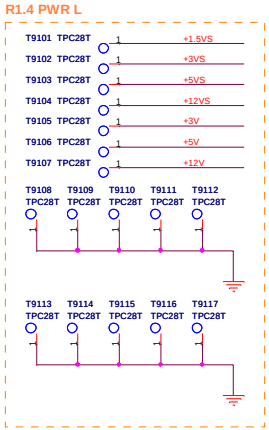
Date: Friday, July 10, 2009 Sheet 88 of 99

R1.2

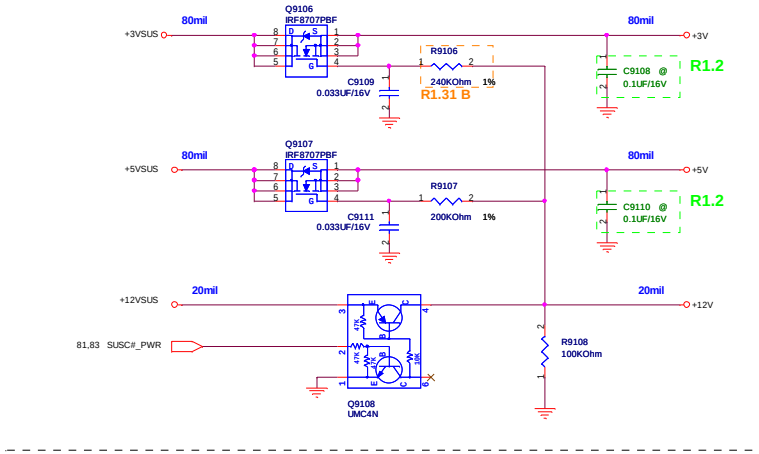
ASUSTeK COMPUTER INC. NB3	Title : POWER_DETECT	
	Engineer: Kenny Chu	
Size: C	Project Name: M52J	Rev: 2.00
Date: Tuesday, July 07, 2009	Sheet 90 of 99	

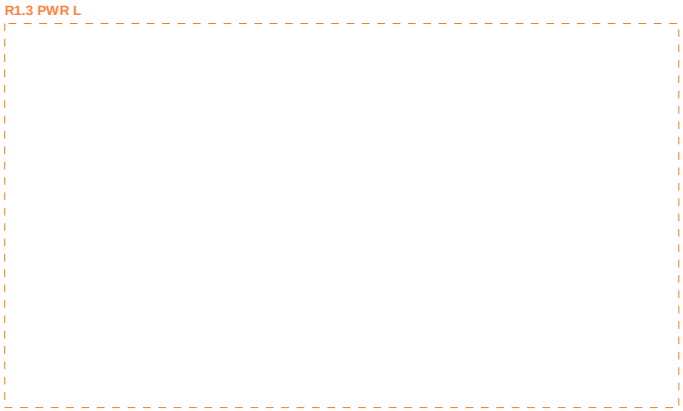
SUSB#_PWR POWER





SUSC#_PWR POWER





<Variant Name>

ASUS	Title : POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB	Engineer: Kenny Chu	
Size: C	Project Name: M52J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 91 of 99	

POWER_SIGNAL

A/D_DOCK_IN	A/D_DOCK_IN	60,88
AC_BAT_SYS	AC_BAT_SYS	70,80,81,82,83,88
BAT_CON	BAT_CON	60
BAT	BAT	60,88
+5VA	+5VA	28,31,56,81
+5VAO	+5VAO	81
+5VO	+5VO	81
+5VSUS	+5VSUS	27,56,81,82,83,88,91
+5V	+5V	31,44,45,52,56,57,65,91
+5VS	+5VS	27,30,31,36,46,47,48,50,51,56,57,70,80,91
+3VA	+3VA	20,30,56,57,60,81
+3VO	+3VO	58,81,82
+3VSUS	+3VSUS	27,30,33,53,58,81,82,83,88,91
+3V	+3V	24,31,33,43,45,53,57,61,64,91
+3VS	+3VS	16,17,20,21,22,23,24,25,26,27,28,29,30,31,32,36,40,43,44,45,46,47,48,50,51,53,56,57,58,64,65,66,67,70,80,91
+3VM	+3VM	26,27,28
+12VSUS	+12VSUS	28,81,91
+12V	+12V	91
+12VS	+12VS	28,45,46,91
+1.8VO	+1.8VO	83
+1.8VS	+1.8VS	6,26,57,70,83
+1.5VO	+1.5VO	83
+1.5V	+1.5V	3,6,16,17,57,83,91
+1.5VS	+1.5VS	26,29,36,43,53,57,64,91
+0.75VS	+0.75VS	16,17,57,83
+1.05VSO	+1.05VSO	82
+1.05VS	+1.05VS	27,82
+VTT_PCH	+VTT_PCH	26,57,80,82
+VTT_CPU_VO	+VTT_CPU_VO	82
+VTT_CPU	+VTT_CPU	3,6,7,25,26,27,57,82
+VCORE	+VCORE	6,57,80

R1.2

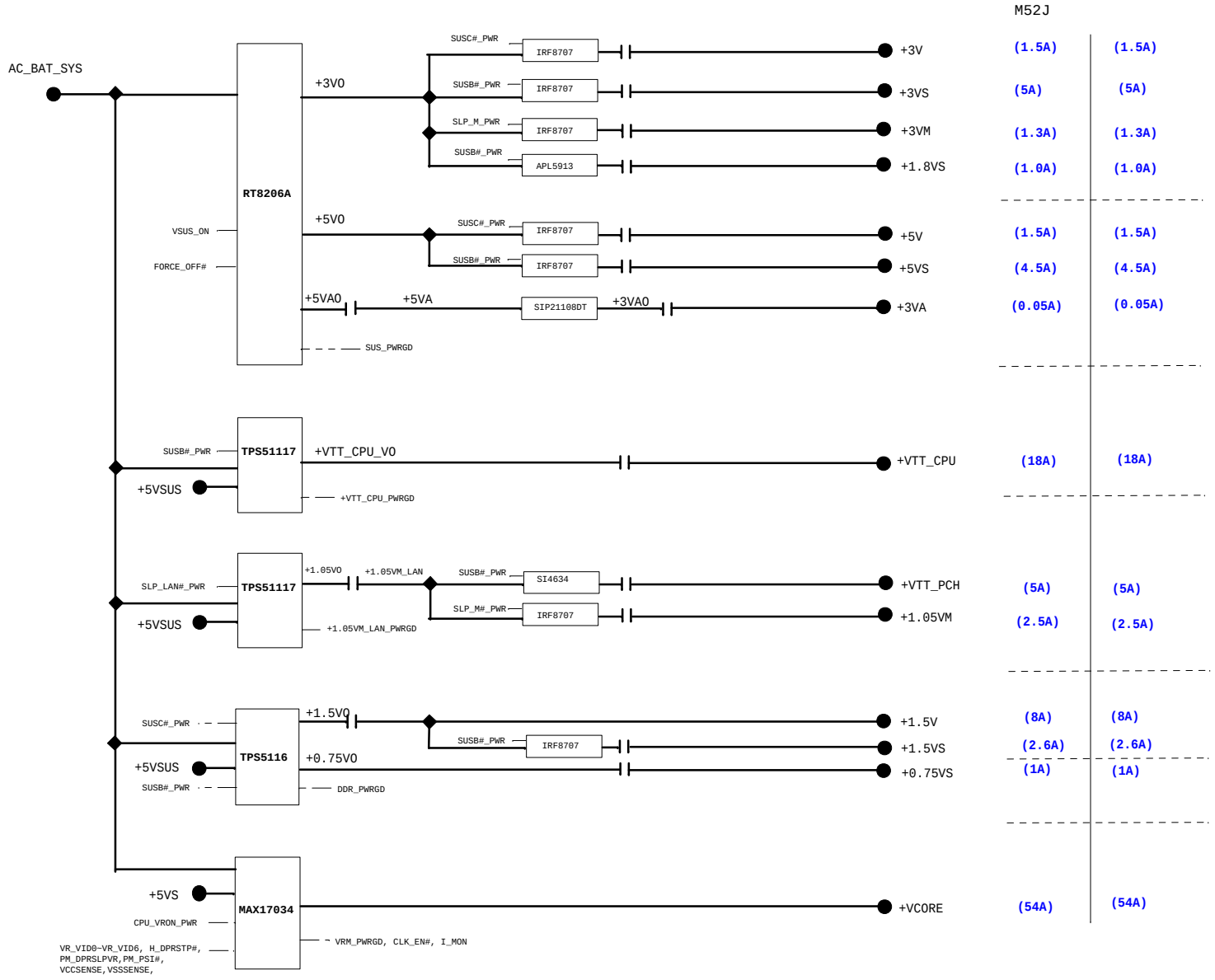
2008-08-27,Chester modify

R1.3 PWR L

R1.2

2008-10-21,Chester modify

ASUSTeK COMPUTER INC. NB3	Title : POWER_SIGNAL	
	Engineer: Kenny Chu	
Size: C	Project Name: M52J	Rev: 2.00
Date: Friday, July 10, 2009	Sheet 93 of 99	



ASUSTeK COMPUTER INC. N83	Title :	Engineer: Chester
Size: Custom	Project Name: M52J	Rev: 2.00
Date: Tuesday, July 07, 2009	Sheet 94 of 99	

[M52J] R1.0

(Release on 2008/09/23)

SR1 Gerber out revision.

[M52J] R1.0 => R1.1

(Release on 2008/10/16)

[Layout Changed - EE]

L1. For ME request:
   1-1. Change J6401 from 12G030000522 to 12G030000525.
   1-2. Change J4201 from 12G340003601 to 12G340003605.
   1-3. Change H6401, H6402, H6403, H6404 from 13GNHC10M020-1 to 13G021043011.
   1-4. Change H5303, H5304, H7003, H7004 from 13GNHC10M020-1 to 13G021036001.

L2. P18: Change M2 circuit for Intel requet.

L3. Re-define J4501 circuit for cost down.
   3-1. P45: Re-define J4501 pin6,pin30~40,delete J4502.
   3-2. P36: Delete C3639. (MONO_OUT)
        Modify circuit for Internal MIC.
   3-3. P38: Delete all items in this page for spec change.

L4. For SPI flash circuit:
   4-1.P28: Change circuit for PCH SPI flash.
        P20: Change R2015 pull-up from +3VM to +3VM_SPI
   4-2.P30: Change circuit for EC SPI flash.

L5. To prevent device damage if power not ready:
   5-1.P20,P30: Add J2001,J3001 to isolate +3VA.
   5-2.P20,P21,P22,P24,P25,P27: Modify +3VSUS to +3VSUS_ORG.
        P27: Add J2703,J3001 to isolate +3VSUS.
   5-3.P27: Modify +5VSUS to +5VSUS_ORG,add J2704 to isolate.

L6. For decoupling:
   6-1: Change C2903 from net +3VS_VDDPCIEX to +VDDIO_42.
   6-2: Change C2904 from net +3VS_VDDPCIEX to +VDDIO_28.
   6-3: Add C2927 to +VTT_CPU.

L7. P29: Reserve net +VTT_CPU and add +3VS for frequency 133MHz.

L8. P03,P29: Delete colay net for PCH buffer mode clock is workable.
        Net: CLK_CPU_BCLK_ICS,CLK_CPU_BCLK_ICS#

L9. For test:
    9-1. P22: Add R2265,R2266@,R2267 for test.
    9-1. P22: Add R2265,R2266@,R2267 for test.

L10. P03,P30: Add power limit circuit for power request.

L11. P91: Add D9101,D9102 for MOS close quickly.

L12. P03: Add R0366,R0367 to disable FDI for discrete GFX.

L13. P30,P31: Reserved circuit for testing U3101 removed.

L14. P31: Exchange D3105 pin 4,5 net for EMI request.

L15. P22: For S0-to-G3,S5-to-G3 solution.

L16. P48: Modify circuit for design IP change.

L17. P30: Delete BAT_LEARN function for power request cost down.

[Layout Changed - PWR]

L1. For reduce noise add inupt CAP CE8006,CE8007,CE8800.

L2. P80 change pull high power
    Follow Intel common schematic from +VTT_CPU_VO to +VTT_PCH

L3. For +12VSUS test
   3-1. P80: bump power from +5VSUS to +5VO
   3-2. P80: Add JP8108 JP8109

L4. To enhance charger bump energy add C8129,D8108,D8109

L5. Change +1.05VM_LAN enable
    from SLP_LAN#_PWR to VSUS_ON_PWR for EE request

L6. For enable frequency test
    Add R8210,R8211,R8212,R8259,R8260,R8264,R8262,R8263,Q8253A,Q8253B,R8405

L7. For test add JP860,JP8606

L8. P88 Change D8807 PIN2 connect D8805 PIN2 to D8805 PIN1
    for solve MAX17015 IC bug

L9. P88: Add power limit circuit

L10. P91: Add D9101,D9102,R9117 for EE request

L11. P92 Change protect circuit to original un-cost down version

[BOM modify - EE]

B1: P05: DNI R0538 for MoW41 Intel's recommand.

B2: P20: DNI R2029 to disable Flash descriptor override.

B3: P31: Change R3101 from 10K ohm to 0 ohm,
        DNI C3105 for EGCLK signal quality.

B4: P42: Change R3101 from 10K ohm to 100L ohm for +12VSUS low rating.

B5: P60: According to "EOS of Battery SMBus" report:
        P60: Change R6001,R6002,R6003 from 0 ohm to 330 ohm.
        P60: Change C6006,C6007,C6008 from 47PF to 33PF.

B6: P32: DNI R3205 for test purpose.

B7: P32: DNI SW3201,R3202 for not support.

B8: P66,51,21: DNI JMB360 circuit for ES1 sample SATA OK.

B9: P33: Mount D3301,D3302 for ESD protect as default setting.

[BOM modify - PWR]

PB1: P80: Adjust loadline change R8021 from 3.92KOhm to 3.65KOhm.

PB2: P80: Reduce transient undershoot
         change R8037,R8060 from 2KOhm to 2.49KOhm.
         change R8035,R8054 from 1.5KOhm to 2.21KOhm.

PB3: P81: +3VO from FB mode to fix mode
         Mount R8133 ,un-mount R8134,change R8111 from 20K Ohm to 0 Ohm

PB4: P82: Change L8201 from 2.2UF to 1.5UF ,un-mount CE8204 for add FB voltage
         Change L8251 from 2.5UF to 1.5UF ,change CE8252 from 100UF to 220UF for reduce transient pulse
         for reduce transient pulse

PB5: P91: Change C9102 from 0.033UF to 0.1UF.

PB6: P91: Change R9109 from 200K to 100K,adjust +1.05VM rising.

PB7: P92: Change R9205 from 100K to 10K,adjust SYSTEM_PWRGD rising.

PB8: P80,P81,P82,P83,P86: Change C8001,C8003,C8006,C8009,C8110,C8113,C from 100K to 10K,adjust SYSTEM_PWRGD rising.

ASUS	Title : System History	
ASUSTeK COMPUTER INC. NB	Engineer:	
Size: C	Project Name: M60J	Rev
Date: Thursday, July 02, 2009	Sheet 95 of 99	

[M52J] R1.1=> R1.2

(Release on 2009/01/12)

[Layout Changed - EE]

L1. P66,51,21: Del JMB360 cirsuit for PCH SATA workable.
P21,24,40,41,42: Change CB_ from R5C833 to R5U230.

L2. For no support AUB,delete or modify related circuit:
P03,P06,P21,P22,P23,P26,P45,P46,P47,P48,,P57,P70,P71,

L3. Change audio circuit from ALC663 to ALC269.

L4. For one phase bug fix:R8047: 0-->10K, R8041.2-->R8047.1, R0616: 10K-->0ohm

L5. Layout modify for DG,Mow,EDS:
P20,P21,P:25,P27,P32

L6. Layout modify for new EC 8541 colay: P28,P30

L7. Modify EC pin assignment for charger change:P30

L8. P45: Add BUF_PLT_RST# to BL_EN circuit.

L9. P45: reserverd for RF request .

L10. P52: Add CE5202 to avoid voltage droop .

L11. P32: Delete SW3201,R3202 for no support force-off switch.

[Layout Changed - PWR]

PL1. P81: SYSTEM PWM change from MAX17020 to pin to pin RT8206A (for IC bug)
PL2. P88: Charger IC change from MAX17015 to MB39A132 (for IC bug & EMI)

PL3. P88,P60: Change BAT in jump & bead from P88 to P60
PL4. P.86: Delete P86 +VGA_CORE
PL5. P.80: PM_PSI# pull low follow intel schematic
PL6. P90 Delete battery detect circuit
PL7. P80 VID0-6, PM_DPRSLPVR, PM_PSI# pull high power from +VTT_PWR
Change to +VTT_PCH
PL8. P81 System +3VS,+5V voltage change from resister adjust to fix mode
PL9. P90 Delete battery detect circuit

[EMI request]

ITEM E:

1.P88. BAT : L8801, L8803 要上 for EMI
-->L6001,L6002
2.P29. CLK Gen. : R2935 , R2936 改 Bead 120 ohm for EMI
-->L2901,L2902
3.P36. SPDIF1,2_OUT : R6502 , SL3652 改 Bead 120 ohm for EMI
-->L6501,L3622
4.USB power : R6501 , R4505 , R5201 改 Bead 120 ohm for EMI
-->L6502,L4504,L5203
5.C4508 要上 for EMI
-->Mount C4508
6.USB I/O port & CMOS 同時 Run 會有 EMI issue,建議在 USB EHCI define
時能將這兩者分開放
-->已交換,port4=WiFi/WiMax,port9=Camera.
7.LAN : R3306 , R3338 , R3332 , R3337 改成 Bead ; +1.05VM_LAN 上 0.1uF 靠近 R3341
-->L3301, L3303,L3302,L3304,C3314.
Note: 1.請協助確認bead是否可只上R3341就好.
2. C3313,C3314是否可以只上一個,上哪一個?
8.LVDS : C4506 要上 0.1uF ; LCD_PWM要上 0.1uF
-->Mount C4506, LCD_PWM預留10PF不上C4514.
9. P36. GND 到 GND_Audio 的 short line 增加三個 (或是電阻直接改 short line)
-->SL3651,SL3652,SL3653

[BOM modify - EE]

B1. BOM modify for DG,Mow,EDS:
P03,P21,P24,P25

[BOM modify - PWR]

B1 P80 Change CE8806,CE8807 from mount to un-mount

B2 P80 +Vcore output CAP from Panasonic 470Uf/2V 4.5m Ohm change to Panasonic 330/2V 6m Ohm

B3 P80 Change Q8007,Q8001,Q8005,Q8000 from SI4686BDY to SI7170DP
Change Q8002,Q8004 from SI4634BDY to SI7686DP

B4 P81 Change CE8101,CE8102 from CHEMICON 220UF/6.3V 10m Ohm to CHEMICON 150UF/6.3V 19m Ohm

B5 P82 Change CE8204,CE8207 from Panasonic 330/2V 6m Ohm to Panasonic 220/2V 15m Ohm

B6 P82 Change CE8252 from CHEMICON 330UF/4V 10m Ohm to CHEMICON 560UF/2.5V 10m Ohm

B7 P83 Change CE8305 from CHEMICON 330UF/4V 10m Ohm to CHEMICON 560UF/2.5V 10m Ohm

B8 P91 Change Q9101 from SI4634DY Rdson=6.7mOhm to IRF8707PBF Rdson=17.5mOhm

B9 P91 Change C9101, C9103, C9105, C9106, C9108, C9110, C9122 from mount to un-mount

[M52J] R1.2=> R1.21

(Release on 2009/03/12)
B1. For EA team signal quality test:
P21 Change RX2103,RX2104 from 0ohm to 22ohm
P24 Change R2404,R2406 from 22ohm to 33ohm

B2. P47 R4708:100K-->1K for bug fix(0.3V-->3V).

[M52J] R1.21=> R1.3

(Release on 2009/04/20)

L1. P29,25: Change clock GEN: ICS9LPR362-->ICS9LRS3197 for corechip.

L2. P33,34,21,25: Change LAN:HANKSVILLE-->AR8131 for corechip.

L3. P18: Delete M2 solution and modify description.

L4. P19: Delete VID controller.

L5. P30: Fix error: TP_DAT,TP_CLK pull up +3VA_EC-->+5VS.

L6. P24,53,P64: For PCH SKU compatible:
TV_Turner: port 6-->port4.
WLAN: port 4 -->port8.

L7. P20,21,24,25,67 delete PCH XDP.

L8. P25 for PCH GPIO define change:

P25. GPIO15,GPIO28 exchange.

L9. P53: Fix error for WLAN_ON#.

L10. R6741,R6742 move to R2621,R2622 for some project without BRAIDWOOD.

L11. P61: D6101 change from RB751V to BAT54C.

L12. P30,P56: for touch sensor board rev 1.2.
Move CAP_ACK#(GPE7)-->CAP_ACK_A#(GPI6),add CAP_ACK_B#,
delete R5624,delete Q5602@,Q5604@,R5626@,add SL3005,SL3006.

L13. For N10P-GS VGA card: (Layout impedance change).
P48:Move D4802 from net HDMI_HPD_CON to HDMI_HPD.
P48:Add R4809~R4816,Q4802 for HDMI termination.

L14. P24,P30: For PCI_CLK layout guide update.
L15. P21,P27:Disable Intel LAN.
P27. Delete R2723,net +1.05VM_LAN.

L16. Change ESD diode to IP4223 for cost down.
D3106,D4301,D4503,D4605,D4701,D4702,D4703,D5201,D6501,D6601

L17. For iAMT disable.

P30,P31,P92. Delete net ME_+VM_PWRGD,D9202,R3070@,R3105,R3108@
P31.Delete U3101(IT8301E) block.
P30.Delete R3066,R3067,R3068,R3072,net EGAD,EGCS,EGCLK,EGCLK_EC.
P57 Delete Q5708,R5709,R5716,R5717,Q5710,R5718,R5719,no connect Q5707B.
P81.Delete net ME_PM_SLP_LAN#,SLP_LAN#_PWR,R8131,JP8117
P81.Delete net ME_SLP_M_EC#,SLP_M#_PWR,R8129,JP8116
P84.Delete +3VM load switch block,ME_+VM_PWRGD block.
P22.Delete ME_PM_SLP_M# to PM_SUSB#,delete R2254,R2238,Add T2208.
P22.Delete net ME_PM_SLP_LAN#,R2254,R2257,add T2207.
Connect ME_PWROK_PCH to PM_PWROK_PCH.
Delete R2272@,R2268,D2204@,R2271.
P27. Delete net +1.05VM_ORG_R[1..4],delete R2736,R2727,R2738,R2739.
Connect +1.05VS to +1.05VM_ORG.
Connect +3VS to +3VM via JP2705.

L18. For EC8541:
P28: Delete R2848,R2856,net PM_RSMRST#.
Add Q2804,Q2805,R2830,R2835,R2836,R2838.
P28: Others: please see the description.

L19. net connection change.(for possible costdown)
PM_PWROK_PCH:D2202.2 -->D2202.1
PM_RSMRST#_PCH:D2203.1 -->D2202.2
R2275:0ohm -->10Kohm
L20. P20,30.connect HDA_DOCK_EN# to EC for BIOS request

L21. P7,P37 change XDP from 60pin to 24pin SFF.

L22. P56: prevent touch sensor board leakage.
Change J5601 net SMB1_CLK-->SMB1_CLK_S,SMB1_DAT-->SMB1_DAT_S

L23. For component kinds down:F5201<--F6501,F4801<--F4502

L24. P45. Delete F4502 for costdown.

L25. P28. Fix SPI circuit for EC8541.

B1. P36. Change ALC269 From A5 to VA6(P/N: 02G611005006).
B2. P30. Change U3001 from IT8512E to IT8541E.
B3. P18. Change Vref solution from M1 to M3.
DNI R1801,R1804,Mount R1805,R1806.
B4. P67. For no support Braidwood:
DNI J6704,R6740,
B5. Intel DG update:
P03. change R0320 & R0321.

B6.P70. correct name to match page rule:
C7709-->C7009...,C7010,C7011,C7012,C7013,C7014,C7705.
T7006,T7007,T7008

B7.P70. DNI R7022, mount R7023 for VGA timing.

B8.P50. Change U5002 from G781-1 to G781 for SMBUS addr.

B9.P21. DNI X2101,C2101,C2102,R2151 for PCH only support BTM mode currently.

B10. Improve clock ppm:
P29: C2907,C2908: 24pF-->27pF.
P40: C4040,C4066: 22pF-->27pF.

B11. Add R3205 support thermal protection.

[M52J] R1.3=> R1.31

(Release on 2009/06/03)
B1. Change connector for ME request.
J4501:12G170010409-->12G170010408
J4801:12G241101928-->12G241101193V

B2. Change MOS 2N7002 P/N to 07G005000313 for RD pool.
Q0301,Q2001,Q2901,Q3302@,Q4301@,Q4402,Q4503,Q4802,Q6102@.

B3. Change U2801,U2802 for vendor EOL.
05G00160F010-->05G00160G010

B4. Change EC from 8541 to 8512.
DNI C2804,R2848,R2855,R2856,U2803,R2857,R2858,R2859,R2860,R2861,R3002,R3003,R3004,R3005
Mount R2846,R2853,R2854,R2827,R2828,U3003,R3053,R3043,C3019
Change U3003: 05G001405010-->05G00120A010.
Change U3001: 06G042025010-->06G042005012.

B5. WW22 MOW,Implement M1 & M3 method: mount R1801,R1804.

B6. WW20 MOW,change R2029 from 100K@ to 1K@.

[M52J] R1.31=> R1.32

(Release on 2009/06/05)

B1. P28. DNI U2802 for costdown.
B2. P30. Change EC from 8512 to 8502 for costdown.

[M52J] R1.32=> R2.00

(Release on 2009/07/02)

L1. P28. ChangeJ2801.1 power for dediprog flash.
L2. P47. ChangeR4701 10K-->100K,add R4709 to fix DP hot-plug issue.
L3. P20. Fix error that HDA_DOCK_EN# can't pull to GND directly.
L4. P36,P20. Remove PC beep circuit for design IP change.
L5. P03,06,20,27,30,32,56,B0,65:Add test point for factory request.
L6. P45: Change C4501 0.1uF(0402)-->0.22uF(0603) for LCD power timing.
L7. P37: Change J3701 12G171000049-->12G17100004F to fix ME bug.
L8. P53: Change J5302 12G030000524-->12G03011052X for EOL.
Change H5303、H5304 13G021036001-->13GP2360M110-1 to match 12G03011052X.
L9. P43: Change U4301 06G030053010-->06G030091110 for design IP.
L10. For EMI request:
Add C2617,C2618,C2736,C2748,C2749,C4509,C4510,C4519@,C5101,mount C3406.
USB_PN0, USB_PN1 在J6501 預留 choke
USB_PN2,3,5 預留 0 ohm
L11. For EC request pin assignment:
GPB.2 (ME_AC_PRESENT);GPG.0 (ME_SusPwrDnAck);GPI.4 (PCH_TEMP_ALERT#)
Change GPF.0 (PCH_SPI_OV) to GPF.7
L12. For Touch seneor default state:
Del RN3007,change CAP_ACK_A#,CAP_ACK_B# pull up to +3VS(RN3008).
L13. Change C2101@(27pF) to ohm to meet Calpella DG R1.6,Page 369.
L14. P29: Colay clock GEN. 9LRS3197/9LVS3162.
L15. Fix thermal policy:
P25. Move & mount R2501,add R2505
P32. Follow designip.
P50. Use GMT G709 as thermal protection.
L16. P45. Reserve soft-start circuit to prevent LCD inrush current.
L17. P65. Add C6514,C6515 for EMI request(prevent TV noise).
L17. P45,P03: change JP4599 for lead part.

B1. P46. Change C4601~C4601 10PF-->5PF for CRT signal quality.
B2. P45. Change J4501:12G170010409-->12G170010408 for footprint not compatible.
B3. P23. ChangeR2321 from 1Kohm,0.5%-->1Kohm,5% for DAC_IREF not used.
B4. P58. Move page 92 to page 58, rename components.
B5. P06. Delete unused nets.
B6. P20,28: Change R2032,R2033,R2837,R2840,R2841 to 33ohm to fix dediprog checksum error issue.
B7. P52: Change L5203 09G012080023--> for common part.
B8. P52: Change C6508,C6509 100pF-->1000pF for EMI request(prevent TV noise).
B9. P24: DNI R2414 for no braidwood.

[M52J] R2.00=> R2.01

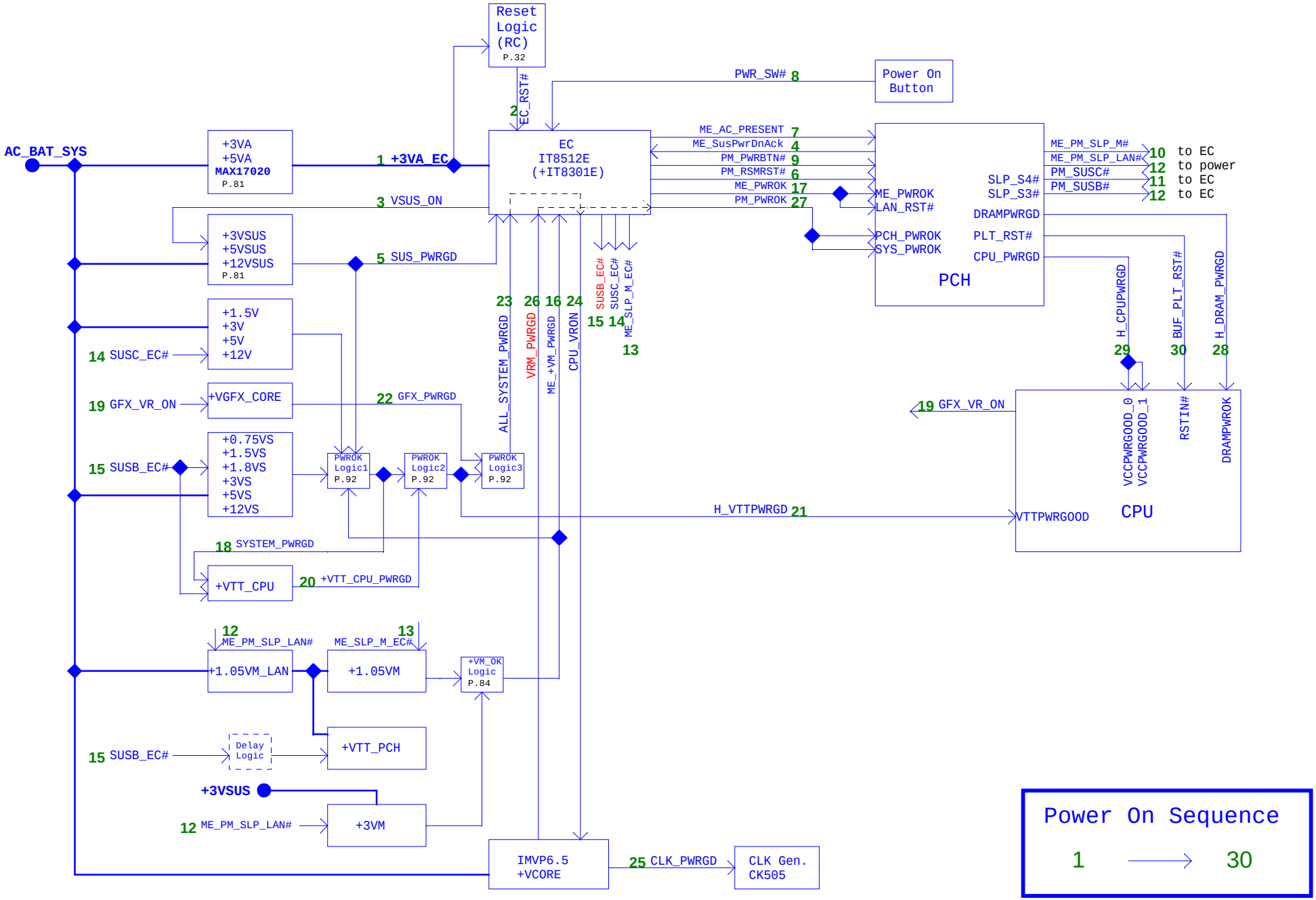
(Release on 2009/07/02)

B10. P20,P28: For only one SPI ROM:
DNI R2834,R2832,C2803,R2828,R2827,R2852,R2850,R2846,R2851,R2823,R2854,R2849,R2853,R2033
B11. P20,P67:remove support of PCH JTAG
P20: R2034,R2035,R2036,R2037,R2038,R2039,R2040,R2041
P67: R6702,J6701,R6721,R6722,R6723,R6724

ASUS	Title : System History	
ASUSTeK COMPUTER INC. NB	Engineer:	
Size: C	Project Name: M60J	Rev
Date: Friday, July 10, 2009	Sheet 96 of 99	

AC-IN Mode

M52J Power On Sequence Diagram Rev. 0.31



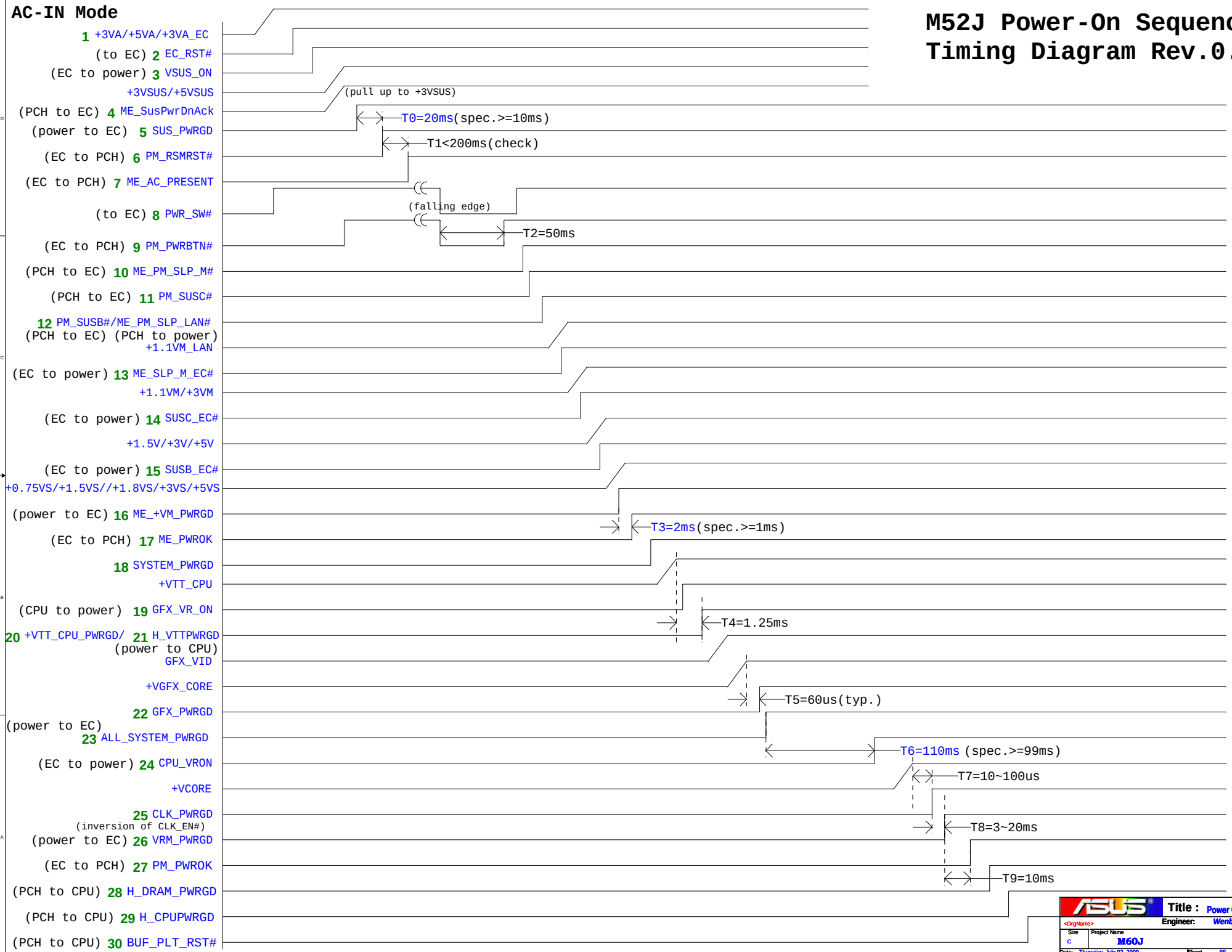
Power On Sequence

1 → 30

ASUS ASUSTeK COMPUTER INC	Title : POWER SEQUENCE	
	Engineer: James1_Wu	
Size C	Project Name M60J	Rev 2.00
Date: Thursday, July 02, 2009	Sheet 98 of 99	

M52J Power-On Sequence Timing Diagram Rev.0.31

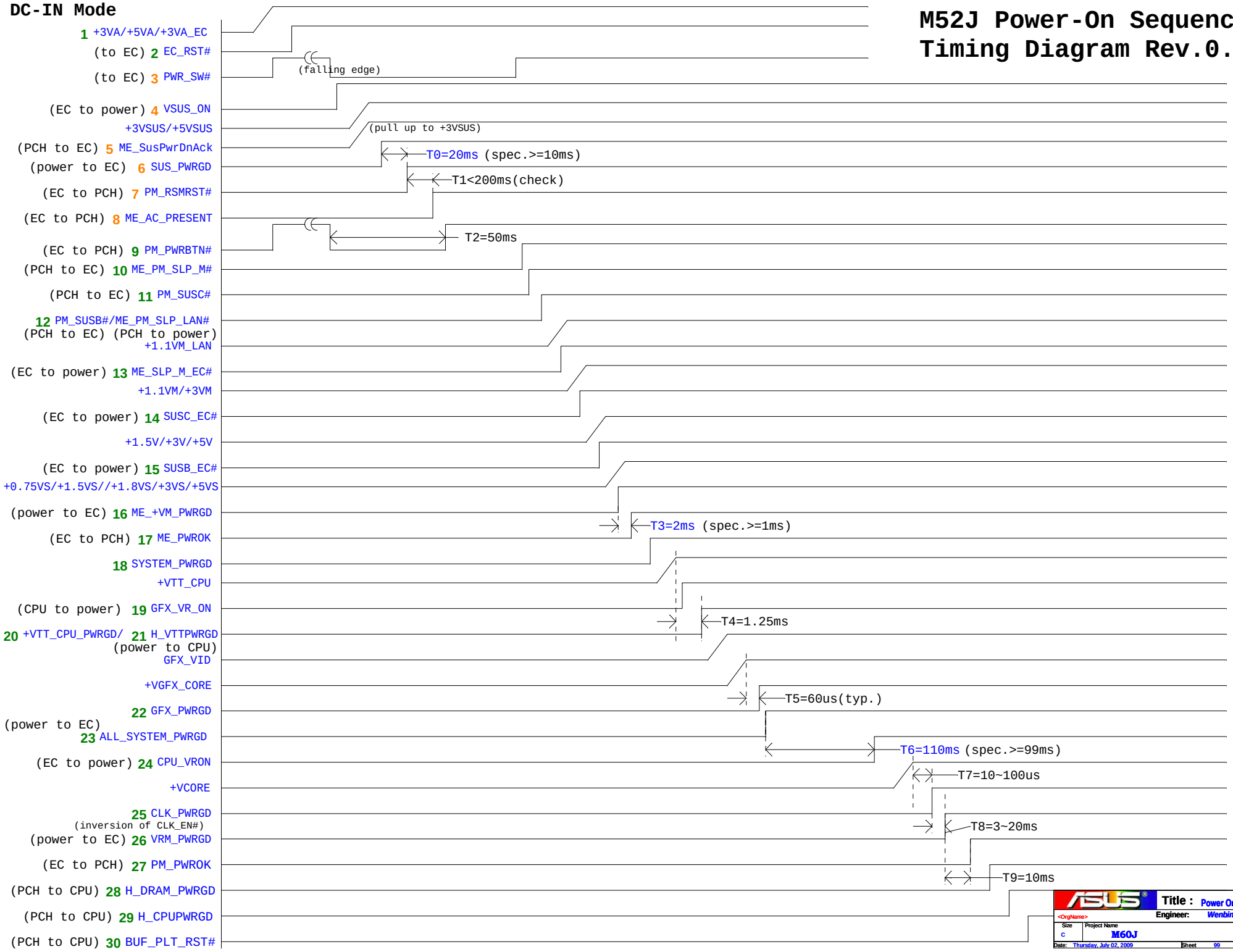
AC-IN Mode



ASUS	Title : Power On Timing		
<OrgName>	Engineer: Wenbin Jian		
Size C	Project Name M60J		Rev 2.00
Date: Thursday, July 02, 2009	Sheet 99 of 99		

M52J Power-On Sequence Timing Diagram Rev.0.31

DC-IN Mode



ASUS	Title : Power On Timing		
<OrgName>	Engineer: Wenbin Jian		
Size C	Project Name M60J		Rev 2.00
Date: Thursday, July 02, 2009	Sheet 99 of 99		