A3E CONTEXT

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36_STARTUP CIRCUIT(1)
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46_POWER ON SEQUENCE
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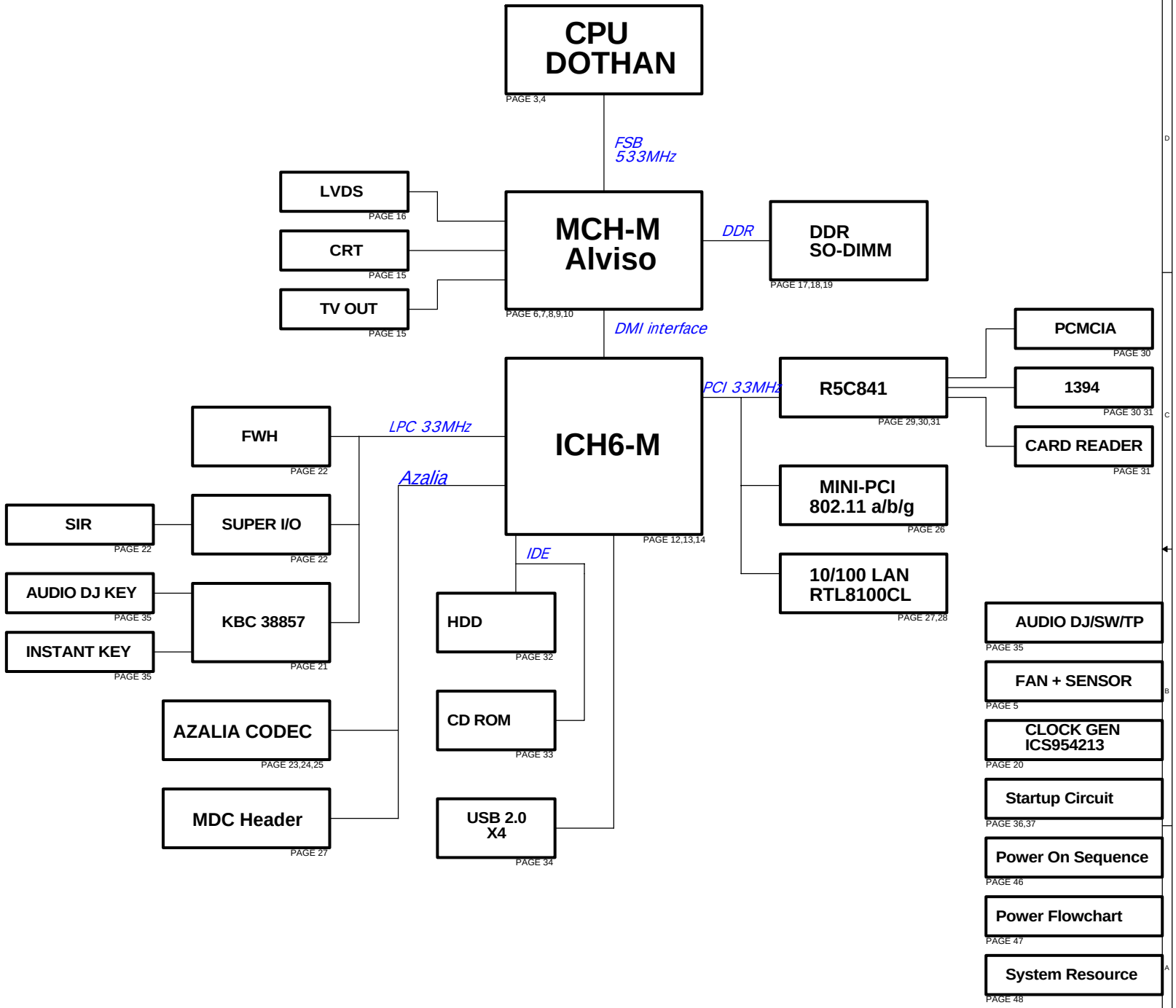

ASUSTeK COMPUTER INC	Title : BLOCK DIAGRAM	Engineer: Quan-Tai Lin
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 1 of 51	

REVISION LIST

R1.0 2005/01/10

POWER INTERFACE

SIGNALS	TYPE	POWER
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
VRON	O	+3.3V
PM_DPRSLPVR	O	+3.3V
CPU_STP#	O	+3.3V
RST_BTN#	O	+3.3V
CLK_EN#	I	+3.3V
DELAY_VR_PWRGD	I	+3.3V
OTP_RESET#	I	+3.3V
SHUT_DOWN#	I	+3.3V
BAT_LEARN	I	+3.3V
BAT_LLOW#_OC	I	+3.3V
BAT_IN#_OC	I	+3.3V
CHG_EN#	I	+3.3V
CHG_FULL_OC	I	+3.3V
CHG_LED_UP	I	+3.3V
SMCLK_BAT1	IO	+3.3V
SMDATA_BAT1	IO	+3.3V
SUSB#	O	+3.3V
SUSC#	O	+3.3V
1.8V_PWRGD	I	+3.3V
1.5VS_PWRGD	I	+3.3V
VSUS_ON	O	+3.3V
ACIN_OC	I	+3.3V
ACIN#	I	AC_BAT_SYS
+3VA	PWR	+3.3V
+5VA	PWR	+5V
+5VLCM	PWR	+5VLCM
A/D_DOCK_IN	PWR	DC
AC_BAT_SYS	PWR	DC

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.95A
+VCC_GMCH	1.05V	4.12A
+0.9VS	1.25V	0.85A
+1.5VS	1.5V	4.33A
+1.5V	1.5V	300 mA
~~+1.5VSUS~~	~~1.5V~~	~~270 mA~~
+2.5V	2.5V	6.68A
+2.5VS	2.5V	0.3 A
+3VS	3.3V	1.732A
+3V	3.3V	1.515A
+3VSUS	3.3V	540 mA
+5VS	5V	4.1A
+5V	5V	0.5A
+5VSUS	5V	0.5A
+12V	12V	0.25A
+12VS	12V	0.25A

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	18 mils

37.5 OHM	WIDTH
TOP/BOT	11 mils
IN1/IN2	9.5 mils

50 OHM	WIDTH
TOP/BOT	6 mils
IN1/IN2	5 mils

55 OHM	WIDTH
TOP/BOT	5.5 mils
IN1/IN2	4.5 mils

75 OHM	WIDTH
TOP/BOT	4 mils
IN1/IN3	3.5 mils

Differential

85 OHM	WIDTH/SPACE
TOP/BOT	5.5 mils/ 4 mils
IN1/IN2	4.5 mils/ 4 mils

90 OHM	WIDTH/SPACE
TOP/BOT	5.5 mils/ 5 mils
IN1/IN2	4.5 mils/ 5 mils

100 OHM	WIDTH/SPACE
TOP/BOT	6 mils/ 11 mils
IN1/IN2	5 mils/ 12 mils

110 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 13 mils
IN1/IN2	4 mils/ 12 mils

PCI INTERFACE

PCI_REQ#

MINIPCI	PCI_REQ#3
10/100	PCI_REQ#2
CB&1394	PCI_REQ#1

IDSEL

MINIPCI	PCI_AD19
10/100	PCI_AD16
CB&1394	PCI_AD17

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1	TOP
L2	GND
L3	IN1
L4	IN2
L5	GND
L6	BOT

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```
SIGNAL  IN:   VR_VID[0..5]
              PM_DPRSLPVR
              STP_CPU#
              PM_PSI#
              CPU_VRON
              MCH_OK
        OUT:  DELAY_VR_PWRGD
              CLK_PWR_GD#

POWER   IN:   AC_BAT_SYS
              +5VO
              +3VO
        OUT:  +VCORE
```

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```
SIGNAL  IN:   SUSC#_PWR
              VSUS_ON

POWER   IN:   AC_BAT_SYS

        OUT:  +12VO
              +3VO
              +5VO
```

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```
SIGNAL  IN:   SUSB#_PWR
              SUSC#_PWR
              CPU_VRON

POWER   IN:   AC_BAT_SYS
              +5VO

        OUT:  +1.8V
              +1.5VS
              +2.5VS
              +VCC_GMCH_CORE
              +5VALWAYS
              +3VALWAYS
              +VCCP
```

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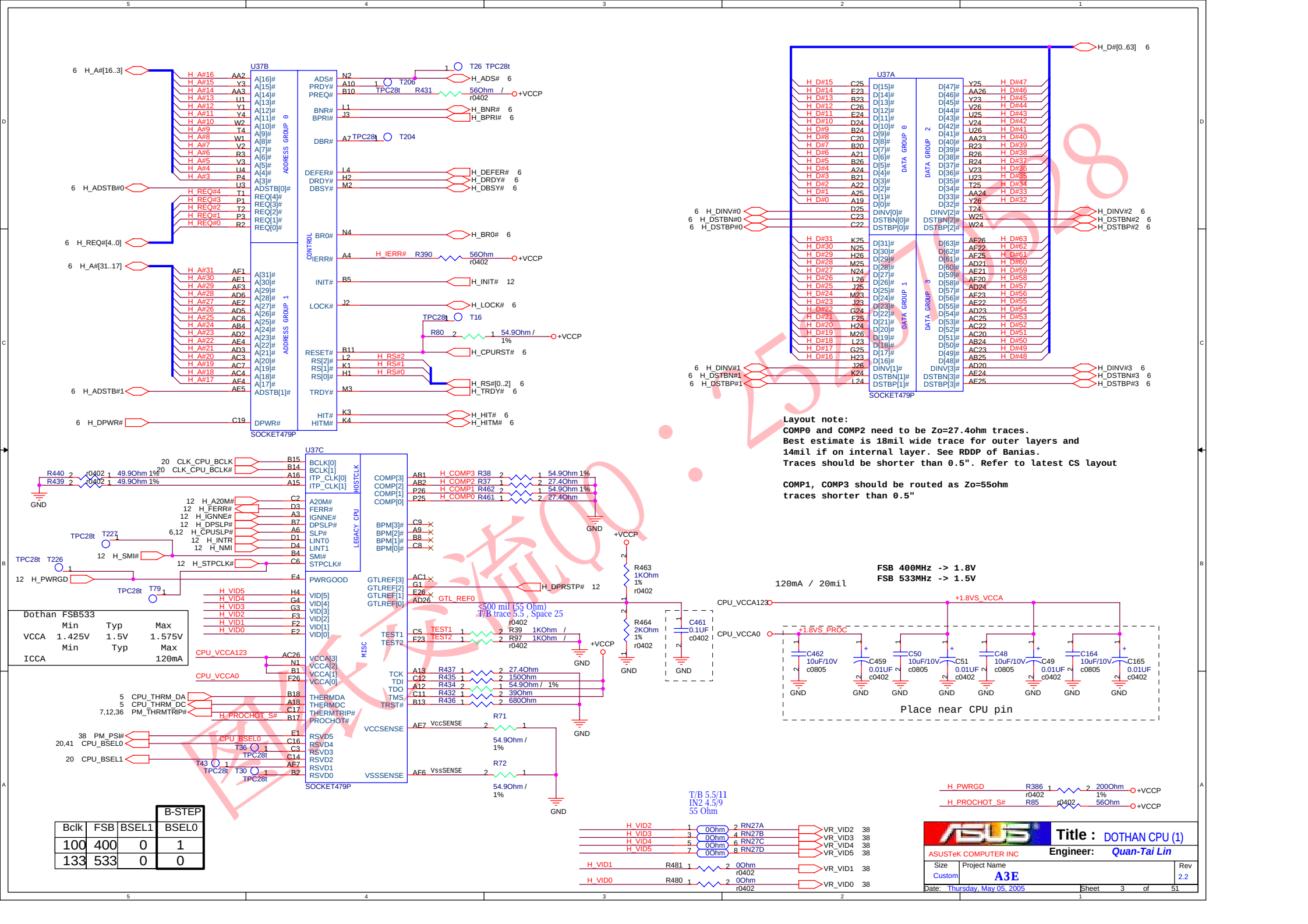
```
SIGNAL  IN:   SUSB#_PWR

POWER   IN:   +3V
              +1.8V

        OUT:  +0.9VS
```

ASUSTeK COMPUTER INC	Title : REVISION LIST	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 2 of 51	


U37B
SOCKET479P
ADDRESS GROUP 0
ADDRESS GROUP 1
CONTROL
6 H_A#[16..3]
6 H_ADSTB#0
6 H_REQ#[4..0]
6 H_A#[31..17]
6 H_ADSTB#1
6 H_DPWR#
ADS# N2 H_ADS# 6
PRDY# A10 T206 TPC28t
PREQ# B10 R431 56Ohm / r0402 +VCCP
BNR# L1 H_BNR# 6
BPRI# J3 H_BPRI# 6
DBR# A7 TPC28t T204
DEFER# L4 H_DEFER# 6
DRDY# H2 H_DRDY# 6
DBSY# M2 H_DBSY# 6
BR0# N4 H_BR0# 6
IERR# A4 H_IERR# R390 56Ohm r0402 +VCCP
INIT# B5 H_INIT# 12
LOCK# J2 H_LOCK# 6
TPC28t T16
R80 54.9Ohm / 1% +VCCP
RESET# B11 H_CPURST# 6
RS[2]# L2 H_RS#2
RS[1]# K1 H_RS#1
RS[0]# H1 H_RS#0
H_RS#[0..2] 6
TRDY# M3 H_TRDY# 6
HIT# K3 H_HIT# 6
HITM# K4 H_HITM# 6
T26 TPC28t
U37A
SOCKET479P
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
H_D#[0..63] 6
6 H_DINV#0
6 H_DSTBN#0
6 H_DSTBP#0
6 H_DINV#1
6 H_DSTBN#1
6 H_DSTBP#1
H_DINV#2 6
H_DSTBN#2 6
H_DSTBP#2 6
H_DINV#3 6
H_DSTBN#3 6
H_DSTBP#3 6
Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
Best estimate is 18mil wide trace for outer layers and
14mil if on internal layer. See RDDP of Banias.
Traces should be shorter than 0.5". Refer to latest CS layout
COMP1, COMP3 should be routed as Zo=55ohm
traces shorter than 0.5"
U37C
SOCKET479P
HOSTCLK
LEGACY CPU
MISC
20 CLK_CPU_BCLK B15
20 CLK_CPU_BCLK# B14
R440 r0402 49.9Ohm 1%
R439 r0402 49.9Ohm 1%
GND
12 H_A20M# C2
12 H_FERR# D3
12 H_IGNNE# A3
12 H_DPSLP# B7
6,12 H_CPUSLP# A6
12 H_INTR D1
12 H_NMI D4
12 H_SMI# B4
12 H_STPCLK# C6
TPC28t T227
TPC28t T226
12 H_PWRGD E4
TPC28t T79
H_VID5 H4
H_VID4 G4
H_VID3 G3
H_VID2 F3
H_VID1 F2
H_VID0 E2
CPU_VCCA123 AC26
CPU_VCCA0 F26
5 CPU_THRM_DA B18
5 CPU_THRM_DC A18
7,12,36 PM_THRMTRIP# C17
H_PROCHOT_S# B17
38 PM_PSI# E1
20,41 CPU_BSEL0 C16
20 CPU_BSEL1 C14
CPU_BSEL0 C3
AF7
B2
T36 TPC28t
T43 TPC28t
T30 TPC28t
BCLK[0]
BCLK[1]
ITP_CLK[0]
ITP_CLK[1]
A20M#
FERR#
IGNNE#
DPSLP#
SLP#
LINT0
LINT1
SMI#
STPCLK#
PWRGOOD
VID[5]
VID[4]
VID[3]
VID[2]
VID[1]
VID[0]
VCCA[3]
VCCA[2]
VCCA[1]
VCCA[0]
THERMDA
THERMDC
THERMTRIP#
PROCHOT#
RSVD5
RSVD4
RSVD3
RSVD2
RSVD1
RSVD0
COMP[3]
COMP[2]
COMP[1]
COMP[0]
BPM[3]#
BPM[2]#
BPM[1]#
BPM[0]#
GTLREF[3]
GTLREF[2]
GTLREF[1]
GTLREF[0]
TEST1
TEST2
TCK
TDI
TDO
TMS
TRST#
VCCSENSE
VSSSENSE
AB1 H_COMP3 R38 54.9Ohm 1%
AB2 H_COMP2 R37 27.4Ohm
P26 H_COMP1 R462 54.9Ohm 1%
P25 H_COMP0 R461 27.4Ohm
C9
A9
B8
C8
AC1
G1
E26
AD26
H_DPRSTP# 12
GTL_REF0
<500 mil (55 Ohm)
T/B trace 5.5 , Space 25
C5 TEST1 R39 1KOhm /
F23 TEST2 R97 1KOhm /
r0402
+VCCP
A13 R437 27.4Ohm
C12 R435 150Ohm
A12 R434 54.9Ohm / 1%
C11 R432 39Ohm
B13 R436 680Ohm
AE7 VccSENSE R71 54.9Ohm / 1%
AF6 VssSENSE R72 54.9Ohm / 1%
R463 1KOhm 1% r0402
R464 2KOhm 1% r0402
C461 0.1UF c0402
FSB 400MHz -> 1.8V
FSB 533MHz -> 1.5V
120mA / 20mil
CPU_VCCA123
CPU_VCCA0
+1.8VS_VCCA
+1.8VS_PROC
C462 10uF/10V c0805
C459 0.01UF c0402
C50 10uF/10V c0805
C51 0.01UF c0402
C48 10uF/10V c0805
C49 0.01UF c0402
C164 10uF/10V c0805
C165 0.01UF c0402
Place near CPU pin
Dothan FSB533
Min Typ Max
VCCA 1.425V 1.5V 1.575V
Min Typ Max
ICCA 120mA
T/B 5.5/11
IN2 4.5/9
55 Ohm
H_VID2 RN27A VR_VID2 38
H_VID3 RN27B VR_VID3 38
H_VID4 RN27C VR_VID4 38
H_VID5 RN27D VR_VID5 38
H_VID1 R481 0Ohm r0402 VR_VID1 38
H_VID0 R480 0Ohm r0402 VR_VID0 38
H_PWRGD R386 200Ohm 1% +VCCP
H_PROCHOT_S# R85 56Ohm +VCCP
B-STEP
Bclk FSB BSEL1 BSEL0
100 400 0 1
133 533 0 0
ASUSTeK COMPUTER INC
Title : DOTHAN CPU (1)
Engineer: Quan-Tai Lin
Size Custom
Project Name A3E
Rev 2.2
Date: Thursday, May 05, 2005
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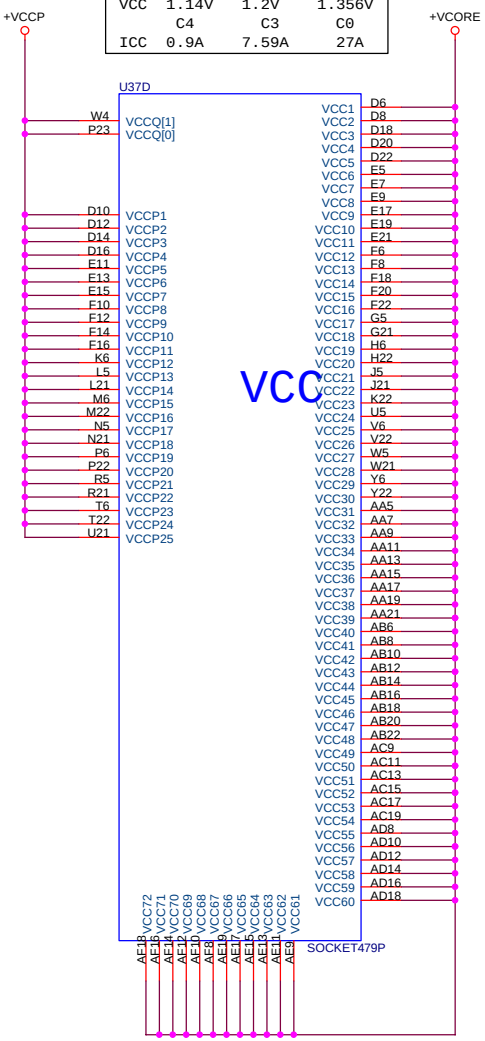
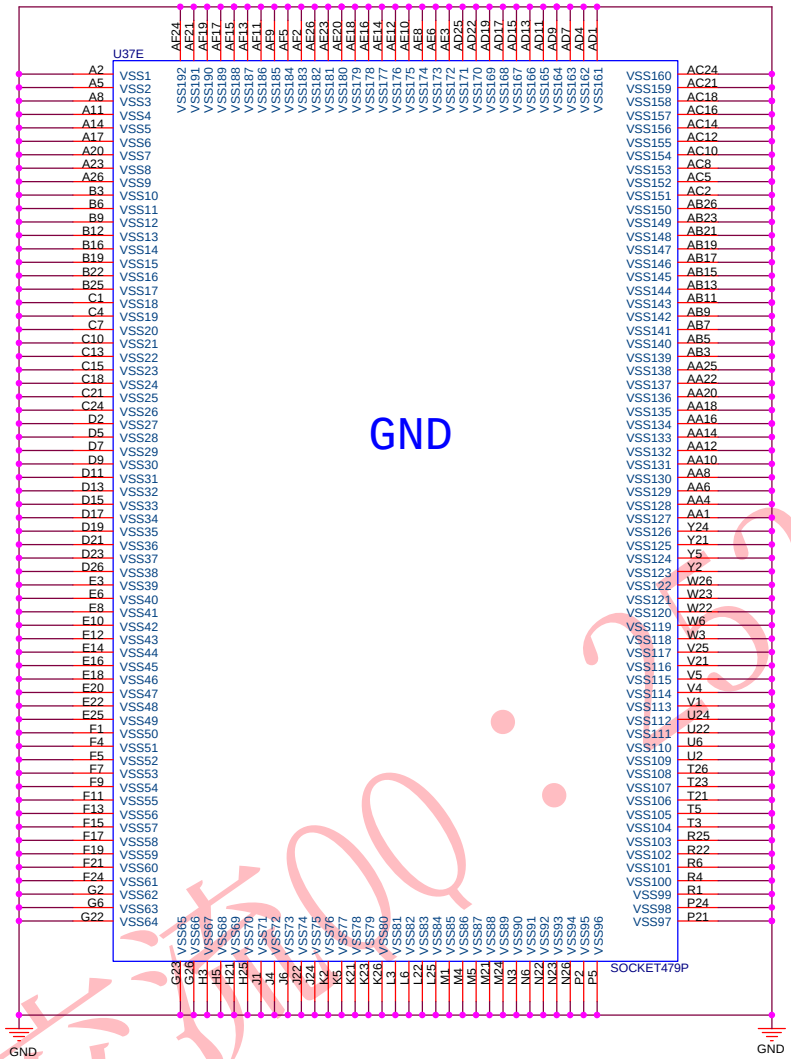
Dothan FSB533	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A



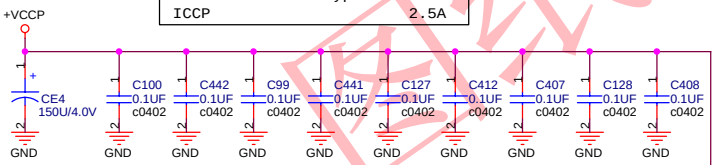


MOBILE DOTHAN VID TABLE

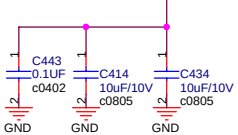
VID[5..0]	Voltage	VID[5..0]	Voltage
0 0 0 0 0 0	1.708V	1 0 0 0 0 0	1.196V
0 0 0 0 0 1	1.692V	1 0 0 0 0 1	1.180V
0 0 0 0 1 0	1.676V	1 0 0 0 1 0	1.164V
0 0 0 0 1 1	1.660V	1 0 0 0 1 1	1.148V
0 0 0 1 0 0	1.644V	1 0 0 1 0 0	1.132V
0 0 0 1 0 1	1.628V	1 0 0 1 0 1	1.116V
0 0 0 1 1 0	1.612V	1 0 0 1 1 0	1.100V
0 0 0 1 1 1	1.596V	1 0 0 1 1 1	1.084V
0 0 1 0 0 0	1.580V	1 0 1 0 0 0	1.068V
0 0 1 0 0 1	1.564V	1 0 1 0 0 1	1.052V
0 0 1 0 1 0	1.548V	1 0 1 0 1 0	1.036V
0 0 1 0 1 1	1.532V	1 0 1 0 1 1	1.020V
0 0 1 1 0 0	1.516V	1 0 1 1 0 0	1.004V
0 0 1 1 0 1	1.500V	1 0 1 1 0 1	0.988V
0 0 1 1 1 0	1.484V	1 0 1 1 1 0	0.972V
0 0 1 1 1 1	1.468V	1 0 1 1 1 1	0.956V
0 1 0 0 0 0	1.452V	1 1 0 0 0 0	0.940V
0 1 0 0 0 1	1.436V	1 1 0 0 0 1	0.924V
0 1 0 0 1 0	1.420V	1 1 0 0 1 0	0.908V
0 1 0 0 1 1	1.404V	1 1 0 0 1 1	0.892V
0 1 0 1 0 0	1.388V	1 1 0 1 0 0	0.876V
0 1 0 1 0 1	1.372V	1 1 0 1 0 1	0.860V
0 1 0 1 1 0	1.356V	1 1 0 1 1 0	0.844V
0 1 0 1 1 1	1.340V	1 1 0 1 1 1	0.828V
0 1 1 0 0 0	1.324V	1 1 1 0 0 0	0.812V
0 1 1 0 0 1	1.308V	1 1 1 0 0 1	0.796V
0 1 1 0 1 0	1.292V	1 1 1 0 1 0	0.780V
0 1 1 0 1 1	1.276V	1 1 1 0 1 1	0.764V
0 1 1 1 0 0	1.260V	1 1 1 1 0 0	0.748V
0 1 1 1 0 1	1.244V	1 1 1 1 0 1	0.732V
0 1 1 1 1 0	1.228V	1 1 1 1 1 0	0.716V
0 1 1 1 1 1	1.212V	1 1 1 1 1 1	0.700V

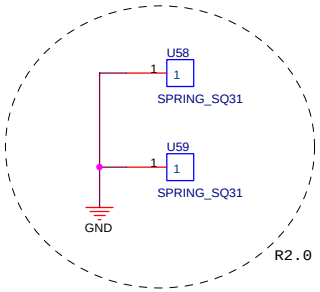
1.0V - 1.2V(+/- 5%)
S0-S1M: 2.5
A(CPU,MCH,ICH)

Dothan FSB533	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



+VCCP (CPU) Decoupling Capacitor
(Place near CPU)





R2.0 For EMI

图纸交流QQ：3267058

ASUSTeK COMPUTER INC	Title : DOTHAN CPU (2)	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 4 of 51	

Fan Speed Control

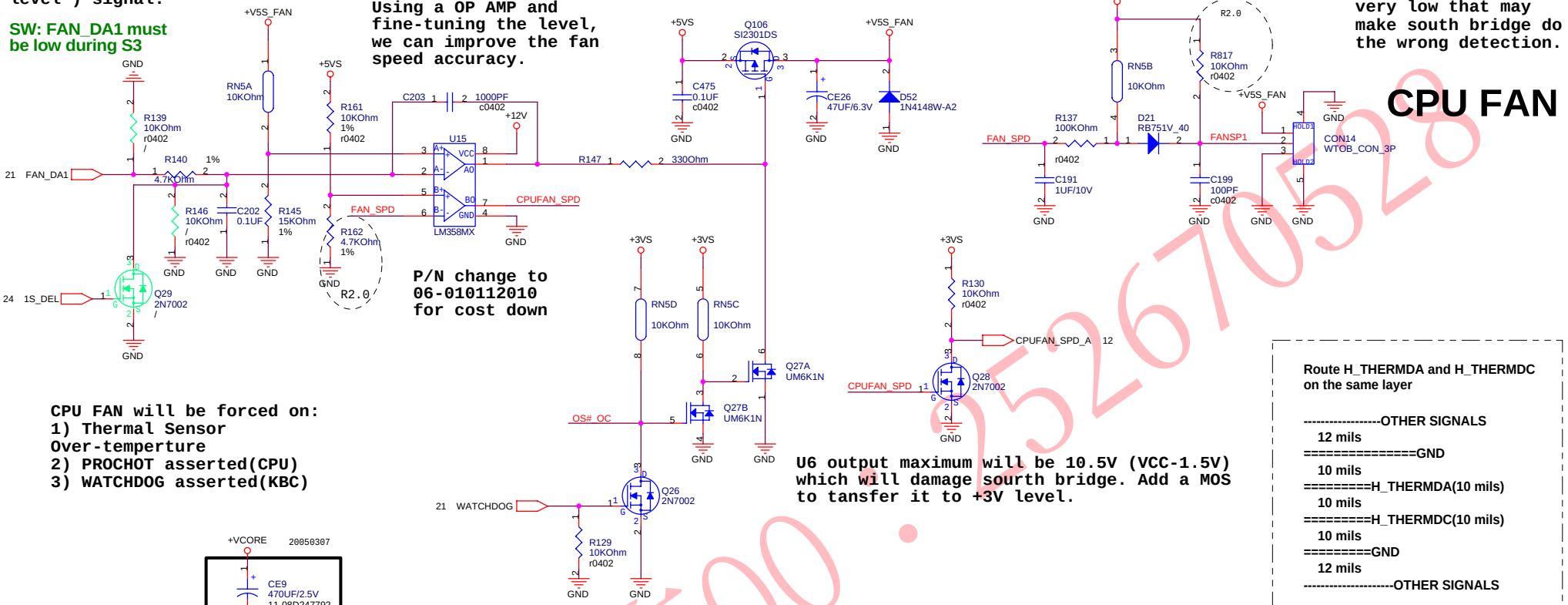
KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

CPU FAN



P/N change to 06-010112010 for cost down

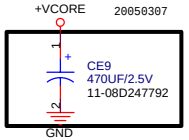
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) PROCHOT asserted(CPU)
3) WATCHDOG asserted(KBC)

U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.

Route H_THERMDA and H_THERMDC on the same layer

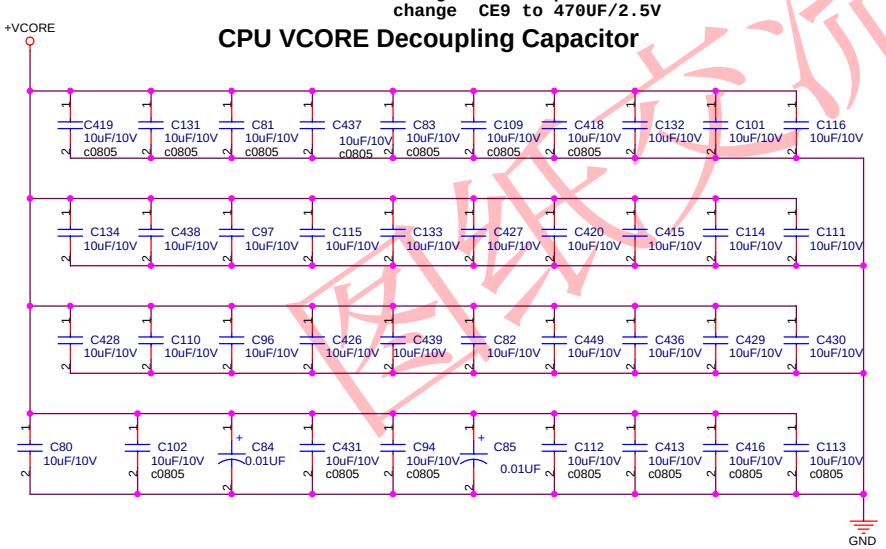
----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



Change CE10 to power and change CE9 to 470UF/2.5V

CPU VCORE Decoupling Capacitor

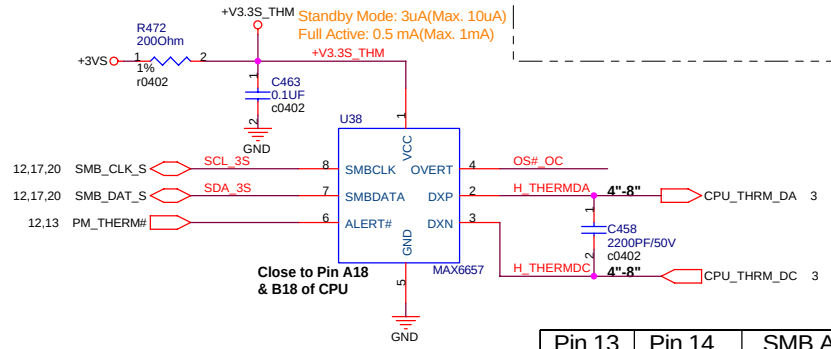


Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling

Four 200 uF are located in IMVP4



Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58

ASUSTeK COMPUTER INC

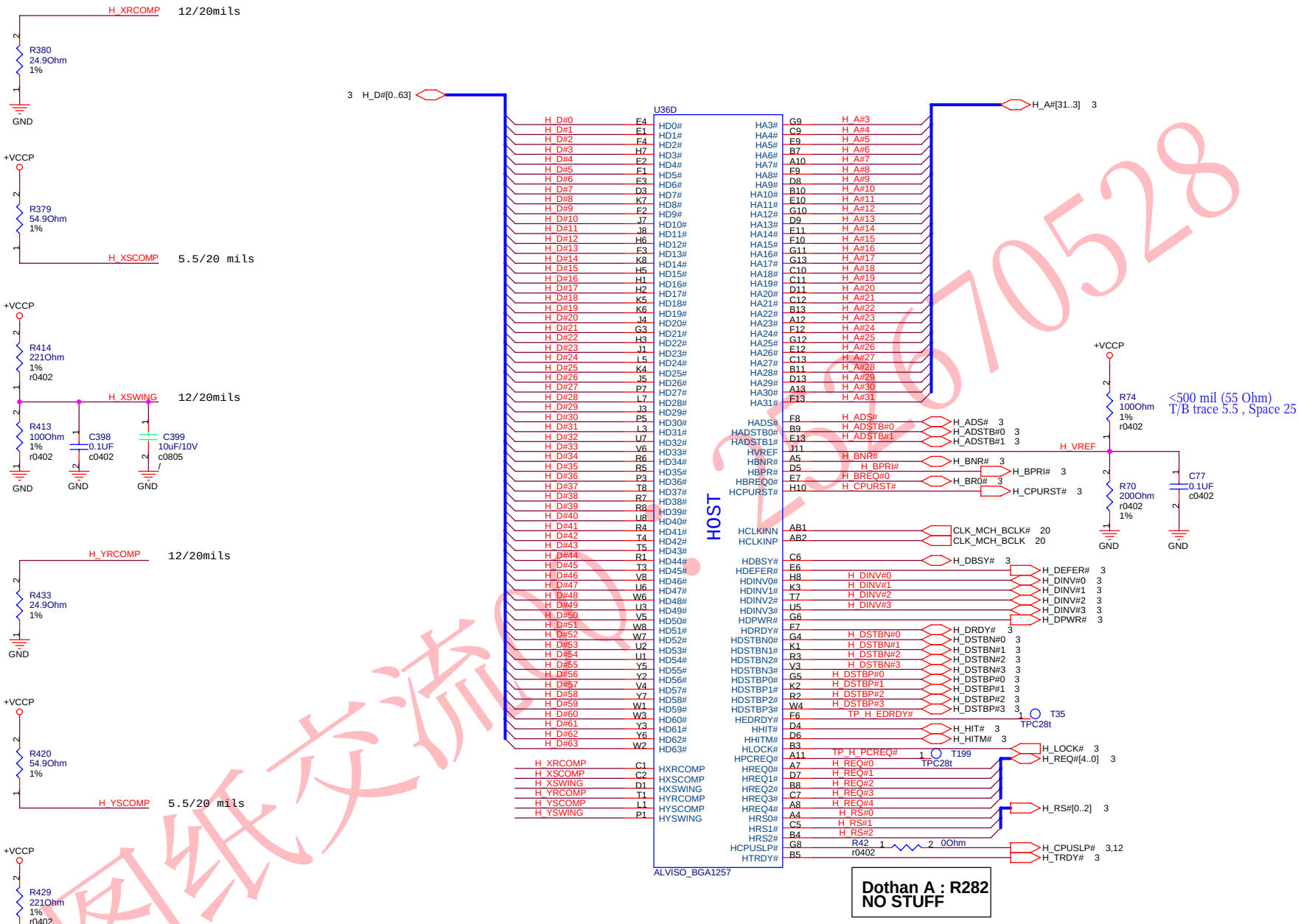
Title : THER-SENSOR,FAN

Engineer: Quan-Tai Lin

Size	Project Name	Rev
Custom	A3E	2.2

Date: Thursday, May 05, 2005 Sheet 5 of 51

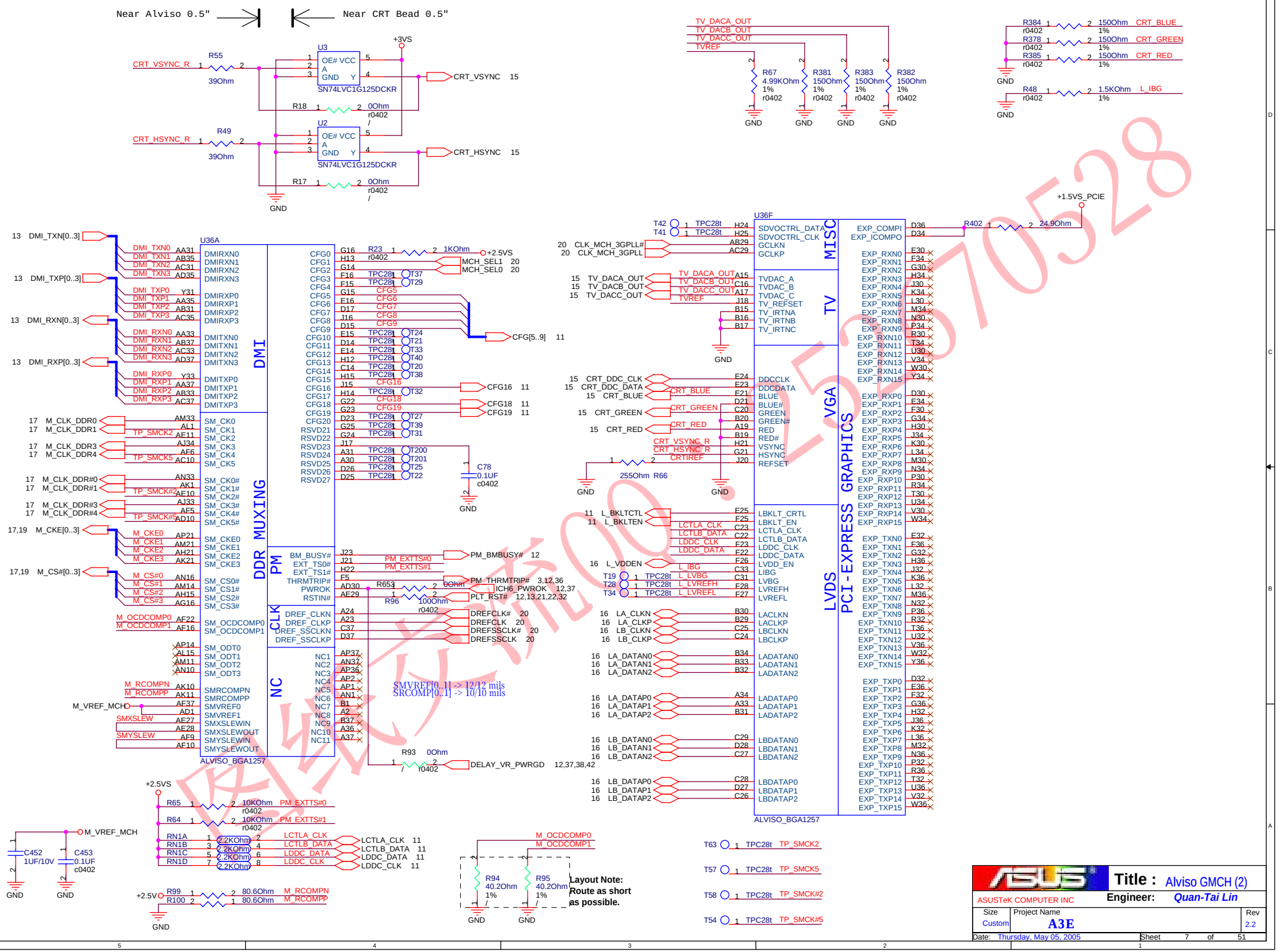
图纸交流QQ：2526705 28



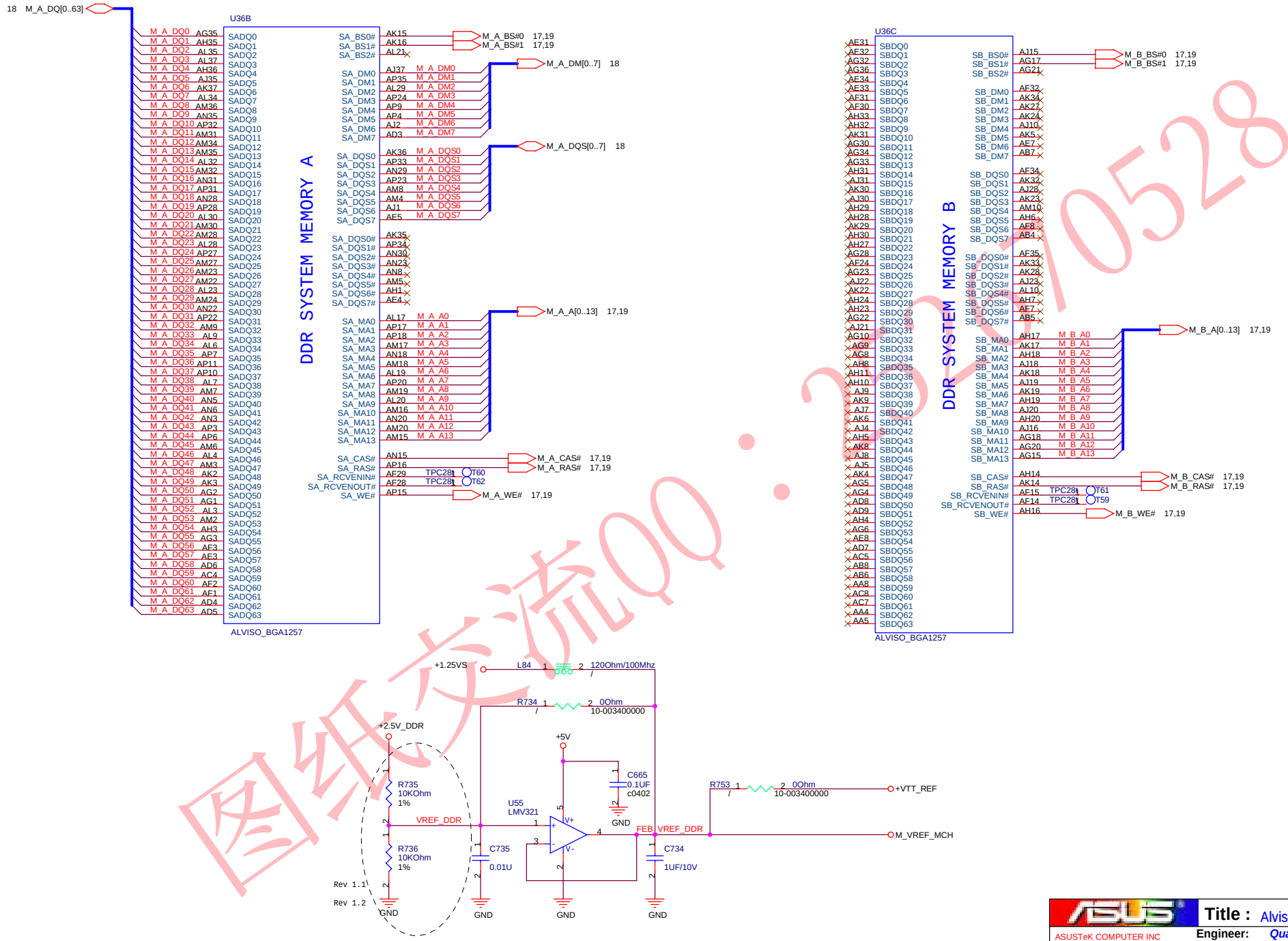
In OrCAD circuit,ALVISO PM P/N :02-010002600
But we have to use ALVISO GM P/N : 02-010002610 in BOM list

图纸交流QQ:2226670528

ASUSTeK COMPUTER INC	Title : Alviso GMCH (1)	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 6 of 51	

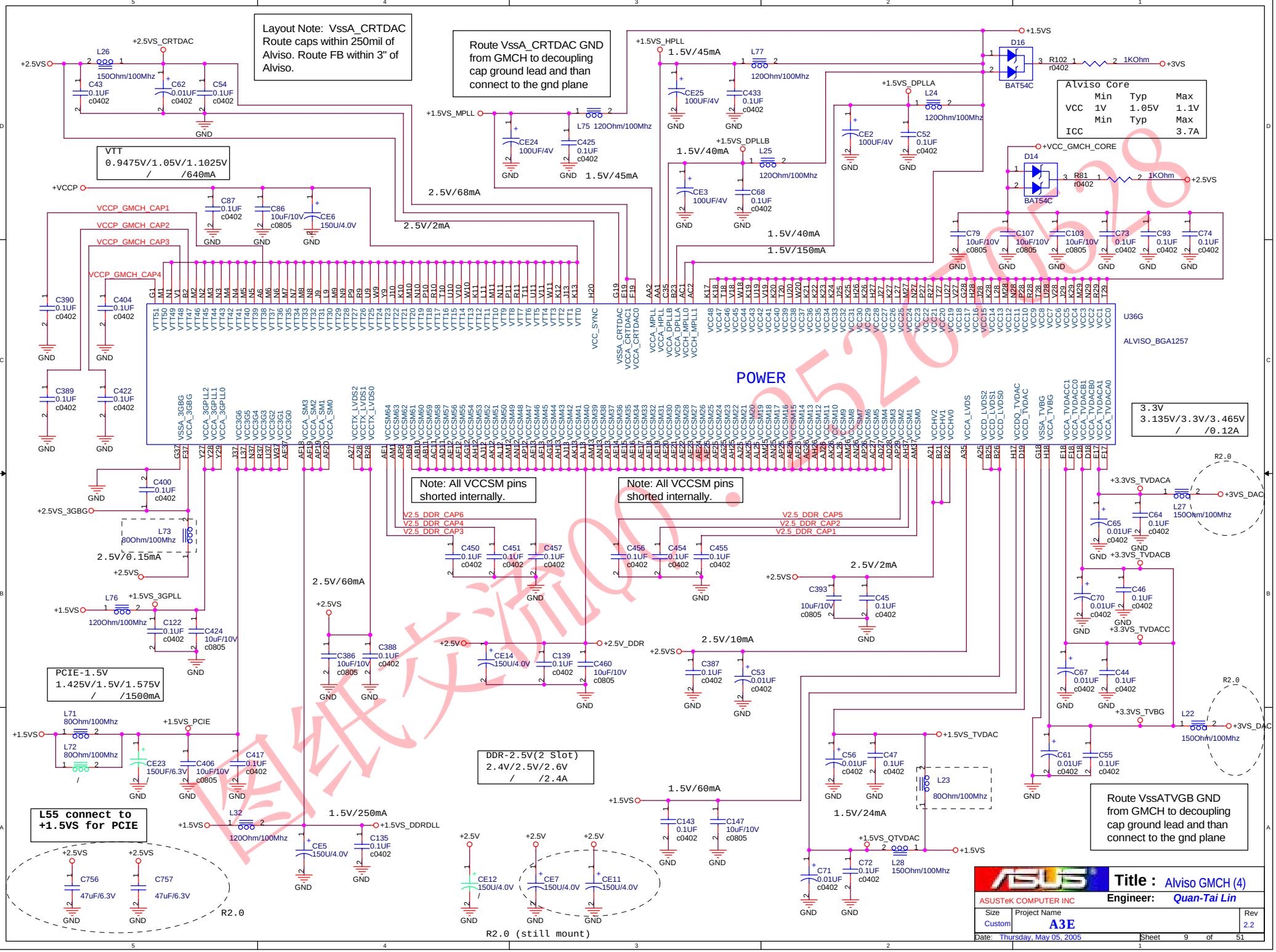


图纸交流QQ:2570528



图纸交流QQ：3227070528

ASUSTeK COMPUTER INC	Title : Alviso GMCH (3)		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 8 of 51		



图纸交流QQ：952676528

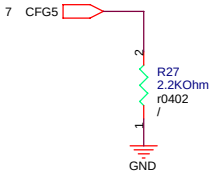
图纸交流QQ：2526706528

ASUSTeK COMPUTER INC	Title : Alviso GMCH (5)		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 10 of 51		

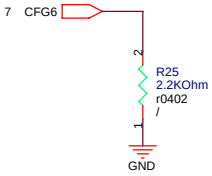
CFG[2:0] are HVCMOS (+2.5VS)
CFG[17..3] have internal pullup resistors. /AGTL+(VCCP)/
CFG[19..18] have internal pulldown resistors./HVCMOS(+2.5VS)/
SDVOCRTL_DATA has internal pulldown resistors.

SDVOCRTL_DATA :
LOW = No SDVO device present (Default)

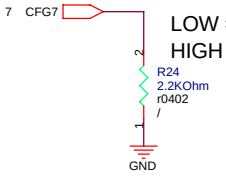
CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)



CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)

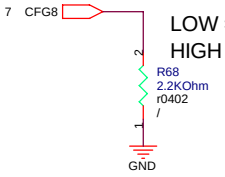


CFG7 : CPU STRAP



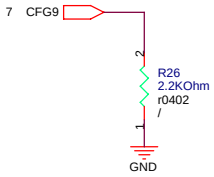
LOW = Mobile Prescott
HIGH = Dothan CPU (Default)

CFG8 : PCI-X POWER Saving

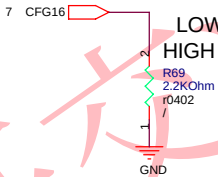


LOW = PCI-X POWER Saving
HIGH (Default)

CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)

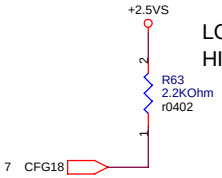


CFG16 : FSB DYNAMIC ODT



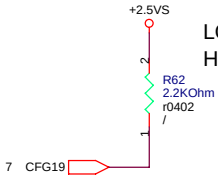
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

CFG18 : VCC SELECT

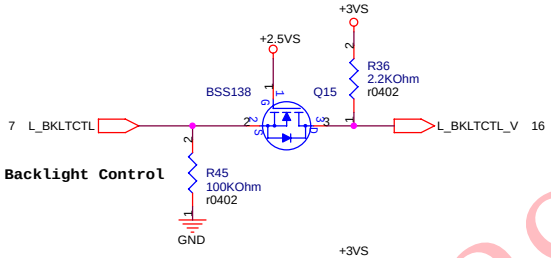


LOW = 1.05V (Default)
HIGH = 1.5V

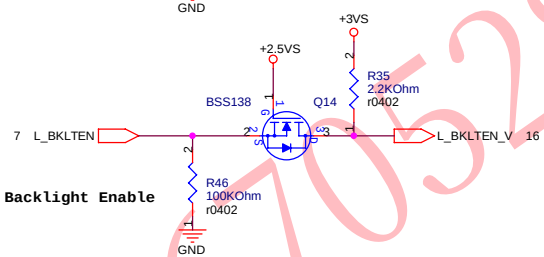
CFG19 : VTT SELECT



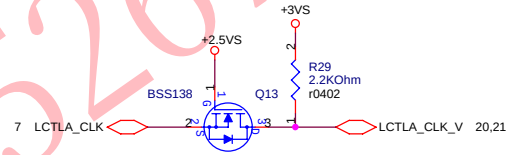
LOW = 1.05V (Default)
HIGH = 1.2V



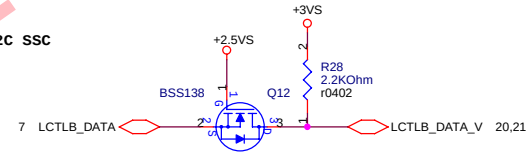
Backlight Control

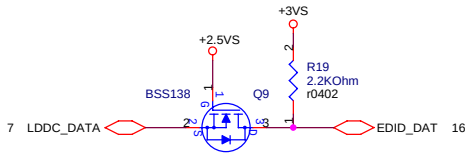


Backlight Enable

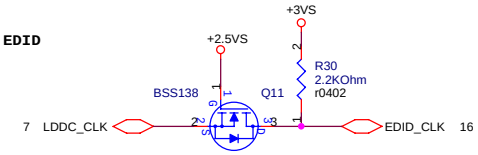


I2C SSC





I2C EDID



图纸交流QQ：2526706528

ASUSTeK COMPUTER INC	Title : GMCH Strapping	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 11 of 51	

ICH6-M from 02-010002500 change to 02-010004402 on bom list

Unused SATA pin
- Connect RX, RBIAS, CLK to GND
- Leave TX, LED# as NC

U20C

32,33 IDE_PDD[0..15]
IDE_PDD15 AD13 DD_15
IDE_PDD14 AG15 DD_14
IDE_PDD13 AE15 DD_13
IDE_PDD12 AC13 DD_12
IDE_PDD11 AB13 DD_11
IDE_PDD10 AB12 DD_10
IDE_PDD9 AF13 DD_9
IDE_PDD8 AE13 DD_8
IDE_PDD7 AB11 DD_7
IDE_PDD6 AD11 DD_6
IDE_PDD5 AC11 DD_5
IDE_PDD4 AE14 DD_4
IDE_PDD3 AD12 DD_3
IDE_PDD2 AF14 DD_2
IDE_PDD1 AE15 DD_1
IDE_PDD0 AD14 DD_0

SATA_0RXN AE3 — R538 0Ohm r0402
SATA_0RXP AD3
SATA_0TXN AG2 — TPC28t T110
SATA_0TXP AF2 — TPC28t T111
SATA_1RXN AC5 — R532 0Ohm r0402
SATA_1RXP AD5
SATA_1TXN AF4 — TPC28t T105
SATA_1TXP AG4 — TPC28t T106
SATA_2RXN AD7 — R529 0Ohm r0402
SATA_2RXP AC7
SATA_2TXN AF6 — TPC28t T104
SATA_2TXP AG6 — TPC28t T103
SATA_3RXN AC9 — R526 0Ohm r0402
SATA_3RXP AD9
SATA_3TXN AF8 — TPC28t T101
SATA_3TXP AG8 — TPC28t T102
GND

SATA_CLKN AC2
SATA_CLKP AC1

32,33 IDE_PDDACK# AB15 DDACK#
32,33 IDE_PDDREQ AB14 DDREQ
32,33 IDE_PDIOR# AE16 DIOR#
32,33 IDE_PDIOW# AC14 DIOW#
32,33 IDE_PIORDY AF16 IORDY
+3VS — R246 4.7KOhm r0402

SATARBIAS# AG11
SATARBIAS AF11

PLACE WITHIN 500mils of ICH6 ball

R256 0Ohm r0402 — GND
R288 0Ohm r0402 — GND

32,33 IDE_PDA0 AC16 DA0
32,33 IDE_PDA1 AB17 DA1
32,33 IDE_PDA2 AC17 DA2

SMBCLK Y4 — SMB_CLK
SMBDATA W5 — SMB_DAT
R281 2.2KOhm — SMB_CLK_S
R282 2.2KOhm — SMB_DAT_S
R275 2.2KOhm
R278 2.2KOhm
+3VSUS +3VS

32,33 IDE_PDCS1# AD16 DCS1#
32,33 IDE_PDCS3# AE17 DCS3#

R243 8.2KOhm r0402 +3VS
32,33 INT_IRQ14 AB16 IDEIRQ

LINKALERT# Y5 — LINKALERT# 13
SMLINK_0 W4 — SM_LINK0 13
SMLINK_1 U6 — SM_LINK1 13

SATALED# AC19 — TPC28t T233
SATA_0GP/GPI26 AE17 — SATA_DET_#0 13 3 H_FERR#
SATA_1GP/GPI29 AE18 — PCB_ID0 13
SATA_2GP/GPI30 AE18 — PCB_ID1 13
SATA_3GP/GPI31 AG18 — PCB_ID2 13
INTRUDER# AA3 — +VCC_RTC
R541 1M r0402
R2.0

RSMRST# Y3 — PM_RSMRST# 36

RTCX1 Y1 — RTC_X1 — C308 12PF/50V c0402
RTCX2 Y2 — RTC_X2 — R303 10MOhm
X3 SIDE 32.768KHZ +/-20ppm/12.5PF
RTCRST# AA2 — RTC_RST# — C313 12PF/50V c0402
GND

INTVRMEN AA5 — 33KOhm R543 — +VCC_RTC
TPC28t T309
JRST1 1 2 GND Rev 1.1
SPKR F8 — SB_SPKR 23
INTERNAL PULL-DOWN
PULL-UP : NO REBOOT

R544 180KOhm +VCC_RTC
C537 0.1UF c0402 GND

ICH6_M

+5VS
5,17,20 SMB_CLK_S — Q64 2N7002 — SMB_CLK
+5VS
5,17,20 SMB_DAT_S — Q72 2N7002 — SMB_DAT

Battery(RTC) P/N:07-016202032

+3VSUS — R300 8.2KOhm r0402 — CB_SD#

U20D

+3VS — R701 8.2KOhm r0402 — P4 LDRQ_1#/GPIO41

21,22,26 LPC_AD0 P2 LAD_0/FWH0
21,22,26 LPC_AD1 N3 LAD_1/FWH1
21,22,26 LPC_AD2 N5 LAD_2/FWH2
21,22,26 LPC_AD3 N4 LAD_3/FWH3
13,22 LPC_DRQ#0 N6 LDRQ_0#
21,22,26 LPC_FRAME# P3 LFRAME#/FWH4

23,28 ACZ_BCLK — R268 33Ohm — C10 ACZ_BIT_CLK
23,24,28 ACZ_RST# — R262 0Ohm — A10 ACZ_RST#
23 ACZ_SDIN0 — F11 ACZ_SDIN_0
28 ACZ_SDIN1 — F10 ACZ_SDIN_1
ACZ_SDIN_2
T99 TPC28t B10
23,28 ACZ_SDOUT — R273 47Ohm 1% — C9 ACZ_SDOUT
+3VS R270 1KOhm r0402 — B9 ACZ_SYNC
23,28 ACZ_SYNC — R271 33Ohm — E10 CLK14
20 CLK_ICH14

T237 TPC28t — D12 EE_CS
F13 EE_DIN
D11 EE_DOUT
B12 EE_SHCLK
INTERNAL PULL-UP
PULL-DOWN : RESERVED
R523 1KOhm r0402 GND

F12 LAN_CLK
B11 LAN_RSTSYNC
E12 LAN_RXD_0
E11 LAN_RXD_1
C13 LAN_RXD_2
C12 LAN_TXD_0
C11 LAN_TXD_1
E13 LAN_TXD_2

H_CPUSLP# R193 : B STEP NO STUFF
H_DPRSTP# R231 : A STEP NO STUFF

21 A20GATE — AF22 A20GATE
3 H_A20M# — AF23 A20M#
3,6 H_CPUSLP# — R193 0Ohm — AE27 CPUSLP#
13,38 PM_DPRSLPVR — AE20 DPRSLPVR/TP_1
3 H_DPRSTP# — R192 0Ohm — AE24 DPRSLP#/TP_2
3 H_DPSLP# — AD27 DPSTP#
3 H_IGNNE# — AG26 IGNNE#
22 FWH_INIT# — AE22 INIT3_3V#
3 H_INIT# — AE27 INIT#
3 H_INTR — AG24 INTR
+VCCP 56Ohm R197 r0402 — H_FERR# — R196 56Ohm r0402 — AE24 FERR#
3 H_NMI — AF25 NMI
21 RCIN# — AD23 RCIN#
13,21,22,26,29 INT_SERIRQ — AB20 SERIRQ
3 H_SMI# — AG27 SMI#
3 H_STPCLK# — AE26 STPCLK#
3,7,36 PM_THRMTRIP# — R194 56Ohm r0402 — AE23 THRMTRIP#
R190 75Ohm r0402 +VCCP

BMBUSY#/GPI6 AD19 — R227 8.2KOhm r0402 — PM_BMBUSY# 7
GPI7 AE19 — +3VS
GPI8 R1 — EXTSMI# 21
SMBALERT#/GPIO11 W6 — R542 10KOhm r0402 — +3VSUS
GPI12 M2 — KB_SCI# 13,21
GPI13 R6 — SIO_SMI# 13,22
STP_PCI#/GPO18 AC21 — STP_PCI# 13,20
GPIO19 AB21 — PWRLED_1HZ 13
STP_CPU#/GPO20 AD22 — STP_CPU# 13,20,38
GPIO21 AD20 — T308 TPC28t
GPIO23 AD21 — FWH_WP# 22
GPIO24 V3 — 802_LED_EN# 13,35
GPIO25 P5 — CB_SD# — CB_SD# 29
GPIO27 R3 — OP_SD# 24
GPIO28 T3 — TPC28t T241
CLKRUN#/GPIO32 AE19 — PM_CLKRUN# 13,21,26,27,29
GPIO33 AF20 — CPUFAN_SPD_A 5
GPIO34 AC18 — WLAN_ON# 16,26
CPUPWRGD/GPIO49 AG25 — H_PWRGD — H_PWRGD 3

MCH_SYNC# AG21 — MCH_SYNC# 13
PWRBTN# U1 — PM_PWRBTN# 36
RI# T2 — RING# — RING# 13

SLP_S3# T4 — R549 100Ohm r0402 — SUSB# 16,22,27,29,35,36,37,42,45
SLP_S4# T5 — R536 100Ohm r0402 — SUSC# 34,35,36,45
SLP_S5# T6 — TPC28t T236

SUS_STAT#/LPCPD# W3 — SUS_STAT# 13
TPC28t T238
SUSCLK V6 — SUSCLK
SYS_RESET# U2 — R297 10KOhm r0402 — R293 0Ohm r0402 — ICH6_PWROK — +3VSUS
LAN_RST# V5 — LAN_RST#
BATLOW# V2 — PM_BATLOW# 13
TP_3 U3 — R296 10KOhm r0402 — GND
TP_3 INTERNAL PULL-UP
PULL-DOWN : PCI
Express Port chain test

R307 0Ohm r0402 — DELAY_VR_PWRGD 7,37,38,42
VRMPWRGD AF21 — R295 0Ohm r0402 — ICH6_PWROK — T66 TPC28t
THRM# AC20 — PM_THERM# 5,13
LAN_RST# R548 0Ohm r0402
R547 10KOhm r0402 — PLT_RST# 7,13,21,22,32 — GND

WAKE# U5 — R534 1KOhm r0402 — +3VSUS
PWROK AA1 — ICH6_PWROK — ICH6_PWROK 7,37
R306 10KOhm r0402 GND

ICH6_M

+RTCBAT +3VA DELAY 18~25ms +VCC_RTC
T310 TPC28t
R545 1KOhm r0402 — D56 — RB715F — C543 1UF/10V
T311 TPC28t
BAT1 BATT_HOLDER_2P GND

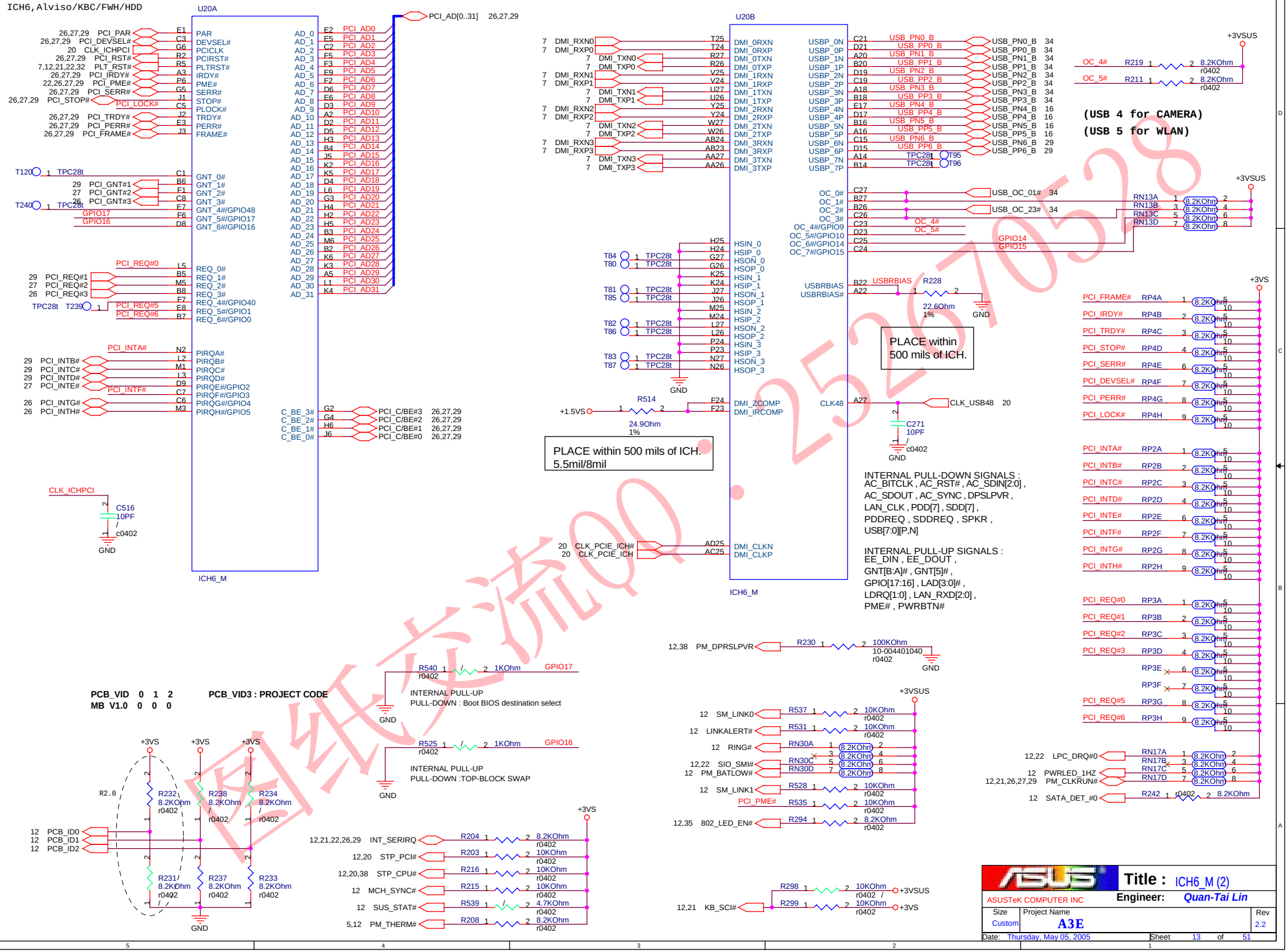
PM_BATLOW# — D36 1N4148W-A2 — BAT_LLOW#_OC 21,42

* 56 within 1" from the ICH6-M pins
* 75 W pull-up to VCCP within 2" from the series resistor

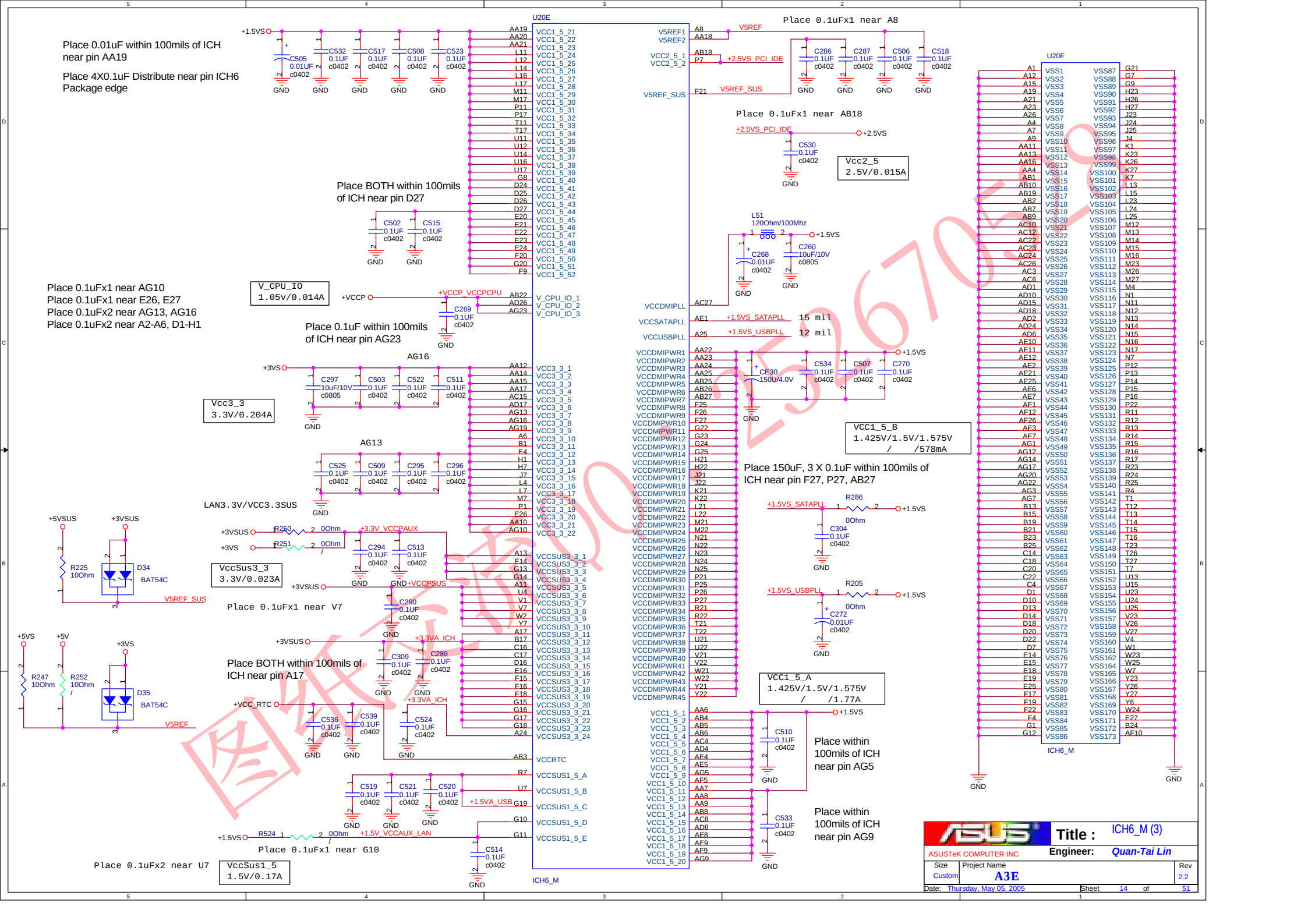
ASUSTeK COMPUTER INC
Title : ICH6_M (1)
Engineer: Quan-Tai Lin
Size Custom | Project Name A3E | Rev 2.2
Date: Thursday, May 05, 2005 | Sheet 12 of 51

图纸交流QQ: 2526705202

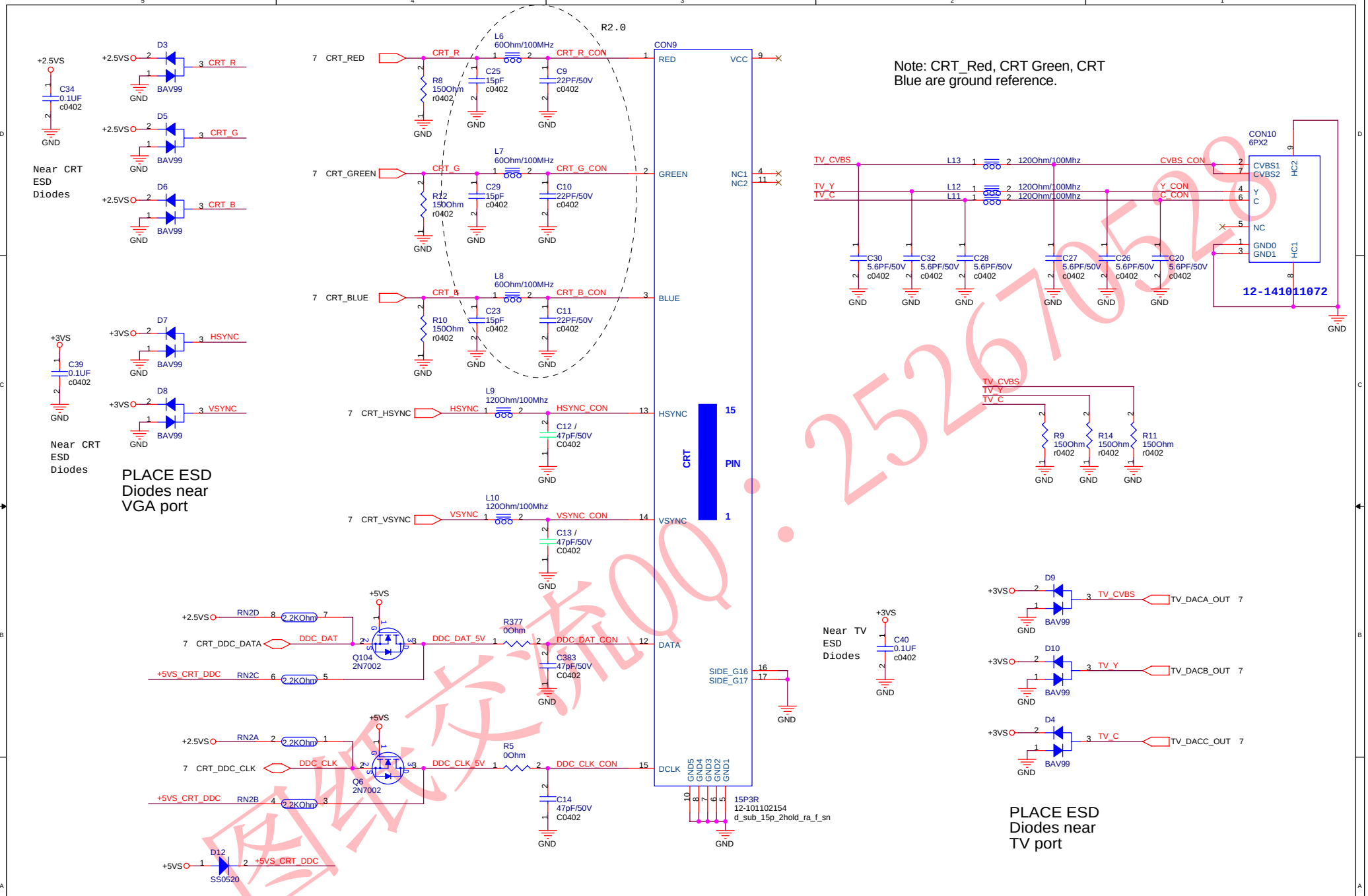
PLT_RST#
ICH6,Alviso/KBC/FWH/HDD



图纸交流QQ：2526705 28



图纸交流QQ:2526705128



图纸交流QQ：2526705 28

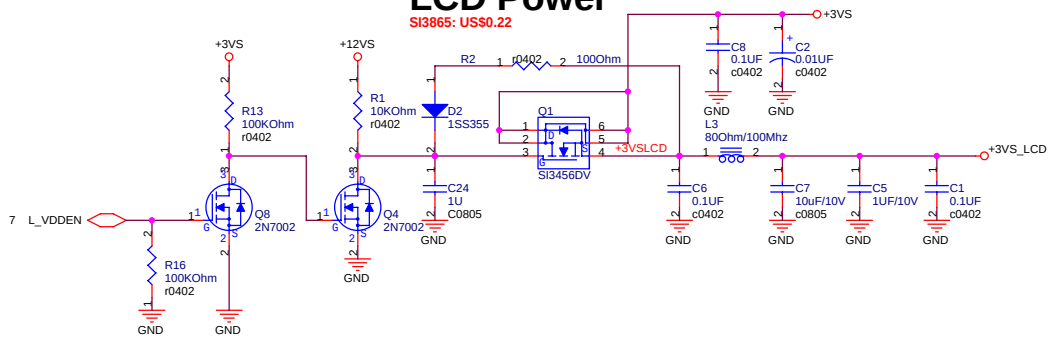
ASUSTeK COMPUTER INC	Title : CRT & TV OUT	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 15 of 51	

LCD Backlight Control

LCD Power

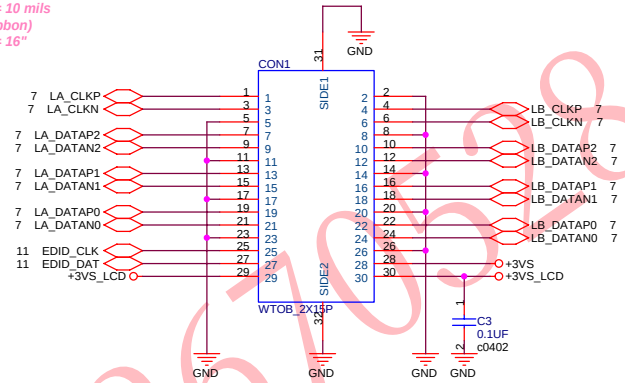
SI3865: US$0.22

3V-3.6V
Full Active: 410 mA(Max. 500 mA)
3-3.6V
S0-S1M:410 mA(500 mA Max.)



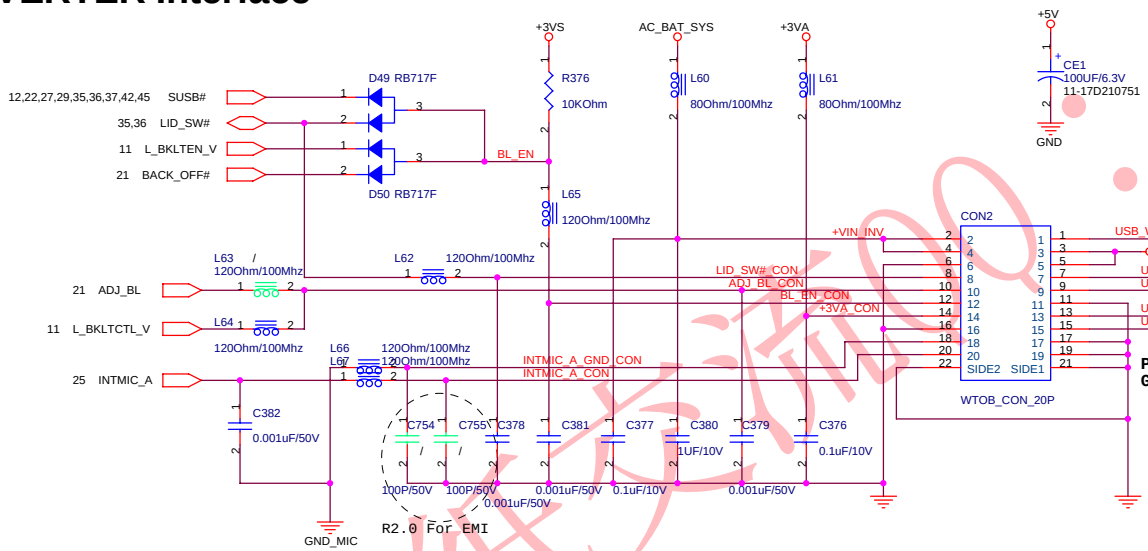
LCD LVDS Interface

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

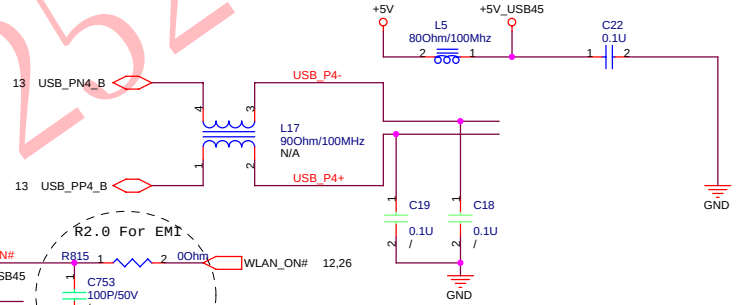


CON1 P/N on BOM List : 12-17001030A

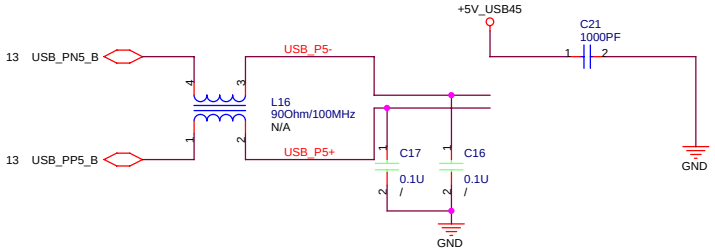
INVERTER Interface



Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.



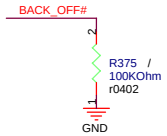
USB PORT 4 for CAMERA



USB PORT 5 for WLAN

BIOS
ADJ_BL: KBC output D/A signal (adjust voltage level) to adjust Back light.

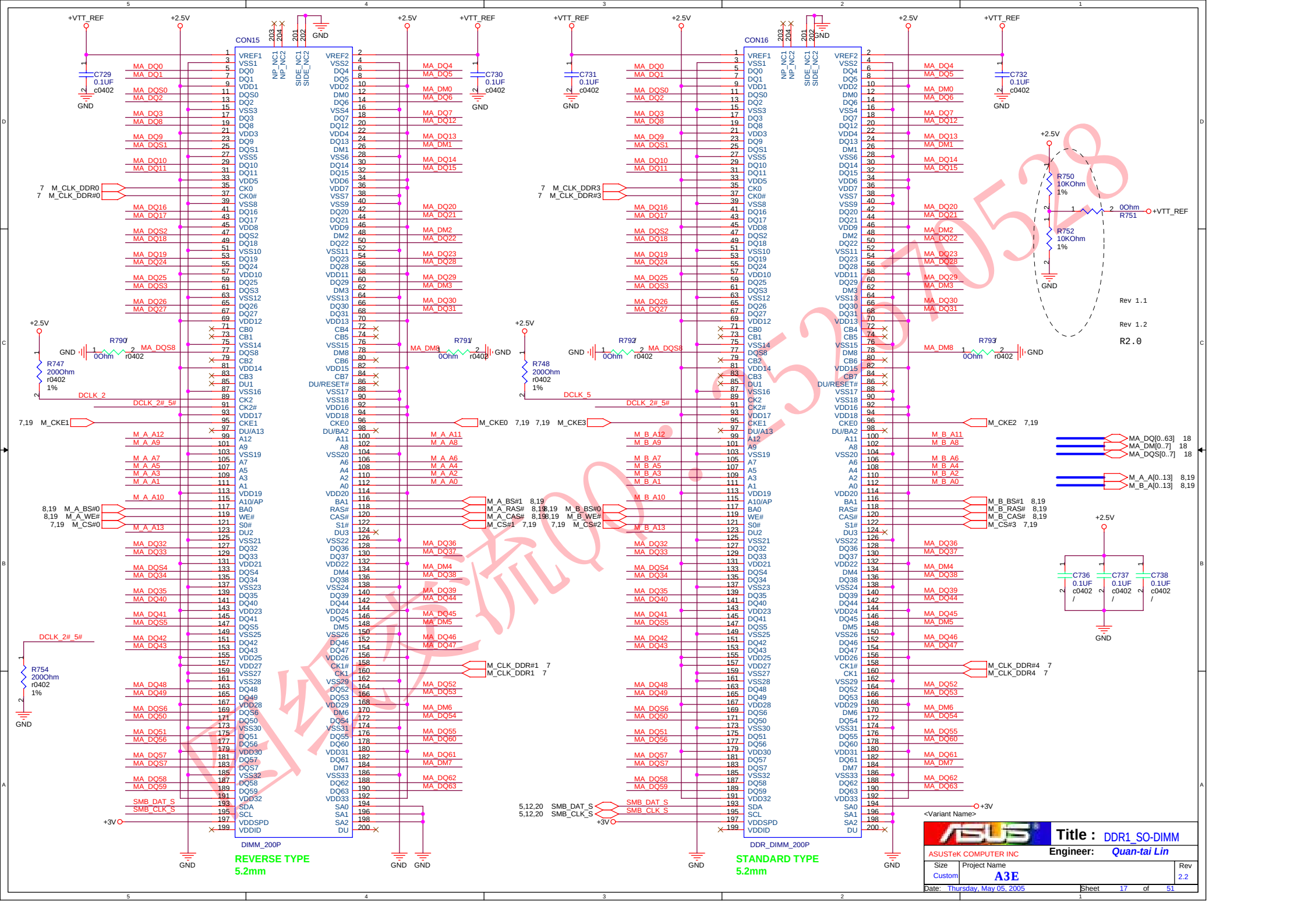
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



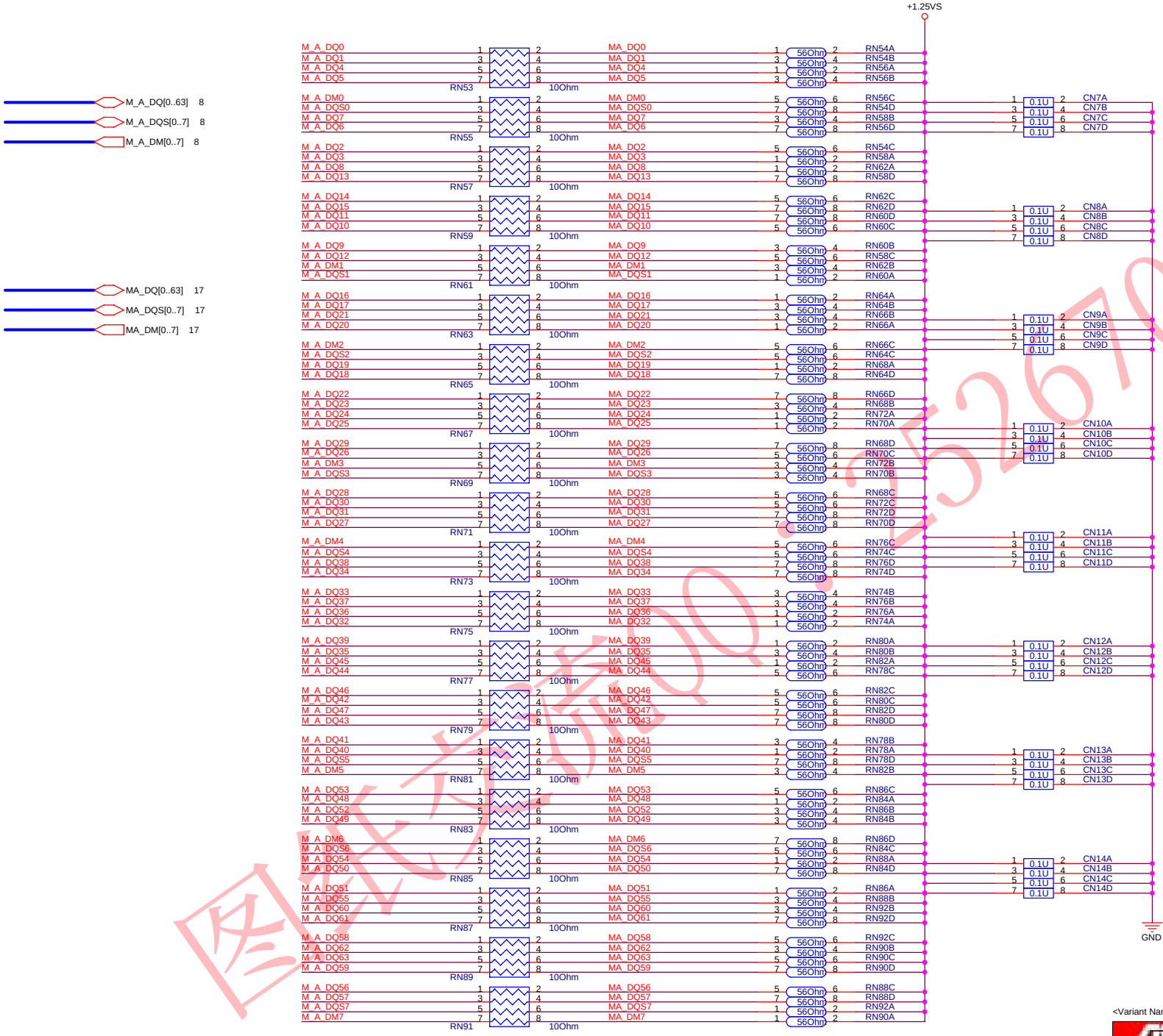
700Vrms@5 mArms
(Min. 3 mArms)6 mArms(Max. 6.5 mArms)

ASUS	Title : LVDS & INVERTER	
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 16 of 51	

图纸交流QQ：2526706528



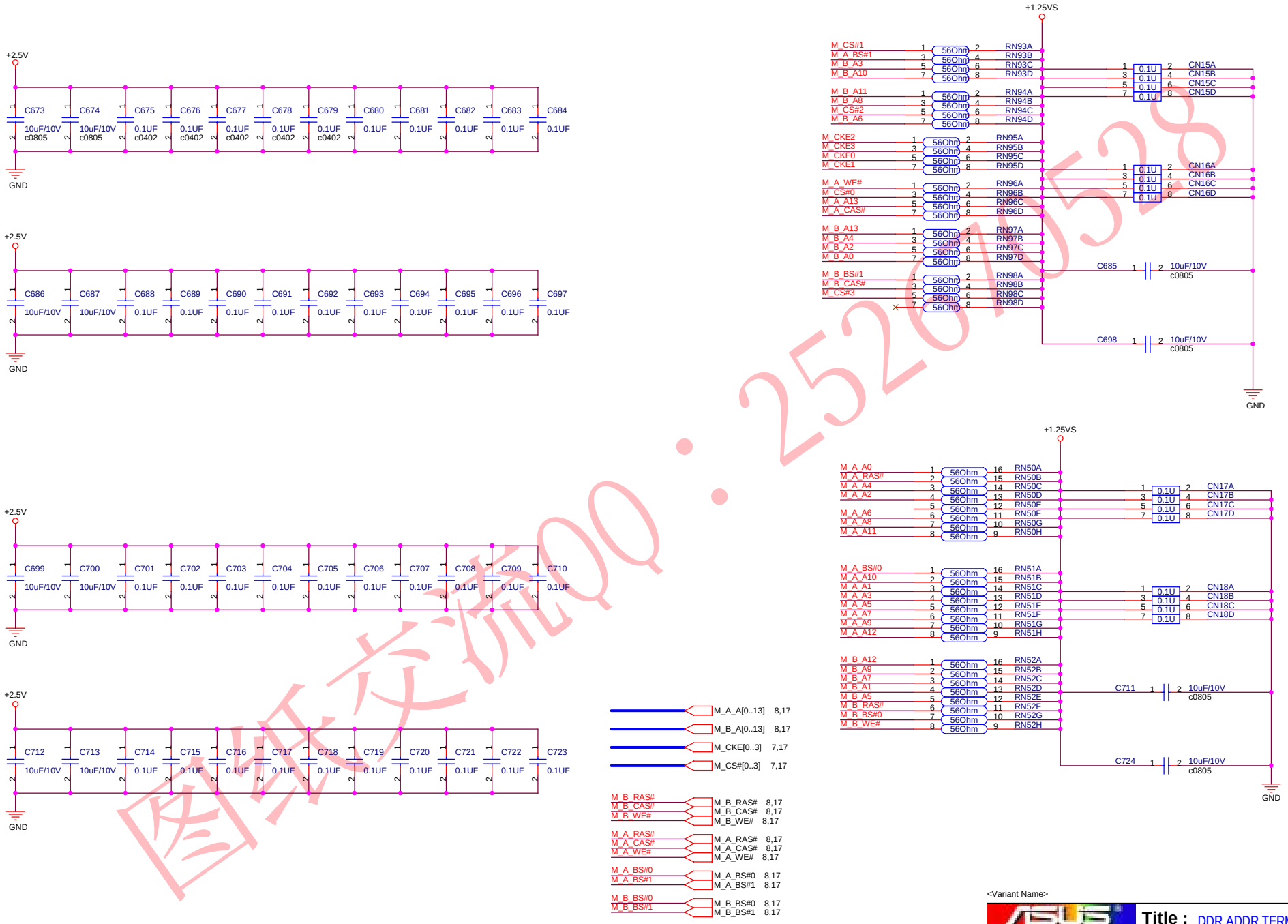
图纸交流QQ：2527052528



图片来源QQ:2526670528

<Variant Name>

ASUSTeK COMPUTER INC	Title: DDR DATA TERMINATION		
	Engineer: Quan-tai Lin		
Size: Custom	Project Name: A3E		Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 18 of 51		

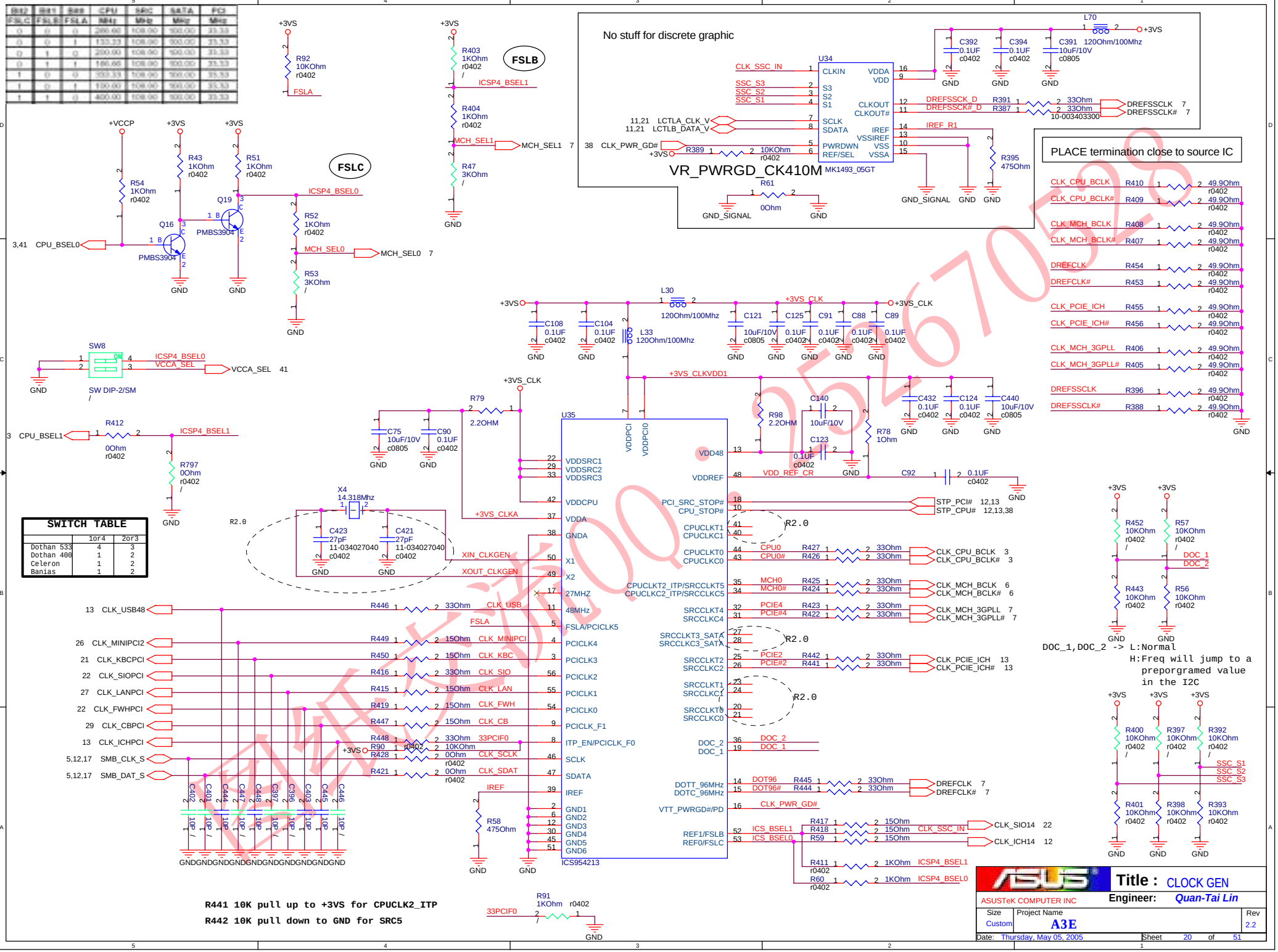


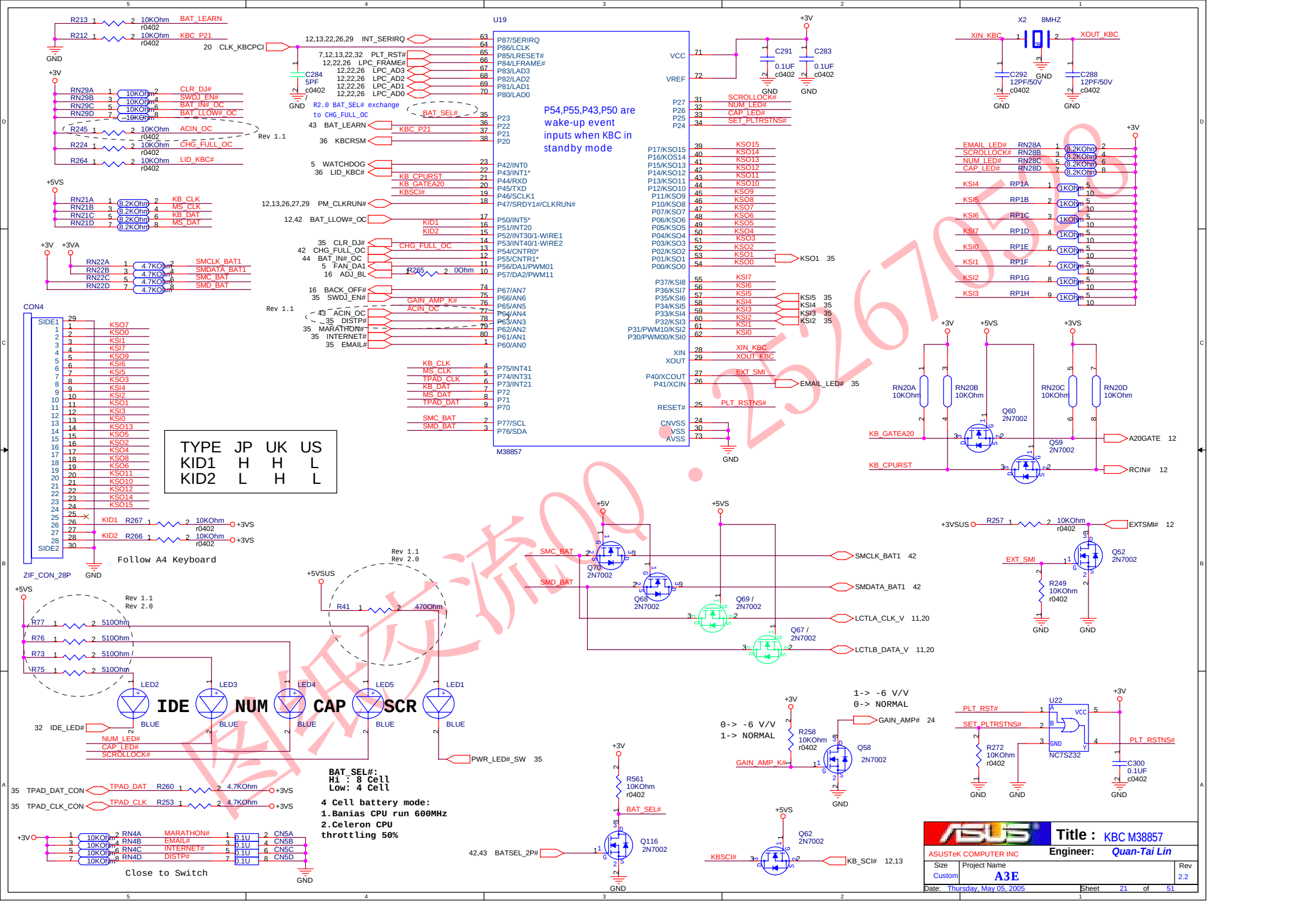
图纸交流QQ：2526705 28

<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR ADDR TERM		
	Engineer: Quan-tai Lin		
Size: Custom	Project Name: A3E		Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 19 of 51		

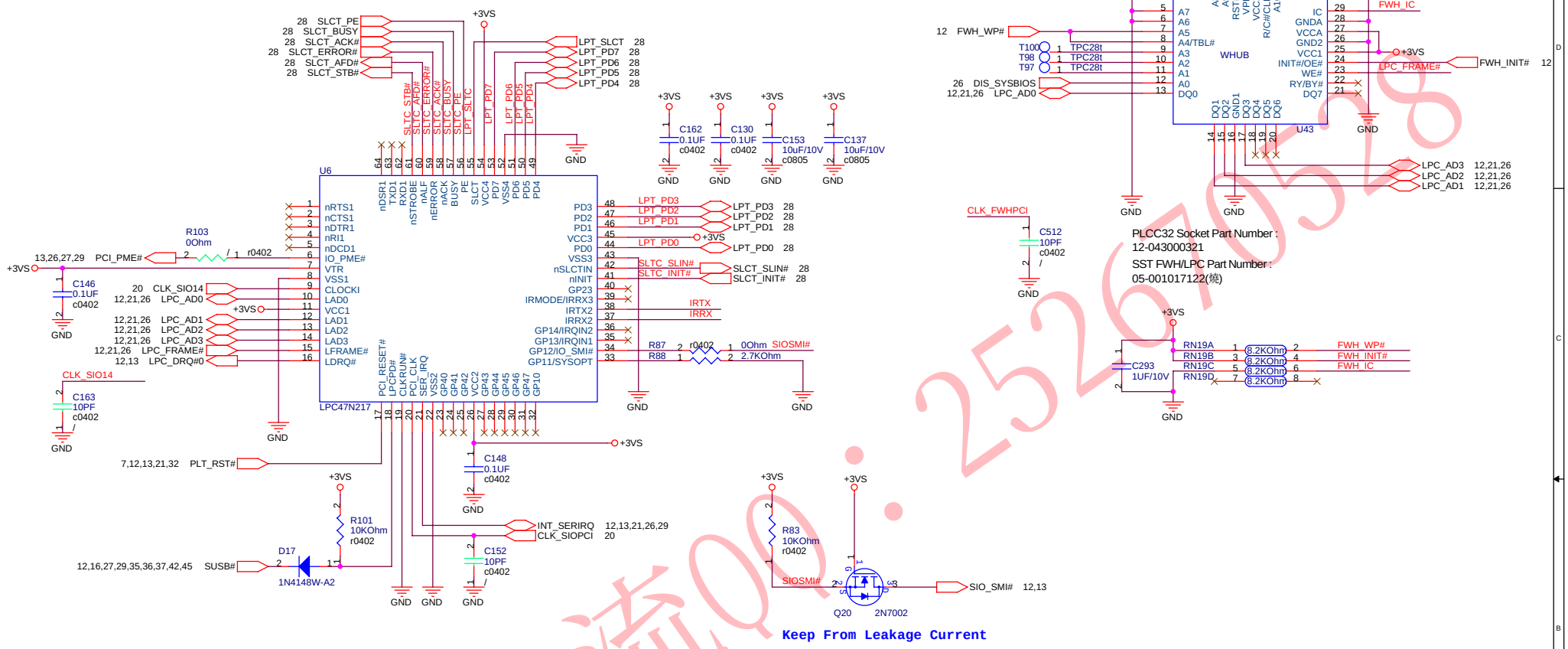
Bit2	Bit1	Bit0	CPU	SRC	SATA	PCI
FSLC	FSLB	FSLA	MHz	MHz	MHz	MHz
0	0	0	266.66	108.00	100.00	33.33
0	0	1	133.33	108.00	100.00	33.33
0	1	0	200.00	108.00	100.00	33.33
0	1	1	166.66	108.00	100.00	33.33
1	0	0	333.33	108.00	100.00	33.33
1	0	1	100.00	108.00	100.00	33.33
1	1	0	400.00	108.00	100.00	33.33

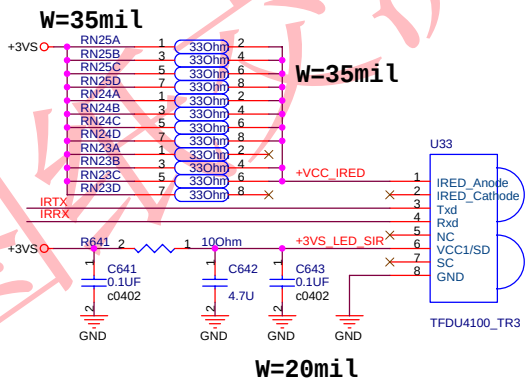




图纸交流QQ：2526705

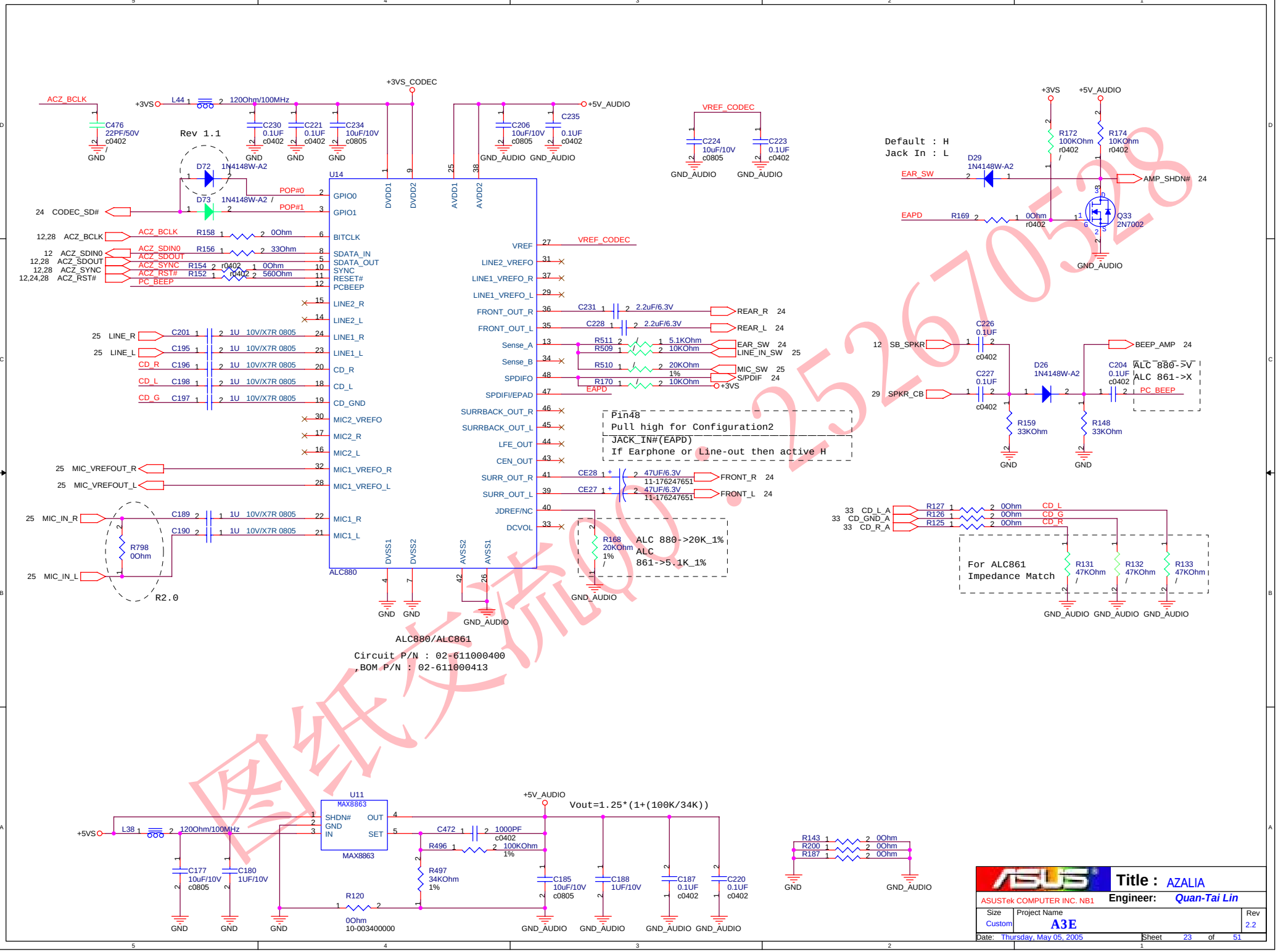
Super I/O



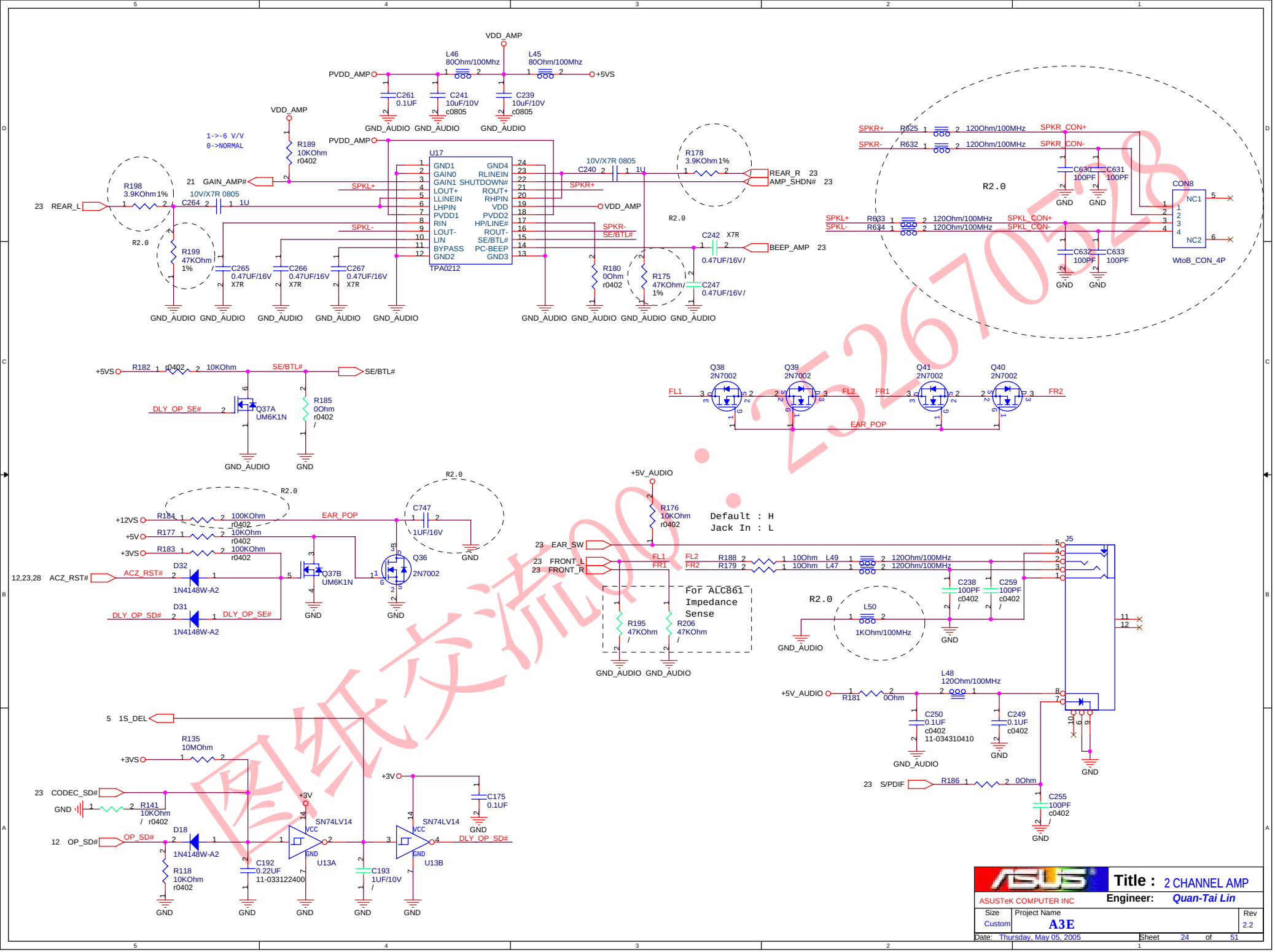


图纸交流QQ：2526705 28

ASUSTeK COMPUTER INC	Title : FWH / SIO / SIR		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 22 of 51		

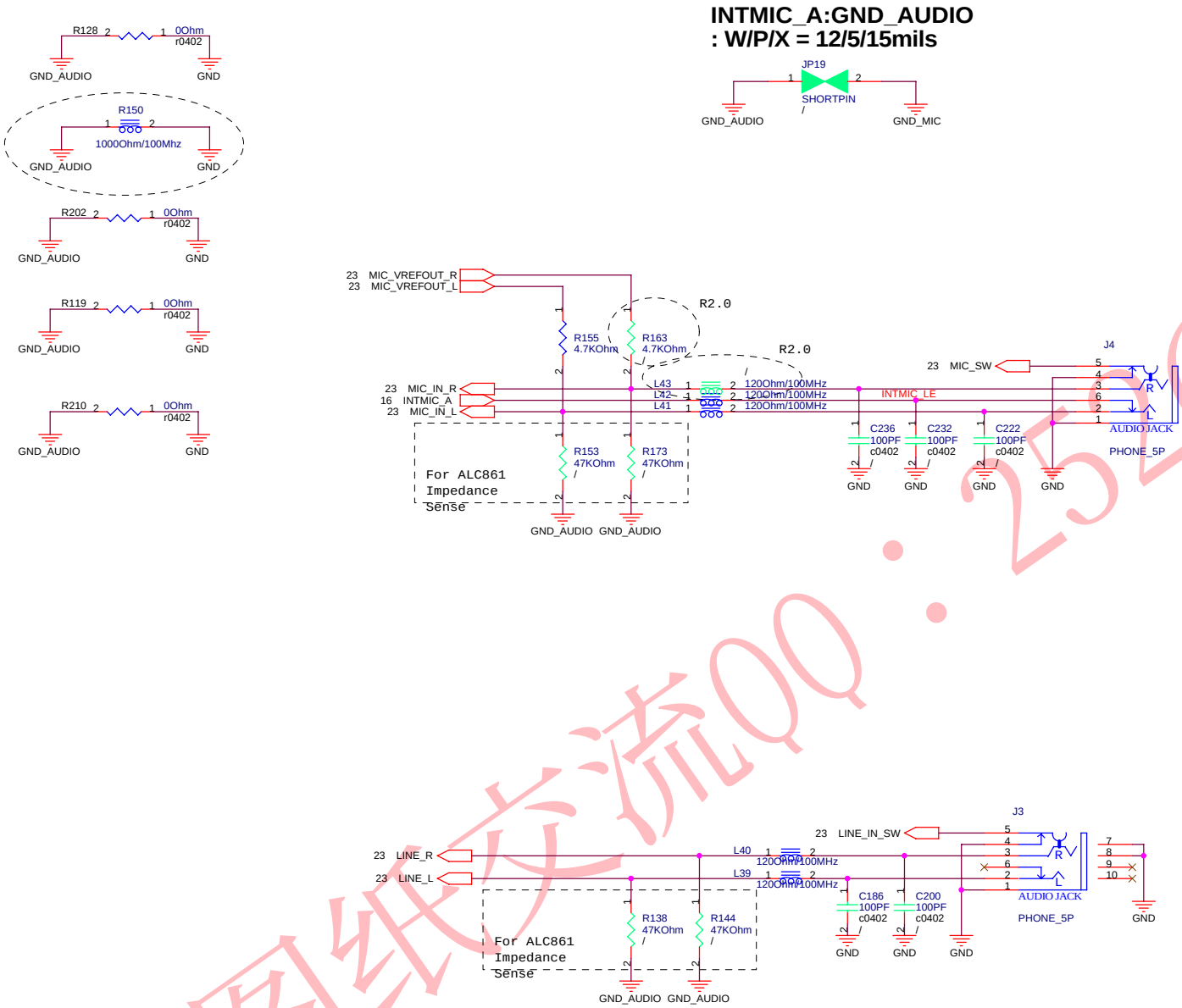


图纸交流QQ:2526706528



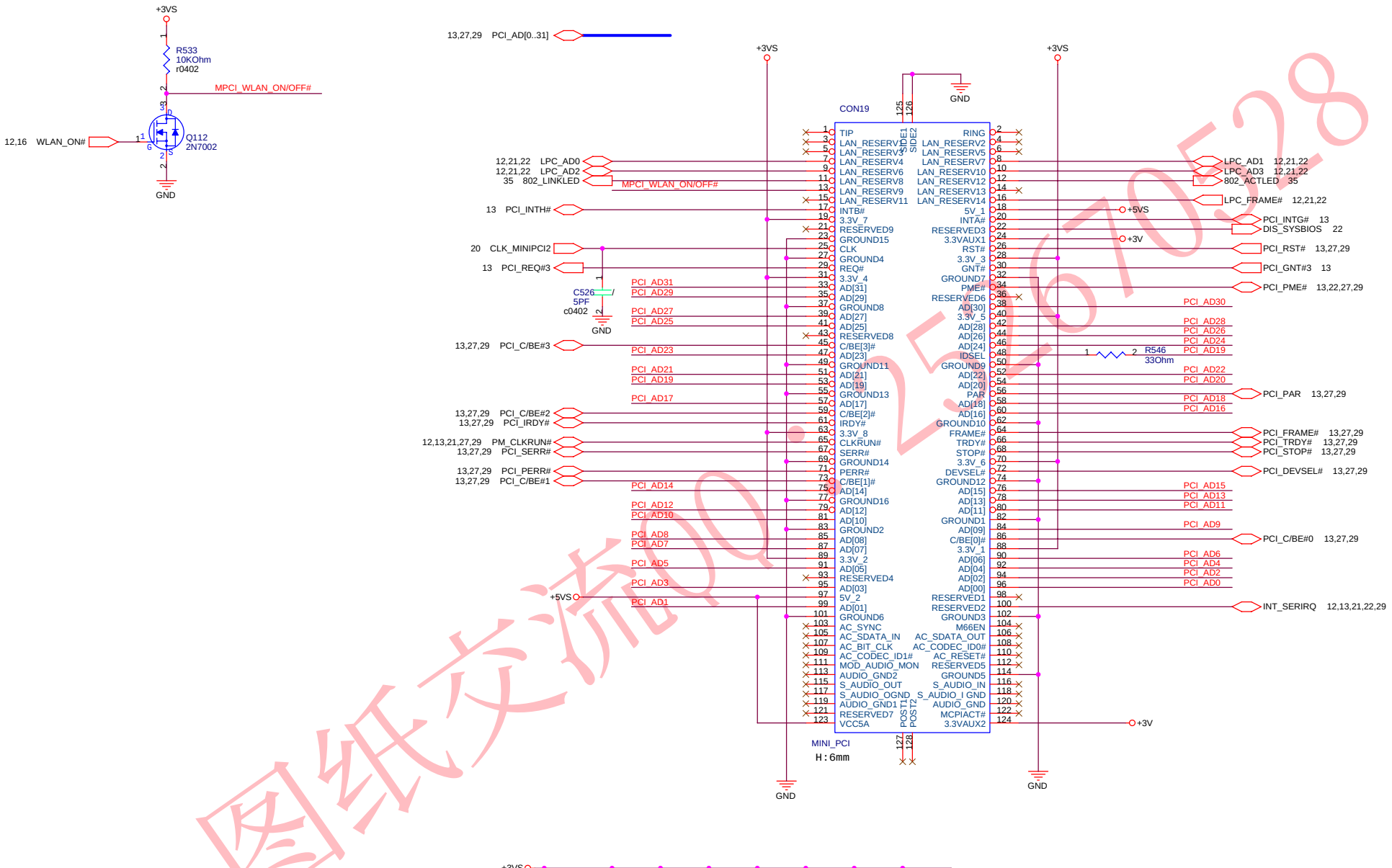
图纸交流QQ：2526705 28

ASUSTeK COMPUTER INC	Title : 2 CHANNEL AMP	Engineer: Quan-Tai Lin
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 24 of 51	



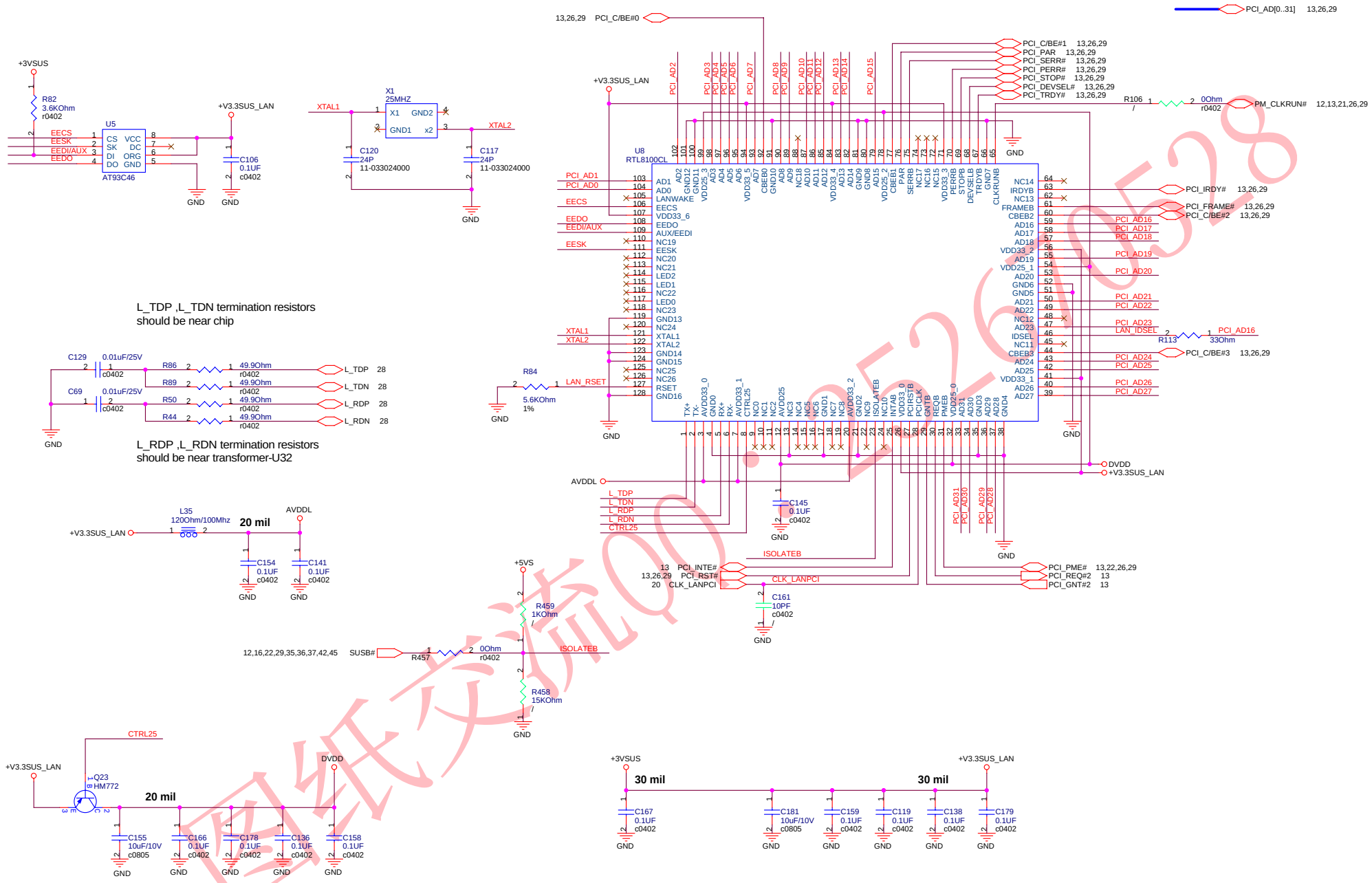
图纸交流QQ：2526670528

ASUSTeK COMPUTER INC	Title : MIC / Line-IN Jack	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 25 of 51	



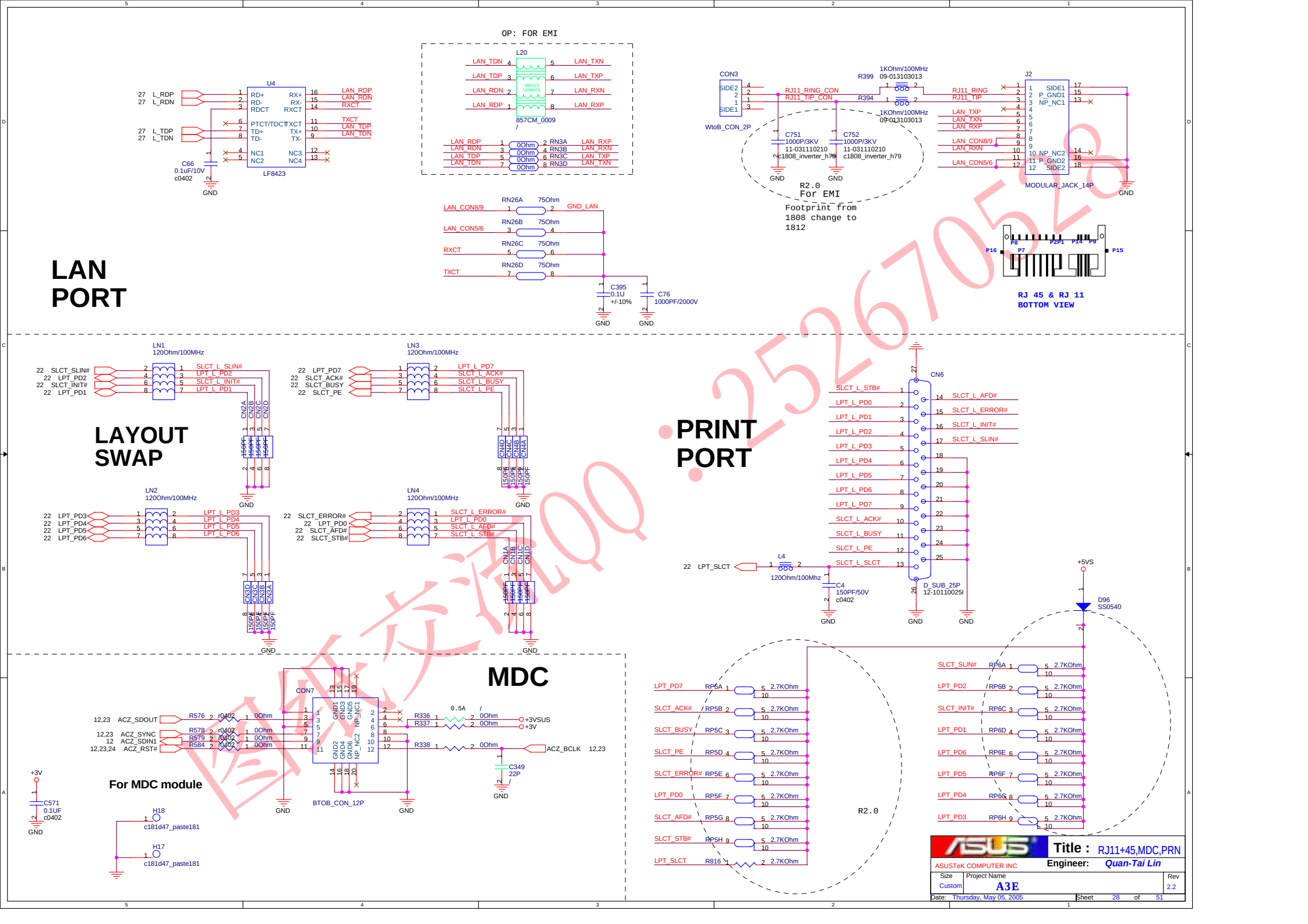
图纸交流QQ:2526706528

ASUSTeK COMPUTER INC	Title : MINIPCI (802.11)	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 26 of 51	

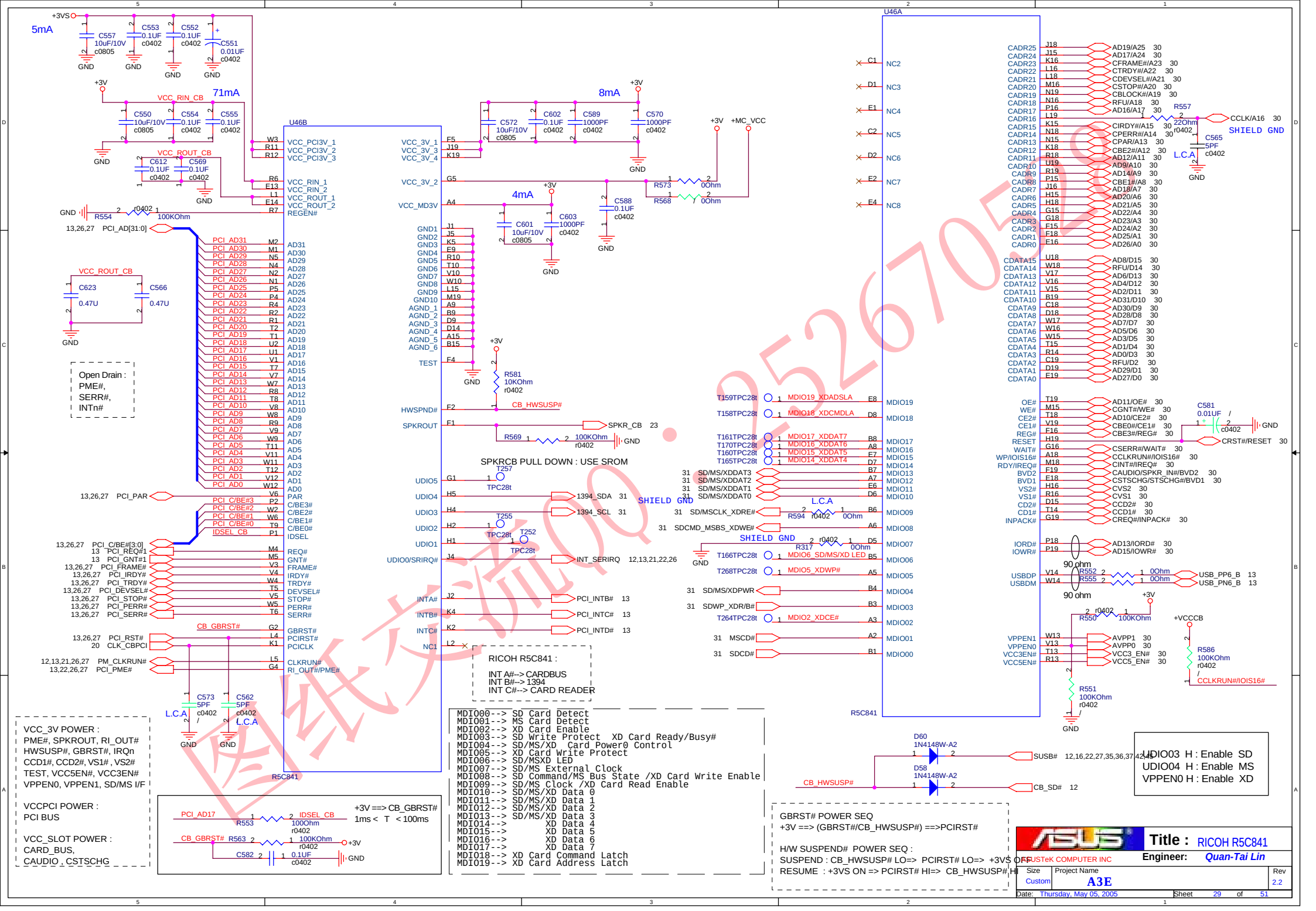


图纸交流QQ:2526705528

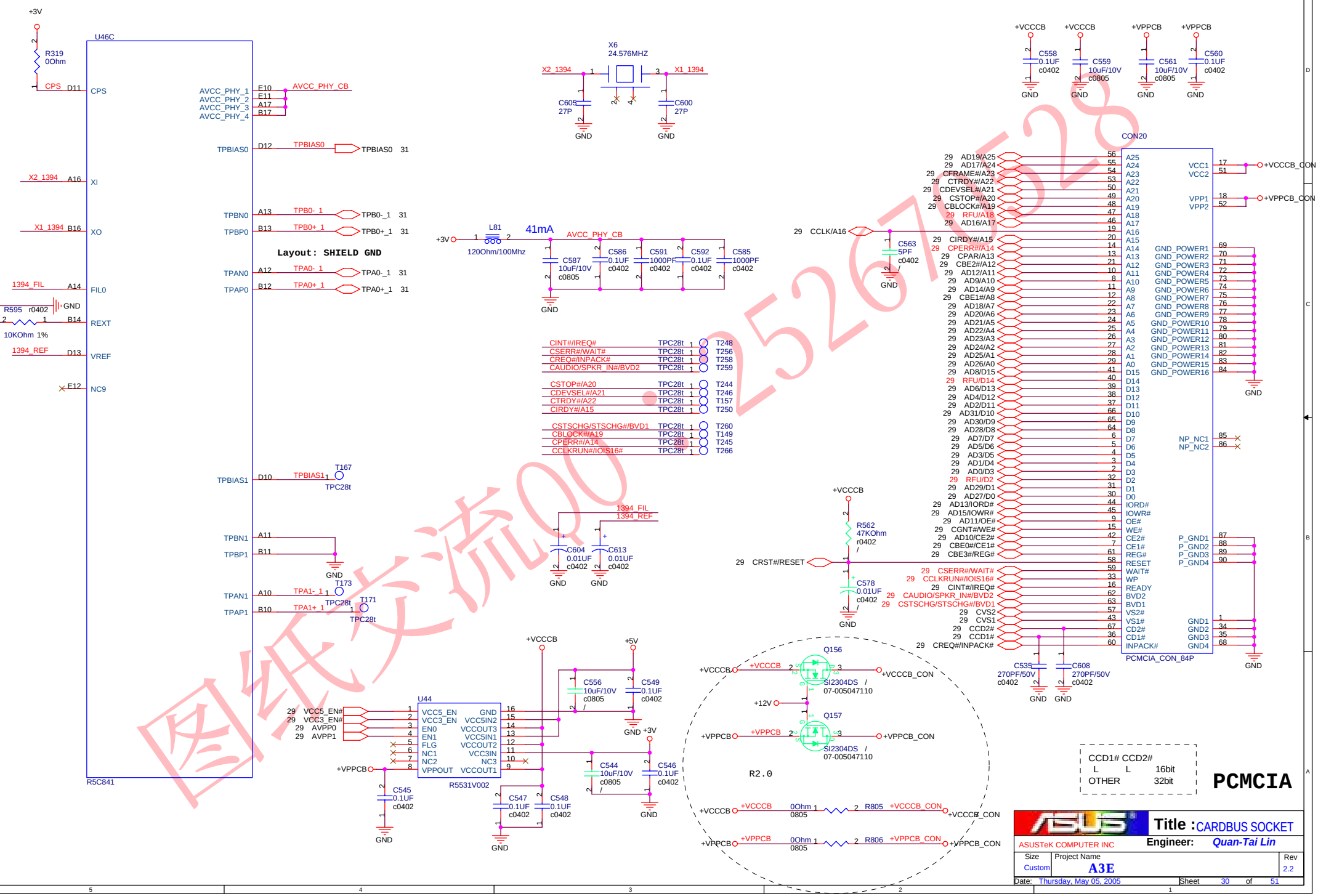
ASUS	Title : 10/100 LAN RTL8100CL		
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 27 of 51		



图纸交流QQ：2526705028



图纸交流QQ：2526705



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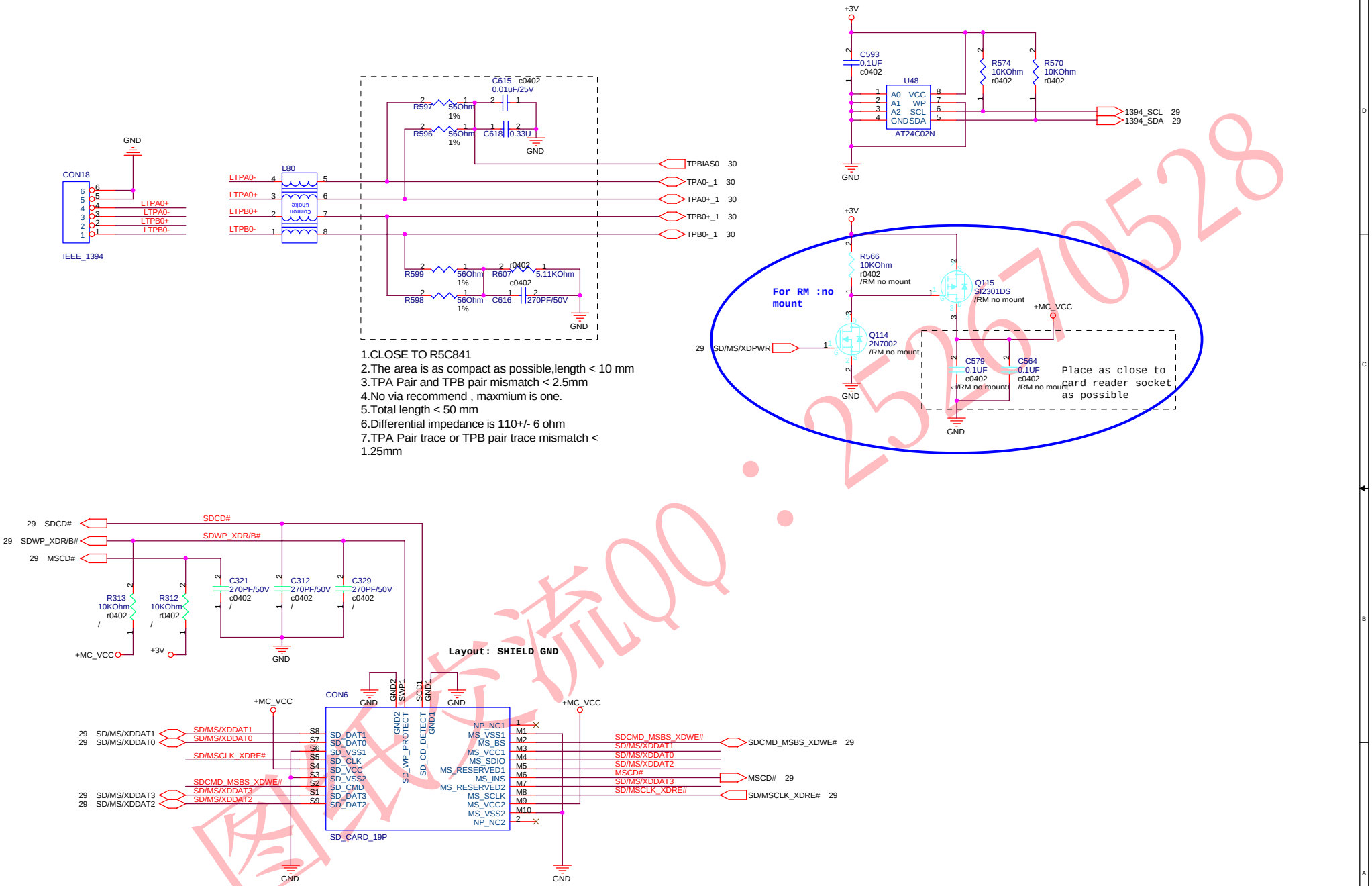
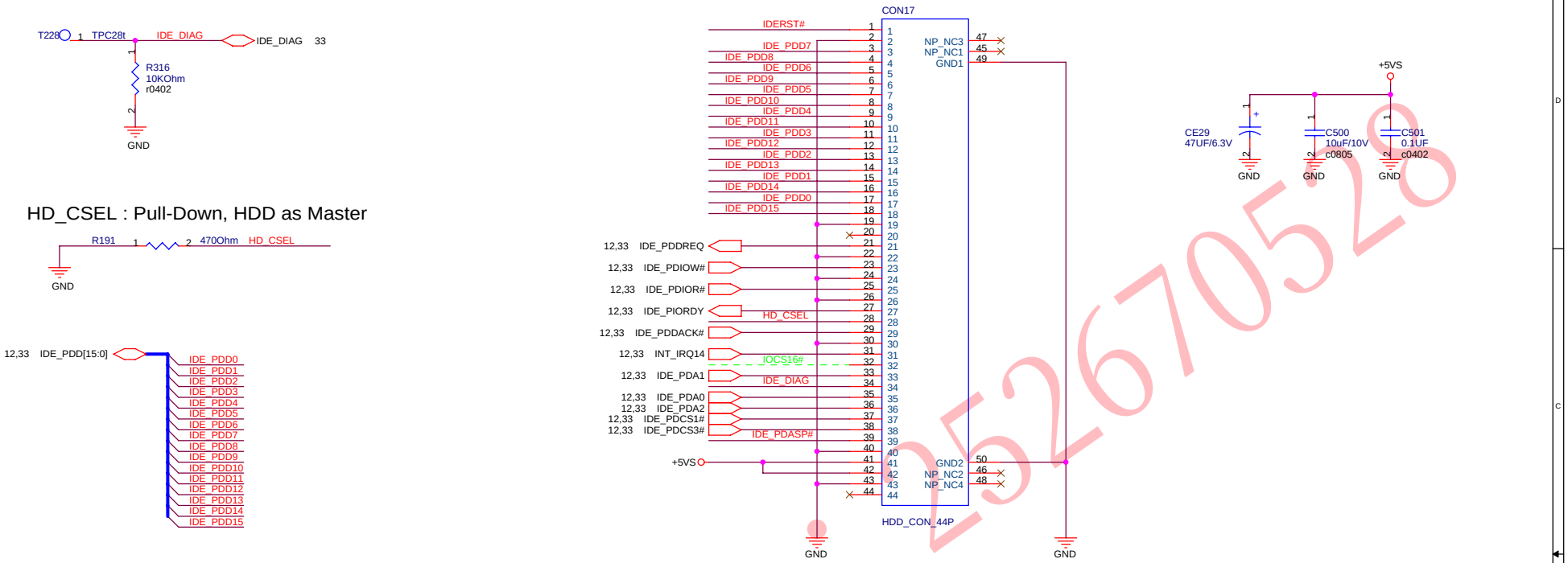
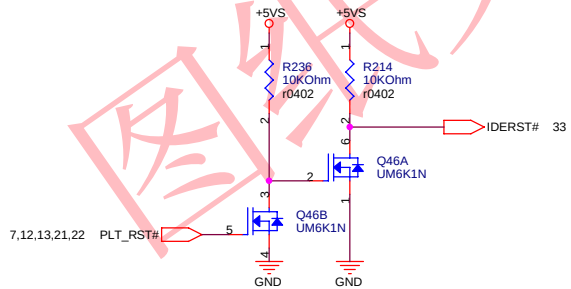


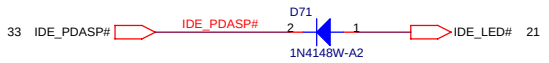
1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm

图纸交流QQ：2526706528

ASUSTeK COMPUTER INC	Title : 1394 & 3 IN 1 CON	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 31 of 51	

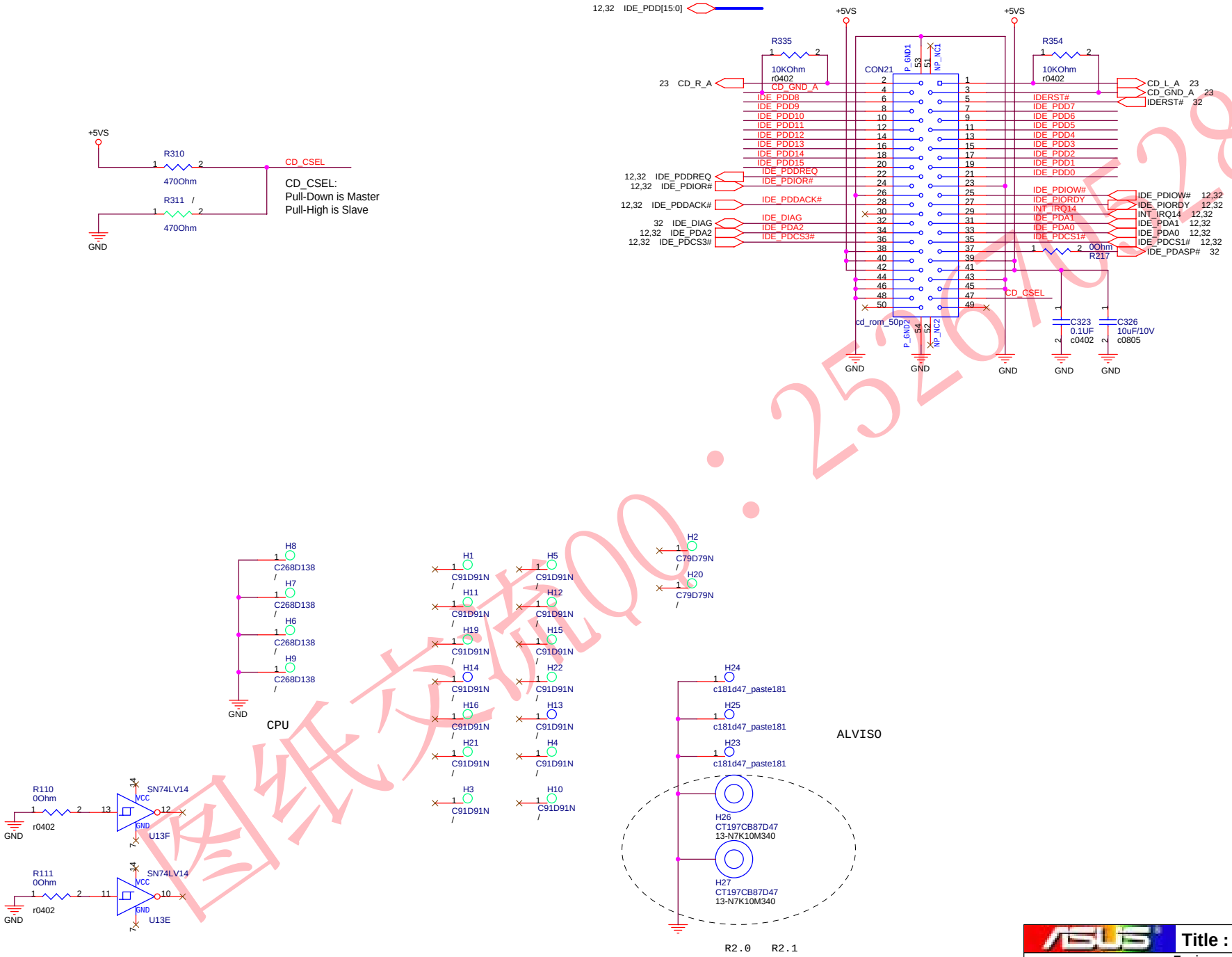






图纸交流QQ：2526705 28

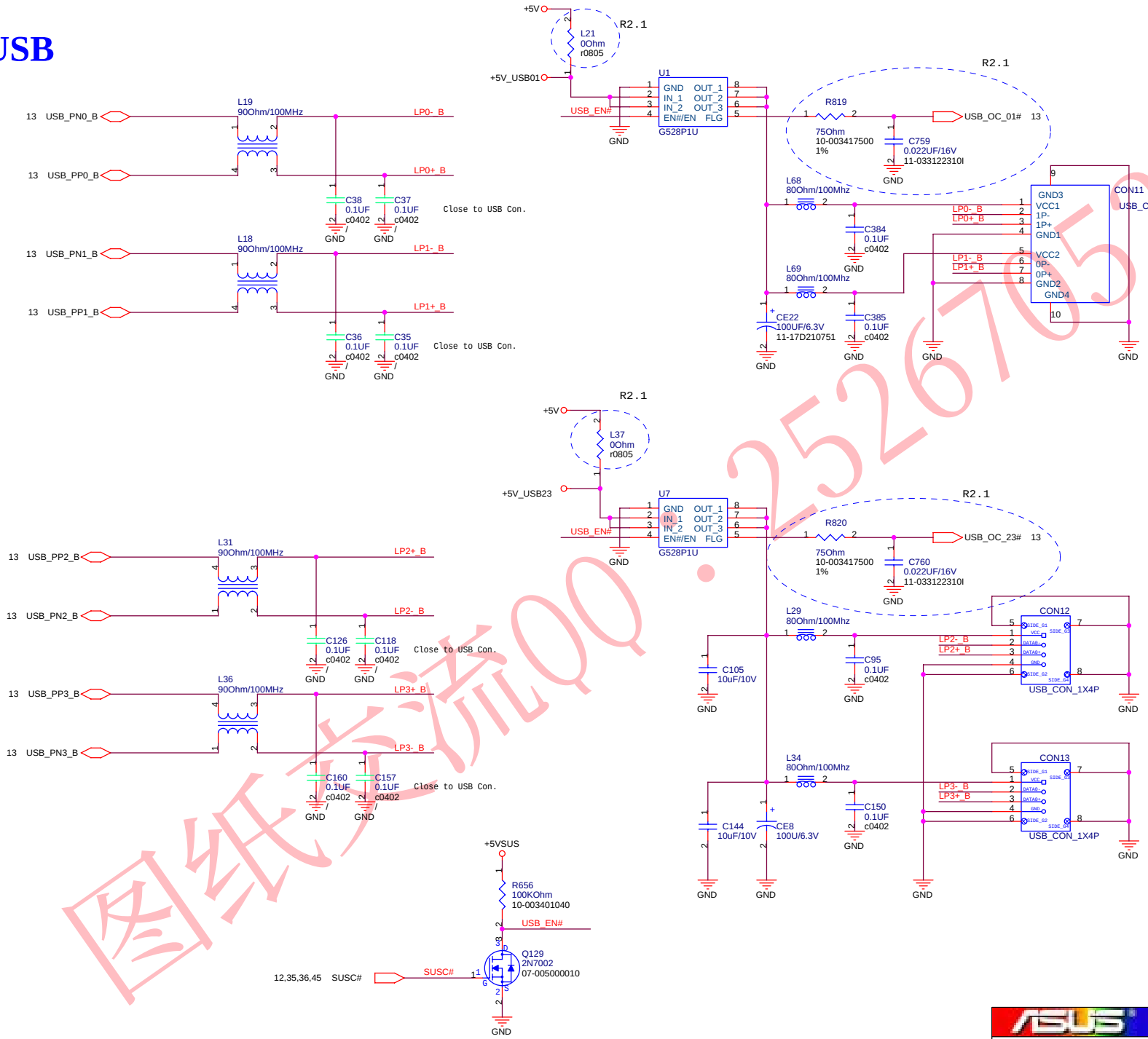
ASUSTeK COMPUTER INC	Title : HDD CONNECTOR		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 32 of 51		



图纸交流QQ：2526705228

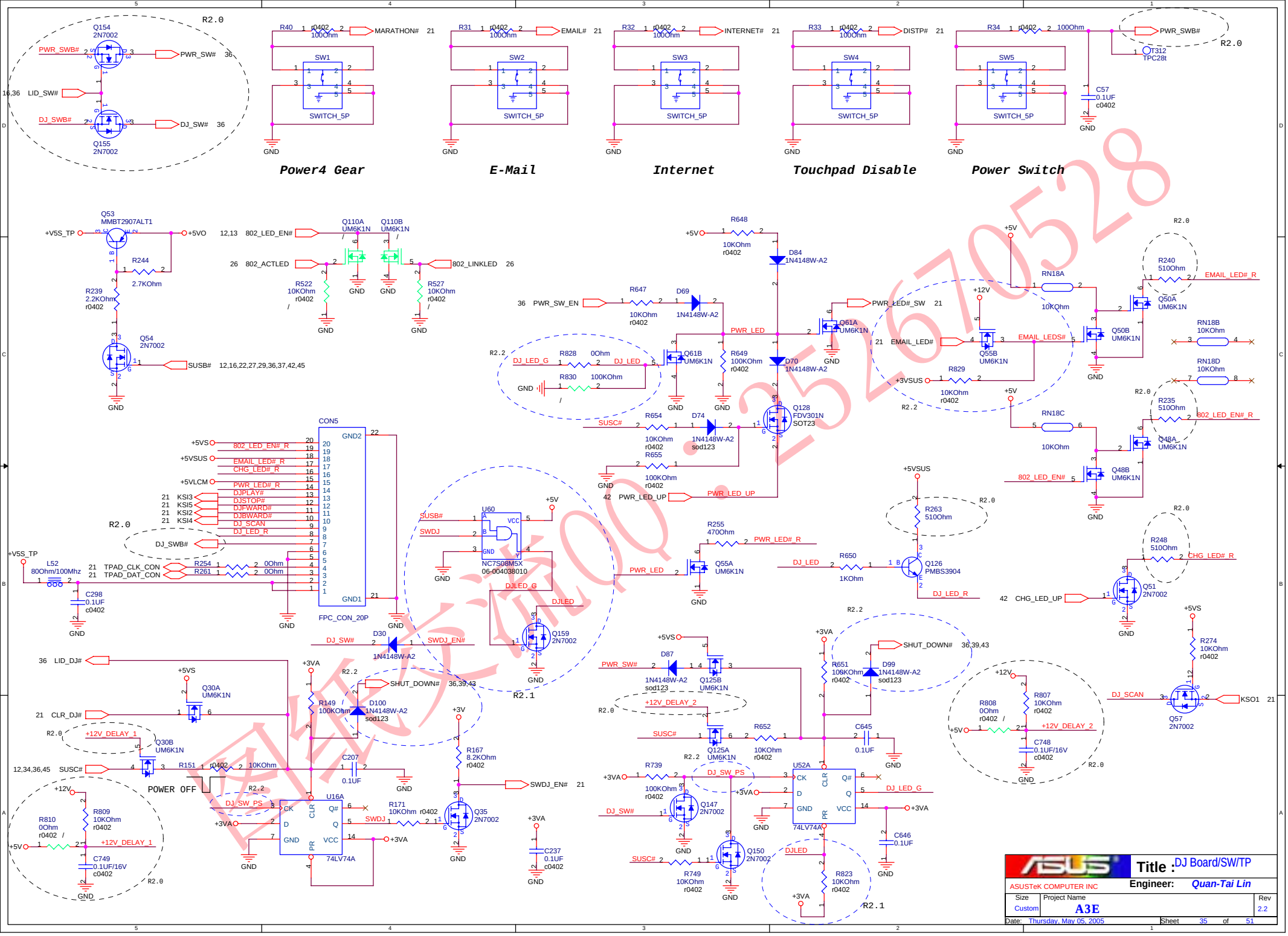
ASUSTeK COMPUTER INC	Title : CDROM		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 33 of 51		

USB

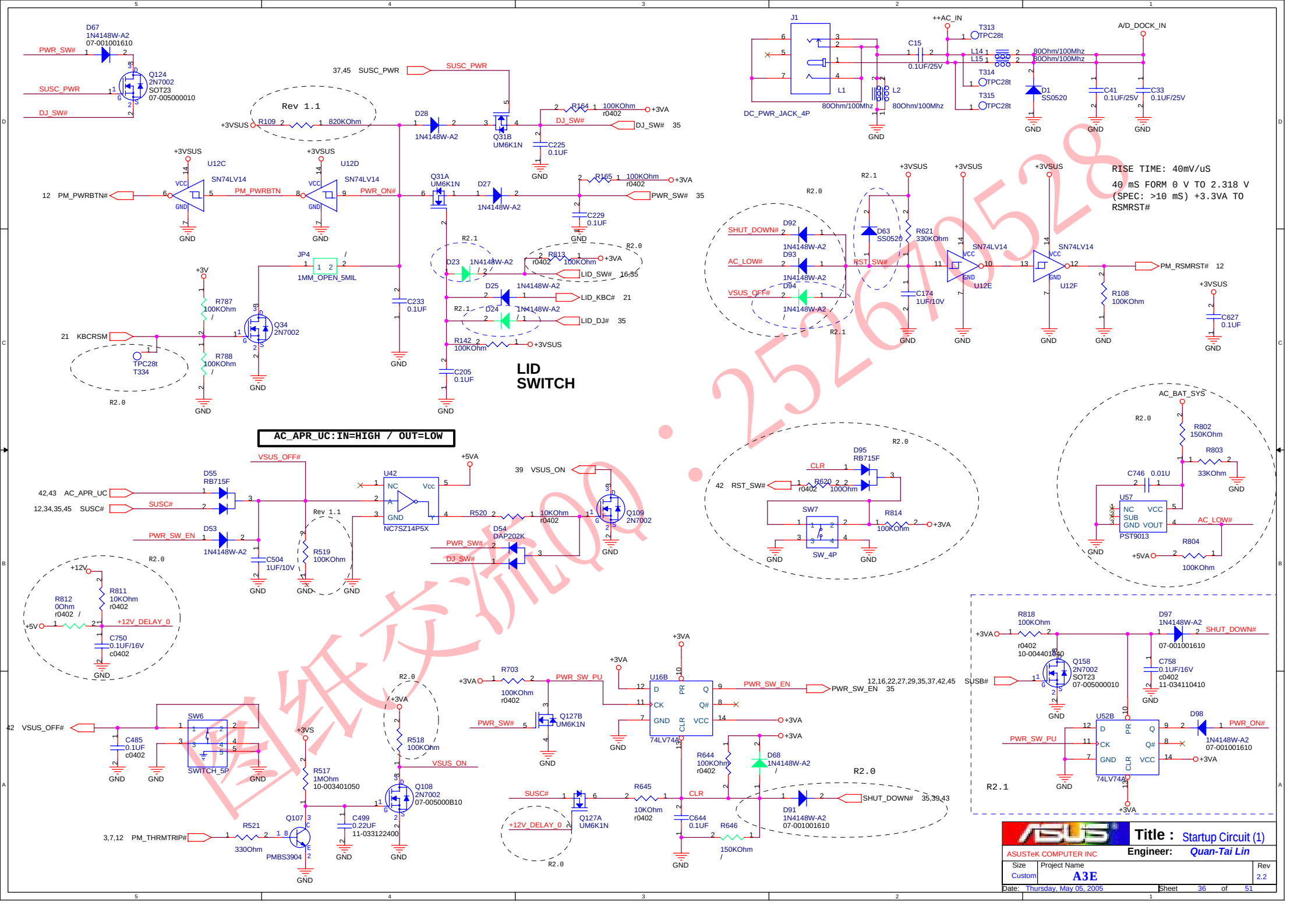


图纸交流QQ：2526706528

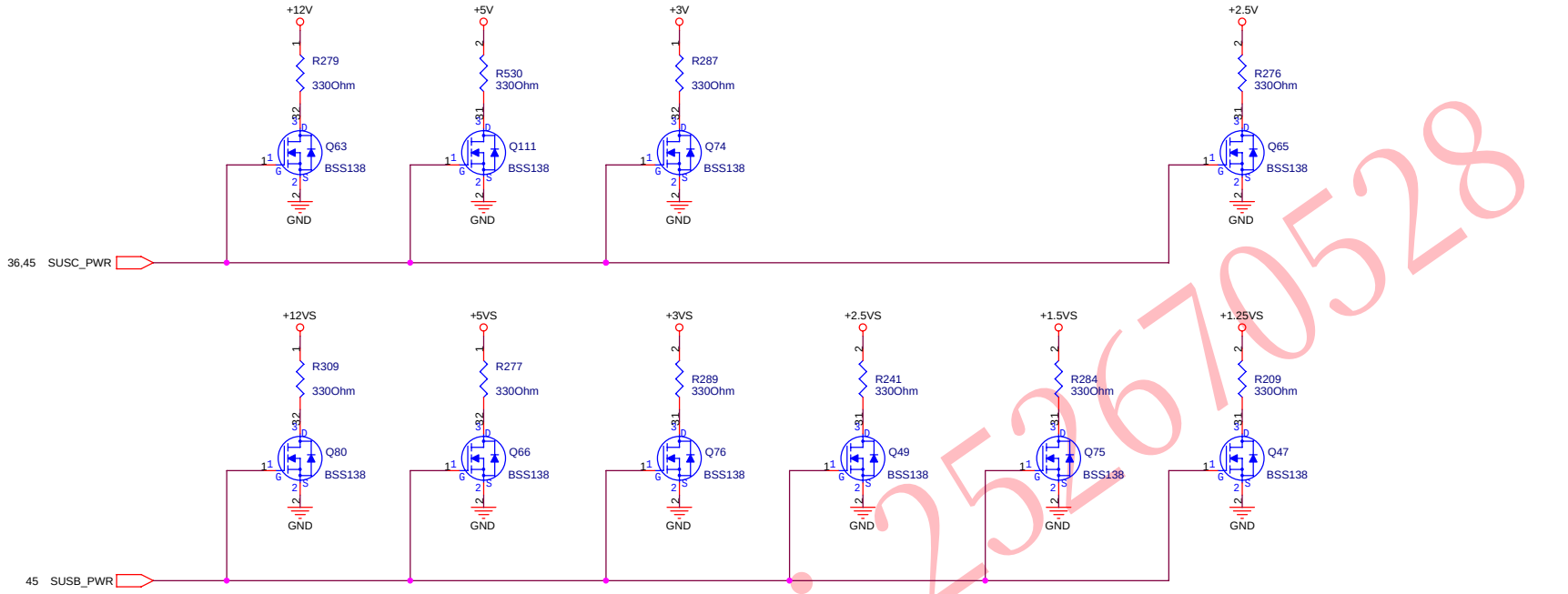
ASUSTeK COMPUTER INC	Title : USB CONN	Engineer: Quan-Tai Lin
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 34 of 51	



图纸交流QQ:2526706528

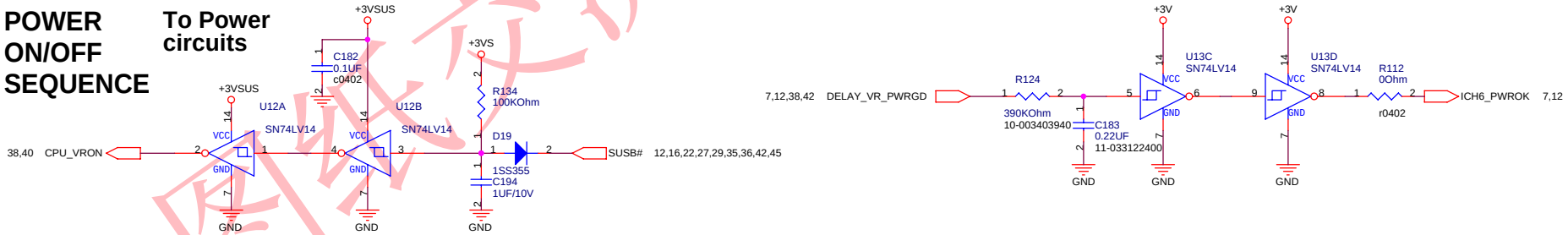


图纸交流QQ：252670528



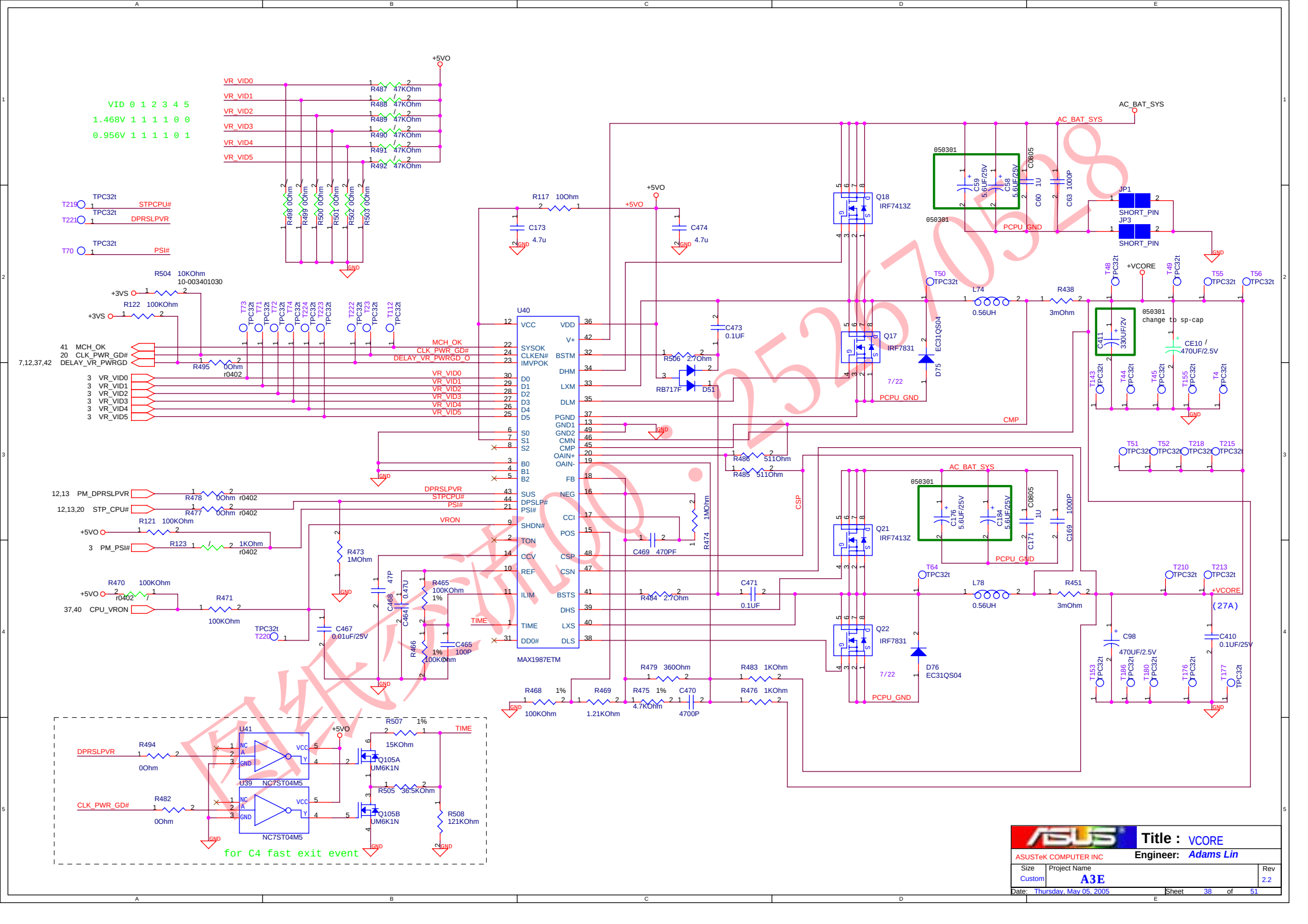
POWER ON/OFF SEQUENCE

To Power circuits



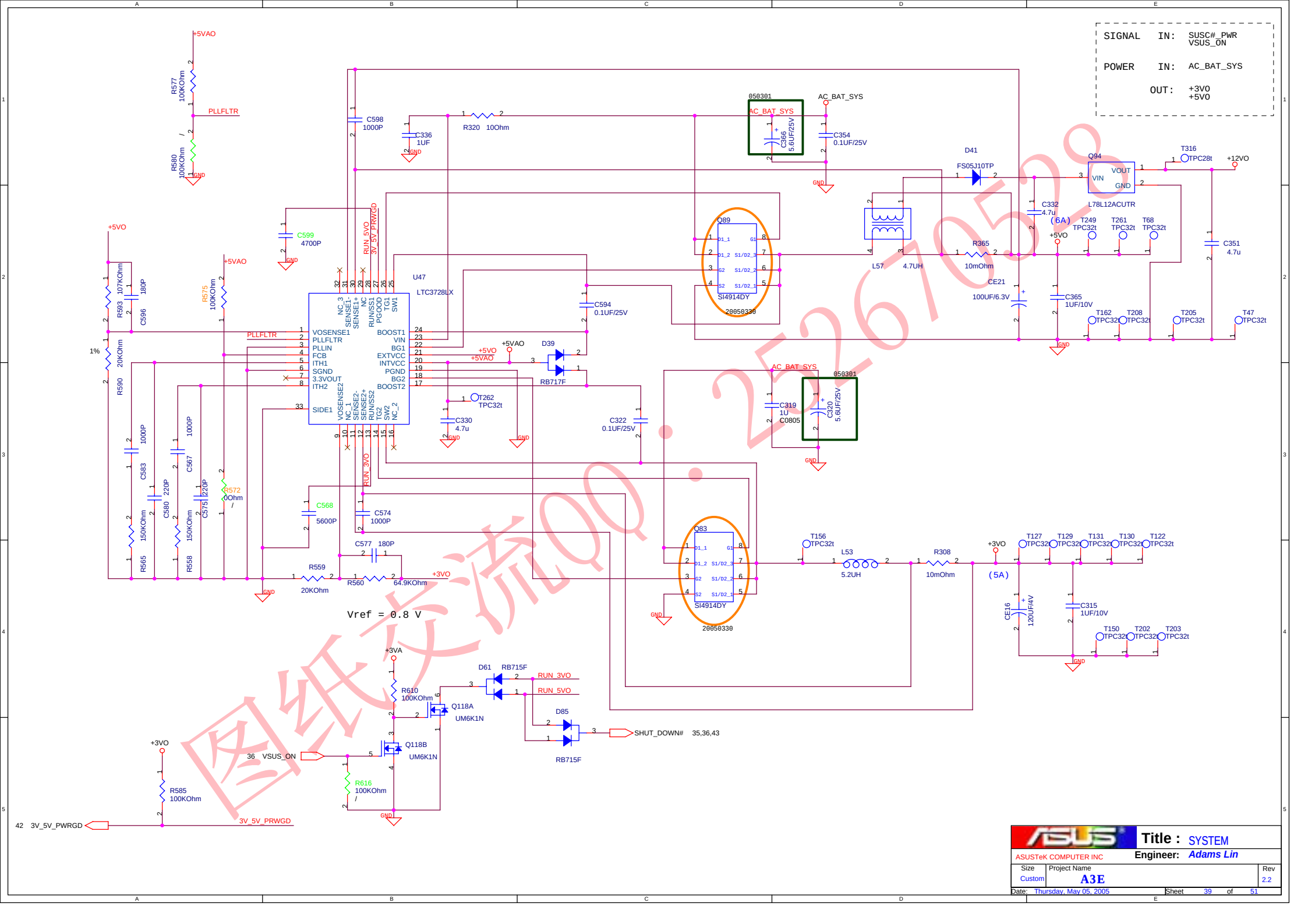
图纸交流QQ：252670528

ASUSTeK COMPUTER INC	Title : Startup Circuit (2)		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 37 of 51		

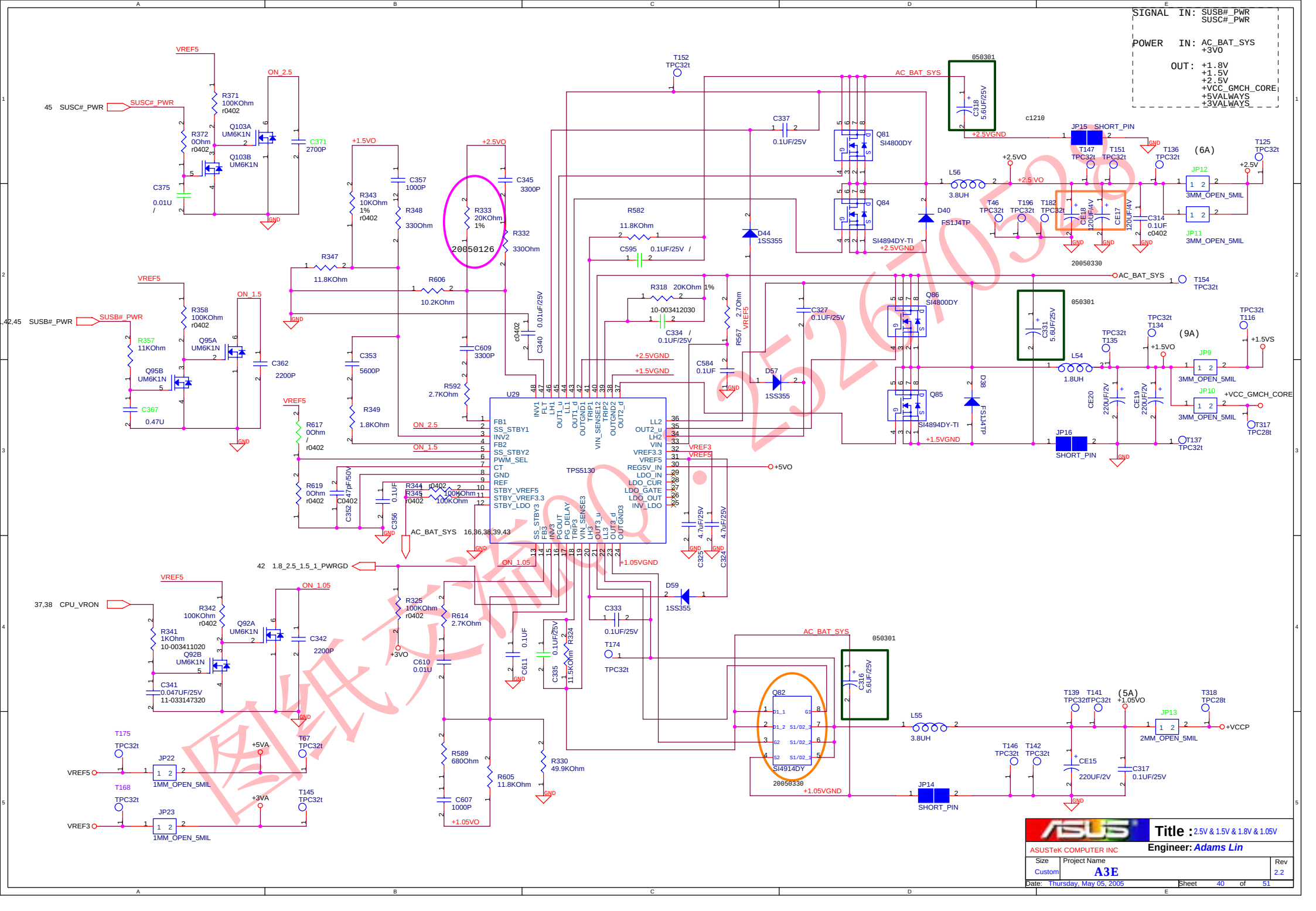


图纸交流QQ：2526706928

ASUSTeK COMPUTER INC	Title : VCORE		
	Engineer: Adams Lin		
Size: Custom	Project Name: A3E		Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 38 of 51		



图纸交流QQ：2526705 28



图纸交流QQ：2526705229

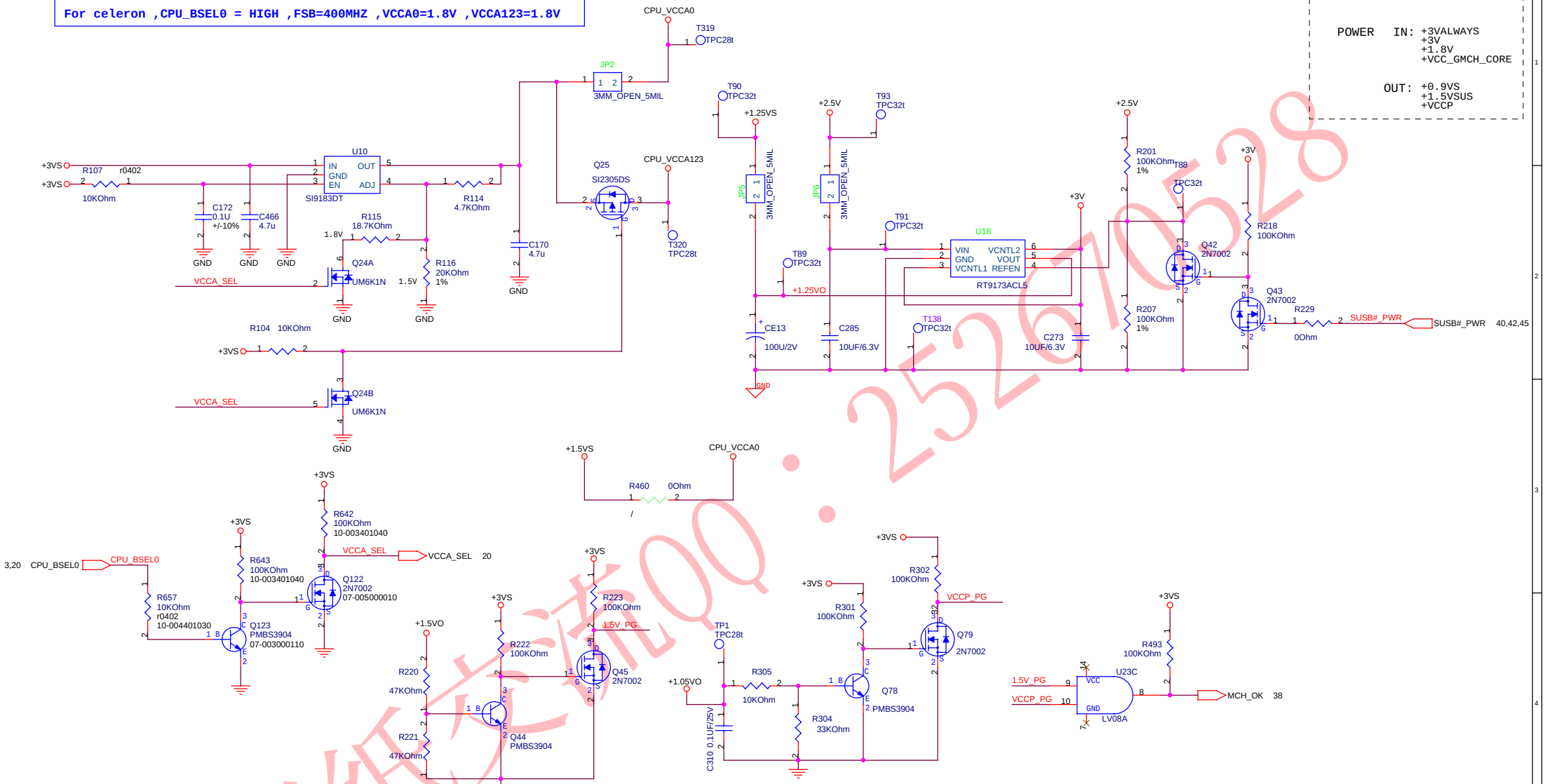
For Duthon ,CPU_BSEL0 = LOW ,FSB=533MHZ ,VCCA0=1.5V ,VCCA123=0V

For celeron ,CPU_BSEL0 = HIGH ,FSB=400MHZ ,VCCA0=1.8V ,VCCA123=1.8V

SIGNAL IN: SUSB#_PWR
CPU_VRON

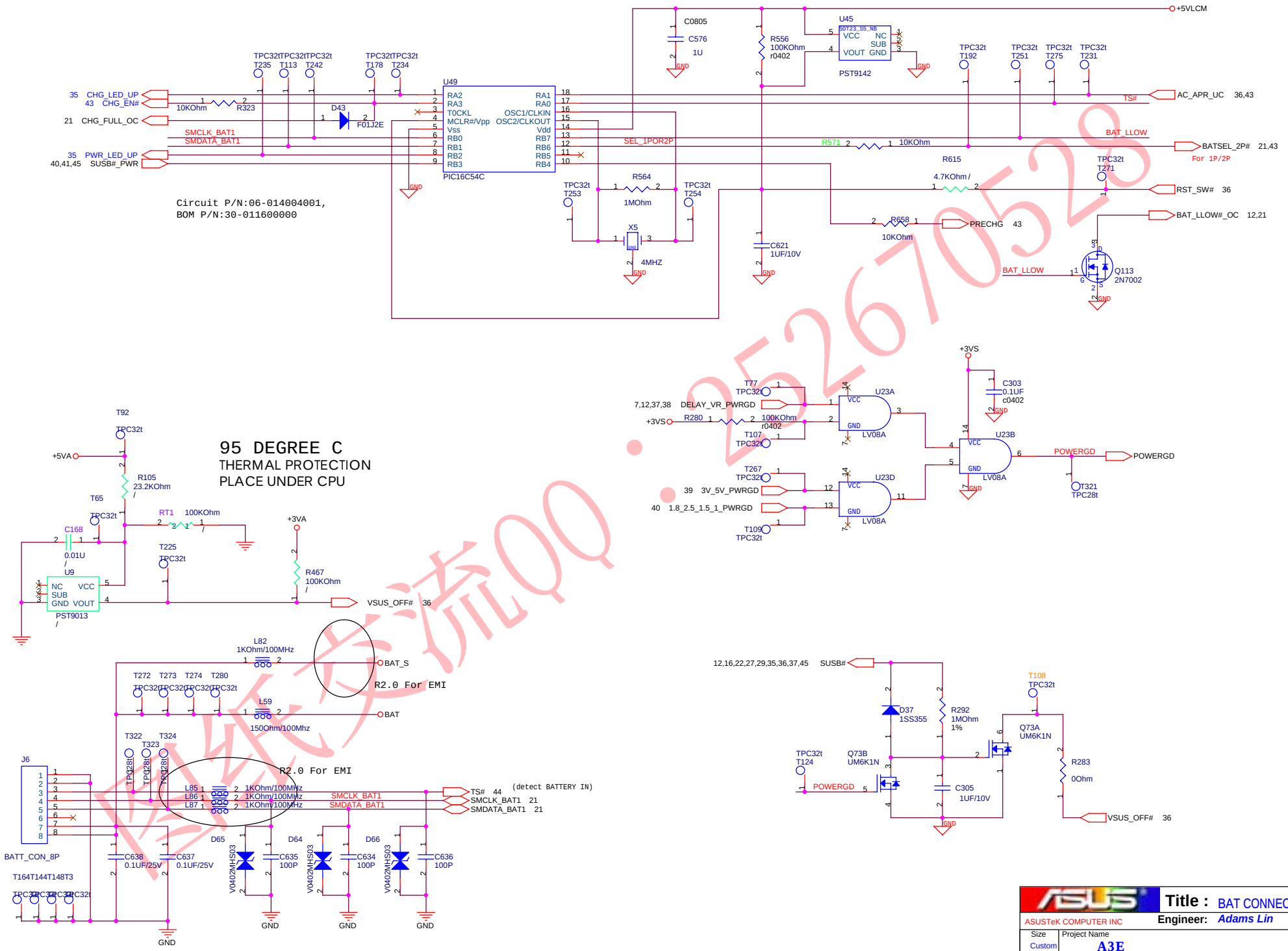
POWER IN: +3VALWAYS
+3V
+1.8V
+VCC_GMCH_CORE

OUT: +0.9VS
+1.5VSUS
+VCCP



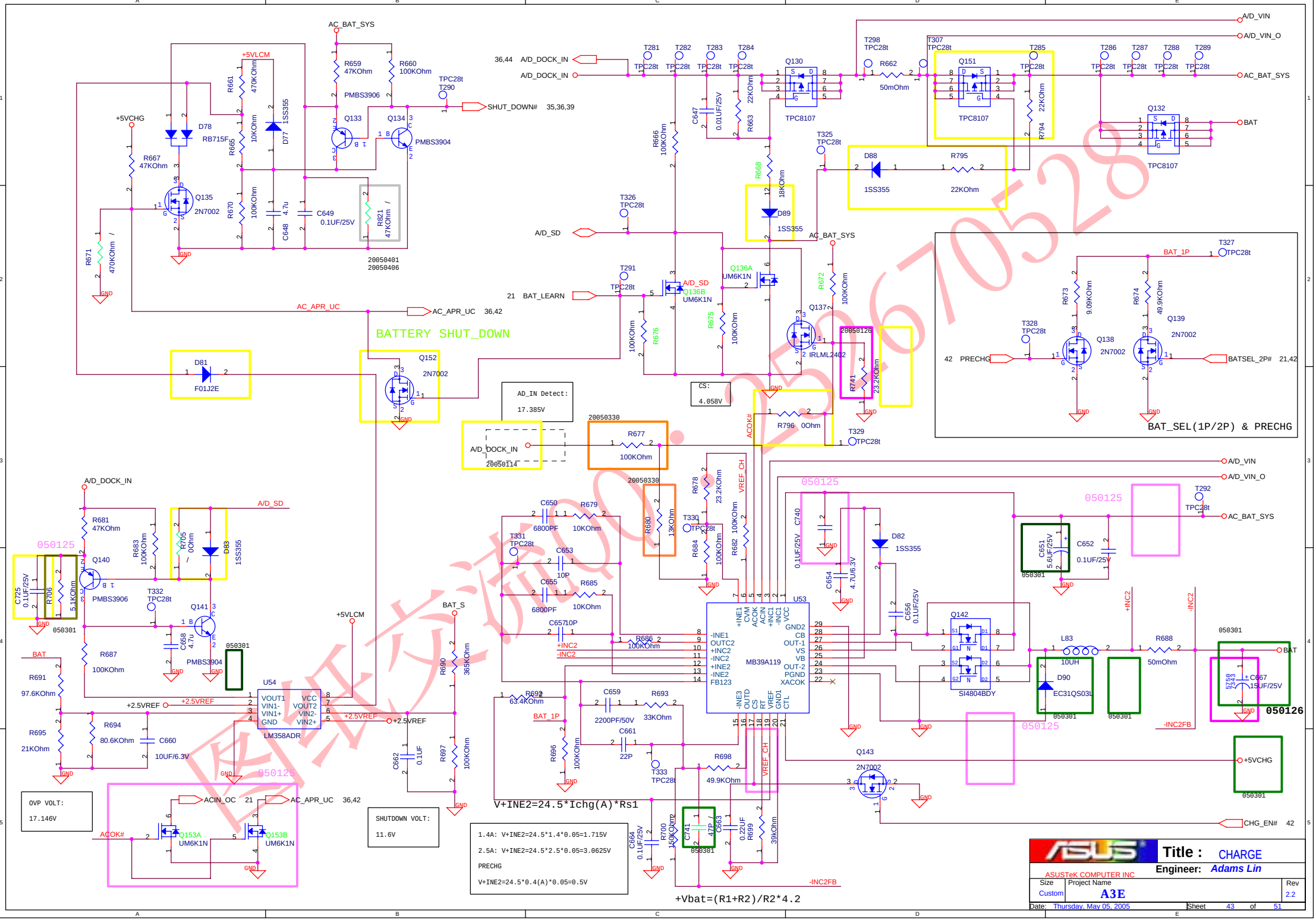
图纸交流QQ：2526706528

ASUS	Title : 1.5VA & DDR2	
ASUSTeK COMPUTER INC	Engineer: Adams Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 41 of 51	

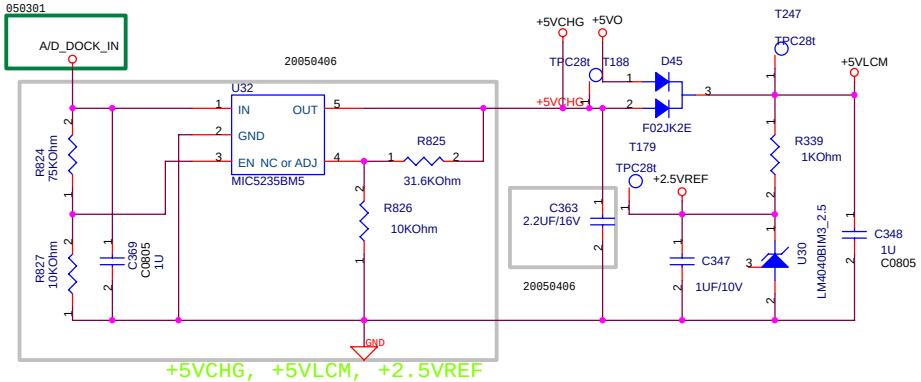


ASUSTeK COMPUTER INC	Title : BAT CONNECT	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 42 of 51	

图纸交流QQ：2526706528



图纸交流QQ：2526670528

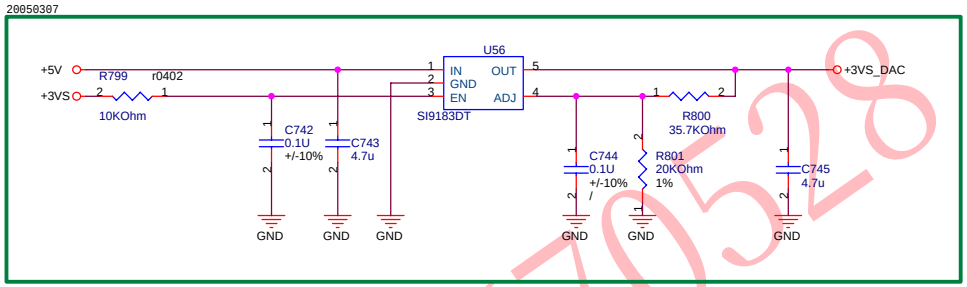


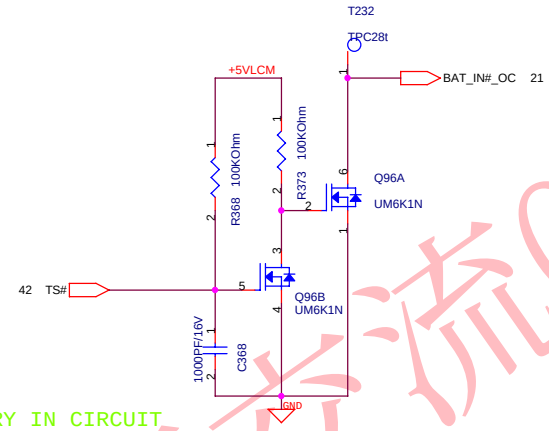
+5VCHG, +5VLCM, +2.5VREF

Ref: 1.24V

ON: EN>2V

OFF: EN<0.6V

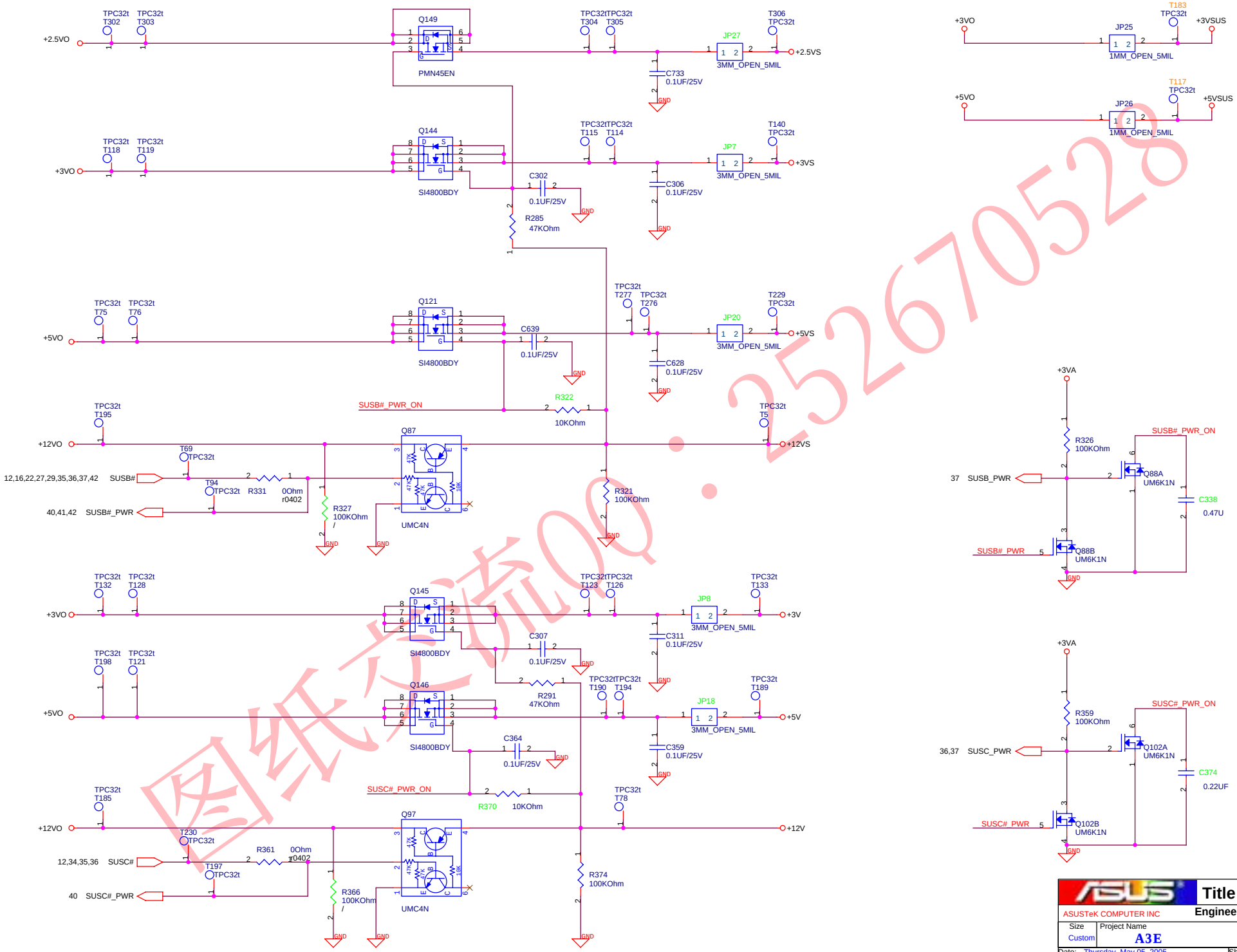




BATTERY IN CIRCUIT

图纸交流QQ：2526705 28

ASUS	Title : BATLOW/SD#	
ASUSTeK COMPUTER INC	Engineer: Adams Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 44 of 51	



图纸交流QQ：2526705 28

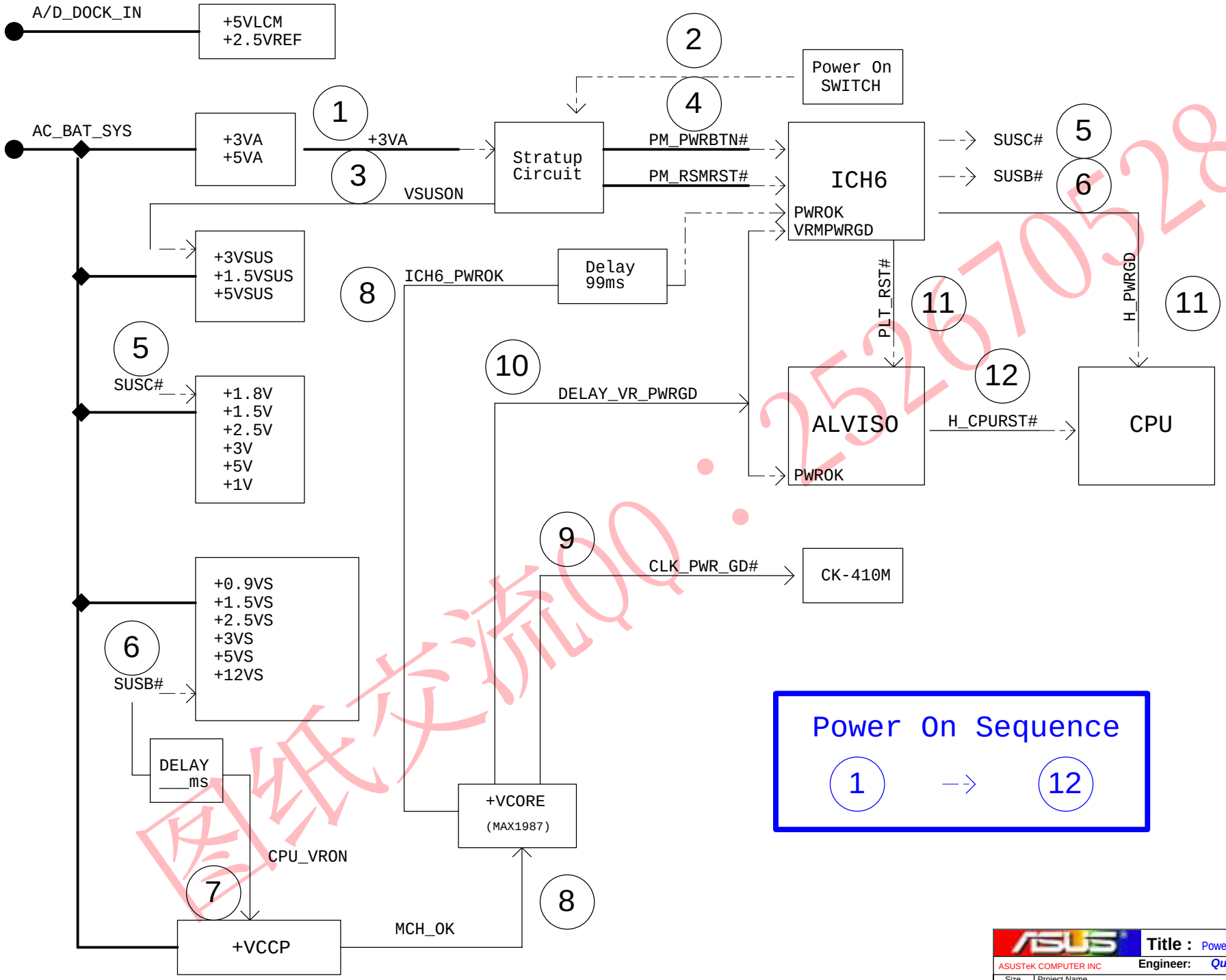
ASUSTeK COMPUTER INC

Title : LOAD SWITCH

Engineer: Adams Lin

Size	Project Name	Rev
Custom	A3E	2.2

Date: Thursday, May 05, 2005 Sheet 45 of 51

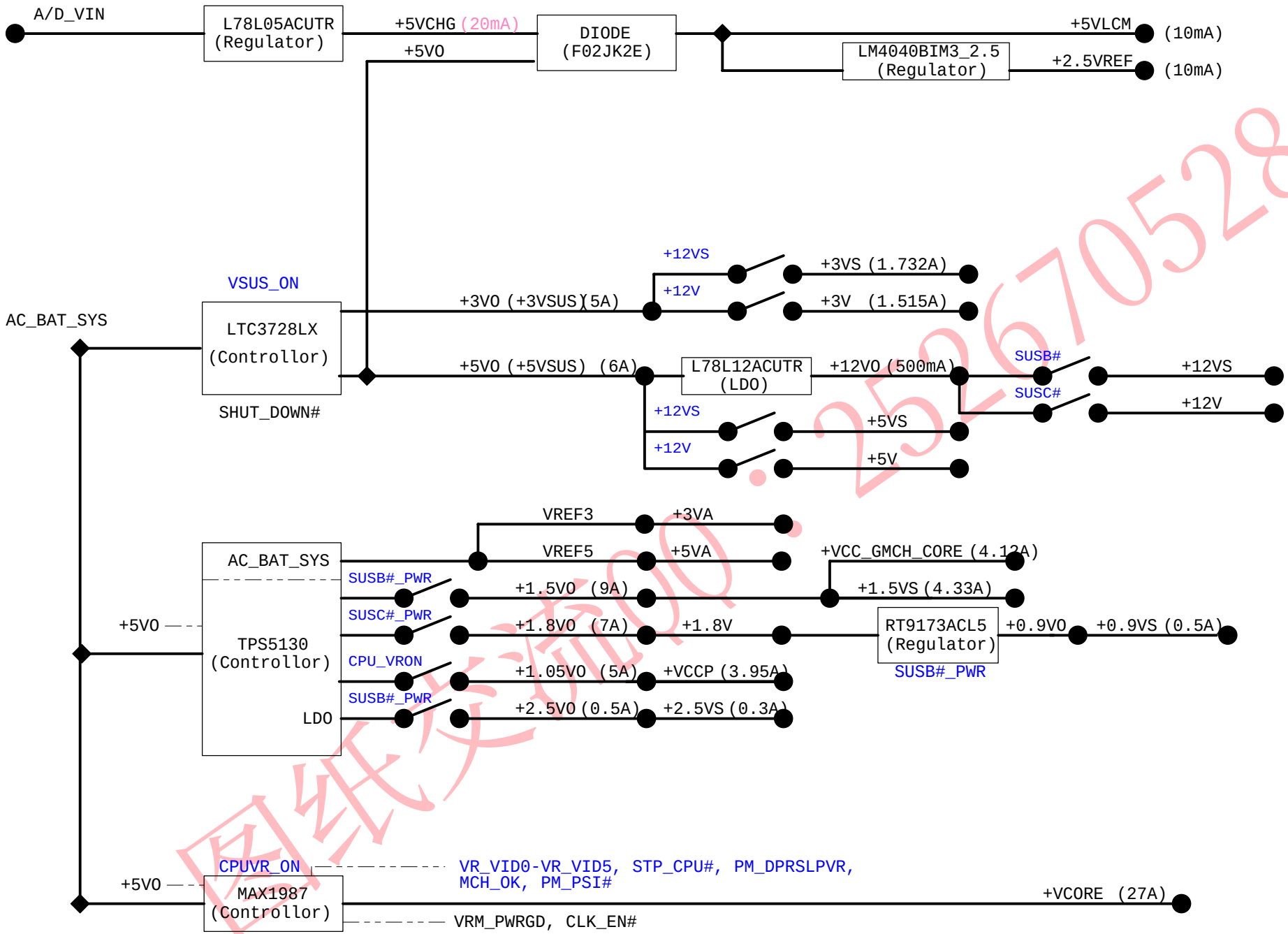


Power On Sequence

1 → 12

图纸交流QQ：252670528

ASUSTeK COMPUTER INC	Title : Power On Sequence		
	Engineer: Quan-Tai Lin		
Size: Custom	Project Name: A3E		Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 46 of 51		



图纸交流QQ：252670528

ASUS	Title : POWER FLOWCHART	
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3E	Rev: 2.2
Date: Thursday, May 05, 2005	Sheet 47 of 51	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)

ICH6-M GPIO	A5V	Note	Volt
GPI 0			+3VS
GPI 1			+3VS
GPI 2			+3VS
GPI 3			+3VS
GPI 4			+3VS
GPI 5			
GPI 7			+3VS
GPI 8	EXTSMI#		+3VSUS
GPI 11	LID_ICH#		+3VSUS
GPI 12	KB_SCI#		+3VSUS
GPI 13	SIO_SMI#		+3VSUS
GPI 14			+3VSUS
GPI 15			+3VSUS
GPO 16			
GPO 17			
GPO 19	PWRLED_1HZ		+3VS
GPO 21	BACK_OFF#		+3VS
GPO 23	FWH_WP#		+3VS
GPO 24	802_LED_EN#		+3VSUS
GPI 26	SATA_DET#0	Unused pull-up to Vcc3_3	+3VS
GPI 27			+3VSUS
GPI 28			+3VSUS
GPI 29	PCB_ID2	Default : 0	+3VS
GPI 30	PCB_ID0	Default : 0	+3VS
GPI 31	PCB_ID1	Default : 0	+3VS
GPI 33	CPUFAN_SPD_A		+3VS
GPO 34	WLAN_ON#		+3VS
GPI 40	PANEL_ID0		+3VS
GPI 41	PANEL_ID1		+3VS
GPO 48			
GPO 49			
GPIO 25	CB_SD#	Diode	+3V

KBC GPIO	A5V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	KBC_P21	
P20(Pin 38)	KBCRSM	
P42(Pin 23)	WATCHDOG	
P43(Pin 22)	OP_SD#	POSTCode前拉Low,ACPI前拉High,ACPI後放掉
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID1	
P52(Pin 15)	KID2	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)	FAN_DA1	
P57(Pin 10)	ADJ_BL	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

图维交流QQ：2267528

ASUSTeK COMPUTER INC

Title : System Resource

Engineer: Quan-Tai Lin

Size	Project Name	Rev
Custom	A3E	2.2

Date: Thursday, May 05, 2005 Sheet 48 of 51

Rev.	Data	Description
1.0	05' 01/06	Initial release
2005/01/21-1140		R735.R736.R750.R752 footprint change to 0603
		JP28 for CMOS clear renames to JRST1 and no mount U19.77 signal changes to ACIN_OC and R245 still mount R73.R75.R76.R77 value change to 470ohm and R41 is 330ohm R519 value changes to 100Kohm
2005/01/24-1035		Add SW8 ,R797 but no mount
2005/01/26-0945		R109 value changes to 820Kohm D72 mount
2005/02/01-1300		R735.R736.R750.R752 tolerance change to 1%
2005/02/21-1300		Add test point :T309(+Vcc_RTC).T310(+RTCBAT).T311(R545.2). T312(PWR_SW#).T313.T314.T315(++AC_IN)
2005/03/01-1130		Add R798 to connect signal MIC_IN_R and MIC_IN_L R163. L43 no mount Add Q154 .Q155 to let LID_SW# to control PWR_SWB# and DJ_SWB# to be on or off Add D91 to connect to SHUT_DOWN# signal
2005/03/04-1600		U19.13 exchange to U19.35 (BAT_SEL# exchange to CHG_FULL_OC) GPIO29=PCB_ID0,GPIO30=PCB_ID1,GPIO31=PCB_ID2 PCB_ID0=1,PCB_ID1=0,PCB_ID2=0
2005/03/07-1500		R518 change to 100Kohm to prevent from +3VA sinking too much current Change CE10 to power and change CE9 to 470UF/2.5V L27.2 and L22.2 change to +3VS_DAC
2005/03/08-0950		Add D92.D93.D94,U57,C746,R802.R803.R804 to prevent from abnormal shut down in startup circuit Change R41 value to 470ohm,R77.R75.R76.R73.R240.R235.R248.R263 to 510ohm Change R184 to 100Kohm and add C747 1uF/10V Add T334 to R788.1 for KBCRSM signal
2005/03/10-1128		Colay Q156, R805and Q157,R806 for keep from PCMCIA device current leakage Q125,Q30,Q127 turn on voltage change to a RC delay +12V Add R811.C750.R812 for +12V_DELAY_0 signal Add R809.C749.R810 for +12V_DELAY_1 signal Add R807.C748.R808 for +12V_DELAY_2 signal
2005/03/11-1120		Add C751.C752 for EMI(P.28) Add C754.C755 100PF for EMI(P.16) Add C753 100PF. R815 0ohm for EMI(P.16) Add U58.U59 for EMI(P.4) Add R813 to pull up LID_SW# to +3VA Add D95.R814 to make RESET button (SW7) function to be ok
2005/03/14-1040		Delete T53.T207.T217.T214.T211.T212.T209.T216 Add C756.C757 47UF/6.3V 1206 to +2.5VS on page 9 Add D96.RP5.RP6.R816 and pull to +5VS for LPT C751.C752 footprint change to 1812_h71 Add H26.H27
2005/03/15-2050		Add R817 10Kohm to pull high to +3VS on page 5

Rev.	Data	Description
2005/03/16-1600		R178.R198 value change to 3.9Kohm 1% C630.C631.C632.C633 still mount C751.C752 still mount R625.R632.R633.R634 change to 120ohm/100MHz bead R175.R199 still mount L50.R150 change to 1Kohm/100MHz bead L6.L7.L8 change to 60ohm /100MHz bead R162 change value to 4.7Kohm 1% CE9 change to 470UF/2.5V
Rev 2.1		
2005/03/29-1710		Add D63 back and D94 is no mount
2005/04/01-1228		Add U52B,D98,D97,R818,C758,Q158 for start up circuit D23.D24 no mount Add R819.C759 between U1.5 (FLG) and USB_OC_01# Add R820.C760 between U7.5 (FLG) and USB_OC_23# C751.C752 footprint changes to C1808_inverter_h79
2005/04/06		L21.L37 change to 0ohm resistance (0805) Add U60.R822.R823.Q159 for LED signal

图纸交流QQ：252670528

ASUS	Title : History-EE(1)	
ASUSTeK COMPUTER INC	Engineer: Quan-Tai Lin	
Size A3	Project Name A3E	Rev 2.2
Date: Thursday, May 05, 2005	Sheet 49 of 51	

Rev.	Data	Description
For RM:		
	2005/01/24-1035	Page 31 no mount : R566,Q114,Q115,C579,C564 Page 20 no mount : R54,R43,Q16,Q19,R412 Page 41 no mount : R657,R643,Q122,Q123 Mount SW8 ,R797 Add SWITCH TABLE for CPU frequency select

Rev.	Data	Description

图纸交流QQ：252670528

ASUSTeK COMPUTER INC

Title : History-EE(2)

Engineer: Quan-Tai Lin

Size	Project Name	Rev
Custom	A3E	2.2

Date: Thursday, May 05, 2005 Sheet 50 of 51

Rev.	Data	Description
1.0	05' 01/06	Initial release
	2005/01/21-1200	Add 22Kohm R794.R795 , P-MOS Q151 , diode D88.D89
	2005/01/21-1200	Add capacitor C739,resistor R796,N-MOS Q152,diode D90
	2005/01/21-1200	R677 value is from 110Kohm to 107Kohm and R677.1 connect to A/D_DOCK_IN
	2005/01/21-1200	R680 value is from 14Kohm to 13.7Kohm and D81 changes to F01J2E
	2005/01/21-1200	D83 mount and R705 no mount and R725 mount
	2005/01/26-0945	R333 value changes to 20Kohm
	2005/01/26-0945	Add Q153 for ACIN_OC and AC_APR_UC signals and delete D90
	2005/01/26-0945	Change U53.18 and U53.19 for signal VREF_CH
	2005/01/26-0945	Delete JP24 and add a cap C740 0.1UF
	2005/01/26-0945	C725 still mount and R706 no mount
	2005/01/26-0945	R741 value changes to 23.2K ohm
	2005/01/26-1250	C666 changes to connect to L83.2
	2005/01/28-1200	C666 no mount
	2005/02/21-1300	Add test point : T316(+12VO).T317(+VCC_GMCH_CORE).T318(+VCCP). T319(CPU_VCCA0).T320(CPU_VCCA123).T322(R631.1).T323(R630.1). T324(R629.1).T321(POWERGD).T329(R796.2).T326(A/D_SD).T325(D88.2). T332(C658.1).T330(R684.2).T333(C661.1).T327(BAT_1P).T331(C653.2). T328(PRECHG)
	2005/03/01-1800	Change C59, C58, C176, C184, C366, C320, C318, C331, C316, C651 to POSCAP 5.6UF/25V Add D90 for Charger noise(P. 43) Remove C666, R705, R689 Change r706 to 5.1Kohm Change U53 Pin 21 connector to +5VCHG Change U32 Pin 1 connector to A/D_DOCK_IN Change C441 to 330UF/2V SP-CAP Change C98 to 470UF/2.5V POSCAP Add C741 47PF/50V with R700(P.43) Change C667 to 15UF/2.5V POSCAP
	2005/03/30-1124	Change R677 to 100Kohm Change R680 to 13Kohm Change CE17,CE18 to 220UF/4V Mount R283 Change Q82, Q83, Q89 to SI4914
	2005/04/01-1640	Change CE17,CE18 to 120UF/4V Add R821 47Kohm for boot issue

Rev.	Data	Description
	2005/04/06-1524	Change U32 to MIC5235BM5 Add R824=75K, R827=10K, R825=31.6K, R826=10K Change C363 to 2.2UF/16V Change R821 to unmount

图纸交流QQ：252670528

ASUSTeK COMPUTER INC	Title : History-PWR	Engineer: Quan-Tai Lin
Size: Custom	Project Name: A3E	Rev: 2.2
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