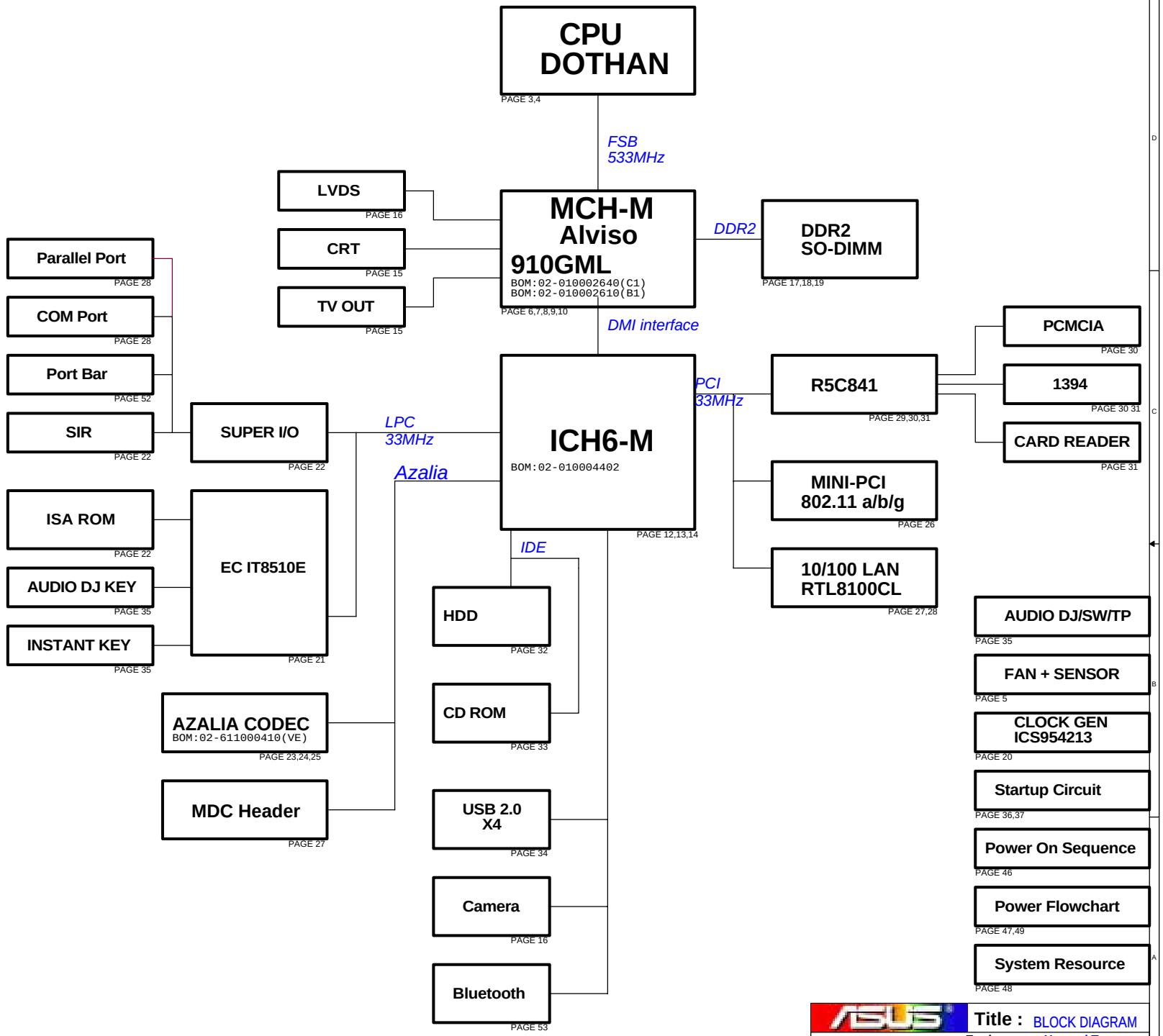
A3H CONTEXT



ASUSTeK COMPUTER INC	Title : BLOCK DIAGRAM	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 1 of 54	

REVISION LIST

POWER INTERFACE

SIGNALS	TYPE	POWER
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
VRON	O	+3.3V
PM_DPRSLPVR	O	+3.3V
CPU_STP#	O	+3.3V
RST_BTN#	O	+3.3V
CLK_EN#	I	+3.3V
DELAY_VR_PWRGD	I	+3.3V
OTP_RESET#	I	+3.3V
SHUT_DOWN#	I	+3.3V
BAT_LEARN	I	+3.3V
BAT_LLOW#_OC	I	+3.3V
BAT_IN#_OC	I	+3.3V
CHG_EN#	I	+3.3V
CHG_FULL_OC	I	+3.3V
CHG_LED_UP	I	+3.3V
SMCLK_BAT1	IO	+3.3V
SMDATA_BAT1	IO	+3.3V
SUSB#	O	+3.3V
SUSC#	O	+3.3V
1.8V_PWRGD	I	+3.3V
1.5VS_PWRGD	I	+3.3V
VSUS_ON	O	+3.3V
ACIN_OC	I	+3.3V
ACIN#	I	AC_BAT_SYS
+3VA	PWR	+3.3V
+5VA	PWR	+5V
+5VLCM	PWR	+5VLCM
A/D_DOCK_IN	PWR	DC
AC_BAT_SYS	PWR	DC

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.95A
+VCC_GMCH	1.05V	4.12A
+0.9VS	1.25V	0.85A
+1.5VS	1.5V	4.33A
+1.5V	1.5V	300 mA
~~+1.5VSUS~~	~~1.5V~~	~~270 mA~~
+1.8V	1.8V	6.68A
+2.5VS	2.5V	0.3 A
+3VS	3.3V	1.732A
+3V	3.3V	1.515A
+3VSUS	3.3V	540 mA
+5VS	5V	4.1A
+5V	5V	0.5A
+5VSUS	5V	0.5A
+12V	12V	0.25A
+12VS	12V	0.25A

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	18 mils

37.5 OHM	WIDTH
TOP/BOT	11 mils
IN1/IN2	9.5 mils

42 OHM	WIDTH
TOP/BOT	9 mils
IN1/IN2	7.5 mils

50 OHM	WIDTH
TOP/BOT	6 mils
IN1/IN2	5 mils

55 OHM	WIDTH
TOP/BOT	5.5 mils
IN1/IN2	4.5 mils

75 OHM	WIDTH
TOP/BOT	4 mils
IN1/IN3	3.5 mils

Differential

70 OHM	WIDTH/SPACE
TOP/BOT	9 mils/ 4 mils
IN1/IN2	7.5 mils/ 4 mils

85 OHM	WIDTH/SPACE
TOP/BOT	5.5 mils/ 4 mils
IN1/IN2	4.5 mils/ 4 mils

90 OHM	WIDTH/SPACE
TOP/BOT	5.5 mils/ 5 mils
IN1/IN2	4.5 mils/ 5 mils

100 OHM	WIDTH/SPACE
TOP/BOT	6 mils/ 11 mils
IN1/IN2	5 mils/ 12 mils

110 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 13 mils
IN1/IN2	4 mils/ 12 mils

PCI INTERFACE

PCI_REQ#

MINIPCI	PCI_REQ#3
10/100	PCI_REQ#2
CB&1394	PCI_REQ#1

IDSEL

MINIPCI	PCI_AD19
10/100	PCI_AD16
CB&1394	PCI_AD17

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1 TOP
L2 GND
L3 IN1
L4 IN2
L5 GND
L6 BOT

PAGE 38

SIGNAL	IN:	VR_VID[0..5] PM_DPRSLPVR STP_CPU# PM_PSI# CPU_VRON MCH_OK
	OUT:	DELAY_VR_PWRGD CLK_PWR_GD#
POWER	IN:	AC_BAT_SYS +5VO +3VO
	OUT:	+VCORE

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SIGNAL	IN:	~~SUSC#_PWR~~ VSUS_ON
POWER	IN:	AC_BAT_SYS
	OUT:	+12VO +3VO +5VO

PAGE 40

SIGNAL	IN:	SUSB#_PWR SUSC#_PWR CPU_VRON
POWER	IN:	AC_BAT_SYS +5VO
	OUT:	+1.8V +1.5VS +2.5VS +VCC_GMCH_CORE +5VALWAYS +3VALWAYS +VCCP

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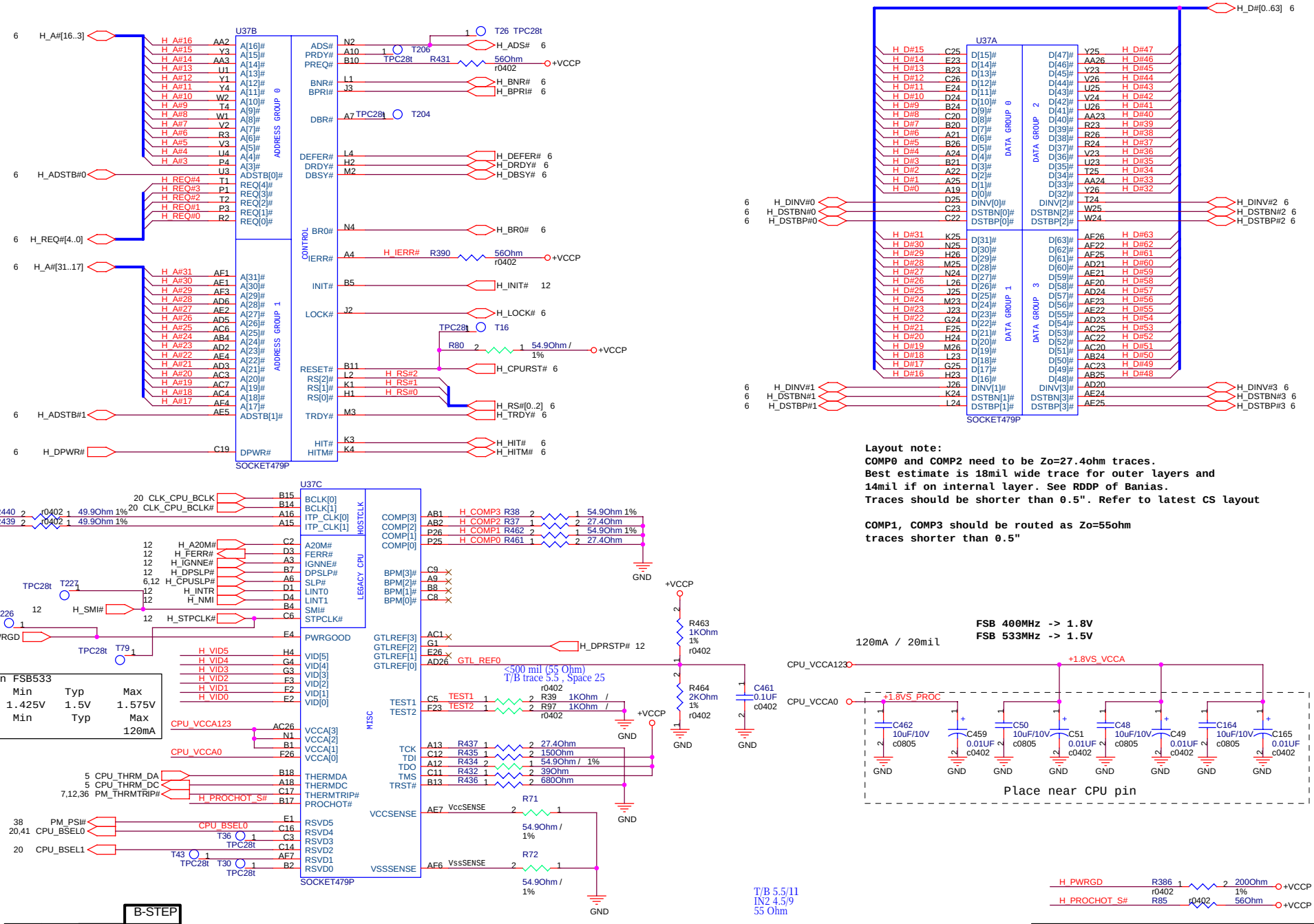
SIGNAL	IN:	SUSB#_PWR
POWER	IN:	+3V +1.8V
	OUT:	+0.9VS

ASUSTeK COMPUTER INC	Title :	REVISION LIST
	Engineer:	Howard Tu
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 2 of 54	


U37B
U37A
U37C
SOCKET479P
ADDRESS GROUP 0
ADDRESS GROUP 1
DATA GROUP 0
DATA GROUP 1
DATA GROUP 2
DATA GROUP 3
CONTROL
H_A#[16..3]
H_ADSTB#0
H_REQ#[4..0]
H_A#[31..17]
H_ADSTB#1
H_DPWR#
H_ADS#
H_BNR#
H_BPRI#
H_DEFER#
H_DRDY#
H_DBSY#
H_BR0#
H_IERR#
H_INIT#
H_LOCK#
H_CPURST#
H_RS#[0..2]
H_TRDY#
H_HIT#
H_HITM#
H_D#[0..63]
H_DINV#0
H_DSTBN#0
H_DSTBP#0
H_DINV#1
H_DSTBN#1
H_DSTBP#1
H_DINV#2
H_DSTBN#2
H_DSTBP#2
H_DINV#3
H_DSTBN#3
H_DSTBP#3
+VCCP
CLK_CPU_BCLK
CLK_CPU_BCLK#
H_A20M#
H_FERR#
H_IGNNE#
H_DPSLP#
H_CPUSLP#
H_INTR
H_NMI
H_SMI#
H_STPCLK#
H_PWRGD
H_VID5
H_VID4
H_VID3
H_VID2
H_VID1
H_VID0
H_DPRSTP#
GTL_REF0
CPU_VCCA123
CPU_VCCA0
CPU_THRM_DA
CPU_THRM_DC
PM_THRMTRIP#
H_PROCHOT_S#
PM_PSI#
CPU_BSEL0
CPU_BSEL1
VccSENSE
VssSENSE
H_COMP3
H_COMP2
H_COMP1
H_COMP0
H_IERR#
H_RS#2
H_RS#1
H_RS#0
H_PWRGD
H_PROCHOT_S#
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID1
VR_VID0
+1.8VS_VCCA
+1.8VS_PROC
GND
Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
Best estimate is 18mil wide trace for outer layers and
14mil if on internal layer. See RDDP of Banias.
Traces should be shorter than 0.5". Refer to latest CS layout
COMP1, COMP3 should be routed as Zo=55ohm
traces shorter than 0.5"
FSB 400MHz -> 1.8V
FSB 533MHz -> 1.5V
120mA / 20mil
Place near CPU pin
<500 mil (55 Ohm)
T/B trace 5.5 , Space 25
T/B 5.5/11
IN2 4.5/9
55 Ohm
Dothan FSB533
Min Typ Max
VCCA 1.425V 1.5V 1.575V
Min Typ Max
ICCA 120mA
Bclk FSB BSEL1 B-STEP BSEL0
100 400 0 1
133 533 0 0
Title : DOTHAN CPU (1)
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size Custom
Project Name A3H
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 3 of 54

Dothan FSB533	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

+VCCP

+VCORE

U37D

VCC

SOCKET479P

U37E

GND

SOCKET479P

GND

GND

MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
0 0 0 0 0 0	1.708V	1 0 0 0 0 0	1.196V
0 0 0 0 0 1	1.692V	1 0 0 0 0 1	1.180V
0 0 0 0 1 0	1.676V	1 0 0 0 1 0	1.164V
0 0 0 0 1 1	1.660V	1 0 0 0 1 1	1.148V
0 0 0 1 0 0	1.644V	1 0 0 1 0 0	1.132V
0 0 0 1 0 1	1.628V	1 0 0 1 0 1	1.116V
0 0 0 1 1 0	1.612V	1 0 0 1 1 0	1.100V
0 0 0 1 1 1	1.596V	1 0 0 1 1 1	1.084V
0 0 1 0 0 0	1.580V	1 0 1 0 0 0	1.068V
0 0 1 0 0 1	1.564V	1 0 1 0 0 1	1.052V
0 0 1 0 1 0	1.548V	1 0 1 0 1 0	1.036V
0 0 1 0 1 1	1.532V	1 0 1 0 1 1	1.020V
0 0 1 1 0 0	1.516V	1 0 1 1 0 0	1.004V
0 0 1 1 0 1	1.500V	1 0 1 1 0 1	0.988V
0 0 1 1 1 0	1.484V	1 0 1 1 1 0	0.972V
0 0 1 1 1 1	1.468V	1 0 1 1 1 1	0.956V
0 1 0 0 0 0	1.452V	1 1 0 0 0 0	0.940V
0 1 0 0 0 1	1.436V	1 1 0 0 0 1	0.924V
0 1 0 0 1 0	1.420V	1 1 0 0 1 0	0.908V
0 1 0 0 1 1	1.404V	1 1 0 0 1 1	0.892V
0 1 0 1 0 0	1.388V	1 1 0 1 0 0	0.876V
0 1 0 1 0 1	1.372V	1 1 0 1 0 1	0.860V
0 1 0 1 1 0	1.356V	1 1 0 1 1 0	0.844V
0 1 0 1 1 1	1.340V	1 1 0 1 1 1	0.828V
0 1 1 0 0 0	1.324V	1 1 1 0 0 0	0.812V
0 1 1 0 0 1	1.308V	1 1 1 0 0 1	0.796V
0 1 1 0 1 0	1.292V	1 1 1 0 1 0	0.780V
0 1 1 0 1 1	1.276V	1 1 1 0 1 1	0.764V
0 1 1 1 0 0	1.260V	1 1 1 1 0 0	0.748V
0 1 1 1 0 1	1.244V	1 1 1 1 0 1	0.732V
0 1 1 1 1 0	1.228V	1 1 1 1 1 0	0.716V
0 1 1 1 1 1	1.212V	1 1 1 1 1 1	0.700V

1.0V - 1.2V(+/- 5%)
S0-S1M: 2.5
A(CPU,MCH,ICH)

Dothan FSB533	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A

+VCCP

CE4 150U/4.0V
C100 0.1UF c0402
C442 0.1UF c0402
C99 0.1UF c0402
C441 0.1UF c0402
C127 0.1UF c0402
C412 0.1UF c0402
C407 0.1UF c0402
C128 0.1UF c0402
C408 0.1UF c0402

GND

C443 0.1UF c0402
C414 10uF/10V c0805
C434 10uF/10V c0805

U69 SPRING_SQ31 /
U70 SPRING_SQ31 /

For EMI

+VCCP (CPU) Decoupling Capacitor
(Place near CPU)

ASUSTeK COMPUTER INC	Title : DOTHAN CPU (2)	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 4 of 54	

Fan Speed Control

CPU FAN

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

P/N change to 06-010112010 for cost down

U6 output maximum will be 10.5V (VCC-1.5V) which will damage sourth bridge. Add a MOS to tansfer it to +3V level.

Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

CPU VCORE Decoupling Capacitor

Mid Frequency Decoupling (Place around Processor)

High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R

+VCORE Bulk Decoupling

Four 200 uF are located in IMVP4

Close to Pin A18 & B18 of CPU

Standby Mode: 3uA(Max. 10uA)
Full Active: 0.5 mA(Max. 1mA)

Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58

Title : THER-SENSOR,FAN
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size: Custom | Project Name: A3H | Rev: 1.0
Date: Thursday, June 30, 2005 | Sheet 5 of 54

In OrCAD circuit,ALVISO PM P/N :02-010002600

But we have to use ALVISO GM P/N : 02-010002610 in BOM list

H_XRCOMP 12/20mils

R380 24.9Ohm 1% — GND

+VCCP

R379 54.9Ohm 1%

H_XSCOMP 5.5/20 mils

+VCCP

R414 221Ohm 1% r0402

H_XSWING 12/20mils

R413 100Ohm 1% r0402 — C398 0.1UF c0402 — C399 10uF/10V c0805 — GND

H_YRCOMP 12/20mils

R433 24.9Ohm 1% — GND

+VCCP

R420 54.9Ohm 1%

H_YSCOMP 5.5/20 mils

+VCCP

R429 221Ohm 1% r0402

H_YSWING 12/20mils

R430 100Ohm 1% r0402 — C405 0.1UF c0402 — C409 10uF/10V c0805 — GND

3 H_D#[0..63]

U36D — HOST — ALVISO_BGA1257

H_D#0	E4	HD0#	
H_D#1	E1	HD1#	
H_D#2	F4	HD2#	
H_D#3	H7	HD3#	
H_D#4	F2	HD4#	
H_D#5	F1	HD5#	
H_D#6	E3	HD6#	
H_D#7	D3	HD7#	
H_D#8	K7	HD8#	
H_D#9	F2	HD9#	
H_D#10	J7	HD10#	
H_D#11	J8	HD11#	
H_D#12	H6	HD12#	
H_D#13	F3	HD13#	
H_D#14	K8	HD14#	
H_D#15	H5	HD15#	
H_D#16	H1	HD16#	
H_D#17	H2	HD17#	
H_D#18	K5	HD18#	
H_D#19	K6	HD19#	
H_D#20	J4	HD20#	
H_D#21	G3	HD21#	
H_D#22	H3	HD22#	
H_D#23	J1	HD23#	
H_D#24	L5	HD24#	
H_D#25	K4	HD25#	
H_D#26	J5	HD26#	
H_D#27	P7	HD27#	
H_D#28	L7	HD28#	
H_D#29	J3	HD29#	
H_D#30	P5	HD30#	
H_D#31	L3	HD31#	
H_D#32	U7	HD32#	
H_D#33	V6	HD33#	
H_D#34	R6	HD34#	
H_D#35	R5	HD35#	
H_D#36	P3	HD36#	
H_D#37	T8	HD37#	
H_D#38	R7	HD38#	
H_D#39	R8	HD39#	
H_D#40	U8	HD40#	
H_D#41	R4	HD41#	
H_D#42	T4	HD42#	
H_D#43	T5	HD43#	
H_D#44	R1	HD44#	
H_D#45	T3	HD45#	
H_D#46	V8	HD46#	
H_D#47	U6	HD47#	
H_D#48	W6	HD48#	
H_D#49	U3	HD49#	
H_D#50	V5	HD50#	
H_D#51	W8	HD51#	
H_D#52	W7	HD52#	
H_D#53	U2	HD53#	
H_D#54	U1	HD54#	
H_D#55	Y5	HD55#	
H_D#56	Y2	HD56#	
H_D#57	V4	HD57#	
H_D#58	Y7	HD58#	
H_D#59	W1	HD59#	
H_D#60	W3	HD60#	
H_D#61	Y3	HD61#	
H_D#62	Y6	HD62#	
H_D#63	W2	HD63#	

H_XRCOMP	C1	HXRCOMP	
H_XSCOMP	C2	HXSCOMP	
H_XSWING	D1	HXSWING	
H_YRCOMP	T1	HYRCOMP	
H_YSCOMP	L1	HYSCOMP	
H_YSWING	P1	HYSWING	

		HA3#	G9 — H_A#3
		HA4#	C9 — H_A#4
		HA5#	F9 — H_A#5
		HA6#	B7 — H_A#6
		HA7#	A10 — H_A#7
		HA8#	F9 — H_A#8
		HA9#	D8 — H_A#9
		HA10#	B10 — H_A#10
		HA11#	E10 — H_A#11
		HA12#	G10 — H_A#12
		HA13#	D9 — H_A#13
		HA14#	E11 — H_A#14
		HA15#	F10 — H_A#15
		HA16#	G11 — H_A#16
		HA17#	G13 — H_A#17
		HA18#	C10 — H_A#18
		HA19#	C11 — H_A#19
		HA20#	D11 — H_A#20
		HA21#	C12 — H_A#21
		HA22#	B13 — H_A#22
		HA23#	A12 — H_A#23
		HA24#	F12 — H_A#24
		HA25#	G12 — H_A#25
		HA26#	E12 — H_A#26
		HA27#	C13 — H_A#27
		HA28#	B11 — H_A#28
		HA29#	D13 — H_A#29
		HA30#	A13 — H_A#30
		HA31#	F13 — H_A#31

H_A#[31..3] 3

		HADS#	F8 — H_ADS# — H_ADS# 3
		HADSTB0#	B9 — H_ADSTB#0 — H_ADSTB#0 3
		HADSTB1#	E13 — H_ADSTB#1 — H_ADSTB#1 3
		HVREF	J11 — H_VREF
		HBNR#	A5 — H_BNR# — H_BNR# 3
		HBPR#	D5 — H_BPRI# — H_BPRI# 3
		HBREQ0#	E7 — H_BREQ#0 — H_BRQ# 3
		HCPURST#	H10 — H_CPURST# — H_CPURST# 3
		HCLKINN	AB1 — CLK_MCH_BCLK# 20
		HCLKINP	AB2 — CLK_MCH_BCLK 20
		HDBSY#	C6 — H_DBSY# 3
		HDEFER#	E6 — H_DEFER# 3
		HDINV0#	H8 — H_DINV#0 — H_DINV#0 3
		HDINV1#	K3 — H_DINV#1 — H_DINV#1 3
		HDINV2#	T7 — H_DINV#2 — H_DINV#2 3
		HDINV3#	U5 — H_DINV#3 — H_DINV#3 3
		HDPWR#	G6 — H_DPWR# 3
		HDRDY#	F7 — H_DRDY# 3
		HDSTBN0#	G4 — H_DSTBN#0 — H_DSTBN#0 3
		HDSTBN1#	K1 — H_DSTBN#1 — H_DSTBN#1 3
		HDSTBN2#	R3 — H_DSTBN#2 — H_DSTBN#2 3
		HDSTBN3#	V3 — H_DSTBN#3 — H_DSTBN#3 3
		HDSTBP0#	G5 — H_DSTBP#0 — H_DSTBP#0 3
		HDSTBP1#	K2 — H_DSTBP#1 — H_DSTBP#1 3
		HDSTBP2#	R2 — H_DSTBP#2 — H_DSTBP#2 3
		HDSTBP3#	W4 — H_DSTBP#3 — H_DSTBP#3 3
		HEDRDY#	F6 — TP_H_EDRDY# — 1 T35 TPC28t
		HHIT#	D4 — H_HIT# — H_HIT# 3
		HHITM#	D6 — H_HITM# — H_HITM# 3
		HLOCK#	B3 — H_LOCK# 3
		HPCREQ#	A11 — TP_H_PCREQ# — 1 T199 TPC28t
		HREQ0#	A7 — H_REQ#0
		HREQ1#	D7 — H_REQ#1
		HREQ2#	B8 — H_REQ#2
		HREQ3#	C7 — H_REQ#3
		HREQ4#	A8 — H_REQ#4 — H_REQ#[4..0] 3
		HRS0#	A4 — H_RS#0
		HRS1#	C5 — H_RS#1
		HRS2#	B4 — H_RS#2 — H_RS#[0..2] 3
		HCPUSLP#	G8 — R42 1 2 0Ohm r0402 — H_CPUSLP# 3,12
		HTRDY#	B5 — H_TRDY# 3

+VCCP

R74 100Ohm 1% r0402 <500 mil (55 Ohm) T/B trace 5.5 , Space 25

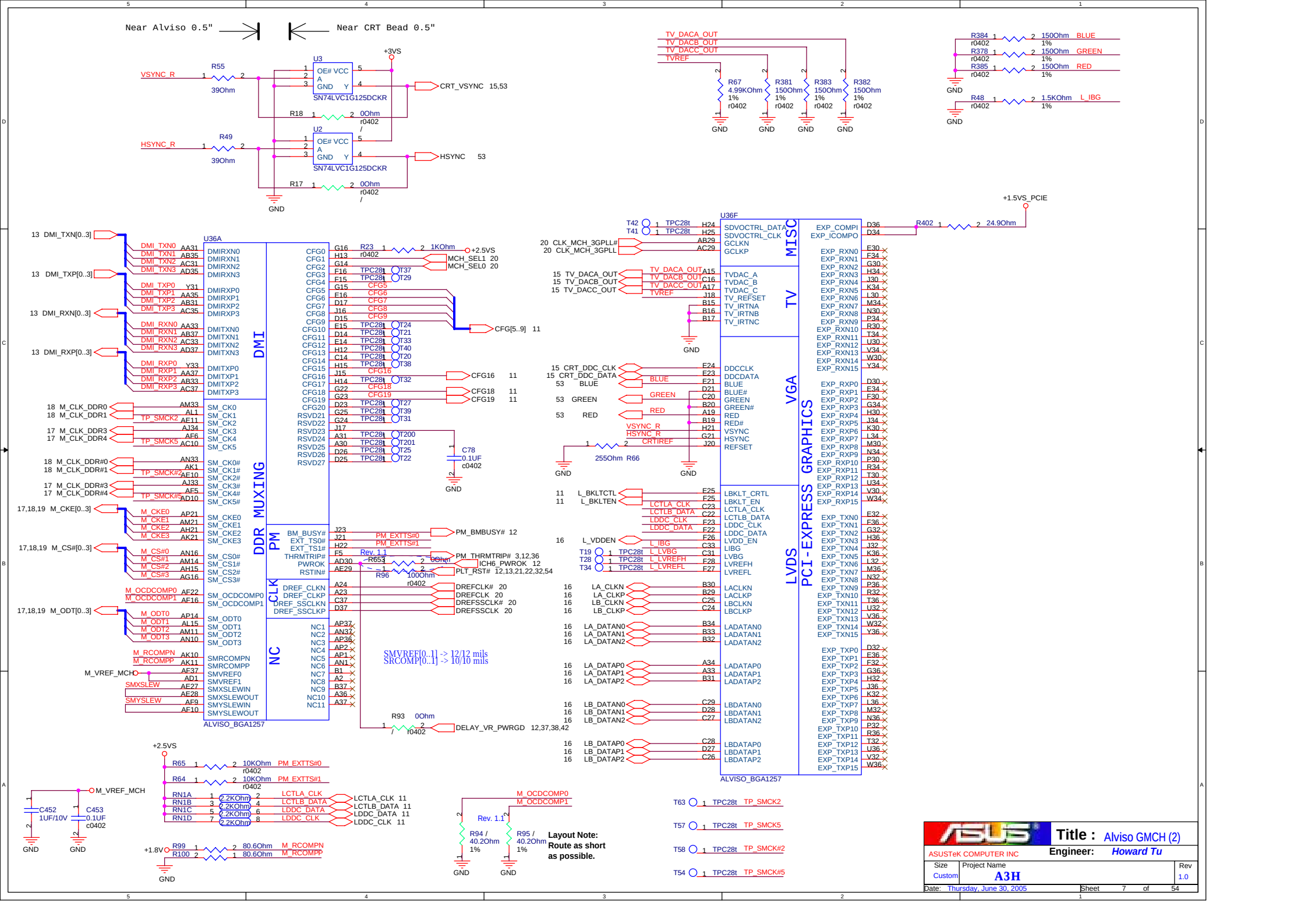
H_VREF

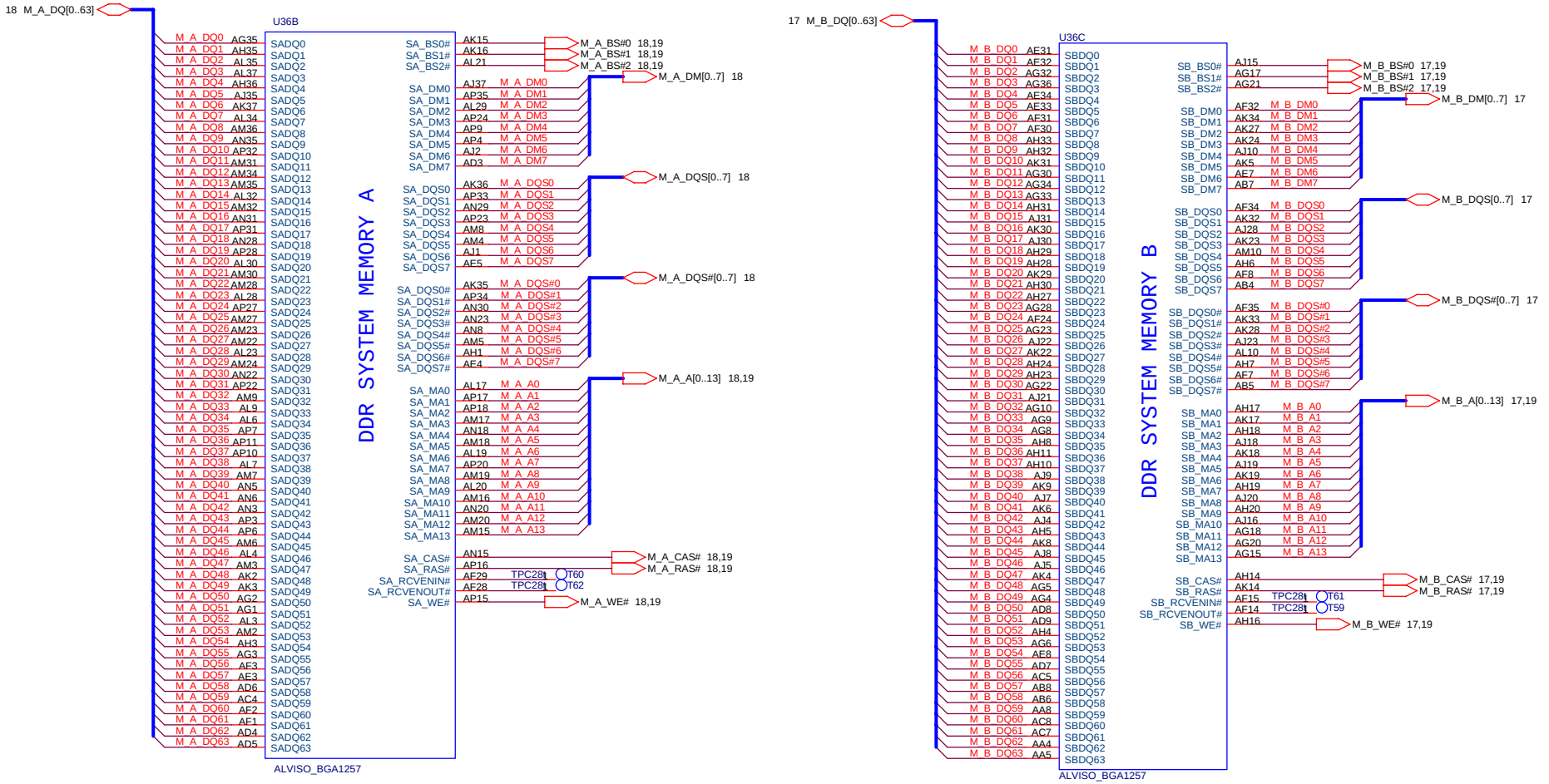
R70 200Ohm r0402 1% — GND

C77 0.1UF c0402 — GND

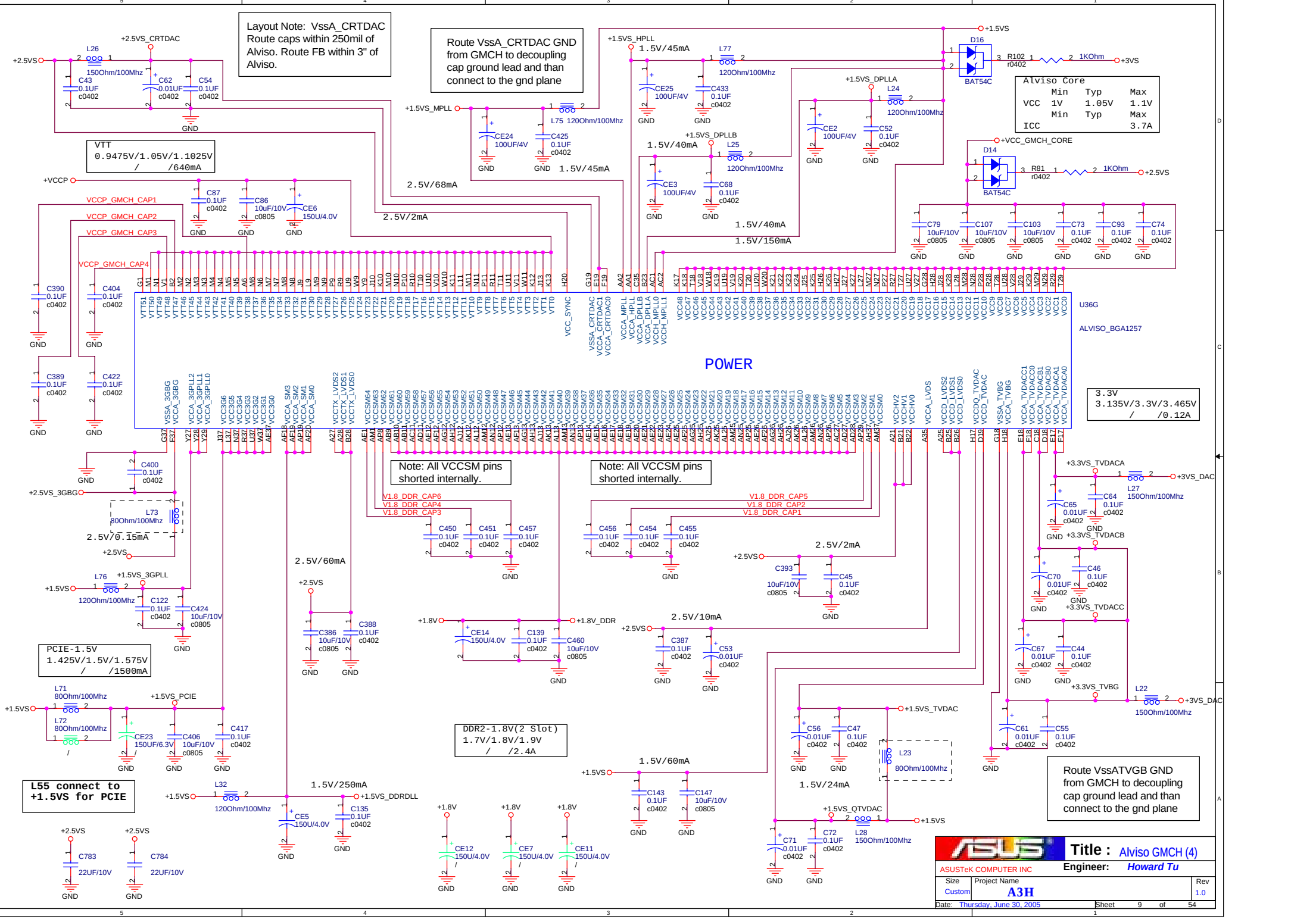
Dothan A : R282 NO STUFF

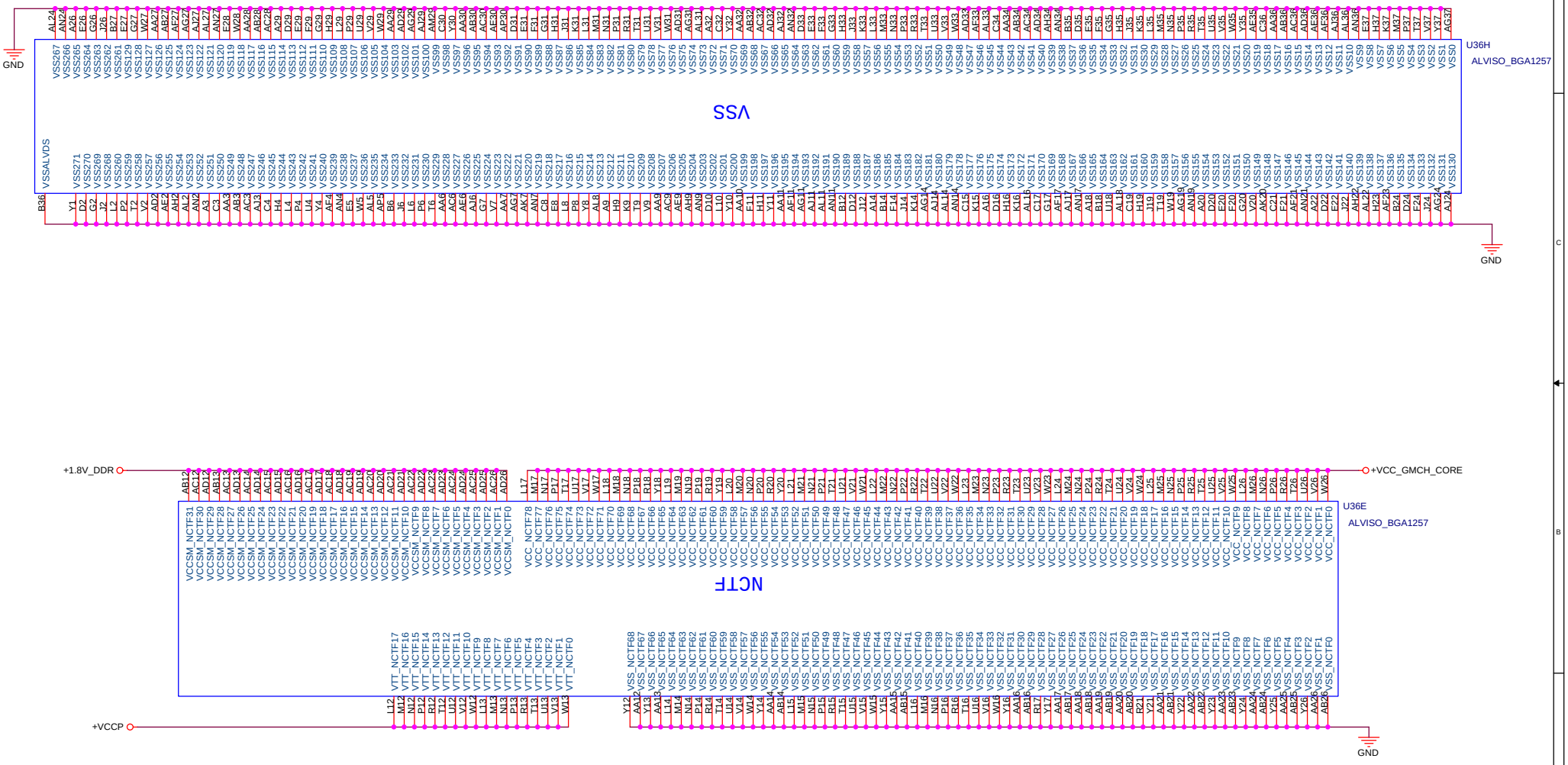
Title : Alviso GMCH (1)		
ASUSTeK COMPUTER INC	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 6 of 54	


Near Alviso 0.5"
Near CRT Bead 0.5"
U3
SN74LVC1G125DCKR
U2
SN74LVC1G125DCKR
+3VS
VSYNC_R
HSYNC_R
R55
R49
R18
R17
39Ohm
0Ohm
r0402
CRT_VSYNC 15,53
HSYNC 53
GND
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TVREF
R67 4.99KOhm 1% r0402
R381 150Ohm 1% r0402
R383 150Ohm 1% r0402
R382 150Ohm 1% r0402
R384 150Ohm 1% BLUE
R378 150Ohm 1% GREEN
R385 150Ohm 1% RED
R48 1.5KOhm 1% L_IBG
U36A
DMI
DDR MUXING
PM
CLK
NC
ALVISO_BGA1257
DMI_TXN[0..3]
DMI_TXP[0..3]
DMI_RXN[0..3]
DMI_RXP[0..3]
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR3
M_CLK_DDR4
M_CLK_DDR#0
M_CLK_DDR#1
M_CLK_DDR#3
M_CLK_DDR#4
M_CKE[0..3]
M_CS#[0..3]
M_ODT[0..3]
M_OCDCOMP0
M_OCDCOMP1
M_RCOMPN
M_RCOMPP
M_VREF_MCH
SMXSLEW
SMYSLEW
TP_SMCK2
TP_SMCK5
TP_SMCK#2
TP_SMCK#5
CFG[5..9] 11
CFG16 11
CFG18 11
CFG19 11
C78 0.1UF c0402
PM_BMBUSY# 12
PM_THRMTRIP# 3,12,36
ICH6_PWROK 12
PLT_RST# 12,13,21,22,32,54
DREFCLK# 20
DREFCLK 20
DREFSSCLK# 20
DREFSSCLK 20
DELAY_VR_PWRGD 12,37,38,42
SMVREF[0..1] -> 12/12 mils
SRCOMP[0..1] -> 10/10 mils
U36F
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
ALVISO_BGA1257
+1.5VS_PCIE
R402 24.9Ohm
CLK_MCH_3GPLL#
CLK_MCH_3GPLL
CRT_DDC_CLK
CRT_DDC_DATA
BLUE
GREEN
RED
VSYNC_R
HSYNC_R
CRTIREF
255Ohm R66
L_BKLTCTL
L_BKLTEN
L_VDDEN
L_IBG
L_LVBG
L_LVREFH
L_LVREFL
LCTLA_CLK
LCTLB_DATA
LDDC_CLK
LDDC_DATA
LA_CLKN
LA_CLKP
LB_CLKN
LB_CLKP
LA_DATAN0
LA_DATAN1
LA_DATAN2
LA_DATAP0
LA_DATAP1
LA_DATAP2
LB_DATAN0
LB_DATAN1
LB_DATAN2
LB_DATAP0
LB_DATAP1
LB_DATAP2
+2.5VS
R65 10KOhm PM_EXTTS#0
R64 10KOhm PM_EXTTS#1
RN1A 2.2KOhm LCTLA_CLK
RN1B 2.2KOhm LCTLB_DATA
RN1C 2.2KOhm LDDC_DATA
RN1D 2.2KOhm LDDC_CLK
C452 1UF/10V
C453 0.1UF c0402
+1.8V
R99 80.6Ohm M_RCOMPN
R100 80.6Ohm M_RCOMPP
R94 / 40.2Ohm 1%
R95 / 40.2Ohm 1%
Rev 1.1
Layout Note: Route as short as possible.
T63 TPC28t TP_SMCK2
T57 TPC28t TP_SMCK5
T58 TPC28t TP_SMCK#2
T54 TPC28t TP_SMCK#5
Title : Alviso GMCH (2)
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size Custom
Project Name A3H
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 7 of 54



ASUSTeK COMPUTER INC	Title : Alviso GMCH (3)	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 8 of 54	


Layout Note: VssA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VssA_CRTDAC GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
Alviso Core
Min Typ Max
VCC 1V 1.05V 1.1V
Min Typ Max
ICC 3.7A
VTT
0.9475V/1.05V/1.1025V
/ /640mA
POWER
ALVISO_BGA1257
U36G
3.3V
3.135V/3.3V/3.465V
/ /0.12A
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
PCIE-1.5V
1.425V/1.5V/1.575V
/ /1500mA
DDR2-1.8V(2 Slot)
1.7V/1.8V/1.9V
/ /2.4A
L55 connect to +1.5VS for PCIE
Route VssATVGB GND from GMCH to decoupling cap ground lead and than connect to the gnd plane
Title : Alviso GMCH (4)
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size Custom
Project Name A3H
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 9 of 54

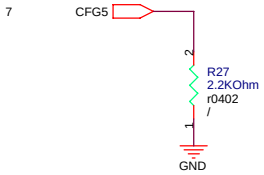


ASUSTeK COMPUTER INC	Title : Alviso GMCH (5)		
	Engineer: Howard Tu		
Size: Custom	Project Name: A3H		Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 10 of 54		

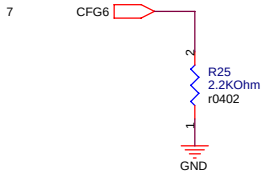
CFG[2:0] are HVCMOS (+2.5VS)
CFG[17..3] have internal pullup resistors. /AGTL+(VCCP)/
CFG[19..18] have internal pulldown resistors./HVCMOS(+2.5VS)/
SDVOCRTL_DATA has internal pulldown resistors.

SDVOCRTL_DATA :
LOW = No SDVO device present (Default)

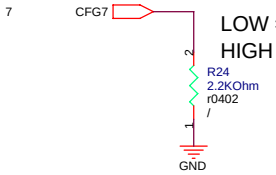
CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)



CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)

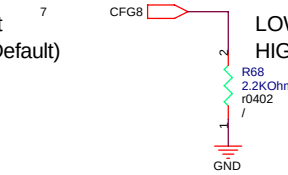


CFG7 : CPU STRAP



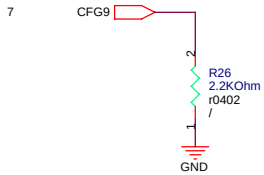
LOW = Mobile Prescott
HIGH = Dothan CPU (Default)

CFG8 : PCI-X POWER Saving

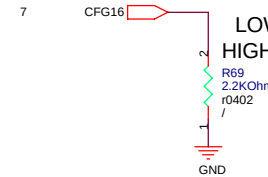


LOW = PCI-X POWER Saving
HIGH (Default)

CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)

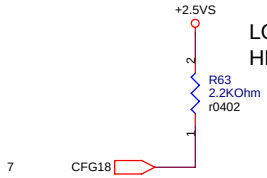


CFG16 : FSB DYNAMIC ODT



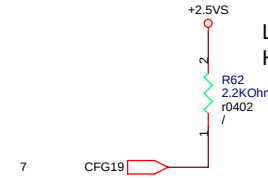
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

CFG18 : VCC SELECT

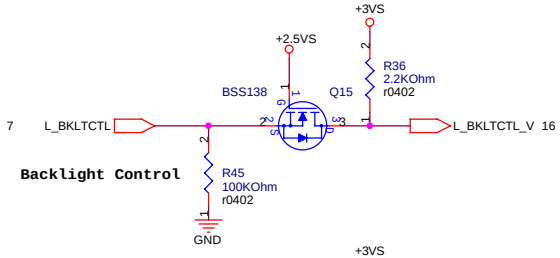


LOW = 1.05V (Default)
HIGH = 1.5V

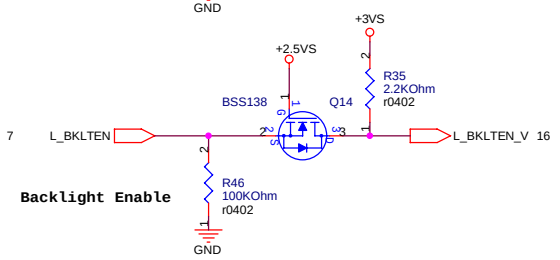
CFG19 : VTT SELECT



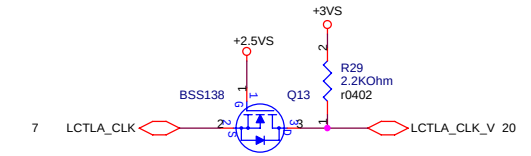
LOW = 1.05V (Default)
HIGH = 1.2V

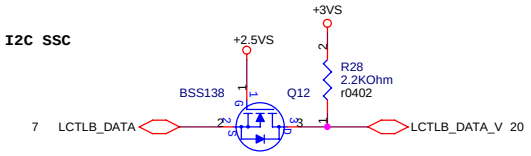


Backlight Control

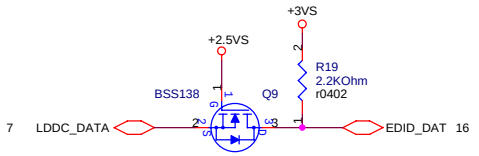


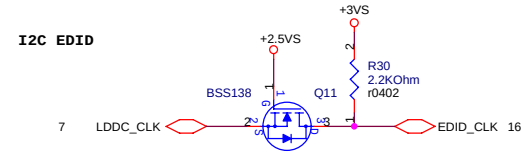
Backlight Enable





I2C SSC





I2C EDID

ASUSTeK COMPUTER INC	Title : GMCH Strapping	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 11 of 54	

Unused SATA pin
- Connect RX, RBIAS, CLK to GND
- Leave TX, LED# as NC

Rev1.2

U20C

U20D

ICH6_M

ICH6_M

INTERNAL PULL-DOWN
PULL-UP : NO REBOOT

PLACE WITHIN 500mils of ICH6 ball

INTERNAL PULL-UP
PULL-DOWN : RESERVED

H_CPUSLP# R193 : B STEP NO STUFF
H_DPRSTP# R231 : A STEP NO STUFF

GPIO21: Program as Output
GPIO23: Program as Output
GPIO27: BT_LED_EN#,+3VSUS
GPIO28: PORTBAR/COM#,+3VSUS
GPIO33: BL_ON,+3VS

Select Port Bar or COM Port

TP_3 INTERNAL PULL-UP
PULL-DOWN : PCI
Express Port chain test

DELAY 18~25ms

BAT HOLDER P/N:
12-201110121
Rev 1.2

RTC BAT P/N: 07-016202032

* 56 within 1" from the ICH6-M pins
* 75 W pull-up to VCCP within 2" from the series resistor

ASUSTeK COMPUTER INC	Title : ICH6_M (1)	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 12 of 54	

PLT_RST#
ICH6,Alviso/KBC/FWH/HDD

U20A

ICH6_M

U20B

ICH6_M

(USB 4 for CAMERA)
(USB 5 for WLAN)

PLACE within 500 mils of ICH.

PLACE within 500 mils of ICH.
5.5mil/8mil

INTERNAL PULL-DOWN SIGNALS :
AC_BITCLK , AC_RST# , AC_SDIN[2:0] , AC_SDOUT , AC_SYNC , DPSLPVR , LAN_CLK , PDD[7] , SDD[7] , PDDREQ , SDDREQ , SPKR , USB[7:0][P,N]

INTERNAL PULL-UP SIGNALS :
EE_DIN , EE_DOUT , GNT[B:A]# , GNT[5]# , GPIO[17:16] , LAD[3:0]# , LDRQ[1:0] , LAN_RXD[2:0] , PME# , PWRBTN#

Rev. 1.1
Change value form 8.2K to 100K

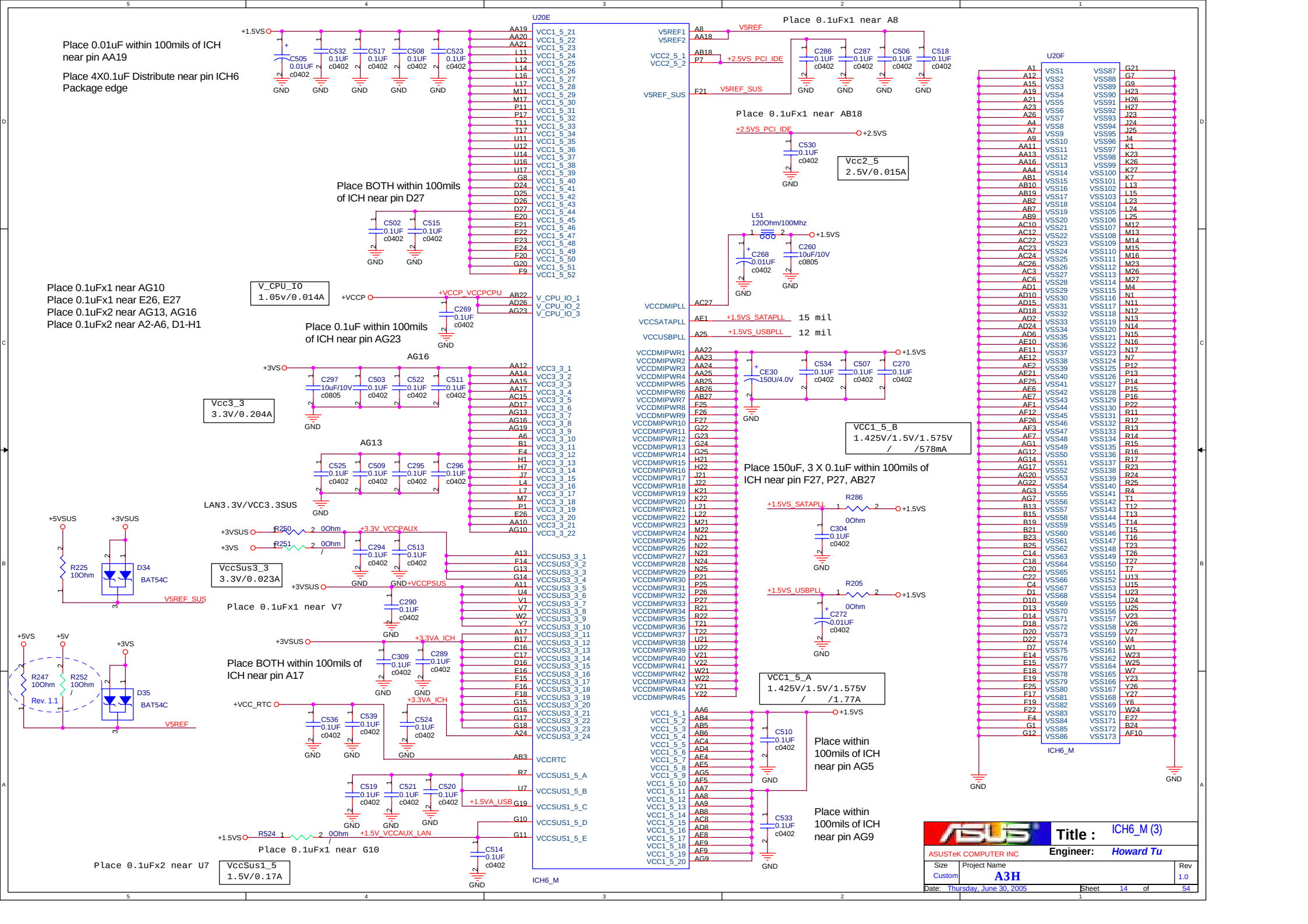
PCB_VID	0	1	2
A3H	0	0	0
A3A	0	0	1

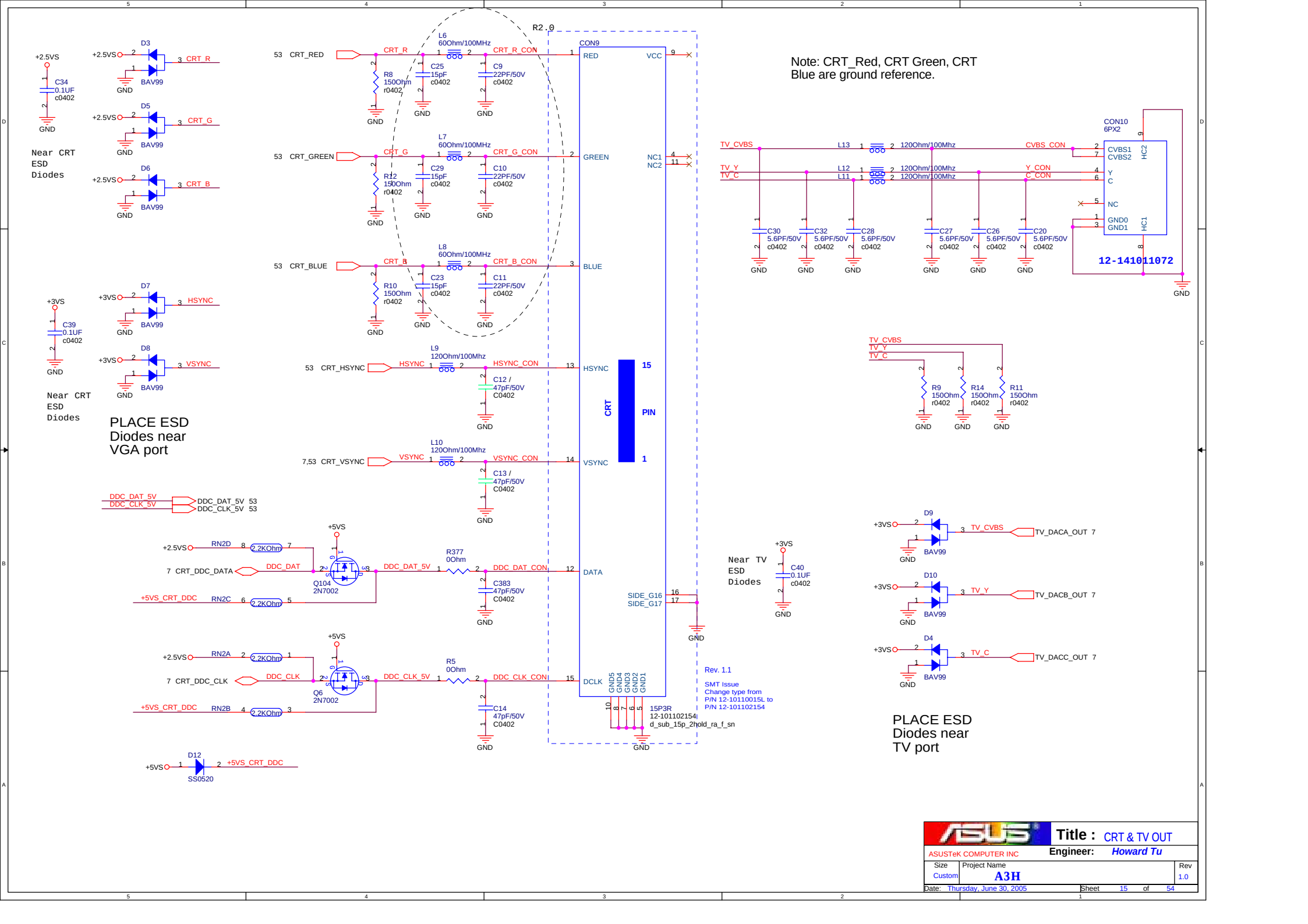
INTERNAL PULL-UP
PULL-DOWN : Boot BIOS destination select

INTERNAL PULL-UP
PULL-DOWN :TOP-BLOCK SWAP

R1.2

Title :	ICH6_M (2)
ASUSTeK COMPUTER INC	Engineer: Howard Tu
Size: Custom	Project Name: A3H
Rev: 1.0	
Date: Thursday, June 30, 2005	Sheet 13 of 54


Place 0.01uF within 100mils of ICH near pin AA19
Place 4X0.1uF Distribute near pin ICH6 Package edge
Place BOTH within 100mils of ICH near pin D27
Place 0.1uFx1 near AG10
Place 0.1uFx1 near E26, E27
Place 0.1uFx2 near AG13, AG16
Place 0.1uFx2 near A2-A6, D1-H1
V_CPU_IO 1.05v/0.014A
Place 0.1uF within 100mils of ICH near pin AG23
AG16
Vcc3_3 3.3V/0.204A
AG13
LAN3.3V/VCC3.3SUS
VccSus3_3 3.3V/0.023A
Place 0.1uFx1 near V7
Place BOTH within 100mils of ICH near pin A17
Place 0.1uFx1 near G10
Place 0.1uFx2 near U7
VccSus1_5 1.5V/0.17A
Place 0.1uFx1 near A8
Place 0.1uFx1 near AB18
Vcc2_5 2.5V/0.015A
15 mil
12 mil
VCC1_5_B 1.425V/1.5V/1.575V / /578mA
Place 150uF, 3 X 0.1uF within 100mils of ICH near pin F27, P27, AB27
VCC1_5_A 1.425V/1.5V/1.575V / /1.77A
Place within 100mils of ICH near pin AG5
Place within 100mils of ICH near pin AG9
U20E
U20F
ICH6_M
Title : ICH6_M (3)
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size Custom
Project Name A3H
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 14 of 54

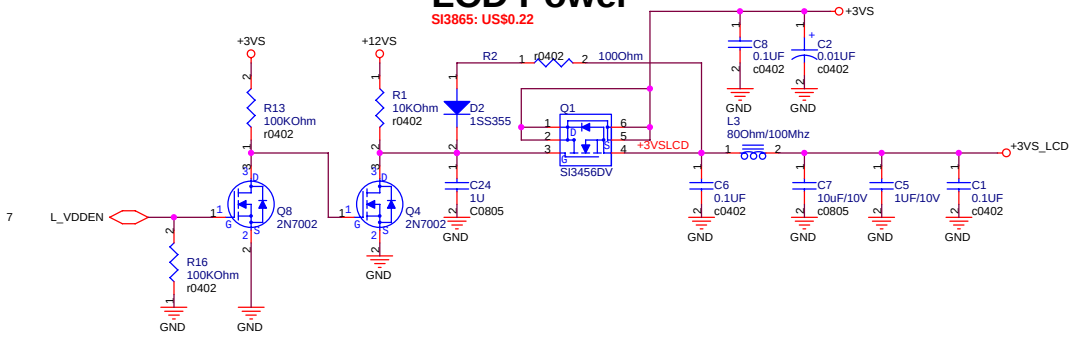

R2.0
CON9
RED
GREEN
BLUE
HSYNC
VSYNC
DCLK
VCC
NC1
NC2
DATA
SIDE_G16
SIDE_G17
CRT
15
PIN
1
CRT_R
CRT_G
CRT_B
CRT_HSYNC
CRT_VSYNC
CRT_DDC_DATA
CRT_DDC_CLK
L6 60Ohm/100MHz
L7 60Ohm/100MHz
L8 60Ohm/100MHz
L9 120Ohm/100Mhz
L10 120Ohm/100Mhz
R8 150Ohm r0402
R12 150Ohm r0402
R10 150Ohm r0402
C25 15pF c0402
C29 15pF c0402
C23 15pF c0402
C9 22PF/50V c0402
C10 22PF/50V c0402
C11 22PF/50V c0402
C12 / 47pF/50V C0402
C13 / 47pF/50V C0402
C34 0.1UF c0402
C39 0.1UF c0402
D3
D5
D6
D7
D8
BAV99
Near CRT ESD Diodes
PLACE ESD Diodes near VGA port
DDC_DAT_5V
DDC_CLK_5V
RN2D 2.2KOhm
RN2C 2.2KOhm
RN2A 2.2KOhm
RN2B 2.2KOhm
Q104 2N7002
Q6 2N7002
R377 0Ohm
R5 0Ohm
C383 47pF/50V C0402
C14 47pF/50V C0402
+5VS_CRT_DDC
D12
SS0520
15P3R 12-101102154
d_sub_15p_2hold_ra_f_sn
Rev. 1.1
SMT Issue
Change type from P/N 12-10110015L to P/N 12-101102154
Note: CRT_Red, CRT Green, CRT Blue are ground reference.
TV_CVBS
TV_Y
TV_C
L13 120Ohm/100Mhz
L12 120Ohm/100Mhz
L11 120Ohm/100Mhz
CVBS_CON
Y_CON
C_CON
CON10 6PX2
CVBS1
CVBS2
Y
C
NC
GND0
GND1
HC1
HC2
12-141011072
C30 5.6PF/50V c0402
C32 5.6PF/50V c0402
C28 5.6PF/50V c0402
C27 5.6PF/50V c0402
C26 5.6PF/50V c0402
C20 5.6PF/50V c0402
R9 150Ohm r0402
R14 150Ohm r0402
R11 150Ohm r0402
C40 0.1UF c0402
Near TV ESD Diodes
D9
D10
D4
TV_CVBS
TV_Y
TV_C
TV_DACA_OUT 7
TV_DACB_OUT 7
TV_DACC_OUT 7
PLACE ESD Diodes near TV port
Title : CRT & TV OUT
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size Custom
Project Name A3H
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 15 of 54

LCD Backlight Control

3V-3.6V
Full Active: 410 mA(Max. 500 mA)
3-3.6V
S0-S1M:410 mA(500 mA Max.)

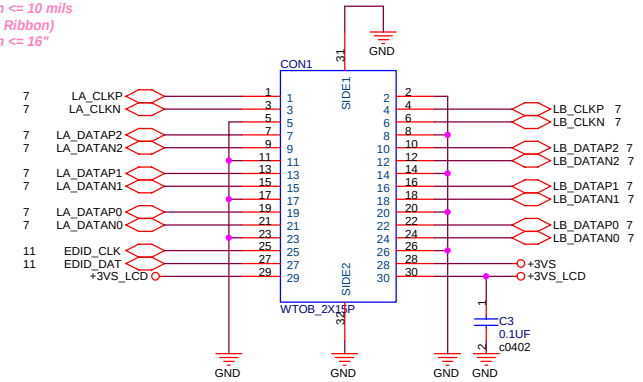
LCD Power

SI3865: US$0.22

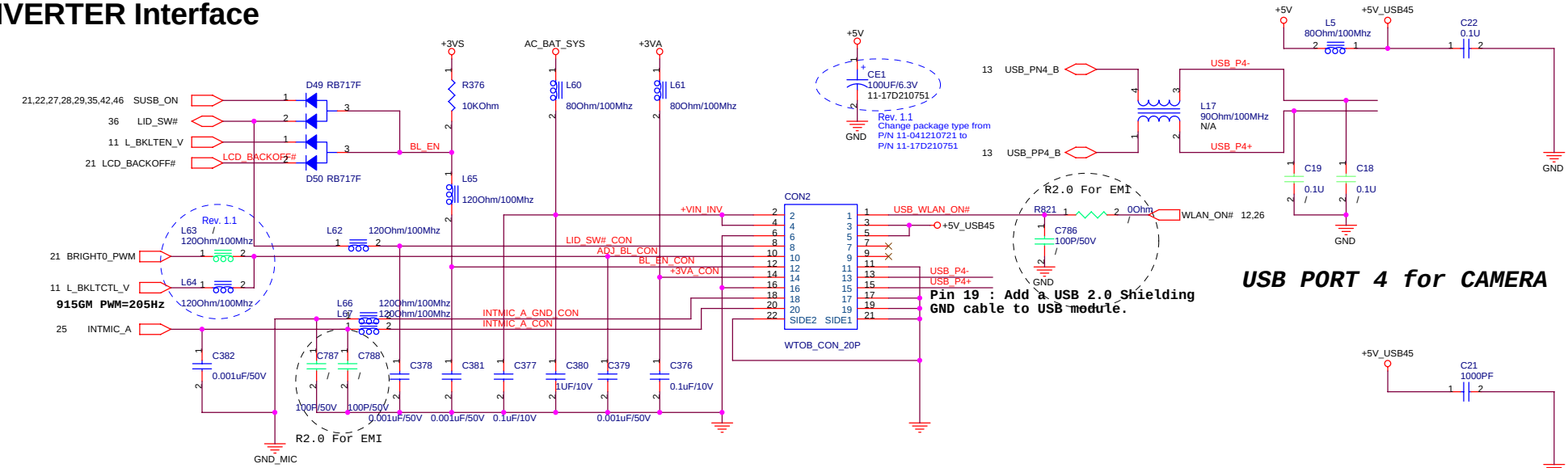


Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface



INVERTER Interface

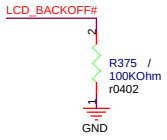


Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.

USB PORT 4 for CAMERA

BIOS ADJ_BL: KBC output D/A signal (adjust voltage level) to adjust Back light.

BIOS BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



700Vrms@5 mArms
(Min. 3 mArms)6 mArms(Max. 6.5 mArms)

A3H/A3A don't use USB PORT 5 for WLAN

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 16 of 54	

For crosstalk

Change to PN:12-02512200B

M_CLK_DDR3
C486 10PF PLACE NEAR SO-DIMM_0 c0402
M_CLK_DDR#3
M_CLK_DDR4
C487 10PF PLACE NEAR SO-DIMM_0 c0402
M_CLK_DDR#4

8,19 M_B_A[0..13]
M_B_BS#2
M_B_BS#0
M_B_BS#1
M_CS#2
M_CS#3
M_CLK_DDR3
M_CLK_DDR#3
M_CLK_DDR4
M_CLK_DDR#4
M_CKE2
M_CKE3
M_B_CAS#
M_B_RAS#
M_B_WE#
R513 10KOhm r0402
+3VS
R512 10KOhm r0402
GND
12,18,20 SMB_CLK_S
12,18,20 SMB_DAT_S
M_ODT2
M_ODT3
8 M_B_DM[0..7]
8 M_B_DQS[0..7]
8 M_B_DQS#[0..7]

CON15A

M_B_A0	102	A0	DQ0 5 M_B_DQ4
M_B_A1	101	A1	DQ1 7 M_B_DQ5
M_B_A2	100	A2	DQ2 17 M_B_DQ7
M_B_A3	99	A3	DQ3 19 M_B_DQ6
M_B_A4	98	A4	DQ4 4 M_B_DQ1
M_B_A5	97	A5	DQ5 6 M_B_DQ0
M_B_A6	94	A6	DQ6 14 M_B_DQ2
M_B_A7	92	A7	DQ7 16 M_B_DQ3
M_B_A8	93	A8	DQ8 23 M_B_DQ13
M_B_A9	91	A9	DQ9 25 M_B_DQ8
M_B_A10	105	A10/AP	DQ10 35 M_B_DQ15
M_B_A11	90	A11	DQ11 37 M_B_DQ14
M_B_A12	89	A12	DQ12 20 M_B_DQ9
M_B_A13	116	A13	DQ13 22 M_B_DQ12
	86	A14	DQ14 36 M_B_DQ10
	84	A15	DQ15 38 M_B_DQ11
	85	A16_BA2	DQ16 43 M_B_DQ21
			DQ17 45 M_B_DQ20
	107	BA0	DQ18 55 M_B_DQ23
	106	BA1	DQ19 57 M_B_DQ19
	110	S0#	DQ20 44 M_B_DQ16
	115	S1#	DQ21 46 M_B_DQ17
	30	CK0	DQ22 56 M_B_DQ18
	32	CK0#	DQ23 58 M_B_DQ22
	164	CK1	DQ24 61 M_B_DQ25
	166	CK1#	DQ25 63 M_B_DQ24
	79	CKE0	DQ26 73 M_B_DQ26
	80	CKE1	DQ27 75 M_B_DQ27
	113	CAS#	DQ28 62 M_B_DQ29
	108	RAS#	DQ29 64 M_B_DQ28
	109	WE#	DQ30 74 M_B_DQ31
	198	SA0	DQ31 76 M_B_DQ30
	200	SA1	DQ32 123 M_B_DQ33
	197	SCL	DQ33 125 M_B_DQ32
	195	SDA	DQ34 135 M_B_DQ34
			DQ35 137 M_B_DQ35
	114	ODT0	DQ36 124 M_B_DQ37
	119	ODT1	DQ37 126 M_B_DQ36
			DQ38 134 M_B_DQ38
M_B_DM0	10	DM0	DQ39 136 M_B_DQ39
M_B_DM1	26	DM1	DQ40 141 M_B_DQ45
M_B_DM2	52	DM2	DQ41 143 M_B_DQ44
M_B_DM3	67	DM3	DQ42 151 M_B_DQ47
M_B_DM4	130	DM4	DQ43 153 M_B_DQ46
M_B_DM5	147	DM5	DQ44 140 M_B_DQ40
M_B_DM6	170	DM6	DQ45 142 M_B_DQ41
M_B_DM7	185	DM7	DQ46 152 M_B_DQ42
			DQ47 154 M_B_DQ43
M_B_DQS0	13	DQS0	DQ48 157 M_B_DQ48
M_B_DQS1	31	DQS1	DQ49 159 M_B_DQ49
M_B_DQS2	51	DQS2	DQ50 173 M_B_DQ50
M_B_DQS3	70	DQS3	DQ51 175 M_B_DQ55
M_B_DQS4	131	DQS4	DQ52 158 M_B_DQ52
M_B_DQS5	148	DQS5	DQ53 160 M_B_DQ53
M_B_DQS6	169	DQS6	DQ54 174 M_B_DQ51
M_B_DQS7	188	DQS7	DQ55 176 M_B_DQ54
M_B_DQS#0	11	DQS#0	DQ56 179 M_B_DQ60
M_B_DQS#1	29	DQS#1	DQ57 181 M_B_DQ57
M_B_DQS#2	49	DQS#2	DQ58 189 M_B_DQ63
M_B_DQS#3	68	DQS#3	DQ59 191 M_B_DQ58
M_B_DQS#4	129	DQS#4	DQ60 180 M_B_DQ61
M_B_DQS#5	146	DQS#5	DQ61 182 M_B_DQ56
M_B_DQS#6	167	DQS#6	DQ62 192 M_B_DQ59
M_B_DQS#7	186	DQS#7	DQ63 194 M_B_DQ62

DDR2_DIMM_200P_REV

M_B_DQ[0..63] 8

+1.8V_DIMM
C484 0.1UF c0402
C248 0.1UF c0402
C483 0.1UF c0402
C482 0.1UF c0402
GND

Layout Note: Place these Caps near SO DIMM 0

+1.8V_DIMM
C156 0.1UF c0402
C149 0.1UF c0402
C142 0.1UF c0402
C151 0.1UF c0402
GND

Layout Note: Place these High-Freq decoupling Caps near the GMCH

+1.8V
+1.8V_DIMM
C478 2.2uF/6.3V
C244 2.2uF/6.3V
C243 2.2uF/6.3V
C246 2.2uF/6.3V
C245 2.2uF/6.3V
GND

+1.8V_DIMM
CON15B

112	VDD1	VSS16	18
111	VDD2	VSS17	24
117	VDD3	VSS18	41
96	VDD4	VSS19	53
95	VDD5	VSS20	42
118	VDD6	VSS21	54
81	VDD7	VSS22	59
82	VDD8	VSS23	65
87	VDD9	VSS24	60
103	VDD10	VSS25	66
88	VDD11	VSS26	127
104	VDD12	VSS27	139
		VSS28	128
199	VDDSPD	VSS29	145
		VSS30	165
83	NC1	VSS31	171
120	NC2	VSS32	172
50	NC3	VSS33	177
69	NC4	VSS34	187
163	NCTEST	VSS35	178
		VSS36	190
1	VREF	VSS37	9
		VSS38	21
201	GND0	VSS39	33
202	GND1	VSS40	155
		VSS41	34
203	NP_NC1	VSS42	177
204	NP_NC2	VSS43	144
		VSS44	156
47	VSS1	VSS45	168
133	VSS2	VSS46	2
183	VSS3	VSS47	3
77	VSS4	VSS48	15
12	VSS5	VSS49	27
48	VSS6	VSS50	39
184	VSS7	VSS51	149
78	VSS8	VSS52	161
71	VSS9	VSS53	28
72	VSS10	VSS54	40
121	VSS11	VSS55	138
122	VSS12	VSS56	150
196	VSS13	VSS57	162
193	VSS14		
8	VSS15		

DDR2_DIMM_200P_REV

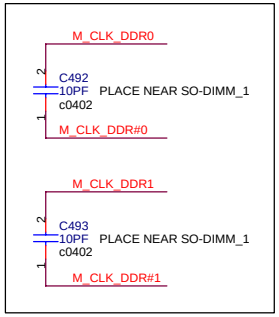
+3VS
C480 0.1UF c0402
C479 0.1UF c0402
GND

VREF -> 10/10 mils
M_VREF_DIMM0
C477 2.2uF/6.3V
C481 0.1UF c0402
GND

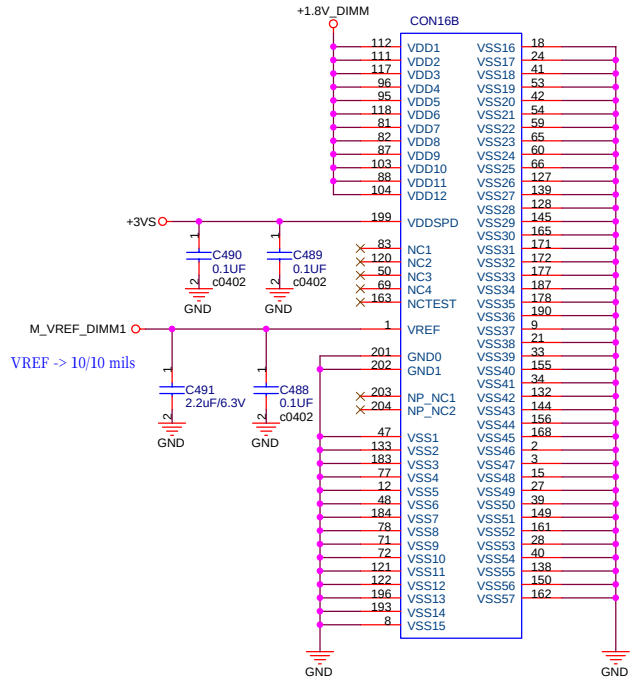
Layout Note: Place these Caps near SO DIMM 0

ASUSTeK COMPUTER INC	Title : DDR2_SO-DIMM_0	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 17 of 54	

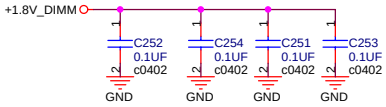
For crosstalk



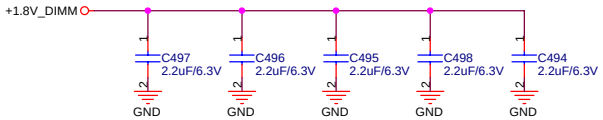
Change to PN:12-02512200A



Layout Note: Place these Caps near SO DIMM 1

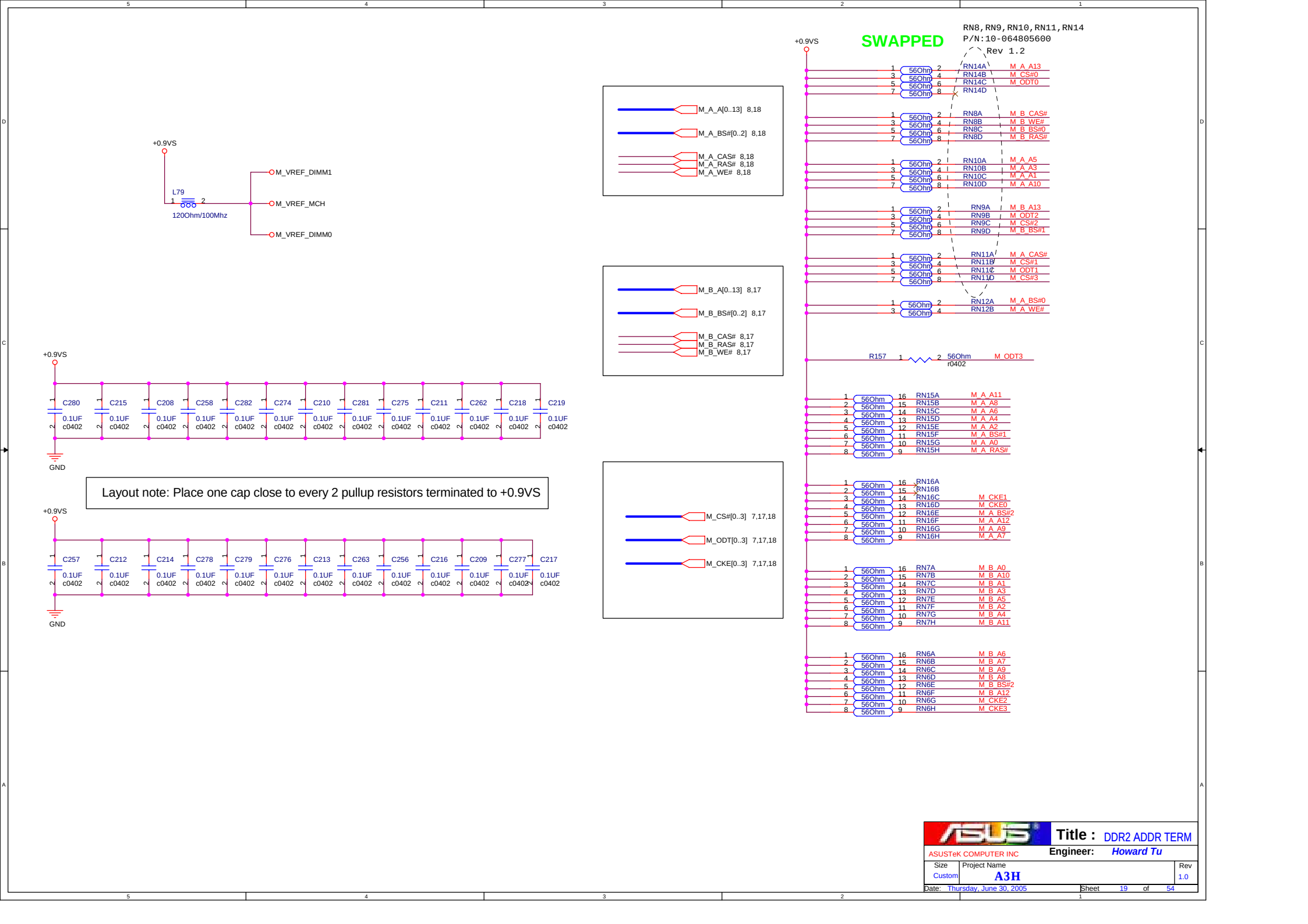


Layout Note: Place these Caps near SO DIMM 1



SO-DIMM 1 is placed father from the GMCH than SO-DIMM 0

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM_1	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 18 of 54	


SWAPPED
RN8,RN9,RN10,RN11,RN14
P/N:10-064805600
Rev 1.2
+0.9VS
L79
120Ohm/100Mhz
M_VREF_DIMM1
M_VREF_MCH
M_VREF_DIMM0
M_A_A[0..13] 8,18
M_A_BS#[0..2] 8,18
M_A_CAS# 8,18
M_A_RAS# 8,18
M_A_WE# 8,18
M_B_A[0..13] 8,17
M_B_BS#[0..2] 8,17
M_B_CAS# 8,17
M_B_RAS# 8,17
M_B_WE# 8,17
M_CS#[0..3] 7,17,18
M_ODT[0..3] 7,17,18
M_CKE[0..3] 7,17,18
RN14A M_A_A13
RN14B M_CS#0
RN14C M_ODT0
RN14D
RN8A M_B_CAS#
RN8B M_B_WE#
RN8C M_B_BS#0
RN8D M_B_RAS#
RN10A M_A_A5
RN10B M_A_A3
RN10C M_A_A1
RN10D M_A_A10
RN9A M_B_A13
RN9B M_ODT2
RN9C M_CS#2
RN9D M_B_BS#1
RN11A M_A_CAS#
RN11B M_CS#1
RN11C M_ODT1
RN11D M_CS#3
RN12A M_A_BS#0
RN12B M_A_WE#
R157 56Ohm M_ODT3
r0402
RN15A M_A_A11
RN15B M_A_A8
RN15C M_A_A6
RN15D M_A_A4
RN15E M_A_A2
RN15F M_A_BS#1
RN15G M_A_A0
RN15H M_A_RAS#
RN16A
RN16B
RN16C M_CKE1
RN16D M_CKE0
RN16E M_A_BS#2
RN16F M_A_A12
RN16G M_A_A9
RN16H M_A_A7
RN7A M_B_A0
RN7B M_B_A10
RN7C M_B_A1
RN7D M_B_A3
RN7E M_B_A5
RN7F M_B_A2
RN7G M_B_A4
RN7H M_B_A11
RN6A M_B_A6
RN6B M_B_A7
RN6C M_B_A9
RN6D M_B_A8
RN6E M_B_BS#2
RN6F M_B_A12
RN6G M_CKE2
RN6H M_CKE3
56Ohm
+0.9VS
C280 C215 C208 C258 C282 C274 C210 C281 C275 C211 C262 C218 C219
C257 C212 C214 C278 C279 C276 C213 C263 C256 C216 C209 C277 C217
0.1UF
c0402
GND
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS
Title : DDR2 ADDR TERM
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size Custom
Project Name A3H
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 19 of 54

SB2	SB1	SB0	CPU	SRC	SATA	PCI
FSLC	FSLB	FSLA	MHz	MHz	MHz	MHz
0	0	0	266.66	108.00	100.00	33.33
0	0	1	133.33	108.00	100.00	33.33
0	1	0	200.00	108.00	100.00	33.33
0	1	1	166.66	108.00	100.00	33.33
1	0	0	333.33	108.00	100.00	33.33
1	0	1	100.00	108.00	100.00	33.33
1	1	0	400.00	108.00	100.00	33.33

No stuff for discrete graphic

PLACE termination close to source IC

DOC_1,DOC_2 -> L:Normal
H:Freq will jump to a preporgramed value in the I2C

R441 10K pull up to +3VS for CPUCLK2_ITP

R442 10K pull down to GND for SRC5

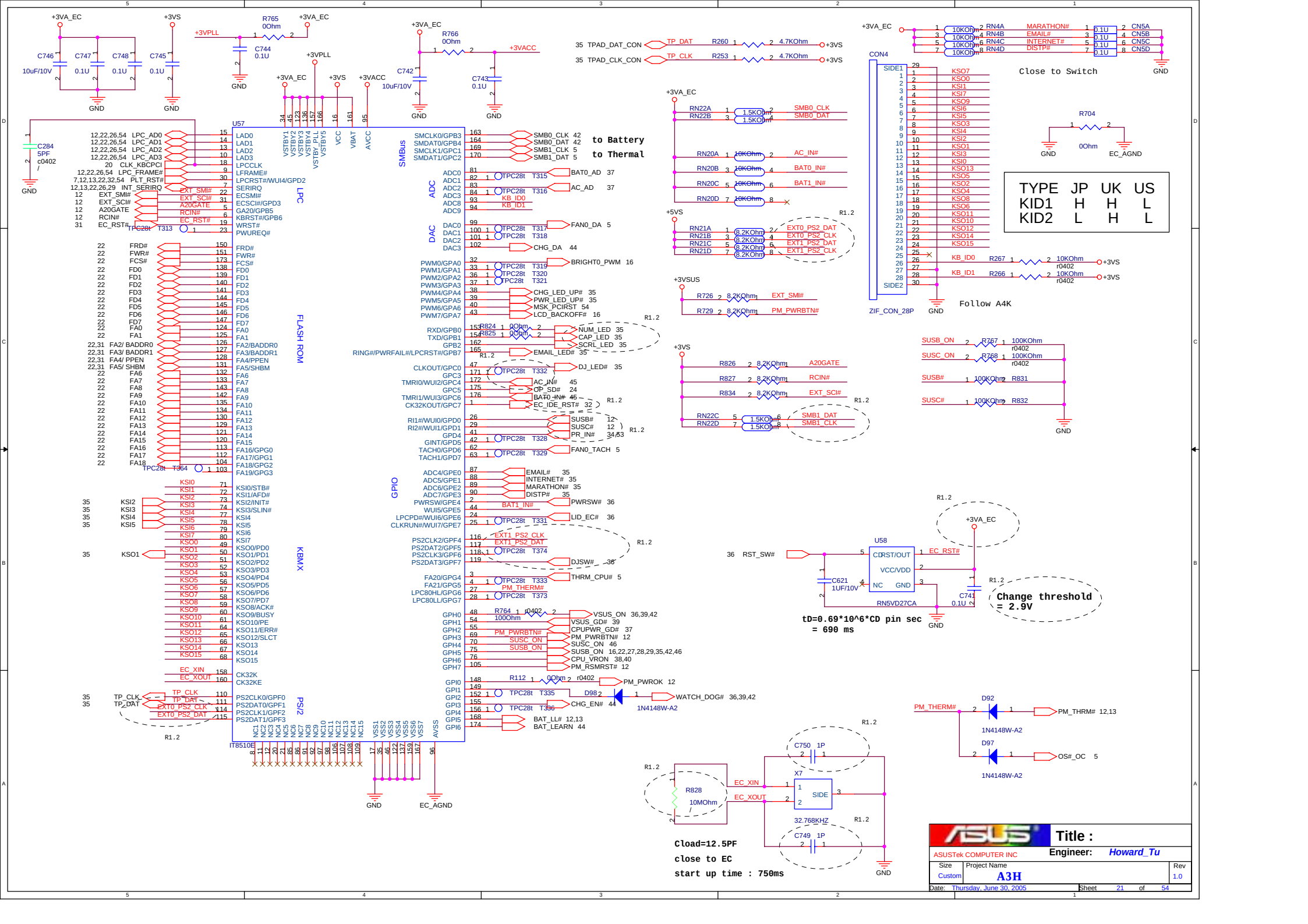
Title : CLOCK GEN

ASUSTeK COMPUTER INC

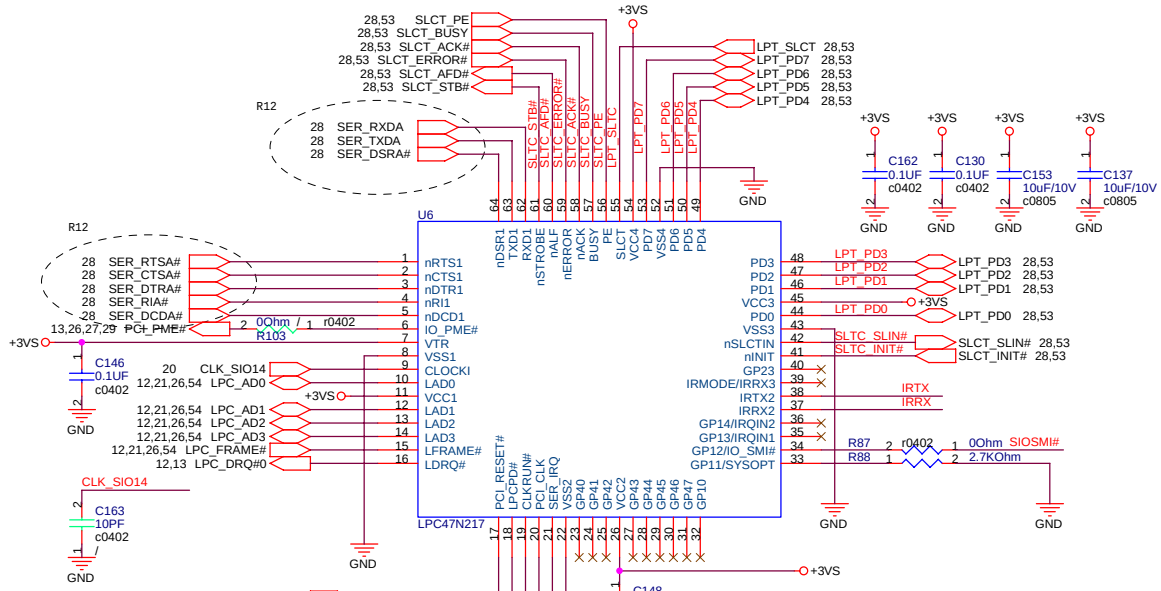
Engineer: Howard Tu

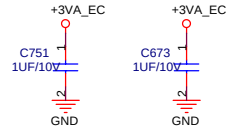
Size	Project Name	Rev
Custom	A3H	1.0

Date: Thursday, June 30, 2005 Sheet 20 of 54


U57
IT8510E
LPC
FLASH ROM
KBMX
PS/2
SMBus
ADC
DAC
GPIO
to Battery
to Thermal
Close to Switch
Follow A4K
Change threshold = 2.9V
tD=0.69*10^6*CD pin sec = 690 ms
Cload=12.5PF
close to EC
start up time : 750ms
TYPE JP UK US
KID1 H H L
KID2 L H L
Title :
ASUSTek COMPUTER INC
Engineer: Howard_Tu
Size Custom
Project Name A3H
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 21 of 54

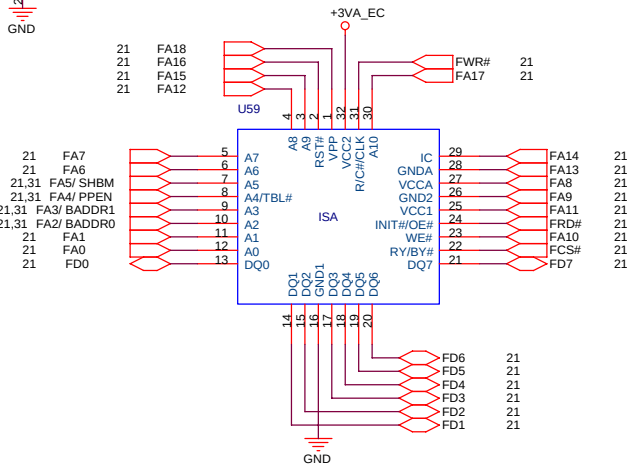
Super I/O

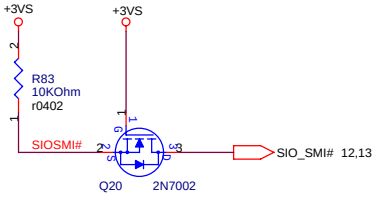




PLCC32 Socket
PN:12-043000321

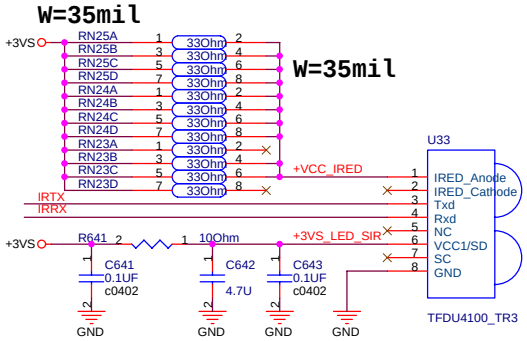
SST-PLCC32 4Mbits Flash ROM
PN:05-001004100(+3.3V)





Keep From Leakage Current

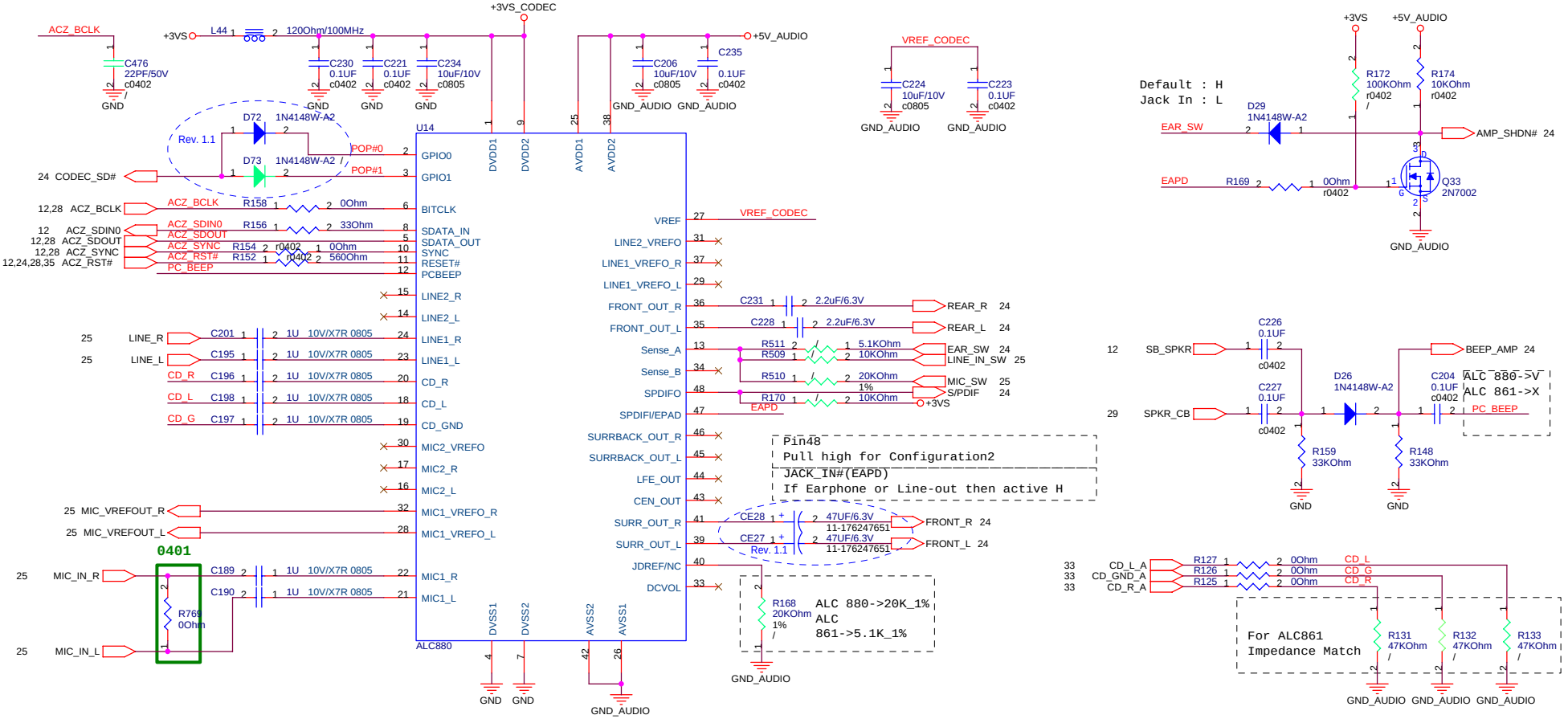
W=35mil

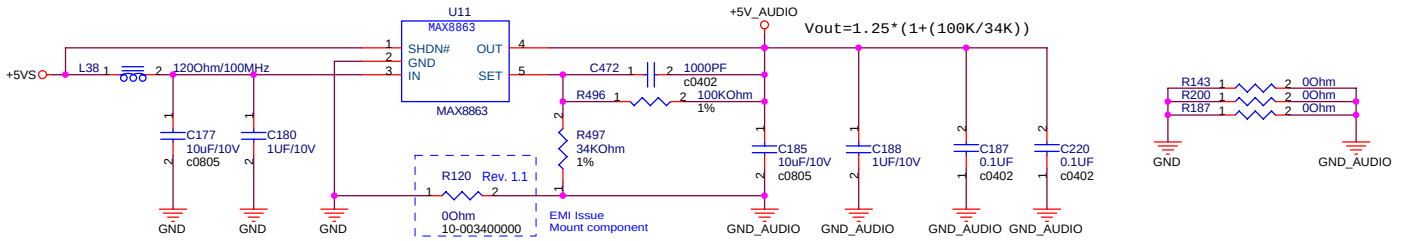


W=35mil

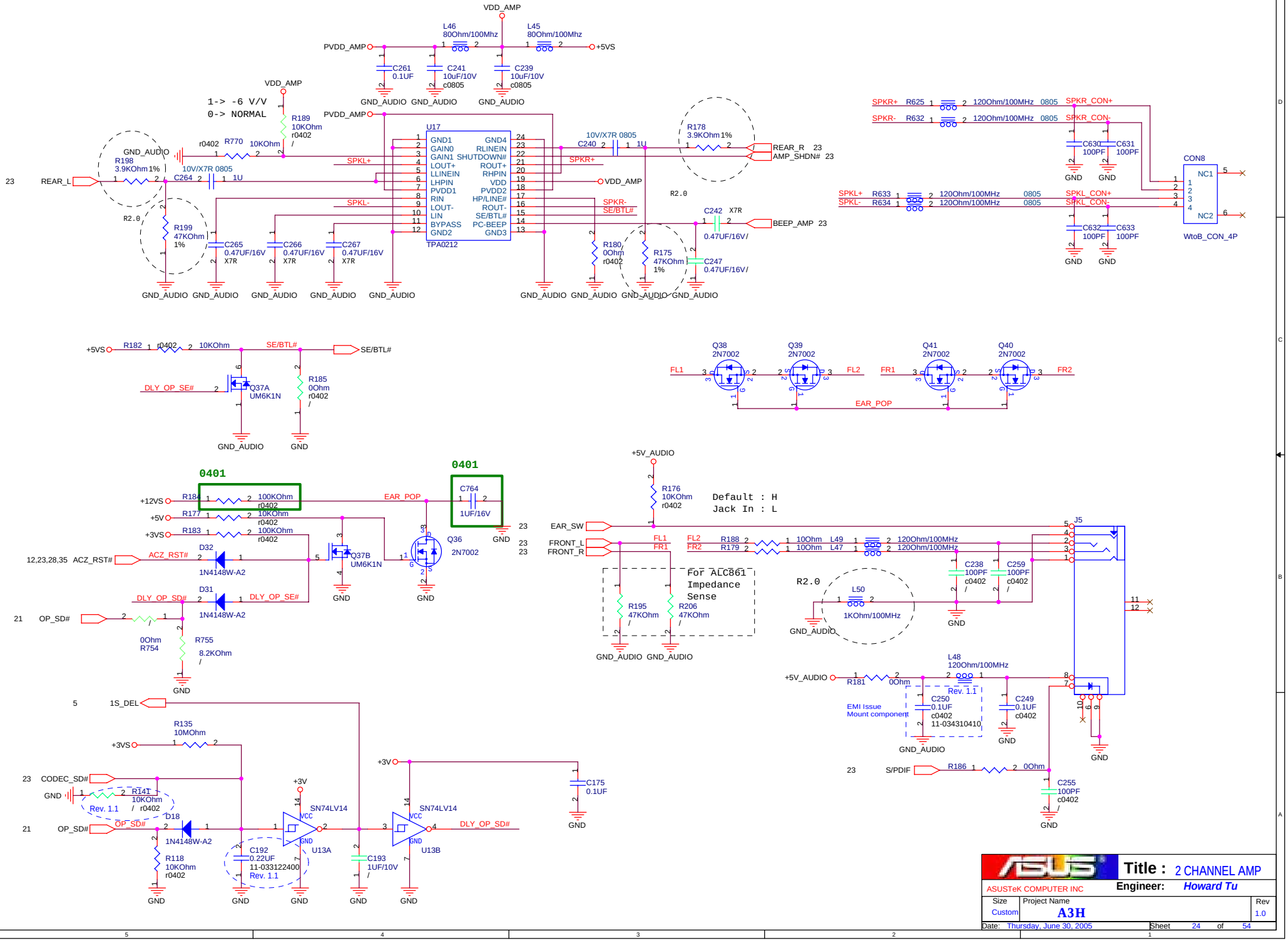
W=20mil

ASUSTeK COMPUTER INC		Title :	FWH / SIO / SIR
		Engineer:	*Howard Tu*
Size: Custom	Project Name: A3H		Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 22 of 54		



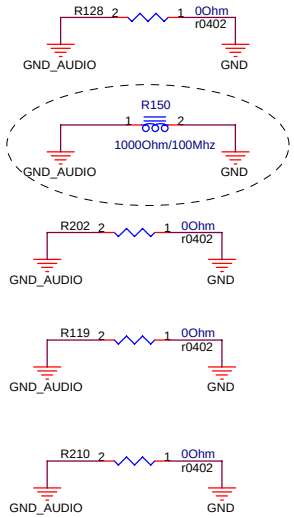


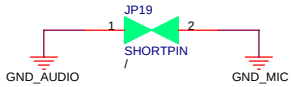
Title : AZALIA		
ASUSTek COMPUTER INC. NB1	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 23 of 54	

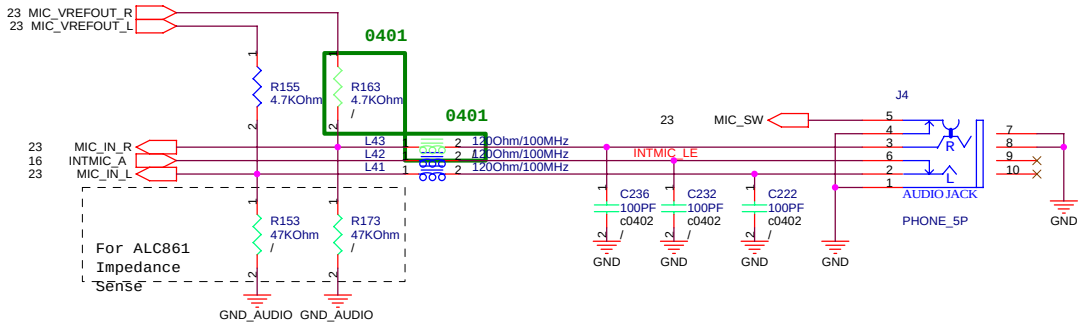


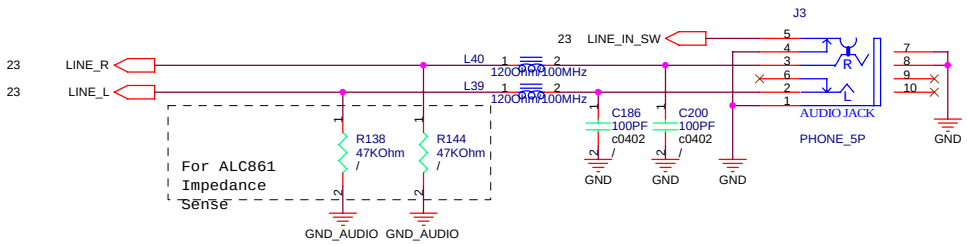
ASUSTeK COMPUTER INC		Title : 2 CHANNEL AMP	
		Engineer: Howard Tu	
Size: Custom	Project Name: A3H		Rev: 1.0
Date: Thursday, June 30, 2005		Sheet 24 of 54	

INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils

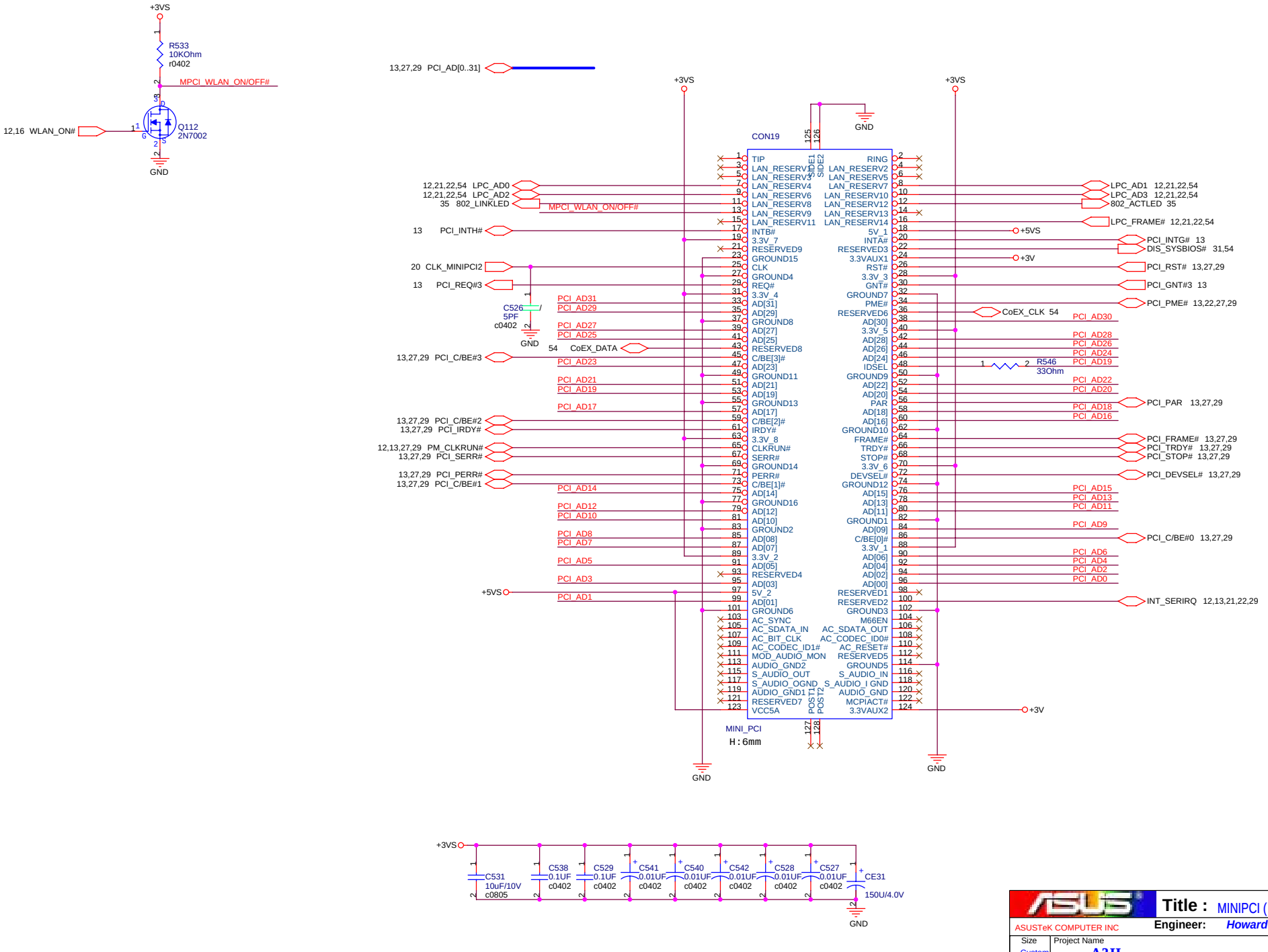




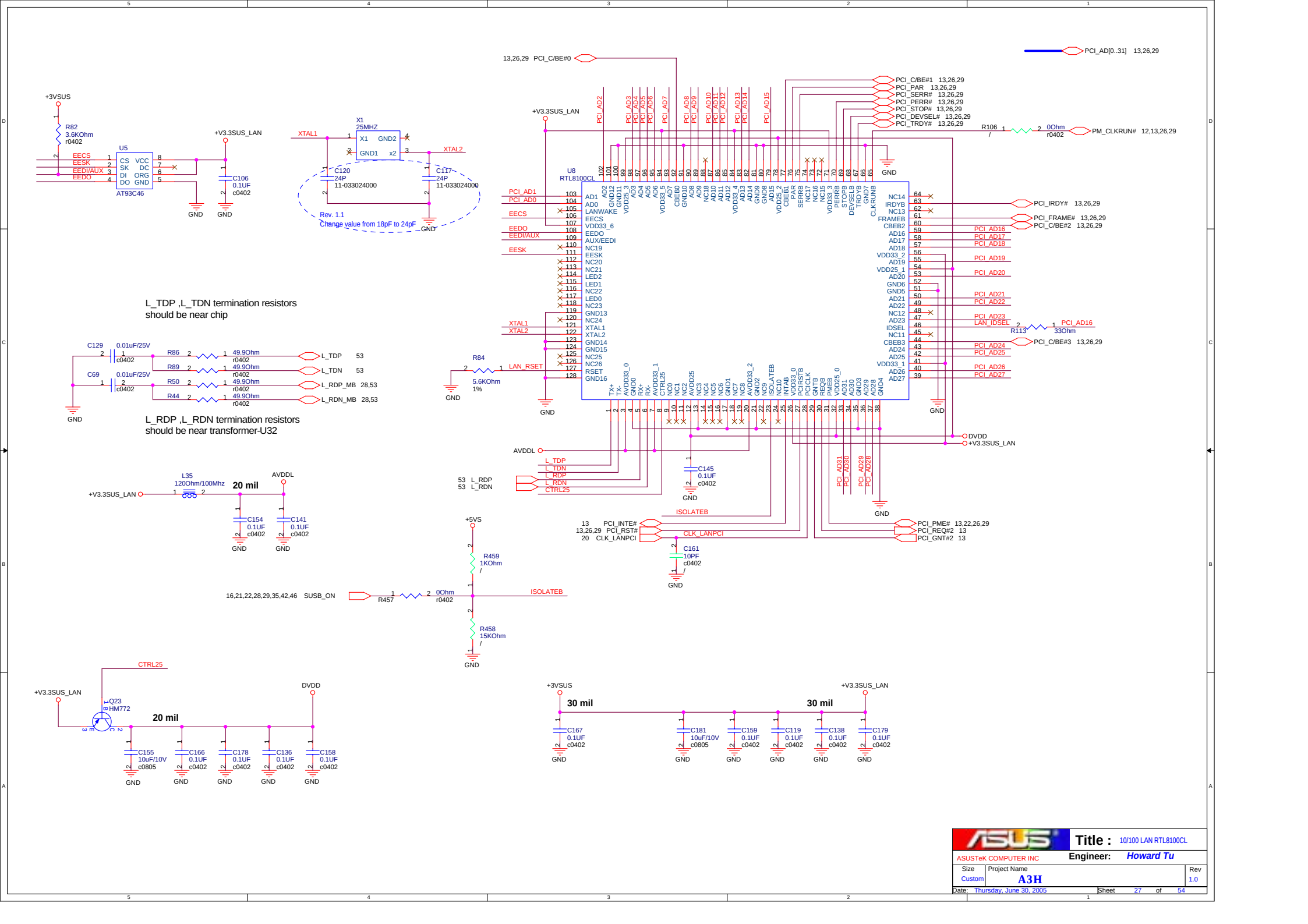




ASUSTeK COMPUTER INC	Title : MIC / Line-IN Jack	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 25 of 54	



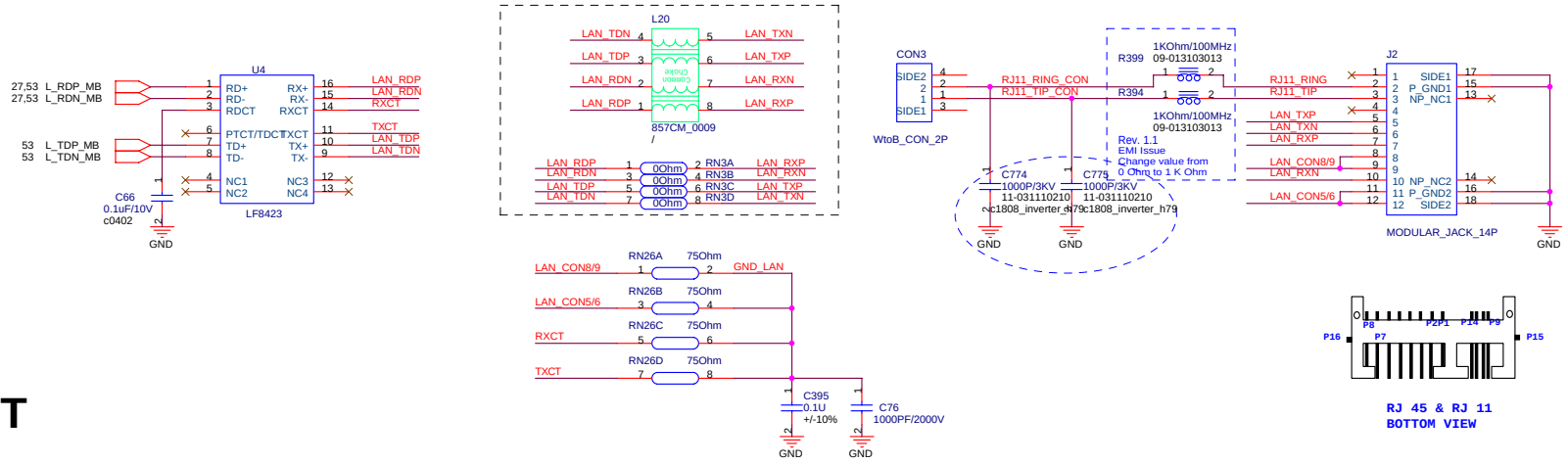
ASUSTeK COMPUTER INC	Title : MINIPCI (802.11)	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 26 of 54	



ASUSTeK COMPUTER INC	Title : 10/100 LAN RTL8100CL		
	Engineer: Howard Tu		
Size: Custom	Project Name: A3H		Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 27 of 54		

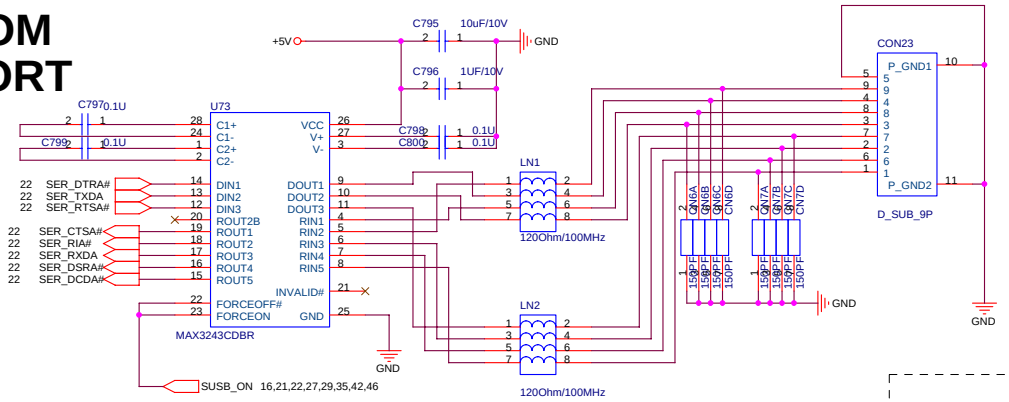
LAN PORT

OP: FOR EMI



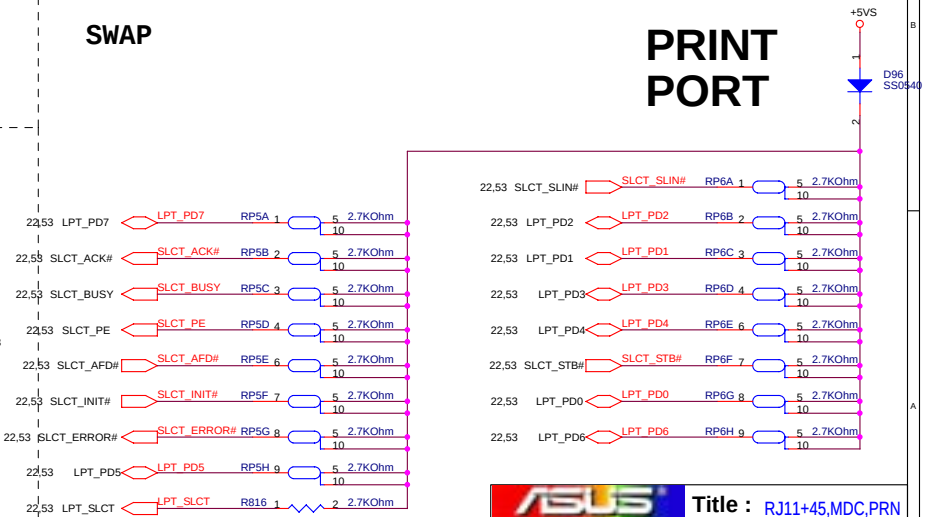
RJ 45 & RJ 11
BOTTOM VIEW

COM PORT



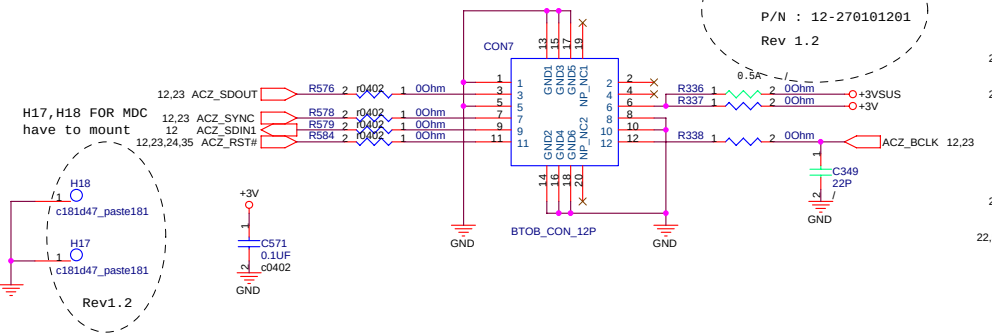
SWAP

PRINT PORT



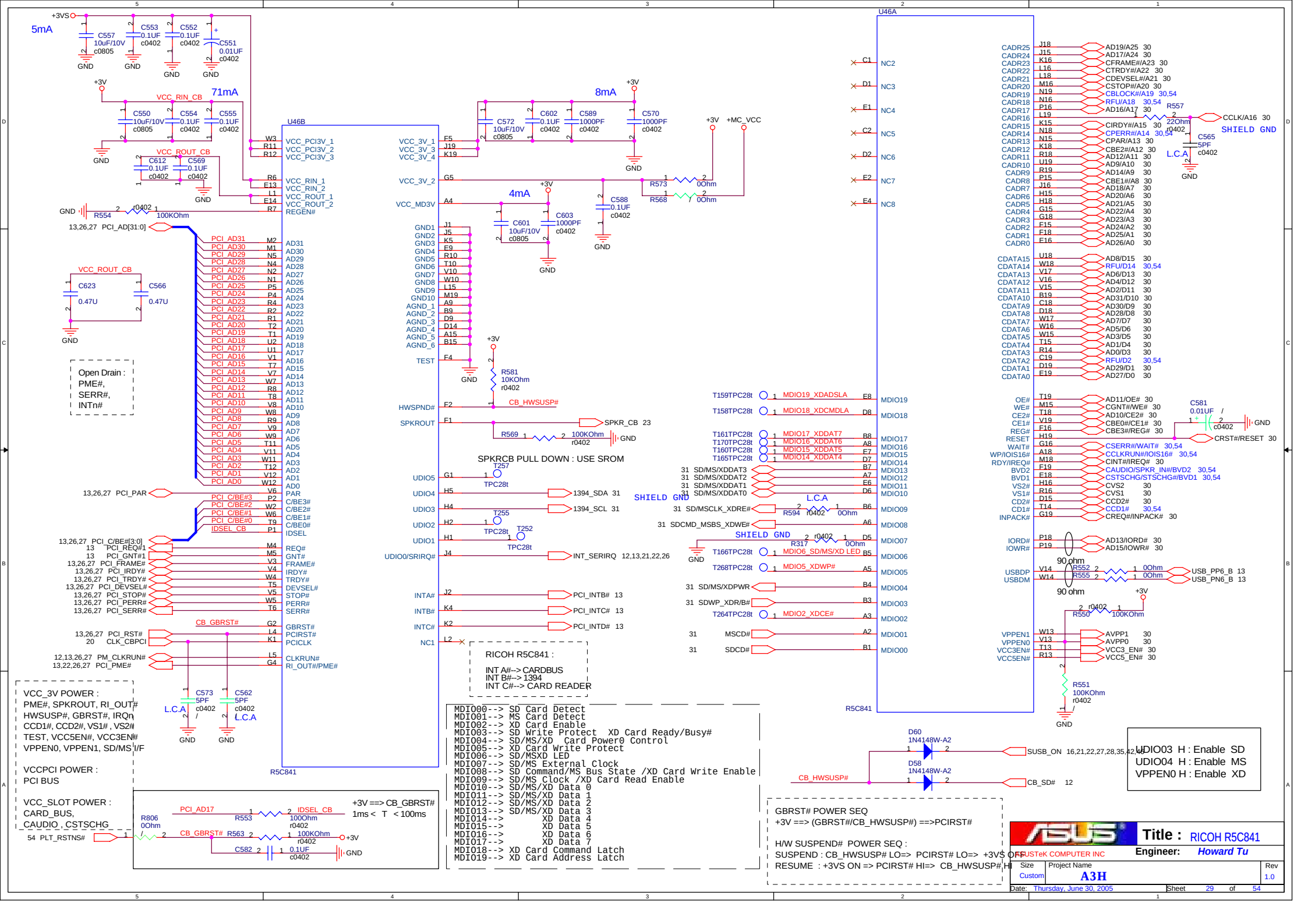
MDC

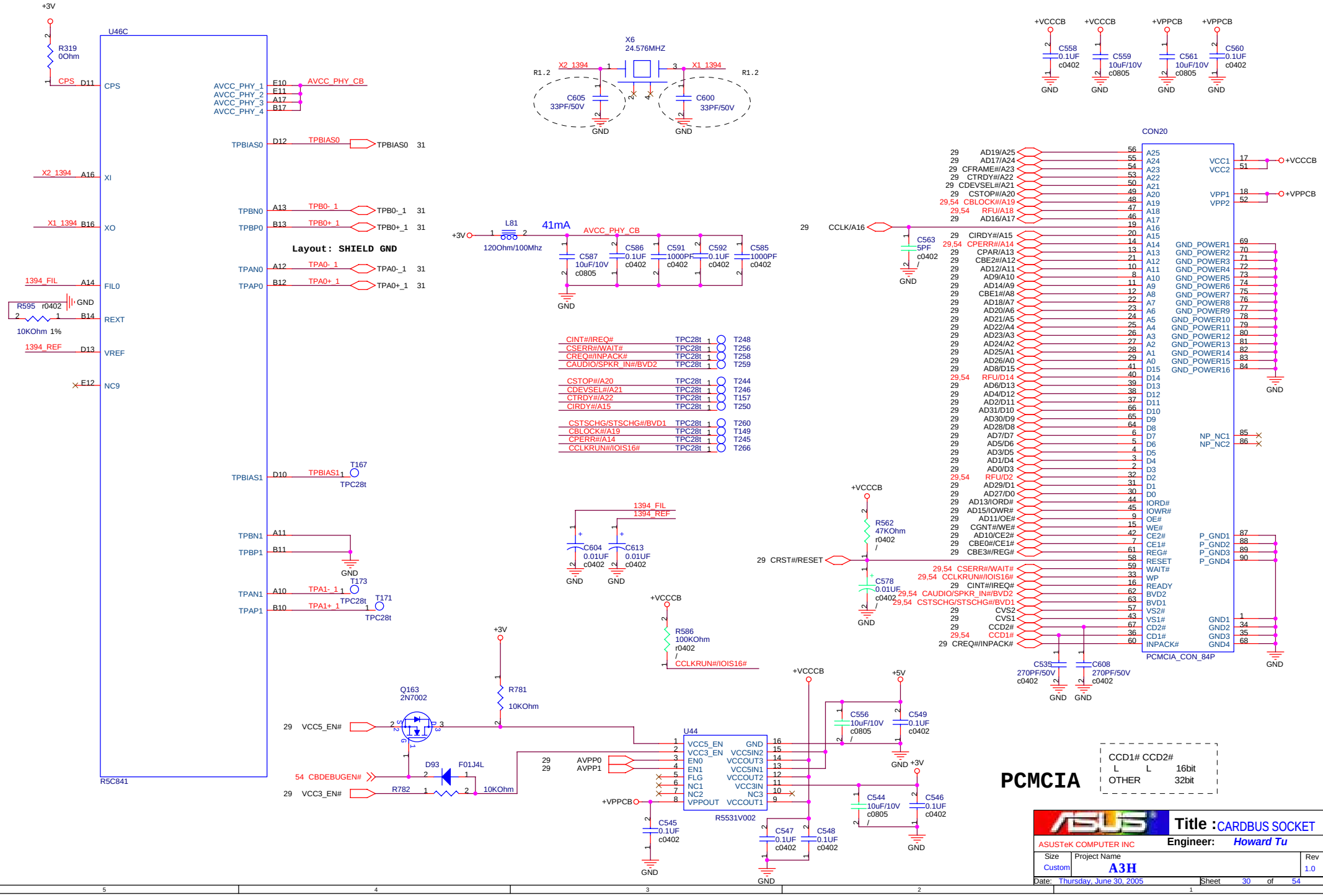
P/N : 12-270101201
Rev 1.2

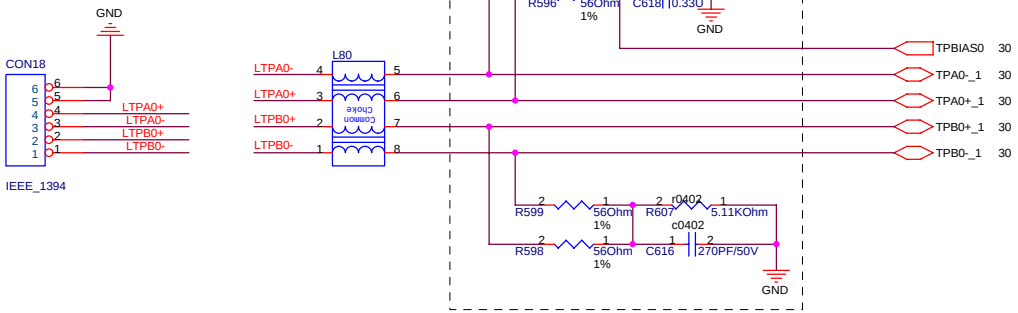


For MDC module

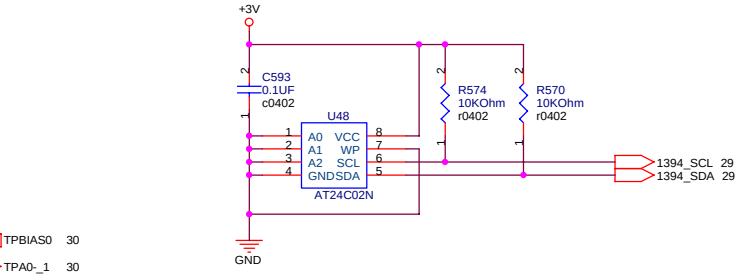
ASUSTeK COMPUTER INC	Title : RJ11+45,MDC,PRN		
	Engineer: Howard Tu		
Size: Custom	Project Name: A3H		Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 28 of 54		

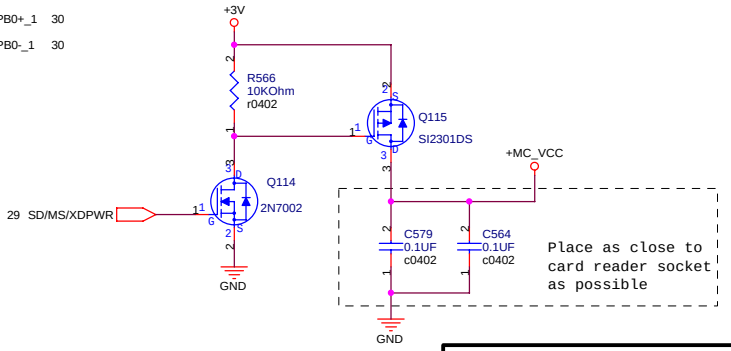

5mA
71mA
8mA
4mA
U46B
R5C841
U46A
Open Drain : PME#, SERR#, INTn#
SPKRCB PULL DOWN : USE SROM
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
VCC_3V POWER : PME#, SPKROUT, RI_OUT# HWSUSP#, GBRST#, IRQn CCD1#, CCD2#, VS1# , VS2# TEST, VCC5EN#, VCC3EN# VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER : PCI BUS
VCC_SLOT POWER : CARD_BUS, CAUDIO , CSTSCHG
+3V ==> CB_GBRST# 1ms < T < 100ms
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
Title : RICOH R5C841
Engineer: Howard Tu
ASUSTeK COMPUTER INC
Size Custom
Project Name A3H
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 29 of 54


+3V
R319
0Ohm
CPS D11
U46C
CPS
XI
XO
FIL0
REXT
VREF
NC9
R5C841
X2_1394 A16
X1_1394 B16
1394_FIL A14
R595 r0402
GND
10KOhm 1%
B14
1394_REF D13
E12
AVCC_PHY_1 E10
AVCC_PHY_2 E11
AVCC_PHY_3 A17
AVCC_PHY_4 B17
AVCC_PHY_CB
TPBIAS0 D12
TPBIAS0 31
TPBN0 A13
TPBP0 B13
TPB0-_1 31
TPB0+_1 31
Layout: SHIELD GND
TPAN0 A12
TPAP0 B12
TPA0-_1 31
TPA0+_1 31
TPBIAS1 D10
T167
TPC28t
TPBN1 A11
TPBP1 B11
GND
TPAN1 A10
TPAP1 B10
T173
T171
X6
24.576MHZ
R1.2
X2_1394
X1_1394
C605
33PF/50V
C600
L81
120Ohm/100Mhz
41mA
C586
0.1UF
c0402
C591
1000PF
C592
C585
C587
10uF/10V
c0805
CINT#/IREQ#
CSERR#/WAIT#
CREQ#/INPACK#
CAUDIO/SPKR_IN#/BVD2
CSTOP#/A20
CDEVSEL#/A21
CTRDY#/A22
CIRDY#/A15
CSTSCHG/STSCHG#/BVD1
CBLOCK#/A19
CPERR#/A14
CCLKRUN#/IOIS16#
TPC28t
T248
T256
T258
T259
T244
T246
T157
T250
T260
T149
T245
T266
1394_FIL
1394_REF
C604
0.01UF
C613
+VCCCB
R586
100KOhm
CCLKRUN#/IOIS16#
Q163
2N7002
R781
10KOhm
29 VCC5_EN#
54 CBDEBUGEN#
D93
F01J4L
R782
29 VCC3_EN#
U44
VCC5_EN
VCC3_EN
EN0
EN1
FLG
NC1
NC2
VPPOUT
GND
VCC5IN2
VCCOUT3
VCC5IN1
VCCOUT2
VCC3IN
NC3
VCCOUT1
R5531V002
29 AVPP0
29 AVPP1
+VPPCB
+5V
C556
10uF/10V
C549
0.1UF
C544
C546
C545
C547
C548
+VCCCB
+VCCCB
+VPPCB
+VPPCB
C558
0.1UF
C559
10uF/10V
c0805
C561
10uF/10V
c0805
C560
0.1UF
CON20
29 AD19/A25
29 AD17/A24
29 CFRAME#/A23
29 CTRDY#/A22
29 CDEVSEL#/A21
29 CSTOP#/A20
29,54 CBLOCK#/A19
29,54 RFU/A18
29 AD16/A17
29 CCLK/A16
C563
5PF
29 CIRDY#/A15
29,54 CPERR#/A14
29 CPAR/A13
29 CBE2#/A12
29 AD12/A11
29 AD9/A10
29 AD14/A9
29 CBE1#/A8
29 AD18/A7
29 AD20/A6
29 AD21/A5
29 AD22/A4
29 AD23/A3
29 AD24/A2
29 AD25/A1
29 AD26/A0
29 AD8/D15
29,54 RFU/D14
29 AD6/D13
29 AD4/D12
29 AD2/D11
29 AD31/D10
29 AD30/D9
29 AD28/D8
29 AD7/D7
29 AD5/D6
29 AD3/D5
29 AD1/D4
29 AD0/D3
29,54 RFU/D2
29 AD29/D1
29 AD27/D0
29 AD13/IORD#
29 AD15/IOWR#
29 AD11/OE#
29 CGNT#/WE#
29 AD10/CE2#
29 CBE0#/CE1#
29 CBE3#/REG#
VCC1
VCC2
VPP1
VPP2
GND_POWER1
GND_POWER2
GND_POWER3
GND_POWER4
GND_POWER5
GND_POWER6
GND_POWER7
GND_POWER8
GND_POWER9
GND_POWER10
GND_POWER11
GND_POWER12
GND_POWER13
GND_POWER14
GND_POWER15
GND_POWER16
NP_NC1
NP_NC2
P_GND1
P_GND2
P_GND3
P_GND4
GND1
GND2
GND3
GND4
PCMCIA_CON_84P
29 CRST#/RESET
R562
47KOhm
C578
0.01UF
29,54 CSERR#/WAIT#
29,54 CCLKRUN#/IOIS16#
29 CINT#/IREQ#
29,54 CAUDIO/SPKR_IN#/BVD2
29,54 CSTSCHG/STSCHG#/BVD1
29 CVS2
29 CVS1
29 CCD2#
29,54 CCD1#
29 CREQ#/INPACK#
C535
270PF/50V
C608
270PF/50V
PCMCIA
CCD1# CCD2#
L L 16bit
OTHER 32bit
Title : CARDBUS SOCKET
ASUSTeK COMPUTER INC
Engineer: Howard Tu
Size Custom
Project Name A3H
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 30 of 54



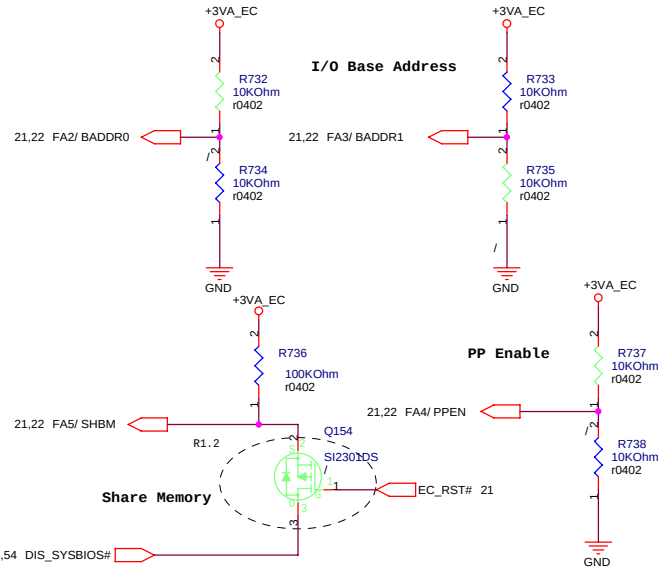
1.CLOSE TO R5C841
2.The area is as compact as possible,length < 10 mm
3.TPA Pair and TPB pair mismatch < 2.5mm
4.No via recommend , maxmium is one.
5.Total length < 50 mm
6.Differential impedance is 110+/- 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm

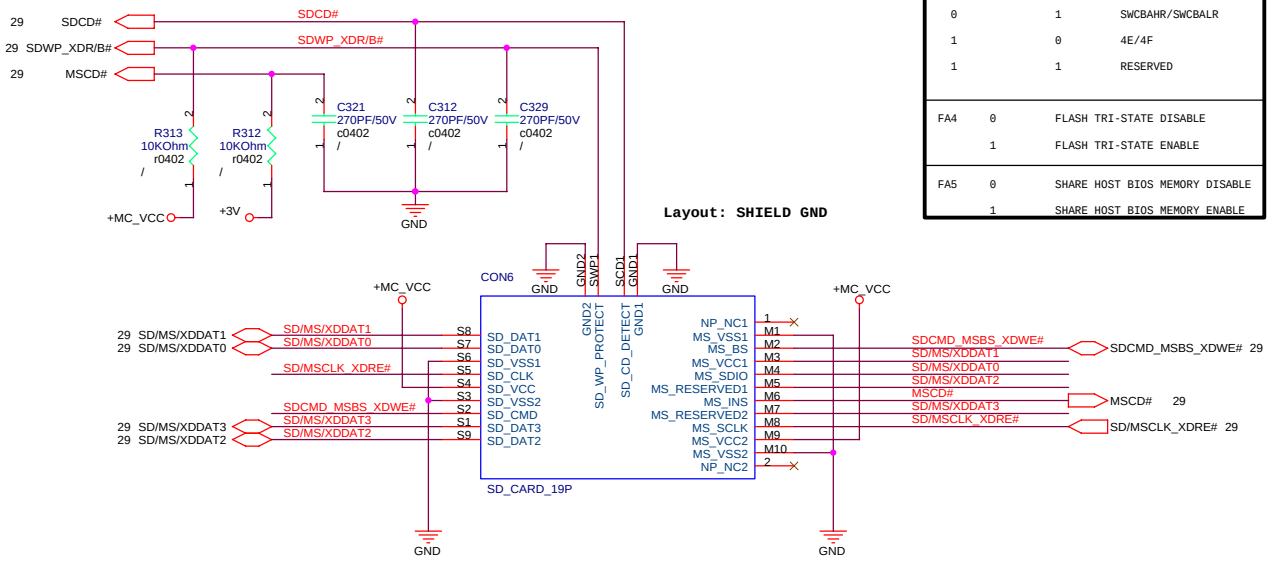


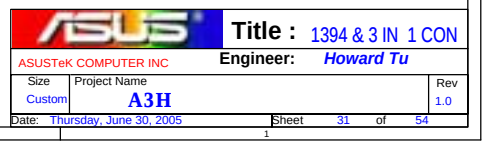


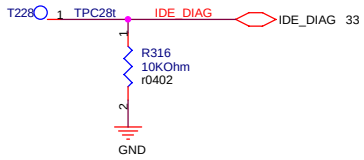
Hardware Strap Pin			
BADDR0/FA2	BADDR1/FA3	PORT	
0	0	2E/2F	
0	1	SWCBAHR/SWCBALR	
1	0	4E/4F	
1	1	RESERVED	
FA4	0	FLASH TRI-STATE DISABLE	
	1	FLASH TRI-STATE ENABLE	
FA5	0	SHARE HOST BIOS MEMORY DISABLE	
	1	SHARE HOST BIOS MEMORY ENABLE	

EC Hardware Strap

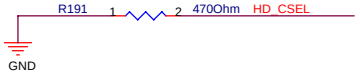


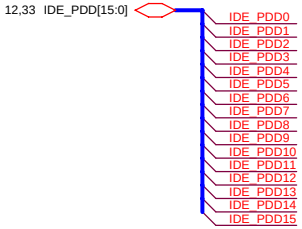


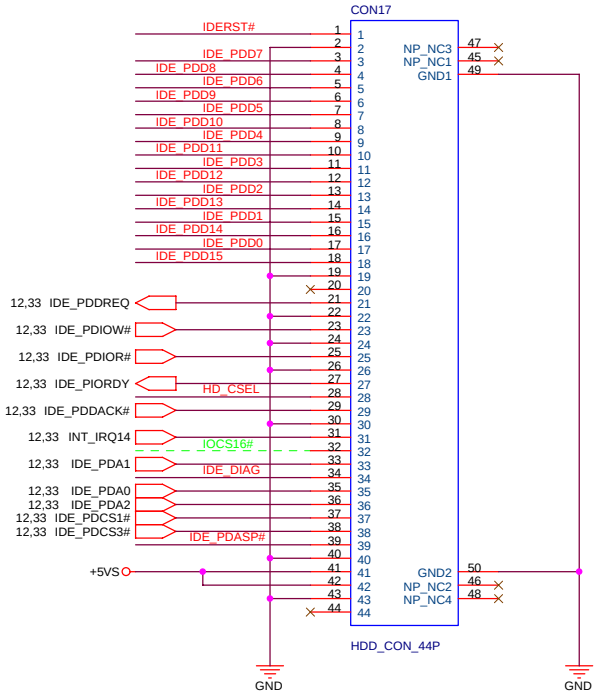


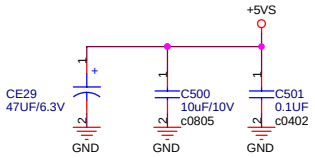


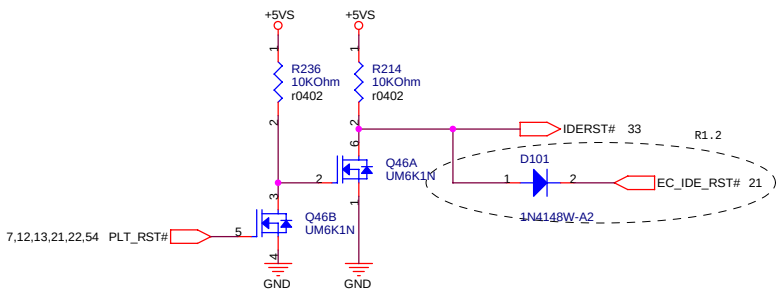
HD_CSEL : Pull-Down, HDD as Master

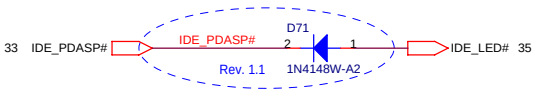










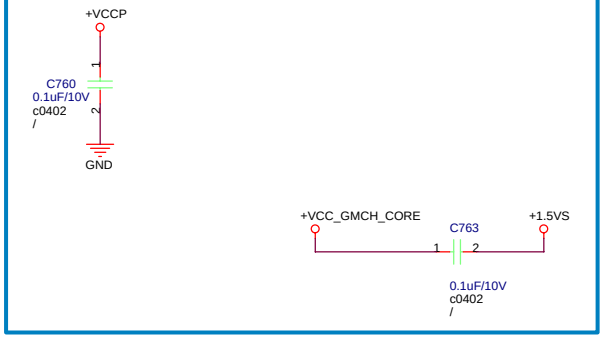


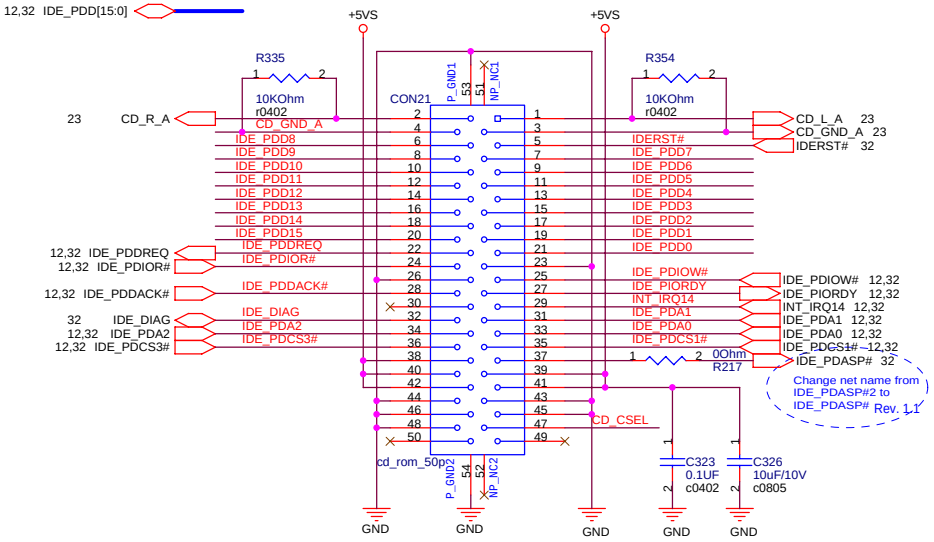
ASUSTeK COMPUTER INC	Title : HDD CONNECTOR	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 32 of 54	

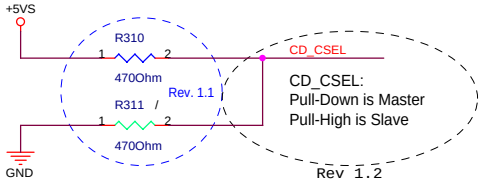
For EMI test (place on TOP layer)

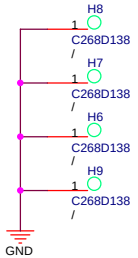
0119

stitching cap.

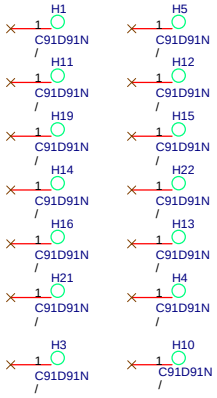


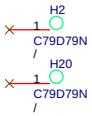


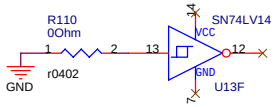


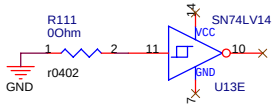


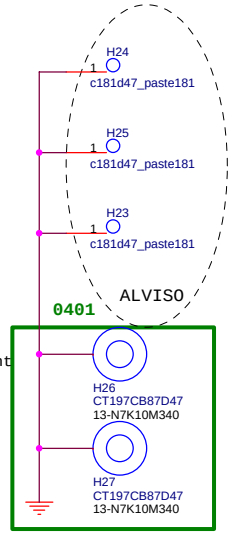
CPU











Holes for ALVISO have to mount

ASUSTeK COMPUTER INC

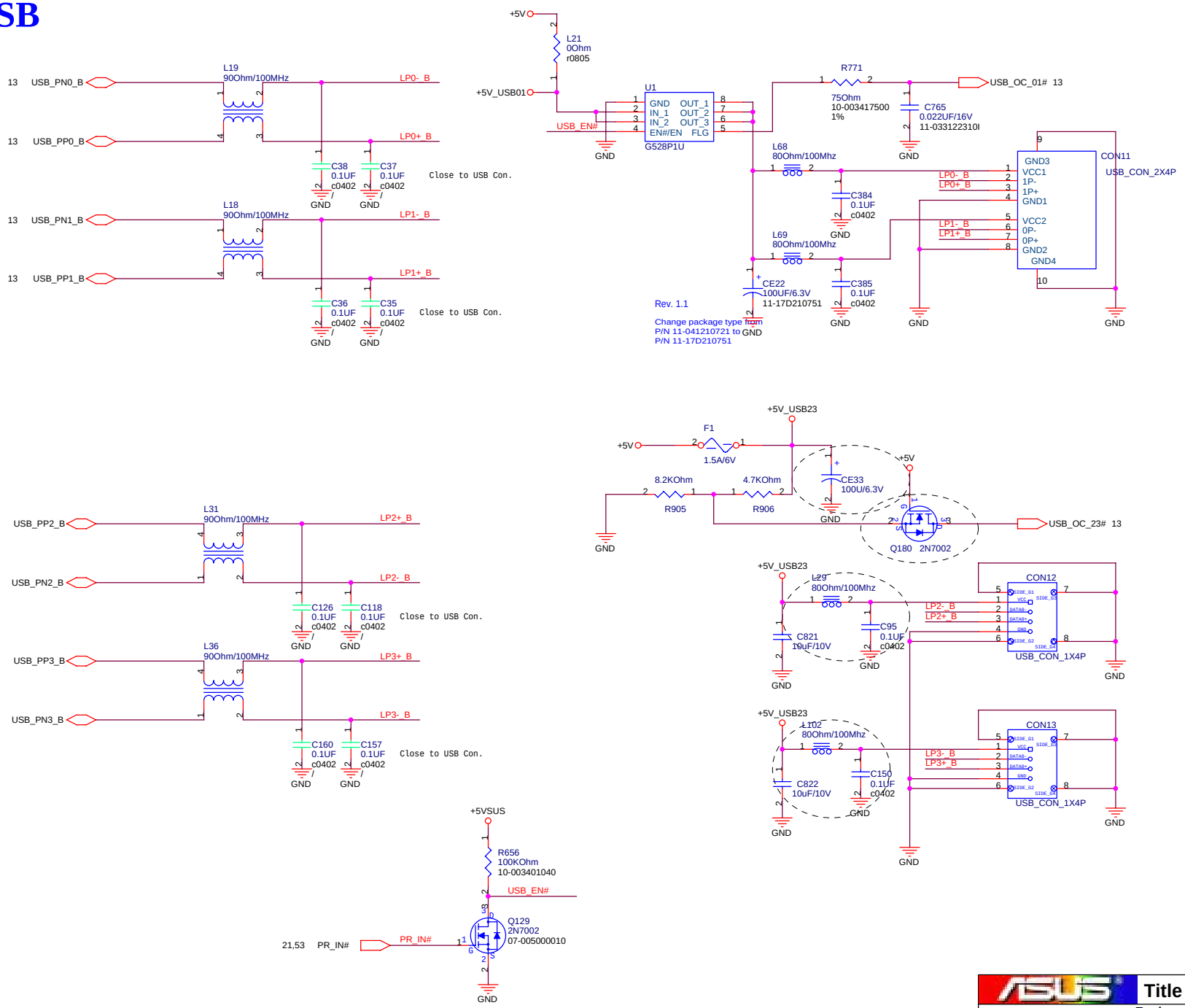
Title : CDROM

Engineer: Howard Tu

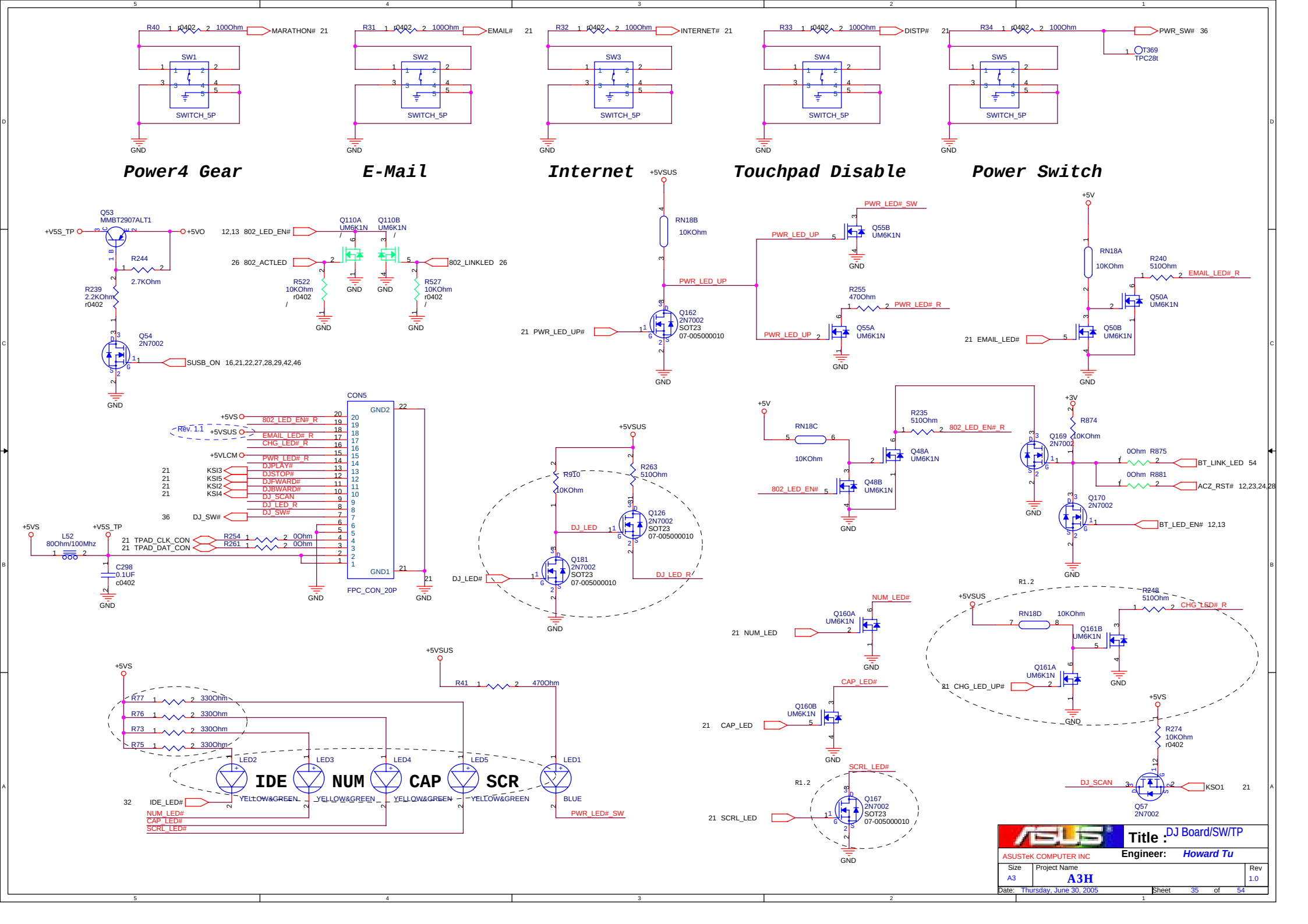
Size	Project Name	Rev
Custom	A3H	1.0

Date: Thursday, June 30, 2005 Sheet 33 of 54

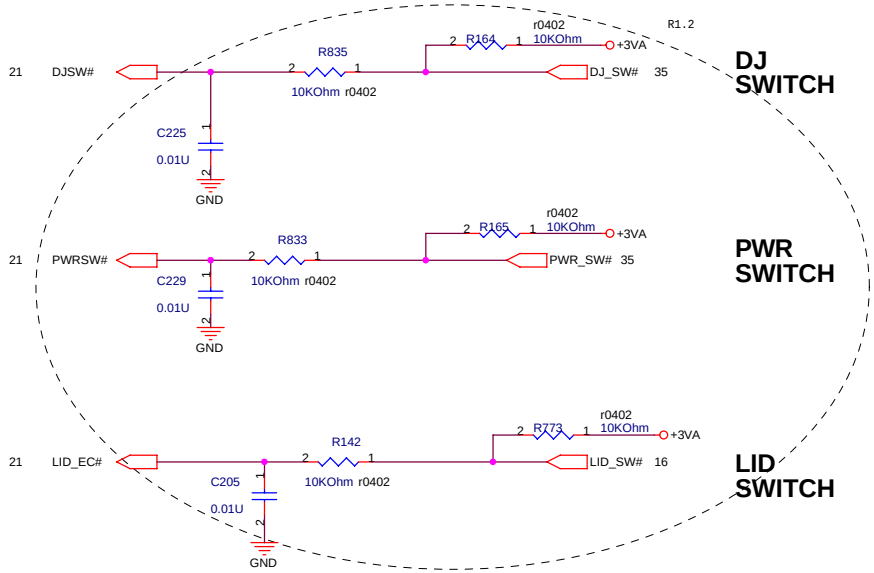
USB

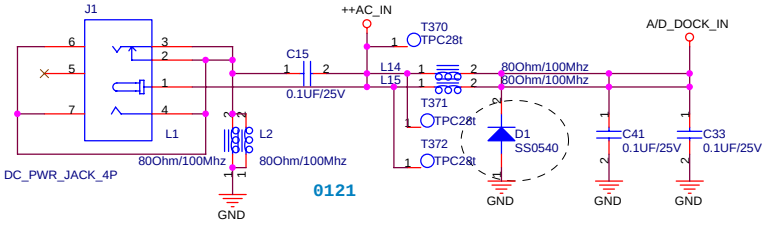


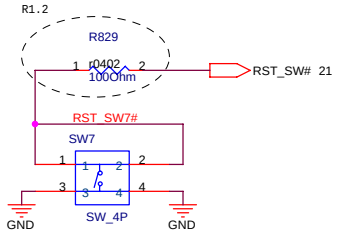
ASUSTeK COMPUTER INC		Title : USB CONN	
		Engineer: Howard Tu	
Size: Custom	Project Name: A3H		Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 34 of 54		



Title :	DJ Board/SW/TP
ASUSTeK COMPUTER INC	Engineer: Howard Tu
Size: A3	Project Name: A3H
Rev: 1.0	
Date: Thursday, June 30, 2005	Sheet 35 of 54





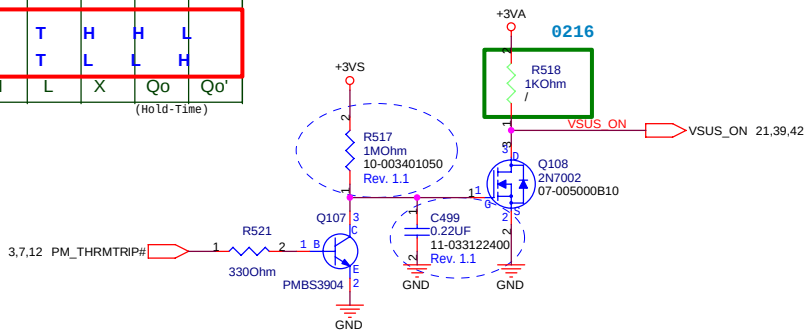


74HC74 TRUTH TABLE

Rev 1.2

PRE#	CLR#	CLK	D	Q	Q'
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	float	float
H	H	T	H	H	L
H	H	T	L	L	H
H	H	L	X	Qo	Qo'

(Hold-Time)



System Power Sequence
+VCCRTC -> RTCRST# ->V5REFSUS ->3.3/1.5VSUS>
RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK
->V5REF->PWROK->GMCH->VCCP->VCORE
SUSSTAT#->PCIRST#
CPU : +VCORE, +VCCP,+1.05VS
NB : +1.05VS, +1.5VS, +2.5V, +VCCP
SB : +1.5VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
DDR : +1.8V, +0.9VS
M24 : +3.3VS, +2.5VS, +1.5VS, +1.8VS, AC_BAT_SYS

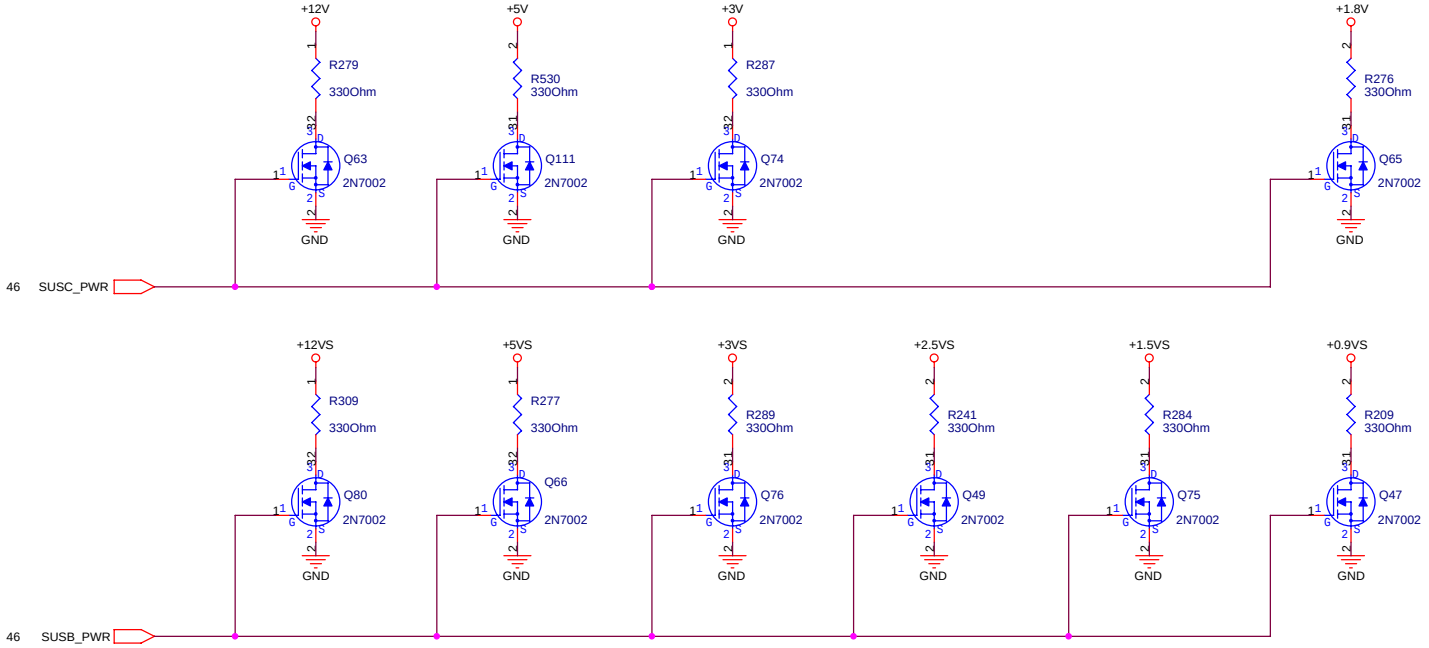
ASUSTeK COMPUTER INC

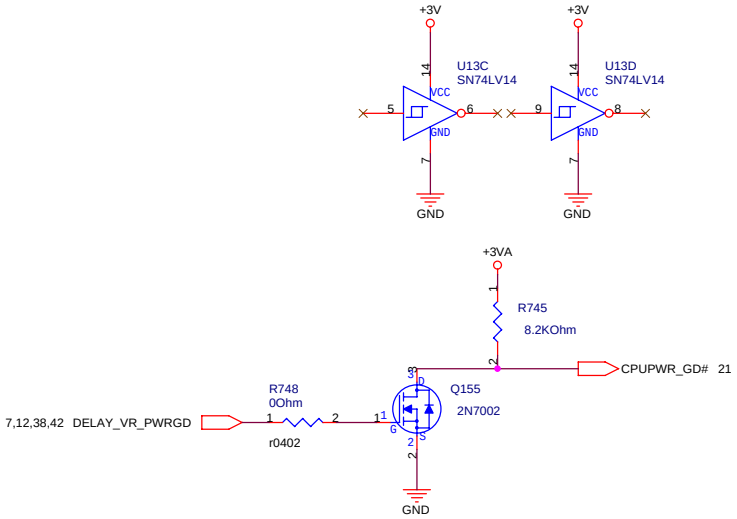
Title : Startup Circuit (1)

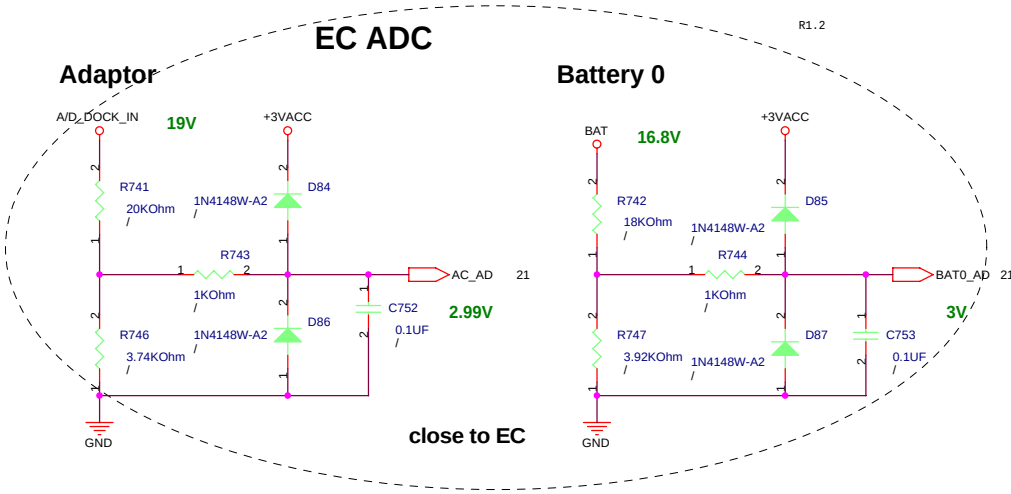
Engineer: Howard Tu

Size	Project Name	Rev
Custom	A3H	1.0

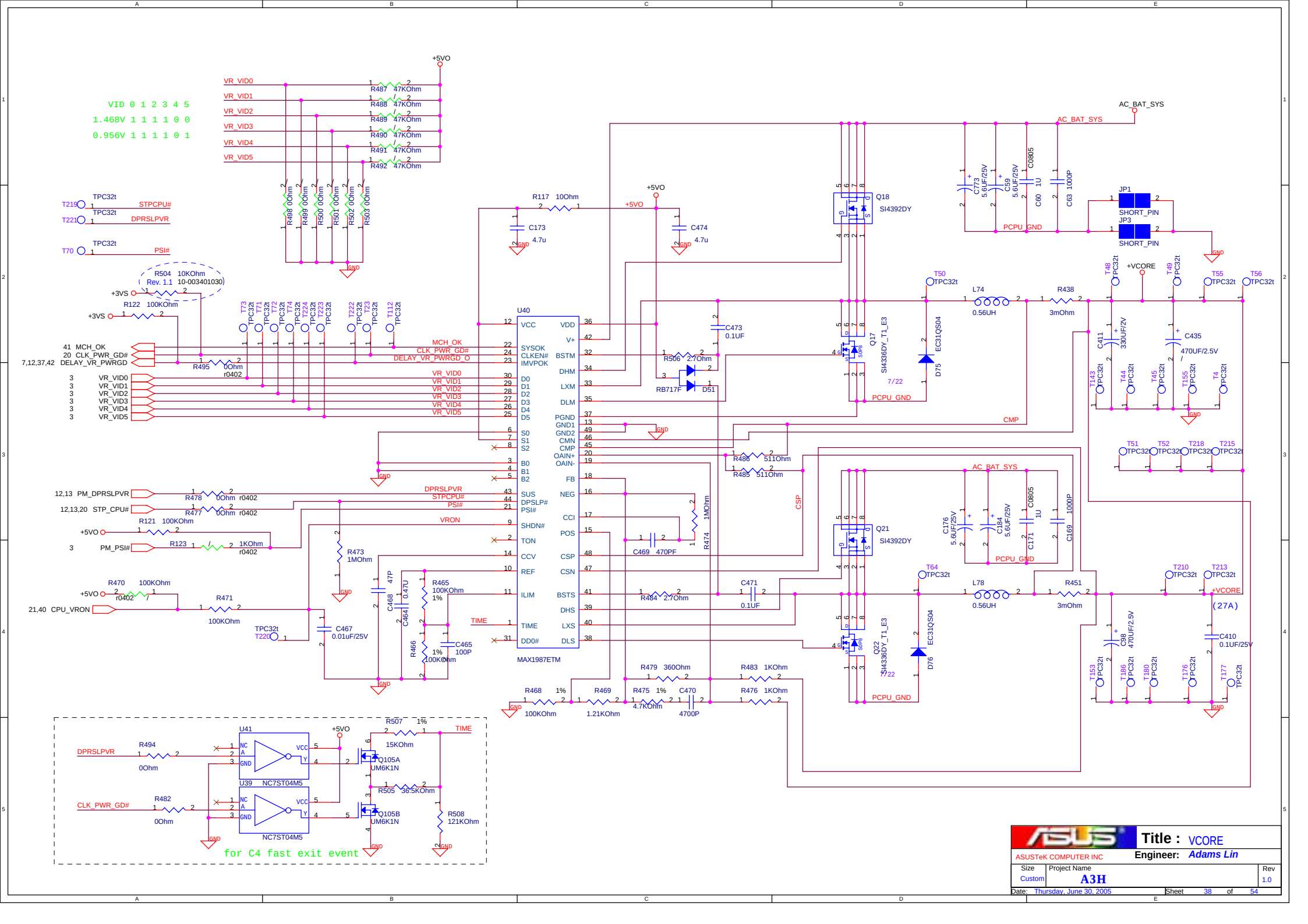
Date: Thursday, June 30, 2005 Sheet 36 of 54

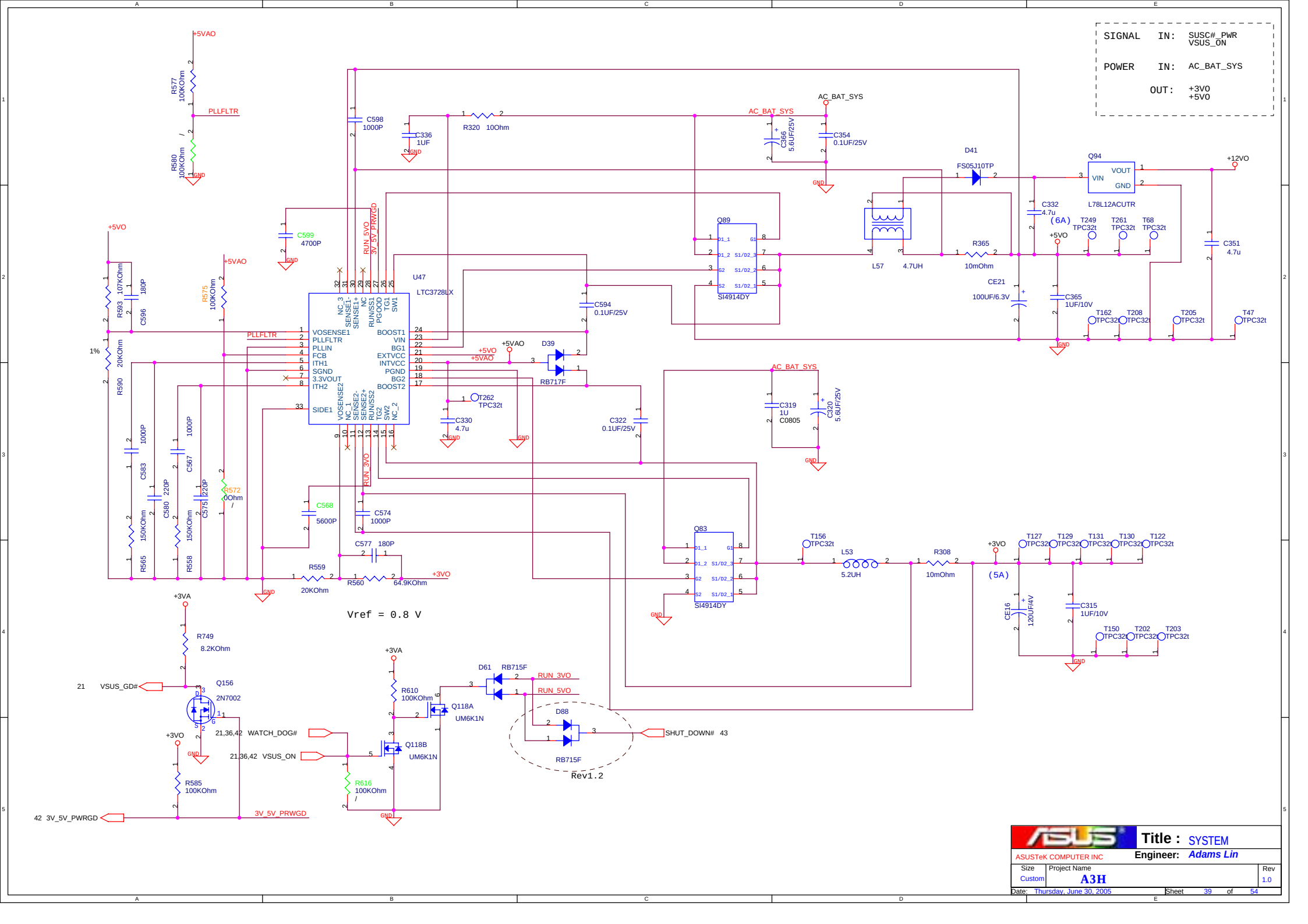


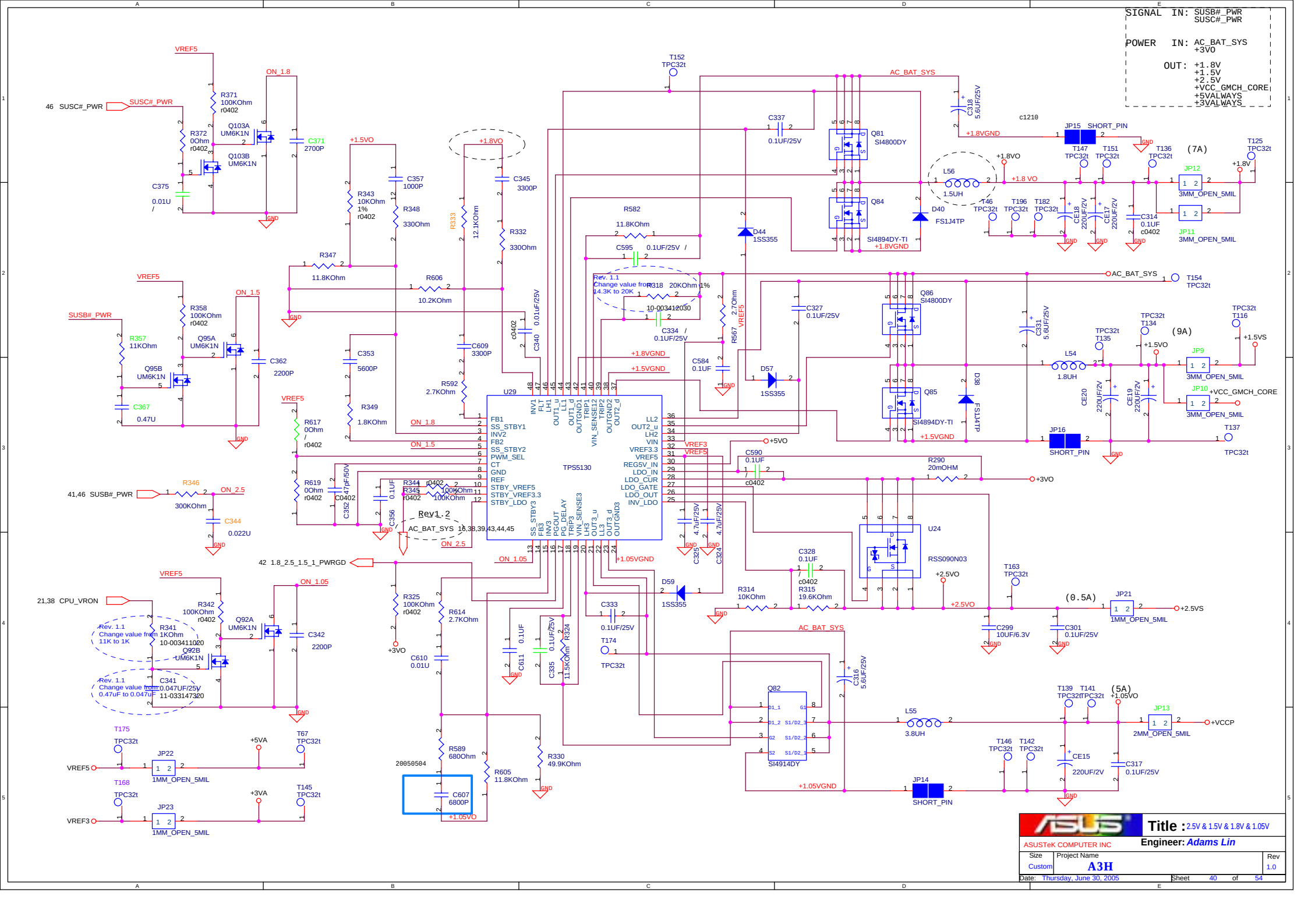




ASUSTeK COMPUTER INC	Title : Startup Circuit (2)	
	Engineer: Howard Tu	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 37 of 54	


VID 0 1 2 3 4 5
1.468V 1 1 1 1 0 0
0.956V 1 1 1 1 0 1
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
+5VO
R487 47KOhm
R488 47KOhm
R489 47KOhm
R490 47KOhm
R491 47KOhm
R492 47KOhm
R498 0Ohm
R499 0Ohm
R500 0Ohm
R501 0Ohm
R502 0Ohm
R503 0Ohm
GND
TPC32t T219 STPCPU#
TPC32t T221 DPRSLPVR
TPC32t T70 PSI#
R504 10KOhm
Rev. 1.1 10-003401030
+3VS
R122 100KOhm
T73 T71 T72 T74 T224 T223 T222 T23 T112
41 MCH_OK
20 CLK_PWR_GD#
7,12,37,42 DELAY_VR_PWRGD
R495 0Ohm r0402
MCH_OK
CLK_PWR_GD#
DELAY_VR_PWRGD_O
U40
MAX1987ETM
VCC VDD V+ BSTM DHM LXM DLM PGND GND1 GND2 CMN CMP OAIN+ OAIN-
SYSOK CLKEN# IMVPOK
D0 D1 D2 D3 D4 D5
S0 S1 S2
B0 B1 B2
SUS DPSLP# PSI#
SHDN# TON CCV REF ILIM TIME DD0#
FB NEG CCI POS CSP CSN BSTS DHS LXS DLS
R117 10Ohm
C173 4.7u
C474 4.7u
C473 0.1UF
R506 2.7Ohm
RB717F D51
Q18 SI4392DY
Q17 SI4336DY_T1_E3
D75 EC31QS04
Q21 SI4392DY
Q22 SI4336DY_T1_E3
D76 EC31QS04
PCPU_GND
AC_BAT_SYS
C772 5.6UF/25V
C59 5.6UF/25V
C0805
C60 1U
C63 1000P
JP1 SHORT_PIN
JP3 SHORT_PIN
L74 0.56UH
L78 0.56UH
R438 3mOhm
R451 3mOhm
+VCORE
C411 330UF/2V
C435 470UF/2.5V
C98 470UF/2.5V
C410 0.1UF/25V
(27A)
CMP
CSP
R488 511Ohm
R485 511Ohm
C176 5.6UF/25V
C184 5.6UF/25V
C171 1U
C169 1000P
R506 2.7Ohm
R484 2.7Ohm
C471 0.1UF
R479 360Ohm
R483 1KOhm
R475 1% 4.7KOhm
C470 4700P
R476 1KOhm
R468 1% 100KOhm
R469 1.21KOhm
12,13 PM_DPRSLPVR
12,13,20 STP_CPU#
R478 0Ohm r0402
R477 0Ohm r0402
R121 100KOhm
3 PM_PSI#
R123 1KOhm r0402
+5VO
R470 100KOhm r0402
21,40 CPU_VRON
R471 100KOhm
TPC32t T220
C467 0.01uF/25V
R473 1MOhm
C468 47P
C464 0.47U
R465 100KOhm 1%
R466 100KOhm 1%
C465 100P
R474 1MOhm
C469 470PF
TIME
VRON
U41 NC7ST04M5
U39 NC7ST04M5
R494 0Ohm
R482 0Ohm
R507 1% 15KOhm
R505 36.5KOhm
R508 121KOhm
Q105A UM6K1N
Q105B UM6K1N
for C4 fast exit event
Title : VCORE
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Size Custom
Project Name A3H
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 38 of 54


SIGNAL IN: SUSC#_PWR
VSUS_ON
POWER IN: AC_BAT_SYS
OUT: +3VO
+5VO
U47
LTC3728LX
Q89
SI4914DY
Q83
SI4914DY
Q94
L78L12ACUTR
D41
FS05J10TP
D39
RB717F
D61
RB715F
D88
RB715F
Q156
2N7002
Q118A
UM6K1N
Q118B
UM6K1N
L57 4.7UH
L53 5.2UH
R308 10mOhm
R365 10mOhm
R320 10Ohm
R559 20KOhm
R560 64.9KOhm
Vref = 0.8 V
Rev1.2
Title : SYSTEM
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Project Name A3H
Size Custom
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 39 of 54


SIGNAL IN: SUSB#_PWR
SUSC#_PWR
POWER IN: AC_BAT_SYS
+3VO
OUT: +1.8V
+1.5V
+2.5V
+VCC_GMCH_CORE
+5VALWAYS
+3VALWAYS
TPS5130
Rev1.2
Rev. 1.1 Change value from 14.3K to 20K
Rev. 1.1 Change value from 11K to 1K
Rev. 1.1 Change value from 0.47uF to 0.047uF
Title : 2.5V & 1.5V & 1.8V & 1.05V
ASUSTeK COMPUTER INC
Engineer: Adams Lin
Project Name A3H
Size Custom
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 40 of 54

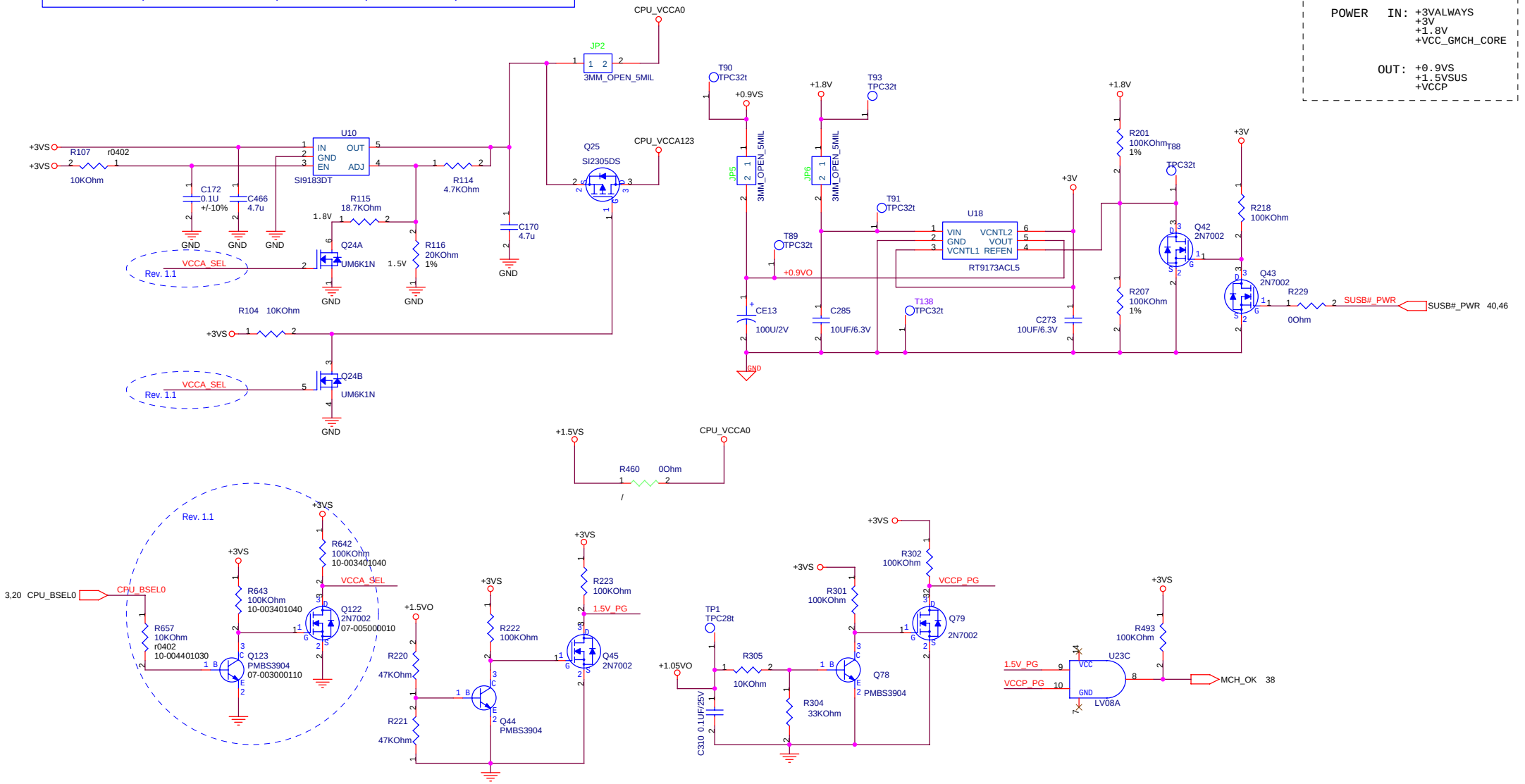
For Duthon ,CPU_BSEL0 = LOW ,FSB=533MHZ ,VCCA0=1.5V ,VCCA123=0V

For celeron ,CPU_BSEL0 = HIGH ,FSB=400MHZ ,VCCA0=1.8V ,VCCA123=1.8V

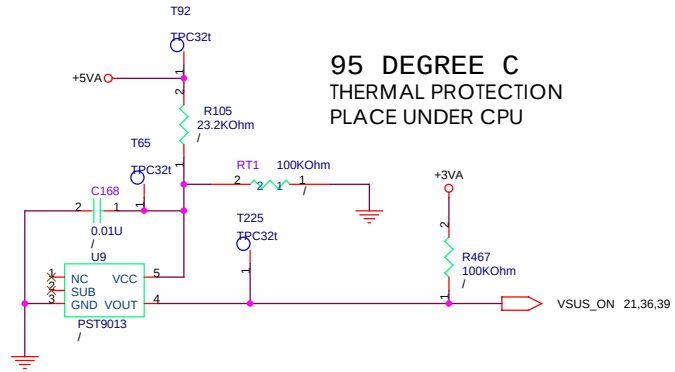
SIGNAL IN: SUSB#_PWR
CPU_VRON

POWER IN: +3VALWAYS
+3V
+1.8V
+VCC_GMCH_CORE

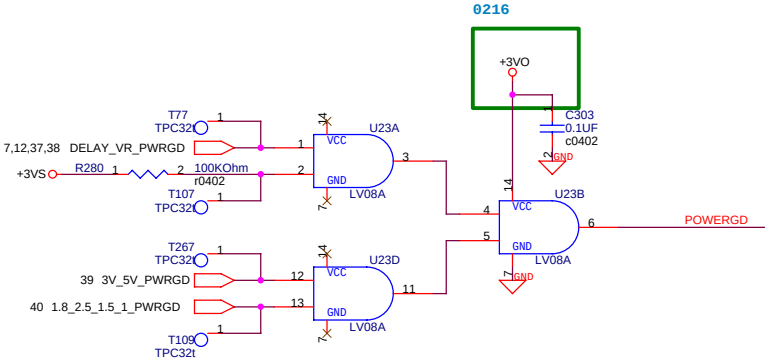
OUT: +0.9VS
+1.5VSUS
+VCCP

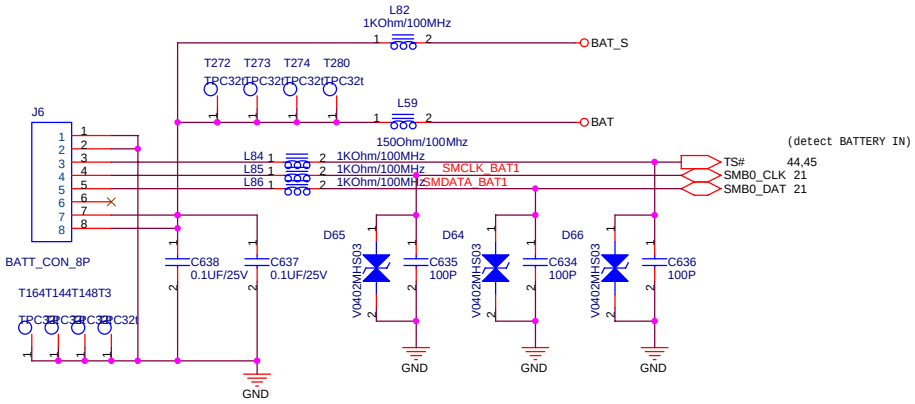


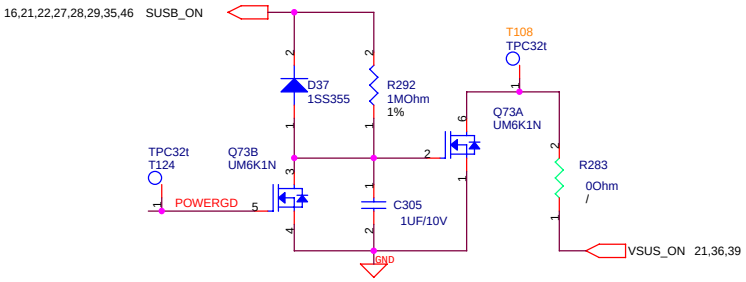
ASUSTeK COMPUTER INC	Title : 1.5VA & DDR2	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 41 of 54	



95 DEGREE C
THERMAL PROTECTION
PLACE UNDER CPU







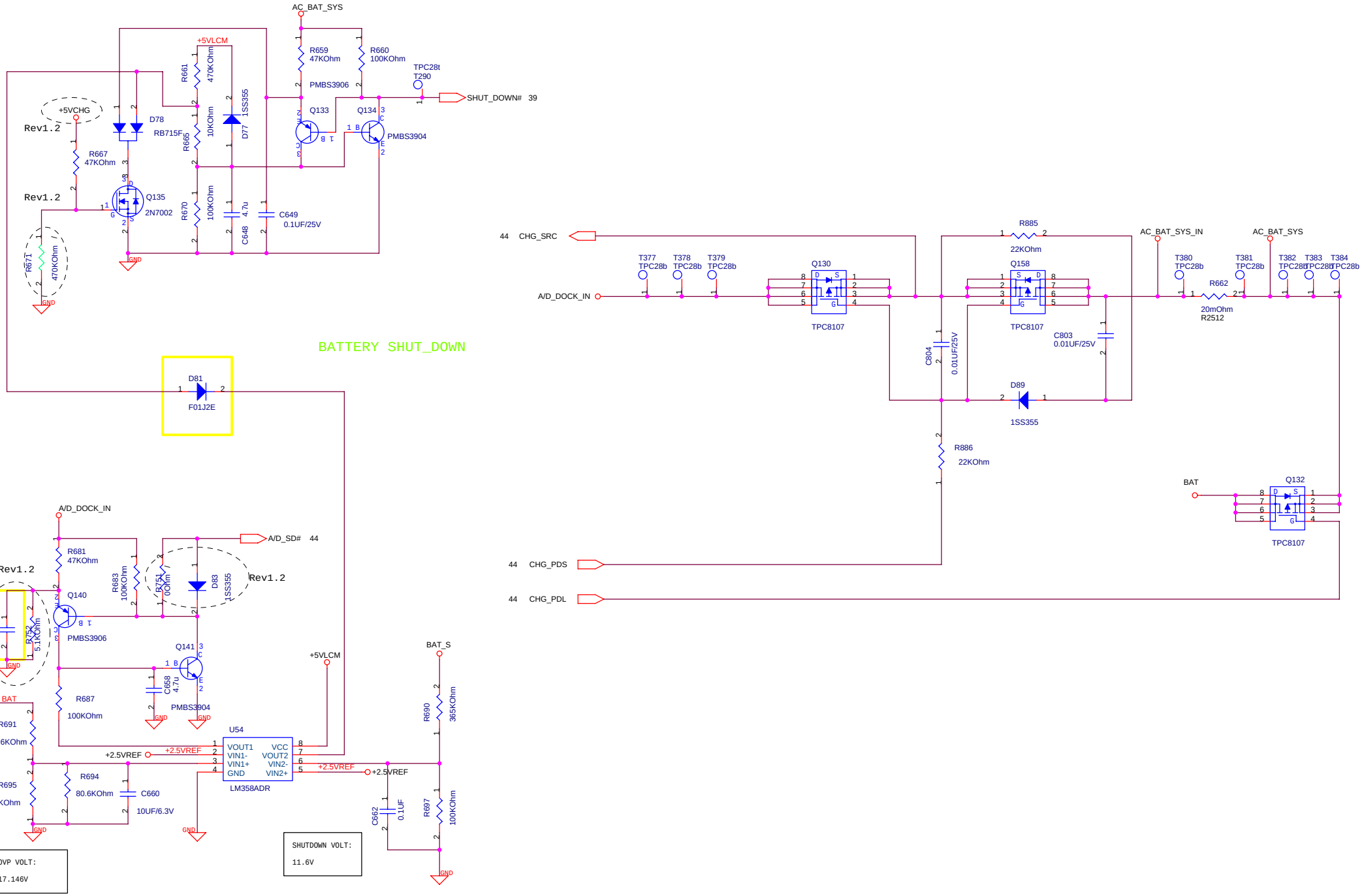
ASUSTeK COMPUTER INC

Title : BAT CONNECT

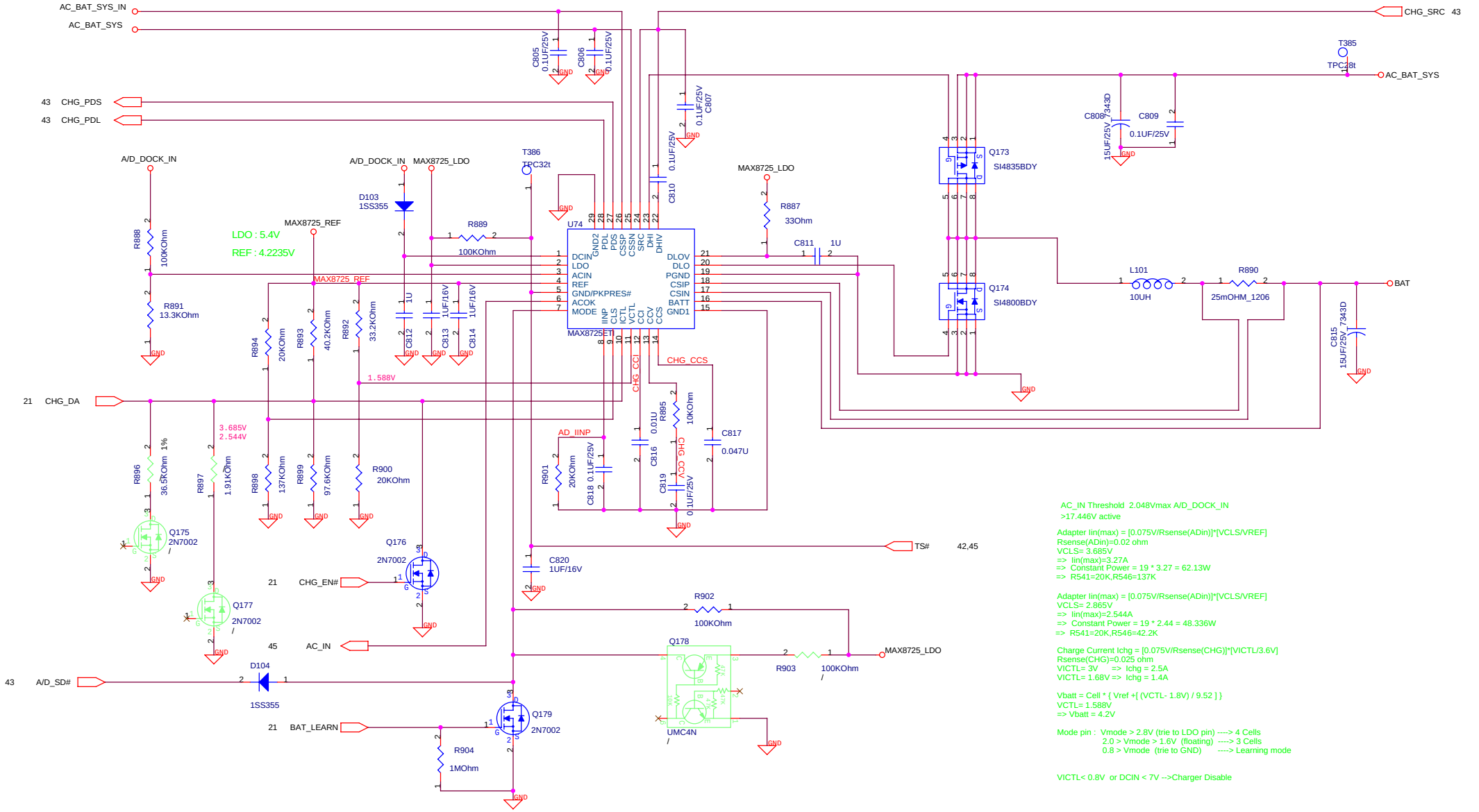
Engineer: Adams Lin

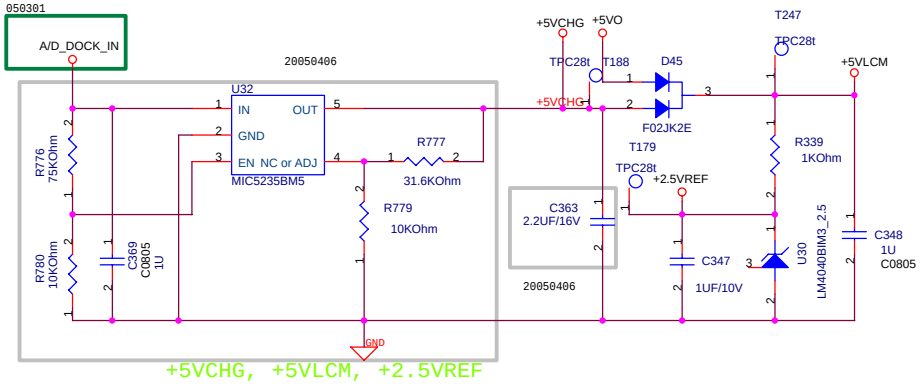
Size	Project Name	Rev
Custom	A3H	1.0

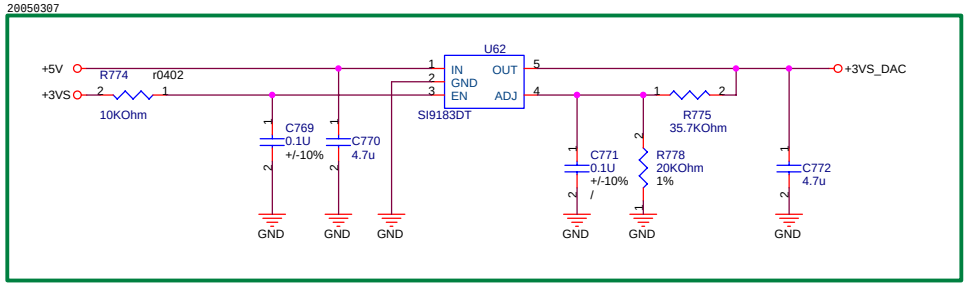
Date: Thursday, June 30, 2005 Sheet 42 of 54



Title : CHARGE		
Engineer: Adams Lin		
ASUSTeK COMPUTER INC		
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 43 of 54	


AC_BAT_SYS_IN
AC_BAT_SYS
CHG_SRC 43
T385
TPC32t
AC_BAT_SYS
43 CHG_PDS
43 CHG_PDL
C805 0.1UF/25V
C806 0.1UF/25V
C807 0.1UF/25V
C808 15UF/25V_7343D
C809 0.1UF/25V
A/D_DOCK_IN
A/D_DOCK_IN MAX8725_LDO
D103 1SS355
T386
TPC32t
MAX8725_LDO
R887 33Ohm
C811 1U
Q173 SI4835BDY
Q174 SI4800BDY
L101 10UH
R890 25mOHM_1206
BAT
C815 15UF/25V_7343D
LDO : 5.4V
REF : 4.2235V
MAX8725_REF
R888 100KOhm
R889 100KOhm
U74
MAX8725ETI
DCIN
LDO
ACIN
REF
GND/PKPRES#
ACOK
MODE
DLOV
DLO
PGND
CSIP
CSIN
BATT
GND1
R891 13.3KOhm
R894 20KOhm
R893 40.2KOhm
R892 33.2KOhm
C812 1U
C813 1UF/16V
C814 1UF/16V
MAX8725_REF
1.588V
21 CHG_DA
CHG_CCI
CHG_CCS
R895 10KOhm
C816 0.01U
C817 0.047U
AD_IINP
R901 20KOhm
C818 0.1UF/25V
C819 0.1UF/25V
R896 36.5KOhm 1%
R897 1.91KOhm
R898 137KOhm
R899 97.6KOhm
R900 20KOhm
3.685V
2.544V
Q175 2N7002
Q176 2N7002
Q177 2N7002
TS# 42,45
C820 1UF/16V
21 CHG_EN#
45 AC_IN
R902 100KOhm
Q178 UMC4N
R903 100KOhm
MAX8725_LDO
43 A/D_SD#
D104 1SS355
21 BAT_LEARN
Q179 2N7002
R904 1MOhm
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
>17.446V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02 ohm
VCLS= 3.685V
=> Iin(max)=3.27A
=> Constant Power = 19 * 3.27 = 62.13W
=> R541=20K,R546=137K
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
VCLS= 2.865V
=> Iin(max)=2.544A
=> Constant Power = 19 * 2.44 = 48.336W
=> R541=20K,R546=42.2K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A
Vbatt = Cell * (Vref +[(VCTL- 1.8V) / 9.52])
VCTL= 1.588V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Title : CHARGE
Engineer: Adams Lin
ASUSTeK COMPUTER INC
Size Custom
Project Name A3H
Rev 1.0
Date: Thursday, June 30, 2005
Sheet 44 of 54

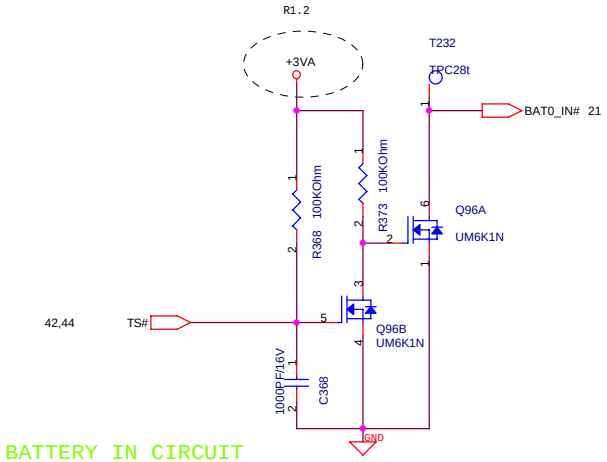


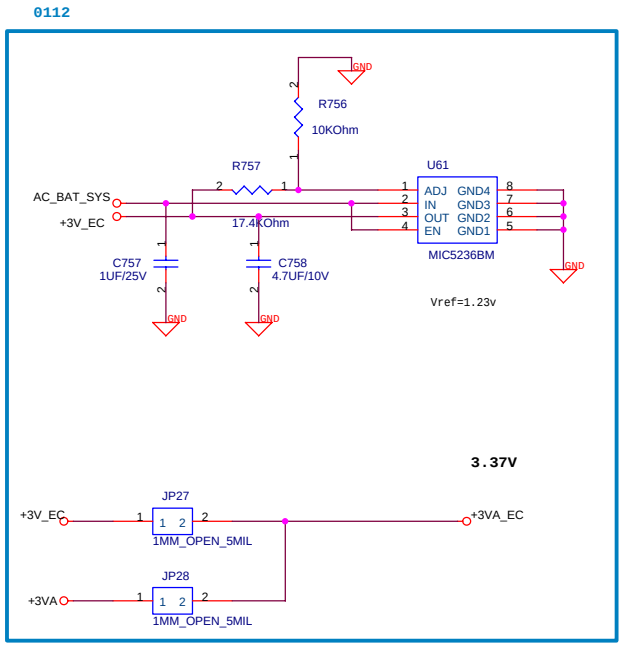


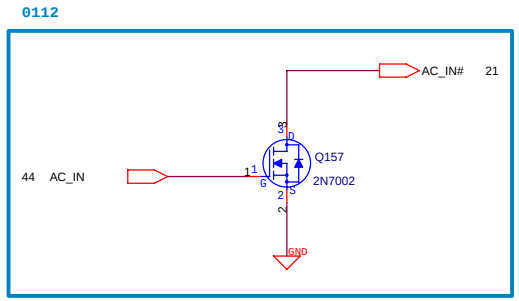
Ref: 1.24V

ON: EN>2V (A/D_DOCK_IN:17V)

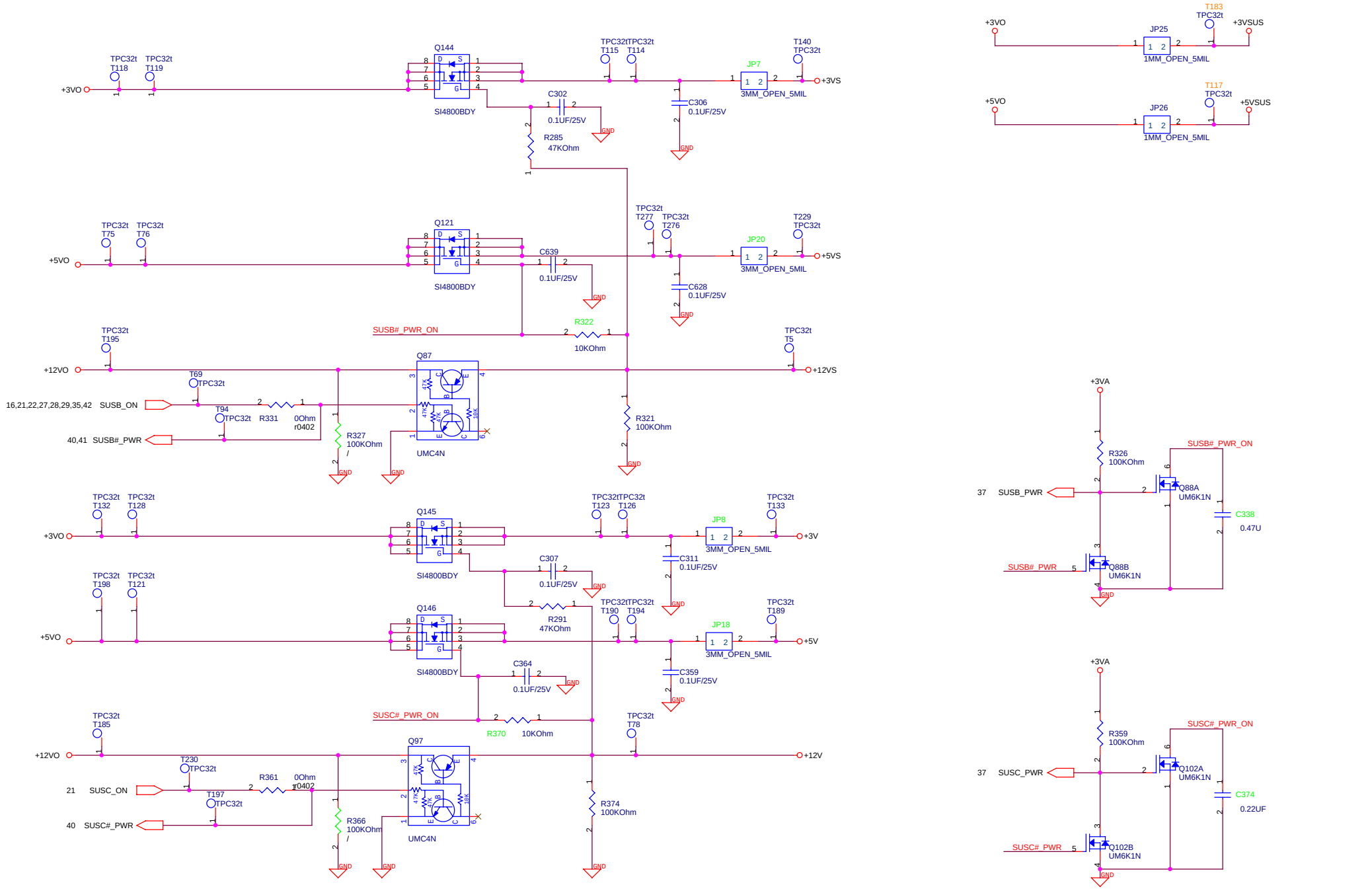
OFF: EN<0.6V(A/D_DOCK_IN:5.1V)



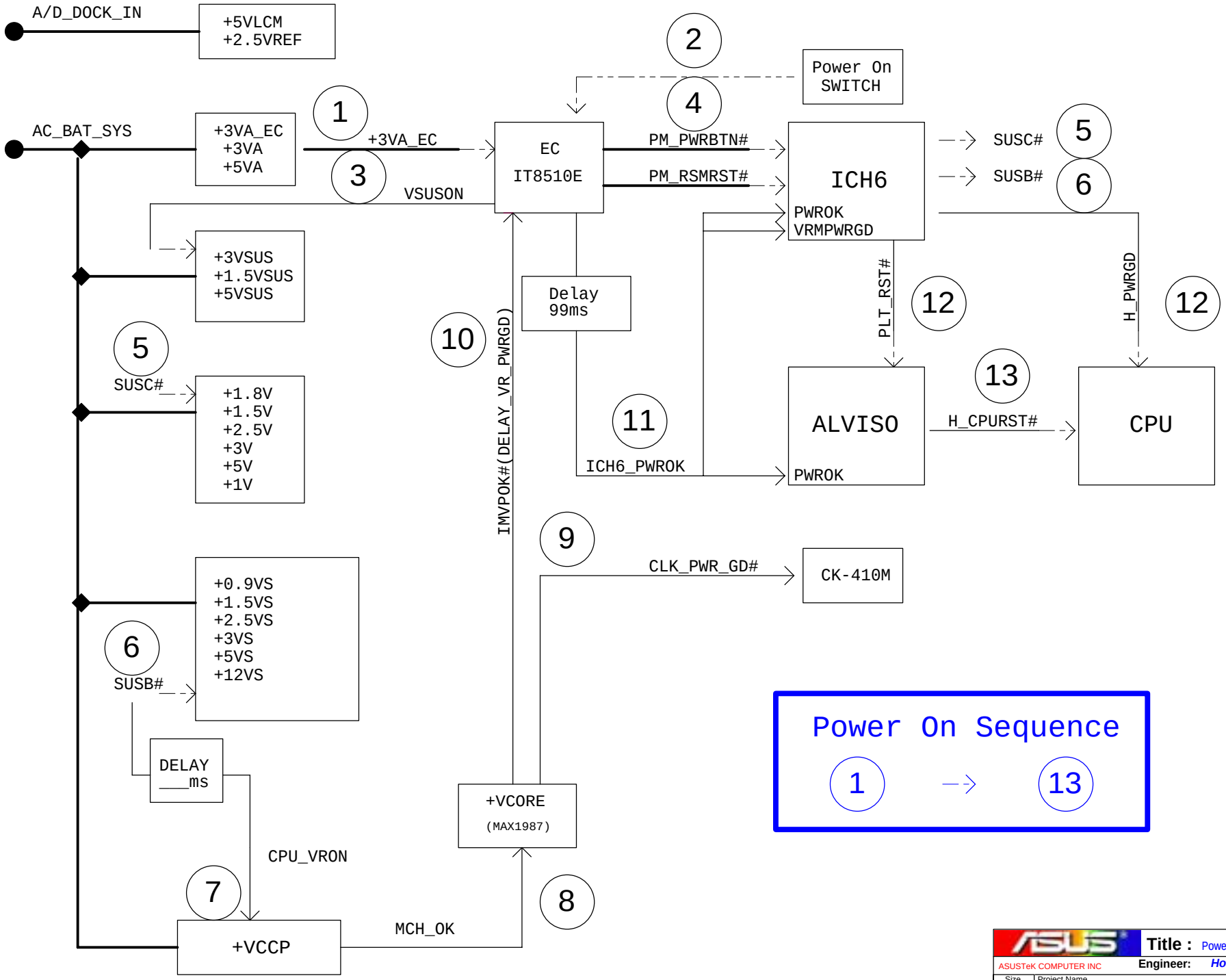




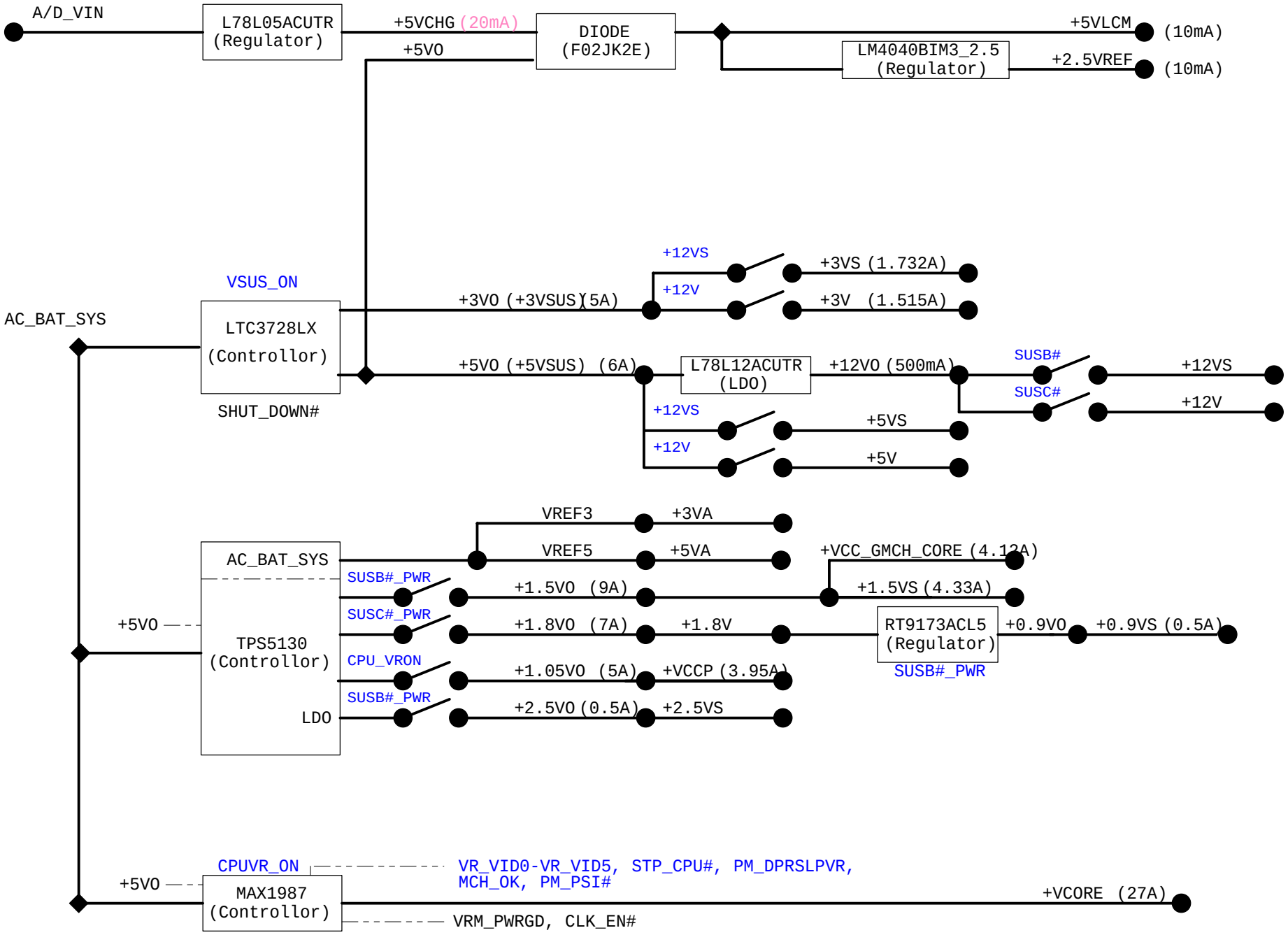
ASUSTeK COMPUTER INC	Title : BATLOW/SD#	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 45 of 54	



ASUSTeK COMPUTER INC	Title : LOAD SWITCH	
	Engineer: Adams Lin	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 46 of 54	



ASUSTeK COMPUTER INC	Title : Power On Sequence		
	Engineer: Howard Tu		
Size: Custom	Project Name: A3H		Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 47 of 54		



ASUSTeK COMPUTER INC	Title : POWER FLOWCHART	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 48 of 54	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

0221

ICH6-M GPIO	A5V	Note	Volt
GPI 0			+3VS
GPI 1			+3VS
GPI 2			+3VS
GPI 3			+3VS
GPI 4			+3VS
GPI 5			
GPI 7			+3VS
GPI 8	EXTSMI#		+3VSUS
GPI 11	LID_ICH#		+3VSUS
GPI 12	KB_SCI#		+3VSUS
GPI 13	SIO_SMI#		+3VSUS
GPI 14			+3VSUS
GPI 15			+3VSUS
GPO 16			
GPO 17			
GPO 19	PWRLED_1HZ		+3VS
GPO 21	BACK_OFF#		+3VS
GPO 23	FWH_WP#		+3VS
GPO 24	802_LED_EN#		+3VSUS
GPI 26	SATA_DET#0	Unused pull-up to Vcc3_3	+3VS
GPI 27			+3VSUS
GPI 28			+3VSUS
GPI 29	PCB_ID2	Default : 0	+3VS
GPI 30	PCB_ID0	Default : 0	+3VS
GPI 31	PCB_ID1	Default : 0	+3VS
GPI 33	CPUFAN_SPD_A		+3VS
GPO 34	WLAN_ON#		+3VS
GPI 40	PANEL_ID0		+3VS
GPI 41	PANEL_ID1		+3VS
GPO 48			
GPO 49			
GPIO 25	CB_SD#	Diode	+3V

KBC GPIO	A5V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	KBC_P21	
P20(Pin 38)	KBCRSM	
P42(Pin 23)	WATCHDOG	
P43(Pin 22)	OP_SD#	POSTCode前拉Low,ACPI前拉High,ACPI後放掉
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID1	
P52(Pin 15)	KID2	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)	FAN_DA1	
P57(Pin 10)	ADJ_BL	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

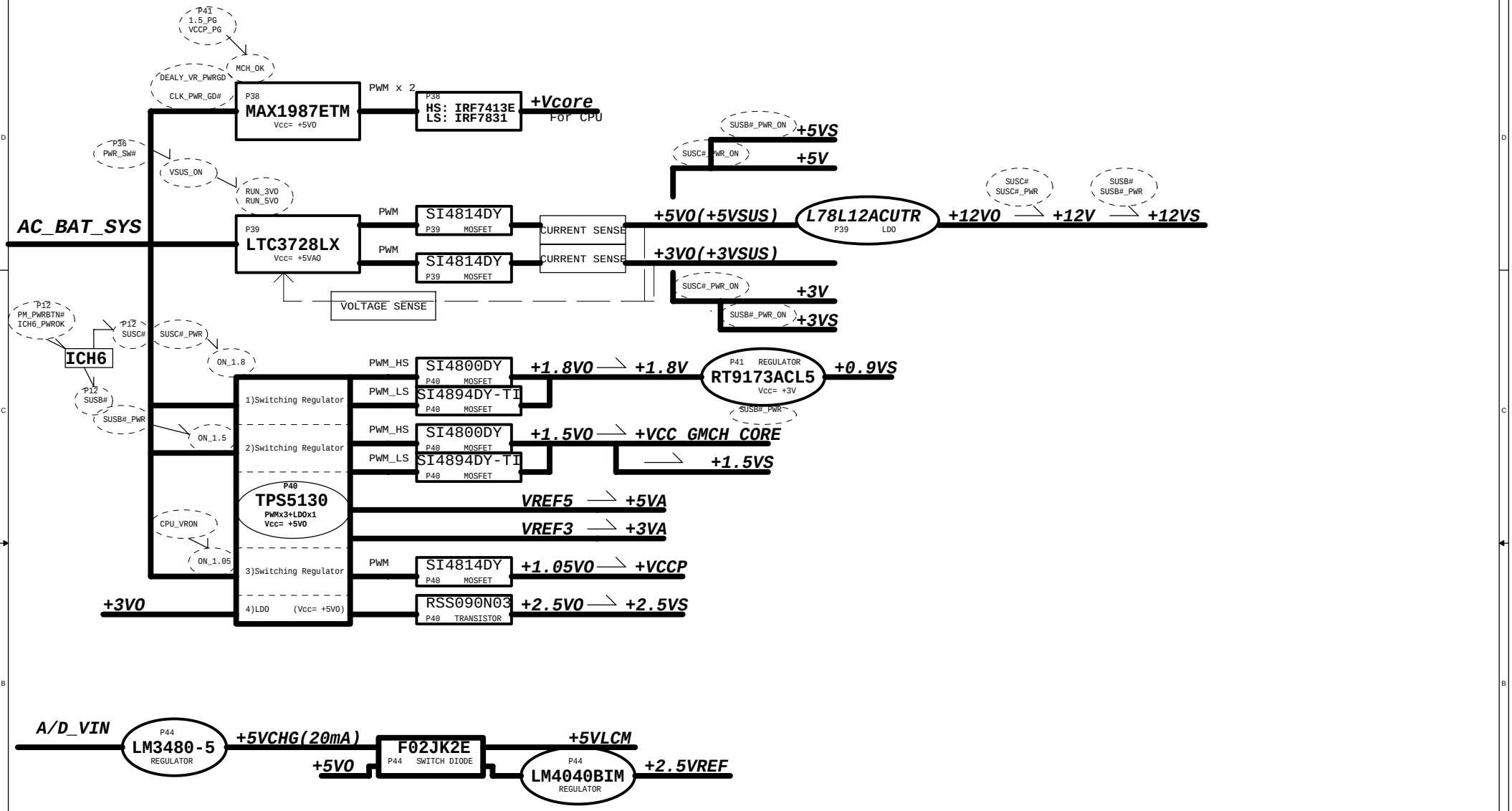
ASUSTeK COMPUTER INC

Title : System Resource

Engineer: Howard Tu

Size	Project Name	Rev
Custom	A3H	1.0

Date: Thursday, June 30, 2005 Sheet 49 of 54



ASUSTeK COMPUTER INC	Title : Power Flow Diagram	
	Engineer: Quan-Tai Lin	
Size: Custom	Project Name: A3H	Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 50 of 54	

Rev.	Data	Description
1.0	04' 10/22	Initial release
1.1	04' 11/08	R193 not insert L63 not insert and mount L64 Q67 & Q69 not insert Modify CON4 pin assignment Mount R230 100K Ohm P/N 10-004401040 R94 & R95 not insert Modify Q71, Q77 & Q101 pin 5 & 6 signals C421 & C423 change value from 47pF to 27 pF P/N 11-034027042 C117 & C120 change value from 18pF to 24 pF P/N 11-033024000 R318 change value from 14.3 K to 20 K P/N 10-003412030
	04' 12/02	R141 not insert Delete R160 and add D72 and D73 (all not insert) R252 not insert and mount R247 Delete D33 and add D71 Net name "IDE_PDASP#2" change to "IDE_PDASP#" R504 change value from 100 K to 10 K P/N 10-003401030 Mount R412 Delete R166, Q32 and D20
	04' 12/06	Add R653 0 Ohm between U36-AD30 and "ICH6_PWROK" R47 & R53 not insert Mount R387 & R391 R41-1 change signal from "+3VS" to "+5VSUS" C192 change value from 0.1 uF to 0.22 uF P/N 11-033122400 R311 not insert and mount R310 CON5-18 change signal from "+5V" to "+5VSUS" Modify POWER & Audio DJ LED Circuit: Delete Q56 Add U52, Q125, Q126, Q128, D69, D70, D74, C645 & C646 Add R647, R648, R649, R650, R651, R652, R654 & R655 Delete Q32 & R166 and Q31-5 chang signal to "SUSC_PWR" Delete D20 D53-1 change signal from "PM_PWRBTN" to "PWR_SW_EN" ~~Q108 not insert~~ Modify Start-Up Circuit: Add D67, Q124, Q127, R644, R645 & C644 Add D68 & R646 but not insert R341 change value from 11 K to 1 K P/N 10-003411020 C341 change value from 0.47 uF to 0.047 uF P/N 11-033147320 Modify CPU_VCCA0 & CPU_VCCA123 Select Circuit: Add Q122, Q123, R642, R643 & R657 Q24-2 & Q24-5 change signal from "CPU_BSEL0" to "VCCA_SEL" R394 & R399 change value from 0 Ohm to 1K Ohm P/N 09-013103013
	04' 12/07	Add R656 & Q129 and U1 & U7 pin4 connect with "USB_EN#"
	04' 12/09	Delete D22 & signal "CODEC_SD#" connect with R135-2 Delete R136 & move C183 to conect with U13-5
	04' 12/13	Move R124 to conect with U13-5 & "DELAY_VR_PWRGD" Change value to 390K Ohm P/N 10-003403940 C183 change value to 0.22 uF P/N 11-033122400 CE27 & CE28 change package type to P/N 11-176247651 CE1 & CE22 change package type to P/N 11-17D210751 CN6 change package type to P/N 12-10110025I

Rev.	Data	Description
1.1	04' 12/13	CON9 change package type to P/N 12-101102154 Mount R120 0 Ohm P/N 10-003400000 Mount L50 0 Ohm P/N 10-003400000 Mount C250 0.1uF P/N 11-034310410
	04' 12/15	R517 change value from 1K Ohm to 1M Ohm P/N 10-003401050 C499 change value from 0.1uF to 0.22uF P/N 11-033122400
	04'12/24	BAT holder P/N: 12-201110121, not temp_5182_rw50
1.2	04'12/27	RN8 ,RN9 ,RN10 ,RN11 ,RN14 P/N Change to 10-064805600 from 10-805600NV
	04'12/27	MDC P/N changes to 12-270101201,not temp_5182_rw49
	05'01/02	Add a diode D? to fix leakage current for power switch's LED (LED1)
	05'01/02	1) Modify the pin3 schematic of U52A (flipflop) 2) Add a resistance R? and a 2N7002 Q?
	05'01/02	1) Modify the pin11 schematic of U16B (flipflop) 2) Add a resistance R? and a UM6K1N Q127B
	05'01/03	ICH6 GPI(GPIO)41 pull high to +3VS with 8.2K ohm R? (P/N:10-004408220)
	05'01/03	LID_KBC# signal pull high to +3V,not +3VSUS
	05'01/03	LED[2..5] pull high to +5VS and change P/N to 07-015700246 as same as M7V
	05'01/03	Delete repeating limit resistance R269 100ohm
	05'01/05	R139 no mount and R109 value change to 1Mohm and P/N is 10-003401050
	05'01/05	R73,R75,R76,R77 change to 330ohm and P/N is 10-003413310
	05'01/05	H17,H18,H23,H24,H25 have to mount

ASUSTeK COMPUTER INC

Title : HISTORY

Engineer: Howard Tu

Size	Project Name	Rev
A3	A3H	1.0

Date: Thursday, June 30, 2005 Sheet 51 of 54

Rev.	Data	Description
1.0	04' 10/22	Initial release
Rev1.2	05' 01/05	Add D? to connect RUN_3VO,RUN_5VO to SHUT_DOWN#
	05' 01/05	TPS5130 pin10.11 are with R344.R345 to connect to AC_BAT_SYS signal
	05' 01/05	R667.1 connect to +5VCHG R671 no mount C? 0.1UF no mount and add a R?47Kohm D83 no mount and add R? 0ohm R666 no mount R677 value change to 110Kohm R678 value change to 23.2Kohm R698 value change to 49.9Kohm R700 value change to 150Kohm Q137change to IRLML2402, add a R? 9.76Kohm, and R672.1 connect to AC_BAT_SYS U53.29 pull ground Add C? and C? 10UF Delete Q131 to change to D? U32.3 connect to A/D_VIN Change adapter in circuit
	05' 06/22	

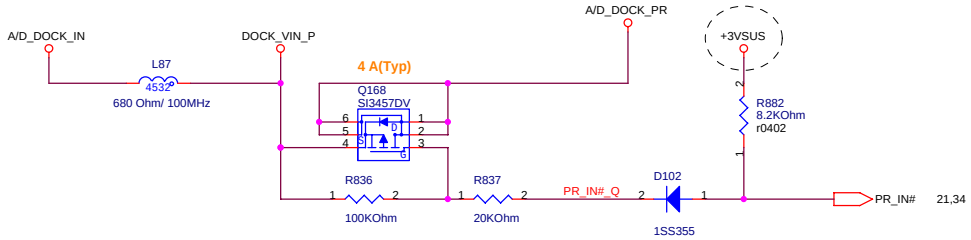
ASUSTeK COMPUTER INC

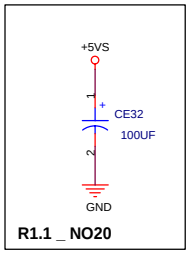
Title : HISTORY(PWR)

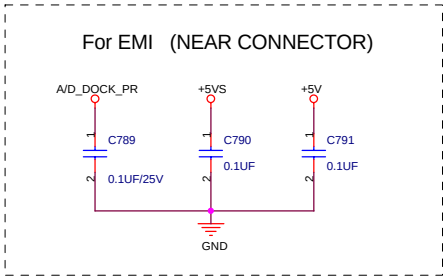
Engineer: *Howard Tu*

Size	Project Name	Rev
Custom	A3H	1.0

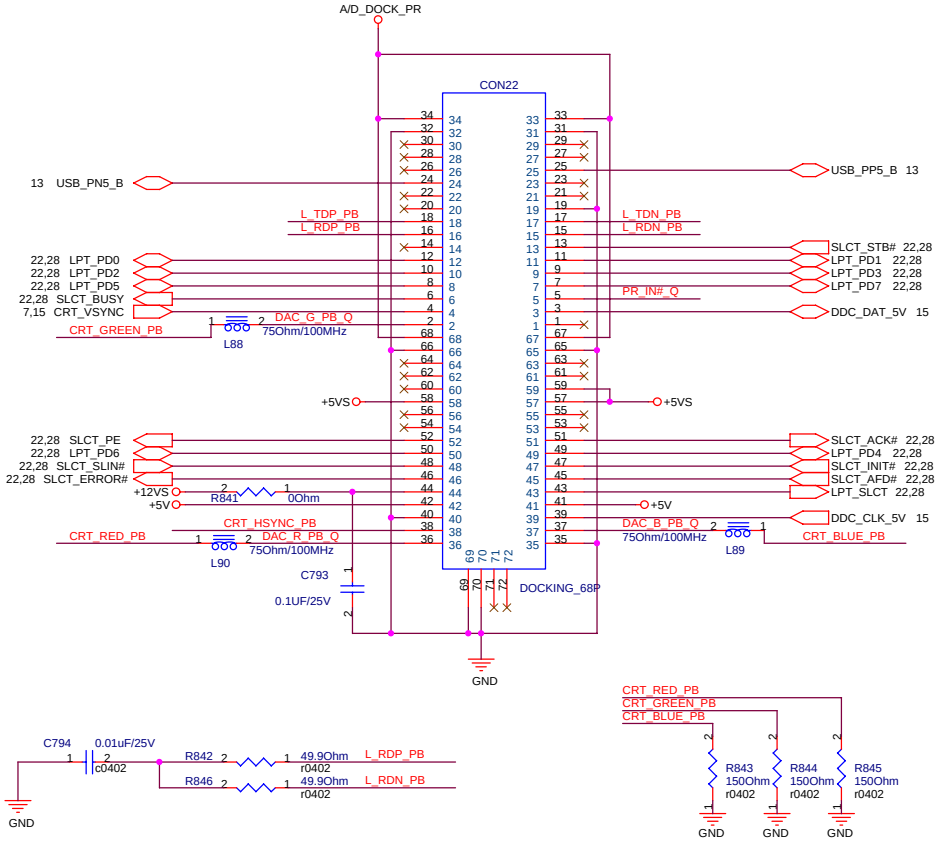
Date: Thursday, June 30, 2005 Sheet 52 of 54







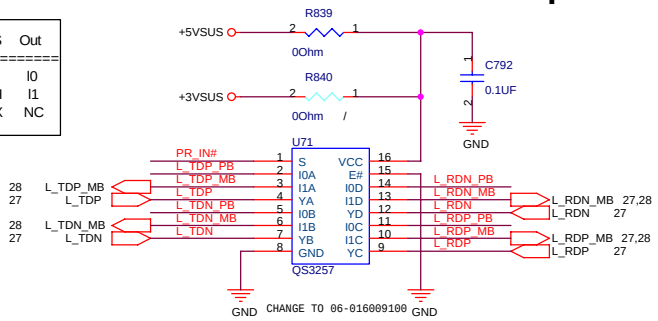
PORT BAR III



LAN Switch

OE	S	Out
L	L	I0
L	H	I1
H	X	NC

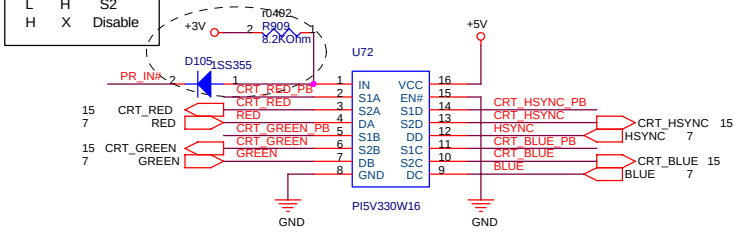
Place near LAN chip!



CRT Switch

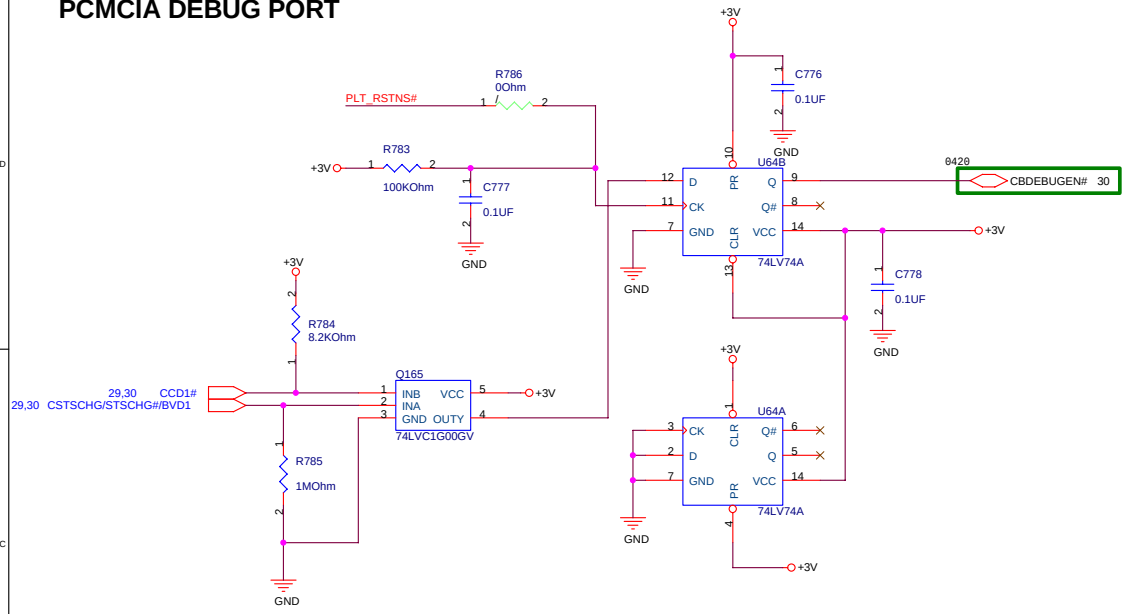
OE#	IN	Out
L	L	S1
L	H	S2
H	X	Disable

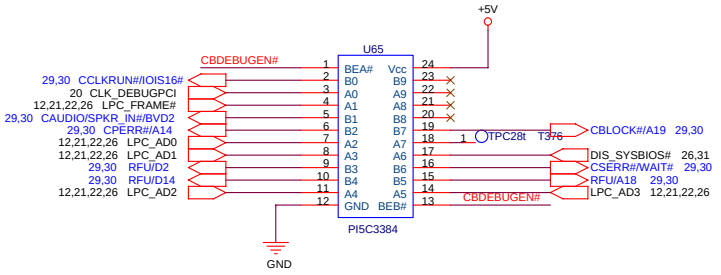
Place near Alviso !

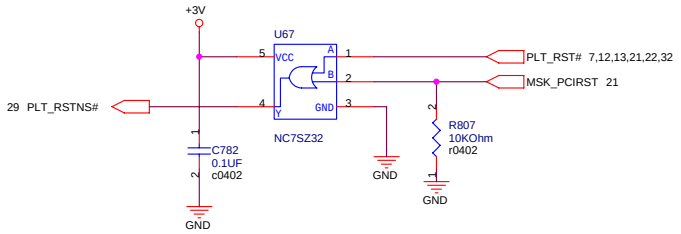


ASUSTek COMPUTER INC	Title : Port Bar		
	Engineer: Howard Tu		
Size: Custom	Project Name: A3H		Rev: 1.0
Date: Thursday, June 30, 2005	Sheet 53 of 54		

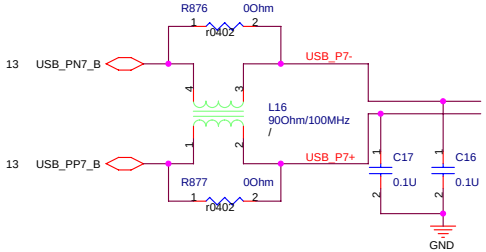
PCMCIA DEBUG PORT



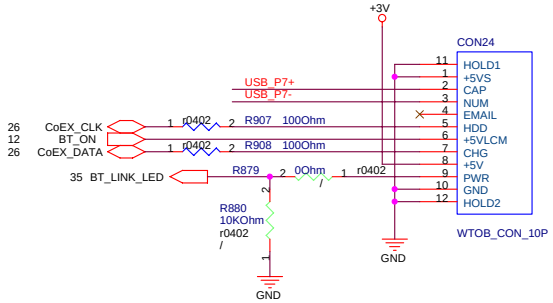




Bluetooth



For Intel Wireless
CoExistence System



ASUSTek COMPUTER INC

Title : Debug Part

Engineer: Howard_Tu

Size	Project Name	Rev
Custom	A3H	1.0

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