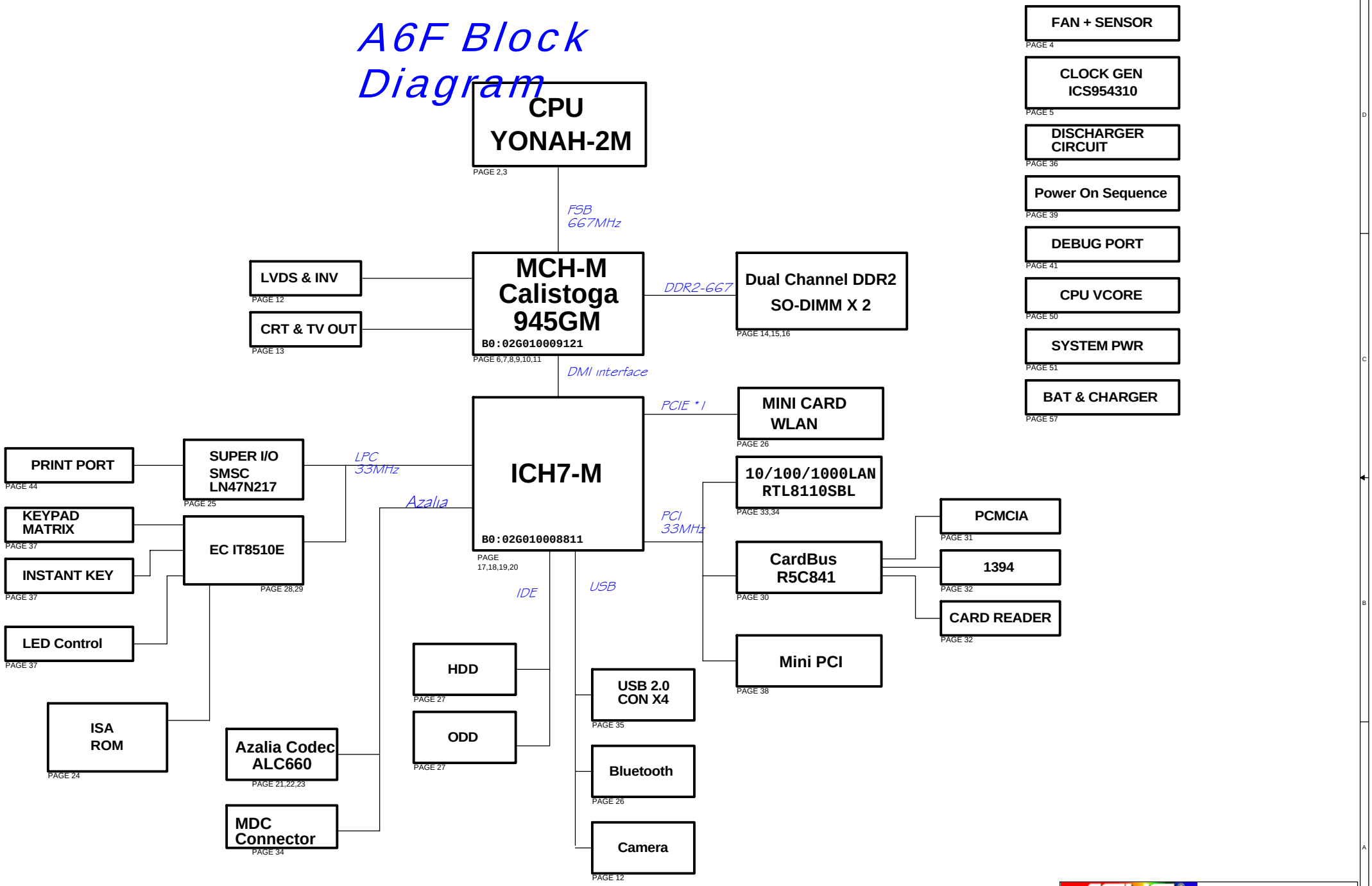
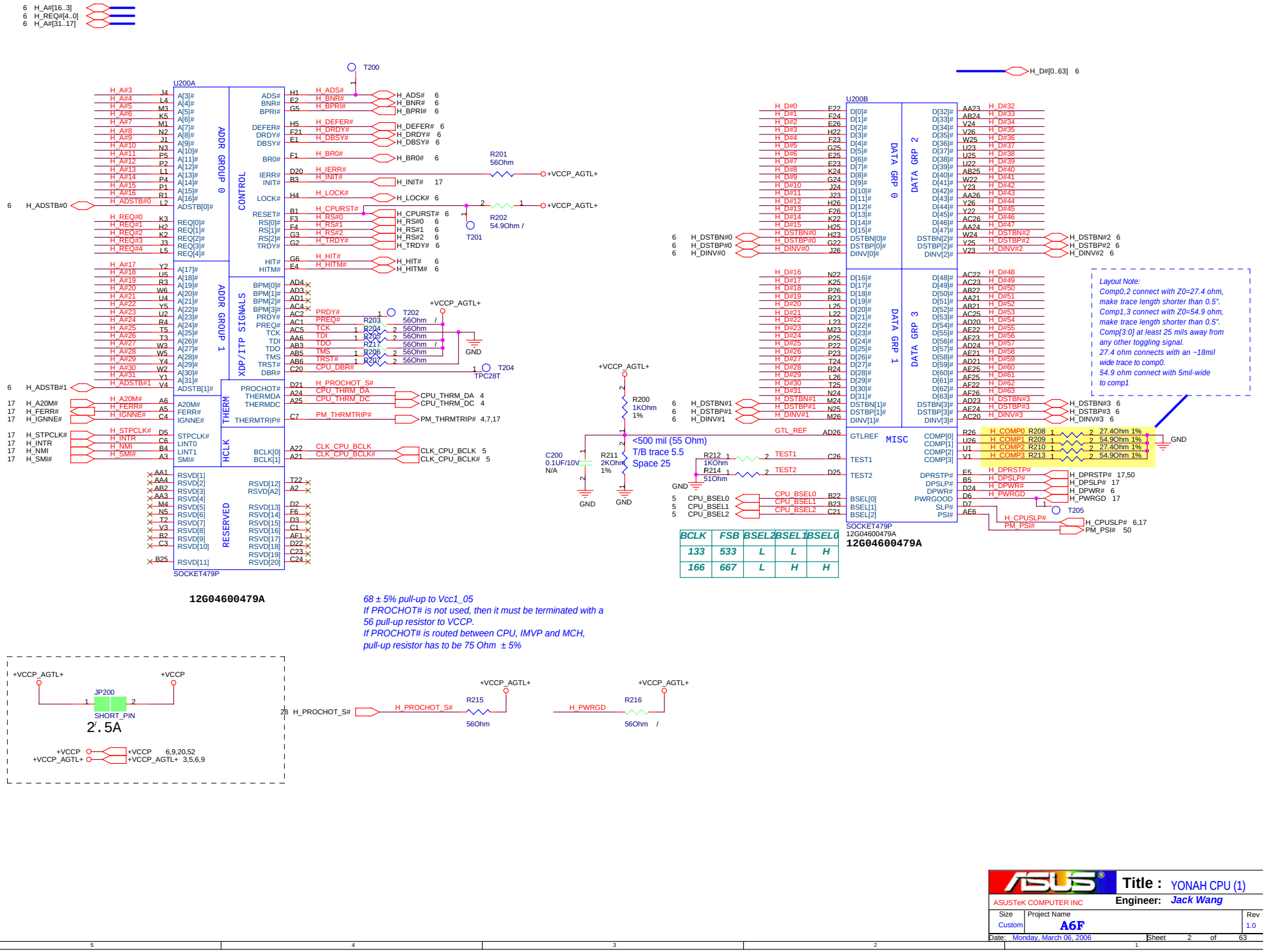
A6F Block Diagram



ASUSTeK COMPUTER INC	Title : BLOCK DIAGRAM	
	Engineer: Jack WANG	
Size: A3	Project Name: A6F	Rev: 1.1
Date: Monday, March 06, 2006	Sheet 1 of 63	

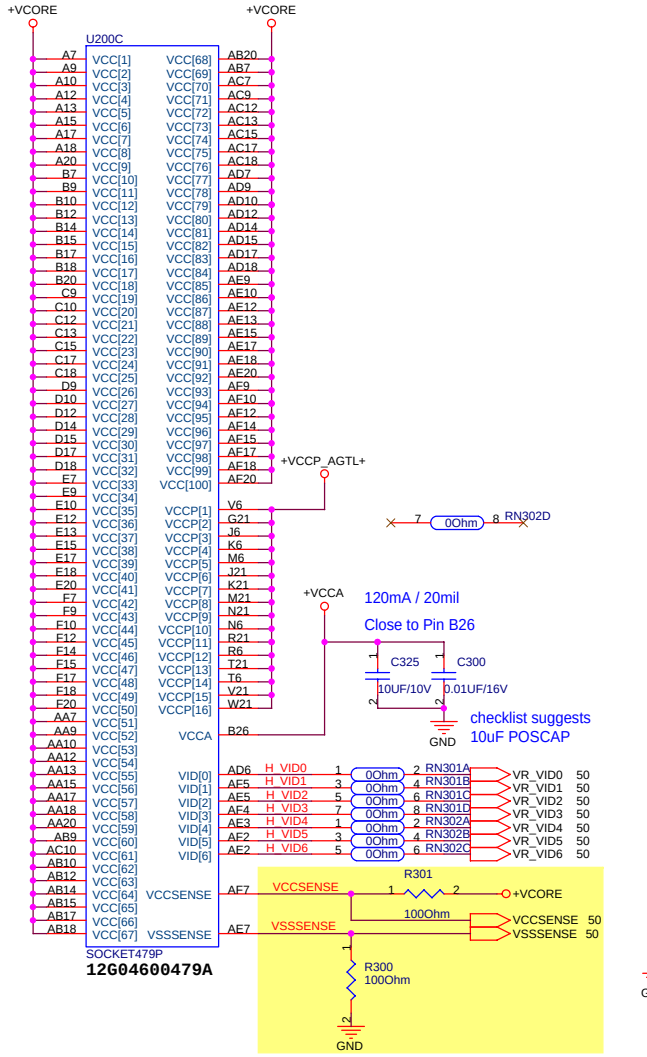


BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

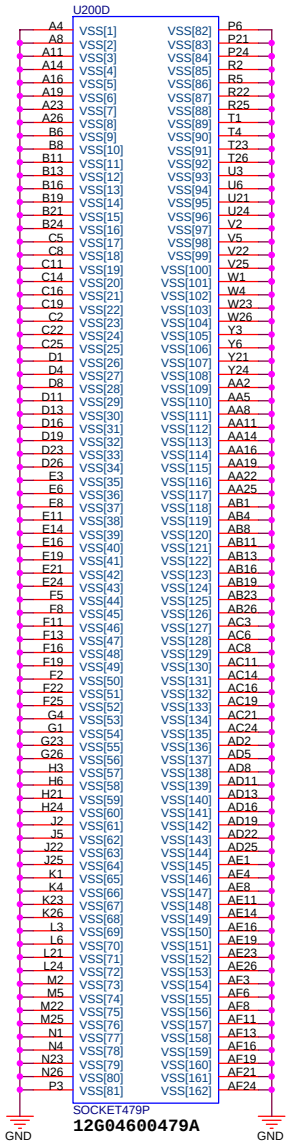
ASUSTeK COMPUTER INC	Title : YONAH CPU (1)			
	Engineer: Jack Wang			
Size: Custom	Project Name: A6F			Rev: 1.0
Date: Monday, March 06, 2006	Sheet 2 of 63			

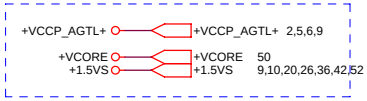
YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

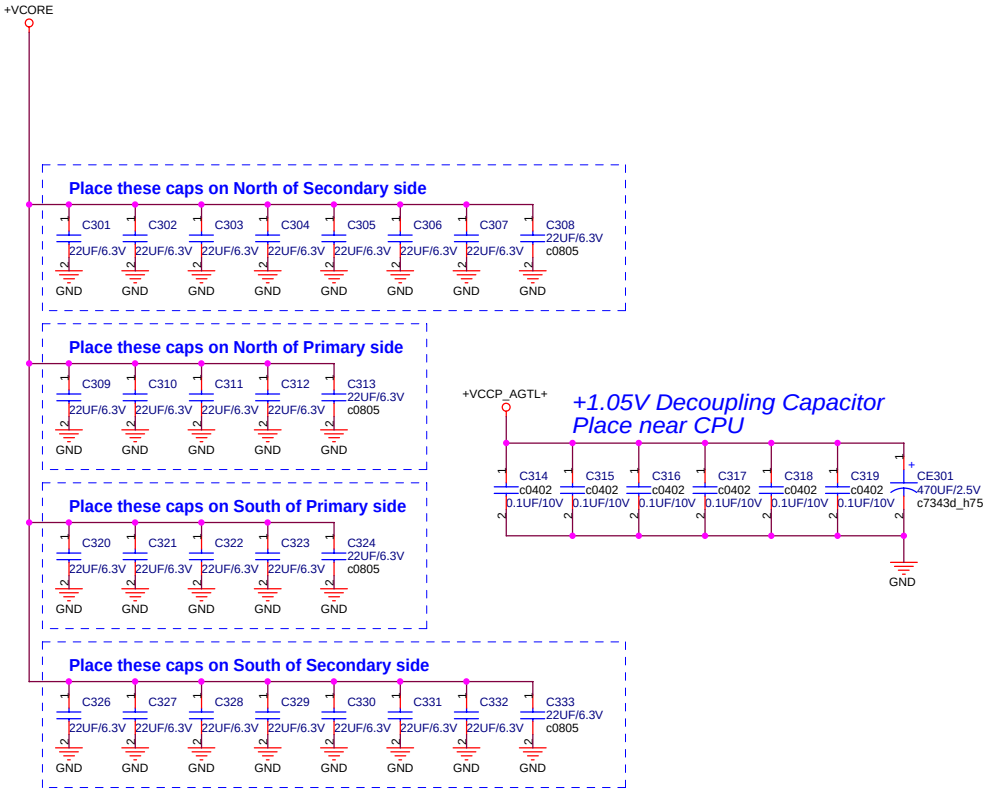
YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.







ASUSTeK COMPUTER INC		Title :	Yonah CPU (2)
		Engineer:	*Jack Wang*
Size	Project Name		Rev
A3	**A6F**		1.0
Date:	Monday, March 06, 2006	Sheet	3 of 63

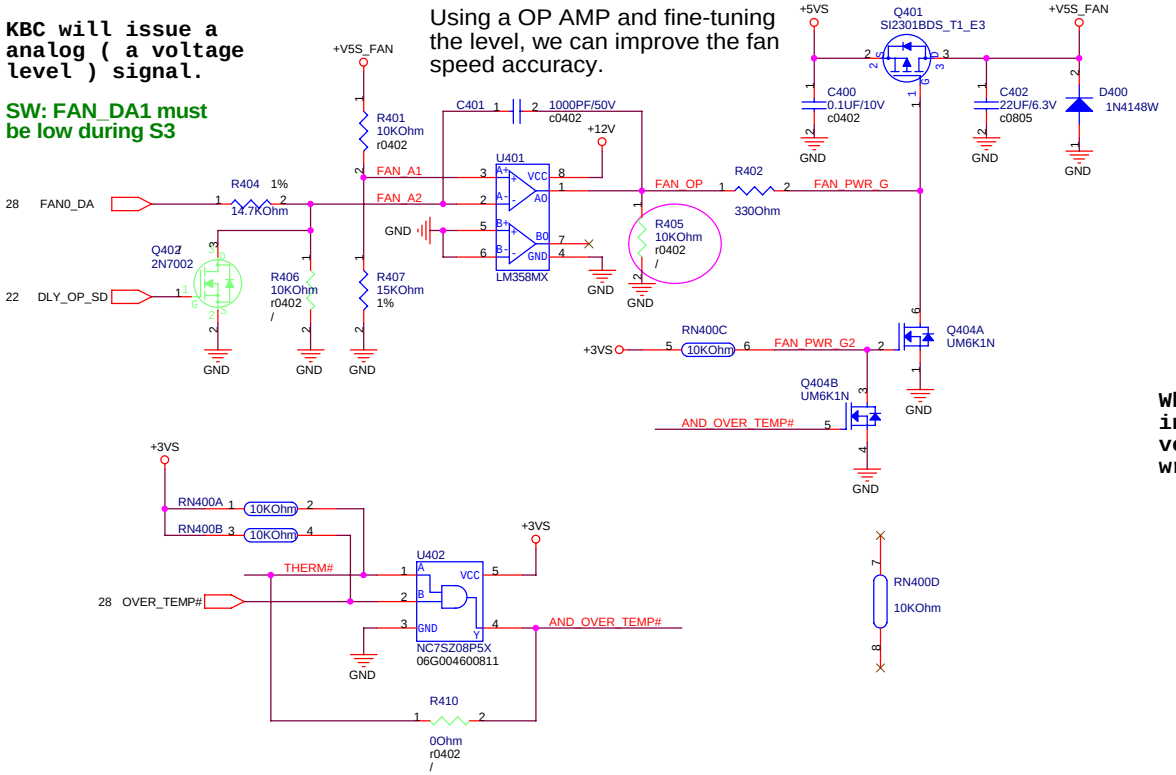
Fan Speed Control

+12V	+12V	32,36,61
+5VS	+5VS	13,19,20,21,22,27,28,36,37,38,44,50,61
+3VS	+3VS	5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61
+3VA	+3VA	12,20,28,37,39,54,59,63

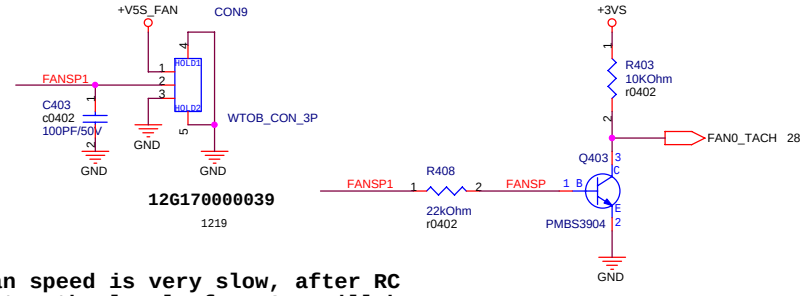
KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

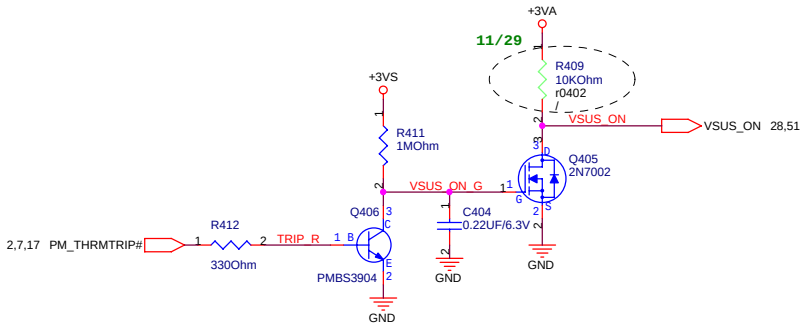
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.



CPU FAN



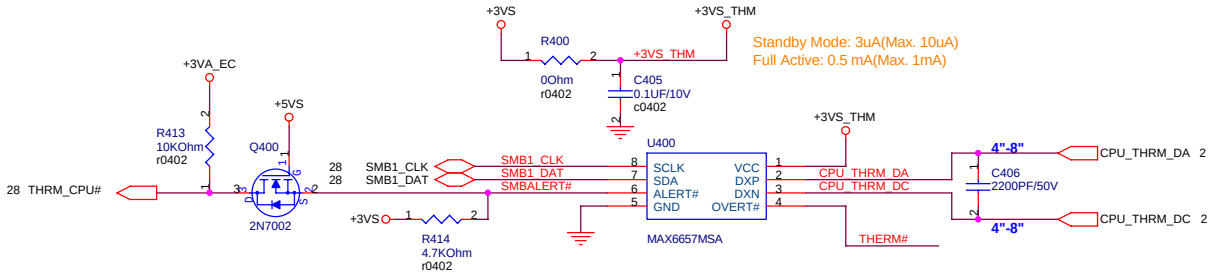
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.



Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



ASUSTeK COMPUTER INC	Title : THER-SENSOR,FAN		
	Engineer: Jack Wang		
Size: A3	Project Name: A6F		Rev: 1.0
Date: Monday, March 06, 2006	Sheet 4 of 63		

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	CLK_MCH_3GPLL(#)

Bclk	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ +VCCP_AGTL+ 2,3,6,9

+3VS +3VS 4,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61

Layout Note:
Place termination close to source IC

Pin34 is PWRSAVE#

SELPCIE0_LCD#:
0-->pin17,pin18=LCDCLK(96MHz) or
27M/27M_SS

SELLCD_27#/PCICLK_F1:
1-->pin17,pin18=LCDCLK(96MHz)

PCICLK2/REQ_SEL:
1-->pin40,pin41=PREQ1#,PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

Realtek:Mount R519,Remove R550 R534

PREQ#1
0=PCIEX 6/0 Not Controlled
1=PCIEX 6/0 Controlled

PREQ#2
0=PCIEX 8/1 Not Controlled
1=PCIEX 8/1 Controlled

PREQ#3
0=PCIEX 4/2 Not Controlled
1=PCIEX 4/2 Controlled

PREQ#4
0=PCIEX 7/5/3 Not Controlled
1=PCIEX 7/5/3 Controlled

2/23/06

2/23/06

Internal Pull-Up Resistor

Internal Pull-Down Resistor

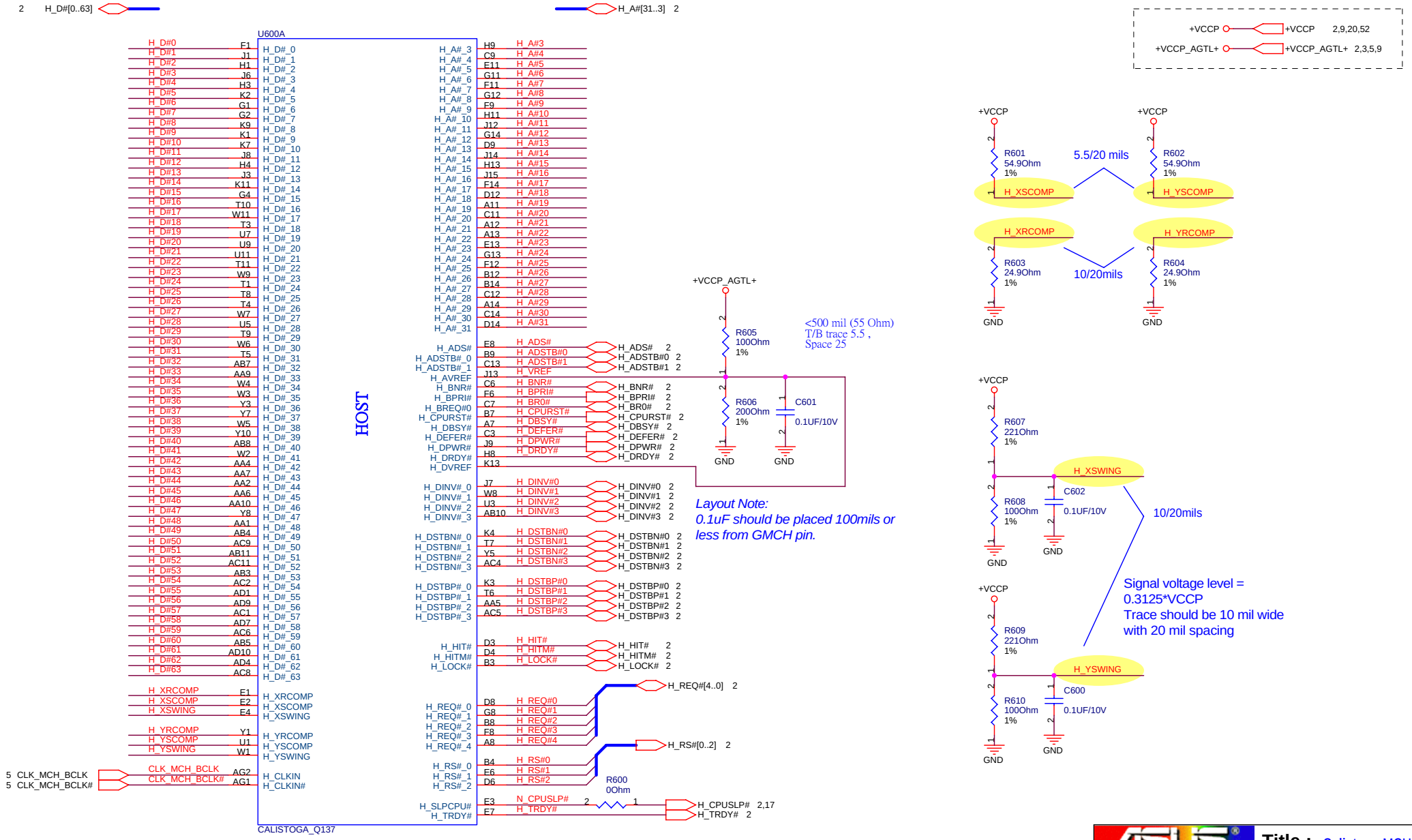
ASUSTeK COMPUTER INC

Title : CLOCK GEN

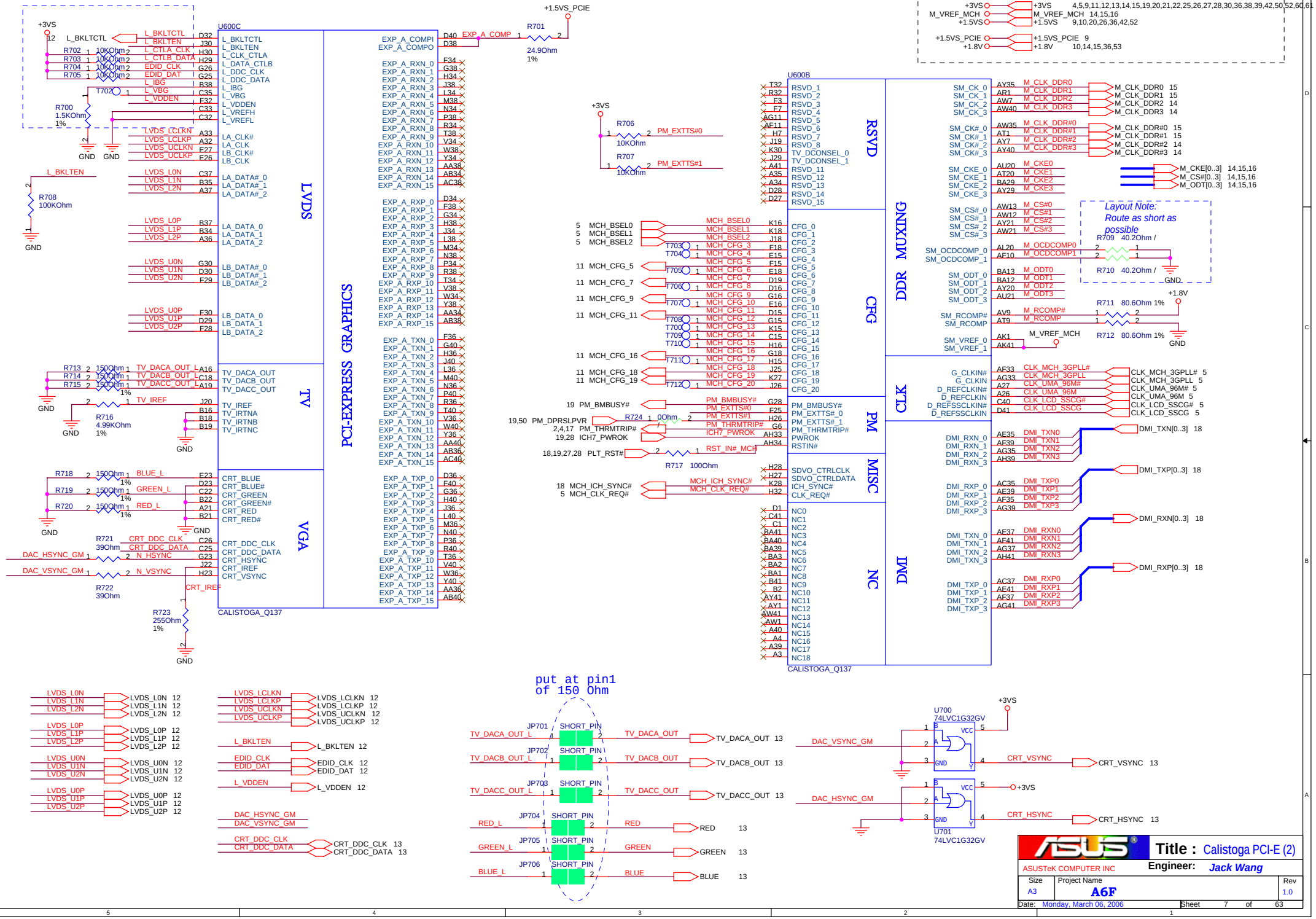
Engineer: Jack Wang

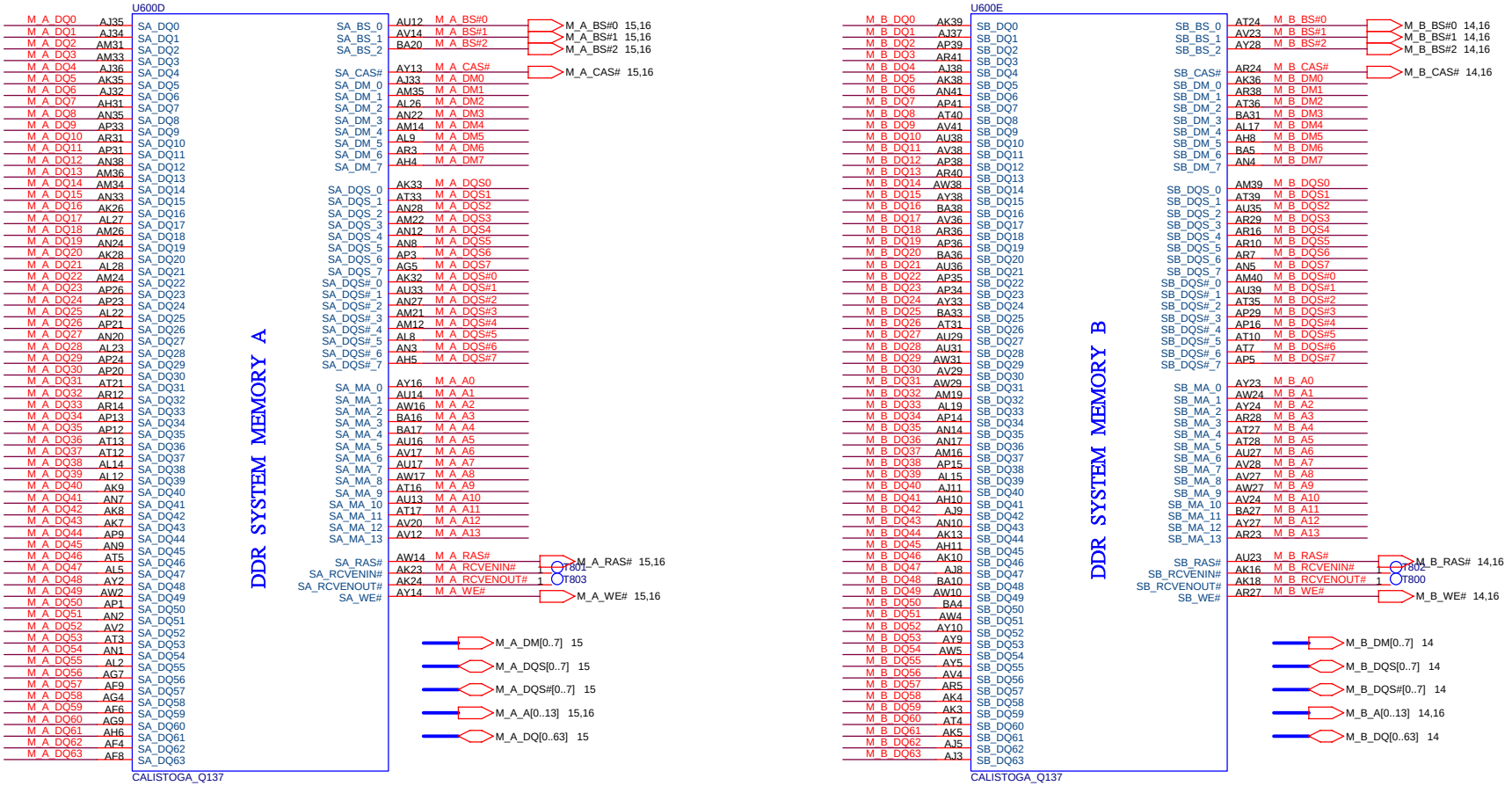
Size	Project Name	Rev
Custom	A6F	1.1

Date: Monday, March 06, 2006 Sheet 5 of 63



ASUSTeK COMPUTER INC	Title : Calistoga MCH (1)		
	Engineer: Jack Wang		
Size: B	Project Name: A6F		Rev: 1.0
Date: Monday, March 06, 2006	Sheet 6 of 63		


U600C
CALISTOGA_Q137
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
U600B
RSVD
CFG
DDR MUXING
CLK
PM
MISC
NC
DMI
Layout Note:
Route as short as possible
put at pin1
of 150 Ohm
SHORT_PIN
U700
74LVC1G32GV
U701
74LVC1G32GV
Title : Calistoga PCI-E (2)
ASUSTeK COMPUTER INC
Engineer: Jack Wang
Size A3
Project Name A6F
Rev 1.0
Date: Monday, March 06, 2006
Sheet 7 of 63



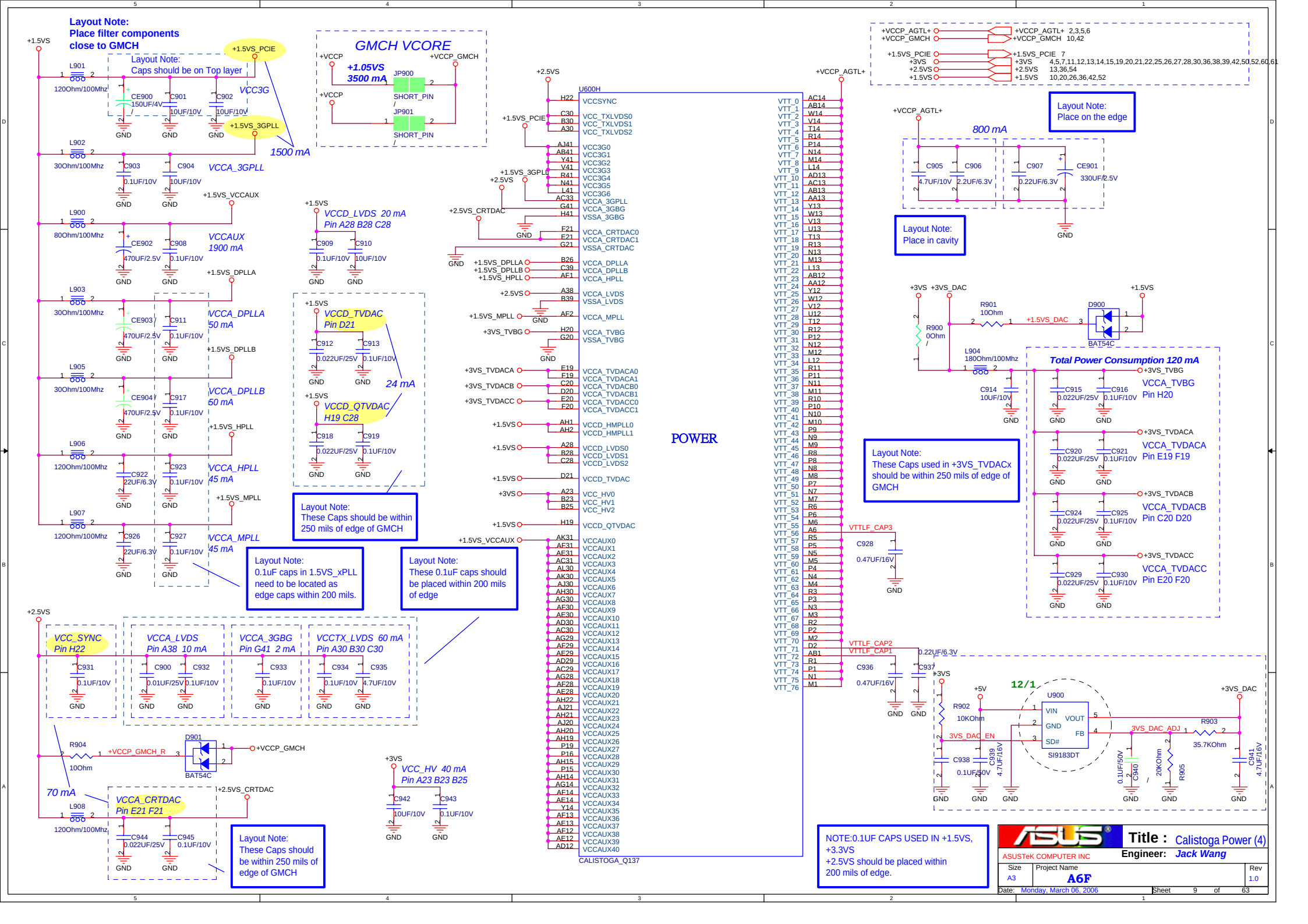
ASUSTeK COMPUTER INC

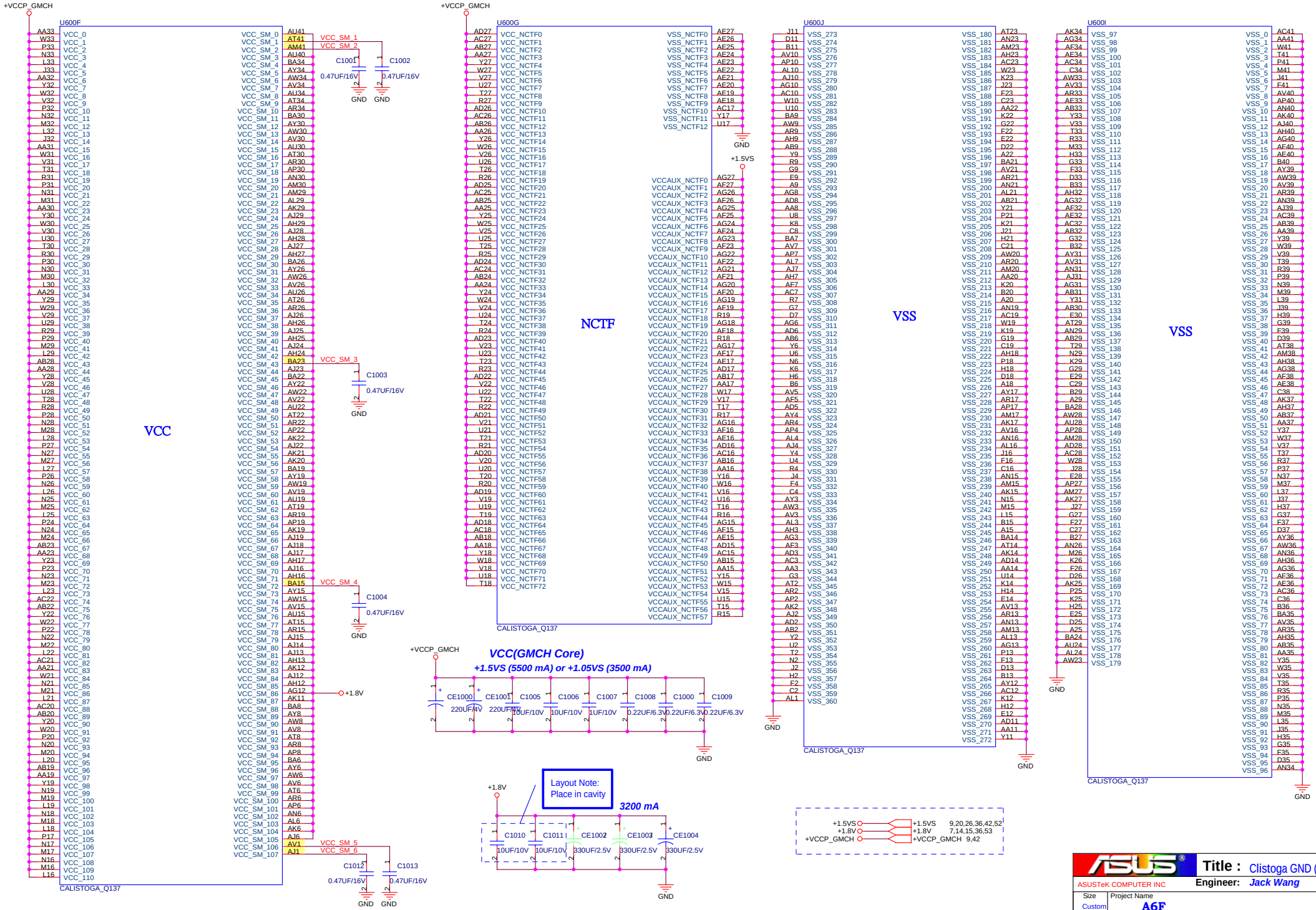
Title : Calistoga DDR2 (3)

Engineer: *Jack Wang*

Size	Project Name	Rev
A3	**A6F**	1.0

Date: Monday, March 06, 2006 Sheet 8 of 63


Layout Note:
Place filter components
close to GMCH
Layout Note:
Caps should be on Top layer
+1.5VS_PCIE
VCC3G
+1.5VS_3GPLL
1500 mA
VCCA_3GPLL
+1.5VS_VCCAUX
VCCAUX
1900 mA
+1.5VS_DPLLA
VCCA_DPLLA
50 mA
+1.5VS_DPLLB
VCCA_DPLLB
50 mA
+1.5VS_HPLL
VCCA_HPLL
45 mA
+1.5VS_MPLL
VCCA_MPLL
45 mA
Layout Note:
0.1uF caps in 1.5VS_xPLL
need to be located as
edge caps within 200 mils.
GMCH VCORE
+1.05VS
3500 mA
JP900
JP901
SHORT_PIN
VCCD_LVDS 20 mA
Pin A28 B28 C28
VCCD_TVDAC
Pin D21
24 mA
VCCD_QTVDAC
H19 C28
Layout Note:
These Caps should be within
250 mils of edge of GMCH
Layout Note:
These 0.1uF caps should
be placed within 200 mils
of edge
U600H
CALISTOGA_Q137
POWER
VCC_SYNC
Pin H22
VCCA_LVDS
Pin A38 10 mA
VCCA_3GBG
Pin G41 2 mA
VCCTX_LVDS 60 mA
Pin A30 B30 C30
VCC_HV 40 mA
Pin A23 B23 B25
70 mA
VCCA_CRTDAC
Pin E21 F21
Layout Note:
These Caps should
be within 250 mils of
edge of GMCH
+VCCP_AGTL+ 2,3,5,6
+VCCP_GMCH 10,42
+1.5VS_PCIE 7
+3VS 4,5,7,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61
+2.5VS 13,36,54
+1.5VS 10,20,26,36,42,52
800 mA
Layout Note:
Place on the edge
Layout Note:
Place in cavity
Total Power Consumption 120 mA
VCCA_TVBG
Pin H20
VCCA_TVDACA
Pin E19 F19
VCCA_TVDACB
Pin C20 D20
VCCA_TVDACC
Pin E20 F20
Layout Note:
These Caps used in +3VS_TVDACx
should be within 250 mils of edge of
GMCH
NOTE:0.1UF CAPS USED IN +1.5VS,
+3.3VS
+2.5VS should be placed within
200 mils of edge.
Title : Calistoga Power (4)
ASUSTeK COMPUTER INC
Engineer: Jack Wang
Size A3
Project Name A6F
Rev 1.0
Date: Monday, March 06, 2006
Sheet 9 of 63


+VCCP_GMCH
U600F
VCC_0
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
VCC_36
VCC_37
VCC_38
VCC_39
VCC_40
VCC_41
VCC_42
VCC_43
VCC_44
VCC_45
VCC_46
VCC_47
VCC_48
VCC_49
VCC_50
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VCC_52
VCC_53
VCC_54
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VCC_57
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VCC_59
VCC_60
VCC_61
VCC_62
VCC_63
VCC_64
VCC_65
VCC_66
VCC_67
VCC_68
VCC_69
VCC_70
VCC_71
VCC_72
VCC_73
VCC_74
VCC_75
VCC_76
VCC_77
VCC_78
VCC_79
VCC_80
VCC_81
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VCC_86
VCC_87
VCC_88
VCC_89
VCC_90
VCC_91
VCC_92
VCC_93
VCC_94
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VCC_97
VCC_98
VCC_99
VCC_100
VCC_101
VCC_102
VCC_103
VCC_104
VCC_105
VCC_106
VCC_108
VCC_109
VCC_110
VCC
CALISTOGA_Q137
VCC_SM_0
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
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VCC_SM_103
VCC_SM_104
VCC_SM_105
VCC_SM_106
VCC_SM_107
C1001
C1002
C1003
C1004
C1012
C1013
0.47UF/16V
GND
+1.8V
+VCCP_GMCH
U600G
VCC_NCTF0
VCC_NCTF1
VCC_NCTF2
VCC_NCTF3
VCC_NCTF4
VCC_NCTF5
VCC_NCTF6
VCC_NCTF7
VCC_NCTF8
VCC_NCTF9
VCC_NCTF10
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VSS_NCTF7
VSS_NCTF8
VSS_NCTF9
VSS_NCTF10
VSS_NCTF11
VSS_NCTF12
GND
+1.5VS
VCCAUX_NCTF0
VCCAUX_NCTF1
VCCAUX_NCTF2
VCCAUX_NCTF3
VCCAUX_NCTF4
VCCAUX_NCTF5
VCCAUX_NCTF6
VCCAUX_NCTF7
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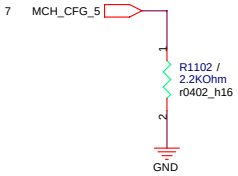
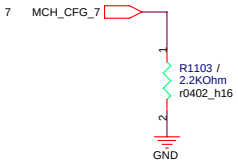
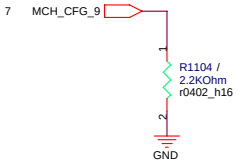
VCC(GMCH Core)
+1.5VS (5500 mA) or +1.05VS (3500 mA)
CE1000
CE1001
C1005
C1006
C1007
C1008
C1000
C1009
220UF/4V
10UF/10V
0.22UF/6.3V
Layout Note:
Place in cavity
3200 mA
C1010
C1011
CE1002
CE1003
CE1004
330UF/2.5V
+1.5VS 9,20,26,36,42,52
+1.8V 7,14,15,36,53
+VCCP_GMCH 9,42
ASUSTeK COMPUTER INC
Title : Clistoga GND (5)
Engineer: Jack Wang
Size Custom
Project Name A6F
Rev 1.0
Date: Monday, March 06, 2006
Sheet 10 of 63



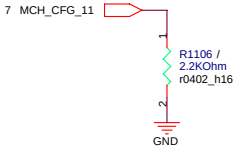
CFG5 : DMI X2 Select
LOW = DMI X 2
HIGH = DMI X 4 (Default)



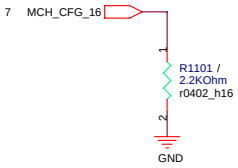
CFG7 : CPU STRAP
LOW = Reserved
HIGH = Mobility CPU (Default)



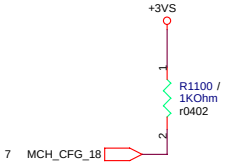
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



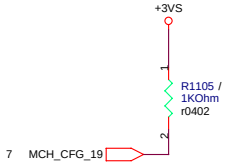
CFG11 : Reserved but need to be pull low



CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



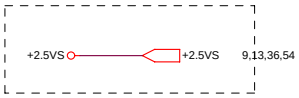
CFG18 : GMCH Core Voltage Level
LOW = 1.05V
HIGH = 1.5V (default)



CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

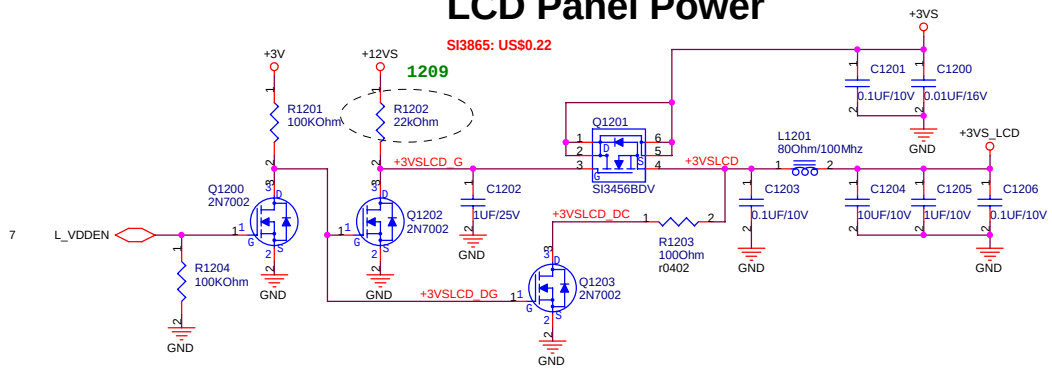
CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



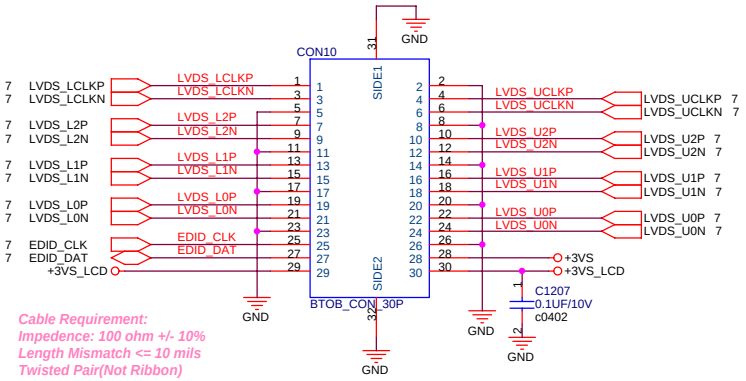
ASUSTeK COMPUTER INC
Title : Calistoga Strapping
Engineer: Jack Wang
Size: Custom | Project Name: A6F | Rev: 1.0
Date: Monday, March 06, 2006 | Sheet 11 of 63

LCD Panel Power

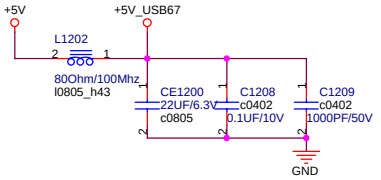
3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)



LCD LVDS Interface



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



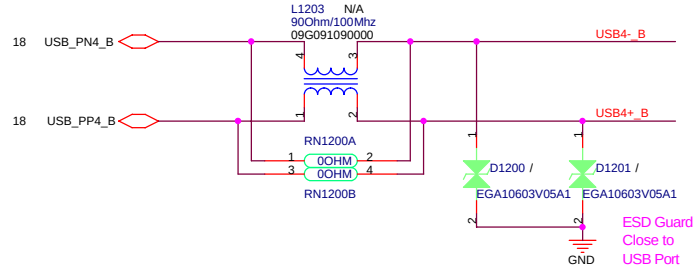
LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to adjust backlight

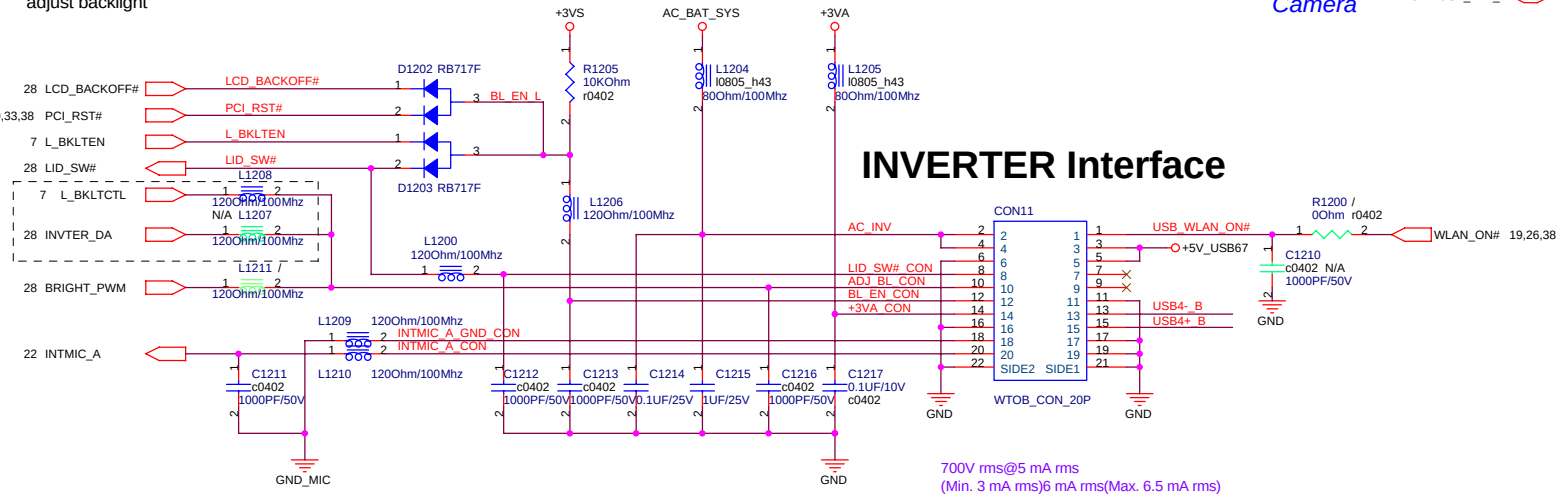
Inverter Board built in 14.1W LCD Panel

USB4 For CMOS Camera



ESD Guard Close to USB Port

INVERTER Interface



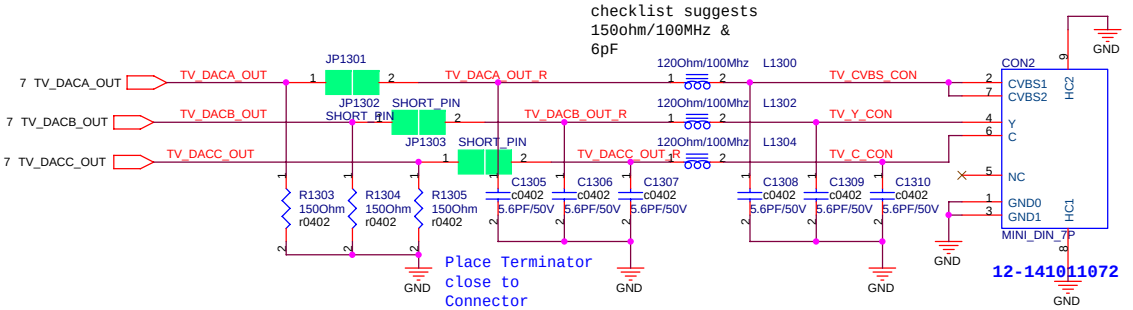
700V rms@5 mA rms
(Min. 3 mA rms)6 mA rms(Max. 6.5 mA rms)

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER		
	Engineer: Jack Wang		
Size: A3	Project Name: A6F		Rev: 1.1
Date: Monday, March 06, 2006	Sheet 12 of 63		

TV OUT

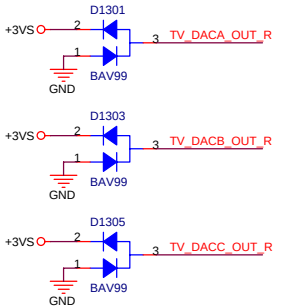
12G14101107D

checklist suggests
150ohm/100MHz &
6pF

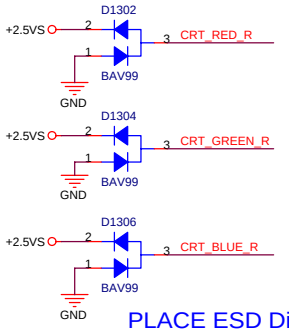


Place Terminator close to Connector

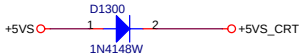
12-141011072

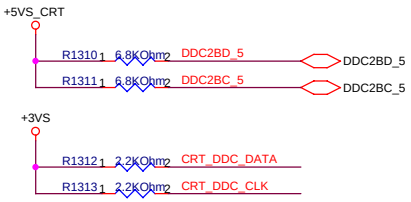


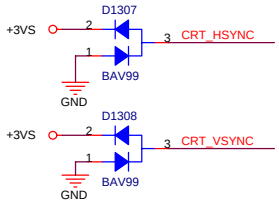
PLACE ESD Diodes near TV port



PLACE ESD Diodes near VGA port

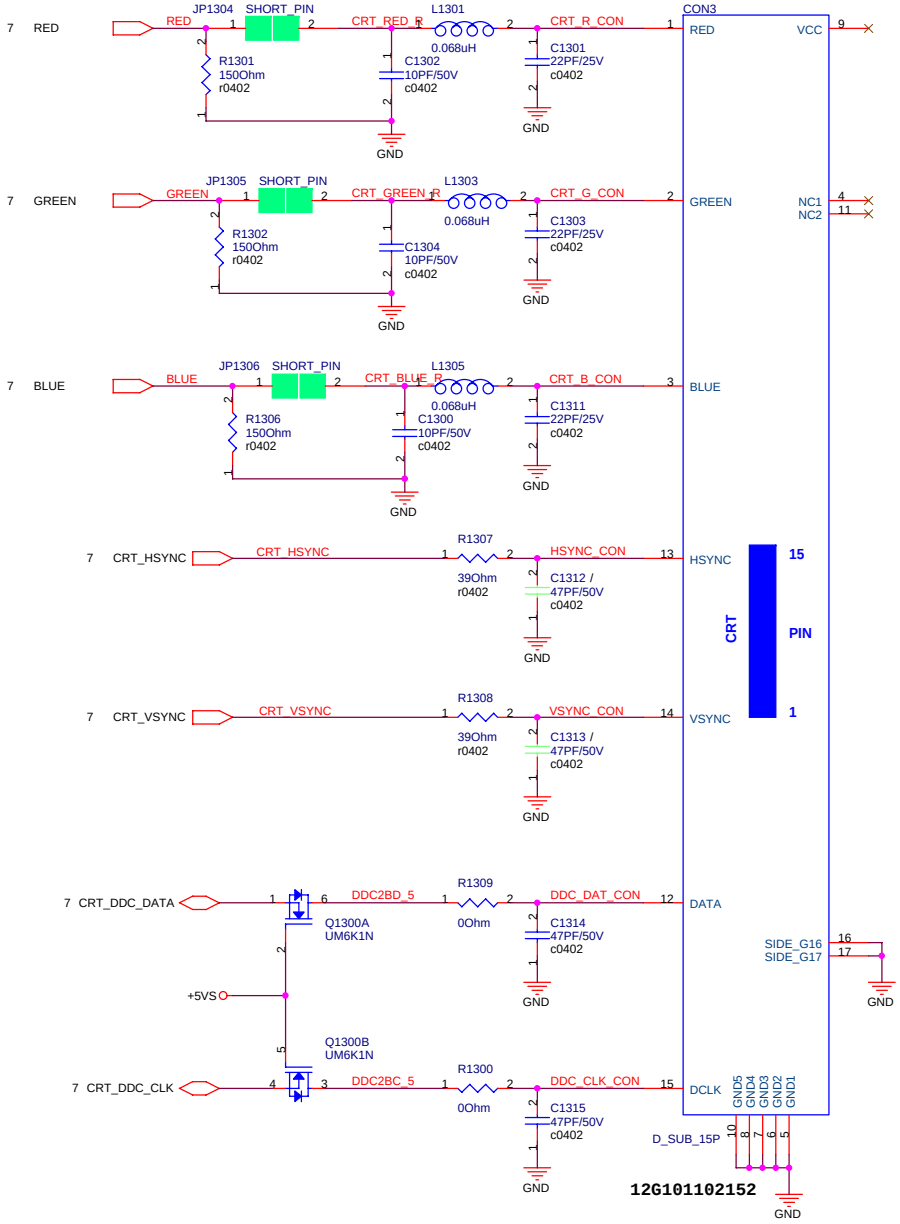






CRT OUT

checklist suggests 47ohm/100MHz



12G101102152

ASUSTeK COMPUTER INC	Title : CRT & TV OUT		
	Engineer: Jack Wang		
Size: A3	Project Name: A6F		Rev: 1.0
Date: Monday, March 06, 2006	Sheet 13 of 63		

8 M_B_DQ[0..63]

8,16 M_B_A[0..13]

M_VREF_DIMM1 → M_VREF_DIMM1 7,15,16

+1.8V → +1.8V 7,10,15,36,53

+3VS → +3VS 4,5,7,9,11,12,13,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61

CON8B

M_B_A0	B102	B:A0	B:DQ0	B5	M_B_DQ1	Group0
M_B_A1	B101	B:A1	B:DQ1	B7	M_B_DQ4	
M_B_A2	B100	B:A2	B:DQ2	B17	M_B_DQ7	
M_B_A3	B99	B:A3	B:DQ3	B19	M_B_DQ3	
M_B_A4	B98	B:A4	B:DQ4	B4	M_B_DQ5	
M_B_A5	B97	B:A5	B:DQ5	B6	M_B_DQ0	
M_B_A6	B94	B:A6	B:DQ6	B14	M_B_DQ2	
M_B_A7	B92	B:A7	B:DQ7	B16	M_B_DQ6	
M_B_A8	B93	B:A8	B:DQ8	B23	M_B_DQ8	Group1
M_B_A9	B91	B:A9	B:DQ9	B25	M_B_DQ9	
M_B_A10	B105	B:A10/AP	B:DQ10	B35	M_B_DQ14	
M_B_A11	B90	B:A11	B:DQ11	B37	M_B_DQ15	
M_B_A12	B89	B:A12	B:DQ12	B20	M_B_DQ13	
M_B_A13	B116	B:A13	B:DQ13	B22	M_B_DQ12	
	B86	B:A14	B:DQ14	B36	M_B_DQ11	
	B84	B:A15	B:DQ15	B38	M_B_DQ10	
M_B_BS#2	B85	B:A16_BA2	B:DQ16	B43	M_B_DQ21	Group2
M_B_BS#0	B107	B:BA0	B:DQ17	B45	M_B_DQ16	
M_B_BS#1	B106	B:BA1	B:DQ18	B55	M_B_DQ22	
M_CS#2	B110	B:S0#	B:DQ19	B57	M_B_DQ23	
M_CS#3	B115	B:S1#	B:DQ20	B44	M_B_DQ17	
M_CLK_DDR3	B30	B:CK0	B:DQ21	B46	M_B_DQ20	
M_CLK_DDR#3	B32	B:CK0#	B:DQ22	B56	M_B_DQ19	
M_CLK_DDR2	B164	B:CK1	B:DQ23	B58	M_B_DQ18	
M_CLK_DDR#2	B166	B:CK1#	B:DQ24	B61	M_B_DQ29	Group3
M_CKE2	B79	B:CKE0	B:DQ25	B63	M_B_DQ25	
M_CKE3	B80	B:CKE1	B:DQ26	B73	M_B_DQ31	
M_B_CAS#	B113	B:CBS#	B:DQ27	B75	M_B_DQ30	
M_B_RAS#	B108	B:RAS#	B:DQ28	B62	M_B_DQ26	
M_B_WE#	B109	B:WE#	B:DQ29	B64	M_B_DQ24	
	B198	B:SA0	B:DQ30	B74	M_B_DQ28	
	B200	B:SA1	B:DQ31	B76	M_B_DQ27	
SMB_CLK_S	B197	B:SCL	B:DQ32	B123	M_B_DQ32	Group4
SMB_DAT_S	B195	B:SDA	B:DQ33	B125	M_B_DQ33	
M_ODT2	B114	B:ODT0	B:DQ34	B135	M_B_DQ34	
M_ODT3	B119	B:ODT1	B:DQ35	B137	M_B_DQ35	
M_B_DM0	B10	B:DM0	B:DQ36	B124	M_B_DQ36	
M_B_DM1	B26	B:DM1	B:DQ37	B126	M_B_DQ37	
M_B_DM2	B52	B:DM2	B:DQ38	B134	M_B_DQ38	
M_B_DM3	B67	B:DM3	B:DQ39	B136	M_B_DQ39	
M_B_DM4	B130	B:DM4	B:DQ40	B141	M_B_DQ41	Group5
M_B_DM5	B147	B:DM5	B:DQ41	B143	M_B_DQ40	
M_B_DM6	B170	B:DM6	B:DQ42	B151	M_B_DQ46	
M_B_DM7	B185	B:DM7	B:DQ43	B153	M_B_DQ43	
M_B_DQS0	B13	B:DQS0	B:DQ44	B140	M_B_DQ44	
M_B_DQS1	B31	B:DQS1	B:DQ45	B142	M_B_DQ45	
M_B_DQS2	B51	B:DQS2	B:DQ46	B152	M_B_DQ42	
M_B_DQS3	B70	B:DQS3	B:DQ47	B154	M_B_DQ47	
M_B_DQS4	B131	B:DQS4	B:DQ48	B157	M_B_DQ53	Group6
M_B_DQS5	B148	B:DQS5	B:DQ49	B159	M_B_DQ49	
M_B_DQS6	B169	B:DQS6	B:DQ50	B173	M_B_DQ54	
M_B_DQS7	B188	B:DQS7	B:DQ51	B175	M_B_DQ51	
M_B_DQS#0	B11	B:DQS0#	B:DQ52	B158	M_B_DQ48	
M_B_DQS#1	B29	B:DQS1#	B:DQ53	B160	M_B_DQ52	
M_B_DQS#2	B49	B:DQS2#	B:DQ54	B174	M_B_DQ50	
M_B_DQS#3	B68	B:DQS3#	B:DQ55	B176	M_B_DQ55	
M_B_DQS#4	B129	B:DQS4#	B:DQ56	B179	M_B_DQ63	Group7
M_B_DQS#5	B146	B:DQS5#	B:DQ57	B181	M_B_DQ57	
M_B_DQS#6	B167	B:DQS6#	B:DQ58	B189	M_B_DQ62	
M_B_DQS#7	B186	B:DQS7#	B:DQ59	B191	M_B_DQ61	
			B:DQ60	B180	M_B_DQ56	
			B:DQ61	B182	M_B_DQ60	
			B:DQ62	B192	M_B_DQ58	
			B:DQ63	B194	M_B_DQ59	
	B111	B:VDD2				
	B117	B:VDD3				
	B95	B:VDD5				
	B81	B:VDD7				
	B87	B:VDD9				
	B103	B:VDD10				
	B47	B:VSS1	B:VSS26	B127		
	B133	B:VSS2	B:VSS27	B139		
	B183	B:VSS3	B:VSS29	B145		
	B77	B:VSS4	B:VSS30	B165		
	B71	B:VSS9	B:VSS31	B171		
	B121	B:VSS11	B:VSS33	B177		
	B193	B:VSS14	B:VSS34	B187		
	B41	B:VSS18	B:VSS37	B9		
	B53	B:VSS19	B:VSS38	B21		
	B59	B:VSS22	B:VSS39	B33		
	B65	B:VSS23	B:VSS40	B155		
			B:VSS47	B3		
	B199	B:VDDSPD	B:VSS48	B15		
	B1	B:VREF	B:VSS49	B27		
			B:VSS50	B39		
			B:VSS51	B149		
			B:VSS52	B161		
			B:NC1	B83		
			B:NC2	B120		
			B:NC3	B50		
			B:NC4	B69		
			B:NCTEST	B163		

DDR_DIMM_331P

11/14

+3VS — R1401 10KOhm — r0402 — GND

+3VS — R1402 10KOhm — r0402 — GND

For Data Swap

+1.8V — C1401 C1402 C1403 C1400 0.1UF/10V — GND

Layout Note:
Place these resistors
near the GMCH

8 M_B_DM[0..7]

8 M_B_DQS[0..7]

8 M_B_DQS#[0..7]

+1.8V — C1408 C1411 C1409 C1410 0.1UF/10V — GND

+1.8V — C1412 C1413 C1414 C1415 C1416 2.2UF/6.3V — GND

Layout Note:
Place these
Caps near
SO DIMM 1

+3VS — C1404 2.2UF/6.3V, C1405 0.1UF/10V — GND

M_VREF_DIMM1 — VREF -> 10/10 mils — C1406 2.2UF/6.3V, C1407 0.1UF/10V — GND

ASUSTeK COMPUTER INC	Title : DDR2_SO-DIMM(1)		
	Engineer: Jack Wang		
Size: A3	Project Name: A6F		Rev: 1.0
Date: Monday, March 06, 2006	Sheet 14 of 63		

8 M_A_DQ[0..63]
8,16 M_A_A[0..13]

Green Part Number:12G025122006

+1.8V +1.8V 7,10,14,36,53
+3VS +3VS 4,5,7,9,11,12,13,14,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61
M_VREF_DIMM0 M_VREF_DIMM0 7,14,16

CON8A

M_A_A0	A102	A:A0	A:DQ0	A5	M_A_DQ6	
M_A_A1	A101	A:A1	A:DQ1	A7	M_A_DQ7	
M_A_A2	A100	A:A2	A:DQ2	A17	M_A_DQ2	
M_A_A3	A99	A:A3	A:DQ3	A19	M_A_DQ3	Group0
M_A_A4	A98	A:A4	A:DQ4	A4	M_A_DQ4	
M_A_A5	A97	A:A5	A:DQ5	A6	M_A_DQ5	
M_A_A6	A94	A:A6	A:DQ6	A14	M_A_DQ0	
M_A_A7	A92	A:A7	A:DQ7	A16	M_A_DQ1	
M_A_A8	A93	A:A8	A:DQ8	A23	M_A_DQ14	
M_A_A9	A91	A:A9	A:DQ9	A25	M_A_DQ8	
M_A_A10	A105	A:A10/AP	A:DQ10	A35	M_A_DQ10	
M_A_A11	A90	A:A11	A:DQ11	A37	M_A_DQ11	Group1
M_A_A12	A89	A:A12	A:DQ12	A20	M_A_DQ13	
M_A_A13	A116	A:A13	A:DQ13	A22	M_A_DQ12	
	A86	A:A14	A:DQ14	A36	M_A_DQ15	
	A84	A:A15	A:DQ15	A38	M_A_DQ9	
M_A_BS#2	A85	A:A16_BA2	A:DQ16	A43	M_A_DQ16	
M_A_BS#0	A107	A:BA0	A:DQ17	A45	M_A_DQ20	
M_A_BS#1	A106	A:BA1	A:DQ18	A55	M_A_DQ18	
M_CS#0	A110	A:S0#	A:DQ19	A57	M_A_DQ23	Group2
M_CS#1	A115	A:S1#	A:DQ20	A44	M_A_DQ21	
M_CLK_DDR0	A30	A:CK0	A:DQ21	A46	M_A_DQ17	
M_CLK_DDR#0	A32	A:CK0#	A:DQ22	A56	M_A_DQ19	
M_CLK_DDR1	A164	A:CK1	A:DQ23	A58	M_A_DQ22	
M_CLK_DDR#1	A166	A:CK1#	A:DQ24	A61	M_A_DQ28	
M_CKE0	A79	A:CKE0	A:DQ25	A63	M_A_DQ25	
M_CKE1	A80	A:CKE1	A:DQ26	A73	M_A_DQ31	Group3
M_A_CAS#	A113	A:CAS#	A:DQ27	A75	M_A_DQ26	
M_A_RAS#	A108	A:RAS#	A:DQ28	A62	M_A_DQ24	
M_A_WE#	A109	A:WE#	A:DQ29	A64	M_A_DQ29	
	A198	A:SA0	A:DQ30	A74	M_A_DQ30	
	A200	A:SA1	A:DQ31	A76	M_A_DQ27	
SMB_CLK_S	A197	A:SCL	A:DQ32	A123	M_A_DQ34	
SMB_DAT_S	A195	A:SDA	A:DQ33	A125	M_A_DQ33	
			A:DQ34	A135	M_A_DQ39	
M_ODT0	A114	A:ODT0	A:DQ35	A137	M_A_DQ38	
M_ODT1	A119	A:ODT1	A:DQ36	A124	M_A_DQ36	Group4
			A:DQ37	A126	M_A_DQ32	
M_A_DM0	A10	A:DM0	A:DQ38	A134	M_A_DQ37	
M_A_DM1	A26	A:DM1	A:DQ39	A136	M_A_DQ35	
M_A_DM2	A52	A:DM2	A:DQ40	A141	M_A_DQ45	
M_A_DM3	A67	A:DM3	A:DQ41	A143	M_A_DQ41	
M_A_DM4	A130	A:DM4	A:DQ42	A151	M_A_DQ47	
M_A_DM5	A147	A:DM5	A:DQ43	A153	M_A_DQ46	
M_A_DM6	A170	A:DM6	A:DQ44	A140	M_A_DQ44	Group5
M_A_DM7	A185	A:DM7	A:DQ45	A142	M_A_DQ40	
			A:DQ46	A152	M_A_DQ43	
M_A_DQS0	A13	A:DQS0	A:DQ47	A154	M_A_DQ42	
M_A_DQS1	A31	A:DQS1	A:DQ48	A157	M_A_DQ52	
M_A_DQS2	A51	A:DQS2	A:DQ49	A159	M_A_DQ53	
M_A_DQS3	A70	A:DQS3	A:DQ50	A173	M_A_DQ54	
M_A_DQS4	A131	A:DQS4	A:DQ51	A175	M_A_DQ55	Group6
M_A_DQS5	A148	A:DQS5	A:DQ52	A158	M_A_DQ49	
M_A_DQS6	A169	A:DQS6	A:DQ53	A160	M_A_DQ48	
M_A_DQS7	A188	A:DQS7	A:DQ54	A174	M_A_DQ51	
M_A_DQS#0	A11	A:DQS0#	A:DQ55	A176	M_A_DQ50	
M_A_DQS#1	A29	A:DQS1#	A:DQ56	A179	M_A_DQ61	
M_A_DQS#2	A49	A:DQS2#	A:DQ57	A181	M_A_DQ63	
M_A_DQS#3	A68	A:DQS3#	A:DQ58	A189	M_A_DQ56	Group7
M_A_DQS#4	A129	A:DQS4#	A:DQ59	A191	M_A_DQ62	
M_A_DQS#5	A146	A:DQS5#	A:DQ60	A180	M_A_DQ57	
M_A_DQS#6	A167	A:DQS6#	A:DQ61	A182	M_A_DQ60	
M_A_DQS#7	A186	A:DQS7#	A:DQ62	A192	M_A_DQ59	
			A:DQ63	A194	M_A_DQ58	

For Data Swap

R15002 10KOhm, R15001 10KOhm

8 M_A_DM[0..7]
8 M_A_DQS[0..7]
8 M_A_DQS#[0..7]

GMCH=====>SODIMM1=>SODIMM0

+1.8V

	A112	A:VDD1	A:VSS21	A54		
	A96	A:VDD4	A:VSS24	A60		
	A118	A:VDD6	A:VSS25	A66		
	A82	A:VDD8	A:VSS28	A128		
	A88	A:VDD11	A:VSS32	A172		
	A104	A:VDD12	A:VSS35	A178		
			A:VSS36	A190		
	A12	A:VSS5	A:VSS41	A34		
	A48	A:VSS6	A:VSS42	A132		
	A184	A:VSS7	A:VSS43	A144		
	A78	A:VSS8	A:VSS44	A156		
	A72	A:VSS10	A:VSS45	A168		
	A122	A:VSS12	A:VSS46	A2		
	A196	A:VSS13	A:VSS53	A28		
	A8	A:VSS15	A:VSS54	A40		
	A18	A:VSS16	A:VSS55	A138		
	A24	A:VSS17	A:VSS56	A150		
	A42	A:VSS20	A:VSS57	A162		
	A199	A:VDDSPD				
	A1	A:VREF	A:NC1	A83		
			A:NC2	A120		
			A:NC3	A50		
			A:NC4	A69		
			A:NCTEST	A163		
			NP_NC1	201	GND1	205
			NP_NC2	203	GND2	206
			NP_NC3	204	GND3	208
			NP_NC4	204	GND4	207

DDR_DIMM_200

Layout Note: Place these Caps near SO DIMM 0

C1500 0.1UF/10V, C1505 0.1UF/10V, C1506 0.1UF/10V, C1507 0.1UF/10V

Layout Note: Place these Caps near SO DIMM 0

C1508 2.2UF/6.3V, C1509 2.2UF/6.3V, C1510 2.2UF/6.3V, C1511 2.2UF/6.3V, C1512 2.2UF/6.3V

+3VS

C1501 2.2UF/6.3V, C1502 0.1UF/10V

M_VREF_DIMM0

VREF -> 10/10 mils

C1503 2.2UF/6.3V, C1504 0.1UF/10V

GND

ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM(0)

Engineer: Jack Wang

Size	Project Name	Rev
A3	A6F	1.0

Date: Monday, March 06, 2006 Sheet 15 of 63

+0.9VS

NEED TO SWAP

1	56Ohm	16	RN1601A	M_A_A2
2	56Ohm	15	RN1601B	M_A_A0
3	56Ohm	14	RN1601C	M_A_BS#1
4	56Ohm	13	RN1601D	M_A_RAS#
5	56Ohm	12	RN1601E	M_ODT0
6	56Ohm	11	RN1601F	M_CS#0
7	56Ohm	10	RN1601G	M_CS#2
8	56Ohm	9	RN1601H	M_ODT2
1	56Ohm	16	RN1602A	M_B_A11
2	56Ohm	15	RN1602B	M_B_A6
3	56Ohm	14	RN1602C	M_B_A7
4	56Ohm	13	RN1602D	M_B_A4
5	56Ohm	12	RN1602E	M_B_A2
6	56Ohm	11	RN1602F	M_B_A0
7	56Ohm	10	RN1602G	M_B_BS#1
8	56Ohm	9	RN1602H	M_B_RAS#
1	56Ohm	16	RN1603A	M_B_BS#0
2	56Ohm	15	RN1603B	M_B_A10
3	56Ohm	14	RN1603C	M_B_WE#
4	56Ohm	13	RN1603D	M_B_CAS#
5	56Ohm	12	RN1603E	M_CS#3
6	56Ohm	11	RN1603F	M_ODT3
7	56Ohm	10	RN1603G	M_ODT1
8	56Ohm	9	RN1603H	M_CS#1
1	56Ohm	16	RN1605A	M_B_A12
2	56Ohm	15	RN1605B	M_B_BS#2
3	56Ohm	14	RN1605C	M_A_A12
4	56Ohm	13	RN1605D	M_A_BS#0
5	56Ohm	12	RN1605E	M_A_BS#2
6	56Ohm	11	RN1605F	M_CKE2
7	56Ohm	10	RN1605G	M_CKE0
8	56Ohm	9	RN1605H	M_CKE3
1	56Ohm	16	RN1606A	M_B_A13
2	56Ohm	15	RN1606B	M_CKE1
3	56Ohm	14	RN1606C	M_A_A13
4	56Ohm	13	RN1606D	M_A_A4
5	56Ohm	12	RN1606E	M_A_A6
6	56Ohm	11	RN1606F	M_A_A7
7	56Ohm	10	RN1606G	M_A_A11
8	56Ohm	9	RN1606H	M_A_A9
1	56Ohm	16	RN1607A	M_A_A5
2	56Ohm	15	RN1607B	M_B_A1
3	56Ohm	14	RN1607C	M_B_A3
4	56Ohm	13	RN1607D	M_B_A5
5	56Ohm	12	RN1607E	M_B_A8
6	56Ohm	11	RN1607F	M_A_A3
7	56Ohm	10	RN1607G	M_A_A8
8	56Ohm	9	RN1607H	M_B_A9
1	56Ohm	2	RN1608A	M_A_CAS#
3	56Ohm	4	RN1608B	M_A_WE#
5	56Ohm	6	RN1608C	M_A_A10
7	56Ohm	8	RN1608D	M_A_A1

M_A_A[0..13] 8,15
M_A_BS#[0..2] 8,15
M_A_CAS# 8,15
M_A_RAS# 8,15
M_A_WE# 8,15

M_B_A[0..13] 8,14
M_B_BS#[0..2] 8,14
M_B_CAS# 8,14
M_B_RAS# 8,14
M_B_WE# 8,14

M_CS#[0..3] 7,14,15
M_ODT[0..3] 7,14,15
M_CKE[0..3] 7,14,15

M_VREF_DIMM0 → M_VREF_DIMM0 7,14,15
M_VREF_DIMM1 → M_VREF_DIMM1 7,14,15
M_VREF_MCH → M_VREF_MCH 7,14,15
+0.9VS → +0.9VS 36,53

+0.9VS
L1600 120Ohm/100Mhz
→ M_VREF_DIMM1
→ M_VREF_MCH
→ M_VREF_DIMM0

+0.9VS

C1601	C1602	C1603	C1604	C1605	C1606	C1607	C1608	C1609	C1610	C1600	C1611	C1612			
c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402			
0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V			

GND

Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

+0.9VS

C1613	C1614	C1615	C1616	C1617	C1618	C1619	C1620	C1621	C1622	C1623	C1624	C1625			
c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402			
0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V			

GND

ASUSTeK COMPUTER INC

Title : DDR2 TERM

Engineer: *Jack Wang*

Size	Project Name	Rev
A4	**A6F**	1.0

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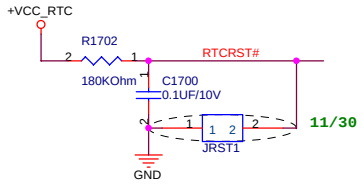
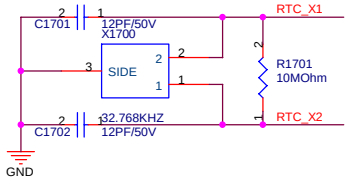
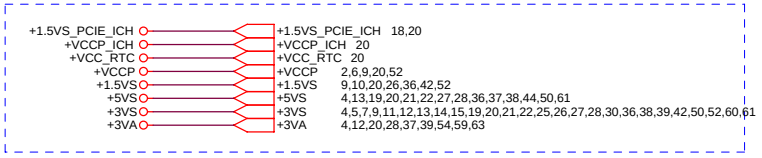
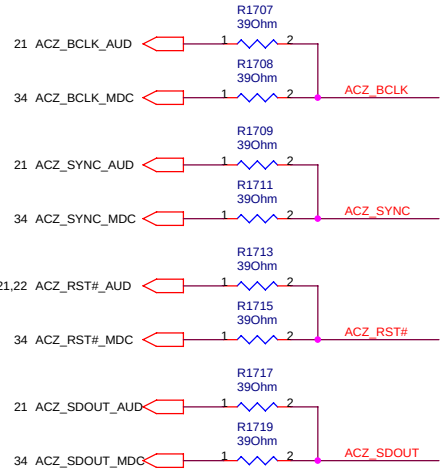
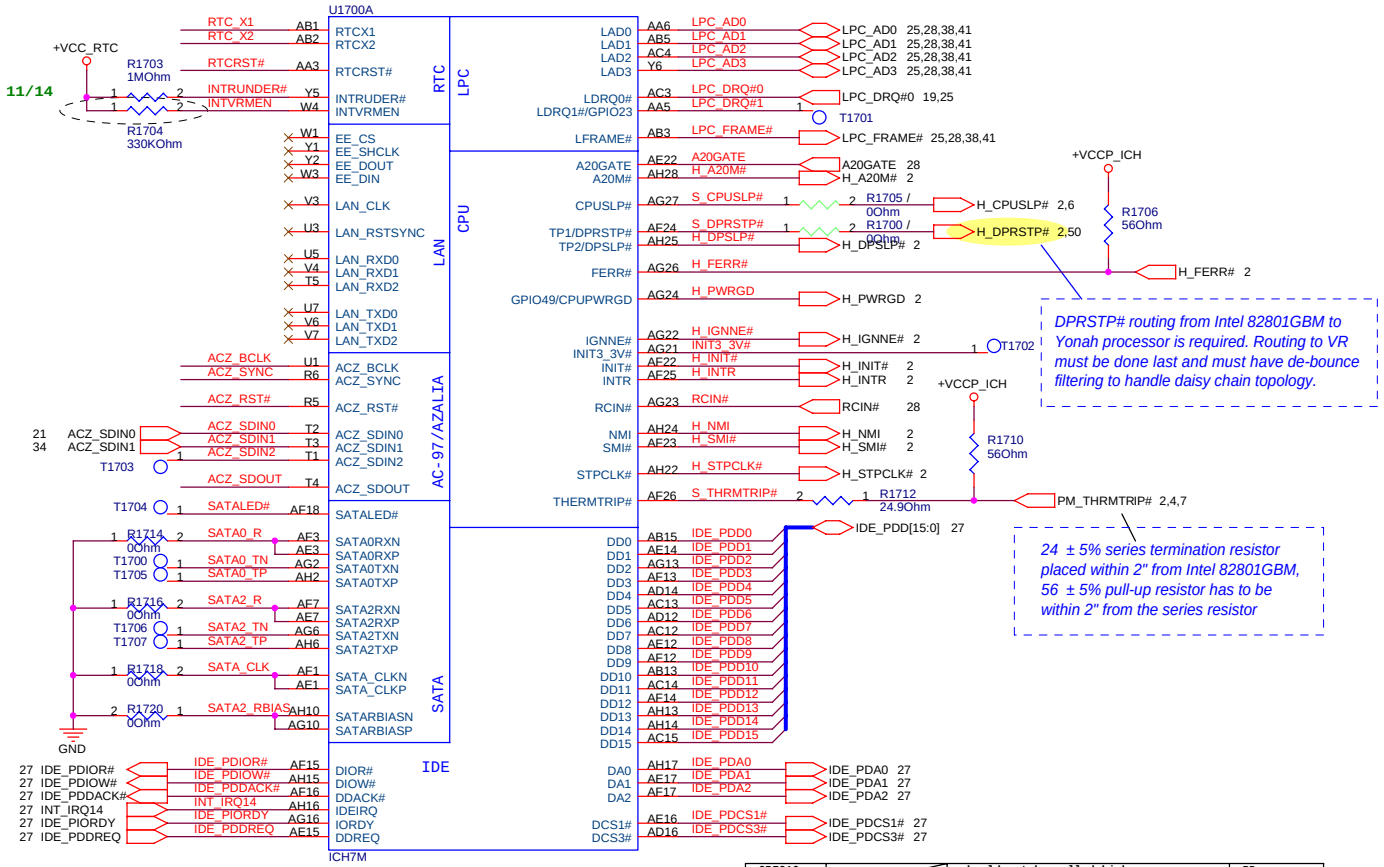










DPRSTP# routing from Intel 82801GBM to Yonah processor is required. Routing to VR must be done last and must have de-bounce filtering to handle daisy chain topology.

24 ± 5% series termination resistor placed within 2" from Intel 82801GBM, 56 ± 5% pull-up resistor has to be within 2" from the series resistor

ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSMRST# rising	should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALERT#		REQUIRE an extenal pull-up R	Need PU
REQ[4:1]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

ASUSTeK COMPUTER INC

Title : ICH7-M (1/4)

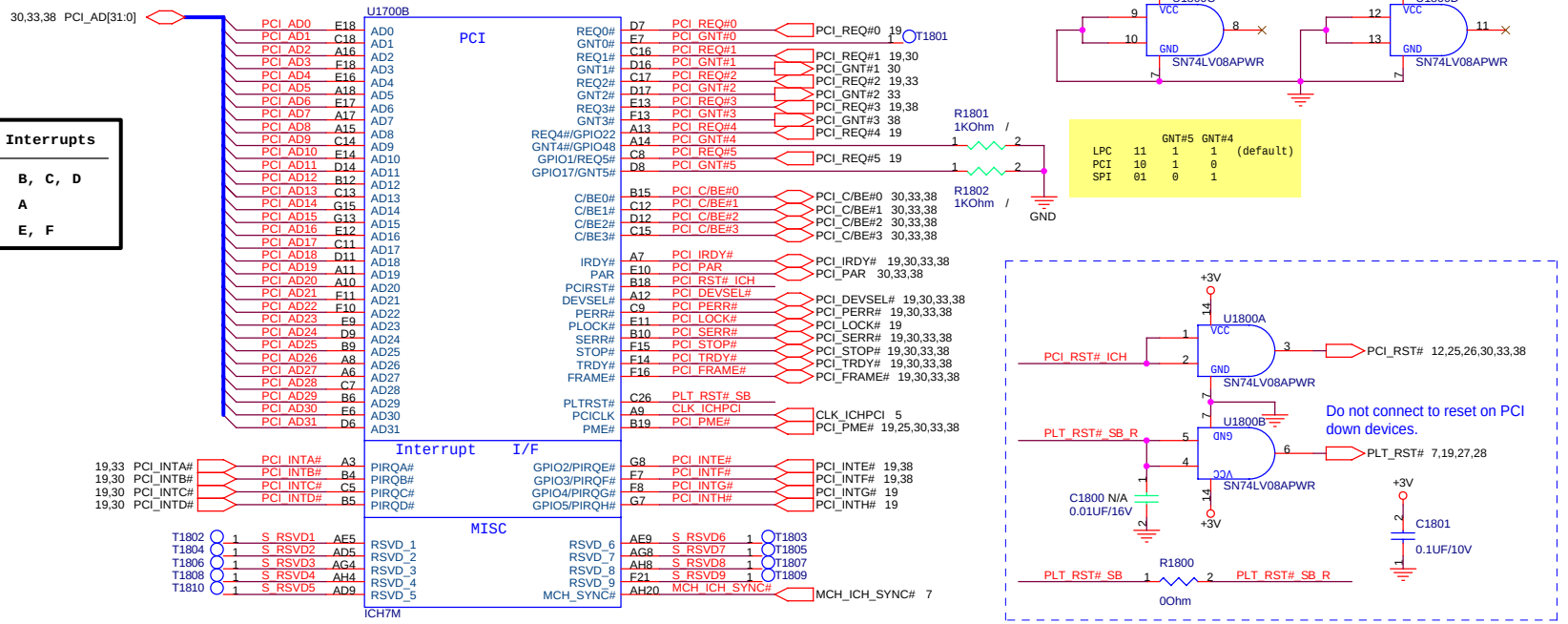
Engineer: Jack Wang

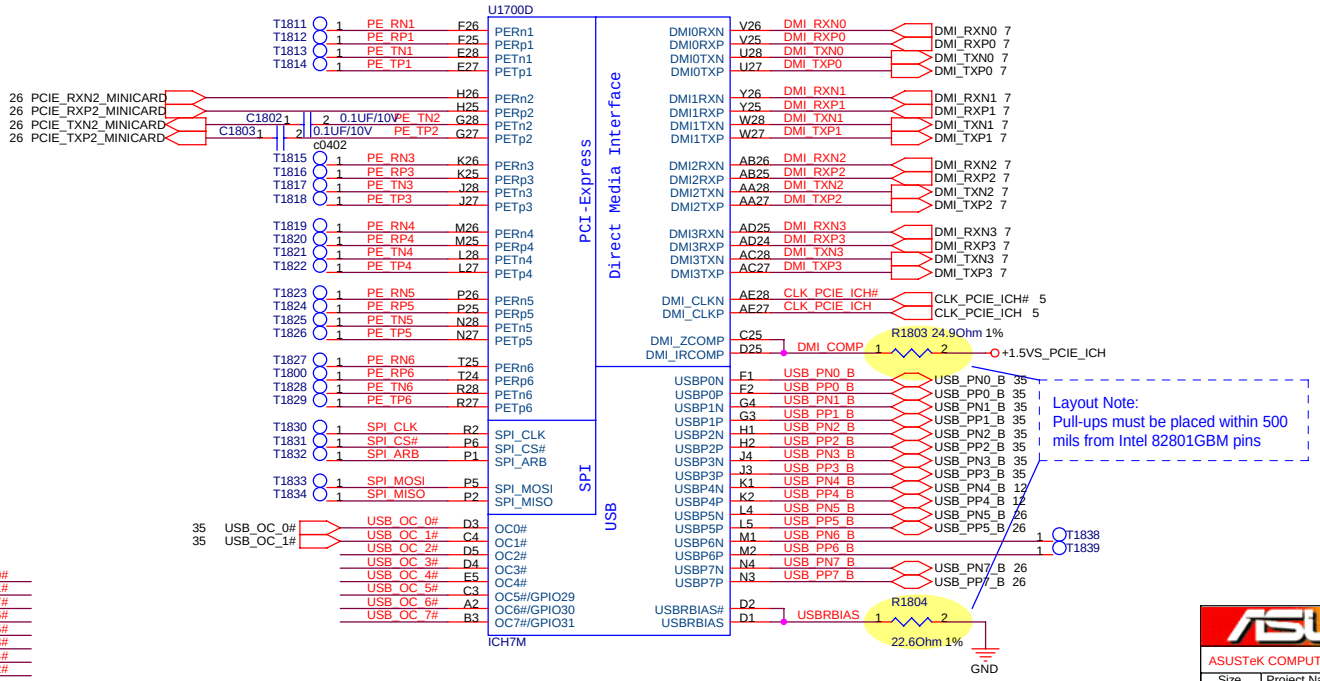
Size	Project Name	Rev
Custom	A6F	1.0

Date: Monday, March 06, 2006 Sheet 17 of 63

PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A
Mini-PCI	AD19	REQ3#/GNT3#	E, F

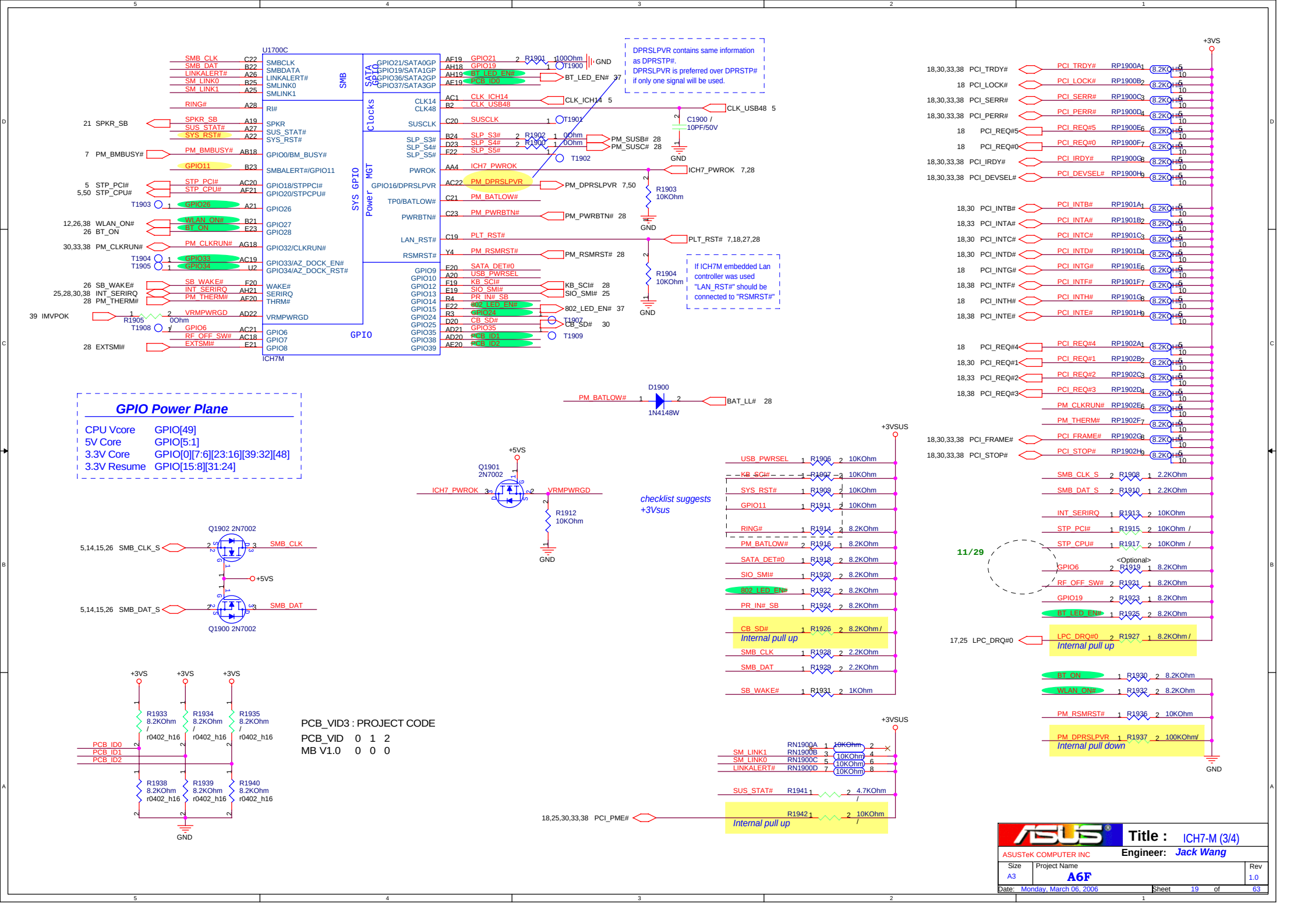


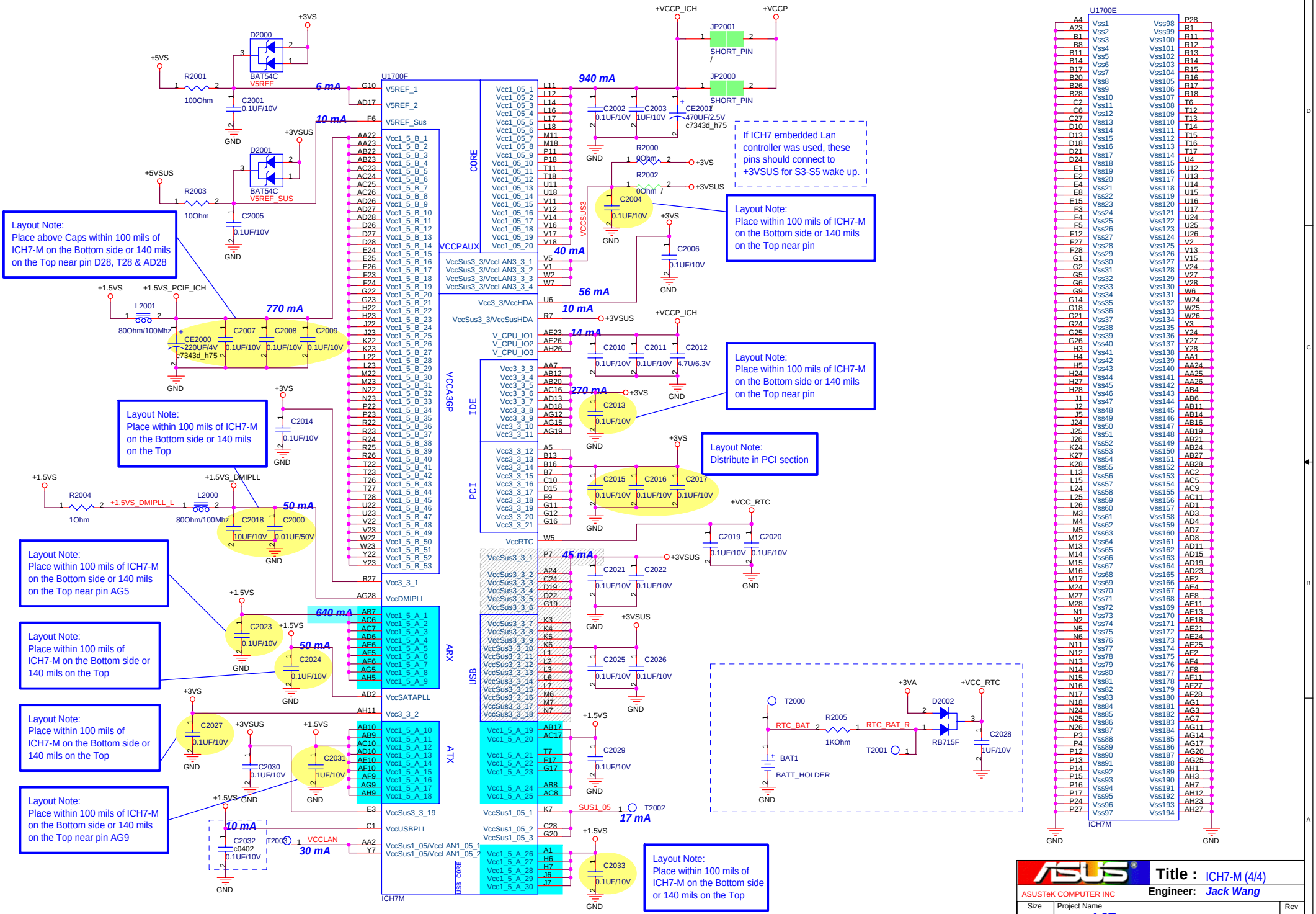


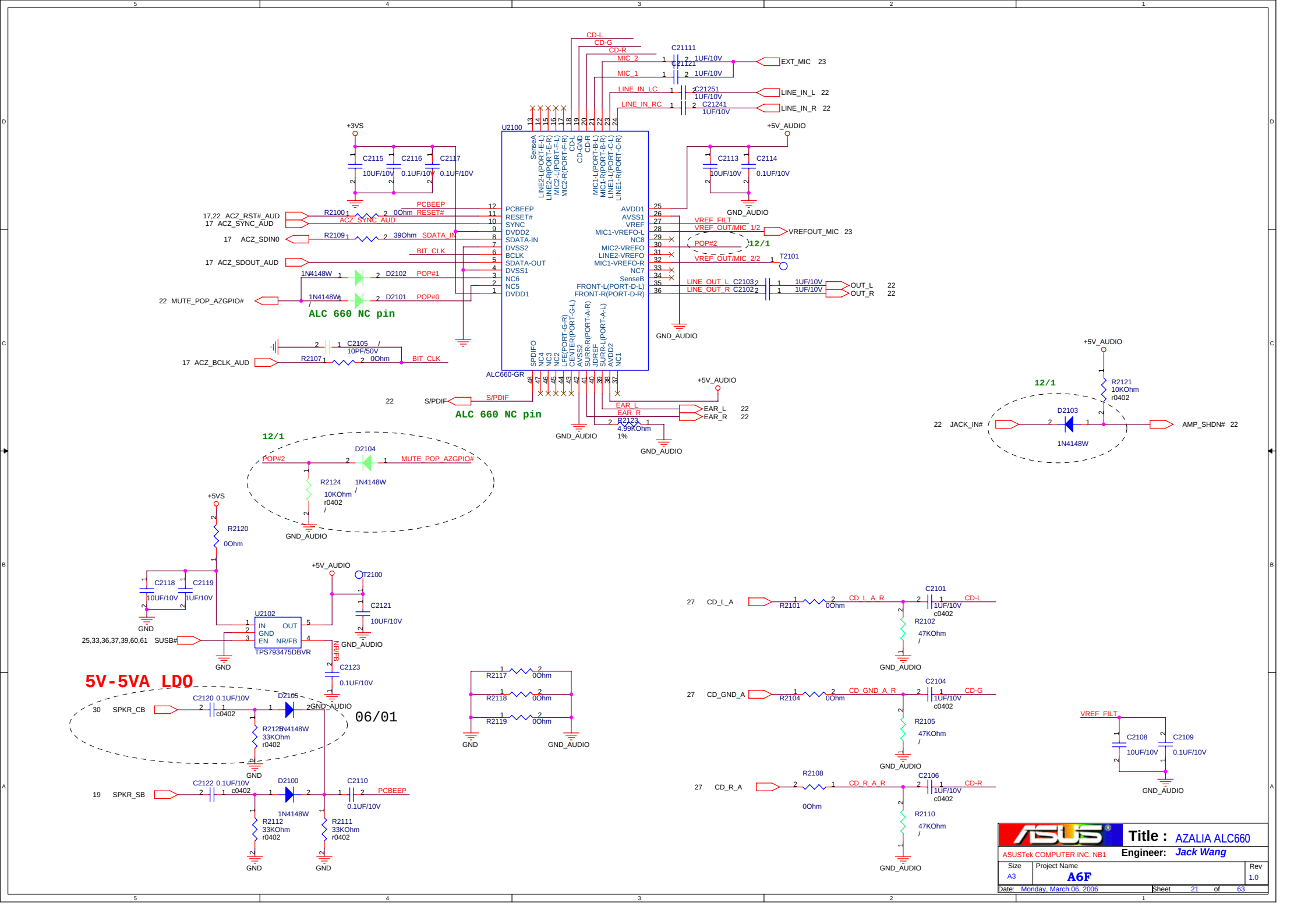
USB Devices

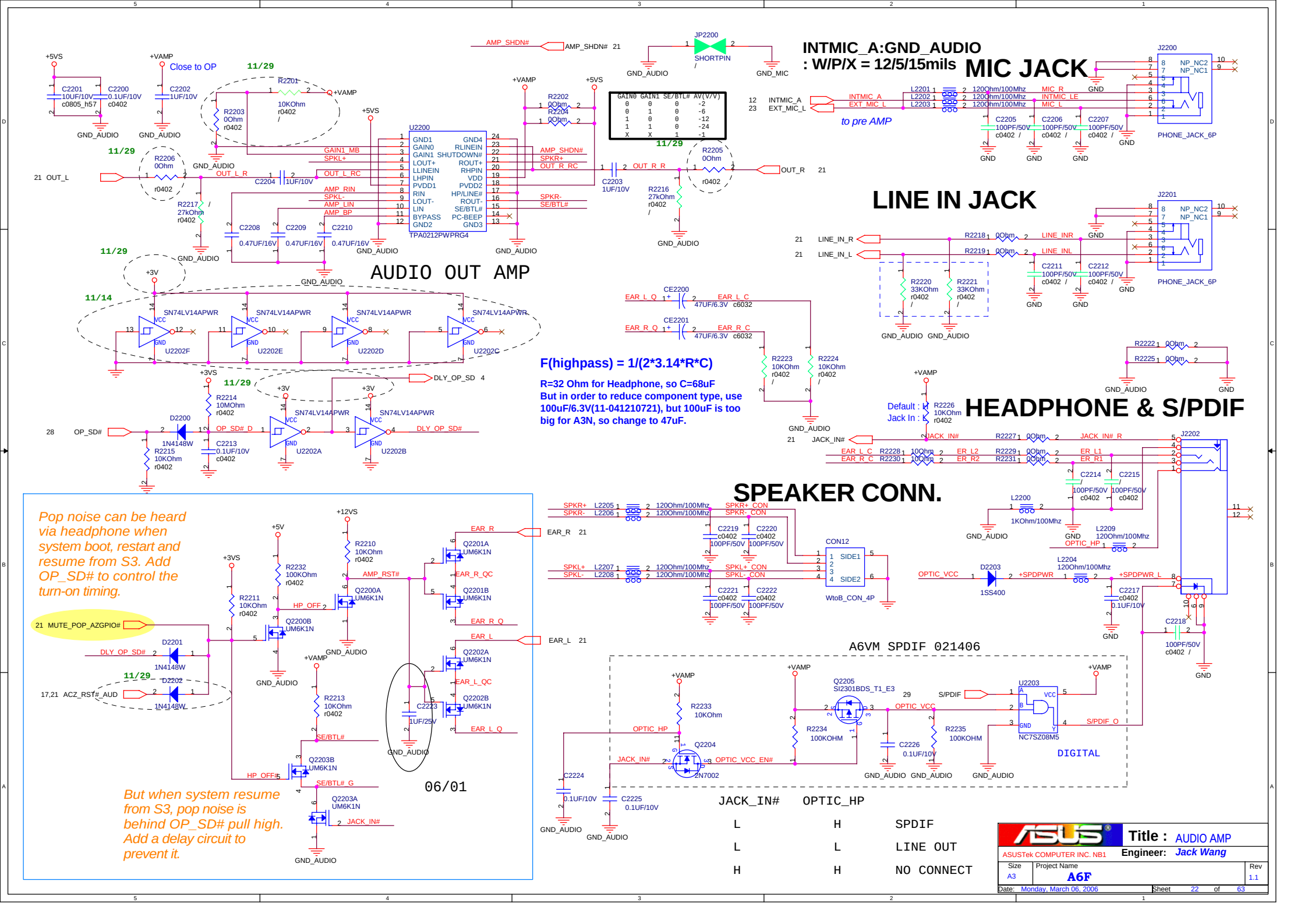
Port 0 Conn. 0
Port 1 Conn. 1
Port 2 Conn. 2
Port 3 Conn. 3
Port 4 CMOS Camera
Port 5 Bluetooth
Port 6 NC
Port 7 Mini Card

ASUSTeK COMPUTER INC	Title : ICH7-M (2/4)	
	Engineer: Jack Wang	
Size: Custom	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 18 of 63	


U1700C
SMB_CLK C22
SMB_DAT B22
LINKALERT# A26
SM_LINK0 B25
SM_LINK1 A25
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
SMB
RING# A28
RI#
21 SPKR_SB
SPKR_SB A19
SUS_STAT# A27
SYS_RST# A22
SPKR
SUS_STAT#
SYS_RST#
7 PM_BMBUSY#
PM_BMBUSY# AB18
GPIO0/BM_BUSY#
GPIO11 B23
SMBALERT#/GPIO11
5 STP_PCI#
5,50 STP_CPU#
STP_PCI# AC20
STP_CPU# AE21
GPIO18/STPPCI#
GPIO20/STPCPU#
T1903
GPIO26 A21
GPIO26
12,26,38 WLAN_ON#
26 BT_ON
WLAN_ON# B21
BT_ON E23
GPIO27
GPIO28
30,33,38 PM_CLKRUN#
PM_CLKRUN# AG18
GPIO32/CLKRUN#
T1904
T1905
GPIO33 AC19
GPIO34 U2
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
26 SB_WAKE#
25,28,30,38 INT_SERIRQ
28 PM_THERM#
SB_WAKE# F20
INT_SERIRQ AH21
PM_THERM# AE20
WAKE#
SERIRQ
THRM#
39 IMVPOK
R1905 1 2 0Ohm
T1908
VRMPWRGD AD22
GPIO6 AC21
RF_OFF_SW# AC18
VRMPWRGD
28 EXTSMI#
EXTSMI# E21
GPIO6
GPIO7
GPIO8
GPIO
ICH7M
SYS GPIO
Power MGT
SATA GPIO
Clocks
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
AF19 GPIO21
AH18 GPIO19
AH19 BT_LED_EN#
AF19 PCB_ID0
2 R1901 1 100Ohm 1 T1900 GND
BT_LED_EN# 37
AC1 CLK_ICH14
B2 CLK_USB48
CLK_ICH14 5
CLK_USB48 5
C20 SUSCLK 1 T1901
C1900 / 10PF/50V
B24 SLP_S3# 2 R1902 1 0Ohm PM_SUSB# 28
D23 SLP_S4# 2 R1903 1 0Ohm PM_SUSC# 28
F22 SLP_S5# 1 T1902
GND
AA4 ICH7_PWROK
ICH7_PWROK 7,28
AC22 PM_DPRSLPVR
PM_DPRSLPVR 7,50
R1903 10KOhm
C21 PM_BATLOW#
C23 PM_PWRBTN#
PM_PWRBTN# 28
GND
C19 PLT_RST#
PLT_RST# 7,18,27,28
Y4 PM_RSMRST#
PM_RSMRST# 28
R1904 10KOhm
GND
F20 SATA_DET#0
A20 USB_PWRSEL
F19 KB_SCI#
E19 SIO_SMI#
R4 PR_IN# SB
F22 802_LED_EN#
R3 GPIO24
D20 CB_SD#
AD21 GPIO35
AD20 PCB_ID1
AE20 PCB_ID2
KB_SCI# 28
SIO_SMI# 25
802_LED_EN# 37
T1907
CB_SD# 30
T1909
DPRSLPVR contains same information as DPRSTP#.
DPRSLPVR is preferred over DPRSTP# if only one signal will be used.
If ICH7M embedded Lan controller was used "LAN_RST#" should be connected to "RSMRST#"
GPIO Power Plane
CPU Vcore GPIO[49]
5V Core GPIO[5:1]
3.3V Core GPIO[0][7:6][23:16][39:32][48]
3.3V Resume GPIO[15:8][31:24]
PM_BATLOW# 1 2 BAT_LL# 28
D1900
1N4148W
+5VS
Q1901 2N7002
ICH7_PWROK 3 2 VRMPWRGD
R1912 10KOhm
GND
checklist suggests +3Vsus
+3VSUS
USB_PWRSEL R1906 2 10KOhm
KB_SCI# R1907 2 10KOhm
SYS_RST# R1909 2 10KOhm
GPIO11 R1911 2 10KOhm
RING# R1914 2 8.2KOhm
PM_BATLOW# R1916 1 8.2KOhm
SATA_DET#0 R1918 2 8.2KOhm
SIO_SMI# R1920 2 8.2KOhm
802_LED_EN# R1922 2 8.2KOhm
PR_IN#_SB R1924 2 8.2KOhm
CB_SD# R1926 2 8.2KOhm /
Internal pull up
SMB_CLK R1928 2 2.2KOhm
SMB_DAT R1929 2 2.2KOhm
SB_WAKE# R1931 2 1KOhm
Q1902 2N7002
5,14,15,26 SMB_CLK_S
SMB_CLK
+5VS
5,14,15,26 SMB_DAT_S
SMB_DAT
Q1900 2N7002
+3VS
R1933 8.2KOhm / r0402_h16
R1934 8.2KOhm / r0402_h16
R1935 8.2KOhm / r0402_h16
PCB_ID0
PCB_ID1
PCB_ID2
R1938 8.2KOhm r0402_h16
R1939 8.2KOhm r0402_h16
R1940 8.2KOhm r0402_h16
GND
PCB_VID3 : PROJECT CODE
PCB_VID 0 1 2
MB V1.0 0 0 0
+3VSUS
RN1900A 1 10KOhm 2
SM_LINK1 RN1900B 3 10KOhm 4
SM_LINK0 RN1900C 5 10KOhm 6
LINKALERT# RN1900D 7 10KOhm 8
SUS_STAT# R1941 1 2 4.7KOhm /
R1942 1 2 10KOhm /
Internal pull up
18,25,30,33,38 PCI_PME#
+3VS
18,30,33,38 PCI_TRDY# PCI_TRDY# RP1900A1 8.2KOhm
18 PCI_LOCK# PCI_LOCK# RP1900B2 8.2KOhm
18,30,33,38 PCI_SERR# PCI_SERR# RP1900C3 8.2KOhm
18,30,33,38 PCI_PERR# PCI_PERR# RP1900D4 8.2KOhm
18 PCI_REQ#5 PCI_REQ#5 RP1900E6 8.2KOhm
18 PCI_REQ#0 PCI_REQ#0 RP1900F7 8.2KOhm
18,30,33,38 PCI_IRDY# PCI_IRDY# RP1900G8 8.2KOhm
18,30,33,38 PCI_DEVSEL# PCI_DEVSEL# RP1900H9 8.2KOhm
18,30 PCI_INTB# PCI_INTB# RP1901A1 8.2KOhm
18,33 PCI_INTA# PCI_INTA# RP1901B2 8.2KOhm
18,30 PCI_INTC# PCI_INTC# RP1901C3 8.2KOhm
18,30 PCI_INTD# PCI_INTD# RP1901D4 8.2KOhm
18 PCI_INTG# PCI_INTG# RP1901E6 8.2KOhm
18,38 PCI_INTF# PCI_INTF# RP1901F7 8.2KOhm
18 PCI_INTH# PCI_INTH# RP1901G8 8.2KOhm
18,38 PCI_INTE# PCI_INTE# RP1901H9 8.2KOhm
18 PCI_REQ#4 PCI_REQ#4 RP1902A1 8.2KOhm
18,30 PCI_REQ#1 PCI_REQ#1 RP1902B2 8.2KOhm
18,33 PCI_REQ#2 PCI_REQ#2 RP1902C3 8.2KOhm
18,38 PCI_REQ#3 PCI_REQ#3 RP1902D4 8.2KOhm
PM_CLKRUN# RP1902E6 8.2KOhm
PM_THERM# RP1902F7 8.2KOhm
18,30,33,38 PCI_FRAME# PCI_FRAME# RP1902G8 8.2KOhm
18,30,33,38 PCI_STOP# PCI_STOP# RP1902H9 8.2KOhm
SMB_CLK_S 2 R1908 1 2.2KOhm
SMB_DAT_S 2 R1910 1 2.2KOhm
INT_SERIRQ 1 R1913 2 10KOhm
STP_PCI# 1 R1915 2 10KOhm /
STP_CPU# 1 R1917 2 10KOhm /
11/29
<Optional>
GPIO6 2 R1919 1 8.2KOhm
RF_OFF_SW# 2 R1921 1 8.2KOhm
GPIO19 2 R1923 1 8.2KOhm
BT_LED_EN# 1 R1925 2 8.2KOhm
17,25 LPC_DRQ#0 LPC_DRQ#0 2 R1927 1 8.2KOhm /
Internal pull up
BT_ON 1 R1930 2 8.2KOhm
WLAN_ON# 1 R1932 2 8.2KOhm
PM_RSMRST# 1 R1936 2 10KOhm
PM_DPRSLPVR 1 R1937 2 100KOhm/
Internal pull down
GND
ASUSTeK COMPUTER INC
Title : ICH7-M (3/4)
Engineer: Jack Wang
Size A3
Project Name A6F
Rev 1.0
Date: Monday, March 06, 2006
Sheet 19 of 63

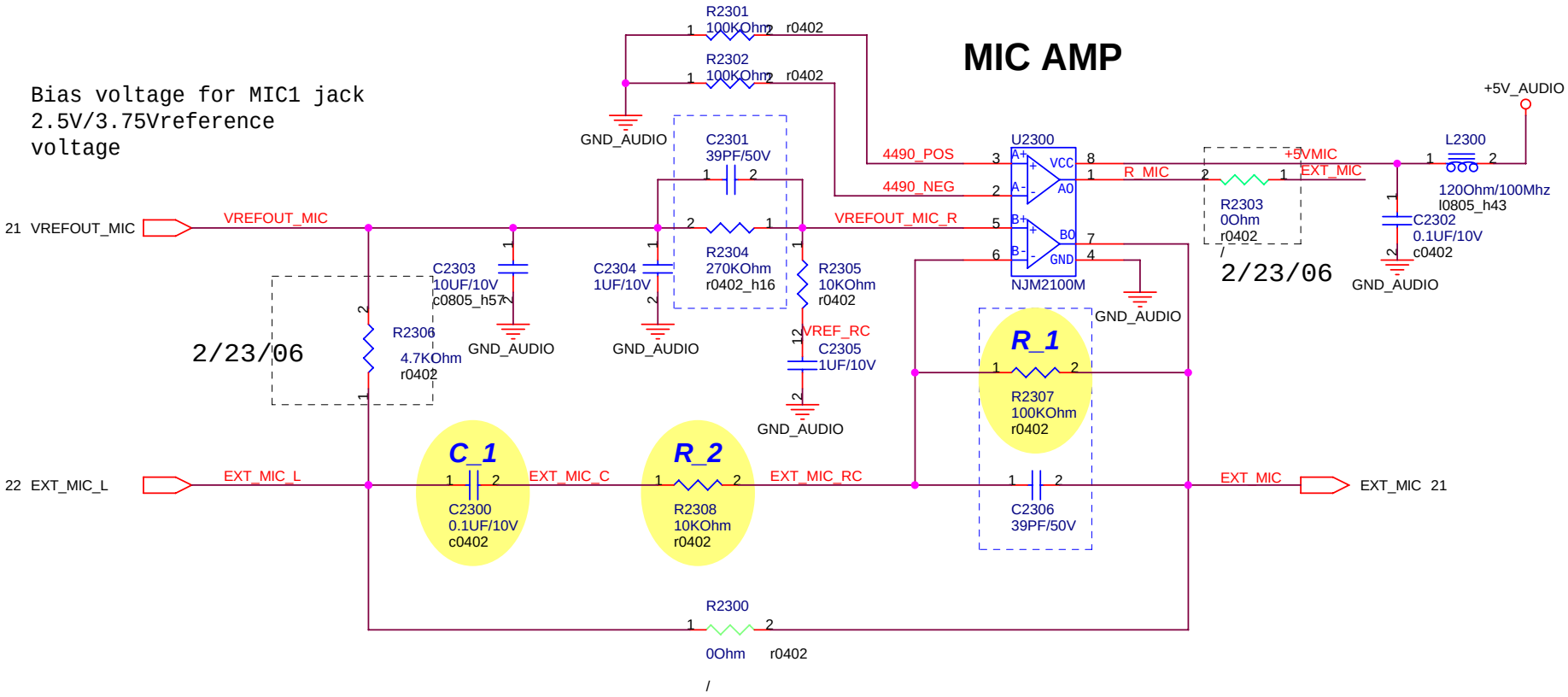

U1700F
ICH7M
U1700E
ICH7M
Layout Note:
Place above Caps within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin D28, T28 & AD28
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG5
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG9
If ICH7 embedded Lan controller was used, these pins should connect to +3VSUS for S3-S5 wake up.
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note:
Distribute in PCI section
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
6 mA
10 mA
770 mA
50 mA
640 mA
50 mA
940 mA
40 mA
56 mA
10 mA
14 mA
270 mA
45 mA
17 mA
10 mA
30 mA
ASUSTeK COMPUTER INC
Title : ICH7-M (4/4)
Engineer: Jack Wang
Size A3
Project Name A6F
Rev 1.0
Date: Monday, March 06, 2006
Sheet 20 of 63


U2100
ALC660-GR
CD-L
CD-G
CD-R
MIC_2
MIC_1
LINE_IN_LC
LINE_IN_RC
C21111
C21121
C21251
C21241
EXT_MIC 23
LINE_IN_L 22
LINE_IN_R 22
+3VS
+5V_AUDIO
GND_AUDIO
C2115 10UF/10V
C2116 0.1UF/10V
C2117 0.1UF/10V
C2113 10UF/10V
C2114 0.1UF/10V
PCBEEP
RESET#
SYNC
DVDD2
SDATA-IN
DVSS2
BCLK
SDATA-OUT
DVSS1
NC6
NC5
DVDD1
17,22 ACZ_RST#_AUD
17 ACZ_SYNC_AUD
17 ACZ_SDIN0
17 ACZ_SDOUT_AUD
17 ACZ_BCLK_AUD
R2100 0Ohm RESET#
R2109 39Ohm SDATA_IN
BIT_CLK
1N4148W D2102 POP#1
1N4148W D2101 POP#0
22 MUTE_POP_AZGPIO#
C2105 10PF/50V
R2107 0Ohm
ALC 660 NC pin
AVDD1
AVSS1
VREF
MIC1-VREFO-L
NC8
MIC2-VREFO
LINE2-VREFO
MIC1-VREFO-R
NC7
SenseB
FRONT-L(PORT-D-L)
FRONT-R(PORT-D-R)
VREF_FILT
VREF_OUT/MIC_1/2
VREFOUT_MIC 23
POP#2
12/1
VREF_OUT/MIC_2/2
T2101
LINE_OUT_L_C2103
LINE_OUT_R_C2102
1UF/10V
OUT_L 22
OUT_R 22
SPDIFO
S/PDIFO
22 S/PDIF
ALC 660 NC pin
EAR_L
EAR_R
R2123 4.99KOhm 1%
EAR_L 22
EAR_R 22
12/1
D2104
POP#2
MUTE_POP_AZGPIO#
R2124 10KOhm r0402 1N4148W
+5VS
R2120 0Ohm
C2118 10UF/10V
C2119 1UF/10V
GND
U2102
IN OUT
GND
EN NR/FB
TPS793475DBVR
25,33,36,37,39,60,61 SUSB#
T2100
C2121 10UF/10V
NR/FB
C2123 0.1UF/10V
5V-5VA_LDO
06/01
30 SPKR_CB
C2120 0.1UF/10V c0402
D2105 1N4148W
R2125 33KOhm r0402
19 SPKR_SB
C2122 0.1UF/10V c0402
D2100 1N4148W
R2112 33KOhm r0402
R2111 33KOhm r0402
C2110 0.1UF/10V
PCBEEP
R2117 0Ohm
R2118 0Ohm
R2119 0Ohm
12/1
D2103 1N4148W
R2121 10KOhm r0402
22 JACK_IN#
AMP_SHDN# 22
27 CD_L_A
R2101 0Ohm
CD_L_A_R
C2101 1UF/10V c0402
CD-L
R2102 47KOhm
27 CD_GND_A
R2104 0Ohm
CD_GND_A_R
C2104 1UF/10V c0402
CD-G
R2105 47KOhm
27 CD_R_A
R2108 0Ohm
CD_R_A_R
C2106 1UF/10V c0402
CD-R
R2110 47KOhm
VREF_FILT
C2108 10UF/10V
C2109 0.1UF/10V
ASUSTek COMPUTER INC. NB1
Title : AZALIA ALC660
Engineer: Jack Wang
Size A3
Project Name A6F
Rev 1.0
Date: Monday, March 06, 2006
Sheet 21 of 63


INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils
MIC JACK
LINE IN JACK
AUDIO OUT AMP
HEADPHONE & S/PDIF
SPEAKER CONN.
F(highpass) = 1/(2*3.14*R*C)
R=32 Ohm for Headphone, so C=68uF
But in order to reduce component type, use 100uF/6.3V(11-041210721), but 100uF is too big for A3N, so change to 47uF.
Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.
But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.
06/01
A6VM SPDIF 021406
DIGITAL
JACK_IN# OPTIC_HP
L H SPDIF
L L LINE OUT
H H NO CONNECT
Title : AUDIO AMP
ASUSTek COMPUTER INC. NB1
Engineer: Jack Wang
Project Name A6F
Rev 1.1
Date: Monday, March 06, 2006
Sheet 22 of 63

MIC AMP

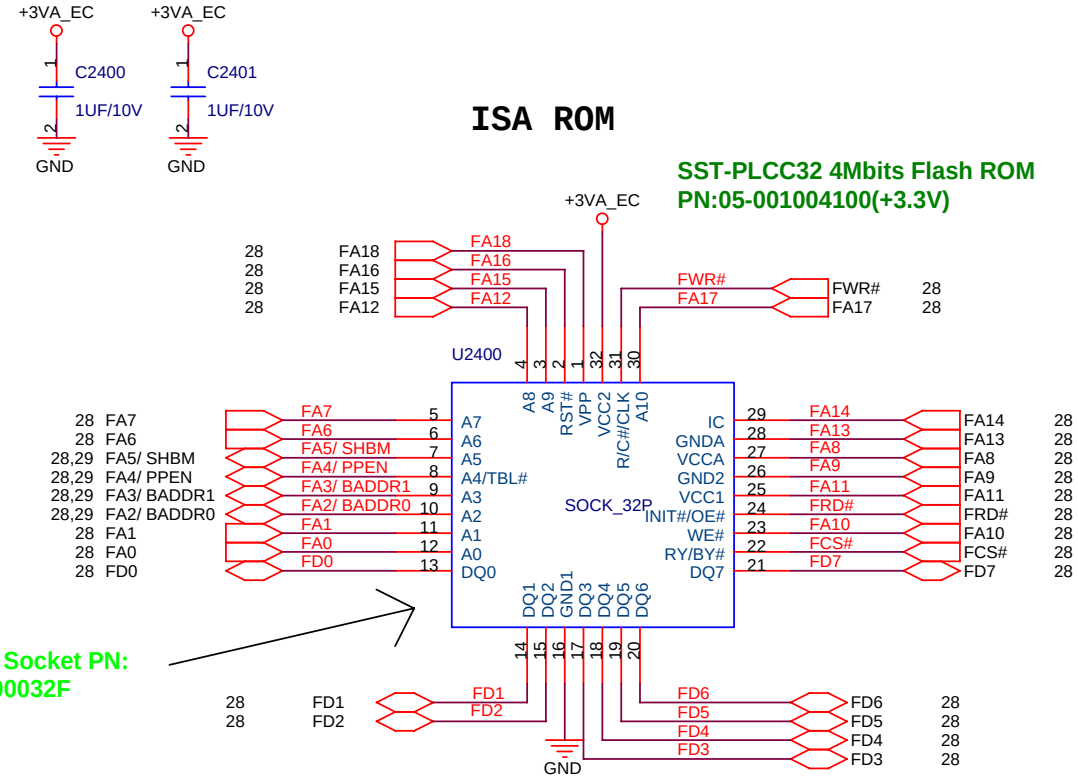
Bias voltage for MIC1 jack
2.5V/3.75Vreference
voltage



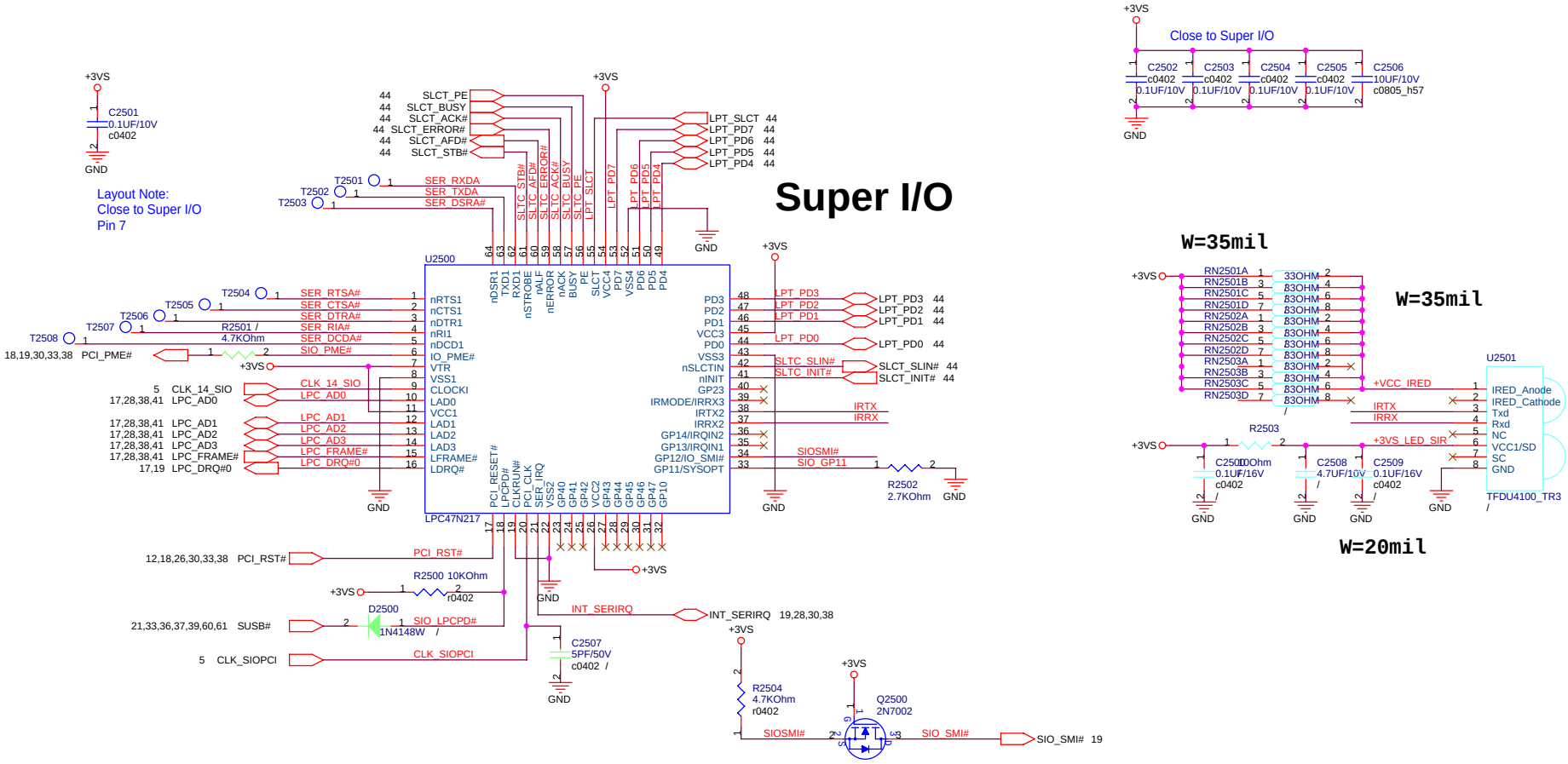
High-Pass Filter Cutoff Frequency
Fc = 1 / (2*3.14*C_1*R_2) = 159 Hz

Gain = - R_1 / R_2 = -10

ASUSTek COMPUTER INC. NB1	Title : MIC Pre-AMP	
	Engineer: *Jack Wang*	
Size: A4	Project Name: **A6F**	Rev: 1.1
Date: Monday, March 06, 2006	Sheet 23 of 63	

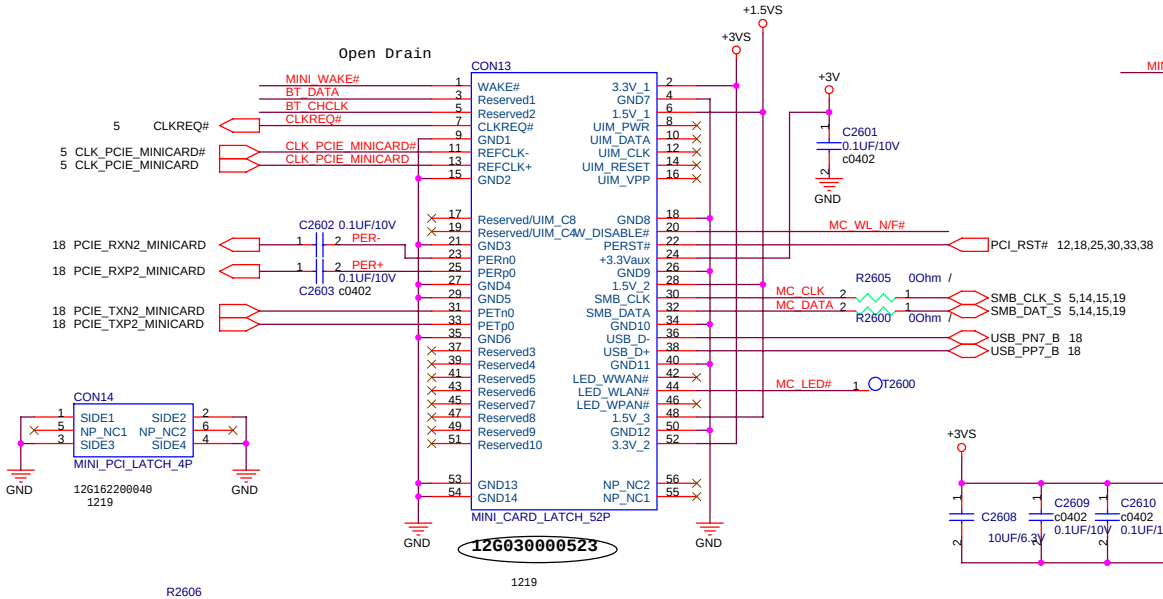


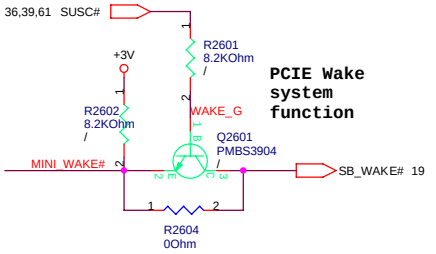
ASUSTeK COMPUTER INC	Title : ISA ROM	
	Engineer: *Jack Wang*	
Size: A4	Project Name: **A6F**	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 24 of 63	

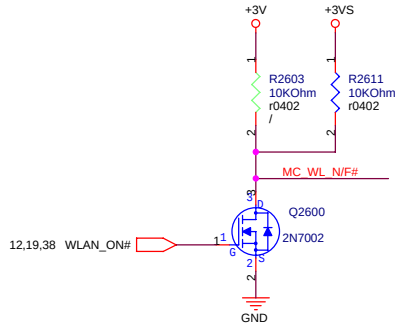


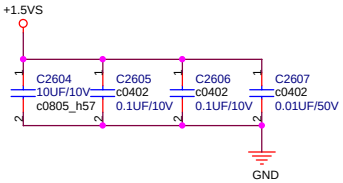
ASUSTeK COMPUTER INC	Title : SUPER I/O		
	Engineer: Jack Wang		
Size: A3	Project Name: A6F		Rev: 1.1
Date: Monday, March 06, 2006	Sheet 25 of 63		

MINI PCIEX CONNECTOR

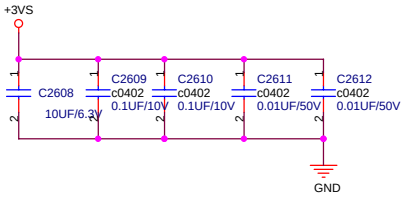




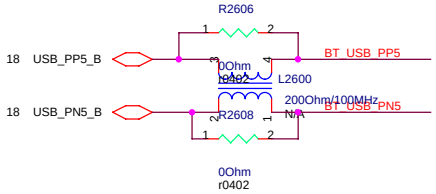




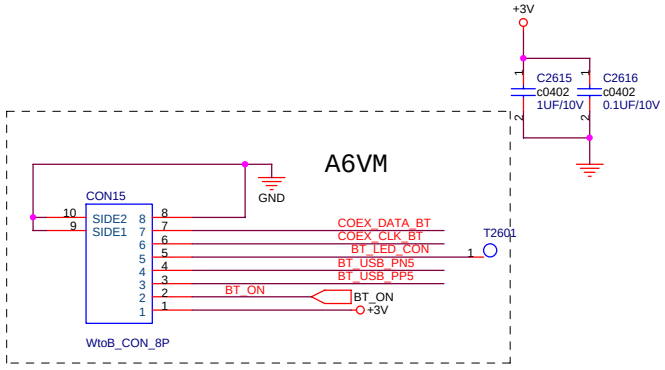
+3V : 1000 mA(peak)
+1.5V: 500mA(peak)
+3VSUS: 330mA(peak)



Check O/D output or push pull



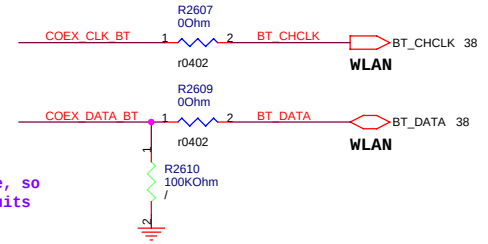
BLUETOOTH CONNECTOR



BT Connector 021406

Signal direction-
CLK: BT -> WLAN;
DATA: WLAN -> BT

BT_ON 3.3V at GPIO38



BT Module has no leakage, so discard PMOS block circuits

ASUSTeK COMPUTER INC

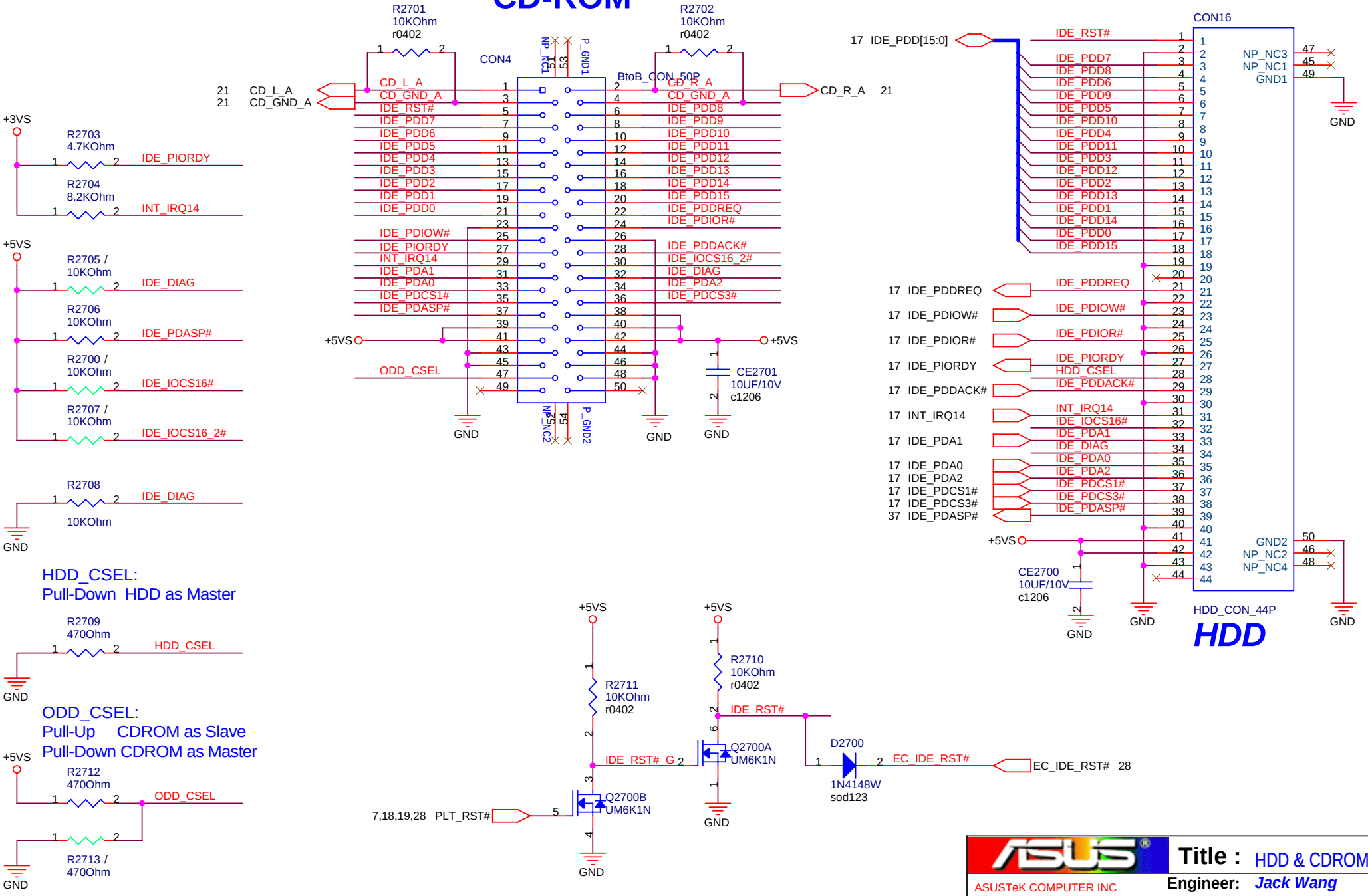
Title : MINI PCIEX (TV) & BT Conn

Engineer: Jack Wang

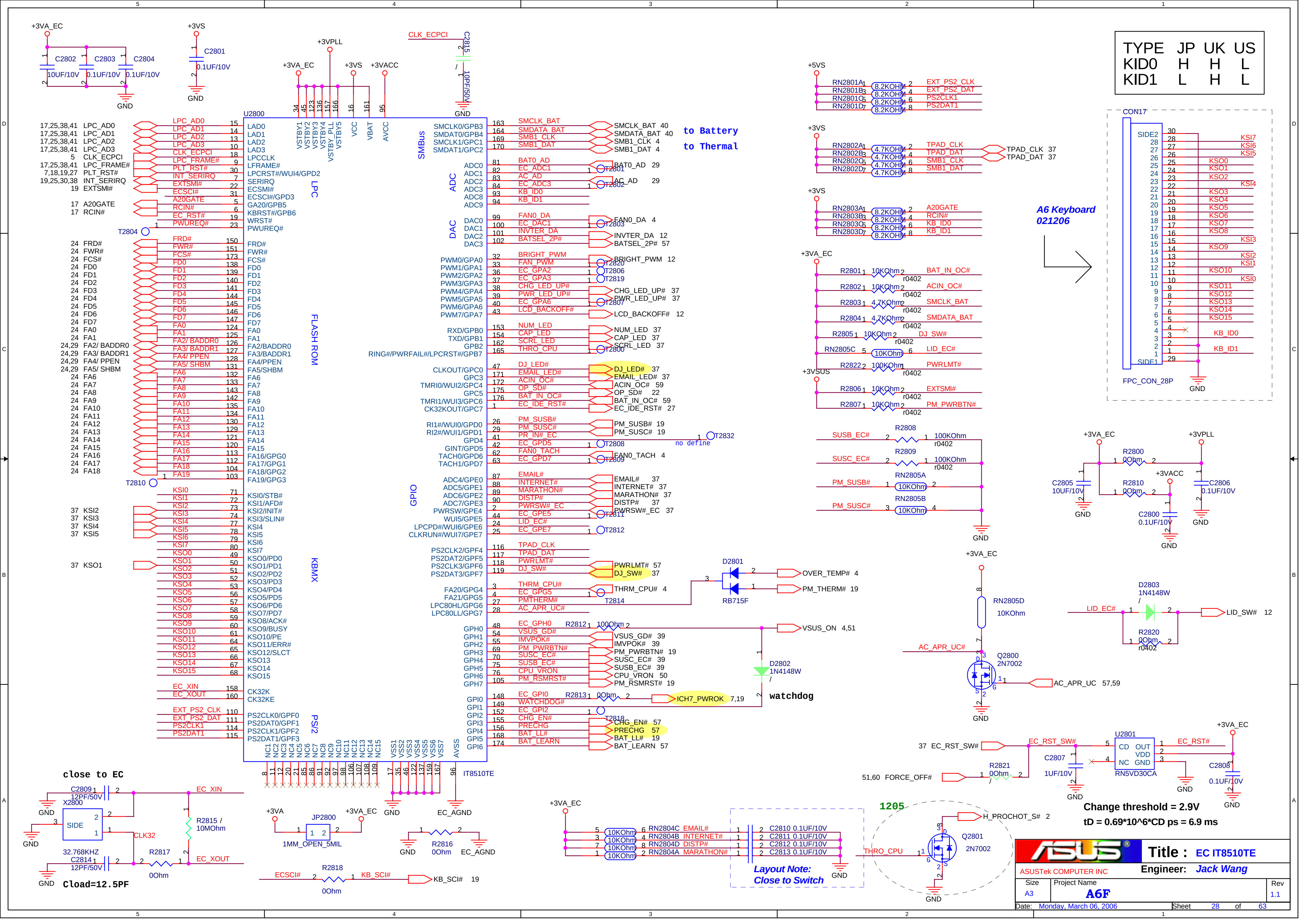
Size	Project Name	Rev
A3	A6F	1.1

Date: Monday, March 06, 2006 Sheet 26 of 63

CD-ROM



ASUSTeK COMPUTER INC	Title : HDD & CDROM		
	Engineer: Jack Wang		
Size: A4	Project Name: A6F		Rev: 1.0
Date: Monday, March 06, 2006	Sheet 27 of 63		



TYPE JP UK US
KID0 H H L
KID1 L H L
U2800
IT8510TE
LPC
FLASH ROM
KBMX
PS/2
SMBus
ADC
DAC
GPIO
to Battery
to Thermal
A6 Keyboard
021206
CON17
FPC_CON_28P
D2801
RB715F
D2802
1N4148W
watchdog
D2803
1N4148W
Q2800
2N7002
Q2801
2N7002
U2801
RN5VD30CA
Change threshold = 2.9V
tD = 0.69*10^6*CD ps = 6.9 ms
close to EC
X2800
32.768KHZ
Cload=12.5PF
JP2800
1MM_OPEN_5MIL
Layout Note:
Close to Switch
1205
ASUSTek COMPUTER INC
Title : EC IT8510TE
Engineer: Jack Wang
Size A3
Project Name A6F
Rev 1.1
Date: Monday, March 06, 2006
Sheet 28 of 63

EC Hardware Strap

Strap value sampled after VSTBY power up reset

+3VA_EC

PNPCFG base address set by SWCBAHR/SWCBALR

R2901 / 10KOhm r0402

FA2/ BADDR0 → FA2/ BADDR0 24,28

R2905 10KOhm r0402

GND

+3VA_EC

R2902 10KOhm r0402

FA3/ BADDR1 → FA3/ BADDR1 24,28

R2906 / 10KOhm r0402

GND

BADDR[1:0]

No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

Share Memory

+3VA_EC

R2909 10KOhm r0402

FA5/ SHBM → FA5/ SHBM 24,28

R2912 / 10KOhm r0402

GND

SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

+3VA_EC

R2900 / 10KOhm r0402

FA4/ PPEN → FA4/ PPEN 24,28

R2913 10KOhm r0402

GND

PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

EC ADC

Battery

BAT **16.8V**

+3VACC

R2903 / 18KOhm r0402_h16

D2901 / 1N4148W

R2904 / 1KOhm

BAT0_R_AD

BAT0_AD 28

R2907 / 3.92KOhm

D2902 / 1N4148W

C2900 / 0.1UF/10V c0402

GND

Adaptor

A/D_DOCK_IN **19V**

+3VACC

R2908 / 20KOhm

D2903 / 1N4148W

R2910 / 1KOhm

AC_R_AD

AC_AD 28

3V

R2911 / 3.74KOhm

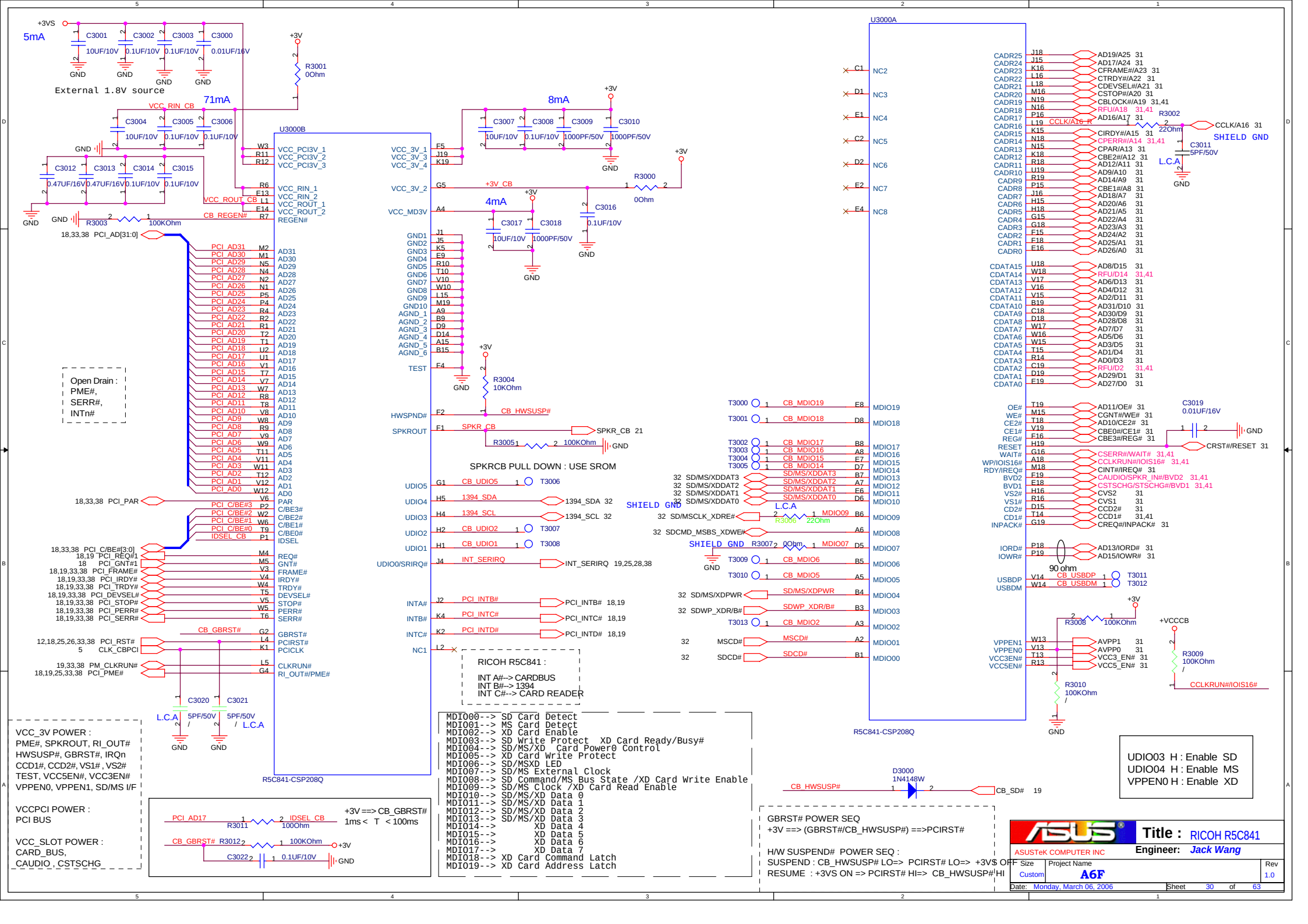
D2900 / 1N4148W

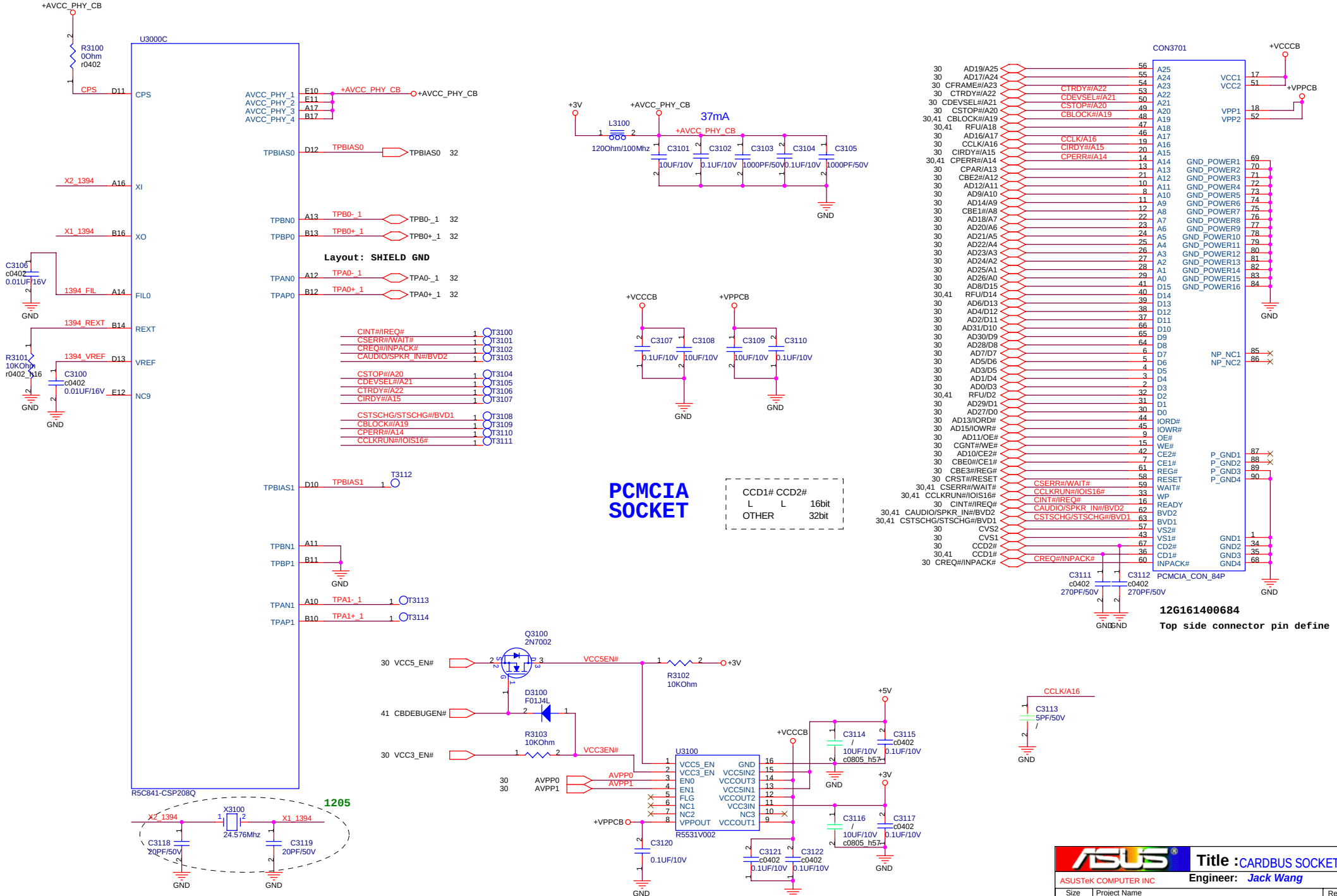
C2901 / 0.1UF/10V c0402

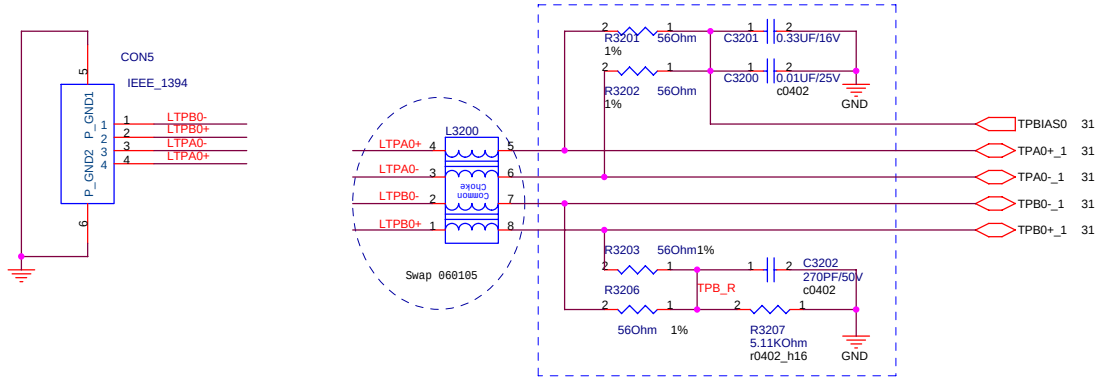
2.99V

GND

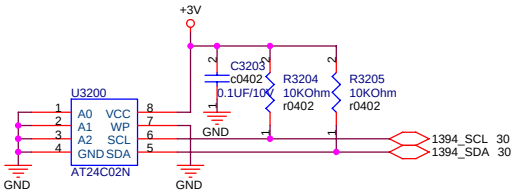
ASUSTek COMPUTER INC	**Title :** EC IT8510TE(2/2)	
	Engineer: *Jack Wang*	
Size: A4	Project Name: **A6F**	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 29 of 63	

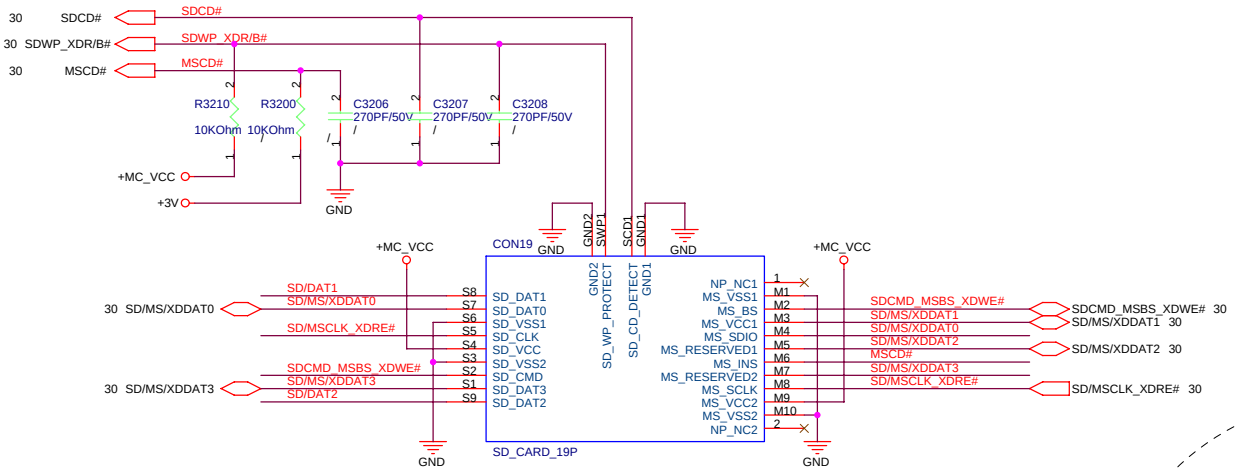

+3VS
5mA
C3001 10UF/10V
C3002 0.1UF/10V
C3003 0.1UF/10V
C3000 0.01UF/16V
GND
External 1.8V source
+3V
R3001 0Ohm
71mA
VCC_RIN_CB
C3004 10UF/10V
C3005 0.1UF/10V
C3006 0.1UF/10V
C3012 0.47UF/16V
C3013 0.47UF/16V
C3014 0.1UF/10V
C3015 0.1UF/10V
VCC_ROUT_CB
CB_REGEN#
R3003 100KOhm
18,33,38 PCI_AD[31:0]
PCI_AD31 PCI_AD30 PCI_AD29 PCI_AD28 PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_AD23 PCI_AD22 PCI_AD21 PCI_AD20 PCI_AD19 PCI_AD18 PCI_AD17 PCI_AD16 PCI_AD15 PCI_AD14 PCI_AD13 PCI_AD12 PCI_AD11 PCI_AD10 PCI_AD9 PCI_AD8 PCI_AD7 PCI_AD6 PCI_AD5 PCI_AD4 PCI_AD3 PCI_AD2 PCI_AD1 PCI_AD0
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
Open Drain : PME#, SERR#, INTn#
18,33,38 PCI_PAR
PAR
18,33,38 PCI_C/BE#[3:0]
C/BE3# C/BE2# C/BE1# C/BE0#
IDSEL_CB
IDSEL
18,19 PCI_REQ#1
18 PCI_GNT#1
REQ# GNT#
18,19,33,38 PCI_FRAME#
18,19,33,38 PCI_IRDY#
18,19,33,38 PCI_TRDY#
18,19,33,38 PCI_DEVSEL#
18,19,33,38 PCI_STOP#
18,19,33,38 PCI_PERR#
18,19,33,38 PCI_SERR#
FRAME# IRDY# TRDY# DEVSEL# STOP# PERR# SERR#
CB_GBRST#
GBRST#
12,18,25,26,33,38 PCI_RST#
5 CLK_CBPCI
PCIRST# PCICLK
19,33,38 PM_CLKRUN#
18,19,25,33,38 PCI_PME#
CLKRUN# RI_OUT#/PME#
C3020 5PF/50V
C3021 5PF/50V
L.C.A
U3000B
VCC_PCI3V_1 VCC_PCI3V_2 VCC_PCI3V_3
VCC_RIN_1 VCC_RIN_2 VCC_ROUT_1 VCC_ROUT_2 REGEN#
R5C841-CSP208Q
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
PCI_AD17
R3011 100Ohm
IDSEL_CB
+3V ==> CB_GBRST#
1ms < T < 100ms
CB_GBRST# R3012 100KOhm
C3022 0.1UF/10V
VCC_3V_1 VCC_3V_3 VCC_3V_4
VCC_3V_2
VCC_MD3V
8mA
C3007 10UF/10V
C3008 0.1UF/10V
C3009 1000PF/50V
C3010 1000PF/50V
+3V_CB
R3000 0Ohm
4mA
C3017 10UF/10V
C3018 1000PF/50V
C3016 0.1UF/10V
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10
AGND_1 AGND_2 AGND_3 AGND_4 AGND_5 AGND_6
TEST
R3004 10KOhm
HWSPND#
CB_HWSUSP#
SPKROUT
SPKR_CB
SPKR_CB 21
R3005 100KOhm
SPKRCB PULL DOWN : USE SROM
UDIO5 CB_UDIO5 T3006
UDIO4 1394_SDA 1394_SDA 32
UDIO3 1394_SCL 1394_SCL 32
UDIO2 CB_UDIO2 T3007
UDIO1 CB_UDIO1 T3008
UDIO0/SRIRQ# INT_SERIRQ INT_SERIRQ 19,25,28,38
INTA# PCI_INTB# PCI_INTB# 18,19
INTB# PCI_INTC# PCI_INTC# 18,19
INTC# PCI_INTD# PCI_INTD# 18,19
NC1
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
U3000A
NC2 NC3 NC4 NC5 NC6 NC7 NC8
T3000 CB_MDIO19 MDIO19
T3001 CB_MDIO18 MDIO18
T3002 CB_MDIO17 MDIO17
T3003 CB_MDIO16 MDIO16
T3004 CB_MDIO15 MDIO15
T3005 CB_MDIO14 MDIO14
32 SD/MS/XDDAT3 SD/MS/XDDAT3 MDIO13
32 SD/MS/XDDAT2 SD/MS/XDDAT2 MDIO12
32 SD/MS/XDDAT1 SD/MS/XDDAT1 MDIO11
32 SD/MS/XDDAT0 SD/MS/XDDAT0 MDIO10
SHIELD GND
32 SD/MSCLK_XDRE# R3006 22Ohm MDIO09
32 SDCMD_MSBS_XDWE# MDIO08
SHIELD GND R3007 0Ohm MDIO07
T3009 CB_MDIO6 MDIO06
T3010 CB_MDIO5 MDIO05
32 SD/MS/XDPWR SD/MS/XDPWR MDIO04
32 SDWP_XDR/B# SDWP_XDR/B# MDIO03
T3013 CB_MDIO2 MDIO02
32 MSCD# MSCD# MDIO01
32 SDCD# SDCD# MDIO00
R5C841-CSP208Q
CADR25 CADR24 CADR23 CADR22 CADR21 CADR20 CADR19 CADR18 CADR17 CADR16 CADR15 CADR14 CADR13 CADR12 CADR11 CADR10 CADR9 CADR8 CADR7 CADR6 CADR5 CADR4 CADR3 CADR2 CADR1 CADR0
AD19/A25 AD17/A24 CFRAME#/A23 CTRDY#/A22 CDEVSEL#/A21 CSTOP#/A20 CBLOCK#/A19 RFU/A18 AD16/A17
CCLK/A16_R
R3002 22Ohm
CCLK/A16 31
SHIELD GND
C3011 5PF/50V
L.C.A
CIRDY#/A15 CPERR#/A14 CPAR/A13 CBE2#/A12 AD12/A11 AD9/A10 AD14/A9 CBE1#/A8 AD18/A7 AD20/A6 AD21/A5 AD22/A4 AD23/A3 AD24/A2 AD25/A1 AD26/A0
CDATA15 CDATA14 CDATA13 CDATA12 CDATA11 CDATA10 CDATA9 CDATA8 CDATA7 CDATA6 CDATA5 CDATA4 CDATA3 CDATA2 CDATA1 CDATA0
AD8/D15 RFU/D14 AD6/D13 AD4/D12 AD2/D11 AD31/D10 AD30/D9 AD28/D8 AD7/D7 AD5/D6 AD3/D5 AD1/D4 AD0/D3 RFU/D2 AD29/D1 AD27/D0
OE# WE# CE2# CE1# REG# RESET WAIT# WP/IOIS16# RDY/IREQ# BVD2 BVD1 VS2# VS1# CD2# CD1# INPACK#
AD11/OE# CGNT#/WE# AD10/CE2# CBE0#/CE1# CBE3#/REG# CRST#/RESET
C3019 0.01UF/16V
GND
CSERR#/WAIT# CCLKRUN#/IOIS16# CINT#/IREQ# CAUDIO/SPKR_IN#/BVD2 CSTSCHG/STSCHG#/BVD1 CVS2 CVS1 CCD2# CCD1# CREQ#/INPACK#
IORD# IOWR#
AD13/IORD# AD15/IOWR#
90 ohm
USBDP USBDM
CB_USBDP T3011
CB_USBDM T3012
R3008 100KOhm
+VCCCB
R3009 100KOhm
CCLKRUN#/IOIS16#
VPPEN1 VPPEN0 VCC3EN# VCC5EN#
AVPP1 AVPP0 VCC3_EN# VCC5_EN#
R3010 100KOhm
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
CB_HWSUSP#
D3000 1N4148W
CB_SD# 19
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3V$ OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP#/HI
ASUSTeK COMPUTER INC
Title : RICOH R5C841
Engineer: Jack Wang
Size Custom
Project Name A6F
Rev 1.0
Date: Monday, March 06, 2006
Sheet 30 of 63


+AVCC_PHY_CB
R3100
0Ohm
r0402
U3000C
CPS
D11
CPS
X2_1394
A16
XI
X1_1394
B16
XO
1394_FIL
A14
FIL0
1394_REXT
B14
REXT
1394_VREF
D13
VREF
E12
NC9
C3106
c0402
0.01UF/16V
R3101
10KOhm
r0402_h16
C3100
c0402
0.01UF/16V
GND
AVCC_PHY_1
AVCC_PHY_2
AVCC_PHY_3
AVCC_PHY_4
E10
E11
A17
B17
+AVCC_PHY_CB
TPBIAS0
D12
TPBIAS0
TPBN0
A13
TPB0-_1
TPBP0
B13
TPB0+_1
Layout: SHIELD GND
TPAN0
A12
TPA0-_1
TPAP0
B12
TPA0+_1
CINT#/IREQ#
CSERR#/WAIT#
CREQ#/INPACK#
CAUDIO/SPKR_IN#/BVD2
CSTOP#/A20
CDEVSEL#/A21
CTRDY#/A22
CIRDY#/A15
CSTSCHG/STSCHG#/BVD1
CBLOCK#/A19
CPERR#/A14
CCLKRUN#/IOIS16#
T3100
T3101
T3102
T3103
T3104
T3105
T3106
T3107
T3108
T3109
T3110
T3111
TPBIAS1
D10
T3112
TPBN1
A11
TPBP1
B11
TPAN1
A10
TPA1-_1
T3113
TPAP1
B10
TPA1+_1
T3114
R5C841-CSP208Q
X3100
24.576Mhz
C3118
20PF/50V
C3119
20PF/50V
1205
+3V
L3100
120Ohm/100Mhz
37mA
C3101
10UF/10V
C3102
0.1UF/10V
C3103
1000PF/50V
C3104
0.1UF/10V
C3105
1000PF/50V
+VCCCB
+VPPCB
C3107
0.1UF/10V
C3108
10UF/10V
C3109
10UF/10V
C3110
0.1UF/10V
PCMCIA
SOCKET
CCD1# CCD2#
L L 16bit
OTHER 32bit
CON3701
PCMCIA_CON_84P
+VCCCB
+VPPCB
C3111
c0402
270PF/50V
C3112
c0402
270PF/50V
12G161400684
Top side connector pin define
Q3100
2N7002
VCC5_EN#
VCC5EN#
R3102
10KOhm
D3100
F01J4L
CBDEBUGEN#
R3103
10KOhm
VCC3_EN#
VCC3EN#
AVPP0
AVPP1
U3100
R5531V002
C3120
0.1UF/10V
C3121
c0402
0.1UF/10V
C3122
c0402
0.1UF/10V
C3114
10UF/10V
C3115
c0402
0.1UF/10V
C3116
10UF/10V
C3117
c0402
0.1UF/10V
c0805_h57
+5V
CCLK/A16
C3113
5PF/50V
ASUSTeK COMPUTER INC
Title : CARDBUS SOCKET
Engineer: Jack Wang
Size A3
Project Name A6F
Rev 1.0
Date: Monday, March 06, 2006
Sheet 31 of 63

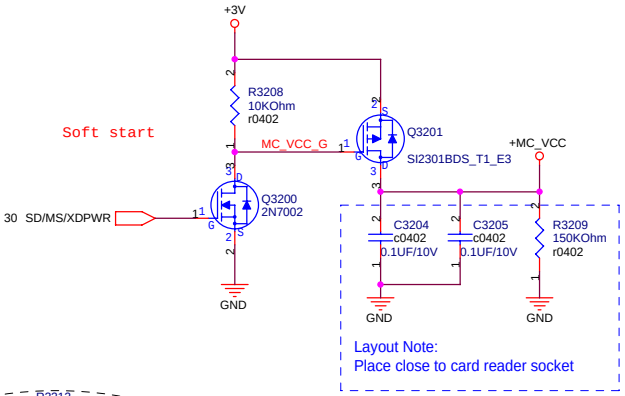


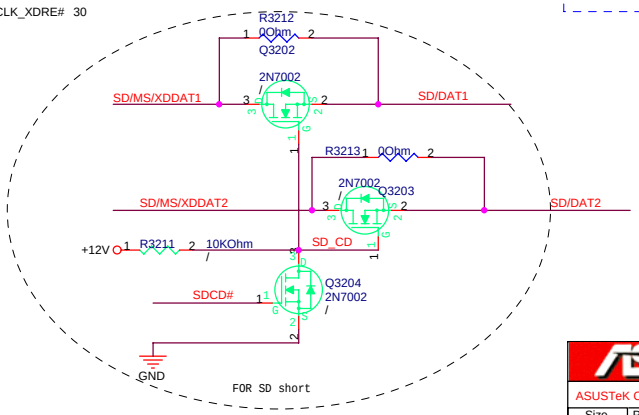
1. Close to R5C841
2. The area is as compact as possible,length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5mm
4. No via recommend , maxmium is one.
5. Total length < 50 mm
6. Differential impedance is 110+/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25mm



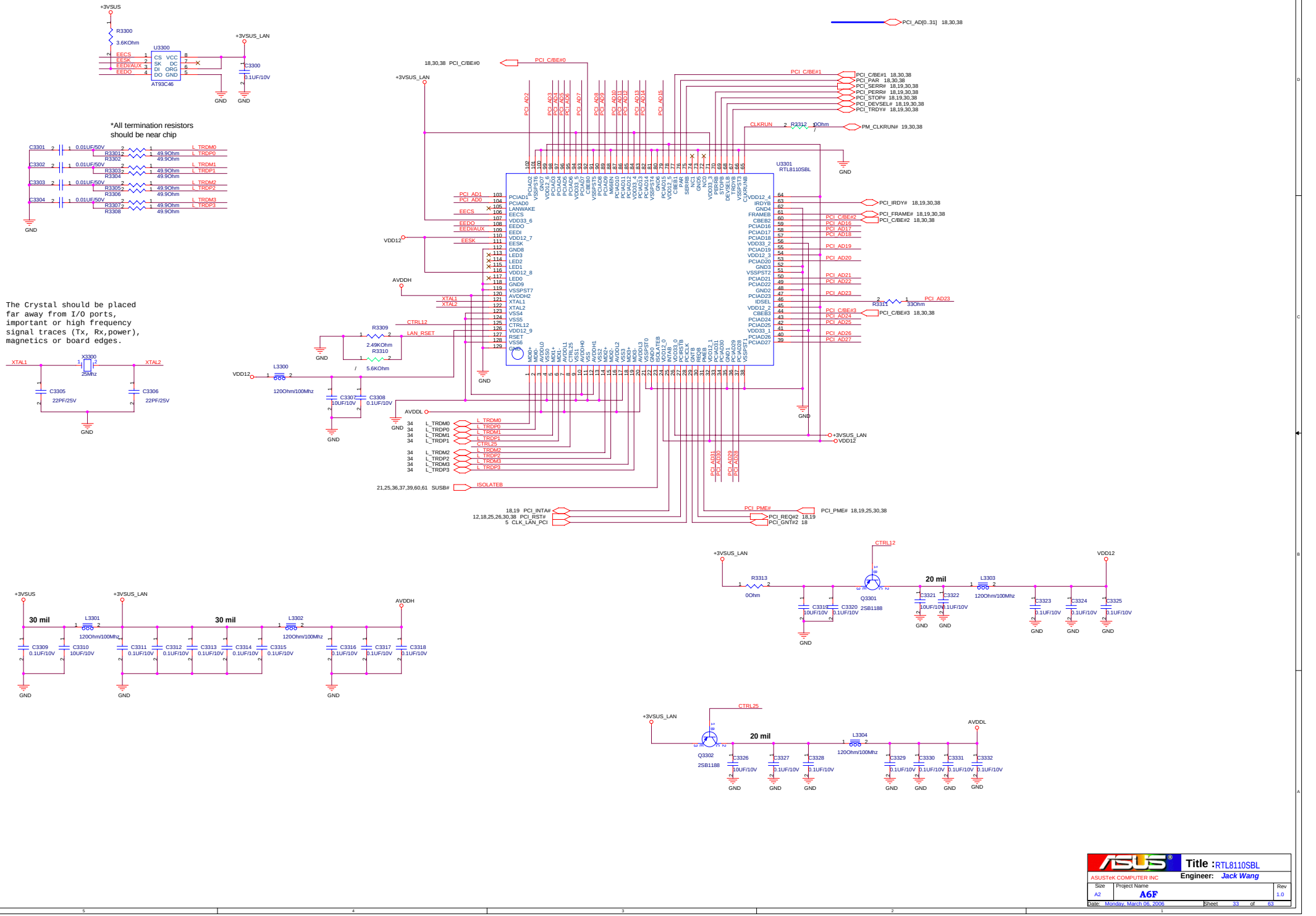


Layout: SHIELD GND

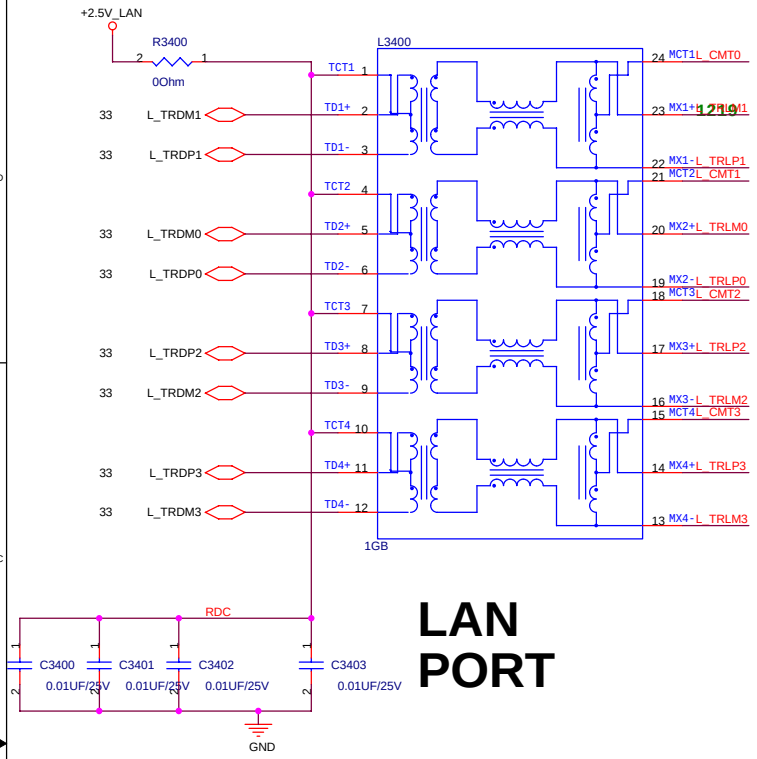


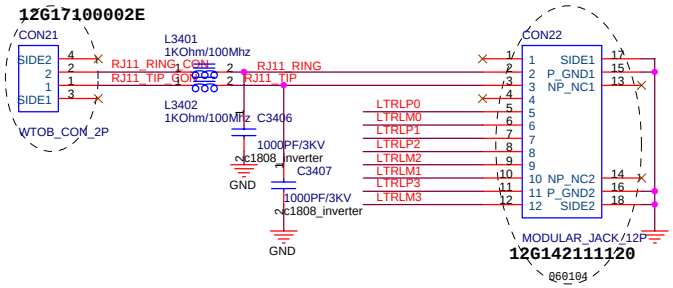


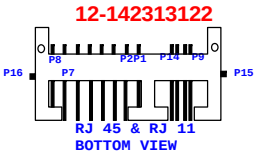
ASUSTeK COMPUTER INC	Title : 1394 & 3 IN 1 CON	
	Engineer: *Jack Wang*	
Size: A3	Project Name: **A6F**	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 32 of 63	

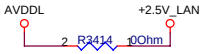

+3VSUS
R3300
3.6KOhm
U3300
EECS
EESK
EEDI/AUX
EEDO
CS VCC
SK DC
DI ORG
DO GND
AT93C46
+3VSUS_LAN
C3300
0.1UF/10V
GND
*All termination resistors
should be near chip
C3301 0.01UF/50V
R3301 49.9Ohm
R3302 49.9Ohm
L_TRDM0
L_TRDP0
C3302 0.01UF/50V
R3303 49.9Ohm
R3304 49.9Ohm
L_TRDM1
L_TRDP1
C3303 0.01UF/50V
R3305 49.9Ohm
R3306 49.9Ohm
L_TRDM2
L_TRDP2
C3304 0.01UF/50V
R3307 49.9Ohm
R3308 49.9Ohm
L_TRDM3
L_TRDP3
The Crystal should be placed
far away from I/O ports,
important or high frequency
signal traces (Tx, Rx,power),
magnetics or board edges.
XTAL1
X3300
25Mhz
XTAL2
C3305 22PF/25V
C3306 22PF/25V
PCI_AD[0..31] 18,30,38
18,30,38 PCI_C/BE#0
PCI_C/BE#0
PCI_C/BE#1
PCI_C/BE#1 18,30,38
PCI_PAR 18,30,38
PCI_SERR# 18,19,30,38
PCI_PERR# 18,19,30,38
PCI_STOP# 18,19,30,38
PCI_DEVSEL# 18,19,30,38
PCI_TRDY# 18,19,30,38
CLKRUN
R3312 10Ohm
PM_CLKRUN# 19,30,38
U3301
RTL8110SBL
PCI_IRDY# 18,19,30,38
PCI_FRAME# 18,19,30,38
PCI_C/BE#2 18,30,38
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
PCI_AD21
PCI_AD22
PCI_AD23
R3311 33Ohm
PCI_C/BE#3 18,30,38
PCI_AD24
PCI_AD25
PCI_AD26
PCI_AD27
PCI_AD1
PCI_AD0
EECS
EEDO
EEDI/AUX
EESK
XTAL1
XTAL2
CTRL12
R3309 2.49KOhm
LAN_RSET
R3310 5.6KOhm
L3300
120Ohm/100Mhz
C3307 10UF/10V
C3308 0.1UF/10V
AVDDL
L_TRDM0
L_TRDP0
L_TRDM1
L_TRDP1
CTRL25
L_TRDM2
L_TRDP2
L_TRDM3
L_TRDP3
21,25,36,37,39,60,61 SUSB#
ISOLATEB
18,19 PCI_INTA#
12,18,25,26,30,38 PCI_RST#
5 CLK_LAN_PCI
PCI_PME#
PCI_PME# 18,19,25,30,38
PCI_REQ#2 18,19
PCI_GNT#2 18
+3VSUS_LAN
VDD12
+3VSUS
30 mil
L3301
120Ohm/100Mhz
C3309 0.1UF/10V
C3310 10UF/10V
+3VSUS_LAN
30 mil
L3302
120Ohm/100Mhz
C3311 0.1UF/10V
C3312 0.1UF/10V
C3313 0.1UF/10V
C3314 0.1UF/10V
C3315 0.1UF/10V
C3316 0.1UF/10V
C3317 0.1UF/10V
C3318 0.1UF/10V
AVDDH
GND
CTRL12
+3VSUS_LAN
R3313 0Ohm
Q3301 2SB1188
C3319 10UF/10V
C3320 0.1UF/10V
20 mil
L3303
120Ohm/100Mhz
C3321 10UF/10V
C3322 0.1UF/10V
C3323 0.1UF/10V
C3324 0.1UF/10V
C3325 0.1UF/10V
VDD12
CTRL25
+3VSUS_LAN
Q3302 2SB1188
20 mil
L3304
120Ohm/100Mhz
C3326 10UF/10V
C3327 0.1UF/10V
C3328 0.1UF/10V
C3329 0.1UF/10V
C3330 0.1UF/10V
C3331 0.1UF/10V
C3332 0.1UF/10V
AVDDL
GND
ASUSTeK COMPUTER INC
Title : RTL8110SBL
Engineer: Jack Wang
Size A2
Project Name A6F
Rev 1.0
Date: Monday, March 06, 2006
Sheet 33 of 63

LAN PORT

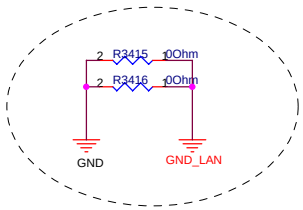




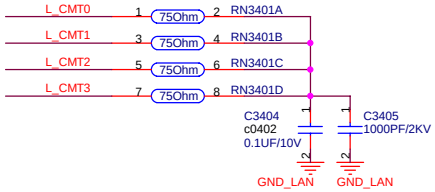


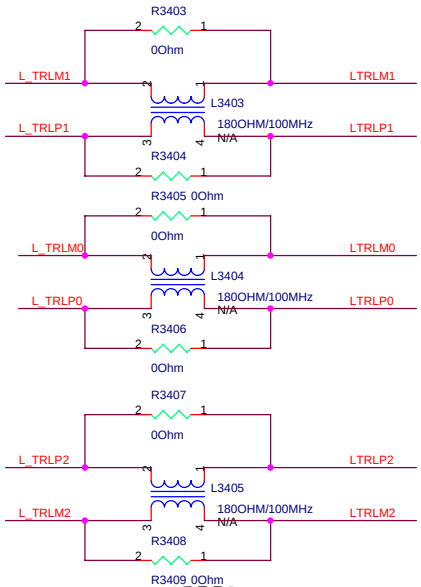


LAN PORT

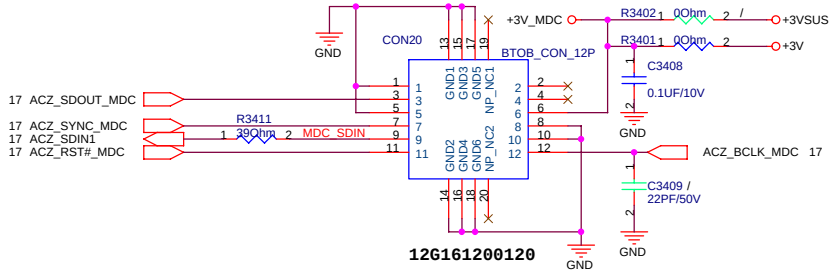


Change 1228



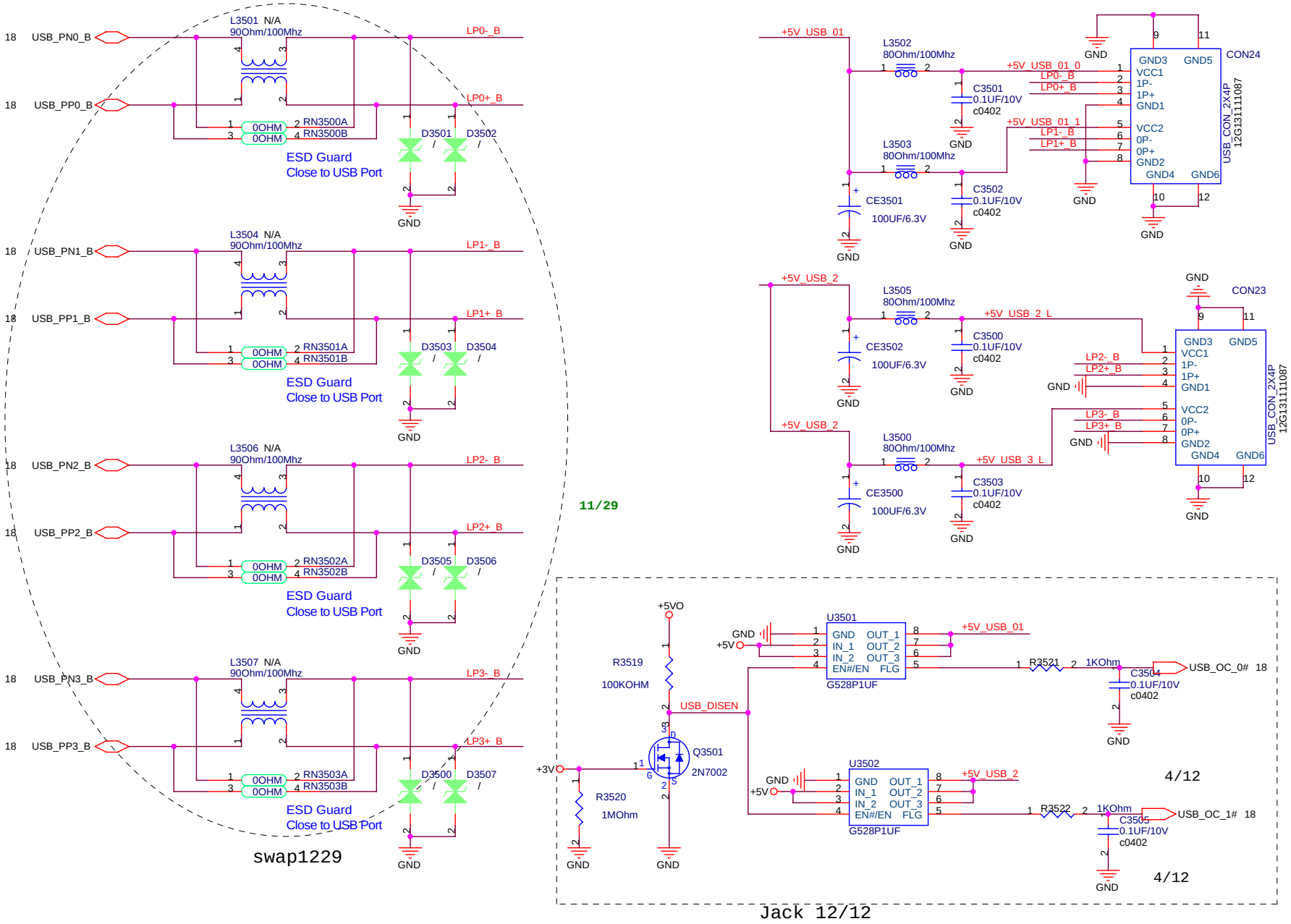


MDC Conn

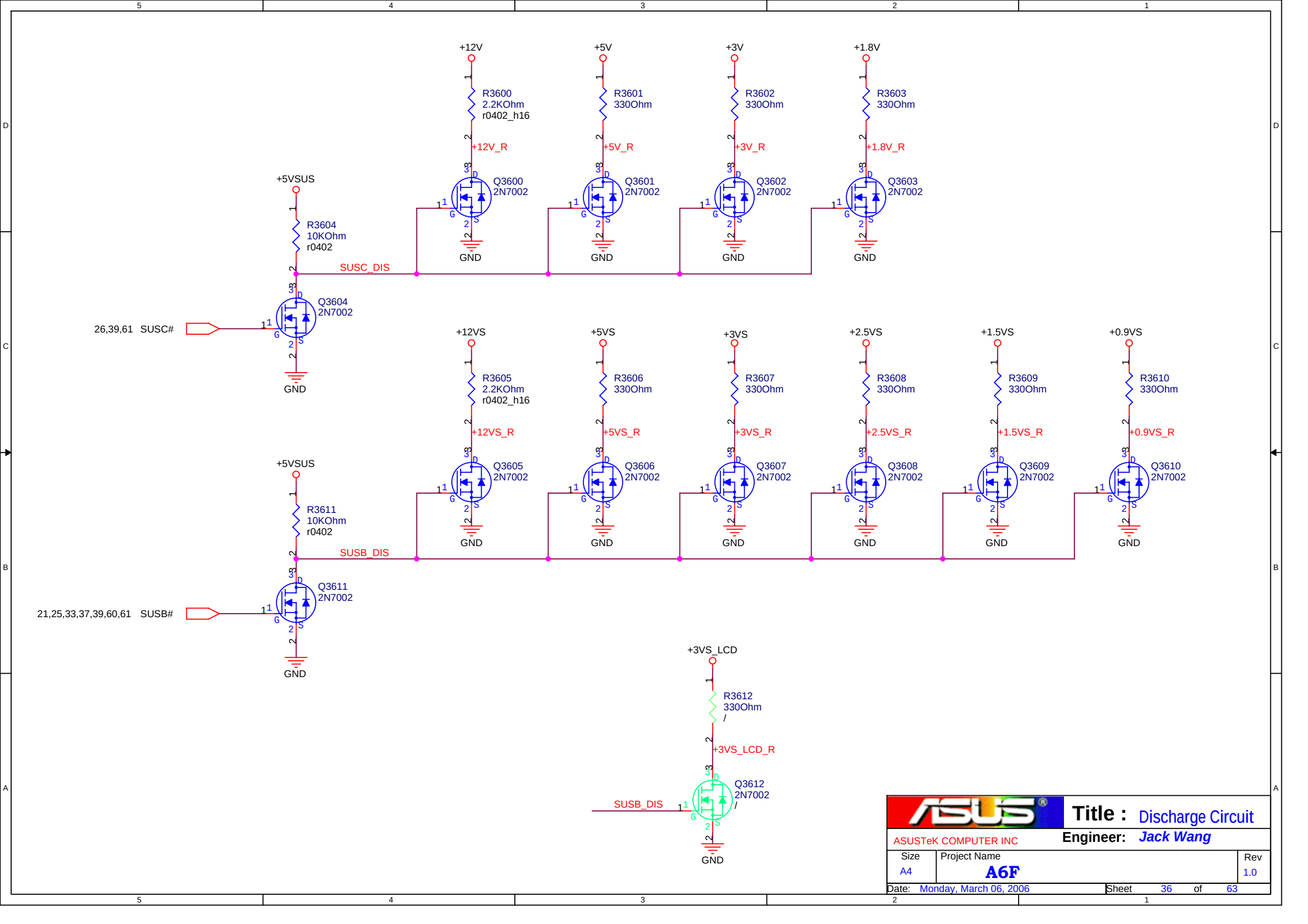


12.26 swap1229

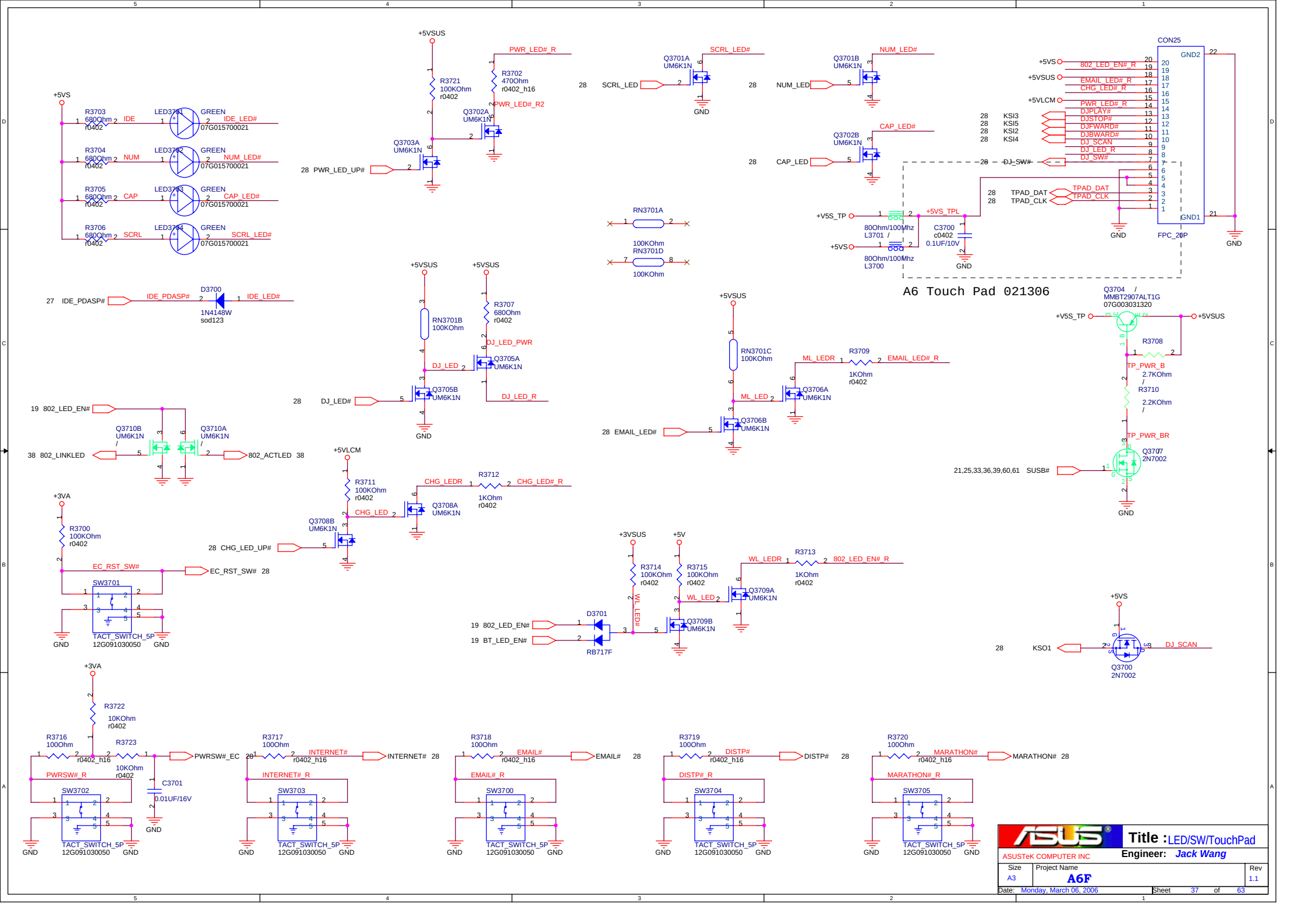
ASUSTeK COMPUTER INC		Title :	RJ11/45 & MDC
		Engineer:	Jack Wang
Size	Project Name		Rev
A3	A6F		1.0
Date: Monday, March 06, 2006		Sheet 34 of 63	



ASUSTeK COMPUTER INC	Title : USB CONN X 4	
	Engineer: Jack Wang	
Size: Custom	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 35 of 63	



ASUSTeK COMPUTER INC	Title : Discharge Circuit	
	Engineer: Jack Wang	
Size: A4	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 36 of 63	



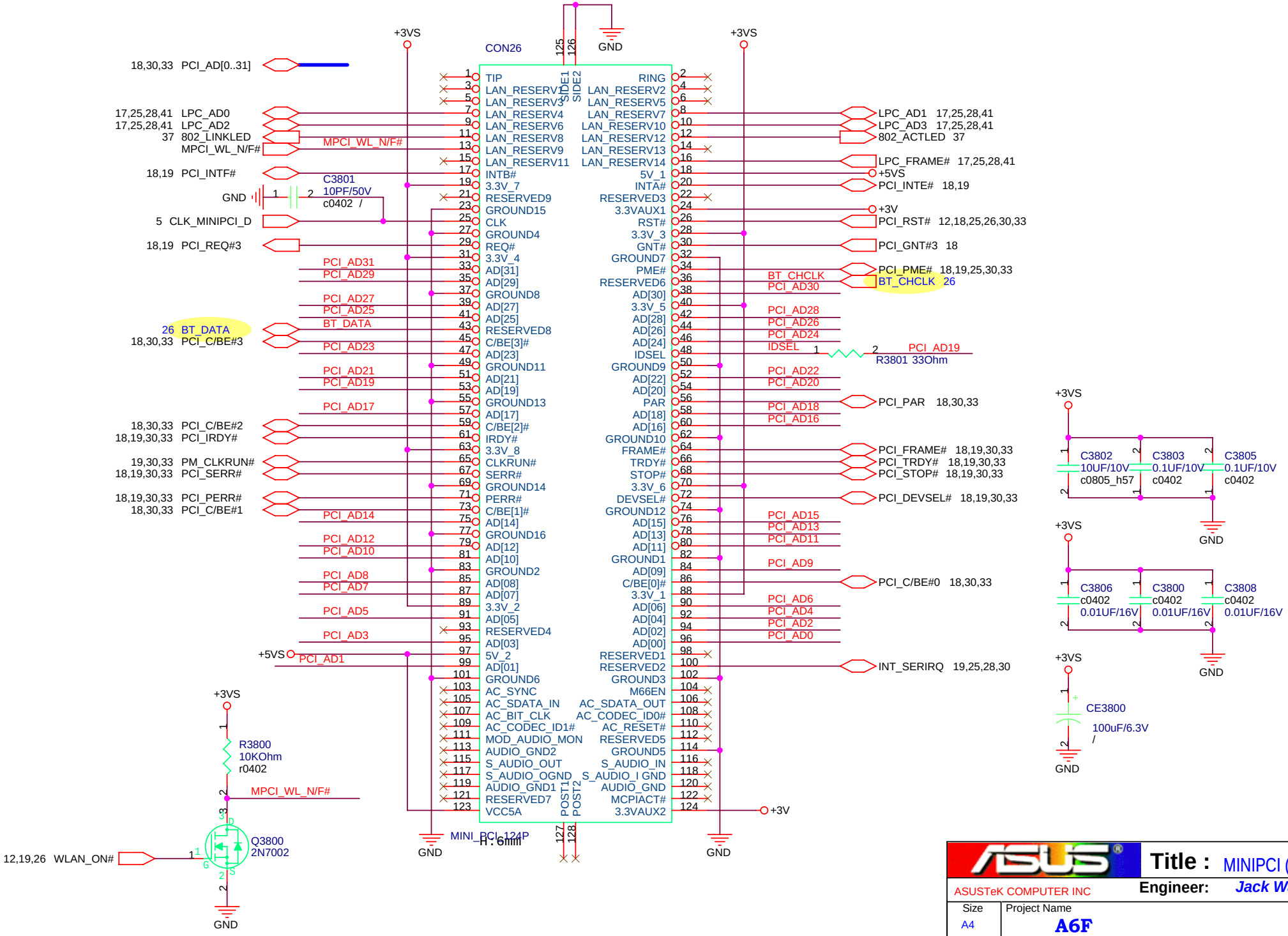
ASUSTeK COMPUTER INC

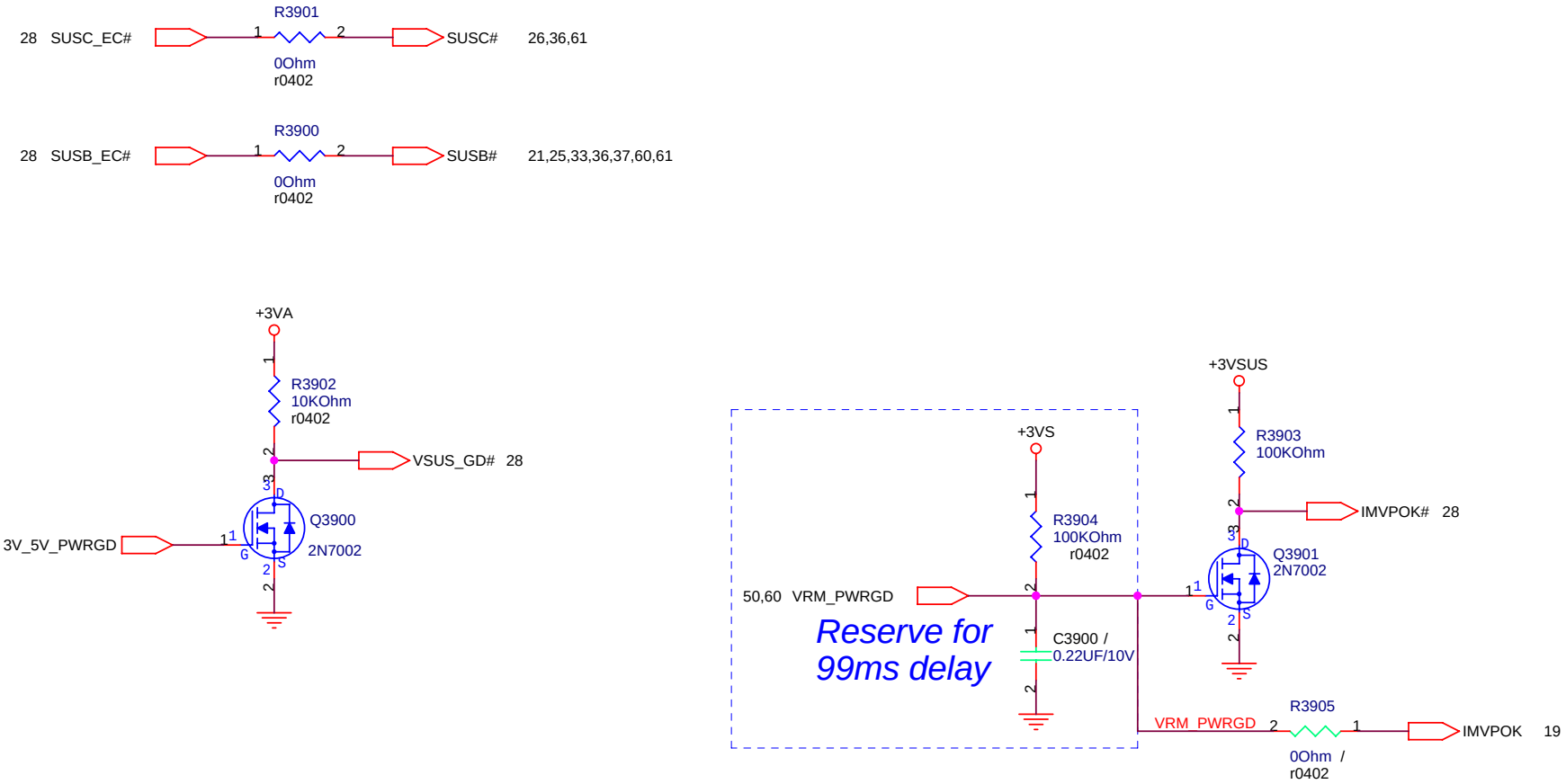
Title : LED/SW/TouchPad

Engineer: Jack Wang

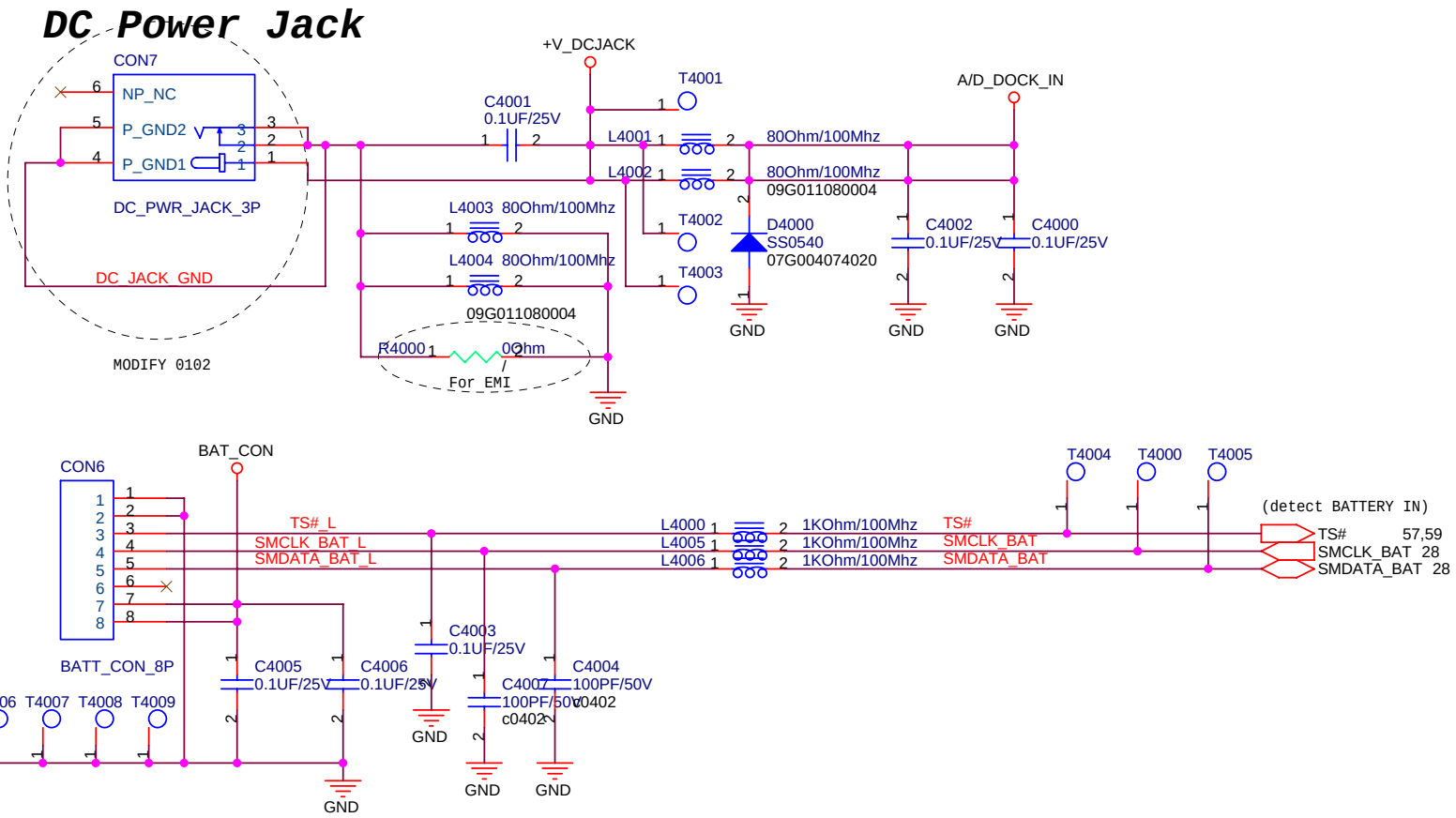
Size	Project Name	Rev
A3	A6F	1.1

Date: Monday, March 06, 2006 Sheet 37 of 63


CON26
MINI_PCI_124P
H: 6mm
TIP
RING
LAN_RESERV1
LAN_RESERV2
LAN_RESERV3
LAN_RESERV5
LAN_RESERV4
LAN_RESERV7
LAN_RESERV6
LAN_RESERV10
LAN_RESERV8
LAN_RESERV12
LAN_RESERV9
LAN_RESERV13
LAN_RESERV11
LAN_RESERV14
INTB#
5V_1
3.3V_7
INTA#
RESERVED9
RESERVED3
GROUND15
3.3VAUX1
CLK
RST#
GROUND4
3.3V_3
REQ#
GNT#
3.3V_4
GROUND7
AD[31]
PME#
AD[29]
RESERVED6
GROUND8
AD[30]
AD[27]
3.3V_5
AD[25]
AD[28]
RESERVED8
AD[26]
C/BE[3]#
AD[24]
AD[23]
IDSEL
GROUND11
GROUND9
AD[21]
AD[22]
AD[19]
AD[20]
GROUND13
PAR
AD[17]
AD[18]
C/BE[2]#
AD[16]
IRDY#
GROUND10
3.3V_8
FRAME#
CLKRUN#
TRDY#
SERR#
STOP#
GROUND14
3.3V_6
PERR#
DEVSEL#
C/BE[1]#
GROUND12
AD[14]
AD[15]
GROUND16
AD[13]
AD[12]
AD[11]
AD[10]
GROUND1
GROUND2
AD[09]
AD[08]
C/BE[0]#
AD[07]
3.3V_1
3.3V_2
AD[06]
AD[05]
AD[04]
RESERVED4
AD[02]
AD[03]
AD[00]
5V_2
RESERVED1
AD[01]
RESERVED2
GROUND6
GROUND3
AC_SYNC
M66EN
AC_SDATA_IN
AC_SDATA_OUT
AC_BIT_CLK
AC_CODEC_ID0#
AC_CODEC_ID1#
AC_RESET#
MOD_AUDIO_MON
RESERVED5
AUDIO_GND2
GROUND5
S_AUDIO_OUT
S_AUDIO_IN
S_AUDIO_OGND
S_AUDIO_I GND
AUDIO_GND1
AUDIO_GND
RESERVED7
MCPIACT#
VCC5A
3.3VAUX2
SIDE1
SIDE2
POST1
POST2
+3VS
GND
+5VS
+3V
18,30,33 PCI_AD[0..31]
17,25,28,41 LPC_AD0
17,25,28,41 LPC_AD2
37 802_LINKLED
MPCI_WL_N/F#
18,19 PCI_INTF#
C3801
10PF/50V
c0402
5 CLK_MINIPCI_D
18,19 PCI_REQ#
PCI_AD31
PCI_AD29
PCI_AD27
PCI_AD25
26 BT_DATA
18,30,33 PCI_C/BE#3
PCI_AD23
PCI_AD21
PCI_AD19
PCI_AD17
18,30,33 PCI_C/BE#2
18,19,30,33 PCI_IRDY#
19,30,33 PM_CLKRUN#
18,19,30,33 PCI_SERR#
18,19,30,33 PCI_PERR#
18,30,33 PCI_C/BE#1
PCI_AD14
PCI_AD12
PCI_AD10
PCI_AD8
PCI_AD7
PCI_AD5
PCI_AD3
PCI_AD1
LPC_AD1 17,25,28,41
LPC_AD3 17,25,28,41
802_ACTLED 37
LPC_FRAME# 17,25,28,41
PCI_INTE# 18,19
PCI_RST# 12,18,25,26,30,33
PCI_GNT#3 18
PCI_PME# 18,19,25,30,33
BT_CHCLK
PCI_AD30
PCI_AD28
PCI_AD26
PCI_AD24
IDSEL
PCI_AD19
R3801 33Ohm
PCI_AD22
PCI_AD20
PCI_PAR 18,30,33
PCI_AD18
PCI_AD16
PCI_FRAME# 18,19,30,33
PCI_TRDY# 18,19,30,33
PCI_STOP# 18,19,30,33
PCI_DEVSEL# 18,19,30,33
PCI_AD15
PCI_AD13
PCI_AD11
PCI_AD9
PCI_C/BE#0 18,30,33
PCI_AD6
PCI_AD4
PCI_AD2
PCI_AD0
INT_SERIRQ 19,25,28,30
R3800
10KOhm
r0402
MPCI_WL_N/F#
Q3800
2N7002
12,19,26 WLAN_ON#
C3802
10UF/10V
c0805_h57
C3803
0.1UF/10V
c0402
C3805
0.1UF/10V
c0402
C3806
c0402
0.01UF/16V
C3800
c0402
0.01UF/16V
C3808
c0402
0.01UF/16V
CE3800
100uF/6.3V
Title : MINIPCI (802.11)
ASUSTeK COMPUTER INC
Engineer: Jack Wang
Size A4
Project Name A6F
Rev 1.0
Date: Monday, March 06, 2006
Sheet 38 of 63



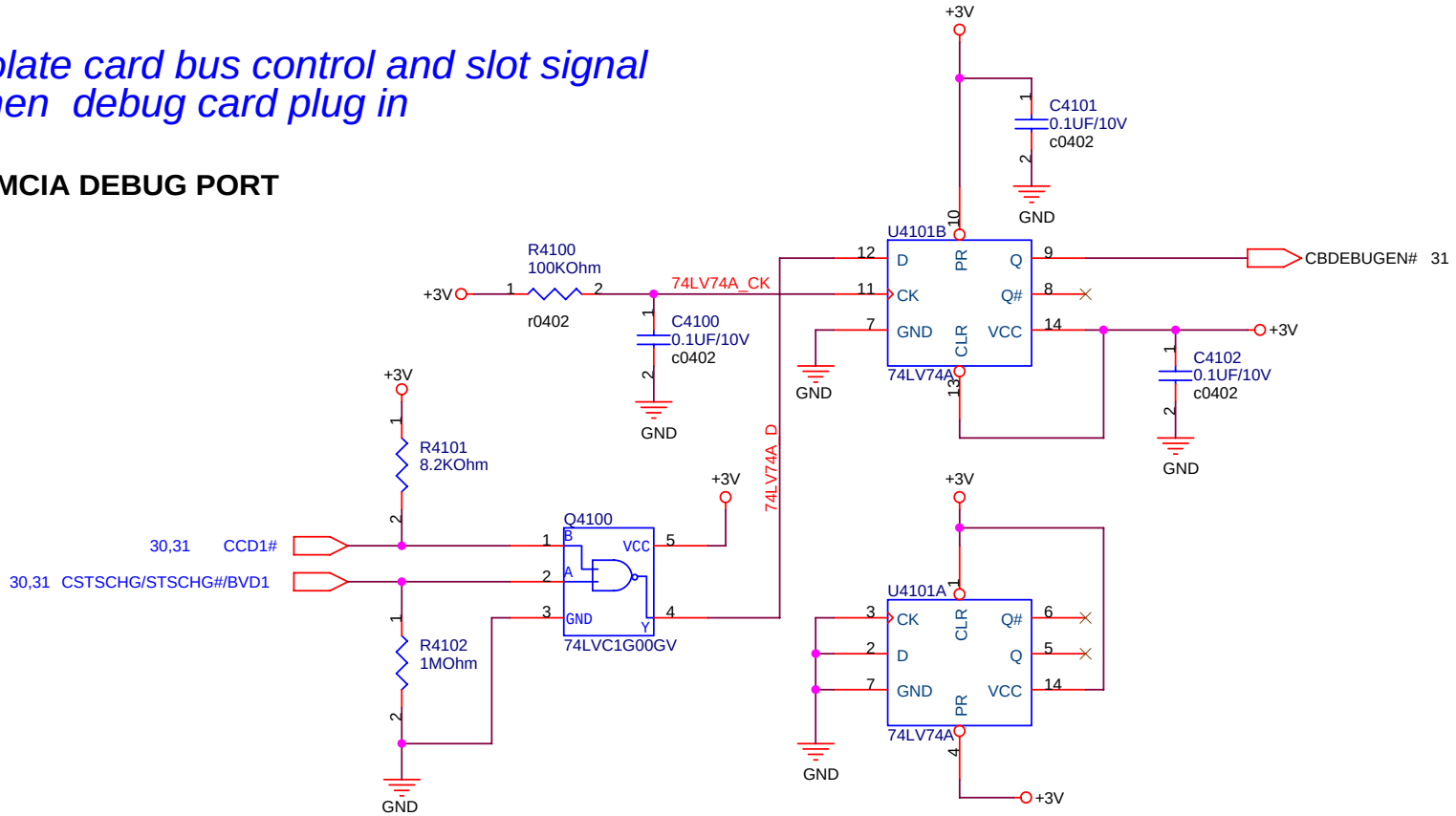
ASUSTeK COMPUTER INC	Title : POWER-ON SEQ.	
	Engineer: Jack Wang	
Size: A4	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 39 of 63	

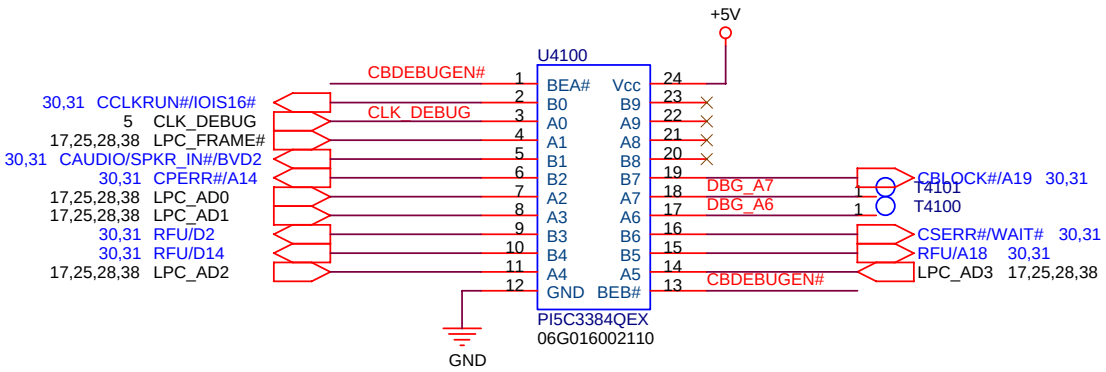


ASUSTeK COMPUTER INC	Title : DC/ BATT IN	
	Engineer: Jack Wang	
Size: A4	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 40 of 63	

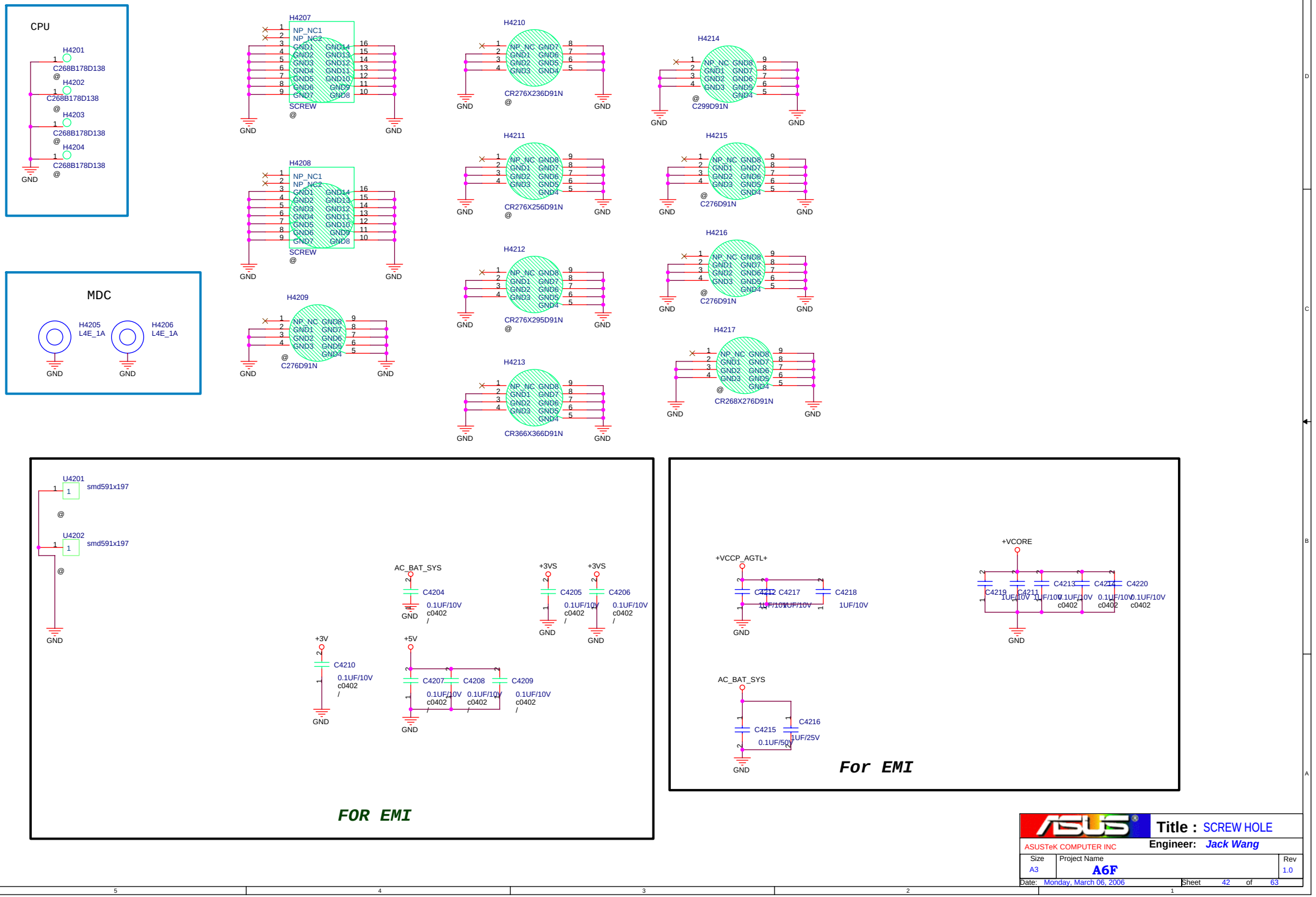
Isolate card bus control and slot signal when debug card plug in

PCMCIA DEBUG PORT





ASUSTeK COMPUTER INC	Title : PCMCIA Debug	
	Engineer: *Jack Wang*	
Size: A4	Project Name: **A6F**	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 41 of 63	



ASUSTeK COMPUTER INC	Title : SCREW HOLE		
	Engineer: Jack Wang		
Size: A3	Project Name: A6F		Rev: 1.0
Date: Monday, March 06, 2006	Sheet 42 of 63		

R1.1

11/14 1. Change resistor number from R1 to R1401

2. Change R1704 value from 10K to 330K

3. Add U2202 C D E F

4. Change C2511 value from 0.1uF to 0.047uF(11G232147316360)

5. Change C2510, C2514 and C2515 value from 0.1uF to 0.33uF(11G232333436030)

11/29 1. Remove R409

2. USB port (J3500) power control on shutdown of AC mode

3. Change U2202 power source form "+3VS" to "+3V" to solve pop noise

4. Add D2202 1N 4148W P/N 07G001001612 to solve pop noise when power off

5. Remove R2201 and mount R2203 to change Gain Setting

12/1 1. Change component D2103 DAP202K to 1N4148W P/N 07G001001612

2. Add Components 10K Ohm & 1N4148W P/N 07G001001612 and connect U2100 pin 30

3. Change J1500,U900,U2502,U3400,H4225,H4226,H4228,H4229,H4230 ,H4223,H4231,Q4400 to green part

12/2 1. Change Thermal Sensor to SO-8 MAX6657

2. USB4-->Camera, USB6-->PB

12/5 1.Change material CE1200, F3500, F3501, F3502

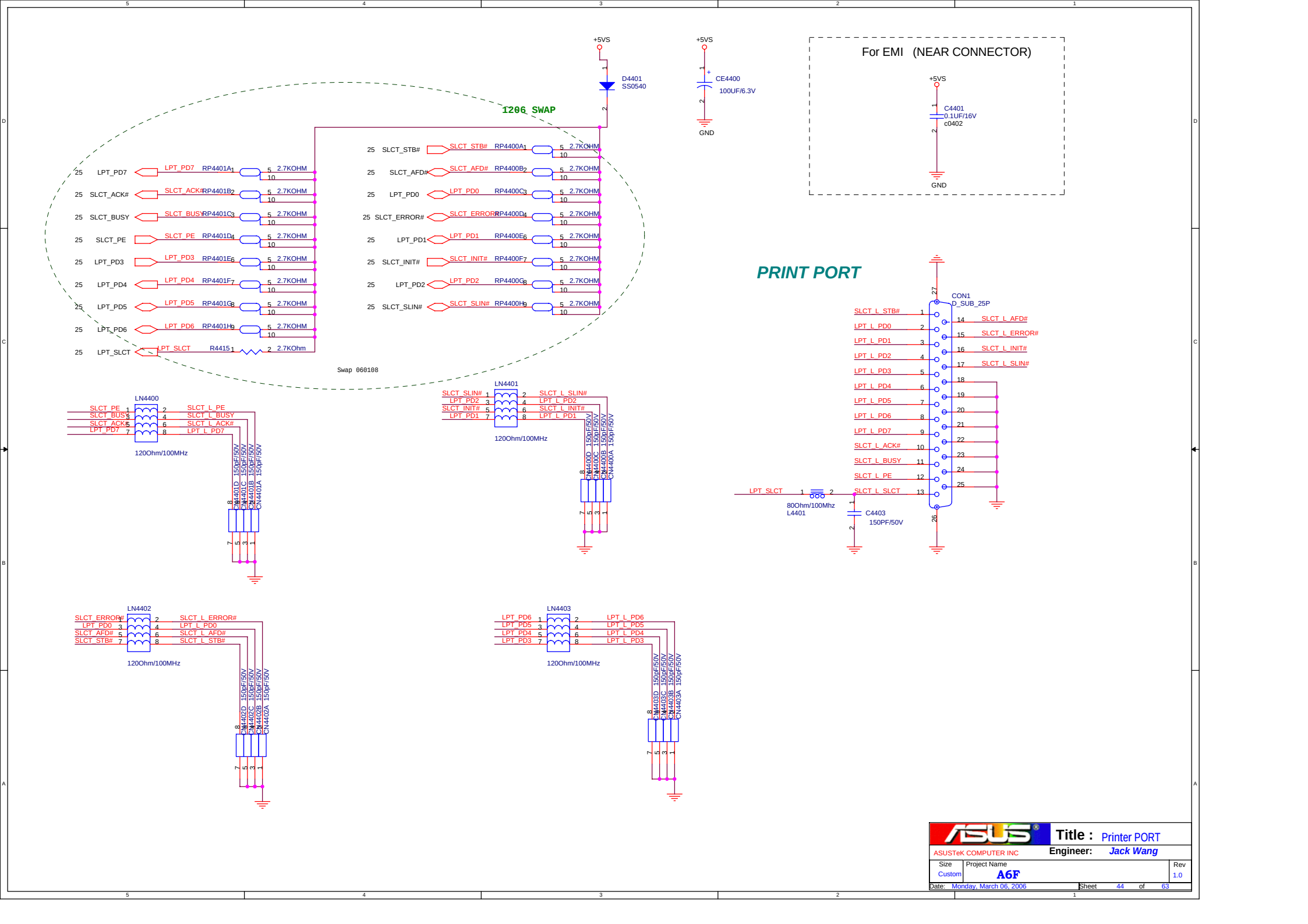
2. Add EC new function-->THRO_CPU

3. Change X3100, C3118, C3119 J3401 part number

12/7 1.Change J2500 footprint

12/9 1.Change R1202 value

ASUSTeK COMPUTER INC	Title : HISTORY	
	Engineer: Jack Wang	
Size: Custom	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 43 of 63	



ASUSTeK COMPUTER INC	Title : Printer PORT	
	Engineer: Jack Wang	
Size: Custom	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 44 of 63	

A3F --> A6F Change List

1.Page 35, USB Power change Ploy fuse to TPS2024

2. Page 44, delete Dockig add Printer Port

3. Page 22, add SPDIF on/off circuit

4. Page 14,15 2 DDR2 Socket --> single double side DDR2 socket

5. change connector part reference .

6. change CON23, CON24, CON21, CON13, CON14, CON9 Part Number.

7. change Q2211A,Q2211B part number

8. change bat1 part number .

9. page 33 , change L_RDP and L_RDN net name to connect correctly.

10. Remove the LED 3700.

11. Remove C2512, C2513.

12. Change all hole to A6.

13. ChangeX1700 X2800 Partnumber for height reason.

14. Change R2811,R2819 to RN2805C/D.

15. Change PCMCIA footprint.

15. Remove c3804 c3807 c2600 c2613 c2614 for space.

16. Remove CE300,CE302 for power side has Add.

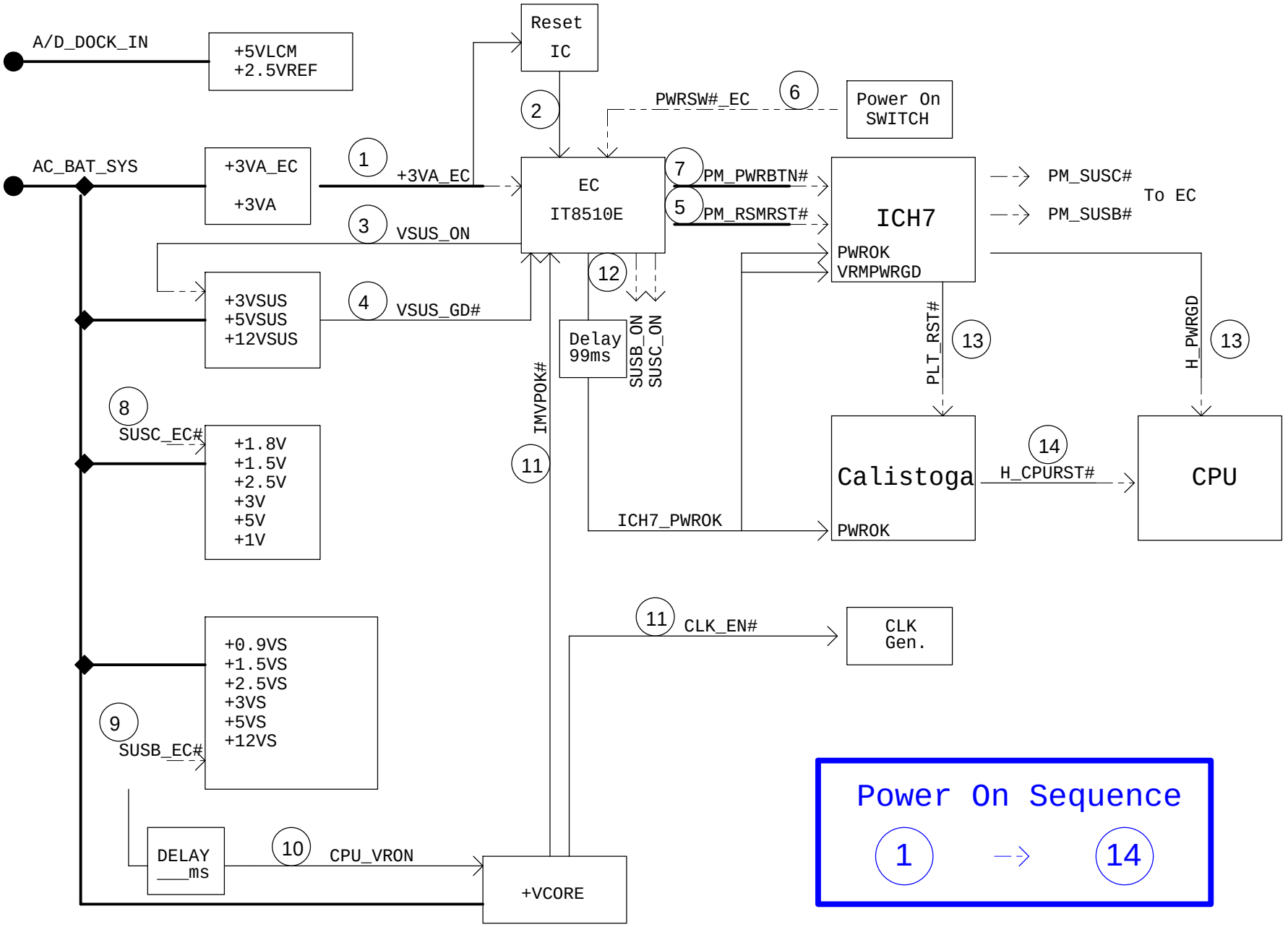
17. Remove Hole for VGA(South Bridge)

18. Add Chock on LAN connector.

19. change the R,C sequence at the connector of MDC and BAT.

20. change the LAN to 1000M LAN.Add PME to SouthBridge(Ref.A7T)

ASUSTeK COMPUTER INC	Title : Change List	
	Engineer: Jack Wang	
Size: A	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 45 of 63	



ASUSTeK COMPUTER INC	Title : FLOWCHART	
	Engineer: Jack Wang	
Size: Custom	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 46 of 63	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARD READER	AD17	1	D
CARDBUS	AD17	1	B
1394	AD17	1	C
MINIPCI (802.11a/b/g)	AD19	3	E,F

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

ICH7-M GPIO	A3F	Note	Volt
GPIO08	EXTSMI#		+3VSUS
GPIO09	SATA_DET#0		+3VSUS
GPIO12	KBCSCI#		+3VSUS
GPIO13	SIO_SMI#		+3VSUS
GPIO14	PWRLED_1Hz		+3VSUS
GPIO15	802_LED_EN#		+3VSUS
GPIO25	CB_SD#		+3VSUS
GPIO27	WLAN_ON#		+3VSUS
GPIO28	BT_ON		+3VSUS
GPIO36	BT_LED_EN#		+3VS
GPIO37	PCB_ID0		+3VS
GPIO38	PCB_ID1		+3VS
GPIO39	PCB_ID2		+3VS

ASUSTeK COMPUTER INC

Title : SYSTEM RESOURCE

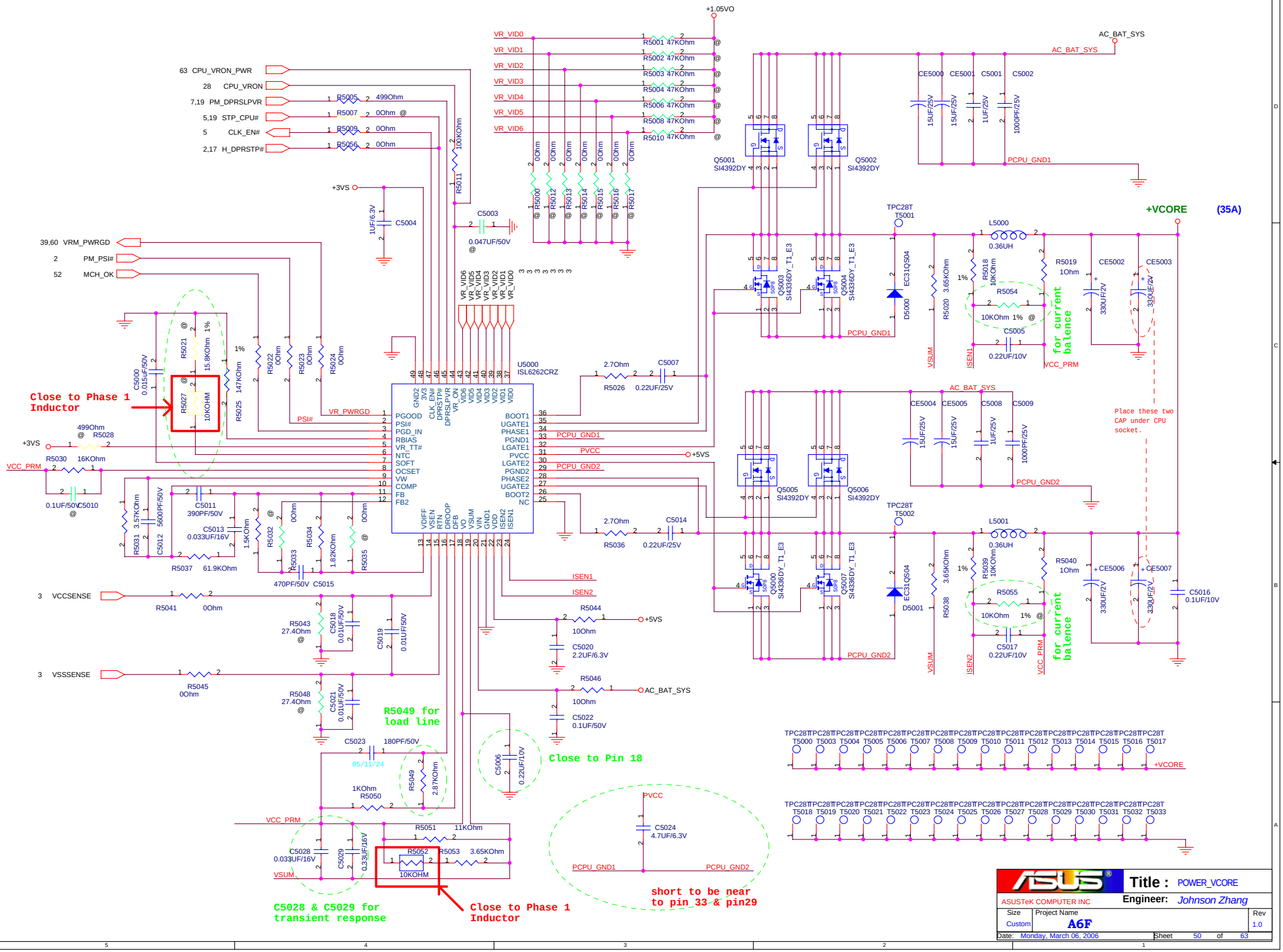
Engineer: Jack Wang

Size	Project Name	Rev
Custom	A6F	1.0

Date: Monday, March 06, 2006 Sheet 47 of 63

Title :	N/A
ASUSTeK COMPUTER INC	Engineer: Jack Wang
Size: Custom	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 48 of 63

ASUSTeK COMPUTER INC	Title : N/A	
	Engineer: Jack Wang	
Size: C	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 49 of 63	


+1.05VO
AC_BAT_SYS
+VCORE (35A)
63 CPU_VRON_PWR
28 CPU_VRON
7,19 PM_DPRSLPVR
5,19 STP_CPU#
5 CLK_EN#
2,17 H_DPRSTP#
39,60 VRM_PWRGD
2 PM_PSI#
52 MCH_OK
3 VCCSENSE
3 VSSSENSE
+3VS
VCC_PRM
VR_VID0
VR_VID1
VR_VID2
VR_VID3
VR_VID4
VR_VID5
VR_VID6
U5000
ISL6262CRZ
PGOOD
PSI#
PGD_IN
RBIAS
VR_TT#
NTC
SOFT
OCSET
VW
COMP
FB
FB2
BOOT1
UGATE1
PHASE1
PGND1
LGATE1
PVCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
NC
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
GND1
VDD
ISEN2
ISEN1
Q5001 SI4392DY
Q5002 SI4392DY
Q5003 SI4336DY_T1_E3
Q5004 SI4336DY_T1_E3
Q5005 SI4392DY
Q5006 SI4392DY
Q5000 SI4336DY_T1_E3
Q5007 SI4336DY_T1_E3
D5000 EC31QS04
D5001 EC31QS04
TPC28T T5001
TPC28T T5002
L5000 0.36UH
L5001 0.36UH
PCPU_GND1
PCPU_GND2
PVCC
+5VS
VSUM
ISEN1
ISEN2
VCC_PRM
Close to Phase 1 Inductor
Close to Phase 1 Inductor
Close to Pin 18
R5049 for load line
C5028 & C5029 for transient response
short to be near to pin 33 & pin29
Place these two CAP under CPU socket.
for current balence
for current balence
05/11/24
TPC28T T5000 T5003 T5004 T5005 T5006 T5007 T5008 T5009 T5010 T5011 T5012 T5013 T5014 T5015 T5016 T5017
TPC28T T5018 T5019 T5020 T5021 T5022 T5023 T5024 T5025 T5026 T5027 T5028 T5029 T5030 T5031 T5032 T5033
Title : POWER_VCORE
ASUSTeK COMPUTER INC
Engineer: Johnson Zhang
Size Custom
Project Name A6F
Rev 1.0
Date: Monday, March 06, 2006
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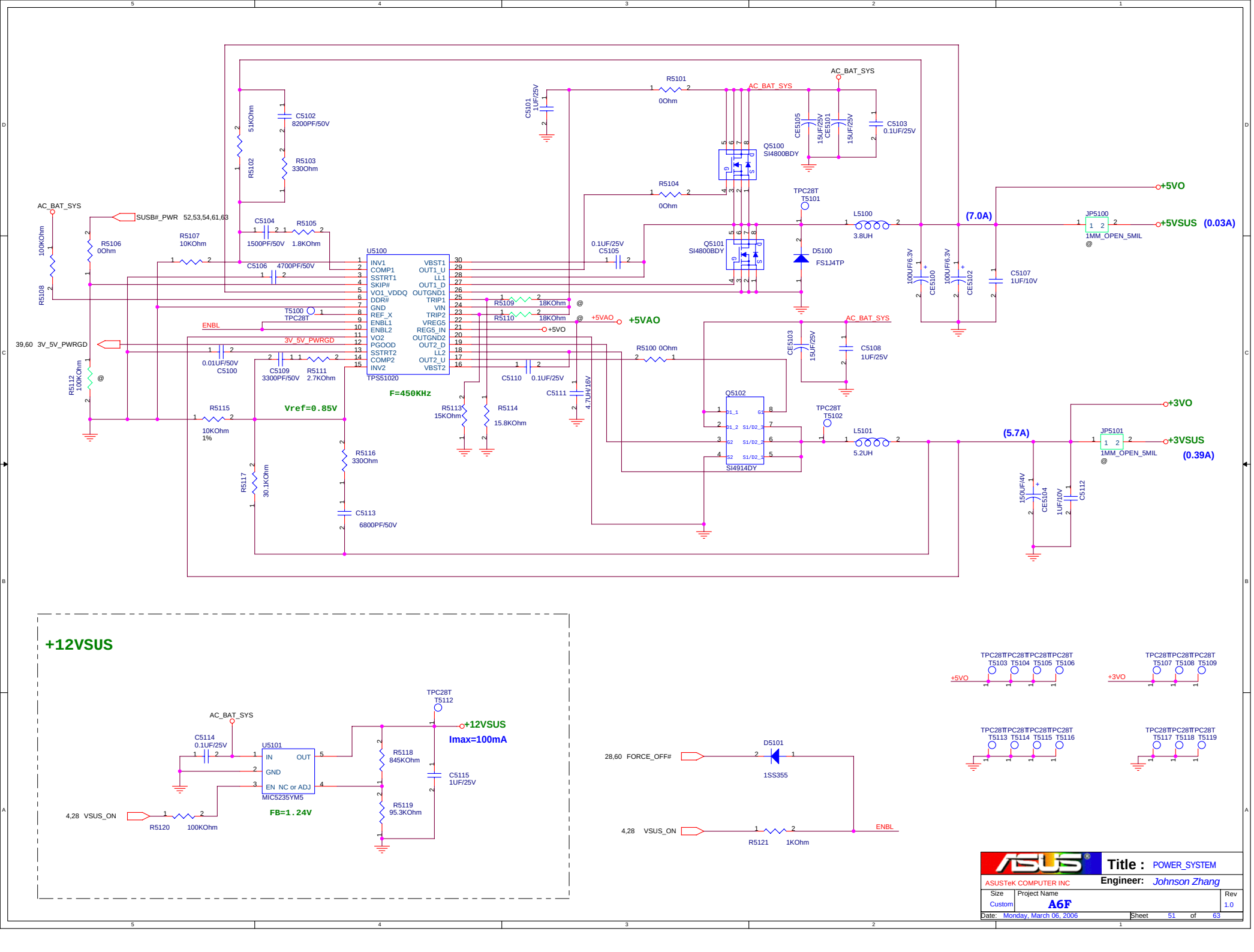
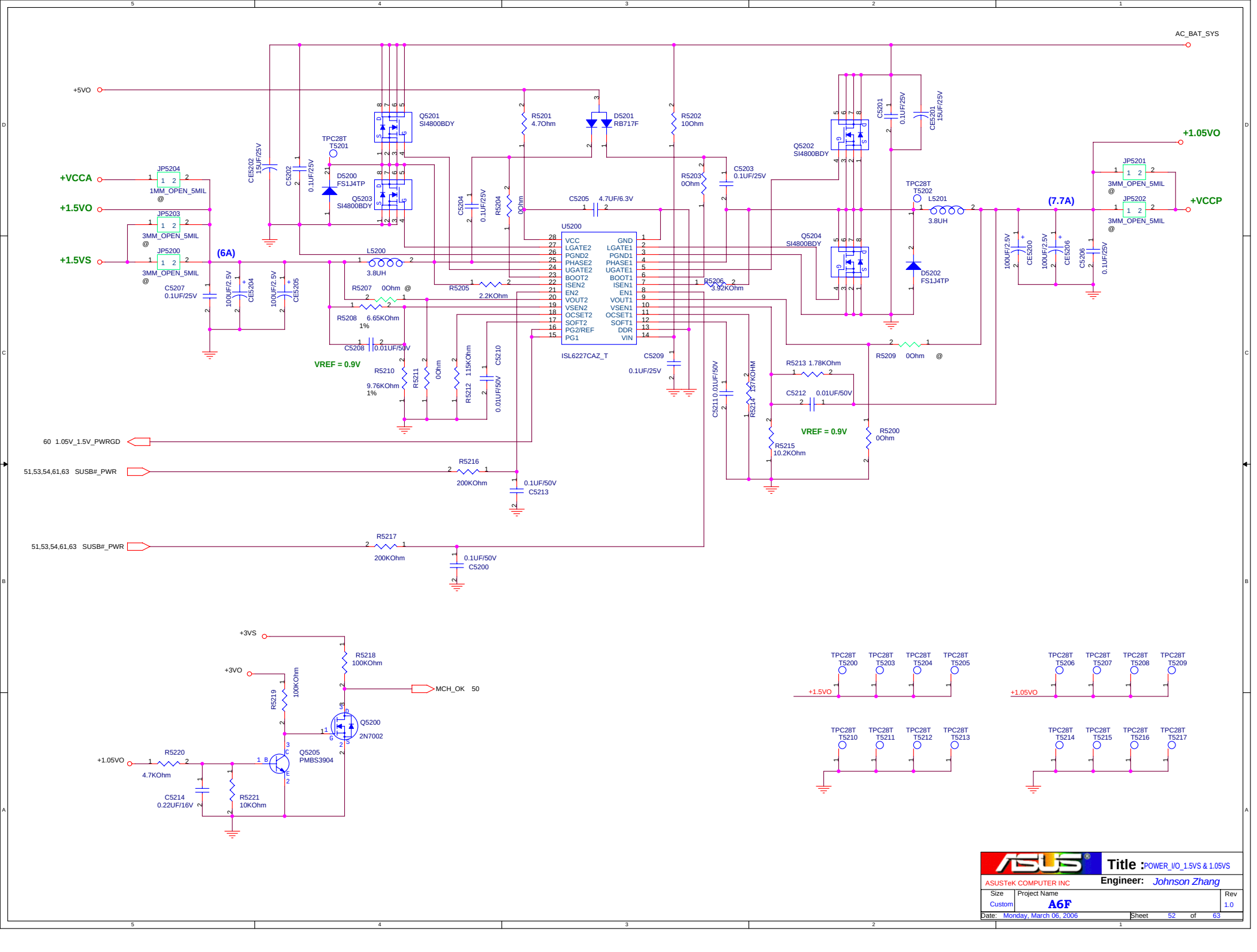
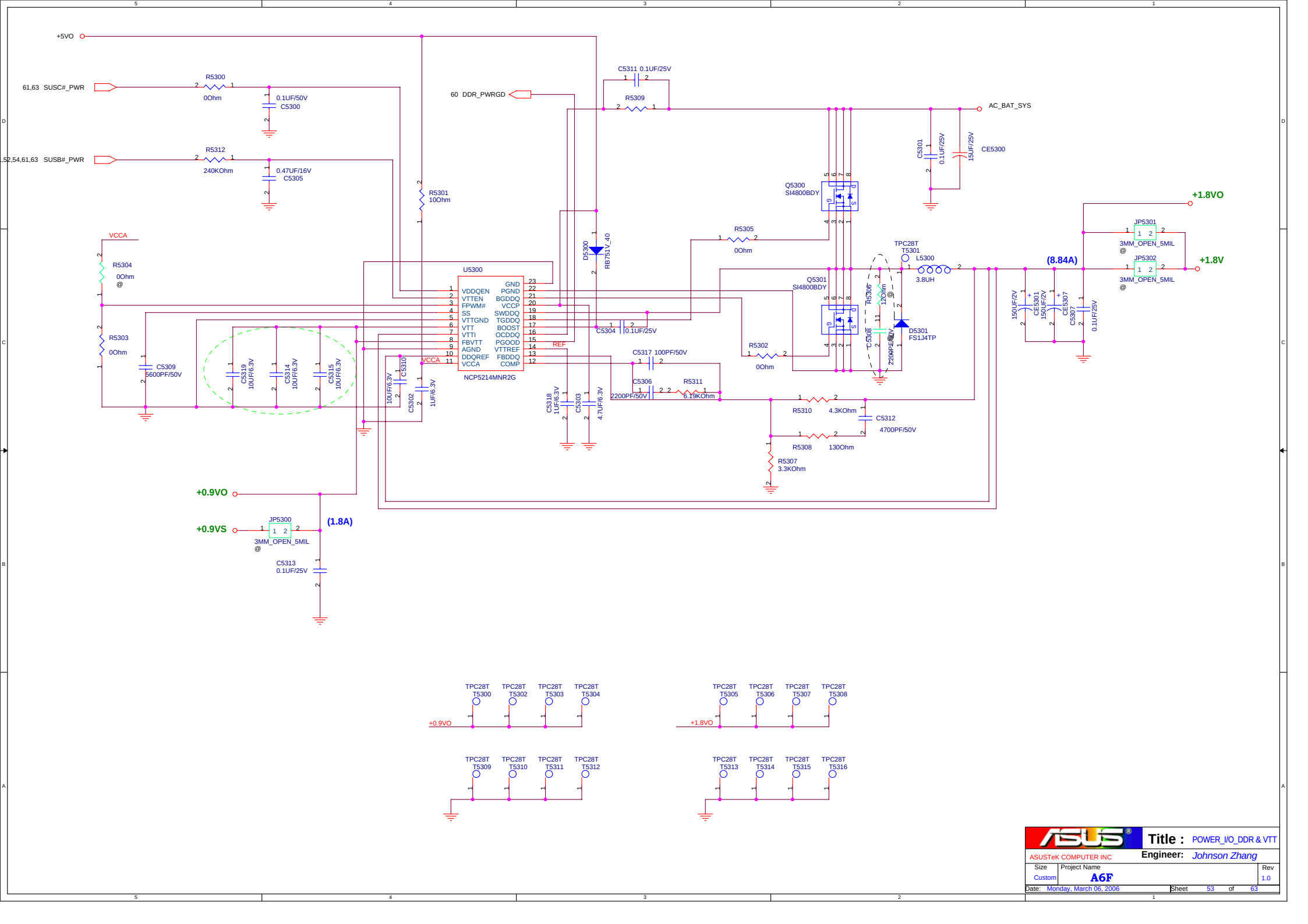


ASUSTeK COMPUTER INC	Title : POWER_SYSTEM		
	Engineer: Johnson Zhang		
Size: Custom	Project Name: A6F		Rev: 1.0
Date: Monday, March 06, 2006	Sheet 51 of 63		



ASUSTeK COMPUTER INC	Title : POWER_I/O_1.5VS & 1.05VS	
	Engineer: Johnson Zhang	
Size: Custom	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 52 of 63	



ASUSTeK COMPUTER INC	Title : POWER_I/O_DDR & VTT	
	Engineer: Johnson Zhang	
Size: Custom	Project Name: A6F	Rev: 1.0
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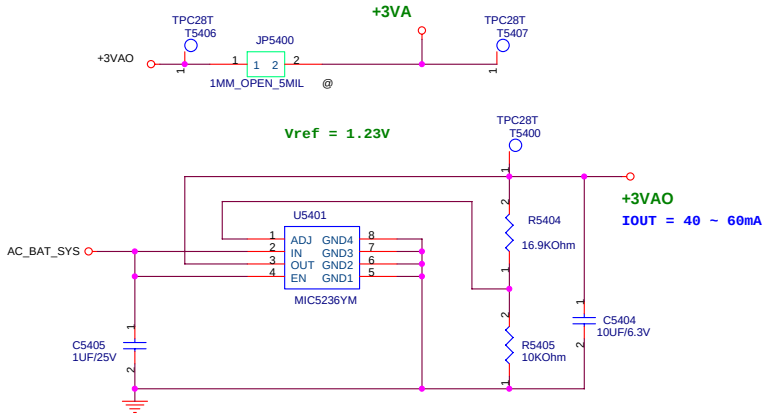
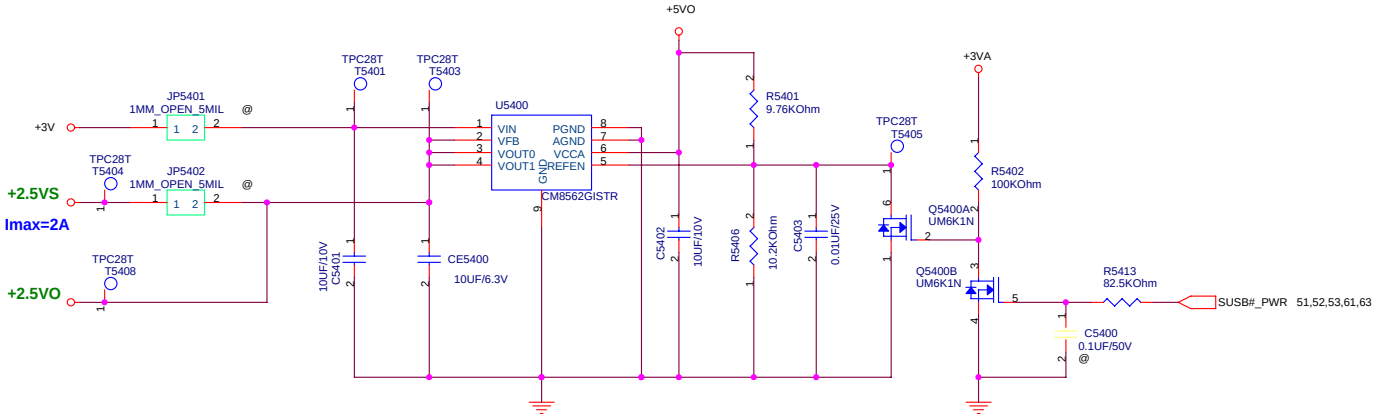
+3VA0



+2.5VS



ASUSTeK COMPUTER INC	Title : POWER_I/O_+3VA & +2.5VS	
	Engineer: Johnson Zhang	
Size: Custom	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 54 of 63	

Title : Dummy

Engineer: *Johnson Zhang*

ASUSTeK COMPUTER INC

Size	Project Name	Rev
C	**A6F**	1.0

Date: Monday, March 06, 2006 Sheet 55 of 63

Title : Dummy

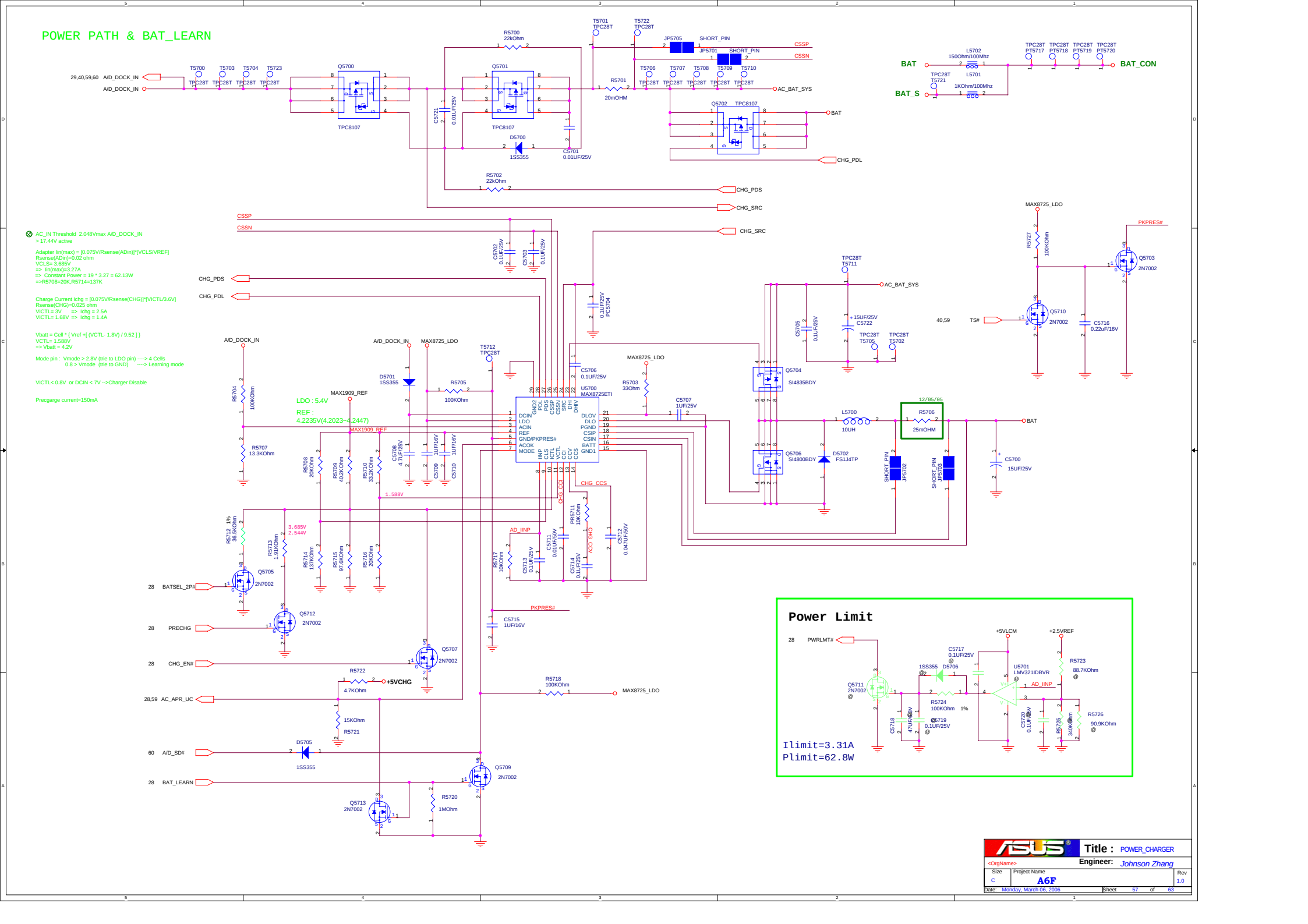
Engineer: Johnson Zhang

ASUSTeK COMPUTER INC

Size	Project Name	Rev
C	A6F	1.0

Date: Monday, March 06, 2006 Sheet 56 of 63

POWER PATH & BAT_LEARN



Title :	POWER_CHARGER
<OrgName>	Engineer: Johnson Zhang
Size: C	Project Name: A6F
Rev:	1.0
Date:	Monday, March 06, 2006
Sheet	57 of 63

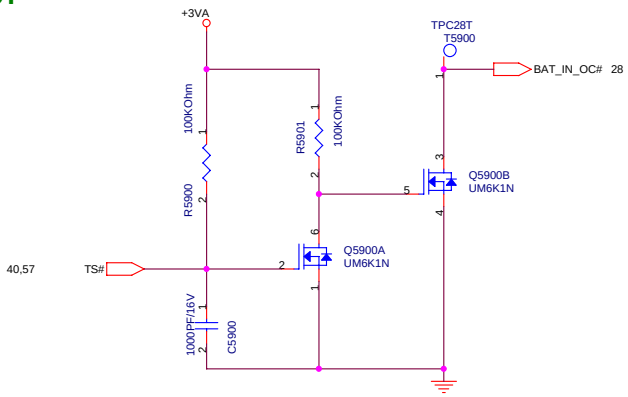
Title :	Dummy
Engineer:	Johnson Zhang

ASUSTeK COMPUTER INC

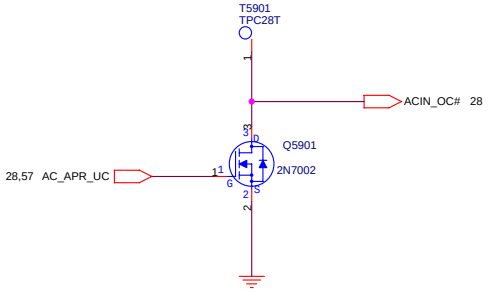
Size	Project Name	Rev
C	A6F	1.0

Date: Monday, March 06, 2006 Sheet 58 of 63

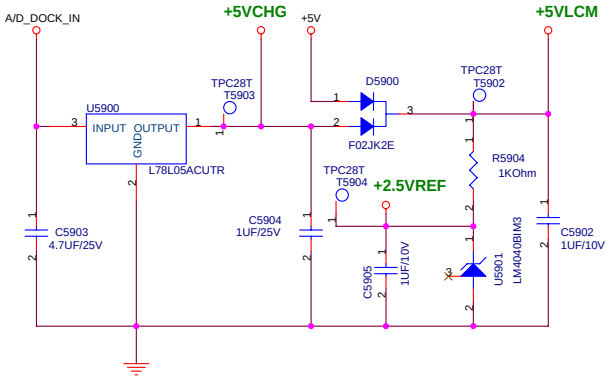
BATTERY IN DETECT



ADAPTER IN DETECT

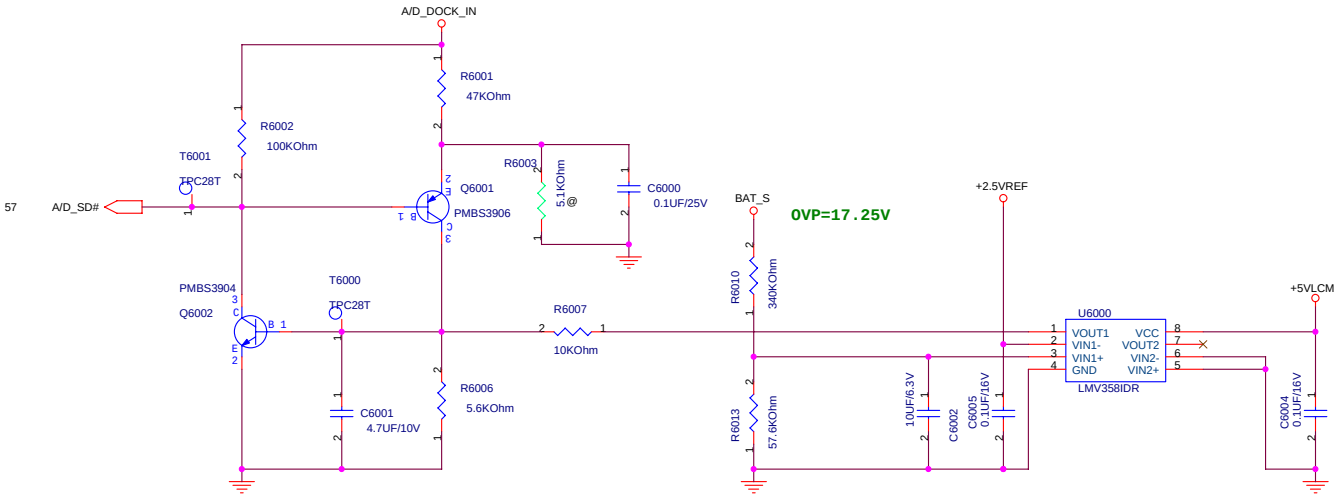


+5VLCM, +5VCHG & +2.5VREF

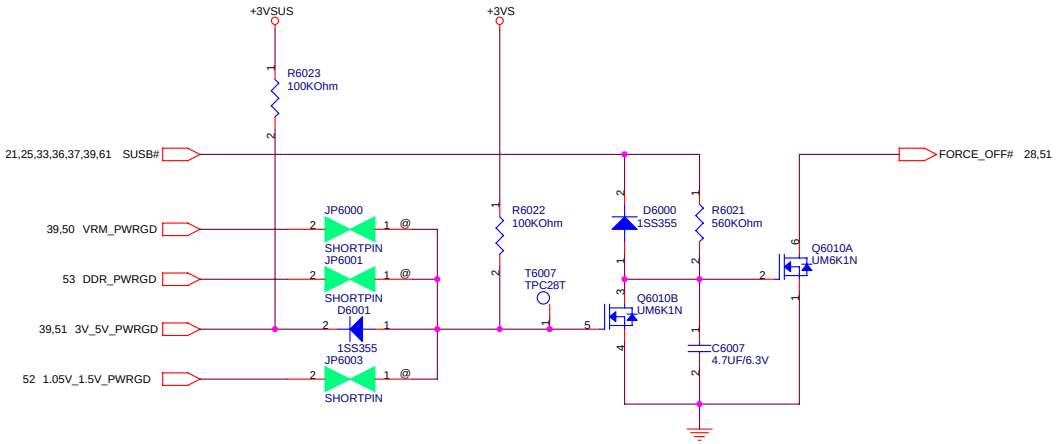


ASUSTeK COMPUTER INC	Title : POWER_DETECT	
	Engineer: Johnson Zhang	
Size: Custom	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 59 of 63	

BATTERY A/D_SD# (OVP)



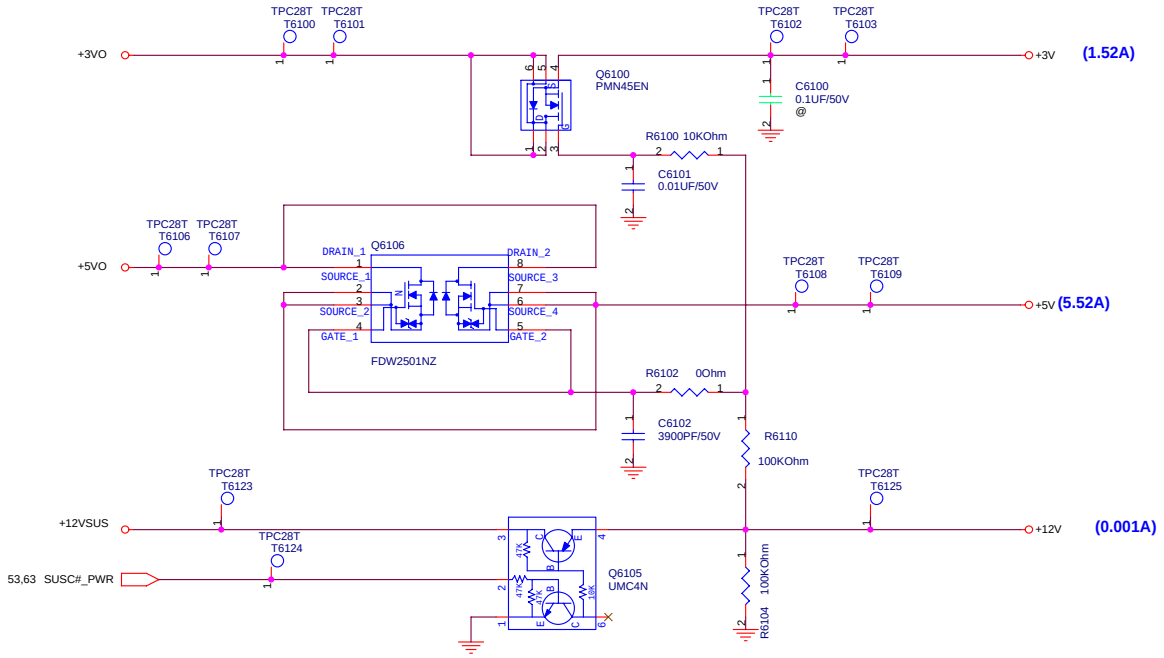
POWER GOOD DETECTER

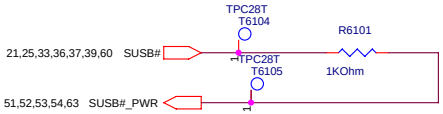


TPC28T T6003 1 — VRM_PWRGD
TPC28T T6004 1 — DDR_PWRGD
TPC28T T6005 1 — 3V_5V_PWRGD
TPC28T T6006 1 — 1.05V_1.5V_PWRGD

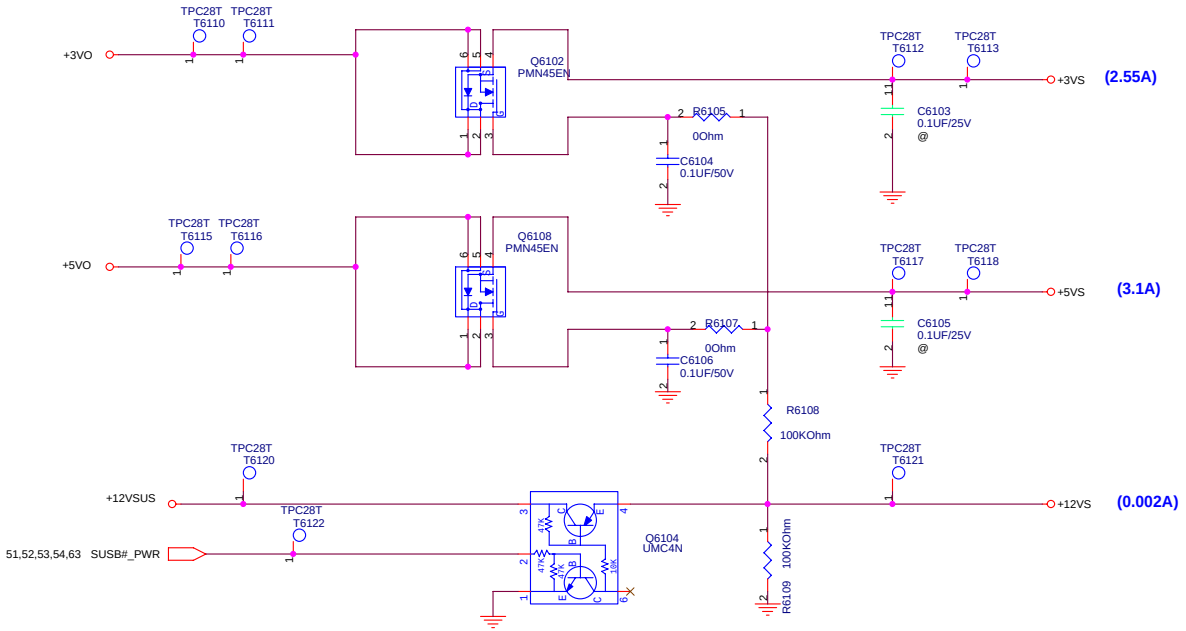
ASUSTeK COMPUTER INC	Title : POWER_PROTECT	
	Engineer: Johnson Zhang	
Size: Custom	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 60 of 63	

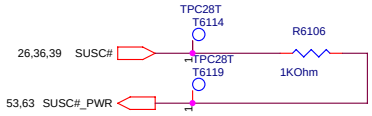
SUSC#_PWR POWER



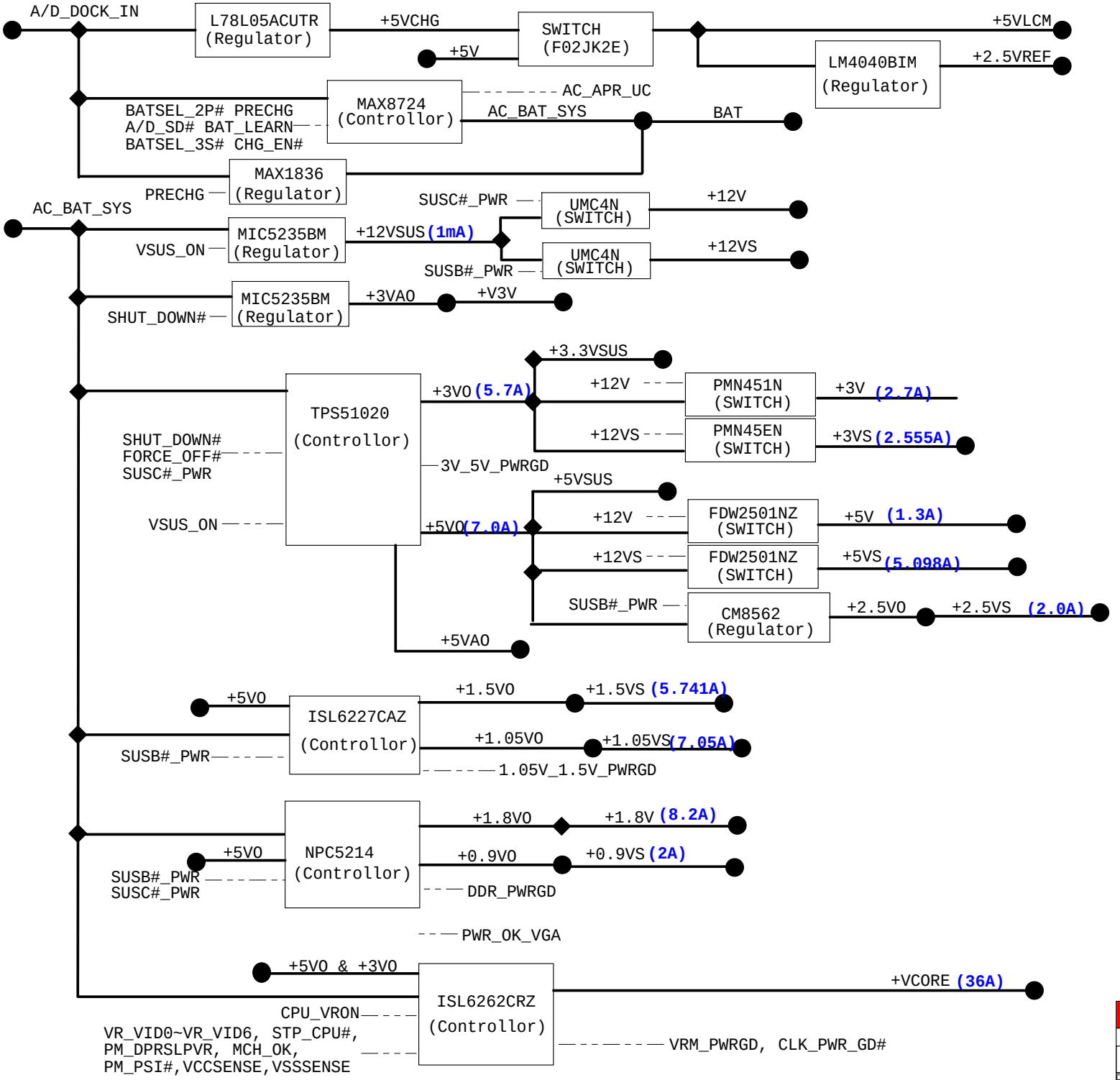


SUSB#_PWR POWER





ASUSTeK COMPUTER INC	Title : POWER_LOAD SWITCH	
	Engineer: Johnson Zhang	
Size: Custom	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 61 of 63	



ASUSTeK COMPUTER INC	Title : POWER_FLOWCHART	
	Engineer: Johnson Zhang	
Size: Custom	Project Name: A6F	Rev: 1.0
Date: Monday, March 06, 2006	Sheet 62 of 63	

AC_BAT_SYS → AC_BAT_SYS 12,50,51,52,53,54,57

+3VA → +3VA 4,12,20,28,37,39,54,59

+5VO → +5VO 35,51,52,53,54,61

+3VO → +3VO 51,52,61

+3VSUS → +3VSUS 18,19,20,28,33,34,37,39,51,60

+5VSUS → +5VSUS 20,36,37,51

+3V → +3V 12,18,22,26,30,31,32,34,35,36,38,41,54,61

+3VS → +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 4,32,36,61

+12VS → +12VS 12,22,36,61

+5V → +5V 9,12,22,31,35,36,37,41,59,61

+5VS → +5VS 4,13,19,20,21,22,27,28,36,37,38,44,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 9,13,36,54

+1.8VO → +1.8VO 53

+1.8V → +1.8V 7,10,14,15,36,53

+0.9VS → +0.9VS 16,36,53

BAT → BAT 29,57

+5VCHG → +5VCHG 57,59

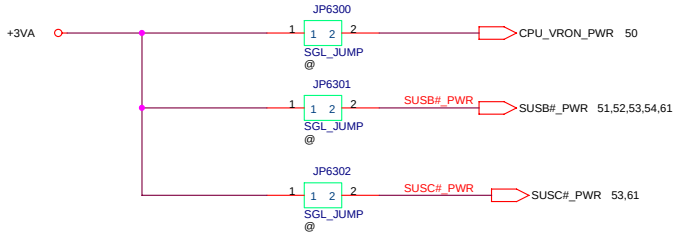
+5VLCM → +5VLCM 37,57,59,60

+2.5VREF → +2.5VREF 57,59,60

+VCORE → +VCORE 3,50

BAT_CON → BAT_CON 40,57

FOR POWER TEST



ASUSTeK COMPUTER INC	Title : POWER_SIGNAL		
	Engineer: Johnson Zhang		
Size: Custom	Project Name: A6F		Rev: 1.0
Date: Monday, March 06, 2006	Sheet 63 of 63		